



128K x 8 Static RAM

Features

- **High speed**
— $t_{AA} = 12$ ns
- **CMOS for optimum speed/power**
- **Low active power**
— 1020 mW
- **Low standby power**
— 250 mW
- **2.0V data retention (optional)**
— 100 μ W
- **Available in 450 x 550-mil LCC**
- **Automatic power-down when deselected**
- **Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options**

Functional Description

The CY7C1009 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

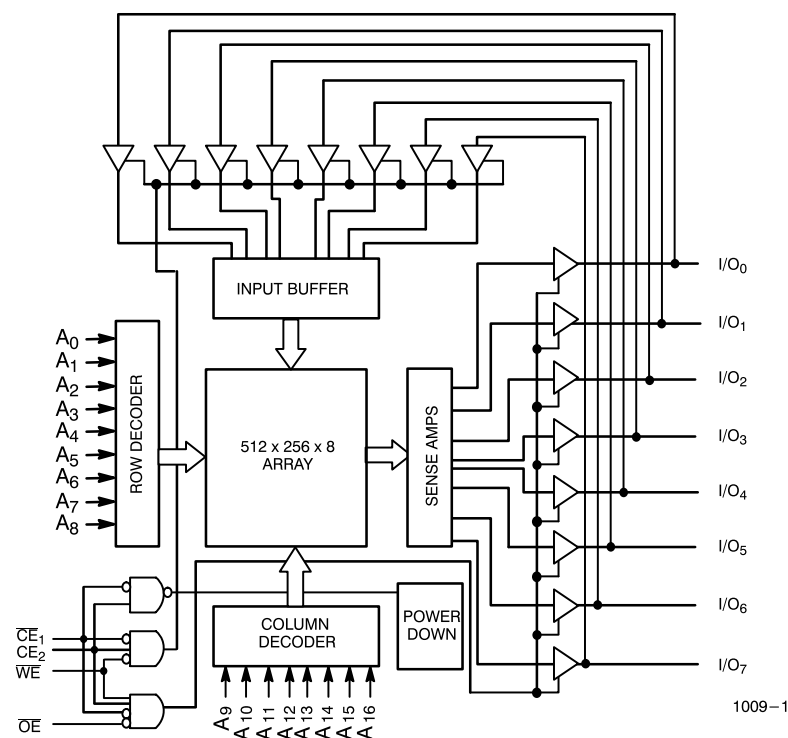
Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

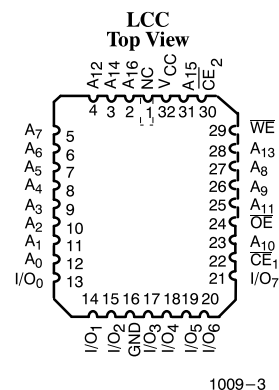
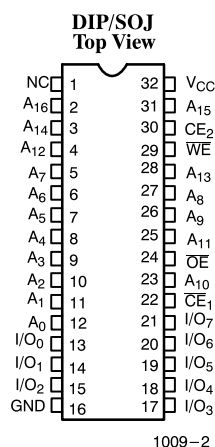
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C1009 is available in standard 300-mil-wide DIPs, SOJs and a small footprint 450 x 550-mil leadless chip carrier.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C1009-12	7C1009-15	7C1009-20	7C1009-25
Maximum Access Time (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	185	170	155	145
	Military		180	170	160
Maximum Standby Current (mA)	Commercial	45	40	30	30
	Military		40	30	30

Shaded area contains advanced information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -55°C to $+125^{\circ}\text{C}$
 Supply Voltage on V_{CC} to Relative GND^[1] .. -0.5V to $+7.0\text{V}$
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5\text{V}$
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1009-12		7C1009-15		7C1009-20		7C1009-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0\text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0\text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$, Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current ^[4]	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$		-300		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0\text{ mA}, f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Com'l	185		170		155		145	mA
			Mil			180		170		160	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC} , $\overline{\text{CE}}_1 \geq V_{IH}$ or $\text{CE}_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{\text{MAX}}$	Com'l	45		40		30		30	mA
			Mil			40		30		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC} , $\overline{\text{CE}}_1 \geq V_{CC} - 0.3\text{V}$, or $\text{CE}_2 \leq 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$, or $V_{IN} \leq 0.3\text{V}, f=0$	Com'l	10		10		10		10	mA
			L	2		2		2		2	
			Mil			10		10		10	
			L			2		2		2	

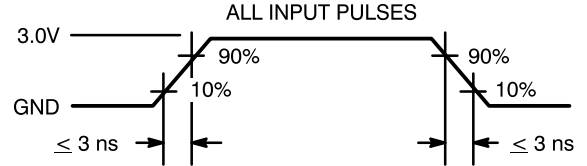
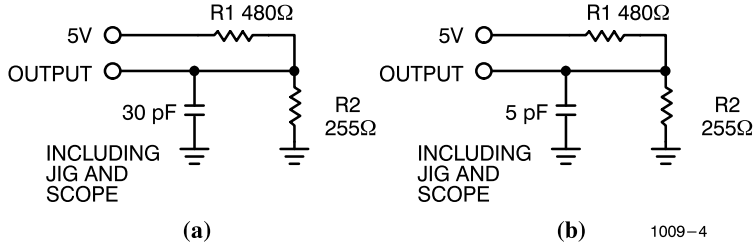
Shaded area contains advanced information.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN} : Address	Input Capacitance	$T_A = 25^{\circ}\text{C}, f = 1\text{ MHz}, V_{CC} = 5.0\text{V}$	7	pF
C_{IN} : Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

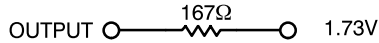
Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


1009-5

Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[3, 6]

Parameter	Description	7C1009–12		7C1009–15		7C1009–20		7C1009–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	12		15		20		25		ns
t _{AA}	Address to Data Valid		12		15		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	\overline{CE}_1 LOW to Data Valid, CE ₂ HIGH to Data Valid		12		15		20		25	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		7		8		10	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		6		7		8		10	ns
t _{LZCE}	\overline{CE}_1 LOW to Low Z, CE ₂ HIGH to Low Z ^[8]	3		3		3		3		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z, CE ₂ LOW to High Z ^[7, 8]		6		7		8		10	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up, CE ₂ HIGH to Power-Up	0		0		0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down, CE ₂ LOW to Power-Down		12		15		20		25	ns
WRITE CYCLE ^[9, 10]										
t _{WC}	Write Cycle Time	12		15		20		25		ns
t _{SCE}	\overline{CE}_1 LOW to Write End, CE ₂ HIGH to Write End	10		12		15		20		ns
t _{AW}	Address Set-Up to Write End	10		12		15		20		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		12		15		20		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		6		7		8		10	ns

Shaded area contains advanced information.

Notes:

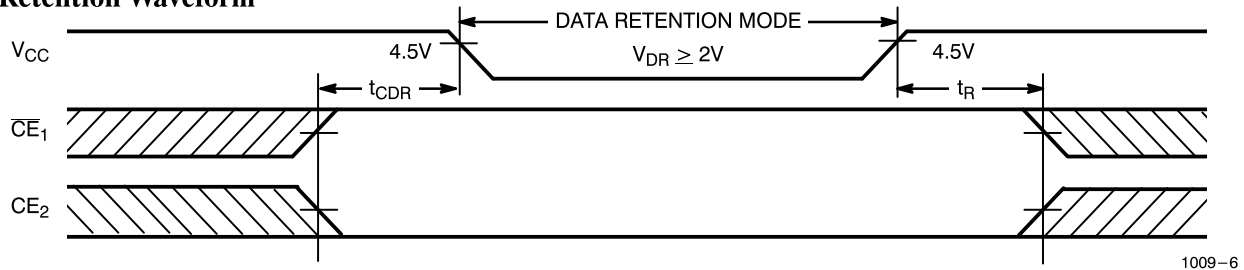
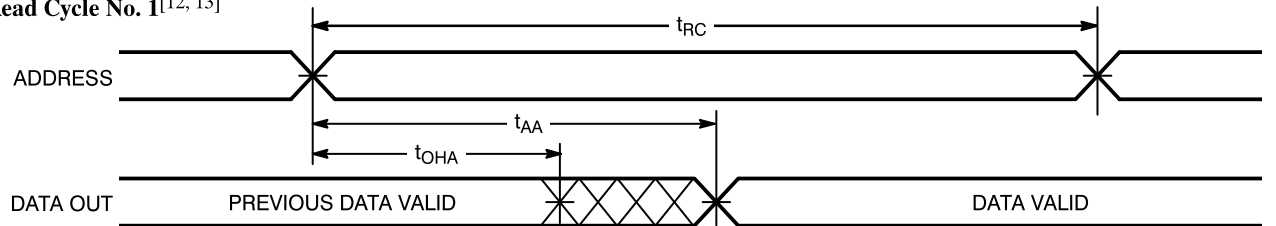
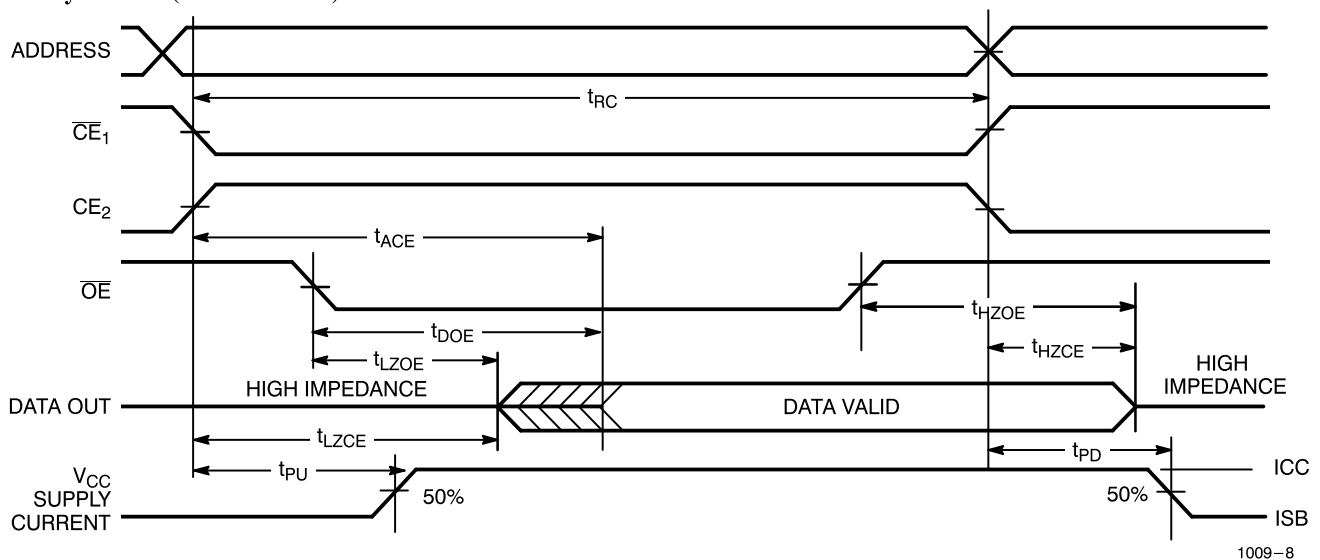
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions ^[11]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Data Retention		2.0		2.0		V
I _{CCDR}	Data Retention Current	V _{CC} = V _{DR} = 2.0V, CE ₁ ≥ V _{CC} - 0.3V or CE ₂ ≤ 0.3V,		50		70	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	0		0		ns
t _R ^[5]	Operation Recovery Time		t _{RC}		t _{RC}		ns

Note:

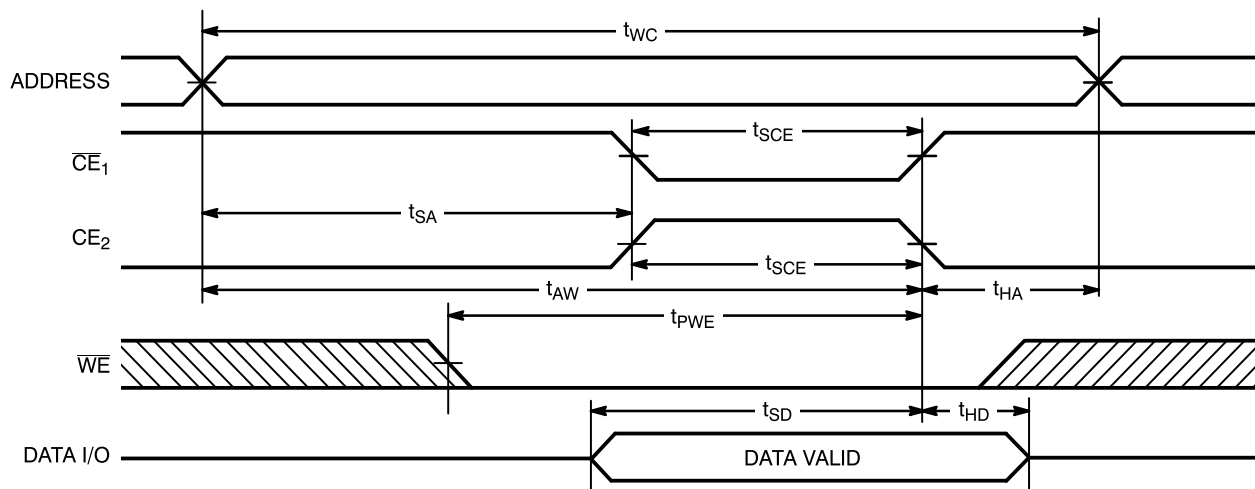
 11. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[12, 13]

Read Cycle No. 2 (OE Controlled)^[13, 14]

Notes:

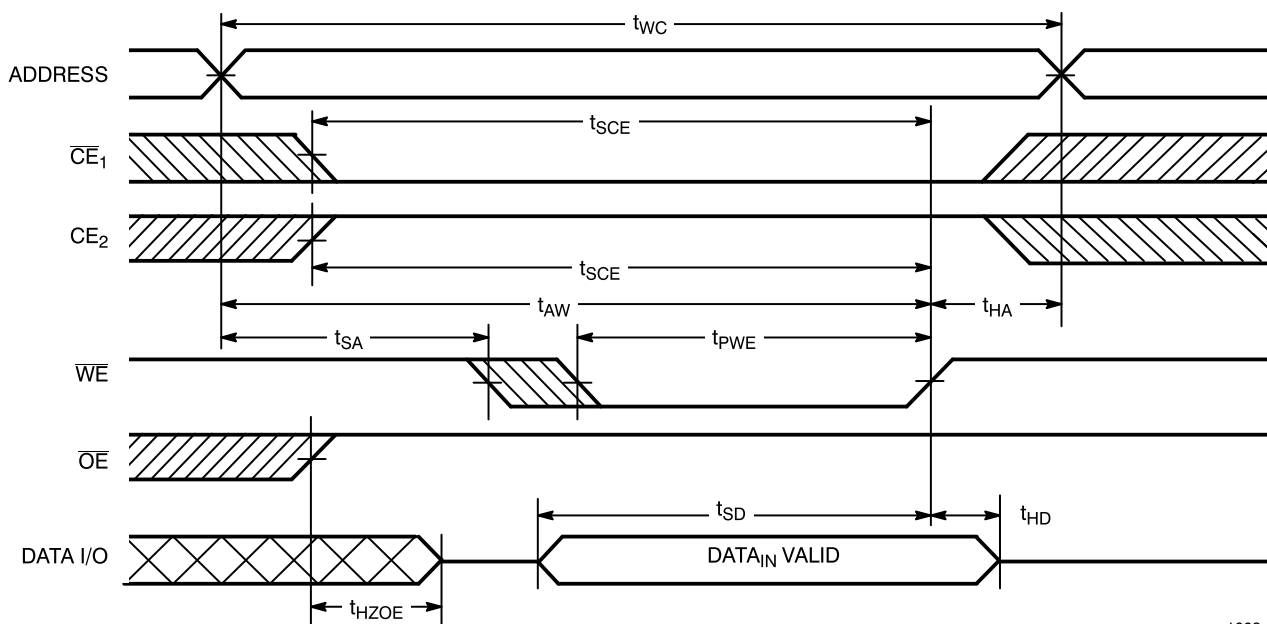
 12. Device is continuously selected. OE, CE₁ = V_{IL}, CE₂ = V_{IH}.

13. WE is HIGH for read cycle.

 14. Address valid prior to or coincident with CE₁ transition LOW and CE₂ transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled)^[15, 16]


1009-9

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[15, 16]


1009-10

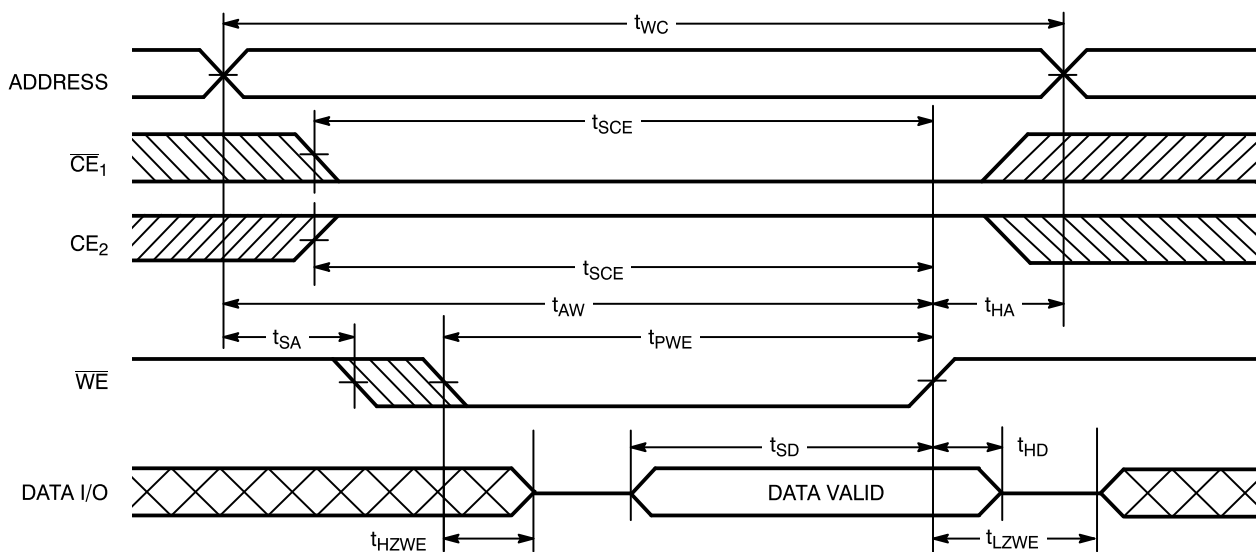
Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

16. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[10, 16]



1009-11

Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ - I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1009–12PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–12VC	V32	32-Lead (300-Mil) Molded SOJ	
15	CY7C1009–15PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–15VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–15DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C1009–20PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–20VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C1009–25PC	P31	32-Lead (300-Mil) Molded DIP	Commercial
	CY7C1009–25VC	V32	32-Lead (300-Mil) Molded SOJ	
	CY7C1009–25DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C1009–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.
Contact factory for “L” version availability.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

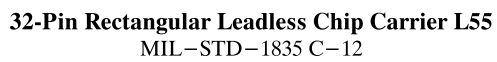
Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

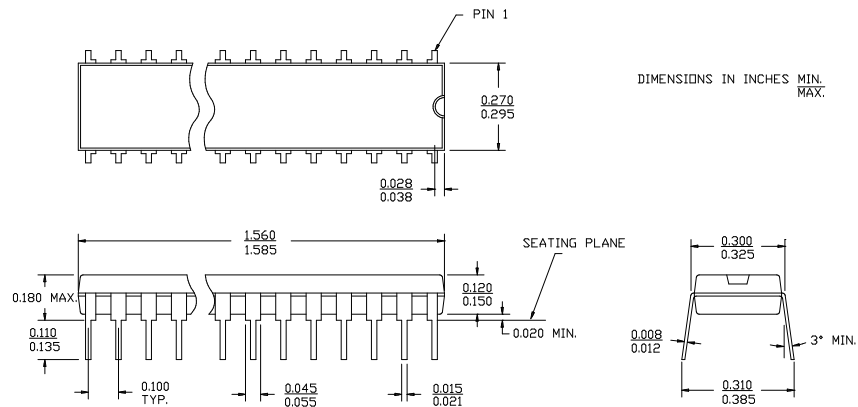
Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11



32-Lead (300-Mil) CerDIP D32



Package Diagrams (continued)
32-Lead (300-Mil) Molded DIP P31

32-Lead (300-Mil) Molded SOJ V32
