



## Intel™ 82430NX Chip Set Level II Cache Module Family

### Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74AP54) or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins
- Ideal for Intel P54C-based systems with the 82430NX (Neptune) chip set
- Operates at 60 and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

### Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chip set.

CYM74AP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74AP54 is organized as 32K by 64.

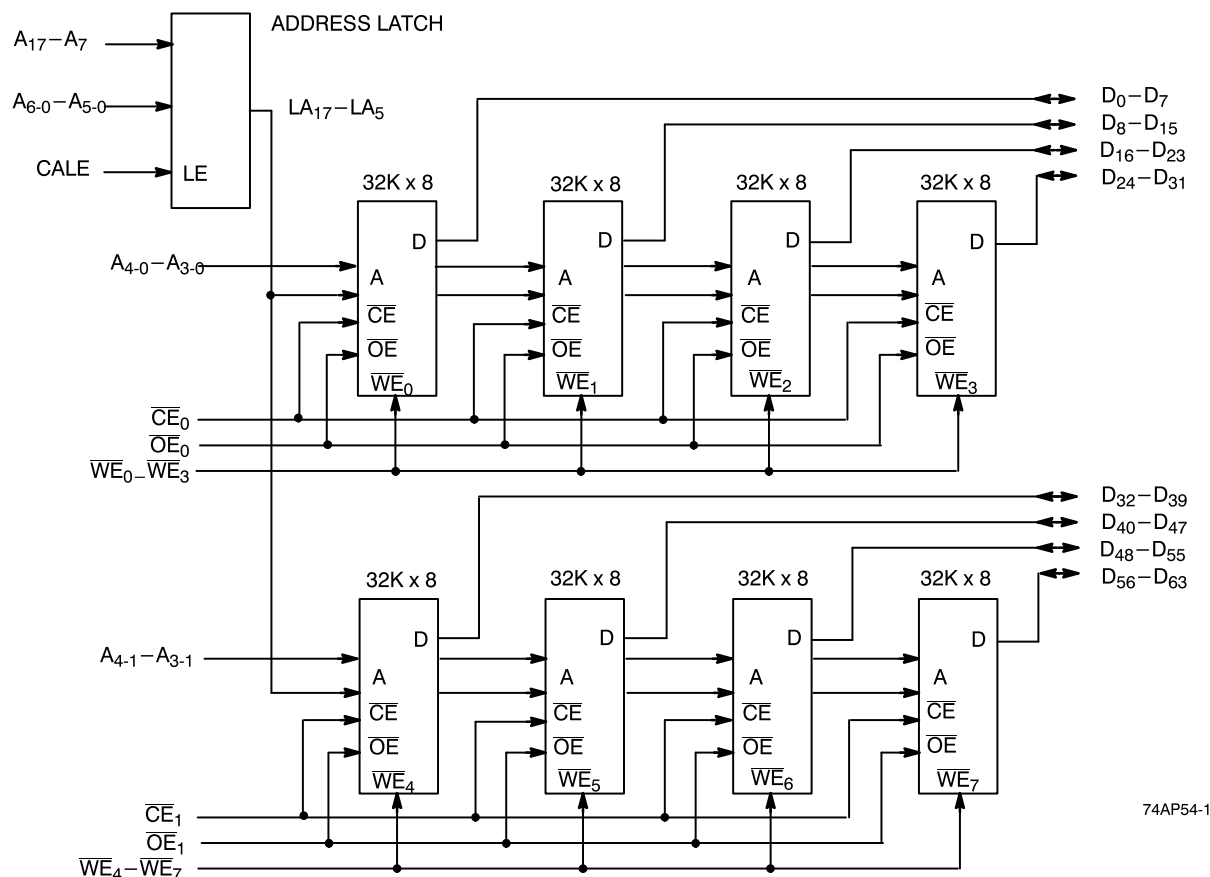
The CYM74SP54 and CYM74SP55 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity.

The CYM74SP55 is a 512-Kbyte cache module with byte parity.

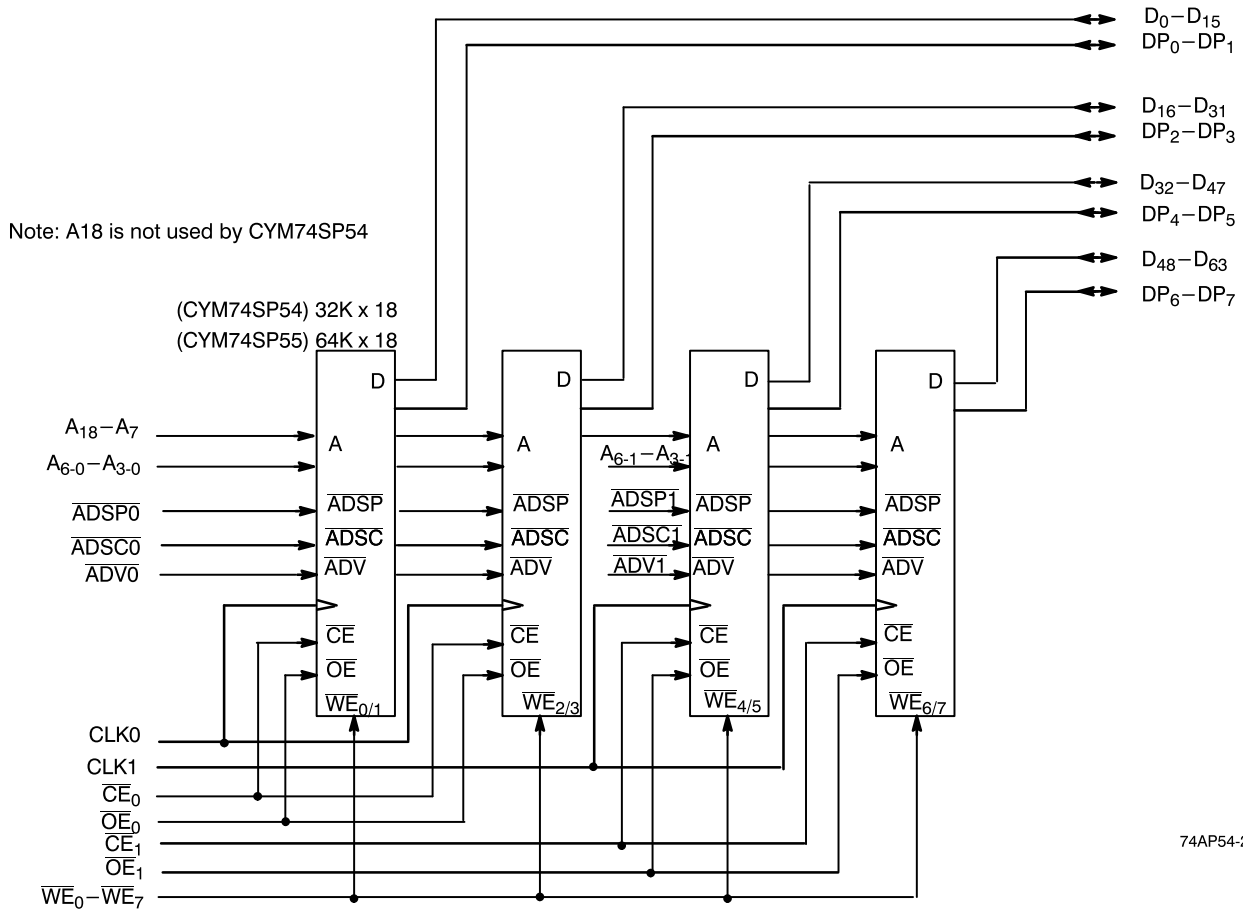
Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

**Logic Block Diagram – CYM74AP54**



Intel is a trademark of Intel Corporation.

**Logic Block Diagram – CYM74SP54/CYM74SP55**

**Selection Guide**

	<b>74AP54-60</b>	<b>74AP54-66</b>	<b>74SP54-60</b>	<b>74SP54-66</b>	<b>74SP55-60</b>	<b>74SP55-66</b>
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	$t_{AA}=15$ ns	$t_{AA}=12$ ns	$t_{CDV}=10.5$ ns	$t_{CDV}=8.5$ ns	$t_{CDV}=10.5$ ns	$t_{CDV}=8.5$ ns



## Pin Configuration

### Dual Read-Out SIMM (DIMM)

#### Top View

GND	81	1	GND
D <sub>63</sub>	82	2	D <sub>62</sub>
V <sub>CC</sub>	83	3	V <sub>CCQ</sub>
D <sub>61</sub>	84	4	D <sub>60</sub>
V <sub>CC</sub>	85	5	V <sub>CCQ</sub>
D <sub>59</sub>	86	6	D <sub>58</sub>
D <sub>57</sub>	87	7	D <sub>56</sub>
GND	88	8	GND
DP <sub>7</sub> (74SP5X) / NC (74AP54)	89	9	NC (74AP54) / DP <sub>6</sub> (74SP5X)
D <sub>55</sub>	90	10	D <sub>54</sub>
D <sub>53</sub>	91	11	D <sub>52</sub>
D <sub>51</sub>	92	12	D <sub>50</sub>
GND	93	13	GND
D <sub>49</sub>	94	14	D <sub>48</sub>
D <sub>47</sub>	95	15	D <sub>46</sub>
D <sub>45</sub>	96	16	D <sub>44</sub>
D <sub>43</sub>	97	17	D <sub>42</sub>
GND	98	18	GND
D <sub>41</sub>	99	19	D <sub>40</sub>
DP <sub>5</sub> (74SP5X) / NC (74AP54)	100	20	NC (74AP54) / DP <sub>4</sub> (74SP5X)
D <sub>39</sub>	101	21	D <sub>38</sub>
D <sub>37</sub>	102	22	D <sub>36</sub>
D <sub>35</sub>	103	23	D <sub>34</sub>
GND	104	24	GND
D <sub>33</sub>	105	25	D <sub>32</sub>
D <sub>31</sub>	106	26	D <sub>30</sub>
D <sub>29</sub>	107	27	D <sub>28</sub>
D <sub>27</sub>	108	28	D <sub>26</sub>
D <sub>25</sub>	109	29	D <sub>24</sub>
GND	110	30	GND
DP <sub>3</sub> (74SP5X) / NC (74AP54)	111	31	NC (74AP54) / DP <sub>2</sub> (74SP5X)
D <sub>23</sub>	112	32	D <sub>22</sub>
D <sub>21</sub>	113	33	D <sub>20</sub>
V <sub>CC</sub>	114	34	V <sub>CCQ</sub>
D <sub>19</sub>	115	35	D <sub>18</sub>
GND	116	36	GND
D <sub>17</sub>	117	37	D <sub>16</sub>
V <sub>CC</sub>	118	38	V <sub>CCQ</sub>
D <sub>15</sub>	119	39	D <sub>14</sub>
D <sub>13</sub>	120	40	D <sub>12</sub>
GND	121	41	GND
D <sub>11</sub>	122	42	D <sub>10</sub>
V <sub>CC</sub>	123	43	V <sub>CCQ</sub>
D <sub>9</sub>	124	44	D <sub>8</sub>
DP <sub>1</sub> (74SP5X) / NC (74AP54)	125	45	NC (74AP54) / DP <sub>0</sub> (74SP5X)
V <sub>CC</sub>	126	46	V <sub>CCQ</sub>
D <sub>7</sub>	127	47	D <sub>6</sub>
D <sub>5</sub>	128	48	D <sub>4</sub>
D <sub>3</sub>	129	49	D <sub>2</sub>
D <sub>1</sub>	130	50	D <sub>0</sub>
GND	131	51	GND
A <sub>3-1</sub>	132	52	A <sub>3-0</sub>
A <sub>4-1</sub>	133	53	A <sub>4-0</sub>
A <sub>5-1</sub>	134	54	A <sub>5-0</sub>
A <sub>6-1</sub>	135	55	A <sub>6-0</sub>
A <sub>7</sub>	136	56	A <sub>8</sub>
GND	137	57	GND
A <sub>9</sub>	138	58	A <sub>10</sub>
A <sub>11</sub>	139	59	A <sub>12</sub>
A <sub>13</sub>	140	60	A <sub>14</sub>
A <sub>15</sub>	141	61	A <sub>16</sub>
A <sub>17</sub>	142	62	A <sub>18</sub>
GND	143	63	GND
(Reserved A <sub>19</sub> ) NC	144	64	PD <sub>0</sub>
PD <sub>1</sub>	145	65	PD <sub>2</sub>
CLK <sub>0</sub> (74SP5X) / NC (74AP54)	146	66	NC (74AP54) / CLK <sub>1</sub> (74SP5X)
(Reserved CLK <sub>2</sub> ) NC	147	67	NC (Reserved CLK <sub>3</sub> )
GND	148	68	GND
WE <sub>7</sub>	149	69	WE <sub>6</sub>
WE <sub>5</sub>	150	70	WE <sub>4</sub>
WE <sub>3</sub>	151	71	WE <sub>2</sub>
WE <sub>1</sub>	152	72	WE <sub>0</sub>
GND	153	73	GND
ADSC <sub>1</sub> (74SP5X) / NC (74AP54)	154	74	CALE (74AP54) / ADSC <sub>0</sub> (74SP5X)
CE <sub>1</sub>	155	75	CE <sub>0</sub>
ADV <sub>1</sub> (74SP5X) / NC (74AP54)	156	76	NC (74AP54) / ADV <sub>0</sub> (74SP5X)
OE <sub>1</sub>	157	77	OE <sub>0</sub>
V <sub>CC</sub>	158	78	V <sub>CCQ</sub>
ADSP <sub>1</sub> (74SP5X) / NC (74AP54)	159	79	NC (74AP54) / ADSP <sub>0</sub> (74SP5X)
GND	160	80	GND

74AP54-3



*PRELIMINARY*

**CYM74AP54**  
**CYM74SP54**  
**CYM74SP55**

## Pin Definitions

Signal Name	Description
V <sub>CC</sub>	5V Supply
V <sub>CCQ</sub>	3.3V Supply
GND	Ground
A <sub>7</sub> –A <sub>19</sub>	Addresses from processor
A <sub>3</sub> – <sub>0</sub> , A <sub>4</sub> – <sub>0</sub> , A <sub>5</sub> – <sub>0</sub> , A <sub>6</sub> – <sub>0</sub>	Lower address from chip set, identical to the bank1 addresses
A <sub>3</sub> – <sub>1</sub> , A <sub>4</sub> – <sub>1</sub> , A <sub>5</sub> – <sub>1</sub> , A <sub>6</sub> – <sub>1</sub>	Lower address from chip set, identical to the bank0 addresses
$\overline{CE}_0$ , $\overline{CE}_1$	Chip Enable (same signal)
$\overline{OE}_0$ , $\overline{OE}_1$	Output Enable (same signal)
$\overline{WE}_0$ , $\overline{WE}_1$ , $\overline{WE}_2$ , $\overline{WE}_3$ , $\overline{WE}_4$ , $\overline{WE}_5$ , $\overline{WE}_6$ , $\overline{WE}_7$	Byte Write Enables
CALE	Latch Enable – CYM74AP54 only
PD <sub>0</sub> –PD <sub>2</sub>	Presence Detect pins
D <sub>0</sub> –D <sub>63</sub>	Data lines from processor
DP <sub>0</sub> –DP <sub>7</sub>	Data Parity lines (Optional), CYM74SP54 or CYM74SP55 only
$\overline{ASDP}_0$ , $\overline{ADSP}_1$	Processor Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADSC}_0$ , $\overline{ADSC}_1$	Cache Controller Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADV}_0$ , $\overline{ADV}_1$	Burst Address Advance – CYM74SP54 or CYM74SP55 only
CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , CLK <sub>3</sub>	Clock signals – CYM74SP54 or CYM74SP55 only, should be given own clk drivers
NC	Signal not connected on module.

## Presence Detect Pins

	PD <sub>2</sub>	PD <sub>1</sub>	PD <sub>0</sub>
Asynchronous – CYM74AP54	NC	GND	NC
Synchronous – CYM74SP54	GND	GND	NC
Synchronous – CYM74SP55	GND	GND	GND



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Ambient Temperature  
with Power Applied . . . . .  $-0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

3.3V Supply Voltage to Ground Potential . . . .  $-0.5\text{V}$  to  $+4.6\text{V}$

5V Supply Voltage to Ground Potential . . . .  $-0.5\text{V}$  to  $+5.25\text{V}$

DC Voltage Applied to Outputs  
in High Z State . . . . .  $-0.5\text{V}$  to  $+4.6\text{V}$

DC Input Voltage . . . . .  $-0.5\text{V}$  to  $+4.6\text{V}$

Output Current into Outputs (LOW) . . . . . 20 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$ $3.3\text{V} \pm 5\%$

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CCQ</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min. I <sub>OH</sub> = -4 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min. I <sub>OL</sub> = 8 mA		0.4	V
I <sub>CC</sub> (74AP54)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1500	mA
I <sub>CC</sub> (74SP54)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1500	mA
I <sub>CC</sub> (74SP55)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1500	mA

### Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74AP54PM-60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 15-ns Access RAMs	Commercial
	CYM74SP54PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
66	CYM74AP54PM-66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 12-ns Access RAMs	Commercial
	CYM74SP54PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	

Document #: 38-M-00070-A

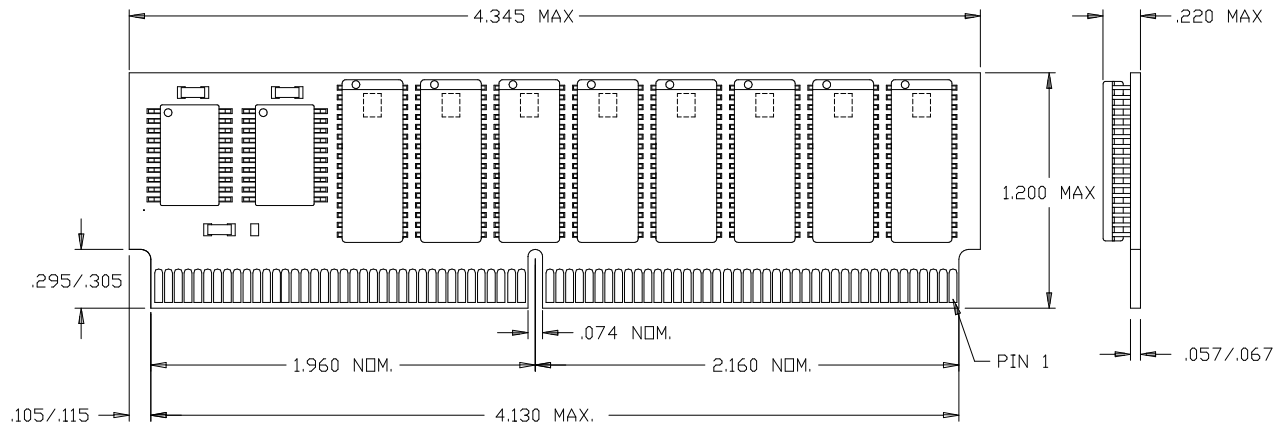


PRELIMINARY

CYM74AP54  
CYM74SP54  
CYM74SP55

## Package Diagrams

160-Pin Dual-Readout SIMM PM25



160-Pin Dual-Readout SIMM PM26

