



CY54/74FCT821T CY54/74FCT823T CY54/74FCT825T

8-/9-/10-Bit Bus Interface Registers

Features

- Function, pinout and drive compatible with FCT, F, and Am29821/23/25 logic
- FCT-C speed at 6.0 ns max. (Com'l)
FCT-B speed at 7.5 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 64 mA (Com'l),
32 mA (Mil)
- Source current 32 mA (Com'l),
12 mA (Mil)
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common clock enable (\overline{EN}) and asynchronous clear input (\overline{CLR})

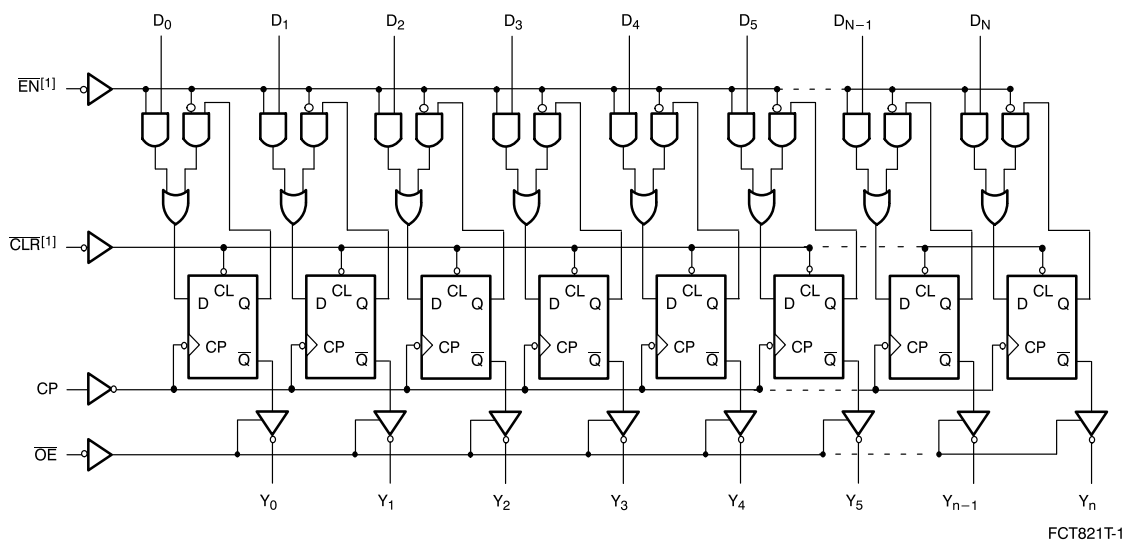
Functional Description

These bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T is a buffered, 10-bit wide version of the popular FCT374 function. The FCT823T is a 9-bit wide buffered register

with clock enable (\overline{EN}) and clear (\overline{CLR})—ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T is an 8-bit buffered register with all the FCT823T controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$) to allow multiuser control of the interface, e.g., \overline{CS} , DMA, and RD/\overline{WR} . They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

These devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



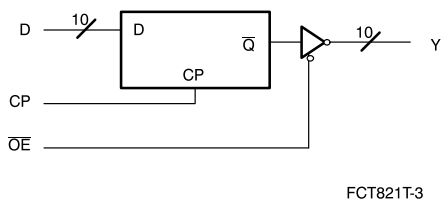
Note:

1. Not on FCT821.

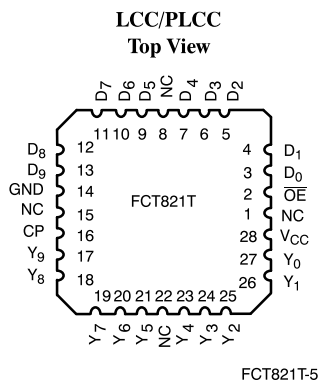
Logic Diagrams

Pin Configurations

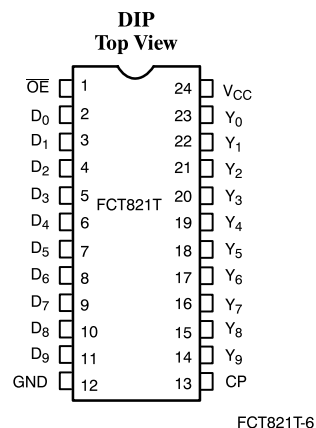
FCT821T (10-Bit Register)



FCT821T-3

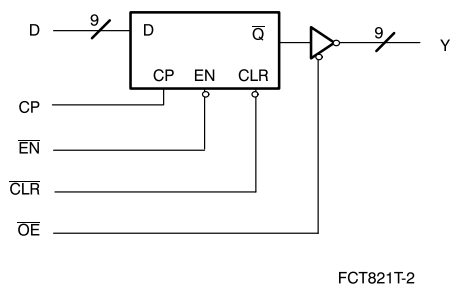


FCT821T-5

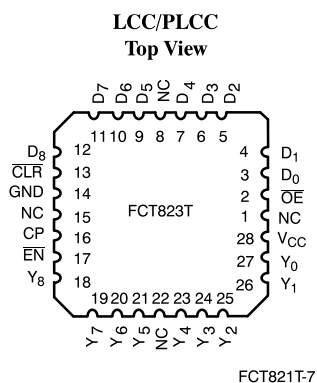


FCT821T-6

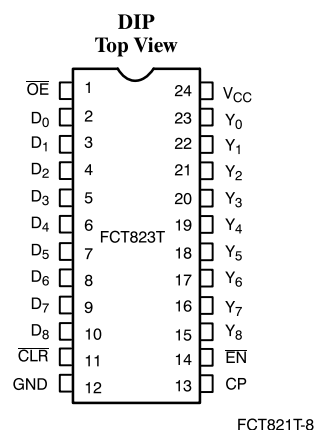
FCT823T (9-Bit Register)



FCT821T-2

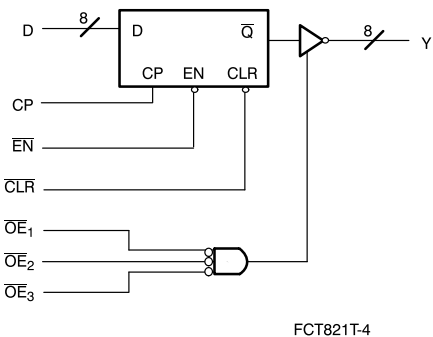


FCT821T-7

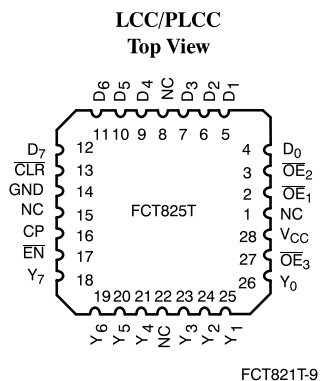


FCT821T-8

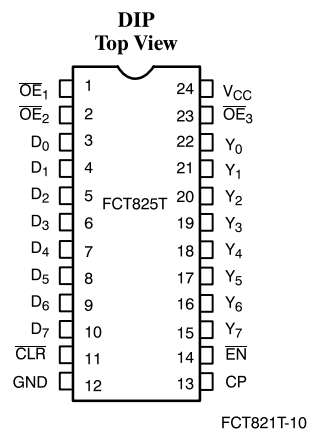
FCT825T (8-Bit Register)



FCT821T-4



FCT821T-9



FCT821T-10



Pin Description

Name	I/O	Description
D	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is LOW and $\overline{\text{OE}}$ is LOW, the Q outputs are LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y	O	The register three-state outputs.
$\overline{\text{EN}}$	I	Clock Enable. When $\overline{\text{EN}}$ is LOW, data on the D input is transferred to the Q output on the LOW-to-HIGH clock transition. When $\overline{\text{EN}}$ is HIGH, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When $\overline{\text{OE}}$ is HIGH, the Y outputs are in the high-impedance state. When $\overline{\text{OE}}$ is LOW, the TRUE register data is present at the Y outputs.

Function Table^[2]

Inputs					Internal Outputs		Function
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D	CP	Q	Y	
H H	H H	L L	L H	\downarrow \uparrow	L H	Z Z	High Z
H L	L L	X X	X X	X X	L L	Z L	Clear
H L	H H	H H	X X	X X	NC NC	Z NC	Hold
H H L L	H H H H	L L L L	L H L H	\downarrow \downarrow \downarrow \downarrow	L H L H	Z Z L H	Load

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
Ambient Temperature with
Power Applied -65°C to $+135^{\circ}\text{C}$
Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
DC Input Voltage -0.5V to $+7.0\text{V}$
DC Output Voltage -0.5V to $+7.0\text{V}$
DC Output Current (Maximum Sink Current/Pin) 120 mA
Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	AT, BT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[5]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Notes:

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, \downarrow = LOW-to-HIGH Transition, Z = HIGH Impedance.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[6]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =−32 mA	Com'l	2.0			V
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =−15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =−12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[7]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =−18 mA			−0.7	−1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				−10	μA
I _{OS}	Output Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} =0.0V		−60	−120	−225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[7]

Parameter	Description	Typ. ^[6]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

6. Typical values are at V_{CC}=5.0V, T_A= +25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order

to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$, ^[9] $f_1 = 0$, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}$, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	1.2	3.4	mA
		$V_{CC} = \text{Max.}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	1.6	3.2 ^[12]	mA
		$V_{CC} = \text{Max.}$, $f_0 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5 \text{ MHz}$, $\overline{OE} = \overline{EN} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	3.9	12.2 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

11. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL HIGH input}$
 $(V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL inputs HIGH}$

$N_T = \text{Number of TTL inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an input transition pair (HLH or LHL)}$

$f_0 = \text{Clock frequency for registered devices, otherwise zero}$

$f_1 = \text{Input signal frequency}$

$N_1 = \text{Number of inputs changing at } f_1$

All currents are in milliamps and all frequencies are in megahertz.

12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range

Param.	Description	Test Load	FCT821AT/FCT823AT/ FCT825AT				FCT821BT/FCT823BT/ FCT825BT				Unit	Fig. No. ^[14]
			Military		Commercial		Military		Commercial			
			Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW)	C _L =50 pF R _L =500Ω		11.5		10.0		8.5		7.5	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW) ^[7]	C _L =300 pF R _L =500Ω		20.0		20.0		16.0		15.0	ns	1, 5
t _{PLH}	Propagation Delay CLR to Y	C _L =50 pF R _L =500Ω		15.0		14.0		9.5		9.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C _L =50 pF R _L =500Ω		13.0		12.0		9.0		8.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time OE to Y ^[7]	C _L =300 pF R _L =500Ω		25.0		23.0		16.0		15.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y ^[7]	C _L =5 pF R _L =500Ω		8.0		7.0		7.0		6.5	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time OE to Y	C _L =50 pF R _L =500Ω		9.0		8.0		8.0		7.5	ns	1, 7, 8
t _{SU}	Data to CP Set-Up Time	C _L =50 pF R _L =500Ω	4.0		4.0		3.0		3.0		ns	4
t _H	Data to CP Hold Time		2.0		2.0		1.5		1.5		ns	4
t _{SU}	Enable \overline{EN} to CP Set-Up Time		4.0		4.0		3.0		3.0		ns	4
t _H	Enable \overline{EN} to CP Hold Time		2.0		2.0		0.0		0.0		ns	4
t _{REM}	Clear Recovery Time CLR to CP		7.0		6.0		6.0		6.0		ns	6
t _W	Clock Pulse Width		7.0		7.0		6.0		6.0		ns	5
t _W	\overline{CLR} Pulse Width LOW		7.0		6.0		6.0		6.0		ns	5

Notes:

13. Minimum limits are guaranteed but not tested on Propagation Delays.

14. See "Parameter Measurement Information."



Switching Characteristics Over the Operating Range (continued)

Param.	Description	Test Load	FCT821CT/FCT823CT/FCT825CT				Unit	Fig. No. ^[14]
			Military		Commercial			
			Min. ^[13]	Max.	Min. ^[13]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW)	C _L =50 pF R _L =500Ω		7.0		6.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to Y (\overline{OE} =LOW) ^[7]	C _L =300 pF R _L =500Ω		13.5		12.5	ns	1, 5
t _{PLH}	Propagation Delay CLR to Y ₁	C _L =50 pF R _L =500Ω		8.5		8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} to Y	C _L =50 pF R _L =500Ω		8.0		7.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} to Y ^[7]	C _L =300 pF R _L =500Ω		13.5		12.5	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time \overline{OE} to Y ^[7]	C _L =5 pF R _L =500Ω		6.2		6.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time \overline{OE} to Y	C _L =50 pF R _L =500Ω		6.5		6.5	ns	1, 7, 8
t _{SU}	Data to CP Set-Up Time	C _L =50 pF R _L =500Ω	3.0		3.0		ns	4
t _H	Data to CP Hold Time		1.5		1.5		ns	4
t _{SU}	Enable \overline{EN} to CP Set-Up Time		3.0		3.0		ns	4
t _H	Enable \overline{EN} to CP Hold Time		0.0		0.0		ns	4
t _{REM}	Clear Recovery Time CLR to CP		6.0		6.0		ns	6
t _W	Clock Pulse Width		6.0		6.0		ns	5
t _W	\overline{CLR} Pulse Width LOW		6.0		6.0		ns	5



Ordering Information – FCT821T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT821CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY54FCT821CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT821BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY54FCT821BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY74FCT821ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT821ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT821ATLMB	L64	28-Square Leadless Chip Carrier	

Ordering Information – FCT823T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT823CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.3	CY54FCT823CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823CTLMB	L64	28-Square Leadless Chip Carrier	
7.5	CY74FCT823BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
8.0	CY54FCT823BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823BTLMB	L64	28-Square Leadless Chip Carrier	
10.0	CY74FCT823ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT823ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT823ATLMB	L64	28-Square Leadless Chip Carrier	



Ordering Information—FCT825T

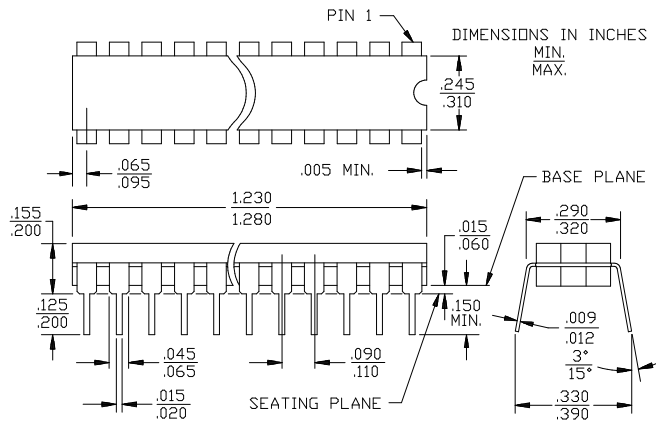
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT825CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT825CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT825BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825BTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT825BTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825BTLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT825ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT825ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT825ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT825ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT825ATLMB	L64	28-Square Leadless Chip Carrier	

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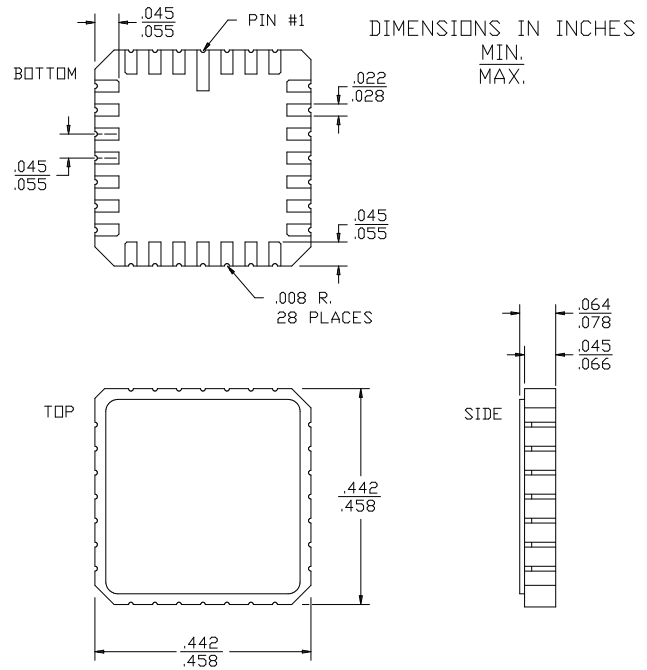


Package Diagrams

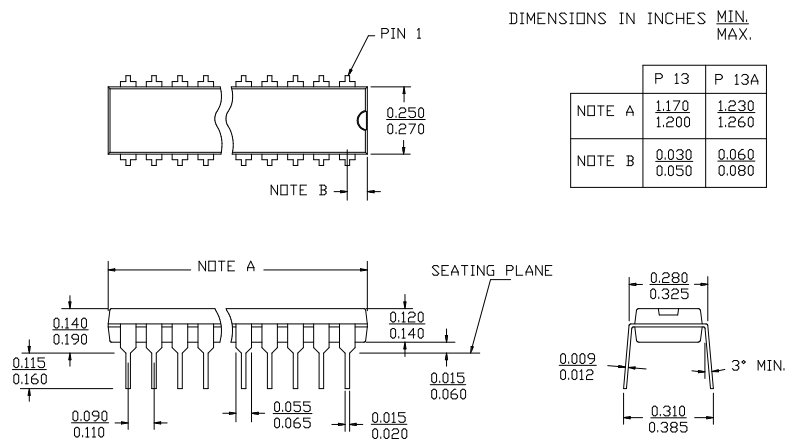
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config. A



28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4

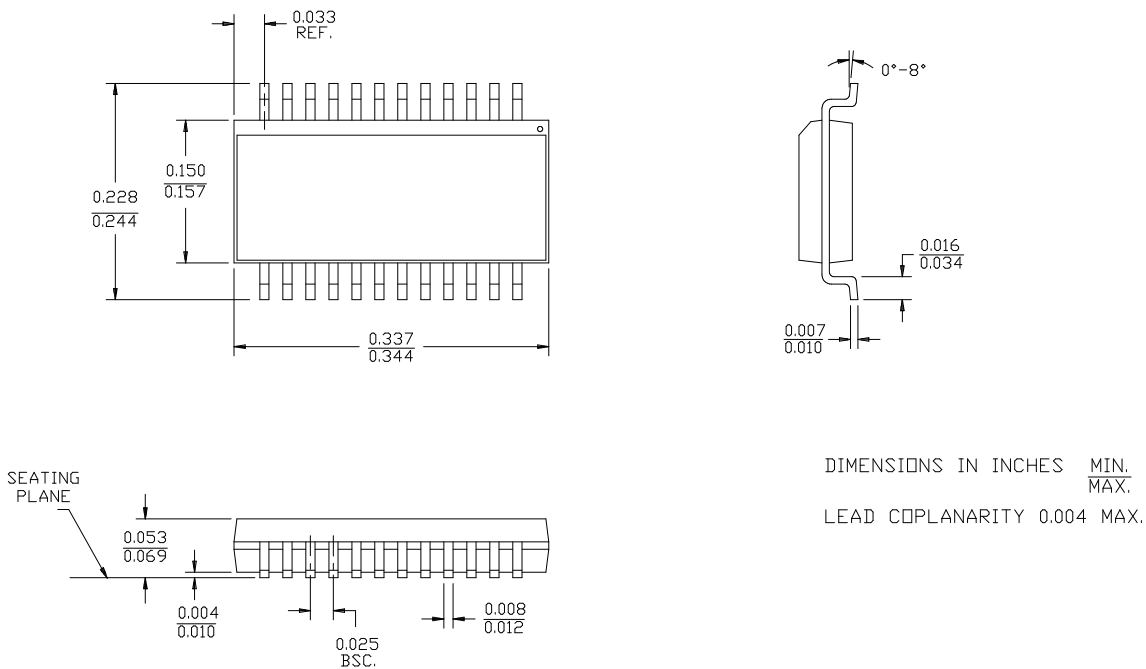


24-Lead (300-Mil) Molded DIP P13/P13A





24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13

