

8-Bit Registered Transceiver

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),
 48 mA (Mil)
- Source current 32 mA (Com'l),
 12 mA (Mil)
- ESD > 2000V

- Independent register for A and B buses
- Multiplexed real-time and stored data transfer

Functional Description

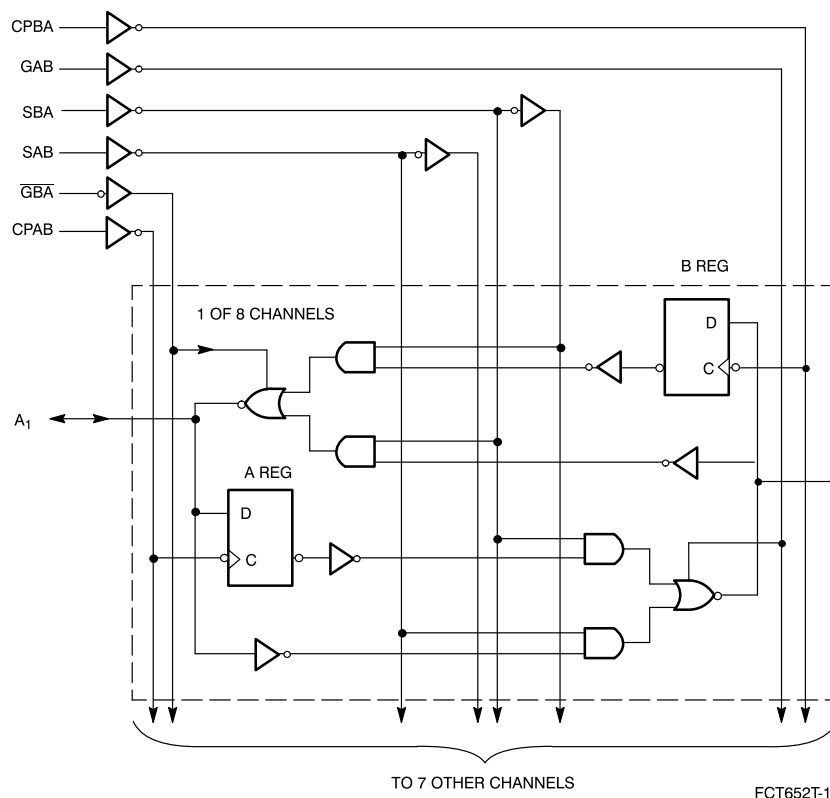
The FCT652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. \overline{GAB} and \overline{GBA} control pins are provided to control the transceiver functions. \overline{SAB} and \overline{SBA} control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time

data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When \overline{SAB} and \overline{SBA} are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling \overline{GAB} and \overline{GBA} . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

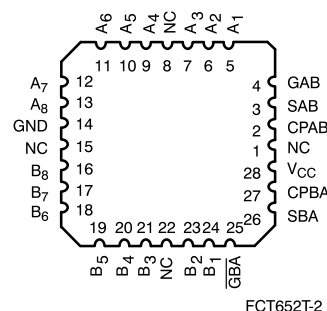
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

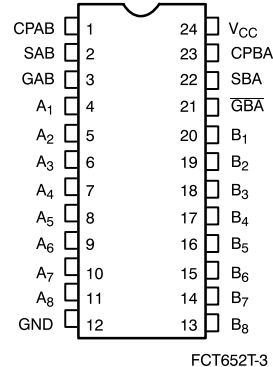


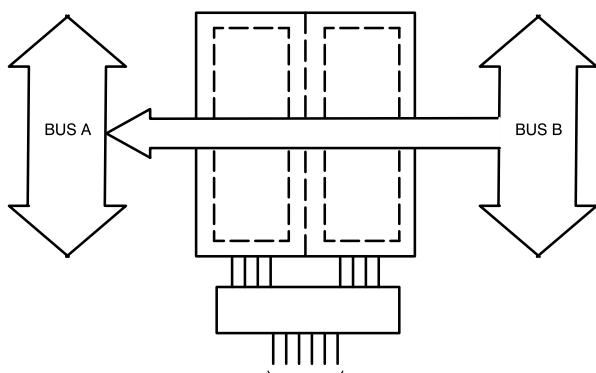
Pin Configurations

LCC Top View



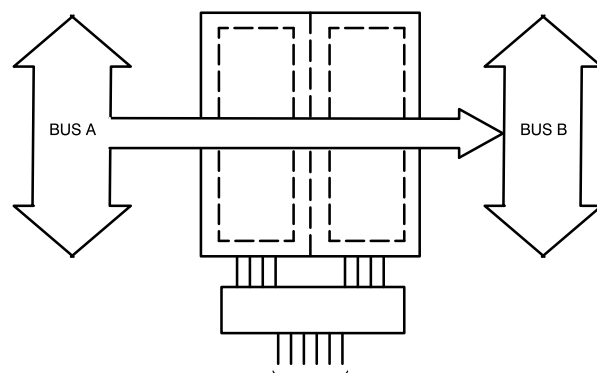
DIP/SOIC/QSOP Top View





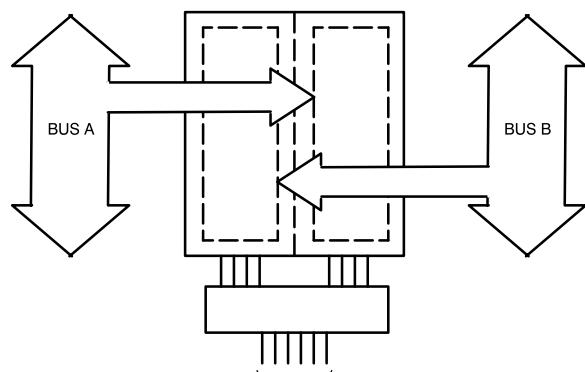
GAB L $\overline{\text{GBA}}$ L CPAB X CPBA X SAB X SBA L

Real-Time Transfer
Bus B to Bus A



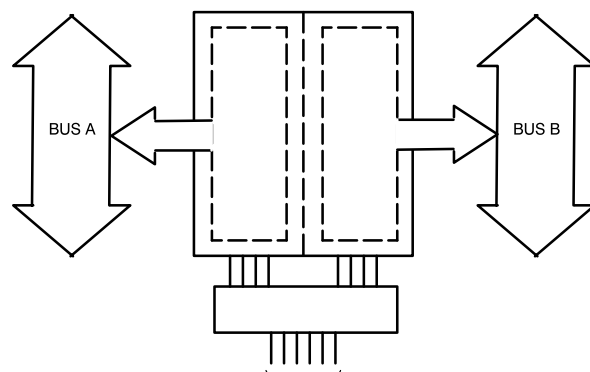
GAB H $\overline{\text{GBA}}$ H CPAB X CPBA X SAB L SBA X

Real-Time Transfer
Bus A to Bus B



GAB X L L $\overline{\text{GBA}}$ H X H CPAB X X X CPBA X X X SAB X X X SBA X X X

Store Data from A and/or B



GAB H $\overline{\text{GBA}}$ L CPAB H or L CPBA H or L SAB H SBA H

Transferred Stored Data
to A and/or B

Function Table^[1]

Inputs						Data I/O		Operation or Function
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA	A ₁ thru A ₈	B ₁ thru B ₈	
L L	H H	H or L ┐	H or L ┐	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	┐ ┐	H or L ┐	X X ^[1]	X X	Input Input	Unspecified ^[2] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ┐	┐ ┐	X X	X X ^[1]	Unspecified ^[2] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

- Select control=L: clocks can occur simultaneously.
Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level.
X = Don't Care. ┐ = LOW-to-HIGH Transition.
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



CY54/74FCT652T

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
Ambient Temperature with
Power Applied -65°C to $+135^{\circ}\text{C}$
Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
DC Input Voltage -0.5V to $+7.0\text{V}$
DC Output Voltage -0.5V to $+7.0\text{V}$
DC Output Current (Maximum Sink Current/Pin) 120 mA
Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	T, AT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[5]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[6]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} = -32 mA	2.0			V
		V _{CC} =Min., I _{OH} = -15 mA	2.4	3.3		V
		V _{CC} =Min., I _{OH} = -12 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} = 64 mA		0.3	0.55	V
		V _{CC} =Min., I _{OL} = 48 mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[7]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA
I _{IH}	Input HIGH Current ^[7]	V _{CC} =Max., V _{IN} = 2.7V			± 1	μA
I _{IL}	Input LOW Current ^[7]	V _{CC} =Max., V _{IN} = 0.5V			± 1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} = 2.7V			10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} = 0.5V			-10	μA
I _{OS}	Output Short Circuit Current ^[8]	V _{CC} =Max., V _{OUT} = 0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} = 0V , V _{OUT} = 4.5V			± 1	μA

Capacitance^[7]

Parameter	Description	Typ. ^[6]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}= 5.0V , T_A= $+25^{\circ}\text{C}$ ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V$, ^[9] $f_1 = 0$, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $GAB = GND, \overline{GBA} = GND,$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz},$ $GAB = GND, \overline{GBA} = GND,$ $SAB = CPAB = GND$ $SBA = V_{CC},$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5 \text{ MHz},$ $GAB = GND, \overline{GBA} = GND,$ $SAB = CPAB = GND$ $SBA = V_{CC},$ $V_{IN} = 3.4V$ or $V_{IN} = GND$	1.2	3.4	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz},$ 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 5 \text{ MHz},$ $GAB = \overline{GBA} = GND,$ $SAB = CPAB = GND$ $SBA = V_{CC},$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	2.8	5.6 ^[12]	mA
		$V_{CC} = \text{Max.}, f_0 = 10 \text{ MHz}, 50\% \text{ Duty Cycle},$ Outputs Open, Eight Bits Toggling at $f_1 = 5 \text{ MHz},$ $GAB = \overline{GBA} = GND,$ $SAB = CPAB = GND$ $SBA = V_{CC},$ $V_{IN} = 3.4V$ or $V_{IN} = GND$	5.1	14.6 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics^[13] Over the Operating Range

Parameter	Description	FCT652T				FCT652AT				Unit	Fig. No. ^[15]
		Military		Commercial		Military		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus	2.0	15.0	1.5	14.0	2.0	10.5	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	1.5	9.0	2.0	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	2.0	7.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	2.0	8.4	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW Bus to Clock	4.5		4.0		2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		1.5		ns	4
t _W	Clock Pulse Width, ^[16] HIGH or LOW	6.0		6.0		5.0		5.0		ns	5

Parameter	Description	FCT652CT				FCT652DT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min. ^[14]	Max.	Min. ^[14]	Max.	Min. ^[14]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	1.5	4.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus	1.5	8.9	1.5	7.8	1.5	5.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time Enable to Bus	1.5	7.7	1.5	6.3	1.5	4.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	1.5	4.4	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	1.5	5.0	ns	1, 5
t _S	Set-Up Time HIGH or LOW Bus to Clock	2.0		2.0		1.5		ns	4
t _H	Hold Time HIGH or LOW Bus to Clock	1.5		1.5		1.0		ns	4
t _W	Pulse Width, ^[16] HIGH or LOW	5.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

13. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1 of "Parameter Measurement Information" in the General Information section.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information section.
16. With one data channel toggling, t_W(L) = t_W(H) = 4.0 ns and t_r = t_f = 1.0 ns.



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT652DTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652DTSOC	S13	24-Lead (300-Mil) Molded SOIC	
5.4	CY74FCT652CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT652CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652CTLMB	L64	28-Square Leadless Chip Carrier	
6.3	CY74FCT652ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.7	CY54FCT652ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652ATLMB	L64	28-Square Leadless Chip Carrier	
9.0	CY74FCT652TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT652TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT652TSOC	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT652TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT652TLMB	L64	28-Square Leadless Chip Carrier	

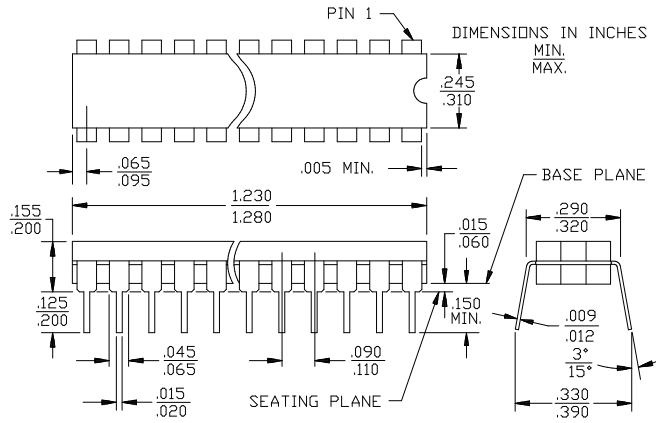
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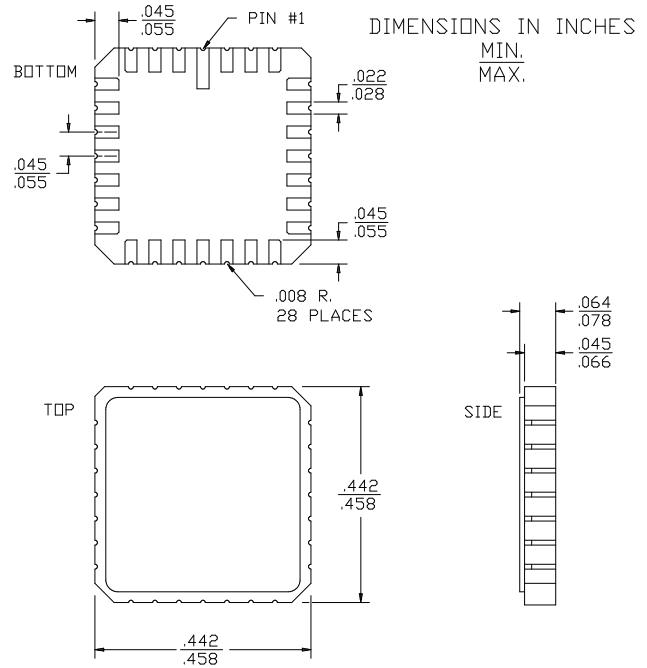


Package Diagrams

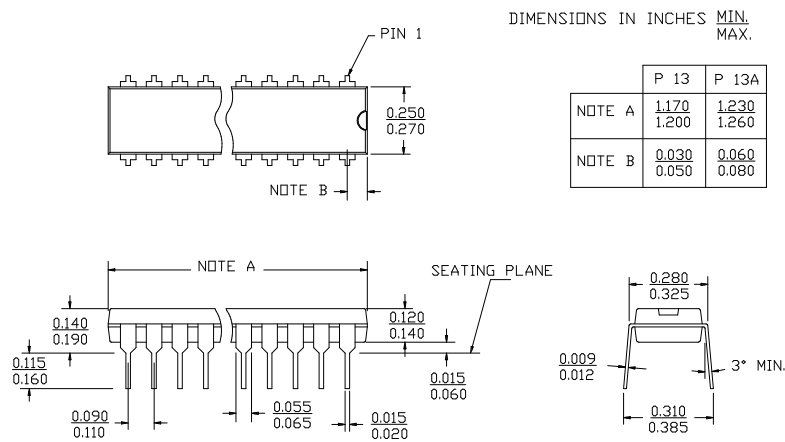
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9 Config. A



28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4

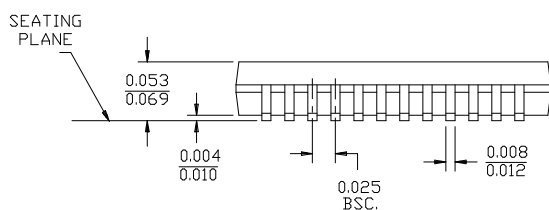
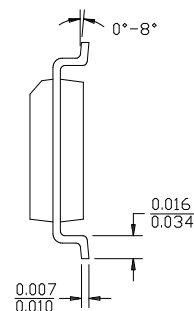
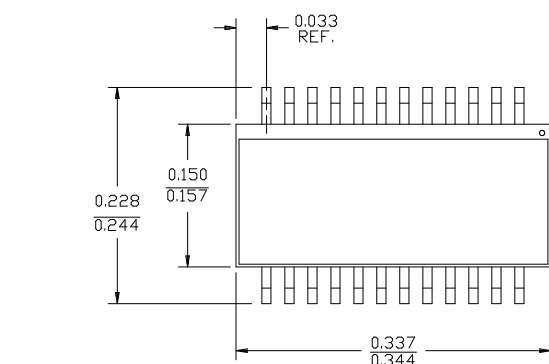


24-Lead (300-Mil) Molded DIP P13/P13A



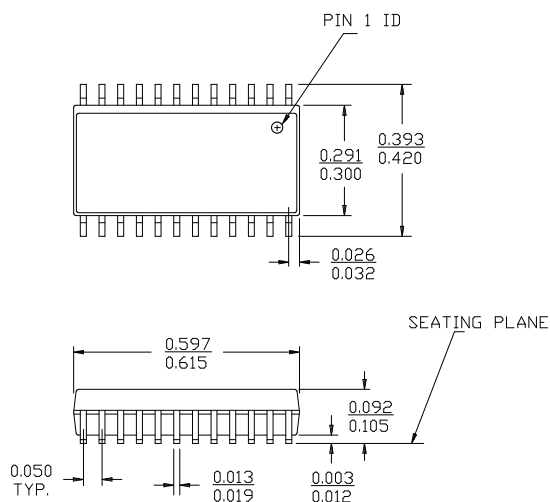


24-Lead Quarter Size Outline Q13



DIMENSIONS IN INCHES MIN. MAX.
LEAD COPLANARITY 0.004 MAX.

24-Lead (300-Mil) Molded SOIC S13



DIMENSIONS IN INCHES MIN. MAX.
LEAD COPLANARITY 0.004 MAX.

