



8-Bit Transceiver

Features

- Function, pinout, and drive compatible with FCT, F logic
- FCT-C speed at 4.1 ns max. (Com'l), FCT-A speed at 4.6 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l), 48 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)

Functional Description

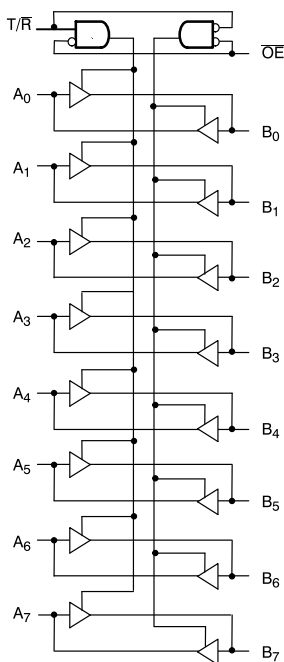
The FCT245T contains eight non-inverting bidirectional buffers with three-state outputs and is intended for bus oriented applications. For the FCT245T, current

sinking capability is 64 mA at the A and B ports.

The Transmit/Receiver (T/R) input determines the direction of data flow through bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports. The output enable (\overline{OE}), when HIGH, disables both the A and B ports by putting them in a High Z condition.

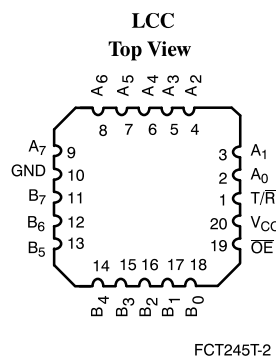
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

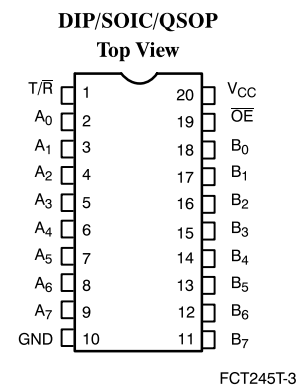


FCT245T-1

Pin Configurations



FCT245T-2



FCT245T-3

Function Table^[1]

\overline{OE}	T/R	Operation
L	L	B Data to Bus A
L	H	A Data to Bus B
H	X	High Z State

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -65°C to $+135^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Input Voltage -0.5V to $+7.0\text{V}$
 DC Output Voltage -0.5V to $+7.0\text{V}$
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	T, AT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[4]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V^{[8]}, f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC} = \text{Max.}, \text{One Input Toggling, } 50\% \text{ Duty Cycle, Outputs Open, } T/\bar{R} \text{ or } \overline{OE} = \text{GND and } V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current ^[10]	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, One Bit Toggling at } f_1 = 10 \text{ MHz, } T/\bar{R} \text{ or } \overline{OE} = \text{GND and } V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, One Bit Toggling at } f_1 = 10 \text{ MHz, } T/\bar{R} \text{ or } \overline{OE} = \text{GND and } V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.2	3.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, Eight Bits Toggling at } f_1 = 2.5 \text{ MHz, } T/\bar{R} \text{ or } \overline{OE} = \text{GND and } V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	1.3	2.6 ^[11]	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle, Outputs Open, Eight Bits Toggling at } f_1 = 2.5 \text{ MHz, } T/\bar{R} \text{ or } \overline{OE} = \text{GND and } V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 $I_{CC} = \text{Quiescent Current with CMOS input levels}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL HIGH input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL inputs HIGH}$

$N_T = \text{Number of TTL inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an input transition pair (HLH or LHL)}$

$f_0 = \text{Clock frequency for registered devices, otherwise zero}$

$f_1 = \text{Input signal frequency}$

$N_1 = \text{Number of inputs changing at } f_1$

All currents are in milliamps and all frequencies are in megahertz.

11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



CY54/74FCT245T

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245T				FCT245AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to B or B to A	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} or T/ \overline{R} to A or B	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OE} or T/ \overline{R} to A or B	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns	1, 7, 8

Switching Characteristics Over the Operating Range

Parameter	Description	FCT245CT				FCT245DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to B or B to A	1.5	4.5	1.5	4.1	1.5	3.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time OE or T/R to A or B	1.5	6.2	1.5	5.8	1.5	5.0	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OE or T/R to A or B	1.5	5.2	1.5	4.8	1.5	4.3	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.



CY54/74FCT245T

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT245DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT245DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT245CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.5	CY54FCT245CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245CTLMB	L61	20-Square Leadless Chip Carrier	
4.6	CY74FCT245ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.9	CY54FCT245ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245ATLMB	L61	20-Square Leadless Chip Carrier	
7.0	CY74FCT245TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT245TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT245TSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT245TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT245TLMB	L61	20-Square Leadless Chip Carrier	

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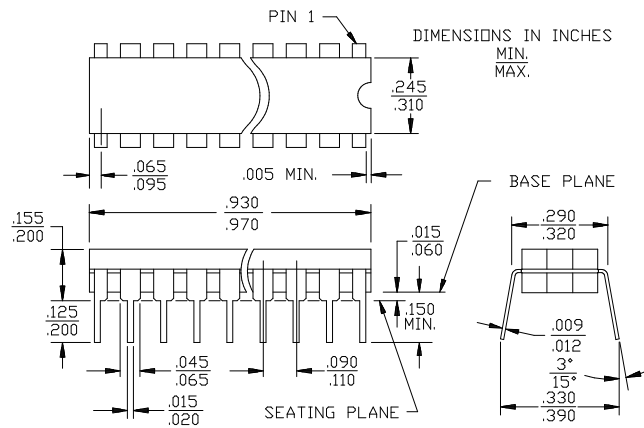
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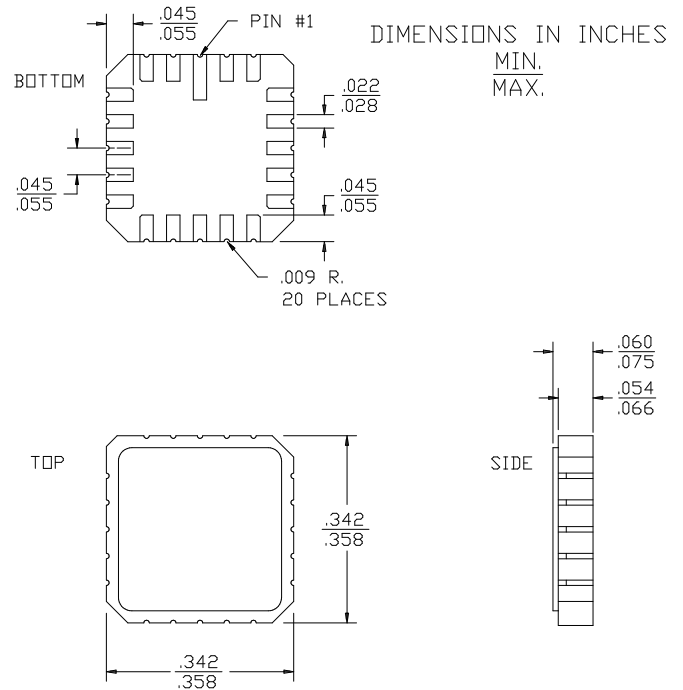
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Package Diagrams

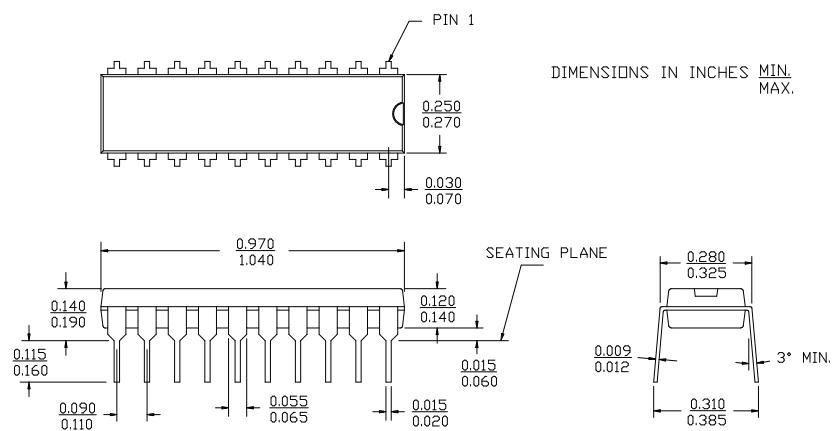
20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



20-Lead (300-Mil) Molded DIP P5

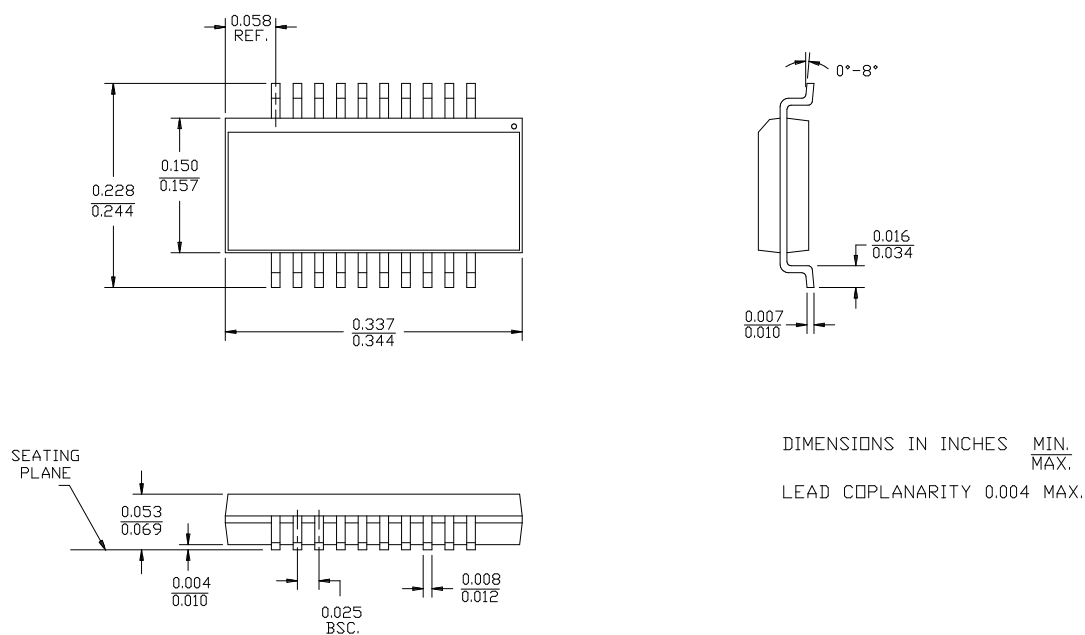




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Package Diagrams (continued)

20-Lead Quarter Size Outline Q5



20-Lead (300-Mil) Molded SOIC S5

