



CY54/74FCT2373T CY54/74FCT2573T

8-Bit Latches

Features

- Function and pinout compatible with the fastest bipolar logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.7 ns max. (Com'l)
FCT-A speed at 5.2 ns max. (Com'l)
- Reduced V_{OH} (typically=3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- ESD > 2000V

- Fully compatible with TTL input and output logic levels

Sink current	12 mA (Com'l), 12 mA (Mil)
Source current	15 mA (Com'l), 12 mA (Mil)

Functional Description

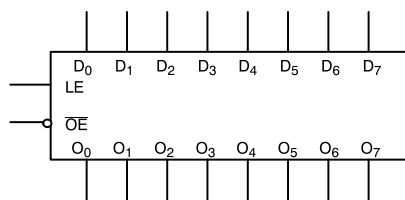
The FCT2373T and FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. FCT2373T can be used to replace

FCT373T, and FCT2573T to replace FCT573T to reduce noise in an existing design.

When latch enable (LE) is HIGH, the flip-flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable (OE) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

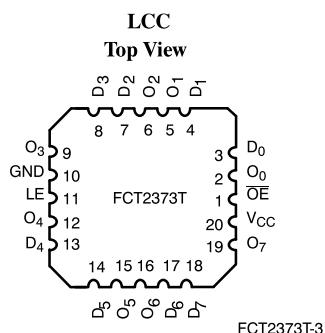
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Symbol



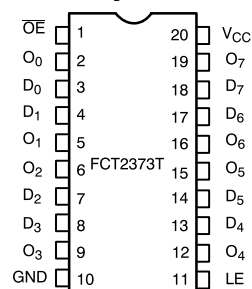
FCT2373T-1

Pin Configurations



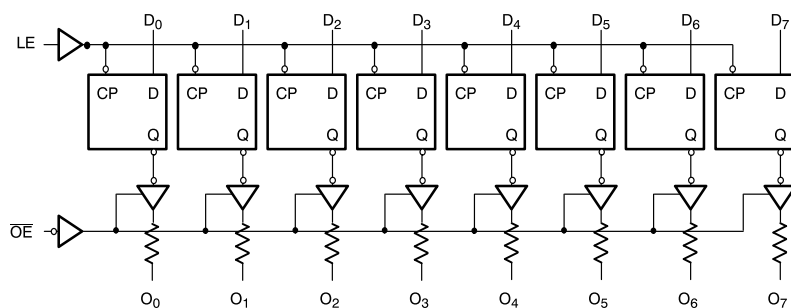
FCT2373T-3

DIP/SOIC/QSOP Top View



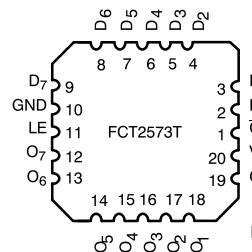
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Logic Block Diagram



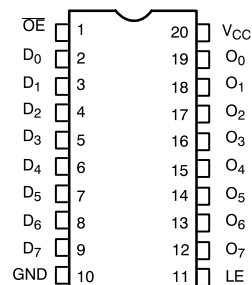
FCT2373T-2

LCC Top View



FCT2373T-5

DIP/SOIC/QSOP Top View



FCT2373T-6

Function Table^[1]

Inputs			Outputs
\overline{OE}	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied -65°C to $+135^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$

DC Input Voltage -0.5V to $+7.0\text{V}$

DC Output Voltage -0.5V to $+7.0\text{V}$

DC Output Current (Maximum Sink Current/Pin) 120 mA

Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	CT, DT	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Commercial	T, AT	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 5\%$
Military ^[4]	All	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =12 mA	Mil		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	28	40	Ω
		V _{CC} =Min., I _{OL} =12 mA	Mil		25		Ω
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				± 1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				± 1	μA
I _{IOZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V				10	μA
I _{IOZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				± 1	μA

Notes:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
Q_n = Previous state of flip flops (Q_{n-1})
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



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Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, \overline{OE} =GND, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, \overline{OE} =GND, LE=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, \overline{OE} =GND, LE=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, \overline{OE} =GND, LE=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, \overline{OE} =GND, LE=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



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Switching Characteristics Over the Operating Range^[12]

Parameter	Description	FCT2373T/FCT2573T				FCT2373AT/FCT2573AT				Unit	Fig. No. ^[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to O	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LE to O	2.0	14.0	2.0	13.0	2.0	9.8	2.0	8.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	12.5	1.5	11.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.5	1.5	7.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t _S	Set-Up Time, HIGH to LOW D to LE	2.0		2.0		2.0		2.0		ns	9
t _H	Hold Time, HIGH to LOW D to LE	1.5		1.5		1.5		1.5		ns	9
t _W	LE Pulse Width HIGH	6.0		6.0		6.0		5.0		ns	5

Parameter	Description	FCT2373CT/FCT2573CT				FCT2373DT/ FCT2573DT		Unit	Fig. No. ^[13]
		Military		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to O	1.5	5.1	1.5	4.2	1.5	3.8	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LE to O	2.0	8.0	2.0	5.5	2.0	4.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.3	1.5	5.5	1.5	4.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.9	1.5	5.0	1.5	4.0	ns	1, 7, 8
t _S	Set-Up Time, HIGH to LOW, D to LE	2.0		2.0		1.5		ns	9
t _H	Hold Time, HIGH to LOW, D to LE	1.5		1.5		1.0		ns	9
t _W	LE Pulse Width HIGH	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.



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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT2373DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2373DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2373CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2373CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2373ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2373ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2373TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2373TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2373TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2373TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2373TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information

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3.8	CY74FCT2573DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2573DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.2	CY74FCT2573CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT2573CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573CTLMB	L61	20-Pin Square Leadless Chip Carrier	
5.2	CY74FCT2573ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.6	CY54FCT2573ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT2573TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT2573TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT2573TSOC	S5	20-Lead (300-Mil) Molded SOIC	
8.5	CY54FCT2573TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT2573TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

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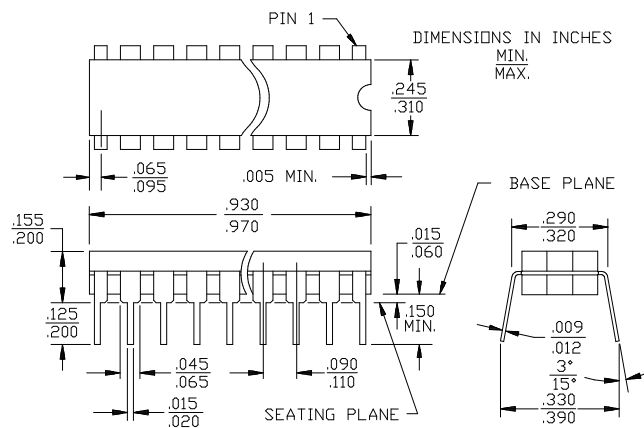


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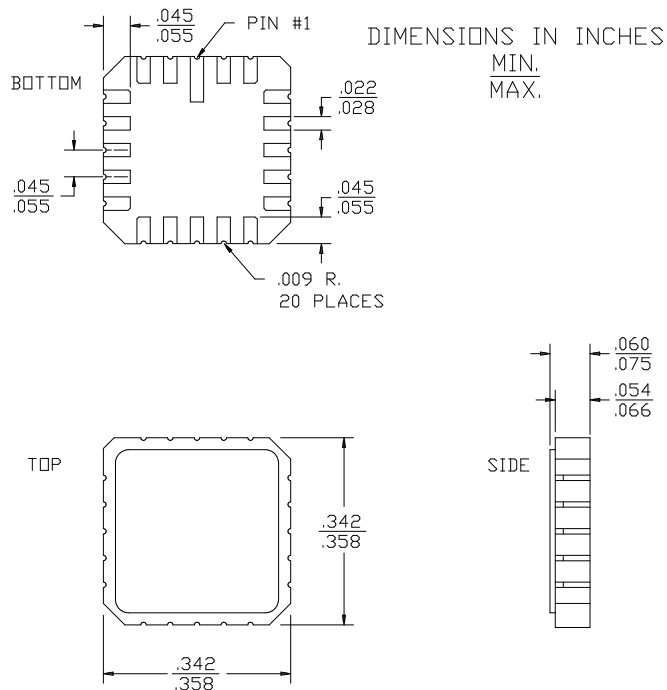
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Package Diagrams

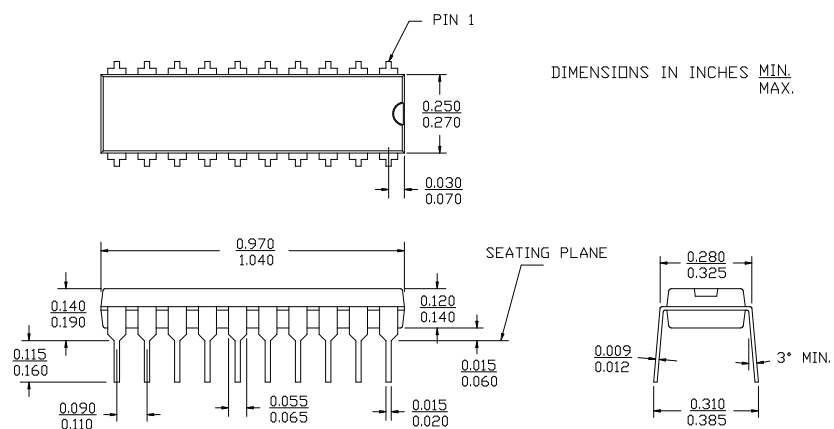
20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



20-Lead (300-Mil) Molded DIP P5



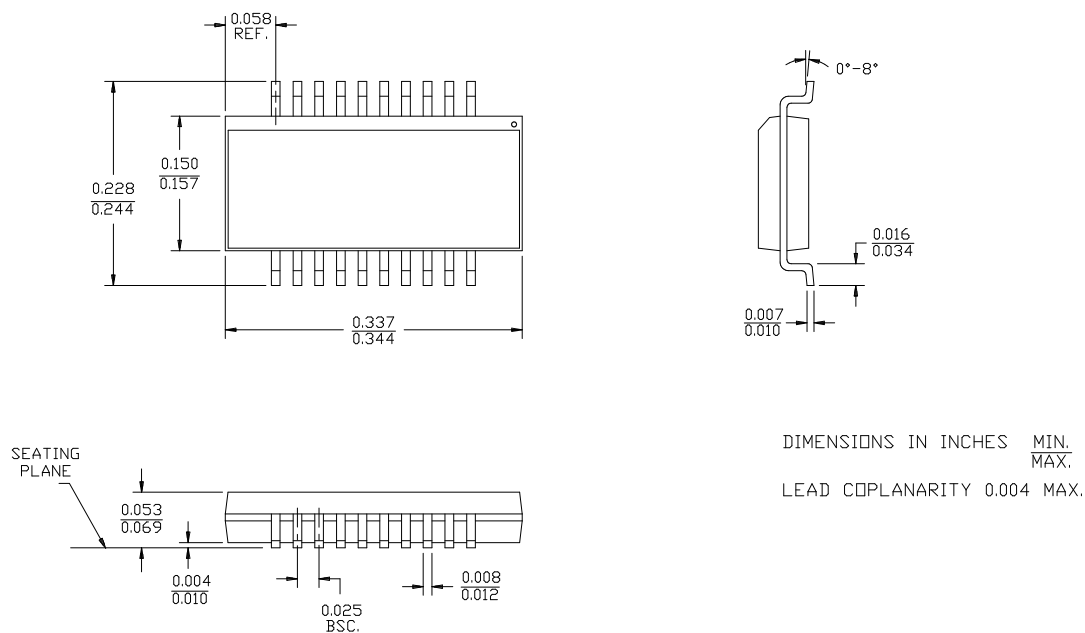


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Package Diagrams (continued)

20-Lead Quarter Size Outline Q5



20-Lead (300-Mil) Molded SOIC S5

