

Quad 2-Input Multiplexer

Features

- Function and pinout compatible with FCT and F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.3 ns max. (Com'l)
FCT-A speed at 5.0 ns max. (Com'l)
- TTL output level versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Fully compatible with TTL input and output logic levels
- ESD > 2000V

- Sink current 12 mA (Com'l),
12 mA (Mil)
- Source current 15 mA (Com'l),
12 mA (Mil)

Three-state outputs

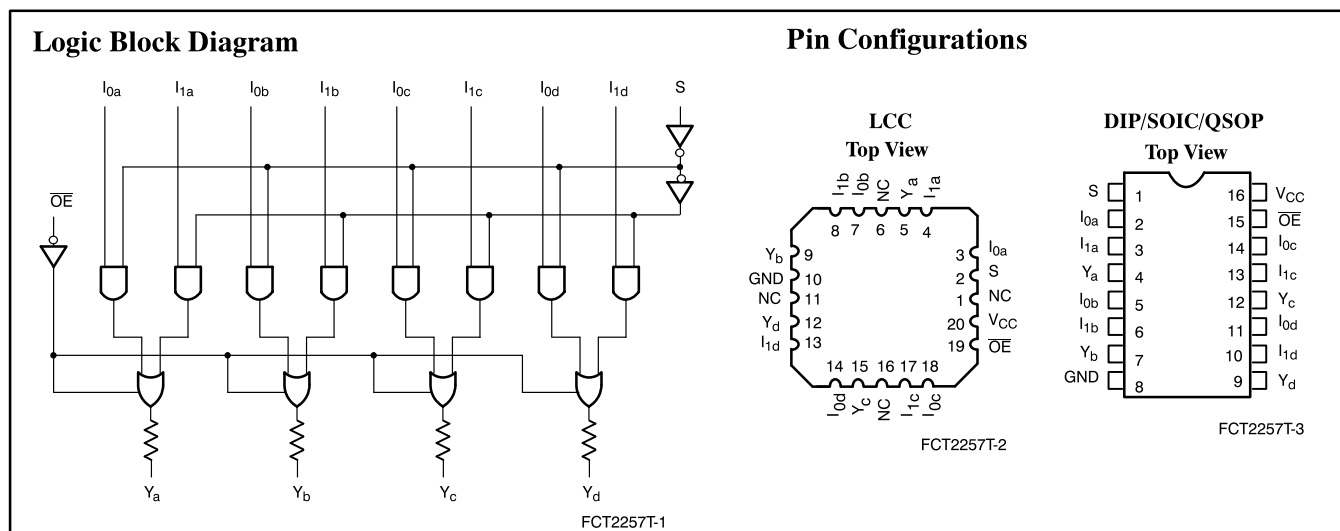
Functional Description

The FCT2257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT2257T. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2257T can be used to replace the FCT257T to reduce noise in an existing design.

The FCT2257T is a logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance "OFF" state when the Output Enable input (\overline{OE}) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.



Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Temperature with
 Power Applied -65°C to $+135^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5V to $+7.0\text{V}$
 DC Input Voltage -0.5V to $+7.0\text{V}$
 DC Output Voltage -0.5V to $+7.0\text{V}$
 DC Output Current (Maximum Sink Current/Pin) 120 mA
 Power Dissipation 0.5W

Static Discharge Voltage $>2001\text{V}$
 (per MIL-STD-883, Method 3015)

Operating Range

| Range | Range | Ambient Temperature | V _{CC} |
|-------------------------|-------|---|----------------------|
| Commercial | CT | 0°C to $+70^{\circ}\text{C}$ | $5\text{V} \pm 5\%$ |
| Commercial | T, AT | -40°C to $+85^{\circ}\text{C}$ | $5\text{V} \pm 5\%$ |
| Military ^[4] | All | -55°C to $+125^{\circ}\text{C}$ | $5\text{V} \pm 10\%$ |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Typ. ^[5] | Max. | Unit |
|------------------|---|---|-------|------|---------------------|---------|---------------|
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-15 mA | Com'l | 2.4 | 3.3 | | V |
| | | V _{CC} =Min., I _{OH} =-12 mA | Mil | 2.4 | 3.3 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =12 mA | Com'l | | 0.3 | 0.55 | V |
| | | V _{CC} =Min., I _{OL} =12 mA | Mil | | 0.3 | 0.55 | V |
| R _{OUT} | Output Resistance | V _{CC} =Min., I _{OL} =12 mA | Com'l | 20 | 25 | 40 | Ω |
| | | V _{CC} =Min., I _{OL} =12 mA | Mil | | 25 | | Ω |
| V _{IH} | Input HIGH Voltage | | | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | | | | | 0.8 | V |
| V _H | Hysteresis ^[6] | All inputs | | | 0.2 | | V |
| V _{IK} | Input Clamp Diode Voltage | V _{CC} =Min., I _{IN} =-18 mA | | | -0.7 | -1.2 | V |
| I _{IH} | Input HIGH Current | V _{CC} =Max., V _{IN} =2.7V | | | | ± 1 | μA |
| I _{IL} | Input LOW Current | V _{CC} =Max., V _{IN} =0.5V | | | | ± 1 | μA |
| I _{OZH} | Off State HIGH-Level Output Current | V _{CC} = Max., V _{OUT} = 2.7V | | | | 10 | μA |
| I _{OZL} | Off State LOW-Level Output Current | V _{CC} = Max., V _{OUT} = 0.5V | | | | -10 | μA |
| I _{OS} | Output Short Circuit Current ^[7] | V _{CC} =Max., V _{OUT} =0.0V | | -60 | -120 | -225 | mA |
| I _{OFF} | Power-Off Disable | V _{CC} =0V, V _{OUT} =4.5V | | | | ± 1 | μA |

Capacitance^[6]

| Parameter | Description | Test Conditions | Typ. ^[5] | Max. | Unit |
|------------------|--------------------|-----------------|---------------------|------|------|
| C _{IN} | Input Capacitance | | 5 | 10 | pF |
| C _{OUT} | Output Capacitance | | 9 | 12 | pF |

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ. ^[5] | Max. | Unit |
|-----------------|---|---|---------------------|---------------------|------------|
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ | 0.1 | 0.2 | mA |
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs) | $V_{CC} = \text{Max.}, V_{IN} = 3.4V$, ^[8] $f_1 = 0$, Outputs Open | 0.5 | 2.0 | mA |
| I_{CCD} | Dynamic Power Supply Current ^[9] | $V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | 0.06 | 0.12 | mA/ MHz |
| I_C | Total Power Supply Current ^[10] | $V_{CC} = \text{Max.}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10 \text{ MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | 0.7 | 1.4 | mA |
| | | $V_{CC} = \text{Max.}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10 \text{ MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ | 1.0 | 2.4 | mA |
| | | $V_{CC} = \text{Max.}$, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 2.5 \text{ MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | 0.7 | 1.4 ^[11] | mA |
| | | $V_{CC} = \text{Max.}$, 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1 = 2.5 \text{ MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ | 1.7 | 5.4 ^[11] | mA |

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
- I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
- f_0 = Clock frequency for registered devices, otherwise zero
- f_1 = Input signal frequency
- N_1 = Number of inputs changing at f_1
- All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



CY54/74FCT2257T

Switching Characteristics Over the Operating Range^[12]

| Parameter | Description | FCT2257T | | | | FCT2257AT | | | | Unit | Fig. No. ^[13] |
|--------------------------------------|---|----------|------|------------|------|-----------|------|------------|------|------|--------------------------|
| | | Military | | Commercial | | Military | | Commercial | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay I _a , I _b to Y | 1.5 | 7.0 | 1.5 | 6.0 | 1.5 | 5.8 | 1.5 | 5.0 | ns | 1, 3 |
| t _{PLH} t _{PHL} | Propagation Delay S to O | 1.5 | 12.0 | 1.5 | 10.5 | 1.5 | 8.1 | 1.5 | 7.0 | ns | 1, 3 |
| t _{PZH} t _{PZL} | Output Enable Time | 1.5 | 10.0 | 1.5 | 8.5 | 1.5 | 8.0 | 1.5 | 7.0 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time | 1.5 | 8.0 | 1.5 | 6.0 | 1.5 | 5.8 | 1.5 | 5.5 | ns | 1, 7, 8 |

| Parameter | Description | FCT2257CT | | Unit | Fig. No. ^[13] |
|--------------------------------------|---|------------|------|------|--------------------------|
| | | Commercial | | | |
| | | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay I _a , I _b to Y | 1.5 | 4.3 | ns | 1, 3 |
| t _{PLH} t _{PHL} | Propagation Delay S to O | 1.5 | 5.2 | ns | 1, 3 |
| t _{PZH} t _{PZL} | Output Enable Time | 1.5 | 6.0 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time | 1.5 | 5.0 | ns | 1, 7, 8 |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------|--------------|-------------------------------------|-----------------|
| 4.3 | CY74FCT2257CTPC | P1 | 16-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT2257CTQC | Q1 | 16-Lead (150-Mil) QSOP | |
| | CY74FCT2257CTSOC | S1 | 16-Lead (300-Mil) Molded SOIC | |
| 5.0 | CY74FCT2257ATPC | P1 | 16-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT2257ATQC | Q1 | 16-Lead (150-Mil) QSOP | |
| | CY74FCT2257ATSOC | S1 | 16-Lead (300-Mil) Molded SOIC | |
| 5.8 | CY54FCT2257ATDMB | D2 | 16-Lead (300-Mil) CerDIP | Military |
| | CY54FCT2257ATLMB | L61 | 20-Pin Square Leadless Chip Carrier | |
| 6.0 | CY74FCT2257TPC | P1 | 16-Lead (300-Mil) Molded DIP | Commercial |
| | CY74FCT2257TQC | Q1 | 16-Lead (150-Mil) QSOP | |
| | CY74FCT2257TSOC | S1 | 16-Lead (300-Mil) Molded SOIC | |
| 7.0 | CY54FCT2257TDMB | D2 | 16-Lead (300-Mil) CerDIP | Military |
| | CY54FCT2257TLMB | L61 | 20-Pin Square Leadless Chip Carrier | |

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.

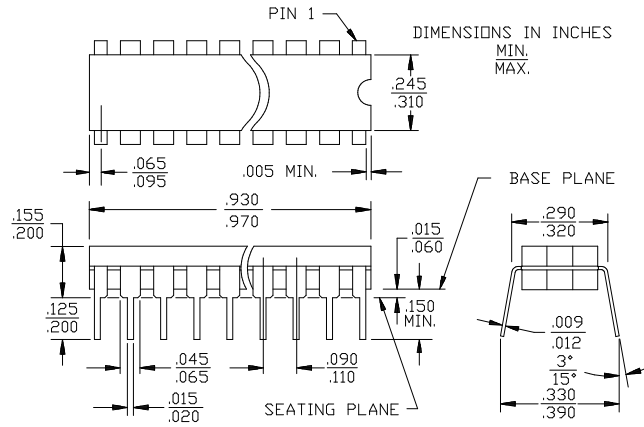
13. See "Parameter Measurement Information" in the General Information section.



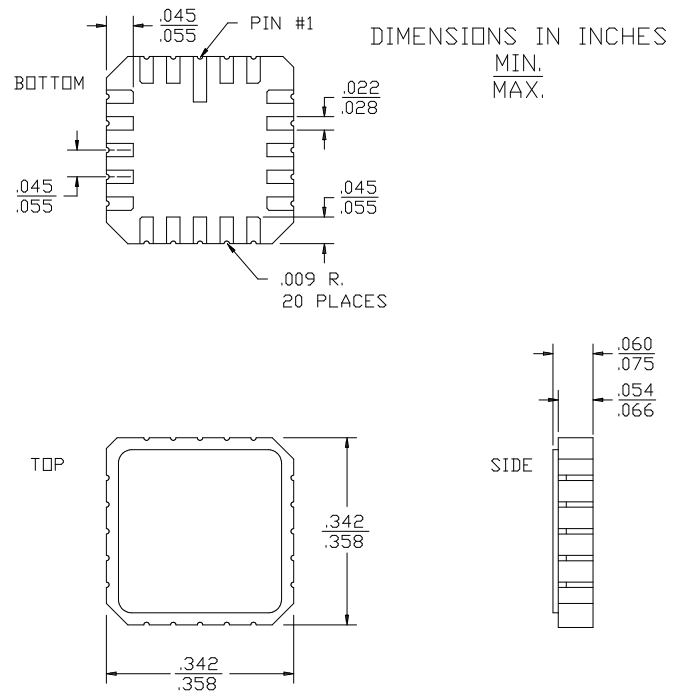
CY54/74FCT2257T

Package Diagrams

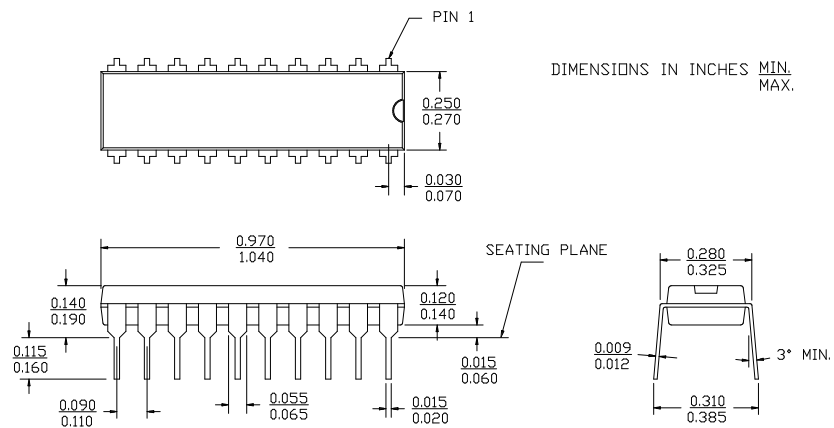
20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



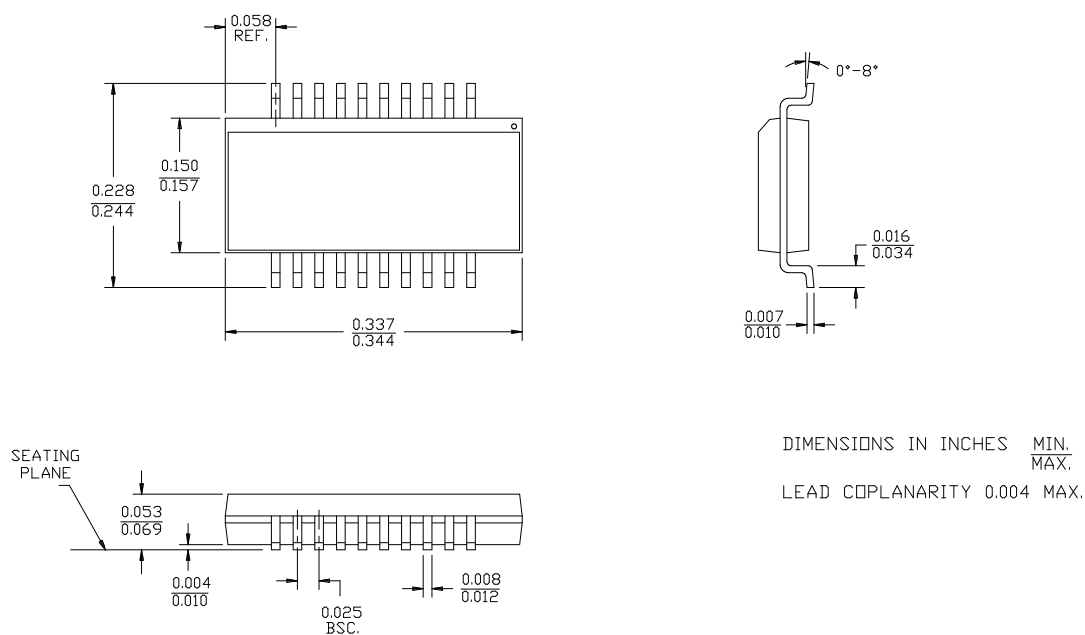
20-Lead (300-Mil) Molded DIP P5





Package Diagrams (continued)

20-Lead Quarter Size Outline Q5



20-Lead (300-Mil) Molded SOIC S5

