



CY74FCT16543T CY74FCT162543T

16-Bit Latched Transceivers

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 5.1 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16543T Features:

- 64 mA sink current (Com'l), 32 mA source current (Com'l)
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162543T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

Functional Description

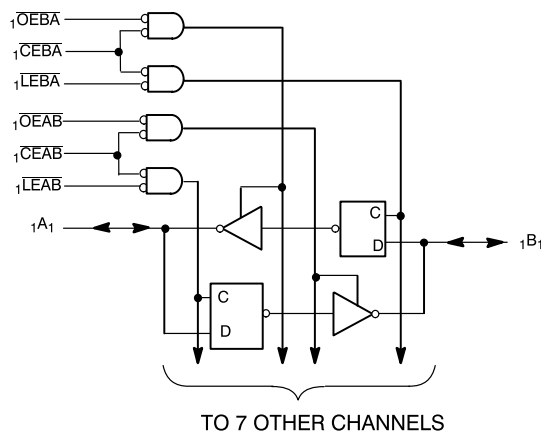
The CY74FCT16543T and CY74FCT162543T are 16-bit, high-speed, low power latched transceivers that are organized as two independent 8-bit D-type latched transceivers containing twosets of eight D-type latches with separate Latch Enable ($\overline{\text{LEAB}}$, $\overline{\text{LEAB}}$) and Output Enable ($\overline{\text{OEAB}}$, $\overline{\text{OEAB}}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable ($\overline{\text{CEAB}}$) must be LOW in order to enter data from A or to take data from B as indicated in the truth table. With $\overline{\text{CAEB}}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) makes the A-to-B latch-transparent; a subsequent LOW-to-

HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{\text{CEAB}}$, $\overline{\text{LEAB}}$, and $\overline{\text{OEAB}}$ inputs flow-through pinout and small shrink packaging and in simplifying board design. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

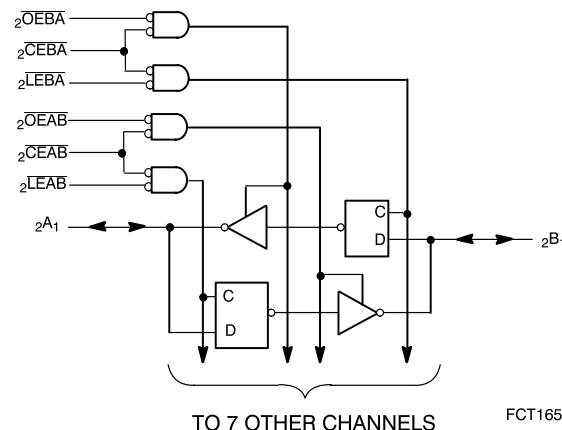
The CY74FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162543T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162543T is ideal for driving transmission lines.

Logic Block Diagrams



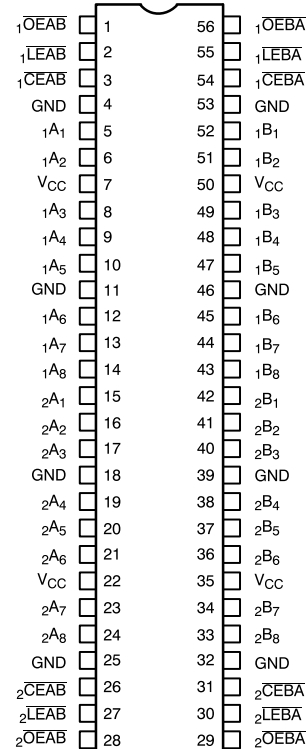
FCT16543T-1



FCT16543T-2

Pin Configuration

Top View SSOP/TSSOP



FCT16543T-3



Pin Description

Name	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
\overline{CEAB}	A-to-B Enable Input (Active LOW)
\overline{CEBA}	B-to-A Enable Input (Active LOW)
\overline{LEAB}	A-to-B Latch Enable Input (Active LOW)
\overline{LEBA}	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature Com'l -55°C to +125°C
DC Output Voltage -0.5V to +7.0V
DC Output Current
(Maximum Sink Current/Pin) -60 to +120 mA
Power Dissipation 1.0W

Notes:

1. A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
2. Data prior to \overline{LEAB} LOW-to-HIGH Transition
H = HIGH Voltage Level. L = LOW Voltage Level.
X = Don't Care. Z = High Impedance.

Function Table^[1]

Inputs			Latch Status	Output Buffers
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs ^[2]

Ambient Temperature with
Power Applied Com'l -55°C to +125°C
DC Input Voltage -0.5V to +7.0V
Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =−18 mA		−0.7	−1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	−80	−140	−200	mA
I _O	Output Drive Current ^[7]	V _{CC} =Max., V _{OUT} =2.5V	−50		−180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16543T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =−3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =−15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =−32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162543T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I _{ODL}	Output LOW Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	−60	−115	−150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =−24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.

6. This parameter is guaranteed but not tested.

7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

8. This parameter is guaranteed but not tested.

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V^{[9]}$	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^[10]	$V_{CC} = \text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	60	100	$\mu A/\text{MHz}$
I_C	Total Power Supply Current ^[11]	$V_{CC} = \text{Max.}$, $f_1 = 10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.6	1.5	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	0.9	2.3	mA
		$V_{CC} = \text{Max.}$, $f_1 = 2.5 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.4	4.5 ^[12]	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	6.4	16.5 ^[12]	mA

Notes:

9. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH

- N_T = Number of TTL inputs at D_H
- I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
- f_0 = Clock frequency for registered devices, otherwise zero
- f_1 = Input signal frequency
- N_1 = Number of inputs changing at f_1
- All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range^[13]

Parameter	Description	Conditions ^[14]	74FCT16543T 74FCT162543T		74FCT16543AT 74FCT162543AT		74FCT16543CT 74FCT162543CT		Unit	Fig. No. ^[15]
			Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A to B or B to A	C _L =50pF R _L =500Ω	1.5	8.5	1.5	6.5	1.5	5.1	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay LEBA to A, LEAB to B		1.5	12.5	1.5	8.0	1.5	5.6	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A or B CEBA or CEAB to A or B		1.5	12.0	1.5	9.0	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time OEBA or OEAB to A or B CEBA or CEAB to A or B		1.5	9.0	1.5	7.5	1.5	6.5	ns	1, 7, 8
t _{SU}	Set-up Time HIGH or LOW A or B to LEAB or LEBA		2.0	—	2.0	—	2.0	—	ns	4
t _H	Hold Time HIGH or LOW A or B to LEAB or LEBA		2.0	—	2.0	—	2.0	—	ns	4
t _W	LEBA or LEAB Pulse Width LOW		4.0	—	4.0	—	4.0	—	ns	5
t _{SK(O)}	Output Skew ^[16]		—	0.5	—	0.5	—	0.5	ns	—

Notes:

13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See test circuits and waveforms.
15. See “Parameter Measurement Information” in the General Information section.
16. Skew between any two outputs of the same package switching in the same directional. This parameter is guaranteed by design.



Ordering Information CY74FCT16543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	CY74FCT16543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT16543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT16543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16543TPVC	O56	56-Lead (300-Mil) SSOP	

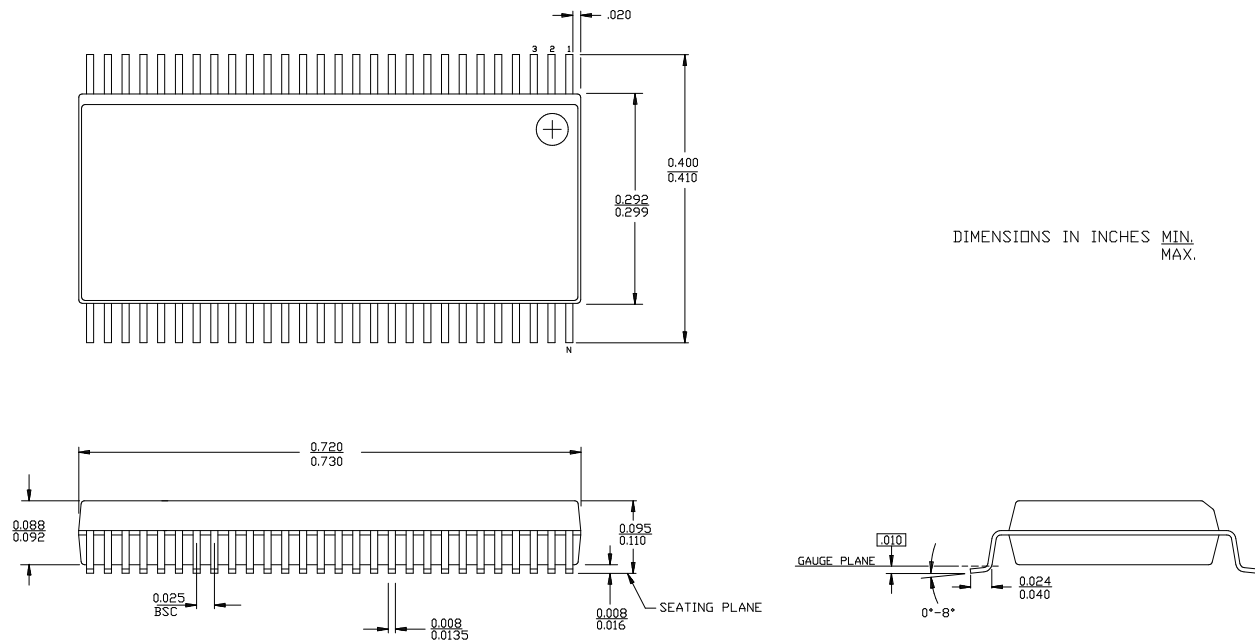
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5.1	CY74FCT162543CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
6.5	CY74FCT162543ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543ATPVC	O56	56-Lead (300-Mil) SSOP	
8.5	CY74FCT162543TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162543TPVC	O56	56-Lead (300-Mil) SSOP	

Document #: 38–00388

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56

