



PRELIMINARY

CY7C371i

# UltraLogic™ 32-Macrocell Flash CPLD

## Features

- 32 macrocells in two logic blocks
- 32 I/O pins
- 5 dedicated inputs including 2 clock pins
- In-System Reprogrammable (ISR™) Flash technology
  - JTAG interface
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
  - $f_{MAX} = 143$  MHz
  - $t_{PD} = 8.5$  ns
  - $t_S = 5$  ns
  - $t_{CO} = 6$  ns
- Fully PCI compliant
- Available in 44-pin PLCC, and TQFP packages
- Pin compatible with the CY7C372i

## Functional Description

The CY7C371i is an In-System Reprogrammable Complex Programmable Logic

Device (CPLD) and is part of the FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C371i is designed to bring the ease of use and high performance of the 22V10, as well as PCI Local Bus Specification support, to high-density CPLDs.

Like all of the UltraLogic FLASH370i devices, the CY7C371i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a 4-pin serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin ( $V_{PP}$ ). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

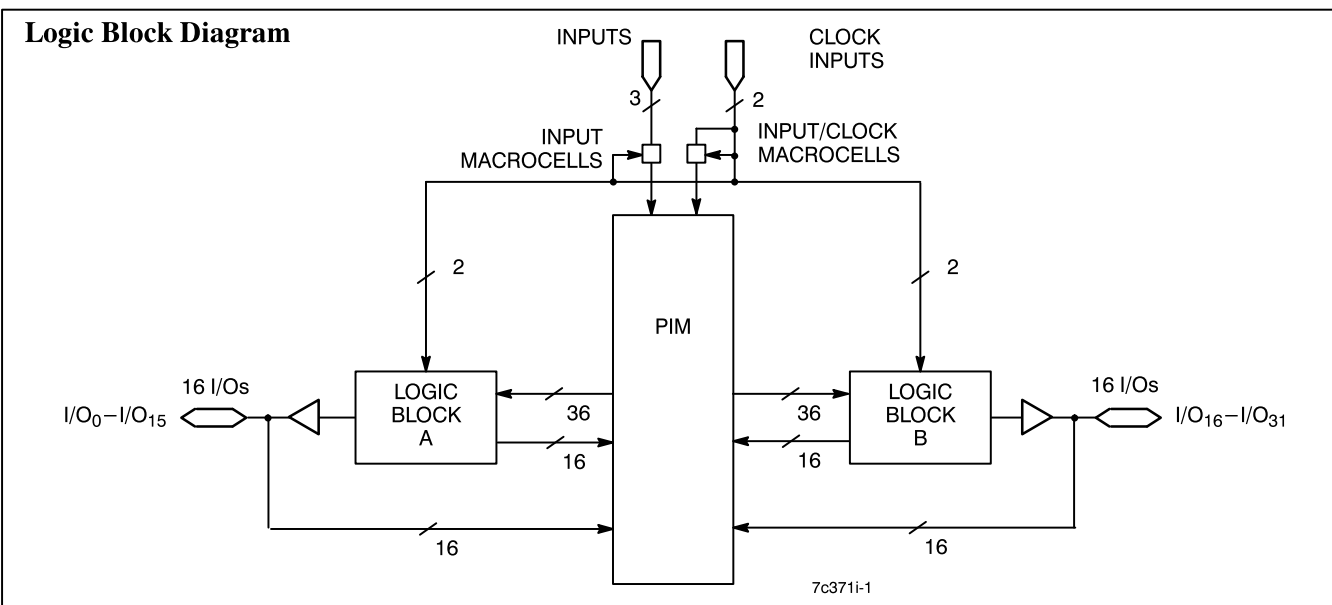
The 32 macrocells in the CY7C371i are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86

product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C371i is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371i. In addition, there are three dedicated inputs and two input/clock pins.

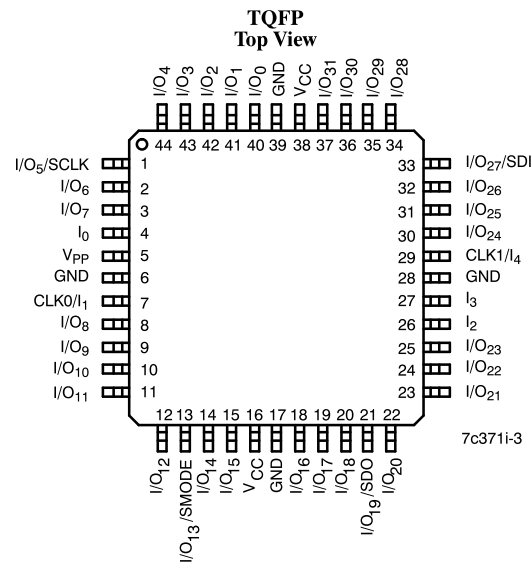
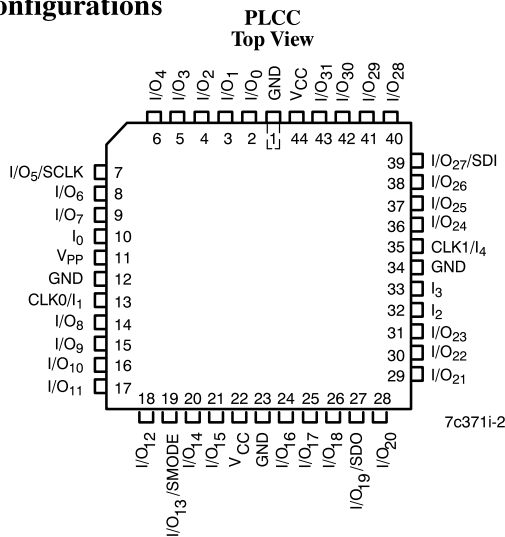
Finally, the CY7C371i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371i remain the same.



## Selection Guide

		7C371i-143	7C371i-110	7C371i-83	7C371iL-83	7C371i-66	7C371iL-66
Maximum Propagation Delay, $t_{PD}$ (ns)		8.5	10	12	12	15	15
Minimum Set-Up, $t_S$ (ns)		5	6	8	8	10	10
Maximum Clock to Output, $t_{CO}$ (ns)		6	6.5	8	8	10	10
Maximum Supply Current, $I_{CC}$ (mA)	Commercial	220	175	175	90	175	90
	Industrial			220	110	220	110

## Pin Configurations



### Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C371i includes two logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

#### Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

#### Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i CPLDs. Note that product term allocation is handled by software and is invisible to the user.

#### I/O Macrocell

Each of the macrocells on the CY7C371i has a separate associated I/O pin. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

### Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the two logic blocks on the CY7C371i to the inputs and to each other. All

inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

### Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, "An Introduction to In System Reprogramming with FLASH370i."

### PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

### Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V<sub>CC</sub> or GND.

### Design Tools

Development software for the CY7C371i is available from Cypress's Warp2™, Warp2Sim™, and Warp3™ software packages. All of these products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools such as ABEL™, CUPL™, MINC, and LOG/iC™. Please refer to third-party tool support for further information.



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State .....	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Program Voltage .....	12.5V

Output Current into Outputs (LOW) .....	16 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 5%
Industrial	-40°C to +85°C	5V ± 10%

## Electrical Characteristics Over the Operating Range<sup>[1]</sup>

Parameter	Description	Test Conditions		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -3.2 mA (Com'l/Ind) <sup>[2]</sup>	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 16 mA (Com'l/Ind) <sup>[2]</sup>		0.5	V
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs <sup>[3]</sup>		2.0	7.0	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs <sup>[3]</sup>		-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	V <sub>I</sub> = Internal GND, V <sub>I</sub> = V <sub>CC</sub>		-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-50	+50	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4, 5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V		-30	-160	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 1 MHz, V <sub>IN</sub> = GND, V <sub>CC</sub> <sup>[6]</sup>		Com'l	175	mA
				Com'l "L" -66, -83	90	
				Com'l-143, Ind	220	
				Ind "L" -66, -83	110	
I <sub>BHL</sub>	Input Bus Hold LOW Sustaining Current	V <sub>CC</sub> = Min., V <sub>IL</sub> = 0.8V		+75		μA
I <sub>BHH</sub>	Input Bus Hold HIGH Sustaining Current	V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V		-75		μA
I <sub>BHLO</sub>	Input Bus Hold LOW Overdrive Current	V <sub>CC</sub> = Max.		+500		μA
I <sub>BHHO</sub>	Input Bus Hold HIGH Overdrive Current	V <sub>CC</sub> = Max.		-500		μA

## Capacitance<sup>[5]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz		8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 5.0V at f = 1 MHz		12	pF
C <sub>CLK</sub>	Clock Signal Capacitance	V <sub>IN</sub> = 5.0V at f = 1 MHz	5	12	pF

## Inductance<sup>[5]</sup>

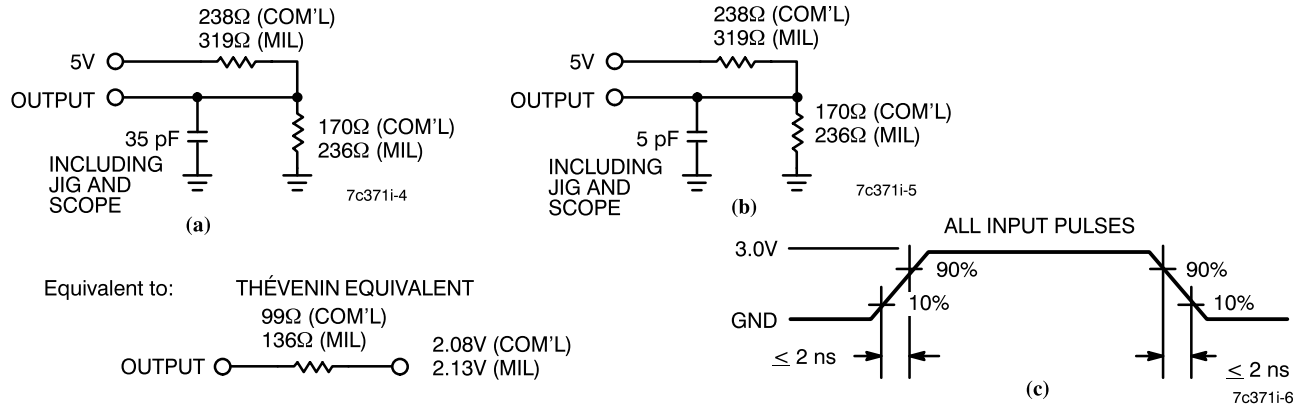
Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	Unit
L	Maximum Pin Inductance	V <sub>IN</sub> = 5.0V at f = 1 MHz	2	5	nH

### Notes:

- See the last page of this specification for Group A subgroup testing information.
- I<sub>OH</sub> = -2 mA, I<sub>OL</sub> = 2 mA for SDO. Note: SDI, SMODE, SCLK, have same V<sub>IH</sub> and V<sub>IL</sub>.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Measured with 16-bit counter programmed into each logic block.

**Endurance Characteristics<sup>[5]</sup>**

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

**AC Test Loads and Waveforms**


Parameter <sup>[7]</sup>	V <sub>X</sub>	Output Waveform—Measurement Level
t <sub>ER</sub> (-)	1.5V	V <sub>OH</sub> 0.5V
t <sub>ER</sub> (+)	2.6V	V <sub>OL</sub> 0.5V
t <sub>EA</sub> (+)	1.5V	V <sub>X</sub> 0.5V
t <sub>EA</sub> (-)	V <sub>thc</sub>	V <sub>X</sub> 0.5V

**(d) Test Waveforms**
**Switching Characteristics Over the Operating Range<sup>[8]</sup>**

Parameter	Description	7C371i-143		7C371i-110		7C371i-83 7C371iL-83		7C371i-66 7C371iL-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t <sub>PD</sub>	Input to Combinatorial Output		8.5		10		12		15	ns
t <sub>PDL</sub>	Input to Output Through Transparent Input or Output Latch		11.5		13		18		22	ns
t <sub>PDLL</sub>	Input to Output Through Transparent Input and Output Latches		13.5		15		20		24	ns
t <sub>EA</sub>	Input to Output Enable		13		14		19		24	ns
t <sub>ER</sub>	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t <sub>WL</sub>	Clock or Latch Enable Input LOW Time <sup>[5]</sup>	2.5		3		4		5		ns
t <sub>WH</sub>	Clock or Latch Enable Input HIGH Time <sup>[5]</sup>	2.5		3		4		5		ns
t <sub>IS</sub>	Input Register or Latch Set-Up Time	2		2		3		4		ns
t <sub>IH</sub>	Input Register or Latch Hold Time	2		2		3		4		ns
t <sub>ICO</sub>	Input Register Clock or Latch Enable to Combinatorial Output		12		14		19		24	ns
t <sub>ICOL</sub>	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		14		16		21		26	ns

**Notes:**

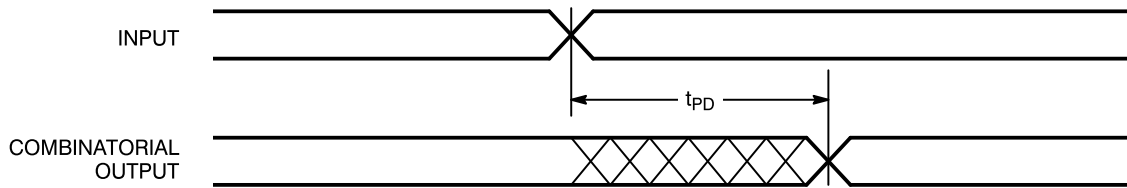
- t<sub>ER</sub> measured with 5-pF AC Test Load and t<sub>EA</sub> measured with 35-pF AC Test Load.
- All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

**Switching Characteristics** Over the Operating Range<sup>[8]</sup> (continued)

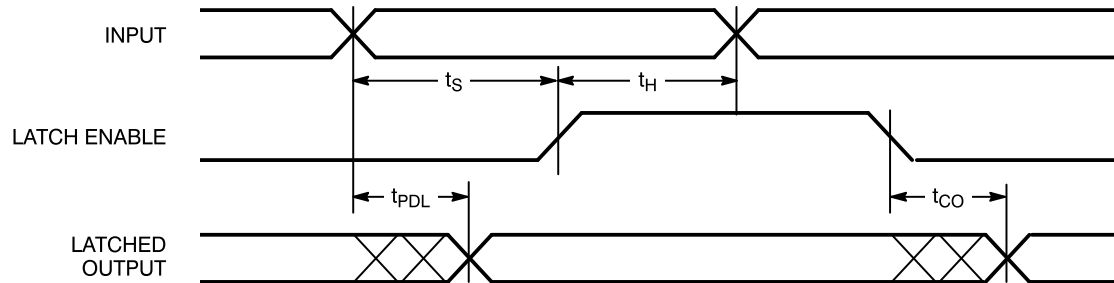
Parameter	Description	7C371i–143		7C371i–110		7C371i–83 7C371iL–83		7C371i–66 7C371iL–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Output Registered/Latched Mode Parameters										
t <sub>CO</sub>	Clock or Latch Enable to Output		6		6.5		8		10	ns
t <sub>S</sub>	Set-Up Time from Input to Clock or Latch Enable	5		6		8		10		ns
t <sub>H</sub>	Register or Latch Data Hold Time	0		0		0		0		ns
t <sub>CO2</sub>	Output Clock or Latch Enable to Output Delay (Through Memory Array)		12		14		19		24	ns
t <sub>SCS</sub>	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t <sub>SL</sub>	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t <sub>HL</sub>	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f <sub>MAX1</sub>	Maximum Frequency with Internal Feedback (Least of 1/t <sub>SCS</sub> , 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[5]</sup>	143		111		83.3		66.6		MHz
f <sub>MAX2</sub>	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>S</sub> + t <sub>H</sub> ), or 1/t <sub>CO</sub> ) <sup>[5]</sup>	166.7		153.8		100		83.3		MHz
f <sub>MAX3</sub>	Maximum Frequency with external feedback (Lesser of 1/(t <sub>CO</sub> + t <sub>S</sub> ) and 1/(t <sub>WL</sub> + t <sub>WH</sub> )) <sup>[5]</sup>	91		80		50		41.6		MHz
t <sub>OH</sub> –t <sub>IH</sub> 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x <sup>[5, 9]</sup>	0		0		0		0		ns
Pipelined Mode Parameters										
t <sub>ICS</sub>	Input Register Clock to Output Register Clock	7		9		12		15		ns
f <sub>MAX4</sub>	Maximum Frequency in Pipelined Mode (Least of 1/(t <sub>CO</sub> + t <sub>IS</sub> ), 1/t <sub>ICS</sub> , 1/(t <sub>WL</sub> + t <sub>WH</sub> ), 1/(t <sub>IS</sub> + t <sub>IH</sub> ), or 1/t <sub>SCS</sub> )	125		111		76.9		62.5		MHz
Reset/Preset Parameters										
t <sub>RW</sub>	Asynchronous Reset Width <sup>[5]</sup>	8		10		15		20		ns
t <sub>RR</sub>	Asynchronous Reset Recovery Time <sup>[5]</sup>	10		12		17		22		ns
t <sub>RO</sub>	Asynchronous Reset to Output		14		16		21		26	ns
t <sub>PW</sub>	Asynchronous Preset Width <sup>[5]</sup>	8		10		15		20		ns
t <sub>PR</sub>	Asynchronous Preset Recovery Time <sup>[5]</sup>	10		12		17		22		ns
t <sub>PO</sub>	Asynchronous Preset to Output		14		16		21		26	ns
t <sub>POR</sub>	Power-On Reset <sup>[5]</sup>		1		1		1		1	μs
Tap Controller Parameters										
f <sub>TAP</sub>	Tap Controller Frequency	500		500		500		500		kHz

**Note:**

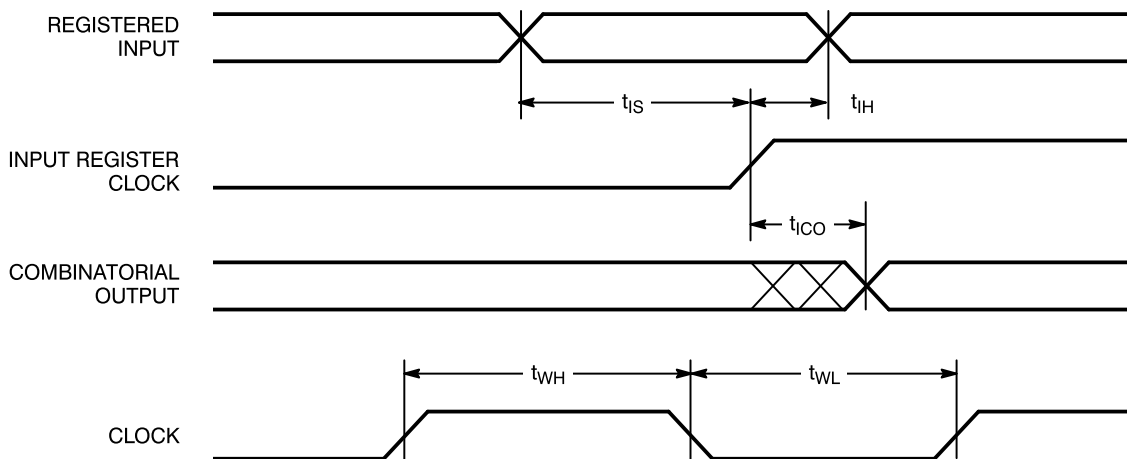
9. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C371i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

**Switching Waveforms**
**Combinatorial Output**


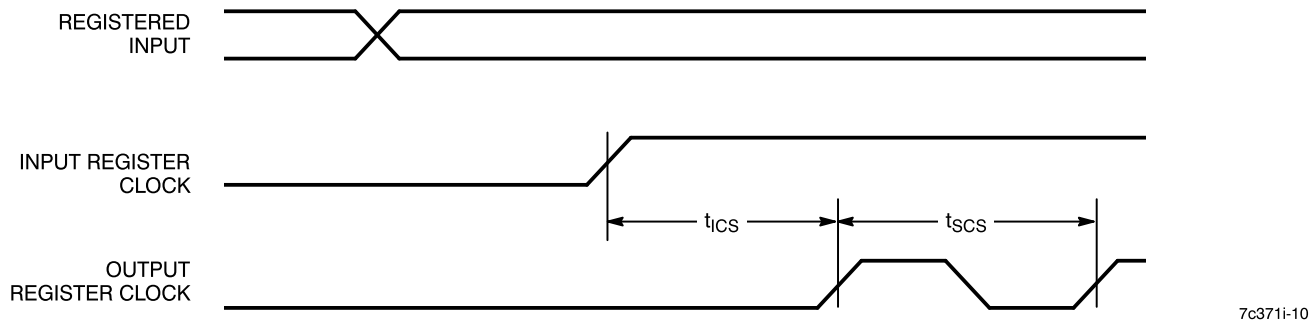
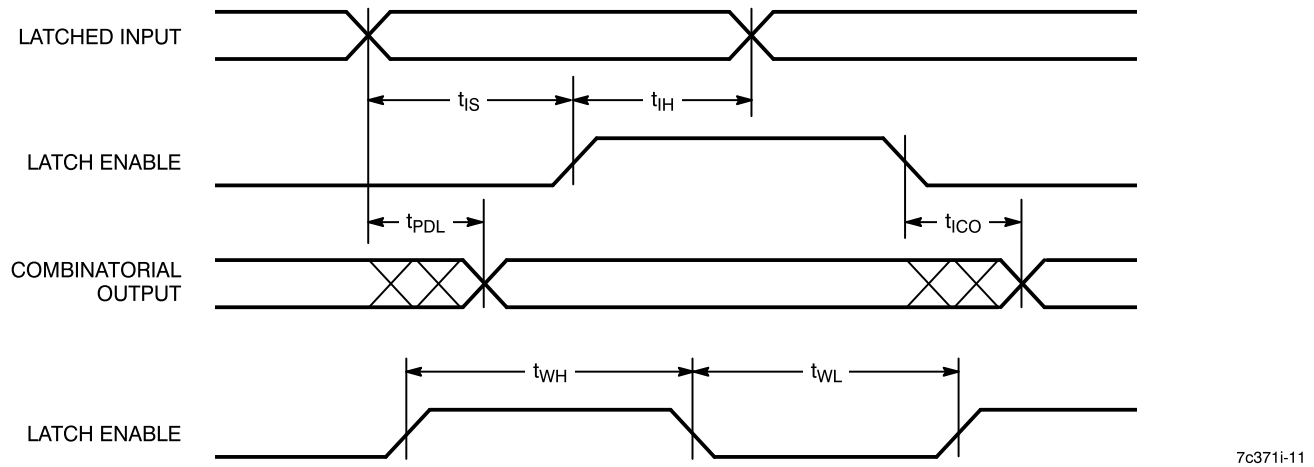
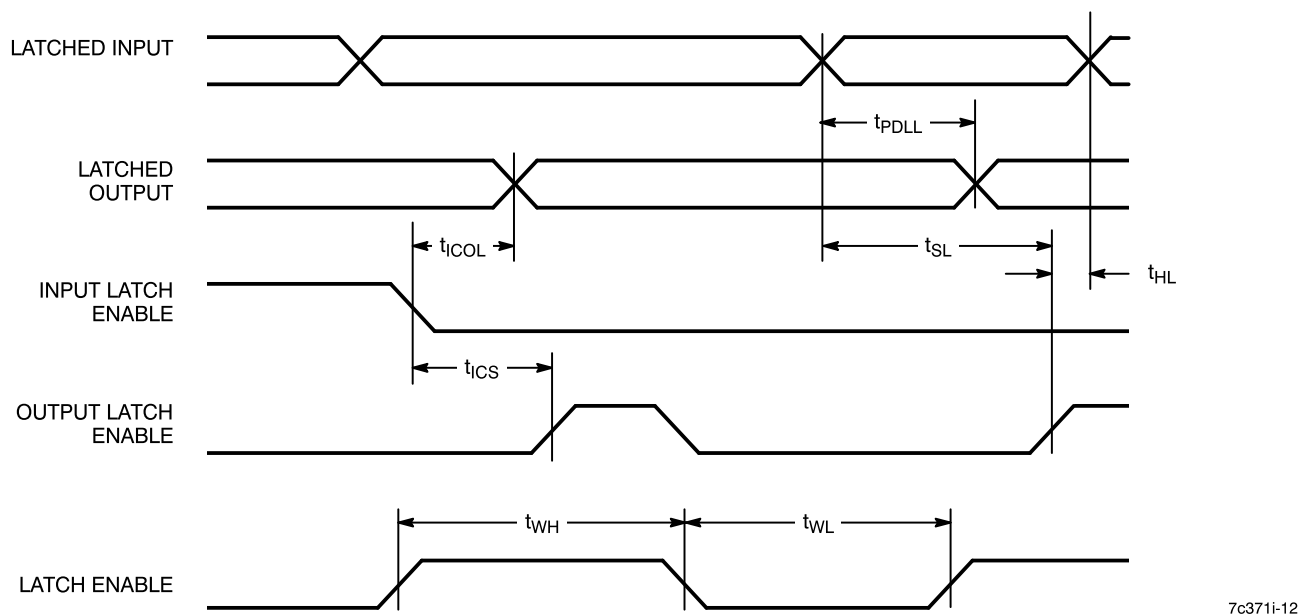
7c371i-7

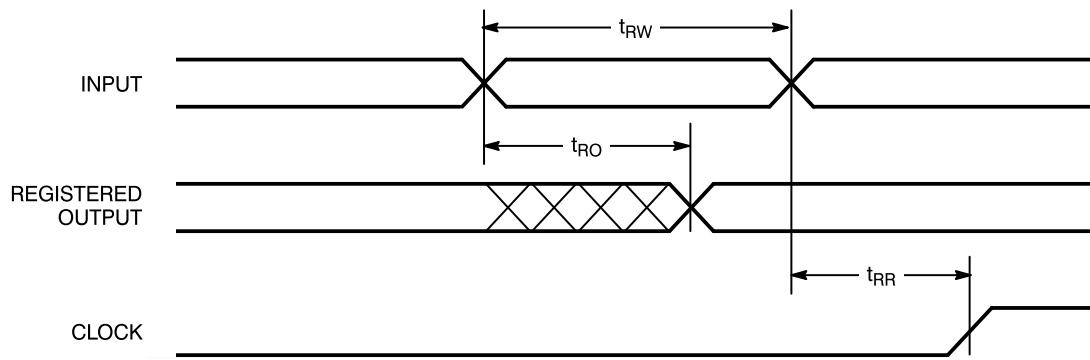
**Latched Output**


7c371i-8

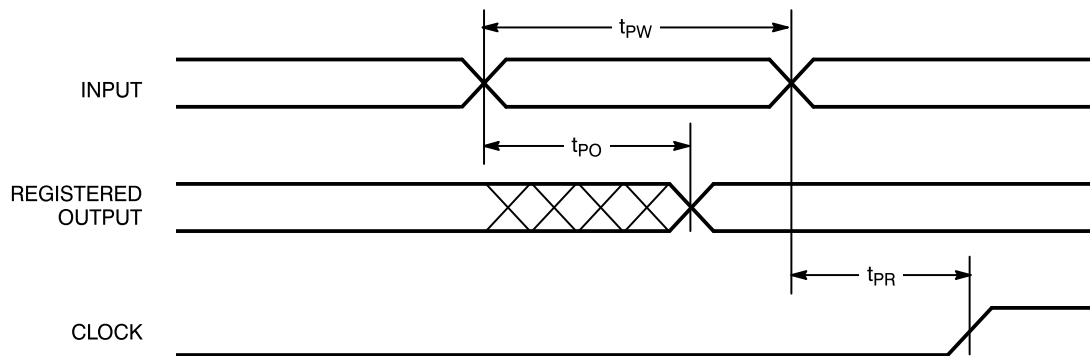
**Registered Input**


7c371i-9

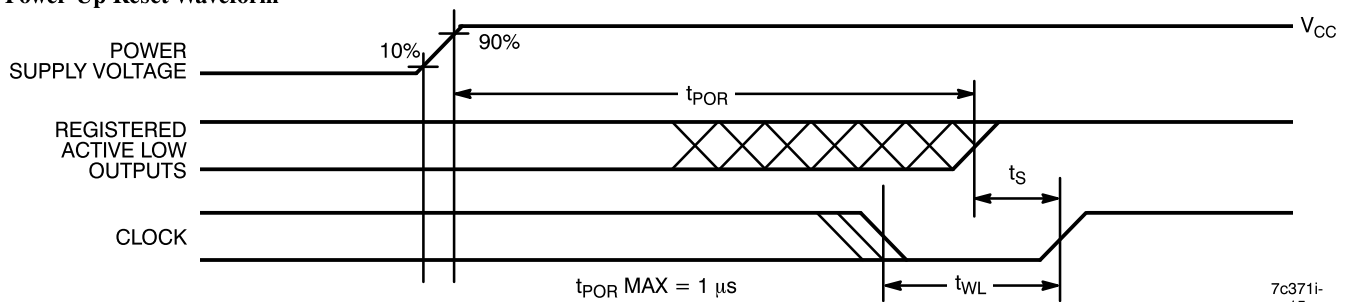
**Switching Waveforms (continued)**
**Clock to Clock**

**Latched Input**

**Latched Input and Output**


**Switching Waveforms (continued)**
**Asynchronous Reset**


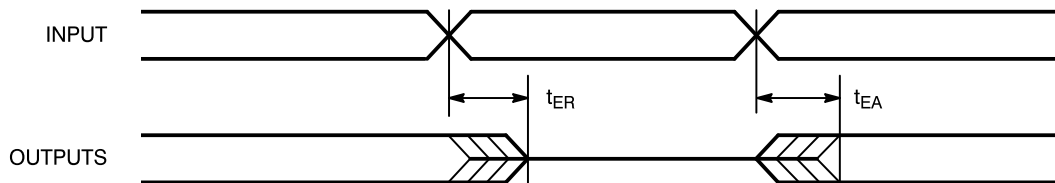
7c371i-13

**Asynchronous Preset**


7c371i-14

**Power-Up Reset Waveform**


7c371i-15

**Output Enable/Disable**


7c371i-16





### Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371i-143AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
110	CY7C371i-110AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-110JC	J67	44-Lead Plastic Leaded Chip Carrier	
83	CY7C371i-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL-83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL-83JI	J67	44-Lead Plastic Leaded Chip Carrier	
66	CY7C371i-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371i-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371i-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371i-66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371iL-66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371iL-66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371iL-66JI	J67	44-Lead Plastic Leaded Chip Carrier	

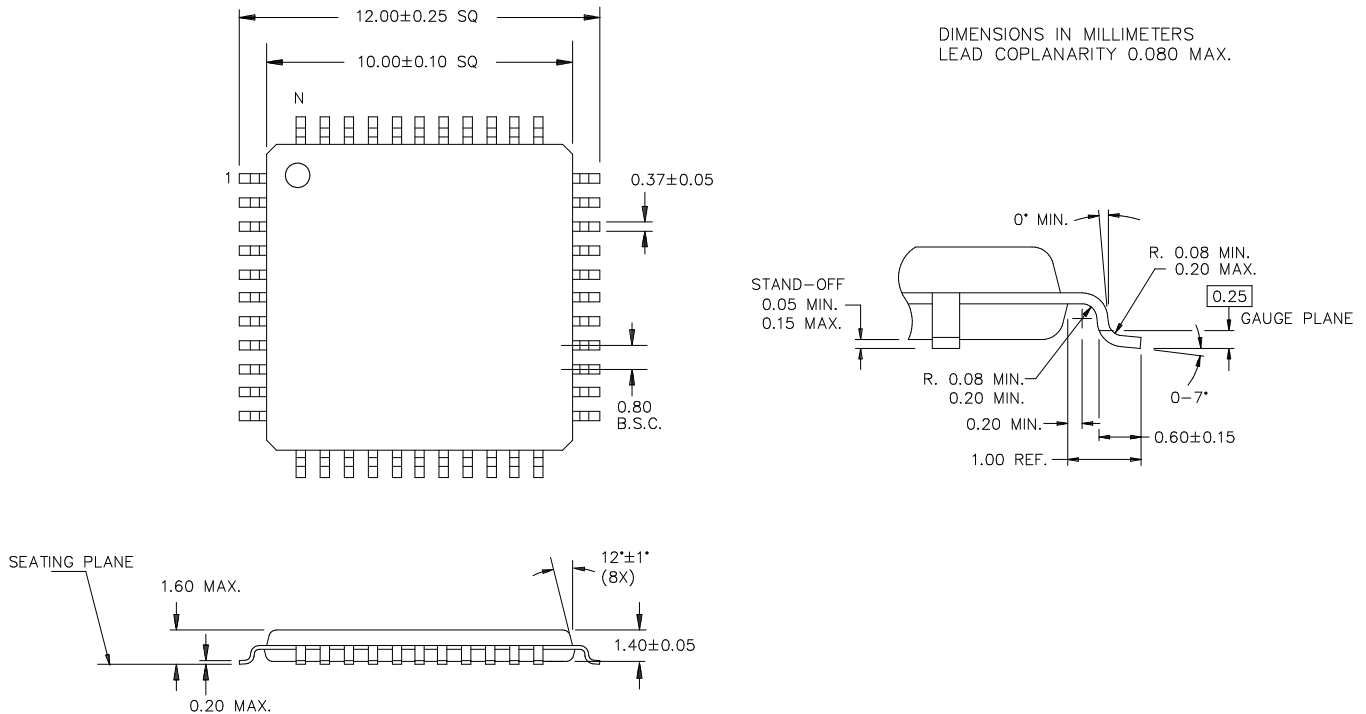
Document #: 38-00497-A

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LOG/iC is a trademark of Isdata Corporation.

CUPL is a trademark of Logical Devices Incorporated.

**Package Diagrams**
**44-Lead Thin Plastic Quad Flat Pack A44**

**44-Lead Plastic Leaded Chip Carrier J67**
