



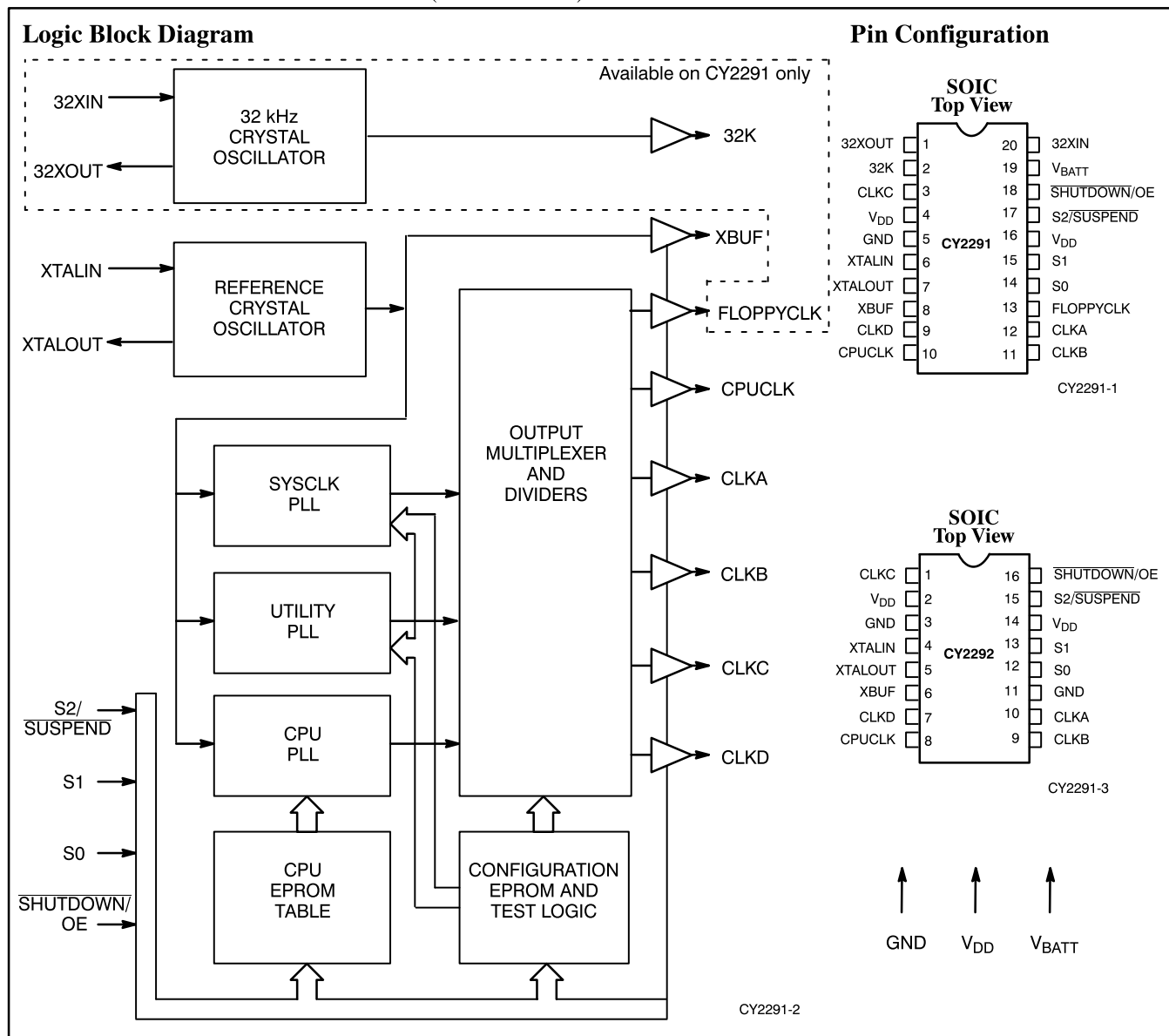
PRELIMINARY

CY2291
CY2292

Three-PLL Clock Generator

Features

- CY2291 pin compatible with ICD2028 (20-pin 300-mil SOIC). Upward compatible with 2023 (without serial channel)
- Three PLLs provide all necessary clocks for modern motherboards and other synchronous systems
- Eight outputs (2291), six outputs (2292)
- Four configurable clocks can choose 1 of 30 frequency options. These clocks can have any frequency between 200 kHz and 100 MHz (80 MHz at 3.3V)
- Low skew (500 ps) between related signals available on any or all configurable outputs
- Phase-locked loop oscillator input derived from external crystal (10 MHz to 25 MHz) or external reference clock (1 MHz to 30 MHz)
- Configuration includes permanent shutdown options for unused PLLs and configurable clocks
- Suspend feature allows shutting down a factory configurable set of PLLs and outputs with the S2 pin
- Smooth frequency transitions on CPUCLK from 8 MHz to 100 MHz (80 MHz at 3.3V)
- **SHUTDOWN/OE** pin three-states outputs and powers down part. OE available as an option. Power-down current draw of less than 50 μ A, plus 15 μ A max. for 32 kHz subsystem (CY2291 only)
- Factory EPROM programmable for fast turnaround times
- Weak pulldowns in outputs pull signals low when three-stated
- Compatible with 486 and Pentium™ processor clock specifications
- 3.3V or 5V operation
- Capable of withstanding greater than 2000V static discharge



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Pin Summary

Name	Pin Number (CY2291)	Pin Number (CY2292)	Description
32XOUT	1	—	32.768 kHz crystal feedback (CY2291 only)
32K	2	—	32.768 kHz output (always active if V_{BATT} is present) (CY2291 only)
CLKC	3	1	Configurable clock output C
V_{DD}	4	2	Voltage supply to I/O
GND	5	3	Ground
XTALIN ^[1]	6	4	Reference crystal input or external reference clock input
XTALOUT ^[1, 2]	7	5	Reference crystal feedback
XBUF	8	6	Buffered reference clock output
CLKD	9	7	Configurable clock output D
CPUCLK	10	8	CPU frequency clock output
CLKB	11	9	Configurable clock output B
CLKA	12	10	Configurable clock output A
FLOPPYCLK	13	—	Floppy clock output (24 or 32 MHz) (CY2291 only)
GND	—	11	Ground (CY2292 only)
S0	14	12	CPU clock select input, bit 0
S1	15	13	CPU clock select input, bit 1
V_{DD}	16	14	Analog voltage supply to core
S2/SUSPEND	17	15	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.
SHUTDOWN/OE	18	16	Places outputs in three-state ^[3] condition and shuts down chip when LOW. Optionally, only places outputs in three-state ^[3] condition and does not shut down chip when LOW.
V_{BATT}	19	—	Battery supply for 32.768 kHz circuit (CY2291 only)
32XIN	20	—	32.768 kHz crystal input (CY2291 only)

Operation

The CY2291 and CY2292 are a third-generation family of clock generators. The CY2291 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock generation needs of modern motherboards and other synchronous systems. The CY2292 differs from the CY2291 in that it comes in a 16-pin 150-mil SOIC package, and does not provide either the 32-kHz or FLOPPYCLK outputs.

Both parts provide a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs (CLKA–CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related^[4] frequencies will have low (≤ 500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2291 and CY2292 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing factory configuration for operation at non-standard frequencies. The reference oscillator has been designed for 10-MHz to 25-MHz crystals, providing additional

Notes:

- For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF.
- Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
- The CY2291 has weak pull-downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used. Customers using the 32-kHz oscillator on the CY2291 should connect a 10 M Ω resistor in parallel with the 32-kHz crystal.

Output Configuration

The CY2291 (and CY2292) have five (four) independent frequency sources on chip. These are the 32-kHz oscillator (not available on CY2292), the reference oscillator, and three Phase Locked Loops (PLLs). Each PLL has a specific function. The SYSCLK PLL drives the FLOPPYCLK output (not available on CY2292) and provides the fixed frequencies on the configurable outputs. The CPU PLL responds to the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The Utility PLL is available to provide miscellaneous frequencies not provided by the other frequency sources.

All configurations are factory programmable, providing short sample and production lead times. Please refer to the application note “Understanding the CY2291 and CY2292” for information on configuring the part.

- Please refer to applications note “Understanding the CY2291 and CY2292” for more information.

Power Saving Features

The $\overline{\text{SHUTDOWN/OE}}$ input three-states the outputs when pulled LOW (the 32-kHz clock output is not affected). If system shutdown is enabled (the default), a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 50 μA (plus 15 μA max. for the 32-kHz subsystem) and is typically 10 μA . After leaving shutdown mode, the PLLs will have to re-lock. All outputs except 32K have a weak pull-down so that the outputs do not float when three-stated.^[3]

The S2/SUSPEND input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs

and any of the outputs except 32K can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.^[3]

The CPUCLK can slew (transition) smoothly between 8 MHz and 100 MHz (80 MHz at 3.3V). This feature is extremely useful in “Green” PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium processor slewing requirements.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5V to +7.0V
DC Input Voltage -0.5V to +7.0V
Storage Temperature -65°C to +150°C

Max. Soldering Temperature (10 sec) 260°C
Junction Temperature 150°C
Package Power Dissipation 750 mW
Static Discharge Voltage >2000V
(per MIL-STD-883, Method 3015)

Operating Conditions^[5]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V (3.3V) operation	4.5 (3.0)	5.5 (3.6)	V
V_{BATT}	Battery Backup Voltage	2.0	5.5	V
T_A	Operating Temperature, Ambient	0	70	°C
C_{LOAD}	Max. Load Capacitance 5.0V (3.3V) Operation		25 (15)	pF
f_{REF}	Reference Frequency	10.0	25.0	MHz
	Reference Frequency, External Reference Clock ^[6, 7]	1	30	MHz

Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	$I_{OH} = 4.0 \text{ mA}$	2.4			V
V_{OL}	LOW-Level Output Voltage	$I_{OL} = 4.0 \text{ mA}$			0.4	V
V_{OH-32}	32.768 kHz HIGH-Level Output Voltage	$I_{OH} = 0.5 \text{ mA}$	$V_{BATT} - 0.5$			V
V_{OL-32}	32.768 kHz LOW-Level Output Voltage	$I_{OL} = 0.5 \text{ mA}$			0.4	V
V_{IH}	HIGH-Level Input Voltage ^[8]	Except crystal pins	2.0			V
V_{IL}	LOW-Level Input Voltage ^[8]	Except crystal pins			0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD} - 0.5V$		< 1	10	μA
I_{IL}	Input LOW Current	$V_{IN} = +0.5V$		< 1	10	μA
I_{OZ}	Output Leakage Current	Three-state outputs			250	μA
I_{DD}	V_{DD} Supply Current ^[9]	$V_{DD} = V_{DD} \text{ max.}, 5V (3.3V) \text{ operation}$		75(50)	100(65)	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode ^[9]	Shutdown active, excluding V_{BATT}		10	50	μA
I_{BATT}	V_{BATT} Power Supply Current	$V_{BATT} = 3.0V$		5	15	μA

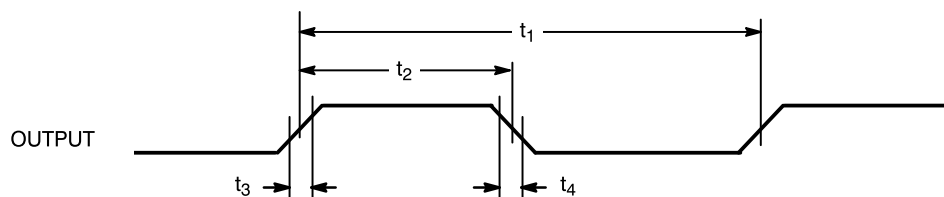
Notes:

- Electrical parameters are guaranteed with these operating conditions.
- External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
- Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
- Xtal inputs have CMOS thresholds.
- Load = Max., $V_{IN} = 0V$ or V_{DD} . Typical (-104) configuration, CPUCLK = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation):

$$I_{DD} = 10 + 0.06 \cdot (F_{CPLL} + F_{UPLL} + 2 \cdot F_{SPLL}) + 0.27 \cdot (F_{CLKA} + F_{CLKB} + F_{CLKC} + F_{CLKD} + F_{CPUCLK} + F_{FLOPPYCLK} + F_{XBUF})$$

Switching Characteristics^[10]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t ₁	Output Period	Clock output range, 5V operation	10 (100 MHz)		5000 (200 kHz)	ns
t ₁	Output Period	Clock output range, 3.3V operation	12.5 (80 MHz)		5000 (200 kHz)	ns
	Output Duty Cycle ^[11]	Duty cycle for outputs, defined as $t_2 \div t_1$ ^[12]	40%	50%	60%	
t ₃	Rise time	Output clock rise time ^[13]			5	ns
t ₄	Fall time	Output clock fall time ^[13]			4	ns
t ₅	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			15	ns
t ₆	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			15	ns
t ₇	Skew	Skew delay between any identical or related outputs ^[4, 12]		< 0.25	0.5	ns
t ₈	CPUCLK Slew	Frequency transition rate	2.0		20.0	MHz/ ms
t _{9A}	Clock Jitter ^[14]	Peak-to-peak period jitter (t _{9A} max. – t _{9A} min.), % of clock period (f _{OUT} ≤ 16 MHz)		< 2	5	%
t _{9B}	Clock Jitter ^[14]	Peak-to-peak period jitter (16 MHz ≤ f _{OUT} ≤ 50 MHz)			700	ps
t _{9C}	Clock Jitter ^[14]	Peak-to-peak period jitter (f _{OUT} ≥ 50 MHz)			500	ps
t ₁₀	Lock Time	Time for VCO to settle between changes		25	50	ms
	Slew Limits	CPU PLL Slew Limits	8		100 (5V) 80 (3.3V)	MHz

Switching Waveforms
All Outputs, Duty Cycle and Rise/Fall Time


CY2291-4

Notes:

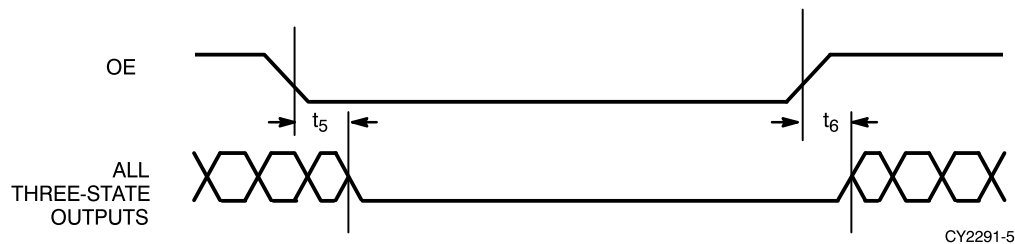
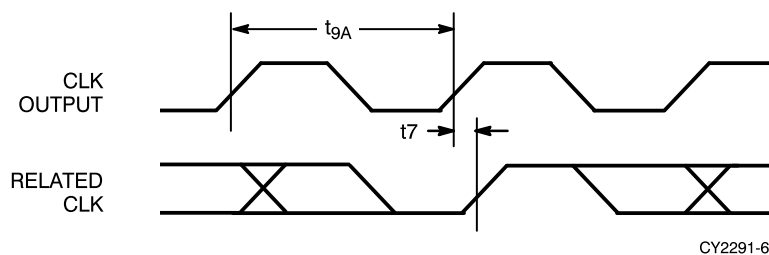
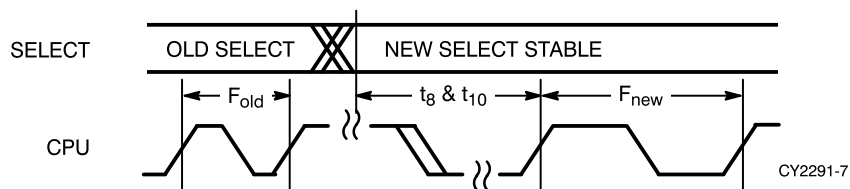
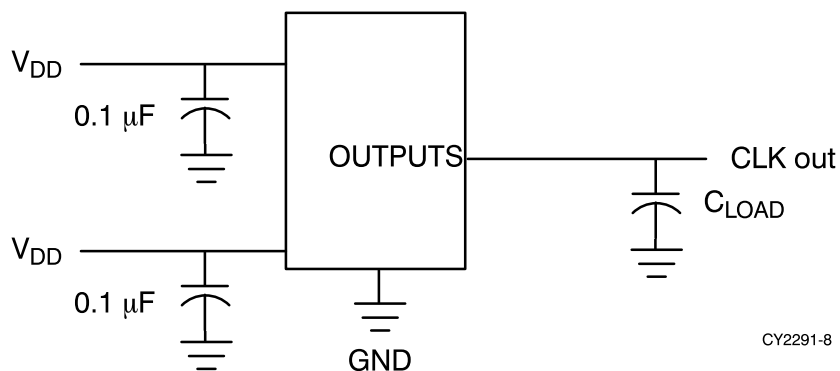
10. Guaranteed by design, not 100% tested.

11. XBUF duty cycle depends on XTALIN duty cycle.

12. Measured at 1.4V.

13. Measured between 0.4V and 2.4V.

14. For more information on jitter, please refer to the application note: "Jitter in PLL-Based Systems."

Switching Waveforms (continued)
Output Three-State Timing^[3]

CLK Outputs Jitter and Skew

CPU Frequency Change

Test Circuit

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2291SC-XXX	S5	20-Lead (300-Mil) SOIC	Commercial ^[15]
CY2292SC-XXX	S16	16-Lead (150-Mil) SOIC	Commercial

Note:
15. 0°C to +70°C

Document #: 38-00410



CY2291/2 CUSTOM CONFIGURATION REQUEST FORM

Company _____ Engineer _____ FAE/Sales _____
Phone # _____ Fax # _____ Date _____

CIRCLE ONE **CY2291** **CY2292**

The CY2291 and CY2292 are the industry's most flexible frequency synthesizers, offering a high degree of configurability due to their unique internal factory-programmable EPROM array. Of the CY2291/2's outputs, six (five on the CY2292) may be defined within the scope of the PLL frequencies and divider criteria described in the following. The process may require several iterations to achieve the desired frequencies. Shaded areas are for Cypress use only. Contact your local Cypress representative for assistance.

1. **OPERATING VOLTAGE** (Circle one) **3.3V** **5.0V**
2. **INPUT REFERENCE FREQUENCY** (Circle one) **Crystal** **External Clock** **14.31818 MHz** (Default)
If a different reference is required, specify the frequency in the box to the right
(must be between 10 MHz and 25 MHz for crystal, 1 MHz and 30 MHz for external clock):
3. **CPU-PLL FREQUENCIES** ("Off" is a valid selection for any address and will automatically be entered for blanks.)

Select	Requested	Actual
0 0 0		
0 0 1		
0 1 0		
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

Range: 8–100 MHz at 5V; 8–80 MHz at 3.3V

If the Suspend Option is specified in #7 below, the Select MSB (S2) serves a dual function as both the MSB CPU address and as the Suspend select pin. The CPU frequencies specified for addresses 000–011 will be active unless the CPU-PLL is shut down during the suspend mode (CPU-PLL is circled in #7). Also, any outputs derived from a non-suspended CPU-PLL (assigned in #5 as options 5–8) that are not circled in #7 will remain active during the suspend mode.

4. **UTILITY-PLL AND SYSTEM-PLL FREQUENCIES** ("Off" is a valid frequency selection for either PLL.)
To minimize harmonic effects, avoid setting any PLL to an equal or multiple frequency of another PLL.

	Requested	Actual
U-PLL		

Range: 8–100 MHz at 5V; 8–80 MHz at 3.3V

	Requested	Actual
S-PLL		

Range: 8–100 MHz at 5V; 8–80 MHz at 3.3V
Default = 96 MHz at 5V; 48 MHz at 3.3V

5. **OUTPUT CONFIGURATION** ("Off" is a valid selection for any output and will automatically be entered for blanks.)
Assign by number from the Output Options Table below and fill in the Frequency column as a double-check.

Output Options Table

1. Ref	6. CPLL/2	11. UPLL/4	16. SPLL/4	21. SPLL/12	26. SPLL/40
2. Ref/2	7. CPLL/4	12. UPLL/8	17. SPLL/5	22. SPLL/13	27. SPLL/48
3. Ref/4	8. CPLL/8	13. SPLL	18. SPLL/6	23. SPLL/20	28. SPLL/52
4. Ref/8	9. UPLL	14. SPLL/2	19. SPLL/8	24. SPLL/24	29. SPLL/96
5. CPLL	10. UPLL/2	15. SPLL/3	20. SPLL/10	25. SPLL/26	30. SPLL/104

	Option	Frequency
32K (Fixed 32 kHz)	—	32.768 kHz
FLOPPYCLK (Options 14–16, Off)		
XBUF (Option 1 only)	1	
CPUCLK (Options 5–7, Off)		

32K and FLOPPYCLK are not available on the CY2292.

	Option	Frequency
CLKA (Options 1–30, Off)		
CLKB (Options 1–30, Off)		
CLKC (Options 1–30, Off)		
CLKD (Options 1–30, Off)		

For CLKD only: option #4 (Ref/8) is replaced with Ref/3.

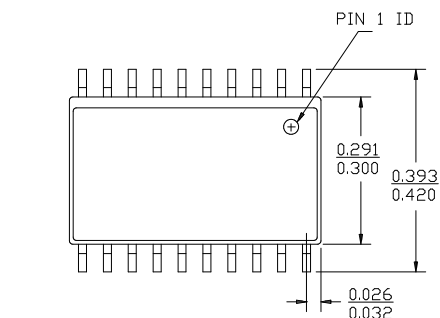
6. **SHUTDOWN OPTION** (Circle Yes or No) **Yes** **No**
7. **SUSPEND OPTION** (Circle Yes or No) **Yes** **No**

IF SUSPEND = "Yes": Circle each resource to be shut down when the Suspend mode is active (S2=0). Note that suspending a PLL automatically suspends its outputs.

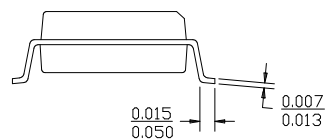
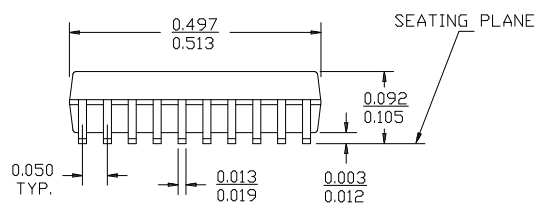
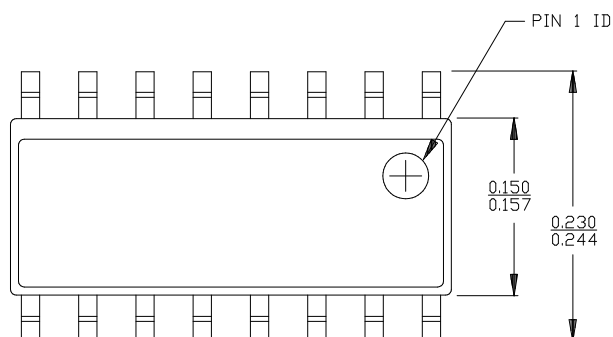
CPU-PLL	XBUF	CLKA
UTIL-PLL	CPUCLK	CLKB
SYS-PLL	FLOPPYCLK	CLKC
		CLKD

FOR CYPRESS USE ONLY (Shaded areas above and below)

Customer Configuration	Marking
Date	Quantity

Package Diagrams
20-Lead (300-Mil) Molded SOIC S5


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.


16-Lead (150-Mil) Molded SOIC S16


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

