



PRELIMINARY

CY2255

Pentium™ Processor Compatible Clock Synthesizer/Driver for OPTi Viper™ Chipset

Features

- Multiple clock outputs to meet requirements of OPTi Viper™ chipset
 - Five CPU clocks @ 66.66 MHz, 60 MHz, and 50 MHz, pin selectable
 - One Early clock, leads CPU clocks by 2 to 5 ns
 - Six PCI clocks (CPUCLK/2)
 - Two Ref. clocks @ 14.318 MHz
 - Ref. 14.318 MHz Xtal oscillator input
- CPU clock jitter ≤ 250 ps cycle-to-cycle
- Low skew outputs
 - ≤ 250 ps between CPU clocks
 - ≤ 500 ps between PCI clocks
 - ≤ 750 ps between CPU clocks and PCI clocks

- Freq. stability = 0.01 % (max.)
- Output duty cycle 40% min. to 60% max.
- Test mode support
- 3.3V operation
- CMOS technology

Functional Description

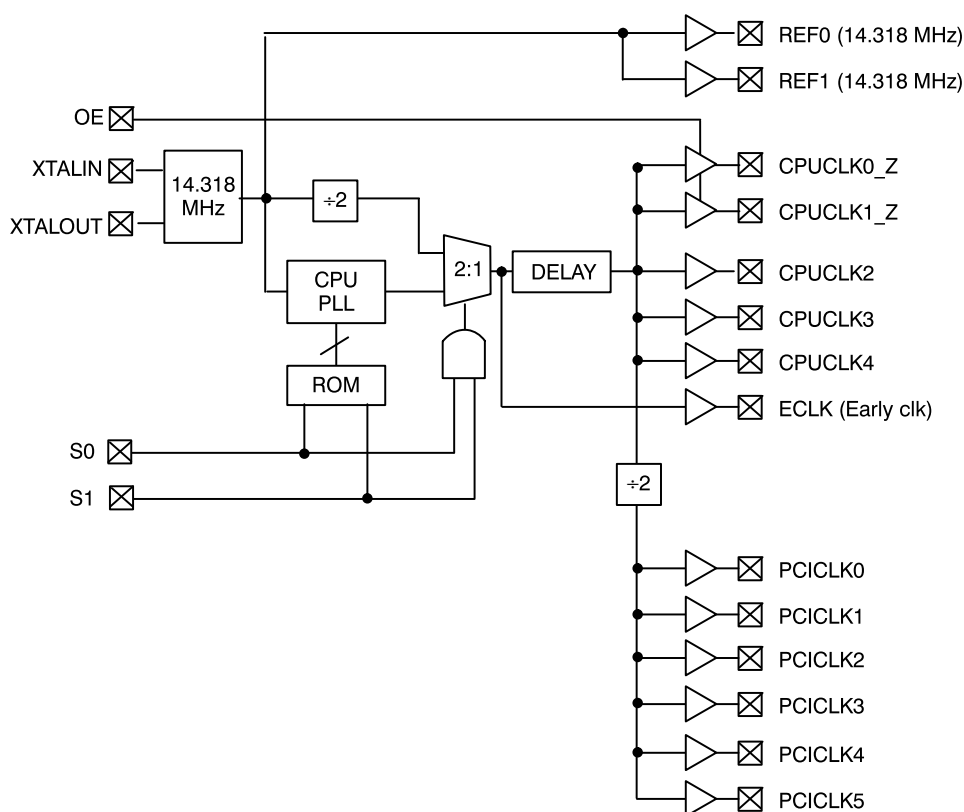
The CY2255 is a Clock Synthesizer/Driver chip with multiple output clocks, for the OPTi Viper™ chipset. The CY2255 outputs six CPU clocks at pin-selectable frequencies of 50, 60, and 66.66 MHz. One CPU clock leads the rest by 2 to 5 ns, and is denoted as Early Clock (ECLK). Two of the remaining five CPU clocks are three-stateable, controlled by an active-HIGH Output Enable (OE) pin. The

CY2255 has six synchronous PCI clock outputs, each having a frequency of CPUCLK/2. The CY2255 also outputs two copies of the Reference clock.

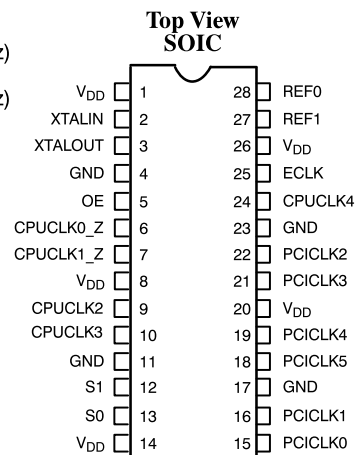
The CY2255 has low-skew outputs (≤ 250 ps between the CPU Clocks, ≤ 500 ps between the PCI Clocks). In addition, the CY2255 CPU clock outputs have less than 250 ps cycle-to-cycle RMS jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of a Pentium™ processor-based system.

The CY2255 accepts a 14.318 MHz reference signal as its input, and uses it to generate the CPU and PCI clocks from a single PLL. The CY2255 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration



2255-2

2255-1

Pentium is a trademark of Intel Corporation.
Viper is a trademark of OPTi.

Pin Summary

Name	Number	Description
V _{DD}	1	Digital voltage supply
XTALIN ^[1]	2	Reference crystal input
XTALOUT ^[1]	3	Reference crystal feedback
GND	4	Ground
OE	5	Output Enable, Active HIGH
CPUCLK0_Z	6	CPU clock output, three-stateable by OE
CPUCLK1_Z	7	CPU clock output, three-stateable by OE
V _{DD}	8	Digital voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
GND	11	Ground
S1	12	CPU clock select input, bit 1
S0	13	CPU clock select input, bit 0
V _{DD}	14	Digital voltage supply
PCICLK0	15	PCI clock output
PCICLK1	16	PCI clock output
GND	17	Ground
PCICLK5	18	PCI clock output
PCICLK4	19	PCI clock output
V _{DD}	20	Digital voltage supply
PCICLK3	21	PCI clock output
PCICLK2	22	PCI clock output
GND	23	Ground
CPUCLK4	24	CPU clock output
ECLK	25	Early clock output, leads CPU clocks by 2 to 5 ns
V _{DD}	26	Digital voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:

- For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.



Function Table

OE	S0	S1	XTALIN Input	CPUCLK_Z [0:1]	ECLK, CPUCLK [2:4]	PCICLK	Ref. Clock Output
0	0	0	14.318 MHz	High-Z	50 MHz	CPUCLK/2	14.318 MHz
0	0	1	14.318 MHz	High-Z	60 MHz	CPUCLK/2	14.318 MHz
0	1	0	14.318 MHz	High-Z	66.66 MHz	CPUCLK/2	14.318 MHz
0	1	1	TCLK ^[2]	High-Z	TCLK/2	TCLK/4	TCLK
1	0	0	14.318 MHz	50 MHz	50 MHz	CPUCLK/2	14.318 MHz
1	0	1	14.318 MHz	60 MHz	60 MHz	CPUCLK/2	14.318 MHz
1	1	0	14.318 MHz	66.66 MHz	66.66 MHz	CPUCLK/2	14.318 MHz
1	1	1	TCLK ^[2]	TCLK/2	TCLK/2	TCLK/4	TCLK

PCI/CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V
Input Voltage -0.5V to $V_{DD}+0.5$
Storage Temperature (Non-Condensing) ... -65°C to +150°C
Max. Soldering Temperature (10 sec) +260°C
Junction Temperature +150°C

Static Discharge Voltage >2000V
(per MIL-STD-883, Method 3015)

Operating Range

Ambient Temperature	V_{DD}
$0^{\circ}\text{C} \leq T_{\text{AMBIENT}} \leq 70^{\circ}\text{C}$	$3.3\text{V} \pm 5\%$

Operating Conditions^[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK REF0 REF1		20 30 30 15	pF
$f_{(\text{REF})}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:

- TCLK is a test clock on the XTALIN input during test mode.
- Electrical parameters are guaranteed with these operating conditions.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V _{OH}	HIGH-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OH} = 6 mA	CPUCLK, ECLK	2.4		V
			I _{OH} = 12 mA	PCICLK, REF0			
			I _{OH} = 8 mA	REF1			
V _{OL}	LOW-level Output Voltage	V _{DD} = V _{DD} Min.	I _{OL} = 6 mA	CPUCLK, ECLK		0.4	V
			I _{OL} = 12 mA	PCICLK, REF0			
			I _{OL} = 8 mA	REF1			
V _{IH}	HIGH-level Input Voltage	Except Crystal Inputs			2.0		V
V _{IL}	LOW-level Input Voltage	Except Crystal Inputs				0.8	V
I _{IH}	Input HIGH Current	V _{IH} = V _{DD} - 0.5V			-5	+5	μA
I _{IL}	Input LOW Current	V _{IL} = 0.5V			-5	+5	μA
I _{OZ}	Output Leakage Current	Three-state outputs			-10	+10	μA
I _{DD}	Power Supply Current	V _{DD} = 3.465, V _{IN} = 0 or V _{DD}				90	mA

Switching Characteristics^[4]

Parameter	Output	Name	Description	Min.	Max.	Unit
t ₁	All	Output Duty Cycle ^[5]	t ₁ = t _{1A} ÷ t _{1B}	40%	60%	
t ₂	CPUCLK, ECLK, PCICLK	Output Slew Rate	0.4–2.4V	1		V/ns
t ₃	REF0	Rise Time	20% – 80% of V _{DD}		2.5	ns
t ₃	REF1	Rise Time	20% – 80% of V _{DD}		4	ns
t ₄	REF0	Fall Time	20% – 80% of V _{DD}		2.5	ns
t ₄	REF1	Fall Time	20% – 80% of V _{DD}		4	ns
t ₅	CPUCLK	CPU Skew	CPU-CPU clock skew		250	ps
t ₆	ECLK, CPUCLK	ECLK Skew	Early-CPU clock skew (ECLK leads)	2	5	ns
t ₇	PCICLK	PCI Skew	PCI-PCI clock skew		500	ps
t ₈	CPUCLK, PCICLK	CPU-PCI Skew	CPU to PCI clock skew (CPU leads)		750	ps
t ₉	CPUCLK	Cycle-Cycle Clock Jitter	Clock jitter		250	ps

Notes:

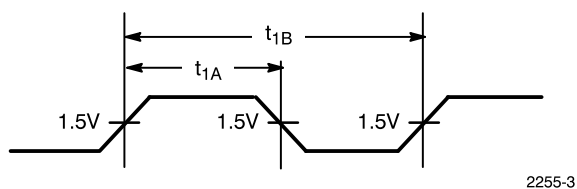
4. All parameters specified with outputs fully loaded.

5. Duty cycle is measured at 1.5V.

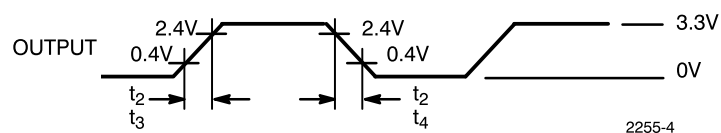


Switching Waveforms

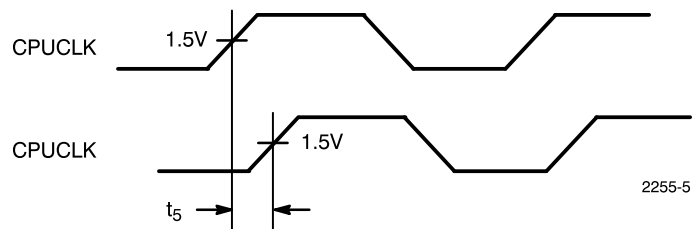
Duty Cycle Timing



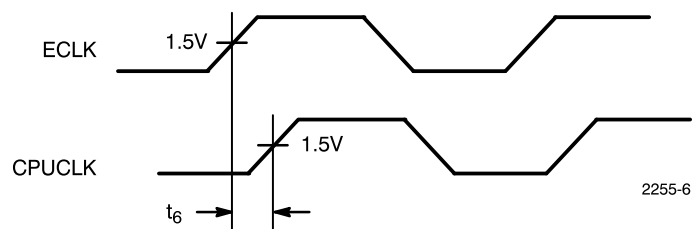
All Outputs Rise/Fall Time



CPU-CPU Clock Skew



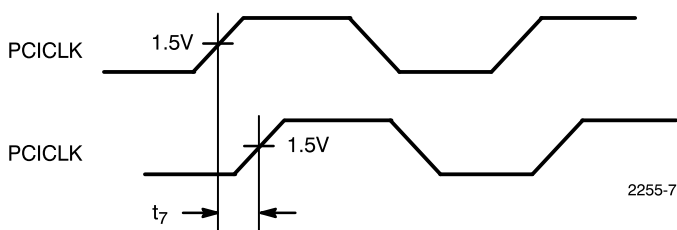
Early-CPU Clock Skew



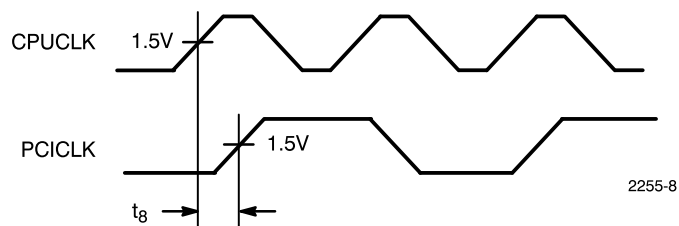


Switching Waveforms (continued)

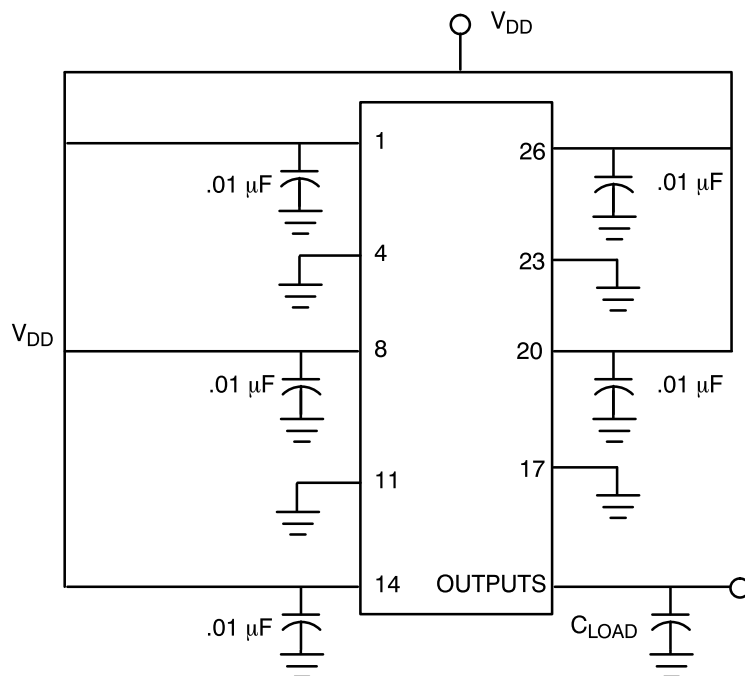
PCI-PCI Clock Skew



CPU-PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.



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Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2255	S21	28-Pin SOIC	Commercial

Document #: 38-00442

Package Diagram

28-Lead (300-Mil) Molded SOIC S21

