Am29334

Four-Port, Dual-Access Register File

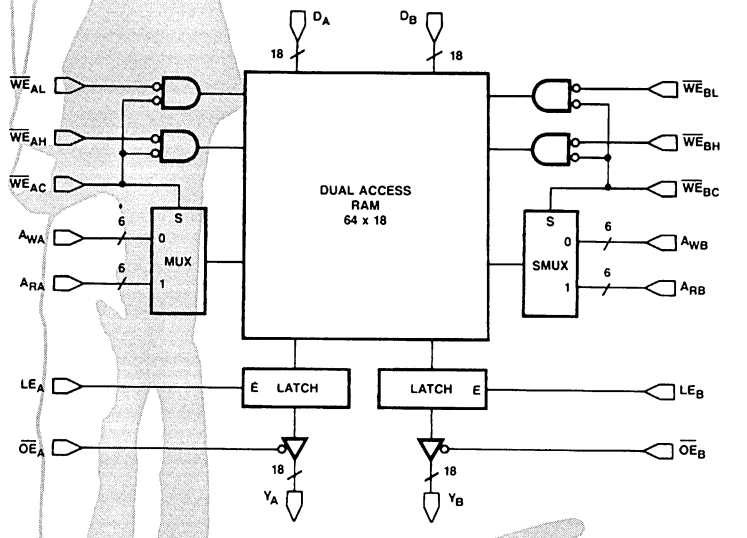
DISTINCTIVE CHARACTERISTICS

- **Fast**
  With an access time of 24ns, the Am29334 supports 80-90ns microcycle time when used with the Am29300 Family for 32-bit systems.
- **64 x 18 Bits Wide Register File**
  The Am29334 is a high-performance, high-speed, dual-access RAM with two READ ports and two WRITE ports.
- **Cascadable**
  The Am29334 is cascadable to support either wider word widths, deeper register files, or both.
- **Simplified Timing Control**
  Control for write enable timing and for on-chip read/write address multiplexer are derived from a single-phase clock input.
- **Byte Parity Storage**
  Width of 18 bits facilitates byte parity storage for each port and provides consistency with the Am29332 32-bit ALU.
- **Byte Write Capability**
  Individual byte-write enables allows byte or full word write.

GENERAL DESCRIPTION

The Am29334 is a 64-word deep and 18-bit wide dual-access register file designed to support other members of the Am29300 Family by providing high-speed storage. It has two write and two read ports for data and four 6-bit address ports. Two address ports are associated with each pair of read and write data ports, one to read data and the other to write. The device is capable of performing two reads and two writes in one cycle. The 18-bit wide register file allows storage of byte parity to support parity check and generate in the Am29332 32-bit ALU. Independent control for each read and write data port allows the Am29334 to be used as a high-speed shared memory or as a mailbox for a multiprocessor system. The device is designed with an access time of 24ns. It is housed in a 120 lead pin grid array package.

BLOCK DIAGRAM

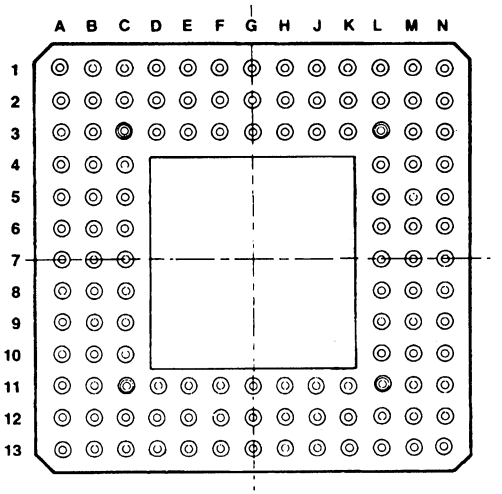


Order # 05731C

RELATED PRODUCTS

Part No.	Description
Am29323	32 x 32 Parallel Multiplier
Am29325	32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU

CONNECTION DIAGRAM



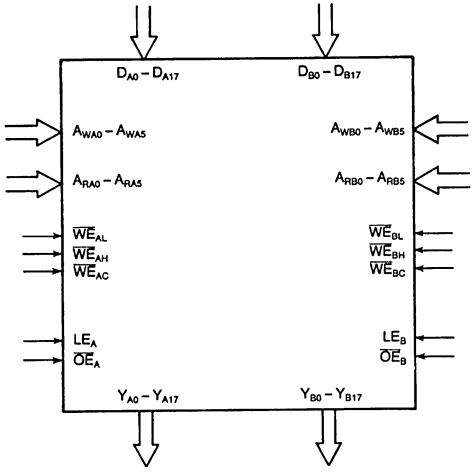
CD009170

TABLE OF INTERCONNECTIONS

PIN NAME	PAD NUMBER	PIN NUMBER	PIN NAME	PAD NUMBER	PIN NUMBER	PIN NAME	PAD NUMBER	PIN NUMBER	PIN NAME	PAD NUMBER	PIN NUMBER
A_{WA2}	1	A-1	A_{WB1}	31	N-13	A_{RA2}	61	B-1	A_{RB1}	91	M-13
A_{WA1}	2	C-1	A_{WB0}	32	L-12	A_{RA1}	62	C-2	A_{RB0}	92	K-11
A_{WA0}	3	D-3	D_{B17}	33	K-12	A_{RA0}	63	D-2	D_{B16}	93	K-13
D_{A0}	4	D-1	D_{B15}	34	H-11	D_{A1}	64	E-3	D_{B14}	94	H-13
D_{A2}	5	E-1	D_{B13}	35	L-13	D_{A3}	65	E-2	D_{B12}	95	H-12
D_{A4}	6	F-1	D_{B11}	36	G-12	D_{A5}	66	F-2	D_{B10}	96	G-13
D_{A6}	7	G-3	–	37	–	D_{A7}	67	G-2	–	97	–
GND	8	F-3	GND	38	J-11, J-12, J-13	V_{CC}	68	H-3	V_{CC}	98	E-11, E-12, E-13
D_{A8}	9	G-1	–	39	–	D_{A9}	69	H-1	–	99	–
D_{A10}	10	H-2	D_{B9}	40	G-11	D_{A11}	70	J-3	D_{B8}	100	F-11
D_{A12}	11	J-1	D_{B7}	41	C-13	D_{A13}	71	J-2	D_{B6}	101	F-13
D_{A14}	12	K-3	D_{B5}	42	F-12	D_{A15}	72	K-2	D_{B4}	102	D-11
D_{A16}	13	K-1	D_{B3}	43	D-12	D_{A17}	73	L-3	D_{B2}	103	D-13
LE_A	14	L-1	D_{B1}	44	C-11	A_{RA5}	74	L-2	D_{B0}	104	C-12
A_{WA5}	15	M-2	LE_B	45	B-12	$\overline{WE}_{AC}$	75	M-1	A_{RB5}	105	B-13
$\overline{WE}_{AL}$	16	N-1	A_{WB5}	46	A-13	$\overline{WE}_{AH}$	76	N-2	$\overline{WE}_{BC}$	106	A-12
A_{WB4}	17	N-3	$\overline{WE}_{BL}$	47	A-11	A_{RB4}	77	M-3	$\overline{WE}_{BH}$	107	B-11
Y_{A0}	18	L-4	Y_{B17}	48	C-10	Y_{A1}	78	M-4	Y_{B16}	108	B-10
Y_{A2}	19	N-4	Y_{B15}	49	A-10	Y_{A3}	79	L-5	Y_{B14}	109	C-9
GND_A	20	N-5	GND_A	50	A-9	Y_{A4}	80	M-5	Y_{B13}	110	B-9
Y_{A5}	21	N-6	Y_{B12}	51	A-8	Y_{A6}	81	M-6	Y_{B11}	111	B-8
Y_{A7}	22	L-7	Y_{B10}	52	C-7	Y_{A8}	82	M-7	Y_{B9}	112	B-7
$\overline{OE}_A$	23	L-6	$\overline{OE}_B$	53	C-8	V_{CCA}	83	L-8	V_{CCA}	113	C-6
Y_{A9}	24	N-7	Y_{B8}	54	A-7	Y_{A10}	84	N-8	Y_{B7}	114	A-6
Y_{A11}	25	M-8	Y_{B6}	55	B-6	Y_{A12}	85	L-9	Y_{B5}	115	C-5
GND_A	26	N-9	GND_A	56	A-5	Y_{A13}	86	M-9	Y_{B4}	116	B-5
Y_{A14}	27	L-10	Y_{B3}	57	C-4	Y_{A15}	87	M-10	Y_{B2}	117	B-4
Y_{A16}	28	N-10	Y_{B1}	58	A-4	Y_{A17}	88	L-11	Y_{B0}	118	C-3
A_{WB3}	29	N-11	A_{WA4}	59	A-3	A_{RB3}	89	M-11	A_{RA4}	119	B-3
A_{WB2}	30	M-12	A_{WA3}	60	B-2	A_{RB2}	90	N-12	A_{RA3}	120	A-2

Notes:
1. V_{CC} and GND are power for internal ECL chip logic.
2. V_{CCA} and GND_A are power for output TTL buffers.
3. Pins E-1, E-12 and E-13 are physically shorted together in the package.
4. Pins J-11, J-12 and J-13 are physically shorted together in the package.

LOGIC SYMBOL



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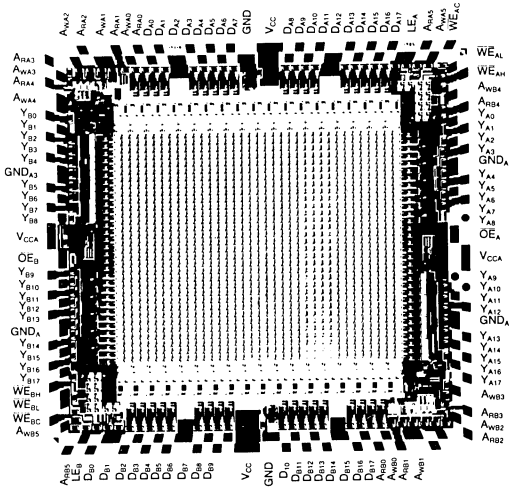
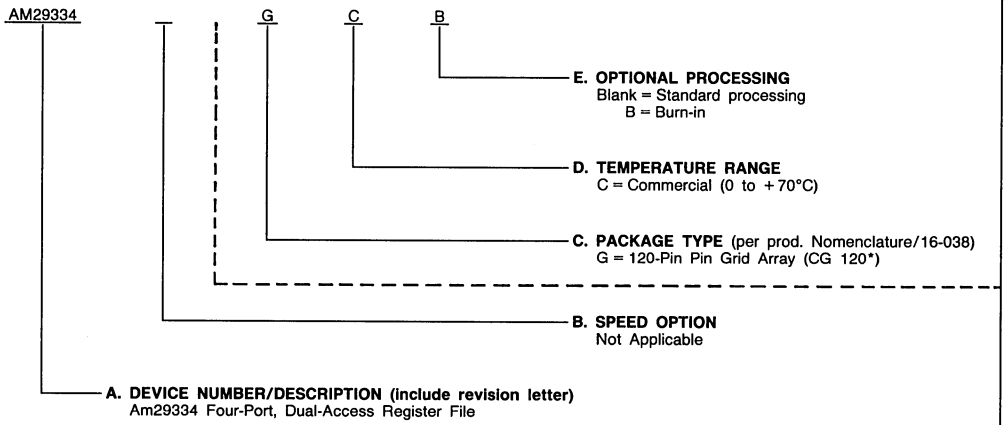
METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



* Preliminary. Subject to Change.

Valid Combinations	
AM29334	GC, GCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_{RA0} - A_{RA5}$ Addresses (Inputs, Active HIGH)
The 6-bit field presented at the AR_A inputs, selects one of 64 memory words for presentation to the Y_A Data Latch.

$A_{RB0} - A_{RB5}$ Addresses (Inputs, Active HIGH)
The six-bit field presented at the AR_B inputs, selects one of 64 memory words for presentation to the Y_B Data Latch.

$Y_{A0} - Y_{A17}$ Data Latch (Outputs, Three-State)
The 18-bit Y_A Data Latch Outputs.

$Y_{B0} - Y_{B17}$ Data Latch (Outputs, Three-State)
The 18-bit Y_B Data Latch Outputs.

$A_{WA0} - A_{WA5}$ Addresses (Inputs, Active HIGH)
The six-bit field presented at the AW_A inputs, selects one of 64 words for writing new data from the D_A inputs.

$A_{WB0} - A_{WB5}$ Addresses (Inputs, Active HIGH)
The six-bit field presented at the AW_B inputs, selects one of 64 words for writing new data from the D_B inputs.

$D_{A0} - D_{A17}$ Data (Inputs, Active HIGH)
New data is written into the word, selected by the AW_A address inputs, through these inputs.

$D_{B0} - D_{B17}$ Data (Inputs, Active HIGH)
New data is written into the word, selected by the AW_B address inputs, through these inputs.

LE_A Y_A Data Latch Enable (Input)
The LE_A input controls the Latch for the Y_A output port. When LE_A is HIGH, the latch is open (transparent), and data from the RAM, as selected by the AR_A address inputs, is present at the Y_A outputs. When LE_A is LOW, the Latch is closed and it retains the last data read from the RAM selected by the AR_A address inputs.

LE_B Y_B Data Latch Enable (Input)
The LE_B input controls the Latch for the Y_B output port. When LE_B is HIGH, the Latch is open (transparent), and data from the RAM, as selected by the AR_B address inputs, is present at the Y_B outputs. When LE_B is LOW, the Latch is closed and it retains the last data read from the RAM selected by the AR_B address inputs.

$\overline{OE}_A$ Y_A Output Enable (Input, Active LOW)
When $\overline{OE}_A$ is LOW, data in the Y_A Data Latch is present at the Y_A outputs. If $\overline{OE}_A$ is HIGH, Y_A outputs are in the high-impedance (off) state.

$\overline{OE}_B$ Y_B Output Enable (Input, Active LOW)
When $\overline{OE}_B$ is LOW, data in the Y_B Data Latch is present at the Y_B outputs. If $\overline{OE}_B$ is HIGH, Y_B outputs are in the high-impedance (off) state.

$\overline{WE}_{AC}$ Write Enable (Input, Active LOW)
When $\overline{WE}_{AC}$ is LOW together with $\overline{WE}_{AH}$ and $\overline{WE}_{AL}$, new data is written into the word selected by the AW_A address inputs. When $\overline{WE}_{AC}$ is HIGH, no data is written into the RAM through the A port.

$\overline{WE}_{BC}$ Write Enable (Input, Active LOW)
When $\overline{WE}_{BC}$ is LOW together with $\overline{WE}_{BH}$ and $\overline{WE}_{BL}$, new data is written into the word selected by the AW_B address inputs. When $\overline{WE}_{BC}$ is HIGH, no data is written into the RAM through the B port.

$\overline{WE}_{AH}$ High-Byte Write Enable (Input, Active LOW)
When $\overline{WE}_{AH}$ is LOW together with $\overline{WE}_{AC}$, new data is written into the high byte of the word selected by the AW_A address inputs. When $\overline{WE}_{AH}$ is HIGH, no data is written into the high byte of the word selected by the AW_A address inputs.

$\overline{WE}_{BH}$ High-Byte Write Enable (Input, Active LOW)
When $\overline{WE}_{BH}$ is LOW together with $\overline{WE}_{BC}$, new data is written into the high byte of the word selected by the AW_B address inputs. When $\overline{WE}_{BH}$ is HIGH, no data is written into the high byte of the word selected by the AW_B address inputs.

$\overline{WE}_{AL}$ Low-Byte Write Enable (Input, Active LOW)
When $\overline{WE}_{AL}$ is LOW together with $\overline{WE}_{AC}$, new data is written into the low byte of the word selected by the AW_A address inputs. When $\overline{WE}_{AL}$ is HIGH, no data is written into the low byte of the word selected by the AW_A address inputs.

$\overline{WE}_{BL}$ Low-Byte Write Enable (Input, Active LOW)
When $\overline{WE}_{BL}$ is LOW together with $\overline{WE}_{BC}$, new data is written into the low byte of the word selected by the AW_B address inputs. When $\overline{WE}_{BL}$ is HIGH, no data is written into the low byte of the word selected by the AW_B address inputs.

FUNCTIONAL DESCRIPTION

The part has two read ports ($Y_{A0} - Y_{A17}$, $Y_{B0} - Y_{B17}$), two write ports ($D_{A0} - D_{A17}$, $D_{B0} - D_{B17}$), four addresses ($A_{RA0} - A_{RA5}$, $A_{WA0} - A_{WA5}$, $A_{RB0} - A_{RB5}$, $A_{WB0} - A_{WB5}$), two latch enables (LE_A, LE_B), two output enables ($\overline{OE}_A$, $\overline{OE}_B$), and six write enables $\overline{WE}_{AC}$, $\overline{WE}_{AL}$, $\overline{WE}_{AH}$, $\overline{WE}_{BC}$, $\overline{WE}_{BL}$, $\overline{WE}_{BH}$) that allow writing of data into one or both bytes of a word. The separate read and write addresses facilitate creation of three- and four-address architectures and allow address set-up and RAM access to overlap.

Since the A and B sides are identical, only operation of the A side is described. The address multiplexer provides the RAM with the address A_{RA} when $\overline{WE}_{AC}$ = HIGH and with the address A_{WA} when $\overline{WE}_{AC}$ = LOW. Internally the part is designed so that there is no race condition between the write address and the write enable. In most cases $\overline{WE}_{AC}$ and LE_A will be connected to the clock as shown in Figure 2 so that reading will take place in the first part of a clock cycle and writing in the last part. The latch at the output of the RAM is transparent when LE_A = HIGH and retains the data when LE_A = LOW. The latch has a three-state output Y_A controlled by $\overline{OE}_A$. Each word is split into two bytes of nine bits that can be individually written. The low byte covers bits 0 through 8 and the high byte covers bits 9 through 17. One or both bytes of the data at D_A are written into the location given by A_{WA} when the common write enable ($\overline{WE}_{AC}$) and the appropriate byte write enables ($\overline{WE}_{AL}$ and $\overline{WE}_{AH}$) are active. Two special cases arise. First, if a location is written into and read at the same time, the value read is the value being written. Second, if a location is written into from both the A side and the B side, the value written is undefined, but the operation is not harmful.

Extension To Four Read Ports and Two Write Ports

A RAM with four read ports and two write ports can be made by using two dual access RAMs and connecting each of the write ports, write addresses, and write enables in parallel for the two devices. As an example, this RAM may provide data storage for a data ALU and an address adder as shown in Figure 3. A location should not be read before it has been written into for the first time as the contents of the two dual access RAMs are likely to be different upon power-up.

32 Words x 36 Bits Single Access Ram

It is possible to convert the 64 words x 18 bits dual access RAM into a 32 word x 36 bit single access RAM by storing the upper half of the 36 bits in the upper half of the 64 words and address these from the A side and storing the lower half of the 36 bits in the lower half of the 64 words and address these from the B side. This arrangement, which is shown in Figure 4, does not change the capacity of the RAM, but the dual access is lost.

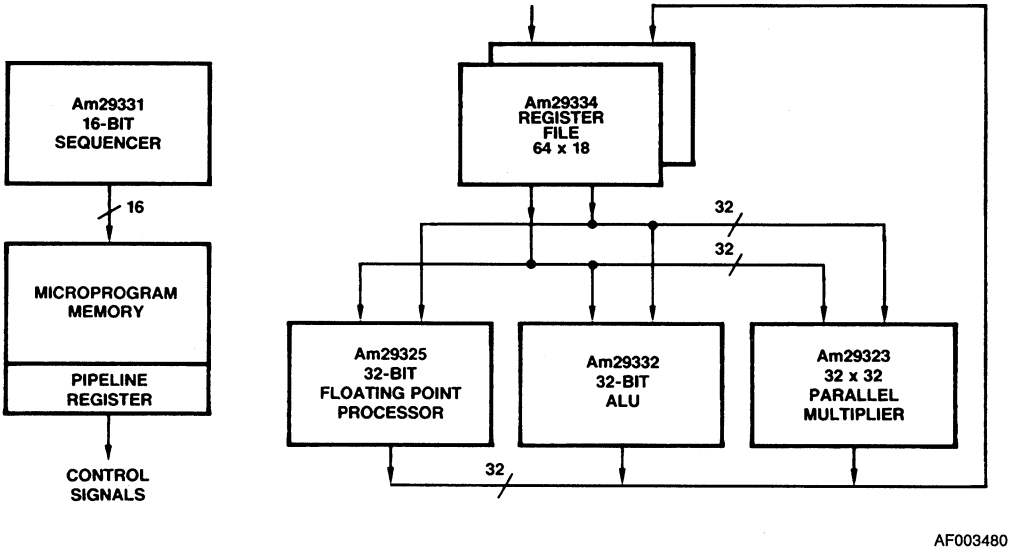


Figure 1. Am29300 Family High Performance System Block Diagram

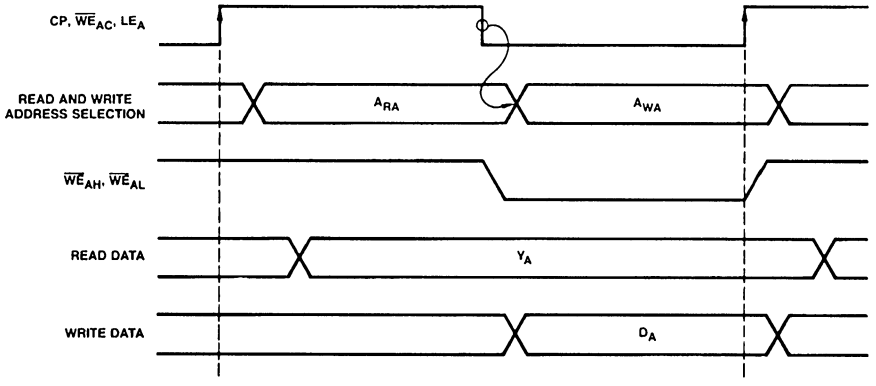


Figure 2. Read through Y_A and Write through D_A in a Single Cycle (Two Bytes)

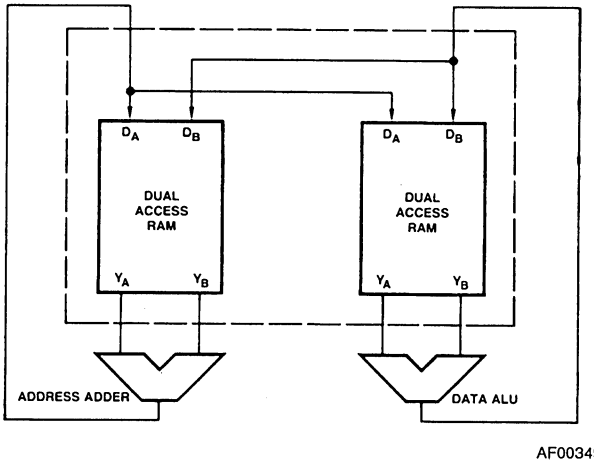


Figure 3. RAM with 4 Read Ports and 2 Write Ports

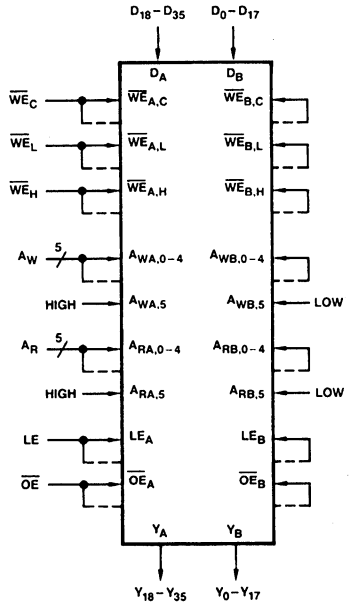


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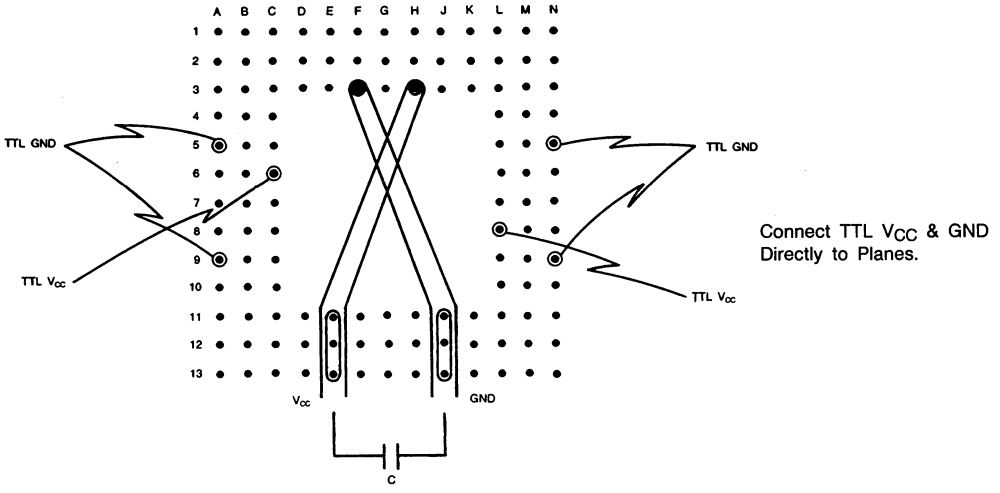
Figure 4. 32 x 36 RAM (Single Access) Using 64 x 18 Dual Access RAM

APPLICATIONS

Suggested Printed Circuit Board Layout

Bottom View



AF004150

Connect ECL V_{CC} & GND Directly to Planes from E-13 and J-13.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias - T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
for High State ..... −0.5 V to +V_{CC} Max
DC Input Voltage ..... −0.5 to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage ..... +4.75 to +5.25 V
Air Velocity ..... 200 linear feet per minute

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH} I_{OH} = −3 mA			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH} I_{OL} = 16 mA					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = −18 mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = 0.5 V					−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = 2.4 V					50	µA
I_I	Input HIGH Current	V_{CC} = Max. V_{IN} = 5.5 V					1.0	mA
I_{OZH} I_{OZL}	Off State (High-Impedance) Output Current	V_{CC} = Max.		V_O = 2.4 V			50	µA
				V_O = 0.5 V			−50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = Max. to +0.5 V V_O = 0.5 V			−15		−50	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max						mA
			COM'L Only	T_A = 0 to +70°C			950	
				T_A = +70°C			850	
			MIL Only	T_A = −55 to +125°C				
				T_A = +125°C				

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical values are for V_{CC} = +25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with all inputs HIGH.

SWITCHING CHARACTERISTICS (Commercial Only)

Parameters	From	To	Test Conditions	Delay (ns)
Access Time	A_{RA} or A_{RB}	Y_A or Y_B	LE_A or LE_B = H	24
Turn-On Time	$\overline{OE}_A$ or $\overline{OE}_B$ = L	Y_A or Y_B		20
Turn-Off Time**	$\overline{OE}_A$ or $\overline{OE}_B$ = H	Y_A or Y_B = Z	C_L = 5 pF load	16
Enable Time	LE_A or LE_B = H	Y_A or Y_B		16
Transparency	$\overline{WE}_A$ or $\overline{WE}_B$ = L	Y_A or Y_B	LE_A or LE_B = H	32
Transparency	D_A or D_B	Y_A or Y_B	LE_A or LE_B = H $\overline{WE}_A$ or $\overline{WE}_B$ = L	33

Minimum Setup and Hold Time

Parameters	For	WRT	Delay (ns)
Data Setup	D_A or D_B	$\overline{WE}_A$ or $\overline{WE}_B$ (L TO H)	9
Data Hold	D_A OR D_B	$\overline{WE}_A$ or $\overline{WE}_B$ (L TO H)	2
Address Setup	A_{WA} or A_{WB}	$\overline{WE}_A$ or $\overline{WE}_B$ (H TO L)	0
Address Hold	A_{WA} or A_{WB}	$\overline{WE}_A$ or $\overline{WE}_B$ (L TO H)	3
Address Setup	A_{RA} or A_{RB}	LE_A or LE_B (H TO L)	7
Address Hold	A_{RA} or A_{RB}	LE_A or LE_B (H TO L)	4
Latch close before Write	LE_A or LE_B (H TO L)	$\overline{WE}_A$ or $\overline{WE}_B$ (H TO L)	0

Minimum Pulse Widths

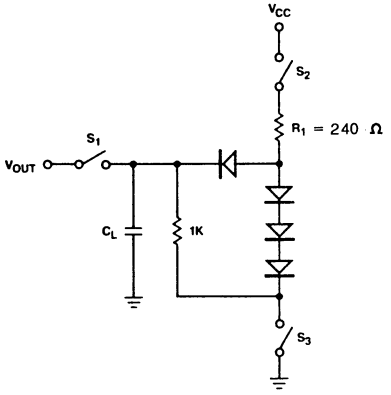
Parameters	Input	Pulse	Delay (ns)
Write Pulse	$\overline{WE}_A$ or $\overline{WE}_B$	HIGH – LOW – HIGH	18
Latch Data Capture	LE_A or LE_B	LOW – HIGH – LOW	10

$WE_A = WE_{AC} \bullet (WE_{AL} + WE_{AH})$
$WE_B = WE_{BC} \bullet (WE_{BL} + WE_{BH})$

** Y_A and Y_B Are Tested Independently

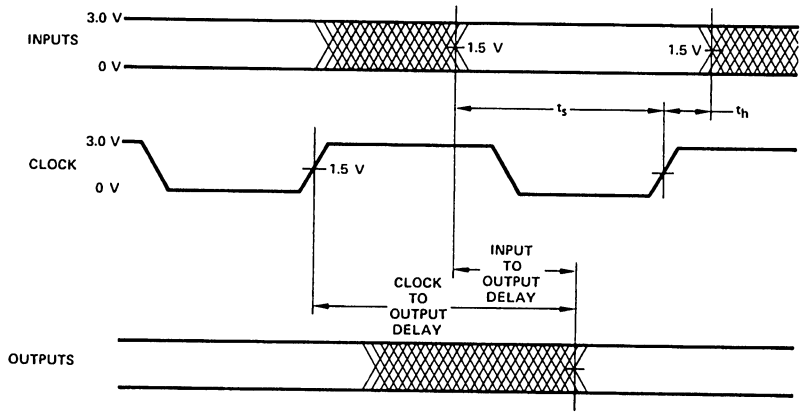
SWITCHING TEST CIRCUIT

THREE STATE OUTPUTS



Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

SWITCHING WAVEFORMS



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Notes on Test Methods

The following points give the general philosophy which we apply to tests which must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown.

1. Ensure the part is adequately decoupled at the test head. Large changes in supply current when the device switches may cause function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 – 8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide actual Sentry programs, under license from Sentry.
7. Capacitive Loading for A.C. Testing

   Automatic testers and their associated hardware have stray capacitance which varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays into and out of the high impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.

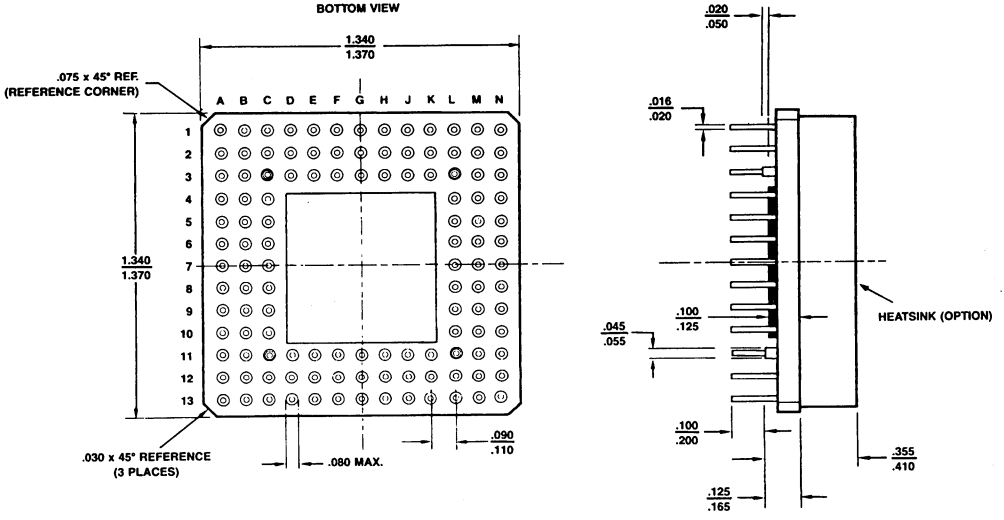
   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain D.C. measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special D.C. tests are performed in order to facilitate this correlation.
8. Threshold Testing

   The noise associated with automatic testing, the long, inductive cables, and the high gain of bipolar devices when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and A.C. testing are performed at "hard" input levels rather than at V_{IL} max and V_{IH} min.
9. A.C. Testing

   Occasionally, parameters are specified which cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other A.C. tests which have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain D.C. parameters have already been measured and are within specification.
   In some cases, certain A.C. tests are redundant since they can be shown to be predicted by other tests which have already been performed. In these cases, the redundant tests are not performed.

PHYSICAL DIMENSIONS

CG 120*



* Preliminary. Subject to Change.

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