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91A04A, 91AE04A, AND P6453 SERVICE MANUAL ADDENDUM

TO THE DAS 9100 SERIES SERVICE MANUAL (PART NUMBER 062-5848-00, -01, AND UP)

This Tektronix Manual Addendum supports the following products

91A04A Data Acquisition Module
91AE04A Data Acquisition Module
P6453 Data Acquisition Probe

The 062-5848-00 manual set is a package consisting of loose leaf binders with manuals and addenda. Each manual and addendum in the set has its own part number starting with the prefix 070.

This addendum contains service information specific to the 91A04A and 91AE04A Data Acquisition Modules and the P6453 Data Acquisition Probe.

Refer to the DAS 9100 Series Service Manual for information on other DAS products, including mainframes, instrument modules, probes, and options.

How To Use This Addendum. This addendum is organized similarly to the DAS 9100 Series Service Manual: sections in the addendum correspond to the sections in the service manual. You can either leave the addendum whole and place it in one of the service manual binders, or you can separate the sections and insert them after the corresponding section in the main manual.

NOTE: You can order an extra service manual binder (Vol. III) by using P/N 016-0769-00.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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SERIAL NUMBER _____

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DAS9100 Series 91A04A-91AE04A Service

OPERATOR'S SAFETY SUMMARY

The general safety information in this summary is for both operator and service personnel. Specific cautions and warnings are found throughout the manual where they apply but may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS AS MARKED ON EQUIPMENT

 **DANGER** — High voltage.

 Protective ground (earth) terminal.

 **ATTENTION** — refer to manual.

GROUNDING THE PRODUCT

The mainframe in which this product is installed is intended to operate from a power source that does not apply more than 250 V rms between the supply conductors or between either supply conductor and ground.

This product is grounded through the mainframe in which it is operating. To avoid electrical shock, plug the power cord of the mainframe into a properly wired receptacle before connecting to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including keys and controls that may appear to be insulated) can render an electric shock.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury, do not operate this product without mainframe covers or panels installed. Circuit boards and components can become very hot during operation.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY
Refer also to the preceding Operator's Safety Summary.

DO NOT SERVICE ALONE

Do not perform service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before soldering or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages.

NOTE

Observe safety precautions stated in the DAS 9100 Series Service Manual *concerning CRT safety, X-ray emission, and loose objects.*

Section 1
INTRODUCTION AND SPECIFICATIONS

This section provides a general description of the electrical and physical attributes of the 91A04A and 91AE04A High Speed Acquisition Modules, and lists their electrical and environmental specifications.

DESCRIPTION

The 91A04A Series Data Acquisition Modules are plug-in circuit board assemblies compatible with any DAS 9100 Series mainframe. They feature acquisition rates of 330 MHz (3 ns) with four data channels, or 660 MHz (1.5 ns) with two data channels. Each module uses one P6453 Data Acquisition Probe.

The 91A04 and 91A04A master modules are functionally identical, as are the 91AE04 and 91AE04A expander modules. Therefore, pre-A and A version modules can be used in the same DAS mainframe in any combination provided the following criteria are observed:

- Only one master module is installed.
- No more than three expander modules are installed.
- All expander modules are installed on the same side of the master module.

A maximum of one master module may be installed in a DAS mainframe. Up to three expander modules may also be installed to increase the channel width. The expander modules can only be used if a master module is installed.

MODES OF OPERATION

DATA ACQUISITION MODE

Each 91A04 Series module provides four incoming data channels supplied by a P6453 Data Acquisition Probe. Special deskew procedures are provided to correct any propagation delays between data channels and clocks. Deskewing ensures accurate setup and hold times, and minimizes channel-to-channel skew.

The 91AE04A Data Acquisition Expander Module is an etched circuit board assembly that is slaved to a 91A04A or 91A04 master module. 91AE04A and 91AE04 modules are functionally interchangeable. Each 91AE04A allows an additional four channels of 2048-word-deep data acquisition with word recognition for triggering. Clocks are distributed to all 91AE04A modules from the master module. Word recognizer signals from all expander modules in the system are sent to the master module.

The 91A04 Series modules can acquire data using the DAS internal clock at intervals ranging from 5 ms to 3 ns, or using an external clock's rising or falling edge (300 MHz maximum). The maximum memory depth in this mode is 2048 words.

The 91A04 Series modules have a one-word trigger. Triggering can be positioned in the beginning, center, or end of acquisition memory; or it may be delayed for up to 32,767 clock cycles.

Data may be displayed in either the DAS State Table or Timing Diagram menus.

HIGH-RESOLUTION MODE

The 91A04 Series modules can be operated in a 1.5 ns high-resolution mode, each module acquiring two channels of data instead of four, for a maximum of eight parallel channels. The memory depth is increased to 4096 words.

Data acquired in the high-resolution mode can only be displayed in the Timing Diagram menu.

ARMS TRIGGER MODE

The 91A04 series of data acquisition modules can be used in an ARMS TRIGGER mode with the 91A32 or 91A24 Data Acquisition Modules (slow cards) provided the following conditions are met:

- If the 91A04 series module has V2 software, it must reside in the DAS mainframe with V1.11 firmware.
- If the 91A04 series module has V1 software, it must reside in a DAS mainframe with V1.09 or lower firmware.

NOTE

DAS mainframes that are shipped with a 91A04A and/or a 91A24 have V1.11 firmware.

In this mode, the arming module and the armed module run simultaneously, but at different clock rates. The 91A24 trigger enables the 91A04 Series modules to begin looking for a trigger.

If the 91A04 Series acquisition rate is ≤330 MHz, the resulting time-aligned display can be viewed in either the DAS State Table or Timing Diagram menus. If the 91A04 Series 660 MHz high-resolution clock is used, the resulting time-aligned data can only be viewed in the Timing Diagram menu.

In the ARMS mode, the 91A04 Series data display is limited to the last 512 words acquired.

STANDARD AND OPTIONAL ACCESSORIES

91A04A DATA ACQUISITION MODULES

The following lists include the standard and optional accessories for 91A04A modules.

Standard Accessories

1		P6453 Data Acquisition Probe
1	070-4678-00	*91A04A Instructions*
1	070-4676-00	*91A04A, 91AE04A, and P6453 Operator's Manual Addendum (to the DAS 9100 Series Operator's Manual)*

Optional Accessories

The following optional accessories are used for service and adjustment procedures.

070-4298-00	*91A04A Series Service Manual Addendum (to the DAS 9100 Series Service Manual)*
175-7322-00	10-inch Extender Cable
195-0995-00	12-inch Threshold VBB Cable

The remaining optional accessory is used for reference when 91A04A or 91AE04A Data Acquisition Modules are used with 91A04 or 91AE04 modules.

070-4254-00	*91A04, 91AE04, and P6453 Operator's Manual Addendum (to the DAS 9100 Series Operator's Manual)*

91AE04A HIGH SPEED ACQUISITION EXPANDER MODULE

The following lists include the standard and optional accessories for the 91AE04A Data Acquisition Expander Module. There are no optional accessories to this module.

Standard Accessories

1		P6453 Data Acquisition Probe
1	195-0693-00	3.5-inch Threshold Jumper Cable
2	175-6425-00	3-inch Coaxial Cables
1	070-4677-00	*91AE04A Instructions*

P6453 DATA ACQUISITION PROBE

The following list includes the standard accessories for the P6453 Data Acquisition Probe.

Standard Accessories

1	195-2234-06	Package of 10 leads (probe tip leads for DIP IC packages)
1	195-1943-06	Package of 10 leads (miniature probe tips for flat packs)
1	070-3704-00	*P6453 Instructions*

Optional Accessories

195-3659-00	Package of 2 leads with grabber tips

SPECIFICATIONS

INSTALLATION REQUIREMENTS

The 91A04A or 91AE04A may not meet specifications unless the modules are installed in the DAS mainframe in accordance with the *Module Installation* instructions in the *Operating Instructions* section of this addendum.

Table 1-1
91A04A/91AE04A ELECTRICAL SPECIFICATIONS: POWER

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
91A04A Input Power (from mainframe)		+12 V ±3%, 0.45 A max. +6 V ±3%, 0.4 A max. +5 V ±3%, 11 A max. (see *Installation Requirements)* -5 V ±3%, 0.2 A max. -12 V ±10%, 0.4 A max.
91AE04A Input Power (from mainframe)		+12 V ±3%, 0.4 A max. +6 V ±3%, 0.4 A max. +5 V ±3%, 9.0 A max. -5 V ±3%, 0.2 A max. -12 V ±10%, 0.4 A max.
Output Power from any 91A04A or 91AE04A Module to Probe		+15 VC and D ±5%, 75 mA max. ea., 150 mA max. total +5 V ±3%, 150 mA max.
Internal Supply Voltages	Supply Voltage = Vcc - 0.80 V ±50 mV	
+4.2 V Supply		
+3 V Supply	Supply voltage = Vcc - 1.92 ±50 mV	
+15 V Supply Switching Frequency	160 kHz ±30%	

Table 1-2
91A04A/91AE04A ELECTRICAL SPECIFICATIONS: TRIGGER AND STORAGE

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Minimum Data Amplitude	600 mV p-p	
Minimum Data Slew Rate at Probe Tip		0.05 V/ns
Trigger		
Trigger Types		Single-level word recognition
Word Recognition		Single-level data word, externally armable
Word Recognition with 1.5 ns Internal Clock (async)	To guarantee triggering, the trigger word must be present for 1 sample period +2.5 ns.	
Word Recognition with Internal Clocks Slower than 1.5 ns (async)	To guarantee triggering, the trigger word must be present for 1 sample period +2 ns.	
Word Width		Same as memory width
Bit Specification		Logic 1, or 0, or X (don't care)
Trigger Position		Begin, center, end, or delay
Stop-store Delay		In 91A04 ONLY mode, selectable from 1 to 32,767 sample periods after trigger. In ARMS mode, the maximum 91A04A delay is 500 as set in the Trigger Specification menu.
Pattern-sequence Comparison		Compare until equal and compare until not equal
Comparison Sequence Length	From 1 to 2048 words with V2 firmware	
ARMS Mode Characteristics		The 91A04A trigger will be armed within ten slow-card clock cycles after the occurence of the slow-card trigger.
Time Alignment Requirements		The DAS will not display time-aligned ARMS data unless the following conditions are met: 1. No qualifiers can be used by the slow module.

Table 1-2 (Cont.)
91A04A/91AE04A ELECTRICAL SPECIFICATIONS: TRIGGER AND STORAGE

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
		2. Data saved in the 91A04A memory must overlap the data saved by the slow module by at least five slow clock periods. 3. The fast clock must be at least twice as fast as the slow clock. 4. The fast trigger must be in memory.
Time Alignment Accuracy		The fast data displayed in ARMS mode will line up with the corresponding slow clock within ± (+1 slow clock +1 fast clock +13 ns), worst case.
Acquisition Memory		
Memory Depth		2048 words (40-96 in high-resolution mode)
Memory Width		4 channels (one 91A04A and one probe). Expandable to 16 channels (with one 91A04A and 3 91AE04As, and 4 probes). High-resolution mode has a minimum of 2 channels available, and a maximum of 8 (1 to 4 modules).
Minimum Sampling Period	1.5 ns	+15% -10% accuracy
Internal Sample Periods		Selectable: 1.5 ns (high resolution), 3 ns, 5 ns, 10 ns, 20 ns, 40 ns, 50 ns, 100 ns, 200 ns, 500 ns, 1 μs, 2 μs, 5 μs, 10 μs, 20 μs, 50 μs, 100 μs, 200 μs, 500 μs, 1 ms, 2 ms, 5 ms
Internal Clock Accuracy		
3 ns Clock	3.0 ns +5%, -3%	In the 1.5 ns acquisition mode, the 3.0 ns clock is used and two evenly spaced samples are taken per rising edge. Nominal value is 3.06 ns.
5 ns Clock	5.0 ns ±5%	
10 ns and up		±1%, ±1 ns (this clock is provided by the 91A08 clock on the Trigger-/Time Base board)
Minimum 3 ns Clock Pulse Width at TP125		1.30 ns, high or low measured at Vbb

NOTE

If the data at the probe tip always passes through the region from 100 mV below the programmed threshold to 100 mV above the programmed threshold in less than 0.4 ns, Tdata is:

Tdata = 0 ns

If an edge of the data ever requires more than 0.4 ns to pass through this region, Tdata is defined as:

Tdata = (maximum transit time through region) minus 0.4 ns

Table 1-3
91A04A/91AE04A ELECTRICAL SPECIFICATIONS: ASYNCHRONOUS DATA ACQUISITION

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Typical Channel-to-channel Data Skew on a Single Module		
Rising Edge		0.90 ns + Tdata
Falling Edge		1.2 ns + Tdata
Minimum Detectable Pulse Width with 1.5 ns Internal Clock (High-Resolution Mode)	3.5 ns + [2 x Tdata]	

Supplemental Information

Minimum detectable pulse width is verified with a 600 mV p-p signal centered around the programmed threshold. Tdata of the test signal is 0 ns for both rising and falling edges.

A symetrical 7.0 ns square wave is acquired in high-resolution mode to verify minimum asynchronously detectable pulse width. The acquired signal is then displayed in the Timing Diagram menu. The data should be acquired three times, and should show no missing pulses any of the three times. The displayed pulses should be from one to three samples wide.

Table 1-4
91A04A/91AE04A ELECTRICAL SPECIFICATIONS:
SYNCHRONOUS DATA ACQUISITION

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
External Clock		
Minimum External Clock Amplitude to Probe Input	700 mV p-p	
Minimum External Clock Slew Rate at Probe Tip		0.05 V/ns from 100 mV below to 100 mV above the programmed threshold
External Clock Polarity		Selectable: rising or falling edge
Maximum External Clock Frequency with all Data Channels Active	300 MHz	
Maximum External Clock Frequency With Only One Channel Active		Typically 330 MHz
Minimum Clock Pulse Width Below 275 MHz	1.80 ns	
Required Clock Duty Cycle above 275 MHz		Between 45%. and 55% with 1.65 ns min.

NOTE

If the data and clock signals at the probe tip always pass through the region from 100 mV below to 100 mV above the programmed threshold in less than 0.4 ns, then Tdata = 0 ns and Tclk = 0 ns.

If the data and/or clock ever requires more than 0.4 ns to pass through this region, Tdata and/or Tclk are defined as:

Tdata = (Maximum data transit time through region) minus 0.4 ns.

Tclk = (Maximum clock transit time through region) minus 0.4 ns.

Under no conditions will Tdata or Tclk be less than 0 ns.

Table 1-4 (Cont.)
91A04A/91AE04A ELECTRICAL SPECIFICATIONS:
SYNCHRONOUS DATA ACQUISITION

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Typical Single-Channel Acquisition Speed		330 MHz
Typical 330 MHz Single-Channel Data Setup		2.4 ns + Tdata + Tclk
Typical 330 MHz Single-Channel Data Hold		0.0 ns + Tdata + Tclk
300 MHz Acquisition		
300 MHz Data Setup	3.0 ns + Tdata + Tclk	
300 MHz Data Hold	0.3 ns + Tdata + Tclk	
Minimum Data Period for Synchronous Acquisition	3.3 ns	Sampled data must not make any transitions inside this period.

Table 1-5
91A04A/91AE04A ELECTRICAL SPECIFICATIONS:
INTERCONNECTIONS BETWEEN MODULES

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Clock Outputs from 91A04A		
Output Levels	+5 V Referenced ECL	
Skew Between Clocks		±200 ps (measured at J131, J135, and J138)
Clock Received by 91AE04A		
Levels Received		+5 V referenced ECL, 760 mV p-p minimum at 330 MHz (measured at U341, pin 11 or 13)
Offset Adj.		From approx +20 mV to +85 mV for power supply differences
Word Recognizer Output from 91AE04A		
Output Levels		+5 V referenced ECL
Minimum Signal Duration		2.5 ns with 3 ns internal time base

Table 1-5 (cont)
91A04A/91AE04A ELECTRICAL SPECIFICATIONS:
INTERCONNECTIONS BETWEEN MODULES

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Time Period from Clock Input to Word Recognizer Output		11.9 ns ±0.3 ns
Word Recognizer Inputs to 91A04A		
Minimum Signal Duration		2.5 ns with 3 ns internal time base
Time Period from any Clock Output to U641 pin 2		14.0 ns ±0.3 ns
Inputs, Levels	+5 V referenced ECL	

Table 1-6
91A04A/91AE04A ELECTRICAL SPECIFICATIONS:
PROBE INTERFACE AND SUPPORT

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Probe-to-Module Signals	5 channels, identify, and pod presence	
Channels	4 data and 1 external clock	
Channel Signal Characteristic		Single-ended with 2 mA/V sensitivity
Identify Signal		Ground-true, normally open
Pod Presence		Grounded
Data Delay Time		13 ±0.5 ns
Clock Delay Time		10.07 ±0.5 ns
Module-to-Probe Signals		Threshold reference voltage
TTL Threshold		+1.4 V
Variable (VAR) Threshold		-2.5 V to 5.0 V in 50 mV steps
Threshold Accuracy at Probe Tip	Menu select value ±50 mV ±0.75% of menu setting	
Threshold Accuracy at Connector		±3 mV without probe ±1.5 mV initial setting accuracy

Table 1-7
P6453 ELECTRICAL SPECIFICATIONS:
OPERATING CHARACTERISTICS (INCLUDING CIRCUITS ON 91A04A MODULE)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Channel Input Impedance		
Input Resistance, Tip of Probe Lead to REF Input		1 MΩ ±5%
Input Capacitance		5 pF ±1 pF
Reference Input Characteristic at Tip	Floating reference input	
Maximum Non-Destructive Voltage to Either Input		25 V (dc + peak ac)
Maximum Non-Destructive Voltage to Vref		25 V (dc + peak ac)
Voltage Range		
Operating Input	-2.5 V to +5 V (dc + peak ac)	
Common Mode	-2.5 V to +5 V (dc + peak ac)	
Minimum Input Signal Slew-Rate		500 V/μs

Environmental Specifications

The environmental specifications for the operation and non-operation of these instrument modules shall meet or exceed those specified for the operation and non-operation of any DAS mainframe. Refer to the *DAS 9100 Series Service Manual*.

Temperature

Operating ambient temperature: 0°to +50° C
Storage temperature: -40° to +50° C

Humidity

MIL-T-28800B, Class V with the following exception: before applying power, the mainframe must reside in <70% relative humidity for two hours.

Altitude

Operating altitude: 15,000 ft., maximum
Storage altitude: 50,000 ft., maximum

Vibration

Operates with 0.015 inches p-p displacement from 10 Hz to 45 Hz.

Shock

Withstands 30 g's.

Bench Handling

45°, or 4 inches, or equilibrium, whichever comes first.

Packaged Product Vibration and Shock

Qualifies under National Safe Transit Association's Preshipment Test Procedures1A-B-1 and 1A-B-2.

Electrostatic Immunity

The 91A04A and 91AE04A modules withstand discharge through 2 kΩ resistance of a 250 pF capacitor charged to 8 kV. The limiting component is the P6453 Probe.

Electromagnetic Compatibility

The 91A04A and 91AE04A modules qualify under the test limits specified in the FCC Rules, Part 15, Sub-part J, Class B.

91A04A/91AE04A Physical Specifications

The physical characteristics of the 91A04A and 91AE04A High Speed Acquisition Modules are consistent with those of all DAS 9100 Series instrument modules as described in the *DAS 9100 Series Service Manual.*

Table 1-8
P6453 PHYSICAL CHARACTERISTICS

Characteristic	Description
Length	
Probe Tip to Connector	2.4 m (8 ft.)
Input Leads	38 mm (1.5 in.)
Weight, Probe Assembly	390 gm (13.7 oz.)

Section 2

OPTIONS

There are no options to the 91A04A Data Acquisition Modules, the 91AE04A Data Acquisition Expander Module, or the P6453 Data Acquisition Probe. For information regarding DAS system options, refer to the *DAS 9100 Series Service Manual.*

Section 3
OPERATING INSTRUCTIONS

GENERAL INFORMATION

DESCRIPTION

The 91A04A and 91AE04A Data Acquisition Modules are plug-in circuit board assemblies that are compatible with any DAS 9100 Series mainframe. They feature acquisition rates of 330 MHz (3 ns) with four data channels, or 660 MHz (1.5 ns) with two data channels. Each module uses one P6453 Data Acquisition Probe.

Only one 91A04A module may be installed in a DAS mainframe. Also, a 91A04A may not be installed in a mainframe containing a 91A04 module.

Up to three 91AE04A modules may also be installed to increase the 91A04A or 91A04 channel width. The 91AE04As are expander modules and can only be used if a 91A04A or 91A04 module is installed.

91A04A and 91AE04A modules (called A-version modules) are completely compatible with 91A04 and 91AE04 modules. When used with 91A04 or 91AE04 modules, the A version modules meet or exceed the specifications of the 91A04 modules. When the A-version modules are used alone, they meet or exceed the specifications published in this manual.

P6453 Data Acquisition Probes are needed to acquire data with 91A04A and 91AE04A modules. These high-impedance probes properly buffer signals for acquisition by these modules.

MODES OF OPERATION

Each 91A04A and 91AE04A module provides four incoming data channels supplied by a P6453 high-speed probe. Special deskew procedures are provided to correct any propagation delays between data channels and clocks. Deskewing ensures accurate setup and hold times, and minimizes channel-to-channel skew.

The 91A04A and 91AE04A modules can acquire data using the DAS internal clock at intervals ranging from 5 ms to 3 ns, or using an external clock's rising or falling edge (300 MHz maximum). The maximum memory depth in this mode is 2048 words.

The 91A04A and 91AE04A modules have a one-word trigger. Triggering can be positioned in the beginning, center, or end of acquisition memory or it may be delayed for up to 32,767 clock cycles.

Data may be displayed in either the State Table or Timing Diagram menus.

High-Resolution Mode (1.5 ns). The 91A04A and 91AE04A modules can be run in a 1.5 ns high-resolution mode using the DAS internal clock. When run in this mode, each module acquires two channels of data instead of four, for a maximum of eight parallel channels with four modules. The memory depth is increased to 4096 words.

Data acquired in the high-resolution mode can only be displayed in the Timing Diagram menu.

ARMS Trigger Mode. The 91A04A and 91AE04A modules can be used in an ARMS trigger mode with 91A32 and 91A24 Data Acquisition Modules. In this mode, the two types of modules run simultaneously, but at different clock rates. The trigger from the slower module enables the 91A04A/91AE04A modules to begin looking for a trigger.

The resulting time-aligned display can be viewed in either the State Table or Timing Diagram menus if the 91A04A acquisition rate is ≤330 MHz. If the 91A04A's 660 MHz high-resolution clock is used, the resulting time-aligned data can only be viewed in the Timing Diagram menu.

In the ARMS mode, the 91A04A/91AE04A data display is limited to the last 512 words acquired.

MODULE INSTALLATION

Throughout the following discussion, it is assumed that you are already familiar with the procedures for removing the mainframe top panel and module compartment cover, and with the procedures for installing modules into the mainframe bus slots. If you are not familiar with these procedures, refer to the *Maintenance: General Information* section in the *DAS 9100 Series Service Manual.*

Do not remove or install a 91A04A or 91AE04A module until you have read the following warnings, cautions, adjustment procedures, and configuration requirements.

WARNING

When installing or removing instrument modules, the operator may gain access to the mainframe's module compartment only. Unless you are a qualified service technician, do not open any other compartments within the mainframe because they contain hazardous voltages.

After installing or removing modules, be sure to replace the mainframe covers. Circuit boards and components can become very hot during operation.

CAUTION

When instrument modules are being installed, the mainframe should be turned off and unplugged from its power source. Damage to the module's circuitry may occur if the module is installed while the mainframe is receiving power.

DO NOT PRESS ON MODULE COMPONENTS. Use care when handling the 91A04A and 91AE04A modules or the circuitry may be damaged.

FIRMWARE COMPATIBILITY

91A04A modules only operate in a mainframe containing firmware version 1.11 or higher. The firmware version of the mainframe can be found in the upper right-hand corner of the DAS power-up menu. If your DAS does not contain firmware version 1.11, contact your Tektronix representative for a firmware update kit.

91AE04A modules operate with 91A04 modules in mainframes containing firmware versions 1.11 or lower. 91AE04A modules operate with 91A04A modules in mainframes containing firmware version 1.11 or higher.

CONFIGURATION REQUIREMENTS

The power and configuration requirements for 91A04A, 91A04, 91AE04A and 91AE04 modules are as follows:

1. Only one 91A04A or 91A04 module may be operated in the mainframe at one time.
2. Because of the power consumption of the 91A04A and 91A04 modules, a 91A04A or 91A04 module can only share a +5 V Power Supply with the modules indicated in Table 3-1. These modules may also share their supply with an empty slot. Table 3-1 also has a sample list of modules that draw too much power to share a supply with a 91A04A or 91A04 module.

Table 3-1
91A04A AND 91A04
+5 V POWER SUPPLY RESTRICTIONS

Description	Module
Modules that can share a +5 V Power Supply with a 91A04A or 91A04	91A08 91P32 91AE24
Some modules that cannot share a +5 V Power Supply with a 91A04A or 91A04	91AE04A 91AE04 91A24 91A32 91P16

CAUTION

The 91A04A or 91A04 may only share a power supply with one of the three modules declared acceptable in Table 3-1. Otherwise, neither module sharing the supply will operate correctly.

When positioning modules around the 91A04A or 91A04, be sure to allow for the power supply restriction. One possible positioning of 91A04A and 91AE04A modules is shown in Table 3-2.

You can see which power supplies are present in the mainframe by checking the chrome pins visible through the power supply area cover.

Table 3-2
91A04A AND 91AE04A
SAMPLE BUS SLOT PLACEMENT

Bus Slot	Module
0	Controller
1	91A24 Data Acquisiton Module
2	91AE24 Data Acquisition Module
3	91AE24 Data Acquisition Module
4	91A04A Data Acquisition Module
5	91AE04A Data Acquisition Module
6	91AE04A Data Acquisition Module
7	Trigger/Time Base Module

Note that the 91A04A module is sharing its power supply with a 91AE24. Also note that both 91AE04A modules are on the same side of the 91A04A module.

Word Recognizer and Clock Cables

Each 91AE04A module comes with two 3-inch coaxial cables. These cables are used to transmit word recognition and clock signals between master 91A04A or 91A04 modules and expander 91AE04A and 91AE04 modules. The cables must be correctly attached for the expander modules to work properly.

Figure 3-1 illustrates how to attach these coaxial cables.

Connecting the Cables to the 91AE04A or 91AE04. Attach the two cables to the two coaxial connectors located on top of the 91AE04A and 91AE04 modules.

The connector on top and closest to the front of the module (J141) is for word recognition signals. The connector on top and toward the rear of the module (J138) is for clock signals.

Connecting the Cables to the 91A04A or 91A04. Attach the cables to the six coaxial connectors located on top of the 91A04A or 91A04 module.

The three connectors on top and toward the front of the 91A04A or 91A04 module (J145, J143, and J141) are all for word recognition signals. Plug the cable that is attached to the forward connector of the expander 91AE04A or 91AE04 module into one of these three connectors.

The three connectors on the top and toward the rear of the 91A04A or 91A04 module (J138, J135 and J131) are all for clock signals. Plug the cable that is attached to the rear connector of the expander 91AE04A or 91AE04 modules into one of these three connectors.

91A04A and 91A04 modules provide enough connectors for a total of up to three 91AE04A or 91AE04 modules.

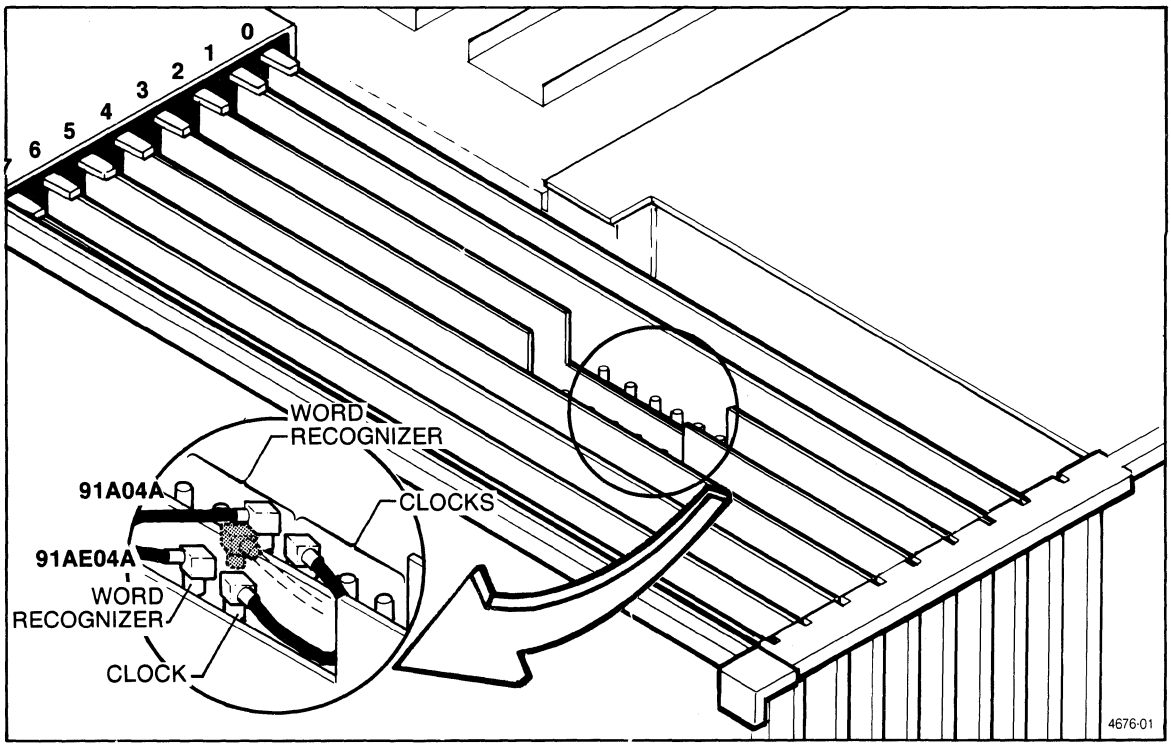


Figure 3-1. Connecting the word recognizer and clock cables between the 91A04A and 91AE04A modules.

Threshold Cables

All 91AE04A and 91AE04 expander modules come with one 3.5-inch jumper cable that is used to obtain threshold information from the master 91A04A or 91A04 module.

NOTE

You only need to connect the threshold cables if you have a 91AE04 (non-A version) module in your system.

These threshold cables are attached in a daisy-chain fashion, going from the 91AE04A or 91AE04 expander module positioned farthest from the master to the next expander module, then to the next expander module, and finally to the master module.

Attach the first cable in the chain to J125 Pin 3 of the 91AE04A or 91AE04 expander module positioned farthest from the master, and to J125 Pin 2 of the second expander module (going toward the master). Attach the second cable to J125 Pin 3 of the second expander module and to J125 Pin 2 of the third expander module (the module nearest the master). Attach the third cable to J125 Pin 3 of the third expander module and to J125 Pin 1 of the master 91A04A or 91A04.

Figure 3-2 illustrates how the threshold jumper cables are connected. This illustration shows one master 91A04A module and three expander 91AE04A modules.

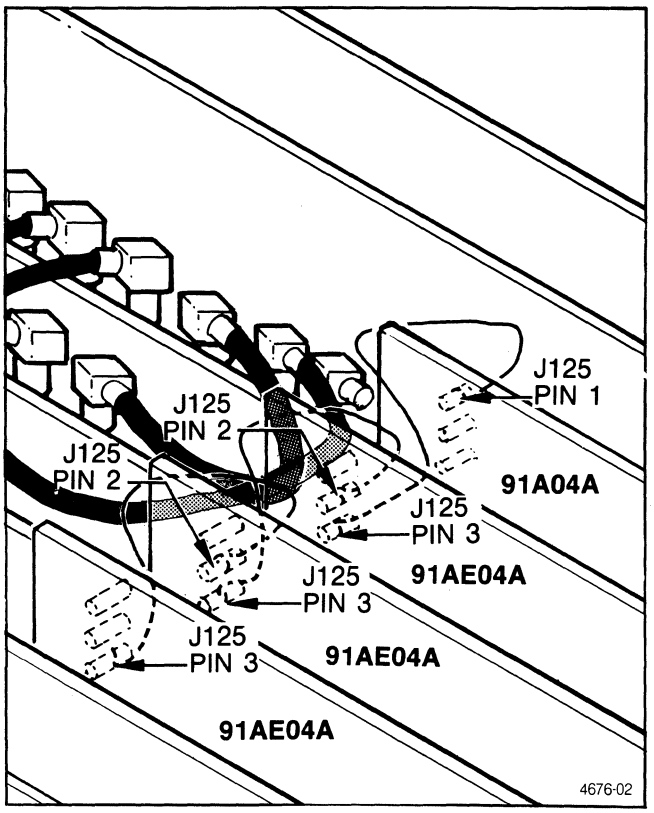


Figure 3-2. Connecting the threshold jumper cables.

Required Adjustments

91A04A modules, 91AE04A modules, and certain 91AE04 modules require some adjustment when they are first installed in a mainframe. These adjustments tune the modules to operate with the mainframe and with the other 91A04-type modules.

If your modules were installed in their mainframe at the factory, they arrived properly adjusted. If you received modules that were not installed in a mainframe, you must perform these adjustments yourself. Table 3-3 indicates conditions in which the adjustments must be performed.

NOTE

91A04A, 91AE04A, and 91AE04 specifications are not guaranteed unless all adjustments are properly performed.

The 91AE04A and 91AE04 adjustments require a 3.5-digit digital multimeter. The adjustment procedure for all three modules is given in *Module Adjustment Procedures* at the end of this section.

Table 3-3
MODULE ADJUSTMENT CONDITIONS

Module Name	Conditions Requiring Adjustment
91A04A	91A04A just installed in mainframe, or 91A04A, that was previously operating alone, is operated with expanders, or 91A04A, that was previously operating with expanders, is operated alone.
91AE04A	91AE04A just installed in mainframe, or 91AE04A has changed its +5 V Power Supply, or the master module has changed its +5 V Power Supply
91AE04 with serial number below B01011B	91AE04 just installed in mainframe, or 91AE04 clock cable connection changed, or 91AE04 driven by a new master 91A04A or 91A04 module, or the 91AE04 has changed its +5 V Power Supply, or the master module has changed its +5 V Power Supply

CONNECTING THE P6453 PROBE

The P6453 Data Acquisition Probes connect to the 91A04A and 91AE04A modules through backpanel openings on the mainframe. The probes attach to the modules' Pod C connectors.

To connect the probe (see Figure 3-3):

1. Grasp the probe by its cable holder.
2. Align the cable connector with the module's pod connector. Be sure the probe cable is pointing downward.
3. Gently push the cable connector onto the module's pod connector. Do not force the connection.

NOTE

When a probe is first connected to a module, that module must be deskewed. For more information, refer to Module Deskewing *later in this section.*

CAUTION

You may damage the probe cable if you try to disconnect the probe by pulling on the cable rather than the cable holder.

Disconnect the probe by pulling gently on its cable holder.

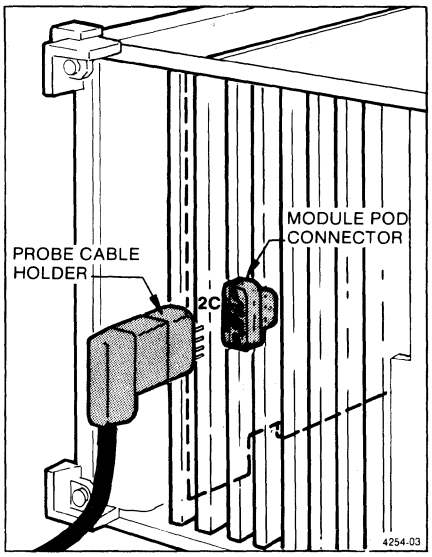


Figure 3-3. Connecting the P6453 probe.

P6453 PROBE OPERATION

The P6453 is a 330 MHz, 5-channel probe. It provides four data input channels and one clock channel. The clock channel is active only when connected to a 91A04A or 91A04 module. This clock then serves as the external clock for the master 91A04A or 91A04 module and for all of the 91AE04A and 91AE04 expander modules.

Figure 3-4 illustrates the various elements of the P6453 probe. Refer to this figure when reading the following paragraphs.

Probe Leads and Tips. Each channel lead on the P6453 has a hybrid tip that converts an external signal to an appropriate level for processing by the acquisition module. The conversion requires two inputs: IN (input signal) and REF (reference voltage).

The inputs to the channel hybrid are supplied by gripper-tipped leads. The probe comes with two types of leads (a package of 10 each). One type of lead has 0.10 inch centers for connecting to DIP ICs, and the other has 0.05 inch centers for connecting to flat packs. These gripper-tipped leads lock to the circuitry under test to ensure signal fidelity.

The P6453 also has larger leads available as optional accessories. The larger leads are easier to use, but may degrade operation of the probe at frequencies above 150 MHz.

IN (Input) and REF (Reference Voltage) Signals. The hybrid circuitry at the channel tip functions as a 1 MΩ input, 50 Ω output, 10X FET probe. The two inputs, IN and REF, perform the same function as the signal and ground inputs on standard probes, except that REF may be referenced to a dc voltage other than ground. This reference voltage must lie between −2.5 V and +5 V.

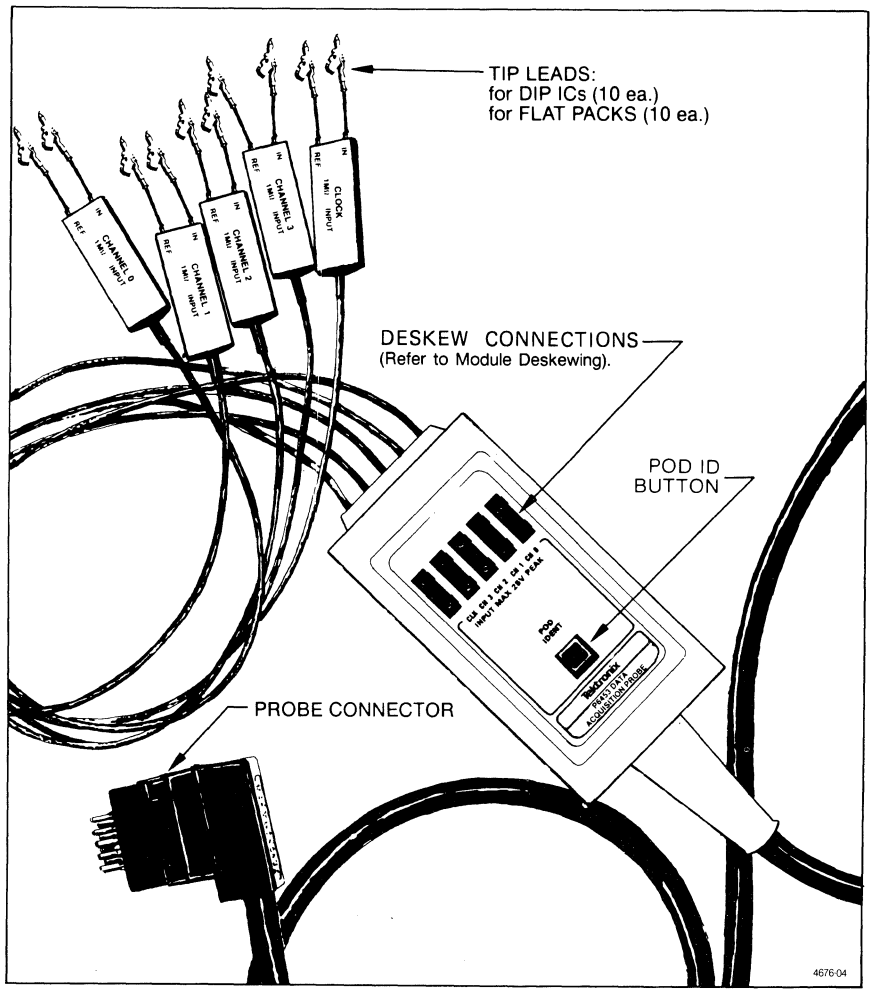


Figure 3-4. The P6453 Data Acquisition Probe parts.

The reference voltage establishes the channel threshold. If REF is connected to ground, the channel threshold is the same as that specified for the module to which it is connected. If REF is connected to a voltage source, the channel has a threshold equal to the specified module threshold plus the reference voltage. (You specify the module threshold in the Channel Specification menu.)

The IN signal for data channels must be 600 mV peak-to-peak, or greater, centered around the threshold. The IN signal for the clock channel may also be approximately 600 mV peak-to-peak, unless the clock is operating at rates above 250 MHz. Clocks higher than 250 MHz should be at least 700 mV p-p, centered around the threshold.

Attaching the Probe to the Circuit. Connect the leads from the probe so the probe and the circuit have the least possible interaction. Proper placement of the leads minimizes line reflections in the circuit. To minimize the interaction in high speed circuits, leads must be attached as close to the transmission line driver or the termination resistor as possible.

Good placement of the lead connection is especially important with sensitive circuits or when you are using the larger optional grabber tips.

Maximum Non-Destructive Voltage. The maximum input voltage that may be used with the P6453 probe is ±25 V peak.

CAUTION

Probe circuitry may be damaged if the P6453 Data Acquisition Probe is connected to a voltage source greater than ±25 V peak.

Impedance. The input impedance of the P6453 probe is 1 MΩ with a 5 pF nominal input capacitance.

OPERATOR'S CHECKOUT PROCEDURE

When the DAS mainframe is powered up, any installed 91A04A and 91AE04A modules are identified on the power-up configuration display. A PASS or FAIL notation appears next to each module to denote the results of that module's power-up testing. Table 3-4 describes the power-up errors for the 91A04A and 91AE04A modules and their possible causes.

Table 3-4
POWER-UP ERROR CONDITIONS

Error Condition	Definition
FAIL	The 91A04A module has failed the power-up test. A failure may be caused if the modules's P6453 probe is receiving +6.3 V or more at an input during the test. Disconnect the probe from the circuit under test and power up the DAS again. If the test fails again, refer the 91A04A module to qualified service personnel. This failure does not affect the operation of any installed pattern generator modules or other data acquisition modules, except for 91AE04As and 91AE04s. 91AE04A and 91AE04 modules will not operate without a working 91A04A or 91AE04 module.
91AE04A Data Acquisition Module FAIL	The 91AE04A module has failed the power-up test. The module will not operate properly. This failure will occur if the clock and word recognizer cables of the 91AE04 have been disconnected from the 91A04 module. Power down the mainframe, check the cables, then power up the mainframe. This failure may also be caused by the master 91A04A or 91A04 module's P6453 probe receiving +6.3 V or more during the test. Disconnect the leads of the master module's probe from the circuit under test and power up the mainframe again. This failure does not affect the operation of the master 91A04A or 91A04 module, other expander modules, or any other data acquisition or pattern generator modules.

MODULE DESKEWING

The channels of the P6453 Data Acquisition Probe can be verified by the deskewing operation. This operation is used to correct any propagation delay between acquisition channels.

The modules should be deskewed under the following conditions:

- **Power-Up** - The deskew operation should be performed whenever the mainframe is powered up. The deskew parameters are then saved in memory until the mainframe is turned off.

  You can also save the deskew parameters on tape by creating a DESKEW, an ACQ SETUP, or an ALL file after the deskew operation has been performed. This file can then be restored when the mainframe is powered up. Restoring the file re-enters the deskew parameters into the system.

  NOTE

  Before the tape file is restored, the 91A04A, 91A04, 91AE04A, and 91AE04 probes should all be connected the same way they were when the tape was made. Otherwise, the parameters restored from the tape are invalid.

- **Probe Connection Changes .** Perform the deskew operation on a module whenever its probe is changed or disconnected.

  If you change a 91AE04A or 91AE04 expander module's probe, only that module needs to be deskewed. If you change a master 91A04A or 91A04 module's probe, however, that module plus all expander modules should be deskewed since the clock is channeled through the master module's probe.

  With 91A04A and 91A04 firmware version 2, a tape file can be created that contains just the deskew values from 91A04A, 91A04, 91AE04A, and 91AE04 modules. To save only the deskew values in a tape file:

  1. Insert a tape in the tape drive.
  2. Enter the Input Output menu.
  3. Select SAVE STATUS in the operation field.
  4. Select file type DESKEW.
  5. Specify a file name.
  6. Press the INPUT OUTPUT key.

  The DAS creates a new tape file containing the probe deskew values.

Setting Up the Deskew Operation. The deskew operation is a function of the Trigger Specification menu. To set up the operation, enter the menu and perform the following steps (see Figure 3-5):

1. If not already viewing the 91A04 ONLY sub-menu, use the SELECT key to set the MODE field to the 91A04 ONLY value.

   A message reading DESKEW INCOMPLETE appears on the second line of the screen, and a message reading PODS TO DESKEW appears on the bottom line of the screen. The PODS TO DESKEW message identifies which module probes need to be deskewed. The module probes are identified by their POD ID (bus slot number, pod connector letter).

NOTE

The PODS TO DESKEW message appears at the bottom of the display whenever the mainframe is powered up or a probe connection is changed.

2. Position the screen cursor in the DESKEW field, and use the SELECT key to select the module probe to be used during the deskew operation.
3. Connect the probe channels as specified in the bottom portion of the menu. (See following description of channel connections.)
4. Press the TRIGGER SPEC key to start the deskew operation.

   If all channels of the probe deskewed properly, the probe is deleted from the list of PODS TO DESKEW.

   If any channels did not deskew properly, a message appears at the bottom of the display reading UNABLE TO DESKEW, followed by the channels which did not deskew. (Refer to *Error and Prompter Messages in the Reference Information* section of this addendum for more information.)

NOTE

After any probe channels have been deskewed successfully, the 91A04A or 91A04 external clock's setup and hold times may be changed in the SETUP/HOLD field. A description of this field is provided later in this addendum under 91A04 ONLY Sub-Menu Fields and Values.

After all channels have been successfully deskewed, the DESKEW field disappears from the screen, since it is no longer needed.

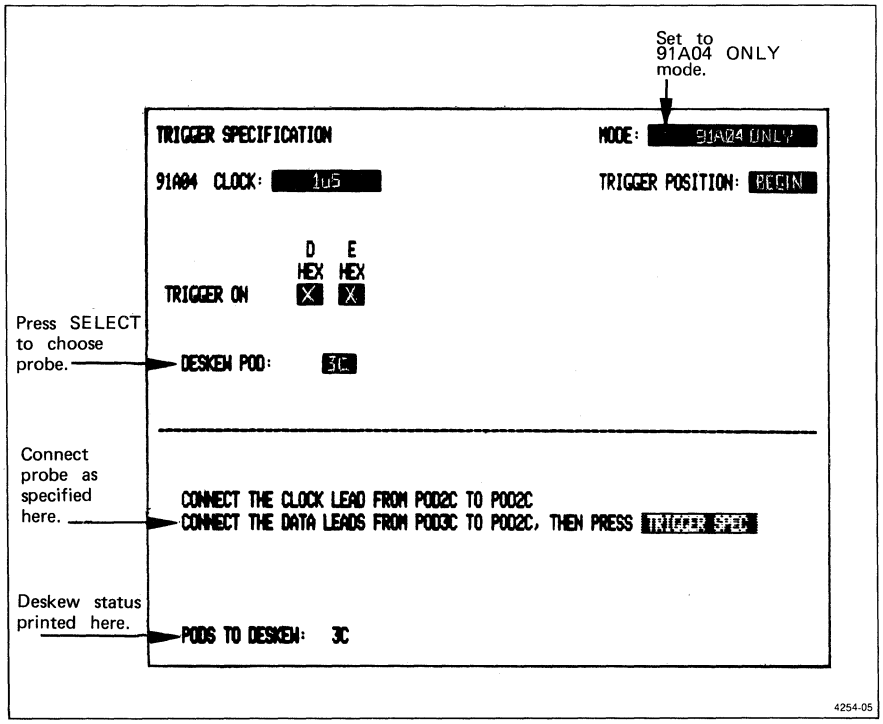


Figure 3-5. Setting up the Trigger Specification menu for the probe deskew operation. The menu fields specify the steps needed for setting up the operation.

Connecting Probe Channels for Deskew. Figure 3-6 illustrates how 91A04A and 91AE04A probes are connected during the deskew operation.

All P6453 probes are deskewed with respect to the master 91A04A or 91A04 module and its clock. Therefore, the clock channel from the master module is always used during the deskew operation.

If the probe being deskewed is connected to the 91A04A module, connect the data channels from that probe to their own deskew connectors.

If the probe being deskewed is connected to a 91AE04A module, connect the data channels from that probe to the deskew connectors of the master 91A04A or 91A04 module's probe.

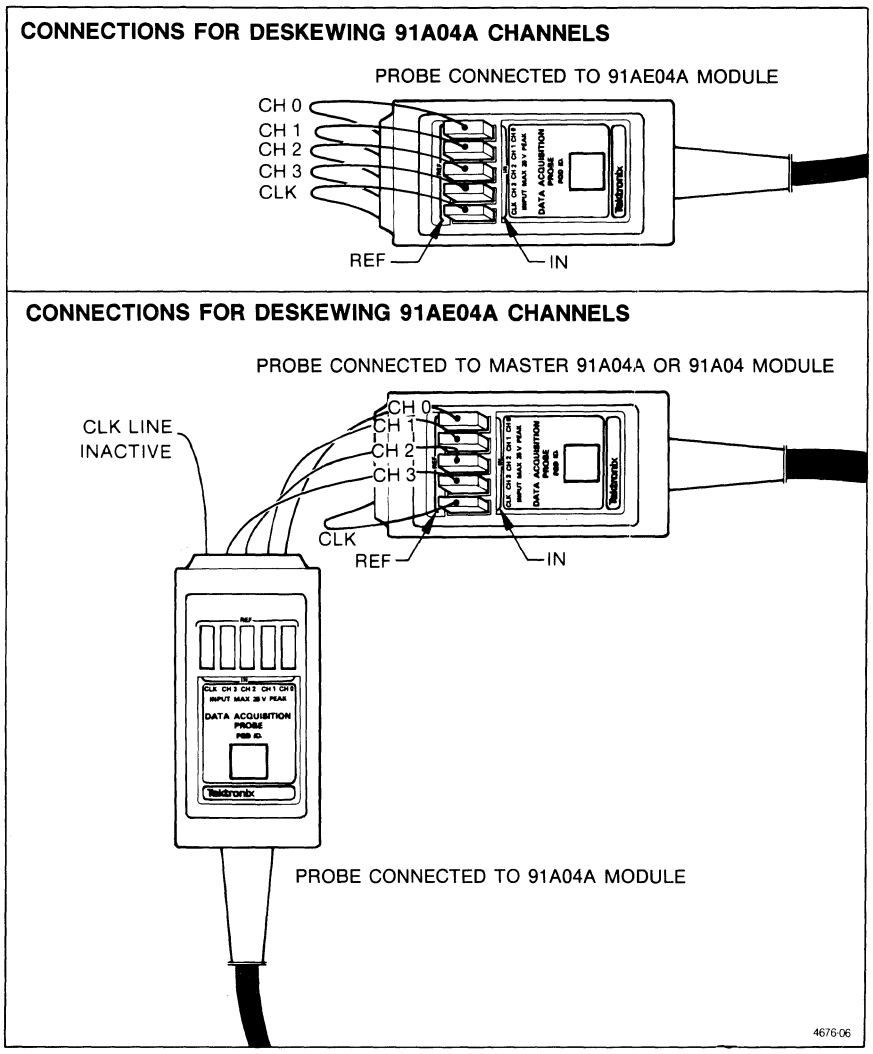


Figure 3-6. Connecting the probe channels for the deskew operation.

TRIGGER SPECIFICATION MENU

The 91A04A, 91A04, 91AE04A, and 91AE04 modules may be used in two modes, as selected in the Trigger Specification menu. They are:

- **91A04 ONLY .** allows acquisition using one master 91A04A or 91A04 module and up to three expander modules. It allows acquisition using 16 parallel data channels at 330 MHz (3 ns), or 8 parallel data channels at 660 MHz (1.5 ns).
- **ARMS 91A04 .** allows acquisition using either 91A24 or 91A32 modules along with 91A04A, 91A04, 91AE04A, and 91AE04 modules. The two types of modules are set at different clock rates to provide a time-aligned display. As in the ONLY mode, the 91A04A, 91A04, 91AE04A, and 91AE04 modules can run at 330 MHz with 16 parallel channels, or at 660 MHz with 8 parallel channels.

The following paragraphs describe these two trigger modes and their parameters.

91A04 ONLY SUB-MENU

Figure 3-7 illustrates a typical 91A04 ONLY sub-menu display and its fields. In this example, one 91A04A and one 91AE04A module are installed in the mainframe.

Refer to the numbered callouts in Figure 3-7 when reading the following field descriptions. These numbers are intended as a visual reference, and do not imply sequence of use.

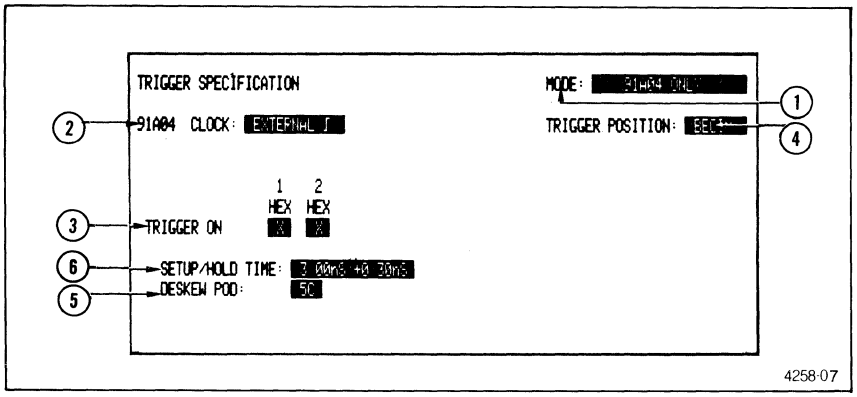


Figure 3-7. The 91A04 ONLY sub-menu and its fields.

(1) MODE Field

The MODE field is used to select between the Trigger Specification menu's available trigger modes. This field only appears in reverse video if more than one type of data acquisition module is installed in the mainframe. The available trigger modes are selected by using the SELECT key.

(2) 91A04 CLOCK Field

The 91A04 CLOCK field is used to specify the rate at which incoming data is sampled and stored in memory. The modules can be set to acquire data using the DAS internal clock set at intervals ranging between 5 ms and 1.5 ns. Or, they can be set to acquire data using an external clock set no faster than 300 MHz.

NOTE

91A04A and 91A04 modules require minimum external-clock duty cycles for acquisition using an external clock. For more information, refer to the Specifications *listed earlier in this addendum.*

In default, the 91A04 CLOCK field is set to the DAS internal clock at 1 μs intervals.

To select the internal clock rate:

Press the INCR key to increase the interval value; press the DECR key to decrease the interval value.

The DAS displays increasing or decreasing values in a 1-2-5 sequence in the range from 5 ms to 5 ns. The last values selected at the low extreme of the clock rate are 3 ns and 1.5 ns.

To select an external clock:

Press the SELECT key.

The DAS displays optional values in this order:

[1μS]
[EXTERNAL ⎍]
[EXTERNAL ⎏]

The external clock is supplied by the master 91A04A or 91A04 module's clock (CLK) channel. The clock channels on the expander modules are ignored.

NOTE

The external clock threshold is determined by the *REF input to the master 91A04A or 91A04 module's CLK channel. Refer to* P6453 Probe Operation *earlier in this addendum.*

Using the High-Resolution (1.5 ns) Mode: When the internal clock is set to 1.5 ns, the modules operate in a high-resolution mode. In this mode, only channels 0 and 2 from each probe are used, but data is acquired at twice the normal resolution. A special data-delay function is implemented on the two channels so that data is sampled at 1.5 ns intervals.

In the high-resolution mode, the module memory depth is increased from 2048 to 4096 words. However, data acquired in the high-resolution mode can only be displayed in the Timing Diagram menu.

(3) TRIGGER ON Field.

The TRIGGER ON field is used to specify the module word recognizer value. This value, when recognized at the probe tips, is then used to generate the acquisition trigger.

If an internal clock, other than the 1.5 ns clock, is used during acquisition, the word recognizer value must be present at the probe tips for one clock cycle plus 2 ns to guarantee correct triggering. When an external clock is used, the word recognizer value must be present at the probe tips for one clock cycle.

When the 1.5 ns internal clock is used, the word recognizer value must be present for 4 ns to guarantee correct triggering.

The number of channels available in this field, as well as their group format and radix, is determined by the Channel Specification menu. Refer to the description of the Channel Specification menu in the *DAS 9100 Series Operator's Manual* for more information.

NOTE

If the 1.5 ns high-resolution mode is used, the number of channels available in the TRIGGER ON field is reduced so that only channels 0 and 2 from each probe are used.

To enter word recognizer values:

Use the data entry keys to enter the desired word value. Don't care values are entered by using the DON'T CARE key.

(4) TRIGGER POSITION Field.

Once a trigger has occurred, the TRIGGER POSITION field determines when the resulting stop/store is generated. It does this by establishing the trigger's position relative to acquisition memory.

Four trigger positions can be selected with this field. The selectable values for 91A04A modules, and for 91A04 modules with firmware version 2, are:

- **BEGIN.** If any data values are specified for word recognition, the trigger is positioned as word 19.

  In high-resolution mode, the trigger is positioned as word 39.

  If all don't care values are specified for word recognition, the trigger is positioned as word 21.

- **CENTER.** If any data values are specified for word recognition, the trigger is positioned as word 1023.

In high-resolution mode, the trigger is positioned as word 2047.

If all don't care values are specified for word recognition, the trigger is positioned as word 1025.

- **END .** If any data values are specified for word recognition, the trigger is positioned as word 2031.

  In high-resolution mode, the trigger is positioned as word 4063.

  If all don't care values are specified for word recognition, the trigger is positioned as word 2033.

- **DELAY .** The trigger can be delayed from 1 to 32,767 clock cycles.

To select the trigger's position in memory:

Press the SELECT key.

The DAS displays optional values in this order:

[BEGIN]
[CENTER]
[END]
[DELAY]

Using the Trigger Delay. If the TRIGGER POSITION field is set to DELAY, a new field appears on the screen. This field is used for specifying the number of clock cycles the trigger will be delayed.

You can specify a delay of up to 32,767 clock cycles by using the data entry keys. The field must be set to a value of at least 1.

NOTE

A delay of 14 clock cycles (28 in high-resolution) is equivalent to the END trigger position, a delay of 1022 (2044 in high-resolution) is equivalent to the CENTER trigger position, and a delay of 2026 (4052 in high-resolution) is equivalent to the BEGIN trigger position.

The DAS searches a small segment of 91A04 data for its trigger word when acquisition stops. Because of this search, certain DELAY values may cause an incorrect trigger indication.

With any clock other than 1.5 ns, and a DELAY value from 2027 to 2040, the actual 91A04 trigger word may no longer be in memory. If the DAS finds a word at the beginning of memory that matches the specified trigger, that word may be marked as the trigger even though the real trigger word is no longer in memory.

An identical situation arises when the 1.5 ns internal 91A04 clock is used. But because of the larger memory, an incorrect trigger may be marked with DELAY values from 4054 to 4080.

(5) DESKEW Field

The DESKEW field is only used during the module deskewing operation. Refer to the *Module Deskewing* discussion earlier in this section for instructions regarding this field. Acquisition specifications cannot be guaranteed through any channel that has not been deskewed.

After all channels have been successfully deskewed, the DESKEW field disappears from the screen.

(6) SETUP/HOLD Field

The SETUP/HOLD field appears only when an external clock source has been selected in the 91A04 CLOCK field and at least one 91A04 channel has been deskewed.

The default setup and hold times for the modules are 3.00 ns setup and 0.30 ns hold. After any 91A04A channel has been successfully deskewed, you can change these setup and hold values by pressing the INCR or DECR keys.

NOTE

The SETUP/HOLD field is only changeable after at least one 91A04A channel listed in the PODS TO DESKEW message has been successfully deskewed. (Refer to Module Deskewing *for more information.)*

ARMS 91A04 SUB-MENU

The ARMS 91A04 mode is used for acquiring data with a slow module, either 91A24 or 91A32 modules, and a 91A04A or 91A04 master module (possibly with expander modules). In this mode, the two types of acquisition modules acquire data simultaneously. In addition, the two types of modules act as linked logic analyzers, where the trigger of the slow module arms the 91A04A or 91A04 trigger.

The ARMS mode supports any valid combination of 91A04A, 91A04, 91AE04A, or 91AE04 modules, armed by either 91A32 modules or 91A24 and 91AE24 modules. All combinations are valid so long as the modules do not exceed their individual limits or the maximum of 104 acquisition channels.

Figure 3-8 shows a typical display of the 91A32 ARMS 91A04 sub-menu. The sub-menu is actually a combination of 91A32 ONLY and 91A04 ONLY sub-menus. The top half of the screen corresponds to the 91A32 ONLY sub-menu, while the bottom half corresponds to the 91A04 ONLY sub-menu.

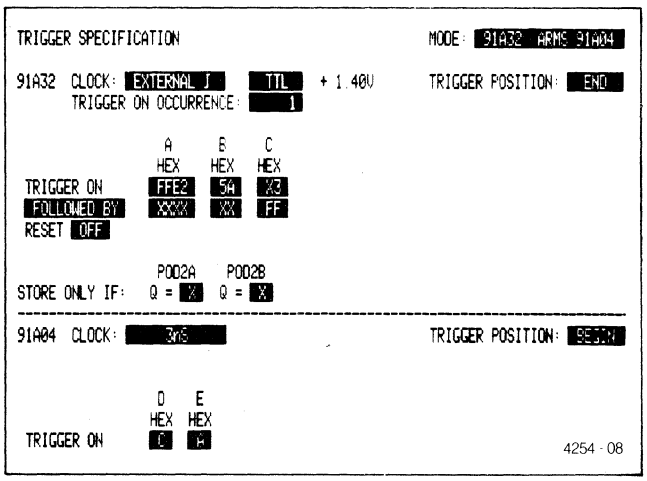


Figure 3-8. Typical 91A32 ARMS 91A04 sub-menu.

The 91A24 ARMS 91A04 sub-menu looks like the 91A24 ONLY sub-menu. To operate the 91A24 ARMS 91A04 mode, enter the 91A04 ONLY Trigger sub-menu and set the 91A04 trigger and acquisition parameters. Then enter the 91A24 ARMS 91A04 sub-menu and set the 91A24 trigger parameters.

With some exceptions, the ARMS mode sub-menu is set up in a manner identical to the procedures described for the 91A32 ONLY and 91A04 ONLY sub-menus. Therefore, detailed setup procedures are not discussed here. Refer to the appropriate portion of this addendum for 91A04 ONLY information. Refer to Section 4 of the *DAS 9100 Series Operator's Manual* for 91A32 ONLY information. Refer to the *91A24, 91AE24, and P6460 Operator's Manual Addendum* for 91A24 ONLY information.

The following paragraphs describe the ARMS 91A04 operating characteristics and restrictions. Read these paragraphs carefully before attempting an ARMS acquisition.

CLOCKING

In ARMS mode, both the fast 91A04-type modules and the slow modules have the same clock capabilities as they have in their respective ONLY modes. For time-aligned data in ARMS mode the 91A04 clock must run at least twice as fast as the clock of the slow module.

NOTE

When the 91A04A or 91A04 is set in the 91A32 ARMS mode, its SETUP/HOLD field disappears from the screen. The setup and hold values for external-clock acquisition remain at the level last specified in the field.

To change the 91A04 SETUP/HOLD field, you must enter the 91A04 ONLY mode. After the desired value is set, you can return to the ARMS 91A04 mode.

TRIGGERING

In the ARMS mode, both types of modules start acquisition at the same time, but the 91A04-type modules are prevented from triggering. The slow trigger occurs first, which then arms the fast 91A04A or 91A04 module to begin looking for its trigger. The fast module trigger is armed within ten cycles of the slow clock following the slow module trigger. The slow module trigger can be delayed up to 32,767 cycles, but to ensure a time-aligned display the trigger should not be positioned outside of memory. (Time alignment can still occur with th slow trigger barely out of memory.)

NOTE

During an ARMS acquisition, only the last 512 words acquired by the 91A04A or 91A04 are displayed in time-alignment with slow data. Therefore, when setting the 91A04 trigger position, the BEGIN, CENTER, and END values are the beginning, center, and end of the last 512 words stored.

CLOCK QUALIFICATION

The clock qualifier lines of the slow modules are available in the ARMS mode. However, to achieve a time-aligned display, no qualifiers should be used.

ARMS ACQUISITION DISPLAY

During the ARMS acquisition, the 91A04A or 91A04 uses its entire memory, but only the last 512 words stored are displayed in time-alignment with slow module data.

NOTE

The TIME ALIGN field is provided in the Timing Diagram menu to allow display of the entire 91A04 memory. Refer to the Timing Diagram Menu *description in this addendum for more information.*

Time Alignment. The armed 91A04 display is only time aligned with the slow module display when the following conditions are met:

1. The slow and fast module triggers must occur so that at least five of the slow clock cycles are overlapped by 91A04 clock cycles.
2. The trigger of the fast module must be in memory. The slow-module trigger does not have to be in memory.
3. If the DELAY field is used in the 91A04 menu, the delay value must be less than 500.
4. The qualifiers of the slow module must be set to don't care. This includes both the data and the clock qualifiers of 91A24 modules.
5. The fast module's clock must be at least twice the speed of the slow module's clock.

If these five conditions are not met by the acquired data, the data display will not be time aligned. Instead, the data from the two modules will be separated in a fence display.

The STOP Key. When the 91A04 is in ARMS mode, and the STOP key is pressed, the DAS may show trigger locations in the State Table and Timing Diagram menus, even though no trigger event occurred.

STATE TABLE MENU

For specific information on how to operate the state table, refer to Section 5 of the *DAS 9100 Series Operator's Manual.* The following paragraphs describe only special display considerations as they apply to 91A04A, 91A04, 91AE04A, and 91AE04 data.

ACQUISITION MEMORY DISPLAY

The state table can be used to display 91A04-type data acquired at clock rates ≤330 MHz (3 ns). Data acquired with the high-resolution, 1.5 ns clock can only be displayed in the timing diagram.

The state table's acquisition memory display shows up to 2048 sequential data words.

ARMS ACQUISITION DISPLAY

In an ARMS acquisition display, only the last 512 words acquired by the 91A04-type modules are displayed.

VARIATION DUE TO CLOCK RATES

If the 91A04 stores identical data at different synchronous clock rates, the acquired data values are the same but the data may reside at different state table sequences. If you have data in your reference memory that was acquired at a different rate than your acquisition memory, the sequences may not match even though the data is the same.

When using the COMPARE functions, store reference memories acquired at the same clock rate to be used during the compare operation.

Internal processing requirements at various synchronous clock rates may also add as many as 15 empty sequences to the beginning of your acquisition. As a result, the highest sequence number in the state table can vary from 2047 to 2062. Be sure to check the actual highest sequence number before storing data in the reference memory.

REFERENCE MEMORY STORAGE

The reference memory can store any sequential section of 91A04 memory, up to and including all 2048 words. However, the reference memory size is limited by the amount of DAS memory used by other modules. For example, if a 91A24 or 91P16 module is installed in the DAS, the reference memory cannot hold the entire 91A04 acquisition memory. Large Define Mnemonics tables also reduce the size of the available reference memory.

The values in the COMPARE field specify which state table sequences are stored in the reference memory. If the limits are too large for the available memory when you press the STORE key, the DAS responds with the error message DECREASE COMPARE LIMITS.

TIMING DIAGRAM MENU

For specific information on how to operate the timing diagram, refer to the Section 6 in the *DAS 9100 Series Operator's Manual*. The following paragraphs describe only special display considerations as they apply to 91A04A, 91A04, 91AE04A, and 91AE04 data.

ACQUISITION DISPLAY

The timing diagram can be used to display 91A04-type data, including data acquired with the high-resolution, 1.5 ns clock.

The timing diagram displays memory data in 512-word blocks. You can see which 512 words are being displayed by setting the MAG (magnification) field to 1. Memory search functions are limited to the 512 words displayed. You can, however, move through the entire 91A04 acquisition memory in the Timing Diagram menu.

To view a new block of 91A04 memory:

Set the MAG field to 1.

Scroll the cursor (C) line to the left to see data towards the beginning of memory, or to the right to see data towards the end of memory. When the cursor reaches the edge of the screen, the menu shifts the cursor back to the center of the screen and shows the next sequential block of 255 words.

When the DAS moves a new block of data onto the timing display, the screen changes. The DAS moves the cursor, and the data the cursor is on, to the center of the display, which requires placing a new timing diagram on the screen.

The DAS moves waveforms behind the cursor when the SHIFT key and a scroll key are pressed simultaneously. The waveform moves until the cursor nears the edge of a 512-word block, then the cursor performs normal unshifted scrolling.

SEARCHING

The SEARCH field in the Timing Diagram menu only searches through the 512-word block currently available for display.

To search through 91A04 memory:

Assuming the 91A04 data is displayed on the top four lines of the timing diagram, enter the search value into the four leftmost bits in the SEARCH field. Press the SEARCH key.

If the cursor is initially located in the first 256 words of the 91A04 memory, the cursor moves to the first occurrence of the word in the entire 512-word block.

If the cursor is not in the first 256 words when you press the SEARCH key, the DAS searches from the original position of the cursor to the end of the current 512-word block. The DAS will never search outside of the currently available 512-word block.

ARMS ACQUISITION DISPLAY

During an ARMS acquisition, only the last 512 data words acquired by the 91A04-type modules are displayed in time-alignment with data from the slow module. You can view the rest of 91A04 memory by using the TIME ALIGN field. This field lets you switch from viewing ARMS mode data to viewing all of 91A04 memory.

As shown in Figure 3-9, the TIME ALIGN field is located in the center of the top line of the display.

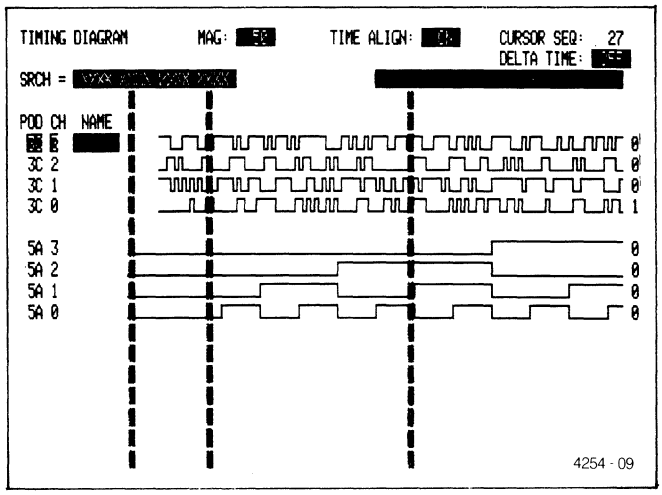


Figure 3-9. 91A32 ARMS 91A04 display in the Timing Diagram menu.

To turn off the time-aligned display:

Move the cursor to the TIME ALIGN field.

Press the SELECT key.

The DAS displays optional values in this order:

[ON]
[OFF]

If the field is ON, the data is shown time-aligned with data from the slow module.

If the field is OFF, all of the 91A04 memory that contains valid data is available for display.

GPIB PROGRAMMING

The 91A04A and 91AE04A modules add parameters to the ACQMEM and BOARDS? commands of the DAS Option 02 GPIB language as described in the *DAS 9100 Series Operator's Manual.* No other Option 02 GPIB commands described are affected.

GPIB commands available with DAS Option 06 are not affected by 91A04A and 91AE04A modules.

ACQMEM COMMAND

The ACQMEM command can be used to retrieve 91A04A, 91A04, 91AE04A, or 91AE04 memory data. The command format is:

ACQMEM <slot>

The <slot> argument is a decimal number identifying the bus slot where the 91A04-type module is installed.

A typical example of this command is:

ACQMEM 3 - this tells the DAS to be ready to send the memory contents of the module residing in bus slot 3.

The specified memory is sent back to the controller after the following query command is sent to the DAS:

ACQMEM? - this tells the DAS to send the specified memory contents to the controller.

The DAS response to the query is in the following format:

ACQMEM %<bytecount><data bytes><checksum>;

where:

<bytecount> is a 16-bit byte count (sent as two 8-bit bytes, high-order byte first), indicating the number of data bytes that follow;

<data> is the packet of data bytes; and

<checksum> is the two's complement of the arithmetic sum (modulo 256) of all bytes following the % sign.

NOTE

If the data being retrieved was acquired at 1.5 ns, interleave the data on bits 0 and 1, and on bits 2 and 3. This will achieve a two-channel format similar to the timing diagram display.

If you are reading data acquired with the 1.5 ns internal clock, bits 1 and 3 were acquired 1.5 ns before the data in bits 0 and 2. So, to interleave the data for a timing diagram display, display bit 1 to the left of bit 0, and display bit 3 to the left of bit 2.

BOARDS? COMMAND

In the BOARDS? command, all 91A04-type modules have a board value of 83.

MODULE ADJUSTMENT PROCEDURES

IMPORTANT INFORMATION

PRECAUTIONS

Some DAS modules require adjustments to match them to the mainframe or to other modules in the system. The adjustment procedures for the modules in this addendum requiring an operator-performed adjustment, are described in this sub-section.

WARNING

Access the mainframe's module compartment only. Other compartments within the mainframe contain hazardous voltages.

Do not place your fingers on components while the mainframe is turned on. DAS circuit boards and components can become very hot during operation.

Do not allow metal jewelry to come in contact with circuit components. A short between components could cause the jewelry to become very hot.

CAUTION

Instrument modules can be damaged if removed or installed while the mainframe is receiving power. To avoid damage, turn off the mainframe.

Remove loose objects from the mainframe. During installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the primary power supply, do not power up the instrument until such objects have been removed.

NOTE

Tektronix Service Centers have the necessary equipment and personnel to perform any of the adjustments described in this subsection. If you desire, a service center can perform any of these adjustments for you.

If you send a module to a service center for adjustment, be sure to include all parts necessary for the adjustment. These may include other modules, the mainframe, probes, and cables. A list of these parts is provided in the adjustment procedure for your module.

LIMITS AND TOLERANCES

All limits and tolerances given in these procedures are adjustment guides; they should not be interpreted as instrument specifications.

Tolerances given are for the instrument under test and do not include test instrument error.

EQUIPMENT

The equipment required to adjust each module is provided in a table with the procedure for each module. The specifications given in these tables are the minimum necessary to produce accurate results. Therefore, any substituted equipment must meet or exceed the listed specifications. Refer to the manual of the specific test instrument if more information is required.

When equipment other than recommended test equipment is substituted, control settings or adjustment setups may need to be altered. If the exact equipment listed in the table is not available, check the specifications column of the table carefully to make sure the substitute equipment is adequate.

91A04A ADJUSTMENT PROCEDURE

You must change the placement of one jumper on the 91A04A Data Acquisition Module whenever expander modules are added to or removed from the system. Proper placement of this jumper increases the reliability of the 91A04A module. The location of the jumper is shown in Figure 3-10.

The 91A04A adjustment should be performed under the following conditions:

- **Installation** — You should adjust the 91A04A when the module is first installed in a mainframe. If the 91A04A module was installed at the factory, the adjustment has already been performed.
- **Adding or Removing Expander Modules** — You must change the 91A04A adjustment when expander modules are added to a 91A04A that previously did not have expanders. The adjustment must also be changed if a 91A04A module that was previously running expander modules has all expander modules removed.

To make the adjustment, you must first decide whether or not the 91A04A module will be connected to any expander modules. You must change the position of a jumper, depending on whether expander modules are used.

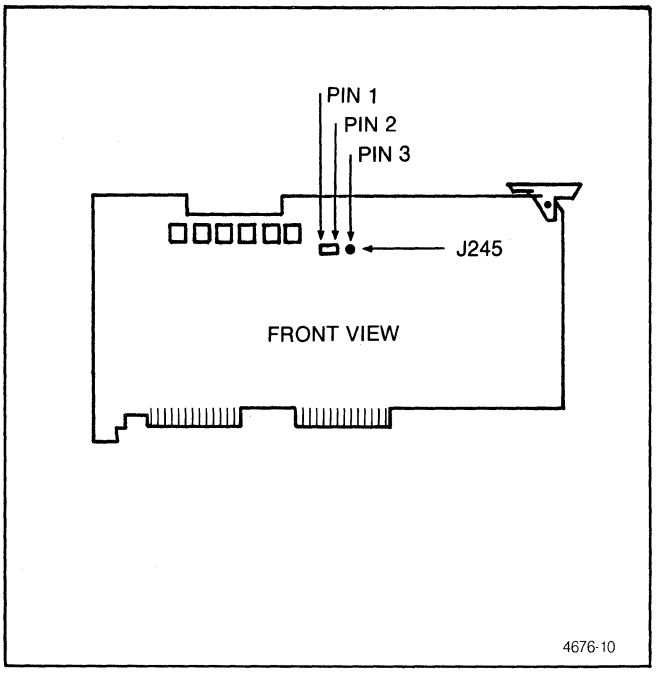


Figure 3-10. Location of jumper J245 on 91A04A modules. If expanders are used with the 91A04A, place the jumper on pins 1 and 2. If the 91A04A module is used alone, place the jumper on pins 2 and 3.

CAUTION

Do not install or remove modules in a DAS mainframe while the mainframe power is on. Doing so may damage the module or the mainframe.

1. Turn off power to the DAS mainframe.
2. Pull the 91A04A out of the two plugs on the bottom of the mainframe. You do not need to disconnect any cables.
3. Without disconnecting any cables, raise the 91A04A module about 5 cm (2 inches) out of the mainframe. J245 should be above the top of the mainframe.
4. Remove the black plastic rectangular jumper from the pins of J245. If the 91A04A is to be used with expander modules, install the jumper on pins 1 and 2 of J245. If the 91A04A is to be used without expander modules, install the jumper on pins 2 and 3 of J245.
5. After the jumper is firmly installed on the correct pins of J245, press the 91A04A module back into the mainframe. The module is in place when it is flush with the tops of the other installed modules.

The 91A04A module is now ready to be used.

91AE04A ADJUSTMENT PROCEDURE

91AE04A Data Acquisition Module adjustment consists of making one voltage measurement and moving one jumper. The placement of this jumper depends on the difference between the +5 V levels of the 91AE04A and the master module.

The 91AE04A adjustment should be performed under the following conditions:

- **Installation** — The 91AE04A adjustment should be performed when the 91AE04A module is first installed in a mainframe. If the 91AE04A module was installed at the factory, the adjustment has already been performed. If the 91AE04A module was ordered separately from the mainframe, perform the adjustments after you have installed the 91AE04A modules and connected their cables to the master 91A04A or 91A04.
- **Slot Position Changes** — The validity of the 91AE04A adjustment depends on the DAS slots used during the adjustment. The 91AE04A adjustment only needs to be performed once so long as all 91AE04A modules remain in the slots they are adjusted to. The master 91A04A or 91A04 module must also stay in the slot used during the adjustment. You must perform the adjustments again if you move any of these modules to different slots.
- **Power Supply Changes** — If any of the +5 V Power Supplies for the 91AE04A modules are changed or replaced, the adjustment must be performed. Also, if the +5 V supply for the master 91A04A or 91A04 module is changed or replaced, the adjustment must be performed on all 91AE04A modules.

The adjustment requires the equipment shown in Table 3-5. The location of the jumper used in the adjustment is shown in Figure 3-11.

Table 3-5
EQUIPMENT REQUIRED FOR 91AE04A ADJUSTMENT

EQUIPMENT	SPECIFICATIONS	EQUIVALENT TETRONIX EQUIPMENT
91A04A or 91A04 Data Acquisition Module	Master module for the 91AE04A during the adjustment and for subsequent use	
Digital Multimeter (DMM)	3.5 digits, 0.1% resolution with floating inputs	Tektronix DM502A Digital Multimeter with a TM 500 mainframe
Test leads for the digital multimeter	Equipped with retractable hook tips	positive lead, 012-042600; negative lead, 012-25-00; retractable hook tips, order two of 013-0107-00
Square pin jumper	0.1 inch centers	131-0993-00

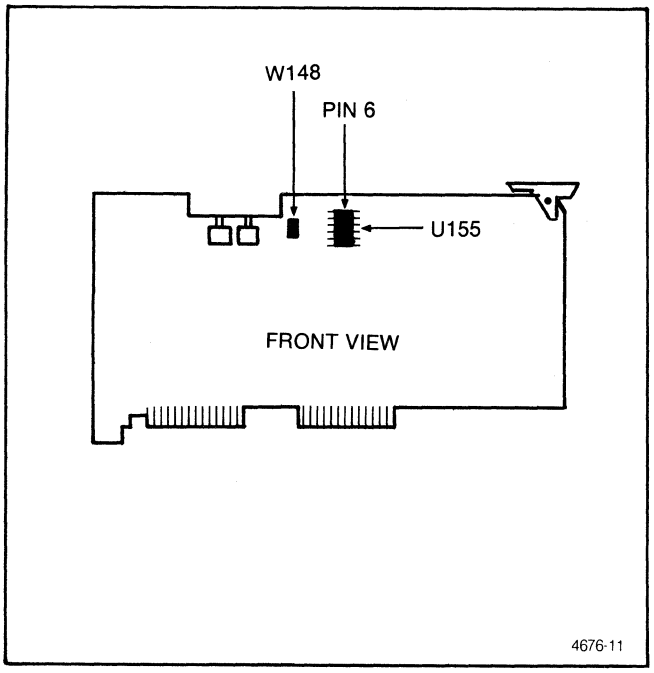


Figure 3-11. Location of jumper W148 and IC U155 pin 16 on 91AE04A modules. If the measured voltage is between −75 mV and +25 mV, place the jumper on W148. If the measured voltage is between +25 mV and +75 mV, remove the jumper.

To make the adjustment, you must first install all 91AE04A modules in the mainframe, and connect them to the 91A04A or 91A04 master module. Then connect the digital multimeter (DMM) between the +5 V supply of the master and the +5 V supply of the 91AE04A. The mainframe is then turned on and the difference between the two supplies is indicated by the DMM. The jumper on W148 is replaced or removed depending on the reading from the DMM.

Perform the following steps to accomplish this adjustment:

CAUTION

Do not install or remove modules in a DAS mainframe while the mainframe power is on. Doing so may damage the module or the mainframe.

1. Turn off power to the DAS mainframe.
2. Install all 91AE04A and 91AE04 modules in the mainframe. Position the modules thoughtfully, because the 91AE04A modules must remain in these slots for the adjustment to remain valid.
3. Install the master 91A04A or 91A04 module in the mainframe. Make sure that all the modules meet the conditions given in *Configuration Requirements* earlier in this section.
4. Connect all cables between the modules as described in *Module Installation* earlier in this section.
5. Before turning on the mainframe, connect the negative lead of the DMM to pin 16 of U155 on the master module.
6. Connect the positive lead of the DMM to pin 16 of U155 on one of the 91AE04A modules.
7. Turn on the DAS mainframe and the DMM. Set the DMM to 200 mV full range, and record the voltage indicated by the DMM.
8. Turn off the mainframe and disconnect the DMM from the 91AE04A module just measured.
9. Lift the measured 91AE04A module about 5 cm (2 inches) out of the mainframe. If the measured voltage was between −75 mV and +25 mV, place the jumper on W148. If the measured voltage was between +25 mV and +75 mV, remove the jumper from W148.
10. Press the adjusted 91AE04A module back into the mainframe. The module is in place when it is flush with the tops of the other installed modules.
11. Repeat steps 6 through 10 for each 91AE04A module in the system.
12. After all 91AE04A modules have been adjusted, remove the DMM leads from the last 91AE04A module and from the master module.

All 91AE04A modules are now ready for use. The adjustment just completed will remain valid so long as the master module and all 91AE04A modules remain in the same slots of the mainframe and no +5 V power supplies are replaced or moved.

91AE04 ADJUSTMENT PROCEDURES

NOTE

Do not perform the 91AE04 adjustment on modules with serial numbers B010118 and up. New circuitry on these modules has eliminated the need for this adjustment.

91AE04 modules with lower serial numbers may also have been modified at a service center to include the new circuitry. R495 is removed from the module during the modification. Modules without R495 do not require the adjustment.

To meet high-speed clock specifications, 91AE04 modules must be adjusted to the master 91A04A or 91A04 module's clock.

The 91AE04 adjustment should be performed under the following conditions:

- **Installation** — The 91AE04 clock adjustments should be performed when the 91AE04 modules are first installed in a mainframe. If the 91AE04 modules were installed at the factory, the adjustments have already been performed. If the 91AE04 modules were ordered separately from the mainframe, perform the adjustments after you have installed the 91AE04 modules and connected their cables to the 91A04.
- **Cable Connection Changes** — The validity of the 91AE04 clock adjustment depends on the clock-cable connection used during the adjustments. The 91AE04 clock adjustments need only be performed once, but the cable transmitting the clock from the 91A04 to the 91AE04 must always use the same connectors that are used during the adjustment. You must perform the adjustments again if you use connectors other than those used in the original clock-cable connection.

The adjustment requires the equipment shown in Table 3-6. The location of the test points and trimmer potentiometer used in the adjustment is shown in Figure 3-12.

Table 3-6
EQUIPMENT REQUIRED FOR 91AE04A ADJUSTMENT

EQUIPMENT	SPECIFICATIONS	EQUIVALENT TEKTRONIX EQUIPMENT
91A04A or 91A04 Data Acquisition Module	Master module for the 91AE04 during the adjustment, and for subsequent use	
Digital multimeter (DMM)	3.5 digits, 0.1% resolution with floating inputs	Tektronix DM502A Digital Multimeter with TM 500 mainframe
Test leads for the digital multimeter	Equipped with retractable hook tips	Positive lead, 012-0426-00; negative lead 012-0426-00; retractable hook tips, order two of 013-0107-00
Adjustment tool (plastic-bladed screwdriver)		003-0301-00

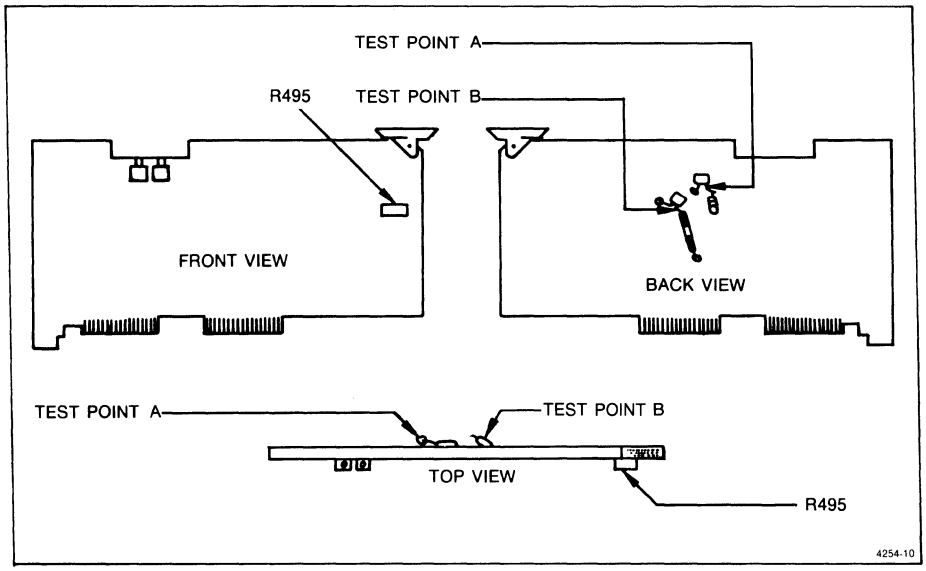


Figure 3-12. Location of trimmer potentiometer R495 and test points on 91AE04 modules.

To make the adjustment, you must first install all 91AE04A modules in the mainframe, and connect them to the 91A04A or 91A04 master module. Then use the digital multimeter to monitor the voltage between two points while adjusting trimmer R495.

Perform the following steps to accomplish this adjustment:

CAUTION

Do not install or remove modules in a DAS mainframe while the mainframe power is on. Doing so may damage the module or the mainframe.

1. Turn off the DAS mainframe.
2. Install the master 91A04A or 91A04 module that will be driving the 91AE04 module if it is not currently in the mainframe. Be sure to follow any installation restrictions noted earlier in this section under *Configuration Requirements*.
3. Install all 91AE04 modules to be adjusted in the desired locations of the DAS mainframe (following any installation restrictions).
4. Locate the two 3-inch coax cables and the 3.5-inch threshold jumper cable that come with each 91AE04 module. Connect these cables between all of the 91AE04 modules and the 91A04 module. Directions for these cable connections are found in the *Module Installation* subsection of these *Operating Instructions*.

NOTE

Do not connect P6453 probes to the 91AE04 modules during these procedures. The probes are disconnected to prevent the DAS from triggering during the adjustment.

5. Turn on the DAS mainframe. All the 91AE04 modules should pass the diagnostic tests. If the diagnostics do not pass, check all cable connections between the 91AE04 modules and the master module.
6. Turn off the DAS mainframe.

CAUTION

Failing to turn off the DAS mainframe at this point may result in damage to the 91AE04 module being adjusted.

7. Turn on the DMM. Set the DMM to 200 mV dc full range.
8. Choose the 91AE04 module you want to adjust. Locate the two test points on the back (solder side) of the module as indicated in Figure 3-12. These test points are each located at the junction of a capacitor and a resistor soldered to the back of the board.
   - **Test point A** is located between a capacitor and a resistor on the solder side of the circuit board. The lead running between the capacitor and the resistor is a short, exposed solder connection.
   - **Test point B** is also at the junction of a capacitor and a resistor, but the resistor lead is long and covered with insulation.
9. Connect the positive gripper-tipped lead of the DMM to test point A, as shown in Figure 3-12. Connect the negative DMM lead to test point B as shown in Figure 3-12.
10. Turn on the DAS mainframe. Enter the Trigger Specification menu. Set the MODE field to 91A04 ONLY. Set the 91A04 CLOCK field to 3 ns.
11. Fill the TRIGGER ON field in the Trigger Specification menu with all Fs. This, in combination with the disconnected data acquisition probe, prevents the 91AE04 module from triggering during the adjustment.
12. Press the START SYSTEM key to let the clock enter the 91AE04 module from the 91A04 module. The DAS screen shows the message WAITING FOR 91A04 TRIGGER.

WARNING

Do not place your fingers on components while the mainframe is turned on. DAS circuit boards and components can become very hot during operation.

Do not allow metal jewelry to come in contact with circuit components. A short between components could cause the jewelry to become very hot.

13. Locate trimmer potentiometer R495 on the component side of the 91AE04 module (as indicated in Figure 3-12). Using the plastic-bladed screwdriver, adjust R495 until the digital multimeter reads between −5 mV and +5 mV. Optimally, the DMM should read 0 mV.
14. Turn off the DAS mainframe.

CAUTION

Failing to turn off the DAS mainframe at this point may result in damage to the 91AE04 module being adjusted.

15. Disconnect the DMM test leads from the back of the 91AE04 module.
16. If you have performed this adjustment on all of the 91AE04 modules in your system, you may turn off and disconnect any test equipment used during the adjustments. If any 91AE04 modules have not yet been adjusted, return to step 8 and perform all subsequent steps on that module.

All of the 91AE04 modules in your mainframe have now been matched to the master module. To maintain the adjustment, do not change the order in which the clock cables are connected between the modules.

Section 4

THEORY OF OPERATION

ORGANIZATION

The theory of operation is presented to familiarize service personnel and others with both general and specific circuit operation of the 91A04A and 91AE04A data acquisition modules, and of the P6453 probe. There are three main subsections covering the theory of operation.

- The first subsection *(Overview: Functions and Acquisition Cycle)* describes large-scale interactions between 91A04A and 91AE04A modules, between modules and P6453 probes, and between 91A04A Series module combinations and the DAS cards and mainframe.
- The second subsection (*General Description)* is a general, or block-diagram-level, description of the 91A04A and 91AE24A modules. Refer to the 91A04A and 91AE04A block diagram in the *Diagrams* section of this addendum while reading this subsection.
- The third subsection (*Detailed Circuit Description*) describes in detail the individual circuits in the modules. The numbers in diamonds in the headings of this subsection refer to specific schematics in the *Diagrams* section of this addendum.

LOGIC CONVENTIONS

Most of the circuitry in the 91A04A and 91AE04A modules is digital. Digital circuit functions are represented using standard digital notations and symbols.

Logic is described with the positive logic convention. Positive logic is a system of notation where the more positive of two voltage levels is the true (or high) state; the more negative voltage is the false (or low) state. The specific voltages that constitute a high or low state may vary, depending on the specific digital logic family.

Whenever a line name on a schematic is referred to in the following text, that line name is followed by either (H) or (L). If the schematic line name has an overscore (is asserted low), that line name is followed by (L) when it is found within this text. If the line name does not have an overscore, the line name is followed by (H) when it is called out in text to show that the line is asserted high.

OVERVIEW: FUNCTIONS AND ACQUISITION CYCLE

91A04A Data Acquisition Modules acquire four channels of data at rates up to 330 MHz. 91A04A and 91AE04A modules each have a memory depth of 2048 words.

91AE04A Data Acquisition Modules are slaves to the 91A04A module; each acquires an additional four channels of data at the same rate as the master 91A04A. Up to three 91AE04A modules can be slaved to a 91A04A for a total of 16 parallel channels of acquisition.

P6453 Data Acquisiton Probes provide the interface between the circuit under test and 91A04A and 91AE04A modules. Each probe can acquire four channels of data. The input impedance of each channel is 1 MΩ paralleled by 5 pF. Each probe channel is effectively a 330 MHz linear amplifier/buffer.

The module-probe combination also has a special deskewing feature. Using this feature, 91A04A and 91AE04A modules can adjust for differences in transit time between probe channels.

91A04A/91AE04A OPERATION

In systems where more than four channels of acquisition at up to 330 MHz are required, 91AE04A modules must be added to the original 91A04A module.

Prior to starting acquisition, the 91A04A and all 91AE04A modules are given their initial parameters by the Controller board. These parameters include such information as the clock to be used, the clock edge, the words to be recognized, and the number of clock cycles to delay the trigger.

When data acquisition is started, the 91A04A starts its own clock and the clocks of the 91AE04A modules. One word of data is acquired by all modules with each active edge of the selected clock.

During each acquisition cycle, the four-bit word acquired is compared to the portion of the trigger word acquired by each module. Whenever a module acquires four bits of data equal to its portion of the trigger word, the module sends a signal to the 91A04A indicating recognition. If all modules in the system (the 91A04A and all 91AE04As) recognize their portions of the trigger at the same time, then the trigger sequence is initiated by the 91A04A.

The 91A04A trigger sequence starts with the recognition of the trigger word by all 91A04A and 91AE04A modules. When this occurs, the delay counter starts. The delay counter activates a STOP STORE sequence after a predetermined number of clock cycles. When the delay counter completes its task, the 91A04A module stops the clock, both to itself and to the 91AE04A modules in the system. Stopping the clock stops data acquisition.

The 91A04A module now signals the mainframe that acquisition is completed and that data can be read back by the Controller.

INTERFACE BETWEEN MODULES AND THE DAS MAINFRAME

The interface between the DAS mainframe and the 91A04A and 91AE04A is like the interfaces between the mainframe and other DAS data acquisition modules. When the 91A04A is to be armed by a slow card, such as a 91A32 module, the word recognizers of the 91A04A and 91AE04A are effectively disabled until the slow card has completed its trigger sequence. The word recognizer on the 91A04A module is then enabled so that the 91A04A can start its trigger sequence.

INTERFACE BETWEEN 91A04A AND 91AE04A MODULES

The 91AE04A expander modules are etched circuit board assemblies that are slaved to the 91A04A master module. Each 91AE04A allows an additional four channels of data with a memory depth of 2048 words, and with word recognition for triggering.

Clocks are distributed to all 91AE04A expander modules in the system from the 91A04A master module. Word recognizer signals are sent from all expander modules in the system to the master module where they are combined with the master module's word recognizer signals.

GENERAL DESCRIPTION

When reading the following description, refer to the 91A04A, 91AE04A, and P6453 probe block diagram. This block diagram is located in the *Diagrams* section at the back of this addendum.

P6453 DATA ACQUISITION PROBE

The P6453 is a five-input active probe that is used with the 91A04A and 91AE04A Data Acquisition Modules. All five inputs are used when the probe is connected to a 91A04A: four channels of data and an external clock. The 91AE04A uses only the four data channels.

Each input to the probe requires two connections: a reference input and a signal input. The reference input acts as a floating ground. For more information about connecting the signal and reference lines of the probe, see the *Operating Instructions* section of this addendum. Refer also to the *Module to P6453 Probe* description at the end of this *General Description* subsection.

91A04A DATA ACQUISITION MODULE

The 91A04A is the master module of a 91A04A/91AE04A system.

91A04A Controller Interface and ROM

The controller interface is the means of communication between the DAS mainframe's Controller and the 91A04A. The interface accepts and stores information written from the Controller and also provides data for the Controller when called for. All blocks in the 91A04A portion of the DAS 91A04A and 91AE04A block diagram identified with an asterisk (*) are connected to the module controller interface. The firmware in the 91A04A is contained in two 8K EPROMs, one for operating code and one for diagnostics.

Probe Receivers

Each incoming signal from the 91A04A's P6453 probe is converted from probe levels to +5 V referenced ECL by the probe receiver comparators. The probe receivers get threshold information from an eight-bit, high-accuracy, digital-to-analog converter (DAC). Because of the 10X attenuation of the P6453 probe, each receiver has a trimmer resister to null out offsets.

Deskew Circuits

The deskew circuits are programmable delay lines. During deskew operations, the DAS mainframe Controller calculates the amount of delay necesssary for each data line from the probe to make set-up and hold specifications. The Controller then programs the deskew circuits to insert the proper amount of delay in the data signal path. Refer to the *Interface Between the Module and the P6453 Probe* discussion for additional information.

Clock Select and Control

This block selects the clock that will drive the 91A04A and 91AE04A modules. The choices are: 3 ns internal, 5 ns internal, 91A08 internal (from the Trigger/Time Base), the 91A04A probe clock, and rising or falling edge. This block also shuts down the clock when the trigger sequence is completed. All blocks identified with an A on the DAS 91A04A and 91AE04A Block Diagram receive clock signals from the clock select and control block.

Login Registers

The login registers are the first clocked element the data encounters. The channel-to-channel skew, the setup and hold times, and the HI-RES mode resolution are determined by the data-clock timing at these registers. Also, the Arms mode clock (91A32 CLOCK) is logged in by these registers (on the 91A04A only, not on the 91AE04A).

Eight-Phase Clock Generator

The acquisition memory consists of eight sequential stages. Each stage requires its own properly timed clock. This clock generator creates the required timing clocks for the acquisition memory and memory address registers using the outputs of the clock select and control circuit.

Memory Address Registers

The memory address registers provide addresses for the acquisition memory. To satisfy all eight stages of the acquisition memory, the memory address must be provided in four stages. Each address stage provides an address for two stages in the acquisition memory. The memory address registers consist of a counter, which provides the address for acquisition memory stages 1 and 2, and three eight-bit latches, each of which provides the address for two more memory stages.

Write Enable Generator

The write enable generator creates eight separate write enable signals from the 91A04A clock. Each of the eight stages of the acquisition memory receives its own, properly timed, write enable pulse from the write enable generator. The write enable generator consists of an eight-bit shift register that is clocked by the clock select and control block.

3 ns and 5 ns Clock Generator

The 3 ns and 5 ns internal clocks for the 91A04A are generated in this block. Any internal clock rate between 10 ns and 5 ms is taken from the DAS mainframe's Trigger/Time Base module.

Acquisition Memory and Clock Array RAMs

The 2K X 4 acquisition memory matrix is where all acquired data is stored for readback by the DAS mainframe's Controller. To meet setup and hold requirements of the acquisition RAM, the memory is organized into eight recycling stages. Each 256 X 4 RAM stores every eighth four-bit word acquired, then the next memory in the sequence stores the following word.

In order to time align 91A04A data with data acquired by slow cards, the 91A32 CLOCK is also stored in the clock array RAMs. Rising edges on the 91A32 CLOCK are then read back by the DAS mainframe's Controller and correlated to data storage by the 91A04A and the slow cards.

Word Recognizer

The 91A04A word recognizer monitors the output of the login registers. When all four bits of the desired trigger word assigned to the 91A04A are output by the login registers, the word recognizer goes true. Any word recognition signals from 91AE04A modules (up to three) are then simultaneously combined with the 91A04A's recognition signal to produce a 16-bit word recognition.

Trigger

The trigger circuit logs in the go-ahead signal from the word recognizer, then tells the delay counter to start.

Delay Counter

The delay counter, once programmed by the controller interface, determines the number of clock cycles (up to 32,767) the stop acquisition signal is delayed after the trigger is satisfied. The counter is loaded with the one's complement of the delay count, and then counts up to all ones to stop acquisition.

Difference Counter

The difference counter counts the number (up to 500) of 91A32 CLOCK cycles between the slow-card trigger and the 91A04A trigger. This information is then made accessible to the controller interface. The Controller board uses this information to ensure correct timing alignment when both 91A04A and slow-card data is displayed in ARMS mode.

91AE04A DATA ACQUISITION MODULE

The 91AE04A is the slave of a 91A04A/91AE04A system. 91AE04A modules acquire an extra four channels of data for a 91A04A system.

The 91AE04A is essentially a depopulated 91A04A. Many circuit functions are identical on the two boards. Duplicate block descriptions (with essential differences) are included below for convenience.

91AE04A Controller Interface

The controller interface is the means of communication between the DAS mainframe's Controller and the 91AE04A. The interface accepts and stores information written from the Controller and also accesses data for the Controller when called for. All blocks identified with an asterisk (*) on the DAS 91A04A and 91AE04A Block Diagram are connected to the module controller interface. The 91AE04A controller interface is a subset of the 91A04A controller interface. Functions handled by the master 91A04A controller interface are eliminated from the 91AE04A.

Probe Receivers

Each incoming signal from the 91A04A's P6453 probe is converted from probe levels to +5 V referenced ECL by the probe receiver comparators. The probe receivers get threshold information from an eight-bit, high-accuracy, digital-to-analog converter (DAC). Because of the 10X attenuation of the P6453 probe, each receiver has a trimmer resister to null out offsets.

Deskew Circuits

The deskew circuits are programmable delay lines. During deskew operations, the DAS mainframe Controller calculates the amount of delay necesssary for each data line from the probe to make set-up and hold specifications. The Controller then programs the deskew circuits to insert the proper amount of delay in the data signal path. Refer to the *Interface Between the Module and the P6453 Probe* discussion for additional information.

Login Registers

The login registers are the first clocked elements the data encounters. The channel-to-channel skew, the setup and hold times, and the HI-RES mode resolution are determined by the data-clock timing at these registers. The Arms mode clock (91A32 CLOCK) is not logged in by these registers in the 91AE04A.

Eight-Phase Clock Generator

The acquisition memory consists of eight sequential stages. Each stage requires its own properly timed clock. This clock generator creates the required timing clocks for the acquisition memory and memory address registers using the outputs of the clock select and control circuit.

Memory Address Registers

The memory address registers provide addresses for the acquisition memory. To satisfy all eight stages of the acquisition memory, the memory address must be provided in four stages. Each address stage provides an address for two stages in the acquisition memory. The memory address registers consist of a counter, which provides the address for acquisition memory stages 1 and 2, and three eight-bit latches, each of which provides the address for two more memory stages.

Write Enable Generator

The write enable generator creates eight separate write enable signals from the 91A04A clock. Each of the eight stages of the acquisition memory receives its own, properly timed, write enable pulse from the write enable generator. The write enable generator consists of an eight-bit shift register that is clocked by the clock select and control block.

Clock Buffers

The clock buffers receive a +5 V referenced ECL clock signal from the master 91A04A module, and then transmit the clock to all necessary blocks of the 91AE04A. Any block in the 91AE04A diagram identified with an A on the DAS 91A04A and 91AE04A Block Diagram receives a clock signal from this block. This clock buffer also contains a level shifter to compensate for voltage differences between the 91A04A and the 91AE04A +5 V power supplies.

Acquisition Memory

The 2K X 4 acquisition memory matrix is where all acquired data is stored for readback by the DAS mainframe's Controller. To meet setup and hold requirements of the acquisition RAM, the memory is organized into eight recycling stages. Each 256 X 4 RAM stores every eighth four-bit word acquired, then the next memory in the sequence stores the following word.

Word Recognizer

The 91AE04A word recognizer monitors the output of the login registers. When all four bits of the desired trigger word assigned to the 91AE04A are output by the login registers, the word recognizer goes true. The word recognition signal is then sent to the 91A04A module at +5 V referenced ECL levels to complete triggering.

MODULE TO P6453 INTERFACE

The P6453 probe is a five-channel 330 MHz linear voltage-to-current converter. Each channel of the probe has its own hybrid amplifier, located in the small box at the end of each cable. Each hybrid has two inputs: data and reference. The data line carries the data or clock signal acquired. The reference line is the ground or logic reference in the system under test. The reference line of each channel must be connected individually to the reference of the circuit under test.

NOTE

Each reference input to the probe is independent of the DAS ground. The DAS threshold setting locates the logic threshold above or below each separate reference voltage, not above or below the DAS ground.

Each of the five channels has a separate coaxial cable that runs from the hybrid to the module. The hybrid receives power from the DAS and transmits back the acquired data over this cable. To power the hybrid, the DAS +5 V and ground is used, as well as the shield at +15 V and the inner channel conductor at approximately +3.75 V. The hybrid acts as a voltage-to-current converter and voltage divider that converts at 2 mA/V sensitivity. It then sends this signal back to the module at 15 mA static current referenced to the +3 VL power supply. Each channel is then terminated by a precision 50 Ω resistor to convert the current back to a voltage level.

The probe also has a deskewing feature, located in the large plastic housing from which the individual data cables originate. The 91A04A sends a pulse to the probe housing. This pulse is distributed to all of the probes connected to the deskewing fixture. The module then detects the difference in arrival time at the login register between the signal received by the clock line and the data lines. The module then adds or subtracts delay to all necessary lines to find the center of the setup and hold times. An UNABLE TO DESKEW message is generated if the module cannot meet setup and hold requirements. The deskewing is changed on all modules when the 91A04A is running on internal timebase so that all channels arrive at the login registers at the same time.

P6453 DATA ACQUISITION PROBE

The P6453 Data Acquisition Probe is used by 91A04A and 91AE04A data acquisition modules. The probe acquires four channels of data when connected to either a 91A04A or a 91AE04A. The probe can also acquire an external clock signal when it is connected to a 91A04A module.

All of the component numbers in the P6453 probe circuit description are assumed to have an A27 or an A27A1 prefix unless otherwise noted. Refer to the P6453 schematic (schematic 67) in the *Diagrams* section of this addendum while reading this circuit description. Due to the simplicity of the schematic, no block diagram is supplied.

The data-receiving portion of the probe consists of five hybrid circuits. The hybrids act as 1 MΩ 5 pF inputs, differential 50 Ω output, and 10X FET probes. The two inputs to each hybrid, IN and REF, perform the same function as the signal and ground inputs of standard probes. The only exception is that REF may be referenced to a dc voltage. This exception changes the input impedance to 500 KΩ with reference to ground. The hybrid output tracks the input with respect to the reference level.

When the POD ID button, S01, on the probe housing is depressed, an active low signal is sent to the attached acquisition module. This active low signal allows the DAS screen to indicate which module the probe is attached to.

DETAILED CIRCUIT DESCRIPTION

INTRODUCTION

This detailed circuit description applies to both the 91A04A and 91AE04A Data Acquisition Modules. Portions of the circuit description that do not apply to the 91AE04A are marked *91A04A Only*. Portions which do not apply to the 91A04A are marked *91AE04 only*. Portions which are not thus identified apply to both modules.

This circuit description is divided into several subsections. The subsection divisions are by schematic, then by functional blocks on the schematic. Numbers in the diamonds refer to the numbers on schematic tabs in the *Diagrams* section of this addendum. The first such number is the number of the schematic for the 91A04A. The second such number is the number of the schematic for the 91AE04A. The schematics for the two modules are nearly identical except that some components and functional blocks on the 91A04A schematics are deleted from the 91AE04A schematics.

The A numbers in Table 4-1 are the assembly numbers assigned to the products described in this addendum.

Table 4-1
ASSEMBLY NUMBERS

A NUMBER	ASSEMBLY NAME
A26	91A04A Data Acquisition Module
A27	P6453 Data Acquisition Probe
A27A1	P6453 Data Acquisition Probe ECB
A28	91AE04A Data Acquisition Module

91A04A DATA ACQUISITION MODULE

The 91A04A Data Acquisition Module can acquire four independent channels of data at speeds up to 330 MHz. The module has a single-word event recognizer for triggering, stores up to 2048 data words (up to 4096 words in high resolution) and is externally armable by slow DAS cards. All reference designations used in the 91A04A module circuit description have an A26 preface.

91AE04A DATA ACQUISITION MODULE

The 91AE04A Data Acquisition Module can acquire four independent channels of data at speeds up to 330 MHz. The module has a single-word event recognizer for triggering, and stores up to 2048 data words (up to 4096 words in special cases). The 91AE04A expander module is a slave to the 91A04A master module and will not operate without certain cable connections to the master module. All component numbers used in the 91AE04A module circuit description are assumed to have an A28 preface.

Since the 91AE04A is a subset of the 91A04A, the detailed circuit description is not repeated for the 91AE04A. Refer to the *General Description* subsection as a guideline for differences between the two modules.

91A04A AND 91AE04A CIRCUIT DESCRIPTION

CONTROLLER INTERFACE 51A/59A

The 91A04A controller interface takes data from the Controller board and sends it to appropriate registers by decoding the lowest four bits on the address bus and interpreting BWR(L), SEL SLOT(L), PERSONALITY(L), PORT(L), and BRD(L) from the Controller board. The interface also takes data from the module and writes it on the data bus at read command BRD(L) of the Controller board.

For example, suppose the Controller board is reading the probe status. The address bus has 1 (hexadecimal) written on the least significant three bits. The lowest four bits of the address bus are inverted by buffer U685, so decoders U688 and U865 receive inverted addresses. Simultaneously, PORT(L) and BRD(L) go active. This action enables decoder U865, which decodes the inverted address bus so that Y6(L) goes active. The pod status register, U658, is then enabled and allows data onto the data bus. The writing procedure is similar, except that the BWR(L) and PORT(L) signals must be active to enable U688, and SEL SLOT(L) enables decoder U868 to turn on write buffer U655. Table 4-2 shows which registers are connected to the data bus by each hexadecimal address and the BWR(L), BRD(L), and PORT(L) lines.

Table 4-2
CONTROLLER INTERFACE MAP

Hex Addr	*BWR (L)	BRD (L)	PORT (L)	Line Name	ICs Affected U#	Schem.
XXX0	H	L	L	CARD ID(L)	U855	51
XXX0	L	H	L	MAP 1(L) (switch for ROMs)	U678B	51
XXX1	H	L	L	POD STATUS(L)	U658	51
XXX1	L	H	L	THRESHOLD(L)	U811	53
XXX2	H	L	L	CARD MOS STATUS(L)	U661	51
XXX2	L	H	L	CLK SEL(L)	U731	52
XXX3	H	L	L	MAR RD(L)	U655	55
XXX3	L	H	L	DELAY 2(L)	U585	57
XXX4	H	L	L	MEM RD(L)	655	55
XXX4	L	H	L	MEM LD(L)	U861A	56
XXX5	H	L	L	DIFF 0(L)	U671	58
XXX5	L	H	L	DELAY 0(L)	U741	57
XXX6	H	L	L	DIFF 1(L)	U668	58
XXX7	L	H	L	DELAY 1(L)	U588 & U591	57
XXX8	L	H	L	WRITE DATA(L)	U651	52
XXX9	L	H	L	WRITE CNTL(L)	U735	52
XXXA	L	H	L	DESK 1(L)	U725	53
XXXB	L	H	L	DESK 0(L)	U225	53
XXXC	L	H	L	TRIG CNTL(L)	U738	52
XXXD	L	H	L	MEM CNTL(L)	U745	52
XXXE	L	H	L	HIGH RES(L)	U728	52
XXXF	L	H	L	DESKEW PULSE OUT(L)	U545D & probe	51

*With SEL SLOT(L) also active.

91A04A only: The 91A04A controller interface contains two ROMs, U878 and U881. These ROMs contain changes to menus, instructions for programming 91A04A and 91AE04A modules, a record of the type of readback data present at each address, and diagnostics. These ROMs are selected for reading when the BRD(L), PERSONALITY(L), and SEL SLOT(L) lines are active. The signal MAP 1(L) determines which ROM is to be used, and the software reads a header in each ROM to determine which ROM is in which socket.

CONTROL REGISTERS 52A/60A

The six control registers on schematics 52A/60A (U651, U728, U731, U735, U738, and U745), and the two control registers on schematics 53A/61A (U225 and U725) store information from the Controller board that will be referred to by the 91A04A circuits. The data is sent by the Controller over the Interconnect board and is received by the registers through buffered data bus TTL0-TTL7(H). This data controls the behavior of the qualifier and storage circuits. Also, this data bus is translated for clocking and addressing information (see Table 4-2).

Definitions of the control registers are provided in Table 4-3.

Table 4-3
CONTROL REGISTER FUNCTIONS

SCHEMATIC	CONTROL REGISTER	CONTROL LINE	DATA BUS	PURPOSE
52/60	U731	CLK SEL(L)	Bits 0, 1, 2, 4, & 5	This register selects among the five different sources for clocks for the 91A04A/91AE04A system.
			Bit 7	Bit 7 is used to set the data login registers to prevent spurious start-up triggering.
52/60	U728	HIGH RES(L)	Bits 2 & 3	These bits are used to switch to two-channel, high-resolution (1.5 ns) mode of operation.
			Bits 4, 5, & 6	These bits are used to select the source of the stored slow-card clock.
			Bit 7	This bit is used in diagnostics to test control register U728.
52/60	U735	WRITE CNTL(L)	Bits 0 - 3	These bits control which bits of the word recognizer are to be DONT CARE.
			Bits 4 - 7	These bits control which word satisfies the word recognition.
52/60	U738	TRIG CNTL(L)	Bits 4 & 5	These bits determine whether the 91A04A/91AE04A system is armed from a slow card or is self-arming.
			Bit 7	This bit initializes the word recognizer and trigger delay latches, and resets the data login registers to prevent spurious start-up triggering.

Table 4-3 (Cont.)
CONTROL REGISTER FUNCTIONS

SCHEMATIC	CONTROL REGISTER	CONTROL LINE	DATA BUS	PURPOSE
53/61	U225	DESK 0(L)	Bits 0 - 7	This control register adds or subtracts delay in channels 0 and 1 when the module is being deskewed.
53/61	U725	DESK 1(L)	Bits 0 - 7	This control register adds or subtracts delay in channels 2 and 3 when the module is being deskewed.
52/60	U651	WRITE DATA(L)	Bits 0 - 7	This register controls which RAM in the acquisition memory is being read.
52/60	U745	MEM CNTL(L)	Bits 0 & 4	These bits control whether the clock phase generator is loading initial conditions or running (shifting) with clocks.
			Bit 1	This bit controls whether the memory address generator is loading initial conditions or running (counting) with clock-phase strobes.
			bits 2 & 3	These bits control whether the write-enable generator is loading initial conditions or running (shifting) with clocks.
			Bit 5	This bit determines whether U741 (the high-speed section of the delay counter) is loading initial conditions, or is ready to run.
			Bits 6 & 7	These bits give the DAS Controller access to the clock circuitry of the module for slow CPU clocking.

DATA RECEIVERS 53A/61A

Probe Threshold. The output of the probe threshold circuit controls the threshold of the comparators that receive the clock and data from the probe. This allows the threshold to be digitally controlled through the DAS menus.

The high-accuracy, digital-to-analog current converter (DAC) U811 has level-setting information written to it by the 91A04A controller interface. The eight bits of level-setting data is clocked in by the THRESHOLD(L) signal. The DAC has a current output that is converted to a voltage by op amp U818.

The reference voltages necessary for the DAC to produce a current proportional to the menu setting are provided by the +3 VL supply and Zener diode VR917 so that the plus reference is +3 VL and the minus reference is +1.775V.

Op amp U818 has its noninverting input tied to +3 VL. The output voltage of the op amp will therefore vary so that R812 draws the amount of current necessary to maintain the inverting input at +3 VL. As the current output of the DAC varies, the op amp will cause more or less current to be drawn through R812, as the situation demands, thereby controlling the output voltage. This output voltage exactly tracks the +3 VL supply and the output current of the DAC. Trimmer resistor R818 nulls out all initial errors in the DAC and op-amp circuitry.

The conversion of measured threshold voltage at the comparator (Vt) to the menu setting of the threshold (R-TH) is as follows:

$$(Vt\text{-}3.750) \times 10 = R\text{-}TH$$

Refer to Table 4-4 for menu-setting versus threshold-output information.

Table 4-4
MENU SETTING VERSUS THRESHOLD OUTPUT

Menu Setting	Threshold	Output
+5.0 V	4.2500 V	±1 mV
0.0 V	3.7500 V	±1 mV
-2.5 V	3.5000 V	±1 mV

Probe Data Receivers. The data signals from the probe are translated to +5 V referenced ECL data by comparators U211, U311, U411, and U511. The offset voltage of the probe threshold circuit and of each comparator is adjusted by trimmer potentiometers R201, R301, R401, and R501. The threshold voltage from the probe threshold circuit is applied to the inverting input of the comparator, and the signal from the probe is applied to the noninverting input.

The inverting output of the comparators is used as the output of of the data receivers, so the signal out of the receivers is the complement of the data received by the probe. (The signal from the data receivers is re-inverted in a later stage, before being stored.) Refer to the *Module to P6453 Interface* description in the *General Description* subsection for additional information.

Deskew Circuits. The deskew circuits are programmable delay lines with a resolution of 400 ±50 ps, and a total delay range from 0 to 5.6 ns. The specific channel delay value of each deskew circuit is programmed by four bits in latches U225 and U725.

Each deskew selector is best visualized as a 5.6 ns delay line with taps every 400 ps. A deskew selector has one input tied to each of the taps. The effective delay then depends on the tap selected by the deskew selector. The outputs of the deskew selectors go to login registers U525A, B, C, and D.

The deskew circuit simultaneously sends a positive deskew pulse to the clock channel and to the data channels. If a logic low is stored in memory for a particular channel, the deskew circuit adds a small amount of delay and checks the memory again. This process is repeated until the memory stores its first logic high. This is approximately the point at which the channel deskews.

A positive setup time and a near-zero hold time are required, so three increments of delay are added to set the theoretical setup and hold times at typically 1.2 ns during sync (probe clock) operation only.

These additional three increments of delay limit the possible valid deskew values to between 1 and 12 steps (4.4 ns).

The test path of many of the diagnostic self tests starts here. When a data selector is programmed to select data from input 15, the ECL data bus from the controller interface (ECL0-ECL3(H)) replaces the output of the 5.6 ns delay line. Refer to the *Module to P6453 Interface* description in the *General Description* subsection for more details.

Login Registers. The login registers sample and hold the data coming from the deskew circuits. Data passes from the deskew selectors through login register U525. The signals out of U525 are sampled by registers U428A and C and U628A and C on the rising edge of the LOGIN A(H) and LOGIN B(H) clocks. The outputs of these registers are sent to the acquisition memory for storage.

Note that the Q(H) outputs of the login registers are active low signals and the Q(L) outputs are active high signals. This is because the outputs of the probe data receivers are complements of the actual data. The login registers re-invert the data so it is high true.

U525 usually transmits the data from the deskew circuits on selector side 1 directly to the respective login register. If the board is programmed to acquire data at 660 MHz (high-resolution mode), only channel 0 and channel 2 are operational using side 0 of the register. The inputs to side 0 of the data selectors are:

- Deskew circuit channel 0
- Deskew circuit channel 0 delayed by 1.5 ns
- Deskew circuit channel 2
- Deskew circuit channel 2 delayed by 1.5 ns

In this way, in one acquisition cycle, the 91A04A can log in the data currently present at channels 0 and 2, and the data that was present 1.5 ns previously. Since the internal clock driving the login registers is running at 3.0 ns (330 MHz), the effective acquisition rate becomes 660 MHz from two channels.

Finally, in the bottom right corner of the schematic, registers U851A and U628B divide the 91A32 CLK signal by two and transmit the new signal for acquisition along with the data from the probe. The 91A32 clock is read back whenever the 91A04A is armed by a slow card so that all the acquired data can be time correlated.

First-Half Acquisition Memory ◇54◇A/◇62◇A

NOTE

A careful study should be made of the discussion on Clocks and Memory Control *before reading the following text on acquisition memory.*

Memory Address 0 and 1. Counters U355 and U458 comprise the first stage of a four-stage address generator. The initial value of the address is loaded from the ECL data bus (ECL0-ECL7(H)) by LD MAR(L). The address then increments 00 to FF (hexadecimal) whenever EPC0(H) has 256 rising edges. The address controls the first and second stages of the acquisition memory as well as the second stage of the address generator.

Before acquisition, counters U355 and U458 are loaded with 00 (hexadecimal). During read back, the counters are loaded with whatever memory address the Controller wants to read back.

Data Latches 0 and 1. The data latches hold data coming from the login registers for eight clock cycles. There are eight data latches that clock in data sequentially. Data latches 0 and 1 (U158 and U165) are the first two data latches. They are clocked by EPC0(H) and EPC1(H), respectively.

By holding the data to be stored for eight clock cycles, the data latches allow the acquisition memory adequate setup and hold time for reliable storage.

Acquisition Memory 0 and 1. The acquisition memory is the final storage place for data coming from the probes. The memory has eight stages that operate sequentially. During acquisition, the data is stored in acquisition memory 0 (U258) at address XX. The seven subsequent data words are stored at the same address, in the other seven acquisition memories (memories 1 through 7). The ninth acquired word is stored at address XX+1 of acquisition memory 0. Storage locations continue to spiral up until all RAM is filled. After the memory is filled, the memory address wraps around to 0 and the new stored data is written over the oldest stored data.

The acquisition memory stores data from the data latches. The address for storage is provided by the memory address 0 and 1 block. The falling edge of the write enable signal for the RAM follows the rising edge of the clock phase for the data latches by two clocks. The write enable pulse lasts for three clock periods.

For further information on acquisition timing, see the eight-phase clock generator and write enable generator functional blocks on schematic 56A.

Memory Address 2 and 3. U468 is the second stage of the four stage address generator. Two clock cycles after the memory address 0 and 1 block increments, the memory address 2 and 3 block is clocked. U468 provides the storage and readback address for acquisition memories 2 and 3.

Data Latches 2 and 3. The data latches hold data coming from the login registers for eight clock cycles. There are eight data latches that clock in data sequentially. Data latches 2 and 3 (U171 and U175) are the second pair of data latches. They are clocked by EPC2(H) and EPC3(H), respectively.

By holding the data to be stored for eight clock cycles, the data latches allow the acquisition memory adequate setup and hold time for reliable storage.

Acquisition Memory 2 and 3. The acquisition memory is the final storage place for data coming from the probes. The memory has eight stages that operate sequentially, of which U271 and U275 are stages 2 and 3. The acquisition memory stores data from the data latches. The address for storage is provided by the memory address 2 and 3 block. The falling edge of the write enable signal for the RAM follows the rising edge of the clock phase for the data latches by two clocks. The write enable pulse lasts for three clock periods. On acquisition-cycle start up, the first real data is stored in acquisition memory 3 at address location 0.

See the *Acquisition Memory 0 and 1* discussion for more operating details. For further information on acquisition timing, see the eight-phase clock generator and write enable generator functional blocks on schematic 56A/64A.

Clock Array Memory 0 to 3 (91A04A Only). The clock array memory for memory stages 0 through 3 is U475. The clock array memory stores the status of the 91A32 clock while the 91A04A is operating. The stored information is later recovered and used to time correlate 91A04A and slow-card data.

Data is stored in the acquisition memories in a similar manner. The address for this clock array RAM is provided by the memory address 2 and 3 block. The 91A32 clock data is stored from each of data latches 0, 1, 2, and 3, rather than from a specific data latch. (The clock array data from data latch 0 is latched into data latch 2 so that it will meet setup and hold requirements of the clock array RAM.)

MAR Overflow Register. MAR (memory address register) overflow is monitored by U851B. Prior to starting acquisition, MAR overflow register U851B is reset by CLEAR TRIG ECL(H). If the memory address 0 and 1 block rolls over from FF hexadecimal to 00, the MAR overflow register is clocked, thereby asserting MAR OVERFLOW(H). MAR OVERFLOW(H) is read by the Controller by way of the Interconnect board. If MAR OVERFLOW(H) is asserted, the Controller assumes that the entire acquisition memory is filled (except location 00)and that the last data stored corresponds to the current data address.

Second-Half Data Acquisition Memory  A/A

Memory Address 4 and 5. U481 is the third stage of a four-stage address generator. Two clock cycles after the memory address 2 and 3 block is loaded, the memory address 4 and 5 block is clocked. U481 provides the storage and readback address for acquisition memories 4 and 5.

Data Latches 4 and 5. The data latches hold data coming from the login registers for eight clock cycles. There are eight data latches that clock in data sequentially. Data latches 4 and 5 (U181 and U185) are the third pair of data latches. They are clocked by EPC4(H) and EPC5(H), respectively.

By holding the data to be stored for eight clock cycles, the data latches allow the acquisition memory adequate setup and hold time for reliable storage.

Acquisition Memory 4 and 5. The acquisition memory is the final storage place for data coming from the probes. The memory has eight stages that operate sequentially, of which U281 and U285 are stages 4 and 5. The acquisition memory stores data from the data latches. The address for storage is provided by the memory address 4 and 5 block. The falling edge of the write enable signal for the RAM follows the rising edge for the data latches by two clocks. The write enable pulse lasts for three clock periods.

See the *Acquisition Memory 0 and 1* discussion for more operating details. For further information on acquisition timing, see the eight-phase clock generator and write enable generator function blocks on schematic 56A/64A.

Memory Address 6 and 7. U485 is the last stage of a four-stage address generator. Two clock cycles after the memory address 4 and 5 block is loaded, the memory address 6 and 7 block is clocked. U485 provides the storage and readback address for acquisition memories 6 and 7.

Data Latches 6 and 7. The data latches hold data coming from the login registers for eight clock cycles. There are eight data latches that clock in data sequentially. Data latches 6 and 7(U191 and U198) are the fourth pair of data latches. They are clocked by EPC6(H) and EPC7(H), respectively.

By holding the data to be stored for eight clock cycles, the data latches allow the acquisition memory adequate setup and hold time for reliable storage.

Acquisition Memory 6 and 7. The acquisition memory is the final storage place for data coming from the probes. The memory has eight stages that operate sequentially, of which U291 and U298 are stages 6 and 7. The acquisition memory stores data from the data latches. The address for storage is provided by the memory address 6 and 7 block. The falling edge of the write enable signal for the RAM follows the rising edge for the data latches by two clocks. The write enable pulse lasts for three clock periods.

See the *Acquisition Memory 0 and 1* discussion for more operating details. For further information on acquisition timing, see the eight-phase clock generator and write enable generator function blocks on schematic 56A/64A.

Clock Array Memory 4 to 7 (91A04A Only). The clock array memory for memory stages 4 through 7 is U491. The clock array memory stores the status of the 91A32 clock while the 91A04A is operating. The stored information is later recovered and used to time correlate 91A04A and slow-card data.

Data is stored to the acquisition memories in a similar manner. The address for this clock array RAM is provided by the memory address 6 and 7 block. The 91A32 clock data is stored from each of data latches 4, 5, 6, and 7, rather than from a specific data latch. (The clock array data from data latch 4 is latched into data latch 6, so that it will meet setup and hold requirements of the clock array RAM.)

Acquisition Readback. The DAS Controller reads the contents of the 91A04A acquisition memory through the acquisition readback block. When EN MEM ACCESS(H) is high, data from the acquisition RAM selected by U651 and the current clock phase is passed through U548 and U465 to tri-state buffer U665. When EN MEM ACCESS(H) is low, the current memory address is transmitted to buffer U665 through comparators U565 and U568. Whenever MEM/MAR RD(H) goes active, the data present at the inputs of U665 is transmitted onto the Interconnect data bus for the Controller board to read.

Clocks and Memory Control 56A/64A

91A08 Internal Clock Receiver (91A04A Only). There are four possible clock sources for the 91A04 clock: the external clock, and three internal clocks. For asynchronous acquisition at rates of 100 MHz or less, the 91A04A module uses the 91A08 internal clock. The 91A08 internal clock is generated on the Trigger/Time Base board and transmitted through the Interconnect board differentially to difference amplifiers Q922 and Q923.

The 91A08 internal clock is selected to drive the 91A04A module whenever the 91A08 INTL CLK SEL(H) line is active and all other select lines are inactive.

3 ns Clock and 5 ns Clock (91A04A Only). The 91A04A module derives its 1.5 ns and 3 ns internal clocks from the 3 ns clock oscillator built around U235A. When 3 ns EN(H) goes active, U235A becomes a functional inverter, the output of which is attached to the input. The U235A then oscillates at a frequency determined by R334 and C335. C335 is adjusted until U235A oscillates at 330 MHz.

The 91A04A module derives its 5 ns internal clock from the 5 ns clock oscillator built around U235B. When 5 ns EN(H) goes active, U235B becomes a functional inverter, the output of which is attached to the input. The U235B then oscillates at a frequency determined by R333 and C332. C332 is adjusted until U235B oscillates at 200 MHz.

Probe Clock Receiver (91A04A Only). The clock signal from the probe is translated to +5 V referenced ECL by comparator U115. The clock signal being received goes to the noninverting input of the comparator. The threshold voltage from the probe threshold circuit is applied to the inverting input of the comparator. The offset voltage of the clock threshold circuit and the comparator is nulled by trimmer adjustment R111.

Probe Clock Buffer (91A04A Only). U121 allows the selection of either a falling or rising edge external clock. If SEL PROBE CLK(L) is active, the buffers transmit the rising edge clock. If SEL PROBE CLK NOT(L) is active, the buffers transmit the inverted or falling edge clock.

Start-up Circuit (91A04A Only). The start-up circuit receives the selected clock through OR gates U228B, U125A, and U125B. The output of U125B goes to the start-up registers U453A, B, and C.

The start-up registers prevent marginally-stable (meta-stable) states from producing clock glitches upon start-up and during shut-down of an acquisition cycle. This circuit also provides a three-clock delay after the completion of the trigger and delay sequence.

Prior to acquisition, the registers are set by toggling CLEAR TRIG ECL(H). The selected clock is then started, but it is not allowed to pass the 91A04A and 91AE04A clock drivers block because of the high output of the start-up registers. When it is time to start acquisition, START ACQ(H) goes active. The active START ACQ(H) is inverted by U545C, so registers U435A, B, and C start to clock through a low signal. After three clock periods, the low signal passes out of the start-up registers, so the selected clock may pass through the 91A04A and 91AE04A clock drivers U241 and U245.

The 91A04 STOP STORE(H) signal is wire-ORed to the D input of the first start-up register. When 91A04 STOP STORE(H) goes active, the start-up circuit starts clocking through a high signal. After three clock periods, the start-up circuit stops the selected clock from passing through the clock drivers, which stops acquisition.

91A04A and 91AE04A Clock Drivers (91A04A Only). This block receives the selected clock from the clock start-up block, and derives the basic clocks for all the circuitry on the 91A04A board. Clock drivers U241 and U245 also provide the acquisition clock that is sent to all 91AE04A boards. The clock drivers are controlled by the start-up circuit. For more information on the start-up circuit, refer to the *Start-up Circuit* description, given previously.

Clock Distribution Circuit (91A04A Only). The integrated circuits U228A, U328, U342, U345, and U348B distribute and time 330 MHz clocks with the minimum amount of loading on each driver. These circuits are timed by many different delays to produce reliable clocking. These delays consist of transmission lines (MICROSTRIPs) whose lengths have been adjusted so that the timing has the greatest margins with the typical components in the clock distribution circuit. Also, clocks that drive the eight-phase clock generator and the write enable generator are provided by U348.

Clock Distribution Circuit (91AE04A Only). The clock distribution circuit is the same as that in the 91A04A except for the drive of clock-interface IC U341. The clock coming in on J138 is referenced to the +5 V supply on the 91A04A. This supply is specified to be within 100 mV of the 91AE04As +5 V supply. To compensate for a possible voltage offset within that limit, transistor Q436 is an adjustable current source which causes an opposite and cancelling offset across R436.

For voltage differences of -75 mV to +25 mV between the 91A04A +5 V supply and a specific 91AE04A +5 V supply, jumper W148 is installed. With differences of +25 mV to +75 mV, the jumper should be removed.

Eight-Phase Clock Generator. The eight-phase clock generator creates clocks for the eight data latches that hold data to be stored. Since the acquisition memory has an eight-stage architecture, eight sequential clocks are needed. These clocks are derived from an eight-stage shift register that reloads itself.

The eight-stage shift register consists of shift register U151. Prior to acquisition, the eight-stage shift register is loaded with 02 (hexadecimal). During acquisition, the shift register shifts up with each WE CLK(H) rising edge. After the high bit reaches position 7 which is connected to the serial input, it shifts back to the 0 bit on the next rising edge of WE CLK(H).

After acquisition is complete, the Controller board reads the clock phase to discover what data was written last. Decoder U155 reads the current clock phase and translates the clock phase into octal. The octal value is then output for read-back by the controller interface. Figure 4-1 shows the timing relation between the different clocks and the write-enable pulses.

Write Enable Generator. Write enable generator U251 creates write enable pulses for the eight RAMs in the acquisition memory. Since the acquisition memory has an eight-stage architecture, eight sequential write enable pulses are needed. These pulses are derived from an eight-stage shift register that reloads itself. The eight-stage shift register consists of shift register U251. Prior to acquisition, the eight-stage shift register is loaded with 8F (hexadecimal). During acquisition, the write enable generator provides a write enable pulse to each of the acquisition RAMs that is three clock periods long and is centered between the clocks for the corresponding data latch.

NOTE

Each clock phase (EPCX) and each write-enable pulse (WEX) defines a stage of the memory matrix.

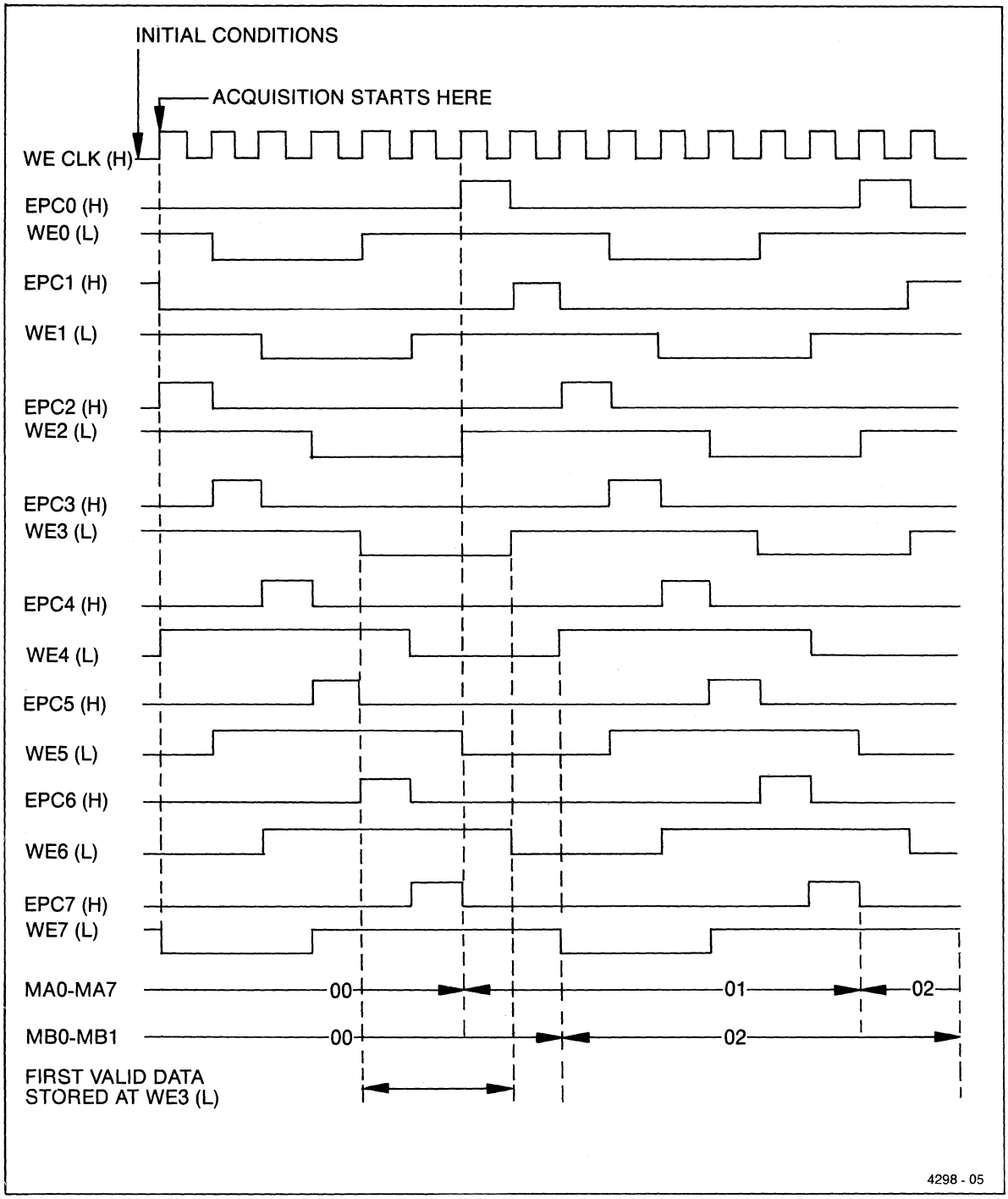


Figure 4-1. Acquisition pulse timing for 3 ns or slower acquisition. (All data stored before address 01 is discarded by firmware.)

Trigger◇57◇A/◇65◇A

Word Recognizer. The word recognizer monitors the data received by the 91A04A module. When the trigger word is recognized, the word recognizer signals the trigger. The word recognizer consists of three parts:

- The first part determines whether a specific bit must be high or low for a trigger.
- The second part determines the trigger care or don't-care status of a particular bit
- The third part determines wheather all lines meet the requirements for a trigger simultaneously.

The first part of the word recognizer (U531) consists of four exclusive-OR gates. The exclusive-ORs are used as programmable inverters. The control lines to the exclusive-ORs are set so that a trigger signal out of the exclusive-OR is active low. For example, D0 must be high for a trigger to occur. WD0 would then be programmed high so that when D0 was high, the output of the exclusive-OR would be low, and when D0 was low, the exclusive-OR output would be high.

The second part of the word recognizer consists of four registers: three registers in U538 and register 1 of U635. The bits to which X (don't care) is assigned are held RESET by control lines, so their outputs are always low. All other bits are latched in as they come from the exclusive-OR gates.

The third part of the word recognizer is five-input OR gate U641C. Whenever all four of the input data lines meet the requirements for word recognition, all five inputs to the OR gate are low. The OR gate output is usually high, and outputs a low to the trigger to signify recognition of the trigger word.

The low input to U635A is passed to the trigger circuit on the next rising edge of CLK C. The delay in W642 is selected to properly align propagation time of the master module to any installed expander modules.

Trigger. The trigger consists of a latch for the 91A04A word recognizer (U635A), a five-input NOR gate (U641A), and a trigger latch (U448A).

NOTE

In the 91AE04A, the word-recognizer output is delivered to the 91A04A by way of DL635B, W642, and J141. The remainder of this discussion applies to the 91A04A only.

Word recognizer latch U635A holds the word recognition signal while the signals from the 91AE04A modules are settling at the inputs to U641A. If all the word recognition signals from all attached modules and from the 91A04A itself are low, the NOR gate outputs a high. If any word recognizer cables are not attached to a 91AE04A module, then pull-down resistors hold the unattached inputs of the NOR gate low.

When NOR gate U641A outputs a high, U448A latches in that high on the rising edge of clock D. U448A then outputs a high which is held high until it is RESET prior to starting the next acquisition.

U448A also controls the arming feature of the 91A04A module. Note that the clock to the register may be masked out by a high on pin 16 of U448A, so the register may not clock in a new trigger. Pin 16 of U448 can be held high through NOR gate U545A and AND gate U861D. In situations where the 91A04A module must be armed by the slow-card trigger, pin 16 of U448 will not go low until the slow card has triggered.

Delay Counter-Lower 1/4 (91A04A Only). Lower 1/4 delay counter U741 allows the 91A04A module to delay the end of acquisition by a preset number of clock periods after the trigger sequence is completed. The delay counter is divided into two parts, the lower 1/4 and the upper 3/4, because the lower section must operate faster than the upper section. The lower 1/4 is therefore designed with ECL, while the upper section is designed with TTL.

Neither the upper or lower part of the delay counter can operate at 330 MHz, so the clock to the delay counter is divided by four (by U448B and U448C). Before acquisition, the two registers in the divide-by-four circuit are set by ENABLE DELAY COUNTER LOAD(H). The divide-by-four network starts clocking when the trigger is complete and latched (indicated by a low on Q(L) of U448A).

Because the delay counter clock is divided by four, and because the delay counter counts up, the value loaded into the counter must be manipulated by the firmware. First, the firmware calculates the one's complement of the value from the DELAY field in the Trigger Specification menu. Then, the one's complement is divided by four. This manipulated value is then loaded into the lower and upper portions of the delay counter.

The lower 1/4 of the counter (U741) is loaded with a delay value by the controller interface. When ENABLE DELAY COUNTER LOAD(H) is high, U741 is loaded with the four bits on the ECL0-ECL3(H) data bus.

Once loaded, the counter increments once with every rising edge from U545B (which runs at 1/4 the rate of the acquisition clock). U545B does not output a clock until the 91A04A trigger conditions have been satisfied.

The Q3(H) output of the lower 1/4 delay counter clocks the upper 3/4 delay counter after being translated from ECL to TTL by Q965 and Q966.

The end of the delay count is also detected in this circuit block. When the top 3/4 of the delay counter reaches its terminal count, the CO(L) pin of U591 goes low. Then when the lower 1/4 of the counter reaches its terminal count, all of the inputs to OR gate U641B are low. OR gate U641 then outputs a high signal to accomplish the 91A04 STOP STORE(H). An active 91A04 STOP STORE(H) turns off the delay counter by pulling the CE(L) input of the lower 1/4 counter high.

Once STOP STORE(H) is asserted, the acquisition cycle stops after three more clocks. The Controller board reads the data stored in the 91A04A and displays it on the screen. Because the clock to the delay counter is divided by four, and because of the delays in the delay counter, there is an uncertainty about the location of the trigger word. The firmware overcomes this difficulty by searching for the first occurrence of the trigger word in the data block in question. The screen then displays the first occurrence of the word in that data block as the trigger.

Delay Counter-Upper 3/4 (91A04A Only). The top 3/4 of the delay counter (U585, U588, and U591) allows the 91A04A module to delay stopping acquisition for over 32,700 clock cycles after the occurrence of the trigger word. The top 3/4 of the delay counter is driven by the lower 1/4 of the counter. See the *Delay Counter-Lower 1/4* circuit description for further details on the delay counter operation.

Difference Counter and Power Supplies 58A/66A

Difference Counter (91A04A Only). If both 91A04A and slow-card modules are installed in the same DAS mainframe, they may be made to trigger at different times. The difference counter counts the number of 91A32 clock cycles between the two triggers.

The 91A04 TRIGRD(L) and 91A32 TRIG 0(H) signals control when the difference counter starts and stops. 91A04 TRIGRD(L) is converted to TTL levels and inverted by Q942 and Q944. 91A32 TRIG 0(H) is inverted by U581C. The inversion of these two signals is then NORed by U581B, which then controls enable pin ENP(H) of counter U578.

The clock for the difference counter is 91A32 CLK(H). This ECL-level clock is converted to TTL by Q943 and Q945. Since the clock is now inverted TTL, it is re-inverted by U581A.
Prior to acquisition, the difference counter is cleared by the CLEAR TRIG(H) signal. The difference counter is now ready.

The difference counter only operates if the slow-card module(s) triggers prior to the 91A04A module, as happens in 91A32 ARMS 91A04 mode. When acquisition starts, the conditioned 91A32 CLK(H) tries to clock the difference counter, but the counter is not yet enabled by a high from U581B. The output of U581B is held low because both 91A32 TRIG 0(H) and 91A04 TRIGRD(L) are inactive.

After the slow card completes its trigger sequence, 91A32 TRIG 0(H) goes active. At this point, U581B outputs a high and the difference counter starts counting up from m 0000 (hexadecimal).

The up count continues until the 91A04A module triggers. Now 91A04 TRIGRD(L) goes active, so U581B outputs a low. The low from U581B stops the counter. If the counter should increment past 7FFF (hexadecimal), the counter stops itself through inverter U675C. This prevents the counter from wrapping around and providing erroneous data.

After acquisition is finished, the Controller board reads the value in the difference counter back through the controller interface. DIFF 0(L) and DIFF 1(L) are used by the controller interface to enable tri-state buffers U671 and U668, which transmit the values held by the counter onto the Interconnect data bus BD0-BD7(H).

+10 V Supply. +10 V is required by the probe data and clock receivers, U115, U211, U311, U411, and U511 (schematics 53A and 56A). +10 V is derived from three diode drops from the +12 V supply across CR201, CR301, and CR401.

+3 V Supply. There are actually two separate supplies in this functional block. Both supplies share a common +3 V reference created by voltage divider VR938, VR939, R932, and R936. This configuration makes the +3 (Vt) supplies track the +5 (Vcc) supply so that:

$$Vt = Vcc\text{-}1.92\ V$$

Both +3 V supplies use an op amp controlling the amount of current drawn by a transistor for voltage regulation. The output of the op amp controls the current to the base of the transistor through a 100 ohm resistor. The voltage of the +3 V supply is monitored by the inverting input of the op amp. When the +3 V supply drifts from the reference voltage at the noninverting input of the op amp, the current to the base of the transistor is adjusted to bring the supply back to regulation.

The +3 V supply, built around U991B and Q595, sinks most of the +3 V current on the board (around 2 amps). Rather than dissipate all the current through the transistor, R695 draws one amp to reduce the transistor load.

The +3 V supply, built around U991A and Q982, is an isolated supply for the probe interface. This supply draws less than 0.5 A. Diode CR986 is a safety clamp that prevents the +3 V level from rising above +5 V in case any components of the supply should fail.

+15 V Supply. The +15 V supply is a DC-to-AC-to-DC converter. A 160 KHz square wave is generated by U905. This square wave drives Q901 and Q902 to supply a 10 V p-p square wave to T901 (aproximately 2 V are lost across the transistors). The center tap of T901 is tied to +12 V, so the output waveform is centered around +12 V.

Diodes CR801 and CR802 form a full-wave rectifier. The output of this rectifier, after filtering, is about +19 V. L905 averages out the current demands on the transformer, which helps prevent transformer core saturation.

U901 and U902 are linear voltage regulators. They take the +19 V input from the full-wave rectifier and produce two independent +15 V sources. For circuit protection, each voltage regulator current limits at 100 mA, so no more than 200 mA can be drawn from transformer T901.

+4.2 V Supply. This power supply is used for the CMOS latches and resistor pullups in the control registers (schematics 52 and 60). These latches (U725, U728, U731, U735, and U738) and the resistors are used to provide nonsaturating compatability to the TTL-ECL interface to maintain speed in critical circuits. Also, this supply tracks the +5 V supply within 0.80 V.

Section 5
VERIFICATION AND ADJUSTMENT PROCEDURES

INTRODUCTION

This section contains three main parts: functional check procedures, adjustment procedures, and performance check procedures. These procedures, along with the test setup information at the beginning, allows a qualified technician to verify the operation of a 91A04A Series module or a P6453 probe, or to adjust variables to achieve the specified performance.

A diagram showing the locations of test points, adjustments, and jumpers is located in the *Reference Information* section of this addendum.

NOTE

The term verification *is used to mean either a functional check or a performance check*

Functional Check Procedures. These tests verify that the device being functionally tested is basically operational. The procedure exercises the main user interfaces of the device to verify their operation. The procedure also checks the main internal features for operation. These tests can be used to determine whether adjustment and/or repair is necessary.

Adjustment Procedures. These instructions for setting variables should bring the device being adjusted to or within product specifications. If the device cannot meet the specifications given in this addendum after adjustment, repair is necessary.

Performance Check Procedures. These tests provide a detailed check of internal and external product characteristics. All specifications listed in the performance requirements column of the specifications are verified. These checks can be extensive and time consuming. Under normal circumstances the functional check procedures provide an adequate test of product performance.

TEST SETUP INFORMATION

These functional check, adjustment, and performance check procedures require some test setups relevant only to 91A04A Series modules. This information is consolidated here to prevent duplication.

SUGGESTED TEST INSTRUMENTS

Tables 5-1, 5-2, and 5-3 list the test instruments and accessories required for the functional checks, adjustment procedures, and performance checks provided in this section of the addendum. Unless otherwise specified, equivalent equipment may be substituted for the recommended type.

NOTE

Each separate procedure uses only some of the equipment given in these tables. Check the procedure in question before appropriating test instruments.

Table 5-1
EQUIPMENT NEEDED FOR THE FUNCTIONAL CHECK PROCEDURES

Qty.	Function	Recommended Type
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	slow-card data acquisition module	Tektronix 91A32 or 91A24
1	pattern generator module	Tektronix 91P16 (no substitute)
1	data acquisition probe	Tektronix P6453 Data Acquisition Probe with nine pairs of leads and TTL gripper tips (TTL gripper tips have p/n 195-3659-00 per pair)
1	pattern generator probe	Tektronix P6455 TTL/MOS Pattern Generator Probe (no substitute)
2	pattern generator optional lead sets	p/n 012-1001-00
2	rows of 10-each square pins	p/n 131-1939-00
18	probe leads	part of P6453's TTL-type gripper tips, p/n 195-3659-00

Table 5-2
EQUIPMENT NEEDED FOR THE ADJUSTMENT PROCEDURES

Qty	Function	Recommended Type
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	module extender	DAS Main Extender Board, p/n 670-6748-00 (no substitute)
1	digital multimeter (DMM)	Tektronix DM501A
1	maintenance kit	DAS Service Maintenance Kit (no substitute)
1	⩾400 MHz oscilloscope (see note 1)	Tektronix 7904 mainframe with a 7A26 vertical amplifier, a 7B10 timebase, and a P6106 probe (X10, 10 MΩ)
1	constant current source (see note 1)	Fluke 5101B Multimeter Calibrator
1	current source cable (see note 1)	Refer to *Fabricating the Current Source Cable* in the *Adjustments* subsection
1	⩾400 MHz oscilloscope (see note 2)	Tektronix 7904 mainframe with a 7A19 vertical amplifier, a 7B10 timebase, and a P6201 FET X10 probe
1	250 MHz pulse generator (see note 2)	Tektronix PG502 250 MHz Pulse Generator
1	high-speed acquisition test fixture (see note 2)	p/n 067-1139-00 (no substitute)
1	5-1/4 inch probe ground cable (see note 2)	p/n 175-0848-01

Note 1: This equipment is required when adjusting comparator offsets using the Fluke 5101B Multimeter Calibrator as a current source.

Note 2: This equipment is required when adjusting comparator offsets using the Tektronix PG502 250 MHz Pulse Generator as a signal source.

Table 5-3
EQUIPMENT NEEDED FOR THE PERFORMANCE CHECK PROCEDURES

Qty	Function	Recommended Type
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	data acquisition probe	Tektronix P6453 with leads and TTL-type gripper tips (no subsitutute). Gripper tips have p/n 195-3659-00 per pair.
1	maintenance kit	DAS 9100 Series Service Maintenance Kit (no substitute)
1	module extender	DAS Main Extender board (no substitute), one required for each module to be extended
1	digital multimeter (DMM) with 0.05% accuracy	Tektronix DM501A
1	pulse generator, 250 MHz with rise and fall times <1 ns	Tektronix PG502
1	sinewave generator, $\geq$300 MHz with levelled output	Tektronix SG504
1	two-channel oscilloscope with $\geq$400 MHz bandwidth and $\leq$2.5 pF input capacitance	Tektronix 7904 mainframe with a 7A19 vertical amplifier, a 7B10 timebase, and two P6201 FET X10 probes installed
1	350 MHz frequency counter, ECL compatible for time measurements of 14.0 ns $\pm$0.1 ns	Tektronix DC510
1	high-speed acquisition test fixture	p/n 067-1139-00 (no substitute)
1	+5 V power supply	Tektronix PS503A
2	cables with banana connectors	p/n 012-0031-00
2	rows of 10 each square pins	p/n 012-0031-00

CONNECTING A P6453 PROBE TO A P6455 PROBE

This connection is required to allow a 91P16 Pattern Generator Module to drive 91A04A and 91AE04A modules. The connection procedure assumes a 91A04A and one 91AE04A are to drive eight data channels. The equipment required for this connection is:

- two P6453 probes (one for each data acquisition module)
- 18 probe leads (nine pairs) removed from the P6453s TTL-type gripper tips (195-3659-00)
- one P6455 Pattern Generator Probe
- one pattern generator lead set
- two rows of 10-each square pins (p/n 131-1939-00)

CAUTION

Use special care when connecting the pigtails. Reversed polarity could cause damage to the pattern generator circuits. On the pattern generator lead set, the IN (data) lead is the colored wire and the REF (reference) lead is the black wire. The REF line on the P6453 probe must be connected to the black wire of the pattern generator lead set.

Refer to Figure 5-1 while performing the following connections:

1. Connect the probes to their modules.
2. Set the diagnostic slide switch on the back of the P6455 probe to AUX.
3. Connect the pattern generator lead set to the P6455 TTL/MOS Pattern Generator probe.
4. Install the two rows of 10 square pins in the square receptacles on the opposite end of the pattern-generator lead set.
5. Remove 18 probe leads from the P6453 Data Acquisition Probe gripper tips and connect them to all of the square pins except the strobe pair (see Figure 5-1). (Figure 5-1 shows probe leads connected to data channel 0 only.)
6. Connect the other end of the probe leads to the hybrid connectors on the P6453 probes with black leads in the pairs to REF, and connect the colored leads to IN as follows:

   Data channels 0-3 pairs to the 91A04As P6453 probe data inputs

   Data channels 4-7 pairs to the 91AE04As P6453 probe data inputs

   Clock channel pair to the 91A04A's P6453 probe clock input

   VL from pattern generator lead set to common pin (black wire) on unused input pair (strobe).

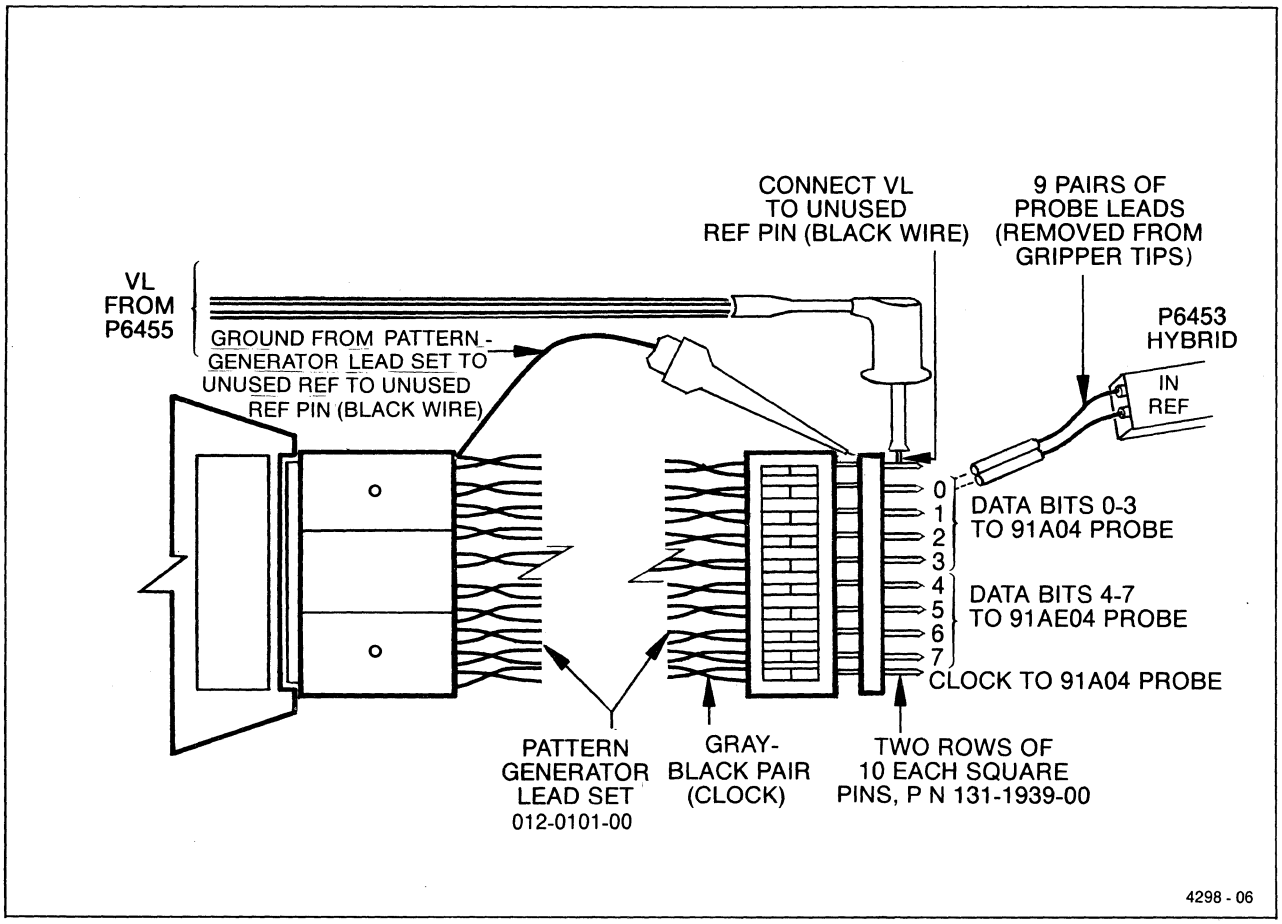


Figure 5-1. How to connect a P6453 Data Acquisition Probe to a P6455 Pattern Generator Probe. (Black lead in twisted pair is REF, colored lead is data.)

FUNCTIONAL CHECKS

The Functional Check Procedure verifies that all the major sections of the product being checked are operational. These tests can be used to determine whether adjustment and/or repair is necessary.

The Functional Check Procedure is organized into a set of tests for 91A04A/91AE04A module combinations, then a seperate test for the P6453 probe.

NOTE

These procedures assume that the user is familiar with the operation of the DAS menus and hardware.

Test equipment required for this procedure may be found in Table 5-1 at the beginning of this section.

91A04A AND 91AE04A DATA ACQUISITION MODULES FUNCTIONAL CHECK

This procedure verifies the operation of the deskewing, acquisition, and word recognition capabilities of the 91A04A and 91AE04A modules. Any valid combination of the modules may be checked with this functional check procedure. All 91A04A and 91AE04A modules operate as a system, so they must be checked as a system.

You will need the following equipment to perform this procedure:

- DAS 9100 Mainframe
- 91P16 Pattern Generator Module
- P6455 TTL/MOS Pattern Generator Probe
- Enough P6453 Data Acquisition Probes with leads and TTL-type gripper tips for all 91A04A and 91AE04A modules in the system
- Pattern generator lead set
- two rows of 10-each square pins (p/n 131-1939-00)

If available, add the following:

- 91A32 or 91A24 (slow card) Data Acquisition Module with probes (used to check ARMS 91A04 mode)

Refer to the *Module Installation* instructions in the *Operating Instructions* section of this addendum for module installation requirements. Refer to *Connecting a P6453 Probe to a P6455 Probe* at the beginning of this section of the addendum for information on connecting P6453 probes to a 91P16 pattern generator with the pattern generator lead set.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe for the functional check.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so may damage the module or sub-assembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe power.
2. Check the jumpers on the 91A04A and 91AE04A modules for correct placement in accordance with the *Module Adjustment Procedures* subsection of the *Operating Instructions* section of this addendum.
3. If the 91A04A/91AE04A system to be tested is already properly installed in the mainframe, leave it there. If the system to be tested is not yet in the mainframe, install it now. Be sure to follow the *Module Installation* procedures given in the *Operating Instructions* and *Maintenance: General Information* sections of this addendum. Refer also to the *Maintenance: General Information* section of your *DAS 9100 Series Service Manual.*

CAUTION

Failure to follow the installation guidelines will invalidate test results and may result in damage to +5 V Power Supply modules.

4. Connect all cables between the 91A04A and 91AE04A modules.
5. Install the 91P16 Pattern Generator Module in a powered bus slot of the DAS mainframe.
6. If a slow-card (91A32 or 91A24) is available, it should be installed in a powered bus slot of the DAS mainframe (used to check the ARMS 91A04 mode).
7. Double check that the module installation requirements (see step 1) have been met, then turn on the mainframe.
8. Follow the instructions for setting clock offset on 91AE04A modules. This information is found in the *Module Adjustments* subsection of the *Operating Instructions* section of this addendum.
9. Follow the instructions for setting DAC (digital-to-analog comparator) threshold and input comparator offsets on 91A04A and 91AE04A modules. This information is located in the *Adjustments* subsection of these *Verification and Adjustment* procedures.

(2) Executing the Diagnostic Self Test

The following steps run all available self-test diagnostics on the 91A04A and 91AE04A modules.

NOTE

If a P6453 probe is connected to a 91A04A module during diagnostics, a signal of +6.3 V ± 100 mV at the probe tip will cause a failure of diagnostics.

1. Turn off the mainframe, then turn on the mainframe while holding down the STOP key on the keyboard. This will cause the power-up self test to fail.
2. Press START SYSTEM to enter the Diagnostics menu. Press SELECT to select the slot containing the 91A04A module.

3. Select ALL mode, then press START SYSTEM. The DAS diagnostics will perform all available tests on the slot. The diagnostic tests; REG, MEM ADDR, DEL CNTR, DIF CNTR, ACQ MEM, CLK ARRAY, HIGH RES, and WRD REC, should all pass. (The DESKEW EX and DAC THRSH tests have no internal read back, so they can neither pass nor fail.)
4. When the diagnostic tests of the 91A04A module are complete, the cursor will return to the DAS screen. Press SELECT to select the slot for the desired 91AE04A module. The diagnostic tests REG, MEM ADDR, ACQ MEM, HIGH RES, and WRD REC, should all pass. (Clock and word-recognizer connections must be in place between 91A04A and 91AE04A to pass MEM ADDR and WRD REC tests.)
5. Repeat step 4 for other 91AE04A modules in the system. The results should be the same as in step 4.

(3) Verifying Deskew Operation

This procedure verifies the operation of the 91A04A and 91AE04A deskewing circuits.

NOTE

Once the modules have been deskewed, do not turn off the mainframe until the functional check is complete. If the mainframe is turned off before the procedure is dinished, the deskew operation must be performed again.

1. Exit the Diagnostics menu by pressing the TRIGGER SPEC key.
2. Set the MODE field in the Trigger Specification menu to 91A04 ONLY.
3. Connect P6453 probes to the Pod C connector on the back of the 91A04A and 91AE04A modules. When the probe is connected to a module, the mainframe should beep and display the message POD XC CONNECTED (where X is the slot number of the module). (If the probe is already connected, disconnect it; then re-connect it to obtain the beep and the message.)
4. Press the POD ID button on each probe housing. The mainframe should beep again and the screen should show POD XC (where X is the slot number of the module).
5. Select the 91A04 ONLY mode and move the screen cursor into the DESKEW POD field. Follow the instructions given on the screen. If your 91A04 firmware is version 2.0 or above, you can view deskew steps by pressing the SHIFT and TRIGGER SPEC keys simultaneously, instead of the TRIGGER SPEC key by itself. The display should show a deskew step between 2 through 8.
6. After all modules have been deskewed, the DAS screen should read DESKEW COMPLETE. If any channels do not deskew, make sure their hybrids are properly oriented in the probe housing. Also make sure that the probe hybrid is well seated on the deskewing pins.

If any probe channels do not deskew, either the probe or the module the probe is attached to is not functional. Perform the functional check on the probe in a different (known good) module before assuming the module is not operational.

(4) Probe Setup for the Functional Check of a Module

This procedure provides the initial test setup for the remaining functional checks. Perform the procedure provided under *Connecting a P6453 Probe to a P6455 Probe* which appears at the beginning of this *Verification and Adjustments* section.

(5) Verifying Pod Connector C

The following steps verify the operation of all data lines of all the modules. The operation of the external clock is verified at the same time.

1. Set the 91A04 CLOCK field in the Trigger Specification menu to external rising edge.
2. Press the PATTERN GENERATOR key to enter the Pattern Generator menu. Set the pattern generator clock to 50 ns.
3. Adjust the pattern generator program to look like this:

SEQ	LABEL	HEX	INSTRUCTIONS	STROBES
0		0000	GOTO 200	
200	200	0000		
201		1111		
202		2222		
203		4444		
204		8888		
205		FFFF	GOTO 200	

4. Press START SYSTEM.
5. Examine the Timing Diagram menu. If necessary, adjust the timing display so the data acquired by the 91A04A and 91AE04A is displayed on the screen.
6. Set the magnification of the Timing Diagram to 10; this should produce a display like Figure 5-2. Examine the data acquired by all 91A04A and 91AE04A modules. Proper data verifies that the modules acquire and display data and that the 91A04A external clock operates. The trigger word is not critical. This step also checks the TTL threshold and the clock interface between modules.

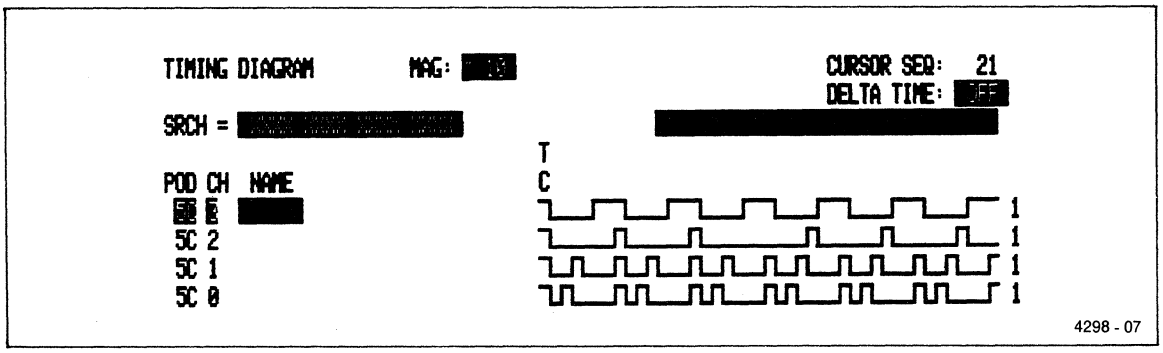


Figure 5-2. Initial test data acquired by 91A04A and 91AE04A modules.

The previous steps verified the operation of the data and external clock lines of the modules. The remaining steps verify the operation of the inversion of the external clock.

7. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to external falling edge.
8. Press START SYSTEM.
9. The data acquired, as displayed in the Timing Diagram menu, should match the data shown in Figure 5-2.

(6) Verifying the Acquisition Memory Cycle

The following steps check the ability of a 91A04A/91AE04A to complete a full acquisition memory cycle and repeat the exact storage cycle five times.

1. Change the trigger word to all zeros.
2. Press START ACQUISITION.
3. Press STORE to store the newly acquired data in reference memory.
4. Switch to the state table and change the display to acquisition and reference memory, then move the cursor to the COMPARE field and expand to 2048 locations by changing the 511 to 2047.
5. Press the COMPARE $\neq$ key and verify at least five restarts before terminating the passing test.

(7) Verifying Triggering On 1s and Slow Internal Clocks

The following steps verify that the single-level data trigger contained on the 91A04A and 91AE04A modules is functional.

1. Press the PATTERN GENERATOR key to enter the Pattern Generator menu. Adjust the pattern generator program to look like a 256-count pattern as follows:

SEQ	LABEL	HEX	INSTRUCTIONS	STROBES
0	ABC	0000	COUNT 255	
1		00FF	GOTO ABC	

2. Enter the Trigger Specification menu. Set the TRIGGER ON field to all 0s. (For example, if there are one 91AE04A and one 91A04A module in your system, the trigger word is 00 hexadecimal.)
3. Set the 91A04 CLOCK field in the Trigger Specification menu to 50 ns. (This verifies that the 91A04A can receive low-speed clocks from the Trigger/Time Base board.)
4. Press START SYSTEM.
5. Enter the State Table menu. Note that the data next to the highlighted T is the trigger word. This data should match the trigger value specified in the Trigger Specification menu.
6. Repeat steps 4 and 5 once.
7. Enter the Trigger Specification menu. Set the TRIGGER ON field to all 1s (hexadecimal).
8. Press START SYSTEM.
9. Enter the State Table menu. Note that the data highlighted is the trigger word. This data should match the trigger value specified in the Trigger Specification menu.
10. Repeat steps 8 and 9 once.
11. Enter the Trigger Specification menu. Set the TRIGGER ON field to all 2s (hexadecimal).
12. Press START SYSTEM.
13. Enter the State Table menu. Note the data highlighted as the trigger word. This data should match the trigger value specified in the Trigger Specification menu.
14. Repeat steps 12 and 13 once.
15. Enter the Trigger Specification menu. Set the TRIGGER ON field to all 4s (hexadecimal).
16. Press START SYSTEM.
17. Enter the State Table menu. Note that the data highlighted is the trigger word. This data should match the trigger value specified in the Trigger Specification menu.
18. Repeat steps 16 and 17 once.
19. Enter the Trigger Specification menu. Set the TRIGGER ON field to all 8s (hexadecimal).
20. Press START SYSTEM.
21. Enter the State Table menu. Note that the data highlighted is the trigger word. This data should match the trigger value specified in the Trigger Specification menu.
22. Repeat steps 20 and 21 once.

(8) Verifying Triggering On Xs

The following steps verify the word recognizer's ability to ignore specific bits in the trigger.

1. Enter the Channel Specification menu. Set the RADIX field of all 91A04A and 91AE04A modules to BIN (binary).
2. Enter the Trigger Specification menu. Set the TRIGGER ON field for all the 91A04A and 91AE04A modules to XXX1 binary. (For example, if there is one 91AE04A module and one 91A04A module in your system, the trigger word is XXX1 XXX1.)

3. Press START SYSTEM.
4. Enter the State Table menu. Note that the data highlighted is the trigger word. Each module should have only odd numbers as the trigger word.
5. Repeat steps 3 and 4 four more times.
6. Enter the Trigger Specification menu and change the trigger word to XXIX.
7. Press START SYSTEM.
8. Enter the State Table menu. Note that the data highlighted is the trigger word. Each module should have every third or fourth word as the trigger word.
9. Repeat steps 7 and 8 four more times.
10. Enter the Trigger Specification menu. Set the trigger word for all 91A04A and 91AE04A modules to X1XX binary.
11. Press START SYSTEM.
12. Enter the State Table menu. Note that the data highlighted is the trigger word. Each module should have every fifth, sixth, seventh, or eighth word as a possible trigger word.
13. Repeat steps 11 and 12 four more times.
14. Enter the Trigger Specification menu. Set the trigger word for all 91A04A and 91AE04A modules to 1XXX binary.
15. Press START SYSTEM.
16. Enter the State Table menu. Note that the data highlighted is the trigger word. Each module should have all words from 8 and higher as possible trigger words.
17. Repeat steps 15 and 16 four more times.

(9) Verifying the High-Speed Internal Clocks

The following steps verify the operation of the two high speed clocks (5 ns and 3 ns) that are resident on the 91A04A board.

1. Press the PATTERN GENERATOR key to enter the Pattern Generator menu. Adjust the CLOCK field to 40 ns, then adjust the pattern generator program to look like this:

SEQ	LABEL	HEX	INSTRUCTIONS	STROBES
0		0000	GOTO 200	
200	200	0000		
201		1111		
202		2222		
203		4444		
204		8888		
205		FFFF	GOTO 200	

2. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 5 ns.
3. Enter the Trigger Specification menu. Set the TRIGGER ON field for all the 91A04A and 91AE04A modules to 0001 binary. (For example, if there were one 91AE04A and one 91A04A module in your system, the trigger word would be 0001 0001.)
4. Press START SYSTEM.
5. Examine the data acquired in the Timing Diagram menu. Decrease the magnification of the menu to 1. The display should show a walking-ones pattern in the four channels of each of the modules under test (similar to Figure 5-2).
6. Increase the magnification of the menu to 10. Count the number of sequences across an average high bit. The bit should be about 7 sequences wide (5, 6, 7, 8, 9, and 10 are all acceptable widths because of variations in the pattern generator data width and because acquisition is asynchronous).
7. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 3 ns. Leave the TRIGGER ON field set to 0001 binary.
8. Press START SYSTEM.
9. Examine the data acquired in the Timing Diagram menu. Decrease the magnification of the menu to 1. The menu should show a walking-ones pattern in each of the modules under test (similar to Figure 5-2).
10. Increase the magnification of the menu to 10. Count the number of sequences across an average high bit. The bit should be about 13 sequences wide (10, 11, 12, 13, 14, 15, 16, and 17 are all acceptable widths because of variations in the pattern generator data width and because acquisition is asynchronous).

(10) Verifying the High-Resolution Mode

The following steps verify the high-resolution mode of operation. This mode uses some data steering latches not used in any other mode. Operation of these latches is verified in the following steps.

1. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 1.5 ns. Set the TRIGGER ON field for each module to 01.
2. Press START SYSTEM.
3. Enter the Timing Diagram menu. Set the magnification of the menu to 1. The pattern of acquired data should be like the data shown in Figure 5-3. Note that each 91A04A and 91AE04A module has only two channels of data acquisition.

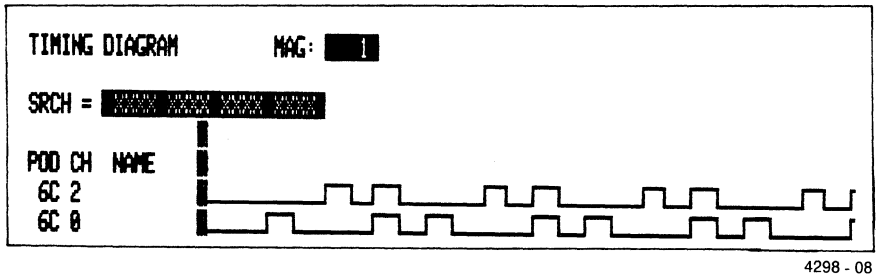


Figure 5-3. High-resolution test data.

4. Increase the magnification of the timing diagram to 10. Count the number of sequences across an individual high data bit in channel 0. The high bit should be between 19 and 35 sequences wide. Variations in the acquired bit width are caused by variations in the data width from the pattern generator module and by asynchronous acquisition.

(11) Verifying 91A32 (Slow Card) ARMS 91A04 Mode

The next test verifies the operation of the 91A04A in ARMS mode. To perform the following tests, the mainframe must contain a slow card (91A32 or 91A24) module as well as the 91A04A module under test. The slow card should have already been installed in the mainframe.

NOTE

Any slow card such as a 91A24 or 91A32 can be used to functionally check the ARMS mode of the 91A04A. If a slow card is not available, the remaining functional tests on the 91A04A cannot be performed. In that case, the 91A04A and 91AE04A functional tests are completed.

1. Enter the Pattern Generator menu. Set the pattern generator clock to 1 μs. The menu should still contain the short walking-ones program entered during the high-speed internal clock verification portion of these tests.
2. Enter the Trigger Specification menu. Set the MODE field to 91A32 ARMS 91A04.
3. In the Trigger Specification menu, set the 91A32 CLOCK to 1 μs. Set the 91A32 TRIGGER POSITION field to CENTER. Set the TRIGGER ON OCCURRENCE field to 250. Finally, verify that the 91A32 TRIGGER ON field is set to Xs (don't care).
4. Still in the Trigger Specification menu, set the 91A04 CLOCK to 500 ns. Set the 91A04 TRIGGER ON field for each 91A04A and 91AE04A module to 0001 binary. Lastly, set the 91A04 TRIGGER POSITION field to CENTER.
5. Press START SYSTEM.
6. Enter the Timing Diagram menu. Decrease the magnification field to 1. The data acquired by the 91A04A and 91AE04A modules should appear fuzzy because of an over-density of data. The 91A32 module should have acquired only 0s.

7. The slow trigger (the 91A32 trigger) should have occurred at the center of the acquired data. The 91A04A trigger (the fast trigger) should have occurred on 1 hexadecimal, within 31 sequences of the slow trigger. (31 [fast] sequences provide sufficient time for the maximum arming delay [ten slow clock periods] as well as the slow six-step pattern. See Figure 5-4.)
8. Enter the State Table menu. Examine the stored data. Verify that the display shows two 91A04A samples for every 91A32 sample.

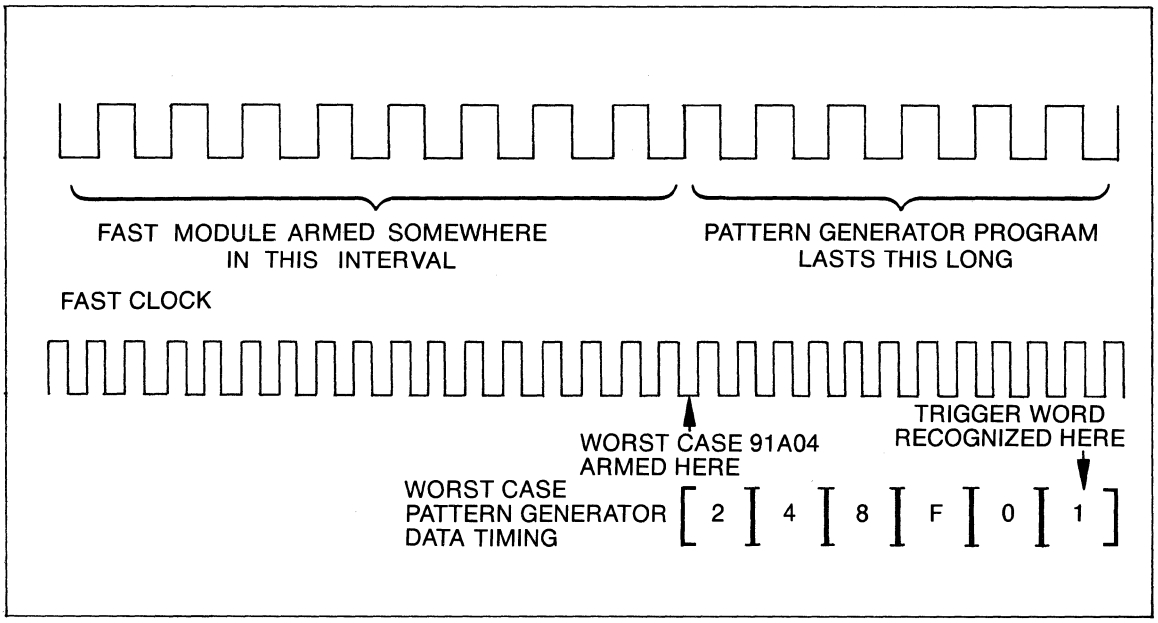


Figure 5-4. Worst-case timing for the 91A32 ARMS 91A04 test.

This completes the functional check procedure for the 91A04A and 91AE04A Data Acquisition Modules. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules to prevent damage to the modules or to the mainframe.

P6453 DATA ACQUISITION PROBE FUNCTIONAL CHECK

The P6453 functional check verifies the operation of the acquisition and deskewing capabilities of the module.

NOTE

The P6453 probe functional check is not necessary if the P6453 probe to be checked was used in a functional check for a 91A04A or 91AE04A Data Acquisition Module. The deskew circuits and channel isolation were verified in those functional checks.

You will need the following equipment to perform this procedure:

- DAS 9100 Mainframe
- 91A04A Data Acquisition Module

The following equipment is required if you wish to perform procedure *(3) Optional Probe Checks:*

- 91P16 Pattern Generator Module
- P6455 TTL/MOS Pattern Generator Probe
- Enough P6453 Data Acquisition Probes with leads and TTL-type gripper tips for all 91A04A and 91AE04A modules in the system
- Pattern generator lead set
- two rows of 10 each square pins (p/n 131-1939-00)

Refer to the *Operating Instructions* section of this addendum for instructions on module installation.

(1) Mainframe Setup for the Functional Check

The following steps configure the DAS mainframe for this functional check.

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so may damage the module or subassembly.

NOTE

The following steps may require removing modules that were previously installed in the mainframe.

1. Turn off the mainframe.
2. If a 91A04A Data Acquisition Module is already properly installed in the mainframe, leave it there. If the 91A04A is not yet in the mainframe, install it now. Be sure to follow the *Module Installation* guidelines given in the *Operating Information* section of this addendum.

CAUTION

Failure to follow the installation guidelines may result in damage to a +5 V Power Supply module.

3. Install the 91P16 Pattern Generator Module in a powered bus slot of the DAS mainframe.

(2) Verifying Deskew Operation

Next, the 91AE04A modules must be deskewed to verify the operation of the probe's deskew circuits. At the same time the POD ID button, and the pod sense line, are verified.

NOTE

Once a 91AE04A has been deskewed, do not turn off the mainframe power until the functional check is complete. If the mainframe power is turned off before the functional check is finished, the deskew operation must be performed again.

1. Enter the Trigger Specification menu. Set the MODE field in the Trigger Specification menu to 91A04 ONLY.
2. Connect the P6453 probe under test to the Pod C connector on the back of the 91A04A module. When the probe is connected to the 91A04A, the mainframe should beep and display the message POD XC CONNECTED (where X is the slot number of the 91A04A). (If the probe is already connected, disconnect it, then re-connect it to obtain the beep and message.)
3. Press the POD ID button on the housing of the probe connected to the 91A04A. The mainframe should beep again and the screen should show POD XC (where X is the slot number of the 91A04A).
4. Move the screen cursor into the DESKEW field. Follow the instructions given on the screen. All channels of the 91A04A module should deskew successfully.
5. Leave the 91A04A master module clock in deskew operation and repeat steps 2, 3, and 4 for all 91AE04A expander modules installed.

(3) Optional Probe Checks

At this point, the P6453 probes are functionally checked. If further testing is desired, perform procedures (4) and (5) in the *91A04A and 91AE04A Data Acquisition Modules Functional Check* procedure.

ADJUSTMENTS

The procedures in this subsection apply to both the 91A04A and 91AE04A unless otherwise specified. Procedures or procedural steps which apply to only one of the modules are prefixed with *91A04A only* or *91AE04A only*. If a procedure or step is not so prefixed, it applies to both modules.

These adjustments are required after extensive repair or rework on a module, or when adjustment is implied by a troubleshooting procedure or diagnostic routine.

This subsection contains a procedure for adjusting the DAC (digital-to-analog converter), and contains two procedures for adjusting comparator offsets: one using a Fluke 5101B Multimeter Calibrator as a current source, and one using a Tektronix PG502 Pulse Generator as a signal source. First, perform the *DAC Adjustment* procedure, then perform the comparator offset adjustment procedure best suited to your test equipment inventory.

CAUTION

Before attempting these adjustment procedures, make sure the modules are placed in slots according to the Module Installation *procedures in the* Operating Instructions *section of this addendum. Improper slot allocation can damage the power supplies in the DAS mainframe.*

DAC (DIGITAL-TO-ANALOG-CONVERTER) ADJUSTMENT

The following steps describe the DAC adjustment procedure. This procedure must be accomplished before attempting to adjust comparator offsets.

Test Equipment Required

Table 5-4 contains a list of test instruments and accessories required to perform the DAC setup and adjustment procedures.

Table 5-4
EQUIIPMENT REQUIRED FOR THE DAC ADJUSTMENT PROCEDURE

QTY	FUNCTION	RECOMMENDED TYPE
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	module extender	DAS Main Extender Board, p/n 670-6748-00 (no substitute)
1	digital multimeter (DMM)	Tektronix DM501A
1	maintenance accessories	DAS Service Maintenance Kit (no substitute)

Equipment Setup Procedure

NOTE

Do not install or remove any electrical module or subassembly in a DAS mainframe while the power is on. Doing so can damage the module or subassembly.

1. Power down the DAS.
2. Install the jumpers on the DAS Main Extender Board over the upper two pins (for slots 1 through 6).
3. Install the DAS Main Extender Board in the appropriate slot in the DAS, and place the module under test on the extender. If the module under test is a 91AE04A, use the long clock and word recognizer cables from the DAS Service Maintenance Kit in place of the normal clock and word recognizer cables.
4. Power up the DAS.

DAC Adjustment Procedure

Adjust the DAC on the module under test as follows:

1. Enter the Diagnostics menu (power down the DAS, then power up while holding down any key except SHIFT).
2. Select the slot in which the module under test resides, then select function 9. The DAS should display the default threshold value of 1.250 V.
3. Set the DMM to the 2 Vdc scale and monitor TP600 (just above J600) with the red meter lead, and monitor the junction of C105 and +3 VL (the minus side of C105) with the black meter lead.
4. If the threshold voltage is off by more than ±1.0 mV, adjust R818 for a DMM indication of 1.2500 V ±0.001 V.

ADJUSTING COMPARATOR OFFSETS USING THE FLUKE 5101B MULTIMETER CALIBRATOR AS A CURRENT SOURCE

Use this procedure if the P6453 used with the 91A04A/91AE04A is not available, or if the probe is not dedicated to the module under adjustment.

If a Fluke 5101B is not to be used, proceed now to the procedure titled *Comparator Offset Adjustment Using the Tektronix 250 MHz Pulse Generator as a Signal Source.*

Test Equipment Required

Table 5-5 lists the test equipment required to adjust 91A04A/91AE04A comparator offsets using the Fluke 5101B Multimeter Calibrator as a current source. Unless otherwise specified, equivalent test equipment may be substituted for the items listed in Table 5-5.

Table 5-5
EQUIPMENT REQUIRED FOR THE COMPARATOR OFFSET ADJUSTMENT PROCEDURE USING THE FLUKE 5101B

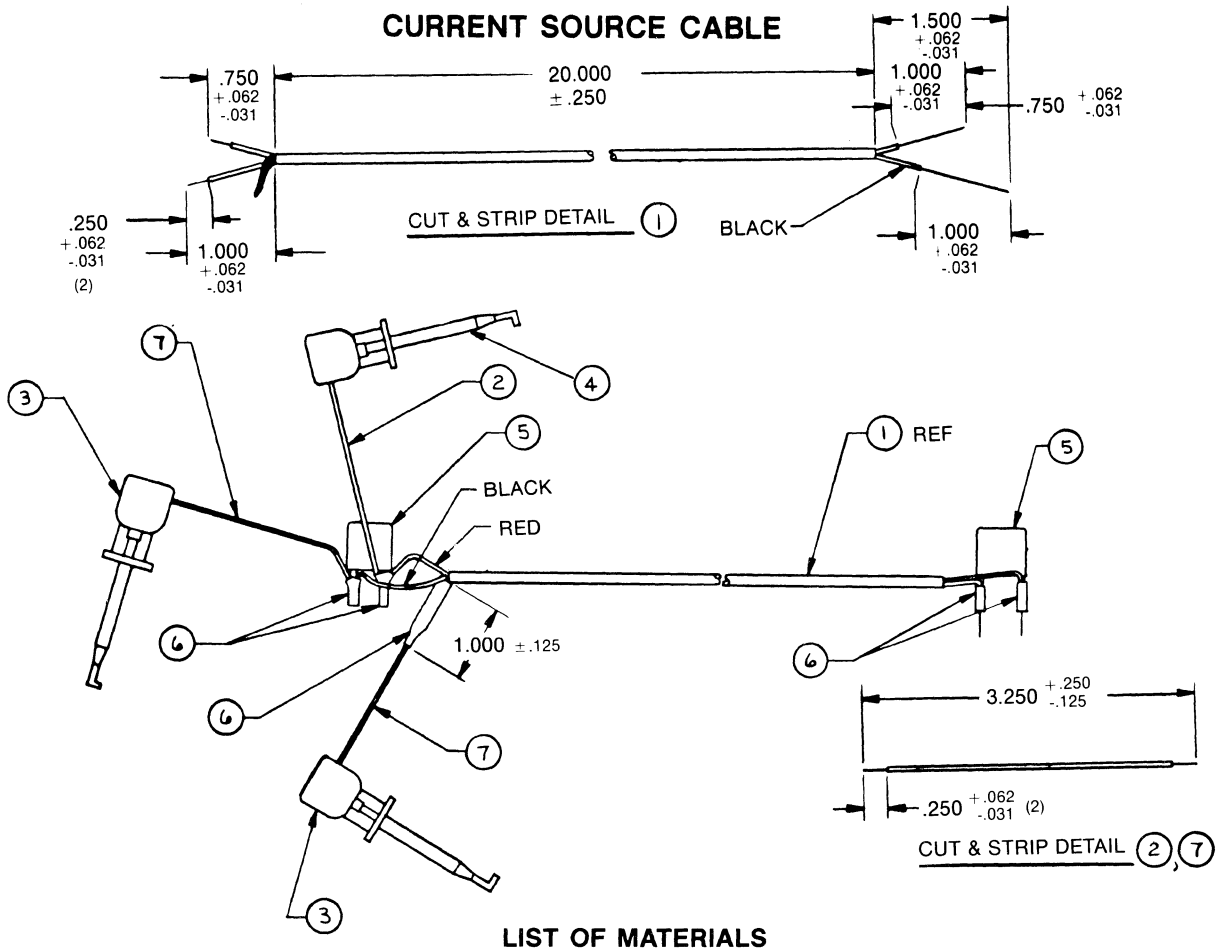
QTY	FUNCTION	RECOMMENDED TYPE
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	module extender	DAS Main Extender Board, p/n 670-6748-00 (no substitute)
1	⩾400 MHz oscilloscope	Tektronix 7904 mainframe with a 7A26 vertical amplifier, a 7B10 timebase, and a P6106 probe (X10, 10 MΩ) installed
1	constant current source	Fluke 5101B Multimeter Calibrator
1	current source cable	Refer to the *Fabricating the Current Source Cable* procedure following this table
1	maintenance accessories	DAS Service Maintenance Kit (no substitute)

Fabricating the Current Source Cable

Fabricate the current source cable in accordance with Figure 5-5. Pay special attention to lead lengths and strip lengths.

NOTE

This current cable is required only if a Fluke 5101B Multimeter Calibrator is to be used as a current source for comparator-offset adjustments. It is not required if a Tektronix PG502 250 MHz Pulse Generator is to be used as a signal source.



LIST OF MATERIALS

Item	Quantity.	Description
①	as required	Cable, SP Elect: 26 AWG (2-N & 0-N) twisted pair, shielded and jacketed (or equivalent cable)
②	as required	Wire, Elect: insulated, 26 AWG (2-N) stranded, tin top-coat, 80° PVC insulation (or equivalent wire).
③	2	Tip, Hook (black) p/n 003-0625-00 (E-Z Hook X100-W)
④	1	Tip, Hook (red) p/n 003-0624-00 (E-Z Hook X100-W)
⑤	2	Capacitor, 4.7 μf, Sprague Elect. Co. 5C37Z5U475M050B, or equivalent **(SEE NOTE)**
⑥	as required	Tubing, heatshrink, 0.093 in. dia., (Insulectro Versafit or equivalent)
⑦	as required	Wire, Elect: insulated, 26 AWG (0-N) 80° PVC insulation (or equivalent wire)

NOTE: Connect the second capacitor (not shown) across the current source binding posts in parallel with the cable connection.

4510-05

Figure 5-5 Current-source cable details.

Equipment Setup Procedure

CAUTION

Do not install or remove any electrical module or sub-ssembly in a DAS mainframe while the power is on. Doing so can damage the module or subassembly.

The following steps describe the DAS configuration and test equipment setup required to begin the comparator offset adjustment procedure for 91A04A and 91AE04A Data Acquisition Modules. This procedure uses a Fluke 5101B Multimeter Calibrator as a current source. Refer to the *Reference Information* section of this addendum for test point locations. Set up the equipment as follows:

1. Perform the *DAC Adjustment* procedure located earlier in this section. Leave the module under test on the extender when finished with the DAC adjustment.
2. Set up the oscilloscope as follows:
   a. Set vertical sensitivity to 500 mV/div.
   b. Connect the X10 probe to +5 V on the module under test.
   c. Position the oscilloscope trace on the first major division line below the top of the graticule.
3. Connect the current source cable to the Fluke 5101B: red twisted-pair to the red binding post, black twisted-pair to the black binding post.
4. Enter the 91A04A Trigger Specification menu and select external clock, rising edge. Enter the Channel Specification menu and select a threshold value of 0.00 V. Press START ACQUISITION to set the threshold on the module under test then press STOP.
5. Disconnect the P6453 Data Acquisiton Probe from the module under test.

Comparator Offset Adjustment Procedure

1. Connect the black shield connector of the current-source cable (green wire) to the GND test point near U115 on the module under test.

NOTE

Position the current-source cable as far as possible from the DAS rear cooling fan to obtain the best results from the following procedure.

2. Connect the remaining black connector of the current-source cable to +3 VL (top lead of C105).
3. Connect the oscilloscope ground also to the GND test point near U115 on the module under test.
4. Connect the red connector and the oscilloscope probe to the appropriate test points for the channel under test as listed in Table 5-6.

Table 5-6
CHANNELS, TEST POINTS, AND OFFSET ADJUSTMENTS FOR FLUKE 5101B METHOD

CHANNEL	RED CONNECTOR	OSCILLOSCOPE PROBE TIP	ADJUSTMENT (RXXX)
Data 0	U218, pin 1 (top of R203)	U218, pin 1	R201
Data 1	U311, pin 2 (top of R303)	U418, pin 1	R301
Data 2	U411, pin 2 (top of R403)	U518, pin 1	R401
Data 3	U511, pin 2 (top of R503)	U618, pin 1	R501
Clock (91A04A only)	U115, pin 2 (top of R113)	U121, pin 13	R111

5. Perform the following measurements for each channel listed in Table 5-6.
   a. Program the Fluke 5101B to output 15.080 mA, and adjust RXXX for a solid ECL high (approximately 4.1 V) on the oscilloscope with no noise present.
   b. Program the Fluke 5101B to output 14.020 mA, and adjust RXXX for a solid ECL low (approximately 3.3 V) on the oscilloscope with no noise present.
   c. Program the Fluke 5101B to output 15.060 mA, and adjust RXXX for a solid ECL high with very little noise present.
   d. Program the Fluke 5101B to output 14.040 mA, and adjust RXXX for a solid ECL low with very little noise present.
   e. Program the Fluke 5101B to output 15,040 mA, and adjust RXXX for a solid ECL high; some noise may be present.
   f. Program the Fluke 5101B to output 14.060 mA, and adjust RXXX for a solid ECL low; some noise may be present.

ADJUSTING COMPARATOR OFFSETS USING A TEKTRONIX PG502 250 MHz PULSE GENERATOR AS A SIGNAL SOURCE

This procedure describes an alternate method of adjusting comparator offset levels in a 91A04A or 91AE04A Data Acquisition Module using a Tektronix PG502 250 MHz Pulse Generator as a signal source. Performing this test requires that the P6453 Data Acquisition Probe be kept with the data acquisition module with which it was calibrated.

Test Equipment Required

Table 5-7 lists test equipment required for comparator offset adjustment using a Tektronix PG502 250 MHz Pulse Generator as a signal source. Unless otherwise specified, equivalent test equipment may be used.

Table 5-7
EQUIPMENT REQUIRED FOR THE COMPARATOR OFFSET ADJUSTMENT USING THE TEKTRONIX PG502

QTY	FUNCTION	RECOMMENDED TYPE
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	module extender	DAS Main Extender Board, p/n 670-6748-00 (no substitute)
1	⩾400 MHz oscilloscope	Tektronix 7904 mainframe with a 7A19 vertical amplifier, a 7B10 timebase, and Tektronix P6201 X10 FET probe
1	250 MHz pulse generator	Tektronix PG502 250 MHz Pulse Generator
1	high-speed acquisition test fixture	Tektronix p/n 067-1139-00 (no substitute)
1	5-1/4 inch probe ground cable	Tektronix p/n 175-0848-01

Equipment Setup Procedure

CAUTION

Do not install or remove any electrical module or sub-ssembly in a DAS mainframe while the power is on. Doing so can cause damage to the module or subassembly.

The following steps describe the DAS configuration and test equipment setup required to begin the comparator offset adjustment procedure for 91A04A and 91AE04A Data Acquisition Modules. This procedure uses a Tektronix PG502 250 MHz Pulse Generator as a signal source. Refer to the *Reference Information* section of this addendum for test point locations. Set up the equipment as follows:

1. Perform the *DAC Adjustment* procedure located earlier in this section. Leave the module under test on the extender when finished with the DAC adjustment.
2. Connect the output of the 250 MHz pulse generator to data input connector J350 on the High-Speed Acquisition Test Fixture using cable 012-0057-02. (Do not apply power to the test fixture.)
3. Connect the data outputs of the test fixture through the P6453 Probe to data channels 0-3 of the module under test.
4. Set the pulse generator as follows:
   a. Set the pulse generator to the <4 ns scale. Monitor the data output at J355 of the test fixture with the oscilloscope P6201 FET probe and 7A19 vertical amplifier.
   b. Adjust the pulse generator for an output of 600 mV p-p centered around ground, and for a 5 ns high period and a 5 ns low period (±5%). (Note any asymmetry for future use in the *Comparator Offset Adjustment Procedure.*)
5. Enter the 91A04 Trigger Specification menu and select external clock, rising edge. Enter the DAS Channel Specification menu and select 0.00 V threshold. Press START ACQUISITION to set the threshold of the module under test.
6. Adjust and connect the oscilloscope as follows:
   a. Set sensitivity to 200 mV/div.
   b. Set the FET probe to +dc offset.
   c. Connect the probe tip to pin 1 of J125 (Vbb) on the module under test.
   d. Connect the 5 1/4 inch probe ground cable to TP116 (GND) on the module under test. (Probe ground will remain at this position for all comparator offset test and adjustment steps.)
   e. Position the oscilloscope trace at the center graticule line.

Comparator Offset Adjustment Procedure

Perform the following steps to adjust comparator offset for data channels 0-3 and the clock channel. (Clock channel adjustment applies to the 91A04A only.)

1. Connect the oscilloscope probe tip to data channel 0 (pin 1 of deskew register U218) on the module under test.
2. Adjust R201 for symmetry identical to that previously noted at the pulse generator output. The signal at this test point should be centered on the graticule center line ±10%, and have a duty cycle of about 5 ns high and 5 ns low.
3. Move the oscilloscope probe tip to data channel 1 (pin 1 of deskew register U418).
4. Adjust R301 for symmetry identical to that previously noted at the pulse generator output. The signal at this test point should be centered on the graticule center line ±10%, and have a duty cycle of about 5 ns high and 5 ns low.

5. Move the oscilloscope probe tip to data channel 2 (pin 1 of deskew register U518).
6. Adjust R401 for symmetry identical to that previously noted at the pulse generator output. The signal at this test point should be centered on the graticule center line ±10%, and have a duty cycle of about 5 ns high and 5 ns low.
7. Move the oscilloscope probe tip to data channel 3 (pin 1 of deskew register U618).
8. Adjust R501 for symmetry identical to that previously noted at the pulse generator output. The signal at this test point should be centered on the graticule center line ±10%, and have a duty cycle of about 5 ns high and 5 ns low.

NOTE

If the module under test is a 91AE0A, this procedure is completed. If the module under test is a 91A04A, perform the remaining steps to adjust the clock channel.

9. **91A04A only:** Disconnect data channel 0 of the data acquisition probe from the test fixture's data output connector, and connect the data acquisition probe's clock channel to the vacated data output connector.
10. **91A04A only:** Move the oscilloscope probe tip to the clock channel (pin 13 of U121). (Pin 13 of U121 connects to pin 7 of U115.)
11. **91A04A only:** Adjust R111 for symmetry identical to that previously noted at the pulse generator output. The signal at this test point should be centered on the graticule center line ±10%, and have a duty cycle of 5 ns high and 5 ns low.

INTERNAL OSCILLATOR ADJUSTMENTS (91A04A ONLY)

You will need the following test equipment for these adjustments:

- Frequency counter
- Probe for the frequency counter

This procedure assumes that the 91A04A remains on the DAS Main Extender Board from the previous procedure.

3 ns Oscillator Adjustment

The following steps adjust the oscillator for the 3 ns internal clock.

1. Install all probe hybrids in their deskew fixtures. This biases all channels to logic highs.
2. Connect the frequency counter probe tip to TP125 on the 91A04A, and connect the probe ground to the ground (G) test point just to the left of TP125.
3. Go to the Trigger Specification menu and select 3 ns for a timebase and all 0s for word recognition.
4. Press START ACQUISITION.
5. Adjust capacitor C335 for a frequency counter indication of 330.0 MHz. Watch the frequency indication for several minutes to make sure the 91A04A is properly warmed up and the oscillator is stable.

5 ns Oscillator Adjustment

The following steps adjust the oscillator for the 5 ns internal clock.

1. Connect the frequency counter probe tip to TP125 on the 91A04A, and connect the probe ground to the ground (G) test point just to the left of TP125.
2. Go to the Trigger Specification menu and select 5 ns for a timebase and all 0s for word recognition.
3. Press START ACQUISITION.
4. Adjust capacitor C332 for a frequency counter indication of 200.0 MHz. Watch the frequency indication for several minutes to make sure the 91A04A is properly warmed up and the oscillator is stable.

J600 REPLACEMENT AND CALIBRATION

If J600 of a 91A04A master module requires replacement, the entire connector assembly, including all of the connected coaxial cables, must be replaced and the coaxial clock line must be trimmed to the proper electrical length in order for the probe to deskew correctly. A P6453 probe and a Main Extender Board is required for this procedure.

NOTE

If any component other than J600 in the clock path or data path up to the login registers is replaced, calibration of the J600 clock line must be checked. It may be necessary to retrim the clock line to achieve the proper calibration. If all channels deskew to between steps 2 through 8, no recalibration is necessary.

If J600 is replaced on the 91AE04A expander module, cut off the clock line flush with the rear of the connector and perform the Replacing J600 *procedure in the* Maintenance: General Information *section of this addendum.*

Be sure to note the exact positions of the coaxial cables relative to the board and to the connector pins when unsoldering the coaxial cables.

Replace and calibrate J600 as follows:

CAUTION

Do not remove or install a module in the DAS mainframe with the power on. Doing so can damage the module.

1. Power down the DAS and remove the 91A04A from the mainframe.
2. Unsolder the coaxial lines and remove the old J600 connector housing from the bracket as shown in Figure 6-1.
3. Install the new J600 connector in the probe bracket.

4. Cut off the clock line of the new connector to a length about eight inches longer than the clock line on the old connector, then usolder the old clock line.

5. Cut the data lines on the new connector to the same length as the corresponding lines on the old connector.

6. Solder the new data lines to the appropriate terminals on the board.

7. Connect the clock line to the holes provided near U115.

8. Set the jumpers on the module extender for slots 5 and 6, and install the extender in the mainframe.

9. Install the 91A04A on the extender and power up the DAS.

10. Deskew the probe in accordance with the *Verifying Deskew Operation* procedure which appears earlier in this section.

11. Simultaneously press SHIFT and TRIGGER SPEC to display the deskew information. Note the step at which the longest channel deskewed. This should be between steps 8 and 0C hexadecimal.

12. Calculate the length of coaxial line to be removed from the cable in order to move the deskew step back to step 7 or below.

Each deskew step is 400 ps. The desired step upon which to deskew is step 7 (2800 ps). The coaxial line propagates at 125 ps per inch. Therefore, calculate the length to be removed as follows:

$$L = \frac{(A \times 400) - (2800 - 100)}{125}$$

Where:

L= the length in inches to be removed from the cable.
A= actual deskew step with present length. (If A is a hexadecimal number, convert it to decimal.)
400= time in ps per deskew step.
2800= desired deskew step (7) X 400 ps per step.
100= a number subtracted to make sure the results are in steps 6 or 7. (The value of A may be approaching the next higher step.)
125= propagation rate of the coaxial cable in ps per inch.

For example: if A was step 9 (3600 ps), it would be necessary to remove 900 ps (7.2 inches) from the cable (7.25 inches would be acceptable).

13. Power down the DAS.

14. Unsolder the clock cable, cut it back to the calculated length, then resolder it to the holes provided.

15. Power up the DAS and again check the deskew to verify that deskew for the longest channel occurs on or before step 7. If it does, proceed to the next step. If it does not, recalculate and recalibrate in accordance with step 12.

16. Tie the coaxial cables down so that they lie flat against the board.

Positioning Word Recognizer Timing Jumper W642

In the *Performance Check* subsection of this *Verification and Adjustments* section, simplified procedures for the word recognizer timing are presented [Procedures (15) and (16)]. These procedures should be performed when a component is replaced in either the clock distribution system or in the word recognizer circuitry. If the specifications in Figure 5-9 are not met during verification, jumper W642 requires repositioning to meet the timing requirements.

Equipment Required

You will need the following test equipment and accessories to perform this procedure:

1 DC510 or DC5010 Counter/Timer with two P6201 probes.
1 Oscilloscope, 7904 or equivalent.
1 DAS Main Extender Board for each module to be extended.
1 91P16 Pattern Generator with a P6455 probe and a pattern generator lead set.
1 three-inch jumper wire.

DAS and Module Setup Procedure

CAUTION

Do not install or remove modules in a DAS mainframe with the power on. Doing so can damage the modules.

1. Power down the DAS.

2. If a 91A04A only is involved (no expander module), place a module extender in the appropriate slot (make sure the jumpers on the extender are set for slots 1 through 6), and make sure jumper J245 is placed on pins 2 and 3.

If a 91A04A is the module under test, and a 91AE04A expander module is installed, disconnect the expander module and test the 91A04A master module separately. Make sure jumper J245 is placed on pins 2 and 3 (for 91A04A-only operation), and make sure extender jumpers are set for slots 1 through 6.

CAUTION

Do not extend two or more modules without proper ventilation (refer to Extending the Modules *in the* Maintenance: General Information *section of this addendum.*

If a 91AE04A is to be the module under test, install two module extenders (one for the master module and one for the expander module under test), make sure jumper J245 on the master module is placed on pins 1 and 2, and install the modules on the extender using the short word recognizer and clock cables to connect the two modules. Install the 91AE04A to be tested so that the component side of the board is accessable.

3. Connect the pattern generator probe and lead set to the P6453 probe as described in the *Connecting a P6453 probe to a P6455 probe* procedure which appears at the beginning of this *Verification and Adjustments* section, with the following exception: **DO NOT CONNECT DATA CHANNELS 0, 1, and 2,** connect only data channel 3, ground, and VL.

4. Power up the DAS.

5. Perform steps 1 through 4 of procedure (5), *Verifying Pod Connector C*, in the *Functional Check* subsection of these *Verification and Adjustment* procedures.

6. Set channel 3 of the module under test to a 1 in the word recognizer, and set all other channels (0, 1 and 2) to DON'T CAREs.

7. Connect a three-inch jumper from TP821 (+4.2 V) to TP641 on the 91A04A master module to prevent the 91A04A from stopping by inhibiting STOP STORE(H).

91A04A Measurement Equipment Setup Procedure

Set up the test equipment as follows:

1. Set the P6201 probes to AC, DC OFFSET to OFF, 50 Ω TERM to EXT, and 1X operation.

2. Attach two 10X FET probes to the counter/timer, and to the probe power connector on the oscilloscope (or other probe power source).

3. Turn on the counter/timer and allow at least one minute warm-up time.

4. Set up the counter/timer as follows:

   a. Channel A: 50 Ω TERM, + SLOPE, DC COUPLING, 1X ATTEN, and THRES at 0.0 V.

   b. Channel B: (Same as Channel A.)

   c. Press TIME A→B.

5. Press START SYSTEM on DAS keyboard.

6. Connect both probes, using short ground leads, to TP121 and ground (G) on the module under test.

7. Press NULL on the counter/timer to zero the counter/timer-probe measurement system.

8. Press TIME A→B on the counter/timer and note the counter/timer indication for the correction factor.

9. Disconnect the probes from the reference (TP121 and ground).

91A04A W642 Delay Jumper Selection and Positioning Procedure

Measure the W642 delay and position its jumpers as follows:

1. Change the polarity on counter/timer channel B to - SLOPE.

2. Connect the counter/timer channel A probe to pin 2 of U245 (the earliest signal). Use a short lead for probe ground.

3. Connect the counter/timer channel B probe to pin 2 of U641 (the last signal in the chain). Use a short lead for probe ground.

4. Record the counter/timer indication and compute the true reading by subtracting the correction factor obtained earlier from this measured indication. The true reading should be between 14.20 ns and 14.80 ns.

NOTE

The DC5010 Counter/Timer will sometimes add the period of the 20 MHz clock to the reading. When this occurs, measure the period of the clock at TP121, and subtract it from the measured reading; i.e., 64.75 − 50.00 = 14.75 ns.

CAUTION

Do not u*se a soldering iron with a rating in excess of 15 W. Doing so can cause circuit board laminations to separate.*

If the number is too large, remove the appropriate delay (in ps) by using the delay chart on schematic 57A for the different delay steps in jumper W642. If the number is too small, add the appropriate delay. A pinout diagram of W642 is included in the *Test Point, Jumper, and Adjustment Locations* diagram in the *Maintenance: Reference Information* section of this addendum.

5. Perform step (15) *High Speed Word Recognizer Timing Check* in the *Performance Check* subsection of these *Verification and Adjustment* procedures. If the timing is out of the tolerances shown in Figure 5-9, an adjustment of jumper W150 (schematic 57A) is necessary. (This adjustment is rarely required and should not be done unless you are absolutely certain correct timing cannot be accomplished with W642.) W150 is hard-wired to the board and, by re-wiring, 400 ps can be added or subtracted in the CLK D line.

To subract 400 ps, cut the wires connected to the bottom two pins (pins 1 and 2) of W150, and solder a small jumper wire directly across pins 1 and 2. This will subtract from hold time and add to set-up time.

To add 400 ps, cut the wires connected to the bottom two pins (pins 1 and 2 of W150, then connect a small jumper wire across the two pins on the left (pins 1 and 4) and connect another small jumper wire across the two pins on the right (pins 2 and 3). This will add to hold time and subtract from set-up time.

Positioning W642 on a 91AE04A Expander Module. Proceed as follows:

If the module under test is an expander module, perform the *DAS and Module Setup Procedure*.

91AE04A Measurement Equipment Setup Procedure

Set up the test equipment as follows:

1. Set the P6201 probe COUPLING to AC, DC OFFSET to OFF, 50 Ω TERM to EXT, and 1X operation.
2. Attach the two 1X FET probes to the counter/timer, and to the probe power connector on the oscilloscope (or other probe power source).
3. Turn on the counter/timer and allow at least one minute warm-up time.
4. Set up the counter/timer as follows:
   a. Channel A: 50 Ω TERM, + SLOPE, DC COUPLING, 1X ATTEN, and THRES at 0.0 V.
   b. Channel B: (Same as Channel A.)
   c. Press TIME A→ B.
5. Press START SYSTEM on DAS keyboard.
6. Connect both probes, using short ground leads, to TP121 and ground (G) on the module under test.
7. Press NULL on the counter/timer to zero the counter/timer-probe measurement system.
8. TIME A→B on the counter/timer and note the counter/timer indication for the correction factor.
9. Disconnect the probes from the reference (TP121 and ground).

91AE04A W642 Delay Selection and Positioning Procedure

Measure the W642 Delay and position its jumpers as follows:

1. Change the polarity on counter/timer channel B to - SLOPE.
2. Press TIME A→B on the counter/timer.
3. Connect the counter/timer channel A probe to J138 (the earliest signal) on the module under test. Use a short lead for probe ground.
4. Connect the counter/timer channel B probe to J141 (the latest signal) on the module under test. Use a short lead for probe ground.
5. Record the counter/timer indication and compute the true reading by subtracting the correction factor obtained earlier from this measured indication. The true reading should be between 11.60 ns and 12.20 ns.

CAUTION

Do not use a soldering iron with a rating in excess of 15 W. Doing so can cause circuit board laminations to separate.

If the number is too large, remove the appropriate delay (in ps) by using the delay chart on schematic 65A for the different delay steps in jumper W642. If the number is too small, add the appropriate delay. A pinout diagram of W642 is included in the *Test Point, Jumper, and Adjustment Locations* diagram in the *Maintenance: Reference Information* section of this addendum.

6. Perform step (16) *91AE04A to 91A04A High Speed Word Recognizer Timing* check in the *Performance Check* subsection of these *Verification and Adjustment* procedures. If the timing is out of the tolerances shown in Figure 5-9, readjust W642 in the appropriate direction without going outside the 11.9 ns ±0.3 ns range. (If this is not possible, a component in the 91AE04A is probably defective.)

PERFORMANCE CHECK

The Performance Check Procedure provides a detailed check of internal and external product characteristics. These procedures assume that the P6453 Data Acquisition Probe to be used in these performance checks is the probe to be used with the module in normal operation.

The Performance Check Procedure is organized into a set of tests for 91A04A/91AE04A module combinations.

91A04A AND 91AE04A DATA ACQUISITION MODULES CHECK PERFORMANCE

This procedure checks the performance of any valid combination of 91A04A and 91AE04A modules and probes. All 91A04A and 91AE04A modules and their probes operate as a system, so they must be tested as a system.

CAUTION

Before attempting these performance checks, make sure the modules are installed in accordance with the Module Installation *procedures in the* Operating Instructions *section of this addendum. Improper slot allocation can damage the power supplies in the DAS mainframe.*

You will need the following equipment to complete this performance check procedure.

- DAS mainframe
- Enough P6453 Data Acquisition Probes for all 91A04A and 91AE04A modules in the system
- The High-Speed Acquisition Test Fixture (067-1139-00)
- +5 V power supply
- Two power cables with banana plugs on each end
- DAS Main Extender Board (one for each module to be extended)
- Two coaxial extender cables for 91A04A to 91AE04A connections
- 12-inch-long threshold Vbb cable
- 400 MHz two-channel oscilloscope with low capacitance probes

- 300 MHz sinewave generator
- 250 MHz pulse generator
- Digital multimeter (DMM)
- 350 MHz frequency counter

NOTE

These procedures require familiarity with high-speed electrical measurement techniques. Refer to Oscilloscope Techniques for High Frequency Measurements *in the* Reference Information section of this addendum.

What These Procedures Test

When all the 91A04A/91AE04A perfomance check procedures are completed, the 91A04A/91AE04A system will have verified that it can perform the following functions:

- Acquire synchronous data at speeds up to 300 MHz
- Consistently store data with 3 ns setup and 0.3 ns hold times with 600 mV p-p data
- Sample data at 660 MHz (high-resolution mode)
- Trigger on 4-ns-wide data (high-resolution mode)
- Meet the specified high-speed internal clock accuracy
- Meet minimum detectable pulse width specifications at 1.5 ns and 3.0 ns sampling rates

(1) Test Equipment Setup for the Performance Checks

The test equipment setup given next is used to test internal clock accuracy, asynchronous word recognition, the minimum detectable pulse width, and setup and hold times.

The equipment required for the test setup includes the following:

- High speed-acquisition test fixture and its three cables
- +5 V power supply
- 300 MHz sine wave generator
- 250 MHz pulse generator
- Digital Multimeter (DMM)

Figure 5-6 shows the test equipment connections. Refer to this figure while making the connections.

The High-Speed Acquisition Test Fixture comes with three cables, two of which have been adjusted to match the test fixture with the 250 MHz pulse generator. For this reason **ALWAYS USE THE SAME 250 MHz PULSE GENERATOR AND CABLES WITH THE TEST FIXTURE.** As long as the same three cables and the same pulse generator are used with the fixture, it only needs to be adjusted once. If a different pulse generator or cable is used, or if the 250 MHz pulse generator went in for service and had parts replaced in the trigger-to-output path, the test fixture must be re-adjusted.

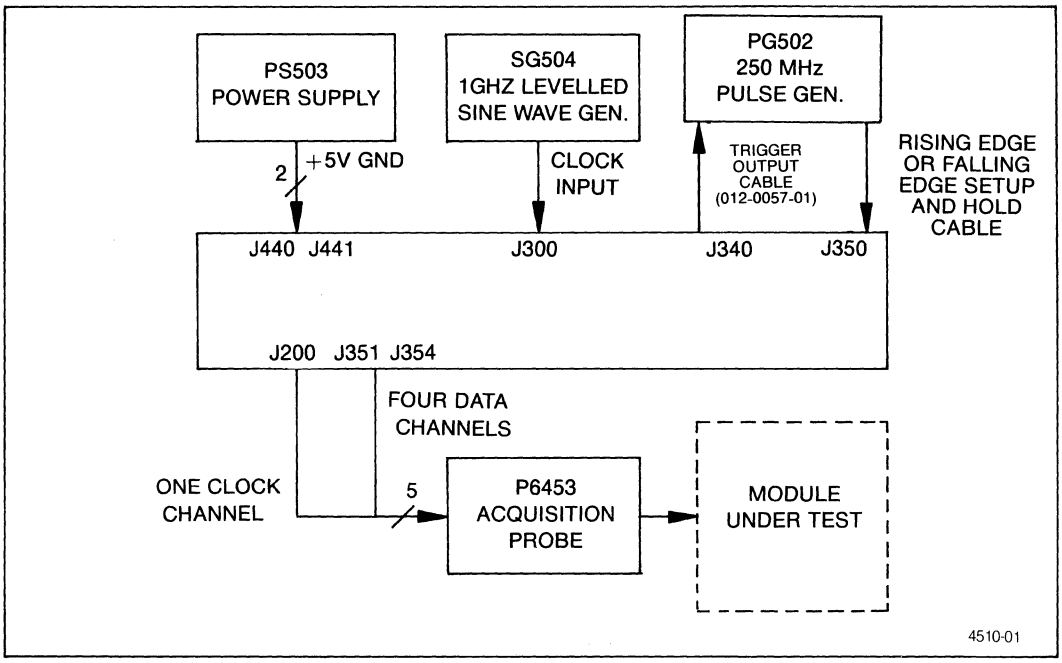


Figure 5-6. 91A04A and 91AE04A performance check test equipment connections.

The next steps describe attachment of the test equipment to the test fixture. Figure 5-11 shows how the test equipment is configured.

CAUTION

Do not connect power-supply voltage lines to the test fixture with the power supply turned on. Doing so can damage test-fixture circuits.

1. Turn the +5 V power supply off.
2. Connect +5 V from the power supply to J441 (+5 V input) on the test fixture.
3. Connect the power supply ground to J440 (ground) on the test fixture.
4. Connect the DMM negative lead to clock offset test point TP520, and connect the DMM positive lead to +5 V test point TP340 on the test fixture (These test points are not labeled on the test fixture, only on the schematic.)

WARNING

Make sure the power supply cord is plugged into a grounded outlet before turning the power supply on. An ungrounded power cord can result in hazardous voltages at the test fixture.

5. Turn on the +5 V power supply and wait until the DMM indication has stabilized.
6. Adjust clock offset potentiometer R422 on the test fixture for a DMM indication of +1.30 V ±20 mV.
7. Connect the output of the sinewave generator to the 50 Ω input of the frequency counter. Set the sinewave generator frequency to 300 MHz ±0.2 MHz.

8. Connect the sinewave generator output to clock input J300 on the test fixture.
9. Connect the clock line of the acquisition probe to clock input J200 on the test fixture.
10. Monitor the output of the sinewave generator at clock test point J400 on the test fixture using the oscilloscope's 10X 500 Ω probe (P6056). Set the sinewave generator output level to 700 mV centered around ground.
11. Connect trigger output J340 of the test fixture to the 50 Ω input of the oscilloscope. Check the amplitude of the trigger output signal for ≥1.0 V p-p (typically 2.0 V p-p). Clock offset potentiometer R422 on the test fixture may require readjustment to obtain the required level.
12. Replace the oscilloscope with the frequency counter and check the indicated frequency for approximately 150 MHz.
13. Connect the trigger cable (p/n 012-0057-01) from trigger output J340 on the test fixture to the pulse generators + TRIG DURATION input connector.
14. Connect the coaxial cable labeled RISING EDGE CABLE between the pulse generator's output connector and data input J350 on the test fixture.
15. Connect the P6453 probe of the 91A04A under test to data output connectors J351 through J354 (data bits 0-3, respectively) on the test fixture.
16. Set the pulse generator to external trigger. Set the internal period to the ≤2 ns range. Connect the oscilloscope's 10X 500 Ω probe (P6056) to data output test connector J355 on the test fixture, and adjust the pulse generator output as follows:
    a. Set the amplitude at 600 mV p-p centered around ground.
    b. Set the duty cycle at 3.33 ns high and 3.33 ns low ±5%.
17. Disconnect the trigger cable (p/n 012-0057-01) from J340 on the test fixture. This cable will not be used again until later in the tests.

The test equipment is now set for use.

(2) Mainframe Setup for the Performance Checks

The first tests of the 91A04A module examine the clock signals on the module. The tests involve observing signals on the 91A04A module itself, so the module must be placed on an extender.

The next steps require the following equipment:

- DAS mainframe
- P6453 probe
- DAS Main Extender board

CAUTION

Do not install or remove any electrical module in the DAS mainframe while the power is on. Doing so can damage the module.

1. Turn off the DAS mainframe.
2. Set the square pin jumpers on the main extender board for slots 1-6.
3. If the 91A04A module is currently installed in a mainframe, remove it.
4. Install the main extender board in a powered bus slot of the DAS mainframe in accordance with the *Module Installation* procedures in the *Introduction and Specifications* section of this addendum. If two or more modules are to be placed on extenders, provide for ventilation as prescribed in *Extending the Modules* in the *Maintenance: General Information* section of this addendum.
5. Install the 91A04A module under test on top of the extender board.
6. Turn on the DAS mainframe.
7. Install a P6453 probe in the back of the 91A04A module.

(3) Internal Power Supply Test

This test verifies the accuracy of the +3 V, +4.2 V, and +15 V internal power supply voltages in the 91A04A (or 91AE04A) Data Acquisition Module. A DMM is required for these checks. Verify power supply accuracy in accordance with Table 5-8.

Table 5-8
INTERNAL POWER SUPPLY MEASUREMENTS

Voltage	Tolerance	DMM +Lead	DMM -Lead
+3 V	Vcc−1.92 V±50 mV	R195, top end	+5V
+3 VL	Vcc−1.95 V ±100 mV	C105, top end	ground (G)
+4.2 V	Vcc−0.8 V ±50mV	TP821 (4.2 V)	+5 V
+15 VC	±5%	junction of T201 and C201	TP116 (ground)
+15 VD	±5%	junction of T401 and C401	TP116 (ground)

(4) Internal Clock Accuracy Test (91A04A Only)

The next steps test the accuracy of the two high-speed time bases resident on the 91A04A module. The equipment required for the next few steps includes the following:(Air should be blowing on the 91A04A and the temperature stablizers when making these measurments.)

- 350 MHz frequency counter
- Probe for the frequency counter

1. Turn on the frequency counter to allow the counter to stabilize.
2. Install all of the probe hybrids in their deskew fixtures. This biases the hybrids so they always read 1.
3. Enter the Trigger Specification menu of the DAS. Set the MODE field to 91A04 ONLY. Set the 91A04 CLOCK field to 3 nS. Set the TRIGGER ON field to all 0s. This will prevent the modules from triggering during the test.
4. Connect the probe for the counter to test point TP125 of the 91A04A. If the probe needs a ground, the probe may be grounded at the ground test point labeled G and located just to the left of TP125.
5. Press START ACQUISITION on the DAS keyboard. The 91A04A module should now send its 330 MHz clock to the frequency counter.
6. Read the frequency counter. The measured frequency should read between 326 MHz and 334 MHz. Perform the *3-ns Oscillator Adjustment* procedure (in this section) if the frequency is at or beyond those limits.

The previous steps verified the accuracy of the 3 ns internal clock. The next steps examine the 5 ns internal clock.

7. Leave the frequency-counter probe connected to the same test points.
8. Press the STOP key on the DAS. Enter the Trigger Specification menu of the DAS. Set the 91A04 CLOCK to 5 nS.
9. Press the START ACQUISITION key.
10. The frequency counter should now read between 195 MHz and 205 MHz. Perform the *5-ns Oscillator Adjustment* procedure (in this section) if the frequency is at or beyond those limits.
11. Remove the frequency counter probe from the 91A04A module.

The accuracy of the 91A04A module's two internal clocks has now been verified.

(5) Functional Tests

In order to perform a complete performance check on a 91A04A and 91AE04A system, the functional check must also be performed on the system. At this point, go to the *Functional Check* procedure and perform all the tests given there. When the functional check is complete, return to this point in the performance check and continue.

(6) DAS Mainframe Setup

The following steps provide the setup of the DAS mainframe for the remainder of the performance check procedure.

CAUTION

Do not install or remove any module in the DAS mainframe while the power is on. Doing so can damage the module.

Also, failing to follow the installation guidelines will make test results invalid, and may result in the failure of a +5 V Power Supply. Refer to Module Installation *in the* Operating Instructions *section of this addendum.*

The following steps assume that the functional check has just been completed, and that the 91A04A and 91AE04A modules are installed in accordance with the installation guidelines.

1. Turn off the DAS.
2. Connect all cables between the 91A04A and 91AE04A modules.
3. Double-check that the module installation requirements have been met, then turn on the mainframe.
4. Follow the instructions for the setting clock offset on 91AE04A modules. This information is found in the *91A04A, 91AE04A, and P6453 Operator's Manual Addendum* or in the *Adjustments* subsection of this *Verification and Adjustments* section.
5. Install P6453 probes on the back of all 91A04A and 91AE04A modules under test.
6. Enter the Trigger Specification menu. Set the MODE field to 91A04 ONLY. Deskew all the 91A04A and 91AE04A probes according to the instructions given in the menu.
7. Enter the Channel Specification menu of the DAS. Change the RADIX field of all 91A04A and 91AE04A modules to BIN (binary).
8. DO NOT turn off the mainframe. Leave the mainframe on so the 91A04A and 91AE04A modules will stay warmed up and the deskewing parameters are not lost.

(7) 660 MHz Asynchronous Word Recognition Test, Channel 0

This test verifies that the data trigger will synchronize across different modules and that a 4-ns-wide word can be recognized in channel 0 of each 91A04A and 91AE04A module in the system. In addition to the previous equipment setup, you will need the following equipment:

- 400 MHz oscilloscope
- Low-capacitance oscilloscope probe

NOTE

This procedure is based on the assumption that there are three expander modules installed in addition to the 91A04A master module.

1. Observing polarity, connect data channel 0 of each module installed to one of the pairs of data output pins on the test fixture (J351-J354). (Connect directly to the P6453. Do not use gripper tips or the leads from the gripper tips.) Connect unused channels to the deskew connectors on the P6453 Probe.
2. Set the oscilloscope to 200 mV/div and 5 us/div, then connect its low capacitance probe tip to pin 1 of J125 (Vbb) on the module under test. Ground the oscilloscope probe to the ground test point (G) just to the left of TP125, then position the oscilloscope trace at the graticule center line.
3. Observe the signal from one of the data outputs of the fixture (J351-J354) with the oscilloscope. Change the setting of the pulse generator so the oscilloscope displays a 4 ns positive-going pulse with a 10 μs period.
4. Use the oscilloscope to set the output amplitude of the data output to 600 mV p-p centered about ground. Verify that this did not change the pulse width. If necessary, readjust the pulse shape.
5. Set the pulse generator to trigger manually, rather than at a constant rate.
6. Enter the Channel Specification menu. Change the THRESHOLD field of all 91A04A and 91AE04A modules in the mainframe to VAR +0.00V.
7. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 1.5 ns.
8. Set the 91A04A and 91AE04A triggers to 1 in the least significant positions of each module. For example, if the system contains one 91A04A and three 91AE04A modules, the trigger word should be (binary) X1 X1 X1 X1 (X1 for each board installed).
9. Press START SYSTEM to start acquisition.
10. The DAS display should show the message WAITING FOR 91A04 TRIGGER.
11. Press the manual trigger button on the pulse generator. The 91A04A should trigger immediately.
12. Set the magnification to 1 and examine the acquired data to locate the trigger word. Once the trigger is located, increase the magnification to 10. Each line that received the trigger should show a high pulse that is two to four sequences wide. All of these pulses on the display should overlap by at least one storage cycle.

(8) 660 MHz Asynchronous Word Recognition Test, Channel 2

The previous test verified that channel 0 of all 91A04A and 91AE04A modules in the system can capture a 4-ns-wide trigger word. The next test verifies channel 2.

Move the data connections to channel 2 of of each module installed and repeat procedure (7). Connect unused channels to the deskew connectors on the P6453 Probe.

(9) 330 MHz Asynchronous Word Recognition Test, Channel 1

The previous tests verified that channels 0 and 2 of all 91A04A and 91AE04A modules in the system can capture a 4 ns trigger word. The next test verifies that channel 1 can capture a 5 ns trigger word.

1. Set the pulse generator duration to 5 ns.
2. Move the data connections from channel 0 to channel 1 of each module. Connect the unused channels to the deskew connectors on the P6453 Probe.
3. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 3 ns. Verify that the MODE field says 91A04 ONLY.
4. Set the 91A04A and 91AE04A triggers to 1 in the next to least significant positions of each module. For example, if the system contains one 91A04A and one 91AE04A module, the trigger word should be XX1X XX1X (binary).
5. Press START SYSTEM to start acquisition.
6. The DAS display should show the message WAITING FOR 91A04 TRIGGER.
7. Press the manual trigger button on the pulse generator. The 91A04A should trigger immediately. (If the modules do not trigger, the performance check has not passed.)
8. Set the magnification to 1 and examine the acquired data to locate the trigger word. Once the trigger is located, increase the magnification to 10. Each line that received the trigger should show a high pulse that is one to two sequences wide. All of these pulses on the display should overlap by at least one storage cycle.

(10) 330 MHz Asynchronous Word Recognition Test, Channel 3

The previous tests verified that channels 0, 1, and 2 of all 91A04A and 91AE04A modules in the system can capture a trigger word. The next test verifies that channel 3 can capture a 5 ns wide trigger word.

Move the data connections to channel 3 and repeat procedure (9). Connect unused channels to the deskew connectors on the P6453 probe.

(11) 1.5 ns Data Acquisition Test

The next steps verify that the 91A04A/91AE04A system can consistently acquire 3.5-ns-wide pulses.

1. Disconnect data acquisition channels 1 and 3 from the high-speed acquisition test fixture and connect channels 0 and 2.
2. Use the oscilloscope to observe the signal on one of the DATA pins on the test fixture. Change the setting of the pulse generator so the oscilloscope displays a 7-ns-period square wave, 3.5 ns high and 3.5 ns low.
3. Use the oscilloscope to set the output amplitude of the pulse generator to 600 mV p-p centered about ground. Verify that this did not change the pulse period and width. If necessary, readjust the pulse shape.
4. Enter the Trigger Specification menu. Set the 91A04 CLOCK field to 1.5 ns. Set the 91A04 trigger to all Xs (don't care).
5. Press START SYSTEM.
6. Examine the data acquired by the two modules under test. Increase the magnification of the display until the displayed data is easy to interpret.
7. The data acquired should consistently show 1-to-3-sequence-wide alternating high and low pulses but the edges on different channels will probably not line up. Scan all the acquired data to make sure that none of the modules under test dropped any pulses.
8. The two modules just tested have now passed the 1.5 ns data acquisition test. If there are other 91AE04A modules in the system that have not yet performed this test, select the next one(s) to test and repeat all of the steps given under this heading *(11) 1.5 ns Data Acquisition Test.*

(12) Setup and Hold Time Test Setup

The next tests verify a wide variety of the 91A04A and 91AE04A module's capabilities. Capabilities verified are:

- Minimum data and clock amplitude :600 mV-700 mV
- Minimum data period for synchronous acquisition :3.3 ns
- Maximum external clock frequency with all channels operating :300 MHz
- Setup time:3 ns
- Hold time:0.3 ns

These steps assume that the high speed acquisition test fixture has already been calibrated to match your pulse generator. If this is not the case, calibrate the test fixture according to *Instructions: High Speed Acquisition Test Fixture 067-1139-00.*

1. The 250 MHz pulse generator, the 330 MHz sine wave generator, and the high-speed acquisition test fixture should still be connected as they were at the beginning of this performance check procedure.
2. Connect the cable labled TRIGGER IN (p/n 012-0057-01) between the OUTPUT connector on the test fixture and the trigger- in connector on the pulse generator. The clock and data signals must be synchronized for the remaining tests.
3. Using the oscilloscope, monitor clock output test point J400 on the test fixture. Adjust the sine wave generator so that the oscilloscope displays a 300 MHz sine wave that is 700 mV p-p centered around ground.
4. Set the pulse generator controls to receive an external trigger.
5. Using the oscilloscope, observe the signal from one of the DATA connectors of the test fixture. The signal should be a pulse train at one-half the frequency of the sine wave generator. Adjust the pulse generator to output a square wave that is 600 mV p-p and centered around ground.
6. Trigger the oscilloscope on the positive external trigger output of the pulse generator and measure the time from any ground crossing of the data square wave to a rising edge ground crossing of the clock sine wave (setup time). This time should be 3.0 ns ±100 ps (refer to Figure 5-7). Otherwise, the test fixture is not properly calibrated.
7. Connect the frequency counter to clock test point J400 on the test fixture.
8. Adjust the frequency of the sine generator between 299.5 and 300.5 MHz so the data signal has precisely 3.0 ns setup time. The data signal should also show precisely 0.3 ns hold time (refer to Figure 5-7).

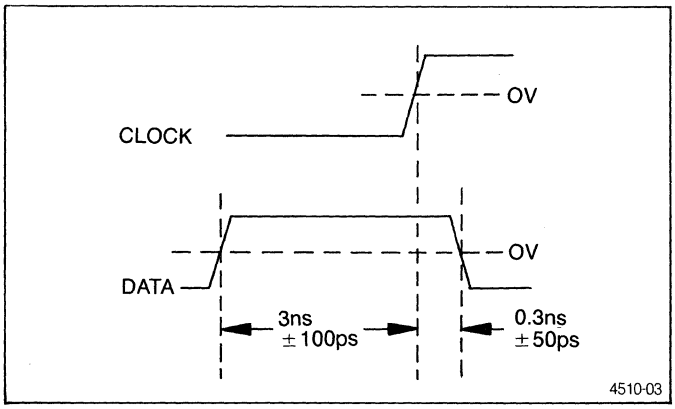


Figure 5-7. Rising-edge setup and hold time waveforms.

9. The previous adjustments should not have changed the pulse width and voltage setup, but double-check them now. The clock waveform should be:

- 700 mV p-p and centered around ground
- Running at 300 MHz

The data waveform should be:

- 600 mV p-p and centered around ground
- Running at half the clock rate

(13) 300 MHz Rising-Edge Clock Setup-and-Hold-Time Test

The next steps verify that the modules under test can acquire a 300 MHz 0 - F pattern that meets the data setup and hold time specifications.

1. The data and clock channels from the 91A04A's P6453 probe should still be connected to the high speed acquisition test fixture.
2. Enter the Channel Specification menu of the DAS. Verify that all the 91A04A and 91AE04A modules have their THRESHOLD fields set to VAR +0.00V.
3. Enter the Trigger Specification menu of the DAS. The MODE field should be set to 91A04 ONLY. Set the 91A04 CLOCK field to EXTERNAL rising edge. Set the TRIGGER ON field to all 1s.
4. Press the START ACQUISITION key. The DAS should trigger immediately.
5. Enter the Timing Diagram menu. Increase the magnification of the display to 10. The four channels of acquired data should all show an alternating high/low pattern. All four channels should rise and fall at the same time and the high and low pulses should all have the same duration.
6. Scan through all of the acquired data. The acquired data pattern should be consistent throughout all the data.
7. Press STORE to store 512 (default) bits in reference memory.
8. Press COMPARE ≠, then wait for five restarts to ensure intermittent storage cycles.
9. Disconnect only the data channels of the module previously tested. The 91A04A clock channel must remain attached to clock output connector J200 of the high speed acquisition test fixture.
10. The module just tested has now passed the rising-edge clock setup-and-hold-time test. If all 91A04A and 91AE04A modules have been tested, you have completed the rising edge clock setup-and-hold-time test. If any 91AE04A modules have not yet been tested, select the module you want to test next and repeat the procedure.

(14) 300 MHz Falling-Edge Clock Setup-and-Hold-Time Test

The next steps verify that the modules under test can acquire a 300 MHz 0 - F pattern that meets the data setup and hold time specifications. The setup for this test and the test results are similar to the previous setup-and-hold-time test.

1. Disconnect the cable labeled RISING EDGE CABLE from the pulse generator and the test fixture. Connect the cable labeled FALLING EDGE CABLE in place of the cable just removed.
2. Using the oscilloscope, measure the time from any ground crossing of the data square wave to a falling edge ground crossing of the clock sine wave (setup time). This time should be 3.0 ns ±100 ps (refer to Figure 5-8). Otherwise the test fixture is not properly calibrated.

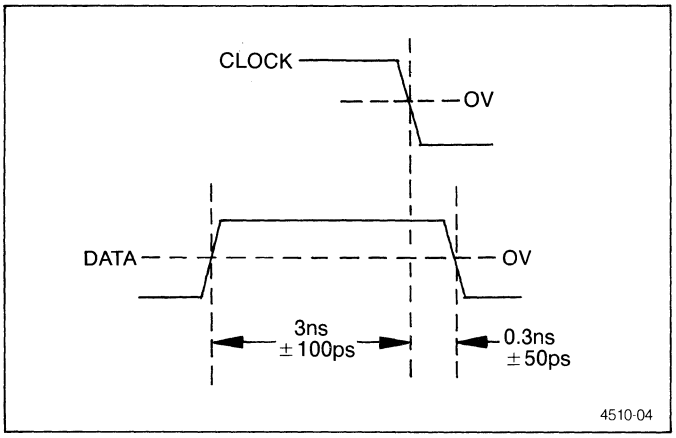


Figure 5-8. Falling-edge setup and hold time waveforms.

3. Connect the frequency counter to data test point J355 on the test fixture.
4. Adjust the frequency of the sine generator between 299.5 and 300.5 MHz so the data signal has precisely 3.0 ns setup time. The data signal should also show precisely 0.3 ns hold time (refer to Figure 5-8).
5. The previous adjustments should not have changed the pulse width and voltage setup, but double check them now. The clock waveform should be:
   - 700 mV p-p and centered around ground
   - Running at 300 MHz

   The data waveform should be:
   - 600 mV p-p and centered around ground
   - Running at half the clock rate
6. Enter the Channel Specification menu of the DAS. Verify that all the 91A04A and 91AE04A modules have their THRESHOLD fields set to VAR +0.00V.
7. Enter the Trigger Specification menu of the DAS. The MODE field should be set to 91A04 ONLY. Set the 91A04 CLOCK field to EXTERNAL falling edge. Set the TRIGGER ON field to all 1s.
8. Press the START ACQUISITION key. The DAS should trigger immediately.

9. Enter the Timing Diagram menu. Increase the magnification of the display to 10. The four channels of acquired data should all show an alternating high/low pattern. All four channels should rise and fall at the same time and the high and low pulses should all have the same duration.
10. Scan through all of the acquired data. The acquired data pattern should be consistent throughout all the data.
11. Press STORE to store 512 (default) bits in reference memory.
12. Press COMPARE ≠, then wait for five restarts to ensure intermittent storage cycles.
13. Disconnect only the data channels of the module previously tested. The 91A04A clock channel must remain attached to clock connector J200 of the high-speed acquisition test fixture.
14. The module just tested has now passed the falling-edge clock setup-and-hold-time test. If all 91A04A and 91AE04A modules have been tested, you have completed the rising edge clock setup-and-hold-time test. If any 91AE04A modules have not yet been tested, select the module you want to test next.

(15) High-Speed Word Recognizer Timing Check (91A04A Only)

The following steps verify timing of the word recognizer circuit in the 91A04A master module.

The next steps require a three-inch jumper wire in addition to the equipment used in the previous procedure.

CAUTION

Do not remove or install instrument modules in the DAS mainframe with the power on. Doing so can damage the module.

1. Power down the DAS.
2. Place the 91A04A on a module extender (place the jumpers on the extenders for slots 1-6).
3. Power up the DAS and deskew the probe in accordance with the *Module Deskewing* procedure located in the *Operating Information* section of this addendum.
4. Connect a jumper wire between TP821 and TP549 on the 91A04A to inhibit the word recognition signal.
5. Enter the DAS Trigger Spsecification menu and select:
   - falling-edge clocking (in the 91A04 External Trigger sub-menu, and
   - F (hexadecimal) as the trigger word
6. Set up the oscilloscope as follows:
   a. Set the sensitivity at 200 mV/div.
   b. Set the sweep rate at 500 ps/div.
   c. Connect the P6201 FET probe tip to 100 K Vbb at TP533, and connect the probe ground to the ground (G) test point next to U435.

d. Trigger on the external trigger output of the pulse generator.

e. Position the trace at the graticule center line.

7. Move the oscilloscope probe tip to pin 20 of U448, and connect the probe ground to TP449 (ground test point).
8. Press START ACQUISITION.
9. Carefully center the rising edge of the clock pulse on the vertical and horizontal center lines of the graticule (see Figure 5-9).
10. Move the P6201 FET probe tip to pin 15 of U448.
11. Verify that the pulse geometry of the trigger input signal at pin 15 is at least 2.7 ns high and at least 2.7 ns low.
12. Verify that the setup time is ≤1.1 ns and hold time is ≤0.6 ns as shown in Figure 5-9.

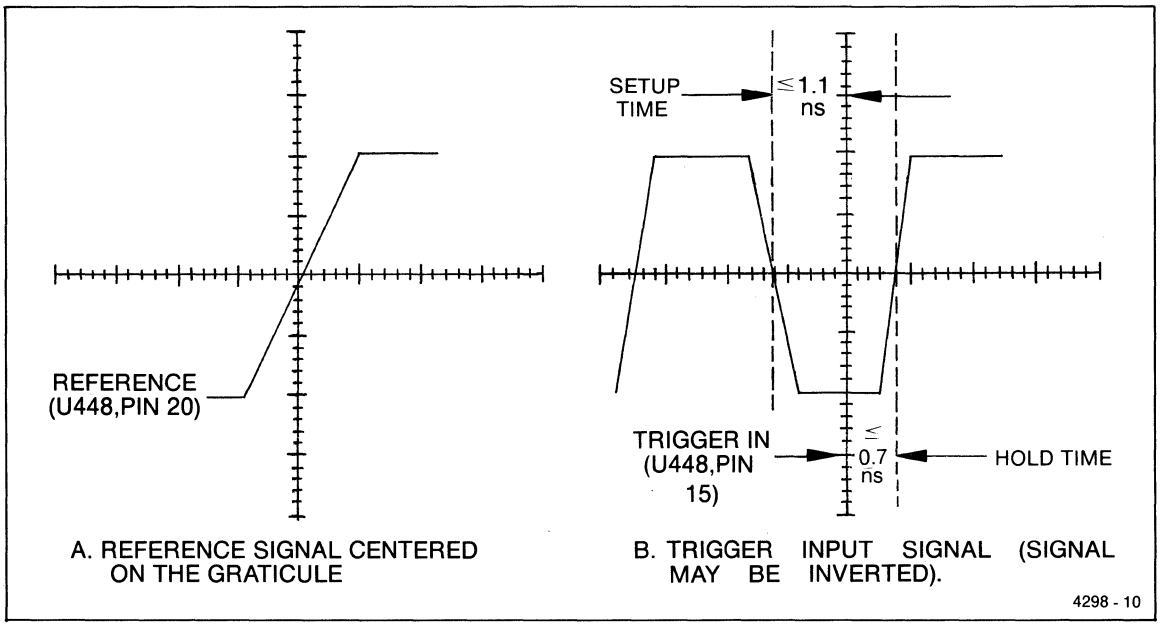


Figure 5-9. 91A04A high-speed clock setup and hold times.

(16) 91AE04A to 91A04A High-Speed Word Recognizer Timing

The following steps verify timing of the word recognizer circuits in any 91AE04A expander modules installed.

CAUTION

Do not install or remove any instrument modules in the DAS mainframe with the power on. Doing so can damage the module.

1. Power down the DAS.
2. Place the 91AE04A to be tested and the 91A04A master module on module extenders so that the short clock and word recognizer cables can be used.
3. Power up the DAS and perform the *Module Deskewing* procedure located in the *Operating Instructions* section of this addendum.

4. Connect channels 0 and 1 on the 91A04A P6453 probe to data channels 0 and 1 on the test fixture, connect channels 0 and 1 on the 91AE04A P6453 probe to data channels 2 and 3 on the test fixture, and connect the unused probe channels to the deskew connectors on the probe.
5. Enter the DAS Trigger Specification menu and select:
   - falling-edge triggering in the 91A04 External Trigger sub-menu, and
   - XX11 XX11 (binary) as the trigger word
6. Set up the oscilloscope as follows:
   a. Set the sensitivity at 200 mV/div.
   b. Set the sweep rate at 500 ps/div.
   c. Connect the P6201 FET probe tip to 100 K threshold at TP533, and connect the probe ground to the ground (G) test point next to U435.
   d. Trigger on the the external trigger output of the pulse generator.
   e. Position the trace at the graticule center line (reference).
7. Move the oscilloscope probe tip to pin 20 of U448 on the 91A04A master module, and connect the probe ground to TP449 (ground test point).
8. Press START ACQUISITION.
9. Carefully center the rising edge of the clock pulse on the center vertical and horizontals lines of the graticule (see Figure 5-9).
10. Move the P6201 FET probe tip to pin 15 of U448 on the 91A04A master module.
11. Verify that the pulse geometry of the trigger input signal at pin 15 is at least 2.3 ns high and at least 2.3 ns low.
12. Verify that the setup time is $\leq$1.1 ns and hold time is $\leq$0.6 ns as shown in Figure 5-9
13. Repeat this procedure (16) for each 91AE04A in the system. This completes the performance check of the 91A04A and 91AE04A system. The test setup may now be dismantled. Turn off the DAS mainframe before removing any modules in order to prevent damage to the modules or the mainframe.

6453 DATA ACQUISITION PROBE PERFORMANCE CHECK

Perform the *P6453 Data Acquisition Probe Function Check* that appears in the *Functional Check* subsection of this *Verification and Adjustments* section.

Section 6

MAINTENANCE: GENERAL INFORMATION

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and at the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

MAINTENANCE PRECAUTIONS

The maintenance procedures for 91A04A Series modules, and the P6453 probe, are similar to the procedures for any other DAS module or probe.

NOTE

Refer to the DAS 9100 Series Service Manual *for general maintenance procedures and precautions. Only new or changed maintenance information is included in this addendum.*

INSTALLING AND REMOVING INSTRUMENT MODULES

The procedure for installing or removing 91A04A Series modules in a DAS mainframe is nearly identical to that of any other instrument module. For additional information on module installation or removal, see the *Operating Instructions* section of this addendum.

CAUTION

The 91A04A and 91AE04A modules are extremely fragile. Be very careful when removing or installing these modules. Be especially careful not to press or flex the modules when they are extended for maintenance.

INSTALLATION SLOT RESTRICTIONS

Because of current drains on the +5 V Power Supplies, the following constraints apply to slot assignments in the DAS:

- If the 91A04A (or 91A04) shares its +5 V Power Supply with a DAS card, it can only be a 91AE24, a 91A08, or a 91P32.
- All 91AE04A expander modules must be installed in adjacent bus slots. A 91A04A master module is installed either adjacent to the first expander module, or with an empty slot between the master and expander.
- Expander modules will operate only with a 91A04A or 91A04 master module installed in the DAS.
- Neither a master nor an expander module should ever be installed in slot 1 of the DAS. Also, where possible, avoid installing a master or expander module in slot 6.

Refer also to *Module Installation* in the *Operating Instructions* section of this addendum.

PREVENTIVE AND CORRECTIVE MAINTENANCE

Preventive maintenance procedures for 91A04A Series modules and the P6453 probe are the same as the preventive maintenance procedures for the other parts of a DAS system. Refer to the *DAS 9100 Series Service Manual* for further information.

CLEANING 91A04A AND 91AE04A MODULES

When cleaning 91A04A and 91AE04A modules after they have been soldered, perform the following steps:

CAUTION

Do not brush the module while rinsing with isopropyl alcohol. Brushing causes the solder residue to adhere to the board where it remains after the alcohol evaporates. This can degrade operation with high-speed signals.

1. Flush the module repeatedly with isopropyl alcohol (do not brush).
2. Wait 60 seconds after flushing, then blow-dry the board with low-velocity air.
3. Heat the module for 60 seconds in a compartment or oven using circulating air at +51° C to +65° C (+125° F to +150° F).

REPAIRING A 91A04A SERIES MODULE

Replacing the Probe Connector Bracket

If the probe connector bracket becomes broken or otherwise damaged, use the following procedure to replace it:

1. Remove the probe connector from the bracket by loosening the two connector locking screws and lifting the connector clear of the bracket (see Figure 6-1).
2. Wrap the connector with plastic or similar material to prevent metal filings from falling into the connector pins.
3. Position the circuit board so that loose metal particles will not fall among the circuit components on the board while you are drilling out the rivets.

CAUTION

Drilling off rivet flanges on the side of the board opposite the bracket can cause damage to the board. Drill only on the bracket end of the rivets.

4. Use a 0.25-inch drill to drill the flanges off the rivets. Drill only on the bracket side of the board.
5. Lift the bracket from the board and press the old rivets out through the back of the board.
6. Carefully clean the module in accordance with the *Cleaning the 91A04A and 91AE04A Modules* instructions provided earlier in this section.
7. Inspect the board carefully with a magnifying glass to ensure no metal particles are present.
8. Position the new bracket on the board and secure it with new rivets. Refer to the *Mechanical Parts List* in this addendum for part numbers of the bracket and rivets.
9. Reinstall the connector on the bracket and tighten the two locking screws (see Figure 6-1).

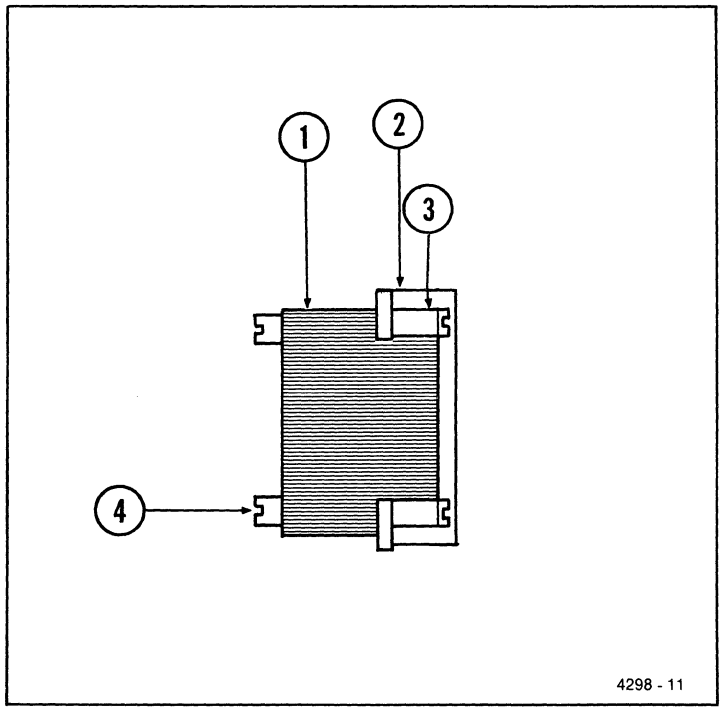


Figure 6-1. Removing the probe connector from its mounting bracket. The numbers in the following legend correspond to the numbers in the diagram.

(1) Probe Connector
(2) Probe Connector Bracket
(3) Spacers (2 ea)
(4) Locking Screws (2 ea)

Replacing J600

If J600 of a 91A04A Series module requires replacement, the entire connector assembly, including all of the connected coaxial cables, must be replaced.

91A04A Master Module. Perform the *J600 Replacement and Calibration* procedure in the *Verification and Adjustment* section of this addendum.

NOTE

If any component in the clock path or data path up to the login registers is replaced on a 91A04A master module, the J600 clock line must be checked and, if necessary, recalibrated.

91AE04A. Replace J600 on the expander module as follows:

NOTE

Be sure to note the exact positions of the coaxial cables relative to the board and to the connector pins when unsoldering the coaxial cables.

CAUTION

Do not remove or install a module in the DAS mainframe with the power on. Doing so can damage the module.

1. Power down the DAS and remove the 91AE04A from the mainframe.
2. Unsolder the coaxial lines and remove the old J600 connector housing from the bracket as shown in Figure 6-1.
3. Install the new J600 connector in the probe bracket.
4. Cut off the clock line of the new connector flush with the rear edge of the connector housing.
5. Cut the data lines on the new connector to the same length as the corresponding lines on the old connector.
6. Solder the new data lines to the appropriate terminals on the board.
7. Set the jumpers on the module extender for slots 1 - 6, and install the extender in the mainframe.
8. Install the 91AE04A on the extender and power up the DAS.
9. Verify that the probe deskews in accordance with the *Verifying Deskew Operation* procedure which appears in the *Verification and Adjustment* section of this addendum.

Extending the Modules

CAUTION

If two or more 91A04A Series modules are on extenders in the same mainframe, hot air may build up between the boards and damage one or both of the modules.

To avoid destroying these modules, place a folded piece of heavy paper or cardboard between the two extender boards in such a way that air from the mainframe fan is forced into the space between the modules. See Figure 6-2.

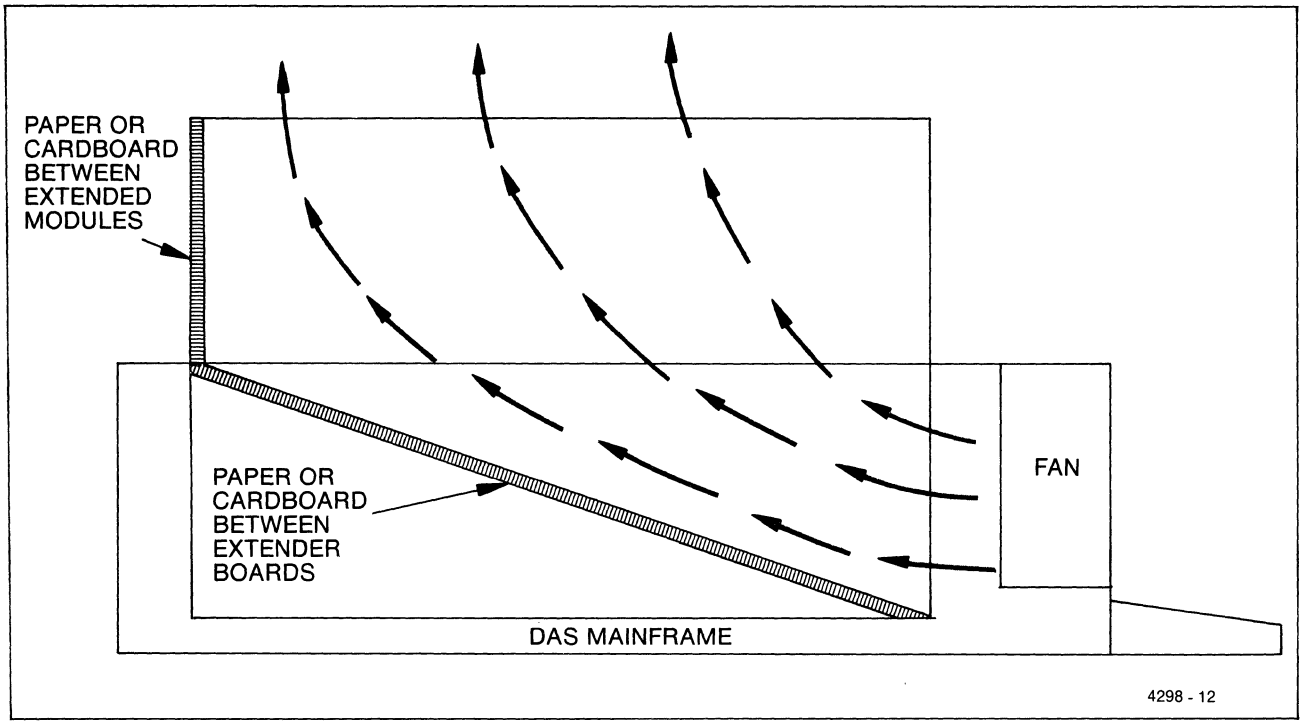


Figure 6-2. How to safely extend two 91A04A Series modules.

Connecting Jumper Cables for Extended Modules

The short 3.2 inch clock and word recognition coaxial cables provided with the 91A04A/91AE04A modules are designed for normal operation. They are not long enough to reach the connectors on an extended module. The DAS Service Maintenance Kit contains two coaxial jumper cables (p/n 175-7322-00) of sufficient length to reach from an in-slot module to an extended module. Prepare the modules as follows:

CAUTION

Do not remove or install instrument modules or sub-assemblies in a DAS mainframe with the mainframe power on. Doing so can damage the module or sub-assembly.

1. Power down the DAS.
2. Remove the DAS top cover and instrument-module cover in accordance with the *Maintenance: General Information* section of the *DAS 9100 Series Service Manual.*
3. Install the Main Extender Board in the appropriate slot to accomodate the module under test. Refer to the *Maintenance: General Information* of the *DAS 9100 Series Service Manual* for Main Extender Board installation instructions.
4. Install the module under test on the extender.

5. Connect the clock and word recognition signals using the long coaxial jumper cables from the DAS Service Maintenance Kit in place of the short jumper cables used in normal operation. Connections are as follows:
   a. Connect a clock cable from 91A04A J131 to J138 on the first 91AE04A.
   b. Connect a clock cable from 91A04A J135 to J138 on the second 91AE04A (if a second 91AE04A is installed).
   c. Connect a clock cable from 91A04A J138 to J138 on the third 91AE04A (if a third 91AE04A is installed).
   d. Connect a word recognizer cable from J141 on the first 91AE04A to J141 on the 91A04A.
   e. Connect a word recognizer cable from J141 on the second 91AE04A (if installed) to J143 on the 91A04A.
   f. Connect a word recognizer cable from J141 on the third 91AE04A (if installed) to J145 on the 91A04A.
6. Connect test equipment as required for the tests you are going to make.
7. Power up the DAS.

NOTE

If the system does not function correctly at high speeds with only one module extended, it may be necessary to extend both the master and the expander module and use the standard clock and word-recognizer cables. Refer back to Figure 6-2 *and the* Extending the Modules *procedure for instructions and precautions on dual-module extension.*

Air Core Inductors

Both the master and the expander modules use a number of unprotected air core inductors wound on the leads of resistors soldered in the board. If any of these inductors is shorted out or deformed, the module may not meet high-speed specifications. These inductors are identified by Note 1 on the schematics. The inductors are dipped in lacquer to minimize shorting or deformation.

REPAIRING P6453 DATA ACQUISITION PROBES

An assembly which consists of the P6543 Hybrid Pod is part numbered and available (refer to the *Mechanical Parts List* in this addendum). This includes the pre-tested hybrid, the hybrid's shield, two brass connectors, and the two housing halves. It should be used as the replacement part whenever one of the probe's hybrids fail.

CAUTION

The following precautions should be observed during hybrid replacement to prevent damage to the hybrid:

- Perform the replacement in a static-free environment.
- Use only 3% silver solder to ensure a good connection, and use a grounded-tip soldering iron with as low a wattage rating as possible (about 15 W for the center conductor and 25 W for the shield) to prevent separation of the laminations.
- When soldering the braided cable to the ground plate tab, heat-sink it with a scissors clamp. This prevents the center conductor's insulation from melting and causing short circuits. Also use this heat sink when removing the faulty assembly from the cable.
- Do not allow braid or solder to touch the hybrid edge.
- When soldering the center conductor, dress it flush with the hybrid. This allows adequate clearance when putting the housing halves back on.
- Do not cut and shorten the center conductor if at all possible.
- Before replacing the housing halves, make sure that the heatshrink extends far enough to be enclosed by the housing halves. This helps to provide strain relief.

After the hybrid has been replaced, check your work by performing the *Module Deskewing* procedure in the *Operating Instructions* section of this addendum. The display should indicate that the probe deskewed between steps 2 and 8 in the channel which was repaired.

REPACKAGING INFORMATION

All DAS 9100 Series products are shipped in specially designed transportation packaging. If you need to ship a product, use its original packaging. If the original packaging is no longer fit for use, contact your nearest Tektronix Field Office and obtain new DAS packaging.

If you need to ship any part of your 91A04A Series system to a Tektronix Service Center, always include all components of the system: both your master and slave modules, and their P6453 probes and gripper-tipped leads.

When you ship a product to a Tektronix Service Center, be sure to attach an identifying tag to the product (inside the packaging). On this tag include: your name, the name of your company, the name and serial number of the enclosed product, a detailed description of all failure indications, and a description of the service requested.

Section 7
MAINTENANCE: TROUBLESHOOTING

INTRODUCTION

HOW TO USE THIS SECTION

This section contains information on troubleshooting the 91A04A and 91AE04A Data Acquisition modules. Note the following conventions:

- Most troubleshooting procedures are based on the DAS self-diagnostic routines.
- Internal diagnostic routines of the DAS are integrated with the detailed theory of operation.
- Subsections correspond to the diagnostic structure of the DAS. The user will access the Diagnostics menu of the DAS as the first step in the troubleshooting procedures.
- Some high-speed problems are not detectable by diagnostics. Refer to the *Detecting and Isolating High-Speed Problems* discussion at the end of this section. Refer also to *Oscilloscope Techniques for High Frequency Measurements* in the *Maintenance: Reference Information* section of this addendum.

If you are not familiar with DAS diagnostic capabilities, read the description of the Diagnostics menu later in this section.

The self-diagnostics progressively test each module in the DAS. The diagnostics test as much of the module as possible. Therefore, the first function and test to fail will have isolated a small number of possible component failures.

Use the self-diagnostics as follows:

1. Run all tests in all functions by running each function separately, and make a list of how each test and function failed.
2. Look for a failure in the earliest test in the earliest function which would also cause subsequent tests and functions to fail. Use the color-coded schematics in the *Diagrams* section of this addendum, and the troubleshooting information in this section to isolate the component.

Detailed descriptions of the 91A04A and 91AE04A diagnostic tests are given in this section under the appropriate diagnostic-function heading. Use the *Table of Contents* at the beginning of this addendum to locate the appropriate descriptions and troubleshooting information.

TROUBLESHOOTING PRECAUTIONS

Internal Instrument Access

WARNING

Electric shock hazards inside the DAS mainframe may be exposed when protective covers are removed.

CAUTION

Do not remove or replace any instrument module or sub-assembly in the DAS mainframe with the mainframe power on. Doing so can cause damage to the module or sub-assembly.

Soldering

Most of the components in the modules are soldered in place. If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

Static Discharge Damage

CAUTION

All devices in the instrument are susceptible to damage by static discharge. Perform all maintenance in a static-free environment and ground yourself to prevent static discharge through components.

Most of the devices in the DAS are static-sensitive and may be damaged by improper handling. See Table 7-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Table 7-1
RELATIVE SUSCEPTIBILITY OF SEMICONDUCTORS TO STATIC DISCHARGE DAMAGE

Semiconductor Class	Danger Voltage
MOS or CMOS	100 - 500 V
ECL	200 - 500 V
Schottky signal diodes	250 V
Schottky TTL	500 V
High-frequency bipolar transistors	400 - 600 V
JFETs	600 - 800 V
Linear microcircuits	400 - 1000 V
Low-power Schottky TTL	1200 V

TROUBLESHOOTING EQUIPMENT

Table 7-2 lists the test equipment recommended for troubleshooting the 91A04A and 91AE04A modules and the P6453 probe. Unless otherwise specified, equivalent test instruments may be substituted for the recommended items.

Table 7-2
EQUIPMENT NEEDED FOR TROUBLESHOOTING

Qty	Function	Recommended Type
1	logic analyzer mainframe	DAS 9100 Series (no substitute)
1	data acquisition probe	Tektronix P6453 with leads, TTL-type gripper tips, and grabber tips (no subsitutute)
1	maintenance kit	DAS 9100 Series Service Maintenance Kit (no substitute)
1	digital multimeter (DMM) with 0.05% accuracy	Tektronix DM501A
1	pulse generator, 250 MHz with rise and fall times ≤1 ns	Tektronix PG502
1	sinewave generator, ≥300 MHz with leveled output	Tektronix SG504
1	two-channel oscilloscope with ≥400 MHz bandwidth and ≤2.5 pF input capacitance installed	Tektronix 7904 mainframe with a 7A19 vertical amplifier, a 7B10 timebase, and two P6201 FET X10 probes
1	350 MHz frequency counter, ECL-compatible for time measurements of 14.0 ns ±0.1 ns	Tektronix DC510

Table 7-2 (cont.)
EQUIPMENT NEEDED FOR TROUBLESHOOTING

Qty	Function	Recommended Type
1	high-speed acquisition test fixture	p/n 067-1139-00 (no substitute)
1	+5 V power supply	Tektronix PS503A
2	cables with banana connectors	p/n 012-0031-00

TROUBLESHOOTING AIDS

Color-Coded Schematics

As an additional troubleshooting aid, schematics for the 91A04A and 91AE04A modules show the signal flow of the self-diagnostics in color. For information on how to use the color coding on the schematics, refer to the introduction to the *Diagrams* section in your *DAS 9100 Series Service Manual* and to the introduction to the *Diagrams* section of this addendum.

The Diagnostics Menu

The DAS diagnostics present their information in two ways: the power-up display and the Diagnostics menu.

The DAS self-diagnostics are only accessible when the power-up display shows that one of the modules has failed the power-up diagnostics. The power-up diagnostics are a limited number of brief functional tests that are run whenever the DAS mainframe power is turned on. These tests verify the basic functions of the DAS, but are shortened versions of the self-diagnostics

When the power-up diagnostics fail, the power-up display should be similar to Figure 7-1. To enter the Diagnostics menu after a power-up diagnostics failure, press the START SYSTEM key.

NOTE

Do not press any key other than START SYSTEM. If you do, you may leave the power-up display and lose access to the Diagnostics menu. The Diagnostics menu is accessible only when the power-up display shows a failure.

It is possible for a module in the DAS to fail in such a way that the power-up diagnostics do not detect the failure. To simulate a power-up diagnostics failure in that situation, you can perform the following sequence:

1. Select any key except SHIFT and hold it down.
2. Power up the DAS mainframe.
3. Wait until the power-up diagnostics are complete, then release the key. The DAS Controller will read a failure caused by a stuck key.

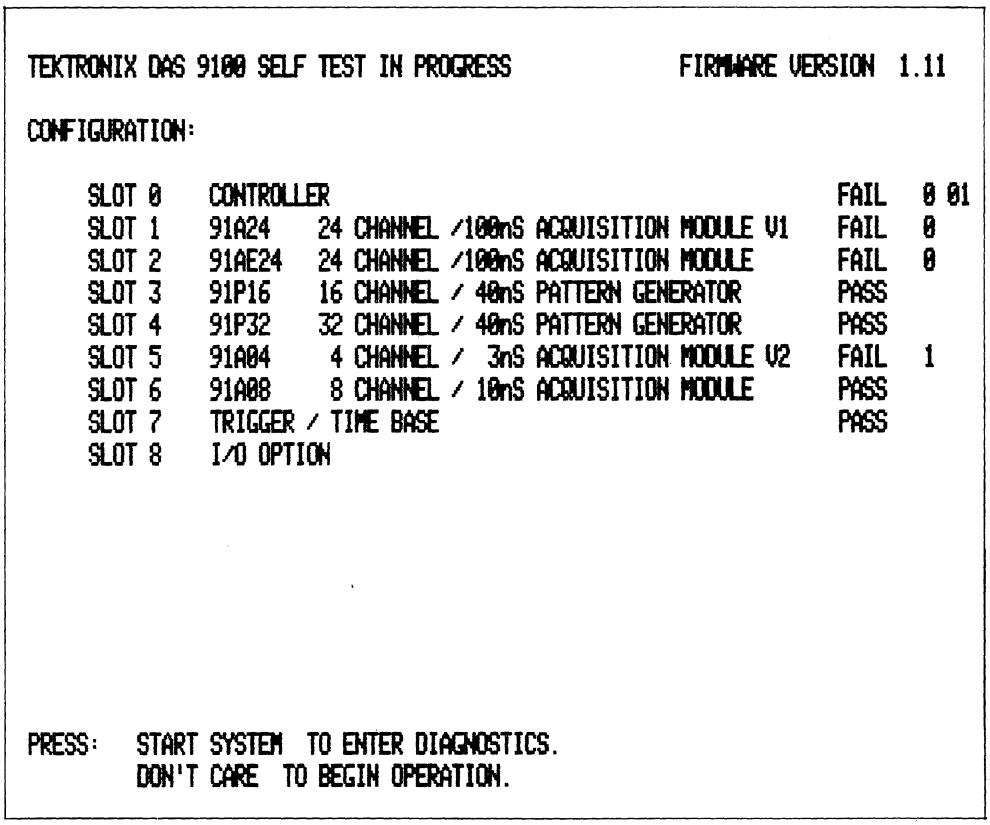


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Figure 7-1. Failure in the power-up self test.

When first entered, the Diagnostics menu should look similar to Figure 7-2. The Diagnostics menu is controlled in the same way as the standard DAS menus.

All changeable fields are shown in reverse video. You can change a field by moving the blinking screen cursor into that field. You can control cursor movement with the up, down, right, and left cursor arrows, and the NEXT key. You can change the value in the field either by using the SELECT key, or by entering a hexadecimal value using the data entry keys.

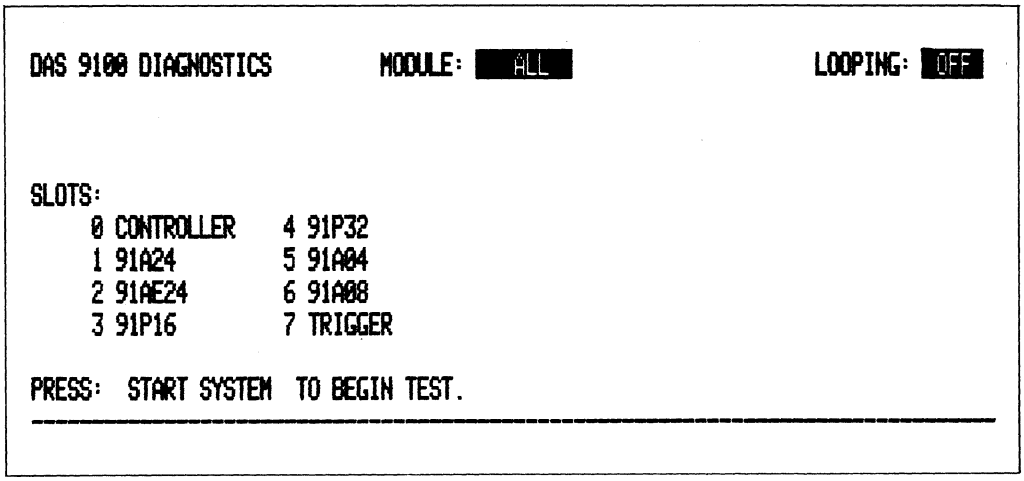

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Figure 7-2. Diagnostics menu.

After the various fields have been changed to run the desired test, the test can be started by pressing the START SYSTEM key. A test can be stopped at any time by pressing the STOP key.

The Diagnostics menu may be exited by pressing any menu selection key while no tests are running. This will display the selected menu on the screen. The diagnostics cannot be re-entered from the standard menu displays.

Diagnostics Control Summary

In summary, the diagnostics are controlled as follows:

- Force a power-up diagnostic failure by holding down a keyboard key while turning on the DAS mainframe power.
- Press the START SYSTEM key to enter the Diagnostics menu.
- Change the reverse video fields on the display to the desired values using the cursor control keys and the data entry keys.
- Press the START SYSTEM key to start the diagnostic test or function.
- You can press stop the function at any time by pressing the STOP key.
- Exit the Diagnostics menu may by pressing a menu selection key while no tests are running. The DAS must be turned off or reset to re-enter the Diagnostics menu.

Diagnostic Menu Fields

There are six user-changeable fields normally used in the Diagnostics menu. All of these fields can apply to any diagnostic test. These fields, and procedures for changing them, are described below. There may also be other changeable fields associated with individual functions. These unique fields are defined in the Diagnostics menu.

Module. This field is used to specify whether a single module or all of the modules are to be tested. Set to a value of either SINGLE or ALL using the select key.

If the field is set to ALL, all modules in the system are run through a limited number of diagnostic functions. Not all of the diagnostic functions are run when ALL is selected to keep the running time reasonable. The tests eliminated in ALL operation are those tests in which the diagnostics stop and external test equipment connections are required. In the 91A04A and 91AE04A tests, all tests in all functions are run except the last two (deskew and DAC threshold).

If the field is set to SINGLE, another field (SLOT) appears that allows the user to select the specific module (slot) to be tested. All available functions for that module can then be run.

Slot. This field appears when the MODULE field is set to SINGLE. The SLOT field is used to specify which individual module is to be tested. The individual module is specified by entering the module's bus-slot number into the field.

Mode. The MODE field appears when a bus slot number has been entered into the SLOT field. The MODE field is used to specify whether a single function or all of the module functions are to be tested.

The MODE field may be set to a value of either SINGLE or ALL by using the SELECT key.

When the cursor is moved to the MODE field, a list of module functions appears on the DAS display. If the MODE field is set to ALL, all of these module functions will be tested.

Function. The FUNCTION field appears when the MODE field is set to SINGLE. The FUNCTION field is used to specify which one of the displayed list of functions will be tested. A function is specified by entering its corresponding number into the FUNCTION field.

Looping. The LOOPING field is always present and may be set to either ON or OFF using the SELECT key. When the field is set to ON, the looping feature allows one test or a sequence of tests to be run continuously. If it is set to OFF, the selected function tests will be run once, then stopped.

NOTE

When the DAS self-diagnostics are in looping mode, the signal at TP191 on the Trigger/Time Base module (slot 7) is pulsed low at the end of each execution of any diagnostic test in the DAS. Use this test point to trigger an oscilloscope or a logic analyzer.

While the LOOPING field is set to ON and an individual function is selected, only one test in a function will loop at one time. The looping sequence starts by running test 0, the first test in a function. The SELECT key must be pressed to run the next test. All the tests in the function can be selected by pressing the SELECT key repeatedly. Pressing SELECT while the last test of a function is looping will select the first test in the function.

The looping feature (ON and OFF) reacts to failures as follows:

If looping is on, the test runs to the first failure, then loops back to the beginning of the test and again runs to the first failure. This looping continues until you press the STOP key.

If looping is off, the diagnostics run to the end of the tests, then stop. The DAS displays the status of all functions (PASS or FAIL) in the ALL mode, or the status of all tests in the selected function in the SINGLE mode. Also, if the an individual test has more than one failure code, the first one found is reported.

Running the diagnostics with looping off is a useful diagnostic aid if there are multiple failure indications. In many cases, you can use the color-coded schematics to trace all of the indicated failures back to a single area of dependency; that is, the circuitry used in the first test in the first function that failed may also be used in subsequent tests in subsequent functions that failed.

If there are multiple failures, or if a circuit fails in more than one way, the DAS displays all failures if looping is off. If looping is on, the test runs to the first failure, then loops. The diagnostic routine does not stop (nor lock up circuit conditions) at the point of failure in either looping condition.

There is no way of knowing from the failure indications how many components have failed. The diagnostics can only indicate that functions or tests pass or fail. After a component has been isolated as a fault source, make the repair, then run the diagnostics again, continuing until all tests in all functions pass.

For additional information on the looping function, refer to the *Looping* discussion in the *Maintenance: Diagnostic Test Descriptions* in your *DAS 9100 Series Service Manual.*

Display. The DISPLAY field only appears on the screen when the LOOPING field is set to ON and the MODE field is set to SINGLE. The field may be used to turn off the video screen during a looping test. This is useful when tracing circuits with an oscilloscope, because it helps to stabilize the oscilloscope's traces and shortens the loop.

The DISPLAY field may be set to ON or OFF with the SELECT key. If the field is set to ON, the video screen display is present. If the field is set to OFF, the screen is blank.

NOTE

When the DISPLAY field is turned off, the test loop being run can only be terminated by pressing the STOP key or turning off power to the DAS.

When the DISPLAY field has been set to OFF and a test is being run, the following keys have these effects:

- STOP ends the test and returns the display to normal.
- SELECT displays the results of the previous test momentarily, then turns the display off and runs the next test of the selected function.
- Any key on the keyboard (except SHIFT) turns the display on momentarily.

If an error occurs while a diagnostic test is running and the DISPLAY field is set to OFF, the LOCK-OUT and REMOTE indicators on the keyboard will be lit.

ORGANIZATION OF FUNCTION AND SUBTEST DESCRIPTIONS

Information on diagnostic functions and subtests is organized as follows:

- A listing of quick-reference diagnostic function descriptions is given for the 91A04A and 91AE04A.
- Each diagnostic function and its subtests are described in detail. Troubleshooting information is included.

Table 7-3 lists diagnostic function descriptions for the 91A04A and 91AE04A. Refer to the *Table of Contents* at the front of this addendum for the location of each function description.

Table 7-3
DIAGNOSTIC FUNCTION DESCRIPTIONS

91A04A	91AE04A	Circuit Tested
Function 0	Function 0	REG (registers)
Function 1	Function 1	MEM ADDR (memory address register)
Function 2	----N/A---	DEL CNTR (delay counter)
Function 3	----N/A---	DIF CNTR (difference counter)
Function 4	Function 2	ACQ MEM (acquisition memory)
Function 5	----N/A---	CLK ARRAY (clock array memory)
Function 6	Function 3	HIGH RES (high resolution)
Function 7	Function 4	WRD REC (word recognizer)
Function 8	Function 5	DESKEW EX (deskew register exerciser)
Function 9	Function 6	DAC THRSH (DAC threshold exerciser)

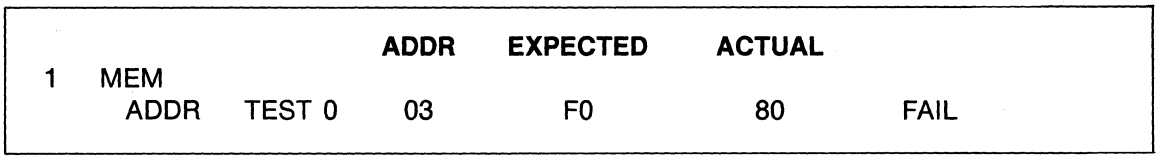
Each of the functions listed in Table 7-3 contains one or more subtests. Each function subsection provides details of function and subtest operation. There is an overview of the theory of the circuitry exercised by the function and a brief description of the diagnostic routine within the function. This specifies how data is loaded and read back. There is also a description of the first subtest (TEST X) within the function. This description includes:

a. TEST X troubleshooting information. This includes:

- Interpretation of the test readback display on the DAS. Refer to Figure 7-3 for an example. In Figure 7-3, 03 is the readback port, F0 is the expected hexadecimal readback value, and 80 is the actual hexadecimal readback value
- An analysis of diagnostic-detected error indications with their possible cause and recommended action.

b. Detailed description of TEST X, including:

- A diagram showing circuitry blocks of the 91A04A or 91AE04A excercised by TEST X.
- A detailed description of the subtest diagnostic routine, including initial conditions and readback ports.
- A table indicating all states of relevant ICs required to pass the test.



			ADDR	EXPECTED	ACTUAL	
1	MEM					
	ADDR	TEST 0	03	F0	80	FAIL

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Figure 7-3. Example of test readback display for a DAS diagnostic function.

NOTE

The troubleshooting portion of each test contains a discussion on Analyzing the Test Indications *wherein a typical error indication, observation, and action are presented. Only one typical error indication is discussed for each test, although each test has many possible error indications. When there are two possible error indications per pass or subtest, the discussion is concentrated on these multiple indications.*

QUICK REFERENCE FUNCTION DESCRIPTIONS

The following list briefly describes the diagnostic functions for the 91A04A and 91AE04A Data Acquisition modules. If functions are run individually, they should be run in the order listed under the module type. Only the functions for the questionable module need be run.

The tests in each function can be selected individually only when the diagnostics are in a looping mode. (Refer to the *Looping* description provided earlier in this section.)

91A04A Master Module Functions

REG (Function 0)

This function consists of tests 0-9 which verify the correct writing and reading of at least one bit of each of five control registers. See schematics 52A and 53A.

MEM ADDR (Function 1)

This test verifies the ability of the memory address registers to be loaded and clocked from the clock-phase generator by diagnostics-generated clocks. See schematics 55A and 56A.

DEL CNTR (Function 2)

These tests verify that each bit of the delay counter can be loaded with a 1 or a 0, and that STOP STORE will be set or reset accordingly. These tests load the delay counters with 1s and check for a STOP STORE, then walk a 0 through the delay counters to verify that the low state of each bit inhibits STOP STORE. See schematic 57A.

DIF CNTR (Function 3)

These tests verify that the difference counters can be cleared and clocked from the Trigger/Time Base module. See schematic 58A.

ACQ MEM (Function 4)

These tests verify operation of the eight RAMs in the acquisition memory, the stages of memory address latches, the write enable bus, the stages of data latches, the login registers, and the memory readback bus. See schematics 54A and 55A.

CLK ARRAY (Function 5)

This test verifies 91A04A clock array RAM operation and data latches by making three passes, and writing a different pattern to each location on each pass. This verifies bit-cell functionality and address independence of each location. See schematics 54A and 55A.

HIGH RES (Function 6)

This test verifies operation of the high-resolution circuitry in the login register area by writing data through the login registers to the eight RAMs at location 0 with different patterns, then reading these RAMs to ensure that all are rearranged properly by the high-resolution circuitry. See schematic 53A.

WRD REC: (Function 7)

This test verifies the word-recognizer circuitry. It checks all 16 combinations of the word recognizer and, with a walking zeros pattern, checks the individual don't-care bits. See schematics 56A and 57A.

DESKEW EX (Function 8)

This is a manual test that excercises the deskew registers. To use this function, a probe must be connected and the leads plugged into the probe deskew connectors. See schematic 53A.

DAC THRSH (Function 9)

This is a manual test that excercises the threshold DAC by setting the DAC to different values using the SELECT key. See schematic 53A. This function is also used during adjustment to set the DAC threshold (R818).

91AE04A Expander Module Functions

REG (Function 0)

This function consists of tests 0-9 which verify the correct writing and reading of at least one bit of each of the five control registers. See schematics 60A and 61A. This function is identical to 91A04A Function 0.

MEM ADDR (Function 1)

This test verifies the ability of the memory address registers to be loaded and clocked (by the single-step clock). See schematics 63A and 64A. This function is similar to 91A04A Function 1 except the 91AE04A is clocked by the 91A04A in MAR test 4. Also, the fourth test (MAR test 3) is not run on the 91AE04A.

ACQ MEM (Function 2)

These tests verify operation of the eight RAMs in the acquisition memory, the stages of memory address latches, the write enable bus, the stages of data latches, the login registers, and the memory readback bus. See schematics 62A and 63A. This test is identical to the 91A04A master module acquisition memory function.

HIGH RES (Function 3)

This test verifies operation of the high-resolution circuitry in the login register area by writing data through the login registers to the eight RAMs of location 0 with different patterns, then reading these RAMs to ensure that all are rearranged properly by the high-resolution circuitry. See schematic 61A.

WRD REC: (Function 7)

This test verifies the word-recognizer circuitry. It checks all 16 combinations of the word recognizer and, with a walking zeros pattern, checks the individual don't-care bits. The 91AE04A word recognizer line is checked by the 91A04A master module to verify that the triggered condition is present. See schematics 64A and 65A.

DESKEW EX (Function 5)

This is a manual test that excercises the deskew registers. To use this function, probes must be connected to both the 91A04A master module and the 91AE04A expander module. The clock hybrid must be connected to the expander module's probe deskew connectors, and the data hybrids of the expander module must plugged into the master module's probe deskew connectors. See schematic 61A. This test is identical to the 91A04A deskew function except for the deskew connections.

DAC THRSH (Function 6)

This is a manual test that excersises the threshold DAC by setting the DAC to different values using the SELECT key. See schematic 61A. This function is also used during adjustment to set the DAC threshold (R818). This function is identical to the 91A04A DAC threshold function.

91A04A/91AE04A FUNCTION 0, REGISTER TESTS

CIRCUIT OVERVIEW

The control registers on schematics 52A/60A (U651, U728, U735, U738, and U745) store command information from the DAS Controller module. This stored data controls all of the high-speed circuits in the 91A04A/91AE04A modules. Refer to the table of *Control Register Functions* in the *Theory of Operation* section of this addendum for a bit-by-bit description of control register functions.

Function 0 Description

This function consists of tests 0-9 which verify the correct writing and reading of at least one bit of each of five control registers. The writing and reading of each register consists of address decoding, clocking, and specific bit recognition. See schematic 52A (91A04A) or 60A (91AE04A).

Loading The Data

The DAS controller sends an I/O write command with a particular bit pattern on the data bus to the specific address (port). (Each control register has a different I/O port number or address.) All tests of Function 0 load the BD0-BD7 data into the control registers through the TTL0-TTL7 bus in the 91A04A and 91AE04A modules.

NOTE

The Maintenance: Reference Information *section of this addendum contains an I/O map which provides hexadecimal port numbers and descriptions of all read and write ports.*

Reading The Results

All test results are read back through pod-status register U658 (read port 01_{hex}) and MOS-status register U661 (read port 02_{hex}). See schematics 51A/59A.

91A04A/91AE04A REGISTER TROUBLESHOOTING

Reading The Register Test 0-9 Error Codes

NOTE

The diagnostic routines do not completely verify the registers, but do test the functionality of address decoding, clocking, and specific bits of the registers. Refer to Troubleshooting Undiagnosed Register Functions *for further information.*

Tests of the 91A04A/91AE04A control register function provides test results like those shown in Figure 7-4. The DAS presents this display at the end of each test.

Table 7-4 is a matrix which shows, by test, the value written to each register and the value expected from each port for the value written. Port numbers and readback values in the table are hexadecimal. In Figure 7-4, 01 is the readback port (POD status buffer U658 on schematic 51A or 59A), 00 (converted from 0XXX XXXX) is the expected hexadecimal readback value, and 80 (converted from 1XXX XXXX) is the actual hexadecimal value read. (Don't cares (Xs) are masked out and displayed as 0s in the error codes.)

		Adder	Expected	Actual	
0 REG	TEST 7	01	00	80	FAIL

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Figure 7-4. 91A04A/91AE04A typical register-test display.

Table 7-4
91A04A/91AE04A FUNCTION 0 WRITE-READ MATRIX

Test	Write Port (Port No.)	Read Port Write Value	Expected (Port No.)	Read Value
0	MEM CNTL U745 (0C)	01000000	POD status U658 (01)	XXXXXX1X
1	MEM CNTL U745 (0C)	10111111	POD status U658 (01)	XXXXXX0X
2	WRT CNTL U735 (08)	00001000	POD status U658 (01)	XXXX1XXX
3	WRT CNTL U735 (08)	11110111	POD status U658 (01)	XXXX0XXX
4	TRIG CNTL U738 (0B)	00010000	MOS status U661 (02)	XXXXXX1X
5	TRIG CNTL U738 (0B)	11101111	MOS status U661 (02)	XXXXXX0X
6	WRT DATA U651 (07)	00000100	POD status U658 (01)	1XXXXXXX
7	WRT DATA U651 (07)	11111011	POD status U658 (01)	0XXXXXXX
8	HIGH RES U728 (0D)	10000000	MOS status U661 (02)	XX1XXXXX
9	HIGH RES U728 (0D)	01111111	MOS status U661 (02)	XX0XXXXX

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indications

			Addr	Expected	Actual	
0	REG	TEST 0	01	*02	*00	FAIL
1	MEM ADDR (and others)	TEST 1	04	*E0	*F0	FAIL

*Don't Cares (Xs) are masked out and displayed as 0s in the error codes.

OBSERVATIONS	ACTION
These multiple failures are related to bit 6 of memory-control latch U745 (schematic 52A or 60A). Since there are multiple failures connected with this bit, the EN MEM ACCESS(H) line is probably stuck low. (The failure in register test 0 indicates that bit 6 of U745 has a problem. The failure in the other test verifies that this bit can cause global failures.	First, check to see if U745 is operational by checking for a timely clock at pin 11. Then, ensure that pin 12 of U745 is not connected to something (grounded through a solder bridge, for example) that is holding it low.

91A04A/91AE04A REGISTER TEST DESCRIPTION

Refer to Figure 7-5, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds in Figure 7-5 identify the relevant schematics.

The five control registers tested by all of the tests in function 0 are:

MEM CNTL U745 (schematic 52A/60A)

WRT CNTL U735 (schematic 52A/60A)

TRIG CNTL U738 (schematic 52A/60A)

WRT DATA U651 (schematic 52A/60A)

HIGH RES U728 (schematic 52A/60A)

These 10 tests of function 0 are taken together because each pair of tests (0 and 1, 2 and 3, etc.) tests a different register (write port) exactly the same way. As shown in Table 7-4, a particular bit of each of the five registers is tested for a high state, then for a low state, in each pair of tests.

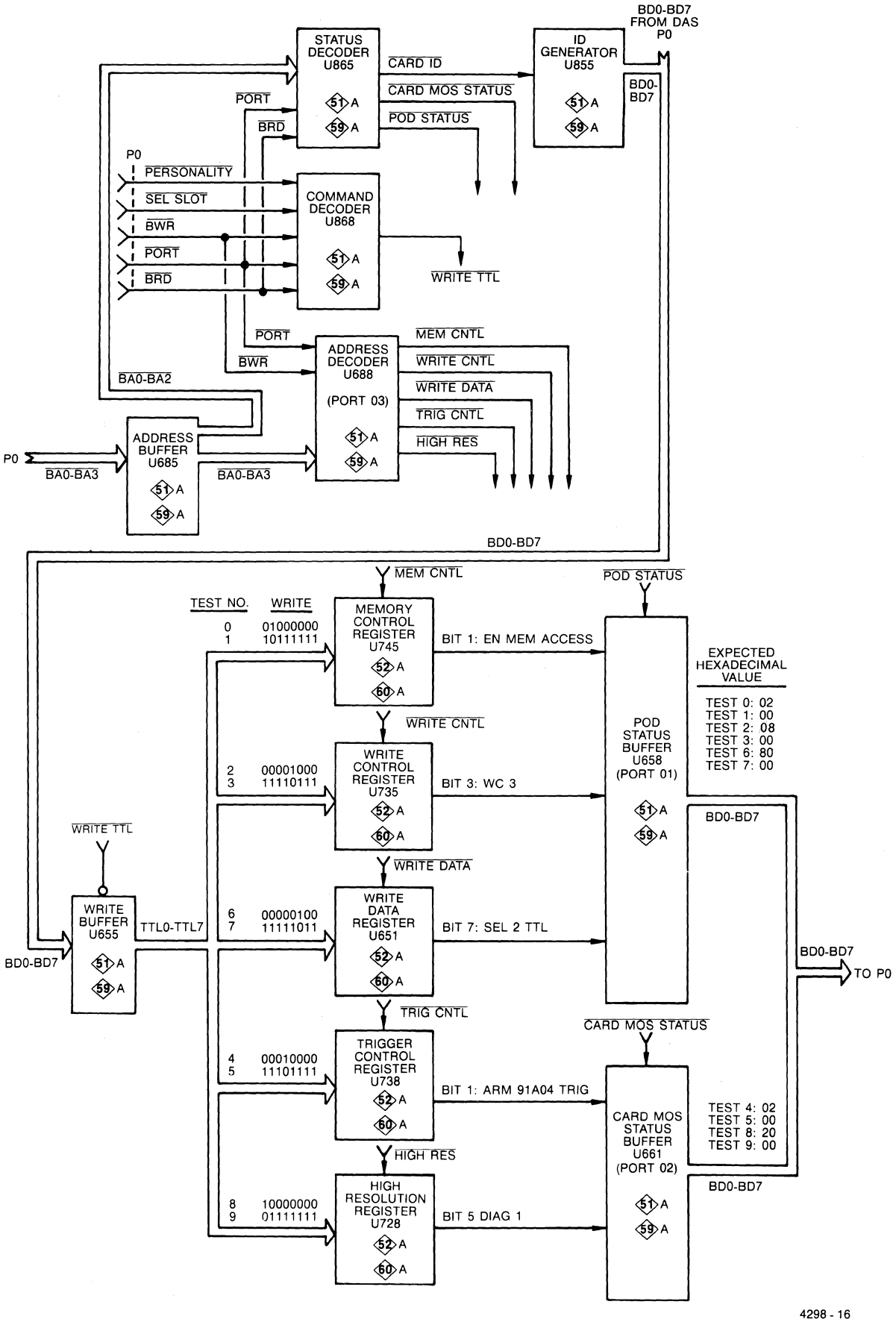

Figure 7-5. Blocks of the 91A04A/91AE04A tested by register function 0.

Circuit Conditions

Table 7-5 lists the exact state of each pin or bit component needed to pass the test. Table 7-5 is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure complete verification.

NOTE

The lowest-numbered tests in the lowest-numbered functions verify circuits that are used in the functions and tests that follow. Therefore, if multiple tests and/or functions fail, go to the **earliest** *test that failed in the* **lowest** *function to determine the cause of the failure.*

The states checked can be high, low, tristate (tri), rising edge (⌐), or falling edge (¬). The word *circuit* used in Table 7-5 includes all connections to the labeled IC, including resistors, capacitors, and transistors. Only the target circuits and the secondary circuits are included in the table (not all possibilities).

Table 7-5
CONDITIONS FOR REGISTER TESTS

Test No.	Read Write	Target Circuit	State	Secondary Circuit	State
0	write	U745, bit 6	high	U685, bits 3-0	0011
		U655, bit 6	high	U681A	high
		U688, pin 4	⌐	U681B	low
		U868, pin 12	low		
	read	U658, bit 1	high	U685, bits 3-0	X110
		U865, pin 9	low	U868, pin 4	high
				U861C, pin 8	high
				U661,U871,U855,	tri
				U671,U688,U665	tri
1	write	U745, bit 6	low	U685, bits 3-0	0011
		U655, bit 6	low	U681A	high
		U688, pin 4	⌐	U681B	low
		U868, pin 12	low		
	read	U658, bit 1	low	U685, bits 3-0	X110
		U865, pin 9	low	U868, pin 4	high
				U861C, pin 8	high
				U661,U871,U855,	tri
				U671,U688,U665	tri
2	write	U735, bit 3	high	U688, pin 8	⌐
		U655, bit 3	high	U685	0111
	read	U658, bit 3	high		
3	write	U735, bit 3	low	U688, pin 8	⌐
		U655, bit 3	low	U685	0111
	read	U658, bit 3	low		

Table 7-5 (cont.)
CONDITIONS FOR REGISTER TESTS

Test No.	Read Write	Target Circuit	State	Secondary Circuit	State
4	write	U738, bit 4 U655, bit 4	high high	U688, pin 5 U685	⌐ 0100
	read	U661, bit 1	high	U865, pin 9	low
5	write	U738, bit 4 U655, bit 4	low low	U688, pin 5 U685	⌐ 0100
	read	U661, bit 1	low	U865, pin 9	low
6	write	U651, bit 2 U655, bit 2	high high	U688, pin 9 U685	⌐ 1000
	read	U658, bit 7	high		
7	write	U651, bit 2 U655, bit 2	low low	U688, pin 9 U685,	⌐ 1000
	read	U658, bit 7	low		
8	write	U728, bit 7 U655, bit 7	high high	U688, pin 3	⌐
	read	U661, bit 5	high		
9	write	U728, bit 7 U655, bit 7	low low	U688, pin 3	⌐
	read	U661, bit 5	low		

TROUBLESHOOTING UNDIAGNOSED REGISTER FUNCTIONS

Some of the register functions are not verified in function 0. However, most of the untested functions are used (therefore verified) in the functions that follow function 0.

The key to understanding these troubleshooting procedures is to recognize their limitations. The major limitation is the fact that some items not listed can cause a test to fail. These items fall into two categories:

1. The circuits that must be inhibited to make a test pass. The major ones are covered in any initial conditions that may be set up to start a test.

2. Components that are wired to the wrong circuitry, through solder bridges for example.

91A04A/91AE04A FUNCTION 1, MEMORY ADDRESS TESTS

CIRCUIT OVERVIEW

Memory address registers (MARs) U355 and U458 (schematics 54A/62A) comprise the first stage of a four-stage address generator. The initial value of the address is loaded from the ECL0-ECL7 data bus by LD MAR(L). The MAR controls the first and second stages of the acquisition memory as well as the second stage of the address generator. Clock-phase generator U151 (schematics 56A/64A) provides clocks to the memory matrix for proper timing. The EPC0 output of the clock-phase generator is used as the master clock for the MAR. Refer to the description of *First Half Acquisition Memory, Memory Address 0 and 1* in the *Theory of Operation* section of this addendum.

FUNCTION 1 DESCRIPTION

The purpose of these five tests is to verify the clock phase generator, the memory address register, and the clock distribution system.

Test 0 verifies that clock phase generator U151 (schematics 56A/64A) can be loaded by walking a 1 through the register in nine passes, and reading back the results at the high half (four bits) of U558 and U665 (read port 03_{hex} on schematic 55A or 63A). This test also verifies the generation of diagnostic clocks through U861A and U341 (schematics 56A/64A) in the clocks and memory-control circuits.

Test 1 verifies the carry from bit 7 to bit 0 of clock phase generator U151 by loading it with 80_{hex}, then clocking it left to 01_{hex}. Readback is at U565, U568, and U665 (port 04_{hex} on schematic 55A or 63A).

Test 2 verifies that the MAR can be loaded by walking a 1 from bit 7 down to bit 0, and ends with 00_{hex} being loaded. The results are verified in each of the nine passes, and are read through buffer U665 (read port 03_{hex} on schematic 55A or 63A).

Test 3 checks MAR overflow by clearing the module [asserting CLEAR TRIG ECL(H)], loading MAR with FF_{hex}, then clocking and checking for MAR overflow by reading MAR OVERFLOW(H) through U661 (read port 02_{hex} on schematic 51A or 59A).

Test 4 tests the MAR's ability to count by loading 00_{hex}, then clocking to FF_{hex} and verifying the count after each of the 255 counts through U665 (read port 03_{hex} on schematic 55A or 63A). This test also checks the clock distribution system from U121 to U341 in the 91A04A clocks and memory control circuit (schematic 56A), and generates clocks for this function on any 91AE04A expander module present.

Loading The Data

To test the MAR, the DAS loads data onto the BD0-BD7 bus of the 91A04A/91AE04A controller interface (schematics 51A/59A). The data is buffered by U655 and U451 to provide the ECL0-ECL7 input to the MAR.

Reading The Results

Test data is read back as follows:

Test 0 is read at U558 and U665 (read port 04_{hex}). See schematics 55A/63A.

Test 1 is read back at U558 and U665 (read port 04_{hex}). See schematics 55A/63A.

Test 2 is read back at U565, U568, and U665 (read port 03_{hex}). See schematics 55A/63A.

Test 3 is read back at U661 (read port 02_{hex}). See schematics 51A/59A.

Test 4 is read back at U565, U568, and U665 (read port 03_{hex}). See schematics 55A/63A.

91A04A/91AE04A MEMORY ADDRESS TEST 0 TROUBLESHOOTING

Reading The Test 0 Error Codes

Test 0 of the 91A04A/91AE04A memory address function provides results like those shown in Figure 7-6. Table 7-6 provides a list of results expected from the readback port as the logic 1 is walked through bit 7 to bit 0 of clock phase generator U151 (schematic 56A or 64A). F0 (converted from 1111 XXXX) is the expected hexadecimal encoded value, and 80 (converted from 1000 XXXX) is the actual hexadecimal value read. (the Xs are masked out and displayed as 0s).

		Addr	Expected	Actual	
1 MEM ADDR	TEST 0	*03	F0	80	FAIL

*The DAS displays 03 as the read port, but the actual port used is 04.

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Figure 7-6. 91A04A/91AE04A memory address function, typical test 0 readback display.

Table 7-6 is a matrix showing which values are written and what the expected results are, as read from acquisition-readback buffer U665. In the event of an error, the expected value can be used to determine the value being loaded.

Also, in the event of an error when looping is enabled, if the test is stopped while running test 0, clock phase generator U151 (schematics 56A/64A) will be in the failed state.

In Table 7-6, the *Loaded Value* is loaded into clock-phase generator U151 (schematics 56A/64A) and the *Expected Value* is read from acquisition readback buffer U665 (read port 04_{hex}), (schematics 55A/63A). Port numbers and expected values in the table are hexadecimal.

Table 7-6
91A04A/91AE04A MEMORY ADDRESS FUNCTION: TEST 0 EXPECTED READBACK

Pass No.	Write Port	Loaded Value	Read Port	Expected Value
0	0C	10000000	04	FX
1	0C	01000000	04	EX
2	0C	00100000	04	DX
3	0C	00010000	04	CX
4	0C	00001000	04	BX
5	0C	00000100	04	AX
6	0C	00000010	04	9X
7	0C	00000001	04	8X
8	0C	00000000	04	0X

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			Adder	Expected	Actual	
1	MEM ADDR	TEST 0	04	B0	F0	FAIL

OBSERVATIONS

This single failure indicates that the problem is in the read-back system of clock phase generator U151 (schematic 56A or 64A). This is because a failure in U151 itself should cause multiple failures in the MAR, acquisition memory, clock array, high resolution, and word recognizer functions.

ACTION

Check pin 15 of U155 (schematic 56A or 64A) and pin 14 of U558 (schematic 55A or 63A) (see Table 7-7).

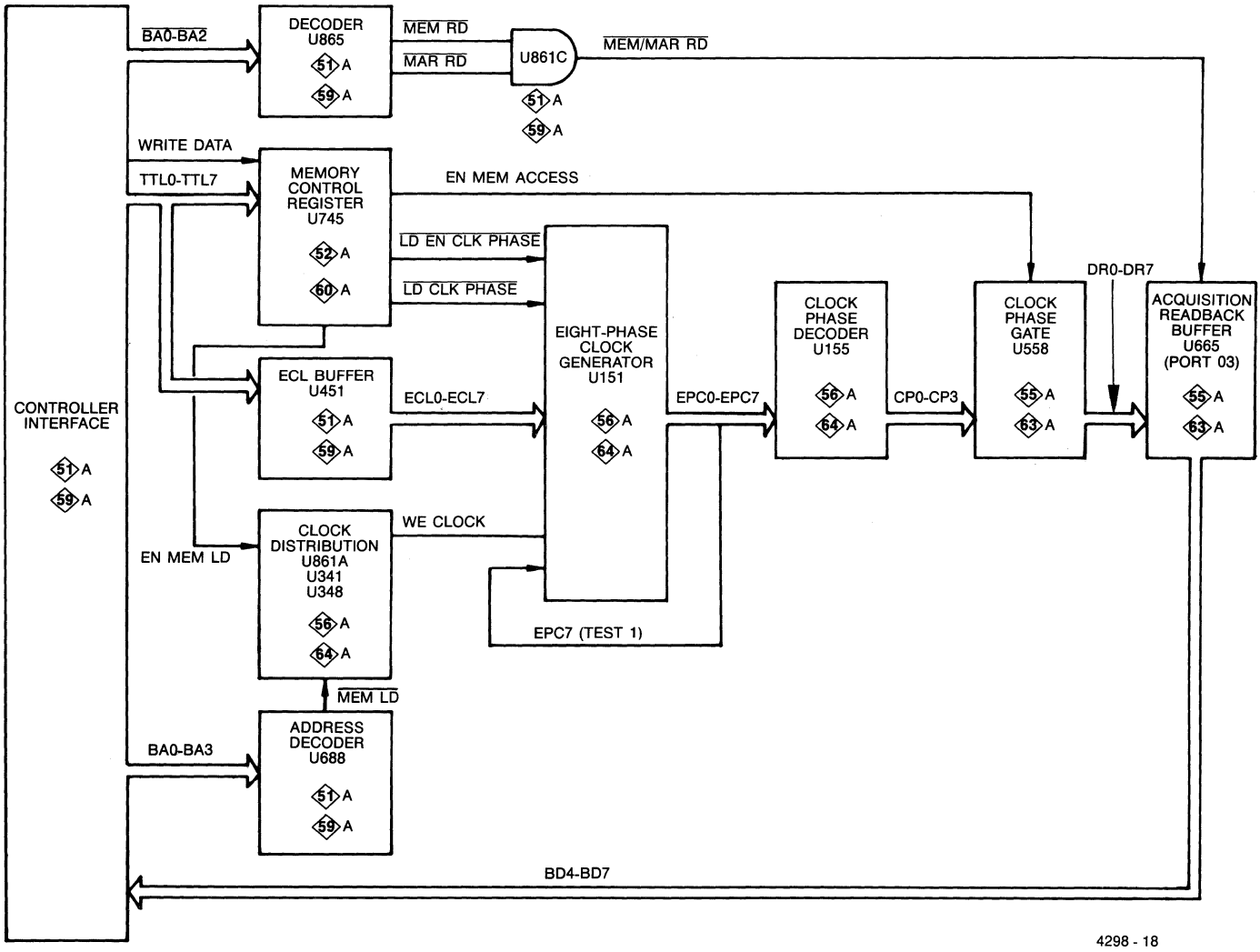

Figure 7-7. 91A04A/91AE04A blocks tested by memory address tests 0 and 1.

91A04A/91AE04A MEMORY ADDRESS TEST 0 DESCRIPTION

Refer to Figure 7-7, and to the indicated schematics, while reading the following description. The numbers enclosed in diamonds in Figure 7-7 identify the relevant schematics.

In nine passes, this test verifies that the clock phase generator bits can be loaded with highs or lows by using a walking-ones pattern (see Table 7-6).

The loading of the clock phase generator also checks the ECL0-ECL7 bus through U451, EPC0-EPC7 encoding and detection through U155 (schematic 56A or 64A), U558 and U665 (read port 04_{hex} on schematic 55A or 56A), and diagnostic single-step clock generation through U861A, and part of the clock distribution circuitry (schematics 56A/64A).

Each of the nine passes is accomplished as follows:

- Initially, bits 0 and 4 of write port $0C_{hex}$ (U745) (schematics 52A/60A) are written with zeros to enable loading of clock phase generator U151.
- Bit 7 [EN MEM LD(H)] is set to high to enable diagnostic single-step clocking and the assertion of bit 6 [EN MEM ACCESS(H)] high to enable read port 04_{hex} (U558 and U665).
- The diagnostic single-step clock is then stepped by writing to write port 04_{hex} which sends a low-going MEM LD(L) pulse through U861A, U341, and U348 (schematic 56A or 64A), clocking clock phase generator U151. This clock loads the initial test value into U151 through the ECL data bus.
- The above test value is encoded by U155 (schematic 56A or 64A) and sent to U665 (read port 04_{hex} on schematic 55A or 56A). The read of the clock phase value is ultimately accomplished by stimulating MEM/MAR RD(L) from U865 which enables buffer U665 to put the data bus on the DAS Controller.
- The above sequence is repeated eight more times (passes) to complete MAR test 0.

Circuit Conditions

Table 7-7 lists the exact state of each pin or bit component needed to pass the test. Table 7-7 is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure complete verification.

NOTE

The lowest-numbered tests in the lowest-numbered functions verify circuits that are used in the functions and tests that follow. Therefore, if multiple tests and/or functions fail, go to the earliest *test that failed in the* lowest *function to determine the cause of the failure.*

The states checked can be high, low, rising edge (⌐), or falling edge (¬). The word *circuit* used in Table 7-5 includes all connections to the labeled IC, including resistors, capacitors, and transistors. Only the target circuits and the secondary circuits are included in the table (not all possibilities).

Table 7-7
CONDITIONS FOR MAR TEST 0

Sub-Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
0	W	U451, bit 7	high	U655, bits 0,1,5	low
		U451, bit 6	low	U861, pin 3	⌐
		U151, bit 7	high	U745, bit 0	low
		U151, bit 6	low	U745, bit 4	low
		U151, pins 22,23	low	U745, bit 7	high
		U341, pin 2	¬		
		U348B	⌐		
		U688, pin 13	⌐		
	R	U665, bits 7, 6,5,4	1111	U848, pin 4	high
		U558	1111	U848, pin 2	low
		U155	1111	U745, pin 12	high
				U861, pin 8	low
				U865, pin 11 or 12	low
				U568	off
1	W	U451, bit 7	low	U655, bits 0,1,5	low
		U451, bit 6	high	U861, pin 3	⌐
		U151, bit 7	low	U745, bit 0	low
		U151, bit 6	high	U745, bit 4	low
		U151, pins 22, 23	low	U745, bit 7	high
		U341, pins 7,2	¬		
		U348B	⌐		
		U688, pin 13	⌐		
	R	U665, bit 4	low	U848, pin 4	high
		U558, pin 1	low	U848, pin 2	low
		U155, pin 3	low	U745, pin 12	high
		U558	1111	U861, pin 8	low
				U865, pin 11 or 12	low
				U568	off
2	W	U451, bit 5	high	U655, bit 5	high
		U151, bit 5	high		
	R	U655, bit 5	low		
		U558, pin 2	low		
		U155, pin 2	low		

Table 7-7 (cont.)
CONDITIONS FOR MAR TEST 0

Sub-Test No.	Read/ Write	Targe Circuit	State	Secondary Circuit	State
3	W	U451, bit 4 U151, bit 4	high high		
4	W	U451, bit 3 U151, bit 3	high high		
	R	U655, bit 6 U558, pin 14 U155, pin 15	low low low		
5	W	U451, bit 2 U151, bit 2	high high		
6	W	U451, bit 1 U151, bit 1	high high	U655, bit 1	high
	R	U665, bit 7 U558, pin 13 U155, pins 3,14	low low low		
7	W	U451, bit 0 U151, bit 0	high high	U655, bit 0	high
8	W	*all zeros			
	R	*all zeros			

*All ICs have been previously checked.

91A04A/91AE04A MEMORY ADDRESS TEST 1 TROUBLESHOOTING

Reading The Test 1 Error Codes

Test 1 of the 91A04A/91AE04A memory address function provides results like Figure 7-8. In Figure 7-8, 04 is the readback port, 80 (converted from 1000 XXXX) is the expected hexadecimal encoded value, and C0 (converted from 1100 XXXX) is the actual hexadecimal value read.

		Addr	Expected	Actual	
1 MEM ADDR	TEST 1	04	*80	C0	FAIL

*80 is the only value expected for this test.

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Figure 7-8. 91A04A/91AE04A memory address function, typical test 1 readback display.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

		Addr	Expected	Actual	
1 MEM ADDR	TEST 1	04	80	00	FAIL
2 MEM ADDR	TEST 2	03	80	FE	FAIL
3 MEM ADDR	TEST 3	03	08	00	FAIL
4 MEM ADDR	TEST 4	03	08	00	FAIL
(and others)					

OBSERVATIONS	ACTION
Memory address test 0 passes but clock (schematic 56A or 64A) phase generator U151 cannot be made to shift left.	Check U745 (schematic 52A or 64A) bit 0 for a high during the test. Also check U151 pins 4 and 22 (see Table 7-8).

91A04A/91AE04A MEMORY ADDRESS TEST 1 DESCRIPTION

Refer back to Figure 7-7, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds on Figure 7-7 are numbers of the relevant schematics.

This test verifies that clock-phase generator U151 (schematic 56A or 60A) is capable of doing a shift-left operation from bit 7 to bit 0.

MAR test 1 is similar to MAR test 0 in that the clock-phase generator is identically loaded with 80_{hex}. Instead of reading the clock-phase generator at this point, a write to port $0C_{hex}$ (U745 on schematic 52A or 60A) sets LD EN CLK PHASE(L) high, causing a shift-left mode of operation for the clock-phase generator. Then a second clock is generated by diagnostic single-step clocking. This clock causes the clock-phase generator to shift left from 80_{hex} to 01_{hex}. The result is read through port 04_{hex} (U565, U568, and U665 on schematic 55A or 63A).

Circuit Conditions

Table 7-8 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high, or shift left.

Table 7-8
CONDITIONS FOR MAR TEST 1

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U151, pins 4,22	high	U745, bit 0	high
R	U151 U151, bit 0	shift left low		

91A04A/91AE04A MEMORY ADDRESS TEST 2 TROUBLESHOOTING

Reading The Test 2 Error Codes

Test 2 of the memory address function provides results like those shown in Figure 7-9. Table 7-9 is a matrix showing the values loaded as a logic 1 is walked through the MAR, and the expected readback value for each pass. Port numbers and expected readback values in the table are in hexadecimal. In Figure 7-9, 03 is the readback port, 80 is the expected heaxadecimal readback value, and EE is the actual hexadecimal value read.

		Addr	Expected	Actual	
1 MEM ADDR	TEST 2	03	80	EE	FAIL

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Figure 7-9. 91A04A/91AE04A memory address function, typical test 2 readback display.

Table 7-9
91A04A/91AE04A MEMORY ADDRESS FUNCTION:
TEST 2 EXPECTED READBACK

Pass No.	Write Port)	Loaded Value	Read Port	Expected Value
0	0C	10000000	03	80
1	0C	01000000	03	40
2	0C	00100000	03	20
3	0C	00010000	03	10
4	0C	00001000	03	08
5	0C	00000100	03	04
6	0C	00000010	03	02
7	0C	00000001	03	01
8	0C	00000000	03	00

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			Addr	Expected	Actual	
1	MEM ADDR	TEST 2	03	08	00	FAIL
1	MEM ADDR	TEST 4	03	08	00	FAIL
4	ACQ MEM (and others)	TEST8 04	08 10	01	0A	

OBSERVATIONS	ACTION
This set of failures consistantly indicats that there is a failure of the MAR (first stage) bit 3. Also, since many tests are failing in the same place, the problem is not in the readback circuitry.	Check bit 3 of MAR counter U355 (schemaic 55A or 63A) for a stuck-low condition.

91A04A/91AE04A MEMORY ADDRESS TEST 2 DESCRIPTION

Refer to Figure 7-10, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds on Figure 7-10 identify the relevant schematics.

This test verifies that the MAR counter can be loaded with a walking-ones pattern. This test loads clock phase generator U151 and puts it into the shift-left mode as in MAR test 1. However, as the software loads bit 0 of register U745 (schemaic 52A or 60A) with a high, it resets bit 1 low to enable loading of the MAR, and resets bit 6 low to enable reading the MAR through port 03_{hex} (U565, U568, and U665 on schemaic 55A or 63A).

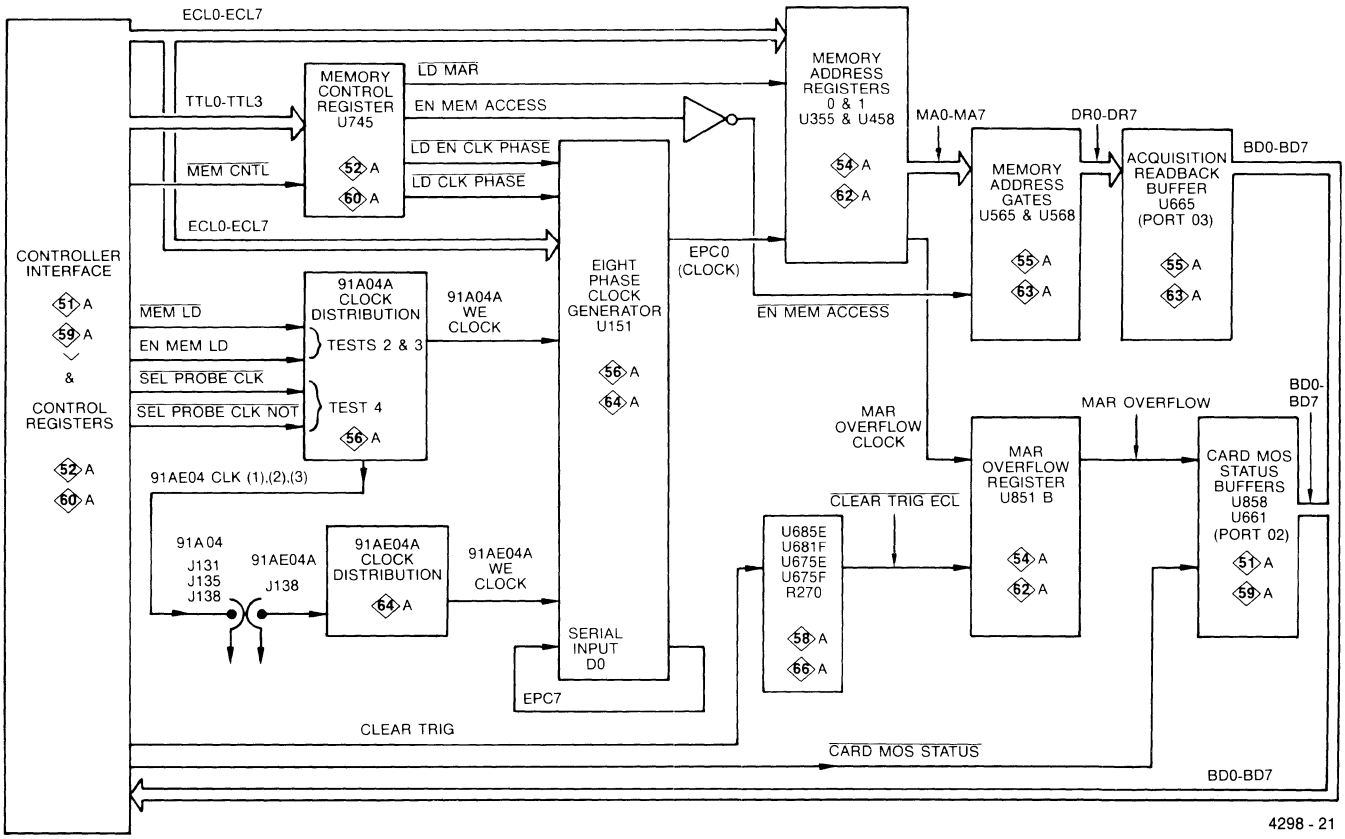

Figure 7-10. 91A04A/91AE04A blocks tested by memory address tests 2, 3, and 4.

To load the MAR with the first value, the diagnostic single-step clock makes clock-phase generator U151 (schematic 56A or 64A) shift left once, thereby causing a rising edge on the EPC0 line. This rising edge of EPC0 clocks the MAR, thereby loading the data that is currently on the ECL0-ECL7 data bus.

The MAR is then read through port 03_{hex} by asserting MEM/MAR RD(L) low to enable acquisition readback buffer U665 (schematic 55A or 63A).

The above procedure is repeated eight more times until the walking-ones pattern is completed.

Circuit Conditions

Table 7-10 lists the exact state of each pin or bit component needed to pass the test. Table 7-10 is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure complete verification.

NOTE

The lowest-numbered tests in the lowest-numbered functions verify circuits that are used in the functions and tests that follow. Therefore, if multiple tests and/or functions fail, go to the **earliest** *test that failed in the* **lowest** *function to determine the cause of the failure.*

The states checked can be high, low, rising edge (⎍), or falling edge (⎏). The word *circuit* used in Table 7-5 includes all connections to the labeled IC, including resistors, capacitors, and transistors. Only the target circuits and the secondary circuits are included in the table (not all possibilities).

Table 7-10
CONDITIONS FOR MAR TEST 2

Sub-Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
0	W	U355 U458, bit 7 U458, bit6-4	low high low	U745, bit 1 U745, bit 6	low low
	R	U565 U568	0000 1000	U848A U848B	high low
1	W	U355 U458, bit 7 U458, bit 6	low low high	U745, bit 1 U745, bit 6	low low
	R	U568	01XX	U848A U848B	high low
2	W	U458B, bit 5	high		
	R	U568	XX1X		
3	W	U458, bit 4	high		
	R	U568	XXX1		
4	W	U355, bit 3	high		
	R	U565	1XXX		
5	W	U355, bit 2	high		
	R	U565	X1XX		
6	W	U355, bit 1	high		
	R	U565	XX1X		
7	W	U355, bit 0	high		
	R	U565	XXX1		
*8					

*All values of concerned ICs have been previously tested.

91A04A/91AE04A MEMORY ADDRESS TEST 3 TROUBLESHOOTING

NOTE

This test is not performed on 91AE04A expander modules.

Reading The Test 3 Error Codes

Test 3 of the memory address function provides results like those shown in Figure 7-11. In Figure 7-11, 02 is the readback port, 10 is the expected hexadecimal readback value, and 00 is the actual hexadecimal value read. There are only two valid *EXPECTED* readback values. One is shown as 10 [MAR OVERFLOW(H)] true, and the other is 00 [MAR OVERFLOW(H)] false. This test checks the circuit response to both possibilities. All bits other than bit 4 are DON'T CAREs.

		Addr	Expected	Actual	
1 MEM ADDR	TEST 3	02	10	00	FAIL

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Figure 7-11. 91A04A/91E04A memory address function, typical test 3 readback display.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indications

		Addr	Expected	Actual	
1 MEM ADDR	TEST 3	02	10	00	FAIL

OBSERVATIONS	ACTION
Since this is the only failure and the failure is in the overflow bit, the latching of the indication in U851B (schematic 54A or 62A) and the bit 4 readback through port 02_{hex} (card MOS status buffer U661 schematic 51A or 59A) is suspect.	Check U851B for a low-to-high transition on pins 11 and 15, and check bit 4 readback through U858 and U661 (schematic 51A or 59A).

91A04A/91AE04A MEMORY ADDRESS TEST 3 DESCRIPTION

Refer back to Figure 7-10, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds on Figure 7-10 identify the relevant schematics.

MAR test 3 verifies that the MAR overflow (terminal count) functions, and that MAR overflow flip-flop U851B (schematic 54A or 62A) holds the first memory-full indication (first overflow) for the software to read after storage.

Clock phase generator U151 (schematic 56A or 64A) is loaded with $A0_{hex}$ and the MAR is loaded with FF_{hex}. (The loading sequence is the same as for MAR test 2.) MAR overflow flip-flop U851B is then reset and released by first resetting CLEAR TRIG(H) low and then high at bit 4 of U738(port OB_{hex}. Bit 4 at Port 02_{hex} (U661 on schematic 51A or 59A) is read to ensure that MAR overflow is reset low. If it is not, the test stops here and the error message is displayed.

Clock phase generator U151 is set up to shift left and the MAR is set to the count mode. The single-step clock is used to produce an EPC0 rising edge which clocks the MAR to count from FF_{hex} to 00_{hex}. This transition also produces a rising edge at the terminal count of U458 (schematic 54A or 62A) which is latched into overflow flip-flop U851B. Finally, bit 4 at port 02_{hex} (U661 on schematic 51A or 59A) is read to ensure that the MAR overflow is now set.

Circuit Conditions

Table 7-11 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high, low, rising edge (⌐), or falling edge (¬).

Table 7-11
CONDITIONS FOR MAR TEST 3 - 91A04A ONLY

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U851B	low then high	U738, bit 7	low then high
	U355, pin 4	⌐	U675E, F	low then high
	U458, pin 4	⌐	U681, pin 8	low then high
			U685E	low then high
R	U858, pins 9,14	low then high	U661, bit 4	low then high

91A04A/91AE04A MEMORY ADDRESS TEST 4 TROUBLESHOOTING

Reading The Test 4 Error Codes

Test 4 of the 91A04A/91AE04A memory address function provides results like those shown in Figure 7-12. In Figure 7-12, 03 is the readback port, 00 is the expected hexadecimal coded value that indicates the address the MAR should be pointing at, and EF is the actual hexadecimal value read.

		Addr	Expected	Actual	
1 MEM ADDR	TEST 4	03	00	EF	FAIL

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Figure 7-12. 91A04A/91AE04A memory address function, typical test 4 readback display.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			Addr	Expected	Actual	
1	MEM ADDR	TEST 4	03	01	00	FAIL

(Also, the module and the P6453 probe will not deskew properly.)

OBSERVATIONS	ACTION
Since these are the only two symptoms known, it is assumed that the problem is in the clock distribution circuitry between U115 and U341 (schematic 56A).	Check U435C to see if it is in the low condition to pass clocks through U245. Also, check jumpers J245 and W433 to see if they are installed in the correct positions (schematic 56A).

91A04A/91AE04A MEMORY ADDRESS TEST 4 DESCRIPTION

Refer back to Figure 7-10, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds on Figure 7-10 identify the relevant schematics.

This test verifies that the MAR counts correctly through all possible combinations from 00_{hex} to FF_{hex}. It also verifies the clock distribution system from clock-polarity selector U121 to clock gate U341 where it is again common with the diagnostic single-step clock.
MAR test 4 is initialized as follows:

1. 00_{hex} is written to port 06_{hex} LD DELAY 1 (L) to U588 and U591 or schematic 57A. This loads 00_{hex} into the upper section of the delay counter for a very long count, thereby ensuring that no stop-acquisition occurs during this test.

2. START ACQ(H) is sent from the Trigger/Time Base module to the start-up circuit.

3. CLEAR TRIG(H) is asserted, then released as in MAR test 3 to set start-up flip-flop U435 (schematic 56A) and clear all triggers.

4. DAC U811 (port 01_{hex} on schematic 53A or 61A) is loaded with FF_{hex} to set the threshold at +6.35 V so that the probe will not interfere with the test.

The test initially consists of setting up the clock-phase generator and the MAR the same as in MAR test 3, except that the MAR is started at 00_{hex}. At this point, the testing starts by alternating 1s and 0s at bits 4 and 5 of U731 (write port 02_{hex} on schematic 52A or 60A). Each set of 16 writes causes eight clock pulses through the clock distribution system (U121 to U151 on schematic 56A and part of 64A). This circulates the clock-phase generator once to increment the MAR on the rising edge of EPC0.

Since it takes three clocks to change the state of U435C and enable U245 (schematic 56A), the following events occur:

1. After the first 16 toggles of polarity selector U121, the MAR is still at 00_{hex}.

2. After the next 16 toggles, the MAR is at 01_{hex}.

3. After the next 16 toggles, the MAR is at 02_{hex}.

After each 16 toggles, the MAR is read through port 03_{hex} (U565, U568, and U665 on schematic 55A or 63A). This process is repeated 255 times to test the MAR from 00_{hex} to FF_{hex} (00 to 07_{hex} during power-up diagnostics).

NOTE

In power-up diagnostics, this test is shortened to seven passes instead of 256.

When running this test on 91AE04A expander modules, the MAR in the expander is being tested, but the clock originates in the 91A04A master module.

Circuit Conditions

Table 7-12 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high, low, rising edge (⌐‾), falling edge (‾⌐), or analog signal (voltage).

Table 7-12
CONDITIONS FOR MAR TEST 4 - 91A04A ONLY

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U355	low then high	U545, pins 11	low
	U458	low then high	U731, pins 6,9	low then high
	U245, pin 2	⌐	U228, pin 6	low
	U125, pin 2	‾⌐	U235, pins 7,2	low
	U125, pin 7	⌐	U545, 15	low
	U121, pins 2,7	⌐	U731, pins 19,5,16	high
	U435, pins 14,11,7	low	U591, pin 12	high
			U811	voltage
			U641, pin 12	low
			U818	voltage
			U115	no transitions
R	U565	low then high		
	U568	low then high		

Table 7-13
CONDITIONS FOR MAR TEST 4 - 91AE04A ONLY

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U458	low then high	Q436	voltage
	U355	low then high	*U545, pin 11	low
	*U245, pin 7		*U731, pins 6,9	low then high
	or *U241,		*U228, pin 6	low
	*pin 7 or 2	⌐	*U235, pins 7,2	low
	*U125, pin 2	¬	*U545, 15	low
	*U125, pin 7	⌐	*U731, pins	high
	*U121, pins		19,5,16	
	2,7	⌐	*U591, pin 12	high
	*U435, pins		*U811	voltage
	14,11,7	low	*U641, pin 12	low
			*U818	voltage
			*U115	no trans-
				itions
			*J245	continuity

*These ICs are located on the 91A04A master module, and are used in developing the clocks for the 91AE04A expander modules. J245 must be installed on pins 2 and 3 to deliver clocks to the expanders.

91A04A FUNCTION 2, DELAY COUNTER

NOTE

This function applies only to the 91A04A master module. The 91AE04A expander module has no delay counter function.

CIRCUIT OVERVIEW

The delay counter is programmed by the controller interface, and determines the number of clock cycles (up to 32,767) the STOP-STORE(H) signal is delayed after the trigger is satisfied. The counter is loaded with the 1s complement of the delay count, then counts up to all 1s to stop acquisition. Refer also to the discussions of the *Lower 1/4 Delay Counter* and the *Upper 3/4 Delay Counter* in the *Theory of Operation* section of this addendum. This information appears in the *Trigger* circuit discussion that refers to schematic 57A.

FUNCTION 2 DESCRIPTION

Refer to Figure 7-13 while reading the following description. Figure 7-13 is a functional block diagram that applies to all tests in the delay counter function.

Test 0 loads the delay counter with all 1s, then reads the MOS-status buffer (port 02_{hex} on schematic 51A) to verify that the STOP-STORE(H) bit is asserted high to indicate that all bits of the delay counter are high.

Test 1 loads the delay counters with all 1s, then walks a 0 from ECL3 down to ECL0 to verify that STOP-STORE(H) and TTL DELAY DONE(L) are inhibited by each low bit input through write ports $0C_{hex}$ [MEM CNTL (L) on schematic 52A] and 05_{hex} [LD DELAY 0 (L) on schematic 57A] to the lower 1/4 delay counter. The read port is the same as in step 0.

Test 2 loads the delay counters with all 1s, then walks a 0 from TTL5 down to TTL0 through write port 06_{hex} LD DELAY 1 (L) on schematic 57A to verify that STOP-STORE(H) is inhibited (low) and TTL DELAY DONE(L) is asserted (high) by each low bit input to the DELAY 1(L) portion of the upper 3/4 delay counter. The read port is the same as in step 0.

Test 3 loads the delay counters with all 1s, then walks a 0 from TTL7 to TTL4 through write port 03 [LD DELAY 2 (L) on schematic 57A] to verify that each low bit input to the DELAY 2(L) portion of the upper 3/4 delay counter sets STOP STORE(H) low and asserts TTL DELAY DONE(L). The read port is the same as in step 0.

Loading The Data

The lower 1/4 delay counter is loaded through the controller interface by ECL0-ECL3 writing through DELAY 0(L) (port 05_{hex}). The upper 3/4 delay counter is loaded by TTL0-TTL7 writing through DELAY 1(L) (port 06) and DELAY 2(L) (port 03_{hex}). Also, an enable signal [EN DEL CNTR LD(H)] must be asserted high through write port $0C_{hex}$ before the lower 1/4 delay counter can be loaded.

Reading The Results

There is no readback for the delay counter. Therefore, the output of the delay counter enables, or inhibits, the STOP-STORE(H) signal which is read through the MOS-status buffer (port 02_{hex}) as bit 0 on the BD0-BD7 data bus. The TTL DELAY DONE(L) signal (bit 6) is read through the same port. See schematic 51A.

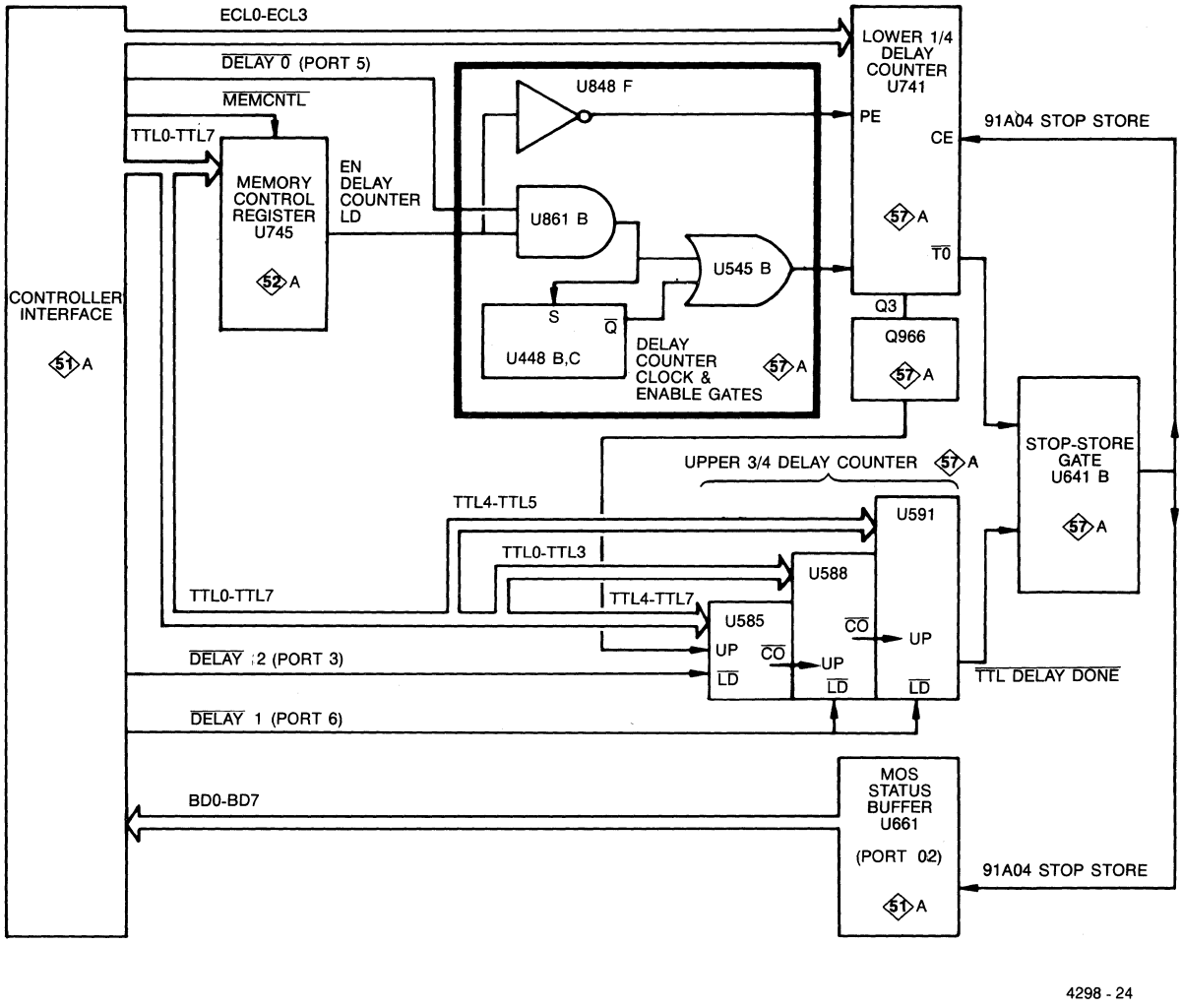

Figure 7-13. 91A04A blocks tested by delay counter tests 0 through 3.

91A04A DELAY COUNTER TEST 0 TROUBLESHOOTING

Reading The Test 0 Error Codes

Test 0 of the 91A04A delay counter function provides results like those shown in Figure 7-14. In Figure 7-14, 02 is the readback port, 01 (XXXX XXX1) is the expected hexadecimal value, and 00 (converted from XXXX XXX0) is the actual hexadecimal value read.

			ADDR	EXPECTED	ACTUAL	
2	DEL CNTR	TEST 0	02	01	00	FAIL

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Figure 7-14. 91A04A delay counter function, typical test 0 display. There are only two expected results: 01 [STOP STORE(H) asserted] and 00 [STOP STORE(H) inhibited].

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
2	DELAY CNTR	TEST 0	02	01	00	FAIL
2	DELAY CNTR	TEST 1	02	00	00	PASS

OBSERVATIONS

The key to troubleshooting this problem is the combining of a FAIL indication with a PASS indication. Because delay test 0 looks at one bit to determine correct operation of a 15-bit counter, suspicion should be directed at the pass-fail bit first. The codes of the FAIL and PASS indicate that trhe 91A04 STOP STORE(H) signal never goes to the high state.

ACTION

Check the 91A04 STOP STORE(H) signal to see if it can be forced high. Check to see if bit 0 of port 02_{hex} (U661 on schematic 51A) is reading the signal polarity correctly.

91A04A DELAY COUNTER TEST 0 DESCRIPTION

Refer back to Figure 7-13, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-13 identify the relevant schematics.

This test verifies that all parts of the delay counter can be loaded with ones, causing a terminal count. This is detected by reading the 91A04 STOP STORE bit (bit 0) through the MOS-status buffer (port 02_{hex}).

To load these 1s into lower 1/4 delay counter U741, the EN DELAY COUNTER LD(H) signal is set high by writing a 1 to bit 5 of port $0C_{hex}$ (U745, pin 6). This enables U741 to be to be loaded and clocked by the diagnostic single-step clock. Loading the counter is accomplished by loading $0F_{hex}$ through the ECL0-ECL3 bus at port 05_{hex} (DELAY 0(L) to U741. The DELAY 0(L) signal from U688 clocks the data into U741 through U545B and U861B.

The upper 3/4 delay counter (U585, U588, and U591) does not require an enable. Therefore, a $0F_{hex}$ write to DELAY 2(L) (port 03_{hex}) loads U585 with all ones and an FF_{hex} write to DELAY 1(L) (port 06_{hex}) loads U588 and U591 with all 1s.

Since all bits of all counters are at terminal count, all inputs to stop-store gate U641B are low. This sets 91A04 STOP STORE(H) high. The STOP STORE(H) bit (bit 0) is then read through MOS status buffer U661 (port 02_{hex}).

Circuit Conditions

Table 7-13 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high, low, or rising edge (⌐).

NOTE

This test and test 1 combine to fully check delay counter support circuits.

Table 7-14
CONDITIONS FOR DELAY COUNTER TEST 0

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U585, pin 12	low	U745, pin 6	high
	U588, pin 12	low	U545B	⌐
	U591, pin 12	low	U861B	⌐
	U741, pin 4	low	U688, pins 11,10,14	⌐
	U741, pin 14	high	U848F	low
R	U858, pin 13	high	U641B	high
			U545C	high
			U661, bit 0	high

91A04A DELAY COUNTER TEST 1 TROUBLESHOOTING

Reading The Test 1 Error Codes

Test 1 of the delay counter function provides results like those shown in Figure 7-15. Table 7-15 is a matrix showing the values loaded as the 0 is walked through the delay counters. In Figure 7-15, 02 is the readback port, 00 (converted from X0XX XXX0) is the expected hexadecimal readback value, and 01 is the actual hexadecimal value read.

			ADDR	EXPECTED	ACTUAL	
2	DEL CNTR	TEST 1	02	00	01	FAIL

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Figure 7-15. 91A04A delay counter function, typical test 1 display. The only possible expected value is 00.

Table 7-15
LOAD SEQUENCE FOR DELAY COUNTER TEST 1

Pass No.	Write Port (Hexadecimal)	Loaded Value	Read Port (Hexadacimal)	Expected Read Value Bit 0 Bit 6
1	05	11110111	02	0 0
2	05	11111011	02	0 0
3	05	11111101	02	0 0
4	05	11111110	02	0 0

Analyzing The Test Indications

Refer back to the analysis provided for the delay counter test 0.

91A04A DELAY COUNTER TEST 1 DESCRIPTION

Refer back to Figure 7-13, and to the indicated schematics, while reading this description. The numbers enclosed in diamonds on Figure 7-13 identify the relevant schematics.

This test loads the upper 3/4 delay counter (U585, U588, and U591) with 1's, then walks a low through each bit of lower 1/4 delay counter U741 to make sure each bit of the lower 1/4 delay counter disables the 91A04 STOP STORE(H) signal.

First the lower 1/4 delay counter is loaded with one of the patterns in Table 7-15 as described in the *91A04A Delay Counter Test 0 Description.* Next, the rest of the counter is loaded with all 1's, with U585, then U588, then U591, loaded as in test 0. The 91A04 STOP STORE(H) signal (bit 0) and the TTL DELAY DONE(H) signal (bit 6) are then tested for a low by reading them back through MOS status buffer U661 (port 02_{hex}). The above sequence is repeated four times to check all bits of lower 1/4 delay counter U741.

Circuit Conditions

Table 7-16 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure proper verification. States checked can be high, low, or rising edge.

NOTE

This test and test 0 combine to fully check delay-counter support circuits.

Table 7-16
CONDITIONS FOR DELAY COUNTER TEST 1

Sub-Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
1	W	U741, pin 4	high	U545B	⌐
		U741, bit 3	low	U861B	⌐
				U688, pin 11	⌐
				U848F	low
				U745, bit 5	high
	R	U858, pin 13	low	U661, bits 0,6	low
				U641B	low
				U545C	low
2	W	U741, bit 2	low		
3	W	U741, bit 1	low		
4	W	U741, bit 0	low		

91A04A DELAY COUNTER TEST 2 TROUBLESHOOTING

Reading The Test 2 Error Codes

Test 2 of the delay counter function provides results like those shown in Figure 7-16. Table 7-17 is a matrix showing the values loaded as a 0 is walked through the delay counters. In Figure 7-16, 02 is the readback port, 40 (converted from X1XX XXX0) is the expectad hexadecimal readback value, and 01 (converted from X0XX XXX1) is the actual hexadecimal value read.

			ADDR	EXPECTED	ACTUAL	
2	DEL CNTR	TEST 2	02	40	01	FAIL

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Figure 7-16. 91A04A delay counter function, typical test 2 display. The only possible expected result is 40.

Table 7-17
LOAD SEQUENCE FOR DELAY COUNTER TEST 2

Pass No.	Write Port (Hexadecimal)	Loaded Value	Read Port (HexadecimaL)	Expected Read Value Bit 0 Bit 6
1	06	11011111	02	0 1
2	06	11101111	02	0 1
3	06	11110111	02	0 1
4	06	11111011	02	0 1
5	06	11111101	02	0 1
6	06	11111110	02	0 1

Analyzing The Test Indictions

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
2	DELAY CNTR	TEST 2	02	40	01	FAIL
2	DELAY CNTR	TEST 3	02	40	01	FAIL

(Tests 0 and 1 passed.)

OBSERVATIONS

Combining these two tests indicates that whatever is affecting the first test makes the following test fail in the same manner. Also, since tests 0 and 1 passed, the 91A04 STOP STORE(H) signal is functioning properly.

ACTION

Check U585, U588, and U591 (schematic 57A) circuitry for TTL DELAY DONE(L) signal stuck low.

91A04A DELAY COUNTER TEST 2 DESCRIPTION

Refer back to Figure 7-13, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-13 identify the relevant schematics.

This test verifies operation of the U588 and U591 portions of the upper 3/4 delay counter by loading the rest of the counter with all ones as in tests 0 and 1. This test then walks a low through the most significant bits of the delay counter (U588 and U591) and checks the 91A04 STOP STORE(H) signal for a low and TTL DELAY DONE(H) for a high. This test is accomplished in six passes (refer back to Table 7-17).

Circuit Conditions

Table 7-18 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high or low.

Table 7-18
CONDITIONS FOR DELAY COUNTER TEST 2

Sub-Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
1	W	U591, bit 1 U591, pin 12	low high	U688, pin 10 U661, bit 6	low high
2	W	U591, bit 0	low		
3	W	U588, bit 3 U588, pin 12	low high		
4	W	U588, bit 2	low		
5	W	U588, bit 1	low		
6	W	U588, bit 0	low		

91A04 DELAY COUNTER TEST 3 TROUBLESHOOTING

Reading The Test 3 Error Codes

Test 3 of the delay counter function provides results like those shown in Figure 7-17. The load sequence for the test is shown in Table 7-19. In Figure 7-17, 02 is the readback port, 40 (converted from X1XX XXX0) is the expected hexadecimal value, and 00 (converted from X0XX XXX0) is the actual hexadecimal value read.

			ADDR	EXPECTED	ACTUAL	
2	DEL CNTR	TEST 3	02	40	00	FAIL

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Figure 7-17. 91A04A delay counter function, typical test 3 display. The only possible expected result is 40.

Table 7-19
LOAD SEQUENCE FOR DELAY COUNTER TEST 3

Pass No.	Write Port (Hexadecimal)	Loaded Value	Read Port (Hexadecimal)	Expected Read Value Bit 0 Bit 6
1	05	01111111	02	0 1
2	05	10111111	02	0 1
3	05	11011111	02	0 1
4	05	11101111	02	0 1

Analyzing The Test Indications

Refer back to the delay counter test 2 analysis.

91A04A DELAY COUNTER TEST 3 DESCRIPTION

Refer back to Figure 7-13, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-13 identify the relevant schematics.

This test verifies the operation of the U585 portion of the upper 3/4 delay counter by loading all ones as in tests 0 and 1, then walking a low through the DELAY 2(L) portion of the counter (U585). This test is accomplished in four passes (refer back to Table 7-19). The readback is is the same as in test 2.

Circuit Conditions

Table 7-20 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be high or low.

Table 7-20
CONDITIONS FOR DELAY COUNTER TEST 3

Sub-Test No.	Read/Write	Target Circuit	State
1	W	U585, pin 12 U585, bit 3	high low
2	W	U585, bit 2	low
3	W	U585, bit 1	low
4	W	U585, bit 0	low

91A04A FUNCTION 3 DIFFERENCE COUNTER

NOTE

This function applies only to the 91A04A master module. The 91AE04A expander module has no difference counter.

CIRCUIT OVERVIEW

The difference counter counts the number (up to 500) of slow-card clock cycles between the slow-card trigger and the 91A04A trigger. This information is then made accessible to the 91A04A controller interface. The DAS Controller uses this information to ensure correct timing alignment when both the 91A04A and slow-card data are displayed in the ARMS mode. Refer also to the discussion of the *Difference Counter and Power Supplies* in the *Theory of Operation* section of this addendum, and to schematic 58A.

FUNCTION 3 DESCRIPTION

Tests 0 and 1 verify that the difference counter can be cleared (to all 0s) by writing to the trigger control register (write port $0B_{hex}$ U738 on schematic 52A) to assert CLEAR TRIG (H). In test 0, bits 0-7 are read from the DIFF 0 buffer (read port 05_{hex}, U671 on schematic 58). In test 1, bits 8-15 are read from the DIFF 1 buffer (read port 06_{hex}).

Test 2 verifies that the difference counter can be clocked by writing to the high-resolution register (write port $0D_{hex}$ U728 on schematic 52A) to enable the slow-card clock, then single-stepping the slow-card clock [91A32 INT CLK(L)] to clock the difference counter from 00 to 100_{hex}. Readback is similar to tests 0 and 1.

Loading The Difference Counter

Refer to Figure 7-18 while reading the following description:

To test the difference counter, the DAS loads data onto the TTL0-TTL7 bus of the 91A04A controller interface. This data is written to trigger-control register U738 (port $0B_{hex}$) to produce CLEAR TRIG(H), and high-resolution register U728 (Port $0D_{hex}$) to enable the slow-card single-step clock to the difference counter circuits. This procedure clears the counter and enables clocking of the counter.

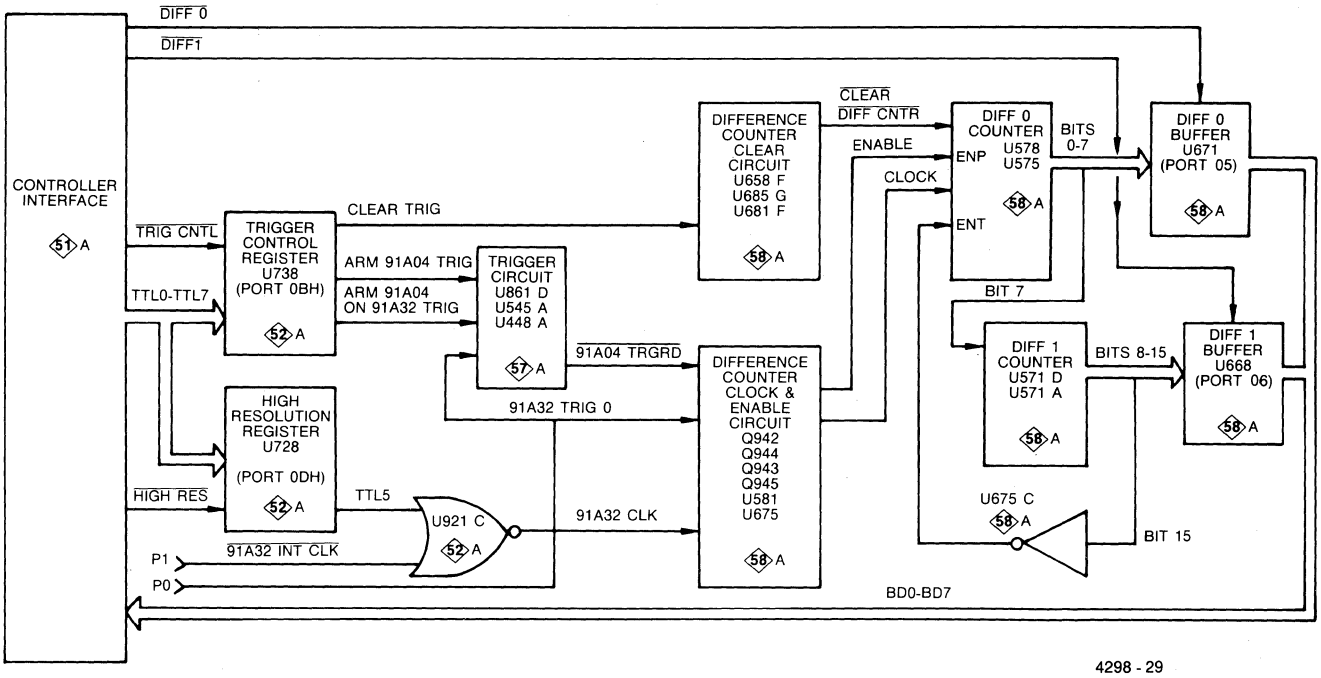

Figure 7-18. Blocks tested by difference counter tests 0, 1, and 2.

Reading The Results

The difference counter output count is buffered by U671 and U688 and placed on the BD0-BD7 data bus for readback to the DAS Controller. Readback for bits 0-7 of the difference counter is through DIFF 0 buffer U671 (port 05_{hex}). Readback for bits 8-15 is through DIFF 1 buffer U668 (port 06_{hex}).

91A04A DIFFERENCE COUNTER TESTS 0 AND 1 TROUBLESHOOTING

Reading The Tests 0 And 1 Error Codes

Tests 0 and 1 of the difference counter function provides results like those shown in Figure 7-19. In Figure 7-19, 05 is the readback port, 00 is the expected hexadecimal readback value, and 0A is the actual hexadecimal readback value. (For test 1, the readback port is 06_{hex} and the expected value is 00_{hex}.)

			ADDR	EXPECTED	ACTUAL	
3	DIF CNTR	TEST 0	05	00	0A	FAIL

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Figure 7-19. 91A04A difference counter function, typical tests 0 and 1 display. The only possible expected result is 00.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
3	DIF CNTR	TEST 0	05	00	FE	FAIL
3	DIF CNTR	TEST 1	06	00	FF	FAIL
(and others)						

OBSERVATIONS

The fact that both tests failed, and that there are no zeros in the data read at port 05_{hex}, indicates that the problem is common to both the upper and lower sections of the difference counter.

ACTION

Since other tests also failed, first check the CLEAR TRIG(H) circuitry (U685E, U581F, and pin 15 of U738).

91A04A DIFFERENCE COUNTER TESTS 0 AND 1 DESCRIPTION

Refer back to Figure 7-18, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-18 identify the relevant schematics.

These tests verify that the difference counters can be cleared. Test 0 verifies the DIFF-0 counter U575 and U578, and test 1 verifies DIFF-1 counter U571A and U571B.

The difference counter is cleared by asserting CLEAR TRIG(H) from pin 15 of U738. (CLEAR TRIG(H) was verified in MAR test 3.) This signal is applied to the clear inputs of all elements of the difference counter (U578, U575, and U571) to reset all inputs low.

The lower part of the counter (difference 0) is read through DIFF-0 buffer U671 (port 05_{hex}) and the upper part of the counter (difference 1) is read through DIFF-1 buffer U688 (port 06_{hex}).

Circuit Conditions

Table 7-21 lists the exact state of each component needed to pass test 0 and 1. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. All states checked should be low.

Table 7-21
CONDITIONS FOR DIFFERENCE COUNTER TESTS 0 AND 1

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U578	low	U675D	low
	U575	low		
	U571B	low		
	U571A	low		
R	U671	low	U865, pins 13,14	low
	U688	low		

91A04A DIFFERENCE COUNTER TEST 2 TROUBLESHOOTING

Reading The Test 2 Error Codes

Test 2 of the difference counter function provides results like those shown in Figure 7-20. In Figure 7-20, 06 is the readback port, 01 is the expected hexadecimal value, and 00 is the actual hexadecimal value read.

			ADDR	EXPECTED	ACTUAL	
3	DIF CNTR	TEST 2	06	01	00	FAIL

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Figure 7-20. 91A04A difference counter function, typical test 2 display. There are four possible expected codes: 55_{hex} at address 05, AA_{hex} at address 05, and 00_{hex} or 01_{hex} at address 06.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
3	DIFF CNTR	TEST 2	05	AA	2A	FAIL

OBSERVATIONS	ACTION
The error code indicates that U575 is not operating correctly relative to its MSB. Also, the problem could be in the bit 7 readback through U671 (read port 05_{hex}). See schematic 58A.	Check pin 6 of U575 for a stuck-low condition.

91A04A DIFFERENCE COUNTER TEST 2 DESCRIPTION

Refer back to Figure 7-18, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-18, identify the relevant schematics.

Test 2 verifies that the difference counter can be clocked from the Trigger/Time Base module after 91A32 TRIG 0(H) is asserted.

Initally, 91A32 TRIG 0(H) is asserted high. Also, on the Trigger/Time Base module, the 91A32 single-step clock [91A32 INT CLK(L)] is selected and enabled. The 91A32 INT CLK(L) is then selected by writing $D0_{hex}$ to port $0D_{hex}$ (U728). This selects the proper clock through U921C.

Next, the difference counter is cleared by asserting CLEAR TRIG(H) as in tests 0 and 1, and a large delay is added to the 91A04A delay counter (U588 and U591) to ensure 91A04 STOP STORE(H) is not asserted.

Testing is begun by asserting the 91A32 single-step clock 85 times and checking the lower part of the counter (port 05_{hex}) for a count of 55_{hex}. If 55 is not detected, an error is reported and the test stops at this point.

The 91A32 single-step clock is then stepped 85 more times and the count is checked for AA_{hex} if the count is not correct, an error is reported and the test stops.

Finally the counter is clocked 86 more times and the counter is checked for a count of 100_{hex}. As before, if an error is detected, the test stops and the error is reported.

Circuit Conditions

Table 7-22 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure proper verification. States checked can be high, low, rising edge (⌐), or falling edge (¬).

Table 7-22
CONDITIONS FOR DIFFERENCE COUNTER TEST 2

Sub-Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
0	W	U578, U575, bits 0,2,4,6	high	U728, bit 6	low
				U728, bits 7,5,4	high
		U578, pin 11	⌐	U921, pin 10	⌐
				Q943, Q945	⌐
				U581A	⌐
				U675C	high
				U581B	high
				U581C	low
				Q942, Q944	⌐
	R	U671, bits 0,2,4,6	high		
1	W	U578, U575 bits 1,3,5,7	high		
	R	U671, bits 1,3,5,7	high		
2	W	U571, pin 11	high		
		U575, pin 6	⌐		
	R	U668, bit 0	high		

91A04A FUNCTION 4/91AE04A FUNCTION 2, ACQUISITION MEMORY

Circuit Overview

The 2K x 4 acquisition memory matrix stores all high-speed acquired data for readback by the DAS Controller module. To meet the setup and hold requirements of the acquisition RAM, the memory is organized into eight recycling stages. These stages include eight levels of memory-address register and one level of staggered pipeline data latches. Also, the login registers are used for a source of data in these tests. For additional information, refer to the discussions of the *First Half Acquisition Memory* and the *Second Half Acquisition Memory* in the *Theory of Operation* section of this addendum.

FUNCTION DESCRIPTION

Tests 0-7 verify operation of the acquisition memory, memory address latches, write enable bus, staged data latches, login registers, and memory readback bus. All RAMs except the one under test are loaded with AA_{hex}. The RAM under test is loaded with 55_{hex}. This loading is accomplished by loading the complement of the desired data in the login registers and single-step clocking the data into the memory using most of the storage system.

Table 7-23 lists the loading sequence from test 0 through test 7. After writing to all eight RAMs at location 00 only, the eight RAMs are read for the proper contents through acquisition readback buffer U665 (port 05_{hex}).

Table 7-23
ACQUISITION MEMORY TESTS 0-7, LOAD SEQUENCE

Test No.	RAM 0	RAM 1	RAM 2	RAM 3	RAM 4	RAM 5	RAM 6	RAM 7
0	55	AA	AA	AA	AA	AA	AA	AA
1	AA	55	AA	AA	AA	AA	AA	AA
2	AA	AA	55	AA	AA	AA	AA	AA
3	AA	AA	AA	55	AA	AA	AA	AA
4	AA	AA	AA	AA	55	AA	AA	AA
5	AA	AA	AA	AA	AA	55	AA	AA
6	AA	AA	AA	AA	AA	AA	55	AA
7	AA	AA	AA	AA	AA	AA	AA	55

Test 8 verifies functionality of address independence of the acquisition memory circuit by making three passes through memory and writing a different pattern to each location (from 00_{hex} to FF_{hex}) on each of the three passes. Table 7-24 lists the patterns loaded for each of the three passes. After each pass is loaded, the results are read back through acquisition readback buffer U655 (port 04_{hex} on schematic 55A or 63A).

NOTE

Due to power-up time limitations, only the first eight locations are tested during power-up diagnostics.

Table 7-24
ACQUISITION MEMORY TEST 8 LOAD PATTERNS

Pass 1: Location	RAM 0	RAM 1	RAM 2	RAM 3	RAM 4	RAM 5	RAM 6	RAM 7
00	XA	X1	XC	XA	X1	XC	XA	X1
01	XC	XA	X1	XC	XA	X1	XC	XA
02	X1	XC	XA	X1	XC	XA	X1	XC

through 256 locations to FF_{hex}

Table 7-24 (cont.)
ACQUISITION MEMORY TEST 8 LOAD PATTERNS

Pass 2: Location	RAM 0	RAM 1	RAM 2	RAM 3	RAM 4	RAM 5	RAM 6	RAM 7
00	X1	XC	XA	X1	XC	XA	Z1	XC
01	XA	X1	XC	XA	X1	XC	XA	X1
02	XC	XA	X1	XC	XA	X1	XC	XA

through 256 locations to FF_{hex}

Pass 3: Location	RAM 0	RAM 1	RAM 2	RAM 3	RAM 4	RAM 5	RAM 6	RAM 7
00	XC	XA	X1	XC	XA	X1	XC	XA
01	X1	XC	XA	X1	XC	XA	X1	XC
02	XA	X1	XC	XA	X1	XC	XA	X1

through 256 locations to FF_{hex}

Loading The Data

The data for the test sequence is loaded as follows:

1. All 1s are written to DESK 0 (L) and DESK 1(L) (U255 and U725 on schematic 53A or 61A, ports 09_{hex} and $0A_{hex}$) to enable ECL0-ECL3 data to be applied to the data login register.

2. The MAR is loaded with FF_{hex} by the procedure used in test 2 of function 1, and will increment to 00_{hex} when writing begins.

3. The clock-phase generator is initialized to 60_{hex} and the write-enable register is initialized to DF_{hex}.

4. Write port 07_{hex} is written with zeros to select the RAMs to be written.

5. The single-step clock is used to clock data from the login register into the RAM.

Reading The Results

Each of the eight RAMs (0-7) at each location are read by writing a value with only one bit low to write-data register U651 (write port 07_{hex}). See schematics 52A/60A. For all nine tests in the acquisition memory function, readback is through data buffer U548 and acquisition readback buffer U665 (port 04_{hex} on schematic 55A or 63A).

91A04A/91AE04A ACQUSITION MEMORY TESTS 0-7 TROUBLESHOOTING

Reading The Tests 0-7 Error Codes

Tests 0-7 of the acquisition memory function provides results like those shown in Figure 7-21. In Figure 7-21, 04 is the readback port, 7 is the RAM number, 0A (converted from XXXX 1010) is the expected hexadecimal readback value, and 00 (converted from XXXX 0000) is the actual hexadecimal value read. The only possible expected values are 05_{hex} and $0A_{hex}$ (refer back to Table 7-23).

			ADDR	EXPECTED	ACTUAL	
4	ACQ MEM	TEST 4	04 7	0A	00	FAIL

Figure 7-21. 91A04A/91AE04A acquisition memory function, typical test 0-7 readback display.

ANALYZING THE TEST INDICATIONS

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR			EXPECTED	ACTUAL	
4	ACQ MEM	TEST 4	04		05	X1	FAIL	
4	ACQ MEM	TEST 8	04	0	0	5 0C	X8	FAIL
5	CLK ARRAY	TEST 0	01	28	2	CC	CC	PASS
6	HIGH RES	TEST 0	04		0C	08	FAIL	

OBSERVATIONS	ACTION
Key indications are: function 5 (CLK ARRAY) passed; any time RAM 4 or above needs a high in bit 2, there is a failure in the first try.	Check D2(L) (bit 2) on the data bus from login U628C (see Table 7-25). See schematic 53A or 61A.

91A04A/91AE04A ACQUSITION MEMORY TESTS 0-7 DESCRIPTION

Refer to Figure 7-22, and to the indicated schematics, while reading the following description. The numbers in diamonds on Figure 7-22 identify the relevant schematics.

These tests verify the operation of the login registers, staged data latches, and the acquisition memory by checking both states of data through the system with the diagnostic single-step clock. The MAR staged latches and the write enable register are also checked by loading data into the acquisition memory to simulate acquisition.

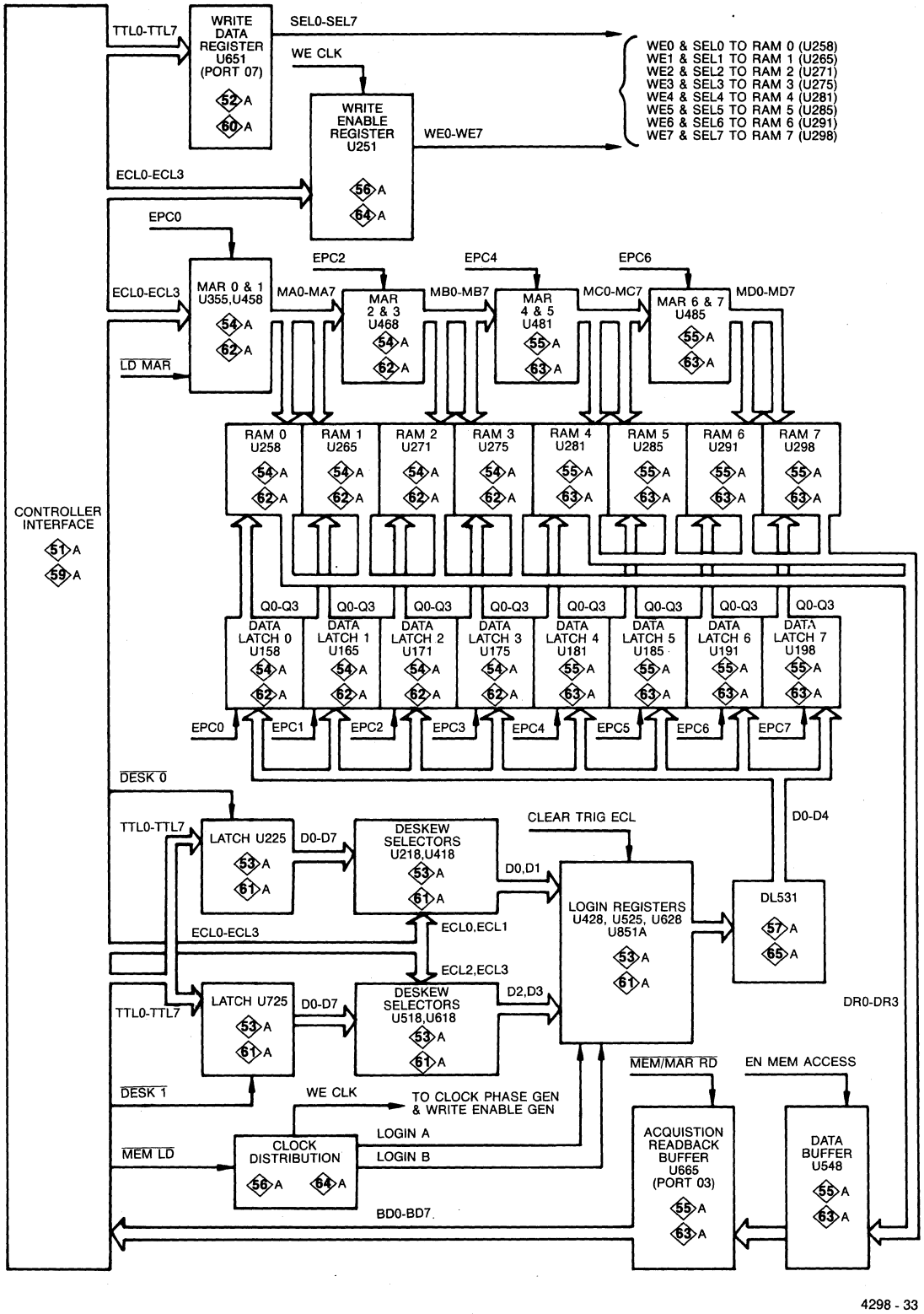

Figure 7-22. Blocks tested by acquisition memory tests 0-8.

Initial Conditions

Circuit conditions for acquisition memory tests 0-7 are set up as follows:

1. The module is set to normal resolution (high resolution inhibited) by writing $0C_{hex}$ to port $0D_{hex}$ (high-resolution register U728).

2. The deskew selectors are set to select the ECL0-ECL3 bus by writing FF_{hex} to ports 09_{hex} and $0A_{hex}$ (deskew latches U725 and U225).

3. The module is prevented from triggering by resetting ARM 91A04 TRIG(H) and ARM 91A04 ON 91A32 TRIG(H). This is done by writing 00_{hex} to port $0B_{hex}$ (trigger control register U738) and asserting CLEAR TRIG(H).

Before the start of each test, MARs 1 and 2 (U355 and U458) are loaded with FF_{hex}. Clock phase generator U151 is loaded with 60_{hex}. Using a similar procedure, write enable register U251 is loaded with DF_{hex} using bits 2 and 3 of memory control register U745. At the start of each test, all RAM select signals are reset low to enable writing by sending 00_{hex} to port 07_{hex} (write data register U651).

Test Sequence

NOTE

Correct timing for data storage can be found in the diagram for Acquisition pulse timing for 3 ns or slower acquisition *in the* Theory of Operation *section of this addendum.*

The test is conducted by writing the complement of the tested-for data state to the login registers with nine single-step clocks. The login registers invert the data and send it to the staged data latches which, on every eight clocks, present new data to the acquisition memory at location 00_{hex}. This causes seven memories to be loaded with XA_{hex} and one to be loaded with $X5_{hex}$ at location 00_{hex}. (Refer back to Table 7-23.) Write enable register U251 is then set to all 1s to turn off the write cycle.

The MAR is set to 00_{hex} and the memories are read through the lower bits (0-3) of port 04_{hex} (acquisition readback buffers U548 and U665). The memories are read one at a time by alternating select lines from write data register U651 (write port 07_{hex}).

Circuit Conditions

Table 7-25 lists the exact state of each pin or bit component needed to pass the test. Table 7-25 is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure proper verification.

NOTE

The lowest-numbered tests in the lowest-numbered functions verify circuits that are used in the functions and tests that follow. Therefore, if multiple tests and/or functions fail, go to the earliest *test that failed in the* lowest *function to determine the cause of the failure.*

The states checked can be high, low, rising edge (⌐), or falling edge (¬). The word *circuit* used in Table 7-25 includes all connections to the labeled IC, including resistors, capacitors, and transistors. Only the target circuits and the secondary circuits are included in the table (not all possibilities).

Table 7-25
CONDITIONS FOR ACQUISITION MEMORY TESTS 0-7

Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
0	W	U258	X5$_{hex}$	U728, pins 19,2	high
		U265	XA$_{hex}$	U218, pins 19,11	hi/lo
		U251, pins 5,6	hi/lo	U418, pins 19,11	hi/lo
		U158, bits 0-3	X5$_{hex}$	U225	FF$_{hex}$
		U165, bits 0-3	XA$_{hex}$	U725	FF$_{hex}$
		*U428A, C	hi/lo	U525	D0 side
		*U628A, C	hi/lo	U341, pins 6,3	hi/lo
				U651, pin 5	low
	R	U548	hi/lo	U651, pin 5	hi/lo
				U651, other pins	all high
1	W	U258	XA$_{hex}$	U728, pins 19,2	high
		U265	X5$_{hex}$	U218, pins 19,11	hi/lo
		U251, pins 5,6	hi/lo	U418, pins 19,11	hi/lo
		U158, bits 0-3	XA$_{hex}$	U225	FF$_{hex}$
		U165, bits 0-3	X5$_{hex}$	U725	FF$_{hex}$
		*U428A, C	hi/lo	U525	D0 side
		*U628A, C	hi/lo	U341, pins 6,3	hi/lo
				U651, pin 16	hi/lo
				U651, other pins	all high
	R			U651, pin 16	hi/lo
				U651, other pins	all high
2	W	U271	X5$_{hex}$	U468	low
		U275	XA$_{hex}$		
		U171, bits 0-3	X5$_{hex}$		
		U175, bits 0-3	XA$_{hex}$		
		U251, pins 7,8	hi/lo		
3	W	U271	XA$_{hex}$	U651, pin 2	low
		U275	X5$_{hex}$	U468	low

*Except pins 3 and 18 are low only.

Table 7-25 (cont.)
CONDITIONS FOR ACQUISITION MEMORY TESTS 0-7

Test No.	Read/ Write	Target Circuit	State	Secondary Circuit	State
		U171, bits 0-3	XA_{hex}		
		U175, bits 0-3	X_{hex}		
		U251, pins 7,8	hi/lo		
	R			U651, pin 2	hi/lo
4	W	U281	$X5_{hex}$	U651,pin 9	low
		U285	XA_{hex}	U481	low
		U181, bits 0-3	$X5_{hex}$		
		U185, bits 0-3	XA_{hex}		
	R			U651, pin 9	hi/lo
5	W	U281	XA_{hex}	U651, pin 6	low
		U285	$X5_{hex}$	U481	low
		U181, bits 0-3	XA_{hex}		
		U185, bits 0-3	$X5_{hex}$		
		U251, pins 11,12	hi/lo		
	R			U651, pin 6	hi/lo
6	W	U291	$X5_{hex}$	U651, pin 12	low
		U298	XA_{hex}	U485	low
		U191, bits 0-3	$X5_{hex}$		
		U198, bits 0-3	XA_{hex}		
	R			U651, pin 12	hi/lo
7	W	U291	XA_{hex}	U651, pin 15	low
		U298	$X5_{hex}$	U485	low
		U191, bits 0-3	XA_{hex}		
		U198, bits 0-3	$X5_{hex}$		
		U251, pins 13,15	hi/lo		
	R			U651, pin 15	hi/lo

91A04A/91AE04A ACQUISITION MEMORY TEST 8 TROUBLESHOOTING

Reading The Test 8 Error Codes

Test 8 of the acquisition memory function provides results like those shown in Figure 7-21. Figure 7-21 is interpreted as follows:

04 is the port which is read for the results.

7F (hexadecimal) is the location in RAM where the failure was detected.

2 is the pass number.

5 is the RAM or bank (0-7).

0 = U258	2 = U271	4 = U281	6 = U291
1 = U265	3 = U278	5 = U285	7 = U298

0A (converted from XXXX 1010) is the expected hexadecimal value (refer back to Table 7-24).
0C is the actual value read (this is not the expected value).

NOTE

The message in Figure 7-23 indicates that bank (or RAM) number 5 failed on the second pass at location $7F_{hex}$. Bank (or RAM) numbers are from 0 to 7, and locations are from 0 to FF_{hex}.

A failure on this test at location 1 or above when the incorrect actual value is one of the valid patterns (01, 0A or 0C) indicates a probable failure of one of the MARs.

A failure at or above location 1 when the incorrect actual value is not one of the three valid patterns indicates a probable failure of one of the RAMs.

			ADDR		EXPECTED	ACTUAL	
4	ACQ MEM	TEST 8	04	7F	2 5 0A	0C	FAIL

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Figure 7-23. 91A04A/91AE04A acquisition memory function, typical test 8 readback display.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR		EXPECTED	ACTUAL	
4	ACQ MEM	TEST 8	04	6F	2 5 0A	XC	FAIL

(ACQ MEM tests 0-7, the CLK ARRAY function, and the HIGH RES functions all passed.)

OBSERVATIONS	ACTION
The key to this analysis is the tests that pass, and the fact that this test failed on pass 2 at address 6F. This indicates a very narrow set of possibilities.	Check U285 (RAM 5) and associated connections (see Table 7-26). See schematic 55A or 63A.

91A04A/91AE04A ACQUISITION MEMORY TEST 8 DESCRIPTION

Refer back to Figure 7-22, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-22 identify the relevant schematics.

This test makes three passes through the entire memory while writing a different value to each location on each pass. Since each RAM stores four bits, the values used for each pass are XA_{hex}, $X1_{hex}$, and XC_{hex} (refer back to Table 7-24). These passes, which are diagnostic-controlled acquisition cycles, are read differently than standard acquisition cycles in that each location to be read is loaded directly into the MAR rather than incremented.

Initial Conditions

Before the start of each pass, initial conditions established are the same as for tests 0-7.

Test Sequence

Each pass is accomplished with 2056 single-step clocks. The 0A, 01, and 0C (hexadecimal) data is loaded into memory the same as in tests 0-7 except that all locations are written after the acquisition pass is completed.

The write-enable generator is loaded with all 1s to prevent destroying the RAM contents during readback.

The MAR and the staged MAR is loaded with 00_{hex} by single-stepping the clock seven times. This loads the MAR and the staged MAR by producing a low-to-high transition on EPC0, EPC2, ECP4, and EPC6.

Finally, using the individual select lines, the RAMs are read through port 04_{hex} (acquisition readback buffer U665) in the order listed in Table 7-24. This readback procedure is repeated 255 more times to cover each of the 256 locations.

Circuit Conditions

Table 7-26 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked should be both high and low (hi/lo) at some point during the test.

Table 7-26
CONDITIONS FOR ACQUISITION MEMORY TEST 8

Test No.	Read/ Write	Target Circuit	State
8	W	U258	hi/lo
		U265	hi/lo
		U271	hi/lo
		U275	hi/lo
		U281	hi/lo
		U285	hi/lo
		U291	hi/lo
		U298	hi/lo
		*U481	hi/lo
		*U468	hi/lo
		*U485	hi/lo

*These ICs are not fully checked.

91A04A FUNCTION 5, CLOCK ARRAY

NOTE

This function applies only to the 91A04A master module. The 91AE04A expander module has no clock-array function.

CIRCUIT OVERVIEW

The clock array memory stores the status of the slow-card clock while the 91A04A is operating. The stored information is later recovered and used to time correlate 91A04A and slow-card data. The address for clock array RAM 0-3 (U475 on schematic 54A) is provided by MARs 2 and 3, and the address for clock array RAM 4-7 (U491 on schematic 55A) is provided by MARs 6 and 7. The slow-card clock data is stored from data latches 0-7.

FUNCTION 5 DESCRIPTION

Test 0 is the only test in the clock array function. This test verifies the clock array memory by making three passes and writing a different pattern to each pass. These three passes verify bit-cell functionality and address independence of each bit.

The clock array RAM is written, starting at location 0 and ending at location 255. The proper bit value (0 or 1) for each write cycle is selected by single stepping the slow-card clock input from the DAS Trigger/Time Base module.

After each of the three passes, the clock array RAM is assembled into eight-bit bytes (two RAMs at four bits each) and checked against the expected value. If an error is detected, the test stops at that location, and an error message is displayed. The location and pass number of the failure are included with the error message.

Loading The Data

The input data is first loaded into login latch U851A and U628B (schematic 53A) by the diagnostic single-step clock (91A32 CLK) from the Trigger/Time Base module. The target RAMs are loaded from the staged data latches (schematics 54A and 55A) in a manner similar to that used in the acquisition memory function.

Reading The Results

At each pass through the RAM, each section of each RAM is enabled separately by writing a value with one bit low to write-data register U651 (write port 07_{hex}). See schematic 52A.
The outputs of the two clock array RAMs are wire ORed, and read back as the CLK ARRAY RD(H) bit through pod-status register U658 (read port 01_{hex} on schematic 51A).

91A04A CLOCK ARRAY TEST 0 TROUBLESHOOTING

Reading The Test 0 Error Codes

Test 0 of the clock array memory function provides results like those shown in Figure 7-24. Refer to Table 7-27 for expected results.

Figure 7-24 is interpreted as follows:

01 is the read port.

28 is the RAM address location of the failure.

1 is the pass upon which the error was detected.

11 is the expected value.

01 is the actual value assembled from the I/O port.

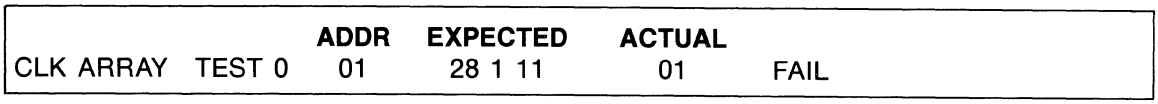

Figure 7-24. 91A04A clock array function, typical test 0 readback display. 4298 - 34

NOTE

The write port for all subtests shown in Table 7-27 is the Trigger/Time Base single-step clock

Table 7-27
CLOCK ARRAY TEST 0: LOADED AND EXPECTED VALUES
Pass 0:

Location	U475 bits 3 2 1 0	U491 bits 3 2 1 0	Write Port	Expected Hexadecimal Value	Read Port
00	1 0 1 0	1 0 1 0		AA	01
01	0 0 0 1	0 0 0 1	..	11	01
02	1 1 0 0	1 1 0 0	..	CC	01
03	1 0 1 0	1 0 1 0	..	AA	01

Pattern repeated through 256 locations

Table 7-27 (cont.)
CLOCK ARRAY TEST 0: LOADED AND EXPECTED VALUES

Pass 1:

Location	U475 bits 3 2 1 0	U491 bits 3 2 1 0	Write Port	Expected Hexadecimal Value	Read Port
00	0 0 0 1	0 0 0 1	..	11	01
01	1 1 0 0	1 1 0 0	..	CC	01
02	1 0 1 0	1 0 1 0	..	AA	01
03	0 0 0 1	0 0 0 1	..	11	01

Pattern repeated through 256 locations

Pass 2:

Location	U475 bits 3 2 1 0	U491 bits 3 2 1 0	Write Port	Expected Hexadecimal Value	Read Port
00	1 1 0 0	1 1 0 0	..	CC	01
01	1 0 1 0	1 0 1 0	..	AA	01
02	0 0 0 1	0 0 0 1	..	11	01
03	1 1 0 0	1 1 0 0	..	CC	01

Pattern repeated through 256 locations

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR		EXPECTED	ACTUAL	
5	CLK ARRAY	TEST 0	01	1	11	01	FAIL
(All tests in the ACQ MEM and HIGH RES functions passed.)							

OBSERVATIONS

The tests that pass indicate that the problem is isolated to the clock array RAM and associated circuitry not common to the rest of the memory matrix. The failure code indicates that RAM U475 (schematic 54A failed the first time a 1 was tried as bit 0.

ACTION

Check the data path from pin 1 of U158 to pin 15 of RAM U475. Also, check RAM U475 for D0(H)-to-Q0(H) storage.

91A04A CLOCK ARRAY TEST 0 DESCRIPTION

Refer to Figure 7-25, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds in Figure 7-25 identify the relevant schematics.

This test verifies operation of the slow clock array RAM. This test is similar to test 8 of the acquisition memory function except that the data stored in the clock-array RAM is the 91A32 INT CLK from the Trigger/Time Base board. Also, the data is changed on each bit rather than on each location.

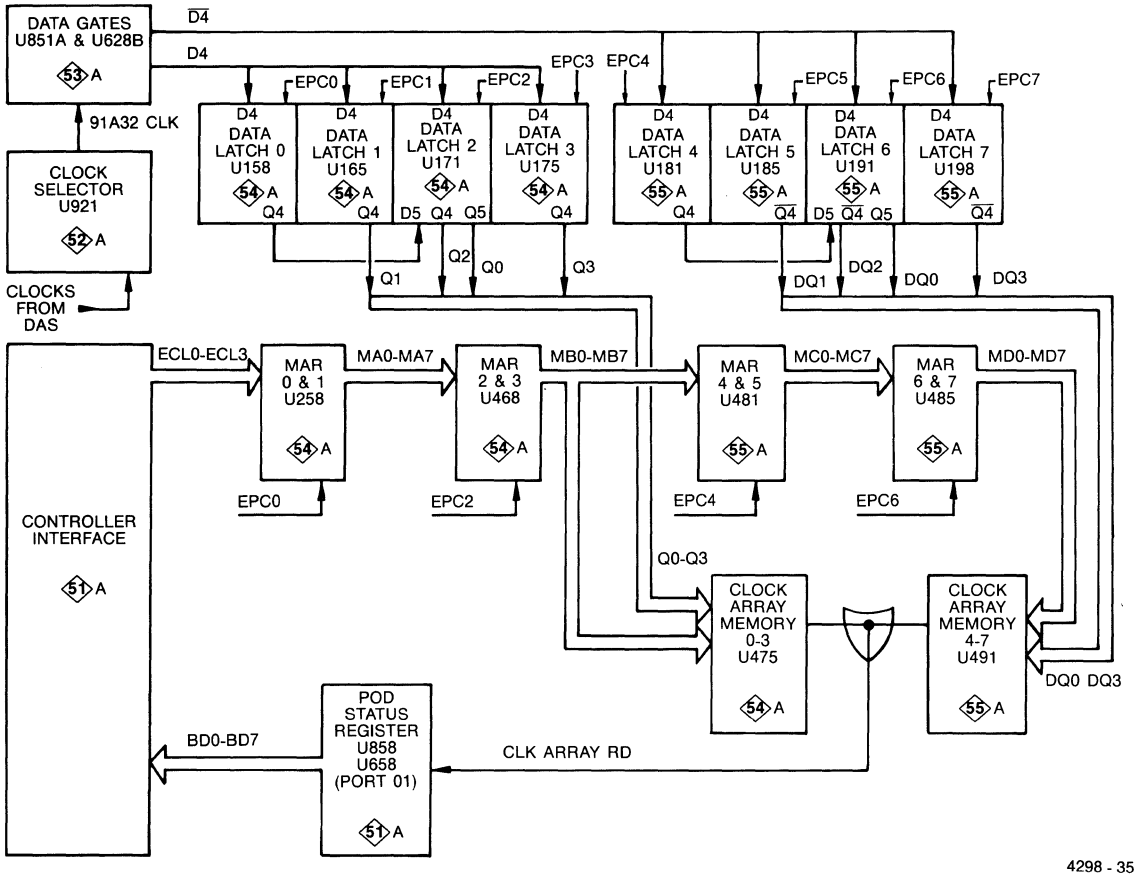

Figure 7-25. 91A04A blocks tested by clock-array test 0.

Initial Conditions

Circuit conditions for clock-array RAM test 0 are initialized as follows:

1. The module is set to normal resolution by writing $0C_{hex}$ to port $0D_{hex}$ (high-resolution register U728 on schematic 52A).

2. The module is prevented from triggering by resetting ARM 91A04 TRIG(H) and ARM 91A04 on 91A32 TRIG(H). This is done by writing 00_{hex} to port $0B_{hex}$ (trigger-control register U738 on schematic), asserting CLEAR TRIG(H).

3. The single step clock is selected and enabled on the Trigger/Time Base module (as in the difference counter function). This clock is selected on the 91A04A by writing $D0_{hex}$to port $0D_{hex}$ (U728 on schematic 52A). This selects the proper clock through U921C.

Before the start of each test, MARs 1 and 2 (U355 and U458 on schematic 54A) are loaded with FF_{hex}. Clock phase generator U151 (schematic 56A) is loaded with 60_{hex}. Using a similar procedure, write enable register U251 (schematic 56A) is loaded with DF_{hex} using bits 2 and 3 of memory control register U745 (schematic 52A). At the start of each test, all RAM select signals are reset low to enable writing by sending $00_{hex}$to port 07_{hex} (write-data register U651 on schematic 52A).

NOTE

Initial conditions for this test are the same as those used for acquisition memory tests 0-7, with the exception that the deskew selectors are not used. The initial conditions for each pass are the same as for test 8 of the acquisition memory function.

Before the first pass is started, the state of U851A (schematic 53A) is determined by loading the first address of the clockarray RAM with the value in U851A. This is accomplished by writing seven diagnostic single-step clocks to the 91A04A after initializing for the first pass, then reading the result (CLOCK ARRAY RD(H) at memory location 00_{hex} through port 01_{hex} (U858 and U658 on schematic 51A). If the value is 1, the 91A32 single-step clock on the Trigger/Time Base board resets U851A to the low state. The initial conditions for the pass are reinstated, and the test is started.

Test Sequence

Each pass operates by clocking the data from U851A through U628B to the clock-array RAM. For each diagnostic single-step clock that is produced to load the clock array RAM, a corresponding clocking of the 91A32 single-step function on the Trigger/Timebase board produces the pattern in memory detailed in Table 7-27.

As in the initializing routine, all data is read through port 01_{hex} (U858 and U658 on schematic 51A) one bit at a time. This is done by resetting the select lines from write-data register U651 (schematic 52A) one at a time at each address until eight bits are read. Then the MAR is loaded with the next address to be read. The read operation is repeated 255 times.

Circuit Conditions

Table 7-28 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States of the listed ICs are both high and low (hi/lo) at some point during the test.

Table 7-28
CONDITIONS FOR CLOCK ARRAY TEST 0

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U491	hi/lo	U198, pin 5	hi/lo
	U475	hi/lo	U175, pin 6	hi/lo
	U628B	hi/lo	U191, pins 5,3	hi/lo
	U851A	hi/lo	U171, pins 3,6	hi/lo
			U185, pin 5	hi/lo
			U165, pin 6	hi/lo
			U181, pin 5	hi/lo
			U158, pin 6	hi/lo
R	U858, pin 1	hi/lo	U658, pin 5	hi/lo

91A04A FUNCTION 6/91AE04A FUNCTION 3, HIGH RESOLUTION

CIRCUIT OVERVIEW

Data selector U525 (schematics 53A/61A) usually transmits the data from the deskew circuits on selector side 1 directly to the respective login register. However, if the board is programmed to acquire data at 660 MHz (high-resolution mode), only channel 0 and channel 2 are operational using side 0 of the selector. The inputs to side 0 of the data selectors are:

- Deskew circuit channel 0
- Deskew circuit channel 0 delayed by 1.5 ns
- Deskew circuit channel 2
- Deskew circuit channel 2 delayed by 1.5 ns

In this way, in one acquisition cycle, the module can log in the data currently present at channels 0 and 2, and the data that was present 1.5 ns previously. Since the internal clock driving the login registers is running at 3.0 ns (330 MHz), the effective acquisition rate becomes 660 MHz from two channels. (Refer also to the *Login Registers* discussion in the *Theory of Operation* section of this addendum.)

HIGH RESOLUTION FUNCTION DESCRIPTION

This function consists of a single test (test 0) which verifies operation of the high-resolution circuitry in the login register area by writing data through the login registers to the eight RAMs at location 0 with different patterns, then reading these RAMs to ensure that all bits are rearranged properly by the high-resolution circuitry.

Loading The Data

The value FF_{hex} is written to deskew registers 0 and 1 (write ports 09_{hex} and $0A_{hex}$, U225 and U725 on schematic 53A or 61A) to select the ECL0-ECL3 data-bus inputs to the four login registers. The ECL0-ECL3 values are then clocked into the login registers by the diagnostic single-step clock.

Reading The Results

Each of the eight RAMs (0-7) at location 0 are read by writing a value with only one bit low to write-data register U651 (port 07_{hex}) an (schematics 52A/60A). This enables one of the RAMs to be read through acquisition readback buffers U548 and U655 (port 04_{hex}) (schematics 55A/63A).

91A04A/91AE04A HIGH RESOLUTION TEST 0 TROUBLESHOOTING

Reading The Test 0 Error Codes

Test 0 of the high resolution function provides results like those shown in Figure 7-26. Table 7-29 lists the written and expected values for each RAM. (Written values, expected values, and port numbers in the table are in hexadecimal.) In Figure 7-16, 04 is the readback port, 0C (converted from XXXX 1100) is the hexadecimal value expected, and 01 (converted from XXXX 0001) is the actual hexadecimal value assembled from the I/0 port. (The Xs are masked out and displayed as 0s.)

			ADDR	EXPECTED	ACTUAL	
6	HIGH RES	TEST 0	04	0C	01	FAIL

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Figure 7-26. 91A04A/91AE04A high resolution function, typical test 0 readback display.

Table 7-29
HIGH RESOLUTION FUNCTION TEST 0:
WRITTEN AND EXPECTED READBACK VALUES

Ram Number	Hexadecimal Value Written	Write Port	Hexadecimal Value Expected	Read Port
00	XC	04	XC	04
01	X9	04	X3	04
02	X6	04	XC	04
03	X3	04	X3	04
04	XC	04	XC	04
05	X9	04	X3	04
06	X6	04	XC	04
07	X3	04	X3	04

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
6	HIGH RES	TEST 0	04	09	09	FAIL

(All other functions passed.)

OBSERVATIONS	ACTION
Since this is the only failure, failure sources are quite limited. The error codes indicate that the first test for the change to the high resolution mode failed (adjacent bits are in opposite states.)	Check pins 2 and 19 of U728 (schematic 52A or 60A), and pins 1, 3,15, and 17 of U525 (see Table 7-30).

91A04A/91AE04A HIGH RESOLUTION TEST 0 DESCRIPTION

Refer to Figure 7-27, and to the indicated schematics, while reading this general description. The numbers enclosed in diamonds on Figure 7-27 identify the relevant schematics.

This test verifies the functionality of the high-resolution circuitry (U525 on schematic 53A or 61A) by using the RAM previously tested in the acquisition memory function. This is done by writing a specific pattern (refer back to Table 7-29) to RAM location 00_{hex}, then reading the RAMs to verify that the pattern was loaded with all odd/even pairs the same (bit 0 = bit 1 and bit 2 = bit 3).

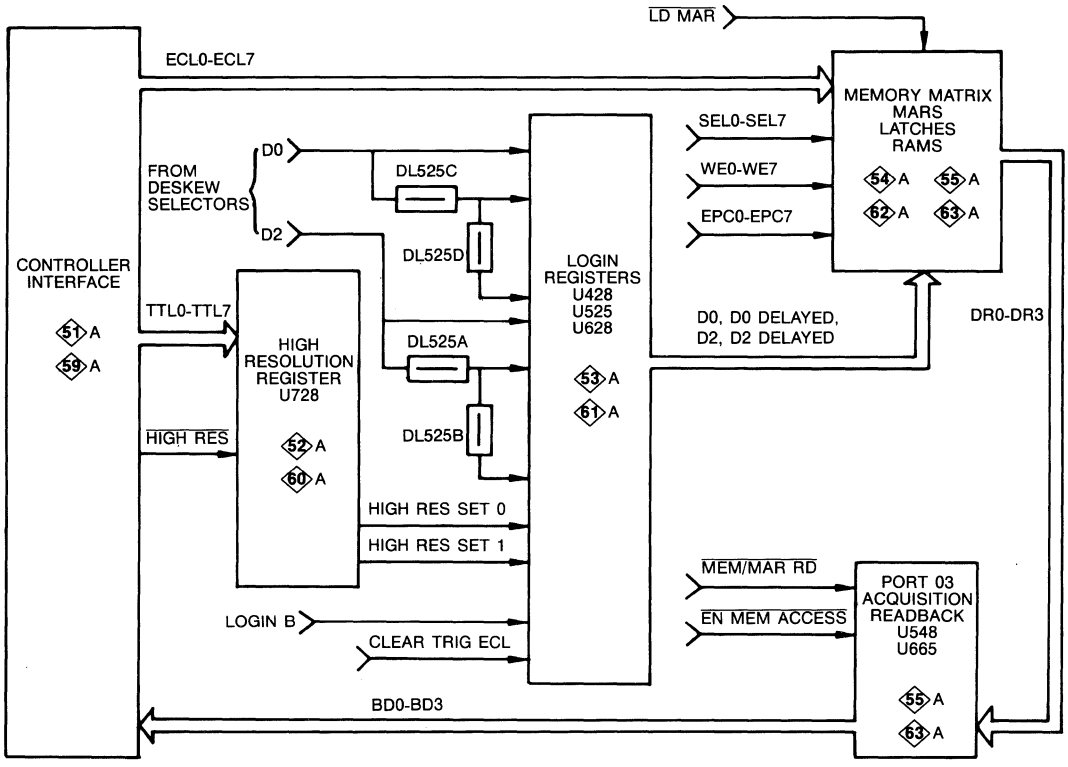

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Figure 7-27. 91A04A/91AE04A blocks tested by high resolution test 0.

Initial Conditions

The high-resolution mode is selected by resetting bits 2 and 3 of port $0D_{hex}$ (high-resolution register U728 on schematic 52A or 60A) to 0. This changes the select mode of 2-to-1 multiplexer U525 (schematic 53A or 61A) to the D0 side.

All 1s are written to port 09_{hex} and $0A_{hex}$ (deskew latches U225 and U725 on schematic 53A or 61A), selecting the ECL0-ECL3 data bus through the deskew selectors (U218, U418, U518 and U618 on schematic 53A or 61A). Port $0B_{hex}$ (U738 on schematic 52A or 60A) is written with 00_{hex}, resetting CLEAR TRIG(H), ARM 91A04 TRIG(H), and ARM 91A04 ON 91A32 TRIG(H).

Initial conditions for the start of each pass are the same as for acquisition memory tests 0-7.

Test Sequence

Ten writes to port 04_{hex} (the diagnostic single-step clock, U688 on schematic 51A or 59A) load the patterns indicated in Table 7-29 into location 00_{hex} in all eight RAMs (the same as in acquisition memory tests 0-7). Also, the memory is read the same as in acquisition memory tests 0-7.

After the RAM is read, bit 0 is checked to verify that it equals bit 1, and bit 2 is checked to verify that it equals bit 3 for each RAM. This ensures that bits 0 and 1 have been combined into one channel, and that bits 2 and 3 have been combined into the other channel.

Circuit Conditions

Table 7-30 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States for each IC listed are both high or low (hi/lo) during the test.

Table 7-30
CONDITIONS FOR HIGH RESOLUTION TEST 0

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U525, pins 1,3,15,17	hi/lo	U728, pins 19,2	low

91A04A FUNCTION 7/91AE04A FUNCTION 4, WORD RECOGNIZER

CIRCUIT OVERVIEW

The word recognizer monitors the data received by the 91A04A module. When the trigger word is recognized, the word recognizer signals the trigger. The word recognizer consists of three parts:

1. The first part determines whether a specific bit must be high or low for a trigger.

2. The second part determines the trigger care or don't-care status of a particular bit.

3. The third part determines wheather all lines in the expander-module simultaneously meet the requirements for a trigger.

Refer to the *Trigger, Word Recognizer* discussion in the *Theory of Operation* section of this addendum for additional information.

WORD RECOGNIZER TEST DESCRIPTION

Test 0 verifies the word recognizer circuitry in 16 passes. On each pass, the module is set to trigger on a particular pattern from $X0_{hex}$ to XF_{hex}. On each pass, all possible patterns except the correct pattern are written to the word recognizer, and the 91A04 TRIGRD(L) line is tested for a not-triggered condition. Finally, the correct pattern is written, and 91A04 TRIGRD(L) is checked for the asserted condition (low).

Test 1 verifies the don't care portion of the word recognizer by setting the module to trigger on a pattern of 1s with only one bit being 0 (see Table 7-31). That bit is also set to DON'T CARE. Then $0F_{hex}$ is written to the registers and 91A04 TRIGRD(L) is checked for the asserted condition. Each of the four bits of the word recognizer is handled in the same manner.

Loading The Data

Loading Test 0

After initial conditions are set up, the pattern being tested ($X0_{hex}$ to XF_{hex}) is written to write control register U735 (port 08_{hex} schematic 52A or 60A) on the upper four bits (WD0-WD3). The lower four bits (WC0-WC3) are reset to the CARE (0) condition. When the tests are running, the 16 possible patterns are written to port 04_{hex} (diagnostic single-step clock) to load the login registers and the word recognizer latches.

Loading Test 1

After initial conditions are set up on each of the four passes, the upper four bits of write-control register U735 (schematic 52A or 60A) is set to recognize the trigger word (see Table 7-31). Table 7-31 also lists the values written for each of the four passes to the CARE part of the write-control register. On each pass, a 0 is loaded into the login and word recognizer registers four times by the diagnostic single-step clock. (Note that the login registers invert data.) The values written, the write ports, and the read ports listed in Table 7-31 are hexadecimal.

Table 7-31
VALUES WRITTEN FOR WORD RECOGNIZER TEST 1

Pass No.	Trigger Word	Care Word 1=Don't Care	Value Written	Write Port	Expected Value	Read Port
1	0111	1000	FF	04	8 20	01
2	1011	0100	FF	04	4 20	01
3	1101	0010	FF	04	2 20	01
4	1110	0001	FF	04	1 20	01

READING THE RESULTS

All results in test 0 and test 1 are read through card-MOS status buffer U661 (read port 01 on schematic 51A). Note that 91A04 TRGRD(L) is inverted by U858 before buffer U661.

91A04A/91AE04A WORD RECOGNIZER TEST 0 TROUBLESHOOTING

Reading The Test 0 Error Codes

Test 0 of the word recognizer function provides results like those shown in Figure 7-28. There are only two possible expected results for test 0: 91A04 TRIGRD(L) low (expect 20 because of U858 inversion), and 91A04 TRIGRD(L) asserted high (expect 00 because of U858 inversion).

Figure 7-28 is interpreted as follows:

01 is the I/O port read.

4 is the value being tested.

20 (converted from XX1X XXXX) is the expected value from the I/O port.

00 (converted from XX0X XXXX) is the actual value read.

			ADDR	EXPECTED	ACTUAL	
7	WRD REC	TEST 0	01	4 20	00	FAIL

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Figure 7-28. 91A04A/91AE04A word recognizer function, typical test 0 readback display.

Analyzing The Test Indications

The following sample error indication, and its analysis, is intended only to illustrate how the error indications can be used to locate the fault.

Error Indication

			ADDR	EXPECTED	ACTUAL	
7	WORD REC	TEST 0	01	0 20	00	FAIL
7	WORD REC	TEST 1	01	8 20	00	FAIL

(All other functions passed.)

OBSERVATIONS	ACTION
Since the only failures are in both tests of the WORD REC function, the area of possible faults is between U538 and U448 in the word recognizer circuit, and in the readback through port 01_{hex} (U658 on schematic 51A).	Disconnect W642 and check to see if the failure code changes. If it changes to always triggered, the readback through U658 and circuitry following W642 is operational. Check, U641C and U635A on schematic 57A or 65A (see Table 7-31).

91A04A/91AE04A WORD RECOGNIZER TEST 0 DESCRIPTION

Refer to Figure 7-29, and to the indicated schematics, while reading the following general description. The numbers enclosed in diamonds on Figure 7-29 identify the relevant schematics.

Test 0 verifies that the word recognizer will select the correct pattern out of 16 possible combinations that are programmed. Sixteen passes verify all 16 combinations.

NOTE

If diagnostics are run with expanders in the system, U635A and W642 in each expander is checked for a low when the master module word-recognizer function is run. This is accomplished by forcing each card to a triggered state by loading don't cares in word recognizer latches U538 and U635B. Also, if a particular expander is the target of the diagnostics, the master 91A04A and all other expanders are set to don't care (as above) and the expander being tested is checked through the master module.

Initial Conditions

The ECL0-ECL3 data bus is used the same as in the acquisition memory function to apply data to the login registers on all 91A04A and 91AE04A modules. All modules are put into the triggered state by writing don't cares to all latches (U635B and U538) and by writing $0F_{hex}$ to port 08_{hex} (write control register U735).

Then, on the master module, $0X_{hex}$ is written to DELAY 1(L) (port 06_{hex}) to ensure that 91A04 STOP STORE(H) is disabled (low) for the duration of test 0.

Normal resolution is selected by writing $0F_{hex}$ to port $0D_{hex}$ (high-resolutiion register U728) on all modules.

The CLEAR TRIG(H) signal is then asserted, then removed, on all modules to set all circuits to a known state.

The diagnostic single-step clock is enabled by setting EN MEM LD(H), and is stepped four times to load 1s into the word recognizer pipeline. This simultaneously triggers all modules.

Test Sequence

Test 0 is accomplished as follows:

1. The CLEAR TRIG(H) signal is asserted in the module under test. This removes the triggered indication from that module.

2. The first value tested (0) is written to port 08_{hex} (write-control register U735) on the upper nibble. The lower nibble is set to all care's (0).

3. If the pass currently conducted is for 0, FF_{hex} followed by $7F_{hex}$ is written to port 02_{hex} (clock-slecect register U731) to assert and remove TRIG PRESET(H). This removes any 0s from the login registers.

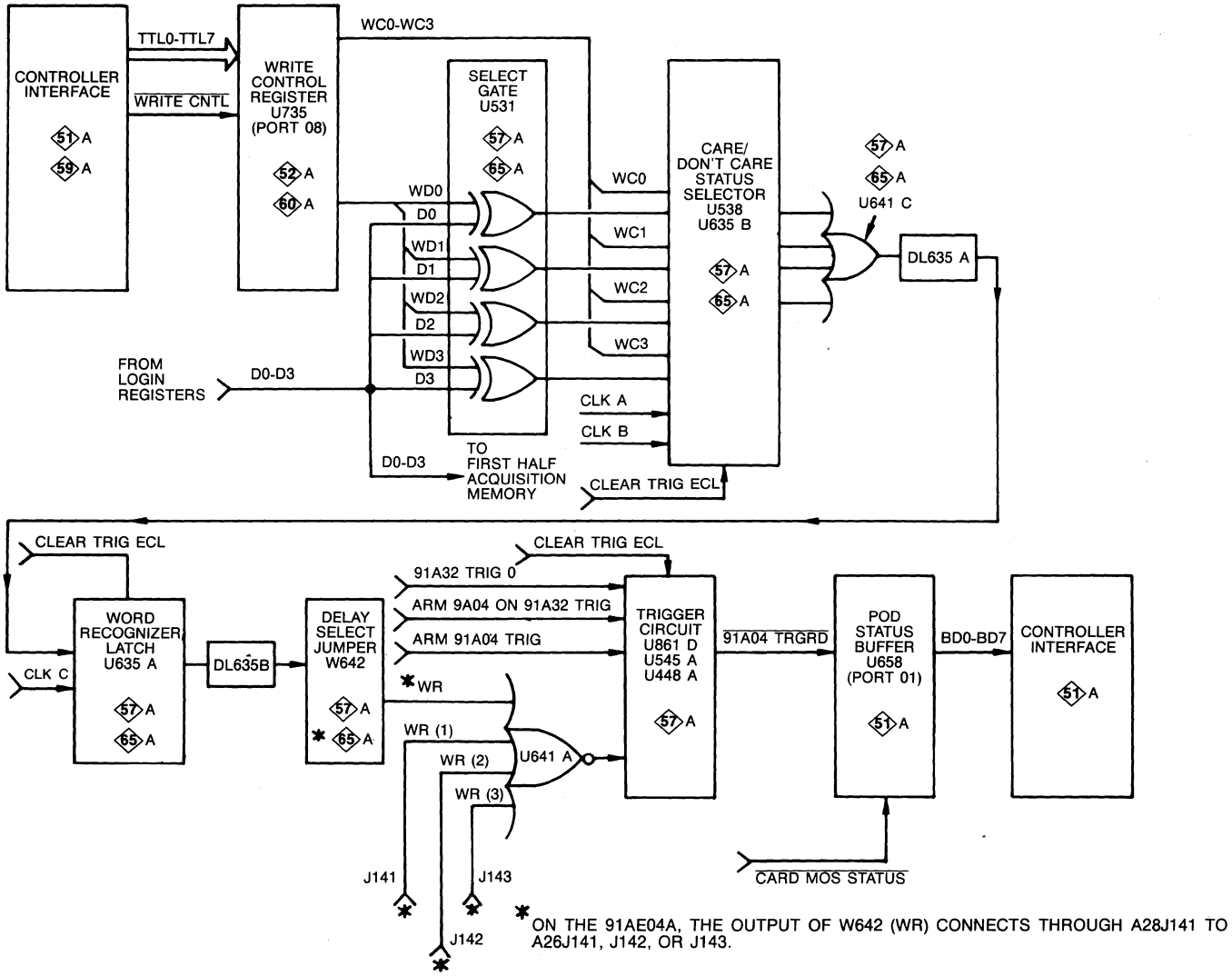

Figure 7-29. 91A04A/91AE04A blocks tested by word recognizer tests 0 and 1.

4. All patterns are then clocked through the login registers and word recognizer latches except the value that matches and the 91A04 TRIGRD(L) is checked for a false indication.

5. If the module under test is an expander module, the master module is cleared and single-step clocked four times to make sure that it is not in the way of testing the target module. If it actually causes a true triggered indication, an error is reported.

6. A diagnostic single-step clock is generated and sent to the expander module to trigger the entire system, and the 91A04 TRIGRD(L) signal is checked for a true indication.

7. The above steps are repeated until all 16 patterns are tested true through the word recognizer of the target module.

Circuit Conditions

Table 7-32 lists the exact state of each pin or bit component needed to pass the test. Table 7-32 is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. Some of the tests are paired so that both polarities are checked to ensure proper verification.

NOTE

The lowest-numbered tests in the lowest-numbered functions verify circuits that are used in the functions and tests that follow. Therefore, if multiple tests and/or functions fail, go to the **earliest** *test that failed in the* **lowest** *function to determine the cause of the failure.*

The states checked can be high, low, rising edge (⌐), or falling edge (¬). The word *circuit* used in Table 7-32 includes all connections to the labeled IC, including resistors, capacitors, and transistors. Only the target circuits and the secondary circuits are included in the table (not all possibilities).

Table 7-32
CONDITIONS FOR WORD RECOGNIZER TEST 0

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U531	hi/lo	U735, bits 0-3	low
	*U538	hi/lo	U735, bits 4-7	hi/lo
	U641A,C	hi/lo	W642	hi/lo
	U635A	hi/lo	U448A, pins 15,20	hi/lo
	*U635B	hi/lo	U345	⌐
			U328, pin 2	⌐
			U328, pin 6	¬
			U228, pin 2	⌐
			U341, pin 7	¬
R	U448A, pin 13	hi/lo	U858, pin 2	hi/lo
			U658, bit 5	hi/lo

*Except reset inputs are low only.

91A04A/91AE04A WORD RECOGNIZER TEST 1 TROUBLESHOOTING

Reading The Test 1 Error Codes

Test 1 of the word recognizer function provides results like those shown in Figure 7-30. (The Xs are masked out and displayed as 0s.)

Figure 7-30 is interpreted as follows:

01 is the I/O port read.

4 is the written DON'T CARE mask (see Table 7-31).

20 (derived from XX1X XXXX) is the expected value from the I/O port.

00 (derived from XX0X XXXX)is the actual value read.

			ADDR	EXPECTED	ACTUAL	
7	WRD REC	TEST 1	01	4 20	00	FAIL

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Figure 7-30. 91A04A/91AE04A word recognizer function, typical test 1 readback display.

Analyzing The Test Indications

Refer back to the word recognizer test 0 analysis.

91A04A/91AE04A WORD RECOGNIZER TEST 1 DESCRIPTION

Refer back to Figure 7-29, and to the indicated schematics, while reading the following general description. The numbers enclosed in diamonds on Figure 7-29 identify the relevant schematics.

Initial Conditions

Initial conditions for word-recognizer test 1 are the same as for test 0.

Test Sequence

Word recognizer test 1 is accomplished as follows:

1. The module under test is cleared and the first pattern listed in Table 7-31 (0111 1000) is written to port 08_{hex} (U735 on schematic 52A or 60A). This causes the word recognizer circuitry to look for X111.

2. Then a 0 is written to the system with the diagnostic single-step clock four times. This is inverted by the login registers and, if the circuitry is operating correctly, the 91A04 TRIGRD(L) line at port 01_{hex} (POD status register U658 on schematic 51A) should read true.

NOTE

The expander modules are tested through the master module as in word recognizer test 0.

Circuit Conditions

Table 7-33 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be both high and low (hi/lo) during the test.

Table 7-33
CONDITIONS FOR WORD RECOGNIZER TEST 1

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U538, pins 2,4,17	hi/lo	U735, bits 0-3	hi/lo
R	U635B, pin 2	hi/lo		

FUNCTION 8 91A04A/FUNCTION 5 91AE04A DESKEW TEST

CIRCUIT OVERVIEW

The deskew circuits are programmable delay lines. During deskew operations, the DAS mainframe Controller calculates the amount of delay necessary for each data line from the P6453 Probe to make setup and hold specifications. The Controller then programs the deskew circuits to insert the proper amount of delay in the data signal path. Refer to the *Theory of Operation* section of this addendum for additional information. Areas of interest are: *Interface Between the Module and the P6453 Probe* in the *General Description* subsection, and the *Deskew Circuits* description in the *Detailed Circuit Description* subsection.

Deskew Test Description

This is a manual test that exercises the deskew registers. To use this function, a P6453 Probe must be connected to the module under test, and the probe hybrids must be plugged into the deskew connectors on the probe. This function repeatedly writes the deskew line in the probe while selecting values from 0 to 14 on the deskew registers. The results are observed on an oscilloscope with a fast probe, Such as a P6201 FET Probe.

While this function is running, the DAS displays the message EXERCISING DESKEW MULTIPLEXERS.

DESKEW TEST TROUBLESHOOTING

To set up the test for the 91A04A, connect a P6453 probe to the probe connector on the 91A04 under test, and connect the probe hybrids to the deskew connectors on the top of the probe housing. Select SINGLE mode in the Diagnostics menu and enter 8 in the FUNCTION field.

To set up the test for the 91AE04A, connect P6453 probes to the 91A04A master module and to the 91AE04A expander module. Connect the clock hybrid from the expander module probe to the deskew connector on the expander module's probe, and connect the four data hybrids on the expander module's probe to the deskew connectors on the master module's probe. Select SINGLE mode in the Diagnostics menu and enter 5 in the FUNCTION field.

To observe the results, set up the oscilloscope as follows:

1. Connect the oscilloscope vertical input through a X10 FET probe (slow probe) to the output of a deskew register (U218, U418, U518, or U618 on schematic 53A or 61A) at pin 11. Make sure the probe is well grounded.

2. Trigger the oscilloscope on the input to the same deskew register at pin 24 using external triggering with a P6106 10X passive probe. Make sure this probe is well grounded also.

3. Observe that the oscilloscope displays a 15-step staircase waveform with approximately 400 ps between steps. (The repetition rate is very low. Adjust oscilloscope sweep rate accordingly.)

4. Repeat the above steps for each of the remaining three deskew registers.

Analyzing The Test Indications

Error Indication
The staircase waveform is not present, and the scope will not trigger on any channel.

OBSERVATIONS	ACTION
Since this symptom applies to all channels, the common circuitry is from the probe pod back to the DESKEW PULSE OUT(H) signal from U545D and U688 schematics 51A/59A. Also, this symptom could indicate a power supply problem in the probe system.	Check DESKEW PULSE OUT(H) from U545D (schematics 51A/59A) and check the +15 V supply, the +3 VL supply, and the +10 V supply.

91A04A/91AE04A DESKEW TEST DESCRIPTION

Refer to Figure 7-31, and to the indicated schematics, while reading this general description. The numbers in diamonds on Figure 7-31 identify the relevant schematics.

The deskew line to the probe is written through address decoder U688 and inverter U545D.

The DESK 0(L) and DESK 1(L) outputs of U688 are asserted low to deskew latches U225 and U725.

The TTL0-TTL7 bus repeatedly writes values from 0 to 14 through the deskew latches to deskew selectors U218, U418, U518, and U618.

The output of each deskew selector, observed with an oscilloscope, is a 15-step (0-14) staircase waveform.

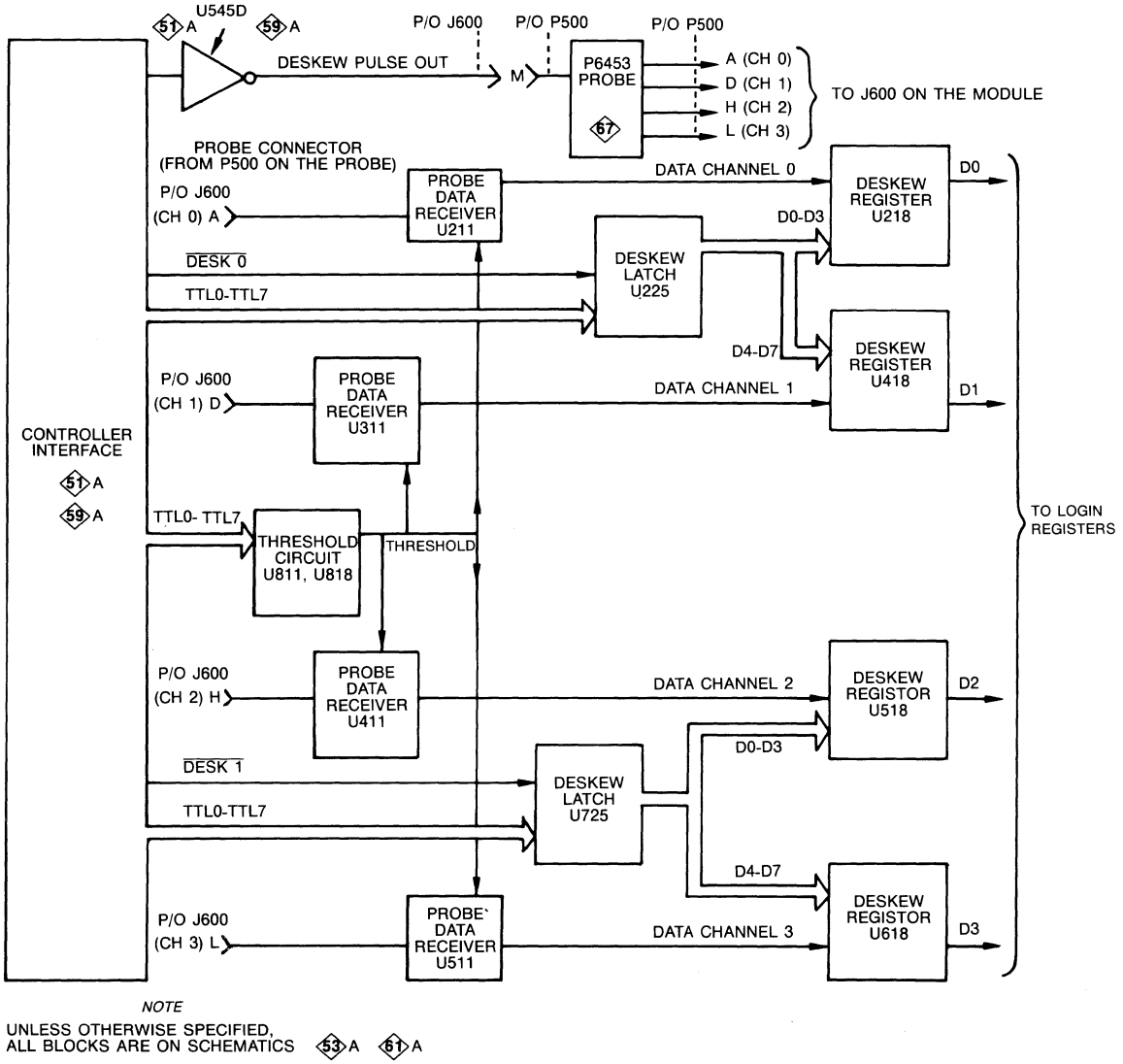


Figure 7-31. 91A04A/91AE04A blocks tested by the deskew test.

Circuit Conditions

Table 7-34 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be low, analog (voltage), or both high and low (hi/lo) during the test.

Table 7-34
CONDITIONS FOR THE DESKEW TEST

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	P6453	hi/lo	U688, pin 2	hi/lo
	U225	low	U688, pin 16	low
	U725	low	U545, pin 14	hi/lo
	*U218	hi/lo	U818	voltage
	*U418	hi/lo	U811	voltage
	*U518	hi/lo	U901	voltage
	*U618	hi/lo	U902	voltage
	U211	hi/lo	U991A	voltage
	U311	hi/lo		
	U411	hi/lo		
	U511	hi/lo		

* Outputs, and pin 19, previously checked in acquisition memory function, tests 0-7.

FUNCTION 9 91A04A/FUNCTION 6 91AE04A, DAC THRESHOLD

CIRCUIT OVERVIEW

Digital-to-analog converter (DAC) U811 on schematic 53A or 61A, and its associated probe-threshold circuits, controls the threshold of the comparators that receive clock and data from the P6453 Probe. This allows the threshold to be digitally controlled through DAS menus. Refer to the *Probe Threshold* discussion in the *Detailed Circuit Description* subsection of the *Theory of Operation* section of this addendum for additional information.

DAC THRESHOLD TEST DESCRIPTION

This is a manual test that exercises the threshold DAC by setting the threshold to different values so that DAC operation can be verified. The default threshold value from the function 9 diagnostic menu is +1.250 V. Other values of +1.120 V, +0.750 V, and +0.500 V can be obtained using the SELECT key. Threshold values can be measured at TP600 using a digital multimeter (DMM).

While this function is running, the DAS displays the message:

DAC THRESHOLD SET +1.250V (default value)
REFERENCE VOLTAGE IS +3.0 VL

Loading The Data

The following values are loaded by writing to the DAC (U811) via the TTL0-TTL7 bus:

- 1.250 V (the default value) is written with $E4_{hex}$.
- 1.120 V is written with CA_{hex}.
- 0.750 V is written with 80_{hex}.
- 0.500 V is written with $4E_{hex}$.
- Ramping is written by repeatedly incrementing from 0 to FF_{hex}.

DAC THRESHOLD TROUBLESHOOTING

To set up the test, proceed as follows:

CAUTION

Do not install or remove any electrical module or sub-assembly in a DAS mainframe while the power is on. Doing so can cause damage to the module or sub-assembly.

1. Power down the DAS.
2. Install the jumpers on the DAS Main Extender Board over the upper two pins (for slots 1 through 6).
3. Install the DAS Main Extender Board in the appropriate slot in the DAS, and place the module under test on the extender. If the module under test is a 91AE04A, use the long clock and word recognizer cables from the DAS Service Maintenance Kit in place of the normal clock and word recognizer cables.
4. Power up the DAS.
5. Deskew the probe for the module under test as described in the *Function 8 91A04A/Function 5 91AE04A Deskew Test* description.
6. Enter the Diagnostics menu.
7. Select the slot in which the module under test resides, then select function 9 (91A04A) or 6 (91AE04A). The DAS should display the default threshold value of +1.250 V.

To Measure The Threshold Voltages, Perform the following steps:

1. Set the DMM to the 2 Vdc scale and monitor TP600 (just above probe connector J600) with the red meter lead, and monitor the junction of C105 and +3 VL (the minus side of C105) with the black meter lead. Refer to the test point location diagram in the *Reference Information* section of this addendum for the locations of TP600, C105, and +3 VL.

2. Verify that the DMM reads 1.2500 V +0.001 V. If the threshold voltage does not meet this requirement, adjust R818 to bring the voltage within tolerance.

3. Press the DAS SELECT key to select each of the other fixed values and verify that the DMM indicates a value within the following limits:

   +1.2000 V selection must be between +1.1170 V and 1.1230 V.

   +0.7500 V selection must be between +0.7480 V and 0.7520 V.

   +0.500 V selection must be between +0.4985 V and 0.5015 V.

4. Disconnect the DMM and connect the oscilloscope as follows:

   a. Connect the probe tip to TP600.

   b. Connect probe ground to the ground (G) test point just below U618 and above U818.

5. Check the oscilloscope display for a voltage waveform which ramps up from approximately +3.150 V to approximately +4.385 V.

If the threshold cannot be adjusted to within the specified limits, or if the ramp is not as specified, check the components in Table 7-35 for the states listed.

NOTE

This ramp is generated by writing the DAC from 00_{hex} to FF_{hex}. Although this generates 255 steps in the ramp, the increments are too small to discern on the displayed waveform.

The TTL0-TTL7 bus has been used for several earlier diagnostic functions. If those functions passed, the bus can be assumed operational.

DAC THRESHOLD FUNCTION DESCRIPTION

Refer to the indicated schematic in the *Diagrams* section of this addendum while reading the following description.

The data input to from the DAS to the controller interface (schematics 51A/59A) is passed through buffer U655 to the TTL0-TTL7 bus, then applied to the DAC (schematics 53A/61A). This data contains the digitized value for the threshold voltage.

Data to address decoder U688 asserts THRESHOLD(L) which enables the DAC to read the data and produce a corresponding analog dc output level to comparator U818 (schematic 53A or 61A). The output of U818 can be measured at TP600 with a DMM.

Circuit Conditions

Table 7-35 lists the exact state of each component needed to pass the test. The table is arranged in the sequence in which the operations are performed. Therefore, tests that pass are used to verify circuits in the tests that follow. States checked can be low, analog (voltage), or both high and low (hi/lo) during the test.

Table 7-35
CIRCUIT CONDITIONS FOR THE DAC TEST

Read/ Write	Target Circuit	State	Secondary Circuit	State
W	U811 U818	voltage voltage	U688, pin 16	low

DETECTING AND ISOLATING HIGH-SPEED PROBLEMS

Some high-speed failures can be identified by specific functional checks, specific performance checks, or deskew procedures. Other problems cannot be identified by those procedures. This discussion addresses both categories.

CIRCUITRY TARGETED BY FUNCTIONAL OR PERFORMANCE CHECKS

Refer to the *Verification and Adjustments* section of this addendum for the functional checks and performance checks referenced in this discussion.

Performance Check (4) Internal Clock Accuracy Test

This test checks only the internal 3 ns and 5 ns oscillator channels up to U125.

Functional Check (9) Verifying the High-Speed Internal Clocks

This is the first test to check the total system operation at 330 MHz. Careful investigation of the data resulting from at least three different storage cycles provides several indications if the test passes. These are:

- The 330 MHz clock is correctly distributed throughout the system.
- The memory matrix is operating correctly (with a 75% confidence factor).
- The word recognition and trigger system is operation correctly (with a 75% confidence factor).
- The initial latches and high=speed data distribution system is operating correctly at 330 MHz (with a 75% confidence factor).

Functional Check (3) Verifying Deskew Operation

This procedure checks the propagation integrity of the external-clock rising edge through the probe and clock distribution system up to the LOGIN A(H) and LOGIN B(H) signals.

Performance Checks:

(11) 1.5 ns Data Acquisition Test

(13) 300 MHz Rising-Edge Clock Setup-and-Hold-Time Test

(14) 300 MHz Falling-Edge Clock Setup-and-Hold-Time Test

These tests extensively test the acquisition and storage of data at 330 MHz internal clock rates and 300 MHz external clock rates. Specific areas checked are:

- The deskew circuits, login latches, and high-speed data distribution at 300 MHz and 330 MHz.
- The 300 MHz and 330 MHz clock distribution.
- The memory matrix at 300 MHz and 330 MHz.

Performance Checks:

(7) 660 MHz Asynchronous Word Recognition Test, Channel 0

(8) 660 MHz Asynchronous Word Recognition Test, Channel 2

(9) 330 MHz Asynchronous Word Recognition Test, Channel 1

(10) 330 MHz Asynchronous Word Recognition Test, Channel 3

(15) High-Speed Word Recognizer Timing Check (91A04A only)

(16) 91AE04A to 91A04A High-Speed Word Recognizer Timing

These tests primarily target the word-recognizer circuitry to make sure it can detect very narrow pulses and supply correctly timed signals to the trigger and delay circuitry to stop acquisition so that the trigger is placed correctly.

HIGH-SPEED PROBLEMS

Some high-speed problems cannot be detected by the functional checks or performance checks. They will probably have some of the following characteristics:

- The failure involves the ARMS mode. Most ARMS mode problems can be resolved by carefully reading the specifications associated with that feature. (Refer to the *Introduction and Specifications* section of this addendum.)
- The failure is frequency sensitive; only at 232 MHz for example.
- The probe has an intermittent hybrid which is degrading performance.
- The user is violating one or more of the guaranteed specifications.
- The module has a heat sensitive component.

- The threshold circuitry is off far enough at the users threshold to degrade high-frequency performance.
- The module has a peculiar pattern sensitivity.
- The user is using the wrong lead set.

Also, the difference counter and the clock array memory system are not checked in high-frequency operation. They are checked only by functional check *(11) Verifying 91A32 (Slow Card) ARMS 91A04 Mode*. Refer to the *Verification and Adjustments* section of this addendum.

NOTE

The Maintenance: Reference Information *section of this addendum contains a special subsection on* Oscilloscope Techniques for High Frequency Measurements.

Section 8
MAINTENANCE:
DIAGNOSTIC TEST DESCRIPTIONS

For diagnostic test descriptions, see *Section 7, Maintenance: Troubleshooting.*

Section 9
REFERENCE INFORMATION

GENERAL INFORMATION

LOADING THE 91A04A AND 91AE04A ACQUISITION MEMORY

The 91A04A and 91AE04A acquisition memories are loaded only by acquiring data.

ERROR CODES AND INDICATORS

Rom Checksum Codes

If the DAS detects a checksum error on power-up, an error code is displayed at the top of the screen reading ROM CHECKSUM ERROR. The message also contains a numeric code that corresponds to a socket location on a DAS board. The code for the 91A04A module is interpreted as shown in Table 9-1. The 91AE04A contains no ROMs.

Table 9-1
91A04A ROM CHECKSUM ERROR CODES

Code Number	Location	Part Location
*,0	91A04A	A26U878
*,1	91A04A	A26U881
*,8	91A04A	A26U878

*This number indicates the slot in which the 91A04A resides (may be slots 1-6).

91A04A and 91AE04A Error and Prompter Messages

Table 9-2 lists error and prompter mesasages which are initiated by the 91A04A/91AE04A Data Acquisition Modules.

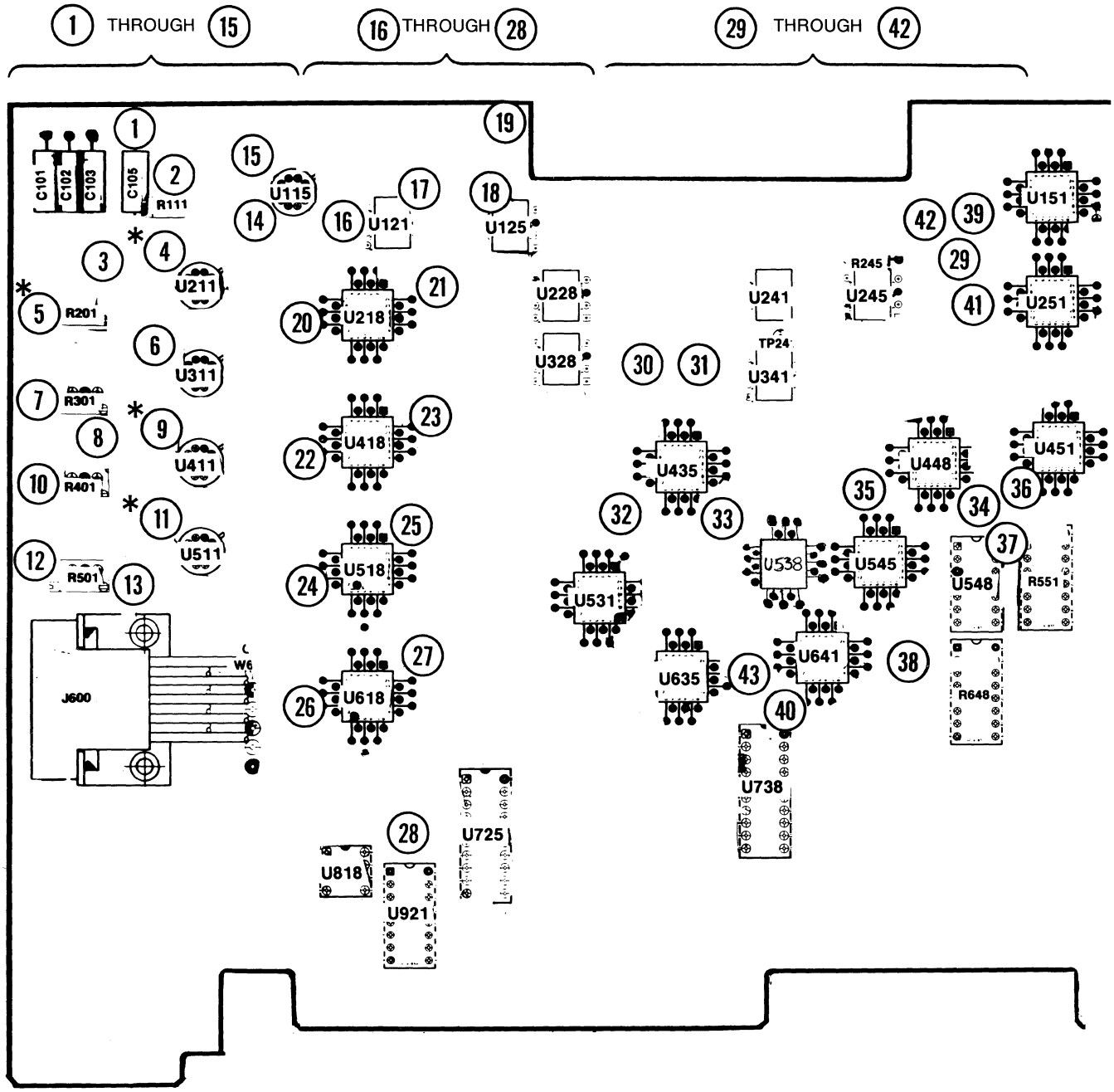
Table 9-2
ERROR AND PROMPTER MESSAGES:
Additions with 91AE04A and 91A04A
Data Acquisition Modules

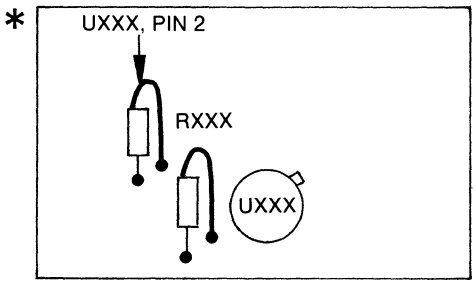
COMPARE =, ≠ DISABLED AT 1.5nS	Data acquired in the high-resolution (1.5 ns) mode cannot be viewed in the state table. Therefore, the state table's reference memory and the comparison functions are not accessible.
DESKEW COMPLETE	The deskew operation for all 91A04A, 91A04, 91AE04A, and 91AE04 probe channels has been completed successfully.
DESKEW INCOMPLETE	At least one of the 91A04A, 91A04, 91AE04A, and 91AE04 probe channels has not been successfully deskewed. The SETUP/HOLD field in the 91A04 ONLY trigger mode does not appear unless at least one channel has been deskewed.
PODS TO DESKEW XX	The listed probes have not been deskewed. (Probe selection is changed by the SELECT key.)
SLOW ACQUISITION	The master 91A04A or 91A04 module has not logged in a clock signal for at least 500 ns. If using an external clock that is known to be running faster than 500 ms, check the clock threshold and verify that an adequate signal is being received. If the condition continues after you have restarted acquisition, service maybe required.
STATE TABLE DISABLED AT 1.5 nS	Data acquired in the high-resolution (1.5 ns) mode can only be displayed in the Timing Diagram menu.
UNABLE TO DESKEW PODXX CH X....	The listed probe channels did not pass the deskew operation. Check the connections between the probe hybrids and the deskewing connectors on the probe. If the probe cannot be deskewed after these connections have been checked, service maybe required.

TEST POINT, JUMPER, AND ADJUSTMENT LOCATIONS

Figure 9-1 and the associated text provide a fast reference for adjusting and troubleshooting 91A04A and 91AE04A modules. The illustration shows the 91A04A master module. Items on the 91AE04A expander module are located in identical positions. The legend associated with the figure identifies those items which apply to the 91A04A only. Items not so specified apply to both 91A04A and 91AE04A modules. The illustration shows points of interest. Call-outs on the illustration describe, or point to a description of, the function of each item of interest.

For further information on adjusting, verifying, or troubleshooting a module, refer to the appropriate section of this addendum.





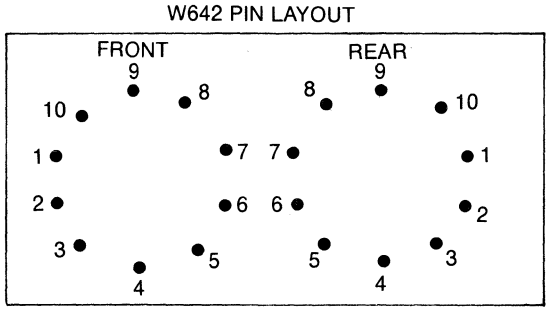


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Figure 9-1. Test-point, jumper, and adjustment locations.

(1) +3 VL.
This is the top lead of C105. It is measured with respect to ground to verify accuracy of +3 VL during the performance checks. It is also used as a reference for the threshold comparator output (TP600) for adjusting the threshold level, and for data channel comparator-offset adjustments. Measured with respect to +5 V.

(2) R111
This is the offset adjustment potentiometer for probe clock comparator U115. Make this adjustment while monitoring the comparator output level relative to its input level.

(3) C201/T201 Junction
This is a convenient test point for measuring +15 VC during the power supply performance check. Use TP116 (ground) just to the left of TP125 for reference.

(4) U211, Pin 2 (top of R203)
Pin 2 of U211 connects to the outer end of R203 (see inset on Figure 9-1). This test point is used to connect the current source while adjusting data channel 0 comparator offset potentiometer R201.

(5) R201
This is the comparator offset adjustment for data channel 0. Make this adjustment while monitoring comparator U211 output relative to its input.

(6) U311, Pin 2 (top of R303)
Pin 2 of U311 connects to the outer end of R303 (see inset on Figure 9-1). This test point is used to connect the current source while adjusting data channel 1 comparator offset potentiometer R301.

(7) R301
This is the comparator offset adjustment for data channel 1. Make this adjustment while monitoring comparator U311 output relative to its input.

(8) C401/T401 Junction
This is a convenient test point for monitoring +15 VD during the power supply performance check. Use TP116 (ground) just to the left of TP126 for reference.

(9) U411, Pin 2 (top of R403)
Pin 2 of U411 connects to the outer end of R403 (see inset on Figure 9-1). This test point is used to connect the current source while adjusting data channel 2 comparator offset potentiometer R401.

(10) R401
This is the comparator offset adjustment for data channel 2. make this adjustment while monitoring comparator U411 output relative to its input.

(11) U511, Pin 2 (top of R503)
Pin 2 of U511 connects to the outer end of R503 (see inset on Figure 9-1). This test point is used to connect the current source while adjusting data channel 3 comparator offset potentiometer R501.

(12) R501
This is the comparator offset adjustment for data channel 3. make this adjustment while monitoring comparator U511 output relative to its input.

(13) TP600
This test point is connected to the output of DAC threshold comparator U811.It is monitored with respect to +3 VL when adjusting the DAC threshold level. It is located near probe connector J600.

(14) GND
This is a ground test point below and to the left of U115. It is used as a ground reference for comparator offset adjustments.

NOTE

There are many ground test points labeled G or GND on the modules. When performing these adjustments, always use the ground test point specified for the specific test. In most cases, this is the ground test point nearest the active test point.

(15) U115, Pin 2 (91A04A only) (top of R113)
Pin 2 of U115 connects to the outer end of R113 (see inset on Figure 9-1). This test point is used to connect the current source while adjusting clock comparator offset potentiometer R111 on the 91A04A master module.

(16) U121, Pin 13 (91A04A only)
This is the input to clock gate U121, and is connected to the output (pin 7) of probe clock comparator U115. It is monitored relative to U115, pin 2 (input) while adjusting clock comparator offset potentiometer R111.

(17) GND (91A04A only)
This is a ground (G) test point located just to the left of TP125. It is used as a reference for the 3 ns and 5 ns oscillator adjustments and performance checks.

(18) TP125 (91A04A only)
This test point is monitored relative to ground with a frequency counter during the 3 ns and 5 ns oscillator adjustment and performance check procedures. The test point monitors whichever oscillator is selected as the internal clock.

(19) J125, Pin 1
This is the upper pin (nearest the top edge of the board) of J125. It is used as a reference to center the oscilloscope trace prior to comparator offset adjustments when the pulse generator is used as a signal source for the adjustments.

(20) U218, Pins 11 and 24
These test points are used in the channel 0 check of the deskew function during diagnostics. Pin 24 is used to trigger an oscilloscope, and pin 11 is used to observe the deskew staircase waveform.

(21) U218, Pin 1
This is the input to data channel 0 deskew selector U218. It connects to the output (pin 8) of channel 0 comparator U211. This test point is monitored relative to U211 input (pin 2) during channel 0 comparator offset adjustment.

(22) U418, Pins 11 and 24
These test points are used in the channel 1 check of the deskew function during diagnostics. Pin 24 is used to trigger an oscilloscope, and pin 11 is used to observe the deskew staircase waveform.

(23) U418, Pin 1

This is the input to data channel 1 deskew selector U418. It connects to the output (pin 8) of channel 1 comparator U311. This test point is monitored relative to U311 input (pin 2) during channel 1 comparator offset adjustment.

(24) U518, Pins 11 and 24

These test points are used in the channel 2 check of the deskew function during diagnostics. Pin 24 is used to trigger an oscilloscope, and pin 11 is used to observe the deskew staircase waveform.

(25) U518, Pin 1

This is the input to data channel 2 deskew selector U518, and connects to the output (pin 8) of channel 2 comparator U411. This test point is monitored relative to U411 input (pin 2) during channel 2 comparator offset adjusment.

(26) U618, Pins 11 and 24

These test points are used in the channel 3 check of the deskew function during diagnostics. Pin 24 is used to trigger an oscilloscope, and pin 11 is used to observe the deskew staircase waveform.

(27) U618, Pin 1

This is the input to data channel 3 deskew selector U618, and connects to the output (pin 8) of channel 3 comparator U511. This test point is monitored relative to U511 input (pin 2) during channel 3 comparator offset adjustment.

(28) TP821

This test point (+4.2 V) is jumpered to the reset input of flip-flop U448 (TP549) to inhibit the word recognition signal during the high-speed word recognition performance check .

(29) J245 (91A04A only)

This jumper is located above and to the left of the clock and word-recognizer connectors. It turns off U241, U245, U246, and U247 when the 91A04A is used without an expander in the system. Connect it to pins 2 and 3 for 91A04A-only operation, and connect it to pins 1 and 2 if one or more expanders are used.

(30) C332 (91A04A only)

This is the frequency adjustment for the 5 ns oscillator. Make this adjustment while monitoring TP125 with a frequency counter and with the 5 ns clock selected as the 91A04A internal clock.

(31) C335 (91A04A only)

This is the frequency adjustment for the 3 ns oscillator. Make this adjustment while monitoring TP125 with a frequency counter and with the 3 ns clock selected as the 91A04A internal clock.

(32) TP533

This test point (100K Vbb) on the 91A04A is used to center the oscilloscope trace prior to the high-speed setup and hold time performance checks for the 100K ECL ICs used in the 91A04A and 91AE04A modules.

(33) GND

This is the ground (G) test point on the 91A04A located near the lower right corner of U435. It is the ground reference for the high-speed word recognition performance checks fot 91A04A and 91AE04A modules.

(34) U448, Pin 20

This test point on the 91A04A is monitored with an oscilloscope during the high-speed setup and hold time performacne check on the 91A04A. It is also used to center the clock pulse rising edge on the oscilloscope prior to the pulse geometry performance check on 91AE04A word recognizer timing.

(35) U448, Pin 15

This test point on the 91A04A module is used to observe high-speed clock setup and hold times during the word recognition timing performance checks on the 91A04A and 91AE04A module.

(36) TP449

This is the ground (G) test point located just below the lower left corner of U451. This is the ground reference for the oscilloscope during the high-speed clock setup and hold performance checks.

(37) TP549

This test point is connected to the reset input (pin 22) of flip-flop U448. It is jumpered to TP821 (+4.2 V) during the high-speed word recognition performance check to inhibit the word recognition signal.

(38) W642

This is a soldered-in jumper setup just to the left of U548. It is used to select delays in both the 91A04A and 91AE04A modules to compensate for differences in word recognition propagation rates. (Refer to the *Maintenance General Information* section of this addendum for the jumper installation procedure.) See the inset in Figure 9-1 for W642 pin layout.

(39) W150 (91A04A only)

This jumper is placed in the CLK D line to the word recognizer. It is used to add or subtract delay in the line for word recognizer timing. It is located near the upper left corner of U151.

(40) TP641 (SS)

This jumper is located below and to the left of U641. It is jumpered to +4.2 V during word recognizer checks and adjustments to inhibit STOP STORE(H).

(41) TP245

This test point is located just below jumper J245. It is used as a 10K Vbb reference when monitoring the inputs of the 11C01 clock drivers.

(42) W148 (91AE04A only)

This jumper is used on the expander module to change compensation for differences in Vcc (+5 V) between the master and expander modules. Make this adjustment during initial installation.

(43) TP640

This test point is located just to the right of U635. It connects to pin 15, the input of OR gate U641. It disables the word recognizer during high-speed word-recognizer checks and adjustments when jumpered to TP821 (+4.2 V).

I/O MAPS

Table 9-3 lists the I/O ports on the 91A04A and 91AE04A.

Table 9-3
91A04A/91AE04A I/O MAP

I/O Addr (Hex)	R/W	Description	Location
0	W	Memory mapping, register	A26/A28 U678B
0	R	Card ID (83)	A26/A28 U855
1	W	DAC, threshold	A26/A28 U811
1	R	Pod Status bit 0: CLK ARRAY READ(H) bit 1: EN MEM ACCESS(H) bit 2: POD ID(L) bit 3: WC3(H) (diagnostic) bit 4: 5 ns EN(H) bit 5: 91A04 TRIGRD(L) bit 6: POD C PRESENT(L) bit 7: SEL 2 TTL(H)	A26/A28 U658
2	W	Clock select bit 0: 3 ns EN(L) bit 1: 5 ns EN(L) bit 2: 91A08 INT CLK SEL(L) bit 3: (not used) bit 4: SEL PROBE CLK NOT(L) bit 5: SEL PROBE CLK(L) bit 6: (not used) bit 7: TRIG PRESET(H)	A26 U731
2	R	Card MOS status bit 0: 91A04 STOP STORE(H) bit 1: ARM 91A04 TRIG(H) bit 2: always 1 (high) bit 3: (not used) bit 4: MAR OVERFLOW(H) bit 5: DIAG 1(H) bit 6: TTL DELAY DONE(L) bit 7: (not used)	A26/A28 U661

Table 9-3 (cont.)
91A04A/91AE04A I/O MAP

I/O Addr (Hex)	R/W	Description	Location
3	W	LD DELAY 2(L) Load the complement of the delay desired. The LSB of the delay counter = four cycles of delay.	A26 U585
3	R	MAR RD(L) (EN MEM ACCESS(H) set low) Bits 0-7 = MAR bits 0-7	A26/A28 U548, U558, U665
4	W	MEM LD(L) (diagnostic single-step)	A26/A28 U688
4	R	MEM RD(L) (EN MEM ACCESS(H) set high) Bits 0-3: data bits 0-3 Bits 4-7: clock phase 0-3	A26/A28 U548 U558, U665
5	W	LD DELAY 0(L) Load the complement of the delay desired. The LSB of the delay counter = four cycles of delay.	A26 U741
5	R	DIFF 0(L) (Difference counter low byte)	A26 U671
6	W	LD DELAY 1(L) Load the complement of the delay desired. The MSB of the delay counter.	A26 U588, U591
6	R	DIFF 1(L) (Difference counter high byte)	A26 U668
7	W	WRITE DATA(L) (Controls chip enables to the RAMs. Must all be zeros for acquisition) Bits 0-7 = RAM SEL 0(L) - RAM SEL 7(L)	A26/A28 U651

Table 9-3 (cont.)
91A04A/91AE04A I/O MAP

I/O Addr (Hex)	R/W	Description	Location
8	W	WRITE CNTL(L) Bit 0: WC0(H) Bit 1: WC1(H) Bit 2: WC2(H) Bit 3: WC3(H) Channel don't cares. 1= ignore channel for triggering Bit 4: WD0 - Bit 5: WD1 Bit 6: WD2 Bit 7: WD2 Channel triggering control. 0 = compare for zero 1= compare for one	A26/A28 U735
9	W	DESK 1(L) (deskew control reg.) 00: minimum delay EE: maximum delay FF: diagnostic data path Bit 0: Ch 2 bit 0 Bit 1: Ch 2 bit 1 Bit 2: Ch 2 bit 2 Bit 3: Ch 2 bit 3 Bit 4: Ch 3 bit 0 Bit 5: Ch 3 bit 1 Bit 6: Ch 3 bit 2 Bit 7: Ch 3 bit 3	A26/A28 U725

Table 9-3 (cont.)
91A04A/91AE04A I/O MAP

I/O Addr (Hex)	R/W	Description	Location
A	W	DESK 0(L) (deskew control reg.) 00: minimum delay EE: maximum delay FF: diagnostic data path Bit 0: Ch 0 bit 0 Bit 1: Ch 0 bit 1 Bit 2: Ch 0 bit 2 Bit 3: Ch 0 bit 3 Bit 4: Ch 1 bit 0 Bit 5: Ch 1 bit 1 Bit 6: Ch 1 bit 2 Bit 7: Ch 1 bit 3	A26/A28 U225
B	W	TRIG CNTL(L) Bits 0-3: (not used) Bit 4: ARM 91A04 TRIG(H) Bit 5: ARM 91A04 ON 91A32 TRIG(H) Bit 6: (not used) Bit 7: CLEAR TRIG(H)	A26/A28 U738
C	W	MEM CNTL(L) Bit 0: LD ENA CLK PHASE(L) Bit 1: LD MAR(L) Bit 2: LD WRITE EN1(L) Bit 3: LD WRITE EN2(L) Bit 4: LD CLK PHASE(L) Bit 5: EN DELAY COUNTER LD(H) Bit 6:= EN MEM ACCESS(H) Bit 7: EN MEM LD(H)	A26/A28 U745
D	W	HI-Res & ARMs Mode Clock Control Bit 0: (not used) Bit 1: (not used) Bit 2: Hi-res set 0 0=1.5 ns 1=normal mode sampling Bit 3: Hi-res set 1 0=1.5 ns 1=normal mode sampling Bit 4: First CLK (H) enable Bit 5: 91A32 INT CLK (L) enable Bit 6: CLK 1 (L) enable Bit 7: CLK 1 (H) enable	A26/A28 U728

OSCILLOSCOPE TECHNIQUES FOR HIGH-FREQUENCY MEASUREMENTS

Calibrating The Oscilloscope

Equipment Required

1 Tektronix PG502 Pulse Generator, or equivalent.
1 Tektronix SG504 Leveled Sinewave Generator, or equivalent.
1 Tektronix 7904 Oscilloscope Mainframe with a 7A19 Vertical Amplifier, a 7B10 Time Base, and a P6201 X10 FET probe (or equivalent.

Oscilloscope Calibration Procedure

A Tektronix 7904 oscilloscope mainframe with a 7A19 vertical amplifier and a P6201 X10 FET probe typically provides about 500 MHz of bandwidth. The accuracy of the oscilloscope/probe system must be measured at 300-330 MHz in order to calibrate the system for high-freqency measurements in 91A04A and 91AE04A modules. The calibration procedure uses the SG504 sinewave generator connected to the P6201 probe. This procedure enables accurate measurements in the 91A04A clock distribution environment by taking the frequency response of the oscilloscope/probe system into account. Calibrate the oscilloscope/probe system as follows:

1. Set the sinewave generator to 6 MHz and adjust the vertical amplitude to display 7.0 divisions of signal on the oscilloscope.

2. Set the sinewave generator frequency to 300 MHz and note the degradation of the waveform amplitude.

3. Set the sinewave generator frequency to 6 MHz and again establish 7.0 divisions of signal on the oscilloscope.

4. Set the sinewave generator frequency to 330 MHz and again note the amplitude degradation.

5. Check the transient response of the oscilloscope/probe system with a fast squarewave generator setup such as the Tektronix PG502 250 MHz Pulse Generator . Verify that signal aberrations are 12% or less.

NOTE

If the signals at 300 or 330 MHz are degraded 15% or more, or if the squarewave aberrations exceed 12%, the oscilloscope/probe combination requires factory calibration as a unit.

High-Speed Measurement Tips

The following list of suggestions can be helpful in making high-speed measurements:

1. High-speed measurements anywhere on the 91A04A or 91AE04A should be made in a manner similar to the *High-speed Word Recognizer Timing Check* procedure [checks (15) and (16)] in the *Verification and Adjustments* section of this addendum.

The only special consideration when making a measurement of this type is whether the receiver of the signal is a 100K-type device or a 11C01-type device. If it is a 11C01, TP245 should be used as a reference instead of the 100K Vbb

2. The spring clips should always be used when making high-speed measurements with the P6201 probe. In the clock-distribution system, ground test points are placed for convenient use with the spring clips.

CAUTION

Be especially careful to attach the spring clips securely. When improperly connected, they can slip off the ground test point and damage circuit components.

3. When probing a transmission line on the 91A04A or 91AE04A module, make the connection near the driving or receiving end of the line.

4. When probing a 91A04A or 91AE04A which is on a module extender, hold the board carefully by the edge to facilitate use of the P6201 probe with spring clip.

Signal Integrity and Solutions To Violations

The signal integrity of ECL running at 250 MHz or higher is very important for proper operation of 91A04A and 91AE04A modules. Consider the following:

1. The amplitudes of signals at any frequency up to 333 MHz (clock frequencies) should be a clean 320 mV above and 320 mV below the Vbb threshold reference of the receiving component. The maximum signal applied should not exceed 600 mV above the Vbb reference of the receiving component.

2. The signal should not have fuzzy edges or crosstalk problems with adjacent signals.

3. Timing in the clock-distribution and word-recognizer systems is critical. If a high-speed failure is identified in a clock distribution area, the first requirement is to find the earliest faulty signal in the clock-distribution chain. The signals in the flip-flops are at the end of the clock chain and, since this distribution is highly linear at 275 MHz and above, the technique would be to back-track through the 11C01 chain to the source of the fault. Areas of interest in the transmission line media of a driver and receiver are:

   a. Is the termination resistor in good condition; does the coil in the termination peak the falling edge of the waveform?

   b. Is there any unexpected capacitive loading on the transmission line?

   c. Does the rising edge of the waveform have a small slow spot at the top (faulty driver)?

   d. Is there an unexpected reflection in the transmission line, causing failures at specific frequencies.

NOTE

Rising and falling edge investigations are best done at slow (100 ns) internal clock speeds.

e. If the timing is faulty (for example, if the 100131 flip-flop setup or hold is being violated in the word recognizer), first check the propagation delay through the preceding components, then check the transmission line.

SIGNAL GLOSSARY

The following signal glossary is arranged in alphanumeric order. Each entry contains the signal mnemonic and a description of the signal function. Schematic numbers which precede the slash (/), or which have no slash, refer to the 91A04A. Schematic numbers which follow a slash refer to the 91AE04A.

ARM 91A04 ON 91A32 TRIG(H): Generated by the high state of TTL data bit 5 (schematic 52A). ANDed with 91A32 TRIG 0(H) (schematic 57A) in the 91A32 ARMS 91A04 trigger mode to arm the 91A04A trigger circuit.

ARM 91A04 TRIG(H): Generated by the high state of TTL data bit 4 (schematic 52A). Arms the 91A04A trigger circuit (schematic 57A) in the 91A04 ONLY trigger mode.

B RESET(L): Generated by the RESET(L) input from the DAS Controller (schematics 58A/66A). Resets the write-data and memory-control registers (schematics 52A/60A).

BA0-BA12: Buffered address bits 0-12 from the DAS Controller. This is the address input to the controller interface (schematics 51A/59A).

BD0-BD7: Buffered data bits 0-7 on the data bus (schematics 51A, 55A, 58A/59A, 63A, 66A).

BRD(L): Buffered read command from the DAS Controller. With PERSONALITY(L), SEL SLOT(L), BWR(L), and PORT(L), selects and controls the data to be read from the ROMs (schematic 51A)

BWR(L): Buffered write command from the DAS Controller.

CLEAR TRIG ECL(H): Clears and resets 91A04A triggering. Generated by DAS RESET(L) or 91A04 CLEAR TRIG(H) (schematic 58A). Resets data selectors (schematics 53A/61A), MAR overflow register (schematics 54A/62A), start-up circuit (schematic 56A), and trigger circuit (schematic 57A). Sets word recognizer flip-flop (schematic 57A).

CLK 1(L) and CLK 1(H): Clocks from the DAS Trigger/Time Base. Source of the slow-card clock when selected by TTL bits 4-6 (schematic 52A).

CLK A(H), CLK B(H), CLK C(H): Word recognizer clocks (schematics 56A, 57A/65A).

CLK D(H): The delay-counter clock.

CLK ARRAY RD(H): The status of the slow-card clock stored in clock array memories (schematics 54A and 55A). Used to time-correlate 91A04A and slow-card data (schematic 51A).

CLK SEL(L): The control input for clock-select register U731 (schematic 52A).

CP0-CP3(H): Encoded clock-phase bits 0-3 from the eight-phase clock generator (schematic 56A/64A).

DR0-DR3 and DR0-DR7: The data readback signals from acquisition memory (DR0-DR3) and from the MARs (DR0-DR7) (schematics 55A/63A).

D0-D3(H): Data bits 0-3 to the acquisition memory and word recognizer circuitry via the deskew selectors and login registers (schematics 53A/61A). Also, an input to the word recognizer (schematic 57A/65A).

D4(H) and D4(L): Bit 4 from the login latches to the clock array RAMs. Produces Q0-Q3 and DQ0-DQ3 inputs to the clock array RAMs (schematics 54A/55A or 62A/63A).

DELAY 0(L), DELAY 1(L), and DELAY 2(L): The load commands for the upper 1/4 and lower 3/4 delay counters (schematic 57A). Decoded by U688 from BA0(L)-BA3(L) (schematic 51A).

DESK 0(L) and DESK 1(L): Control signals for deskew latches U225 and U725 (schematics 53A/61A).

DESKEW PULSE OUT(H): The deskew output to the P6453 Probe (schematics 51A/59A).

DIAG 1(H): The output from high-resolution register U728 (schematics 52A/60A) to bit 5 on the data bus (schematics 51A/59). Tests U728 during diagnostics.

DIFF 0(L) and DIFF 1(L): Difference 0 and 1 -- Enable tri-state buffers U671 and U668 (schematic 58A) to transmit the difference count to the BD0-BD7 bus.

ECL0-ECL3(H): ECL output bits 0-3 from tri-state buffer U451 (schematics 51A/59A). Data input to the deskew selectors during diagnostics (schematics 53A/61A). Provide input data to the lower 1/4 delay counter (schematic 57A).

ECL0-ECL7: ECL bits 0-7 from tri-state buffer U451 (schematics 51A/59A). Input data for the write enable generator and eight-phase clock generator (schematics 56A/64A), and to acquisition memory (schematics 54A/62A).

EN DELAY COUNTER LD(H): TTL bit 5 of the memory control register. Enables loading of the lower 1/4 delay counter (schematic 57A).

EN MEM LD(H): Gives the DAS Controller access to the clock circuit for slow CPU clocking (schematics 51A, 52A, 56A/59A, 60A, 64A).

EN MEM ACCESS(H): Gives access to the output data from the acquisition memory.

EPC0-EPC3(H): Clock phases 0-3 from the eight-phase clock generator. The clock for data latches 0-3 and MARs 0 and 1 (schematics 54A/62A).

EPC4-EPC7(H): Clock phases 4-7 from the eight-phase clock generator. The clock for data latches 4-7 and MARs 2 and 3 (schematics 55A/63A).

FIRST CLK(H): Clock input from the DAS Trigger/Time Base. Source of slow-card clock when selected by TTL bits 4-6 (schematic 52A).

HIGH RES SET 0(H) and HIGH RES SET 1(H): The S0(H) and S1(H) set signals for the data selectors (schematics 53A/61A). Select high-resolution mode when set low.

HIGH RES(L): The control input to high-resolution register U728 (schematics 52A/60A). Selects the high-resolution mode of data acquisition when active (low).

LD CLK PHASE(L): The load command to the eight-phase clock generator (schematics 56A/64A).

LD EN CLK PHASE(L): The load enable command to the eight-phase clock generator (schematics 56A/64A).

LD MAR(L): The load command for memory address registers U355 and U458 (schematics 54A/62A).

LD WRITE EN 1(L) and LD WRITE EN 2(L): The enabling inputs to write enable generator U251 (schematic 56A/64A).

LOGIN A(H) and LOGIN B(H): The clock inputs to the login registers (schematics 53A/61A). These signals clock data from the deskew selectors through the login registers to acquisition memory.

MA0-MA7: Memory address bits 0-7 from memory address registers 0 and 1 (schematics 54A/62A). Input address to acquisition memories 0 and 1.

MAP 1(L): The Y15(L) output of decoder U688 (schematic 51A). This is the clock to mapping register U678B.

MAR OVERFLOW(H): Asserted high when memory address registers 0 and 1 (schematics 54A/62A) roll over from FF to 00 (hexadecimal). Read by the DAS Controller. If high, the DAS Controller assumes the entire acquisition memory is filled (except location 00), and that the last data stored corresponds to the current data address.

MB0-MB7: Memory address bits 0-7 from memory address registers 2 and 3 (schematics 54A/62A). Input address to acquisition memories 2 and 3.

MC0-MC7: Memory address bits 0-7 from memory address registers 4 and 5 (schematics 55A/63A). Input data to acquisition memories 4 and 5.

MD0-MD7: Memory address bits 0-7 from memory address registers 6 and 7 (schematics 55A/63A). Input address to acquisition memories 6 and 7.

MEM CNTL(L): The control input to memory control register U745 (schematic 52A/60A). Asserted low with address XXXD and BWR(L) low, PORT(L) low, SEL SLOT(L) low, and BRD(L) high.

MEM LD(L): The memory load command (ANDed with EN MEM LD(H) (schematic 56A/64A) to produce the diagnostic single-step clock (write port 04).

MEM/MAR RD(L): Enables the data in acquisition memory, or MAR data, to be read back to the DAS Controller (schematics 51A, 55A/59A, 63A). Reads acquisition memory when EN MEM ACCESS(H) is high, and reads MAR data when EN MEM ACCESS(H) is low.

PERSONALITY(L): A control input from the DAS Controller to which allows the controller to read the 91A04A ROMs.(schematic 51A).

POD C PRESENT(L): Asserted low when a P6453 Probe is connected to the probe connector. The bit-6 input to the pod-status register (schematics 51A/59A).

POD ID(L): Asserted low when a P6453 Probe ID button is pressed. The bit 2 input to the pod-status register (schematics 51A/59A).

PORT(L): A control input from the DAS Controller that identifies the module. Enables decoder U688 when BWR(L) is also asserted low, and generates an enable signal for write buffer U655 for I/O write operations. Also functions with the BRD(L) signal to enable read operations (schematics 51A/59A).

RESET(L): The reset command from the DAS Controller. Produces B RESET(L) and CLEAR TRIG ECL(H) (schematics 58A/66A).

SEL PROBE CLK(L) and SEL PROBE CLK NOT(L): Derived from TTL bits 4 and 5 by clock-select register U731 (schematic 52A). Tells the probe clock receiver (schematic 56A) to select which edge of the probe clock input is active.

SEL SLOT(L): A control input from the DAS Controller (schematics 51A/59A) that indicates that this slot is being written or read.

SEL0-SEL3(H) and SEL4-SEL7(H): The select commands for acquisition memories 0-3 (schematics 54A/62A) and acquisition memories 4-7 (schematics 55A/63A).

START ACQ(H): Enables the start-up circuit (schematic 56A) to begin clocking the selected clock through to the clock drivers.

THRESHOLD(L): Clocks level-setting data into DAC (digital-to-analog converter) U811 (schematics 53A/61A) to establish a threshold level for the signals from the probe. See V THRESHOLD(H).

TRIG CNTL(L): Clocks the trigger-control word through trigger-control register U638 (schematic 52A) to determine arming mode and initialization of word recognizer and trigger delay latches (schematic 57A).

TRIG PRESET(H): Sets the data selectors (schematics 53A/61A) to prevent spurious data login triggering during diagnostics and start-up.

TTL DELAY DONE(L): Generates 91A04 STOP STORE(H) when the upper 3/4 delay counter reaches its terminal count (schematic 57A). Outputs bit 6 on the BD0-BD7 bus to the DAS Controller (schematic 51A).

TTL0-TTL7: TTL data bits 0-7 on the data bus (schematics 51A, 52A, 53A/59A, 60A, 61A).

V THRESHOLD: This is an analog voltage derived by the probe threshold circuit (schematics 53A/61A). Sets the threshold level in the data receivers (schematics 53A/61A) and probe clock receiver (schematic 56A). See also THRESHOLD(H).

WC0-WC3(H): Write-control bits 0-3 from write-control register U735 (schematics 52A/60A). Determine which of the word recognizer bits are to be DON'T CARE (schematics 57A/65A).

WD0-WD3(H): Write-control bits 4-7 from write-control register U735 (schematics 52A/60A). Determine which word satisfies word recognition (schematics 57A/65A).

WE0-WE3(L) and WE4-WE7(H): Write-control bits for acquisiton memories 0-3 and 4-7 (schematics 54A, 55A/62A, 63A).

WR1-WR3(H): Word recognition signals to the 91A04A (schematic 57A) from up to three 91AE04A expander modules (schematic 65A).

WRITE CNTL(L): Clocks data through write-control register U735 (schematics 52A/60A).

WRITE DATA(L): Clocks data through RAM-select register U651 (schematics 52A/60A) to select which RAM is to be written to the DAS Controller).

3 nS EN(H): Enables the internal 3 ns clock oscillator when asserted high (schematic 56A).

5 nS EN(H): Enables the internal 5 ns clock oscillator when asserted high (schematic 56A).

91A04 STOP STORE(H): Produced by the terminal count of the delay counters (schematic 57A). Halts the delay counter and stops the acquisition cycle after three more counts.

91A04 TRGRD(L): Tells the difference counter (schematic 58A) that the 91A04A has triggered; i.e., stops the difference count. The count was started by the slow card trigger (91A32 TRIG 0). 91A04 TRORD (L) also starts the delay count (0 to 32K).

91A08 INT CLK(L) and 91A08 INT CLK(H): The internal clock from the DAS Trigger/Timebase for asynchronous acquisition rates of 100 MHz or less (schematic 56A).

91A08 INT CLK SEL(L): The enable signal for the 91A08 INT CLK at NOR gate U545E (schematic 56A).

91A32 CLK(H): Clock derived from 91A32 INTL CLK(L), the slow card clock (schematic 52A). Clocks the difference counter (schematic 58A) when enabled by 91A32 TRIG 0(H).

91A32 INTL CLK(L): The slow-card clock input from the DAS Trigger/Time Base. Generates 91A32 CLK(H) (schematic 52A).

91A32 TRIG 0(H): Input from the DAS Trigger/Time Base. Starts the difference counter (schematic 58A) and arms the 91A04A trigger circuit (schematic 57A).

91AE04 CLOCK 1-3(H): The clock output from the 91A04A (schematic 56A) to up to three 91AE04A expander modules (schematic 64A).

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

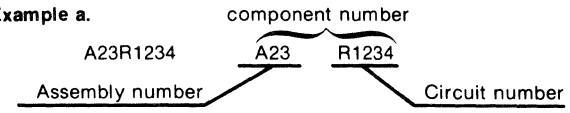
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

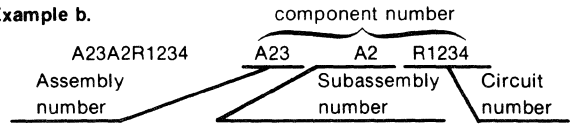
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000IG	FUJITSU-AMERICA INC.	1208 E. ARQUES AVE.	SUNNYVALE, CA 94086
000KD	MITEL SEMICONDUCTOR	18 AIRPORT BLVD.	BROMONT QUEBEC, CANADA J0E1L
000LN	PANASONIC COMPANY DIV OF MATSUSHITA ELECTRIC CORP	ONE PANASONIC WAY	SECAUCUS, NJ 07094
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02763	GRIPPE MACHINING AND MFG. COMPANY	15642 COMMON ROAD	ROSEVILLE, MI 48066
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
07716	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, BURLINGTON DIV.	2850 MT. PLEASANT	BURLINGTON, IA 52601
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
26769	NCI INC.	5900 AUSTRALIAN AVENUE	WEST PALM BEACH, FL 33407
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
32293	INTERSIL, INC.	10900 N. TANTAU AVE.	CUPERTINO, CA 95014
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57924	BOURNS INC NETWORKS DIV 12155	MAGNOLIA AVE	RIVERSIDE, CA 92503
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
98291	SEALECTRO CORP.	225 HOYT	MAMARONECK, NY 10544

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26	670-8077-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	670-8077-00
	----- -----			(91AO4A ONLY)		
A27A1	670-7188-00			CKT BOARD ASSY:DESKEW	80009	670-7188-00
A28	670-8078-00			CKT BOARD ASSY:DATA ACQUISITION	80009	670-8078-00
	----- -----			(91AEO4A ONLY)		
A26	670-8077-00			CKT BOARD ASSY:DATA ACQUISITION MODULE	80009	670-8077-00
	----- -----			(91AO4A ONLY)		
A26B813	321-0724-03			RES.,FXD,FILM:13.6K OHM,0.25W,0.125W	24546	NC55C1362C
A26C101	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C102	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C103	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C105	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C111	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C112	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C117	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C118	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C119	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C120	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C121	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A26C126	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C127	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C130	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A26C131	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C141	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C156	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C161	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C163	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C168	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C173	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C174	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C178	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C182	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C184	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C186	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C187	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C193	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C195	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C201	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C202	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C212	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C213	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C214	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C218	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A26C221	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C236	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C245	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A26C246	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C251	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C301	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C302	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C312	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z

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A26C313	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C322	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C331	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	51642	150 200NP0569C
A26C332	281-0161-00			CAP.,VAR,CER DI:5-15PF,350V	59660	518-000A5-15
A26C335	281-0151-00			CAP.,VAR,CER DI:1-3PF,100V	59660	518 000 A 1.0 3
A26C336	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C342	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C349	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C350	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C351	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C353	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C369	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C382	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C386	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C401	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C402	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C412	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C413	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C414	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C418	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A26C432	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C433	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C459	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C482	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C494	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C498	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C501	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C502	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A26C512	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C513	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C514	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C518	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A26C533	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C547	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C555	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C562	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C572	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C577	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C582	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C591	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C614	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C618	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A26C631	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C632	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C638	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A26C656	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C683	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C724	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A26C726	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C729	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C732	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C740	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C801	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C802	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA

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A26C812	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A26C813	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A26C818	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A26C821	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C857	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C867	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C875	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C895	290-1018-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	000LN	ECEB1AV102SC
A26C901	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A26C904	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A26C907	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	56289	292CC0G471M100B
A26C908	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A26C911	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A26C914	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C917	290-0983-00			CAP.,FXD,ELCTLT:4.7UF,5%,10VDC	56289	150D475X5010A2
A26C919	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	51642	200-050-NP0-101J
A26C930	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A26C932	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A26C939	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A26C948	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A26C949	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C952	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C959	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C961	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C969	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A26C982	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A26C983	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A26C985	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A26CR201	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A26CR301	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A26CR401	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A26CR801	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A26CR802	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A26CR820	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A26CR901	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	04713	1N5817
A26CR904	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	04713	1N5817
A26CR986	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A26I478	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26J125	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26J131	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J135	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J138	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J141	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J143	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J145	131-0265-00			CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
A26J245	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26J245	131-0993-00			BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
A26J433	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26L126	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A26L227	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A26L241	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A26L253	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A26L336	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A26L801	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00

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A26L905	108-0597-00			COIL,RF:TOROIDAL,425UH	80009	108-0597-00
A26Q595	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
A26Q901	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A26Q902	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A26Q922	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A26Q923	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A26Q924	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A26Q930	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A26Q942	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q943	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q944	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q945	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q965	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q966	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A26Q982	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A26R111	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A26R112	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R113	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R114	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R115	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R116	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R120	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A26R121	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A26R122	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R123	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R124	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R126	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R127	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R168	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R172	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R173	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R174	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R175	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R176	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R177	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R178	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R187	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R192	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R194	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R195	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R196	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R197	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R198	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R199	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R201	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A26R202	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R203	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R204	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R205	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R206	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R210	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R222	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R223	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R225	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105

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A26R227	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R231	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R232	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R234	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R235	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A26R241	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R245	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R248	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R253	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R255	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R259	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R268	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R272	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R278	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R284	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R288	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R292	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R299	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R301	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A26R302	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R303	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R304	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R305	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R306	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R310	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R319	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R325	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R331	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R333	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R334	321-0079-00			RES.,FXD,FILM:64.9 OHM,1%,0.125W	91637	MFF1816G64R90F
A26R335	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R336	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R343	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R345	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R347	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R348	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R368	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R379	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R387	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R395	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R397	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R401	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A26R402	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R403	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R404	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R405	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R406	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R410	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R419	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R424	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R425	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R428	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R431	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R438	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02

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A26R441	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R444	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R449	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R450	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R455	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R461	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R471	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R472	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R478	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R479	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R491	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R492	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R496	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R501	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A26R502	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R503	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R504	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A26R505	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A26R506	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A26R510	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R526	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R527	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R528	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R533	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R534	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R535	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R541	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R549	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A26R551	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A26R555	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A26R557	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A26R559	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A26R561	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A26R567	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R569	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R570	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R580	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R581	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R582	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R583	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R586	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R587	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A26R588	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R589	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	57924	4308R-101-101
A26R590	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A26R619	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R624	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R626	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R627	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R628	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R633	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R634	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R635	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R636	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J

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A26R638	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R641	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R642	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R644	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R646	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R648	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A26R658	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R659	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R662	307-0719-00			RES NTWK,FXD,FI:9,1.5K OHM,1%,0.15W EACH	32997	4310R101152F
A26R681	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R695	308-0778-00			RES.,FXD,WW:3 OHM,5%,5W	91637	CW-5-3R000J
A26R715	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R716	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R719	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A26R720	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R729	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A26R732	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R736	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R743	307-0503-00			RES NTWK,THK FI:(9)510 OHM,20%,0.125W	91637	MSP10A01-511G
A26R748	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R785	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26R786	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R787	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R791	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26R792	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26R793	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26R801	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R802	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R809	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A26R812	321-0931-03			RES.,FXD,FILM:1.11K OHM,0.25%,0.125W	91637	MFF1816D11100C
A26R813	321-0931-03			RES.,FXD,FILM:1.11K OHM,0.25%,0.125W	91637	MFF1816D11100C
A26R814	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A26R815	321-0257-09			RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816C46400F
A26R816	321-0257-09			RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816C46400F
A26R817	321-0931-03			RES.,FXD,FILM:1.11K OHM,0.25%,0.125W	91637	MFF1816D11100C
A26R818	311-1859-00			RES.,VAR,NONWIR:TRMR,200 OHM,0.5W,LINEAR	32997	3299X-R27-201
A26R822	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R826	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R829	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R841	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R842	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R846	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R862	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R886	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A26R887	307-0113-00			RES.,FXD,CMPSN:5.1 OHM,5%,0.25W	01121	CB51G5
A26R891	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A26R892	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R904	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R906	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F
A26R907	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A26R917	315-0394-00			RES.,FXD,CMPSN:390K OHM,5%,0.25W	01121	CB3945
A26R923	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A26R924	315-0161-00			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
A26R932	321-1651-04			RES.,FXD,FILM:37.5K OHM,0.1%,0.125W	91637	MFF1816D37501B

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A26R933	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R934	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R935	321-0259-09			RES.,FXD,FILM:4.87K OHM,1%,0.125W	07716	CEAE48700F
A26R936	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A26R937	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A26R941	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R942	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R943	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R944	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R945	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R946	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A26R947	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R948	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R949	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R951	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A26R952	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R953	301-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.50W	01121	EB3615
A26R957	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R958	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R959	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R960	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R961	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R962	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R963	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R964	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R965	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A26R966	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R967	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A26R968	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A26R982	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R985	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A26R987	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A26R992	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26R993	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A26T201	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A26T301	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A26T401	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A26T501	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A26T901	120-1446-00			XFMR,PWR:HF,CONVERTER	80009	120-1446-00
A26TP549	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26TP581	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A26TP918	131-1493-00			CONTACT,ELEC:TEST POINT STRAP	80009	131-1493-00
A26TP919	131-1493-00			CONTACT,ELEC:TEST POINT STRAP	80009	131-1493-00
A26TP924	131-1493-00			CONTACT,ELEC:TEST POINT STRAP	80009	131-1493-00
A26U115	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A26U121	156-1650-00			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-00
A26U125	156-1650-00			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-00
A26U151	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A26U155	156-1022-01			MICROCIRCUIT,DI:8 INPUT PRIORITY ENCODER	04713	MC10165PD/LD
A26U158	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U165	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U171	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U175	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U181	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26U185	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U191	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U198	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A26U211	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A26U218	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A26U225	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U228	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U235	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U241	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U245	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U251	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U258	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U265	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U265	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U275	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U281	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U285	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U291	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U298	156-1578-00			MICROCIRCUIT,DI:ECL		
A26U311	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A26U328	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U341	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U345	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U348	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A26U355	156-1563-00			MICROCIRCUIT,DI:ECL,4-STAGE CNTR/SR	07263	F100136FC
A26U411	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A26U418	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A26U428	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U435	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U448	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U451	156-1515-00			MICROCIRCUIT,DI:9-BIT BUFFER	07263	F100122FC
A26U458	156-1563-00			MICROCIRCUIT,DI:ECL,4-STAGE CNTR/SR	07263	F100136FC
A26U468	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A26U475	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A26U481	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A26U485	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A26U491	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A26U511	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A26U518	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A26U525	156-1496-00			MICROCIRCUIT,DI:QUAD MUX/LATCH	07263	100155FC
A26U531	156-1500-00			MICROCIRCUIT,DI:QUINT EXCL OR/NOR GATE	02763	F100107FC
A26U538	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U545	156-1032-00			MICROCIRCUIT,DI:QUINT 2 OR/NOR	07263	F100102FC
A26U548	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A26U558	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A26U565	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A26U568	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A26U571	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A26U575	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A26U578	156-1044-01			MICROCIRCUIT,DI:4 BIT SYNC BIN CNTR,SCRN	07263	F93S16DCQR
A26U581	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A26U585	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A26U588	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A26U591	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A26U618	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A26U628	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U635	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A26U641	156-1034-00			MICROCIRCUIT,DI:TRIPLE 5 OR/NOR	07263	F100101FC
A26U651	156-1708-00			MICROCIRCUIT,DI:TTL,OCTAL D FF	01295	74273N
A26U655	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U658	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U661	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U665	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U668	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U671	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U675	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A26U678	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A26U681	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A26U685	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A26U688	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02
A26U725	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U728	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U731	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U735	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U738	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A26U741	156-1038-00			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-00
A26U745	156-1708-00			MICROCIRCUIT,DI:TTL,OCTAL D FF	01295	74273N
A26U811	156-1886-00			MICROCIRCUIT,DI:HIGH SPEED MULTR CONV	34335	AM6080APC
A26U818	156-0854-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM308AN
A26U848	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A26U851	156-0230-02			MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A26U855	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U858	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A26U861	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A26U865	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A26U868	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A26U871	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A26U878	160-1701-01			MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1701-01
A26U881	160-1711-02			MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1711-02
A26U901	156-1261-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC78L15ACP
A26U902	156-1261-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC78L15ACP
A26U905	156-1408-00			MICROCIRCUIT,LI:TIMER,LOW POWER	32293	ICM75551PA
A26U921	156-0205-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	04713	MC10102 (P OR L)
A26U931	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A26U991	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A26VR917	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ
A26VR938	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ
A26VR939	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ

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A27A1	670-7188-00			CKT BOARD ASSY:DESKEW	80009	
A27A1C03	290-0308-00			CAP.,FXD,ELCTLT:1UF,20%,35V	26769	40CS105Y035M1C
A27A1R01	317-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.125W	01121	BB8205
A27A1R02	317-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.125W	01121	BB5115
A27A1R03	317-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.125W	01121	BB1215
A27A1R04	317-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.125W	01121	BB5115
A27A1R010	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A27A1R011	317-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.125W	01121	BB5115
A27A1R012	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A27A1R013	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A27A1R014	307-0539-00			RES NTWK,THK FI:(7)510 OHM,10%,1W	01121	208A511
A27A1R020	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A27A1R021	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A27A1S01	260-2072-00			SWITCH,PUSH:SPST,10MA,35VDC,MOMENTARY	31918	532.000.001
A27A1U010	156-1032-00			MICROCIRCUIT,DI:QUINT 2 OR/NOR	07263	F100102FC

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28	670-8078-00			CKT BOARD ASSY:DATA ACQUISITION (91AEO4A ONLY)	80009	670-8078-00
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A28C101	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C102	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C103	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C105	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C117	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C120	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C121	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A28C126	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C127	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C131	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C141	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C148	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C156	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C161	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C163	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C168	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C173	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C174	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C178	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C182	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C184	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C186	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C187	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C193	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C195	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C201	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C202	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C212	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C213	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C214	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C218	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A28C221	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C236	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C246	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C251	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C301	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C302	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C312	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C313	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C322	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C336	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C342	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C349	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C350	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C351	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C353	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C369	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C382	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C386	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C401	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C402	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C412	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28C413	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C414	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C418	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A28C432	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C433	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C436	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	1C10C0G221K200B
A28C439	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C459	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C482	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C494	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C498	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C501	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C502	283-0353-00			CAP.,FXD,CER DI:0.1UF,10%,50V	04222	12105C104KA2075
A28C512	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C513	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C514	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C518	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A28C533	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C547	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C555	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C562	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C572	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C577	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C582	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C591	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C614	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C618	283-0185-00			CAP.,FXD,CER DI:2.5PF,5%,50V	72982	8101B057C0K0295B
A28C631	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C632	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C638	283-0326-00			CAP.,FXD,CER DI:0.082UF,10%,50V	72982	8121N075X7R0823K
A28C656	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C683	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C724	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A28C726	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C729	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C732	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C740	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C801	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C802	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A28C812	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	96733	R2676
A28C813	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A28C818	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710-100NP0101J
A28C821	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C857	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C867	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C875	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C895	290-1018-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	000LN	ECEB1AV102SC
A28C901	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A28C904	283-0164-00			CAP.,FXD,CER DI:2.2UF,20%,25V	04222	SR402E225MAA
A28C907	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	56289	292CC0G471M100B
A28C908	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A28C911	290-0920-00			CAP.,FXD,ELCTLT:33UF,+50-10%,35V	55680	ULB1V330TEAANA
A28C914	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C917	290-0983-00			CAP.,FXD,ELCTLT:4.7UF,5%,10VDC	56289	150D475X5010A2

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28C930	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A28C932	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A28C939	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	2C20Z5U105Z025B
A28C948	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A28C949	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C952	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C959	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C961	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C969	290-0297-00			CAP.,FXD,ELCTLT:39UF,10%,10V	56289	150D396X9010B2
A28C982	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A28C983	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A28C985	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A28CR201	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A28CR301	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A28CR401	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A28CR801	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A28CR802	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A28CR820	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A28CR901	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	04713	1N5817
A28CR904	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	04713	1N5817
A28CR986	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A28L253	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A28L801	108-0088-00			COIL,RF:FIXED,3.35UH	80009	108-0088-00
A28L905	108-0597-00			COIL,RF:TOROIDAL,425UH	80009	108-0597-00
A28Q436	151-0719-00			TRANSISTOR:SILICON,PNP	04713	SPS8226(MPSH81)
A28Q595	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
A28Q901	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A28Q902	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A28Q930	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A28Q982	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A28R146	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A28R147	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A28R148	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A28R168	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R174	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R175	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R176	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R177	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R178	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R187	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R194	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R196	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R197	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R198	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R199	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R201	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A28R202	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R203	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R204	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R205	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R206	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A28R210	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R222	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R232	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105

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A28R248	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R253	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R253	108-0606-00			COIL,RF:37NH	80009	108-0606-00
A28R255	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R258	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R259	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R267	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R268	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R271	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R272	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R278	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R282	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R284	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R286	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R288	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R291	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R292	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R299	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R301	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A28R302	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R303	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R304	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R305	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R306	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A28R310	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R319	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R325	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R335	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R343	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R347	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R348	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R368	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R379	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R387	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R395	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R397	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R401	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A28R402	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R403	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R404	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R405	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R406	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A28R410	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R419	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R424	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R425	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R428	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R431	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R433	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R436	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R439	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A28R440	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R441	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R442	317-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.125	01121	BB1625

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A28R455	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R461	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R471	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R472	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R479	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R491	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R496	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R501	311-1857-00			RES.,VAR,NONWIR:TRMR,200K OHM,0.5W,LINEAR	32997	3299X-R27-204
A28R502	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R503	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R504	321-0751-06			RES.,FXD,FILM:50 OHM,0.25%,0.125W	91637	MFF1816C50R00C
A28R505	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A28R506	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A28R510	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R526	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R527	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R528	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R533	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R534	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R535	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R541	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R549	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A28R551	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A28R555	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A28R557	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A28R559	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A28R561	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A28R567	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R569	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R570	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R580	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R581	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R582	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R586	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R588	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R589	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	57924	4308R-101-101
A28R590	307-0492-00			RES.NTWK,FXD FI:(3)50 OHM,5%,0.125W	91637	CSCO4C01-500J
A28R619	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R624	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R626	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R627	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R628	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R633	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R634	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R635	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A28R636	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R638	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R641	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R644	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R646	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R648	307-0811-00			RES NTWK,FXD,FI:	01121	316T110
A28R658	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R659	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R662	307-0719-00			RES NTWK,FXD,FI:9,1.5K OHM,1%,0.15W EACH	32997	4310R101152F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28R681	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R695	308-0778-00			RES.,FXD,WW:3 OHM,5%,5W	91637	CW-5-3R000J
A28R715	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R716	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R719	317-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.125W	01121	BB5105
A28R720	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R729	108-1148-02			COIL,RF:FIXED,21NH	80009	108-1148-02
A28R732	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R736	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R743	307-0503-00			RES NTWK,THK FI:(9)510 OHM,20%,0.125W	91637	MSP10A01-511G
A28R785	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28R791	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28R792	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28R793	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28R801	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R802	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R809	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A28R812	321-0931-03			RES.,FXD,FILM:1.11K OHM,0.25%,0.125W	91637	MFF1816D11100C
A28R813	321-0724-03			RES.,FXD,FILM:13.6K OHM,0.25W,0.125W	24546	NC55C1362C
A28R814	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A28R815	321-0257-09			RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816C46400F
A28R816	321-0257-09			RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816C46400F
A28R817	321-0931-03			RES.,FXD,FILM:1.11K OHM,0.25%,0.125W	91637	MFF1816D11100C
A28R818	311-1859-00			RES.,VAR,NONWIR:TRMR,200 OHM,0.5W,LINEAR	32997	3299X-R27-201
A28R822	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R826	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R829	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R848	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R862	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R886	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A28R887	307-0113-00			RES.,FXD,CMPSN:5.1 OHM,5%,0.25W	01121	CB51G5
A28R891	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A28R892	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R904	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R906	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F
A28R907	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A28R917	315-0394-00			RES.,FXD,CMPSN:390K OHM,5%,0.25W	01121	CB3945
A28R932	321-1651-04			RES.,FXD,FILM:37.5K OHM,0.1%,0.125W	91637	MFF1816D37501B
A28R933	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R934	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R935	321-0259-09			RES.,FXD,FILM:4.87K OHM,1%,0.125W	07716	CEAE48700F
A28R936	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A28R937	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A28R946	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A28R951	307-0501-00			RES,NTWK,FXD,FI:THICK FILM,(5) 50 OHM,5%	91637	MSP06A01-500J
A28R952	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R953	301-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.50W	01121	EB3615
A28R957	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R958	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R959	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R960	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A28R961	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R962	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A28R966	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28R985	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A28R987	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A28R992	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28R993	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A28T201	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A28T301	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A28T401	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A28T501	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A28T901	120-1446-00			XFMR,PWR:HF,CONVERTER	80009	120-1446-00
A28U151	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A28U155	156-1022-01			MICROCIRCUIT,DI:8 INPUT PRIORITY ENCODER	04713	MC10165PD/LD
A28U158	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U165	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U171	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U175	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U181	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U185	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U191	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U198	156-1501-00			MICROCIRCUIT,DI:HEX D FLIP-FLOP	07263	F100151FL
A28U211	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A28U218	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A28U225	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U251	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A28U258	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U265	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U271	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U275	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U281	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U285	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U291	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U298	156-1845-00			MICROCIRCUIT,DI:ECL,256 X 4 BIT	000IG	MBM100422
A28U311	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A28U328	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A28U341	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A28U345	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A28U348	156-1650-01			MICROCIRCUIT,DI:ECL,DUAL 5-4 INPIT OR/NOR	80009	156-1650-01
A28U355	156-1563-00			MICROCIRCUIT,DI:ECL,4-STAGE CNTR/SR	07263	F100136FC
A28U411	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A28U418	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A28U428	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A28U451	156-1515-00			MICROCIRCUIT,DI:9-BIT BUFFER	07263	F100122FC
A28U458	156-1563-00			MICROCIRCUIT,DI:ECL,4-STAGE CNTR/SR	07263	F100136FC
A28U468	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A28U481	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A28U485	156-1030-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER	80009	156-1030-00
A28U511	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A28U518	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A28U525	156-1496-00			MICROCIRCUIT,DI:QUAD MUX/LATCH	07263	100155FC
A28U531	156-1500-00			MICROCIRCUIT,DI:QUINT EXCL OR/NOR GATE	02763	F100107FC
A28U538	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A28U548	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A28U558	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A28U565	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A28U568	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A28U618	156-1085-03			MICROCIRCUIT,DI:16 INP MULTIPLEXER	80009	156-1085-03
A28U628	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A28U635	156-1031-05			MICROCIRCUIT,DI:ECL,TRIPLE D FLIP FLOP	80009	156-1031-05
A28U641	156-1034-00			MICROCIRCUIT,DI:TRIPLE 5 OR/NOR	07263	F100101FC
A28U651	156-1708-00			MICROCIRCUIT,DI:TTL,OCTAL D FF	01295	74273N
A28U655	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A28U658	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A28U661	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A28U665	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A28U675	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A28U681	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A28U685	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A28U688	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02
A28U725	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U728	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U731	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U735	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U738	156-1646-00			MICROCIRCUIT,DI:CMOS,OCTAL D-TYPE EDGE TRI	000KD	MD74SC374AC
A28U745	156-1708-00			MICROCIRCUIT,DI:TTL,OCTAL D FF	01295	74273N
A28U811	156-1886-00			MICROCIRCUIT,DI:HIGH SPEED MULTR CONV	34335	AM6080APC
A28U818	156-0854-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM308AN
A28U848	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A28U851	156-0230-02			MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	04713	MC10131LD
A28U855	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A28U858	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS
A28U861	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A28U865	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A28U868	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A28U901	156-1261-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC78L15ACP
A28U902	156-1261-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC78L15ACP
A28U905	156-1408-00			MICROCIRCUIT,LI:TIMER,LOW POWER	32293	ICM75551PA
A28U931	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A28U991	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A28VR917	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ
A28VR938	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ
A28VR939	156-1490-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	32293	ICL8069CCSQ
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				CHASSIS PARTS		
U1	155-0251-00			MICROCIRCUIT,LI:ACTIVE DRIVER	80009	155-0251-00
U2	155-0251-00			MICROCIRCUIT,LI:ACTIVE DRIVER	80009	155-0251-00
U3	155-0251-00			MICROCIRCUIT,LI:ACTIVE DRIVER	80009	155-0251-00
U4	155-0251-00			MICROCIRCUIT,LI:ACTIVE DRIVER	80009	155-0251-00
U5	155-0251-00			MICROCIRCUIT,LI:ACTIVE DRIVER	80009	155-0251-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

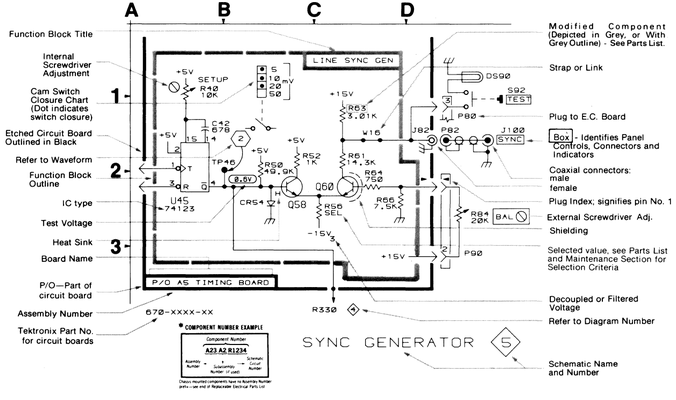
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



INTRODUCTION

This section contains a block diagram showing data flow and interaction of the functional blocks on the 91A04A and 91AE04A Data Acquisition Modules, and set of schematics for each of the two modules. Each schematic is accompanied by a look-up table to aid in the location of components on the schematic, and on the module.

COLORS ON SCHEMATICS

These 91A04A and 91AE04A schematics are color coded for diagnostic functions in a manner similar to the method described in *Section 11* of your *DAS 9100 Series Service Manual*. Minor differences used in the 91A04A/91AE04A scheme are:

- Color coding on the schematics indicates the flow of self-diagnostic tests. In schematics 51A through 66A, all major branches of a line carry the color code of the earliest function which verifies the line, even through all of the major branches may not have been used in that early function. Later functions are indicated by their specific color codes on short segments of the line going to the IC pins. This is done because any solder bridge, stuck bit, or other malfunction on the line will cause a failure indication on the earliest function in which the line is used. For example, on schematic 54A the MA0-MA7 bus was verified by function 1. Therefore, the bus going to U258, U265, and U468 carries the orange code for function 1. The three ICs, however, are not verified until function 4, therefore the individual bits (short line segments) are color coded yellow for function 4.
- When only part of a bus is verified in an early function, the early function is coded only at the IC pin or pins where used. The main bus carries the color code of the first funtion where the entire bus is used. On schematic 54, for example, the EPC0-EPC3 bus is coded yellow (function 4) because only one bit (EPC0) was verified in function 1 (orange).
- Function identification of a line at the edges of a schematics is indicated by the letter F, followed by the numbers of the functions which use that line.

TABLE 11-1
IC Pin Information

Device Type	Vcc or Vdd	GND
100101	9,10	21
100102	9,10	21
100107	9,10	21
100122	4,9,10,16,22	21
100131	9,10	21
100136	9,10	21
100141	9,10	21
100151	9,10	21
100155	9,10	21
100164	9,10	21
100422	9,10	21
10102	1,16	8
10165	1,16	8
11C01	4,5	12
2764	28	16
74273	20	10
74LS00	14	7
74LS08	14	7
74LS138	16	8
74LS139	16	8
74LS154	24	12
74LS193	16	8
74LS240	20	10
74LS244	20	10
74LS393	14	7
74LS74	14	7
74S02	14	7
74S04	14	7
74S05	14	7
74S161	16	8
74SC374	20	10
78L15	--	2
7555	8	1
9685	4,5	12
AM6080APC	20	10
LM308A	7	--
LM339	3	12
LM358	8	4

A26 91A04A DATA ACQUISITION MODULE COMPONENT LOCATIONS.

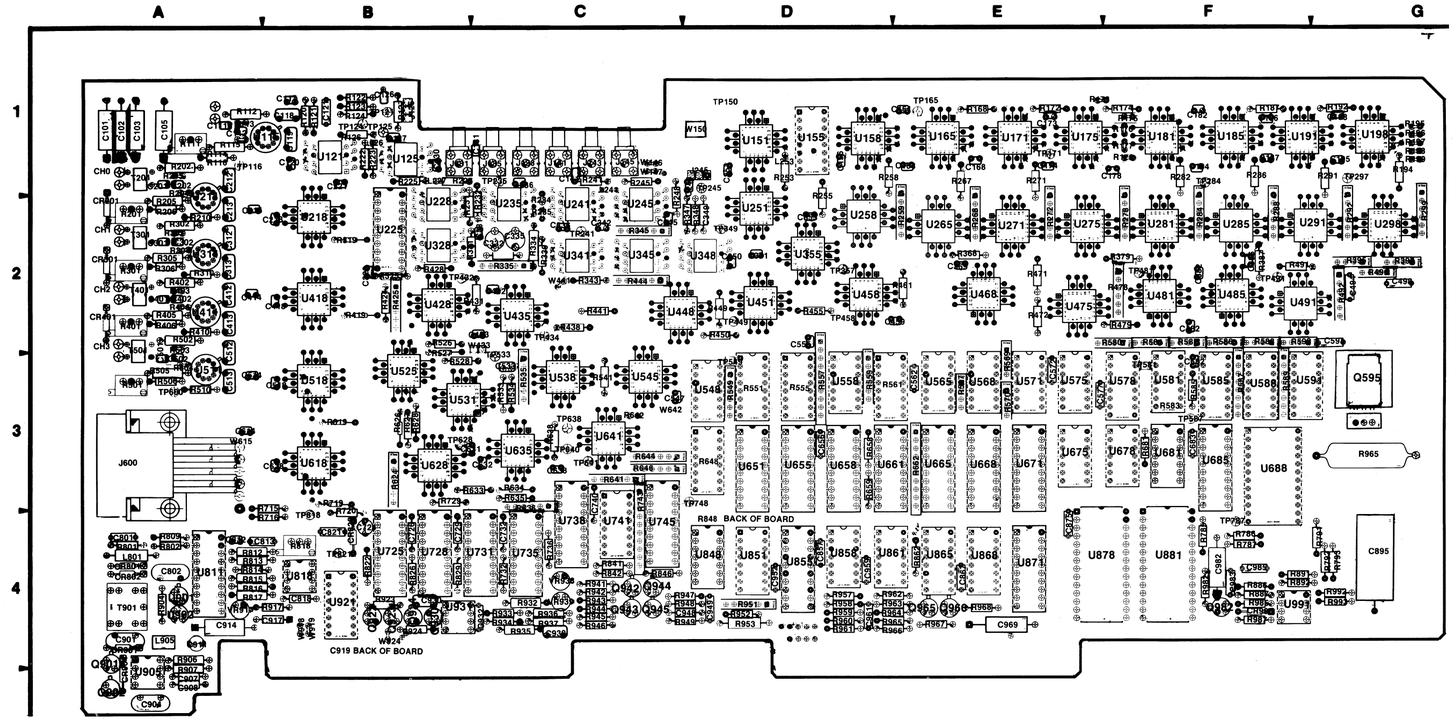
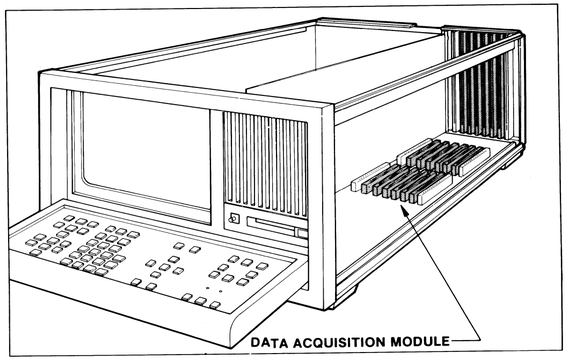


Figure 11-1. A26 91A04A Data Acquisition Module Component Locations.

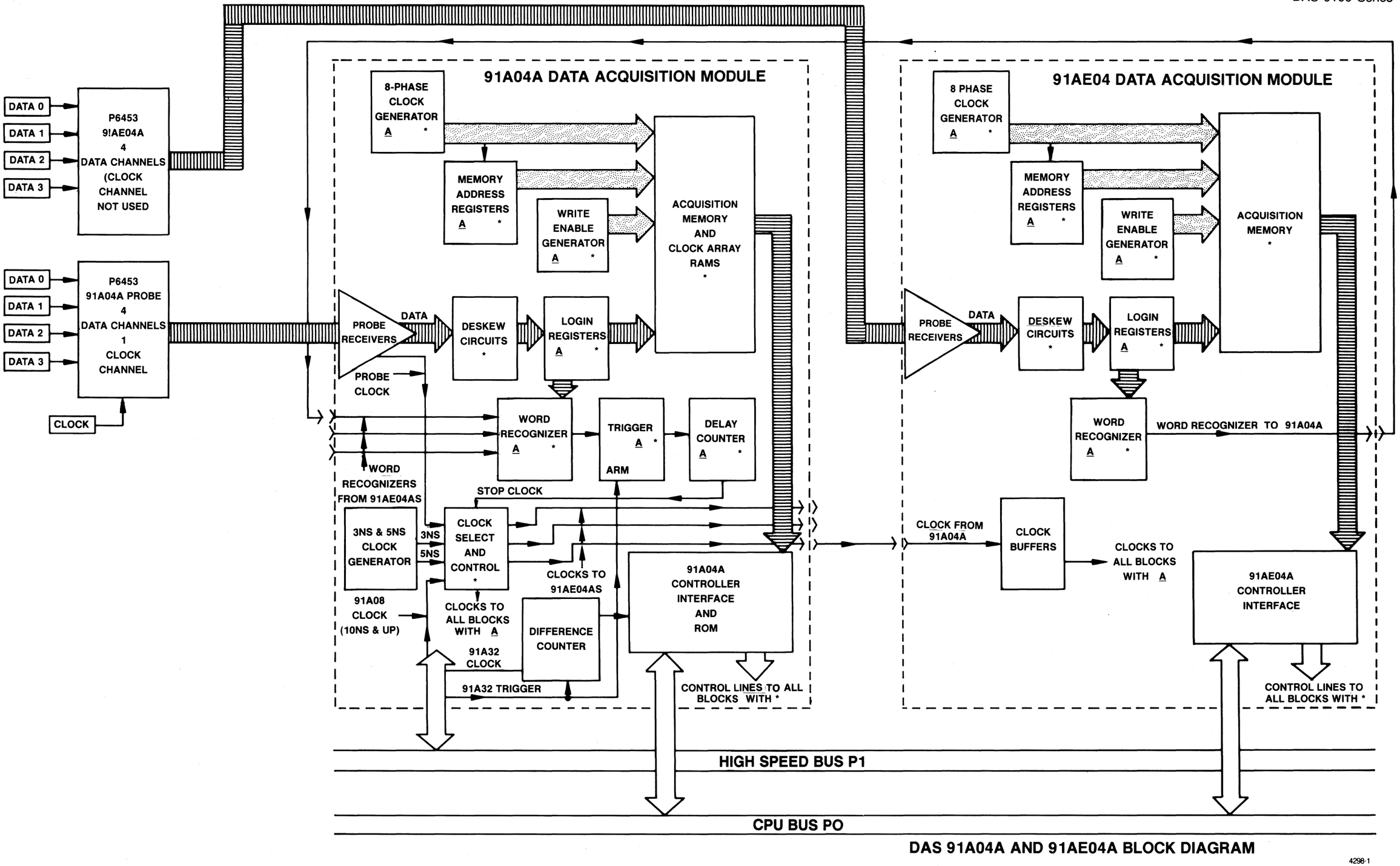


Configuration Guidelines

Module	Max. per Mainframe	Recommended Bus Slot(s)	Functional in Bus Slot(s)	Comments
91A24	1	2-6	1-6	
91AE24	3	2-6	1-6	Will not function without a 91A24 installed
91A04A	1	2-6	1-6	
91AE04A	3	2-6	1-6	Will not function without a 91A04A installed

3836-271

Figure 11-2. A26 91A04A location.



DAS 91A04A AND 91AE04A BLOCK DIAGRAM

4298-1

Table 11-2
91A04A DATA ACQUISITION MODULE 51 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J600	A4	A3	R993	E2	G4
J600	F4	A3	TP458	E5	D2
J600	F1	A3	U451	E4	D2
R555A	E1	D3	U545D	F1	C3
R557	E4	D3	U655	D4	D3
R662F	B4	E3	U661	C4	D3
R681	B3	F3	U678B	D3	F3
R715	B3	A3	U681A	C3	F3
R716	B4	A3	U681B	C3	F3
R743	D5	C3	U685A	D1	F3
R785	E2	F4	U688	E1	F3
R786	D3	F4	U855	E3	D4
R787	D2	F4	U858	B4	D4
R791	F2	G4	U861C	E3	E4
R792	F2	G4	U865	E2	E4
R793	E2	G4	U868	B3	E4
R957	B3	D4	U871	C1	E4
R958	B4	D4	U878	B1	F4
R959	B4	D4	U881	C1	F4
R960	B5	D4	W615	F4	A3
R961	B5	D4	W615	F1	A3
R966	B5	E4	W615	A4	A3
R992	E2	G4			

The colors on this page correspond to the following 91A04A diagnostic functions.

- 0 REG
- 1 MAR
- 2 DELAY CNTR
- 3 DIFF CNTR
- 4 ACQ MEM
- 5 CLK ARRAY
- 6 HIGH RES
- 7 WORD REC
- 8 DESKEW
- 9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

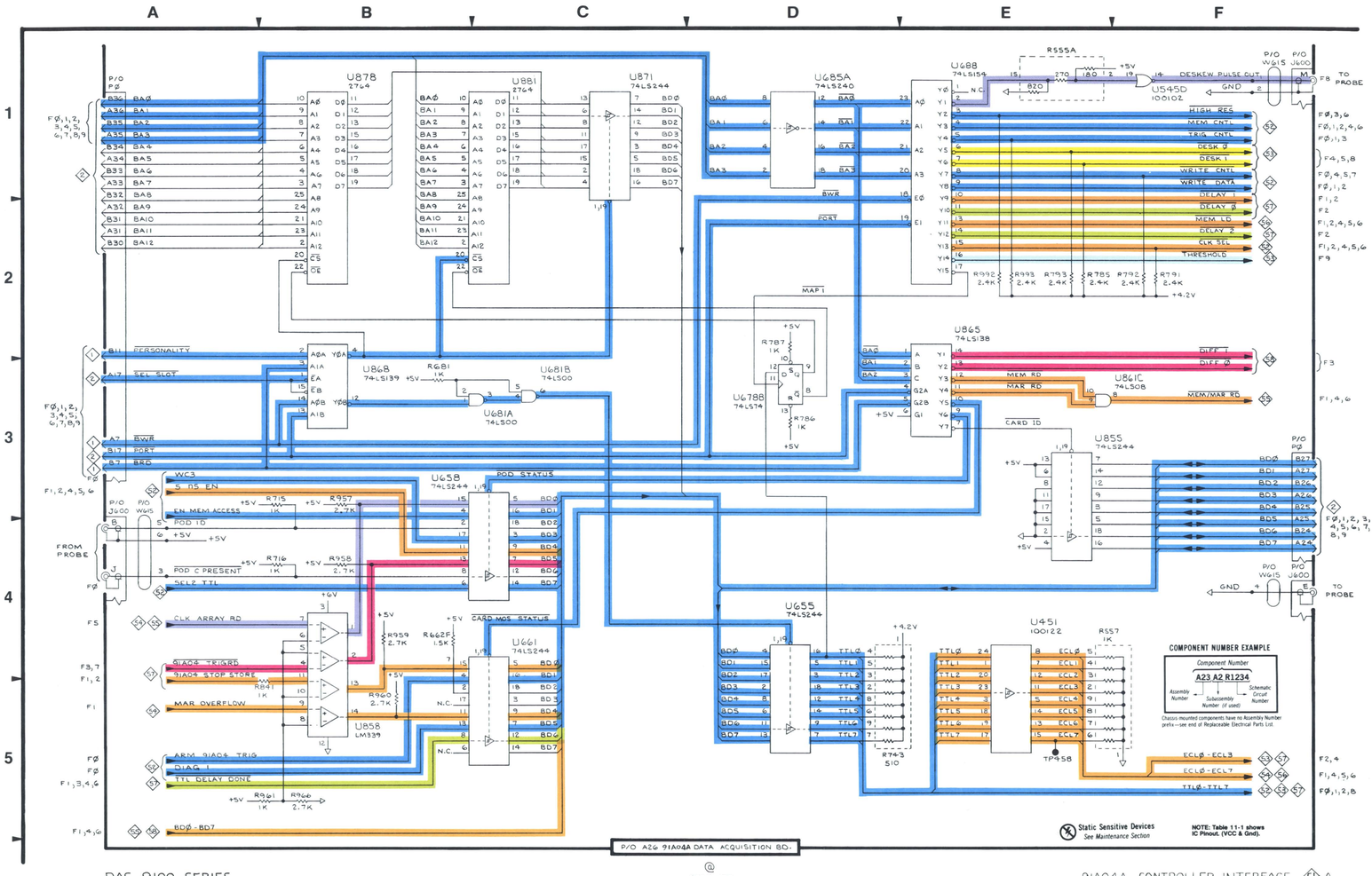


Table 11-3
91A04A DATA ACQUISITION MODULE 52 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C919	B5	B4	R848	C4	D4
R551A	C1	D3	R862	C4	E4
R551B	C1	D3	U651	C1	D3
R551C	E1	D3	U728	B4	B4
R551D	E1	D3	U731	B3	C4
R551E	E1	D3	U735	B1	C4
R551F	E1	D3	U738	D3	C4
R561	C2	E3	U745	D1	C4
R732	B1	C4	U848C	C4	D4
R736	D3	C4	U848E	B4	D4
R743I	C4	C3	U921	C5	B4
R826	B5	B4	W918	B5	B4
R829	B4	B4	W919	B5	B4
			W924	B5	B4

The colors on this page correspond to the following 91A04A diagnostic functions.

0	REG
1	MAR
2	DELAY CNTR
3	DIFF CNTR
4	ACQ MEM
5	CLK ARRAY
6	HIGH RES
7	WORD REC
8	DESKEW
9	DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

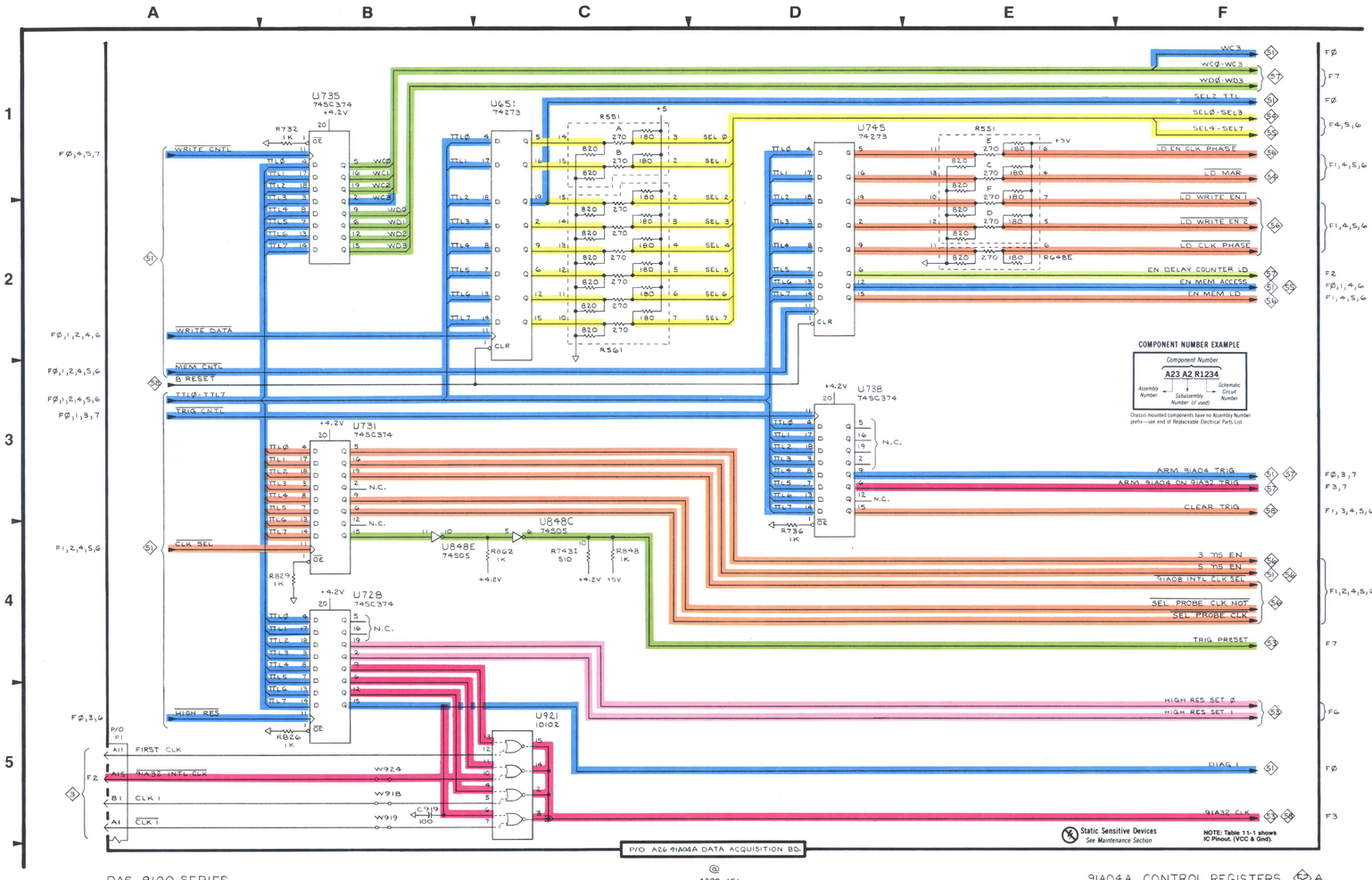


Table 11-4
91A04A DATA ACQUISITION MODULE 53 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C201	A3	A1	R505	B5	A3
C202	B3	A1	R506	B5	A3
C212	B3	A1	R510	B5	A3
C213	B3	A2	R526	E4	B2
C218	D3	B2	R527	C6	B2
C301	A4	A2	R528	C6	B3
C302	B4	A2	R619	E4	B3
C312	B3	A2	R624	F5	B3
C313	B3	A2	R626	D5	B3
C401	A4	A2	R627	D5	B3
C402	B5	A2	R628	F5	B3
C412	B4	A2	R633	E5	C3
C413	B4	A2	R719	F4	B3
C418	E3	B2	R720	E1	B4
C501	A5	A2	R729	D6	B3
C502	B5	A2	R801	B2	A4
C512	B5	A2	R802	B2	A4
C513	B5	A3	R809	B2	A4
C518	F3	B3	R812	B1	A4
C618	F3	B3	R813	B2	A4
C812	B2	A4	R814	A2	A4
C813	C2	B4	R815	A2	A4
C818	B2	B4	R816	B2	A4
C917	A2	B4	R817	B2	A4
J600	A3	A3	R818	C1	B4
R201	B3	A2	R917	B2	B4
R202	B3	A1	R951C	E5	D4
R203	B3	A1	R951D	F5	D4
R204	B3	A1	T201	A3	A1
R205	B3	A2	T301	A3	A2
R206	B3	A2	T401	A4	A2
R210	B3	A2	T501	A5	A2
R301	B4	A2	TP600	C2	A3
R302	B4	A2	U211	B3	A1
R303	B3	A2	U218	D1	B2
R304	B4	A2	U225	C1	B2
R305	B4	A2	U311	B4	A2
R306	B4	A2	U411	B4	A2
R310	B4	A2	U418	D1	B2
R319	D4	B2	U428A	D6	B2
R401	B4	A2	U428C	D5	B2
R402	B4	A2	U511	B5	A3
R403	B4	A2	U518	F1	B3
R404	B5	A2	U525A	D5	B3
R405	B4	A2	U525B	D6	B3
R406	B5	A2	U525C	C5	B3
R410	B4	A2	U525D	C6	B3
R419	D4	B2	U618	F1	B3
R424	C1	B2	U628A	E6	B3
R425B	D5	B2	U628B	F5	B3
R425C	C5	B2	U628C	E5	B3
R425D	C6	B2	U725	E1	B4
R425E	D6	B2	U811	B2	A4
R428	C5	B2	U818	B2	B4
R431	D5	C2	U851A	F5	D4
R501	B5	A3	VR917	A2	A4
R502	B5	A2	W615	A5	A3
R503	B5	A2	W615	A4	A3
R504	B5	A3	W615	A3	A3

DELAY TIMES

DL201A – 0.71 ns
DL301A – 0.59 ns
DL401A – 0.59 ns
DL501A – 0.53 ns

L211A – 0.31 ns
DL311A – 0.31 ns
DL411A – 0.31 ns
DL511A – 0.31 ns

DL211B – 0.400 ns
DL311B – 0.400 ns
DL411B – 0.400 ns
DL511B – 0.400 ns

DL218A – 1.12 ns
DL418A – 1.38 ns
DL518A – 1.34 ns
DL618A – 1.51 ns

DL525A – 0.60 ns
DL525B – 1.50 ns
DL525C – 0.60 ns
DL525D – 1.50 ns

DL428A – 1.24 ns
DL428B – 3.02 ns
DL428C – 0.39 ns
DL428D – 1.24 ns
DL428E – 3.02 ns
DL428F – 0.39 ns

DL628A – 1.19 ns
DL628B – 2.79 ns
DL628C – 0.39 ns
DL628D – 1.19 ns
DL628E – 2.95 ns
DL628F – 0.39 ns
DL628G – 2.05 ns
DL628H – 2.75 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0	REG
1	MAR
2	DELAY CNTR
3	DIFF CNTR
4	ACQ MEM
5	CLK ARRAY
6	HIGH RES
7	WORD REC
8	DESKEW
9	DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

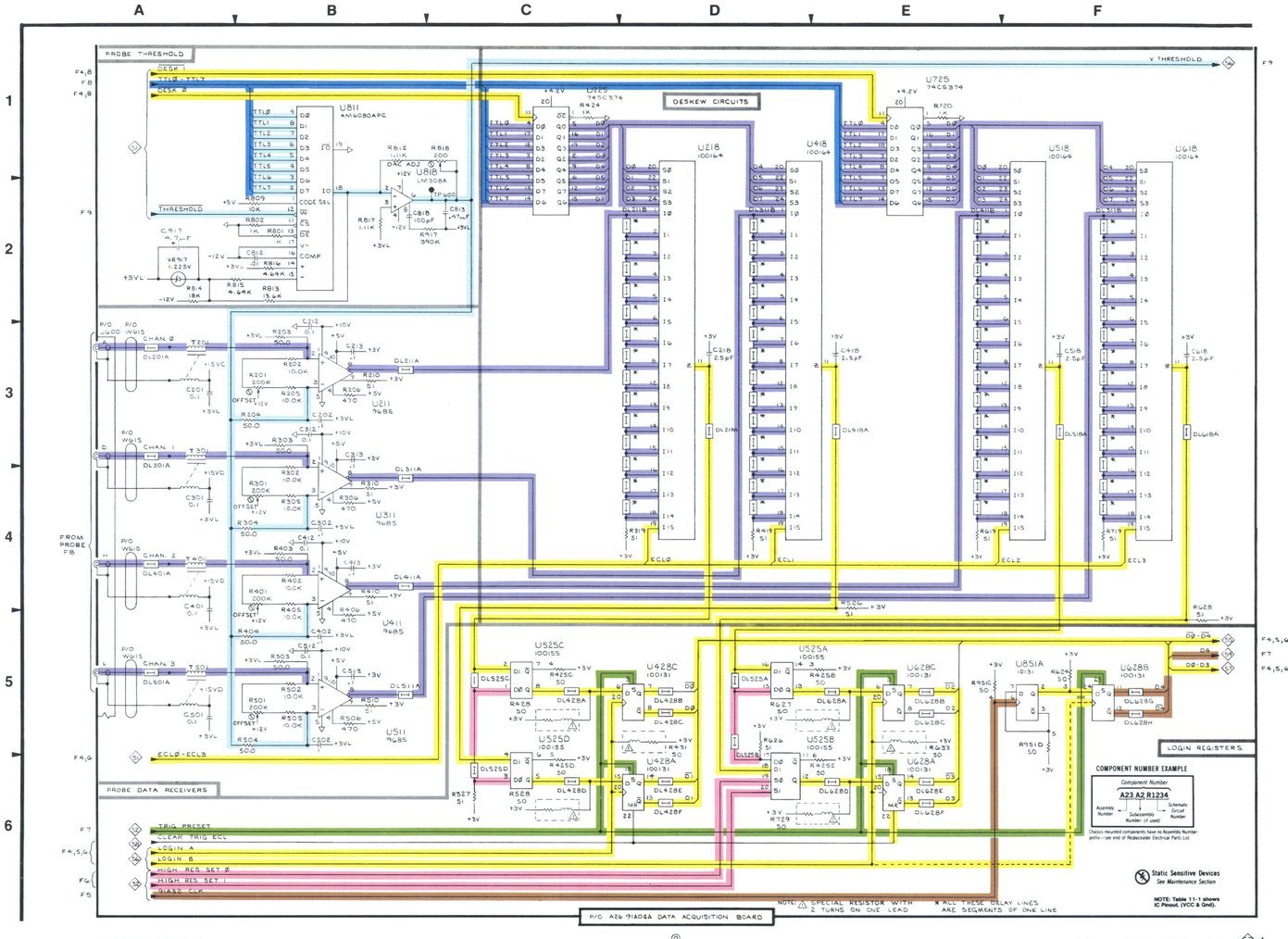


Table 11-5
91A04A DATA ACQUISITION MODULE 54 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R172	B4	E1	R570	B2	E3
R173	B4	E1	R580A	D2	F2
R175	B4	F1	R580B	D2	F2
R176	B3	F1	R580C	D2	F2
R177	B4	F1	R581A	D2	F2
R178	B4	F1	R581B	D2	F2
R255	B4	D1	R581C	D2	F2
R259C	B3	E2	R582B	D1	F2
R259D	C4	E2	R582C	D2	F2
R259E	C4	E2	R951A	B5	D4
R268B	E4	E2	R952	F5	D4
R268C	C3	E2	R962	F5	E4
R268D	C3	E2	R963	F3	E4
R268E	E4	E2	U158	B3	D1
R272B	F4	E2	U165	C3	E1
R272C	E3	E2	U171	D3	E1
R272D	E3	E2	U175	E3	E1
R272E	F4	E2	U258	C1	D2
R278B	F3	F2	U265	C1	E2
R455	B2	D2	U271	E1	E2
R478A	E4	F2	U275	E1	E2
R478B	F4	F2	U355	B1	D2
R478D	B4	F2	U458	B2	D2
R478E	E4	F2	U468	D1	E2
R567	B1	E3	U475	F1	E2
R569B	B2	E2	U851B	F5	D4
R569C	B3	E2			

DELAY TIMES

DL158A - 0.19 ns
DL158B - 0.19 ns
DL158C - 0.19 ns
DL158D - 0.19 ns
DL158E - 0.19 ns

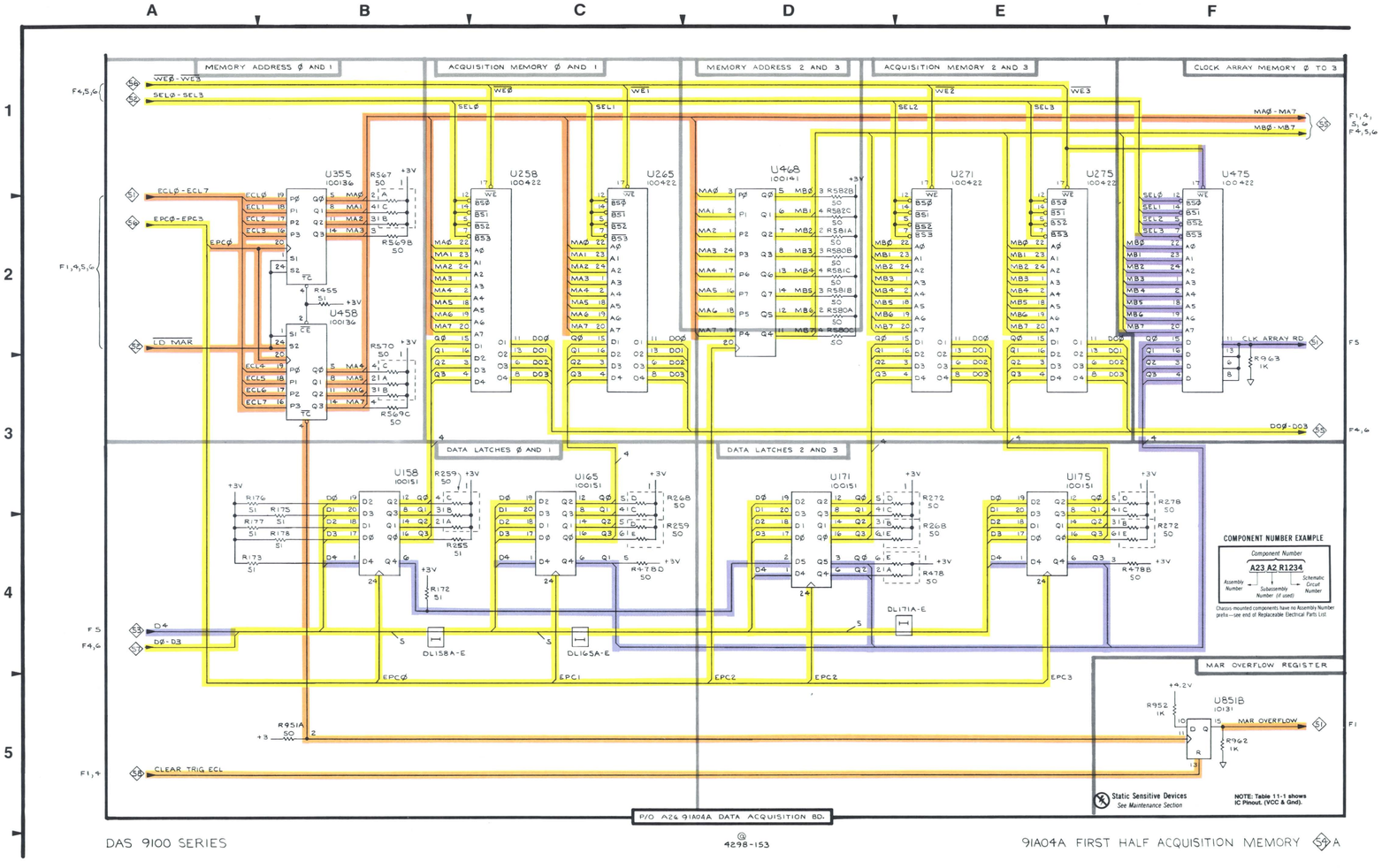
DL165A - 0.19 ns
DL165B - 0.19 ns
DL165C - 0.19 ns
DL165D - 0.19 ns
DL165E - 0.19 ns

DL171A - 0.19 ns
DL171B - 0.19 ns
DL171C - 0.19 ns
DL171D - 0.19 ns
DL171E - 0.19 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 DELAY CNTR
3 DIFF CNTR
4 ACQ MEM
5 CLK ARRAY
6 HIGH RES
7 WORD REC
8 DESKEW
9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.



DAS 9100 SERIES

91A04A FIRST HALF ACQUISITION MEMORY 54 A

Table 11-6
91A04A DATA ACQUISITION MODULE 55 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R192	B4	G1	R559E	C4	D3
R195	A4	G1	R582A	B2	F2
R196	A3	G1	R586A	B1	F2
R197	A3	G1	R586B	B1	F2
R198	A3	G1	R586C	B1	F2
R199	A3	G1	R588A	B2	F2
R278B	B3	F2	R588B	B2	F2
R278E	B3	F2	R588C	B2	F2
R284B	C3	F2	R590B	E4	F2
R284C	B3	F2	R590C	B2	F2
R284D	B3	F2	R658	C5	D3
R284E	C3	F2	R659	C5	D3
R288B	D3	F2	R662A	B5	E3
R288C	C3	F2	R662B	B5	E3
R288D	C3	F2	R662C	B5	E3
R288E	D3	F2	R662D	B5	E3
R292B	D3	G2	R662E	C5	E3
R292B	E3	G2	R662G	C5	E3
R292D	D3	G2	R662H	C5	E3
R292E	E3	G2	R662I	C5	E3
R299	E3	G2	U181	B3	F1
R395A	D1	G2	U185	C3	F1
R395B	D2	G2	U191	D3	F1
R395C	D2	G2	U198	E3	G1
R397A	D2	G2	U281	B1	F2
R397C	D2	G2	U285	C1	F2
R471	D5	E2	U291	E1	G2
R472	D5	E2	U298	E1	G2
R492B	D4	G2	U481	B1	F2
R492C	C4	G2	U485	D1	F2
R492D	D4	G2	U491	E1	F2
R496A	D2	G2	U548	B4	D3
R496B	D1	G2	U558	C4	D3
R496C	D1	G2	U565	D4	E3
R549	A5	D3	U568	E4	E3
R559B	C4	D3	U665	F4	E3
R559C	C4	D3	U848A	A5	D4
R559D	C4	D3	U848B	B5	D4

DELAY TIMES

DL185A - 0.19 ns
DL185B - 0.19 ns
DL185C - 0.19 ns
DL185D - 0.19 ns
DL185E - 0.19 ns

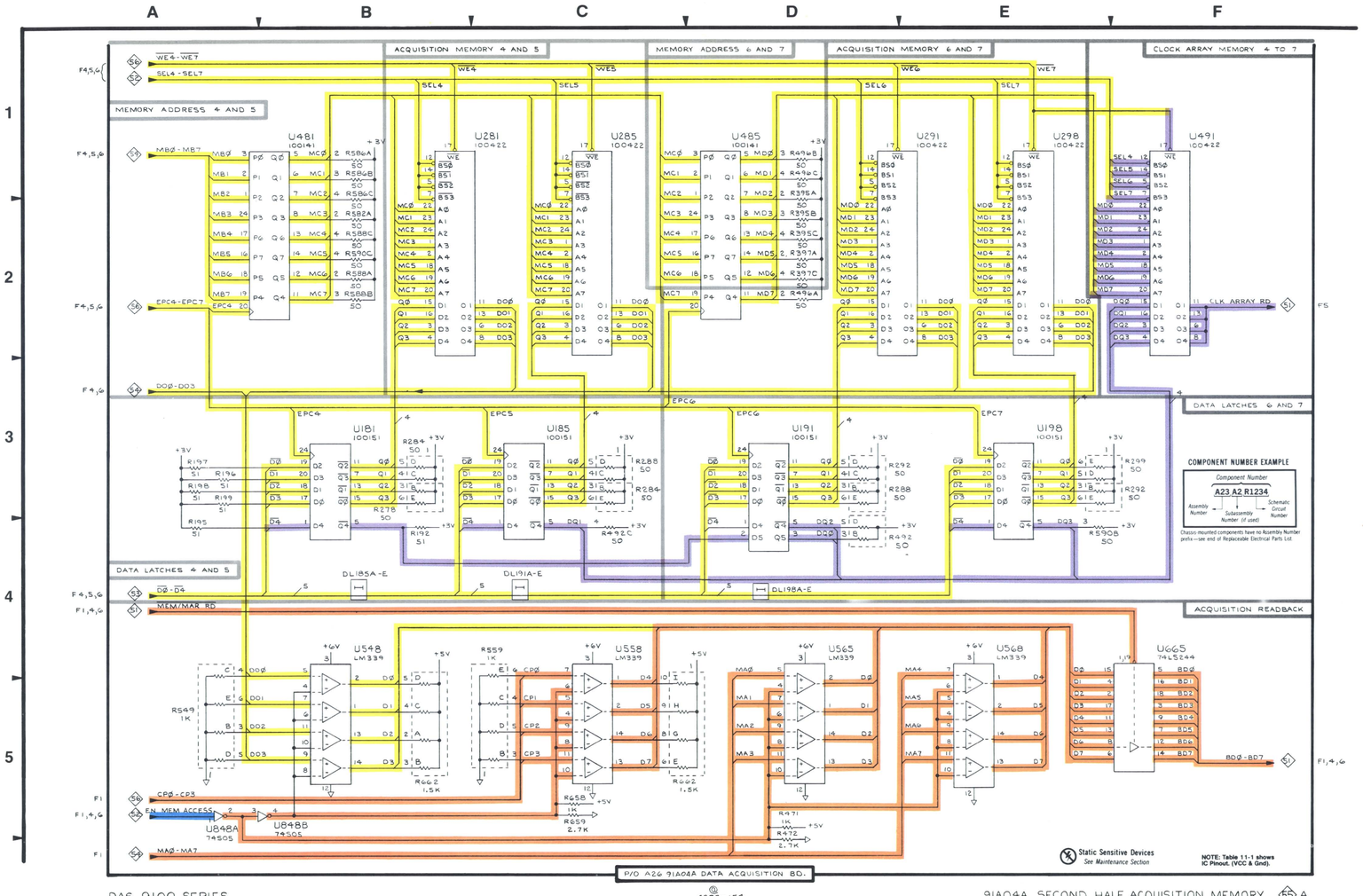
DL191A - 0.19 ns
DL191B - 0.19 ns
DL191C - 0.19 ns
DL191D - 0.19 ns
DL191E - 0.19 ns

DL198A - 0.19 ns
DL198B - 0.19 ns
DL198C - 0.19 ns
DL198D - 0.19 ns
DL198E - 0.19 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 DELAY CNTR
3 DIFF CNTR
4 ACQ MEM
5 CLK ARRAY
6 HIGH RES
7 WORD REC
8 DESKEW
9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.



DAS 9100 SERIES

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91A04A SECOND HALF ACQUISITION MEMORY 55 A

Table 11-7
91A04A DATA ACQUISITION MODULE 56 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C103	A3	A1
C111	A3	A1
C112	B3	A1
C118	B3	B1
C119	B3	B1
C126	E3	B1
C130	D3	B1
C241	F1	C2
C245	E2	C2
C331	F4	C2
C332	B1	C2
C335	B1	C2
C349	E3	D2
C350	E3	D2
C533	C3	C3
J125	E3	B1
J131	F1	B1
J135	F1	C1
J138	F2	C1
J245	E2	D1
J600	A3	A3
L126	C1	B1
L227	C1	B1
L241	E1	C1
L253	B3	D1
P1	A1	E4
Q922	A1	B4
Q923	A1	B4
Q924	B1	B4
R111	A3	A1
R112	A3	A1
R113	A3	A1
R114	B3	A1
R115	B3	A1
R116	B3	A1
R120	B2	B1
R121	B3	B1
R122	D2	B1
R123	D3	B1
R124	C2	B1
R126	C1	B1
R127	B3	B1
R168	D4	E1
R174	D4	F1
R187	D4	F1
R194	D4	G1
R222	E3	B1
R223	B3	B1
R225	B1	B1
R227	C1	B1
R231	B1	B2
R232	F4	C1
R234	B1	C1
R235	B1	C2
R245	E1	C1
R248	E3	C1
R253	B3	D1
R258	B4	D1
267	B4	E1
R271	B4	E1
R282	B4	F1
R286	B5	F1
R291	B5	G1
R325	E4	B2
R331	C1	C2
R333	B1	C2
R334	B1	C2
R335A	D1	C2
R335B	F4	C2
R335C	D1	C2
R335D	F4	C2
R335E	F4	C2
R336	F2	C2
R343	E4	C2
R345A	E2	C2
R345B	E2	C2
R345D	E1	C2
R345E	E1	C2
R347	D3	D2
R348	D3	D2

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R368	D4	E2
R379	D4	F2
R387	D4	F2
R438	D2	C2
R441	D1	C2
R461	D4	E2
R479	B4	F2
R491	B5	F2
R533	C3	C3
R534	D3	C3
R646E	B1	C3
R648A	B2	D3
R648B	B2	D3
R923	A1	B4
R924	B1	B4
TP121	B3	B1
TP125	C1	B1
TP245	E3	D1
TP533	D3	C2
U115	B3	B1
U121	C2	B1
U125	D2	B1
U151	C4	D1
U155	E4	D1
U228A	F4	B2
U228B	C1	B2
U235B	B1	C2
U241	E1	C2
U245	E2	C2
U251	B4	D2
U328	E4	B2
U341	E2	C2
U345	E3	C2
U348	D3	D2
U435A	D1	C2
U435B	D1	C2
U435C	D1	C2
U545C	C2	C3
U545E	B1	C3
U861A	B2	E4
W146	F2	C1
W147	F2	C1
W433	D2	C2
W441	F2	C2
W615	A3	A3

DELAY TIMES

DL103A - TBD

DL115A - 0.08 ns
DL115B - 0.12 ns

DL121A - 0.06 ns

DL125A - 0.55 ns
DL125B - 1.48 ns

DL151A - 0.37 ns
DL151B - 0.66 ns
DL151C - 0.81 ns
DL151D - 0.94 ns
DL151E - 1.27 ns
DL151F - 1.58 ns
DL151G - 1.80 ns
DL151H - 1.91 ns

DL241A - 0.42 ns
DL241B - 0.61 ns

DL245A - 0.15 ns
DL245B - 0.27 ns
DL245C - 0.46 ns
DL245D - 1.84 ns
DL245E - 0.08 ns

DL251A - 0.81 ns
DL251B - 1.08 ns
DL251C - 1.25 ns
DL251D - 1.58 ns
DL251E - 1.83 ns
DL251F - 1.58 ns
DL251G - 1.80 ns
DL251H - 3.16 ns

DL328A - 0.59 ns
DL328B - 0.93 ns

DL341A - 1.77 ns
DL341B - 1.77 ns
DL341C - 0.25 ns
DL341D - 2.20 ns

DL345A - 0.90 ns
DL345B - 0.92 ns
DL345C - 1.75 ns

DL348A - 0.21 ns

DL435A - 0.21 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 DELAY CNTR
3 DIFF CNTR
4 ACQ MEM
5 CLK ARRAY
6 HIGH RES
7 WORD REC
8 DESKEW
9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

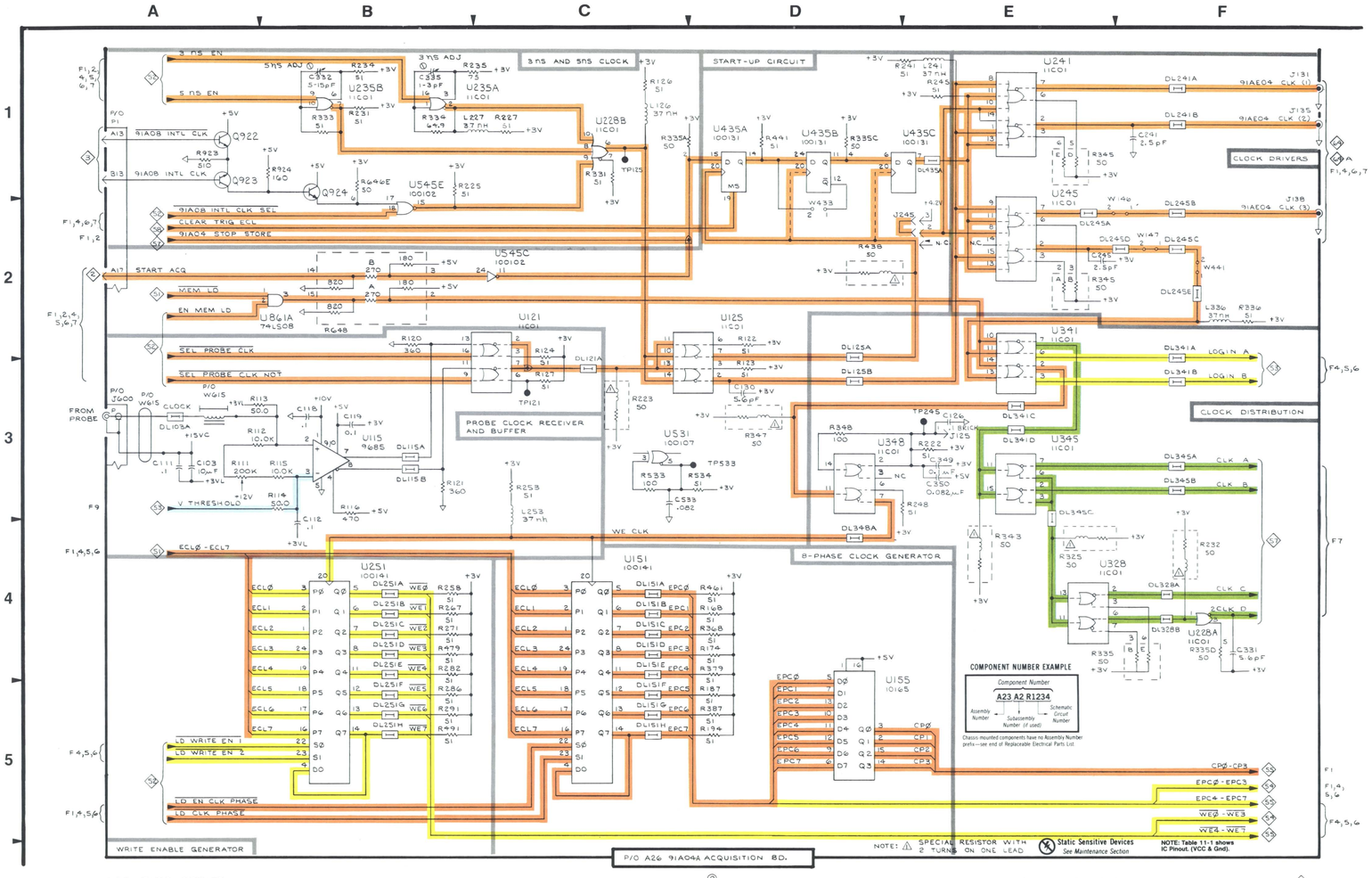


Table 11-8
91A04A DATA ACQUISITION MODULE 57 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C961	E1	D4	642	E3	C3
J141	A4	C1	R644A	E3	C3
J143	A4	C1	R644B	E2	C3
J145	A4	C1	R644C	E3	C3
Q965	F2	E4	R644D	C3	C3
Q966	E2	E4	R644E	E3	C3
R444B	D2	C2	R646B	C3	C3
R444D	D2	C2	R646C	C3	C3
R444E	E3	C2	R646D	E3	C3
R449	C2	D2	R648	C1	D3
R450	D2	D2	R951B	E1	D4
R535A	B2	C3	R951E	D3	D4
R535B	B2	C3	R964	E1	E4
R535C	C2	C3	R965	F2	E4
R535D	B2	C3	R967	F2	E4
R535E	B2	C3	R968	E1	E4
R541	B2	C3	R982	F4	F4
R555D	F3	D3	TP549	D2	D2
R555E	C2	D3	TP581	F3	F3
R587B	E4	F3	TP640	C3	C3
R587C	E4	F3	TP641	E2	C3
R587D	F4	F3	U448A	D2	C2
R587F	F5	F3	U448B	D1	C2
R587G	F5	F3	U448C	D1	C2
R589B	E5	F3	U531	B2	B3
R589C	E5	F3	U538	C2	C3
R589D	F5	F3	U545A	D2	C3
R624A	B2	B3	U545B	E1	C3
R624C	B2	B3	U585	E4	F3
R624D	B2	B3	U588	E4	F3
R624E	B2	B3	U591	F4	F3
R634	D4	C3	U635A	D3	C3
R635	D3	C3	U635B	C3	C3
R636B	C3	C3	U641A	E3	C3
R636C	C3	C3	U641B	C3	C3
R636D	D3	C3	U641C	E2	C3
R638	B3	C3	U741	E1	C4
R641A	E2	C3	U848F	C1	D4
R641B	C3	C3	U861B	C1	E4
R641C	C3	C3	U861D	B1	E4
R641E	C2	C3	W150	B1	D1
			W642	D3	C3

DELAY TIMES

DL228A - 1.94 ns
DL228B - 1.90 ns

DL448A - 0.28 ns

DL531A - 0.81 ns
DL531B - 0.81 ns
DL531C - 0.86 ns
DL531D - 0.83 ns
DL531E - 1.60 ns
DL531F - 1.55 ns
DL531G - 1.30 ns
DL531H - 1.60 ns

DL538A - 0.49 ns
DL538B - 0.49 ns
DL538C - 0.49 ns
DL538D - 0.49 ns

DELAY TIMES

DL635A - 0.97 ns
DL635B - 1.20 ns

DL641A - 2.50 ns
DL641B - 0.97 ns
DL641C - 0.97 ns
DL641D - 0.97 ns
DL641E - 0.08 ns

DL642A - 0.40 ns
DL642B - 0.40 ns
DL642C - 0.60 ns
DL642D - 0.20 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

	0 REG
	1 MAR
	2 DELAY CNTR
	3 DIFF CNTR
	4 ACQ MEM
	5 CLK ARRAY
	6 HIGH RES
	7 WORD REC
	8 DESKEW
	9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

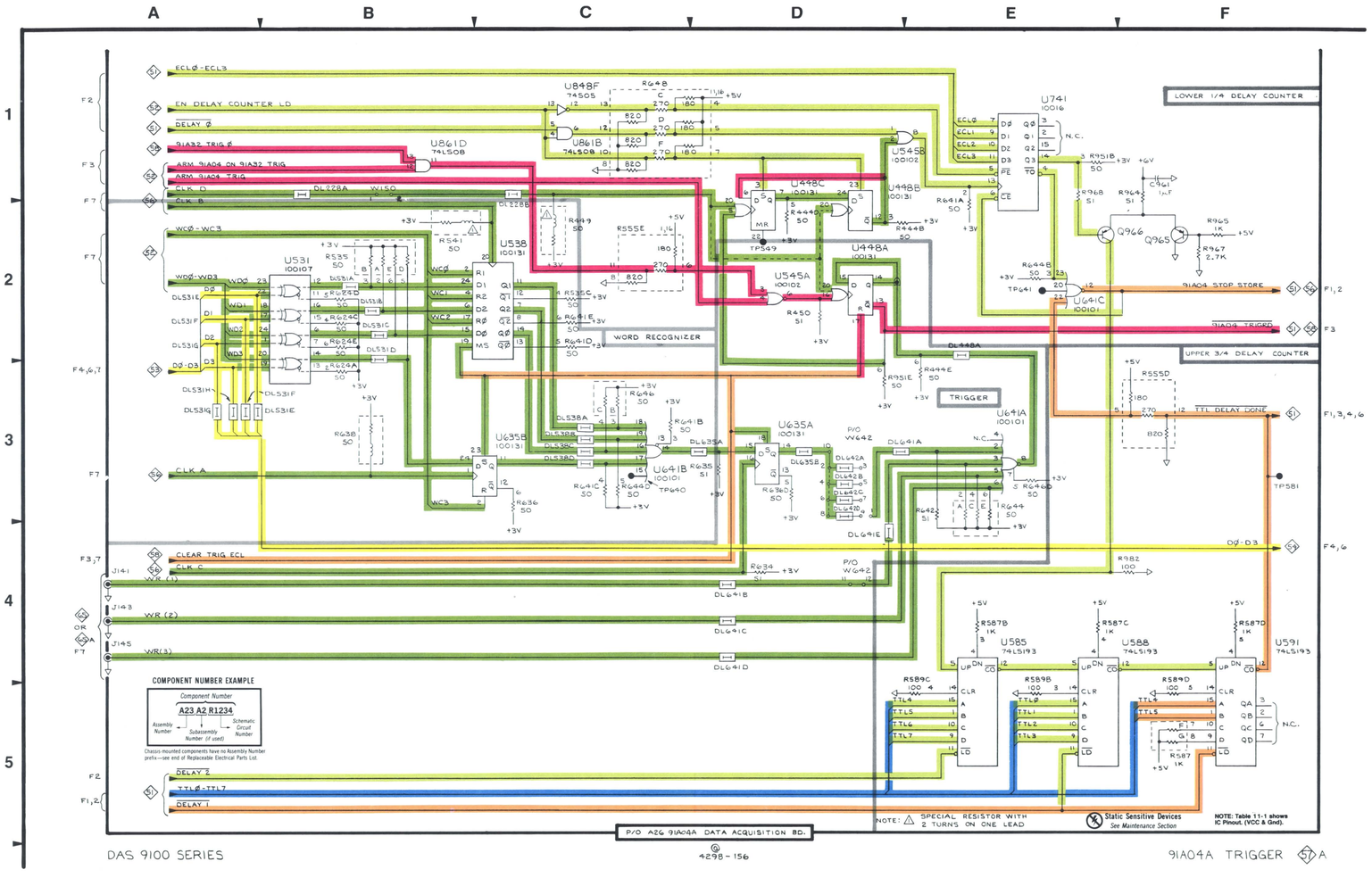


Table 11-9

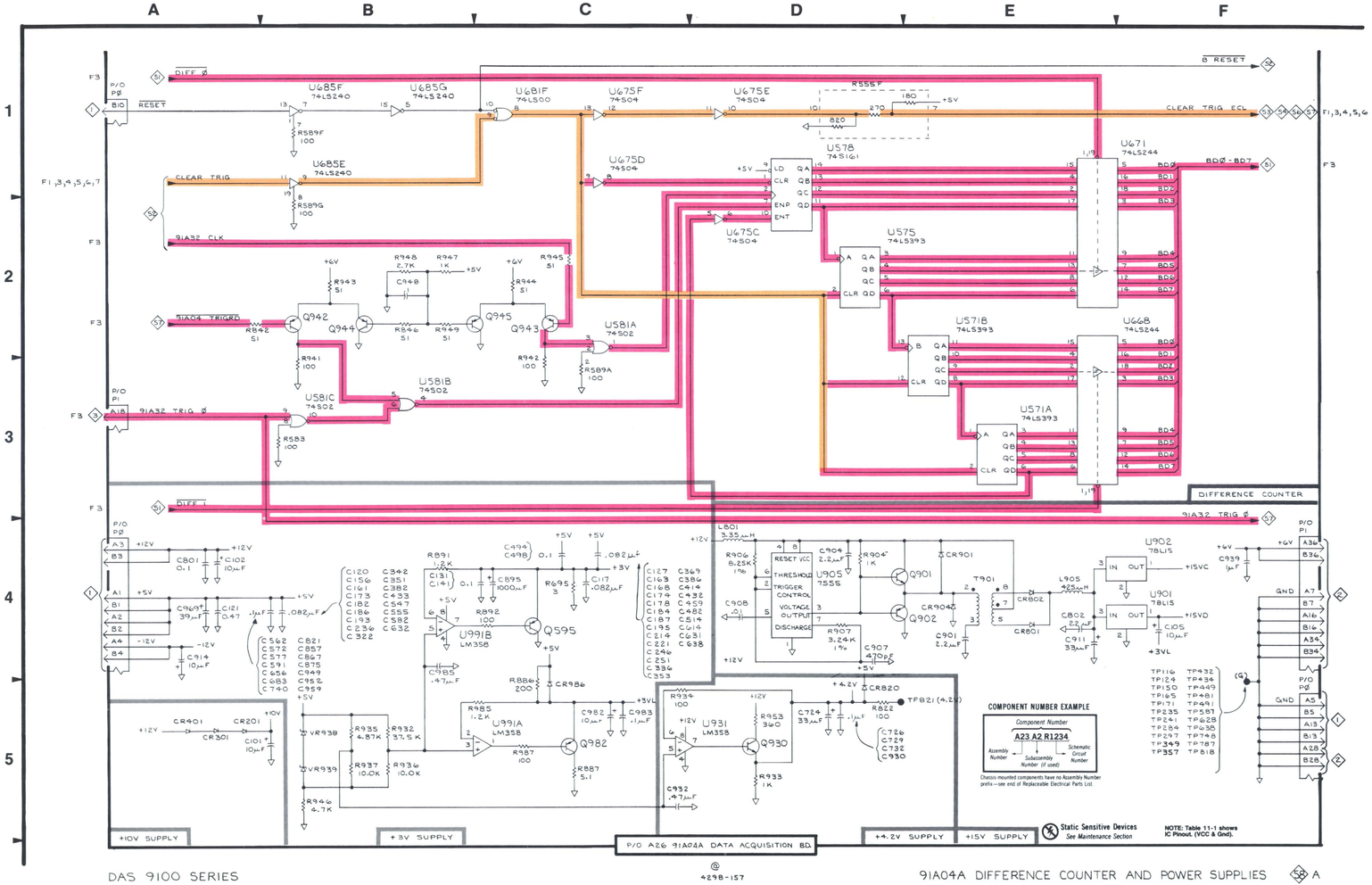
91A04A DATA ACQUISITION MODULE 58 A ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C101	B5	A1	C857	B4	D4	R934	C5	C4
C102	A4	A1	C867	B4	E4	R935	B5	C4
C105	F4	A1	C875	B4	E4	R936	B5	C4
C117	C4	B1	C895	C4	G4	R937	B5	C4
C120	B4	B1	C901	E4	A4	R941	B3	C4
C121	A4	B1	C904	D4	A4	R942	C3	C4
C127	C4	B1	C907	D4	A4	R943	B2	C4
C131	C4	C1	C908	D4	A4	R944	C2	C4
C141	C4	C1	C911	E4	A4	R945	C2	C4
C156	B4	D1	C914	A4	A4	R946	B5	C4
C161	B4	E1	C930	D5	B4	R947	B2	D4
C163	C4	E1	C932	C5	C4	R948	B2	D4
C168	C4	E1	C939	F4	C4	R949	B2	D4
C173	B4	E1	C948	B2	D4	R953	D5	D4
C174	C4	E1	C949	B4	D4	R985	C5	F4
C178	C4	F1	C952	B4	D4	R987	C5	F4
C184	B4	F1	C959	B4	D4	T901	E4	A4
C184	C4	F1	C969	A4	E4	TP116	F5	A1
C186	B4	F1	C982	C5	F4	TP124	F5	B1
C187	C4	F1	C983	C5	F4	TP150	F5	D1
C193	B4	G1	C985	B4	F4	TP165	F5	E1
C195	C4	G1	CR201	A5	A2	TP171	F5	E1
C214	C4	A2	CR301	A5	A2	TP235	F5	C1
C221	C4	B1	CR401	A5	A2	TP241	F5	C2
C236	B4	C1	CR801	E4	A4	TP284	F5	F1
C246	C4	D1	CR802	E4	A4	TP297	F5	G1
C251	C4	D1	CR820	D5	B4	TP349	F5	D2
C322	B4	B2	CR901	E4	A4	TP357	F5	D2
C336	C4	C2	CR904	E4	A4	TP432	F5	B2
C342	B4	C2	CR986	C5	F4	TP434	F5	C2
C351	B4	D2	L801	D4	A4	TP449	F5	D2
C353	C4	D2	L905	E4	A4	TP481	F5	F2
C369	C4	E2	P0	A1	B4	TP491	F5	F2
C382	B4	F2	P0	F5	B4	TP587	F5	F3
C386	C4	F2	P0	A4	B4	TP628	F5	B3
C414	C4	A2	P1	A3	E4	TP638	F5	C3
C432	C4	C2	P1	F4	E4	TP748	F5	D3
C433	B4	C2	Q595	C4	G3	TP787	F5	F4
C459	C4	E2	Q901	E4	A4	TP818	F5	B4
C482	C4	F2	Q902	E4	A4	TP821	D5	B4
C494	C4	G2	Q930	D5	B4	U571A	E3	E3
C498	C4	G2	Q942	B2	C4	U571B	E2	E3
C514	C4	A3	Q943	C2	C4	U575	D2	E3
C547	B4	C3	Q944	B2	C4	U578	D1	F3
C555	B4	D2	Q945	C2	C4	U581A	C2	F3
C562	B4	E3	Q982	C5	F4	U581B	B3	F3
C572	B4	E3	R555F	D1	D3	U581C	B3	F3
C577	B4	F3	R583	B3	F3	U668	E2	E3
C582	B4	F3	R589A	C3	F3	U671	E1	E3
C591	B4	G2	R589F	B1	F3	U675C	D2	E3
C614	C4	A3	R589G	B2	F3	U675D	C1	E3
C631	C4	B3	R695	C4	G3	U675E	D1	E3
C632	B4	C3	R822	D5	B4	U675F	C1	E3
C638	C4	C3	R842	A2	C4	U681F	C1	F3
C656	B4	D3	R846	B2	C4	U685E	B1	F3
C683	B4	F3	R886	C5	F4	U685F	B1	F3
C724	D5	B4	R887	C5	F4	U685G	B1	F3
C726	D5	B4	R891	B4	F4	U901	F4	A4
C729	D5	B4	R892	C4	F4	U902	F4	A4
C732	D5	C4	R904	D4	A4	U905	D4	A4
C740	B4	C3	R906	D4	A4	U931	C5	B4
C801	A4	A4	R907	D4	A4	U991A	C5	F4
C802	E4	A4	R932	B5	C4	U991B	B4	F4
C821	B4	B4	R933	D5	C4	VR938	B5	C4
						VR939	B5	C4

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 DELAY CNTR
3 DIFF CNTR
4 ACQ MEM
5 CLK ARRAY
6 HIGH RES
7 WORD REC
8 DESKEW
9 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.



DAS 9100 SERIES

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91A04A DIFFERENCE COUNTER AND POWER SUPPLIES 58 A

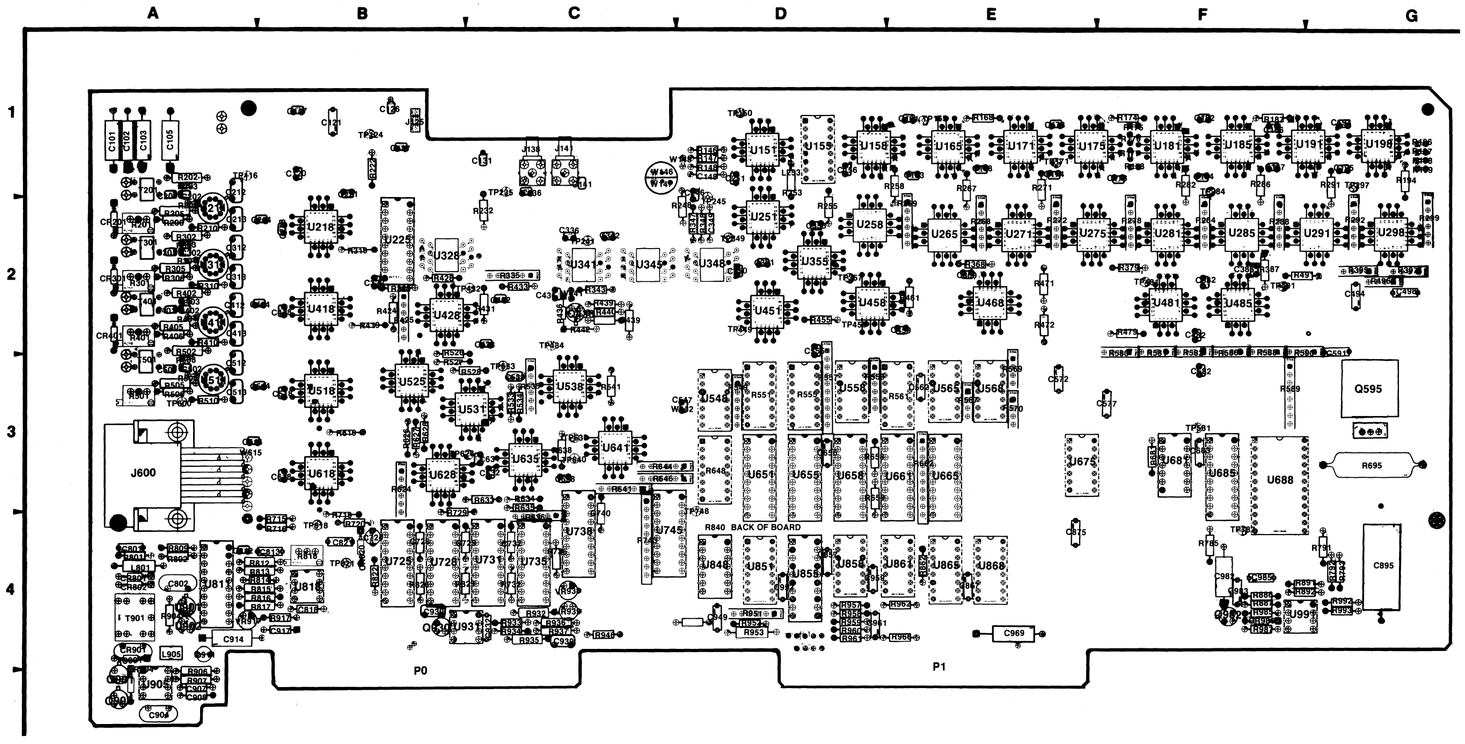
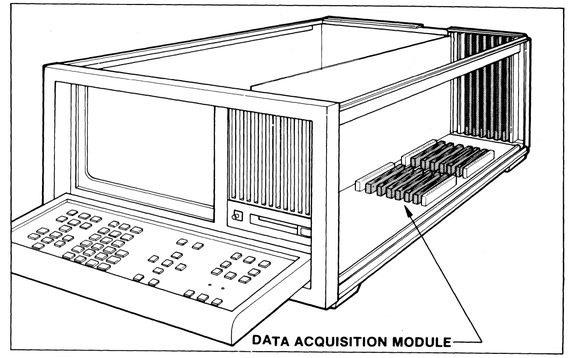


Figure 11-3. A28 91AE04A Data Acquisition Module component locations.



Configuration Guidelines

Module	Max. per Mainframe	Recommended Bus Slot(s)	Functional in Bus Slot(s)	Comments
91A24	1	2-6	1-6	
91AE24	3	2-6	1-6	Will not function without a 91A24 installed
91A04A	1	2-6	1-6	
91AE04A	3	2-6	1-6	Will not function without a 91AE04A installed

3836-271

Figure 11-4. A28 91AE04A locations.

A28 91AE04A DATA ACQUISITION MODULE COMPONENT LOCATIONS

Table 11-10
91A04A DATA ACQUISITION MODULE 59 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J600	F4	A3	R966	B5	E4
J600	A4	A3	R992	E1	G4
P0	F3	B4	R993	E1	G4
P0	A1	B4	TP458	E5	D2
R557	F4	D3	U451	E4	D2
R662F	B4	E3	U655	D4	D3
R681	B3	F3	U658	B3	D3
R715	B3	B4	U661	C4	E3
R716	B4	B4	U681A	C3	F3
R743	D5	C4	U681B	C3	F3
R785	F1	F4	U685	D1	F3
R791	E2	G4	U688	E1	F3
R792	E2	G4	U855	E3	D4
R793	E1	G4	U858	B5	D4
R957	B3	D4	U861C	F3	E4
R958	B4	D4	U865	E2	E4
R959	B4	D4	U868	B3	E4
R960	B5	D4	W615	F4	A3
R961	B5	D4	W615	A4	A3

The colors on this page correspond to the following 91A04A diagnostic functions.

0	REG
1	MAR
2	ACQ MEM
3	HIGH RES
4	WORD REC
5	DESKEW
6	DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.

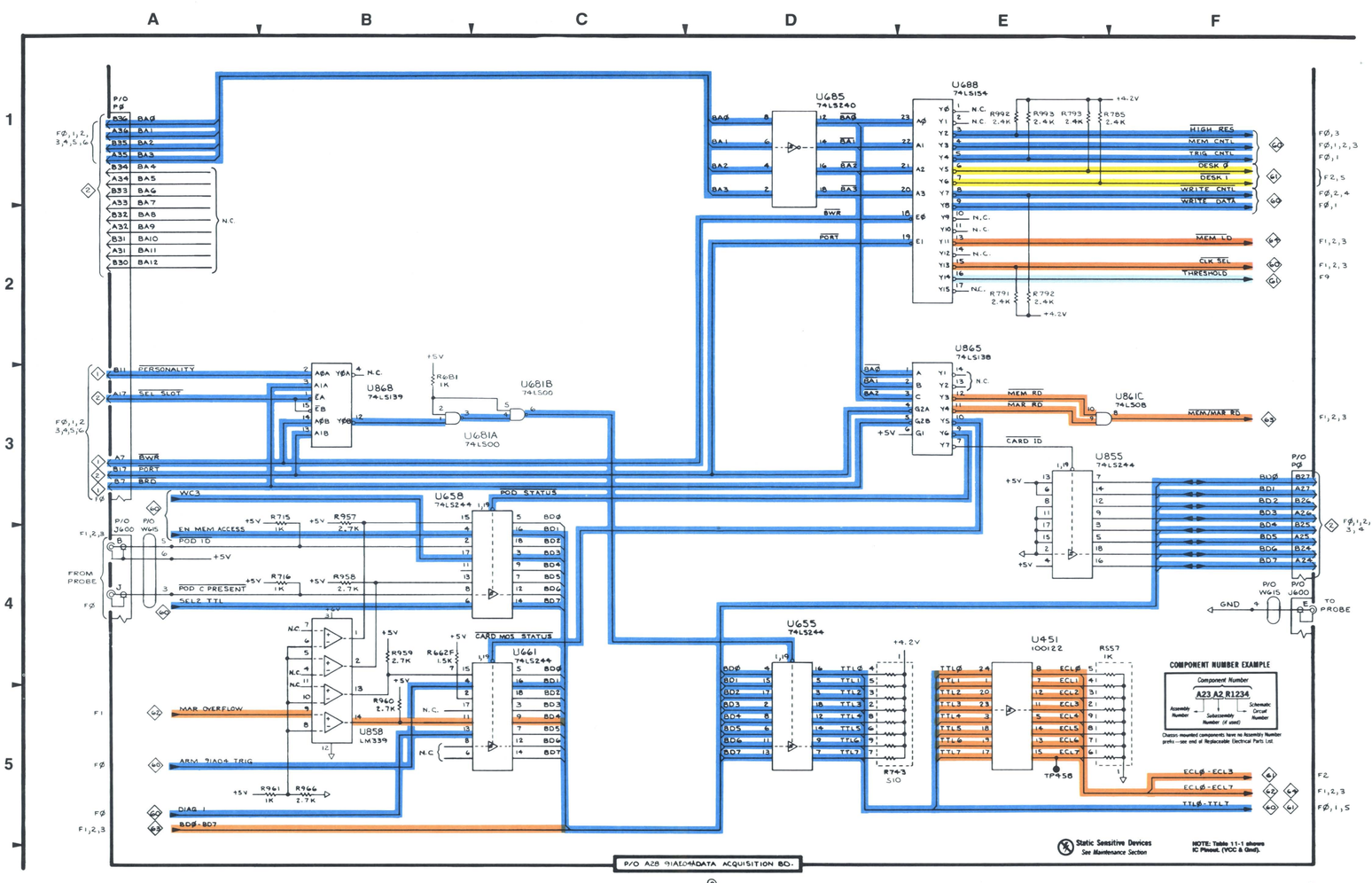


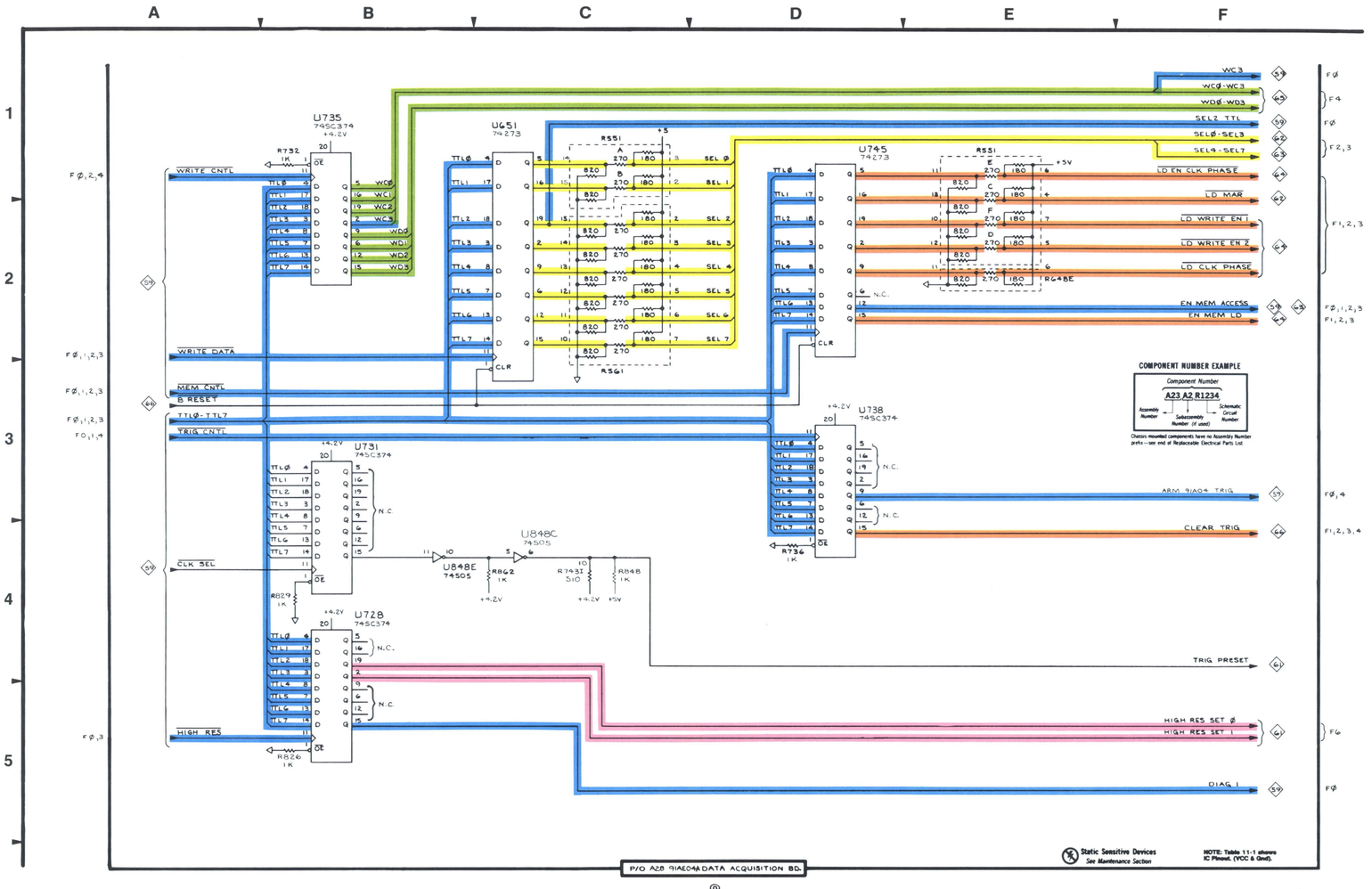
Table 11-11
91A04A DATA ACQUISITION MODULE 60 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R441A	C1	D3	R826	B5	B4
R551B	C1	D3	R829	B4	B4
R551C	E1	D3	R862	C4	E4
R551D	E1	D3	U651	C1	D3
R551E	E1	D3	U728	B4	B4
R551F	E1	D3	U731	B3	C4
R561	C2	E3	U735	B1	C4
R648E	E2	D3	U738	D3	C4
R732	B1	C4	U745	D1	C4
R736	D4	C4	U848C	C4	D4
R743I	C4	C4	U848E	B4	D4

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.



P/O A28 91AE04A DATA ACQ. CONTROL REGISTERS 60 A

Table 11-12
91A04A DATA ACQUISITION MODULE 61 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C201	A3	A2	R502	B5	A2
C201	A3	A2	R503	B5	A3
C202	B3	A2	R504	B5	A3
C212	B2	A1	R505	B5	A3
C213	B3	A2	R506	B5	A3
C218	D2	B2	R510	B5	A3
C301	A4	A2	R526	E4	B3
C302	B4	A2	R527	C5	B3
C312	B3	A2	R528	C5	B3
C313	B3	A2	R619	F4	B3
C401	A4	A2	R626	E5	B3
C402	B5	A2	R627	E5	B3
C412	B4	A2	R628	F4	B3
C413	B4	A2	R633	E5	C3
C418	E2	B2	R719	F4	B4
C501	A5	A3	R720	E1	B4
C502	B5	A3	R729	E5	B4
C512	B5	A3	R801	B2	A4
C513	B5	A3	R802	B2	A4
C518	F2	B3	R809	B2	A4
C618	F2	B3	R812	B1	A4
C812	B2	A4	R813	B2	A4
C813	C2	B4	R814	A2	A4
C818	B2	B4	R815	A2	A4
C917	A2	B4	R816	B2	A4
J600	A3	A3	R817	B2	A4
R201	B3	A2	R818	C1	B4
R202	B3	A1	R917	B2	B4
R203	B3	A1	T201	A3	A1
R204	B3	A2	T301	A3	A2
R205	B3	A2	T401	A4	A2
R206	B3	A2	T501	A5	A3
R210	B3	A2	TP600	C2	A3
R301	B4	A2	U211	B3	A2
R302	B3	A2	U218	D1	B2
R303	B3	A2	U225	C1	B2
R304	B4	A2	U311	B4	A2
R305	B4	A2	U411	B5	A2
R306	B4	A2	U418	E1	B2
R310	B4	A2	U428A	D5	B2
R319	D4	B2	U428C	D5	B2
R401	B4	A2	U511	B5	A3
R402	B4	A2	U518	F1	B3
R403	B4	A2	U525A	E4	B3
R404	B5	A2	U525B	E5	B3
R405	B4	A2	U525C	C4	B3
R406	B4	A2	U525D	C5	B3
R410	B4	A2	U618	F1	B3
R419	D4	B2	U628A	E5	B3
R424	C1	B2	U628C	E4	B3
R425B	E5	B2	U725	E1	B4
R425C	C5	B2	U811	B1	A4
R425D	C5	B2	U818	B2	B4
R425E	E5	B2	VR917	A2	A4
R428	C5	B2	W615	A5	A3
R431	D5	C2	W615	A3	A3
R501	B5	A3	W615	A4	A3

DELAY TIMES

DL201A - 0.71 ns
DL301A - 0.59 ns
DL401A - 0.59 ns
DL501A - 0.53 ns

DL211A - 0.31 ns
DL311A - 0.31 ns
DL411A - 0.31 ns
DL511A - 0.31 ns

DL211B - 0.400 ns
DL311B - 0.400 ns
DL411B - 0.400 ns
DL511B - 0.400 ns

DL218A - 1.12 ns
DL418A - 1.38 ns
DL518A - 1.34 ns
DL618A - 1.51 ns

DELAY TIMES

DL525A - 0.60 ns
DL525B - 1.50 ns
DL525C - 0.60 ns
DL525D - 1.50 ns

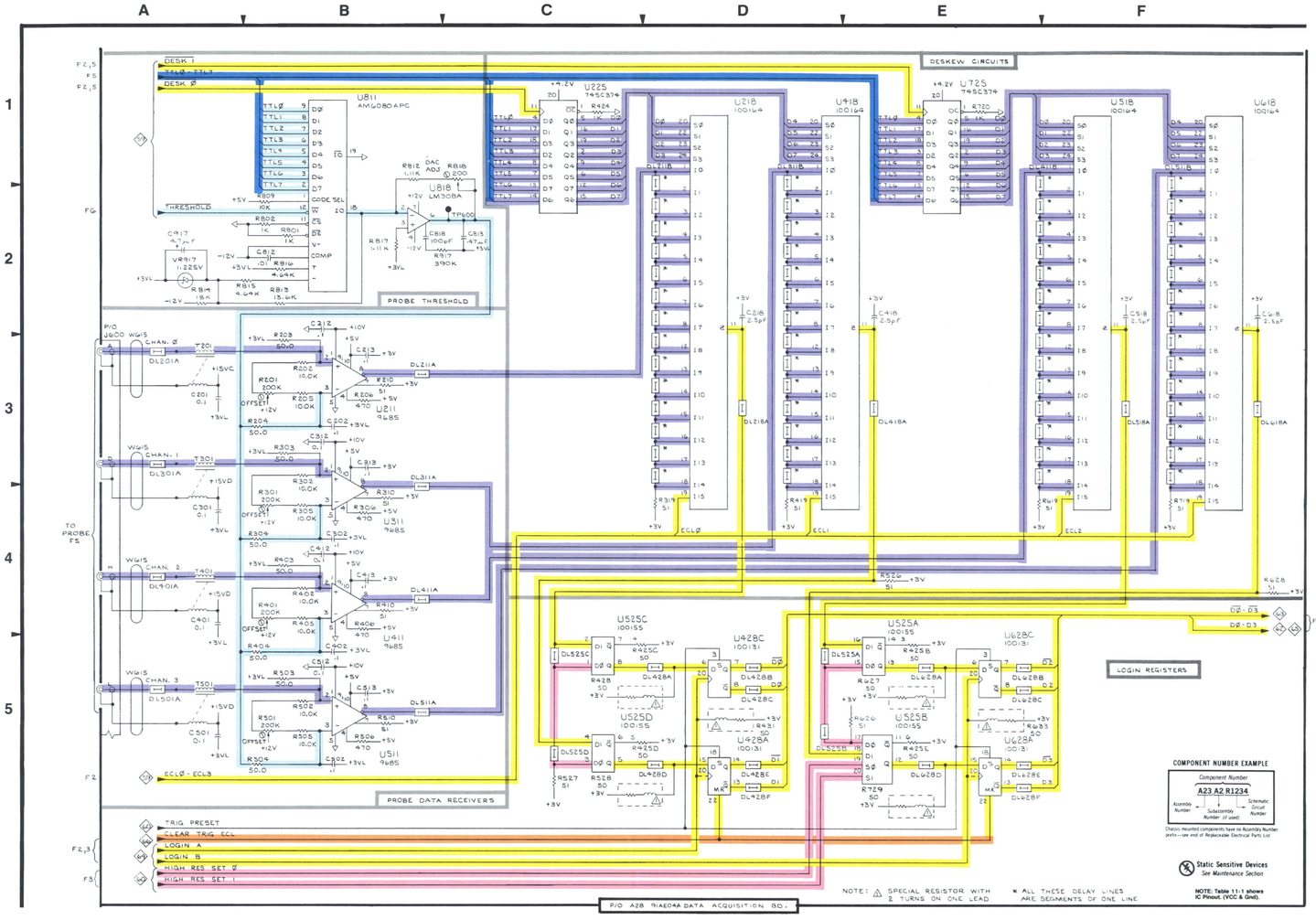
DL428A - 1.24 ns
DL428B - 3.02 ns
DL428C - 0.39 ns
DL428D - 1.24 ns
DL428E - 3.02 ns
DL428F - 0.39 ns

DL628A - 1.19 ns
DL628B - 2.79 ns
DL628C - 0.39 ns
DL628D - 1.19 ns
DL628E - 2.95 ns
DL628F - 0.39 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.



P/O A28 91AE04A DATA ACQ. DATA RECEIVERS (6) A

Table 11-13
91A04A DATA ACQUISITION MODULE 62 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R175	B4	F1	R570B	B3	E3
R176	A4	F1	R570C	B3	E3
R177	A4	F1	R580A	D2	F2
R178	B4	F1	R580B	D2	F2
R259B	B4	E2	R580C	D2	F2
R259C	B4	E2	R581A	D2	F2
R259D	B4	E2	R581B	D2	F2
R259E	B4	E2	R581C	D2	F2
R268B	C4	E2	R582B	D2	F2
R268C	C4	E2	R582C	D2	F2
R268D	C4	E2	R951A	B5	D4
R268E	C4	E2	R952	F5	D4
R272A	D4	E2	R962	F5	E4
R272B	D4	E2	U158	B3	D1
R272C	D4	E2	U165	C4	E1
R272D	D4	E2	U171	D4	E1
R278B	E4	F2	U175	E4	E1
R278C	E4	F2	U258	B2	D2
R278D	E4	F2	U265	C2	E2
R278E	E4	F2	U271	E2	E2
R455	B2	D2	U275	E2	E2
R567	B2	E3	U355	B2	D2
R569B	B2	E3	U458	B2	D2
R569C	B3	E3	U468	D2	E2
R570A	B3	E3	U851B	F5	D4

DELAY TIMES

DL165A - 0.19 ns
DL165B - 0.19 ns
DL165C - 0.19 ns
DL165D - 0.19 ns

DL171A - 0.19 ns
DL171B - 0.19 ns
DL171C - 0.19 ns
DL171D - 0.19 ns

DL175A - 0.19 ns
DL175B - 0.19 ns
DL175C - 0.19 ns
DL175D - 0.19 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEN
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.

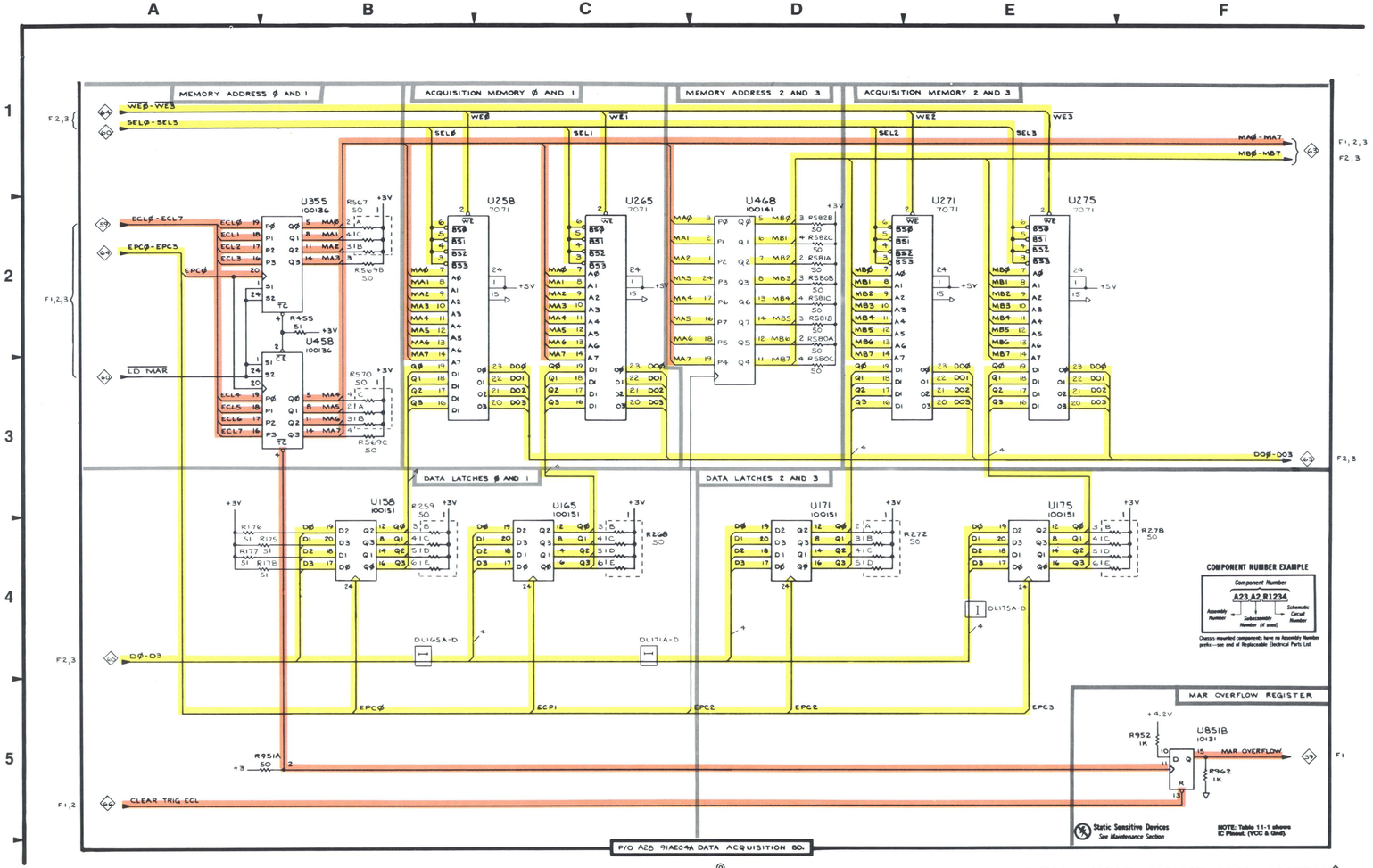


Table 11-14
91A04A DATA ACQUISITION MODULE 63 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
R196	A3	G1	R559D	C5	D3
R197	A3	G1	R559E	C5	D3
R198	A3	G1	R582A	B2	F2
R199	A3	G1	R586A	B1	F2
R284B	B3	F2	R586B	B1	F2
R284C	B3	F2	R586C	B2	F2
R284D	B3	F2	R588A	B2	F2
R284E	B3	F2	R588B	B2	F2
R288A	C3	F2	R588C	B2	F2
R288B	C3	F2	R590C	B2	F2
R288C	C3	F2	R658	C5	D3
R288D	C3	F2	R659	C5	D3
R292A	D3	G2	R662A	B5	E3
R292B	D3	G2	R662B	B5	E3
R292C	D3	G2	R662C	B5	E3
R292D	D3	G2	R662D	B5	E3
R299A	E3	G2	R662E	C5	E3
R299B	E3	G2	R662G	C5	E3
R299C	E3	G2	R662H	C5	E3
R299D	E3	G2	R662I	C5	E3
R395A	D2	G2	U181	B3	F1
R395B	D2	G2	U185	C3	F1
R395C	D2	G2	U191	D3	G1
R397A	D2	G2	U198	E3	G1
R397C	D2	G2	U281	B2	F2
R471	D5	E2	U285	C2	F2
R472	D5	E2	U291	D2	G2
R496A	D2	G2	U298	E2	G2
R496B	D1	G2	U481	A2	F2
R496C	D1	G2	U485	D2	F2
R549B	A5	D3	U548	B5	D3
R549C	A5	D3	U558	C5	D3
R549D	A5	D3	U565	D5	E3
R549E	A5	D3	U568	E4	E3
R559B	C5	D3	U665	E4	E3
R559C	C5	D3	U848A	A5	D4
			U848B	A5	D4

DELAY TIMES

DL185A - 0.19 ns
DL185B - 0.19 ns
DL185C - 0.19 ns
DL185D - 0.19 ns

DL191A - 0.19 ns
DL191B - 0.19 ns
DL191C - 0.19 ns
DL191D - 0.19 ns

DL198A - 0.19 ns
DL198B - 0.19 ns
DL198C - 0.19 ns
DL198D - 0.19 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REC
1 MAR
2 ACQ MEM
3 DIFF CNTR
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the begining and end of each colored line indicate all tests that enter or exit that point. The colors correspond to the the first test that is run on the line. For more information, refer to the colors on SCHEMATICS description in the DIAGRAMS section of your DAS 9100 SERIES SERVICE MANUAL.

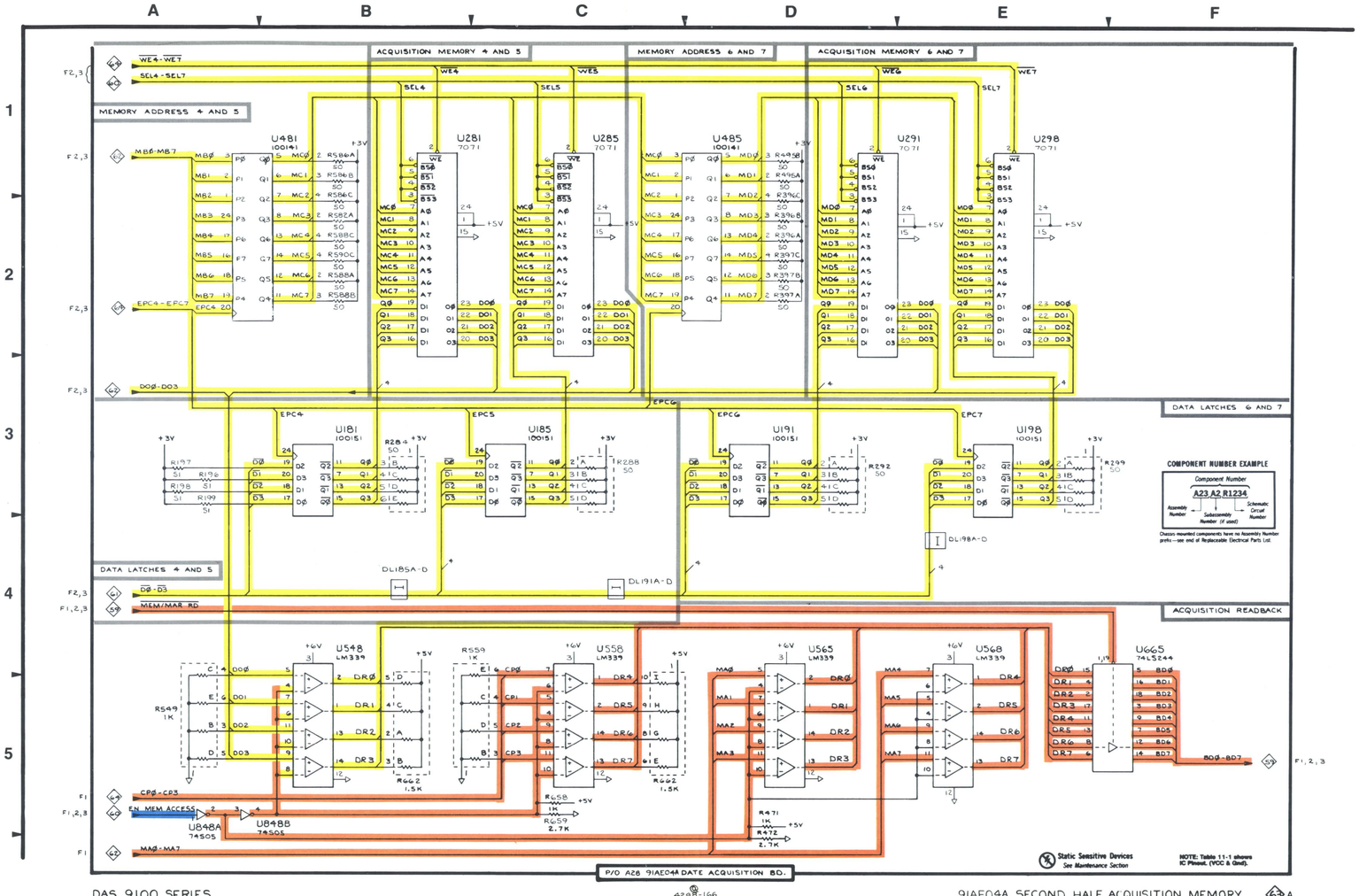


Table 11-15
91A04A DATA ACQUISITION MODULE 64 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C126	D3	B1	R347	D3	D2
C148	C2	D1	R348	D3	D2
C349	E3	D2	R368	D4	E2
C350	E3	D2	R379	D4	F2
C436	C2	C2	R387	D5	F2
C439	C2	C2	R433	C2	C2
C533	C3	C3	R436	C2	C2
J125	E3	B1	R439	D2	C2
J138	A2	C1	R440	D2	C2
L253	C3	D1	R442	C2	C2
Q436	D2	C2	R461	D4	E2
R146	D2	D1	R479	B4	F2
R147	D2	D1	R491	B5	F2
R148	C2	D1	R533	C3	C3
R168	D4	E1	R534	C3	C3
R174	D4	F1	R648A	D1	D3
R187	D5	F1	TP245	E3	D2
R194	D5	G1	TP533	C3	C3
R222	E3	B1	U151	C4	D1
R232	F4	C2	U155	D5	D1
R248	E3	D2	U251	B4	D2
R253	C3	D1	U328	E4	B2
R255	B4	D2	U341	E2	C2
R259A	B4	E2	U345	E3	C2
R268A	B4	E2	U348	D3	D2
R278A	B4	F2	U531A	C3	B3
R284A	B5	F2	U861A	B1	E4
R288A	B5	F2	W146	B2	C1
R325	E4	B2	W147	B2	C1
R335	F4	C2	W148	D2	D1
R343	E4	C2	W441	B2	C2

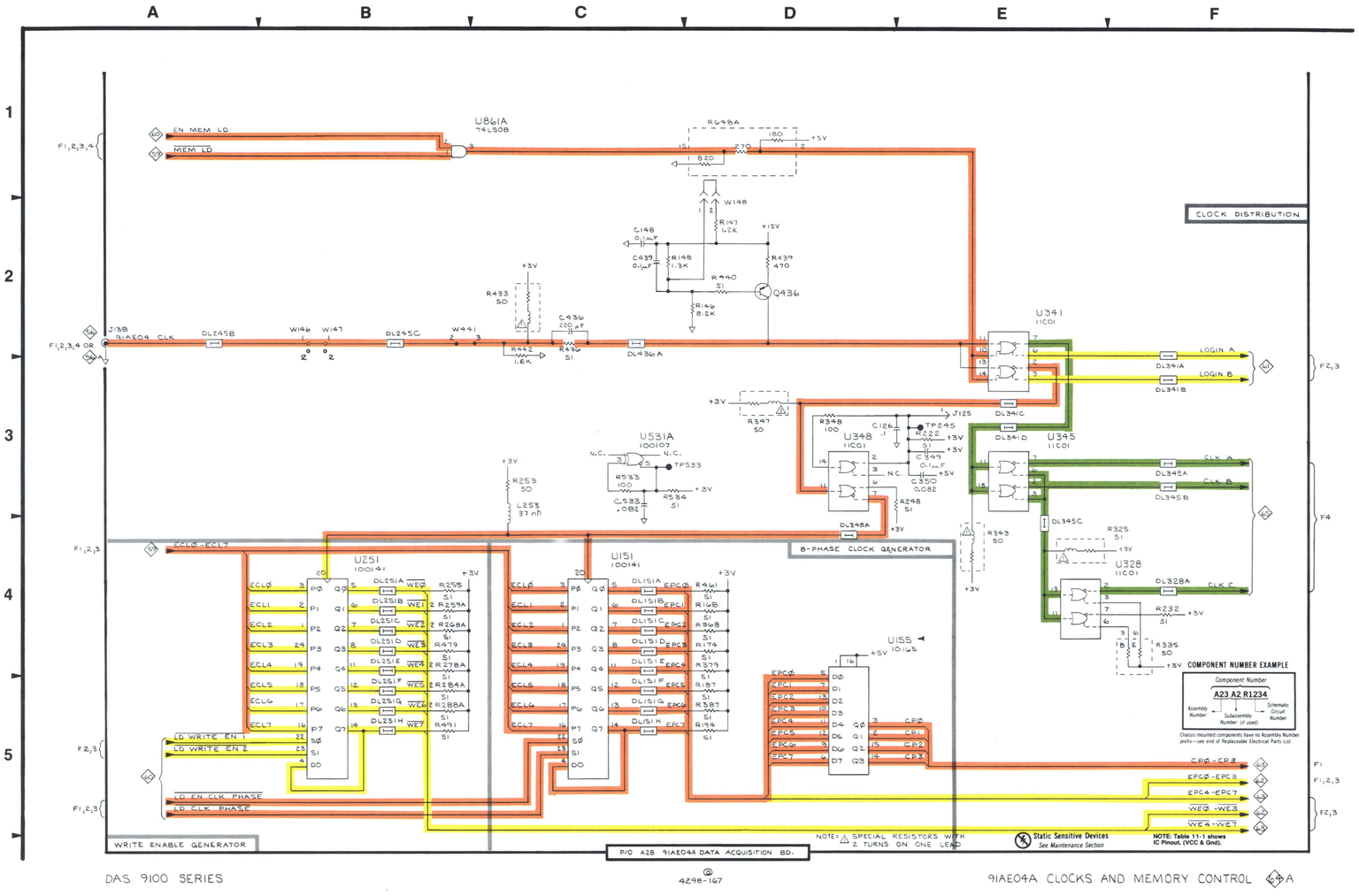
DELAY TIMES

```
DL245B - 0.27 ns
DL245C - 0.57 ns

DL436A - 0.16 ns

DL151A - 0.37 ns
DL151B - 0.66 ns
DL151C - 0.81 ns
DL151D - 0.94 ns
DL151E - 1.27 ns
DL151F - 1.58 ns
DL151G - 1.80 ns
DL151H - 1.91 ns

DL251A - 0.81 ns
DL251B - 1.08 ns
DL251C - 1.25 ns
DL251D - 1.58 ns
DL251E - 1.83 ns
DL251F - 2.08 ns
DL251G - 2.43 ns
DL251H - 3.16 ns

DL328A - 0.59 ns

DL341A - 1.77 ns
DL341B - 1.77 ns
DL341C - 0.25 ns
DL341D - 2.20 ns

DL345A - 1.05 ns
DL345B - 1.02 ns
DL345C - 1.75 ns

DL348A - 0.21 ns
```

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.



DAS 9100 SERIES

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91AE04A CLOCKS AND MEMORY CONTROL 6 5 A

Table 11-16
91A04A DATA ACQUISITION MODULE 65 A
ASSEMBLY A26

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J141	F3	C1	R636E	C4	C4
R535A	B2	C3	R638	B3	C3
R535B	B2	C3	R641B	D3	C3
R535C	C2	C3	R641C	C3	C3
R535D	B3	C3	R641D	C2	C3
R535E	B2	C3	R641E	C2	C3
R541	C1	C3	R644D	D3	C3
R624A	B3	B3	R646	D3	C3
R624C	B2	B3	TP640	D3	C3
R624D	B2	B3	U531	B2	B3
R624E	B2	B3	U538	C2	C3
R634	E4	C3	U635A	E3	C3
R635	D3	C4	U635B	C3	C3
R636D	E3	C4	U641C	D3	C3
			W642	E3	D3

DELAY TIMES

DL531A - 0.81 ns
DL531B - 0.81 ns
DL531C - 0.86 ns
DL531D - 0.83 ns
DL531E - 1.60 ns
DL531F - 1.55 ns
DL531G - 1.35 ns
DL531H - 1.60 ns

DL538A - 0.49 ns
DL538B - 0.49 ns
DL538C - 0.49 ns
DL538D - 0.49 ns

DL635A - 0.97 ns
DL635B - 1.20 ns

DL641A - 2.50 ns

DL642A - 0.40 ns
DL642B - 0.40 ns
DL642C - 0.60 ns
DL642D - 0.20 ns

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.

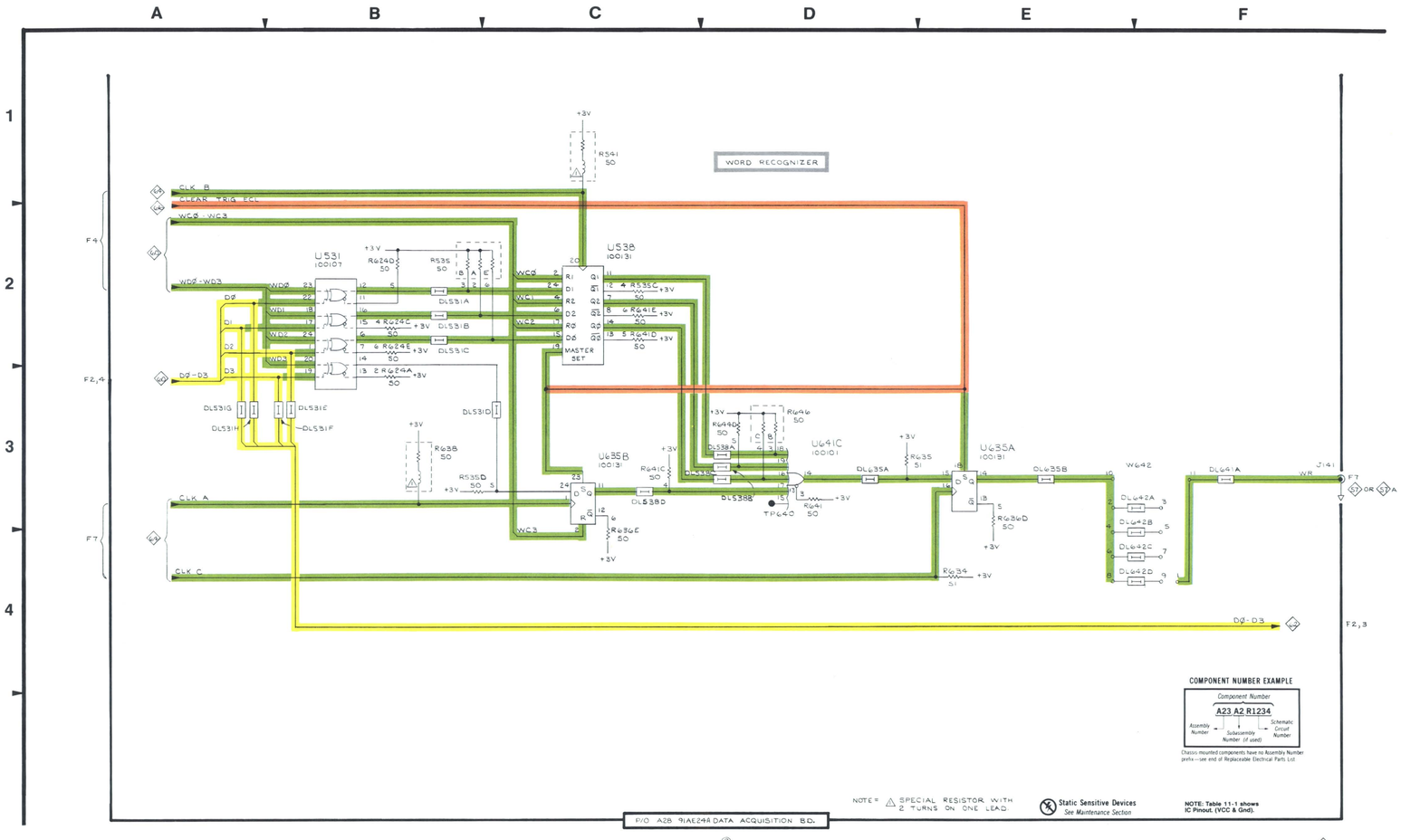


Table 11-17

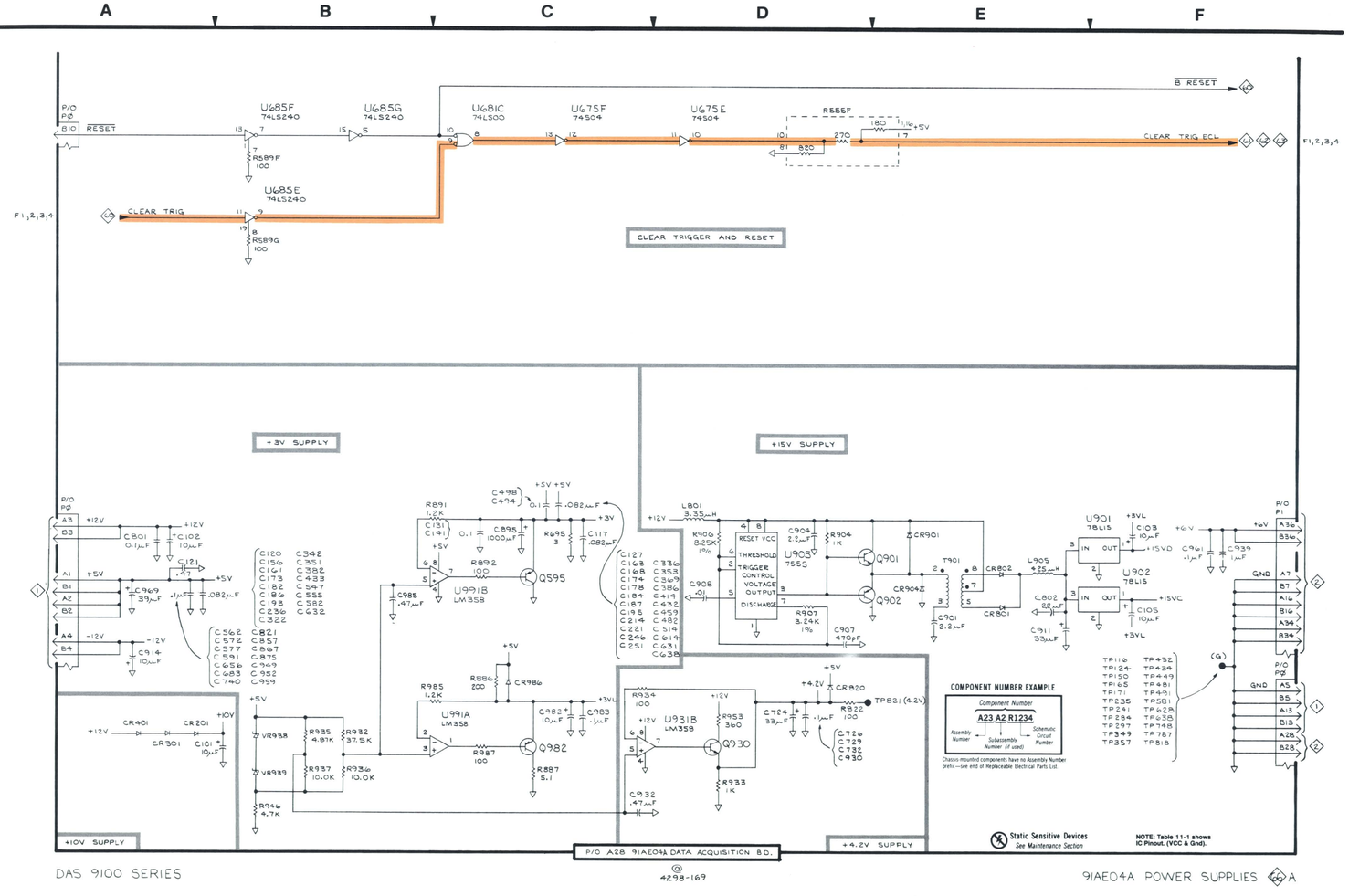
91A04A DATA ACQUISITION MODULE 66 A ASSEMBLY A28

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C101	A5	A1	C683	B4	F3	R822	D5	B4
C102	A4	A1	C724	D5	B4	R886	C4	F4
C103	F4	A1	C726	D5	B4	R887	C5	F4
C105	F4	A1	C729	D5	B4	R891	C3	G4
C117	B4	B1	C732	D5	C4	R892	C4	G4
C120	B4	B1	C740	B4	C4	R904	D4	A4
C121	A4	B1	C801	A4	A4	R906	D4	A4
C127	C4	B1	C802	E4	A4	R907	D4	A4
C131	C3	C1	C821	B4	B4	R932	B5	C4
C141	C4	C1	C857	B4	D4	R933	D5	C4
C156	B4	D1	C867	B4	E4	R934	C4	C4
C161	B4	E1	C875	B4	E4	R935	B5	C4
C163	C4	E1	C895	C3	G4	R936	B5	C4
C168	C4	E1	C901	E4	A4	R937	B5	C4
C173	B4	E1	C904	D3	A4	R946	B5	C4
C174	C4	E1	C907	D4	A4	R953	D5	D4
C178	C4	F1	C908	D4	A4	R985	B4	F4
C182	B4	F1	C911	E4	A4	R987	C5	F4
C184	C4	F1	C914	A4	A4	T901	E4	A4
C186	B4	F1	C930	D5	B4	TP116	F4	A1
C187	C4	F1	C932	C5	C4	TP124	F4	B1
C193	B4	G1	C939	F4	C4	TP150	F4	D1
C195	C4	G1	C949	B4	D4	TP165	F4	E1
C214	C4	A2	C952	B4	D4	TP171	F4	E1
C221	C4	B1	C959	B4	D4	TP235	F5	C1
C236	B4	C1	C961	F4	D4	TP241	F5	C2
C246	C4	D1	C969	A4	E4	TP284	F5	F1
C251	C4	D1	C982	C5	F4	TP297	F5	G1
C322	B4	B2	C983	C5	F4	TP349	F5	D2
C336	D4	C2	C985	B4	F4	TP357	F5	D2
C342	B4	C2	CR201	A5	A2	TP432	F4	B2
C351	B4	D2	CR301	A5	A2	TP434	F4	C2
C353	D4	D2	CR401	A5	A2	TP449	F4	D2
C369	D4	E2	CR801	E4	A4	TP481	F4	F2
C382	B4	F2	CR802	E4	A4	TP491	F4	F2
C386	D4	F2	CR820	D4	B4	TP581	F5	F3
C414	D4	A2	CR901	E4	A4	TP628	F5	B3
C432	D4	C2	CR904	E4	A4	TP638	F5	C3
C433	B4	C2	CR986	C4	F4	TP748	F5	D4
C459	D4	E2	L801	D3	A4	TP787	F5	F4
C482	D4	F2	L905	E4	A4	TP818	F5	B4
C494	C3	G2	P0	A1	B4	TP821	E5	B4
C498	C3	G2	P0	A4	B4	U658F	B1	D3
C514	D4	A3	P0	F4	B4	U675E	D1	E3
C547	B4	D3	P1	F3	E4	U675F	C1	E3
C555	B4	D3	Q595	C4	G3	U681C	C1	F3
C562	B4	E3	Q901	E4	A4	U685E	B1	F3
C572	B4	E3	Q902	E4	A4	U685G	B1	F3
C577	B4	F3	Q930	D5	B4	U901	F3	A4
C582	B4	F3	Q982	C5	F4	U902	F4	A4
C591	B4	G2	R555F	D1	D3	U905	D4	A4
C614	D4	A3	R589F	B1	F3	U931B	D5	B4
C631	D4	C3	R589G	B2	F3	U991A	C5	G4
C632	B4	C3	R695	C4	G3	U991B	C4	G4
C638	D4	C3				VR938	B5	C4
C656	B4	D3				VR939	B5	C4

The colors on this page correspond to the following 91A04A diagnostic functions.

0 REG
1 MAR
2 ACQ MEM
3 HIGH RES
4 WORD REC
5 DESKEW
6 DAC

The function numbers (indicates by the prefix F) at the end of each colored line indicate all tests that enter or exit that point. The colors correspond to the first test that is run on the line. For more information, refer to the colors on schematics description in your DAS 9100 SERIES SERVICE MANUAL.



REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
13103	THERMALLOY COMPANY, INC.	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS, TX 75234
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
74445	HOLO-KROME CO.	31 BROOK ST. WEST	HARTFORD, CT 06110
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247
98291	SEALECTRO CORP.	225 HOYT	MAMARONECK, NY 10544

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			1		CKT BOARD ASSY:DATA ACQ MODULE(SEE A26,		
	----- -----			-		A28 REPL)		
-2	198-4500-00			1		.WIRE SET ELEC:	80009	198-4500-00
						.**********(ATTACHING PARTS)**********		
-3	214-3421-00			2		.SOCKET,GUIDE:0.78 INCH LONG	00779	200390-4
-4	210-0599-00			2		.NUT,SLEEVE:4-40 X 0.391 INCH LONG	80009	210-0599-00
						.**********(END ATTACHING PARTS)*********		
-5	166-0031-00			2		.SPACER,SLEEVE:0.18 ID X 0.25 INCH LONG	80009	166-0031-00
-6	407-2772-00			1		.BRACKET,ANGLE:CONNECTOR	80009	407-2772-00
						.**********(ATTACHING PARTS)**********		
-7	210-1390-00			2		.EYELET,METALLIC:0.121 OD X 0.187 L,BRS	80009	210-1390-00
						.**********(END ATTACHING PARTS)*********		
-8	131-1493-00			3		.CONTACT,ELEC:TEST POINT STRAP	80009	131-1493-00
	----- -----			-		.(91A04A ONLY)		
	131-1493-00			2		.CONTACT,ELEC:TEST POINT STRAP	80009	131-1493-00
	----- -----			-		.(91AE04A ONLY)		
-9	346-0032-00			3		.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2859-75-4
-10	214-0579-00			31		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
	----- -----			-		.(91A04A ONLY)		
	214-0579-00			28		.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
	----- -----			-		.(91AE04A ONLY)		
-11	136-0755-00			2		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
	----- -----			-		.(91A04A ONLY)		
-12	----- -----			1		.TRANSISTOR:(SEE Q595 REPL)		
						.**********(ATTACHING PARTS)**********		
-13	210-0586-00			1		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-14	211-0012-00			1		.SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-15	214-3309-00			1		.HEAT SINK,XSTR:	13103	OBD
-16	214-1337-00			1		.PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-17	105-0160-04			1		.EJECTOR,CKT BD:YELLOW PLASTIC	80009	105-0160-04
-18	131-1343-00			2		.TERM. SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
	----- -----			-		.(91AE04A ONLY)		
-19	131-0265-00			6		.CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
	----- -----			-		.(91A04A ONLY)		
	131-0265-00			2		.CONNECTOR,RCPT,:RIGHT ANGLE MOUNT	98291	51-053-0000
	----- -----			-		.(91AE04A ONLY)		
-20	131-0608-00			10		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		.(91AE04A ONLY)		
	131-0608-00			3		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		.(91AE04A ONLY)		
-21	131-0993-00			1		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-	P6453			1		PROBE,DATA ACQ:4 CHANNEL 300MHZ	80009	P6453
-1	334-4373-00			1		.MARKER IDENT:MKD ACQUISITION PROBE	80009	334-4373-00
-2	334-4660-00			1		.MARKER IDENT:MKD POD INFO	80009	334-4660-00
-3	200-2672-00			1		.COVER,TOP:JUNCTION BOX,PLASTIC		
						.**********(ATTACHING PARTS)**********		
-4	211-0106-00			4		.SCREW,MACHINE:4-40 X 0.625"100 DEG,FLH,ST	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)**********		
-5	200-2673-00			1		.COVER,BOTTOM:JUNCTION BOX,PLASTIC		
-6	----- -----			1		.CKT BOARD ASSY:DESKEW(SEE A27A1 REPL)		
						.**********(ATTACHING PARTS)**********		
-7	211-0008-00			1		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)**********		
	----- -----			-		.CKT BOARD INCLUDES		
-8	131-2696-00			10		..CONTACT,ELEC:MICROMINATURE,FEM,BRS	71468	030-9542-002
-9	----- -----			1		..SWITCH,PUSH:(SEE A27A1 REPL)		
10	198-4518-01			1		..WIRE SET,ELEC:	80009	198-4518-01
11	214-3489-00			2		..PIN,GUIDE:0.156 DIA X 1.03 INCH LONG		
12	213-0007-00			1		..SCR,TPG,THD FOR:10-32 X 0.25 INCH,HEX SO	74445	ORD BY DESCR
13	334-4372-00			1		.MARKER,IDENT:MKD CLOKC	80009	334-4372-00
14	334-4371-00			1		.MARKER,IDENT:MKD CHANNEL 3	80009	334-4371-00
15	334-4370-00			1		.MARKER,IDENT:MKD CHANNEL 2	80009	334-4370-00
16	334-4369-00			1		.MARKER,IDENT:MKD CHANNEL 1	80009	334-4369-00
17	334-4368-00			1		.MARKER,IDENT:MKD CHANNEL 0	80009	334-4368-00
	119-1475-00			1		.HYBRID CKT ASSY:	80009	119-1475-00
18	426-1794-00			5		..FR SECT,PROBE:LOWER	80009	426-1794-00
						..**********(ATTACHING PARTS)**********		
19	211-0317-00			15		..SCREW,MACHINE:0-80 X 0.12,PNH	80009	211-0317-00
20	210-0504-00			15		..NUT,PLAIN,HEX.:0-8 X 0.156 INCH,BRS	73743	3004-402
						..**********(END ATTACHING PARTS)**********		
21	426-1795-00			5		..FR SECT,PROBE:UPPER	80009	426-1795-00
22	131-2695-00			10		..CONTACT,ELEC:MICROMINATURE CONN	71468	031-9569-000
23	386-4566-00			5		..PLATE,GROUND:	80009	386-4566-00
24	195-0693-00			1		LEAD,ELECTRICAL:26 AWG,3.5 L,9-1	80009	195-0693-00
	----- -----			-		(91AE04A ONLY)		
25	175-6425-00			2		CABLE ASSY,RF:50 OHM COAX,3.0 INCH LONG	80009	175-6425-00
	----- -----			-		(91AE04A ONLY)		
						STANDARD ACCESSORIES		
	070-4676-00			1		MANUAL,TECH:OPERATOR'S ADDENDUM	80009	070-4676-00
	070-4678-00			1		SHEET,TECHNICAL:INSTRUCTION	80009	070-4678-00
	----- -----			-		(91A04A ONLY)		
	070-4677-00			1		SHEET,TECHNICAL:INSTRUCTION	80009	070-4677-00
	----- -----			-		(91AE04A ONLY)		
						OPTIONAL ACCESSORIES		
	067-1139-00			1		FIXTURE,CAL:HIGH SPEED ACQUISITION	80009	067-1139-00
	175-7322-00			1		CABLE,ASSY,RF:50 OHM COAX,10.0 INCH LONG	80009	175-7322-00
	----- -----			-		(91AE04A ONLY)		
	195-0995-00			1		LEAD,ELECTRICAL:26 AWG,12.0 L,9-4	80009	195-0995-00
	----- -----			-		(91AE04A ONLY)		
	195-3659-00			1		LEAD,ELECTRICAL:23 AWG,1.5 L,0-N	80009	195-3659-00
	----- -----			-		(91AE04A ONLY)		
	070-4298-00			1		MANUAL,TECH:SERVICE ADDENDUM	80009	070-4298-00

FIG. 2 ACCESSORIES

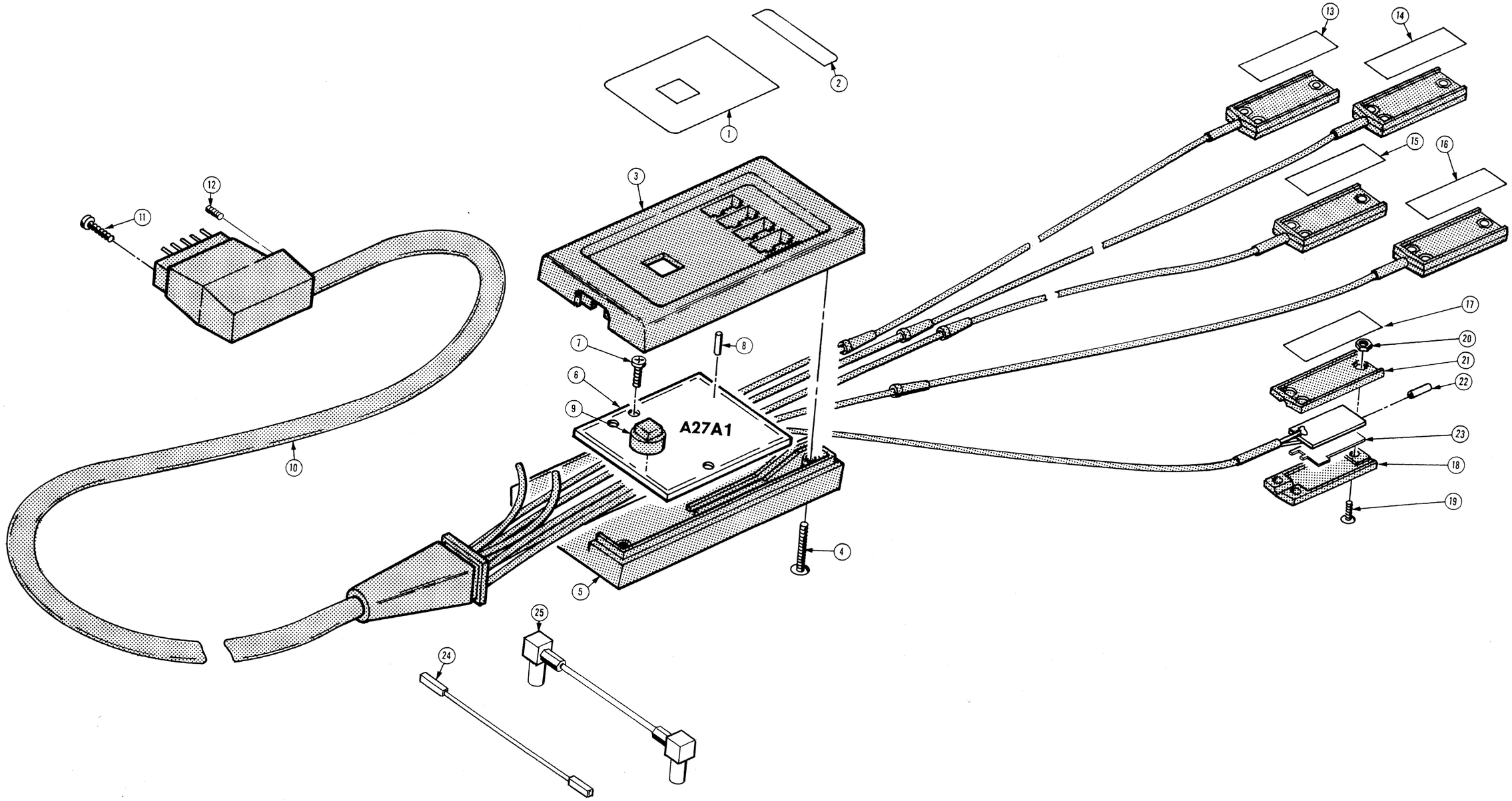


FIG. 1 EXPLODED