# 1. Introduction

# 1. Introduction

Figure 1.1 illustrates Daybreak architecture; the large dashed block contains the units that are described in this manual. Elements outside the large dashed block are described in "Dove IOP Board Technical Reference Manual," "Dove PCE Board Technical Reference Manual," and "Dove Input/Output Subsystem I/O Expansion Bus Interface Specification.

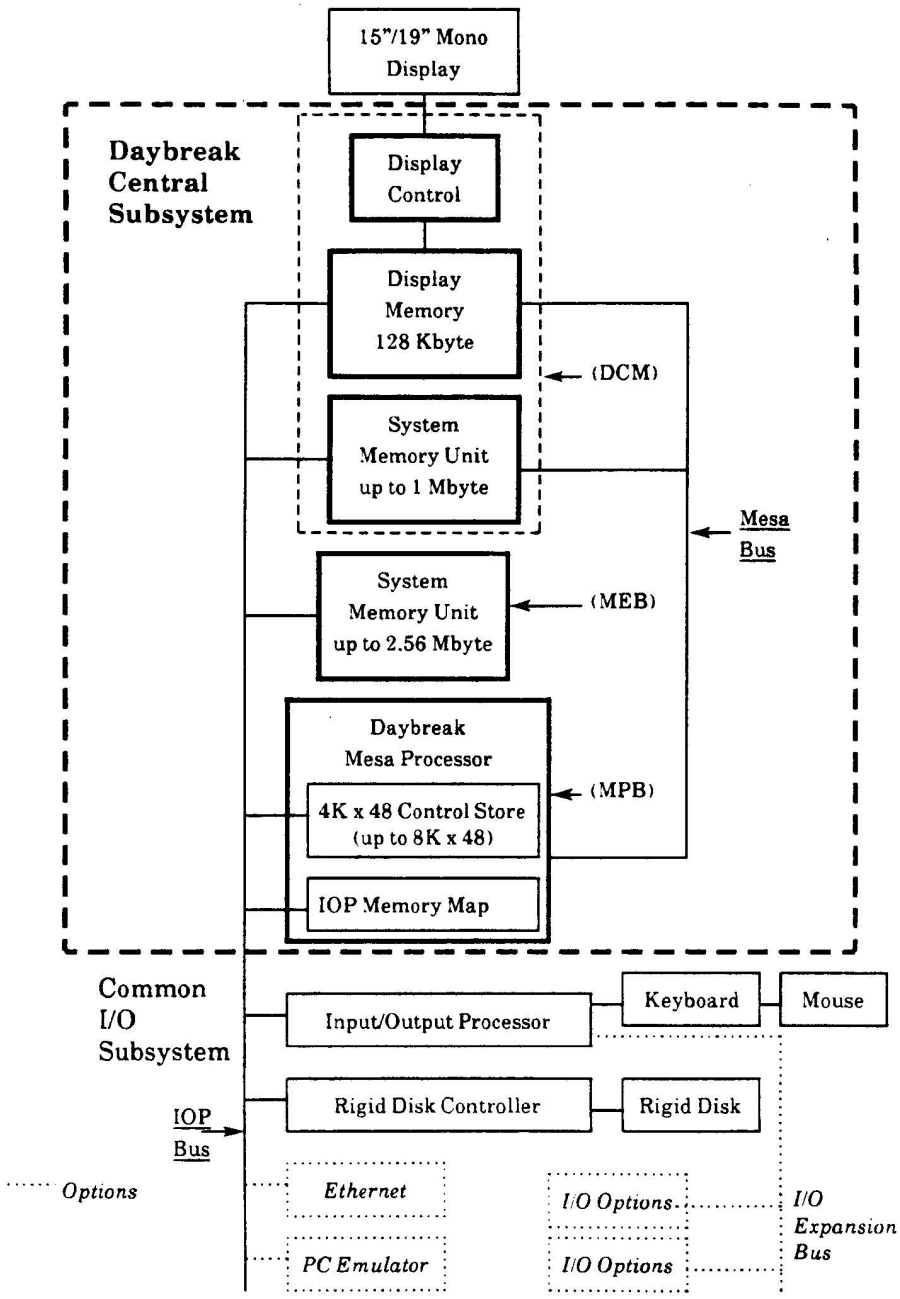


**Figure 1.1.** Daybreak architecture

## 1.1 Central Subsystem Components

The Daybreak central subsystem consists of the Mesa Processor, Display Controller and Memory, and Memory Expansion. Each of the components is implemented on a Printed Wiring Board Assembly, as described in this manual.

### 1.1.1 Mesa Processor

The heart of the ALU is a high-speed 2901C bit-slice processor, served by an auxiliary register file of 256 words and by a special shifter/rotator that rotates a word 4-, 8-, or 12-bit positions.

The Mesa processor executes microinstructions from a 4K by 48-bit, writable control store (expandable to 8K by 48 bits). Every 48-bit microinstruction contains the 12-bit address of the next instruction. Branching and dispatching are accomplished by ORing condition bits into the "next address" field.

The Microinstruction Decoder Chip (MDC), a gate array chip, decodes microinstructions. The decoded signals are pipelined through on-chip, clocked flip-flops.

The Mesa processor accesses memory as determined by the memory controller arbiter on the Display Control and Memory board. The Mesa processor has last priority (after memory refresh, display, and the IOP). When display is not demanding memory cycles, the Mesa processor can obtain at least every other memory cycle. A memory request is initiated by a Mesa bus transaction.

Except for I/O bus lines that load the control store of the Mesa processor, no direct data paths exist between the Mesa processor and the I/O subsystem. They communicate data via the memory subsystem, and interupt each other via two interrupt lines.

### 1.1.2 Display Controller and Memory

The display controller is implemented with three gate array chips: Display Data Chip, Display Cursor Chip, and Display Memory Chip.

The display controller reads quadwords from a 51 KWord bitmap in the memory display bank and produces video and sync signals for the video monitor. The screen has an active image of 737 lines by 1120 bits. A frame (an even field followed by an odd field ) is repainted 38 times a second.

Display memory is implemented in 64K DRAMs, and is controlled by a gate array chip, the Memory Control Chip (MCC). Cycle time for 16-bit word-access is 312.5 ns; for 64-bit nibble mode read-access, cycle time is 618 ns.

Display memory is a 3-ported memory bank with an additional internal refresh port. Refresh is a CAS-before-RAS scheme, with refresh counter in DRAM devices, and refresh timer in the MCC.

### 1.1.3 System Memory

System memory resides on the Display Control and Memory (DCM) board and on the Memory Expansion Board (MEB).

Memory on the DCM is a 2-ported, 2 x 256 KWord memory bank with an additional internal refresh port. A second MCC controls DCM system memory.

The MEB provides for system memory expansion of 2.56 Mbytes in 512 Kbyte sections for a total of 4 Mbytes. System memory is 5 x 256 KW of 256K DRAMs and is controlled by an MCC.

Memory access times and refresh are the same as for display memory.

## 1.2 Daybreak Backplane

The Dove backplane houses the boards that make up the system; that is, Memory Expansion Board (MEB), Display Control and Memory (DCM), Mesa Processor Board (MPB), I/O Processor/Rigid Disk Controller (IOP/RDC), PC Emulator (PCE), Rigid Disk Drive (RDD), and Options.

Pin assignments for the major boards are given in the subsections titled "Hardware" in the section that describes each board. This section describes the backplane in general.

The IOP/RDC, MEB, DCM, and MPB boards are 10.9 inches x 16 inches. The PCE and Options boards are 10.9 inches x 5.0 inches.

Figure 1.2 illustrates the view of the backplane from the logic board side. Note that the figure is not drawn to scale. Option slots 2 and 3 are contained on the board, but are covered by the MEB and MPB, as indicated by the dashed lines.

Figure 1.3 illustrates bus routing on the backplane, as viewed from the logic board side.

Figure 1.4 illustrates a front view of the signal flow of the 165-pin connectors.

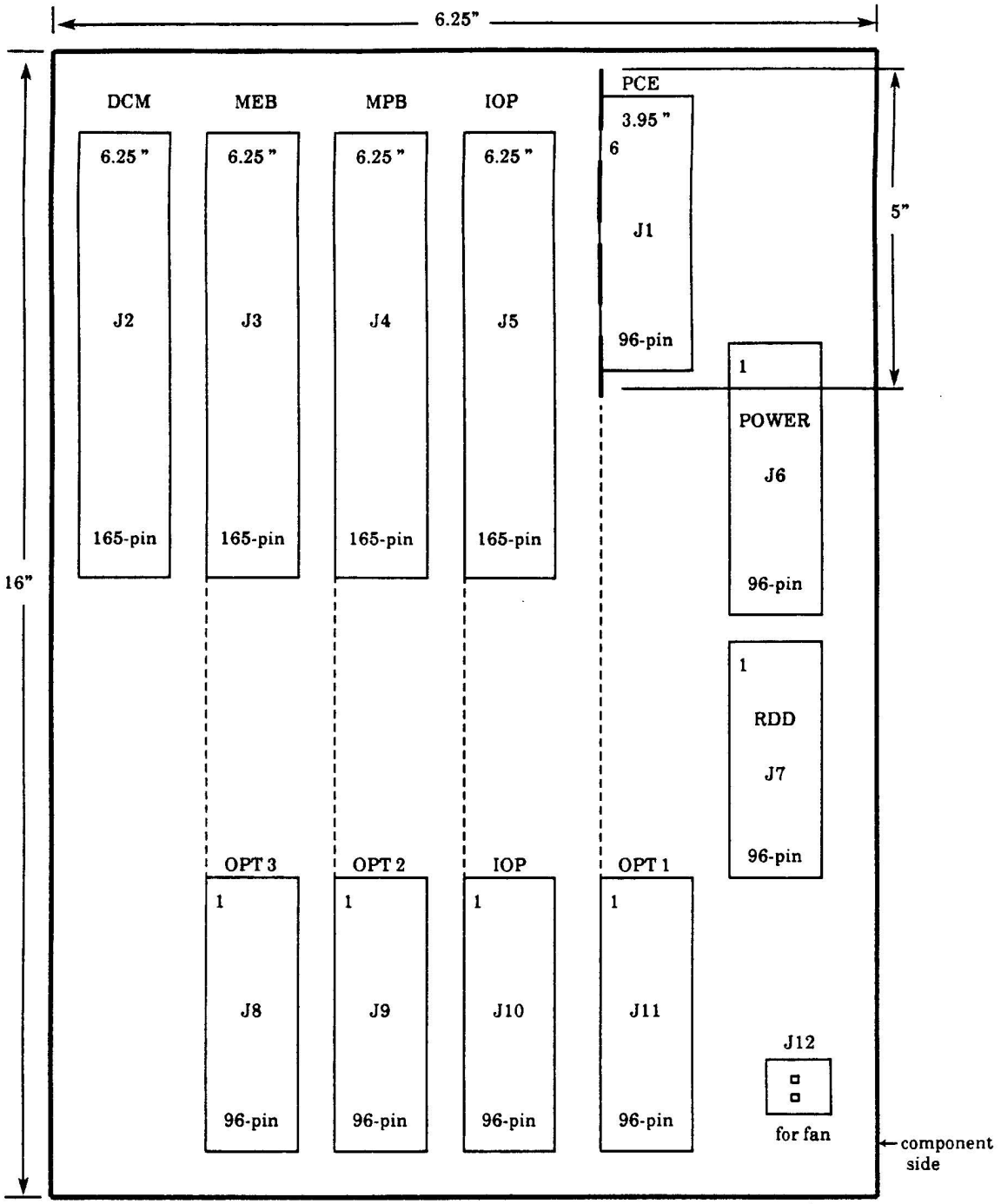


**Figure 1.2.** Backplane from logic board side

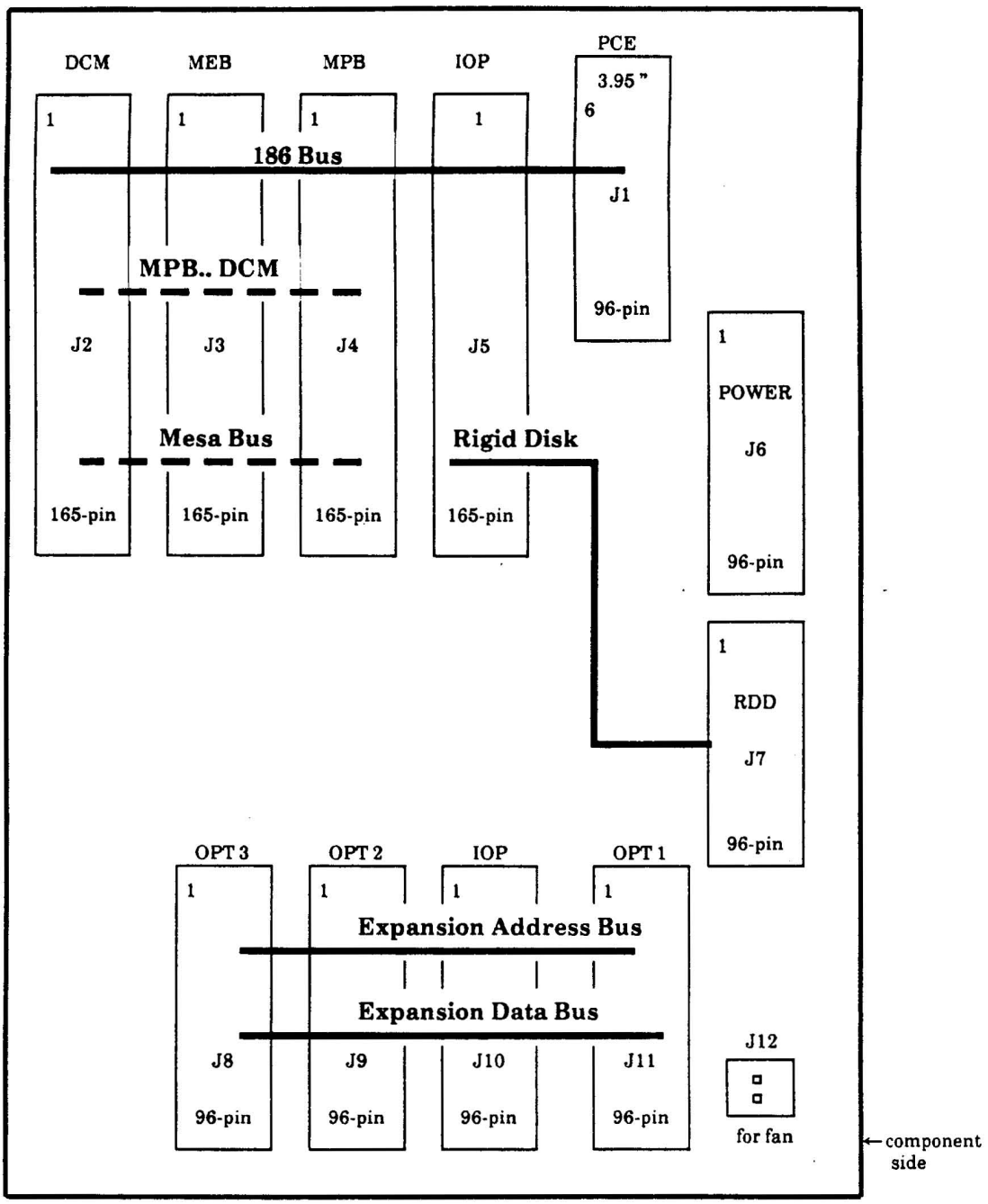


**Figure 1.3.** Bus routing (logic board side)

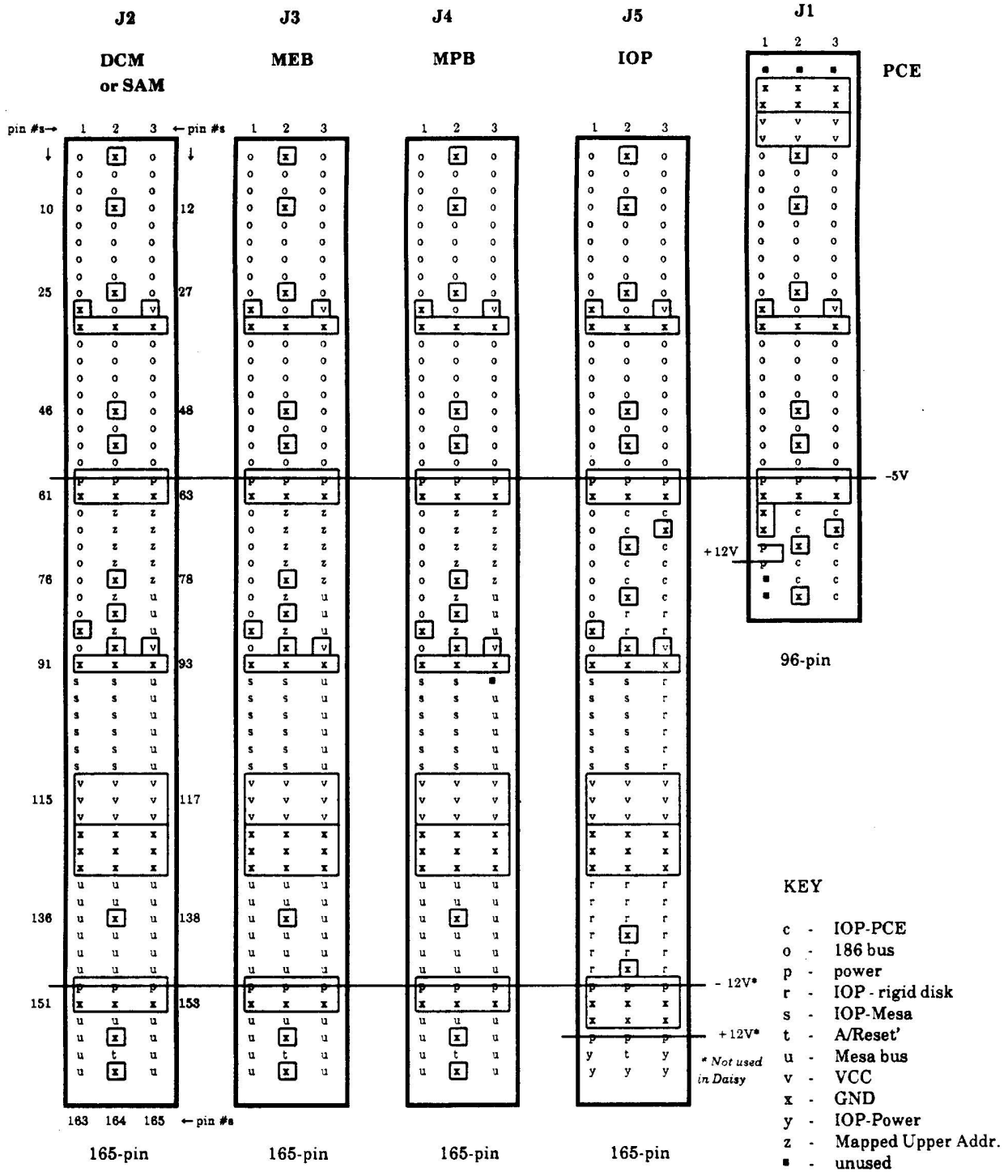


**Figure 1.4.** Signal flow of 165-pin connectors (front view)

## 1.3 Daybreak Power

Table 1.1 lists the Daybreak total dc power (Actual power vs Specified power).

**Table 1.1.** Total Daybreak DC Power

| ITEM | Note No. | +5.2Vdc Amps | +12.2Vdc Amps | -12.0Vdc Amps | -5.2Vdc Amps | TOTAL WATTS |
|---|---|---|---|---|---|---|
| MPB | (1) | 8.00 | 0 | 0 | 0 | 42 |
| DCM | (1) | 8.8 | 0 | 0 | 0.8 (4) | 50 |
| IOP | (1) | 10.0 | 0 | 0 | 0 | 52 |
| PCE | (2) | 3.0 | 0.1 | 0 | 0 | 18 |
| MEB | (2) | 3.8 | 0 | 0 | 0 | 20 |
| OPTION | (2) | 3.0 | 0.1 | 0 | 0 | 18 |
| 3 DC FANS | (3) | 0 | 0.75 | 0 | 0 | 9 |
| RIGID | (3) | 1.8 | 2.5 | 0 | 0 | 40 |
| **CONSOLE DC POWER** | | **38.4** | **3.45** | **0.2** | **1.0** | **249** |
| TRANSCEIVER | (2) | 0 | 1.0 | 0 | 0 | 12 |
| KEYBD/MOUSE | (1) | 0.4 | 0 | 0 | 0 | 2 |
| **Power to Backpanel (via power supply J1)** | | **38.8** | **4.45** | **0.2** | **1.0** | **263** |
| FLOPPY | (3) | 0.9 | 1.2 | 0 | 0 | 19 |
| MAG TAPE | (3) | 1.0 | 1.0 | 0 | 0 | 18 |
| Floppy + Mag Tape Power output (via power supply J2) | | 1.9 | 2.2 | 0 | 0 | 37 |
| **SYSTEM W/O DISPLAY DC POWER (ADDS J1 + J2)** | | **40.7** | **6.65** | **0.2** | **1.0** | **300** |
| **SPECIFIED POWER SUPPLY** | | **43.0** | **8.0** | **0.25** | **1.0** | **330** |

Notes:
(1) = Allocated (worst-case) calculated, verified by measurement
(2) = Allocated; actual is not known
(3) = Worst-case of all manufacturers data sheets
(4) = Actual current has not been verified

## 1.4 Notation

The following notation is used throughout this manual.

Signals notated n-n are inclusive signals. For example, A/A.00-15 indicates signals A/A.00 through A/A.15.

~ logical complement

' active low signal

,, concatentation

← assignment

## 1.5 Glossary

The following list defines terms as they are used in this manual.

**80186 bus** The bus that interfaces between the IOP and other PWBAs. Synonym: A bus

**A bus** The 80186 microprocessor bus.

**A-bypass** The bypass of the ALU that occurs when outputs of registers in 2901 internal register stack addressed by A0-3 (A port) are placed onto the Y bus.

**aD** A microinstruction field that specifies the ALU destination of the output of an ALU operation.

**aF** A microinstruction field that determines the ALU function to be applied to the operands designated by the aS field.

**Arbiter** The logic, located on the Memory Controller Chip, that grants memory access to requesting devices according to priority.

**aS** A microcode field that selects the two ALU source operands, R (output of the A port, value of the X bus, or 0) and S (output of the A or B port, value of the Q register, or 0).

**B bus** The system bus that interfaces between the Mesa processor and DCM and MEB boards. Synonym: Mesa bus.

**Burdock** The symbolic debugger for Mesa or IOP code. Allows the user to load binary files into control store or IOP RAM, set breakpoints, view registers and memory, and start and stop execution.

**click** Three successive cycles, designated c1, c2, and c3, and equal to 375 ns.

**Control Store** 1) On MPB, the 4096 x 48-bit storage (expandable to 8K x 48) that contains microinstructions.
2) On DCM, the storage that contains codes to control vertical and horizontal events.

**cursor** A hardware-controlled display that moves on the display screen according to movie movements.

**cursor buffer** A buffer on the DCM board that holds the cursor pattern. Its contents can be loaded, updated, and changed by the IOP.

**cycle** The basic unit of time, equal to 125 ns. The time in which a microinstruction can be decoded and executed.

**DCC** Display Cursor Chip
A gate array chip, part of the display controller. The DCC controls vertical event control store addressing, receives cursor data from the IOP and Mesa processor, aligns the cursor to bit boundaries, and sends data to the Display Data Chip, where the cursor data is mixed with display data.

**DCM** Display Control andMemory Board
A PWBA on the Dove backplane, containing display control and memory, and up to 2 x 256 KWords of system memory.

**DDC** Display Data Chip
A gate array chip, part of the display controller, that controls horizontal and vertical event generation, horizontal address, and cursor word detection. Regulates border pattern and cursor and display mixing.

**dirty flag** A Map flag bit that, when set, indicates that a store was done into a non-write-protected page.

**Display Data FIFO** A buffer between display memory and the Display Data Chip that translates data from Intel format to Mesa format through byte swapping and bit renumbering.

**DMC** Display Memory Chip
A gate array chip, part of the display controller. The DMC retrieves bitmap data from display memory, and keeps track of display memory address. Fetches display memory in nibble mode; that is, in one quadword per memory request.

**Evaluation stack** A register array that is the primary source of Mesa instruction operands and the primary destination of results. The stack also used passes parameters and results from one context to another during control transfers. The stack is normally accessed in a last in, first out manner.

**error trap** An exception condition; for example, reset, stack overflow, instruction buffer empty, which traps to location 0 of microinstruction control store.

**IB** Instruction Buffer
A 3-byte buffer in the central processor that holds bytes from the code segment while a Mesa opcode is executing. The first byte is called ibFront, the second is IB0, and the third is IB1.

**IBDisp** Instruction Buffer Dispatch
A 256-way dispatch based on the value of ibFront. . The high 4 bits of ibFront replace INIA4-7, while the low 4 bits of ibFront are ORed with INIA8-11, allowing simultaneous branch/dispatches. INIA0-3 is unaffected; therefore, 16 possible 256-way dispatch tables can be simultaneously specified.

**ibempty** — An error trap indicating that the IB contains no more instruction bytes.

**IB refill trap** — A microcode trap caused when an IBDisp is executed and IBPtr ≠ full or MInt = 1.

**IB state machine** — The logic that controls the state of the instruction buffer and determines which byte to read or write.

**INIA** — Immediate Next Instruction Address
The 12-bit microinstruction field that supplies the next microinstruction address. Modified by traps, condition codes, and IB dispatches.

**interval timer** — Timer circuits that allow high resolution measurements on program performance and external events.

**IOP** — Input/Output Processor
The 80186 processor that handles all I/O and boot-up operations.

**line segment** — A subset of a horizontal line in which the displayed words come from contiguous memory locations.

**Link register** — A 4-bit register that stores state information, constants, or branch condition bits.

**lock** — A signal that, when activated by the Mesa processor, prevents other memory ports from accessing memory during memory references by the Mesa processor in which semaphore type of data is fetched, modified, and stored.

**MCC** — Memory Control Chip
A gate array chip that controls a memory unit.

**MDC** — Microinstruction Decoder Chip
A gate array chip on the MPB that decodes control store microinstructions, and pipelines (or clocks) the decoded control signals.

**MEB** — MemoryExpansion Board
A PWBA containing a two-ported memory bank of 5 x 256 KWords. The MEB consists of one memory unit which has five memory banks of 512 Kbytes per bank.

**mem** — A 1-bit microinstruction field. When true in c1, specifies the start of a memory operation. When true in c2, indicates a memory/IO write. When true in c3, indicates a memory read/IO read.

**memory unit** — One of three divisions of memory; that is, display memory unit, system memory unit 1 (on the DCM), and system memory unit 2 (on the MEB). Each memory unit is controlled by an MCC gate array chip.

**Mesa bus** — See B bus.

**Mesa Processor Principles of Operation** — A document that defines the architecture of the Mesa processor. Synonym: PrincOps.

| | |
|---|---|
| **MInt** | Mesa Interrupt<br>A 1-bit register of the central processor used to interrupt the contiguous execution of Emulator macroinstructions. |
| **MIR** | MicroInstruction Register |
| **MPB** | Mesa Processor Board<br>A PWBA containing central processor hardware and the IOP memory map. |
| **NIA** | Next Instruction Address<br>The 12-bit quantity that addresses control store and that is the address of the microinstruction to be executed in the next cycle. |
| **Port A (memory)** | Interface with the 80186 bus, as viewed by a memory unit controlled by a MCC gate array chip. |
| **Port B (memory)** | Interface with the Mesa bus, as viewed by a memory unit controlled by a MCC gate array chip. |
| **process timeout** | A device that times out a process on the condition queue so that the process does not wait indefinitely. When the process timeout occurs, the process, if still waiting on the condition queue, will be made ready on the processor. Process timeout is measured in time units called ticks. The tick time is implemented in the Mesa processor by a 16-bit timer in the 8254 timer chip. |
| **Q register** | A part of the 2901C bit slice. Used in double word shifting, it supports the execution of multiplication and division opcodes. |
| **rA** | A bus source; microinstruction field |
| **rB** | B bus source; microinstruction field |
| **R bus** | The internal bus within the 2901C bit slice. |
| **rD** | 2901C ALU destination/shift control; microinstruction field. |
| **R register** | Main register file that is 64 x 16-bits of two-port register array. Part of 2901C bit slice. |
| **RH register** | An extension of the R registers that can hold highest-order memory address bits. It can also be used for general purpose storage; for example, for flags, temporaries, and subroutine return pointers. |
| **referenced flag** | A memory map entry that, when set, indicates a read or write access of a word location within the associated memory page. |
| **rotator** | A multiplexer that rotates the Y bus contents by 0, 4-, 8-, or 12-bit positions, and then drives the X-bus. |
| **stackP register** | A 4-bit register of the central processor that addresses the locations of the Mesa evaluation and argument stack. |
| **Trap machine** | A small state machine that controls the setting of the trap signal, which causes a branch to microcode address 0. The trap machine also reports the trap code: init trap, stack overflow trap, or IBempty trap. |
| **U register** | A 256-word register file that is written from the Y bus and read onto the X bus. These 16-bit registers hold a 16-word evaluation stack, virtual page addresses, temporaries, counters, and constants. |

**write protect flag** A memory map entry that, when set, indicates that the associated page is not to be written into. If a store to a location in that page is attempted, then a write-protect fault occurs.

**X bus** A 16-bit bus of the central processor, connected to multiple sources and multiple sinks.

**Y bus** A 16-bit bus of the central processor that supplies memory addresses, memory write data, U register data, or device output data. The bus is driven by the 2901C.

**YH bus** An 8-bit extension of the Y bus driven by the RH registers.