# 620/L SERIES

# POWER RE/RESTART AND REAL-TIME CLOCK

# MANUAL

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In Varian 620/L and 620/L-100 computer systems, the power-failure/restart (PF/R) and real-time clock (RTC) features are contained on a single printed-circuit board (DM123-3) in slot 16 of the processor mainframe.

In this manual, section 1 covers the PF/R and section 2 the RTC. Engineering drawings are in Volume 2 of the Maintenance Manual.

**NOTE**

In the running text of this manual, numbers beginning with a digit other than zero are decimal numbers, numbers with a leading zero are octal, and numbers preceded by a dollar sign ($) are hexadecimal.

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# SECTION 1
# POWER FAILURE/RESTART

## 1.1 DESCRIPTION

The power failure/restart (PF/R) is a mainframe feature for the Varian Data 620/L computer system that:

a. Provides an orderly shutdown in case of power failure or turnoff.

b. Restarts the program when power is restored.

The PF/R contains a system power monitor to detect the status of system power and also a sequencer for controlling the processor and core storage during power up or down. It has the highest interrupt priority in the system.

The PF/R indirectly monitors the ac input by measuring a reference voltage of approximately +12V developed by a fullwave bridge within the +5V power supply. A drop in the reference voltage (caused either by power failure or by turning off the power switch) actuates the PF/R and causes an interrupt. The CPU executes a user-programmed service routine that places the contents of volatile registers into memory. The program stops, the memory is disabled, and the system is reset (figure 1-1).

When the power monitor detects restoration of power, the memory is enabled, the processor executes a user-programmed service routine that returns the contents to the volatile registers, and the program resumes at the point of interrupt.

The PF/R is on a 7-3/4-by-12-inch etched-circuit card, which it shares with the real-time clock. The card is installed in slot 16 of the processor mainframe. All connections are through the 122-terminal card-edge connector at the processor backplane (figure 1-2).

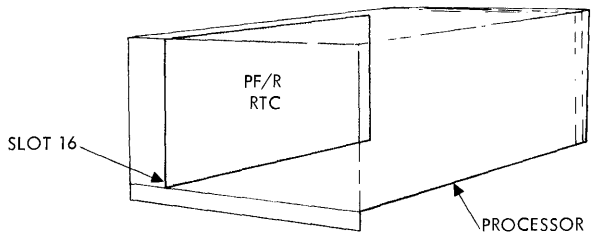


**Figure 1-2. PF/R Installation**

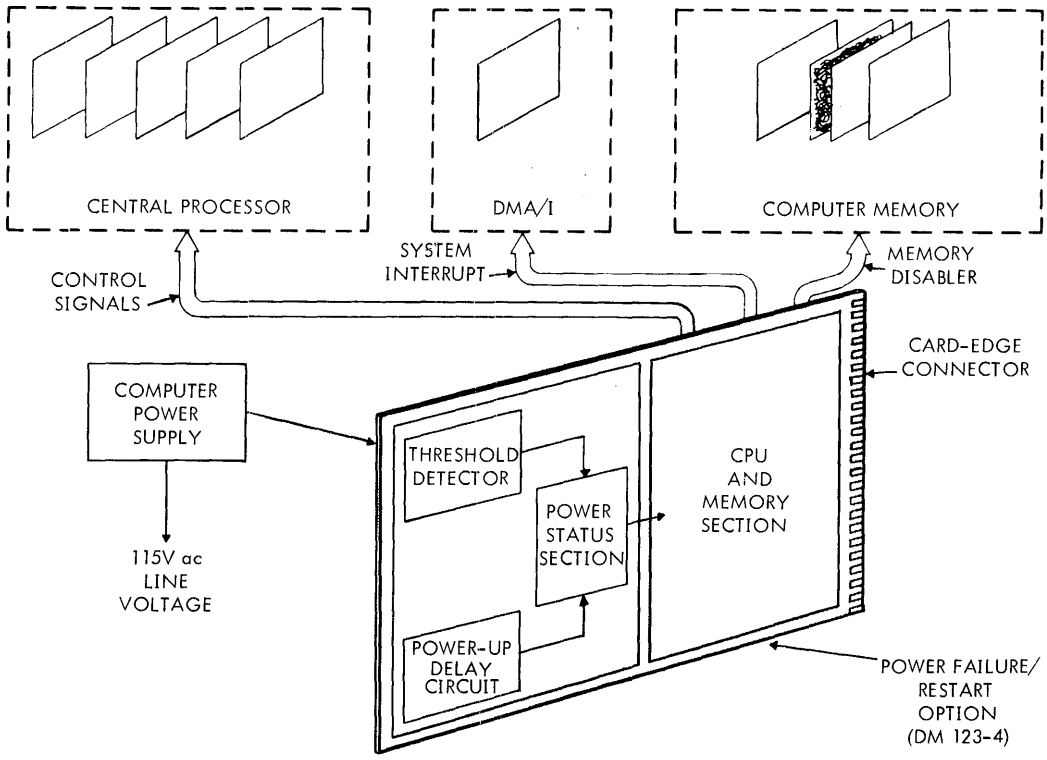


**Figure 1-1. PF/R Configuration**

## 1.1.1 Specifications

Table 1-1 gives the physical, electrical, and operating specifications of the PF/R.

**Table 1-1. Power Failure/Restart Specifications**

| | |
|---|---|
| Organization | Consists of a system power monitor (with a voltage threshold detector), a power-up delay section, a power status section, and a sequencer for the CPU and memory. |
| Size | One 7-3/4-by-12-inch etched-circuit card. |
| Interconnection | Interfaces with CPU and memory circuits through the 122-terminal card-edge connector at the computer backplane. |
| Operational Environment | 5 to 45 degrees C; up to 90 percent relative humidity without condensation. |
| Interrupt Priority | Highest level in the system. |
| Power Failure Detection Timing | Less than one cycle of the ac input voltage after power failure. |
| Power-Down Timing | Less than 500 microcseconds after power failure detection. |
| Power-Up Timing | Less than 1.1 seconds after the return of full power. |
| Interrupt-Memory Addresses | Power-down: 040 and 041.<br>Power-up: 042 and 043. |
| PF/R Input Power | +5V dc; +12V dc; −12V dc. |
| Sensed Voltage | About +12V dc for 115V ac input. |
| Threshold Voltage Range | 100 to 120V ac (normal setting 104 ± 0.5V ac). |
| Logic Levels: | |
| To the I/O Bus | Negative logic:<br>True: 0.0 to +0.5V dc.<br>False: +2.8 to +3.6V dc. |
| To the CPU and the Memory | True: +2.4 to +5.5V dc.<br>False: 0.0 to +0.5V dc. |

## 1.1.2 Functional Description

PF/R functions are divided into power-down and power-up sequences, neither of which is affected by the length of the power failure or turnoff.

Figure 1-3 shows the timing sequence for signals generated during the power-down sequence. The interrupt request is generated at the first negative-going transition of the interrupt clock after detection of a power failure or turnoff. The DMA generates an interrupt-acknowledge signal that causes placement of the interrupt address on the E bus for the duration of the interrupt-acknowledge signal. A delay of 160 microseconds or more allows execution of the power-down service routine stored at the interrupt address. The program must stop within 160 microseconds. Signals that disable the memory and reset the system are sent to the CPU. Lower-priority options and controllers cannot generate trap requests or interrupts during the execution of the power-down service routine.

Figure 1-4 shows the timing sequence for signals generated during the power-up sequence. When power is restored, the restart address (042) is put into the P register, a Halt signal is put into the U register, the W register is cleared, and System Reset is applied. A delay of about 800

milliseconds allows the input power to stabilize. A further delay of about 70 milliseconds settles the power after enabling the memory regulators. Then System Reset is removed, and a start pulse puts the CPU in Run mode at address 042. The power-up service routine is now initiated. For the first 100 ± 20 microseconds following the start pulse, no power-down status is recognized.

If power is restored during the power-down sequence, the PF/R completes that sequence before starting the power-up sequence.

If a power failure or turnoff is detected while the computer is in the Step mode, memory is protected, but the contents of the volatile registers are lost.

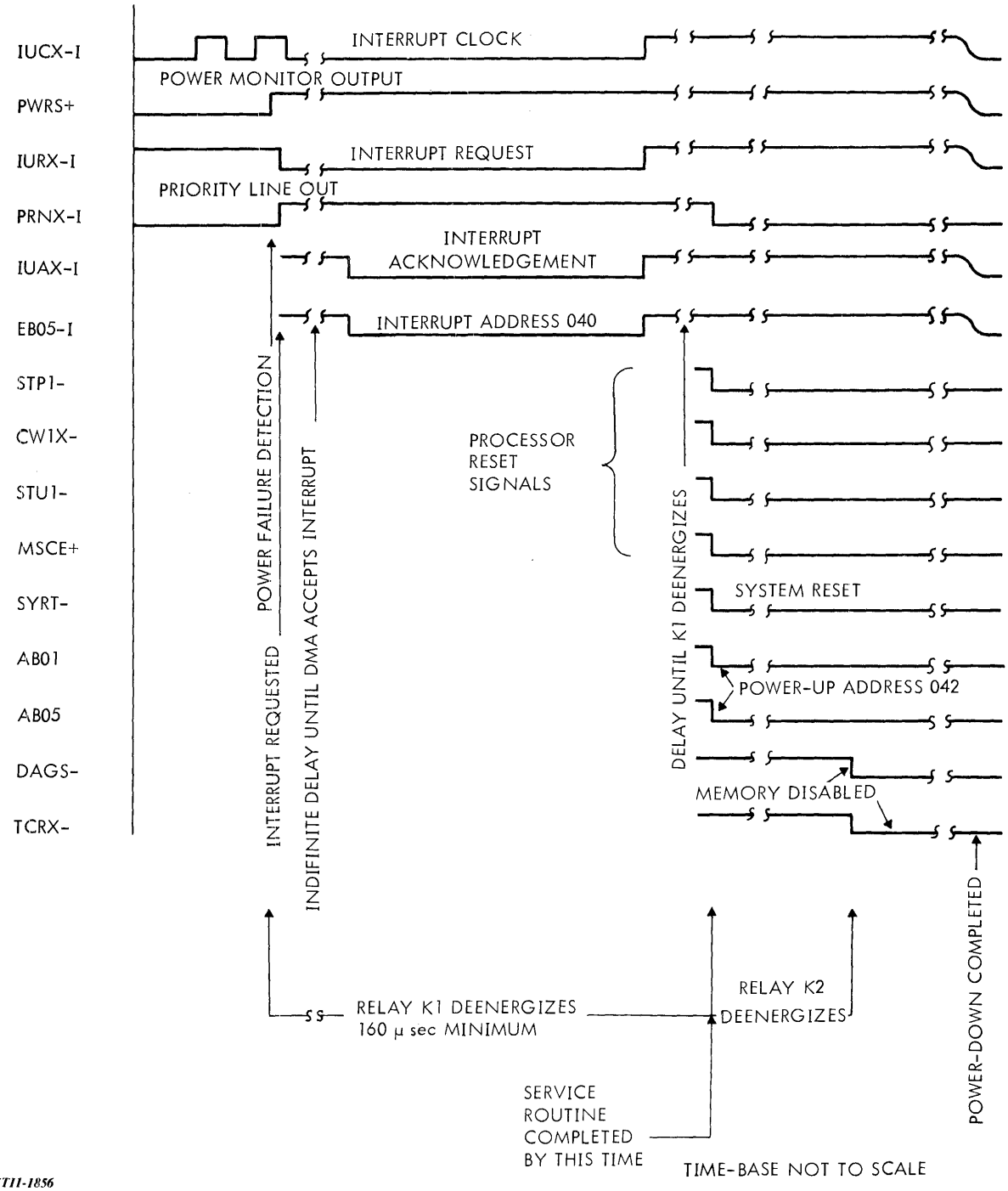


**Figure 1-3. Power-Down Signal Timing**

POWER FAILURE/RESTART

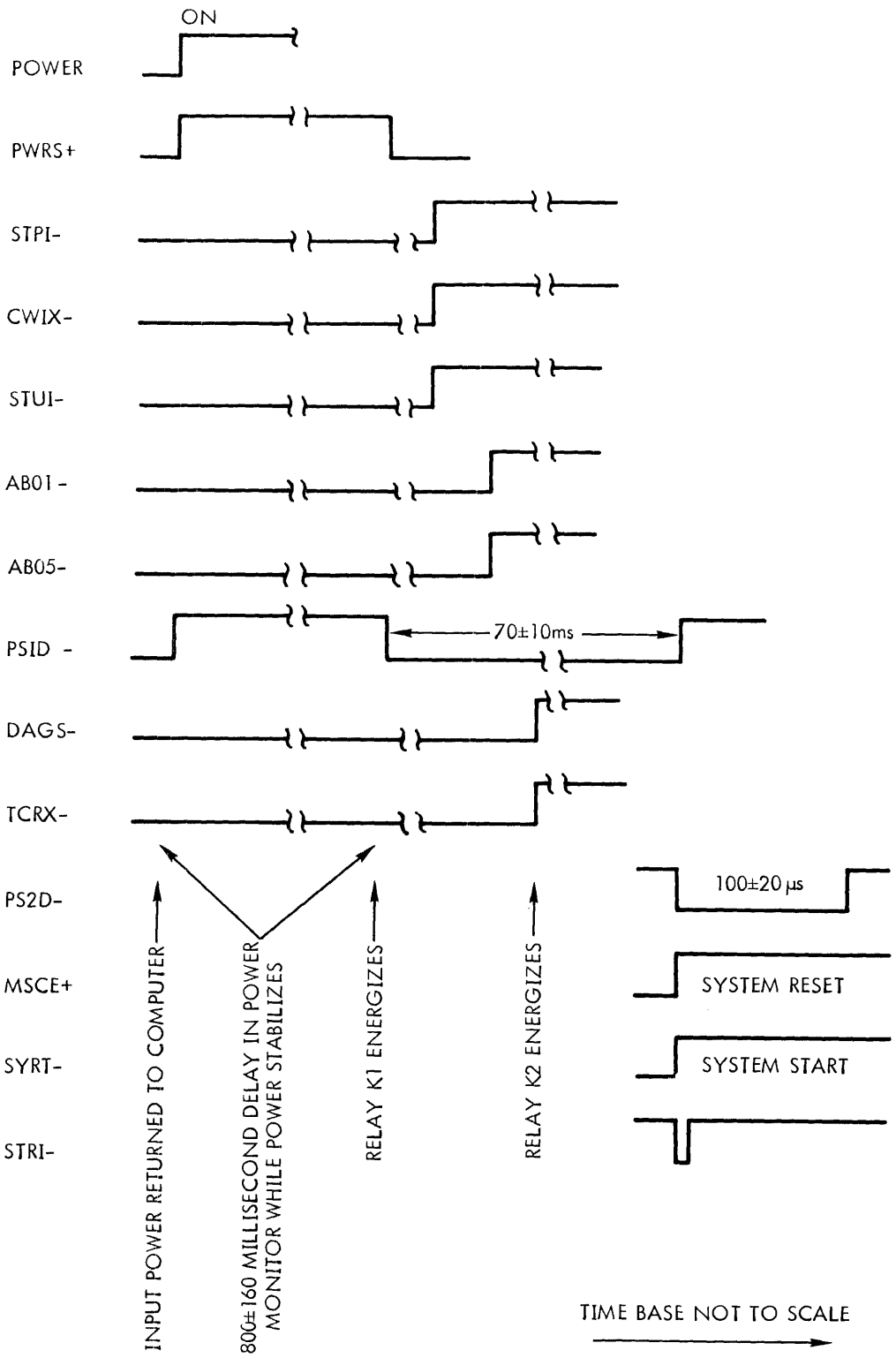


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Figure 1-4. Power-Up Signal Timing

## 1.2 PROGRAMMING

The user programs the PF/R service routines. The power-down service routine should store the contents of the volatile registers (A, B, and X), the overflow status, and the location of the next instruction in the interrupted program. Other functions can be included. The power-down memory addresses 040 and 041 normally contain a Jump and Mark instruction. The service routine must end with a Halt within 160 microseconds after the interrupt request is initiated.

The power-up service routine should put the stored contents of the volatile registers back into the registers, regenerate the overflow status, and resume the program. The power-up memory addresses 042 and 043 normally contain a Jump instruction. The service routine must be completed within 80 microseconds.

Although the PF/R has the highest interrupt priority in the system, at least one NOP instruction must be included in every otherwise uninterruptable sequence of instructions lasting 50 microseconds or longer. Two NOPs are required following an EXC instruction. These restrictions allow time for recognition of a power failure or turnoff.

An interrupt can only be detected during the last cycle of an instruction and then only if not inhibited. Detection of an interrupt is inhibited during the last cycle (and thus during the entire instruction) for the following instructions:

a. Halt (HLT)

b. All jump, jump-and-mark, or execution instructions when the jump condition is met (when the jump condition is not met these instructions are interruptable).

c. All I/O instructions.

d. All shift or rotation instructions.

e. All multiplication or division instructions.

In addition, detection of an interrupt is inhibited under the following conditions:

a. During the processor cycle immediately following an external control (EXC) instruction.

b. During the processor cycle immediately following a shift, rotation, multiplication, or division instruction during which a trap occurred.

c. During the first instruction executed when entering RUN mode if that instruction is a single-word instruction.

d. During a manual STEP operation.

e. When halted.

When program loops contain only uninterruptable instructions, detection of interrupts cannot occur. Thus, when detection of interrupts is imperative (e.g., when using the power failure/restart feature), at least one NO-OP must be added to such loops. Two NO-OPs are required following an external control instruction (EXC).

Data in process on peripherals (i.e., magnetic tape, paper tape, or magnetic disc devices) during a power failure will be lost.

Figure 1-5 shows a typical service routine for the PF/R.

## 1.3 INSTALLATION

The PF/R is installed in the field by Varian Data Machines customer service engineers. Logic diagrams, assembly layout, and wiring information are contained in the Volume II Maintenance Manual.

### 1.3.1 Preinstallation Requirements

Prior to installation of the PF/R, ensure proper operation of the computer with the diagnostic routines described in the maintenance manual.

### 1.3.2 Installation

Install the PF/R in slot 16 of the computer mainframe. Insert the card into the mounting guides with the component side of the card on your left as you face the rear of the 620.

Apply moderate pressure to the card, forcing the 122-terminal card-edge connector to seat firmly in the mating connector on the computer backplane. Take care to apply equal pressure to the upper and lower halves of the card to prevent damage to the backplane connector or to the nylon guides.

Adjust the threshold voltage according to section 3.4. Ensure proper operation of the PF/R, using a service routine (see figure 2-1) and the computer instruction test shown in chapter 6 of the 620 Test Programs Manual.

To remove the card, use a card puller (Titchener 1731 or equivalent).

POWER FAILURE/RESTART

```
000040                          ,ORG      ,040
000040   002000                 ,JMPM     ,STOP     POWER FAIL
000041   000200 R
000042   001000                 ,JMP      ,STRT     RESTART
000043   000210 R
000200                          ,ORG      ,0200     ARBITRARY ROUTINE LOCATION
000200   000000        STOP     ,ENTR     ,0
000201   050222                 ,STA      ,SAVE     SAVE A-REGISTER
000202   060223                 ,STB      ,SAVE+1   SAVE B-REGISTER
000203   070224                 ,STX      ,SAVE+2   SAVE X-REGISTER
000204   005001                 ,TZA      ,
000205   005511                 ,AOFA     ,
000206   050225                 ,STA      ,SAVE+3   SAVE OVERFLOW STATUS
000207   000000                 ,HLT      ,         STOP SYSTEM
000210   007400        STRT     ,ROF      ,
000211   010225                 ,LDA      ,SAVE+3   RESTORE OVERFLOW STATUS
000212   001010                 ,JAZ      ,*+3
000213   000215 R
000214   007401                 ,SOF      ,
000215   010222                 ,LDA      ,SAVE     RESTORE A-REGISTER
000216   020223                 ,LDB      ,SAVE+1   RESTORE B-REGISTER
000217   030224                 ,LDX      ,SAVE+2   RESTORE X-REGISTER
000220   001000                 ,JMP*     ,STOP     RETURN
000221   100200 R
000222   000000        SAVE     ,DATA     ,0,0,0,0  STATUS POOL
000223   000000
000224   000000
000225   000000
         000000                 ,END
```

**Figure 1-5. Typical Service Routine**

### 1.3.3 Threshold-Voltage Adjustment

Set the PF/R for the desired input threshold voltage as follows:

a. Connect the 620 primary power through a variable-voltage transformer and adjust the transformer output to 115V ac.

b. Turn on the 620, press SYSTEM RESET, load a HALT (000000) into memory address 042, disable the memory, and turn the power switch OFF.

c. Set the variable-voltage transformer to the desired threshold voltage (normally 104 ± 0.5V ac).

d. Turn the power switch ON, enable the memory, and select the P register.

e. Read the contents of the P register. Correct threshold adjustment causes the readout to alternate between 042 and 043, indicating that the power monitor is triggering on the ripple voltage of the sense-line input.

f. If there is a constant readout of 042, lower the threshold setting by turning potentiometer R2 clockwise until the readout alternates between 042 and 043.

If there is a constant readout 043, raise the threshold setting by turning potentiometer R2 counterclockwise until there is a constant reading of 042. Then turn R2 clockwise until the readout alternates between 042 and 043.

g. Threshold adjustment is now complete. Disable the memory, turn the power switch OFF, remove the extender card (if any) and the variable-voltage transformer, and restore the system to its operating configuration.

## 1.4 THEORY OF OPERATION

The PF/R monitors the status of the ac input power and controls the computer and memory accordingly. Figure 1-6 is a block diagram of the PF/R.

The PF/R checks the power indirectly by monitoring the Sense +5V line from the main computer power supply (figure 1-7). The voltage on this line is a direct function of the ac line voltage into the supply. This voltage is approximately +12V dc plus ripple when the ac line voltage is 115V ac.

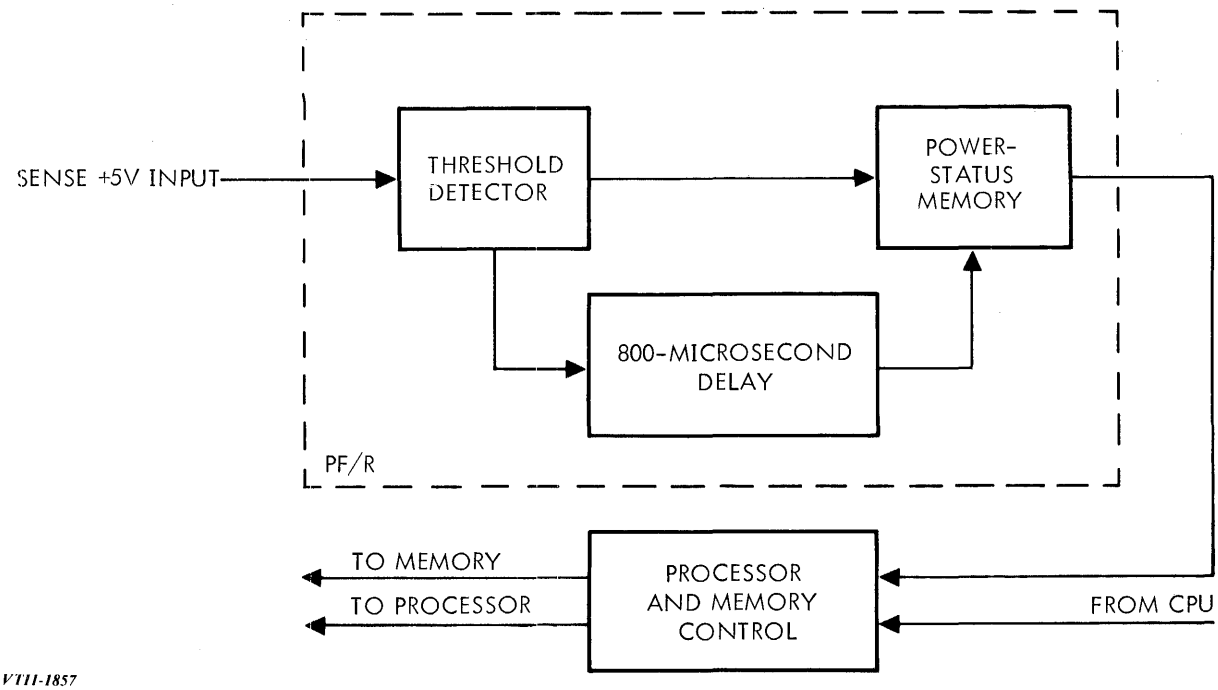


**Figure 1-6. PF/R Block Diagram**

### 1.4.1 Threshold Detector

The threshold detector is a discrete-component threshold detection circuit that monitors the Sense +5V line. When the voltage on the ac line drops below the threshold, a **power-down** condition is indicated. When the voltage is above the threshold, a **power up** condition is indicated.

### 1.4.2 800-Millisecond Delay

The 800-millisecond delay is a discrete-component circuit that provides an 800 ± 160 millisecond period on power up. When a power-up condition is detected, the 800 ± 160 millisecond delay occurs before the power-up status is recognized. This provides time for ac and dc power transients to settle out before initiating computer operations. When a power-down condition is detected, the power-down status obtains immediately.

### 1.4.3 Power-Status Memory

The power-status memory is a discrete-component latch circuit that stores the most recent power status detected by the threshold detector. Upon detection of power up, this latch is set at the end of the 800-millisecond delay. Upon detection of power down, it is reset immediately.

### 1.4.4 Processor Control

The processor control provides proper sequential control of processor functions during power up/down conditions.

**Power-up control:** On power up, the restart address (042) is placed in the P register (AB01−, AB05−, STP1−), a halt (042) is placed in the U-register (STU1−), the W register is cleared (CW1X−) and system reset (SYRT−) is applied. After approximately 870 milliseconds, SYRT− is removed and a start pulse (STR1−) is issued to the processor. The power-up subroutine then takes control of the computer. A power-down status is not recognized for the first 100 ± 20 microseconds following the start pulse.

**Power-down control:** On power down, PWRS+ goes true, K1 begins to de-energize, PS1F and PS2F are set, and an interrupt request (IURX-I) is sent to the processor. Upon receiving an interrupt acknowledgment (IUAX-I) from the processor, the interrupt address (040) is placed in the P register (EB05-I). The subroutine at the interrupt address then takes control of the computer. The PF/R allows 160 microseconds (minimum) for the subroutine to halt before returning to the initial (pre-power up) state.

### 1.4.5 Memory Control

The memory control provides proper sequential control of critical memory factors during a power up/down condition. This prevents power-switching transients from destroying the contents of memory and ensures that the memory timing and control circuitry starts from a reset condition.

**Power-up control:** On power up, the memory regulators are disabled, the memory timing control circuitry is held reset, and recognition of memory-start clocks is inhibited (DAGS−, TCRX−, MSCE+). At the end of the 800 ± 160 millisecond delay, the memory regulators are enabled and

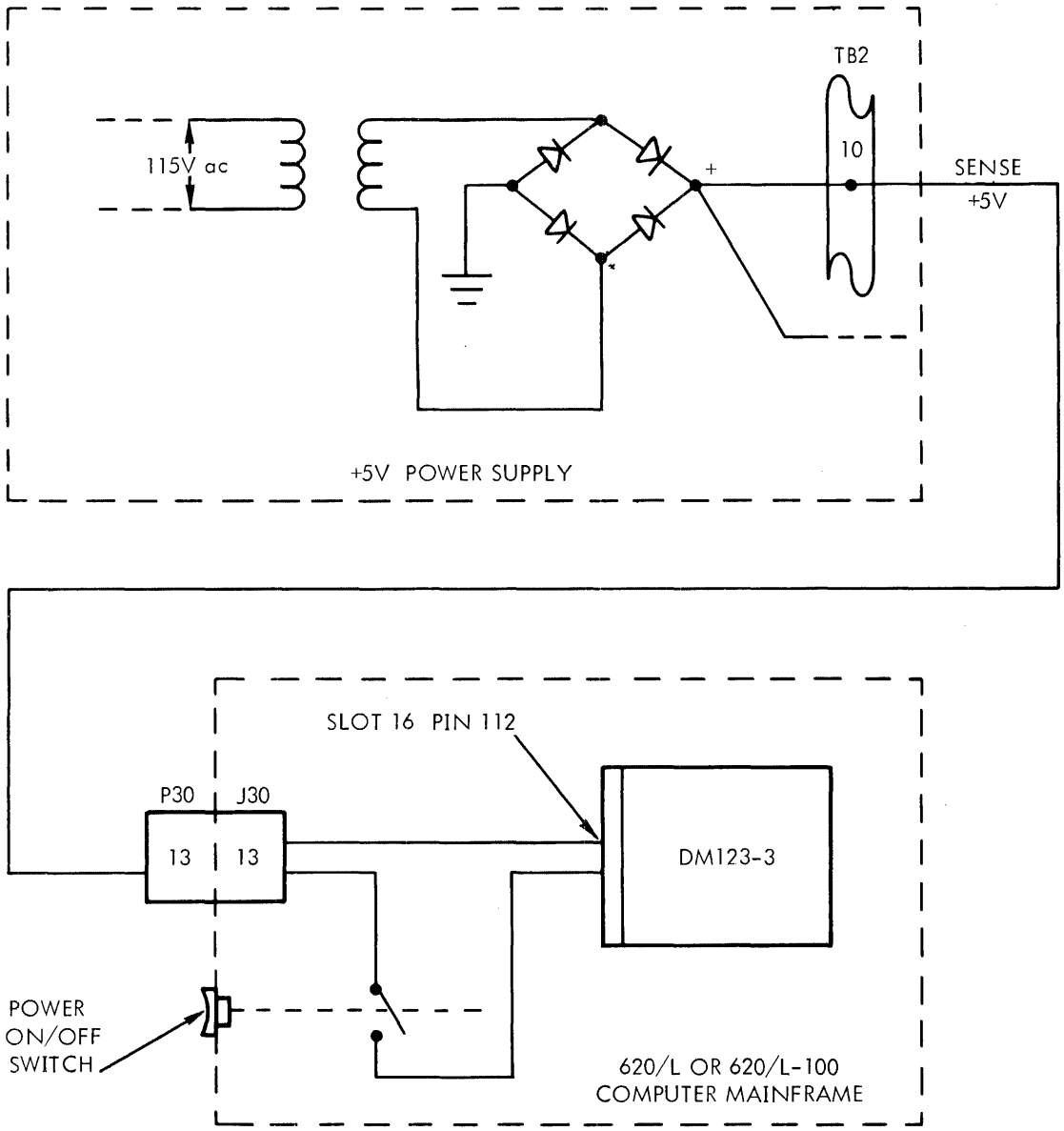


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**Figure 1-7. Source and Routing of Sense +5V**

the timing-and-control reset is removed. At the end of an additional 70 ± 10 milliseconds, recognition of memory-start clocks is enabled. The 70 ± 10 millisecond period allows power transients to settle out after enabling the memory regulators.

**Power-down control:** At least 160 microseconds after a power-down condition is detected, recognition of memory-start clocks is inhibited. Approximately 200 microseconds later, the memory regulators are disabled and the timing-and-control circuitry reset.

## 1.5 MAINTENANCE

For proper adjustment, the PF/R card must be adjusted while installed in the machine in which it will be used. Should the computer power supply be changed, or the PF/R card installed in a different machine, readjustment will be necessary.

The voltage at the power supply bridge is monitored using an adjustable threshold-detection circuit. This circuit is adjusted by varying the setting of potentiometer R2. To

raise the voltage threshold, turn the potentiometer adjustment-screw counter-clockwise. To lower the threshold, turn the adjustment-screw clockwise.

To adjust the PF/R:

a. With the computer power switch turned off, connect the processor to a variable-voltage transformer. Adjust the transformer output to 115V ac, or 230V ac.

b. With PF/R removed, turn on the processor. Apply system reset and then place a halt (000000) in memory location 042.

c. Disable memory and turn off the processor.

d. Install the PF/R in slot 16 of the mainframe.

e. Enable memory, select the P register, and turn on the processor. If the computer halts with 042 in the P register, the threshold is adjusted above the ac input voltage. If 043 appears in the P register, the threshold is below the ac input voltage.

f. Using a meter, adjust the output of the variable-voltage transformer to the desired value of the detection threshold. For a 115V ac system the threshold detection should be adjusted to 104.5 ± 0.5V ac. For a 230V ac system, the threshold detection should be adjusted to 208 ± 1V ac.

g. If 042 appears in the P register, turn the adjustment screw of potentiometer R2 clockwise until the PF/R just begins to trigger on the ripple found on the voltage at the sense point. At the threshold, the contents of the P-register will alternate between 042 and 043. Adjustment of the threshold is now complete.

h. If 043 appears in the P register, turn the adjustment screw of potentiometer R2 counter-clockwise until a constant 042 appears in the P register. Then turn the screw clockwise until the PF/R just begins to trigger on the ripple found on the voltage at the sense point. At the threshold, the contents of the P register will alternate between 042 and 043. Adjustment of the threshold is now complete.

On initial checkout or troubleshooting field problems, consider the following:

a. The delay between the application of power and the energizing of relay K1 is 800 ± 160 milliseconds.

b. The PS1D one-shot (IC 38), when triggered, produces a pulse of 70 ± 10 milliseconds.

c. The PS2D one-shot (IC 29), when triggered, produces a pulse of 100 ± 20 microseconds.

d. The K1 relay (only) has a drop-out transition time (break to first make) of 160 microseconds minimum.

## 1.5.1 Power-Up Sequence

The following order of events occurs upon power up:

a. The 800 ± 160 millisecond delay occurs before relay K1 begins to energize.

b. Signals STP1–, CW1X–, and STU1– go false at the beginning of the relay transition time as relay K1 begins to pull in.

c. AB01– and AB05– go false at the end of the relay transition time as the wiper makes first contact when pulling in. Also at this time, the leading edge of the 70 ± 10 millisecond pulse comes out of one-shot PS1D.

d. Several hundred microseconds after pull-in of relay K1 is completed, relay K2 pulls in. DAGS– and TCRX– go false at this time.

e. At the end of the 70 ± 10 millisecond period, one-shot PS2D is triggered, causing the leading edge of the 100 ± 20 microsecond period. MSCE + goes true, SYRT– goes false, and a several-hundred-nanosecond start pulse (STR1–) occurs.

f. The 100 ± 20 microsecond period ends.

## 1.5.2 Power Down Sequence

The following order of events occurs on power down or power failure:

a. Upon detection of a power down or power failure, relay K1 begins to de-energize.

b. A true-to-false transition of interrupt clock (IUCX-I) returns to the option before the transition of relay K1 to the de-energized state. Upon this transition of IUCX-I, interrupt request (IURX-I) goes true and priority output (PRNX-I) goes false.

c. An interrupt-acknowledgment pulse (IUAX-I) returns to the PF/R before the transition of relay K1 to the de-energized state is completed, but after IURX-I goes true. On the trailing edge of IUAX-I, IURX-I goes false. EB05-I goes true and remain true during the IUAX-I pulse.

d. When relay K1 completes the transition to the de-energized state, STP1–, CW1X–, STU1–, DAGS– and TCRX– go true (contact bounce may be noticed). On the first contact of the relay in the de-energized state, MSCE + goes false. SYRT–, AB01–, AB02– and PRNX-I go true, and relay K2 begins to de-energize.

### 1.5.3 PF/R Priority In/Out

When PRMX-I is true, PRNX-I is true except during and after the interrupt portion of the power down sequence, when it is false. When PRMX-I is false, PRNX-I is also false.

## 1.6 LIST OF PF/R SIGNAL MNEMONICS

| | |
|---|---|
| ABii | A bus bit ii |
| CW1X | Clear W register |
| DAGS | Memory data guard |
| EBii | E bus bit ii |
| IUAX | Interrupt acknowledge |
| IUCX | Interrupt clock |
| IURX | Interrupt request |
| MSCE | Master start clock enable |
| PFID | Pulse former output |
| PKIA | NC contact of relay K1 |
| PRMX-I | Priority input |
| PRMX | Priority interrupt |
| PRNX-I | Priority output |
| PRYL | Logic follower of relay K1 |
| PS1D | Output of 70 milliseconds one-shot |
| PS2D | Output of 100 microseconds one-shot |
| PS1F | Sequence flip-flop 1 |
| PS2F | Sequence flip-flop 2 |
| PWRS | Power status signal |
| STP1 | Set P register |
| STR1 | Start pulse |
| STU1 | Set U register |
| SYRT | System reset |
| TCRX | Timing and control reset |

# SECTION 2
# REAL-TIME CLOCK

## 2.1 DESCRIPTION

The real-time clock (RTC) is a mainframe feature of the Varian Data 620/L computer system. The RTC permits time-of-day accumulation of the recording of known time periods for program sequencing.

The RTC contains an internal time-base oscillator, a pulse counter, an interruption register, interruption control logic circuits, output line drivers, line receivers, an address decoder, an overflow detection circuit, and provision for an external time-base input (figure 2-1).

The RTC periodically interrupts the main program to initiate subroutines for the desired real-time functions. A divide-by-eight counter counts the pulses from the time-base oscillator and initiates incrementation interruptions.

The time-base oscillator generates signals at a predetermined frequency from 400 Hz to 80 kHz slected by the user. Unless otherwise specified, the RTC is delivered with the oscillator set at 8 kHz, thus causing the counter to initiate an incrementation interruption every millisecond. The frequency can be changed (see section 2.3.3).

A potentiometer on the RTC card permits fine adjustment of the frequency.

The RTC is on a 7-3/4-by-12-inch etched-circuit card. It shares this card with the power failure/restart (PF/R). The card is installed in slot 16 of the processor mainframe (figure 2-2).

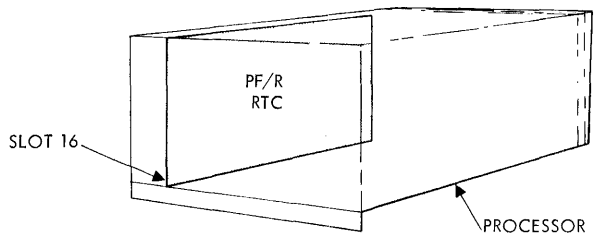



**Figure 2-2. RTC Installation**

### 2.1.1 Specifications

Table 2-1 gives the specifications of the RTC.

### 2.1.2 Functional Description

The address decoder detects the RTC device address (047) by decoding E bus signals EB00-I through EB05-I in the presence of an external control (EXC) signal on EB11-I.

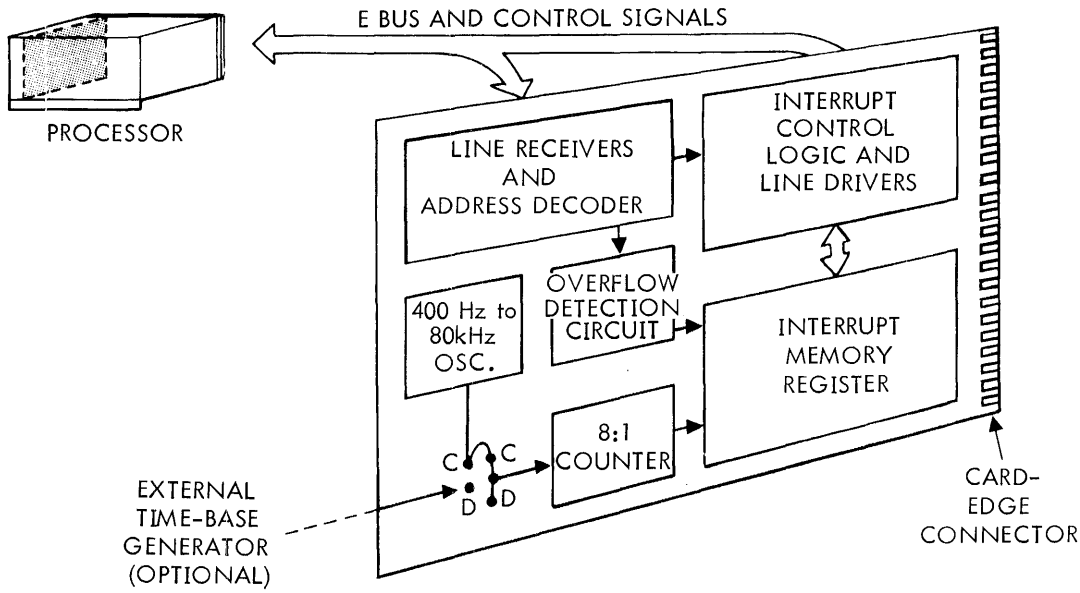



**Figure 2-1. RTC Configuration**

## REAL-TIME CLOCK

The RTC generates both incrementation and overflow interrupts.

Incrementation interupts are initiated by the divide-by-eight counter that counts the pulses from the time-base oscillator. Thus, these interrupts occur at 1/8 the oscillator frequency. They are recorded in the RTC interrupt register for handling by the processor. This processing uses storage address 044, which must contain an Increment and Replace (INR) instruction. Address 045 usually contains the operand incremented by the INR instruction.

Prior to incrementation, the contents of 045 are placed in the W register of the processor and the RTC overflow-detection logic checks the 15th bit (W14X+). If this bit is set, indicating a count of 040,000 or more, the RTC interrupt register records an overflow interrupt for handling by the processor. This processing uses storage addresses 046 and 047. They usually contain a Jump and Mark (JMPM) instruction, but can hold any suitable instruction.

The RTC interrupt register can record one incrementation and one overflow interrupt. When both are present, the processor processes the incrementation interrupt first. Either or both types of interrupt can be inhibited by the appropriate EXC command (section 2.2).

**Table 2-1. Real-Time Clock Specifications**

| Characteristic | Specifications |
|---|---|
| Organization | Contains input line receivers, an address decoder, an internal time-base oscillator, a divide-by-eight pulse counter, an overflow-detection circuit, an interrupt register, interrupt control logic circuitry, output line drivers, and external time-base input. |
| Size | One 7-3/4-by-12-inch etched-circuit card. |
| Interface | With the 620 I/O bus through the mainframe backplane connector If an external time-base is used, the jumper CC (figure 2-1) is removed and the input connected to slot 22, pin 28, with a return to pin 30. |
| Connectors | One 122-terminal card-edge connector mates with female connector on the backplane. |
| I/O Capability | Four external control (EXC) commands. |
| Types of Interrupt | Incrementation and overflow. |
| Device Address | RTC 047 |
| Storage Addresses: Incrementation Interrupt | 044 and 045 |
| Overflow Interrupt | 046 and 047 |
| Priority | Normally second only to the PF/R, but determined by order of placement on the I/O cable. |
| Input Power | +5V dc; +12V dc |
| Internal Time-Base Range | 400 Hz to 80 kHz, preselectable (50 to 10,000 incrementation interrupts per second). |
| Oscillator Output | Rectangular pulses, 0 to +5V dc, 40 to 60 percent duty cycle. |
| Logic Levels: | Negative logic:<br>True = 0.0 to +0.45V dc,<br>False = +2.8 to +3.6V dc.<br><br>Positive logic:<br>True = +2.4 to +5.5V dc,<br>False = 0.0 to +0.5V dc. |
| Operational Environment | 0 to 50 degrees C, up to 90 percent relative humidity without condensation. |

The interupt-control logic section decodes the EXC commands using the decoded address, the function code, and function ready signals. This allows incrementation or overflow interrupts, inhibits overflow interrupts, or initializes the RTC.

Initializing the RTC inhibits both types of interrupt and clears both the RTC interrupt register and the divide-by-eight counter. It does not stop or inhibit the oscillator. Thus, the RTC interrupt register will record an increment not more than 7/8 of an incrementation period later. However, no interrupt will occur without an EXC enabling command. If the interrupts remain inhibited, future increments will be lost until an enabling command is received and the recorded increment processed.

The RTC interrupt priority is determined by the order of placement of the RTC on the I/O cable.

## 2.2 PROGRAMMING

The user writes the RTC service routines. Storage addresses 044 and 045 process incrementation interrupts, where 045 contains the operand incremented by the INR instruction in 044. Addresses 046 and 047 contain a JMPM or other suitable instruction to process overflow interrupts.

An overflow interrupt initiates the RTC service routine. This routine should inhibit the RTC and other options normally capable of generating interrupts. The spacing of overflow interrupts can be adjusted by changing the value of the operand in address 045.

**NOTE**

If address 046 (interrupt location) contains a jump-and-mark instruction, all system PIMs (if any) are disabled.

The RTC service routine concludes with enabling instructions for the RTC and any other features previously inhibited, e.g., priority-interrupt modules (PIMs).

The RTC responds to the four EXC instructions listed in table 2-2. They can be issued at any time.

Figure 2-3 gives a typical service routine for the RTC.

**Table 2-2. RTC External Control Instructions**

| Mnemonic | Octal | Function | Description |
|---|---|---|---|
| EXC 147 | 100147 | Enable RTC | Enables both incrementation and overflow interrupts |
| EXC 447 | 100447 | Inhibit RTC (Initialize) | Inhibits all interrupts; resets interrupt register and divide-by-eight counter |
| EXC 247 | 100247 | Inhibit Overflow | Inhibits only overflow interrupts |
| EXC 347 | 100347 | Enable Increment/ Inhibit Overflow | Enables incrementation interrupts; inhibits overflow interrupts |

**Figure 2-3. Typical Service Routine for the RTC**

```
                    ***REAL TIME CLOCK INITIALIZATION CODING***

                    SET INTV = 1000 (INTERRUPTS DESIRED ONCE EACH SECOND)

          001750                ,EQU      ,1000

000044                          ,ORG      ,044          INITIALIZE LOCATIONS 044-
047

000044    040045                ,INR      ,*+1

000045    036031                ,DATA     ,040001-INTV

000046    002000    R           ,JMPM     ,TIMUP
```

Figure 2-3. Typical Service Routine for the RTC (continued)

```
                ***REAL TIME CLOCK OVERFLOW INTERRUPT SERVICE ROUTINE***

001000                          ,ORG        ,01000

001000    000000    TIMUP       ,ENTR                   PROGRAM COUNTER STORED HERE

001001    100247                ,EXC        0247        INHIBIT RTC OVERFLOW INTERRUPT

001002    051015                ,STA        ,SAVEA      SAVE CONTENTS OF A REGISTER

001003    006010                ,LDAI       ,040002-
INTV   REINITIALIZE RTC COUNTER
001004    036031

001005    050045                ,STA        ,045        REINITIALIZE PERIOD
(OTHER INSTRUCTIONS MAY BE INSERTED HERE)
001014    006010                ,LDAI       ,0          RESTORE CONTENTS OF A REGISTER

001015    000000

001015              SAVEA       ,BES        ,0

001016    100147                ,EXC        ,0147       ENABLE RTC OVERFLOW INTERRUPT

(REENABLE PIMs, IF ANY)

001017    001000                ,JMP*       ,TIMUP      RETURN TO POINT OF INTERRUPT

001020    101000    R

          000000                ,END
```

## 2.3 INSTALLATION

Varian Data Machines customer service engineers usually install the RTC when the system is assembled. Assembly layout, wiring information, and logic diagrams are provided at the time of purchase. The following paragraphs are for information only.

### 2.3.1 Preinstallation Requirements

Prior to installation of the RTC, ensure proper operation of the processor using the diagnostic test procedures described in Chapter 9 of the Maintenance Manual.

**External Time-Base Generator (Optional):** If an external time-base generator is to be used, perform the following installation procedure:

a. Remove the jumper wire marked C-C, connecting the output of the internal time-base oscillator (IC37, pin 12) to the input of the divide-by-eight counter (IC20, pin 5).

b. Add a jumper wire to the points marked D-D, connecting the external time-base receiver circuitry (IC24, pin 11) to the input of the divide-by-eight counter.

c. Connect the output of the external time-base generator to slot 16, pin 28, of the computer backplane.

d. Connect the return line to slot 16, pin 30.

NOTE

Signal ground of the external time-base line must be isolated from chassis ground of the external time-base generator (i.e., from the ac third-wire ground).

The following characteristics are required for the external time-base input signal.

| | | |
|---|---|---|
| a. | Wave shape: | Rectangular pulse, 40 to 60 percent duty cycle |
| b. | Pulse width: | 25 nanoseconds |
| c. | Logic levels: | 0.0 to +0.4V dc<br>+3.0 to +5.0V dc |
| d. | Loading TTL gate): | Source must sink 1.6 ma in zero state. |

### 2.3.2 Installation

Install the RTC in slot 16 of the processor mainframe by inserting the card into the mounting guides with the component side on your left when standing at the rear of the computer.

Apply moderate pressure to force the 122-terminal card-edge connector to seat firmly in the mating connector on the backplane. Take care to apply equal pressure to the upper and lower halves of the card to prevent damage to the backplane connector or the nylon guide.

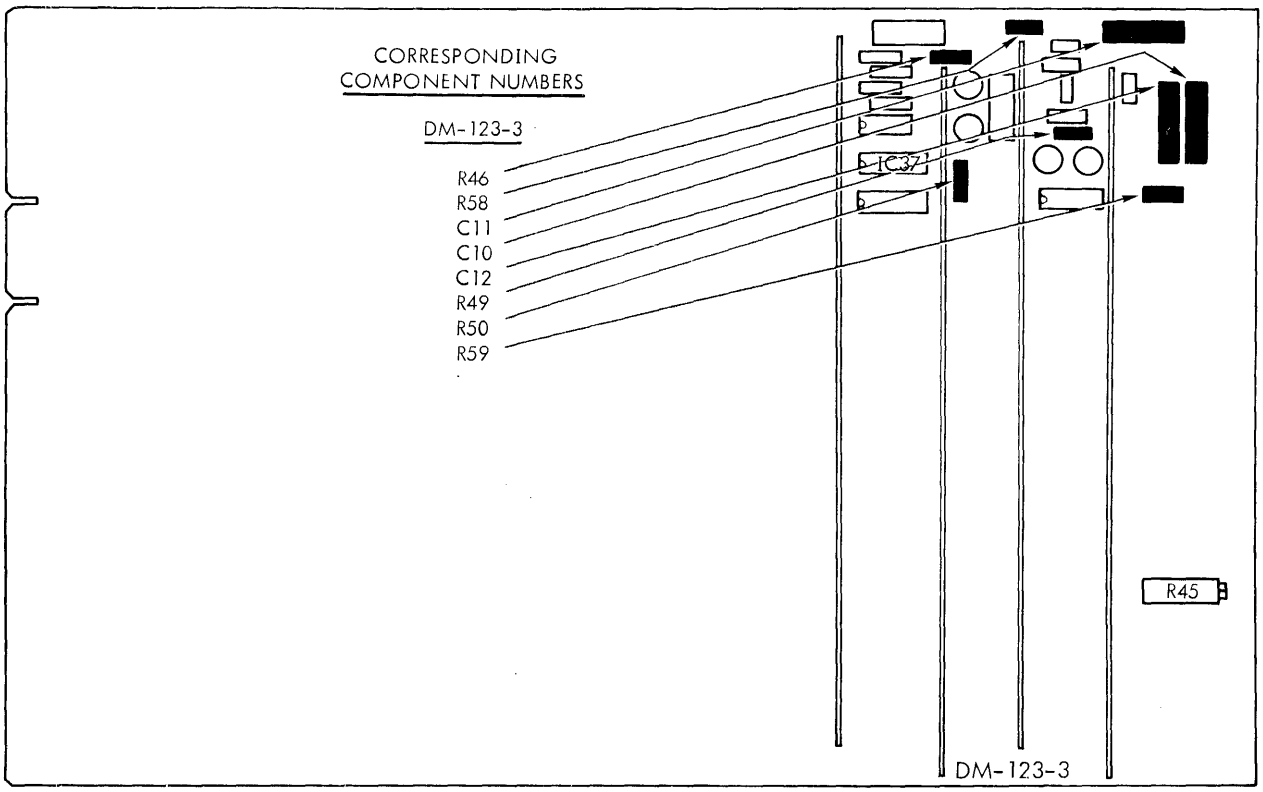
To remove the card, use an etched-circuit card puller (Titchener 1731 or equivalent).

### 2.3.3 Frequency Adjustment Procedures

Potentiometer R45 on the RTC card provides for precise adjustment of the internal time-base oscillator frequency. To monitor the frequency, connect an oscilloscope to pin 8 of IC37.

Turn the adjustment screw of R45 clockwise to lower the frequency or counterclockwise to raise it.

If the desired frequency lies outside the range available with the potentiometer, change the components indicated in figure 2-4 to the values indicated opposite the frequency in table 2-3.




VTII-1860

**Figure 2-4. Oscillator Components**

**Table 2-3. Values of Oscillator Components Corresponding to Output Frequencies**

| Frequency Range (kHz) | Component Number (figure 2-4) | | | | | |
|---|---|---|---|---|---|---|
| | Caps | R46 | R58 | R49 | R50 | R59 |
| 0.39-0.42 | 0.047 μF | 3.0K | 2.2K | 11.0K | 510Ω | 8.2K |
| 0.42-0.46 | | 2.8K | 1.6K | | | |
| 0.46-0.50 | | 2.4K | 1.5K | | | |
| 0.50-0.61 | | 1.6K | 1.2K | | | |
| 0.60-0.66 | | 1.5K | 1.0K | | | |

(continued)

Table 2-3. Values of Oscillator Components Corresponding to Output Frequencies (continued)

| Frequency Range (kHz) | Component Number (figure 2-4) | | | | | |
|---|---|---|---|---|---|---|
| | Caps | R46 | R58 | R49 | R50 | R59 |
| 0.65-0.74 | 0.033 μF | 2.4K | 1.2K | | | |
| 0.74-0.84 | | | 1.0K | | | |
| 0.84-0.94 | 0.022 μF | 2.8K | 1.8K | | | |
| 0.93-1.00 | | 2.4K | 2.0K | | | |
| 1.00-1.09 | | | 1.5K | | | |
| 1.10-1.24 | | | 1.0K | | | |
| 1.25-1.35 | | 2.0K | | | | |
| 1.33-1.39 | 0.015 μF | 2.4K | 2.0K | | | |
| 1.38-1.55 | | | 1.5K | | | |
| 1.46-1.71 | | | 1.3K | | | |
| 1.70-1.77 | | | 1.0K | | | |
| 1.76-1.90 | 0.01 μF | 2.4K | 2.2K | | | |
| 1.89-2.03 | | | 2.0K | | | |
| 2.00-2.20 | | 2.0K | 1.6K | | | |
| 2.16-2.36 | | | 1.5K | | | |
| 2.36-2.41 | 8200 pF | 2.8K | 2.2K | | | |
| 2.40-2.58 | | 2.4K | 2.0K | | | |
| 2.48-2.68 | 7500 pF | | | | | |
| 2.57-2.90 | 0.01 μ F | 1.5K | 1.0K | | | |
| 2.79-3.03 | 6800 pF | 2.4K | 2.0K | | | |
| 2.88-3.21 | 7500 pF | 2.0K | 1.5K | | | |
| 3.22-3.65 | 8200 pF | 1.5K | 1.0K | | | |
| 3.51-3.92 | 7500 pF | | | | | |
| 3.79-4.29 | 6800 pF | | | | | |
| 4.10-4.60 | 5600 pF | 1.6K | 1.2K | | | |
| 4.53-5.13 | | 1.5K | 1.0K | | | |
| 5.12-5.59 | 4300 pF | 2.0K | 1.5K | | | |
| 5.45-6.81 | | 1.6K | 1.1K | | | |
| 6.43-6.81 | 3300 pF | 2.4K | 2.0K | | | |
| 6.70-7.30 | | 2.2K | 1.6K | | | |
| 7.25-7.95 | 3300 pF | 2.0K | 1.5K | 11.0K | 510Ω | 8.2K |
| 7.85-8.62 | 2400 pF | 2.4K | 2.0K | | | |
| 8.10-8.90 | 2700 pF | | | | | |
| 8.62-9.74 | 3300 pF | 1.5K | 1.0K | | | |
| 9.74-10.9 | 2700 pF | | | | | |
| 10.7-12.3 | 2400 pF | | | | | |
| 11.9-13.1 | 1800 pF | 2.0K | 1.5K | | | |
| 12.8-13.8 | 1500 pF | 2.4K | 2.0K | | | |
| 13.6-14.4 | 1800 pF | 1.8K | 1.2K | | | |
| 14.3-16.2 | | 1.5K | 1.0K | | | |
| 15.6-17.0 | 1200 pF | 2.4K | 2.0K | | | |
| 15.8-18.1 | 1300 pF | 2.0K | 1.5K | | | |
| 17.3-19.5 | 1500 pF | 1.5K | 1.0K | | | |
| 18.7-20.0 | 1000 pF | 2.4K | 2.0K | | | |
| 19.7-22.2 | 1300 pF | 1.5K | 1.0K | | | |
| 21.3-23.2 | 1000 pF | 2.0K | 1.5K | | | |
| 22.0-23.9 | 1200 pF | 1.5K | 1.0K | | | |
| 22.6-24.5 | 1000 pF | 2.4K | 2.0K | 5.6K | | 4.3K |
| 24.4-26.7 | | 2.4K | 1.5K | | | |
| 25.5-28.6 | | 1.5K | 1.0K | 11.0K | | 8.2K |

Table 2-3. Values of Oscillator Components Corresponding to Output Frequencies (continued)

| Frequency Range (kHz) | Component Number (figure 2-4) | | | | |
|---|---|---|---|---|---|
| | Caps | R46 | R58 | R49 | R50 | R59 |
| 27.5-30.4 | | 1.8K | 1.3K | 5.6K | | 4.3K |
| 30.3-33.8 | | 1.5K | 1.1K | | | |
| 33.6-36.3 | 680 pF | 2.4K | 1.8K | | | |
| 37.0-40.4 | | 2.0K | 1.5K | | 430Ω | |
| 39.5-43.5 | | 1.6K | 1.3K | | | |
| 42.7-47.6 | | | 1.1K | | | |
| 47.3-53.2 | | 1.2K | 1.0K | | | |
| 49.3-55.6 | 820 pF | | | 2.4K | 330Ω | 1.8K |
| 53.3-61.0 | | 1.0K | 910Ω | | | |
| 61.4-65.9 | 680 pF | 1.2K | 1.0K | | | |
| 63.0-71.8 | | 1.0K | 910Ω | | | |
| 71.8-80.8 | 560 pF | 1.2K | 1.0K | | | |
| 76.3-86.8 | | 1.0K | 910Ω | | | |

Note: The values given in the "Caps" column are the values for each of the capacitors C10, C11, and C12. For any given frequency value, these capacitors are identical.

## 2.4 THEORY OF OPERATION

The RTC allows time-of-day accumulation or the generation of known time periods for program sequencing. Figure 2-5 is a block diagram of the RTC. Operation of each block are discussed below.

### 2.4.1 Line Receivers and Address Decoder

Line receivers interface the E-bus and control bus. In addition, several processor signals are inverted for use in overflow detection. The address decoder decodes E-bus signals EB00-I through EB05-I and EB11-I to detect the RTC device address (047).

### 2.4.2 Interrupt Control Logic

This logic uses the decoded address (RB47+), the function-code (EB06+, EB07+, EB08+), and the function-ready (FRYX+) signals to enable increment and overflow interrupts, to disable the overflow interrupt, or to initialize the RTC.

### 2.4.3 Overflow Detection Circuit

Prior to incrementation, this logic samples the 15th bit (W14X+) of the stored word. A true condition indicates a count of 040,000 or greater. If a true condition is found, an overflow interrupt is generated (IR01+) and stored in the interrupt memory register (SR01). Memory addresses 046 and 047 are reserved for the overflow interrupt. These locations can contain any suitable instruction, but will normally contain a jump-and-mark instruction.

### 2.4.4 Interrupt Memory Register

The interrupt memory register stores the occurrence of an increment and/or of an overflow until their interrupt requests are serviced by the computer. When both an increment and an overflow interrupt are stored in the interrupt memory register simultaneously, the increment interrupt will be serviced first, followed by the overflow interrupt. Either the overflow interrupt or both interrupts can be inhibited by an appropriate EXC instruction.

### 2.4.5 Interrupt Gating and Line Drivers

The interrupt gating interprets the states of interrupt-enable/disable (RENA) logic and the interrupt-memory (SR00 and SR01) logic in order to issue interrupt requests, to inhibit interrupt requests, and to provide control signals to the interrupt memory. The drivers are the interface to the E-bus and control bus.

### 2.4.6 Divide-by-Eight Counter

The divide-by-eight counter divides the frequency of the internal oscillator (or the optional external time-base) bt eight to increase the accuracy of the RTC. The interrupt rate is 1/8 the soure frequency.

### 2.4.7 External Time-Base Receiver

The external-time base receiver buffers the RTC from the optional external time base.

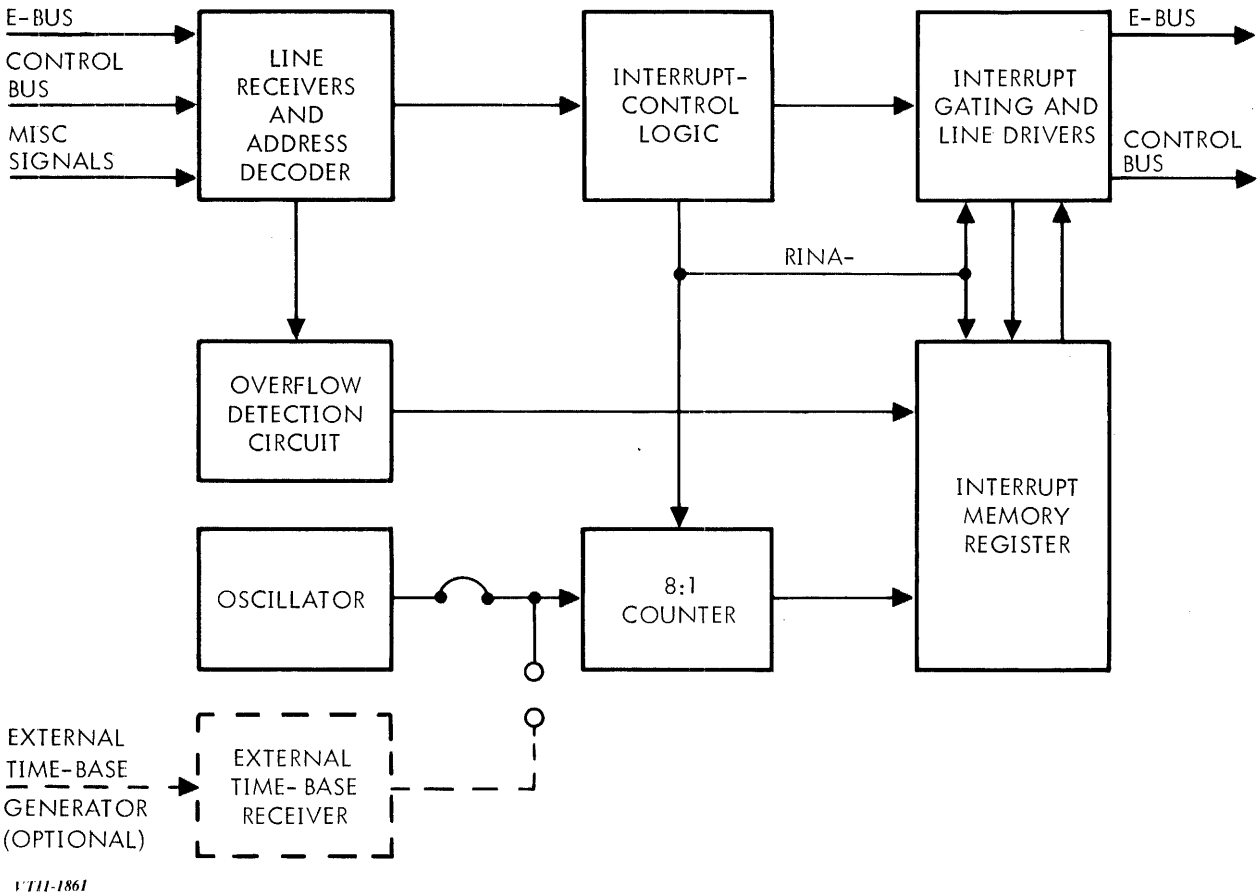



**Figure 2-5. RTC Block Diagram**

## 2.4.8 Internal Oscillator

The internal oscillator is a discrete-component oscillator with a frequency range of 400 Hz to 800 kHz. The user-selectable frequency is determined by choice of capacitor and resistor values in the oscillator circuity and can be changed, if desired, by replacement of one or more of a group of eight components. A 500-ohm potentiometer permits adjustment in a narrow range around the desired frequency. Unless otherwise specified, the RTC is delivered with the oscillator frequency set at 8 kHz, thereby generating an increment interrupt every millisecond.

For a complete listing of component values required to achieve the desired oscillator frequency, see section 2.3.3.

## 2.5 MAINTENANCE

On initial checkout or for troubleshooting field problems verify the following functions:

a. **DC Power to Board:** Check for +5V dc on pin 118, and +12V dc on pin 120.

b. **System Reset:** SYRT must disable the RTC, clear the divide-by-eight counter flip-flops (RK1F+ – RK4F+), increment interrupt sync and memory (SR00+, IR00+), overflow interrupt sync and memory (SR01+, IR01+), and increment interrupt enabler (RENA+).

c. **RTC Initialization:** The execution of EXC 447 disables both increment and overflow interrupts, and resets interrupt memories and the divide-by-eight counter.

d. **Enable Interrupts:** The execution EXC 147 enables both increment and overflow interrupts. Note that this instruction can be issued any time because an interrupt and an external control instruction cannot occur simultaneously on the E-bus. Ensure that RENA+ and ROVF+ are true (+5V).

e. **Disable Overflow Interrupt:** The execution of EXC 247 inhibits overflow inhibits overflow interrupts. Ensure that ROVF is false (0V).

f. **Enable Increment Interrupt and Disable Overflow Interrupt:** The execution of EXC 347 enables increment interrupt requests and inhibits overflow interrupt requests. RENA must be true (+5V) and ROVF false (0V).

g. **Oscillator and Divide-by-Eight Counter:** Unless otherwise specified, the oscillator is set at 8 kHz. Check for the oscillator output at pin 8 of IC 37. The divide-by-eight counter counts down from 8 kHz to 1 kHz. Check for this at IC 20 pin 12. If an external time-base is used, ensure that the output of the external time-base to the RTC is functioning properly at pin 28 on card slot 16.

Potentiometer R45 are for vernier adjustment of the RTC oscillator frequency. Section 2.3.3 describes the adjustment of the frequency and the components required for other frequency ranges.

## 2.6 LIST OF RTC SIGNAL MNEMONICS

Mnemonics used on RTC logic diagrams are listed below.

| Mnemonic | Description |
|---|---|
| ABii– | A Bus Bits (0-17): Common bus where adder and shift logic outputs, E bus input, and console are ORed to drive the C bus (CBii |
| AMED | Automatic Memory Enable/Disable. |
| CL1X + | Clock 1: Major clock function used to identify the start of a memory cycle. |
| CW1X– | Clear/Write: Enables Clear/Write signal. |
| DAGS– | Data Guard: Disables outputs of the memory regulator card during the turning on or off of power. It is controlled by the memory ENABLE/DISABLE switch and/or the PF/R (if any). |
| EBii-I | E Bus Bits (0-17): Main I/O lines. |
| FRYX-I | Function Ready Control: Terminates the address phase on the I/O line. |
| FRYX + | Function Ready: To I/O bus. |
| GND | Ground. |
| IAEX + | Interrupt Acknowledgment Enabler: Enables E bus and the resets for IR00 and IR01. |
| IMCX– | Increment Memory Control: Controls INR instructions. |
| IR00 + | Initial Interrupt-Register Bit 0: Holds and transfers incrementation interrupts to second interrupt-register bit 0. |
| IR01 + | Initial Interrupt-Register Bit 1: Holds and transfers incrementation interrupts to second interrupt-register bit 1. |
| IUAX-I | Interrupt Acknowledgment. |
| IUAX + | Interrupt Acknowledgment after inversion. |
| IUCX-I | Interrupt Clock. |
| IUCX + | Interrupt Clock after inversion. |
| IUIP + | Interrupt (Internal): Sets for every RTC-generated interrupt and enables detection of overflow interrupts. |
| IURC + | Interrupt Request (Internal). |
| IURX-I | Interrupt Request. |
| LP01 + | E Bus Enable: Enables EB01-I when an overflow interrupt is requested. |
| MSCE + | Memory Start Clock Enable: Enables the memory-start-clock pulse into the timing and control circuitry (DM106). |
| PF1D– | Pulse-Former 1 Delayed Output: Delayed output of the one-shot that forms start pulse STR1–. |
| PK1A– | PF/R Relay K1: Output of the normally-closed contact of the relay that provides 15 microseconds delay for the storage of register contents in the power-down sequence. |
| PRMX-I | Priority-In (I/O Bus). |
| PRMX + | Priority-In (I/O Bus) after inversion. |
| PRNX-I | Priority-Out (I/O Bus). |
| PRYL– | PF/R Relay Latch: Places 042 on the A bus during the power-up sequence and triggers the 800 milliseconds one-shot. |
| PS1D– | 70 milliseconds One-Shot. |
| PS2D– | 100 milliseconds One-Shot. |
| PS1F– | PF/R Sequencer Flip-Flop 1: During the power-up sequence, it initiates the start pulse to the computer, enables the MSCE removes SYRT, etc. |
| PS2F– | PF/R Sequencer Flip-Flop 2: Set upon detection of power failure. |

## REAL-TIME CLOCK

| Mnemonic | Description |
|---|---|
| PWRS + | Power Sense: True state indicates power-down. |
| RA47 + | RTC Address 047. |
| RB47 + | RTC Address 047 gated by IUAX–. |
| REF | Reference. |
| RENA + | RTC Enable. |
| RINA– | RTC Initialize: Resets all RTC flip-flops by either SYRT or the command 0100447. |
| RKIF– | RTC Divide-by-Eight Counter Flip-Flops (1-4). |
| ROSC + | RTC Oscillator Output. |
| ROVF + | RTC Overflow Enable Flip-Flop. |
| SETU + | Set U Register: Clock used to load C bus data into the U register. |
| SR00 + | Second Interrupt-Register Bit 0: Flip-flop requests incremenatation interrupt when set. |
| SR01 + | Second Interrupt-Register Bit 1: Flip-flop request overflow interrupt when set. |
| STP1– | Set P Register: Output of set gates selects P register. |
| STR1– | Start Pulse. |
| STU1– | Set U Register: Sets 042 in U register on power-up. |
| SYRT– | System Reset: Ground true signal in computer and on the I/O bus to reset computer and I/O devices. |
| TCRX– | Timing and Control Reset: Resets memory timing and control circuitry. |
| W14X + | W Register Overflow Detection: Detects the overflow and causes an RTC overflow interrupt. |
| XCLR– | External Clock Return. |
| XCLX + | External Clock: Input of the external time-base (if used). |

NOTES

NOTES

# EVALUATION QUESTIONNAIRE

**TITLE** _____

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The purpose of this questionnaire is to provide suggestions about how the manual can be improved when it is revised. It is the goal of the Technical Publications Department to make each manual as useful as possible and at the same time eliminate material that is of no practical value to the user or Customer Service Representative in acquiring initial knowledge of, and in maintaining, the equipment in the field. You, as the person working most closely with the manual and the equipment, can best provide the input needed by the writer to make the best possible manual for your use.

1. Please complete the following chart.

| CHAPTER/SECTIONS | MOST USEFUL | | | NEEDS MORE | | | | | | NEEDS LESS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Field Reference | Training | Big Picture Description | Illustration | Detailed Description | Detailed Description | Detailed Description | | | | | |
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2. Please list any errors, omissions, or difficult areas noticed in the manual. _____

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_____

3. Please list any improvements you recommend for this manual. _____

_____

_____

4. In an overall evaluation of this manual, how do you rate it in the following?

☐ Above Average ☐ Average ☐ Below Average

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