USER'S GUIDE
HIGH-LEVEL MULTIPLEXER MODULE

for use with

Varian 620 and V73 Series Computers

Publication No. 03-996 807A

February 1973

varian data machines/611 hansen way/palo alto/california 94303

PRINTED IN U.S.A.

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1. INTRODUCTION

1.1 GENERAL

The High-Level Multiplexer Module (MUX) is a hardware option that is used with an Analog-to-Digital Converter Module (ADCM) to expand the analog input capability of Varian 620 and V-73 series computers. The MUX provides high-level multiplexing and channel control.

The MUX provides 16 single-ended or differential external analog channels. In addition, the MUX can be expanded by adding 16-channel Multiplexer Expansion Modules (MUXEs). As many as 15 MUXEs can be attached to each MUX to provide a total of 256 analog input channels for the ADCM.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 illustrates the functional elements included in a MUX module. In a configuration employing MUXE modules, the MUX serves as the master module which contains the control logic. The MUXEs, called slave modules, contain only those circuits shown in the shaded area of Figure 1-1. The MUX shares the interface logic shown in the unshaded area with the MUXEs via jumper connections.

Device Address

One to 16 multiplexer and multiplexer expansion modules may be located at one device address. The device address may be any octal number from 40 to 77. The MUX, which is the master module, contains the device address decode logic.

Channel Selection Mode

The multiplexer is designed to operate in either sequential or random mode under computer program control. The mode of channel selection is specified by the program using a standard assembly language instruction.

In sequential mode, the multiplexer module's channel address decode logic automatically increments from channel address 1 to the final address prescribed by the program.

In random mode, the MUX channel address selection is controlled by the computer program. This mode permits the selection of MUX and MUXE channels in any sequence.

Channel Address Decode

The MUX channel address decode logic converts the eight-bit channel address received from the computer into two four-bit select codes. The select codes are routed to the channel on the MUX and MUXEs by jumper connections.

Channel Select Switches

The eight bits of the select code close either one or a pair of channel select switches on a single module to connect the analog input signal on a single-ended or differential channel to the ADCM. Only one switch or pair of switches can be closed at a time.

End of Scan Sense

The program can determine when a sequential channel selection operation is complete by issuing a Sense instruction that selects the End of Scan Sense input line. This line is logically true when the channel address decode selects the final channel address in a sequential operation.

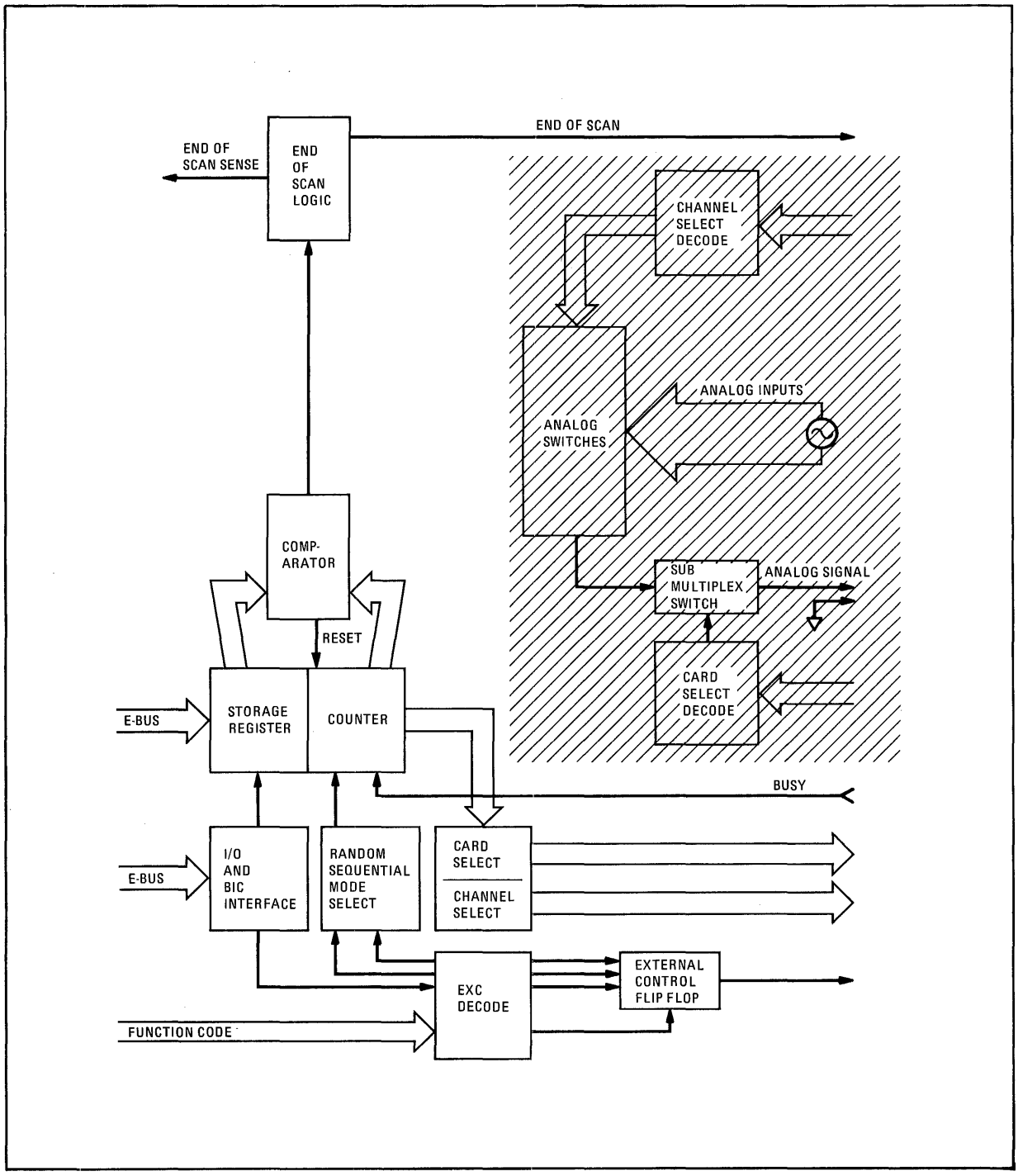


Figure 1-1. Multiplexer Module Block Diagram

2. PROGRAMMING

2.1 INTRODUCTION

This section describes Assembly Language programming techniques for operating the multiplexer. The program directs MUX operation in four ways:

- Determines mode of channel selection.
- Loads channel select codes into the channel select decode logic.
- Enables operation under BIC control.
- Tests for end of scan in sequential mode.

Note that generalized driver programs are supplied with the MUX to accomplish these same functions. Complete details regarding these programs may be found in the Analog-to-Digital Converter User's Guide (Publication No. 03-996 806). That manual also describes the software test package that is provided for ADCM/MUX checkout.

More detailed programming information may be found in the 620 series or V-73 system handbooks.

2.2 MODE SELECTION

The program specifies the mode of channel selection with an EXC instruction. Sequential channel selection is specified with an EXC 02YY instruction, where YY is the MUX device address. Random channel selection is specified with an EXC 01YY instruction.

2.3 CHANNEL SELECT CODE TRANSFER

The program specifies which channel is to be selected by an eight-bit channel select code. This code may be transferred from the computer's A or B register or from memory to the multiplexer using a standard data transfer out operation. The channel select code transfer is accomplished with one of the following instructions:

OAR 0YY Load device YY from A register

OBR 0YY Load device YY from B register

OME 0YY Load device YY from memory

where YY is the MUX device address

In sequential mode, only the channel select code for the final channel address is sent to the multiplexer; all channel select codes from channel address 1 to the final channel address are automatically generated by the MUX once the sequence has begun.

In random mode, each new channel select code requires a separate data transfer out operation. The data transfer operation may be under program control or BIC control.

2.4 BIC ENABLE

The program enables the multiplexer to operate in conjunction with the BIC by issuing an EXC 0YY instruction, where YY is the MUX device address. This sets the MUX in random mode. It also enables it to be connected to the BIC in order to pass random MUX channel addresses to the MUX from memory via the BIC.

2.5 END OF SCAN SENSE

The program can test the status of a sequential channel selection operation to determine if the MUX has selected the final channel (end of scan). It does this by issuing a SEN 0YY instruction. A true level on the computer's sense input line, SERX-I, indicates that the MUX has completed its scan.

The end of scan signal can also provide an interrupt to the program if the optional PIM module is employed.

2.6 TIMING CONSIDERATIONS

The channel selection process requires a delay of approximately 10 microseconds from the start of the channel selection to the start of the analog-to-digital conversion.

For each selected channel in random mode, the delay would extend from the transfer of the channel address to the signal that starts the ADC. In sequential mode, the delay would be required only before the first analog-to-digital conversion. In this case the subsequent delays are provided by the conversions themselves, since the subsequent channel selections occur at the beginning of the following conversions.

The source of the delay will depend on the source of the Start ADC signal. This may be a program start, timer start, or external start. Refer to the ADCM User's Guide for details regarding Start ADC signals.

2.7 PROGRAMMING EXAMPLES

The following examples illustrate typical instruction sequences for programming the multiplexer. In these examples, device address octal 60 is assumed for the ADCM, and device address octal 40 is assumed for the MUX.

Random Mode Channel Selection

```
        LDX     RAN1
        EXC     0140            Select random mode
RAN2    LDA     0,1             Relative to X
        OAR     040             Output to MUX
        LDB     RAN3            Load delay interval
RAN7    DBR                     Delay
        JBZ     RAN6            Check end of delay
        JMP     RAN7            Continue delay
RAN6    EXC     0160            Start ADC
        SEN     060, RAN8       If data ready, read ADC
        JMP     *-2             Not ready continue wait loop
```

```
RAN8    CIA     060         Read ADC
        STA     RAN4, 1     Store data word
        IXR
        TXA
        SUB     RAN5
        SUB     RAN1
        JAN     RAN2
        HLT
RAN1    DATA    xxx         Points to start of channel numbers
RAN3    DATA    xxx         Delay interval
RAN4    DATA    xxx         Points to start of data
RAN5    DATA    xxx         Number of data words
```

Sequential Mode Channel Selection

```
        LDX     SEQ1
        EXC     0240        Select sequential mode
        LDAI    020         Channel 16 is last channel
        OAR     040         Output to MUX
        LDBI    SEQ2        Load delay interval
SEQ5    DBR                 Delay
        JBZ     SEQ3        Check end of delay
        JMP     SEQ5        Continue delay
SEQ3    EXC     0160        Start ADC
        SEN     060, SEQ6   If data ready, read ADC
```

```
        JMP     *-2             Not ready, continue wait loop
SEQ6    CIA     060             Read ADC
        STA     0, 1            Store data word
        IXR
        TXA
        SUB     SEQ4
        SUB     SEQ1
        JAN     SEQ3
        HLT
SEQ1    DATA    xxx             Points to start of data
SEQ2    DATA    xxx             Delay interval
SEQ4    DATA    xxx             Number of data words
```

3. THEORY OF OPERATION

3.1 CHANNEL SELECTION

Channel selection may occur in either of two modes, random or sequential. For sequential operation, the program specifies a final channel address and the multiplexer automatically increments the channel selection logic from channel address 1 to the specified channel. In the random mode, the program specifies the next channel address for each selection; transfer of the channel address word may be under direct program control or BIC control.

Sequential Mode

The program prepares a set of multiplexer modules for sequential channel selection by issuing an EXC 02YY instruction. This sets the Sequential/Random latch on the master module, which remains set until the program issues an EXC 0YY or EXC 01YY instruction or until System Reset is generated. The Q output of the Sequential/Random latch conditions the channel address decode logic for sequential operation.

Following the mode selection, the final channel address is sent to the master module. At the start of the data transfer out operation that executes the address transfer, the DTOS latch is set. The true output of the DTOS latch conditions the clock input gate to the channel address buffer register in preparation for the DRYX (Data Ready) pulse.

The leading edge of DRYX loads the channel address present on E-bus lines EB00 through EB07 into the buffer register. The Load pulse also resets all eight channel address decode latches.

The output of the channel address buffer register and the eight channel address decode latches are set into an eight-bit comparator. The output of the comparator remains logically true (relative high) as long as the present channel address (output of the decode latches) is less than the final channel address (output of the buffer register).

In the sequential mode, the decode latches operate as an eight-bit cascade counter. The counter begins operation reset to 1 (by the Load pulse). A clock input pulse (CLK) increments the counter by one with each analog-to-digital conversion.

At the start of a conversion, the signal Busy from the ADCM goes true. This results in the positive-going pulse CLK, which clocks the channel address decode latches.

When the output of the decode latches equals the final channel address, the output of the comparator goes false (relative low). This output sets the End of Scan latch on the trailing edge of the final CLK pulse in the sequence. The true output of the End of Scan latch is gated with Convert, a signal that is the equivalent of Busy, to reset the channel address decode latches to 1.

If the program issues a SEN 0YY instruction, the signal Select 0 is generated. This signal gates the status of the End of Scan latch onto SERX-I, the sense input to the computer.

End of Scan, inverted once, is also available at P1-89 and may be used with the priority interrupt feature.

Random Mode

The program specifies the random channel selection mode by issuing an EXC 01YY instruction. This resets the Sequential/Random latch on the master module, which remains reset until the program issues an EXC 02YY instruction. The $\overline{Q}$ output of the latch conditions the channel address decode logic for random operation.

Following the mode selection, the address of the first channel to be selected is sent to the master module from the computer. Transfer of the address may be either a program-controlled or BIC-controlled data transfer out operation.

In either case, the channel address is loaded into the buffer register by the Load pulse, which is generated by DRYX from the computer and either DTOS (for program-controlled transfers) or Transfer Enable (for BIC-controlled transfers).

Load is also gated through with the mode signal, Random, to strobe the channel address from the buffer register into the decode latches. Each subsequent channel address transferred in the random mode is loaded into the buffer register and strobed into the decode latches in the same manner. The outputs of the comparator and End of Scan latch have no significance in the random mode.

3.2 CHANNEL SELECT SWITCHES

The eight bits output from the channel address decode logic are routed to the channel select switches on the master and slave modules. The four least significant bits (called A, B, C, and D) select one pair out of 16 pairs of select switches on each module. The four most significant bits (called E, F, G, and H) select the module to which the designated channel is connected.

If there are 32 channels located at the addressed module, the four most significant bits (E, F, G, and H) select the module, and select signal E inhibits one half of each pair of switches selected by signals A, B, C, and D. Jumper wires are required on the module for 32 channel operation. These jumpers are: JPRA, JPRB, JPRC, and JPRD.

The jumper wires used for routing the channel select bits are connected from module to module in an unchanging pattern. The jumper wires that route the card select bits are connected to either the inverting or noninverting input pins of the different modules in combinations that give each module a unique submultiplexing address.

A blanking pulse is applied to all channel select switches with each new channel address selection. This is done to assure that the switch(es) previously selected opens before the newly selected switch(es) closes.

The signal, Blanking, is generated by the Load pulse when channel selection is in the random mode and by CLK when channel selection is in the sequential mode.

3.3 SWITCH DESIGN

The switch design (Figures 3-1 and 3-2) is of monolithic construction with bipolars and FETS on one chip. The design incorporates the following features:

- P-Channel MOS FET switch and driver
- 20-Volt peak-to-peak signal handling capability
- TTL, DTL, RTL direct drive compatibility
- Voltage-limiting diodes protect MOS gate

Each element contains four MOS field-effect transistors designed to function as electronic switches. Level-shifting drivers enable a low-level input (0.8 to 2.0 V) to control the ON-OFF condition of each switch. In the ON state, each switch will conduct current equally well in either direction. In the OFF state, the switches will block voltages up to 20 V peak-to-peak. Positive logic "0" at the driver input will turn each switch ON. A common driver terminal V_L may be used to clock all four switches by switching the device from the ENABLE mode (≥ 4 V) to the INHIBIT mode (≤ 0.4 V).

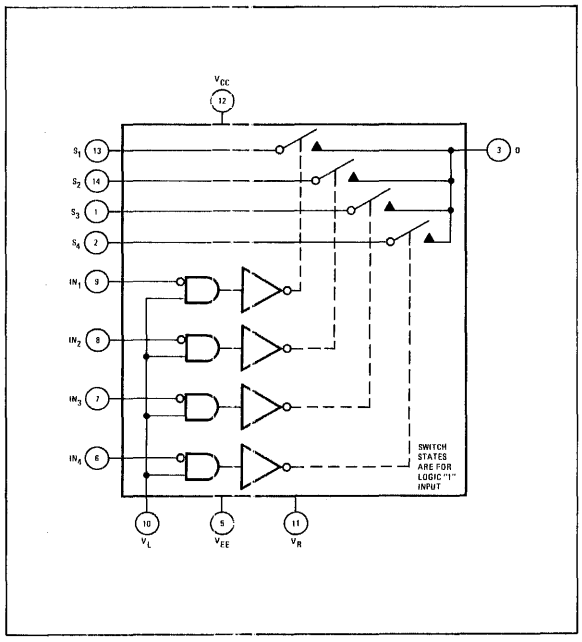


Figure 3-1. MOS Switches With Drivers-Functional Diagram

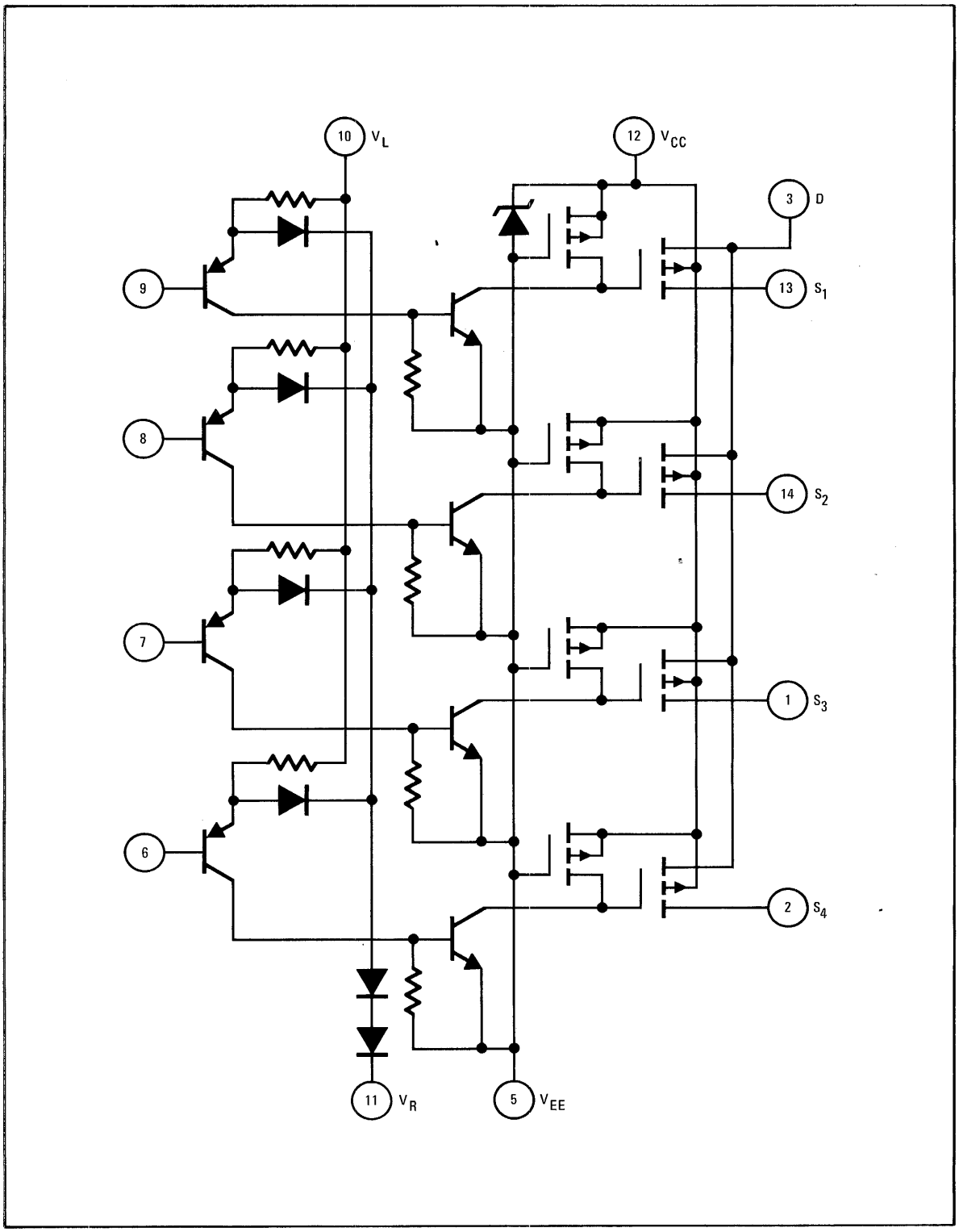


Figure 3-2. MOS Switches With Drivers - Schematic Diagram

4. INSTALLATION

4.1 PREREQUISITES

Each MUX or MUXE requires one card slot in either the mainframe or Memory Expansion/Peripheral Controller frame. No special slots are reserved for use by the multiplexer modules. However, those modules used in conjunction with an ADCM should be installed in adjacent slots to simplify backplane wiring. Note that an example of a typical ADCM/MUX installation procedure is given in the ADCM User's Guide.

A Power Supply Module (Part No. 620-88) must be installed when using one or more multiplexer modules. If a Power Supply Module has been previously installed and sufficient current is available to support the multiplexer modules, an additional module need not be installed.

4.2 INSTALLATION AND INTERCONNECTION

A MUX or MUXE is installed vertically, with its component side to the installer's left in 620/i and 620/L computers, and horizontally in the 620/f computer. Figure 4-1 illustrates a typical installation.

CAUTION

Do not install multiplexer modules in slots that have been previously wired to provide power to other modules; if the intended slot is already wired, remove any connections to power before installing the multiplexer module to protect its components. Refer to Table 4-1 for proper power connections.

The card is installed with the double pin edge pointing toward the installer. Proper orientation of the module is important since the cards are not keyed.

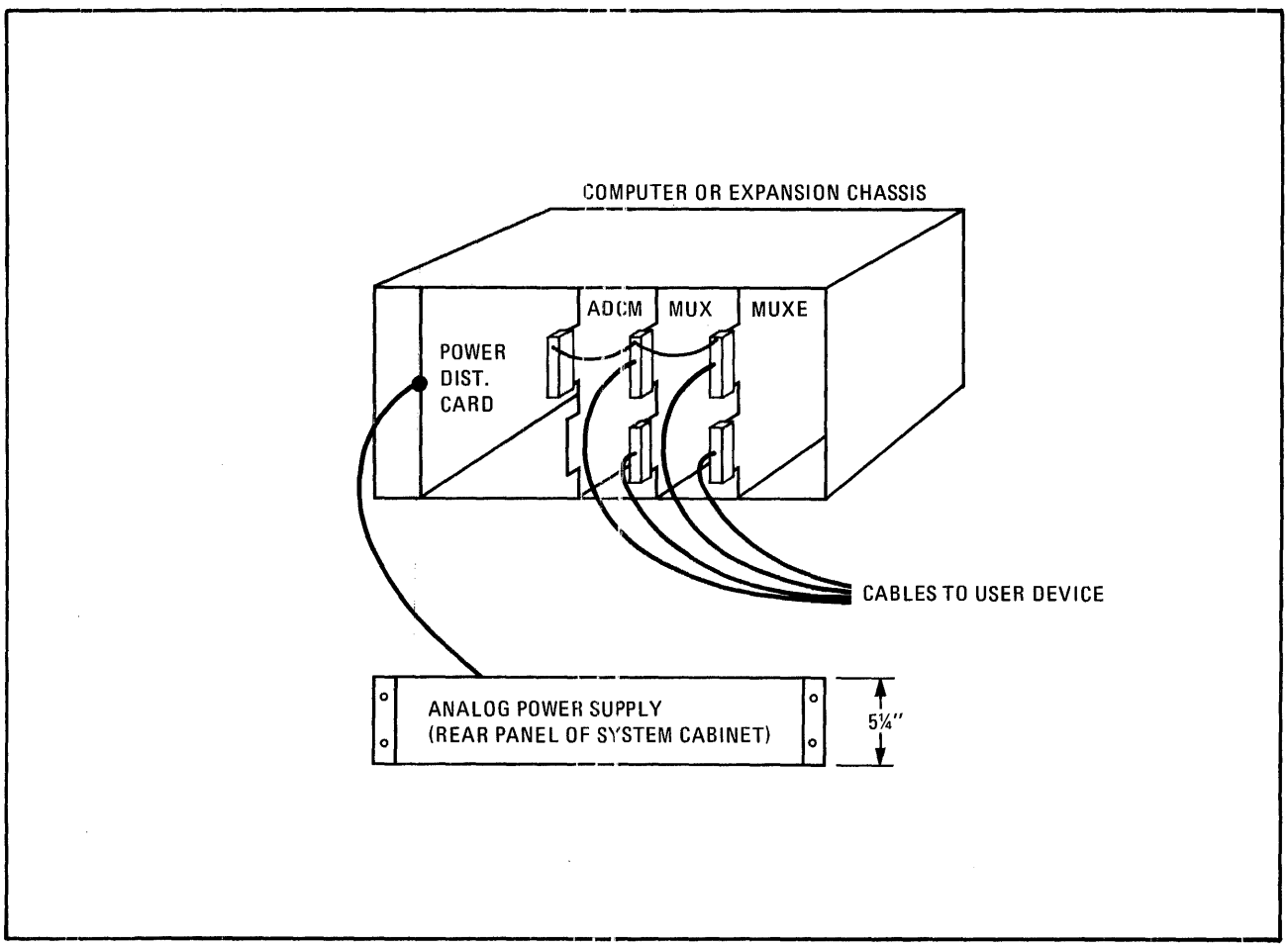


Figure 4-1. Typical Multiplexer Module Installation

Connections to external instruments include, for each multiplexer module, 16 single-ended or 16 differential analog inputs. All pin assignments for these connections are listed in Appendix A.

Power Supply Wiring

Connections to the multiplexer module must be made for five power supply voltages and senses, an analog ground, a digital ground and a digital ground sense. Table 4-1 lists the pin assignments on the MUX wirewrap backplane for these connections. When the multiplexer module is used with other modules (ADCMs, MUXEs, etc.) similar voltages should be tied together, and the voltage sense line should be brought from the mid-point of the voltage tie-line to a voltage sense line on the power supply wirewrap backplane.

The voltages and sense points for the power supply backplane are given in the Power Supply Manual (Publication No. 03-996-812).

Table 4-1. MUX Wirewrap Backplane Pin Connections for Power Supply

Power Supply Voltage	Multiplexer Pins
Digital Ground	P1-1, 22, 48, 51, 100, and 122
+5 Vdc	P1-118, 121
+15 Vdc	P1-111, 112
+20 Vdc	P1-107, 108
-15 Vdc	P1-113, 114
-22 Vdc	P1-109, 110
Analog Ground	P1-115

Device Address Wiring

Table 4-2 lists the jumper connections required to wire a device address for a multiplexer module. Although Table 4-2 lists the connections for device addresses 040 through 077, multiplexer modules are typically assigned device addresses 060 through 067. Note that P1-74 (Enable) is not normally used. It is available, however, and may be used as an additional addressing condition. For example, if two multiplexer modules are assigned the same device address, the Enable input can be used to permit only one module to respond to that address at a given time.

Card/Channel Selection Wiring

Tables 4-3 through 4-5 list the jumper connections required for preparing MUX and MUXE modules for card and channel selection. Note that Tables 4-3 and 4-5 apply only to those configurations in which MUXEs are used.

Table 4-3 shows the initial connections for daisy chain wirewrap of MUX and MUXE modules used in the same configuration.

Table 4-2. Multiplexer Module Device Address Wiring

Address	Wirewrap Jumpers (P1xx to P1xx)				
040	77 to 78	74 to 75	71 to 72	68 to 69	65 to 66
041	77 to 78	74 to 75	71 to 72	68 to 69	64 to 66
042	77 to 78	74 to 75	71 to 72	67 to 69	65 to 66
043	77 to 78	74 to 75	71 to 72	67 to 69	64 to 66
044	77 to 78	74 to 75	70 to 72	68 to 69	65 to 66
045	77 to 78	74 to 75	70 to 72	68 to 69	64 to 66
046	77 to 78	74 to 75	70 to 72	67 to 69	65 to 66
047	77 to 78	74 to 75	70 to 72	67 to 69	64 to 66
050	77 to 78	73 to 75	71 to 72	68 to 69	65 to 66
051	77 to 78	73 to 75	71 to 72	68 to 69	64 to 66
052	77 to 78	73 to 75	71 to 72	67 to 69	65 to 66
053	77 to 78	73 to 75	71 to 72	67 to 69	64 to 66
054	77 to 78	73 to 75	70 to 72	68 to 69	65 to 66
055	77 to 78	73 to 75	70 to 72	68 to 69	64 to 66
056	77 to 78	73 to 75	70 to 72	67 to 69	65 to 66
057	77 to 78	73 to 75	70 to 72	67 to 69	64 to 66
060	76 to 78	74 to 75	71 to 72	68 to 69	65 to 66
061	76 to 78	74 to 75	71 to 72	68 to 69	64 to 66
062	76 to 78	74 to 75	71 to 72	67 to 69	65 to 66
063	76 to 78	74 to 75	71 to 72	67 to 69	64 to 66
064	76 to 78	74 to 75	70 to 72	68 to 69	65 to 66
065	76 to 78	74 to 75	70 to 72	68 to 69	64 to 66
066	76 to 78	74 to 75	70 to 72	67 to 69	65 to 66
067	76 to 78	74 to 75	70 to 72	67 to 69	64 to 66
070	76 to 78	73 to 75	71 to 72	68 to 69	65 to 66
071	76 to 78	73 to 75	71 to 72	68 to 69	64 to 66
072	76 to 78	73 to 75	71 to 72	67 to 69	65 to 66
073	76 to 78	73 to 75	71 to 72	67 to 69	64 to 66

Table 4-2. Multiplexer Module Device Address Wiring (Con't.)

Address	Wirewrap Jumpers (P1xx to P1xx)				
074	76 to 78	73 to 75	70 to 72	68 to 69	65 to 66
075	76 to 78	73 to 72	70 to 72	68 to 69	64 to 66
076	76 to 78	73 to 75	70 to 72	67 to 69	65 to 66
077	76 to 78	73 to 75	70 to 72	67 to 69	64 to 66

Table 4-3. Daisy Chain Wirewrap Connections for Multiplexer Modules

Signal	MUX to	MUXE1 to . . .	to	MUXEn
Blanking	P1-42	P1-42	P1-42	P1-42
Chan Sel-A	P1-86	P1-86	P1-86	P1-86
Chan Sel-B	P1-85	P1-85	P1-85	P1-85
Chan Sel-C	P1-84	P1-84	P1-84	P1-84
Chan Sel-D	P1-102	P1-102	P1-102	P1-102
Card Sel-E	P1-104	P1-104	P1-104	P1-104
Card Sel-F	P1-105	P1-105	P1-105	P1-105
Card Sel-G	P1-90	P1-90	P1-90	P1-90
Card Sel-H*	P1-92	P1-92	P1-92	P1-92

*Card Sel-H must be inverted to operate modules with channel addresses above 128.

Signal	(Any slot below chan 129)	to	(Any slot above chan 128)	to	(Any slot above chan 128)
Card Sel-H	P1-92		P1-83		P1-83
H-Inverted			P1-94 to P1-92		P1-94 to P1-92

Table 4-4 shows the connections required on the master MUX module to provide 16-channel operation.

Table 4-4. MUX Wirewrap Jumpers

Signal	MUX	to	ADC
Busy	P1-101		P1-75
Decode 0	P1-91 to P1-80		
Decode 1	P1-93 to P1-81		

Table 4-5 lists the internal connections to wire each MUXE channel address group.

Table 4-5. MUXE Wirewrap Jumpers

Channel Address Group	From P1-xx	To P1-xx
17 to 32 (MUXE1)	93 95	80 81
33 to 48 (MUXE2)	95 96	80 81
49 to 64 (MUXE3)	96 97	80 81
65 to 80 (MUXE4)	97 98	80 81
81 to 96 (MUXE5)	98 99	80 81
97 to 112 (MUXE6)	99 103	80 81
113 to 128 (MUXE7)	103 106	80 81

Table 4-5. MUXE Wirewrap Jumpers (Con't)

Channel Address Group	From P-1xx	To P1-xx
129 to 144 (MUXE8)	91 93	80 81
145 to 160 (MUXE9)	93 95	80 81
161 to 176 (MUXE10)	95 96	80 81
177 to 192 (MUXE11)	96 97	80 81
193 to 208 (MUXE12)	97 98	80 81
209 to 224 (MUXE13)	98 99	80 81
225 to 240 (MUXE14)	99 103	80 81
241 to 256 (MUXE15)	103 106	80 81

Analog Input Wiring

Connections for analog inputs are available at J1 and J2. Inputs may be either single-ended or differential for a differential MUX. If the MUX is single-ended, only single-ended inputs may be used. Note that differential is recommended since it simplifies system grounding procedures.

To allow full scale swing ($\pm$ 10 V) of the analog input signal, that signal must be referenced to the multiplexer ground. Figure 4-2 illustrates a typical application where the differential input leads are connected to J1-9 (high) and J1-7 (low), and the ground

line is connected to J1-8 (analog ground). Figure 4-3 shows a typical application where the single-ended input lead is connected to J1-7 (low) and the ground line is connected to J1-8 (analog ground). Figure 4-4 illustrates ground connections for sequencing the analog output signal through the multiplexer modules to the ADCM.

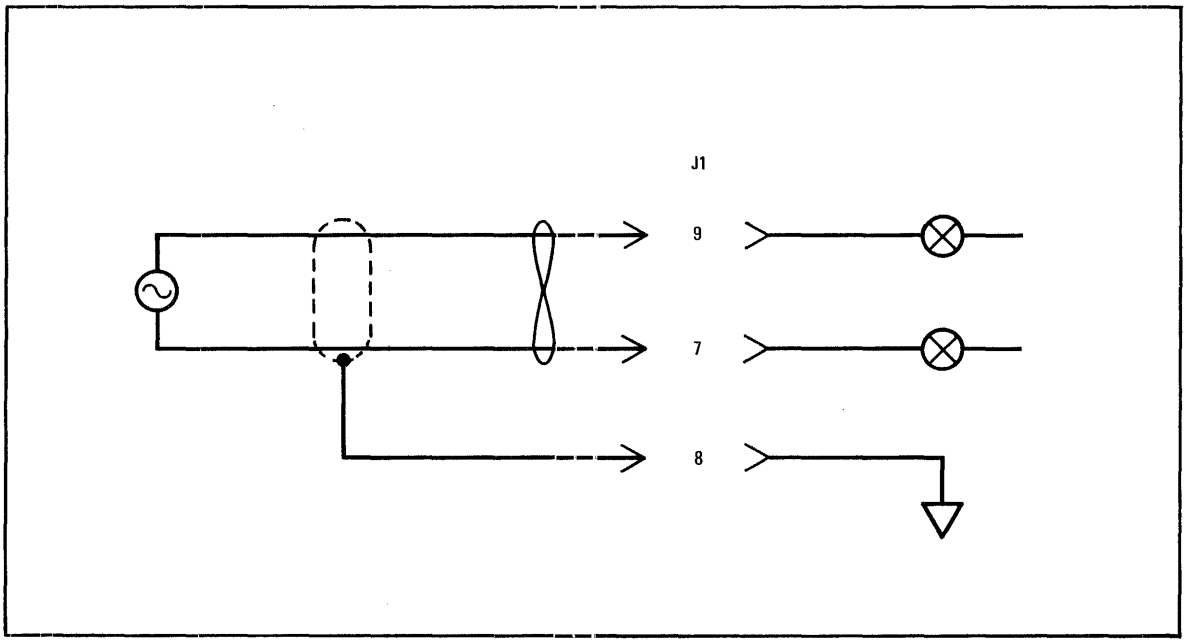


Figure 4-2. Differential Input Connections

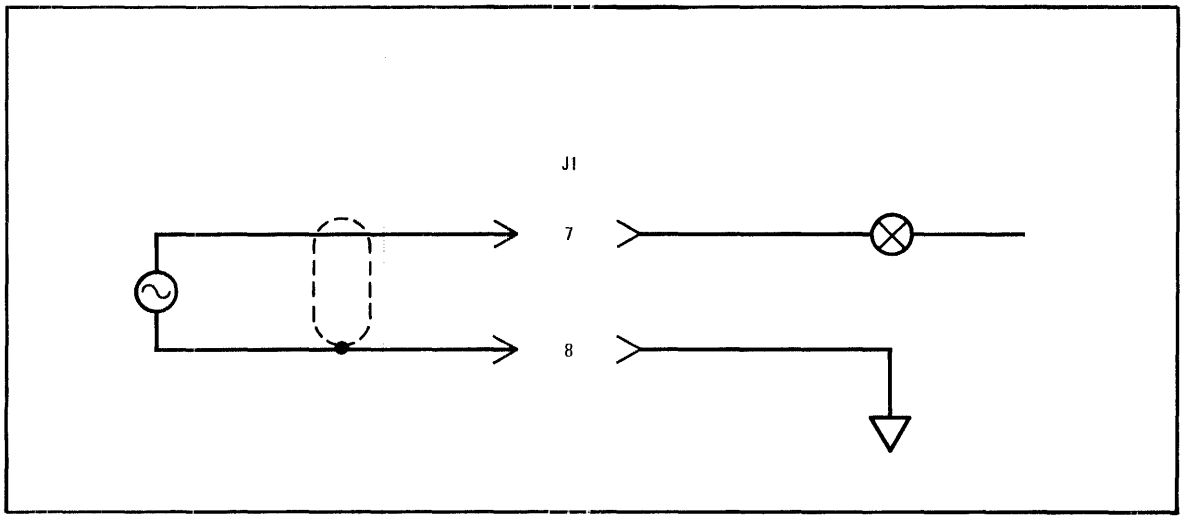


Figure 4-3. Single-Ended Input Connections

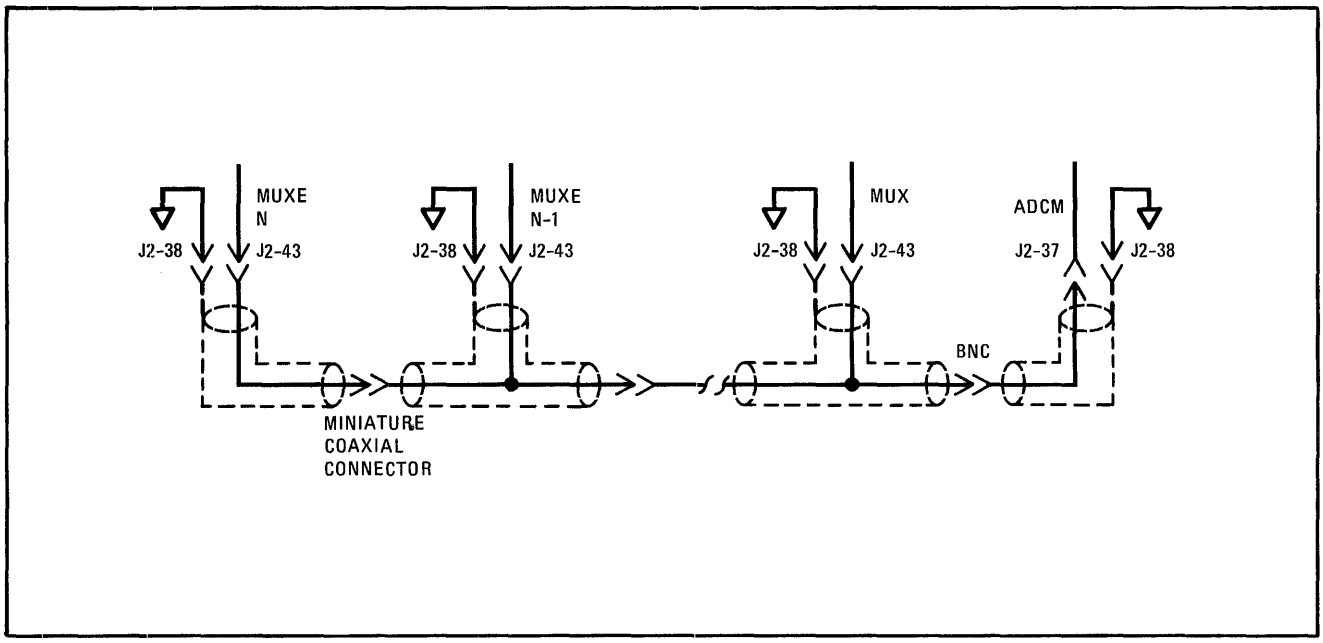


Figure 4-4. Daisy Chain of Analog Output Signal from MUX to ADCM

APPENDIX A: MUX PIN ASSIGNMENTS

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-1	Digital Ground	Digital Ground
-2	EB00-I	EB00-I
-3	Digital Ground	Digital Ground
-4	EB01-I	EB01-I
-5	Digital Ground	Digital Ground
-6	EB02-I	EB02-I
-7	Digital Ground	Digital Ground
-8	EB03-I	EB03-I
-9	Digital Ground	Digital Ground
-10	EB04-I	EB04-I
-11	EB05-I	EB05-I
-12	EB06-I	EB06-I
-13	EB07-I	EB07-I
-14	EB08-I	EB08-I
-15	EB09-I	EB09-I
-16	EB10-I	EB10-I
-17	EB11-I	EB11-I
-18	EB12-I	EB12-I
-19	Not used	Not used
-20	EB14-I	EB14-I
-21	EB15-I	EB15-I
-22	Digital Ground	Digital Ground
-23	Not used	Not used
-24	Digtial Ground	Digital Ground
-25	Not used	Not used
-26	Digital Ground	Digtial Ground
-27	FRYX-I	FRYX-I
-28	Digital Ground	Digital Ground
-29	DRYX-I	DRYX-I
-30	Digital Ground	Digital Ground
-31	SERX-I	SERX-I
-32	Digital Ground	Digital Ground
-33	Not used	Not used
-34	Digital Ground	Digital Ground
-35	Not used	Not used
-36	Digital Ground	Digital Ground
-37	Not used	Not used
-38	Digital Ground	Digital Ground

Pin No.	Name	Name Function
-39	Not used	Not used
-40	Digital Ground	Digital Ground
-41	Not used	Not used
-42	BLANK	BLANK Assures channel select switches break before make
-43	SYRT-I	SYRT-I Resets system logic
-44	IUAX-I	IUAX-I Interrupt acknowledge from computer
-45	Not used	Not used
-46	Not used	Not used
-47	Not used	Not used
-48	Digital Ground	Digital Ground
-49	TRQX-B	TRQX-B Transfer request from multiplexer to BIC
-50	TROX-B	TROX-B Not used
-51	Digital Ground	Digital Ground
-52	Not used	Not used
-53	Digital Ground	Digital Ground
-54	CDCX-B	CDCX-B Notifies BIC that multiplexer is connected
-55	Digital Ground	Digital Ground
-56	DCEX-B	DCEX-B Connect signal from BIC
-57	Digital Ground	Digital Ground
-58	TAKX-B	TAKX-B Transfer request acknowledge from BIC
-59	Digital Ground	Digital Ground
-60	DESX-B	DESX-B Disconnect from BIC
-61	Not used	Not used
-62	Not used	Not used
-63		Output for EXC 3 latch
-64	EB00+	EB00+ Jumper connection for wiring device address
-65	EB00-	EB00- Jumper connection for wiring device address
-66	EB0I+	EB0I+ Jumper connection for wiring device address
-67	EB01+	EB01+ Jumper connection for wiring device address
-68	EB01-	EB01- Jumper connection for wiring device address
-69	EB1I+	EB1I+ Jumper connection for wiring device address
-70	EB02+	EB02+ Jumper connection for wiring device address
-71	EB02-	EB02- Jumper connection for wiring device address
-72	EB2I+	EB2I+ Jumper connection for wiring device address
-73	EB03+	EB03+ Jumper connection for wiring device address
-74	EB03-	EB03- Jumper connection for wiring device address
-75	EB3I+	EB3I+ Jumper connection for wiring device address
-76	EB04+	EB04+ Jumper connection for wiring device address

BACKPLANE WIRING

Pin No.	Name	Name Function
P1-77	EB04-	EB04- Jumper connection for wiring device address
-78	EB4I+	EB4I+ Jumper connection for wiring device address
-79	ENABLE	ENABLE Not normally used
-80	H	H Jumper connection for wiring card select code
-81	G	G Jumper connection for wiring card select code
-82	F	F Jumper connection for wiring card select code
-83	E	E Jumper connection for wiring card select code
-84	C	C Jumper connection for wiring channel select code
-85	B	B Jumper connection for wiring channel select code
-86	A	A Jumper connection for wiring channel select code
-87	Not used	Not used
-88	Not used	Not used
-89	EOS	EOS End of scan output to PIM
-90	G	G Jumper connection for wiring card select code
-91	Not used	Not used
-92	H	H Jumper connection for wiring card select code
-93	Not used	Not used
-94	H	H Jumper connection for wiring card select code
-95	Not used	Not used
-96	Not used	Not used
-97	Not used	Not used
-98	Not used	Not used
-99	Not used	Not used
-100	Digital Ground	Digital Ground
-101	Busy	Busy Busy input from ADCM
-102	D	D Jumper connection for wiring channel select code
-103	Not used	Not used
-104	E	E Jumper connection for wiring card select code
-105	F	F Jumper connection for wiring card select code
-106	Not used	Not used
-107	+20 V	+20 V
-108	+20 V	+20 V
-109	-20 V	-20 V
-110	-20 V	-20 V
-111	+15 V	+15 V
-112	+15 V	+15 V
-113	-15 V	-15 V
-114	-15 V	-15 V
-115	Analog Ground	Analog Ground
-116	Not used	Not used
-117	Not used	Not used

Pin No.	Name	Name Function
-118	+5 V	+ 5 V
-119	Not used	Not used
-120	Not used	Not used.
-121	+5 V	+5 V
-122	Digital Ground	Digital Ground

TERMINAL EDGE CONNECTOR WIRING

Pin No.	Name	Name Function
J1-1	Not used	Not used
-2	Not used	Not used
-3	Not used	Not used
-4	Not used	Not used
-5	Not used	Not used
-6	Not used	Not used
-7	CH-9L	CH-9L Analog input channel (DIFF and Single Ended)
-8	Analog Ground	Analog Ground
-9	CH-9H	CH-9H Analog input channel (DIFF only)
-10	Analog Ground	Analog Ground
-11	CH-10L	CH-10L Analog input channel (DIFF and Single Ended)
-12	Analog Ground	Analog Ground
-13	CH-10H	CH-10H Analog input channel (DIFF only)
-14	Analog Ground	Analog Ground
-15	CH-11L	CH-11L Analog input channel (DIFF and Single Ended)
-16	Analog Ground	Analog Ground
-17	CH-11H	CH-11H Analog input channel (DIFF only)
-18	Analog Ground	Analog Ground
-19	CH-12L	CH-12L Analog input channel (DIFF and Single Ended)
-20	Analog Ground	Analog Ground
-21	CH-12H	CH-12H Analog input channel (DIFF only)
-22	Analog Ground	Analog Ground
-23	CH-13L	CH-13L Analog input channel (DIFF and Single Ended)
-24	Analog Ground	Analog Ground
-25	CH-13H	CH-13H Analog input channel (DIFF only)
-26	Analog Ground	Analog Ground
-27	CH-14L	CH-14L Analog input channel (DIFF and Single Ended)
-28	Analog Ground	Analog Ground
-29	CH-14H	CH-14H Analog input channel (DIFF only)
-30	Analog Ground	Analog Ground
-31	CH-15L	CH-15L Analog input channel (DIFF and Single Ended)
-32	Analog Ground	Analog Ground
-33	CH-15H	CH-15H Analog input channel (DIFF only)

Pin No.	Name	Name Function
-34	Analog Ground	Analog Ground
-35	CH-16L	CH-16L Analog input channel (DIFF and Single Ended)
-36	Analog Ground	Analog Ground
-37	CH-16H	CH-16H Analog input channel (DIFF only)
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Not used	Not used
-41	Not used	Not used
-42	Not used	Not used
-43	Not used	Not used
-44	Not used	Not used
J2-1	Not used	Not used
-2	Not used	Not used
-3	Not used	Not used
-4	Not used	Not used
-5	Not used	Not used
-6	Not used	Not used
-7	CH-1L	CH-1L Analog input channel (DIFF and Single Ended)
-8	Analog Ground	Analog Ground
-9	CH-1H	CH-1H Analog input channel (DIFF only)
-10	Analog Ground	Analog Ground
-11	CH-2L	CH-2L Analog input channel (DIFF and Single Ended)
-12	Analog Ground	Analog Ground
-13	CH-2H	CH-2H Analog input channel (DIFF only)
-14	Analog Ground	Analog Ground
-15	CH-3L	CH-3L Analog input channel (DIFF and Single Ended)
-16	Analog Ground	Analog Ground
-17	CH-3H	CH-3H Analog input channel (DIFF only)
-18	Analog Ground	Analog Ground
-19	CH-4L	CH-4L Analog input channel (DIFF and Single Ended)
-20	Analog Ground	Analog Ground
-21	CH-4H	CH-4H Analog input channel (DIFF only)
-22	Analog Ground	Analog Ground
-23	CH-5L	CH-5L Analog input channel (DIFF and Single Ended)
-24	Analog Ground	Analog Ground
-25	CH-5H	CH-5H Analog input channel (DIFF only)
-26	Analog Ground	Analog Ground
-27	CH-6L	CH-6L Analog input channel (DIFF and Single Ended)
-28	Analog Ground	Analog Ground
-29	CH-6H	CH-6H Analog input channel (DIFF only)
-30	Analog Ground	Analog Ground

Pin No.	Name	Name Function
-31	CH-7L	CH-7L Analog input channel (DIFF and Single Ended)
-32	Analog Ground	Analog Ground
-33	CH-7H	CH-7H Analog input channel (DIFF only)
-34	Analog Ground	Analog Ground
-35	CH-8L	CH-8L Analog input channel (DIFF and Single Ended)
-36	Analog Ground	Analog Ground
-37	CH-8H	CH-8H Analog input channel (DIFF only)
-38	Analog Ground	Analog Ground
-39	Not used	Not used
-40	Not used	Not used
-41	Not used	Not used
-42	Not used	Not used
-43		Analog output to ADCM
-44	Not used	Not used

APPENDIX B: SPECIFICATIONS

GAIN AND ACCURACY

Voltage Gain	+1 or +10
Accuracy	± 0.01% of F.S.
Gain Temp. Coefficient	± 10 PPM/°C

INPUT SPECIFICATIONS

Signal Voltage	± 10 V or ± 1 V
Maximum Source Impedance	1 K ohms
Common Mode Voltage Plus Signal Voltage	± 10 V
Absolute Maximum	± 15 V

"ON" CHANNEL SPECIFICATIONS

Switch Impedance	500 ohms (typical)
Input Impedance	10^9 ohms, 80 pF
Common Mode Rejection	80 dB, 0 to 60 Hz

"OFF" CHANNEL SPECIFICATIONS

Impedance	10^{10} ohms, 4 pF

Note: All switches open when power is turned off.

OUTPUT SPECIFICATIONS

Output Voltage Range	± 10 V
Output Current	100 mA
Output Impedance	20 ohms
Voltage Drift	± 50 μV/°C

DYNAMIC RESPONSE

Frequency Response	Tracking error with F.S. peak-to-peak sine wave applied to a single ON channel. 1K source impedance.
Accuracy of 0.01%	250 Hz
Accuracy of 0.1%	2500 Hz

CROSS TALK

ON Channel 1K to ground	< 1 mV. F.S. peak-to-peak 1 kHz sine wave applied to 15 OFF channels.

SETTLING TIME

To 0.01% of 10 volts	10 microseconds (switching between two channels with dc voltage of +10 V and -10 V on each channel respectively).

DIGITAL OUTPUTS

End of Scan	Low true signal which begins when ADC starts to convert the data for the "Last Channel" of the Multiplexer Sequential Mode, and ends when the ADC starts to convert the next time. Held high when the Multiplexer is in the Random Mode. Fanout 10 logic loads. Maximum capacitive load, 1000 pF.
Control Flip-Flop	R-S flip-flop which is set high true by EXC 03YY, and is reset by EXC 0YY, EXC 01YY, EXC 02YY, or System Clear. Also may be wire-ORed and reset by pulling down the output. 1K pull-up to +5 V. Available fanout, 30 logic loads. Maximum capacitive load 100 pF.

TEMPERATURE RANGE

Specification	0°C to 50°C
Operating	-25°C to 70°C
Storage	-55°C to 100°C

POWER

+5 Vdc ± 5%; 725 mA

± 15 Vdc ± 3%; 15 mA

+22 Vdc ± 5%; 10 mA

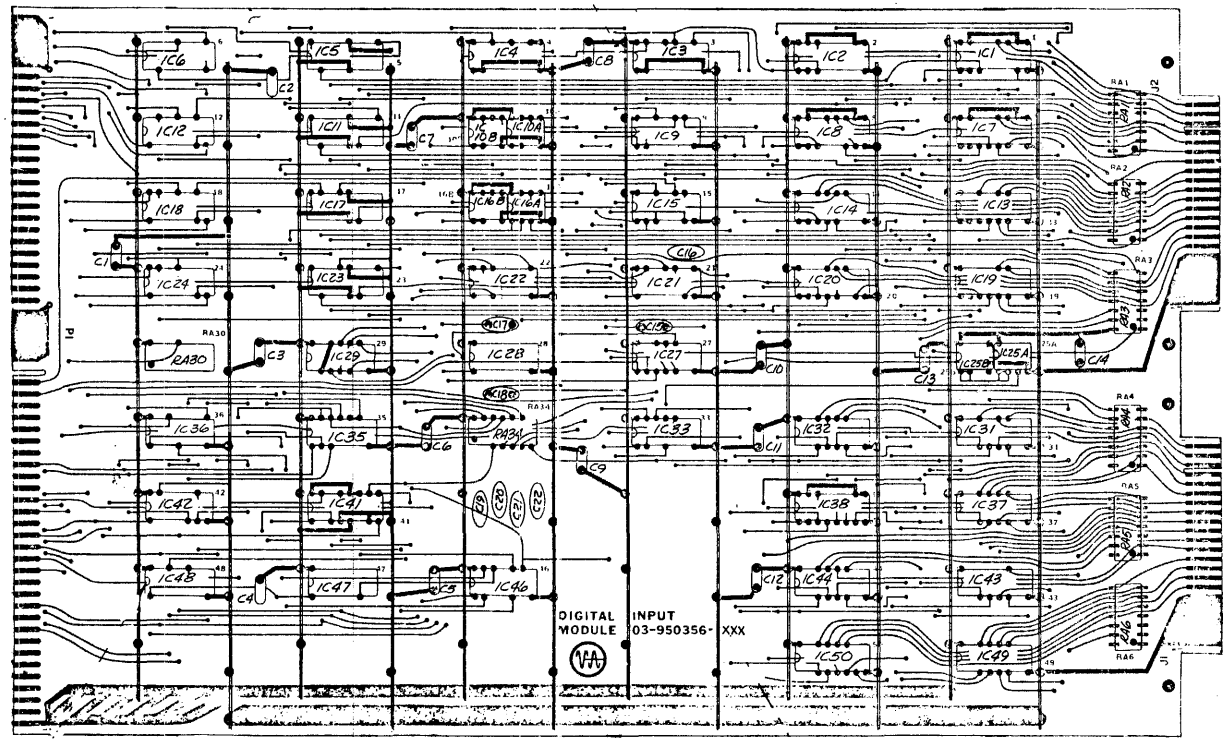
-22 Vdc ± 5%; 5 mA

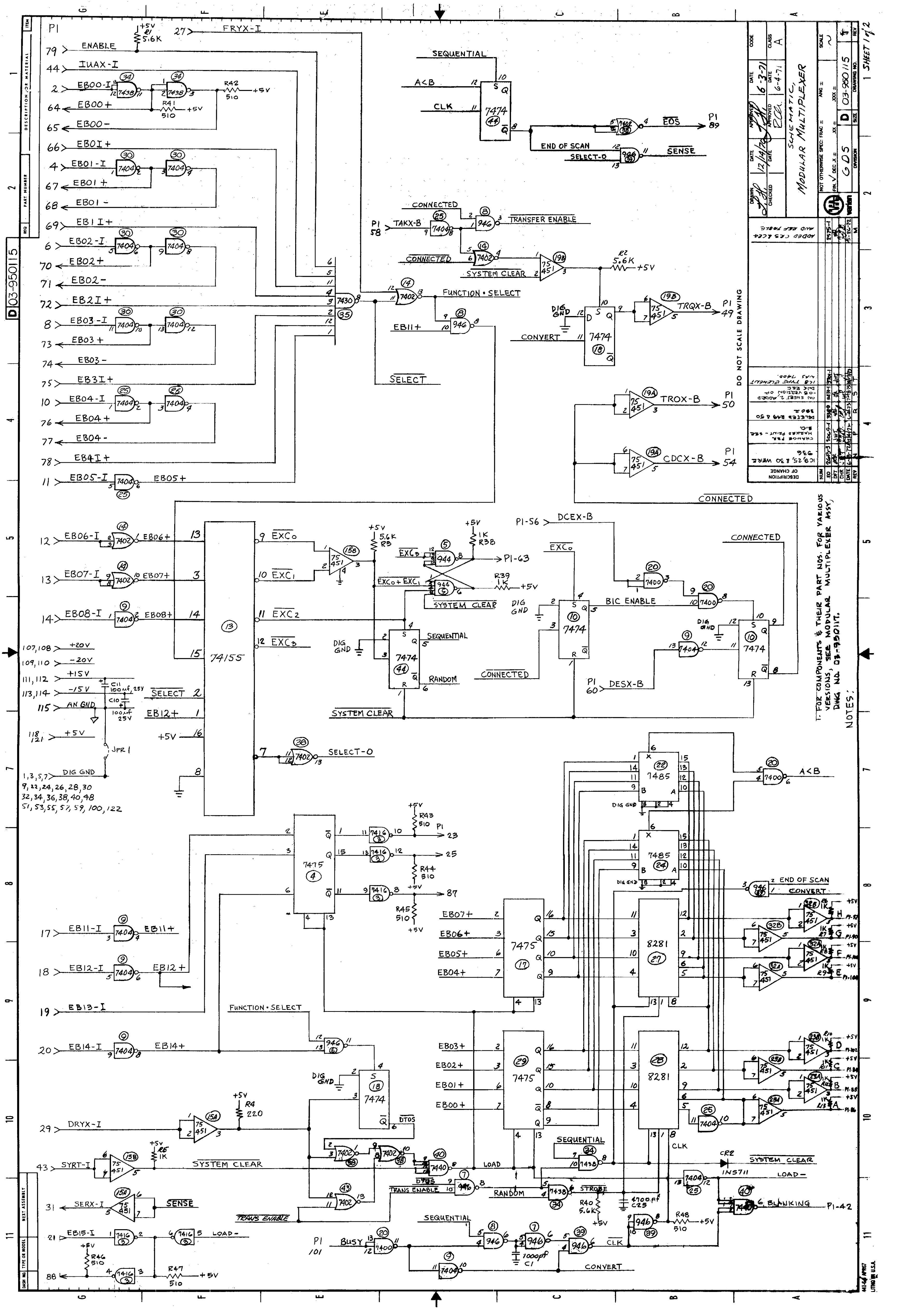
PHYSICAL CHARACTERISTICS

Dimensions	One printed circuit board 7-3/4 x 12 x 1/2 inches
Connectors	Two 44-terminal card edge connectors One 122-terminal card edge connector

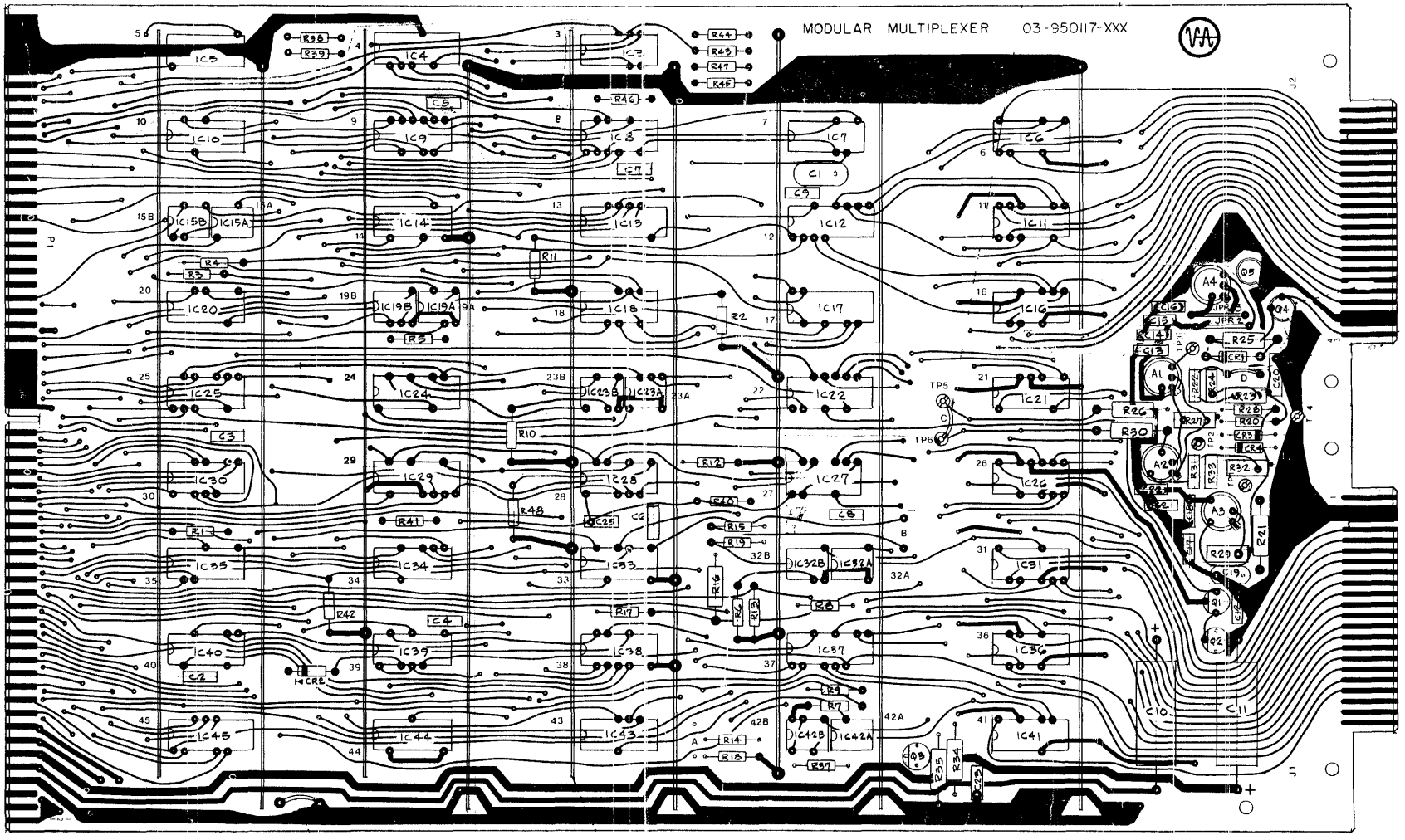
APPENDIX C: SCHEMATICS, ASSEMBLIES, PARTS LIST

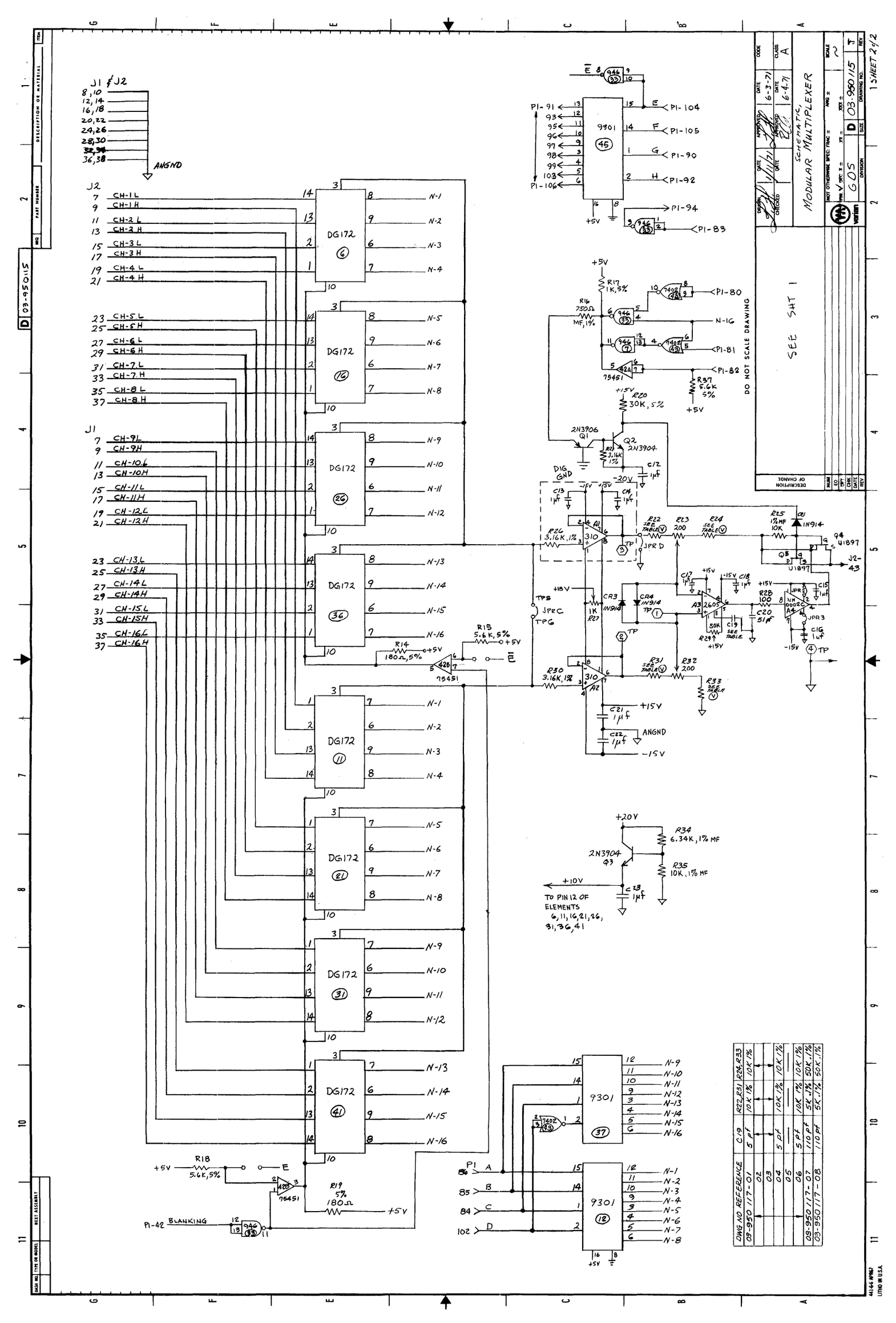
Modular Multiplexer	03-950115 (2 Sheets)


DIGITAL INPUT
MODULE 03-950356-XXX



SCHEMATIC, MODULAR MULTIPLEXER
D 03-950115
GDS
SHEET 1 of 2
DO NOT SCALE DRAWING
NOTES:
1. FOR COMPONENTS & THEIR PART NOS. FOR VARIOUS VERSIONS, SEE MODULAR MULTIPLEXER ASSY, DWG NO. 03-950117.


MODULAR MULTIPLEXER 03-950117-XXX



DWG NO REFERENCE	C19	R22, R31	R24, R33
03-950117-01	5 pf	10K 1%	10K 1%
02			
03	5 pf	10K 1%	10K 1%
04			
05			
06	5 pf	10K 1%	10K 1%
03-950117-07	110 pf	5K 1%	50K 1%
03-950117-08	110 pf	5K 1%	50K 1%

Modular Multiplexer, 950117

Schematic Reference	Description	Varian Part No.
Q1	Transistor, 2N3906	62-903 906
Q2, Q3	Transistor, 2N3904	62-903 904
Q4, Q5	Transistor, U1897E	62-798 125
A1	Amplifier, 310H	62-600 212
A2, A3	Amplifier, 2605	62-600 203
A4	Amplifier, NH0002C	62-600 185
C1	Cap, MICA 1000 Pf	41-159 599
C2-9, 12-18, 21-23	Cap, Cer, 1 uf, 50 V	41-228 009
C10, 11	Cap, Elect, 100 μf, 25 V	41-506 258
C19	Cap, MICA 5 pf	41-159 505
C20	Cap, Cer, 51 pf, 500 V	41-205 860
C25	Cap, Cer, 4700 pf, 200 V	41-229 947
IC6, 11, 16, 21, 26, 31, 36, 41	IC Element DG 172	62-600 261
IC9, 25, 30	IC Element 7404N	62-600 013
IC7, 9, 25, 30, 33, 39	IC Element 946	62-600 303
IC35	IC Element 7430 N	62-600 359
IC40	IC Element 7440N	62-600 310
IC5	IC Element 944	62-600 306
IC10, 18, 44	IC Element 7474N	62-600 365
IC4, 17, 29	IC Element 7475	62-600 351
IC22, 24	IC Element 7485	62-600 338
IC27, 28	IC Element 8281	62-600 364
IC12, 37, 45	IC Element 9301	62-600 400
IC13	IC Element 74155	62-600 271
IC14, 38, 43	IC Element 7402N	62-600 356
IC15A&B, IC19A&B, IC23A&B, IC32A&B, IC42A&B	IC Element 75451	62-600 260
IC3	IC Element 7416	62-600 019
JPR1, C, D	Wire, Bus, Bare, #24 Awg	81-099 924
IC34	IC Element 7438	62-600 294
IC8, 20	IC Element 7400	62-600 355
R28	Res, FXD, Comp, 100Ω, $\frac{1}{4}$W, 5%	32-301 310
R14, 19	Res, FXD, Comp, 180Ω, $\frac{1}{4}$W, 5%	32-301 318
R4	Res, FXD, Comp, 220_, $\frac{1}{4}$W, 5%	32-301 322
R5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 38, 39	Res, FXD, Comp, 1 K, $\frac{1}{4}$W, 5%	32-301 410
R1, 2, 3, 15, 18, 37, 40	Res, FXD, Comp, 5.6 K, $\frac{1}{4}$W, 5%	32-301 456
R20	Res, FXD, Comp, 30 K, $\frac{1}{4}$W, 5%	32-301 530
R41-48	Res, FXD Comp, 510Ω, $\frac{1}{4}$W, 5%	32-301 351
R49, R50	Res, FXD Comp, 390Ω, $\frac{1}{4}$W, 5%	32-301 339

Modular Multiplexer, 950117 (Cont'd)

Schematic Reference	Description	Varian Part No.
R21, 26, 30	Res, MF, 3.16 K, $\frac{1}{4}$W, 1%	31-224 316
R26	Res, MF, 6.34 K, $\frac{1}{4}$W, 1%	31-224 634
R34	Res, MF, 10 K, $\frac{1}{4}$W, 1%	31-225 100
R25, 35	Res, Var, W.W. 200Ω	37-577 310
R23, 32	Res, Var, W.W. 1 K	37-577 311
R27	Res, Var, W.W. 50 K	37-577 315
R29	Res, MF 10 K, 1%	31-239 033
R22, 24, 31, 33	Res, MF 750Ω, 1%	31-223 750
R16	Diode, 1N914	66-304 148
CR1, 3, 4	Diode 1N5711	66-981 101
CR2	Terminal	16-229 862
TP1-TP6	Cap, MICA - 110 pf	41-159 564
C19	Res, MF - 50 K, .1%	31-239 064
R24, 33	Res, MF - 5 K, .1%	31-239 011
R22, 31		