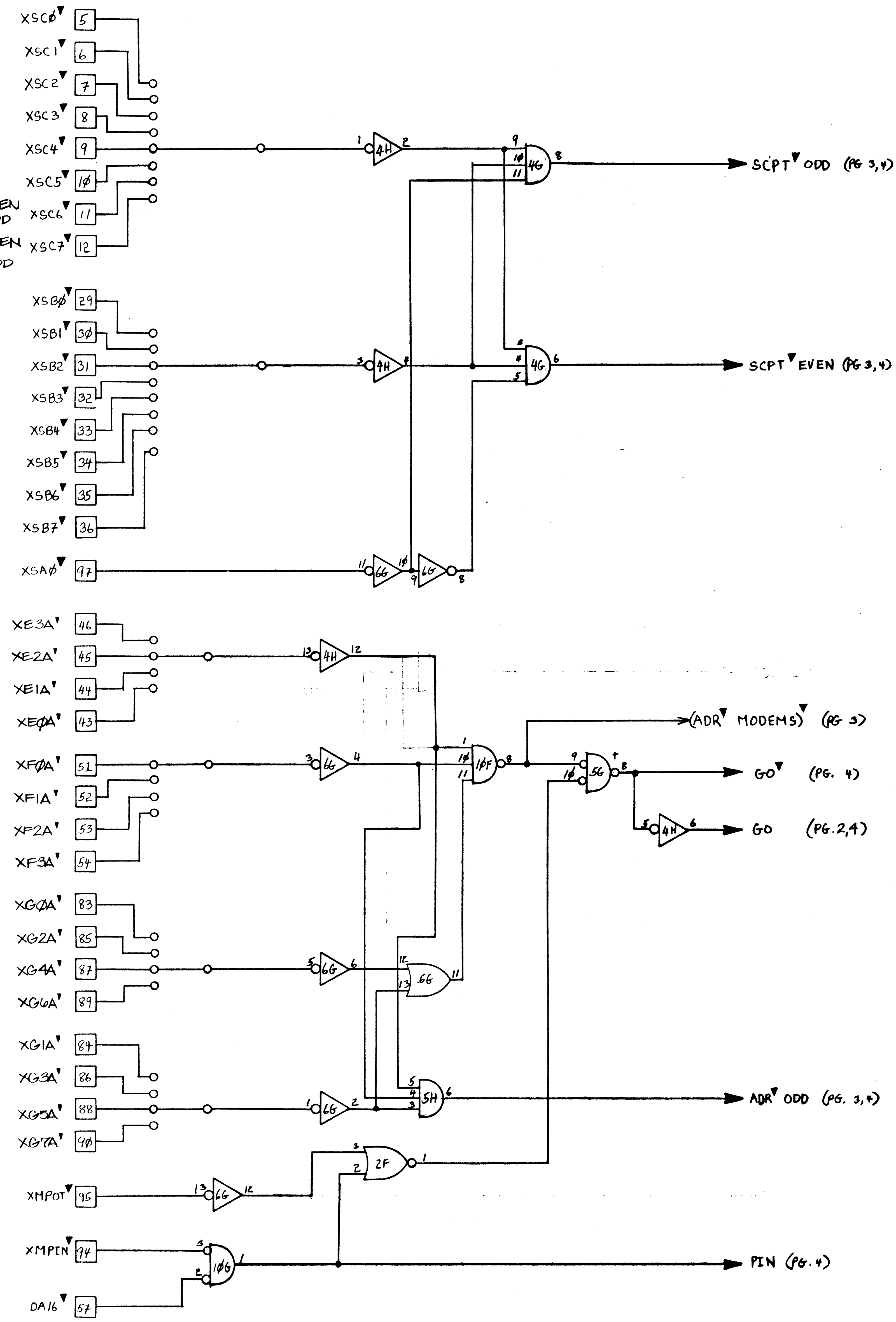
JUMPERS SET FOR:

SCAN ADR = 104 EVEN
105 ODD

DEVICE ADR = 104 EVEN
105 ODD

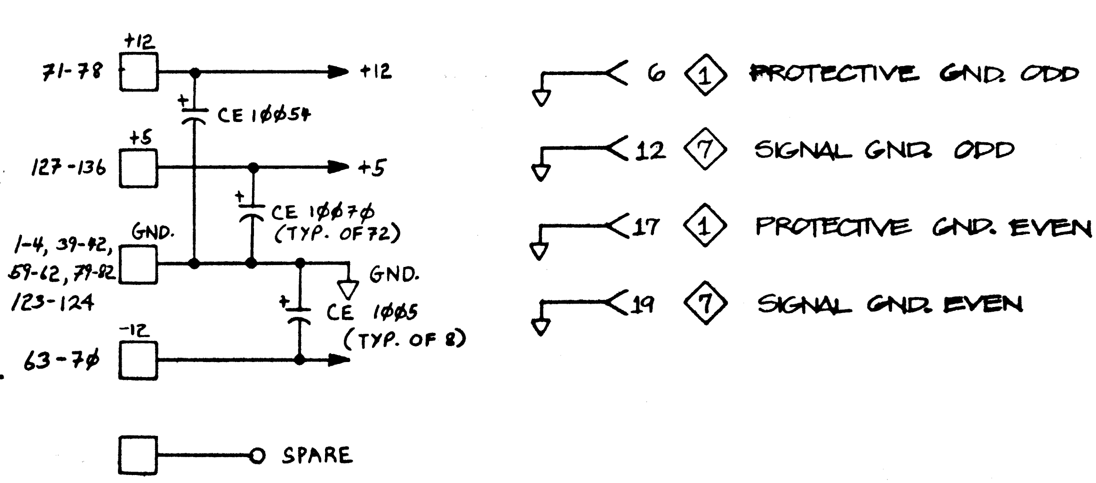


NOTES:

1. ARE CONNECTOR PINS IN BACK OF CARD

2. ARE CONNECTOR PINS IN CINCH DB-255 CONNECTOR ON CHIO MPLXR PATCH PANEL

3. j — i - DEVICE CONNECTOR PIN NO. j - INTERFACE CONNECTOR PIN NO.



NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED LATEST REVISION	8/2/74	—	

REVISIONS

NO. L∅1∅82.∅

The Aloha System BCC-500

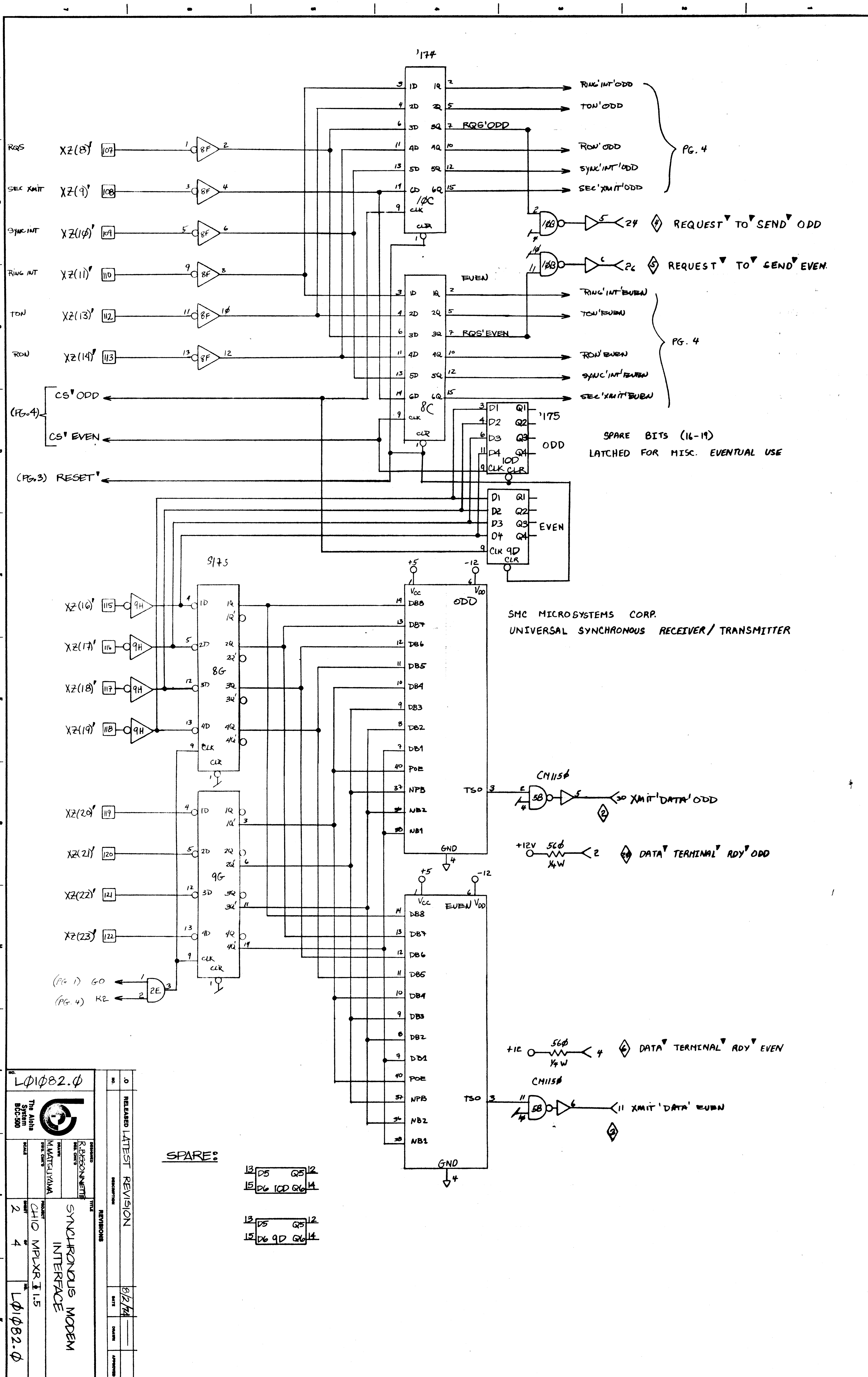
DESIGNED R. BISONETTE
DES. CHK'D R. INEFUKU
DRAWN M. MATSUYAMA

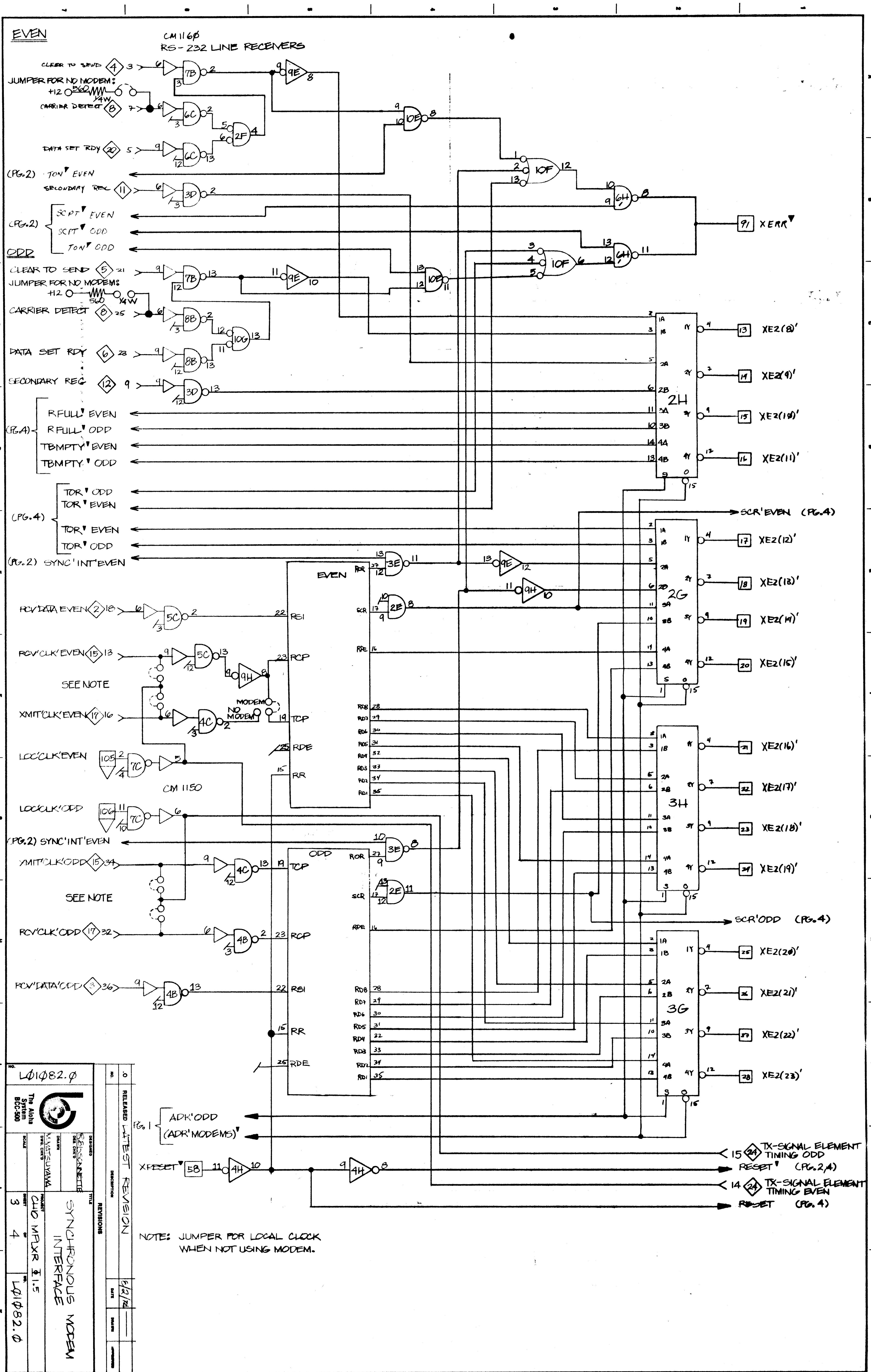
TITLE SYNCHRONOUS MODEM INTERFACE

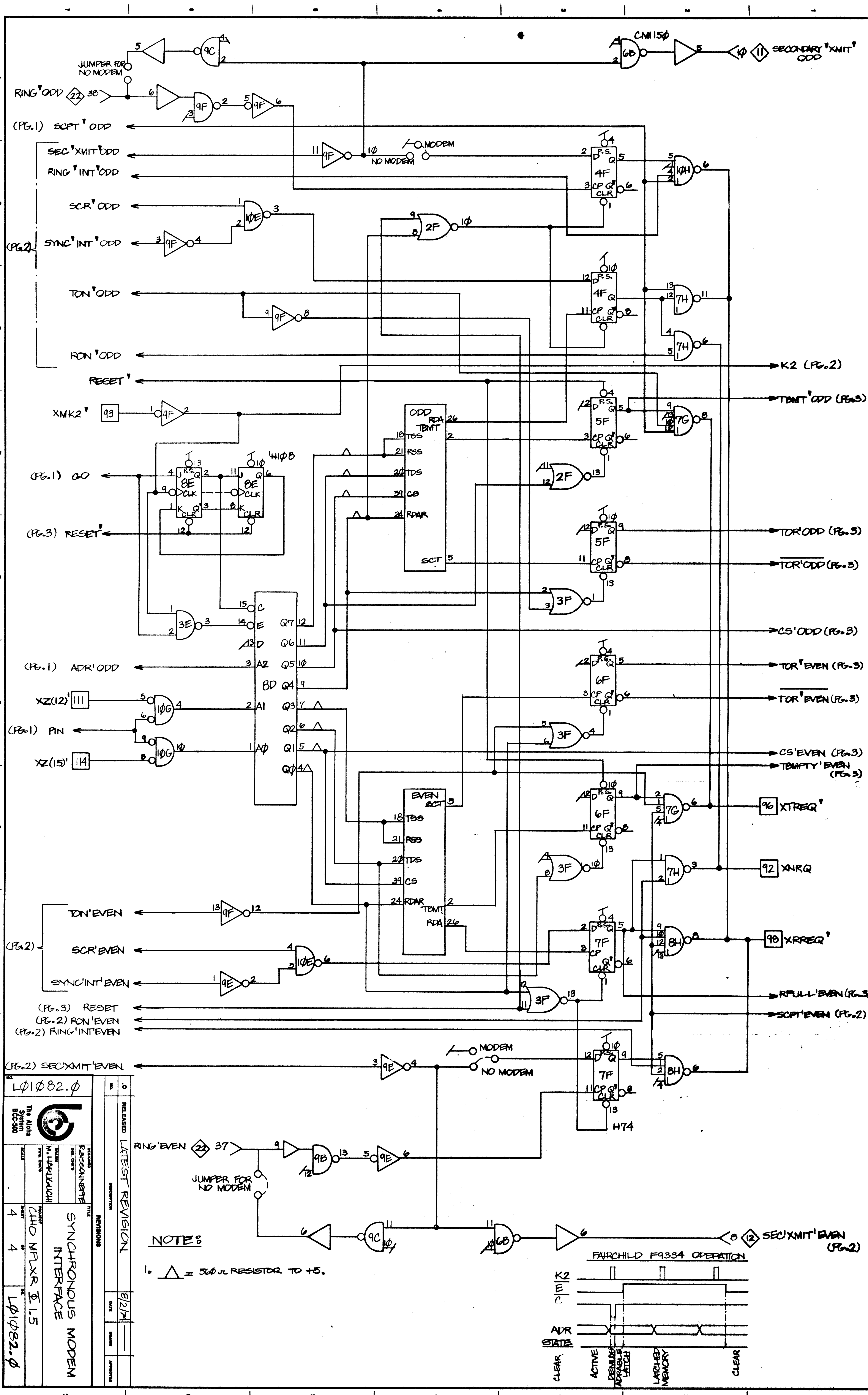
PROJECT CHIO MPLXR ∅1.5

SHEET 1 OF 4

NO. L∅1∅82.∅


'174
RING'INT'ODD
TON'ODD
RQS'ODD
RON'ODD
SYNC'INT'ODD
SEC'XMIT'ODD
PG. 4
RQS XZ(8)' 107
SEC XMIT XZ(9)' 108
SYNC INT XZ(10)' 109
RING INT XZ(11)' 110
TON XZ(13)' 112
RON XZ(14)' 113
8F
10C
8C
EVEN
REQUEST TO SEND ODD
REQUEST TO SEND EVEN
10B
RING'INT'EVEN
TON'EVEN
RQS'EVEN
RON'EVEN
SYNC'INT'EVEN
SEC'XMIT'EVEN
CS' ODD
CS' EVEN
(PG.4)
(PG.3) RESET'
'175
ODD
10D
9D
SPARE BITS (16-19)
LATCHED FOR MISC. EVENTUAL USE
S175
XZ(16)' 115
XZ(17)' 116
XZ(18)' 117
XZ(19)' 118
9H
8G
XZ(20)' 119
XZ(21)' 120
XZ(22)' 121
XZ(23)' 122
9G
(PG 1) GO
(PG 4) K2
2E
SMC MICROSYSTEMS CORP.
UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER
Vcc
VDD
DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1
POE NPB NB2 NB1
TSO
GND
+5
-12
CM1150
5B
XMIT'DATA'ODD
+12V 560 1/4W
DATA TERMINAL RDY ODD
DATA TERMINAL RDY EVEN
XMIT'DATA'EVEN
SPARE:
D5 Q5 D6 10D Q6
D5 Q5 D6 9D Q6
L01082.0
The Aloha System BCC-500
DESIGNED R.BISSONNETTE
DRAWN M.MATSUYAMA
TITLE SYNCHRONOUS MODEM INTERFACE
PROJECT CHIO MPLXR I 1.5
SHEET 2 OF 4
NO. L01082.0
REVISIONS
.0 RELEASED LATEST REVISION 8/2/74


EVEN
CM 116Ø
RS-232 LINE RECEIVERS
CLEAR TO SEND 4
JUMPER FOR NO MODEM:
+12 560 1/4W
CARRIER DETECT 8
DATA SET RDY 20
(PG.2) TON' EVEN
SECONDARY REC 11
(PG.2) SCPT' EVEN
SCPT' ODD
TON' ODD
ODD
CLEAR TO SEND 5
JUMPER FOR NO MODEM:
+12 560 1/4W
CARRIER DETECT 8
DATA SET RDY 6
SECONDARY REC 12
(PG.4) RFULL' EVEN
RFULL' ODD
TBMPTY' EVEN
TBMPTY' ODD
(PG.4) TOR' ODD
TOR' EVEN
TOR' EVEN
TOR' ODD
(PG.2) SYNC'INT'EVEN
91 XERR'
13 XE2(8)'
14 XE2(9)'
15 XE2(10)'
16 XE2(11)'
SCR'EVEN (PG.4)
17 XE2(12)'
18 XE2(13)'
19 XE2(14)'
20 XE2(15)'
2H
2G
3H
3G
EVEN
RSI RCP TCP RDE RR ROR SCR RPE RD8 RD7 RD6 RD5 RD4 RD3 RD2 RD1
RCV'DATA EVEN 2
RCV'CLK'EVEN 15
SEE NOTE
MODEM
NO MODEM
XMIT'CLK'EVEN 17
LOC'CLK'EVEN 105
CM 1150
LOC'CLK'ODD 106
(PG.2) SYNC'INT'EVEN
ODD
XMIT'CLK'ODD 15
SEE NOTE
RCV'CLK'ODD 17
RCV'DATA'ODD 3
21 XE2(16)'
22 XE2(17)'
23 XE2(18)'
24 XE2(19)'
SCR'ODD (PG.4)
25 XE2(20)'
26 XE2(21)'
27 XE2(22)'
28 XE2(23)'
PG. 1 ADR'ODD
(ADR'MODEMS)'
XRESET' 58
4H
15 24 TX-SIGNAL ELEMENT TIMING ODD
RESET' (PG.2,4)
14 24 TX-SIGNAL ELEMENT TIMING EVEN
RESET (PG.4)
NOTE: JUMPER FOR LOCAL CLOCK WHEN NOT USING MODEM.
NO. LØ1Ø82.Ø
The Aloha System BCC-500
DESIGNED R.BISSONNETTE
DRAWN M.YATSUYAMA
TITLE SYNCHRONOUS MODEM INTERFACE
PROJECT CHIO MPLXR Φ1.5
SHEET 3 OF 4
NO. LØ1Ø82.Ø
REVISIONS
.0 RELEASED LATEST REVISION 6/2/72


CM115Ø
SECONDARY 'XMIT' ODD
JUMPER FOR NO MODEM
RING'ODD 22 38
(PG.1) SCPT'ODD
SEC'XMIT'ODD
RING'INT'ODD
SCR'ODD
(PG.2) SYNC'INT'ODD
TON'ODD
RON'ODD
MODEM
NO MODEM
K2 (PG.2)
RESET'
XMK2' 93
TBMT'ODD (PG.3)
'H1Ø8
(PG.1) GO
(PG.3) RESET'
ODD RDA TBMT TSS RSS TDS CS RDAR SCT
TOR'ODD (PG.3)
TOR'ODD (PG.3)
CS'ODD (PG.3)
TOR'EVEN (PG.3)
TOR'EVEN (PG.3)
(PG.1) ADR'ODD
8D
XZ(12)' 111
(PG.1) PIN
XZ(15)' 114
CS'EVEN (PG.3)
TBMPTY'EVEN (PG.3)
EVEN SCT TSS RSS TDS CS RDAR TBMT RDA
96 XTREQ'
92 XNRQ
98 XRREQ'
TON'EVEN
(PG.2) SCR'EVEN
SYNC'INT'EVEN
RFULL'EVEN (PG.3)
SCPT'EVEN (PG.2)
(PG.3) RESET
(PG.2) RON'EVEN
(PG.2) RING'INT'EVEN
(PG.2) SEC'XMIT'EVEN
MODEM
NO MODEM
H74
RING'EVEN 22 37
JUMPER FOR NO MODEM
SEC'XMIT'EVEN (PG.2)
NOTE:
1. △ = 56Ø Ω RESISTOR TO +5.
FAIRCHILD F9334 OPERATION
K2
E
C
ADR
STATE
CLEAR
ACTIVE
DEMUX-ADRABLE LATCH
LATCHED MEMORY
CLEAR
NO. LØ1Ø82.Ø
The Aloha System BCC-500
DESIGNED R.BESONNETTE
DRAWN M. HARUGUCHI
TITLE SYNCHRONOUS MODEM INTERFACE
PROJECT CHO MPLXR Φ 1.5
SHEET 4 OF 4
NO. LØ1Ø82.Ø
REVISIONS
NO. .O DESCRIPTION RELEASED LATEST REVISION DATE 8/2/74