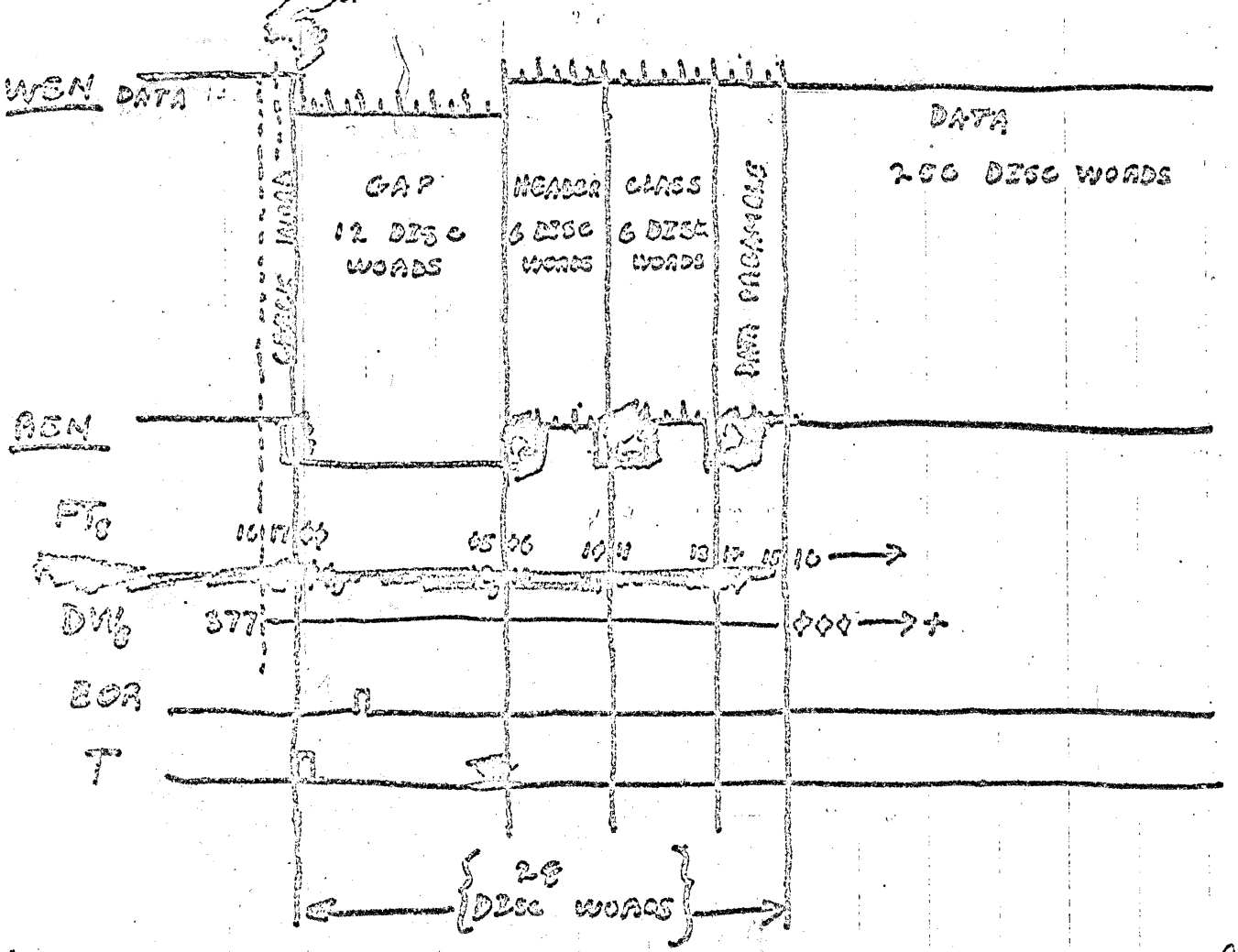
6700 DISC RECORD FORMAT

9/22/68
RLF



ONE FT = 2 DISK WORDS

ONE DISK WORD = 2 24 BIT WORDS + 2 PA

EOR - END OF RECORD

FT_0 - FORMAT TIME - OCTAL DECODE OF FORMAT COUNTER

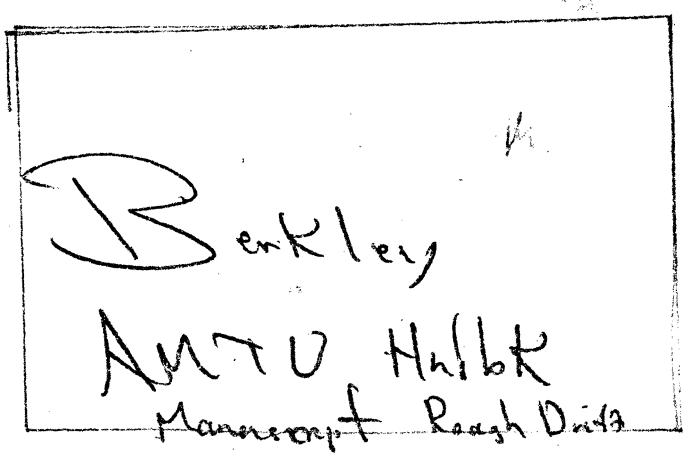
DW_0 - DATA WORD TIME - OCTAL DECODE OF DATA WORD COUNTER

DATA WORD COUNTER COUNTS DISK WORDS

Figure 2-3 Disk Format Timing

FUNCTIONAL DESCRIPTION

AUXILIARY MEMORY TRANSFER UNIT (AMTU)



This Page to Illustrate Overall View Of AMTU

Figure 1-1 Auxiliary Memory Transfer Unit

SECTION I

PHYSICAL DESCRIPTION

1-1 GENERAL

The Auxiliary Memory (AMTU) is housed in a single cabinet designated Bay 3 (See Figure 1-1). The functional printed circuit boards which contain the logic for the AMTU are located within two racks of Bay 3. Each rack has 33 board locations. The two racks are mounted one above the other in Bay 3. The top rack is designated 3A1 and the bottom rack is designated 3A2. All input and output signals to each board enter from the rear through a special 136-pin Elco fingertype connector. Interconnecting wiring between the functional boards of both racks is effected by means of terminals mounted on a solid plane behind the card racks and which connect electrically to the fingers of the Elco Type connectors. Located directly below rack 3A2 is a cable connector panel assigned reference designation 3A3. On this panel are mounted seven Burndy-Type connectors, four of which interface with the Drums and Disks, one of which interfaces with a control Processor (AMCP) and one of which interfaces with the Fast Memory. A single RG58 coaxial connector is also mounted on the connector panel and carries the System Clock into the AMTU. From these connectors the signals interface with the AMCP through six cable cards located in the center portion of the rack designated 3A2. See figure 1-2 for more detail.

1-2 RACK ORGANIZATION

1-2-1 RACK 3A1 This rack ~~Rack 3A1~~ is divided into three distinct functional blocks. Jack locations 33 through 20 are dedicated to the functional boards which implement the logic functions associated with the Drum Transfer Subunit designated TSUØ. Jack location 19 through 14 are dedicated to the functional boards which implement the logic functions associated with the Transfer Unit Interface Multiplexor (TUIM). Jack locations 13 through 1 are dedicated to the functional boards which implement the logic functions associated with the Disk Transfer Unit designated TSU2.

1-2-2 RACK 3A2 This rack is also divided into three distinct functional blocks. Jack locations 33 through 20 are dedicated to the functional boards which implement the logic functions associated with XXXX TSU1. Jack locations 19 through 14 are dedicated to the cable boards which connect the functional boards to the Burndy connectors on the connector panel 3A3.

XXXXXXXN

1-3 FUNCTIONAL BOARD TYPES

There are fifteen different functional board types serving 64 of the 66 available Jack locations on racks 3A1 and 3A2. Boards of the same type are interchangeable except for the external jumpering required as specified XXXX in the following analysis.

1-3-1 DRUM TSU The two Drum TSU's require the following seven basic XXXXXXXXXX board types:

CONTROL REGISTER TYPE # 700606

Each Drum TSU requires five of these boards, one each in Jack locations J33 through J29. The five boards are completely interchangeable. This interchangeability extends to the Jack locations in all four TSU's wherein this board is used.

CONTROL LOGIC TYPE # 700687

Each Drum TSU requires one of these boards in Jack location J28. This board can be used in Jack location J7 of either Disk TSU with some external jumpering required. External jumpering is also required to adapt this functional board to the two different Drum types used in this System.

POSITION COUNTERS TYPE # 700624

Each Drum TSU requires one of these boards in Jack location J27. This board can be used in Jack location J8 of either Disk TSU with some external jumpering required.

DATA BUFFERS TYPE # 700687

Each Drum TSU requires three of these boards, one each in Jack location J26 through J24. A different external jumper configuration is required for each of the three Jack locations.

FORMAT GENERATOR CARD NO. 2 TYPE # 700725-2

Each Drum TSU requires one of these boards in Jack location J23.

FORMAT GENERATOR CARD NO. 1 TYPE # 700725-1

Each Drum TSU requires one of these boards in Jack location J21.

1-3-2 DISK TSU Each of the two Disk TSU's require the following eight basic functional board types:

CONTROL REGISTER TYPE # 700606

Each Disk TSU requires five of these boards, one each in Jack locations J6 through J2. The five boards are completely interchangeable. This interchangeability extends to the Jack locations in all four TSU's wherein this board is used.

CONTROL LOGIC TYPE # 700687

Each Disk TSU requires one of these boards in Jack location J7. This board can be used in Jack location J28 of either Disk TSU with some external jumpering required.

POSITION COUNTERS TYPE # 700624

Each Disk TSU requires one of these boards in Jack location J8. This board can be used in Jack location J27 of either Drum TSU, with some external jumpering required.

FORMAT CONTROL TYPE # 700636

Each Disk TSU requires one of these boards in Jack location J1.

DATA BUFFERS TYPE # 700703

Each Disk TSU requires two of these boards, one each in Jack locations J7 and J8. A different external jumper configuration is required for each of the Jack locations.

TRACK POSITION TYPE # 700621

Each Disk TSU requires one of these boards in Jack location J11.

DISK CONTROL A TYPE # 700708

Each Disk TSU requires one of these boards in Jack location J12.

DISK CONTROL B TYPE # 700711

Each Disk TSU requires one of these boards in Jack location J13.

1-3-3 TUIM The TUIM located in rack 3A1 requires the following Three basic functional board types:

MEMORY INTERFACE TYPE # 700589-1

The TUIM requires three of these boards, one each in Jack locations J14 through J16 of rack 3A1. A different external jumper configuration is required for each of the Jack locations.

~~CLOCK TYPE # 700630-1~~

CLOCK TYPE # 700630-1

The TUIM requires one of these boards in Jack location J17 of rack 3A1.

PRIORITY LOGIC TYPE # 700609-1

The TUIM requires two of these boards, one each in Jack locations J18 and J19 of rack 3A1.

1-3-4 CABLE BOARDS The following two basic cable board types are required:

DRUM AND DISK INTERFACE CABLES TYPE # 700694

Four of these cable boards are required, one each in Jack locations J19 through J16 of rack 3A2. The four boards are completely interchangeable among Jack locations J19 through J16 of rack 3A2.

NOTE

Jack locations J22 on card racks 3A1 and 3A2 are not available for future expansion. The associated space within each rack is required to accomodate the oscillator package mounted on the functional board in Jack location J23.

SECTION II

FUNCTIONAL DESCRIPTION

2-1 INTRODUCTION

The Auxiliary Memory Transfer Unit (AMTU) is controlled by the Auxiliary Memory Control Processor (AMCP), which in turn is supervised by routines stored in Central Memory (See Figure 2-1). The AMCP issues I/O commands to the AMTU which interpets these commands to select a device, determine transfer length and direction, and a Central Memory address between which transfers are to take place and to determine transfer length and direction. Within this section the interface between the AMCP and the AMTU will be discussed on a functional basis and then the interface between the AMTU and Central Memory (Fast Memory and Core Memory) will be discussed.

2-2 DISCUSSIONAL TECHNIQUE

When appropriate this handbook will cover functions according to a real time sequence of events happening within the System. As each logic implementing device is introduced in the discussion for the first time, ample reference into the logic documentation will be made within the text. However when the device is referenced again reference into the logic will not always be provided. In like manner when a function is introduced for the first time it will be discussed in detail but if the function is referenced later it will be in general terms only or in some cases the paragraph in which the function is discussed in detail is referenced for the convenience of the reader.

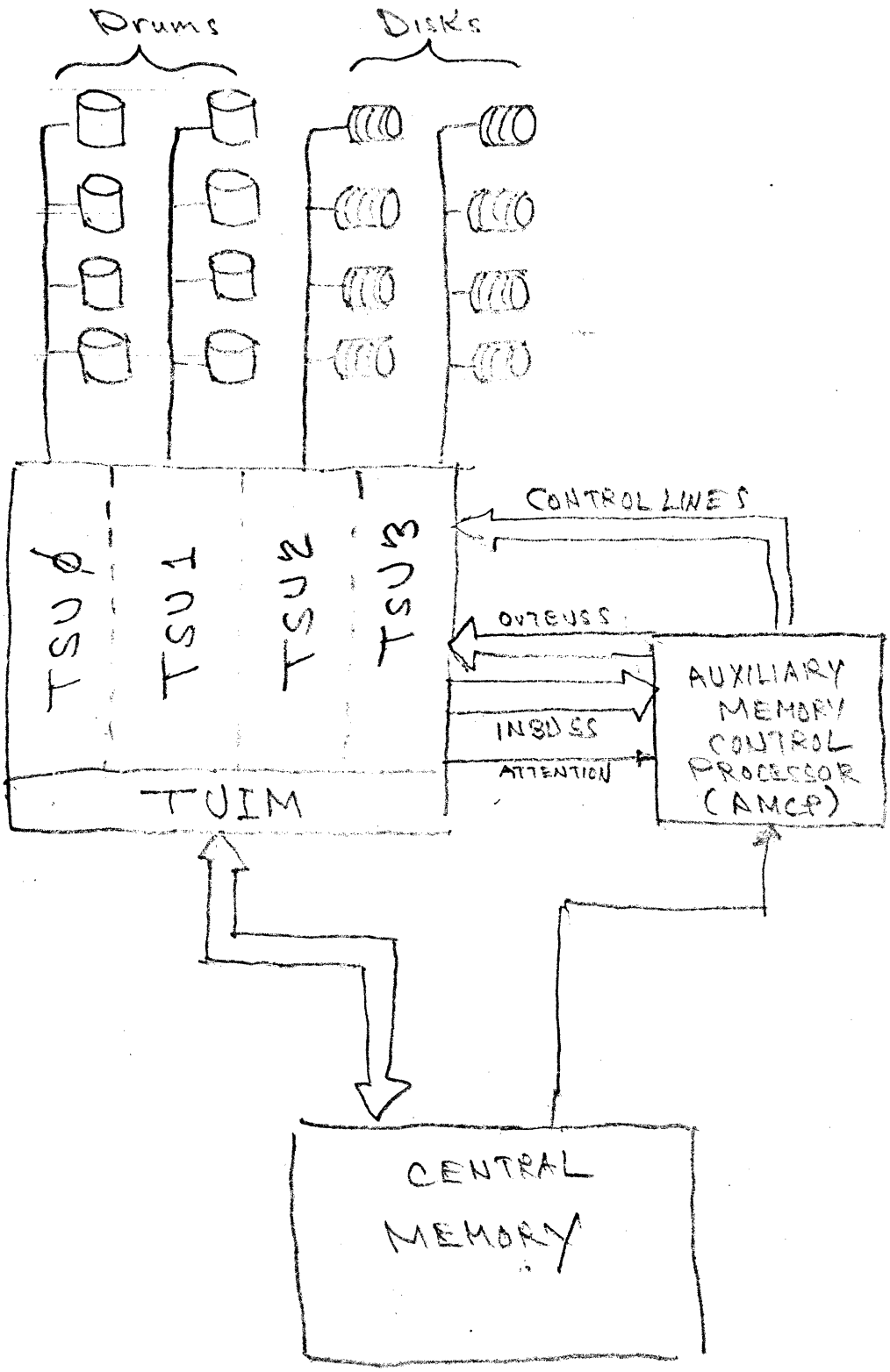

Drums
Disks
TSU 0
TSU 1
TSU 2
TSU 3
CONTROL LINES
OUTBUSS
INBUSS
ATTENTION
AUXILIARY MEMORY CONTROL PROCESSOR (AMCP)
TUIM
CENTRAL MEMORY

Figure 2-1

2-2 I/O CONTROL (BASIC CONCEPT)

The following paragraphs discuss on a concept level the major actions taken between the AMCP and the AMTU, actions which can best be referred to as I/O Control.

2-2-1 ATTENTION Communication between the AMCP and the AMTU is initiated by the AMTU. When power is first applied to the AMTU, it assumes a Reset condition which enables the generation of an Attention pulse (ATTN) by Unit Ø XX within each of the four XX TSU's. The four ATTN lines are OR-gated and enter the AMCP on a single line. The AMCP has an option , once communication begins, to disable any one or all of the four ATTN pulses. The ATTN pulse is generated repeatedly in synchronization with its rate of angular rotation. The pulse is actually a marker referenced to a space of one record length, a record being the space required to store 512 data words XXX each consisting of 24 data bits. After communication begins, the XX ATTN pulse continues to be generated but not necessarily for every sector which will generate and the unit, the ATTN within each TSU becomes a function of AMCP control.

2-2-2 PRESELECTION STATUS MONITORING The AMCP responds to the ATTN pulses by generating a command to one unit in one of the four TSU's, which causes the commanded unit to report its angular position four times per sector and in the case of a Disk , to report its present track position.

The unit is also requested to indicate whether or not it is engaged or is about to engage in a transfer from Central Memory . In the initial stage of communication the response will be negative. However, as communication proceeds the AMCP generates command instructions which will eventually bring a positive response.

2-2-3 OPERATIONAL INSTRUCTIONS The AMCP uses the preselection status information to select a Device for an operational instruction by loading various Control Registers within one of the four TSU's of the AMTU. The operations that can be performed by the AMCP are discussed in the following subparagraphs:

2-2-3-1 Position Only This operation applies to a Disk device only. The operation involves the mechanical positioning of the read/write elements (heads) on the Disk. The instruction is executed within one sector of angular rotation by the Disk, However, the actual mechanical positioning involves on the order of 50 milliseconds for execution. A Position Only operation is indicated only after all space on all available surfaces for the operating track are exhausted or would be exhausted by a transfer under consideration.

2-2-3-2 Read Data And Class Code This operation applies to both Drum and Disk. It is used to transfer data from the Device to Central Memory as indicated by the Read Data portion of the operation. The Read Class Code portion of the instruction indicates that the class code (an information field used by the

AMCP to classify the data field which it precedes) is to be read and stored in a register until the end of the record at which time the AMCP may interrogate the register.

2-2-3-3 Write Data And Class Code This operation applies to both Drum and Disk Devices. It is used to transfer data from Central Memory to the Device, as indicated by the Write Data portion of the operation. The Write Class Code portion of the operation, indicates that the class code which has been loaded into a register as part of the operation, by the AMCP is to be shifted out of the register onto the Device surface into a space within the record preceding the space where the data is to be written.

2-2-3-4 Compare Class Code And Write Data If Equal This operation applies to Disk Devices only. The Compare Class Code portion of the operation signifies that the Class Code which was loaded into a register by the AMCP, as part of the operation, is to be compared with a Class Code written into the space preceding the data field space within the record to be written. When the comparison is equal the Write Data portion of the operation causes data to be transferred from Central Memory to the selected Disk Device.

2-2-3-5 Write Headers This operation applies to the Disk Device only. The Write Header operation causes a header field to be written in to a space on the surface of a Disk , just preceding the Class field and Data field of a record. The

content of the header field is the complete Disk Address of the record in which the header is located.

2-2-3-6 Operational Instruction Modifiers The basic operations just described can be modified by additional instructions from the AMCP as described in the following subparagraphs:

(a) Drum or Disk Policy This modifying instruction applies to both Drums and Disks. Drum Policy indicates that the AMCP is using the angular position report obtained from preselection monitoring, to generate a starting address, which begins with the record space, which should pass under the heads of the selected Device immediately after the operational instructions from the AMCP are received by the AMTU. A Disk Policy signifies that the starting address is not necessarily the sector arriving under the selected heads after the AMTU receives the operational instructions from the AMCP. Disk Policy must always be specifed on a Position Only operation, since Drum Policy imposes conditions that can not be met by the execution of a Drum Policy operation.

(b) Continue This operational modifier applies to both Disks and Drums. Continue is generated by the AMCP when a transfer will extend beyond word 512 of a record. Continue advances the Central Memory Address and the Device Address sequentially into the next record of the transfer and resets a record length

counter to a full record count of 512.

(c) Disable Check Code Cycle This operational modifier applies to the Disk only. Disable Check Code Cycle is used to alter slightly the way in which a longitudinal parity check of data is performed. This modifier is generated by the AMCP following the detenction of a longitudinal parity error which is judged to be caused by a defective read/write element (head). Disable Check Code Cycle helps to identify which of the six heads within the selected band is defective.

2-3 I/O CONTROL (IMPLEMENTATION)

Communication between the AMCP and the AMTU takes place over a 24-bit input buss and a 24-bit output buss. The information on the two busses is controlled and interpreted by means of the following Control Lines from the AMCP.

ACTC	Activate Command	(Select AMTU register)
WTPC	Write Parallel Command	(Load AMTU register)
RDPC	Read Parallel Command	(Sample output buss from AMTU)
PDS	Parallel Data Strobe	(Strobe data on either buss)

The AMTU acknowledges the receipt of signals on any of the first three above Control lines with an ACK signal returned over a separate control line to the AMCP. The AMTU also communicates with the AMCP by means of the attention (ATTN) signal. This signal is generated by one unit in each of the four TSU's. The ATTN signal is referenced to a specific time within a record and is used by the AMCP to determine when to send operational instructions to the AMTU.

2-3-1 ATTENTION When power is first applied to the AMTU, a reset pulse is generated. The reset pulse is generated through the circuit on the Priority Logic board at Jack location 3A1 J19 (Sheet 19 Dwg 700903). With power on the TURESET signal exiting the board through pin 6 stays at ground level until the capacitors charge to a five-volt level causing the TURESET signal to go high.

NOTE

Signals within the AMTU which are common to all four TSU's are given mnemonics prefixed with TU.

2-3-1-1 Enable Attention TURESET is used to reset the AMTU logic and to enable the ATTN signal. The latter function is accomplished by routing TURESET into the Control logic boards for each TSU. The following discussion is referenced to TSUØ. However, implementation is the same for all TSU's. TURESET enters the Control Logic board at location 3A1 J28 (Sheet 28 Dwg 700903) through pin 92. After inversion the continuity of our concern is to logic continuity symbol A16. Following this continuity path it is seen that the RESET* pulse is used to set a latching flip flop producing the enable Attention level (ENATTN). Using the continuity symbol C15 as an aid, ENNATTN can be found gated with three other signals to produce a set pulse for a latching flip flop. The signal identified by continuity symbol A9 signifies the conditions when the ATTN pulse may be generated, beginning with initiation. The actual signals producing the conditions are first, BSY*, indicating the TSU is not engaged in an operation (This is the condition operating when power is first applied to the AMTU), and secondly, EOSWP, which indicates that an operation has just been completed. EOSWP which literally means End-Of-Swap, is a function to be discussed in detail in later paragraphs.

The signal at the gate being discussed, identified by continuity symbol A9, represents , in conjunction with the signal identified by continuity symbol A21, a specific time just following EOSWP, a time well in advance of the actual time the ATTN signal will be produced. The output of the gate latches a flip flop which enables a J-K flip flop. The clock input to the J-K flip flop is generated as a function of angular rotation of the Drum selected within TSUØ. When power is first applied to the AMTU, Drum Unit Ø is automatically selected since the Unit Register controlling Drum selection is automatically reset. This clock pulse entering the Control Logic board through pin 13 is given mnemonic TØSSTRQ or Strobe-Start-Request.

NOTE

Signals pertaining to TSUØ only, are given mnemonics prefixed with TØ.

2-3-1-2 Generate Strobe Start Request The continuing discussion is referenced to the logic on Format Generator board No. 1, at location 3A1 J21 (Sheet 22 Dwg 700903). A prerecorded clock track on Drum Ø, identified by mnemonic BCØ and operating at a frequency equal to one-fourth the data-bit frequency, drives an eight-stage counter. The counter is initially reset by an index pulse generated from another prerecorded clock track on Drum Ø. This pulse occurs once per revolution and is identified as TACHØ. The TACHØ pulse is first synchronized to the BCØ clock before being

used to reset the eight-stage counter. The counter is also reset at the end of each record as determined by a decode of the output of the counter. The mnemonic for this reset ~~is End-Of-Record-Pulse (EORP)~~ ERP. A count decode from this counter marking the end of a gap following each record is used to produce the SSTRQ pulse. In the Disk TSU the pulse is given mnemonic GATTN. In the Disk TSU the Format Generator board called Format Control operates slightly different but a discussion of these differences will be deferred until a later paragraph dedicated to Angular Position Monitoring.

2-3-1-3 Synchronization Of ATTN With The System Clock The continuing discussion refers back to the Control Logic board at location 3A1 J28 (Sheet 28 Dwg 700903). The J-K flip flop operated by the TØSSTRQ pulse enables another J-K flip flop operated by the down-edge of the System Clock identified by the continuity symbol A32. The System Clock enters the AMTU through the Coax Connector at location 3A3 J381 , and is routed to the Clock board at location 3A1 J17 (Sheet 18 Dwg 700903). The System Clock enters the Control Logic board of TSUØ through pin 134 under mnemonic (TØMC*-5) The Attention signal leaves the Control Logic board under mnemonic TØATTN* and enters the Memory Interface No. 3 board of the Transfer Unit Interface Multiplexor (TUIM) at ~~IXX~~ location 3A1 J14 (Sheet 15 Dwg 700903) through pin 123 where it is OR-gated with Attention signals coming from the other three TSU Control Logic boards. The output of the OR-gate

is gated with the System Clock (MC) to release the TUATTN* pulse in synchronization with the 25-nano-second MC pulse. TUATTN* is routed through the cable board at location 3A2 J15 (Sheet 48 Dwg 700903) and through connector 3A3 J380, to the AMCP.

2-3-2 PRESELECTION STATUS MONITORING This function is implemented by loading certain status information regarding a Device selected by the AMCP onto the input buss to the AMCP. The function consists of two steps. First an activate step is generated by the AMCP in which the registers, counters or indicators to be monitored within the AMCP are selected for monitoring. The activate step actually gates the outputs of the registers, counters or indicators onto the buss. The second step generated by the AMCP is implemented for the most part within the AMCP and consists of strobing the buss lines into the AMCP for sampling. This step is referred to as RDPC. The AMCP begins by raising the ACTC signal. This signal enters the AMTU through the cable board at location 3A2 J15 (Sheet 48 Dwg 700903). The signal is distributed to all four Control Logic boards under mnemonic TUACTC. The continuing discussion will be referenced to TSUØ, which comprises the logic in board locations 3A1 J20 through 3A1 J33 as documented in Sheets 21 through 33 of Dwg 700903. Coincident with the raising of TUACTC the AMCP places data on its 24-bit output buss. The output buss enters the AMTU through the cable board at location 3A2 J15

(Sheet 48 XX Dwg 700903). From the cable board the buss lines are routed to the Priority Logic XXXX No. 1 board of the TUIM in location 3A1 J19 (Sheet 20 Dwg 700903). The first two bits of the buss are ignored during the ACTC step. Bits three and four are used to decode one of the XX four TSU's. This decode takes place on the Priority Logic No. 1 board. The remaining 19 bits of the output buss are distributed to the Control Logic boards of the AMTU, XX The distribution path is through the Control Register boards of each TSU. When TSUØ is decoded as the selected TSUXXX the TØTSUØ line is raised on the Control Logic board of TSUØ.

2-3-2-1 Activate Control Logic TUACTC enters the Control Logic board of TSUØ at location 3A1 J28 (Sheet 28 Dwg 700903) through pin 40. TØTSUØ enters the same board through pin 19. Bits 5 through 23 of the output buss enter the same board through pins 20 through 38. TUACTC and TØTSUØ control a latching circuit which is one stage inXX a latching Register-Select Register. The output of this latching circuit is used to enable the output of the Register. The input to the XXXXXX nineteen other stages of the Register is produced by the gating of the nineteen least significant bits of the output buss with a pulse generated by gating TUACTC with the Parallel-Data-Strobe-pulse (PDS). XX The TUPDS pulse enters the AMTU through the cable board at location 3A2 J15 ~~is distributed to the four Positioner Counter boards~~ is routed and to the Priority Logic No. 2 board at location 3A1 J18 of theXXXXXX

TUIM. The TUPDS pulse is inverted to TUPDS* on the Priority Logic No. 2 board. TUPDS* enters the four Control Logic boards through pin 39 (See Sheet 28 Dwg 700903 for the Control Logic board at location 3A1 J28 serving TSUØ). The nineteen least significant bits of the AMCP output buss operate in TSUØ under mnemonics TØCI15 through TØCI23). Any one or more of these nineteen bits being set causes an associated latching circuit of the Register to latch set causing its associated output gate to produce a ground level.

2-3-2-2 Angular Position Monitoring

Refer to Sheet 80 of Specification A3ES33 for the format of the output buss from the AMTU to the AMCP during this function and the other functions associated with Preselection Monitoring. When the AMCP desires to monitor the angular position of Unit Ø within TSUØ, output buss bit from the AMCP designated (TØCI11 will be set during ACTC, causing a ground level to appear on the Select-Position-Counter-Ø (SPØ) line. This signal exits pin 56 of 3A1 J28 and enters Position Counter Board at location 3A1 J27 through pin 84 (Sheet 27 Dwg 700903). With SPØ operating the output of the Position Counter for TSUØ is placed on the output buss to the AMCP (OB15 through OB23). Once selected the output of this counter remains on the buss to be sampled by the AMCP whenever it chooses to do so. The counter is deselected by the AMCP issuing another ACTC command in which the TØCI11 bit is reset

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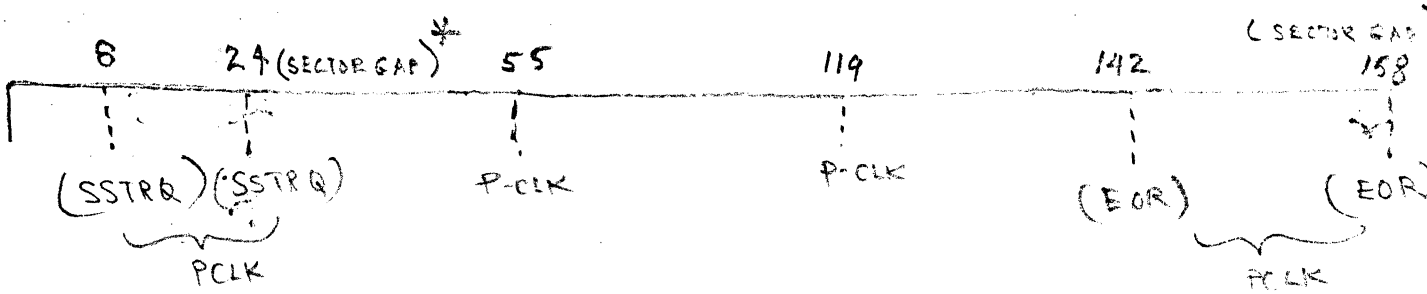
(a) Drum The following subparagraphs are concerned with detailed aspects of the implementation of the Angular Position Monitoring function for the Drum Devices.

1. Position Counter Incrementation The ~~following~~ discussion is referenced to TSUØ. The Position Counter in TSUØ (Sheet 27 Dwg 700903) is incremented by pulses operating under mnemonic PCLKØ. The PCLKØ pulse occurs with each end of record pulse and with each of three pulses representing a point in time within the record, as described on Sheet 54 of Specification A3ES33.XX The clock pulse which indicates the end of the gap and the beginning of the first third of a record is synchronous with the SSTRQ pulse generating ATTN as discussed in paragraph 2-3-1-2. The PCLKØ is decoded from the 8-stage counter on the Format Generator No. 1 board at location 3A1 J21 (Sheet 22 Dwg 700903). ~~XXX~~ This is the counter previously ~~XXXXXXXXX~~ introduced in the discussion of ATTN. ~~A Timing Diagram~~ See Figure 2-2 For Timing

NOTE

The counters and decodes for the PCLK's for ~~the other three~~ Unit 1 Position Counters ~~are~~ is also located on Format Generator No. 1 board of each Drum TSU, and the counters and decodes for the PCLKs for Units 2 and Unit 3 Position Counters are located on Format Generator No. 2 board of each Drum TSU.



* After every Fourth Record additional space is allowed at the end of a record referred to as Sector Gap. The Sector Gap Causes the End of Record (EOR) P-Clock and the SSTRQ P-Clock to be delayed by 16 Format bit clocks

Figure 2-2 Drum P-Clock Timing

2. Clock Specifications For detailed information regarding the prerecorded clock tracks for the two types of Drums used in the System, refer to the following listed Drawings:

DRUM TYPE	DRAWING NO.
~~XXXXXXXX~~ 201920	B700898
1851024	B700852

3. Clock Routing The bit clocks (BCØ through BC3) and index clocks (TACHØ through TACH3) enter the AMTU through the cable board at location 3A2 J19 (Sheet 52 Dwg 700903) for TSUØ and identical bit clocks and index clocks from the Units of TSU1 enter the AMTU through the cable board at location 3A2 J18 (Sheet 51 Dwg 700903). From the cable boards the clocks are routed directly to the Format Generator No. 1 boards.

(b) Disk The following subparagraphs are concerned with detailed aspects of the implementation of the Angular Position Monitoring function for the XX Disk Devices.

1. Position Counter Incrementation The following discussion is referenced to Disk Type TSU (TSU2). In a Disk type TSU, Angular Position Monitoring is essentially the same. However, since the rotational

the orientation of these pulses in regard to the Disk record format, refer to Sheet 56 of Specification A3ES33. The PCLKØ occurring between the gap and the first third of the record is synchronous with the Generate Attention (GATTN) pulse referred to in paragraph 2-3-1-2. The same counter decode on the Format Control board is used for both the GATTN pulse and the PCLK occurring at the end of gap.

2. Clock Specifications For detailed information regarding the prerecorded clock tracks for the Disk, refer to Drawing No. B700769.

3. Clock Routing The bit clocks (T2BØ through T2B3) and index clocks (T2TØ through T2T3) enter the AMTU through the cable board at location 3A2 J17 (Sheet 50 Dwg 700903) for TSU2 and identical bit clocks and index clocks from the Units of TSU3 enter the AMTU through the cable board at location 3A2 J16 (Sheet 49 Dwg 700903). From the cable boards, the clocks are routed directly to the Format Control boards.

2-3-2-3 Track Position Reporting This function applies to Disk type TSU's only. When the Position Counter for a Unit within a Disk TSU is selected the output of a Position Register dedicated to current Track Address of that unit is also loaded ont the output buss to the AMCP. Refer to Sheet 80 of Specification A3ES33 for the format of the output buss from the AMTU to the AMCP during this function. This Track Ad[illegible]

Position Register is a latching register, loaded from the output of the Track Address portion of the Disk Address Control Register. In the performance of an operational command (not to be confused with preselection Selection Status Monitoring) the Control Register output is compared with the Track Address already contained in the Position Register. If the two Track Addresses are different, the command Track Address is loaded into a Track Control Register within the R/W/S of the Disk File.

2-3-2-4 The discussion which follows concerns itself with the initial application of power to the AMTU and Disk File. When power is first applied, the Disk File may be at a different position than is indicated by the Position Register in the AMTU. Therefore if the output of the Position Register were sent to the AMCP immediately after power was applied, as part of the Preselection Status Monitoring function, the Track Position reported would not reflect the true position of the Disk File. To elimintate the possibility of this erroneous report, the AMCP must generate a Track Position command, which causes the Disk File to assume a position which will also be latched into the Position Register, and this command must precede Preselection Status Monitoring for any and all Disk Units. It must be reemphasized that the command Track Address from the AMCP is not loaded into the Disk File if it is the same Track Address already latched in the Position Register. This qualification prevents the unnecessary strobing of the Track Control Register in the R/W/S when the Disk File is already at the commanded track.

speed of a Disk is slower than that of a Drum and since a record on a Disk in six-bit parallel format as opposed to 24-bit parallel format on the Drum a different method of producing an incrementation pulse is used in the Disk TSU than that discussed for the Drum TSU. In the Disk prerecorded clock track pulses are also used to produce a pulse train. These pulses are given mnemonic BØ through B3 to identify Units Ø through 3 within a TSU. The TSU controlling a Disk is identified by adding the prefix T2 for TSU2 or T3 for TSU3. The T2BØ clock pulses enter the Disk Format Control board at location 3A1 JØ1 to be gated with the Unit 2 Ready signal (T2RDYØ) entering the board through pin 132. The T2BØ clock operates a four-stage counter. A decode of decimal 15 from the output of this counter signifies the end of a format word for Unit Ø (EØFWDØ). A format word is defined as two 50-bit data words. Since the number of 50-bit data words in a record is 286, there are 143 format words in a record. Format words are counted in an eight-stage counter on the Format Control board. A tap from the 8-stage counter signifying 32 format words, produces a PCLKØ pulse four times for each record. For information concerning

START

However, when Power is first applied to the System, the Position Register does not reflect the Disk XX File's actual Track position, and if a command Track Address from the AMCP contained in the output of the Track Address portion of the Disk Address Control Register happens to agree with the Track Address latched in the Position Register, the command Track Address is not strobed into the Track Control Register in the R/W/S of the Disk File. To prevent this ~~situation from occurring~~ the AMCP must generate at least two Positioning commands each to a different Track Address for each Disk Unit to assure that the Disk File is brought into the command loop with the AMCP. XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX Once established, this loop can only be XXXXX broken by removing power from the Disk File or the AMTU or both.

2-3-2-5 The Track Address portion of the Disk Address Control Register is located at 3A1 J2 through J4 (Sheets 3,4,and5 of Dwg 700903 for TSU2 and at 3A2 J2 through J4 (Sheets 35,36, and 37 Dwg 700903) for TSU3. The Track Position Registers are located at 3A1 J11 for TSU2 and 3A2 J11 for TSU3. ~~A detailed discussion of the~~ A detailed discussion of the logic implementing the concepts described XXX in this XXXX paragraph, is contained in paragraph 2-4-1, which is dedicated to the Position Only operation. It shall suffice to say here, that the output of one of the Position Registers is gated onto the output buss to the AMCP with the Select Position Counter bit (T2SPØ through T2SP3 for XXXXX TSU2) (Sheet 12 Dwg 700903) or (T3SPØ through T3SP3 for TSU3) (Sheet 44 Dwg 700903) which was selected by the AMCP as described in paragraphs 2-3-2-1

2-3-2-6 Position Not Valid This function applies to both Disks and Drums. Each time the PCLK operates to increment the position counter dedicated to the unit selected for Preselection Monitoring , the AMCP is informed by the setting of a dedicated bit on the output buss. This bit is referred to as Position-Not-Valid (PNV) and goes onto the output buss in bit position OB12. The logic involved is illustrated for TSUØ on Sheet 27 Dwg 700903. The Position-Not-Valid-Clock (PNVCLK) used in the logic is generated by halving through a flip flop a high frequency control clock (CC) (3.4MHZ for the 1851024 Drum and 4.4 MHZ for the 201920 Drum) produced by an oscillator on the Format Generator Board at Jack location 3A1 J23 (Sheet 23 Dwg 700903). In the Disk TSU the PNVCLK is generated by an oscillator on the Format Control board at location 3A1 JØ1 or 3A2 JØ1 (Sheets 2 and 34 Dwg 700903). The oscillator on the Format Control board is slaved to a prerecorded clock track and produces an output sixteen times the frequency of the prerecorded clock input. The output of the oscillator is halved on the Format Control board to produce a control clock (CC) with a frequency of approximately 8.2MHZ before being routed to its associated Position Counter board. The setting of the PNV bit signifies that the actual angular position of the Device being monitored is ambiguous until the bit is reset, since the Position Counter is in the process of changing state in one or more of its stages.

2-3-2-7 Busy/Write This function applies to both Disks and Drums. If the unit selected for preselection monitoring has already been selected for a functional operation by a process to be discussed in detail in later paragraphs, then, two other bits of information are returned to the AMCP over the output buss. These bits of information are Busy, indicating that the unit being monitored has accepted an operational instruction, and Write, indicating that the operation is to perform a transfer from Central Memory to a Device. The generation of an operational instruction and specifically for this discussion , the generation of a write instruction, will be discussed in later paragraphs. However for now, it should be noted that the inversion of an instructional decode signifying a read instruction is actually used in the logic (Sheet 27 Dwg 700903 for TSUØ). It should also be noted that READ is produced from a decode of two bits from the output of an Instruction Register. The two stages of the Instruction Register and the decode of READ are found on the Control Register board at location 3A1 J30 (Sheet 30 Dwg 700903) for TSUØ. The signal BSY, it shall suffice to say here, is produced when the last register in a register loading sequence associated with any operational instruction is loaded. This Register is always what is referred to as the Holding Unit Register. When it is loaded from the AMCP its output identifies the Unit which has been selected for the

commanded operation. The logic for producing BSY is on the Logic Control board location 3A1 J28 (Sheet 28 XX Dwg 700903) for TSUØ. BSY and write (WR) go onto the output buss in bit positions OB13 and OB14, respectively (Sheet 27 Dwg 700903).

2-3-2-8 RDPC Control Logic The data associated with the preselection status of the unit being monitored remains on the output buss to the AMCP until the AMCP deselects the unit being monitored by resetting bit 11 on the output buss from the AMCP while raising the ACTC signal. The data is sampled by the AMCP when the RDPC signal is raised by the AMCP. The strobing of data takes place in the AMCP. However the RDPC does enter the AMTU through the cable board at location 3A2 J15 (Sheet 48 Dwg 700903). From the cable board the RDPC signal enters the Priority Logic board at location 3A1 J19 where the signal is OR-gated with the ACTC and WTPC signal. When any of these three signals are generated by the AMCP the logic on the Priority Logic board returns an acknowledge signal (TUACK) to the AMCP. Other than the generation of the TUACK signal the RDPC signal has no significance to the AMTU during the Preselection Status Monitoring function.

2-3-3 OPERATIONAL COMMAND LOGIC The discussion which follows is concerned with the generation of operational commands by the AMCP and the logic required within the AMTU which translates the commands into the detailed functions required for their execution.

2-3-3-1 Control Registers Each operation to be performed by the AMTU is initiated by the loading of at least three and usually more Control Registers within the AMTU. The formats of these registers are shown on Sheet 79 of Specification A3ES33. The Control Registers are physically located on the five Control Register Boards comprising part of each TSU. Of the thirteen registers shown on Sheet 79 of Specification A3ES33, the following listed registers, only, are Control Registers:

CLASS Ø
CLASS 1
DEVICE ADDRESS
CENTRAL MEMORY ADDRESS
INSTRUCTION
MAP
UNIT NUMBER
WORD COUNT

NOTE

The remaining registers and counters shown on Sheet 79 of Specification A3ES33 are located on the Position Counter board of each TSU, with the exception of the Register Select latching register, which is located on the Control Logic board of each TSU.

(a) Control Register Board Bit Assignment Each Control Register board handles up to five bits of each Control Register according to the following assignment:

BIT NUMBER	CONTROL REGISTER BOARD
23-19	#1
18-14	#2
13-9	#3
8-4	#4
3-Ø	#5

NOTE

Control Register Boards are physically identical. The functional differences are implemented through back plane output input wiring. When a Control Register board does not require certain bits from the AMCP output buss for a given Control Register, the Control Register stages assigned to those bits are simply non-functional.

(b) Control Register Load Sequence To perform an operation with the AMTU, the Control Registers used must be loaded in a specific sequence. Every operation requires the generation of an Instruction command and the Instruction Control Register in which the command is stored must always be the first Control Register to be loaded. The unit within the selected TSU which is to perform the operation is determined by a unit selection command. The Unit Number Control Register in which this command is store must always be loaded last in the

load sequence. The order in which the other Control Registers are loaded is of no concern to the AMTU.

2-3-3-2 Activate (ACTC) Control Logic The AMCP selects one TSU for the execution of an operational command. It begins by raising ACTC to select one of the four TSU's as described in paragraph 2-3-2. The TUACTC signal combines with the signal identifying the selected TSU to select one of the eight Control Registers by setting one of the latching flip flops comprising the Register-Select Register (Refer to paragraph 2-3-2-1). Since an operational command depends on data from the AMCP, which will be loaded into the selected register the register selected must be cleared during the activate step, to prepare it for loading with the data to follow on the subsequent load step XX (WTPC). This is effected from the AMCP by setting bit 7 on the output buss from the AMCP, during the ACTC step. This bit being set also latches a flip flop in the Register-Select latching register, which stores it for additional gating during the WTPC step. Since the Instruction Register must be XXXXXXXXXXXXXXXX loaded first, bit 23 on the output buss from the AMCP must be set during the first ACTC and as stated before bit 7 on the output buss must also be set to generate a clear. Using the selection of TSUØ as an example, refer to Sheet 28 Dwg 700903, XXXX for the continuing discussion. For ease in identifying the logic functions discussed, the mnemonics associated with the logic continuity XXXX symbols for the gating involved is provided in the following list:

X10 TØTSUØ (TSUØ Select Bit)
X11 TØCIØ7 (Enable Load Bit)
B4 SWP (Swap Signal --Reset in This Gating)
B3 EOSWP (End-Of-Swap --Reset in This Gating)
C17 PDS (Data Strobe Pulse)
X1 TUACTC (XX Activate Signal)
X9 XX TØCI23 (Instruction Register Select Bit)
X12 (Load Sequence Flip Flop Set)
X2 WTPC (AMCP Load Signal)
C6 (Enable Load Bit Latched in XX Register)
X14 SHUN (Unit Holding Register Select Bit Latched in Register Select Register)

(a) Clear Instruction Register With the enable load bit and the Instruction Register select bit set and the activate (TUACTC signal raised, the data strobe pulse generates a clear pulse for the Instruction Register, (CLRI). Two other signals involved in the generation of XX CLRI as shown in the logic gating on Sheet 28 Dwg 700903, are Swap (SWP) and End-Of-Swap (EOSWP) which signify specific times within a function XXX not yet discussed. The signals are gated inhibitively here and prevent the generation of CLRI when the Swap function is taking place or XX immediately after.

(b) Set Load Sequence Flip Flop The same gating of signals except for the Swap inhibiting signals that produced CLRI is used to set a flip flop which shall be referred to as the load sequence flip flop. The XXXXXXXXXXXXXX XXXXXXXXX set output of this flip flop identified by the continuity symbol X12 becomes a reset enable for the load sequence flip flop and also enables the generation of the other seven Control Register clear pulses. The generation of the clear signal for any other Control Register also depends on the gating of another ACTC and PDS, represented by the signal identified by continuity

symbol C3 and the enable load bit being set during ACTC time. The activate signal would have to be one occurring subsequent to the activate which set the load sequence flip flop, and of course it would have to occur prior to the reset of the load sequence flip flop. The Control Register to be cleared would be determined by the Register XXX Select bit set on the AMCP output buss diring the activate step.

2-3-3-3 Load (WTPC) Control Logic The activate step is followed by a load step. The load signal from the AMCP (WTPC) enters the AMTU through the cable board at location 3A2 J15 (Sheet 48 Dwg 700903). XXX The signal is distributed to all four Control Logic boards under mnemonic TUWTPC. When the load signal operates the data strobe pulse (PDS) strobes the data on the AMCP output buss into the Control Register cleared during the preceding activate step. Its selection for loading is remembered by XXX a latching flip flop in the Register-Select register. This register remembers the selection until the next activate XXXXXXXXXXXXXX signal resets the selection bit of the just loaded register and sets the selection bit of the register next to be loaded.

(a) Generate Load Pulse (POT) The Control Register load pulse (POT) is produced by PDS strobing WTPC at a gate which also contains the TSU select bit XXXXXXXXXX (TØTSUØ) for TSUØ (Sheet 28 Dwg 700903). Also at the gate are the load sequence flip flop set output, and the output of the enable load latching flip flop of the Register Select register. The two inhibit signals

associated with the Swap function are also present at the gate.

(b) Data Routing ~~For the convenience of the reader the routing of the output data from the AMCP is presented here again.~~ The 24-bit output buss enters the AMTU through the cable board at location 3A2 J15 (Sheet 48 Dwg 700903). From the cable board the buss lines are routed to the Priority Logic board of the TUIM in location 3A1 J19 (Sheet 20 Dwg 700903). From the Priority Logic board the data lines are routed to the Control Register boards according to the bit assignmnet specified in paragraph 2-3-3-1 (a). The data lines enter the Control Register boards under mnemonic (TUCIØØ through TUCI23).

(c) Typical Control Register Clear Load Gating The continuing discussion is based on the logic on Sheet 29 Dwg 700903 and uses the Unit Control Register as an example. The Unit Register clear pulse from the Control Logic board (CLRI) enters the Control Register board for the least significant bits of the AMCP output buss, through pin 100 at location 3A1 J29. The pulse operates on the Control Register board under mnemonic TØCLRUN for TSUØ . This pulse resets the two-stage Unit Control Register. This occurs during the activate step. When the WTPC signal is raised the POT pulse operates. POT enters the same board through pin 49 and is gated with the data at every Control Register jam-set control gate on the board. A third signal operating is the signal representing register selection. This signal is the output of a flip flop set in the latching Register Select register on the Control Logic board. When the

Unit Register has been selected during the activate step the TØSHUN signal is raised and the jam-set control gates to which TØSHUN is presented are enabled and the POT pulse strobes data into the register stages controlled by TØSHUN. In the case of the Unit Register, the data bits involved are TUCI23 and TUCI22 entering the Control Register board through pins 118 and 112, respectively. When a data bit is high, the Control Register stage with which it is associated, sets, and when a data bit is low, the Control Register stage with which its is associated, remains reset. The other Control Registers operate in an identical manner. The only things which differ are the clear pulse, the register select bit, and the assignment of data bits.

(d) Reset Load Sequence Flip Flop To reset the load sequence flip flop , which was set with the Instruction Register selection, (Refer to paragraph 2-3-3-2(b)) a Unit Register selection must be made. The gating of WTPC with the enable load signal and the Unit Register Select (SHUN) signal generates a K-enable for the load sequence flip flop (Sheet 28 Dwg 700903) for TSUØ. The down-edge of the PDS strobe pulse occurring in the WTPC following the latching of these two signals into the Register Select register, causes the load sequence flip flop to set, signifying the completion of the load sequence.

(e) Set Busy and Registers Full Flip Flops The POT pulse

which strobes data into the Unit Register is gated with the Unit Select bit stored in the Register Select Register (SHUN) to produce a jam-set for a Registers Full (RFUL) flip flop and a clock-set for a Busy (BSY) flip flop. It is significant to note that both of these flip flops are set at the end of the load sequence. The resetting of these flip flops is produced by the Swap function, which is discussed in later paragraphs. The logic for these flip flops which is identical for all four TSU's is shown for TSUØ on Sheet 28 Dwg 700903.

2-4 IMPLEMENTATION OF OPERATIONAL COMMANDS

The discussion which follows is concerned with the implementation of each of the possible operational instructions given by the AMCP to the AMTU. Since the interface with the AMCP is of prime concern for this part of the discussion, data flow from Central Memory and data requests to Central Memory will be covered in its most general aspects while the detailed discussion will be dedicated to the control and the select-unit. aspects of each operation which interface with the AMCP. Beginning with paragraph 2-5, the data request logic ~~and data flow logic~~ is discussed in detail.

2-4-1 POSITION ONLY FUNCTION This function applies to Disks only. The discussion which follows will concern itself with TSU2 only . Implementation of Position Only for TSU3 is accomplished in an identical manner. Refer to Sheet 80 of Specification A3ES33 for the instruction format. Bits 15 through 21 on the output buss of the AMCP are used in generating any instruction. Bit 21 is set for a Position Only function. The Drum Policy bit and the Continue bit must be reset. Bit 17 an 18 have no significanee during a Position Only function and the control functions with which they are identified will be inhibited by the Position Only bit being set.

2-4-1-1 Position Only Load Sequence The Instruction Register is loaded first as always with bit 21 being set and bits 16 and 20 being reset. The state of the data loaded into the other stages of the Instruction Register is of no significance to the AMTU. The logic for loading the Instruction Register for TSU2 is shown on Sheets 7 and 6 of Dwg 700903. When the Instruction Register has been loaded the AMCP generates another ACTC signal during which the Instruction Register Select bit in the latching Register Select Register is reset and the Device Address Select flip flop in the Register Select register is set. This is bit 21 on the AMCP output buss and produces the output (SDA) out of the latching flip flop as it clears the Device Address Register under mnemonic T2CLRDA (Sheets 6 and 7 Dwg 700903). The WTPC following ACTC loads the Device Address Control Register with the data on the AMCP output buss. When a Position Only command is operating, only the Track Address portion of the Device Address is of concern. The Track Address portion of the Device Address is shown on Sheets 3,4,and 5 Dwg 700903. The AMCP follows with another ACTC signal during which the Device Address Register Select bit is reset and the Unit Register Select bit is set and a clear pulse is generated for the Unit Register on the Control Register board at location 3A1 JØ6 (Sheet 6 Dwg 700903). The clear pulse enters this board under mnemonic T2CLRHUN. When the AMCP follows the ACTC with the WTPC, the data on the AMCP output buss loads the Unit

Register. The Unit Select bit from the Register Select register enters the Unit Register board at location 3A1 JØ6 under mnemonic T2SHUN.

2-4-1-2 Swap Function (General) The Control Registers are implemented in pairs. The Control Register of each pair, which is loaded from the AMCP is referred to as the Holding Register. At the end of the load sequence and at other times (to be discussed as appropriate) the contents of the Holding Register is loaded into the second Register of each pair referred to as the Functional Register, and the contents of the Functional Register is loaded into the Holding Register. This cross-loading between Control Register pairs, is referred to as swapping. The great advantage of a duplicate set of Registers for each function is that the AMCP can load the Holding Registers required for an operation anticipated, while the Functional Registers hold the information required for the current operation. The Functional Registers are also swapped back into the Holding Registers at the end of an operation. This enables the AMCP to interrogate these registers by selecting them with an ACTC and it enables the reading of the contents of the registers by following with an RDPC.

New Instruction

(a) Generate Swap In the Position Only operation the swapping function begins at the end of the register loading sequence. The gating of the reset state of Busy (BSY*) and a signal produced by the WTPC during which the Unit Holding Register is loaded with the SHUN signal, produces a signal when BSY* goes

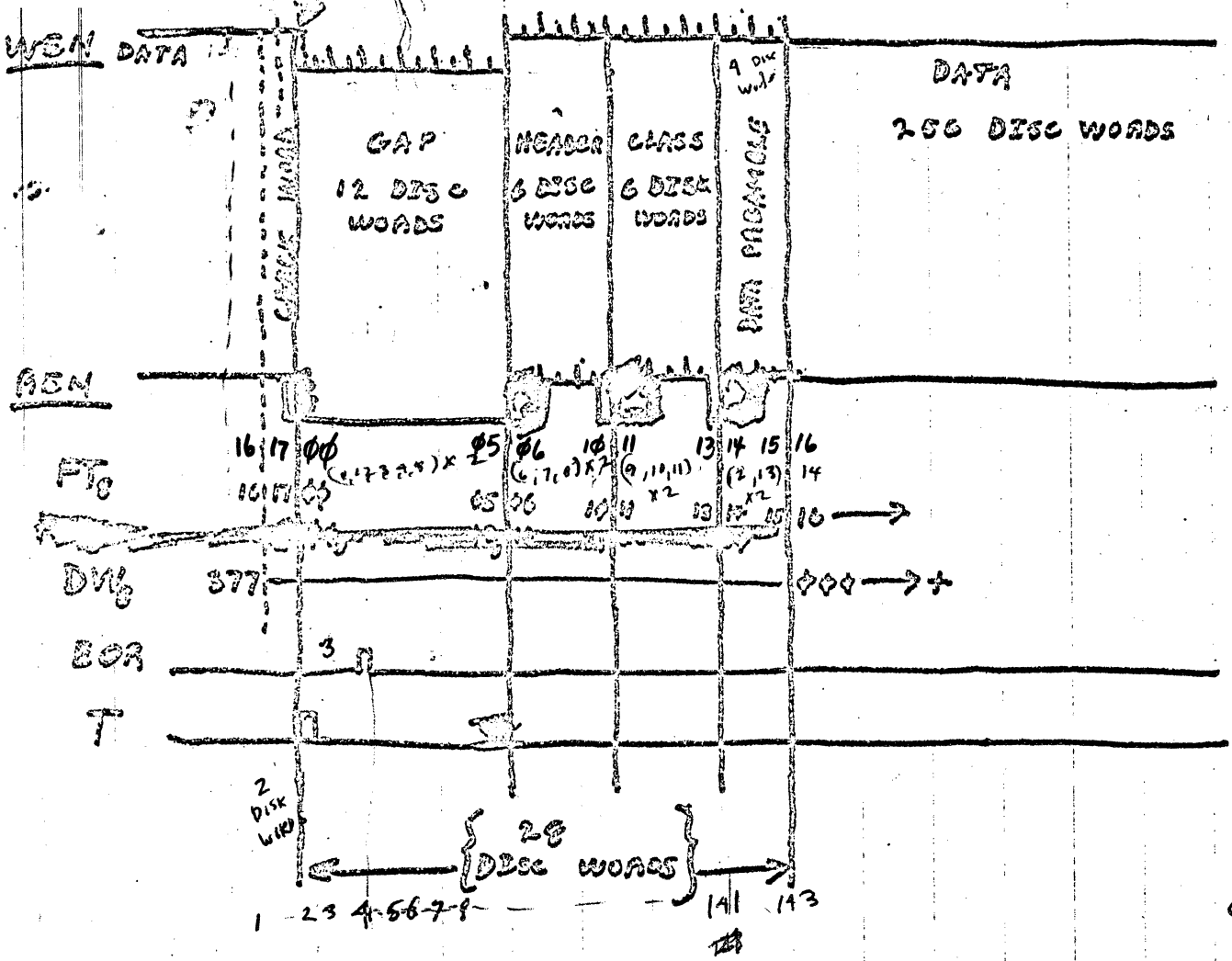
low. This signal sets a flip flop which XXXX shall be referred to as the Swap Required (SWPRQ) flip flop. For the logic just discussed, refer to Sheet 8 Dwg 700903. The gate controlling the flip flop is on the XXX left hand side of Sheet 8. The BSY* signal is identified by the continuity symbol A12 and the load Unit Register WTPC is identified with the continuity symbol A13. The SWPRQ signal is gated with a pulse signifying the end of a record on the Disk (EORP).

(b) Generate End Of Record Pulse For the following discussion refer to the Format Control board at locationXX 3A1 JØ1 (Sheet 2 Dwg 700903). The format word counter discussed in paragraph 2-3-2-2(b) 1 , generates a pulse which latches a flip flop to the set state at the end of 141 format words. This marks the end of the space dedicated to the data field for each record. Six format word times later XXXXXXXXXXXXXXXXXXXXXXXX (accounted for by the two format words filling out the sector space to 143 format words in the sector format and the decode of four from the format word counter in a new count cycle for a new sector format) the end of record pulse (EORP) is generated (See figure 2-3 for the Format Control Timing).

(c) Swap Counter The EOR signal enters the ~~Format~~ Control Logic board through pin 87 (Sheet 8 Dwg XXX 700903) and sets a flip flop. The output of this flip flop enables another flip flop which is set by the high freguency clock pulse (CC) which XXXXXXX was discussed in paragraph 2-3-2-6. When the second flip flop sets the EORP signal is produced. EORP enables a XXXX third flip flop which sets on the following CC pulse. The output of this

B 200 DISC RECORD FORMAT

9/22/68 RLF



572
25-bit Words in A SECTOR

286
DISK WORDS IN A SECTOR

143
FORMAT WORDS IN A SECTOR

ONE FT = 2 DISK WORDS

ONE DISK WORD = 2 24 BIT WORDS + 2 P

BOR - END OF RECORD

FT_D - FORMAT TIME - OCTAL DECODE OF FORMAT GENERATOR

DW_8 - DATA WORD TIME - OCTAL DECODE OF DATA WORD COUNTER

DATA WORD COUNTER COUNTS DISK WORDS

Figure 2-3 Disk Format Timing

flop , which sets on the following CC pulse. The output of this third flip flop enables the CC pulses from the Format Control board to operate the Swap Counter. This counter is a Johnston counter which produces nine significant periods during a complete cycle before resetting.

(d) Swap Flip Flop The SWPRQ and EORP signals are gated to produce an enable for another flip flop, which shall be referred to as the Swap Flip Flop. This flip flop sets with the first CC pulse after the EORP signal. When set,this flip flop generates the Swap (SWP) signal.

NOTE

The Swap counter operates at the end of each record without regard to the Swap (SWP) signal. However most of the decodes of the Johnston counter are gated with SWP to produce the pulses associated with the Swap function.

2-4-1-3 Swap Function During Position Only Operation The continuing discussion shall consider the nine decodes of the Swap Counter as far as they relate to the Position Only function.

(a) Swap Count 1 The decode of 1 out of the Swap Counter is gated with SWP, the reset state of a Continue flip flop (CONF*) and the CC clock to produce the Swap Device Address(SWDA)pulse. The Continue flip flop was inhibited from setting by the Continue bit (bit 16 in the Instruction Register)being reset,as required in a Position Only command).

SWDA is a clock pulse which loads the Functional Device Address Register with the contents of the Holding Device Address Register and loads the Holding Device Address Register with the contents of the Functional Device Address Register. Only the Track Address portion of the Device Address Register is of concern during a Position Only operation (Sheets 3,4, and 5 Dwg 700903).

(b) Swap Count 2 This decode of the Swap Counter is not used in the Position Only operation.

(c) Swap Count 3 The decode of 3 out of the Swap Counter is gated with SWP, CONF*, and CC to produce the Swap Unit Register and Swap Instruction Register (SWUNI)pulse. The SWUNI pulse is used to swap the contents of the Unit and Instruction Holding Registers with the Unit and Instruction Functional Registers (Sheet 7 Dwg 700903). The output of the Functional Unit Register is used to decode a Unit selection. The decode is located on the Control Register board at location 3A1 J6 (Sheet 7 Dwg 700903). The decoded outputs (T2UØ-T2U3) are dedicated each to a separate Disk File Unit.

(d) Swap Count 4 This decode of the Swap Counter is not used in the Position Only operation.

(e) Swap Count 5 This decode from the Swap Counter is gated with the Registers Full (RFUL) flip flop set output, signifying that the load sequence has ended but that the Swap sequence is in progress. (The RFUL flip flop is reset at the end of the Initial Instruction Swap Counter Cycle by the CC clock.).

An additional signal gated is the new unit (T2NEWU) signal produced by a comparison of the outputs of the Holding Unit Register and the Functional Unit Register. The logic for the generation of T2NEWU is on the Control Register board at location 3A1 JØ6(Sheet 7 Dwg 700903). When a new unit has been selected T2NEWU is raised, and this gate produces the SETNUN* pulse. The SETNUN* pulse sets a latching flip flop (NUN) causing its reset output to go low. The NUN* reset output of this latching flip flop is presented to a gate controlled by Swap Count 9. The function of NUN* at that gate will be discussed in paragraph 2-4-1-4 dedicated to Swap Count 9.

(f) Swap Count 6 This decode of the Swap Counter is not used in the Position Only Operation.

(g) Swap Count 7 This decode from the Swap Counter is gated with bit 20 from the Instruction Register, which is reset on a Position Only operation. The bit 20 output operates under the mnemonic Drum-Policy-Not (DPOL*). The output of this gate representing count 7 during a Disk Policy Instruction, is gated with the SWAP and RFUL signals. The RFUL signal indicates that the Swap Cycle in effect resulted from a new instruction. The output of this gate produces a Transfer-Track-Address (XTA) pulse.

1 Track Address Latched This pulse loads the output of the Track Address portion of the Device Address Functional Control Register into one of four latching Track Position Registers on the Track Position board at location 3A1 J11 (Sheet 12 Dwg 700903) for TSU2. The Position Register loaded is dependent upon the Unit selected. These four latching Position Registers serve to hold the Track Address of each of the four devices assigned to a given Disk TSU, allowing the AMCP to monitor Track Address with angular position as part

of Preselection Status Monitoring.

2 Track Address Compare A second function served by the Position Registers is a comparison of present Track Address with the Command Track Address to determine if a strobe pulse must be generated to load the command Track Address in the Device Address Control Register into a Track Control Register in the R/W/S of the selected Disk File Unit. This compare function is implemented by gating the Track Address (T2TAØ through T2TA7) with the Track Address from the Position Register of the Unit selected (Sheet 12 Dwg 700903). The output of this gating is Address-Not-Equal (T2ANE). If the addresses are not equal, this signal is high. Actually, the comparison is taking place constantly , but the comparison is strobed by T2XTA of the selected Unit (signified by the C1 continuity symbol in the logic. The strobe takes place while T2XTA is high and a Positioner-Strobe-Pulse (T2POSP) is produced if the addresses are not equal. It should be noted that the down-edge of T2XTA loads the command Track Address into the Position Register dedicated to the selected Unit and therefore the comparison gate will produce an equal compare indication until a different Track Address is loaded into the Track Address portion of the Device Address Control Register.

3 Track Address Routing to R/W/S The Track Address out of the Device Address Control Register (T2TAØ through T2TA7) is routed through the Disk Cable card at location 3A2 J17 (Sheet 50 Dwg 700903) out of the AMTU into the ~~Positioner~~ Track Control

Register in the R/W/S of the selected Disk File unit. The T2POSP pulse is routed through the same cable board out of the AMTU into the R/W/S of the selected Disk File Unit and loads the Track Address into ~~the~~ its Track Control Register as it operates.

(h) Swap Count 8 This decode from the Swap Counter is gated with SWP to generate the Reset-Swap (RSWP) signal. The RSWP signal is used as a J-enable for an End-Of-Swap (EOSWP) flip flop which sets on the next CC clock and a K- enable for the Swap (SWAP) flip flop which resets on the next CC clock.

(i) Swap Count 9 When the CC clock operates to produce this decode the RFUL signal is still raised and the RSWP signal is high from Swap Count 8. A gating of RFUL and RSWP produces a J-enable for a flip flop which sets with the CC, producing Swap Count 9. The output of this flip flop remembers the condition where RFUL was raised, signifying a new instruction, and the ~~XXX~~ generation of RSWP, until the information is no longer required. This flip flop shall be referred to in text as the Swap-Complete-New-Instruction (~~XX~~ SCNI) flip flop. The set output of the SCNI flip flop is required for the generation of the Equal-Strobe-Pulse (EQSTRB) to be discussed. The RSWP signal is gated with the reset state of a Continue Switch (CONTSW*) signal which is always reset except when operating the AMTU in a maintenance mode. This gating produces a reset for the RFUL flip flop. It should be noted that the same clock which resets the RFUL flip flop also sets the SCNI flip flop. This same CC clock sets the EOSWP flip flop enabled by RSWP during Swap Count 8, thereby producing the End-Of-~~XX~~ Swap-Pulse ~~XX~~ (EOSWP) and the CC also resets the SWAP flip flop.

2-4-1-4 Generate Equal-Strobe (EQSTRB) Swap Count 9 is gated with the set output of the Swap-Complete-New-Instruction(SCNI) flip flop and the NUN* signal. If the Unit number in the Functional Unit Register agrees with the Unit number in the Holding Unit Register, the EQSTRB pulse is generated at this time. If the Unit number loaded into the Holding Unit Register does not agree with the Unit number in the Functional Register XXXXXXXXXXXXXX the NUN* signal will be low inhibiting the generation of EQSTRB. The continuing discussion is based on the case where the Unit numbers do not agree. The significance of the Unit numbers not agreeing is in that the EOR pulse which initiated the Swap Counter Cycle under discussion is associated with the Unit number selected by the Functional Unit Register prior to Swap Count 3 and has no reference to the End-Of-Record time for the Unit selected by the output of the Functional Unit Register after Swap Count 3. Therefore the EOR of the new Unit selected by the Functional Register is XX used to reset the NUN latching register and to initiate another Swap Counter cycle. When Swap Count 9 is reached again in this cycle the EQSTRB pulse is produced since the NUN* signal is high. If the EOR pulse generated by the New Unit XXXXXXXXXX selected by the Functional Unit Register XXXX occurs during the Swap Count Cycle which generated the Unit Register Swap (Swap Count 3 of a new instruction from AMCP) it is ignored. The AMTU, then, has to wait for the next EOR of the New Unit to reset NUN and to produce the EQSTRB pulse. The logic

for ignoring the New Unit EOR during a Swap Count cycle, involves the setting of a flip flop with the EOR occurring before the Swap Count Cycle and using the reset output of this flip flop to inhibit the generation of EORP, which is required to reset the Swap Counter and to enable its incrementation by the CC clock. The Swap Count decode of 9 is used as a K-enable for this same flip flop and the CC clock following Swap Count 9 resets the flip flop permitting the next EOR (New Unit EOR if New Unit has been selected) to initiate another Swap Count Cycle.

2-4-1-5 Generate End Of Position Operation Swap Required When the EQSTRB pulse is generated, it strobes a gate at which the Position Only (POSIT) signal is present, thereby producing a jam set for the Swap Required flip flop. This EOR generates EORP as previously discussed. EOR EORP is gated with SWPRQ to produce a K-enable for the SCNI flip flop and the following CC clock resets the flip flop. The SWPRQ signal waits for the next EOR pulse which generates EORP and consequently another SWP signal.

2-4-1-6 End Of Operation Swap Count Cycle The continuing discussion is based on the assumption that no new instruction from the AMCP was received while the Position Only operation was being executed.

(a) Swap Count 1 The SWDA pulse is produced again causing the Functional Device Address Control Register to swap its contents with the Holding Device Address Control Register. Since the output of the Holding Registers are gated onto the

input buss to the AMCP, the Device XXX Address of the just completed operation is available to the AMCP, and can be monitored by the generation of an ACTC selecting the Device Address Register followed by a RDPC which permits sampling the buss by the AMCP. Swap Count 1 also produces the Load-Status-Error (LDST) pulse which loads the output of ∧ indicators into a Status Register, (Status is discussed in detail in paragraph 2-

(b) Swap Count 2 This decode is not used in the Position Only operation. to produce the Clear Error indicator (CLERR) pulse which resets all status error indicators, (Status is discussed in detail in paragraph 2-)

(c) Swap Count 3 The SWUNI pulse is generated again causing a swap of the Unit XX Registers. The Unit operating during the just completed operation thus becomes available to the AMCP upon request.

(d) Swap Count 4 This decode of the Swap Counter is not used in the Position Only operation.

(e) Swap Count 5 Since the Registers Full (RFUL) flip flop is reset the SETNUN* pulse is not produced.

(f) Swap Count 6 This decode is not used in the Position Only operation.

(g) Swap Count 7 Since the XXXX Registers Full (RFUL) flip flop is reset, the Transfer Track Address (XTA) pulse is not produced.

(h) Swap Count 8 This decode from the XX Swap Counter is gated with SWP again to produce a J-enable for the EOSWP flip flop. and also generates the RBSY* pulse which resets the Busy (BSY) flip-flop.

(i) Swap Count 9 The EOSWP flip flop sets with the CC clock producing Swap Count 9. The EQSTRB pulse, however, is

inhibited by the SCNI flip flop being reset. Therefore no SWPRQ signal is produced until a new operational instruction is received from the AMCP.

2-4-2 WRITE DATA AND CLASS CODE This operation applies to both Drums and Disks. The discussion which follows will reference TSUØ for the logic implementing this operation as pertains to Drums and will reference TSU2 for the logic implementing this operation as pertains to Disks. Refer to Sheet 80 of Specification A3ES33 for the instruction format. Bit 21 on the AMCP output buss must be reset for both Drums and Disks since Position Only is a completely independent operation as discussed in paragraph 2-4-1. Bit 20 on the output buss may be set to signify Drum Policy or reset to signify Disk Policy. Bit 19 should be reset. Bits 17 and 18 should be set to produce the Write instruction. Bits 15 and 16 should also be reset.

2-4-2-1 Write Data And Class Code Load Sequence For this operation the following Holding Control Registers are loaded:

INSTRUCTION
CLASS Ø
CLASS 1
DEVICE ADDRESS
CENTRAL MEMORY ADDRESS
MAP (OPTIONAL)
WORD COUNT

One Control Register is loaded from the AMCP output buss, with each pair of ACTC and WTPC commands as discussed in paragraphs

2-3-3-2 and 2-3-3-3. The Instruction Register is loaded first and the Unit Register last, as discussed in detail in paragraphs 2-3-3-2(b) and 2-3-3-3(d).

(a) Generate Swap Required And Start Swap Counter For this operation a Swap Required (SWPRQ) signal is generated at the end of the Register Loading Sequence, as discussed in paragraph 2-4-1-2(a) and the End-Of-Record pulse (EOR for Disk and ERPØ for Drum) entering pin 87 of the pertinent Control Logic board (Disk or Drum, as the case may be) under mnemonic EOR, initiates a Swap XX Counter Cycle, as discussed in paragraphs 2-4-1-2(b,c and d)

2-4-2-2 Swap Function XXXXXX During XXXXXX Write Data And Class Code XX Operation The continuing discussion shall consider the nine decodes of the Swap Counter as far as they relate to a New Instruction of Write Data and Class Code. Control logic is the same for Drum and Disk TSU's but the Drum Control logic board (Sheet 28 Dwg 700803 is to be referenced for the continuing discussion.

(a) Swap Count 1 The decode of 1 from the Swap Counter is gated with Swap (SWP) the reset state of the Continue flip flop (CONF*) and CC to produce the Swap Device Address (SWDA) pulse. The Continue flip flop was inhibited XX from setting by the Continue bit (bit 16 in the Instruction Register) being XXXX reset. SWDA is a clock pulse which loads the Functional Device Address Register with the content of the Holding Device Register loaded from the AMCP.

1 Drum Device Address Device Address for a Drum consists of a Band Address and a Record Address.

Band Address The Drum Band Address is carried by bits 10 through 16 of the AMCP output buss, and is loaded into the

Drum Band Address Register on Control Register boards No. 2 and No. 3 (Sheets 30 and 31 Dwg 700903). The output of the Drum Functional Band Address Control Register (TØBAØ-TØBA6) is routed through the cable card at location 3A2 J19 (Sheet 52 Dwg 700903) into the R/W/S of the selected Drum Unit. The Band Address bits are used by the Drum R/W/S to select a group of 24 parallel read/write elements (heads) for writing on the Drum surface.

Record Address The Drum Record Address is carried by bits 17 through 23 of the AMCP output buss, and is loaded into the Record Address Register on Control Register boards No. 1 and No. 2 (Sheets 29 and 30 Dwg 700903).

NOTE

The carry bit between stages 2 and 3 and between stages 4 and 5 are brought out of the Control Register board. Continuity to the next stage is implemented by back plane wiring when required. The carry bit is implemented this way to accomodate those address register stages where a carry bit is not desired. In the case at hand, a break is required between the Record Address stages MSB of Record Address and the LSB of the Band Address Register. The break is required since incrementation of Drum Band Address is not a function of the MSB of Drum Record Address.

The output of the Drum Record Address Functional Control Register (TØRAØ-TØRA6) is routed to the Position Counters board at location 3A1 J27 (Sheet 27 Dwg 700903) to be compared with the Position Counter decode of the selected Drum unit. Since only outputs from stage 2 and above of the position counter are looked at in the comparison, the decode is equivalent to a sector count. When the Drum sector count decoded from the Position Counter is equal to the Drum Record Address from the Drum Record Address Functional Register (TØRAØ-TØRA6) Record-Compare-Equal (RCE) is produced. It is to be noted that the output to the comparator from the Position Counter is gated by XXXXX a Unit selection bit (UNØ) in this case, as decoded from the Functional Unit Control Register whereas the output to the AMCP from the Position Counters is selected by a Register Select bit latched during an ACTC when Preselection Status Monitoring is being performed . The output signal being (SPØ) in that case.

NOTE

On a Drum Policy Instruction the Record Address in the Record Address Functional Control Register must agree with the Position Counter output of the selected Unit before Swap Count 9 is XX reached in the Swap Count Cycle generated by the EOR of the unit which is selected at Swap Count 3 of the Instruction Cycle. If the Unit selected is not a New Unit,

(RCE) must be produced in the Instruction Cycle. Since the EOR beginning the Instruction Swap Cycle also increments the Position Counter, there are eight CC clock periods before Swap Count 9 is reached when the selected Unit is not a New Unit.

2 Disk Device Address The Device Address for a Disk File consists of a Track, Band, and Record Address.

Track Address The Track Address is carred by bits 2 through 9 of the AMCP output buss, and is loaded into the Track Address Register on Control Register boards No. 3, No. 4, and No. 5(Sheets 3,4,and 5 Dwg 700903). The Track Address Functional Register output is not looked at until Swap Count 7 of the Instruction Cycle.

Band Address The Disk File Band Address is carried by bits 10 through 16 of the AMCP output buss,and is loaded into the Disk File Band Address Register on Control Register boards No. 2 and No. 3 (Sheets 5 and 6 Dwg 700903). The output of the Disk File Band Address Register (T2BA1-T2BA6) is routed through the cable card at location 3A2 J17 (Sheet 50 Dwg 700903), into the R/W/S of the selected Disk File Unit.

NOTE

One MSB stage on the Control Register board is not required for Disk File Band Address.

Class Ø Control Register. The Class Ø word is carried by bits Ø through 23 and is loaded into the Class Ø Register located on Register boards No.1 through No. 5.

Class Ø (Drum) The output of the Drum Functional Class Ø Register is gated out with the Enable-Class-Ø (ENCLØ) signal produced on the Drum Format Generator board (Sheet 22 Dwg 700903). A discussion of the generation of ENCLØ will be deferred to a later paragraph. The (TØCLØØ through TØCL23) output from the Drum Functional Class Register is presented to gates on the Data Buffer boards at locations 3A1 J24, J25, and J26 (Sheets 24,25, and 26 Dwg 700903). The Class bits are gated with a level signifying the window or space allocated to the writing of the Class Ø word, just preceding the data field of each record. This Class window is given mnemonic Class Time (CLTM). The CLTM signal is also produced on the Format Generator board No. 1 (Sheet 22 Dwg 700903). Detailed discussion of the generation of CLTM will be deferred to a later paragraph. The third and last signal gated with the Class bits is the Write Enable signal (WEN) produced on the Format Generator No. 1 board (Sheet 22 Dwg 700903). This signal switches on the Write amplifiers of the selected address in the Drum Unit selected and enables the Class Ø word to be written onto the Drum.

Class Ø Disk File The output of the Disk File Functional Class Ø Register (Sheets 2 through 6 Dwg 700903) is gated onto the C-Buss to be loaded into the C-Register on the Data Buffer boards at locations 3A1 J9 and J10 (Sheets 10 and 11 Dwg 700903). The mnemonic is (T2CBUSØØ -T2CBUS23). The signal gating the Class Ø Functional Register output onto the C-Buss is given mnemonic T2CLØBUS and is produced by logic on the Disk Control A and Disk Control B boards at locations 3A1 J12 and 3A1 J13 (Sheets 13 and 14 Dwg 700903). The generation of T2CLØBUS will be discussed in detail in later paragraphs. The Class Ø word in the C-Register is shifted into the last 25-bit positions (including parity) within sections of the "D" Shift Registers, and from each of the six "D" shift Registers sections to associated dedicated read/write element (head) to be written as part of a 50-bit word onto six-bit parallel fashion on the Disk surface. The "D" Registers sections are also shown on Sheets 10 and 11 Dwg 700903. The timing pulses required for this scheme is implemented on the Format Control board at 3A1 J01 (Sheet 2 Dwg 700903 and the Disk Control A and Disk Control B boards at locations 3A1 J12 and J13, respectively (Sheets 13 and 14 Dwg 700903). The timing logic will be discussed in detail in later paragraphs.

2-4-2-15.

(h) Swap Count 8 This decode of the Swap Counter is gated with CONF* to generate a Swap Class Register 1 (SWPCL1) pulse. This pulse swaps the Functional and Holding Class 1 Control Register. The Class 1 word is carried by bits Ø through 23

on the AMCP output buss and is loaded into the Class 1 Register located on Control Register boards No. 1 through No. 5. Swap Count 8 also ~~XX~~ produces a Reset-Swap K-Enable signal (RSWP).

1 Class 1 Drum The output of the Class 1 Functional Register is gated with ENCL1 produced on the Drum Format Generator board ~~XXXXXXXX~~ (Sheet 22 Dwg 700903). This second Class word is handled in an identical manner to the Class Ø word except it is processed immediately following Class Ø~~XX~~ in time.

1 Class 1 Disk The output of the Disk File Functional Class 1 Register is gated onto the C-Buss with the T2CL1BUS signal and subsequently is shift-loaded into ~~the first~~ 25 bit positions (including the parity bit) of the ~~six "D"~~ sections of the D Shift Registers. From ~~each of the "D" Registers~~ these sections of the D-Register, the Class 1 word is shifted into a dedicated read/write element (head) to be written ~~in six-bit parallel fashion~~ on the Disk surface. Class Ø and Class 1 words form what is termed herein a Disk Word, which is 50 bits in length including the two parity bits.

~~XX~~(i) Swap Count 9 This counter decode operates as described in paragraph 2-4-1-3 (i).

2-4-2-3 Generate-Equal-Strobe (EQSTRB) The EQSTRB pulse is generated as discussed in paragraph 2-4-1-4.

2-4-2-4 EQUAL(Drum) In the Write Data and Class Code operation on a Drum Unit, EQSTRB is gated with several signals which indicate, when they are in the correct state, that the Drum has reached

the command starting address loaded into the Device Address Control Registers by the AMCP and swapped into the Functional Device Address Register with the CC clock during the Swap Count 1 decode. The signals gated with EQSTRB (Sheet 28 Dwg 700903) are Ready for Unit Selected (RDYØ through RDY3), NO-Register-Loading-Vilolation (RLV*) (Continuity symbol A15), No-Position-Command (POSIT*), and Record-Compare-Equal (RCE) (Refer to paragraph 2-4-2-2(a)1 Record Address for a discussion of RCE). Failure to obtain EQ inhibits the switching on of the Write amplifier and inhibits the operation of the Central-Memory-Request logic. Loss of EQ after once obtaining it, does not switch off the Write amplifier but does inhibit the Central-Memory Request logic and that portion of the record following the loss of EQ will be filled with logic zero bits.

2-4-2-5 Equal (Disk File) In a Write Data and Class Code operation on a Disk File Unit, EQ is produced by a gating of essentially the same signals as for a Drum Unit (Sheet 8 Dwg 700903) and two other signals dealing with the Track Positioning portion of the Disk File Address. One of these signals T2ANE*, should be low indicating that the Track Address contained in the output of the Track Address Functional Control Register is equal to the Track Address contained in the Unit Selected latching Position Register (Sheet 12 Dwg 700903). The other signal is Track Verification (TV). This signal is generated

by a time-out equivalent to six revolutions from the moment T2XTA was produced by Swap-Count 7 in the instruction Swap-Cycle (See Sheet 12 Dwg 700903 for implementation). TV is normally generated by this time-out after a Position Only command. A second means of achieving Track Verivication (TV) is by counting 24 consecutive header fields from about the time the read amplifier is switched on within the record following the End-Of-Record pulse produced by the Unit Selected in the Write Data Class Code instruction. The logic implementation for this means of achieving TV is also on Sheet 12 Dwg 700903. The header field and header count is discussed in paragraph 2-4-2-13. It shall suffice for now to state that the header-field precedes the data field of each record and its content is the address of the sector in which each of the six selected Read/Write heads is located. The failure to obtain EQ inhibits the switching on of the Write amplifier and inhibits the operation of the Central-Memory-Request logic. Loss of EQ after once obtaining it, does not switch off the Write amplifier, but does inhibit the Central-Memory Request logic and that portion of the record following the loss of EQ will be filled withlogic zero bits.

NOTE

The continuing discussion, beginning with paragraph 2-4-2-6, will concern itself first, exclusively with the record format logic for a Drum TSU and beginning with paragraph 2-4-2-11 the discussion will dwell on the record format logic for a Disk File TSU.

2-4-2-6 Enable Drum Bit Counter The End-Of-Record (EORPØ-EORP3) pulses produced by the four P-CLK decoders (Sheets 22 and 23 Dwg 700903) are gated with the selected Unit to produce a Selected-End-Of-Record-Pulse (SERP). This pulse is trapped in a flip flop (Sheet 21 Dwg 700903) to produce EOR in synchronization with the Control Clock (CC). EOR resets two flip flops, which trap the SSTRQ (P-CLK) pulse, and synchronize it with the following CC clock. The outputs of these flip flops, representing SSTRQ, synchronized with CC, enable a four-stage counter to operate from the Drum-Bit-Clock (DBC). It should be noted that the DBC clock is in synchronization with the CC clock.

2-4-2-7 Drum Bit Counter Decodes The output of this four-stage counter given ~~XXXXXXXXX~~ continuity symbols (1 through 8) on Sheet 22 Dwg 700903, is decoded to produce data request initiation pulses and levels, and other significant sector format signals discussed in the immediately following paragraphs. See Figure 2-4 and Sheet 22 Dwg 700903 for the continuing discussion.

(a) Request Initiation Signals ~~See Figure 2-4 and Sheet 22 Dwg 700903 for the continuing discussion.~~ The decodes of 6 ~~and~~ or 7 from the DBC four-stage counter produces the Low-Priority Prefetch Generator initiation pulse (SSTL) for the starting odd ~~and~~ or even ~~XXXXXXXXXXXXXXXXXXXXXXXXXX~~ half of the Central Memory Address (CMA) double word, respectively. The decodes of 10 ~~and~~ or 11 produces the Warning Prefetch initiation pulse (SSTW) for the starting odd or even half of the Central Memory Address (CMA) double word, respectively.

with Write Mode (WMOD) raised by a gating of WR and EQUAL

NOTE

Prefetches by the Low Priority Request Generator and the Warning Request Generator are made only to ~~even~~ she ~~XXXXXXXXX~~ half of double word addresses within Central Memory. Therefore if the command starting address loaded into the CMA from the AMCP is the odd half of a double word, the preceding even half of the double-word is actually requested by the Low Priority and Warning Prefetch Request Generators. When the starting Central Memory Address is the odd half of a double word, the Low Priority ~~XXXXX~~

and Warning Prefetch Generators are initiated one DBC clock earlier than if the CMA begins with and even half word. (See Figure 2-4).

A decode of 12 by the four-stage DBC counter produces an initiation pulse SSTH for the High Priority Request Generator. The High Priority Request Generator fetches both odd and even address double words. The mnemonic OHW gated with the counter output signifies that the starting Central Memory Address is the odd half word and OHW* signifies that the starting Central Memory Address is the even half word. The OHW and OHW* signals are set and reset outputs, respectively, of a latching flip flop which is reset by the End-Of-Record (EOR) pulse of the selected Drum Unit and is set when the LSB of the Central Memory Address (CMA18) stored in the CMA Functional Control Register is a logic "1" indicating odd half of double word. When CMA18 is at a logic "0" for starting Central Memory Address, the latching flip flop remains reset, indicating even half word. The up-edge of the SSTL and SSTW pulses and the down-edge of the SSTH pulse set dedicated flip flops producing the STLRQ STWRQ, and STHRQ levels, respectively. These levels remain until the last word of a Disk Write-Transfer has been fetched as signified by the mnemonic WDCTØ in the gate controlling the reset of these flip flops.

(b) Sector Format Signals Decodes from the four-stage DBC counter are also used to generate a format window for a preamble and signal for initiating and enabling a Class and Data Field counter.

1 Preamble Time (PRETM) A decode of seven (7) from the four-stage Drum-Bit counter, given mnemonic Beginning-Of-Record (BOR) enables a flip flop which sets on the down-edge of the Drum-Bit-Clock (DBC) stepping the counter to a decode of eight (8). This causes a level referred to as Preamble Time (PRETM) to be raised. A counter decode of fifteen (15) enables reset of the same flip flop and the down-edge of the DBC stepping the counter to count sixteen (16) lowers PRETM. PRETM is a level raised for eight DBC periods during which a preamble is written onto the Drum surface. The lowering of the BOR decode which coincides with the raising of the PRETM level also generates a clock for a flip flop, which sets to produce a Write Enable (WEN) level, which enables the write amplifiers serving the selected write heads of the selected Drum Unit to switch on at the beginning of PRETM. The only qualification for raising WEN with the BOR clock is that a Write Mode (WMOD) be in effect. WMOD is produced by gating the Equal (EQ) signal with the Write (WR) command (Sheet 22 Dwg 700903). A decode signifying the last(eighth) bit during PRETM, produces the (PREDATA) pulse. PRETM and PREDATA combine with WEN at a gate controlling the data buss to

the Drum Unit (Sheets 24, 25, and 26 Dwg 700903). With WEN and PRETM raised and PREDATA lowered, seven DBC clock periods of logic zero NRZ data is released over the 24 Drum Data Buss (TUDDØØ-TUDD23) lines. These 24 data lines of the Drum Buss serve all four Drum Units of each Drum TSU. However, the data is gated into the selected Drum Unit only. This is accomplished by gating the WEN signal with a dedicated Unit select line produced from the Unit Select Decode of the output of the Unit Functional Control Register. The Unit Select (US) and WEN gating takes place in the R/W/S electronics of each Drum Unit. The eight 24-bit words during PRETM are written preceding the Class and Data fields of each Drum Sector to ~~XXXXX~~ produce a ~~known~~ Known data configuration for synchronizing read strobe circuits within the Drum Read/Write/Select (R/W/S), when data is to be played back. The eight PRETM data words are not returned to the Drum TSU. However, the logic "1" word represented by the PREDATA decode, enables the words following PRETM to be returned to the TSU during a playback or read operation.

2 Class Time (CLTM) The DBC producing the last bit of the preamble referred to as (PREDATA), also enables a flip flop. The down-edge of the next DBC marking the end of preamble sets the flip flop producing a Class and Data Field (CADF) level.

(c) Class and Data Field Counter The Class and Data Field Counter (CADF) is pulsed first by the raising of CADF and then by the DBC clock when WMOD is operating(Sheet 22 Dwg 700903).

The output of this counter is decoded to produce windows for the Class and Data Fields and for a Check Field and Postamble Field following the Data Field.

1 Class Field The raising of the CADF level, gated with WMOD is used as the first clock for the CADF counter (Sheet 22 Dwg 700903). This clock sets the first stage of the counter, raising the Enable-Class-Ø (ENCLØ signal, used to gate data out of the Class Ø Functional Control Register. It also raises the Class-Time (CLTM) window. The DBC clock continues to operate the CADF counter with WMOD raised and the DBC clock following the CADF clock pulse lowers ENCLØ and raises the ENCL1 signal used to gate data out of the Class 1 Functional Control Register. CLTM and ENCL1 lower with the next DBC clock. This is caused by the setting of the third stage of the CADF counter. During CLTM the two Class words are gated through the data buffer gates on Sheets 24,25, and 26 as previously discussed in paragraphs 2-4-2-2(g) 3 (Class Ø Drum) and 2-4-2-2 (h) 1 (Class 1 Drum). During CLTM, two DBC periods of NRZ data are released onto the Drum Data Buss to be written as the Class Field on the surface of the selected Drum Unit.

2 Data Field The setting of the third stage of the CADF counter also raises the Data-Field-Time (DTM) signal and releases a reset on the succeeding ten stages of the CADF counter dedicated to counting out the Data Field. Since the LSB stage of these ten stages cannot increment

with the same DBC releasing the reset condition, the ten stages remain reset for one DBC period. This period represents the first word time in a 512 word data field. At the end of 512 DBC clock periods, stage ten of the Data Field portion of the CADF counter sets and the DTM level is lowered.

3 Check Field Time (CHKTM) and Postamble Time (POSTAM)

The setting of stage ten in the Data Field portion of the CADF counter also raises the CHKTM level and enables the setting of a flip flop, which can set on the next DBC. When DBC sets this flip flop, CHKTM is lowered and a Postamble (POSTAM) level is raised. The POSTAM level remains raised until the Selected-End-Of-Record-Pulse (SERP) arrives and resets this flip flop and the entire CADF counter as well, under mnemonic (EOR). For a detailed discussion of the Check Field function refer to paragraph 2-4-2-10.

2-4-2-8 Data Drum Buffers The Drum (TSU) has six stages of data buffering. Eight bits of each of th six buffers are located on one of the three Data Buffer boards at locations 3A1 J24, J25, and J26. During a Write Class and Data Field operation, the Low Priority and Warning Request Generators operate to bring data words out of Core Memory into the Fast Memory, enabling the High Priority Fetch Generator to acquire the word it seeks with less chance of failure. The Fetch requests attempt to keep the six data buffers filled. Six flip flops (FLOPØ-FLOP5) two located on each of the three data buffer boards, are dedicated to indicating the empty or full status of the six data buffers. Refer to figure 2-5 during the continuing discussion.

(a) Load Buffers When a word requested from Central Memory is placed on the Input Data Buss to the AMTU (INBUSØØ-INBUS23) a signal indicating that the request has been honored, is raised on a separate control line to the AMTU.This signal is given mnemonic HAK. HAK is gated with WMOD and the Master-Clock -20 (MC20) to produce CLK1 for pulsing a data buffer-load-pointer. The data buffer-load-pointer is a three-stage counter duplicated in its entirety on all three data buffer boards. The three counters produce a six-count cycle in synchronization. Two different count decodes for the cycle are implemented on each of the three data buffer boards. The first two count decodes INRØ and INR1 are load pulses for the first two data buffers and are located on data buffer board No. 1 (Sheet 24 Dwg 700903) . The next two counter decodes INR2 and INR3 are on data buffer board No. 2 (Sheet 25 Dwg 700903). The last two decodes INR4 and INR5 are located on data buffer board No. 3 (Sheet 25 Dwg 700903). In addition to loading the data on the In-Buss from Central Memory into the six buffers in a sequence, the INRØ through INR5 decodes set in succession the six data buffer status flip flops (FLOPØ-FLOP5). The six data buffers are designated as buffers A through F. INRØ loads buffer A, INR1 loads buffer B, etc., etc.

(b) Empty Buffers During a Write operation, each Drum-Bit-Clock (DBC) empties a word in one of the six data buffers (OUTBUSØØ-OUTBUS23) into the Drum Buss gates. Implementation

is by means of an empty data buffer-pointer, which is a three stage counter identical to the load buffer pointer. The clock operating this pointer is CLK2 produced by gating WMOD, DTM and DBC. The six empty buffer pointer decodes (OUTRØ-OUTR5) gate the output of the six data buffers into the Drum Buss gates. The RESØ through RES5 decodes from the empty buffer pointer, reset the data buffer status flip flops in a sequence. In summary, each word placed on the Buss into the AMTU from Central Memory, loads a data buffer and sets its associated data buffer status flip flop , and each DBC during the data field gates out the data in each buffer, sequentially, and resets the corresponding data buffer status flip flop.

Insert A →

(c) Data Buffer Status The outputs of the data buffer status flip flops are gated in various combinations to determine, if one buffer is empty (ONE E), two are empty (TWO E), or if none are empty (EXØE). The EXØE determination lowers the FETCH level, thereby disabling the Fetch Generator. The ONE E determination enables the Fetch Generator and produces a Low Port Priority modifier (LPP), which is part of the Central Memory request. LPP is used to establish the access priority of the Drum Unit to the Fast Memory Module addressed in the Memory Request. The TWO E determination raises the Drum access priority to the port of the Memory Module being accessed to High Port Priority (HPP). The logic for Drum data buffer status during a Write operation is located on the extreme left

Sheet 24 Dwg 700903

Insert A preceding page

NOTE

CLK 3 shown in the logic is produced by a gating of WEN and DTM, which is actually a logic level rather than a clock. The clock mnemonic applies to the generation of CLK 3 in a Read operation.

checking

2-1-2-9 Data Parity Central Memory advises the AMTU of the parity of each word it sends to the AMTU. The Drum TSU checks the parity of each word received and compares its findings with parity as advised by Central Memory. This parity cross-check is a monitoring of transmission between Central Memory and the AMTU. Words written on the drum do not have an associated parity bit written with them (See Figure 2-6 for the continuing discussion).

(a) Data Word Parity Bit Each 24-bit data word is accompanied by a parity bit from Central Memory, which enters data buffer board No. 2 under mnemonic TUP1 (Sheet 25 Dwg 700903). When the parity bit is set it produces LPAR and when even, it produces LPAR* through a latching flip flop. This latching flip flop is reset with each Master Clock Delayed pulse (MCDL). However LPAR is only looked at after MC20 (approximately 20 nano-seconds after MCDL).

(b) Parity Determination Within the AMTU. Each data word loaded into the data buffer is also presented to a parity tree (Sheets 24, 25, and 26 Dwg 700903). The output of the parity tree is gated with the Central Memory Parity bit (LPAR) which causes PIND to be raised if the parity from Central Memory does not agree with the output of the parity tree. PIND is gated with CMP which is a timing window extending from MC20 till the next MCDL pulse (Sheet 26 Dwg 700903). When MC70 (70 nano-seconds after MCDL) arrives a Memory Parity Error (MPE) status flip flop is set if PIND has been raised (Sheet 24 Dwg 700903). The TØ MPE output of this indicator flip flop

is a status condition made available to the AMCP at the end of the record in which it is detected as discussed in paragraph [redacted] 2-6-6.

2-4-2-10 Check Field Write Each 24-bit word exits the outbuss gates shown on the extreme right of Sheets 24,25, and26 Dwg 770903, under mnemonic (TØDØØ-TØD23). From the buffer boards, data is routed to the cable board at location 3A2J19 (Sheet 52 Dwg 700903). On [redacted] the cable board each bit of the data word is amplified in an emitter-follower and is gated into the R/W/S of the selected Drum Unit, under mnemonic (TØDIØØ-TØDI23). Data (TØDIØØ-TØDI23) out of the emitter followers on the cable-board at [redacted] 3A2 J19 (Sheet 52 Dwg 700903), is also returned to the data-buffer boards (Sheets 24,25, and 26 Dwg 700903), where each bit conditions one stage of a 24-bit Check Field Register to set or reset with the Drum-Bit-Clock (DBC). The output of each stage of the Check Field Register is summed in an Exclusive Or Gate with a data bit from the next word. The half-adder summation resulting from this gating is handled two different ways, depending upon bit 19 in the Functional Instruction Control Register. This bit is normally reset producing the Rotation [redacted] (ROT) level (Sheet 29 Dwg [redacted] 700903). When this bit, referred to as the Disable-Check-Code-Cycle bit is set, ROT is reset.

(a) Check Code Cycle When ROT is raised the output of the Exclusive OR-gate is used to condition setting or resetting of the next LSB stage of the Check Field Register except for the exclusive OR-gate following stage 23, which conditions stage ØØ, the MSB stage. The [redacted] DBC pulse then loads the [redacted]

half-adder summation into the next stage of the Check-Field Register, and the output of this stage is exclusively OR-gated with a different bit of the next data word. This causes the half-adder summation of each successive word to be ratated one bit for each word. At the end of the data field the Check Field Register contains a 24-bit word representative of the preceding data field. The Check Field Time (CHKTM) window operates during the DBC period following the data field as previously discussed in paragraph 2-4-2-7 (c) 3. CHKTM gated with WEN causes the output of the Check Field Register (CØØ/-C23) to be gated from the data buffer cards through the cable-card at 3A1 J19, into the RWS to be written in the word space immediately following the data field on the Drum surface.

(b) Check Code Cycle Disable When ROT is reset (ROT*) the output of each stage is gated with a data bit of the next word. When the output and the new bit are of the same logic state , the stage enables itself to reset on the next DBC. If the output and the new bit are of different logic states the stage enables itself to set on the next DBC.

Insert B
(Place before 2-4-2-12)

NOTE

The following discussion beginning with paragraph 2-4-2-12 and continuing through and including paragraph 2-4-2-20 is based on figure 2-7.

NOTE

This concludes the discussion of Drum record formatting during a Write Data and Class operation. The continuing discussion is concerned with record formatting for a Disk File during a Write Data and Class operation.

2-4-2-10 Disk Format Times Decode The Disk Format times ~~decodes~~ XXX designated in octal on the logics of Dwg 700903, are produced by decodes from a Format Control counter which counts the prerecorded bit clock pulses of the selected Disk Unit. (See Disk Control board at location 3A1 J01 ~~A XXXXXXXXXX~~ sheet 2 Dwg 700903.)

A format time period is equivalent to two Disk words. A Disk word is equivalent to ~~XX~~ two 25-bit data words. A Write Data and Class ~~instruction~~ operation for a Disk involves the execution of the following subfunctions.

Write Data and Class Subfunction Breakdown

(a) Reading back a prerecorded header field from the Disk and comparing it with the ~~XXXXX~~ Disk File ~~starting~~ actual address effected from the ~~command~~ instruction, contained in the command instructions.

(b) Achieving Track Verification if the instruction was ~~not~~ qualified as Disk Pol...

(c) ~~Address~~ Finding starting address of instruction.

(d) Writing a Class Field including a Preamble.

(e) Writing a Data Field.

(f) Writing a Check Field.

User B

2-4-2-11 Format Time (FT05) At FT05 a Subfield counter is reset producing a subfield decode of SF0 and a Data Word Counter is reset producing a decode of DW0. In addition, an indicator flip flop is set producing E which ~~enables~~ signifies the E serial Register has been connected for a serial transfer and an AWD/BWD flip flop is reset producing AWD. (See ~~an E-Register Full (EFUL) indicator flip flop is set~~ 50-bit capacity

sheet 13 Dwg 7C0903) and a C Register Empty/Full status indicator (CFUL) flip flop is reset (Sheet 14 Dwg 700903).

2-4-2-13 Format Time (FTØ6) At FTØ6 XX the starting Disk address stored in the XXXXXXXXXXX Device Address Control register, the Position Register and the Position Counter for the selected unit is loaded XXXXXXX onto the CBUS by means of two successive load pulses HACBUS and XX HBCBUS. A load pulse (LDC) then strobes the C BUS in parallel into the 24-bit C Register (See Sheets 10 and 11 Dwg 700903 for C-Register). A HACBUS is produced by gating FTØ6, WHD*, and AWD (See Sheet 14 Dwg 700903) WHD* is a level out of the Instruction Register indicating that as part of the Write Data and Class instruction for a Disk, the prerecorded header is to be read for comparison with the starting address rather than being written on the disk surface, as would be the case in a specific Write Header instruction. The AWD signal ~~is~~ signifying the first 25 bits of the 30-bit starting address word is produced by the reset state of the AWD/BWD flip flop produced by FTØ5 as previously mentioned. The LDC pulse is produced by a gating of ENLDC, DFLD*, and CFUL* (See sheet 14 Dwg 700903) XXX ENLDC is essentially XXX the FTØ6 time period. DFLD* indicates that the data field of the sector has not been reached and CFUL* is the reset state of a flip flop indicator which XXXXXXXXXX XXXXXXXXXXXXX is set by the LDC pulse as XXX the C-Register is loaded by the LDC pulse. The first LDC pulse XXXXX loads the

(a) AWD portion of the starting address XXXX gated on the CBUS by HACBUS, into the C-Register. As soon as the C-Register is loaded the CFUL indicator flip flop is set producing CFUL (See Sheet 14 Dwg 700903.) CFUL and the ~~SFØ~~ Gating of CFUL WHD* at SFØ produces a transfer condition (T2XFR) which enables the contents

of the C-Register to be shifted serially into an E-Register.

~~The complete gating for the production of T2XFR is CFUL, SFØ, and WRM~~ (See Sheet 13 Dwg 700903).

~~2-4-2-13~~ E-Register Format The E-Register consists of six sections. Each section holds a fraction of a 50-bit Disk word, and each section is associated with one of the six data read/write elements (heads) operating simultaneously on the Disk surface. It should be recalled, that on the Disk, data is recorded in six bit parallel. Since the six heads are located at varying radial distances from the center of the disk, the circumference of the tracks to which each is dedicated also varies accordingly. It is immediately apparent that those heads located close to the center of the Disk can sevice fewer bits of a 50-bit word than those located on the outer perimeter of the Disk. Therefore, The bit allocation for each of the six heads ~~is as follows.~~ Beginning with the outer perimeter head is 12, 12, 10, 8, 5, and 3. The E-Register is designed to hold this ratios of bits for each 50-bit word. A different clock rate is also required to operate each section of the E-Register. The six clocks are produced by six different decodes from a counter (T2WCØ - T2WC5 or T2CLKØ - T2CLK5) (See Sheet 2 Dwg 700903 Dwg 700903). When writing on the disk the clocks operating are T2WCØ - T2CLK5, produced by the output of an oscillator slaved to Disk rotational speed since it is driven by

prerecorded clock pulses from the selected unit. The output of the oscillator is the input frequency multiplied by sixteen. When recovering data from the Disk surface, the clocks operating are T2CLKØ - T2CLK5 produced by pulses generated from transitions of the recovered data previously written (T2RCØ - T2RC5). A D-Register formatted identically to the E-Register also is required for Disk File operation.

2 C-Register Format The C-Register is a 24-bit Register loaded in parallel by the LDC pulse for write operation. Its contents are shifted out into the E-Register (or D-Register) during a write operation. The C-Register is divided into a left half and a right half. When data is shifted out of the C-Register it is shifted out of the MSB of each 12-bit half of the C-Register. For the right half the twelve bits exit stage C12 and for the left half twelve bits exit stage CØØ.

(b) Transfer Process Starting Address (AWD) When T2XFR is raised the 24-bit AWD word in the C-Register is gated into the E-Register in the following manner: (Refer to Figure 2-5)
Data from the right half of the C-Register (C12) enters a 12-bit section of the E-Register designated SR5XX and data from the left half of the C-Register (CØØ) enters a 12-bit section of the E-Register designated SR4. SR5 is shown on Sheet 10 Dwg 700903 and SR4 is shown on Sheet 11 Dwg 700903. Data is shifted from the C-Register to E-Register at the Control Clock (CC) frequency which is faster than the frequency at which data is shifted out of the E-Register to be written on the disk surface. The transfer of the AWD

portion of the AWD starting address word into the E-Register requires gating for the ~~XX~~ 24 bits and special gating for including parity as determined by logic within the Disk TSU. ~~For~~ In this discussion we will first concern ourselves with the right half of the starting address AWD. However, ~~XXXXXXXX~~ similar gating is required for the left half of the AWD. Data under mnemonic C12 is gated with (CHFLD*) and a level representing the 12 clock times required to shift the 24-bit AWD into the right and left halves of the E-Register. C12 is identified by continuity symbol B1, CHFLD* by continuity symbol A11, and the 12-bit time period by continuity symbol H6 ~~XXXXXXXXXXXXXXXXXXXXXXXXXXXX~~ The gate is all located at the extreme left hand lower half of Sheet 10 Dwg 700903. This gating produces 12 data bits of the logic state of C12 for the ~~XXXXXX~~ 12 CC pulses during T2XFR time. The output of this gating ~~XXXXX~~ forms one leg of an OR-gate which connects data to the SR5 of the E-Register under mnemonic T2SRIR. The left half of the C-Register output (CØØY is presented to a similar gate producing data to ~~XXXXXXXXXXXXXXXX~~ for SR4 of the E-Register ~~XX~~ under mnemonic ~~T2XXXXX~~ T2SRIL (See Sheet 11 Dwg 700903). ~~XXXXXXXXXXXXXXXX~~

(c) Disk Parity Generation T2SRIR and ~~XXXXXXXXXXXX~~ T2SRIL are gated to determine the final state of a ~~data~~ Disk parity generation flip flop. When corresponding bits of each half of the AWD differ in logic state the ~~Data~~ Disk Parity Generation (DPG) flip flop complements. Since the DPG flip flop is reset before T2XFR an odd number of differences between corresponding bits in of

each half of the AWD would cause the DPG flip flop to be set at the end of the 12 CC clock pulses. This would cause the DPG signal to be low and the parity bit associated with the AWD would be at logic "Ø". The thirteenth CC in the AWD is dedicated to the parity bit. On Sheet 13 Dwg 700903 a counter driven by CC produces a pulse representing parity time (T2P) with the thirteenth CC pulse operating in Format Time FTØ6. This is the same counter that indicates AWD and BWD as a function of CC pulse count. This T2P pulse is gated with the data parity bit DPG at another gate feeding the OR-gate producing T2SRIL and T2SRIR. The state of the bit on these lines at TP2 time depends on the logic state of DPG. The parity bit for the AWD is placed in the E-Register in the bit position following data bit 12 from the left half of the C-Register. At the end of the AWD the parity bit would be located in bit position 11 of SR4 (See figure 2-5).

(d) Transfer Enable Window When T2XFR is raised it also raises an enable window which permits data under mnemonics T2SRIR and T2SRIL to actually be shifted into the E-Register. This window varies for controlling the position of the parity bit in the E-Register for the AWD and the BWD. To be specific, during the AWD the Transfer Window identified by continuity symbol A16 on both sheets 10 and 11 of Dwg 700903, is raised for for 13-bits so, the

each capable of addressing Central Memory independently. Two of the three generators are Prefetch Generators, which operate to bring a double word out of the core portion of Central Memory into Registers within the Fast Memory portion of Central Memory. Once the word is in Fast Memory, the third Drum Request Generator referred to as the Fetch Generator follows up with a Fetch Request, which puts the prefetched word residing in Fast Memory, onto the data buss into the AMTU. Should the prefetch Generators fail to bring a double word into the Fast Memory the Fetch Generator is capable of bringing the double word into Fast Memory and placing it on the output buss independently. Since these three generators are addressing a different location in Central Memory at any given moment, each Generator must be capable of addressing Central Memory independently of the other two. In order to implement the independent addressing a second Central Memory Address Register is used. The output of the Functional CMA Register is dedicated to low priority Prefetch Requests and the second Address Register referred to as the B-Register is dedicated to High Priority Fetch Requests. The B-Register is initially loaded with the output of the functional CMA Register and its LSB stages are incremented independently. When address incrementation of the B-Register extends beyond the LSB stages, the output of the MSB stages of the Functional CMA Register which will have been previously incremented) is loaded into the MSB stages of the

B-Register and the independent LSB stages of the B-Register are reset. The Warning Prefetch Generator has only an independent set of the LSB stages of the Central Memory Address. These stages are initially loaded with the output of the LSB stages of the Functional CMA Register and initially the MSB stages for CMA addressing is provided by the output of the MSB stages of the B-Register. When address incrementation of the Warning Prefetch Generator extends beyond the LSB stages, the MSB stages from the Functional CMA Register are used. When the High Priority Fetch Generator increments beyond its LSB stages as previously discussed the Warning Prefetch Generator switches back to the MSB stages of the B-Register,, again. Drum Request logic is to be discussed in detail in paragraph 2-5-1. The preceding discussion only serves to indicate the reason for a second address register and the duplication of the LSB stages of the CMA Registers. The B-Register and the LSB stages of CMA within the Warning Generator are initially loaded with the output of the Functional CMA Control Register by a pulse developed from Swap Count 7 of the Instruction Swap Cycle.

(f) Swap Count 6 This decoded output of the Swap Counter is not used in Write Data and Class Code operations, initial Swap Cycle.

(g) Swap Count 7 This decode of the Swap Counter produces a pulse for loading the output of the Central Memory Address Register. Its mnemonic is LDRQAD and it specific function varies between Disk and Drum TSU's. Swap Count 7 is also gated with SWP and with RFUL which signifies the Swap Cycle is an instruction cycle and with the Disk Policy modifier bit (DMPOL*) to produce the transfer Track Address pulse XTA for Disk File TSU's only. Swap Count 7 is also gated with CONF* to generate a Swap Class Register Ø (SWPCLØ) pulse.

1 LDRQAD (Drum) This pulse strobes the output of the four LSB stages of the CMA Register into the B-Register and the duplicate LSB stages of the Warning Prefetch Generator. The LSB stages of the B-Register used with the high priority (Fetch) Generator are loaded initially by LDRAQ (Sheet 23 Dwg 700903). The MSB portion of the B-Register is loaded initially by LDRQAD under mnemonic LDB which is produced by an Or-gating of LDRQAD and an incrementation pulse representing the setting of the LSB stages of the B-Register . (Sheet 21 Dwg 700903). The LSB stages of the Warning Prefetch Generator are also loaded initially by the LDRQAD pulse (Sheet 21 Dwg 700903).

2 LDRQAD Disk The Disk File TSU does not use independently operating Request Generators. It issues either Prefetch requests or Fetch requests at different priority levels, but is not capable of generating requests at different levels, simultaneously, as is possible in the Drum TSU. The LDRQAD pulse, generated by Swap Count 7, is used in the Disk File TSU, to load the output of the Functional CMA Control Register into a ~~temporary Holding~~ Buffer Register. The LDRQAD pulse is actually Or-gated with the incrementation pulse (RT4), to be discussed later, to produce the load pulse (LDBH) (sheet 2 pwg 700903). ~~At the end of the~~ At the end of the record following a transfer, the output of the ~~temporary Holding~~ Buffer Register is loaded into the CMA Holding Register with the Swap CMA (SWCMA) pulse. There is no direct load from the Functional CMA Register into the CMA Holding Register.

2 XTA This pulse is generated in Disk File TSU's but only when a Disk Policy instruction (DMPOL*) is in effect. A detailed discussion of the function performed by the XTA pulse is contained in paragraphs 2-4-1-3(g)1,2, and 3. A Drum Policy modifier would require that the Disk File effect Starting Address in the Sector following the Swap Cycle. This would not be possible if a Track Positioning operation were required. Therefore the XTA pulse is only generated with Disk Policy (DMPOL*) operation. Disk Policy waits for positioning to take place before addressing is complete.

3 SWPCLØ Swap Count 7 is gated with the reset output of the Continue flip flop (CONF*), to produce the Swap Class Ø (SWCLØ) pulse. This pulse swaps the Functional and Holding

(d) Writing of Check Field Generation by Data Field

All data shifted out of the C Register into the D or E Registers during the Data Field is also presented to a half-adder circuit to be half-added with the output of a Check Field Register. The logic for this function is on the extreme upper left of Sheets 10 and 11 Dwg 700903. A signal, T2ENCH identified by continuity symbol H4 enables the operation of the Check Field Register during the Data Field and for thereafter additional Disk Words referred to as the Check Field. T2CØØ identified by continuity symbol B1 on Sheet 10 Dwg 700903 which is data out of the left half of the C Register, is gated with READ to become one input to the half-adder. CHOL the output of the half word Check Field Register, identified by continuity symbol A5 on Sheet 10 Dwg 700903, is the other input to the half-adder. The T2XFR level raised for transfer between the C Register and the D or E Registers, except for parity time, identified by continuity symbol H6, is gated with CC, identified by continuity symbol A9. This gating produces shift pulses for the left half Disk Word Check Field Register which clocks in the half-adder results for each bit addition of the left half Disk Word of the Data Field. Sheet 11 Dwg 700903 contains similar logic for the right half of each Disk Word transferred from the C Register. Mnemonics T2C12 and CHOR operate for the right half Disk Word. Each bit of the Data Field is half-added with the results bit summations existing from the Check Field Register of previous half-adder Registers. When an entire Disk Word has been shifted into the Check Field Register from the C Register through the half-adder the

EOWD pulse operates. EOWD is gated with the Rotation (ROT) signal, which is high when bit 19 (Disable Check Code Cycle) in the Instruction Control Register is reset and with CC identified by continuity symbol A9. This gating provides a pulse for shifting the Check Field Register one more bit position before the next Disk Word. At time of rotation , the output of the right half word Check Field Register is connected to the input of the left half-word Check-Field Register and the output of the left half-word Check-Field Register is connected to the input of the right half-word Check-Field Register. Rotation, therefore, shifts the entire 50-bit Check Field Register one bit position for each Disk Word processed through the half-adder.

2-4-2-1 Check Field Each time the BWD of each Disk Word is transferred from the C Register into the D or E Register the EOWD signal is generated. Using the three stages of the Sub Field Data Word Counter (connected by raising DFLO) and an additional five counter stages, a count of 256 is decoded, which marks the end of Data Field and the beginning of Check Field. The pulse is given mnemonic CCHFLD* (Sheet 13, right side, Dwg 700903). CCHFLD* latches a flip flop to the set position, producing DWOVF, which is gated with WEN and the reset output of one stage of the Data Word Counter. As the counter resets from the all stages set decode of DW255 to DWØØ, the reset output from the counter stage pulses a gate, which jam sets a flip flop producing T2CHFLD (Sheet 13, upper right Dwg 700903). When T2CHFLD is raised, the LDC pulse is generated

by a gating of CFUL*, T2WEN, and T2CHFLD. LDC forces CFUL high, thereby raising T2XFR (Sheet 14, lower right XX Dwg 700903). T2XFR except for parity bit time, as identified by continuity symbol H6 on sheets 10 and 11, left side Dwg 700903, is gated with the output of the Check Field Register (CHOR and CHOL) identified by continuity symbol A5 during the Check Field (T2CHFLD) identified by continuity symbol A12. This gating produces a serial input representing the half adder summation rotated for the Data Field, operating under mnemonics T2SRIR and T2SRIL, identified by continuity symbol A15 on sheets 10 and 11 Dwg 700903. The single Disk Word is processed through the Parity Generation Circuit and is shift loaded into the D Serial Register to be written immediately following the Data Field.

2-4-2-20 Postamble With T2CHFLD still raised, the LDC pulse is generated twice more after the Check Field has been loaded into the D Register as an AWD and BWD. These pulses cause CFUL to raise producing T2XFR for first an AWD to the E Register then again for a BWD to the E Register. This 50-bit Disk Word loaded into the E Register , is the output of the Check Field Register, which still contains the Check Field advanced one bit position. The EOWD occurring as the E Register is loaded is gated with DW1, representing the Postamble Data Word time, with CHFLD and WEN to produce R3WEN* which enables the WEN flip flop to reset with the CC pulse. This also produces a Sub Field incrementation pulse (INCRSF) which causes the Sub Field counter to go from SF3 to SF0. Even though WEN has lowered, WENDL is still latched

in the set position and enables the writing of the Postamble onto the Disk Surface. When the last bit of the Postamble is shifted out of the E Register, the EFUL indicator flip flop resets (Sheet 13 Dwg 700903). DFUL and EFUL are now reset, and SF3 and WEN are also down. A gating of these conditions produces a reset for the WENDL latching flip flop and WENDL lowers, disabling the write amplifiets from further writing (Sheet 13 Dwg 700903).

NOTE

Paragraphs 2-4-2-21 and 2-4-2-22, following, discuss Drums and Disks together, rather than independently, since the function discussed in these paragraphs is essentially the same for Drums and Disks.

2-4-2-21 Generate End of Write Data and Class Operation Swap Count Cycle

When no new instruction is received during a record, the Swap-Cycle, which comes at the end of the record will be the last Swap-Cycle of the operation. This is true because the Swap-Complete-New-Instruction (SCNI) flip flop set output identified by continuity symbol X16 (Sheet 28 , Drum, Sheet 8, Disk, Dwg 700903) is inhibited from rising by the fact that RFUL, identified by continuity symbol A18 remains low because of no new instruction having been received and no EQ-Strobe (EQSTRB) pulse is produced. The final Swap-Cycle during a Write Data and Class

described. The SWPRQ flip flop is set in this case by the gating of DMPOL* and RCE in the case of a Disk policy type of operation on a Drum Unit and the same gating plus the Track Verification (TV) signal for a Disk Policy type operation on a Disk Unit. In the case of a Drum-Policy type operation, the DMPOL signal is all that is required to produce SWPRQ (Sheet 28,Drum, Sheet 8, Disk, Dwg 700903).

2-4-2-22 End of Operation(Write Class and Data)Swap-Count-Cycle

The continuing discussion is based on the assumption that no new instruction from the AMCP was received while the Write Data and Class operation was being executed. Logic discussed is to be found on Sheets 8, Disk, and 28, Drum, Dwg 700903.

(a) Swap Count 1 The SWDA pulse is produced again causing the Functional Device Address Control Register to swap its contents with the Holding Device Address Control Register. Since the output of the Holding Registers are gated onto the input buss to the AMCP, the Device Address of the just completed operation is available to the AMCP, and can be monitored by the AMCP's generation of an ACTC selecting the Device Address Register followed by the AMCP's generation of anRDPC, which enables it to sample the output of the Device Address Register now on the input buss to the AMCP. The Swap-Count 1 decode also produces the Load-Status--Register (LDST) pulse, which strobes the output of all status error indicators into a Status Register. (Status is discussed

(b) Swap Count 2 This decode is used to produce the Clear-Error-Indicator (CLERR) pulse, which resets all status error indicators. (Status is discussed in detail in paragraph 2 .)

(c) Swap Count 3 This count produces the Swap Map (SWMAP) and Swap-Unit (SWUNI) pulses, which load the Functional Map and Unit Register contents into the Map and Unit Holding Registers. The output of the Map and Unit Holding Registers can then be sampled by the AMCP.

(d) Swap Count 4 This count produces the Swap-Word-Counter (SWWC) pulse, which swaps the Word Counter/Register count into the Holding Register , making the word count of the operation just completed available to the AMCP.

(e) Swap Count 5 This count produces the Swap-Central-Memory (SWCMA) pulse through which, the swap function makes the Central Memory Address sequential to the last address of the just completed transfer operation available to the AMCP upon request.

(f) Swap Count 7 This count produces the Swap-Class-Ø (SWCLØ) pulse, which through the Swap function, makes the Class Ø word of the Class-Subfield available to the AMCP upon request.

(g) Swap Count 8 This count produces the Swap-Class-1 (SWCL1) pulse which, through the Swap-function, makes the Class 1 word of the Class-Subfield available to the AMCP upon request. This count also produces the Reset-Busy

(RBSY) pulse, which resets the Busy indicator flip flop. The significance of the resetting of Busy, is in that it enables the generation of the Attention interrupt (ATTN) to the AMCP and also provides Preselection Status information required for the AMCP as discussed in paragraph 2-3-2-7. Swap-Count 8 also produces the Clear-Check (CLRCH) pulse, which clears the Check-Field Register in the Drum TSU and resets the Last-Record-Address and Last-Band-Address XXXXXX (LSTRA and LSTBA) traps for both Drum and Disk TSU's (Sheet 28,Disk,Sheet 8, Drum, Dwg 700903). Finally, Swap-Count 8 produces the Reset-Swap (RSWP) pulse, which enables generation of the End-Of-Swap (EOSWP) pulse and the resetting of the Swap flip flop as CC operates(Sheet XXXXXXXXXXXXXXXXXX 8, Drum, Sheet 28 Disk, upper left, Dwg 700903).

(h) Swap Count 9 This decode generates the Reset-Counter (RTC) signal, which enables reset of the Swap Counter.

NOTE

As stated at the beginning of XXX this major paragraph, the lack of a new instruction inhibits the generation of EQSTRB, by inhibiting the setting of the Swap-Complete New-Instruction (SCNI) flip flop XXXXXXXX identified by continuity symbol X16, XXXXXXX Sheets 8 and 28 ,left side, Dwg 700903).

2-4-3 Read Data and Class The discussion which follows will rely heavily on references to the preceding discussion of Write Data and Class operation. Control sequences are much the same for Read as for Write. However, since data flow is in the opposite direction for Read, different control gates operate to route the data. Since Read amplifiers are required rather than Write amplifiers, Read amplifier switching control differs also. As previously stated, Drum Request logic is discussed in detail, beginning with paragraph 2-5.

2-4-3-1 Read Data and Class Load Sequence For this operation, the following Holding Control Registers are loaded:

INSTRUCTION

DEVICE ADDRESS

CENTRAL MEMORY ADDRESS

MAP (OPTIONAL)

WORD COUNT

CLASS (DISKS ONLY)

UNIT

One Control XX Register is loaded from the AMCP output buss with each pair of ACTC and WTPC commands, as discussed in paragraphs 2-3-3-2 and 2-3-3-3. The Instruction Register is loaded first and the Unit Register last, as discussed indetail in

paragraphs 2-3-3-2(b) and 2-3-3-3(d).

(a) Generate Swap Required and Start Swap Counter For this operation, a Swap-Required (SWPRQ) signal is generated at the end of the Register Loading sequence, as discussed in paragraph 2-4-1-2(a) and the End-Of-Record pulse (EOR for Disk and ERPØ for Drum) initiate a Swap-Counter-cycle, as discussed in paragraphs 2-4-1-2(b,c,and d).

2-4-3-2 Swap Function During Read Data and Class The Swap Counter decodes are the same for this operation as for the Write Data and Class operation, discussed in paragraph 2-4-2-2(a through i), except that the Swap pulses for swapping Class Ø and Class 1 Registers (XX Swap Count 7 and 8) are not produced during the Read Data and Class operation. It should be recalled that no class information has been loaded into the Functional Class Control Registers and a swap of Functional and Holding Class Registers would be meaningless at this time.

2-4-3-3 EQUAL EQUAL is effected in this operation just as in a Write Data and Class operation, as discussed in paragraphs 2-4-2-3, 2-4-2-4, and 2-4-2-5.

NOTE

The continuing discussion is based on the effecting of EQUAL. Read Data and Class for Drum is discussed independently, beginning with paragraph 2,4,3,4, following.

2-4-3-4 Enable Drum Bit Counter and Decodes The End-Of-Record pulses (EORPØ-EORP3) produced by the four P-CLK decoders (Sheets 22 and 23 Dwg 700903) are gated with the Unit_Select signal to produce the SERP pulse, which is used to trap the SSTRQ (P-CLK) as discussed in paragraph 2-4-2-6. SSTRQ synchronized with CC enables the first four stages of the Drum-Bit-Clock Counter to operate.

Drum Bit Counter Decodes The output of this four-stage counter identified by continuity symbols (1 through 8) on Sheet 22 Dwg 700903, is decoded to produce the following significant sector format signals.

(a) Read Enable REN A decode of seven (7) from the four-stage Drum-Bit counter (DBC), given mnemonic Beginning-of-Record (BOR) is gated with the DBC pulse to produce a clock which sets the Read Enable (REN) flip flop raising the REN level. The J-enable for this flip flop is the Read Mode (RMOD) level produced by a gating of READ and EQ (Sheet 22 Dwg 700903).

(b) Load Class Pulses and Class Window When REN is raised , the Preamble written on a previous Write operation is read back and the End-Of-Preamble (EOP) bit opens a gate releasing previously written data and a clock derived from the data. The clock(RC), is gated with REN, to produce a clock for incrementing the Class and Data Field portion of the Drum-Bit-Counter(DBC). The down-edge of the first RC in this gate sets the first stage of this portion of the DBC and the up-edge of the following DBC produces the up-edge of the Load

(e) Check-Field (Read) Data being read back from the Drum enters the Drum TSU from the R/W/S under mnemonic (DDIØØ-DDI23), to be presented to the same Check-Field half-adder circuit as described in paragraph 2-4-2-10. At the end of the Data-Field, the Check-Field-Register should contain the same Check-Field word, which was produced during the XXXXXX Write operation. When each bit of the Check-Field word is read into the half-adder circuit with its associated output bit stored in the Check-Field Register, the result should be a logic zero for every stage of the Check-Field Register (Sheets 24,25,and26, Dwg 700903). The output of this Register after this half-adder operation is strobed into XXXXXXXXa Check-Field Holding Register by the load pulse ( )XXXXXXXXX (Sheet 27 Dwg 700903). This same pulse strobes a gate XX at which a signal referred to as Check-Not-Zero (CHNZ) is present ~~(Sheet 27 Dwg 700903)~~. CHNZ is the result of a collector OR-gating of the output of the Check-Field Register (Sheet 27 Dwg 700903). At the time the ( ) pulse operates the CHNZ signal should be low. If any one or more bits of the Check-Field Register output is high, CHNZ goes high and sets the CHNZ status indicator flip flop (Sheet 28 Dwg 700903). ~~Status is discussed in detail in paragraph 2-~~ The T Ø CHNZ output of this indicator flip flop is a status condition mode available to the ANCP at the end of the record in which it is detected, as discussed in paragraph 2-6-5.

2-4-3-5 Drum Data Buffers In a Read Data and Class operation the Store requests to Central Memory attempt to keep the six data buffers empty. Refer to Figure 2-8 for the Continuing discussion,

(a) Load Buffers When a word is read from the Drum, the associated Read Clock (RC) gated with REN, produces a CLK 1 pulse (Sheet 25 left side Dwg 700903). The CLK 1 pulse increments a three-stage counter ~~XX~~ duplicated on each of the three data buffer boards (Sheets 24-26 Dwg 700903), referenced to as the Input Pointer. The three counters produce a six-count cycle in synchronization. Two different count decodes of the cycle are implemented on each of the three data buffer boards. The decodes, given mnemonics (INRØ-INR5) are load signals for strobing data into the six data buffer boards. In addition to loading the data into the buffers in a sequence, the decodes (INRØ- INR5) also operate six data-buffer ~~XXX~~ Empty/Full status flip flops (FLOPØ-FLOP5). The six data-buffers are designated A through F. INRØ loads A, INR1 loads buffer B, etc. etc.

~~(b)~~ Empty Buffers During a Read operation (RMOD) a Store request produces a High-Request to Central Memory (HCM) pulse, ~~which~~ is gated with RMOD to produce a CLK 3 pulse, according to a sequence controlled by an output Pointer discussed next which strobes data out of the data buffers. The request is acknowledged by the return of a signal from Central Memory with mnemonic HAK. The HAK signal is gated with RMOD to produce ~~XXXXXXXXXXXXXXXXXXXX~~ CLK 2, which increments an output Pointer which resets the data buffer Empty/Full Status indicator flip flops (FLOPØ-FLOP5) ~~XXXXXXXXXXXXXXXXXXXX~~ (Sheets 24-26 Dwg 700903). ~~XXXXXXXXXXXXXXXXXXXX~~ sequence in a given

(c) Data Field The setting of the third stage of the Class and Data Field (CADF) portion of the Drum-Bit-Counter raises the Data-Field-Time (DTM) level and releases a reset on the succeeding ten stages of the CADF portion of the Drum-Bit-Counter. At the end of 512 DBC clock periods, stage ten of the Data Field portion of this counter sets and DTM is lowered.

(d) Check Field Time (CHKTM) and Postamble Time (POSTAM) The setting of stage ten in the DATA Field portion of the Drum-Bit-Counter, raises the CHKTM level and enables the setting of a flip flop. When the next DBC pulse operates, this flip flop sets, lowering CHKTM and raising a Postamble Time (POSTAM) level. The POSTAM level remains raised until the Selected-End-Of-Record-Pulse (SERP) arrives and resets this flip flop and the entire CADF portion of the Drum-Bit-Counter as well.

NOTE

The Data Field, Checkfield, and Postamble Times are produced in a Read Data and Class operation the same way as in a Write Data and Class operation, except the DBC clock is produced by the Read Clock(RC) derived from previously written data when reading, and by a prerecorded clock (DBC) when writing (Sheet 22 Dwg 700903).

Class Ø (LDCLØ) pulse. The down-edge of this same clock then increments the DBC lowering LDCLØ and raising the second stage of the DBC. The up-edge of the next RC then produces the up-edge of the Load Class 1 (LDCL1) pulse. The down-edge of this same clock then increments the DBC lowering LDC1. An Or-gating of these two XXXX pulses produces a Class-Time (CLTM) signal representing a window for the two class words being read back from the Drum at this time. Class Word Ø enters the Drum R/W/S, is read, and placed on the input buss to the Drum TSU to be presented to the Class Ø Functional Control XX Register under mnemonic (DDØØ-DD23). At this time the LDCLØ pulse strobes word Ø into the Class Register. XX Immediately following, Class Word 1 is strobed into Class Word Register 1 by the LDCL1 pulse (Sheets 29 through 33 Dwg 700903).

NOTE

The Class Words thus loaded into the Functional Control Registers are swapped back into the Class Holding Register at the end of the record. This allows for if sampling by the AMCP desired.

(c) Data Buffer Status The outputs of the data buffer Status flip flops are gated in various combinations to determine if one buffer is full (ONE F), two are full (TWO F) or if none are full (EXØ F). The EXØ F determination lowers the Store level, thereby disabling the Store request generator. The ONE F determination enables the Store request generator and produces a Low Port Priority (LPP) modifier for the request. The TWO F determination produces a High Port Priority (HPP) modifier for the Store request. The HPP and LPP modifiers establish the access priority of the Drum Unit to the Central Memory Address word being requested. The logic for Drum data buffer status during a Read operation (RMOD) is located on Sheet 25 left side Dwg 700903.

2-4-3-6 Data Parity Generation Each data word read back from the Drum is checked for parity in the same parity tree used for checking parity during the Write mode. Data is presented to the tree under mnemonic (INBUSØØ- INBUS23). The buffer load pulses (INRØ-INR5) strobe parity determination for right and left halves of each word into flip flops corresponding to the word half and corresponding to the buffer into which the word being checked, is loaded. When CLK 3 operates to load data into Central Memory, it also strobes the parity stored in each of the Parity flip flops, through a gate enabled by the RMOD level. The parity bit for each half word (TUDO24 or TUDO23 which is) is gated in the TUIM (Sheet 19 Dwg 2009013) to produce a single Parity bit returned to Central Memory with its corresponding data word. Refer to Figure 2-9 for timing.

NOTE

This concludes the discussion of Drum record formatting during a Read Data and Class operation. The continuing discussion is concerned with record formatting for a Disk File, during a Read Data and Class operation.

2-4-3-7 Read Data and Class Subfunctions A Read Data and Class operation for a Disk involves the execution of the following subfunctions:

(a) Reading back a prerecorded header field from the Disk and comparing it with the Disk File actual address effected from the Read Data and Class instruction.

(b) Achieving Track Verification (TV) if the instruction was qualified as Disk Policy.

(c) Finding the Starting Address contained in the instruction.

(d) Reading a Class Field from the Disk and comparing it with the Class Field loaded into the Functional Class Register as part of the Read Data and Class instruction.

(e) Reading a Data Field and transferring each word to an address in Central Memory.

(f) Generating a Check Field with the Data Field being read and comparing it with the Check Field generated during the Write operation during which the Data Field was written on the Disk.

NOTE

The following paragraphs make references to the discussions of Write Data and Class. Refer to figure 2-10 for the continuing discussion.

2-4-3-8 Format Time FTØ5 At FTØ5, the Sub Field Counter is reset, producing a decode of SFØ, a Data Word Counter is reset producing DWØ. The D/E Register indicator flip flop is set to E, the AWD/BWD indicator flip flop is reset raising the AWD level (See Sheet 13 Dwg 700903) and a C Register Empty/Full status indicator flip flop is reset producing CFUL* (Sheet 14 Dwg 700903).

2-4-3-9 Format Time FTØ6 FTØ6 produces HACBUS which loads the C buss with the AWD portion of the actual Disk address as described in detail in paragraph 2-4-2-12. Since the CFUL flip flop is reset, CFUL* is high and is gated with T2ENLDC, signifying FTØ6, and DFLD*, signifying Sub Field Time. This gating produces a C Register load pulse (LDC) which loads the Disk Address on the C buss into the C Register. With CFUL raised, T2XFR is raised and a serial transfer takes place between the C Register and the E Register. The left and right half of this AWD are transferred simultaneously in 12-bit serial fashion into the E Register. The transfer clock is CC. The Parity of this word as all words transferred between the C Register and the D or E Register is determined

by comparing corresponding bits of the left and right half of the word. The thirteenth CC pulse then resets the T2XFR level and the CFUL level and strobes the Parity bit for the AWD into the E Register, and switches the AWD/BWD indicator flip flop to BWD. The BWD is loaded from the C buss to the C Register, and from the C Register to the E Register in a manner similar to that described for the AWD. The thirteenth CC strobes the Parity of the BWD into the E Register, resets T2XFR, resets the AWD/BWD indicator flip flop to AWD and generates EOWD which advances the Sub Field Counter from SFØ to SF1.

(a) Generate T2CLØCBUS A gating of AWD, Write Not (WR*) and SF1 produces the T2CLØBUS level (Sheet 14 Dwg 700903) which loads the output of the Class Ø Functional Control Register onto the C buss (Sheets 3-7 Dwg 700903).

2-4-3-10 Format Time (FTØ7) At FTØ7 REN is raised as described in detail in paragraph 2-4-2-13, and the D/E indicator flip flop is jammed to E after having complemented to D at the EOWD of the header BWD transfer from the C Register to the E Register. With REN raised, the R/W/S circuits in the Disk File synchronize on the Header Field Preamble, and when the End-Of-Preamble (EOP) bit is read, data is released to the Disk TSU, synchronized with the Read Clocks generated from the Read Data bit-transitions. The RC from each of the six data tracks, shifts out the contents of the six E Registers into a comparator circuit to be compared with the prerecorded Header Field bits

being read from the Disk File.

2-4-3-11 Header Count and Header Word Not Equal For a detailed discussion of these functions, refer to sub paragraphs of paragraph 2-4-2-13. These functions are the same for Read Data and Class as for Write Data and Class.

2-4-3-12 Load Class AWD into C Register The down-edge of the CC producing the EOWD of the Header Word C to E transfer also lowers the EFUL indicator flip flop and lowers the CFUL indicator flip flop, which enables the next CC pulse to produce LDC, which loads the C buss, containing the Class Ø word into the C Register. No transfer takes place to the E Register until the EFUL indicator is raised again. This takes place only after the last bit of the Header Word is read back from the six Disk Tracks, producing the T2LØB through T2L5B pulses. These pulses complement D-type flip flops enabled by REN(Sheet 13 left side Dwg 700903). When these flip flops set, they produce the EØFUL through E5FUL levels, which are gated with REN to produce a set for the EFUL indicator flip flop. With EFUL raised T2XFR is raised and the AWD of the Class word is serially transferred into the E Register. The thirteenth CC pulse lowers CFUL and strobes AWD Parity into the E Register. The AWD/BWD indicator flip flop switches to BWD, the T2CL1BUS pulse is generated, which loads the output of the Class 1 Functional Control Register onto the C buss. LDC operates

With the EFUL and CFUL indicator flip flops now set, T2XFR is raised again and the BWD of class is transferred into the E Register. The EOWD following the BWD produces a clear pulse (CLRFCL) which resets the Functional Class Registers (Sheet 14 extreme right Dwg 700903). This EOWD is also gated with REN and RREN, signifying SF1, in this case, to produce first an increment pulse (INCRSF) stepping the SubField counter to SF2, and second to produce upon the arrival of the next CC pulse the reset of REN and the D/E indicator flip flop. When REN resets the Read Data and Read Clocks are gated off by reset of the End-Of-Preamble (EOP) bits in the R/W/S. Another Preamble must be read and REN must be raised again, before Read Data and the Read Clocks enter the TSU again. The thirteenth CC in the Class BWD transfer from the C Register to E Register loads the BWD Parity bit into the E Register and generates an LDC pulse, which loads the C buss into the C Register. Since no data is on the C buss, logic zeroes are loaded into the C Register.

2-4-3-13 Format Time FT12 REN was reset before FT11 and is set again for reading the Class Field back from the Disk File at FT12. The gating is FT11,EOFWD,EQ,and WHD* producing S2REN, which sets the REN flip flop through its clock input. When synchronization has taken place on the recorded data and the End-Of-Preamble (EOP) levels are generated in the R/W/S, the Read Data and Read Clocks enter the TSU in synchronization. The output of the E Register is shifted into the same comparator used

Read Clocks.

for Header Word comparison by the ~~RC~~. The Read Data from the Disk is the other input to the comparator. The same Read Data is also shifted into the front end of the E Register. ~~XX~~ The results of this comparison is of no significance on a Read instruction and the Class-Not-Equal (CNE) level is inhibited from raising. However, at the end of the Class Word the EFUL indicator flip flop is set by the detection of the last bit of the Class ~~XX~~ Field (LØB-L5B) signified by the setting of the six D-type flip flops on the extreme left side of ~~XX~~ Sheet 13 Dwg 700903. With EFUL set and CFUL set during SF2, ~~XX~~ the T2XFR level is raised and CC pulses shift the C Register output of logic zeroes into the front of the E Register while the Class Field read from the Disk into the E Register is shifted into the front of the C Register. The data entering the C Register is identified by continuity symbol A18 and the shift pulse serially loading the C Register is identified by continuity symbol A19 (Sheets 10 and 11 left side Dwg 700903). At Parity bit time ~~XX~~ (T2P), a load pulse T2XCCLØ is generated by a gating of T2P, WR*, SF2, AWD, and the up-edge of CC. ~~XXXXXX XXXXXX XXXXXX~~ This pulse is used to load the output of the C Register into the Class Ø Functional Class Register. The logic for generating T2XCCLØ is on Sheet 14 Dwg 700903 and the Class Registers are on Sheets 2 through 6 Dwg 700903. The down-edge of the same CC lowers CFUL and the next down-edge of CC generates LDC again, clearing the C Register by loading in the empty C buss. The T2XFR level ~~raises~~ rises again as CFUL ~~raises~~ rises, and the BWD of the

Class Field is transferred into the C Register. A similar load (T2XCCL1) pulse for this BWD is generated with the up-edge of the CC during Parity time. This pulse loads the output of the C Register into the Class 1 Functional Register.

NOTE

At the end of record the Class Field is swapped into the Holding Class Register making it available for sampling by the AMCP.

2-4-3-14 Sub Field 3 A gating of REN, RREN, signifying SF2 in this case, and EOWD increments the Sub Field Counter to SF3 and resets REN on the down-edge of the next CC pulse (Sheet 13 Dwg 700903). As the Sub Field Counter increments to SF3, the CFUL indicator is reset on the down-edge of the CC pulse occurring during (T2P) which corresponds to EOWD in time. When SF3 operates, the T2ENLDC level, which enables the generation of LDC during the Sub Field period, is inhibited and no LDC pulse is generated and CFUL remains reset.

2-4-3-15 Format Time FT15 REN is set again for reading of the Data Field at FT15. The gating is FT14, T2READ, WDCTØ*, signifying the word counter was loaded to some word count during the instruction from the AMCP, and EQ, and EOFWD. This gating produces S3REN, which sets the REN flip flop through the clock input and jam sets the Data Field flip flop raising the DFLD level. S3REN also resets the first three stages of the Data Word Counter. DFLD inhibits the Sub Field decodes of these three stages of the

connects
Data Word Counter and an additional five stages to these three original stages to give the Data Word Counter a capability of counting out the Data Field.

(a) Read Preamble and First Disk Word The Preamble is read and the read circuits in the R/W/S synchronize. The End-Of-Preamble (EOP) level is generated and Read Data (T2RDØ-T2RD5) and Read Clocks (T2RCØ-T2RC5) enter the TSU from the Disk through connector 340 and through the cable board at location 3A2 J17. The EOWD associated with the transfer of the Class Field enabled the D/E indicator flip flop to complement from E to D, and the data being read is assembled in the six serial sections of the D Register. The mnemonics operating are: T2DØ-T2D5 signifying the D Register is operating, T2RDØ-T2RD5 signifying Read Data entering the D Register, and T2CLKØ-T2CLK5 signifying the Read Clocks for the six sections of the D Register used to shift the data into the D Register. These clocks are derived from data transitions by the Read Strobe circuits of the R/W/S.

(b) Transfer AWD From the D Register into the C Register When the last bit of the first word is shifted into the D Register, the D type flip flops shown on the extreme left side of Sheet 14 Dwg 700903, produce the DØFUL through D5FUL levels, which are gated with REN and CC to set the DFUL flip flop through the clock input. With the DFUL level raised during DFLD, the T2XFR level is raised (Sheet 13 Dwg 700903) and the AWD portion

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(d) Disk Parity Error Each 24-bit word shifted out of the D or E Register under mnemonic T2SROL and T2 SROR is checked for parity in the same way parity was generated. T2SROL and T2SROR are gated to enable a Disk-Parity-Check flip flop to complement whenever corresponding bits of each half of a 24-bit word differ in logic state. The Disk-Parity-Check flip flop is held off except during T2XFR. At the end of a 24-bit word, the output of this Disk-Parity-Check flip flop (T2DPCH) indicates the parity of that word. The logic just discussed is on Sheet 11 Dwg 700903. When an AWD is written, the Parity-bit is located in bit thirteen of the left half-word. When a BWD is written its Parity-bit is located in bit thirteen of the right half-word. AWD is gated with SROL and the output of this gate is gated with DPCH at bit thirteen time to see if Parity as written for the AWD agrees with Parity as checked on play-back . The logic being discussed is on Sheet 10 Dwg 700903. A similar gating of BWD and SROR is found in this logic to check for Parity in the BWD. Parity time (T2P) or bit thirteen is represented in the logic by continuity symbol H5. This check takes place during a READ for all words in the Data-Field and Check-Field, as signified by the mnemonic ENCH in the logic. If Parity as written differs from Parity determined on play-back, the Disk-Parity-Error (T2DPE) latching flip flop is set. The

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XX T2DPE output of this indicator flip flop is a status condition made available to the AMCP at the end of the record in which it is detected, as discussed in paragraph 2-6-2.1 ~~4.6 which is dedicated to Status Reporting.~~

of the word in the D Register is shifted into the C Register. Data exits the D Register serially as a left and right half word. The mnemonics operating are SROL and SROR which produce data for the C Register which can be identified by continuity symbol A18 (Sheets 10 and 11 Dwg 700903). The shift pulse operating can be identified by continuity symbol A19 on sheets 10 and 11 Dwg 700903. The shift pulse is derived by gating T2XFR with CC and inhibiting the gate with T2P signifying Parity time.

(c) Half-Word Parity ~~Parity Generation~~ Half-Word Parity is generated by ~~XXXXXXXXXX~~ presenting the left and right half data-bit trains (SROL and SROR) to identical flip flops, which are inhibited except during ~~reset before~~ T2XFR. Each logic "1" data-bit enables the flip flop to complement with the CC pulse, and each logic "Ø" data-bit inhibits the flip flop from complementing. At the end of T2XFR, the ~~XX~~ output of the left and right Parity flip flops indicate ~~X~~ left and right half AWD Parity. ~~which is~~ The outputs of these flip flops are loaded into ~~holding~~ latching flip flops by the CC pulse during T2P at the end of the AWD. This load pulse is identified by continuity symbol H10 on Sheets 10 and ~~XXXXX~~ 11 Dwg 700903). The output of the parity flip flops are designated LP and RP.

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(e) Load A Register When T2P is raised during the Data Field ~~XXXXX~~ of a Read operation the CFUL indicator flip flop is raised (Sheet 14 Dwg 700903). A gating of CFUL, DFLD, READ, AWD, and AFUL* produces a load pulse (LDA) for the A Register. The AFUL indicator flip flop is initially reset at FTØ5 time. LDA strobes the output of the C Register (CØØ-C23) into the A Register and loads the

Left Parity (LP) and Right Parity (RP) bits, determined by the process discussed in the preceding paragraph, from the Holding Parity flip flops into another set of flip flops.

(f) Transfer BWD from D Register to C Register The T2P pulse following transfer of the AWD, sets the AWD/BWD indicator flip flop to BWD and the LDA pulse gated with READ , resets the CFUL indicator flip flop. T2XFR raises and the BWD portion of the first data Disk word is transferred from the D Register into the C Register in the same way as described for the AWD. Parity for the BWD is generated in the same way as for the AWD.

(g) Load B Register At T2P following the BWD, the LDB pulse is generated. LDB is produced by a gating of CFUL, READ, DFLD and BWD. The LDB pulse loads the B Register with the BWD from the output of the C Register, and loads the BWD Parity bits into Parity flip flops.

2-4-3-16 Enable Store Request The DFLD level latches a flip flop which supplies one condition for enabling Store requests to a gate. Other conditions for producing the Enable Request (ENRQ) level are: WDCTØ*, once again signifying some word count has been specified in the instruction from the AMCP, and EQ signifying the correct Starting Address has been effected. In addition, the A and B Register must be full or either A or B must be full when the Store Request

is to and odd Central Memory Address as signified by CMA18 in the logic (Sheet 14 ,extreme lower left,Dwg 700903). The two mnemonics RF3* and RF4* are inhibiting signals when low, and operate after the first word of the data field has been transferred. These signals inhibit the generation of ENRQ for a period of time during which the data buffers, through which each word is processed, are in a transitory state and consequently not able to accept another word.

NOTE

A detailed discussion of Disk Request Generation Circuits is deferred until paragraph 2-6.

With the A and B Registers filled,the Store Request is generated by the raising of ENRQ. Both the A and B Registers are filled. However, there outputs are inhibited until either T2ACBUS or T2BCBUS is raised. These levels are produced by gating the output of the A/B indicator flip flop with READ and DFLD. Since the A indicator flip flop is initially reset and since no acknowledgement to the Store request has as yet been received, the A level is raised now, and the output of the A Register and its associated AWD Parity flip flops are enabled. (See Sheet 14 Dwg 700903 for generation of T2ACBUS and T2CBUS) The request is looked at by the TUIM, which assigns priorities for the use of the Central Memory Data buss shared by the four TSU's. When a buss is assigned to this request and

the request is not rejected, subsequently, by the Central Memory, within a specified time period, a signal with mnemonic RF1 is raised. (The logic generating RF1 will be discussed in detail in paragraph 2-6 dealing with Disk Request Generation.) RF1, gated with READ, produces a signal (CBM) which gates the output of the A Register into Central Memory (Sheet 14 Dwg 700903). Data leaves the output gate on the data buffer boards under mnemonic XXXXX TUDOØØ-TUDO23. The Parity bits leave the data buffer boards under mnemonics TUDO24 and TUDO25. The two Parity bits TUDO24 and TUDO25 are gated in the TUIM to produce a single Parity bit (TUDO24) (Sheet 19 Dwg 700903). This bit and the data bits are latched by Master Clock (MC) and leave the TUIM under mnemonic XXX TUDOØØL*-TUDO23L* and TUD24* (Sheets 19 and 20 Dwg 700903). From the TUIM, the Data and Parity bits are jumpered through a XXXXX Cable board (Sheet 47 Dwg 700903) and leave the AMTU through connectors 382 and 383. The EOWD produced at the end of the BWD transfer from the D Register to the C Register, enables XX the D/E indicator flip flop to complement to E on the CC pulse. This connects the C Register to the E Register, into which the next Disk word will be shifted from the Disk File. It should be noted that the Disk word is broken up into two 24-bit words and Parity, and each of these words require a Store request for its transfer back to Central Memory.

(a) Check Field Generation by Reading of Data Field All data shifted out of the D and E Registers into the C Register during the Data Field , is also presented to a half-adder circuit to be added with the output of a Check-Field Register. The logic for this function is located on the extreme upper left side of Sheets 10 and 11 Dwg 700903. A signal, T2ENCH, identified by continuity symbol H4, enables the operation of the Check-Field Register during the Data Field and for the Check Field which follows. T2SROL and T2SROR representing serial data forming left and right half words from the D or E Register and identified by continuity symbol A4 are gated with READ to produce one input to each half-word half adder circuit. CHOL and CHOR represents the other input to the left and right half-word half-adder circuits. T2XFR inhibited by the Parity bit time (T2P) and identified by continuity symbol H6 in the logic, is gated with CC to produce shift pulses for the Check Field Register. Each Disk word bit of the Data Field is half-added with the results of previous half-adder bit summations exiting from the output of the Check Field Register and the results of this half-adder summation are shifted into the Check-Field Register. When an entire Disk word has been shifted through the half-adder into the Check Field Register, the EOWD pulse operates. EOWD is gated with the Rotation (ROT) signal, which is high when bit 19 (Disable Check Code Cycle) in the Instruction Control Register is reset, and with CC identified by continuity symbol A9 (Sheets 10 and 11 Dwg 700903). This

gating provides a pulse for shifting the Check-Field Register one additional bit position for each Disk word. At time of rotation, the output of the right half-word Check-Field Register is connected to the input of the left half-word Check-Field Register, and the output of the left half-word Check-Field Register is connected to the input of the right half-word Check Field Register. Rotation, therefore, shifts the entire 50-bit Check-Field Register one bit position for each Disk word processed through the half-adder.

2-4-3-17 Check Field Each time the BWD of each Disk word is transferred from the D or E Register, the EOWD signal is generated. Using the three stages of the Sub-Field Data Word Counter and the additional five stages connected to these stages by raising DFLD, a count of 256 is decoded, which marks the end of Data Field and the beginning of Check Field. The pulse is given mnemonic CCHFLD* (Sheet 13, right side, Dwg 700903). CCHFLD* latches a flip flop to the set position, producing DWOVF, which enables a D-type flip flop to set. When the LDB pulse operates to transfer the BWD of the last word of the Data Field into the B Register, the D-type flip flop sets producing the T2CHFLD level (Sheet 13, upper right Dwg 700903). When T2CHFLD is raised, the previously written Check-Field is read into the D Register. When the D Register is full the T2XFR level is raised (Sheet 13 Dwg 700903). The D Register output (T2SROL and T2SROR) identified

shifted into another half-adder circuit with the output of the Check-Field Register (T2CHOL and T2CHOR) identified by continuity symbol A5. The Check-Field Register output at Check-Field time, which is the half-adder summation of each bit of each word of the entire Data-Field, should agree bit-for-bit with the Check-Field word being transferred from the D Register, since this word was formed by the half-adder summation of the same Data-Field, when it was written on the Disk.

(a) Transfer Check-Field Comparison Results to C Register (AWD) The AWD output of this half-adder circuit identified by continuity symbol A18 (Sheets 10 and 11 Dwg 700903) is shifted into the C Register by the CC operating while T2XFR is raised. The shift pulse is identified by continuity symbol A19 (Sheets 10 and 11 Dwg 700903).

(b) Load Check-Field Status Register With AWD of Check-Field When the T2P pulse following the AWD operates at the thirteenth bit-time, the CFUL indicator flip flop is set by the down-edge of CC. The gating of CFUL, AWD, T2CHFLD, READ and CC then produces a load Check Ø pulse (T2LDCHØ) (Sheet 14, right side, Dwg 700903). The T2SDCHØ pulse strobes, the output of the C Register (CØØ-C23) into a holding Check Field Ø Register (Sheet 9 Dwg 700903). The output of this Register is routed through a cable card (Sheet 49 Dwg 700903), and out connector 380 to the AMCP, which can sample the data if it desires.

(e) BWD When CFUL lowers again after T2P time, the T2XFR window raises again, and the BWD portion of the Check-Field word from the Disk is compared XXX with the BWD portion of the Check-Field XX word from the Check-Field Register. The results are transferred XX into the C Register. The CFUL indicator flip flop sets and produces, when gated with T2CHFLD, READ and CC, the LDCH1 pulse, which strobes the BWD portion of the Check Field word now in the C Register into a XXXX holding Check-Field (1) Register (Sheet 9 Dwg 700903). The output of this Register is routed through a cable card (Sheet 49 Dwg 700903), out connector 380 to the AMCP, which can sample the data if it desires.

(d) Set Check Not Zero XXXX Indicator The LDCH1 pulse is not conditioned by AWD or BWD and XXXX therefore actually operates each time CFUL is raised during the Check-Field. Each time the LDCH1 pulse operates, the C Register is full with, first, the AWD of the Check-Field and next with the BWD of the Check-Field. Each time the LDCH1 operates every bit in the C Register should be at logic zero. The individual bits of the C Register are collector OR-gated after one inversion. The results of the OR-gating is called Check-Zero (CHZ), and should be at logic "1" as long as all bits of the C Register are low at LDCH1 time (Sheet 9 Dwg 700903). After one inversion to CHZ*, this signal is gated with the LDCH1 pulse (Sheet 8, middle bottom, Dwg 700903), to set a latch if one bit in either the AWD or BWD Check-Field from the Disk and Check-Field Register fail to match, thereby raising the CHZ* line.

Setting the latch, generates T2 CHNZ. The output of this flip flop (T2 CHNZ) is a status condition made available ~~This is one of many status indicators which will be discussed in more detail in paragraph 2-6.~~ to the AMCP at the end of the record in which it was detected as discussed in paragraph 2-6-5.

NOTE

Paragraphs 2-4-3-18 and 2-4-3-19 following, discuss Drums and Disks together rather than independently, since the function discussed in these paragraphs is essentially the same for Drums and Disks.

~~2-4-3-18 End of Read Data and Class Operation Swap Count Cycle~~

~~When no new instruction has been received from the AMCP during a record, the Swap-Cycle which comes at the end of the record will be the last Swap-Cycle of the operation. For further discussion refer to paragraph 2-4-2-21.~~

2-4-3-18 End of Operation (Read Data and Class) Swap-Count-Cycle

When no new instruction is received from the AMCP while the Read Data and Class operation is in progress, a Swap-Count-Cycle will be generated which swaps the Functional Registers into the Holding Registers in order to make information available to the AMCP upon request. For a detailed discussion of the End-Of Operation Swap-Count-Cycle, refer to paragraph 2-4-2-22, which discusses the End -Of-Operation (Write) Swap-Cycle. The Read End-Of-Operation Swap-Cycle operates in an identical manner.

2-4-4 Write If Class Is Equal This operation applies to Disks only. Essentially, this operation is the same as a Write Data and Class operation except at Class time the Class Word previously written on the Disk, is compared with the Class loaded into the Class Registers during the Instruction sequence. If there is agreement, the TSU logic proceeds with a normal write Data Field operation. If there is not agreement no data transfer takes place.

2-4-4-1 Write-If-Class-Equal Load Sequence For this operation, the following Holding Control Registers are loaded:

INSTRUCTION

DEVICE ADDRESS

CENTRAL MEMORY ADDRESS

MAP (OPTIONAL)

WORD COUNT

CLASS

UNIT

One Control Register is loaded from the AMCP output buss with each pair of ACTC and WTPC commands as discussed in paragraphs 2-3-3-2 and 2-3-3-3. The Instruction Register is loaded first, and the Unit Register is loaded last, as discussed in paragraphs 2-3-3-2 (b) and 2-3-3-3 (d).

(a) Generate Swap Required And Start Swap Counter For this operation, a Swap-Required (SWPRQ) signal is generated at the end of the Register loading sequence, as discussed in paragraph 2-4-1-2 (a) and the End-Of-Record pulse (EOR) for Disk and ERPG

initiates a Swap-Counter-cycle, as discussed in paragraphs 2-4-1-2 (b, c. and d).

2-4-4-2 Swap Function During Write If Class is Equal The Swap Counter decodes are the same for this operation as for the Write Data and Class operation, discussed in paragraph 2-4-2-2 (a through i).

2-4-4-3 Equal EQ is effected in this operation just as in a Write Data and Class operation, as discussed in paragraphs 2-4-2-3, 2-4-2-4, and 2-4-2-5.

2-4-4-4 Format Time FTØ5 At FTØ5, the Sub-Field Counter is reset, producing a decode of SFØ, a Data Word Counter is reset, producing DWØ. The D/E Register indicator flip flop is set to E, the AWD/BWD indicator flip flop is reset raising the AWD level (Sheet 13 Dwg 700903), and the EFUL indicator flip flop is jam set, and the C Register Empty/Full status indicator flip flop is reset producing CFUL* (Sheet 14 Dwg 700903).

2-4-4-5 Format Time FTØ6 FTØ6 produces HACBUS, which loads the C buss with the AWD portion of the actual Disk Address as described in detail in paragraph 2-4-2-12. T2ENLDC enables the LDC pulse to be generated and the Disk Address is loaded from the C buss into the C Register. CFUL raises with the LDC pulse and T2XFR level goes up enabling a serial transfer between the C Register and the E Register. The left and right half of this AWD are transferred simultaneously in 12-bit serial fashion into the E Register. Parity is determined by

serial comparison of corresponding bits of the left and right half-words. The thirteenth CC resets T2XFR and strobes the Parity-bit into the E Register. The BWD is loaded from the C buss into the C Register, and from the C Register into the E Register in a manner similar to that described for the AWD. The thirteenth CC strobes the Parity of the BWD into the E Register, resets T2XFR, resets the AWD/BWD indicator flip flop to AWD and generates EOWD, which advances the Sub-Field Counter from SFØ to SF1.

(a) Generate T2CLØBUS A gating of AWD,WR* and SF1 generates the T2CLØBUS level (Sheet 14 Dwg 700903(which loads the output of the Class Ø Functional Control Register onto the C buss (Sheets 3 through 7 Dwg 700903).

2-4-4-6 Format Time FTØ7 At FTØ7, REN is raised by the S1REN pulse as described in detail in paragraph 2-4-2-13, and the D/E indicator flip flop is jammed to E after having complemented to D at the EOWD of the header BWD transfer from the C Register to the E Register. The S1REN pulse also jams the EO through E5 latching flip flops (Sheet 13, upper left side, Dwg 700903) enabling the E Register for transfer. Finally, S1REN pulse jams the Data Word Counter to DW7. With REN raised, the R/W/S/ circuits in the Disk File synchronize on the Header-Field Preamble, and when the End-Of-Preamble (EOP) bit is read, data is released to the Disk TSU, synchronized with the Read Clocks generated from the Read Data bit-transitions. The RC

from each of the six data tracks shifts out the contents of each of the six E Registers into a comparator circuit to be compared with the prerecorded Header Field bits being read from the Disk File.

2-4-4-7 Header Count and Header Word Not Equal For a detailed discussion of these functions, refer to sub paragraphs of paragraph 2-4-2-13. These functions are the same for Read Data and Class as for Write Data and Class.

2-4-4-8 Load Class AWD Into C Register The down-edge of the CC producing the EOWD of the Header-Word C Register to E Register transfer, also lowers the EFUL indicator flip flop and lowers the CFUL indicator flip flop, which enables the next CC pulse to produce LDC, which loads the C buss, containing the Class Ø word into the C Register. No transfer takes place to the E Register until the EFUL indicator is raised again. This takes place only after the last bit of the Header-Word is read back from the six Disk tracks, producing the T2LØB through T2L5B pulses. These pulses complement D-type flip flops enabled by REN (Sheet 13, left, side, Dwg 700903). When these flip flops set, they produce the EØFUL through E5FUL levels, which are gated with REN to produce a set for the EFUL indicator flip flop. With EFUL raised, T2XFR is raised and the AWD of the Class-Word is serially transferred into the E Register. The thirteenth CC pulse lowers ~~XXXX~~ CFUL and strobes AWD Parity into the E Register. The AWD/BWD indicator flip flop switches to BWD, the T2CL1BUS pulse is ~~XXXX~~ generated, which loads the output

of the Class 1 Functional Control Register onto the C buss. The EOWD associated with the BWD of the Class-Word just transferred to the E Register increments the Data Word Counter to DWØ and increments the Sub-Field XX Counter to XXXX SF2 and resets REN. When REN resets, the Read Data and Read Clocks are gated off by reset of the EOP bit in the R/W/S. Another XXXX Preamble must be read and REN must be raised again, before Read Data and the Read Clocks enter the TSU again. The thirteenth CC in the Class BWD transfer from the C Register to E Register loads the BWD Parity bit into the E Register and generates an LDC pulse, which loads the C buss into the C Register. Since no data is on the C buss, logic zeroes are loaded into the C Register.

2-4-4-9 Format Time FT12 REN was reset before FT11 and is set again for reading the Class -Field back from the Disk File at FT12. The gating is FT11, EOFWD, EQ, and WHD*, producing S2REN, which sets the REN XXXX flip flop through its clock input.

(a) Class Not Equal When synchronization has taken place on the recorded data and the End-Of-Preamble (EOP) levels are generated in the R/W/S, the Read Data and Read Clocks enter the TSU in synchronization. The output of the E Register is shifted into the same comparator used for Header Word comparison, by the Read Clocks. The Read Data from the Disk is the other input to the comparator. The same Read Data is also shifted into the XXXX front end of the E Register. The results of this comparison,

signified by the mnemonics CMPEA and CMPEB are gated with the output of a latch set by the S2REN pulse (Sheet 14 Dwg 700903). REN is the only other level at the gate. If either CMPEA or CMPEB rise, the gate produces an output, setting a latch and thereby producing the Class-Not-Equal (CNE) level. The CMPEA and CMPEB levels are looked at during a compare window defined by setting of a latch by S2REN, previously mentioned, and the resetting of this latch by the RRHD pulse, which is generated by the last bits of the Class-Word being read from the Disk and thereby setting the EØFUL-E5FUL flip flops shown on the left side of Sheet 13 Dwg 700903. The CNE output is a status condition made available to the IMCP at the end of a record as discussed in paragraph 2-6-3.

(b) Write Enable Write Enable (WEN) is inhibited or enabled to set by the results of the Class-Field comparison. A clock input (S3WEN) to the WEN flip flop is produced by gating WRCLC, WEN*, WDCTØ* and FT13. When FT13 arrives the up-edge of the clock is produced. During FT13 the Class comparison takes place. CNE is presented to the J enable and the jam-reset inputs of the WEN flip flop. If Class-Not-Equal (CNE) is set, the WEN flip flop is inhibited and when the Format Counter steps from FT13 to FT14, the S3WEN clock down-edge operates but the WEN flip flop, being inhibited, remains low and no write transfer takes place. If CNE is reset the WEN flip flop is enabled and when the Format Counter steps from FT13 to FT14 the S3WEN clock down-edge sets WEN which in turn latches WENDL.

WENDL is used to enable the write amplifiers in the R/W/S of the Disk File.

(c) Load E Register With ~~First~~ second Word Of Data Preamble Since the detection of the last bit of the Class-Word raised EFUL and since CFUL is raised, T2XFR also rises~~XXX~~ and ~~XXXXXX~~ enables the shifting out of the logic zeroes in the C Register ~~XX~~ loaded during FT1Ø by the LDC produced after the Class-BWD transfer into the E Register. This T2XFR is occurring while the Sub-Field Counter is at SF2. SF2 is gated with the Write-If Class-Compare instruction (WRCLC) produced when bits 17 and 18 of the Instruction Register are at logic "1". This gating produces a level (T2EVP) which forces logic zeroes for every bit being transferred from the C Register. At bit thirteen time, the Parity bit is also forced to a logic zero, as the AWD/BWD indicator flip flop switches to BWD. The BWD is transferred into the E Register while T2EVP continues to operate. T2EVP causes this entire Disk Word to be transferred into the E Register as logic zeroes, thus forming the ~~first~~ second Disk word of the Data Field Preamble.

(d) Load Class Functional Register As the C Register logic zero output is shifted into the front of the E Register, the E Register has the Class-Field which was read in from the Disk during Class comparison, shifted out into the C Register. The data entering the C Register is identified by continuity symbol A18 and the shift pulse serially loading the C Register is identified by continuity symbol A19 (Sheet 10 and 11, left side Dwg 700903).

At T2P time a load pulse (T2XCCLØ) is generated by a gating of T2P, WR*,SF2, AWD, and CC. This pulse is used to load the output of the C Register into the Class Ø Functional Class Register. The logic for generating T2XCCLØ is on Sheet 14 Dwg 700903 and the Class Registers are on Sheets 2 through 6 Dwg 700903. The down-edge of the same CC lowers CFUL and the next down-edge generates LDC again, clearing the C Register by loading in the empty C buss. The T2XFR level rises again as CFUL rises and the BWD of the Class-Field is transferred from the E Register into the C Register. A second load pulse (T2XCCL1) for the BWD is generated with the up-edge of the CC during Parity time. This pulse loads the output of the C Register into the Class 1 Functional Register.

NOTE

> At the end of the record the Class-Field is swapped into the Holding Class Register, making the Class information available for sampling by the AMCP.

2-4-4-10 Write Data Preamble With WENDL raised, the write amplifiers for the selected heads are switched on and the content (All logic zeroes) of the D Register, which was reset at FTØ5, is written on the Disk as the first word in the Data-Field Preamble. The output of the D Register is selected rather than the output of the E Register, since the D or E Write Mode (DWRMOD/EWRMOD) flip flop is initially reset

before WEN is raised (Sheet 13, extreme upper left, Dwg 700903). Write Data exits the D Register through gates enabled by WENDLXXXX and the T2DØ through T2D5 levels (SheetsXX 10 and 11 Dwg 700903). It should be noted that S3WEN jam sets the DFUL and EFUL indicator flip flops (Sheet 13 Dwg 700903). When the last bit of the first word of the Preamble is shifted out of the D Register as signified by the mnemonics LØB and DØ being raised, the DFUL flip flop is reset and the DWRMOD/EWRMOD flip flop sets, producing EWRMOD (Sheet 13, left side, Dwg 700903). Now, the second word of the Data Preamble is written from the E Register, which is loaded with an all logic zero Disk Word. With the DFUL indicator flip flop reset, T2XFR goes up and enables AWDX an AWD-transfer of logic zeroes from the C Register into the D Register. XXThe thirteenth CC produces LDC, which loads the empty C-buss into the C Register again. T2XFR raises and enables the transfer of the logic zero output of the C Register into the D Register. The D Register is now loaded with the third Preamble word, and the EOWD occurring at the end of the WXXX BWD, switches the D/E indicator flip flop to E. When the E Register writes the final bit of the second Preamble -Word, the EWRXEWXXX DWRMOD/EWRMOD flip flop switches back to DWRMOD and the EFUL indicator flip flop resets. The D Register shiftx the third Preamble-Word onto the Disk. The fourth word of the Data-Preamble is produced by gating SF3, DW7, and READ* with AWD and BWD at two separate gates producing T2PACBUS and T2PBCBUS levels which force End-Of-Preamble (EOP) logic one bits onto the C buss. These bits eventually XXXXXXX

produce the EOP-bit for four of the sections of the E Register and the Parity generation logic supplies a logic one for the EOP bit of the remaining two sections of theE Register.

2-4-4-11 Data Field, Check-Field, and Postamble The Data-Field, Check-Field, and Postamble of the Write-If-Class-Compare operation, are handled exactly as in a Write Class and Data operation (Refer to paragraphs 2-4-2-17 through 2-4-2-19.)

2-4-4-12 End of Write-If-Class -Compare Operation Swap-Count- Cycle When no new instruction is received from the AMCP while the Write-If-Class-Compare operation is in progress, a Swap-Count-Cycle will be generated which swaps the Functional Registers into the Holding Registers in order to make information available to the AMCP upom request. For a detailed discussion of the End-Of-Operation Swap-Count-Cycle, refer to paragraph 2-4-22, which discusses the End-Of-Operation Swap-Cycle in a Write Data and Class operation. The Write-If-Class-Compare operation is identical.

2-4-5 Write Headers This operation, which applies to Disk Files only, causes the complete Disk Address of a given record to be written into that record. The Header Field consists of four Preamble Disk words, a Header Disk-word and a Postamble Disk-word. The writing of headers is done before the Disk-File is placed in the Computer System for transfer operation

2-4-5 Write Headers Load Sequence For this operation, the following Holding Control Registers are loaded:

INSTRUCTION

DEVICE ADDRESS

UNIT

One Control Register is loaded from the AMCP output buss with each pair of ACTC and WTPC commands as discussed in paragraphs 2-3-3-2 and 2-3-3-3. Ths Instruction Register with bit 17 set and bit ~~XX~~ 18 reset and thereby producing the Write-Header (WHD) command, is loaded first and the Unit Register is loaded last, as discussed in~~XX~~ paragraphs 2-3-3-2 (b) and 2-3-3-3 (d).

(a) Generate Swap Required And Start Swap Counter For this operation, a Swap Required (SWPRQ) signal is generated at the end of the Register loading sequence, as discussed in paragraph 2-4-1-2 (a) and the End-Of-Record pulse (EOR) initiates a Swap-Counter-Cycle as discussed in paragraphs 2-4-1-2 (b,c,and d).

2-4-5-2 Swap Function During Write-Header The Write-Header operation requires the Swap Device Address (SWDA) decode to load the Device Address into the Functional Device Address Control Registers, and requires the Swap Unit and Instruction (SWUNI) decode to swap the Unit Selection and Instruction into the Functional Control Registers. However, the other Swap decodes discussed in paragraph 2-4-2-2 (a through i) are of no significance for this operation.

2-4-5-3 Equal EQ is effected in this operation just as in a Write Data and Class operation, as discussed in paragraphs 2-4-2-3, 2-4-2-4 and 2-4-2-5.

2-4-5-4 Format Time FTØ5 At FTØ5, the Data Word Counter is reset, producing DWØ, the D/E indicator flip flop is jammed to D [illegible] by the S1DFUL pulse, produced by gating [illegible] WHD and FTØ5. Also at FTØ5 the DFUL and EFUL Empty/Full status indicator flip flops are jammed set. The S1DFUL pulse is used to set the DFUL flip flop while the EFUL flip flop is set by FTØ5 (Sheet 13 Dwg 700903).

2-4-5-5 Format Time FTØ6 At FTØ6, the WEN flip flop is set,

through the clock input. The signal used as a clock is produced by a gating of FTØ5, WHD, EOFWD, and WEN* (Sheet 13 Dwg 700903) . When WEN rises the WENDL latch is also set thereby enabling the write amplifier circuits in the R/W/S of the Disk File. WENDL gated with DWRMOD, which is the reset output of the DWRMOD/EWRMOD flip flop, produces a jam-set for six latches producing DØ-D5 levels (Sheet 13, upper left, Dwg 700903). The D Register, which is filled with logic zeroes by reason of being reset by FTØ5, begins to shift the first Disk-Word of the Header-Preamble into the R/W/S with Clocks (T2CLKØ-T2CLK5) which are enabled at a gate by (T2DØ-T2D5) the output of the six latches (Sheets 10 and 11 Dwg 700903).

(a) Load Third Preamble Word into C Register The T2ENLDC level produced FTØ6 (Sheet 13 Dwg 700903) enables the Load C Register (LDC) flip flop to set on the CC clock producing the LDC pulse. LDC raises the CFUL indicator flip flop (Sheet 14 Dwg 700903) and loads the empty C buss into the C Register causing it to be filled with logic zero bits.

(b). Transfer Third Preamble-Word into D Register When the last bit of the first Preamble-Word is shifted out of the D Register, the LØB decode (Sheet 14, upper left, Dwg 700903), is produced. LØB, DØ, and WENDL are gated to reset the DFUL indicator flip flop (Sheet 13, lower left, Dwg 700903). When DFUL lowers, T2XFR rises and the AWD of what will be the third Preamble-Word is shifted into the D Register. When T2P operates,

LDC loads logic zeroes from the C buss into the C Register again, and T2XFR is lowered. CFUL and T2XFR are set again, and the BWD of what will be the third Preamble-Word is shifted into the D Register. T2EVP produced by gating WHD and DWØ1 force (Sheet 13, extreme right, Dwg 700903) a logic zero for all 50-bits of this Disk-Word (Sheets 10 and 11 Dwg 700903).

(b) Load AWD of Fourth Preamble-Word into C Register The EOWD is decoded, the D/E indicator flip flop switches to E, the AWD/BWD indicator flip flop complements to AWD, the Data Word Counter steps to DW1, the DFUL indicator flip flop is set and T2XFR lowers (Sheet 13 Dwg 700903). The CFUL indicator flip flop resets and the LDC pulse loads the C buss into the C Register. At this time the C buss contains the End-Of-Preamble (EOP) bits associated with the AWD. The EOP bit configuratio has been loaded onto the C buss by the PACBUS signal, produced by a gating of WHD, DW1 and AWD (Sheet 13, extreme right, Dwg 700903). PACBUS forces a logic one into bit positions Ø2 and 16 of ~~the~~ C buss (Sheet 12 Dwg 700903).

(c) Write Second Word Of Header Preamble When the last bit of the first Preamble-Word is detected the DWRMOD/EWRMOD flip flop complements to EWRMOD latching EØ-E5 (Sheet 13, upper left, Dwg 700903). This causes the E Register, which was also reset at FTØ5, to shift the second Preamble-Word consisting of logic zeroes, into the R/W/S by the T2CLK-T2CLK5 clocks, enabled by the sig EØ-E5 latch outputs but now operating under mnemonic T2DØ*-T2D5* (Sheets 10 and 11 Dwg 700903).

(d) Transfer Fourth Preamble-Word into E Register When the last bit of the second word of the Header Preamble is shifted

out of the E Register, the EFUL indicator flip flop lowers, raising T2XFR. The AWD of the fourth Header Preamble-Word is shifted into the E Register. The T2P decode lowers T2XFR, generates another LDC and complements the AWD/BWD indicator flip flop to BWD. A gating of WHD,DW1, and BWD produces PBCBUS (Sheet 13 ,extreme right, Dwg 700903). PBCBUS forces a logic one on bits 11 and 12 of the C buss. These bits will eventually become the EOP bits for two sections of the E Register. LDC loads the BWD into the C Register. CFUL rises and forces T2XFR up again and the BWD of the fourth Preamble-Word is shifted into the E Register.

(e) Write Third Word of Header-Preamble When the last bit of the second Preamble-Word is detected,the DWRMOD/EWRMOD flip flop complements to DWRMOD, producing the D0-D5 latched levels enabling the T2CLK0-T2CLK5 clock pulse under mnemonic T20-T25. With this clock, the ~~B Register shift pulse.~~ The third Preamble-Word (All logic zeroes) is shifted into the R/W/S (Sheets 10 and 11 Dwg 700903).

(f) Load Header AWD into C Register The EOWD is decoded after the transfer of the fourth Preamble BWD, enabling the D/E indicator flip flop to complement to D. The AWD/BWD indicator flip flop complements to AWD, the Data Word Counter steps to DW2, the DFUL indicator flip flop sets, and T2XFR lowers (Sheet 13 Dwg 700903). The CFUL indicator flip flop resets and the LDC pulse loads the AWD of the Header-Word from the C buss into the C Register. The AWD of the Header-Word has been strobed onto the C buss by HACBUS. This signal is produced by gating WHD,DW2, and AWD (Sheet 14, upper

right, Dwg 700903). The Header-AWD consists of the output of the Track Position Register, the Band Address Functional Control Register, and the Position Counter record count decode output(Sheet 12 Dwg 700903).

(g) Write Fourth Preamble-Word When the last bit of the third Preamble-Word is shifted out of the D Register, the DWRMOD/EWRMOD flip flop complements to EWRMOD and the EØ-E5 outputs are latched (Sheet 13,upperleft,Dwg 700903). The T2CLKØ-T2CLK5 pulses enabled by T2DØ*-T2D5* shift the fourth Preamble-Word, which contains the EOP bits,into the Disk File. The EOP bits for Shift Register sections SR3 and SR5 are produced by the generation of Parity for AWD and BWD, respectively.

(h) Transfer Header-Word into D Register When the last bit of the third Preamble-Word is shifted out of the D Register, the DFUL indicator flip flop lowers, raising T2XFR. The AWD of the Header-Word is shifted into the D Register. The T2P decode generates the Parity bit, complements the AWD/BWD indicator flip flop to BWD and produces another LDC pulse, which loads the C buss into the C Register. The BWD of the Header-Word has been strobed onto the C buss by HBCBUS,produced by a gating of WHD, DW2, and BWD (Sheet 14 ,extreme right, Dwg 700903). The BWD of the Header-Word consists of the output of the Track Position Register and the Band Address Functional Control Register (Sheet

12 Dwg 700903). CFUL raises T2XFR again, and the BWD of the Header-Word is transferred into the D Register.

(i) Load AWD of Postamble into C Register The EOWD is decoded and causes the D/E indicator flip flop to complement to E. The AWD/BWD indicator flip flop complements to AWD, The Data Word Counter steps to DW3, and the DFUL indicator flip flop is set while the T2XFR level lowers (Sheet 13 Dwg 700903). The CFUL indicator resets and the LDC pulse loads the C buss (All logic zeroes) into the C Register.

(j) Write Header Word When the last bit of the fourth Preamble-Word is shifted out of the E Register, the DWRMOD/EWRMOD flip flop complements to DWRMOD, and the DØ-D5 outputs are latched (Sheet 13,upper left,Dwg 700903). The T2CLKØ-T2CLK5 pulses enabled by T2DØ-T2D5, shift the Header-Word into the Disk File.

(k) Transfer Postamble Word into the E Register When the last bit of the fourth Preamble-Word is shifted out of the E Register, the EFUL indicator flip flop lowers and raises T2XFR. The AWD of the Postamble-Word (All logic zeroes is shifted into the E Register. The T2P decode generates a Parity-bit, complements the AWD/BWD indicator flip flop to BWD and produces another LDC pulse, which loads the C buss (All logic zeroes) into the C Register. CFUL raises, forcing T2XFR up and the BWD of the Postamble-Word is shifted into the E Register.

(1) Write Postamble-Word When the last bit of the Header-Word is shifted out of the D Register, the DWRMOD/EWRMOD flip flop complements to EWRMOD and the EØ-E5 outputs are latched (Sheet 13, upper left, Dwg 700903). The T2CLKØ-T2CLK5 pulses enabled by T2DØ*-T2D5* shift the Postamble-Word into the Disk File.

2-4-5-6 Reset Write Enable The EOWD produced during DW3 of Sub-Field SFØ produces R1WEN, which resets the WEN flip flop (Sheet 13 Dwg 700903). When WEN lowers the D Register is in the process of shifting out the Header-Word to be written on the Disk File. The last bit of the Header-Word, signified by LØB and DØ resets DFUL. The LDC pulse is produced and loads the C Register and sets CFUL, but T2XFR is inhibited from rising by WEN being reset (Sheets 13 and 14 Dwg 700903). The DFUL indicator flip flop must remain reset now since WEN and EOWD must now remain low for the remainder of this operation. Although WEN is lowered, WENDL is still latched and the Postamble-Word out of the E Register follows the Header-Word out of the D Register into the R/W/S of the Disk File. When the last bit of the Postamble-Word is detected, a gating of LØB and EØ resets the EFUL indicator flip flop (Sheet 13 Dwg 700903). With WEN, DFUL and EFUL all reset and with the Sub-Field Counter at SF1 a reset is produced for the WENDL latch (Sheet 13 Dwg 700903). With WENDL lowered, the Write-Header operation is completed.

2-4-5-7 End Of Operation (Write -Header) Swap-Count-Cycle The continuing discussion is based on the sssumption that no new instruction from the AMCP was received while the Write-Header operation was being executed. Logic discussed is to be found on Sheets 8, Disk, and 28 Drum, Dwg 700903.

(a) Swap Count 1 The Swap Device Address (SWDA) is produced making the Device Address available to the AMCP upon request. Swap-Count-1 also produces the Load-Status-Register (LDST) pulse, which strobes the output of all status error indicators into a Status Register. (Status is discussed in detail in paragraph 2- .)

(b) Swap Count 2 This decode is used to produce the Clear-Error-Indicator (CLERR) pulse, which resets all status error indicators. (Status is discussed in detail in paragraph 2 .)

NOTE

The other Swap-Count decodes are of no pafticular significance during a Write-Header operation.

2-4-6 Continue This operational instruction XXXXXXXXX modifier is not set in an XXX initial instruction, but rather is set in another instruction for continuing an already functioning operation beyond the record in which it is functioning.

2-4-6-1 Continue Register Load Sequence Continue requires different register loading for transfer operations than for a Write-Header operation as explained in the following text.

(a) Continue Transfer Operation During a Continue transfer operation the following Holding Registers are loaded from the AMCP

INSTRUCTION (bit 16 only is set)

CLASS (Except for Write Data and Class)

MAP (OPtional)

UNIT

(b) Continue Write-Header Operation During a Continue Write-Header operation, only the Instruction and Unit Register are loaded by the AMCP.

NOTE

To perform a Continue operation the Unit Holding Register must always be loaded with the same Unit selection as that loaded on the initial instruction. This restriction is necessary to prevent the loss of a complete Disk or Drum revolution on Disk Policy type operations or to prevent Drum Policy Violation on Drum Policy operations. ~~These undersireable operations~~

Disregard of this restriction could result in the generation of the T2NEWU New Unit level(T2NEWU), as described in paragraphs 2-4-1-3(e) and 2-4-1-4. It should be noted that the T2NEWU signal is produced even though the Unit Holding Register is not swapped with the Functional Unit Register.

2-4-6-2 Generate Swap Required and Start Swap Counter for Continue The Swap Required (SWPRQ) flip flop is set for enabling the Continue Swap Count Cycle by the effecting of the command starting Device address of the initial instruction. For Drum units, gating is RCE, and DMPOL* for Disk Policy instructions, and DMPOL only, for Drum Policy instructions(Sheet 28 Dwg 700903). For Disk units, the gating is identical except for Disk Policy instructions, the Track Verification (TV) level is also required (Sheet 8 Dwg 700903). SWPRQ is gated with the EORP pulse arriving at the end of the record during which the initial instruction operation was performed. This initiates a Swap-Counter-Cycle as discussed in paragraphs 2-4-1-2 (b,c,and d).

2-4-6-3 Set Continue Flip Flop The Continue bit (bit 16) in the Holding Instruction Register is gated with EORP and SWPRQ to produce a J-enable for a Continue flip flop (Sheet 8 for TSUØ and Sheet 28 for TSU2 Dwg 700903). When the Continue flip flop sets it produces the CONF level.

2-4-6-4 Swap Function During Continue of Transfer The set condition of the Continue flip flop (CONF) during a transfer operation, qualifies some of the Swap Count decodes as discussed in the following subparagraphs.

(a) Swap Count 1 During a Continue-Swap-Cycle, Swap Count 1 enables address incrementation decode gates. for both Drums and Disks. The gates enabled produce the following incrementation pulses:

INCRA - (Increment Record Address until in last Drum or Disk Record)

CLRRA - (Clear Record Address) (This returns the Record address to Record Ø when the last Record on the Drum or Disk has been exhausted)

INCBA- (Increment Band) (When last Record has been exhausted on Drum or Disk, if not within last Band)

CLRBA (Clear Band Address) (This returns the Band Address to Band Ø, when the last Band on the Drum or Disk has been exhausted)

INCTA- (Increment Track Address) (This increments the Disk Track Address, whenever Band Address is cleared) --- Disk Only

NOTE

The decode for Last Record Address (LSTRA) is decoded within the Drum -TSU (Sheet 27 Dwg 700903) and Disk-TSU (Sheet 9 Dwg 700903). However, the last Band Address (LSTBA) is decoded in the R/W/S unit of each respective Device.

The Swap-Device Address (SWDA) pulse is not produced during a Continue operation. The Functional Device Address Register is incremented only during a Continue operation by the incrementation pulses produced in Swap Count 1. The reset output of the Continue flip flop (CONF*) is used to inhibit the generation of SWDA.

(b) Swap Count 2 This decode produces a Clear-Word-Count-Register/Counter (SCLRWC) pulse, which resets the Word-Count Holding Register/Counter, when CONF is raised.

(c) Swap Count 3 This decode produces the Swap Map (SWMAP) pulse just as in an initial instruction cycle, and in addition produces as a function of Continue, a Set-Word-Count (SETWC) pulse, which jam-sets every stage of the Word-Count Register/Counter, thereby loading in a Word Count of 512. During a Continue-Swap Cycle , the Swap-Unit-and Instruction Registers (SWUNI) pulse is inhibited by the reset output of the Continue flip flop (CONF*). This causes the continuation of the

initial instruction operation, since the initial instruction swapped into the Functional Instruction Register continues to be decoded. The inhibition of SWUNI also causes the unit selected by the initial instruction to continue to be selected.

(d) Swap Count 4 This decode produces the Swap-Word-Count (SWWC) pulse just as in an Initial-Instruction-Swap-Cycle. However, in the case of Continue, the Word-Count Counter/Register has been loaded to a Word-Count of 512 by the TSU, itself. This 512 count is then swapped by the SWWC pulse into the Functional Word-Count Counter/Register.

(e) Swap Count 5 During a Continue-Swap-Cycle, the Swap-Central-Memory (SWCMA) pulse is produced just as in the case of initial instruction cycles. However, in the case of Continue, SWCMA is meaningless except when considered in conjunction with another pulse generated at Swap Count 6, referred to as Double-Swap-of-Memory-Address (DSWCMA). The discussion of SWCMA during Continue is deferred until the subparagraph dedicated to Swap-Count 6. Also during Swap Count 5, the Set-New-Unit Number (SET NUN) pulse is generated if the Unit selected differs from the Unit selection still in the Functional Register from the Initial-Instruction-Cycle.

NOTE

As previously mentioned this pulse should not be produced during Continue, since T2NEWU should never be raised.

(f) Swap Count 6 During a Continue-Swap-Cycle this decode produces the Double Swap of Central Memory Address (DSWCMA) pulse. The SWCMA pulse produced by Swap Count 5 during Continue, swaps the Central Memory Address stored in the address portion of the Store/Fetch Request Generators of the Drum and Disk TSU's into the Holding CMA Register. This address will be updated from the Starting Central Memory Address, which was swapped into the Functional CMA Register on the Initial-Instruction-Cycle, as a result of each successful Fetch or Store request made during the preceding Record. The Continue instruction requires that the next Fetch or Store in the Record enabled by the Continue instruction be sequential to the last Address stored or fetched in the Record preceding the Continue Record. This being the case, the DSWCMA pulse swaps the last Central Memory Address fetched or stored now in the Holding Register, as a consequence of SWCMA, back into the Functional CMA Register.

1 Disk Double Swap In a Disk TSU, the SWCMA loads the Functional CMA Register from the Holding CMA Register (Sheets 3-7 Dwg 700903). However, SWCMA does not swap the contents

of the Functional CMA back into the Holding CMA Register. To understand what does take place, refer to Sheet 2, extreme right, Dwg 700903. The Buffer Register shown there copies the output of the Functional CMA Register. To begin with, when the Functional CMA is loaded from the Holding CMA Register by the SWCMA pulse during an instruction cycle, the Functional CMA Register output, in turn is loaded into the Buffer Register by the LDRQAD pulse which is produced at Swap Count 7 of any Swap-Counter-Cycle. Then, when the Functional CMA Register increments with each request acknowledgement from Central Memory (HAK), the Buffer Register copies the incremented output of the CMA about 120 nano-seconds later. The incrementing pulse for the CMA Register (INCCMA) is produced by logic on Sheet 8, extreme left, Dwg 700903. The incrementing pulse for the Buffer Register is T2RF4, operating under mnemonic LDBH (Sheet 2 Dwg 700903). The logic for generation of T2RF4 is on Sheet 14, upper middle, Dwg 700903. Now, when SWCMA operates, during the Continue-Swap-Counter-Cycle, the output of the Buffer Register (T2BHØØ-T2BH18) (Sheet 2, extreme right, Dwg 700903) is the same as that of the Functional CMA and it is the T2BHØØ-T2BH18 output which is loaded into the Holding CMA Register with the SWCMA pulse (Sheets 3-7,Dwg 700903). The DSWCMA pulse in the case of the Disk TSU simply repeats the CMA-Swap-sequence and the Central Memory Address originally contained in the Functional CMA Register and the Buffer Register is restored to the Functional CMA Register by the DSWCMA pulse and the LDRQAD pulse produced at Swap Count 7 copies the output

of the CMA Functional Register back into the Buffer Register.

2 Drum Double Swap In a Drum TSU the SWCMA pulse occurring during a Continue-Swap-Counter-Cycle loads the output of the Memory Address portion of the Drum Fetch/Store Generator into the CMA Holding Register (Sheets 29-32 Dwg 700903). For a review of the Drum Request Generation scheme, read subparagraph 2-4-2-2 (e)2 Drum. The Drum Fetch/Store Generator consists of the B-Register discussed in the just referenced subparagraph and the three LSB independent stages identified by mnemonics (HRQAD15-HRQAD17)(Sheet 29 Dwg 700903). The Central Memory Address in the Fetch/Store Generator represents the next sequential Central Memory Address for fetching or storing in the record which follows the Continue instruction. This address, of course must be loaded back into the Memory Address portion of the Prefetch Request Generator, the Warning Request Generator and the Fetch/Store Request Generator. The DSWCMA pulse loads this next sequential Central Memory Address now stored in the Holding Register; back into the Functional CMA Register. This is of particular significance since the Functional CMA Register is also the Memory Address portion of the Prefetch Request Generator. At the beginning of the Continue-Swap-Counter-Cycle, the Prefetch Request Generator is addressing as much as six double-word addresses ahead of the Fetch/Store generator, but after the SWCMA and DSWCMA pulses have operated the CMA portion of the Prefetch Generator (CMA Functional Register) is at the next

sequential Central Memory address after that address from or to which a word was actually fetched or stored at the end of the record preceding the Continue instruction. The next Swap-Counter-Cycle , Swap Count 7, produces the LDRQAD pulse, which copies the Central Memory address in the Functional CMA into the B Register and the independent LSB stages of the Warning and Fetch/Store Generators.

(g) Swap Count 7 This decode produces the LDRQAD pulse discussed in the preceding subparagraph, and the Swap-Class-Ø (SWCLØ) pulse, which swaps the contents of the Functional and Holding Class Ø Control Register, except when the Continue instruction is for the continuation of a Write Data and Class (WR) operation, in which case the SWCLØ pulse is inhibited, and the Class Ø Word loaded on the initial instruction Swap-Cycle, remains in the Functional Class Ø Register to be written at Class time , into the Record following the Continue instruction. Swap-Count 7 also produces the XTA pulse if the Continue operation is a Disk Policy instruction (DMPOL*) on a Disk Unit. For details refer to paragraph 2-4-1-3 (g) 1,2.

(h) Swap Count 8 This decode produces the Swap Class 1 (SWCL1) pulse, which swaps the contents of the Functional and Holding Class 1 Control Register, except when the Continue instructions is for the continuation of a Write Data and Class (WR) operation, in which case the SWCL1 pulse is

inhibited and the Class 1 Word loaded during the initial instruction Swap-Cycle remains in the Functional Class 1 Register to be written during Class time, into the Record following the Continue instruction. Swap Count 8 also produces a Reset-Swap (RSWP) signal, which is used as a K-enable for the Swap flip flop and a J-enable for the End-of-Swap indicator flip flop (Sheet 28 Dwg 700903). RSWP also enables reset of the Continue Slip flop.

(i) Swap Count 9 This Swap-Counter decode operates for transfer Continue operations just as described in paragraph 2-4-2-2 (i).

2-4-6-5 Performance of Continue Instruction After the Continue-Swap-Cycle is completed the Drum or Disk TSU operates exactly as if the instruction being continued were an initial instruction. Sub-Fields and Data-Field are handled the same way as in an initial instruction.

2-4-6-6 End-Of-Operation Continue-Operation Swap-Cycle When no new instruction has been received during the execution of a Continue instruction, an End-Of-Operation Swap-Cycle is produced which generates the swapping pulses required for the particular function being continued. Continue is not a qualifier in the End-Of-Operation Swap-Cycle, since the Continue flip flop was reset at the end of the Swap-Cycle in which the Continue instruction was received.

2-6 STATUS REPORTING

The AMTU monitors itself for its performance of the Device Address function and the data transfer function. It also provides two special AMCP/AMTU communication status monitoring functions. The Drum has a total of eight status indicators, while the Disk File has a total of eleven status indicators for performing the status reporting function. The continuing discussion will describe each status indicator separately.

2-6-1 Header-Word-Not-Equal (HWNE) This status function pertains to Disk-type TSU's, only. The generation of HWNE is discussed in detail in paragraph 2-4-2-14 (d). HWNE signifies that the command Device Address loaded into the Device Address Holding Register during the load sequence and swapped into the Device Address Functional Register during an instruction Swap-Cycle, does not compare with the actual head-boom position as read from the prerecorded Disk header fields. The SHWNE pulse which latches the HWNE indicator flip flop (Sheet 12, right side, Dwg 700903) also sets the SWPRQ flip flop (Sheet 8 Dwg 700903). It should be noted that HWNE is not latched until after Track Verification (TV) is effected. The first EORP after HWNE rises generates a swap-cycle in which the HWNE status condition will be loaded into the Status Register in bit position 13 (Sheet 9 Dwg 700903). The actual load pulse generated by the swap-cycle is LDST. The next count in the swap-cycle clears the HWNE indicator flip flop This clear pulse is given mnemonic CLERR. Once in the Status

HWNE reacts EQ, thereby inhibiting the Disk-File Central Memory Request logic.

Register this status condition is available [illegible] in bit 13 position on the input buss to [illegible] the AMCP. The AMCP must generate an ACTC in which the Status Register is selected and then follow with an RDPC [illegible] which causes the input buss to the AMCP to be read by the AMCP.

2-6-2 Device Parity Error (DPE) This status function pertains to Disk-type TSU's, only. The generation of T2DPE is [illegible] discussed in detail in paragraph 2-4-3-15 (d). T2DPE signifies that the parity of a given data word or Check Field word, as written, does not agree with the parity [illegible] for that same word as checked on playback. At the end of the record in which T2DPE is detected, a swap-cycle begins, not as a function of thhis error, but as a result of a SWPRQ signal generated at EQSTRB time as a result of effecting starting address in a Disk-Policy instruction as signified by the gating of RCE, TV, and DMPOL*, or by DMPOL only, in a Drum Policy instruction (Sheet 8 Dwg 700903). The LDST pulse generated at Swap-Count-1 loads the T2DPE output of the indicator flip flop into bit-position 14 of the Status [illegible] Register (Sheet 9 Dwg 700903). Swap-Count 2 in the Swap-Cycle, clears the T2DPE indicator flip flop, under mnemonic CLERR. Once in the [illegible] Status Register, [illegible] the AMCP can select the Status Register with an ACTC and can read the output with [illegible] an RDPC.

2-6-3 Class Not Equal (CNE) This status function pertains to Disk-type TSU's, only. The generation of T2CNE is discussed in detail in paragraph 2-4-4-9(a). T2CNE signifies that the Class-Word received as part of an instruction does not match the Class Word written in the record addressed by the instruction. T2CNE is only generated if the transfer to follow is a Write Class-If Class-Compare operation. When T2CNE is produced it holds off the Write amplifiers in the R/W/S of the Disk File and thereby prevents overwriting of a class-protected sector. T2CNE also lowers EQ, thereby inhibiting the Disk Central-Memory Request logic. At the end of the record in which T2CNE is detected, a Swap-Cycle begins as a function of effecting starting address in a Disk-Policy instruction as signified by the gating of RCE, TV, and DMPOL*, or by DMPOL,only, in a Drum Policy instruction (Sheet 8 Dwg 700903). The LDST pulse loads the output of the T2CNE flip flop into bit-position 15 of the Status Register (Sheet 9 Dwg 700903) and thereby becomes available to the AMCP.

2-6-4 Excessive Time Consumed (ETC) This status function pertains to Disk Policy instructions for Disk and Drum Units, alike.

(a) Drum ETC When a Disk-Policy instruction load sequence ends, the Busy (BSY) flip flop sets (Sheet 28, lower right, Dwg 700903). This releases the ETC counter for the counting of ETCCLK pulses(Sheet 28, extreme right, Dwg 700903). BSY

is identifed in the logic by continuity symbol B8. The ETCCLK is produced by a Position Counter decode (Sheet 27 Dwg 700903). If the ETC counter operates until the last stage and first stage are set, the counter locks up and produces the Excessive-Time-Consumed (ETC) status condition. ETC represents approximately three Drum revolutions. Normally, the Drum will have found the starting address loaded into the Device Address Register during the load instruction, long before the ETC signal is produced. Finding the starting address produces EQ, which resets the ETC counter and holds it off. At the end of an operation when EQ drops BSY resetting holds the ETC counter off.

(b) Disk (ETC) When an instruction sequence ends the BSY flip flop sets, releasing the ETC counter (Sheet 8 Dwg 700903). BSY is identified by continuity symbol B8 in the logic. However, if the instruction involved positioning to a new track position TV will be reset and the ETC counter will be held off until TV is set again. TV is identified by continuity symbol A7 in the logic on Sheet 8 Dwg 700903. Once TV is produced, the Disk ETC counter counts Nine Disk revolutions to produce ETC if EQ is not generated first.

(c) Drum and Disk ETC ETC is only produced when EQ is not achieved within a specified time. Failure to

X

produce EQ on a Disk Policy instruction is strictly a failure to produce RCE. If RCE is not produced the SWPRQ signal is not produced and no Swap-Cycle is initiated. When ETC is produced the SWPRQ flip flop is set. Gating is ETC and DMPOL* (Sheet 8 XXXXXXXXXX,Disk, and Sheet 27,Drum, left side, Dwg 700903).

NOTE

If the instruction is Drum Policy, failure to achieve RCE in the following sector produces the Drum-Policy-Violation (DPV) status signal and the ETC counter is reset and held off by the resetting of BSY.

Swap-count 1 in the Swap-Cycle produced by ETC generates the LDST pulse, which loads XXXXXXXXXX ETC into bit position 16 of the Status Register (Sheet 9 Disk, Sheet 28 Drum,Dwg 700903). Swap-Count 2 produces CLERR which resets the ETC counter. Once ETC is in the Status Register it becomes available for sampling by the AMCP.

2-6-5 Check-Not-Zero (CHNZ) This status function applies to both Drums and Disks.

(a) Drum CHNZ The generation of TØCHNZ is discussed in detail in paragraph 2-4-3-4 (e). TØCHNZ signifies that a longitudinal parity error has been detected, indicating that data has altered between recording and playback.

~~(b) The generation of TØCHNZ is discussed in detail~~

(b) Disk CHNZ The generation of T2CHNA is discussed in detail in paragraph 2-4-3-17. T2CHNZ indicates that data has altered between recording and play-back.

(c) Drum and Disk CHNZ If a CHNZ error is detected while bit 19 in the Instruction Register is reset, the normal procedure is to issue a Write instruction followed by a Read Instruction, to the same record, in both of which bit 19 is set, thereby disabling the cycling of Check-Code. This procedure will facilitate isolation of the cause of CHNZ to one of the six Read/Write heads serving the Disk File. At the end of the record in which CHNZ is detected, a Swap-Cycle begins, not as a function of CHNZ itself, but rather, as a result of a SWPRQ signal generated at EQSTRB time as a result of effecting starting address, as signified by the gating of RCE, and DMPOL* and in the case of Disk Units, TV also, or as a result of a DMPOL instruction modifier. When the Swap-Cycle is produced at the end of the record, Swap-Count 1 produces LDST, which is used to load CHNZ into bit-position 17 of the Status Register (Sheet 9, Disk, Sheet 21, Drum, Dwg 700903). Swap-Count 2 in the Swap-Cycle clears the CHNZ indicator flip flop under mnemonic CLERR. Once in the Status Register, the Chnz error can be read by the AMCP if desired.

2-6-6 Memory Parity Error (MPE) This status function applies to both Drum and Disk Units.

(a) Drum MPE The generation of TØMPE is discussed in detail in paragraph 2-4-2-9 (b). TØMPE signifies that parity XX of a word from Central Memory as checked in ~~Central~~ Core Memory before transmission, does not agree with the parity determination made within the Drum XXXXX TSU after the word has been received from Central Memory.

(b) Disk MPE The generation of T2MPE is discussed in detail in paragraph 2-4-2-18 (c) . T2MPE signifies that parity of a word from Central Memory as checked in ~~Central~~ Core Memory before transmission, does not agree with the parity determination made within the Disk TSU after the word has been received from Central Memory.

(c) Drum and Disk MPE At the end of the record in which MPE is detected, a Swap-Cycle begins as a result of a SWPRQ signal generated at EQSTRB time as a result of effecting starting address. In Disk-Policy operations the gating is RCE, DMPOL* and TV for Disk Units (Sheet 8 Dwg 700903) and RCE and DMPOL* for Drum Units (Sheet 28 Dwg 700903). In XXXXX Drum-Policy operations the DMPOL signal is all that is required for both Disks and Drums. When the Swap-Cycle is produced at the end of the record, Swap-Count 1 produces LDST, which loads MPE into bit position 18 of the Status Register (Sheet 9, Disk, Sheet 27, Drum, Dwg 700903). Swap-Count 2 produces CLERR, which resets the MPE indicator flip flop. Once the MPE status error has been loaded into the Status Register it is available

to the AMCP.

2-6-7 Data Late (DTL)

2-6-8 Drum-Policy Violation (DPV) This status function pertains to Drums and Disks. When bit 20 in the Instruction Register is set the Drum-Policy (DMPOL) Instruction-Modifier operates. DMPOL generates a SWPRQ signal, which produces a Swap-Cycle at the end of the record for which the DMPOL instruction is intended. At the end of the Instruction Swap-Cycle, which begins at the end of the load sequence in which the DMPOL modifier is sent, the EQSTRB pulse is produced. EQSTRB and DMPOL are gated with a third signal RCE, (Sheet 8, Disk, Sheet 29, Drum, Dwg 700903). RCE indicates that the record, under the Drum or Disk heads, matches the command starting address. Refer to paragraph 2-4-2-2 (a) 1 for a discussion of the generation of RCE. If RCE is not produced by the time EQSTRB of the Instruction Swap-Cycle is produced, the Drum-Policy-Violation (DPV) status indicator flip flop sets. The DMPOL instruction modifier generates a SWPRQ signal and at the end of the record following the Instruction Swap-Cycle in which DMPOL was loaded into the Functional Instruction Register, another Swap-Cycle begins. Swap-Count 1 (LDST) loads DPV into bit-position 20 of the Status Register making this status information available to the AMCP. Swap-Count 2 (CLERR) resets the DPV status indicator flip flop.

2-6-9 Device Not Available (DNA) This status function pertains to Drums and Disks. Any Device addressed by the AMCP during a load sequence should be ready to perform an operation. This ready status indicates that the Drum or Disk is operating at the proper speed. The ready status for each device is communicated to its TSU by a dedicated Ready line (RDYØ-RDY3) (Sheet 28, Drum, Sheet 7, Disk, Dwg 700903). Each Unit selection line produced from a decode of the output of the Unit Functional Control Register (UØ-U3) is gated with its corresponding Ready line. If the Unit selected during a load sequence is not ready the Device Not Available (DNA) indicator flip flop sets producing DNA. The detection of DNA also sets the SWPRQ flip flop and the next end-of-record pulse generates a Swap-Cycle. Swap-Count-1 (LDST) loads DNA into bit-position 21 of the Status Register, making this status information available to the AMCP. Swap-Count 2 (CLERR) resets the DPV status indicator flip flop.

2-6-10 Register Loading Violation (RLV) The RLV status function pertains to Disks and Drums. The RLV status indicator is set for either of two fault conditions associated with the Register loading sequence (refer to paragraphs 2-3-3-1 through 2-3-3-3). The first condition involves loading out of sequence. If any Control Register is loaded before the Instruction Register, the

RLV indicator is jam set. The second condition sets the RLV status indicator flip flop through its clock input, The second condition occurrs if there is an attempt to load the Holding Registers during a Swap-Cycle, or if a Register loading sequence is not completed before a Swap-Cycle begins. The logic for the RLV function is located on the upper right side of Sheet 28,Drum, and Sheet 7,Disk, Dwg 700903. The gating of signals identified by continuity symbols X10, X11, X21, X22, and C13 signify the conditions for producing RLV, when other than the Instruction Register is loaded first. The signals identified by these continuity symbols are as follows:

X10-(TSU Selection)

X11-(Enable Load Bit) This signal indicates a Register is selected for loading rather than for sampling.

X21-(Reset state of Load Sequence flip flop) The significance of the reset state of this flip flop in this gating is in that it indicates that the Instruction Register has not been loaded.

X22-(Instruction Register Select Bit) The reset state of this bit in this gate indicates that the Instruction Register is not being selected although the other signals in the gate indicate that the Instruction Register should be being selected now.

C3- (Register Selection) This signal is produced by gating ACTC the Register Selection Control level and PDS, which strobes the data lines during a Register selection.

The flip flop identified as PRECLK, located in the logic just to the left of the RLV flip flop identified as CLK is jam-set if during a Swap-Cycle (SWP) identified by continuity symbol B6, the load Sequence flip flop is set indicating the Instruction Register was loaded but a Swap-Cycle began before the Unit Register was loaded; that is to say before the end of the Load Sequence. It should be recalled that loading the Unit Register resets the Load-Sequence flip flop. Also, if the Instruction Register is selected during SWP, the PRECLK flip flop is set. Selection of the Instruction Register is signified by the gating of signals identified by continuity symbols X10, X11, X1, and X9. The signals identified by the continuity symbols are as follows:

X10-(TSU Selection)

X11-(Enable Load Bit)

X1- (ACTC level)
This is the Activate level
which selects Registers for loading.

X9- (Instruction Register Selection Bit)

The continuing discussion relates to the different End-Of-Record times at which an RLV condition is reported to the AMCP. If an RLV is caused by attempting to load any Register other than the Instruction Register first, the RLV signal generates a SWPRQ level and the End-Of-Record pulse which occurs at the end of the record during which RLV is detected generates a Swap-Cycle, and the RLV condition is reported before the record which would have been written into

RLV

been produced. If the RLV condition is a result of the Load Sequence taking place during a Swap-Cycle, it is evident the End-Of-Record pulse preceding the record which would have been written into or read from had no error occurred, is the End-Of Record pulse which began the Swap-Cycle, producing the RLV. Therefore an RLV of this type cannot be reported until the occurrence of a second End-Of-Record pulse which will occur at the end of the record which would have been written into or from had the Load-Sequence been successful. When the Swap-Cycle generated by RLV begins, Swap-Count-1 (LDST) loads the output of the RLV flip flop into bit position 22 the Status Register for sampling by the AMCP if desired. Swap-Count-2 (CLERR) clears the RLV status indicator flip flop.

2-6-11 Present Status Read (PSR) This status function pertains to Disks and Drums. PSR is used to inform the AMCP that the Status Register of a given TSU has already been sampled by the AMCP. The logic for the PSR function is on the bottom left of Sheet 27, Drum, Sheet 9, Disk, Dwg 700903. When the LDST pulse produced at Swap Count-1 of a Swap-Cycle, operates to load the Status Register, it also resets the PSR flip flop. If the Status Register is selected by an ACTC as signified by SST being raised, ~~the output buss bit position 23 (BB23) [illegible] to the XX AMCP at a logic "0" state, indicating that status has not [illegible]~~ and ~~[illegible]~~. However, if the AMCP follows with an RDPC, the down-edge of ~~the data strobe pulse (DS3) accompanying~~ RDPC ~~and~~

[illegible] the status on the AMPL output [illegible] sets the PSR flip flop , thereby [illegible]. It should be noted that OB2 is reported on this RDPC [illegible] as a logic "0" since the strobe pulse, RDPC, which [illegible] status from [illegible] down does not set the PSR flip flop until [illegible] has taken place at which time it is no longer [illegible]ing the [illegible], however [illegible] the next RDPC at [illegible] 823 [illegible] ". OB" at a logic "1" indicates to [illegible] that [illegible] has been sampled previously [illegible] Register, the LDST pulse [illegible] PSR flip flop again.

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MOST SIGNIFICANT ⟷ LEAST SIGNIFICANT

AMCP BUS 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

CLASS Ø 0 ... 23

CLASS 1 0 ... 23

CHECK Ø 0 ... 23

CHECK 1 0 ... 23

DEVICE ADDRESS 0 1 | 2 TRACK 9 | 10 BAND 16 | 17 RECORD 23

CENTRAL MEMORY ADDRESS 5 ... 23

INSTRUCTION * 15 ... 21

MAP 5 ... 14

UNIT NUMBER 22 23

WORD COUNT 14 ... 23

POSITION COUNTER*
(Ø or 1 or 2 or 3) 3 ... 23

STATUS * 13 ... 23

REGISTER SELECT *
(ACT COMMAND) 4 ... 23

ALL UNUSED BITS WILL BE SENT TO THE AMCP AS "ONES".

* SEE AMPLIFICATION ON SHEET 2

AMCP-AMTU
BIT ASSIGNMENTS

Figure 8

FORM CP-103-ENG. POST 3348

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A3ES33 REV. B
DATE 12/10/68
SHEET 80 OF

"DECODE" STATUS (DRUM USES 17 23 ONLY INSTRUCTION

17	18	
0	0	READ
0	1	WRITE
1	0	WRITE HEADERS
1	1	WRITE IF CLASS IS EQUAL

13 DEVICE PARITY ERROR
14 HEADER NOT EQUAL
15 CLASS NOT EQUAL
16 EXCESSIVE TIME CONSUMED
17 CHECK NOT ZERO
18 MEMORY PARITY ERROR
19 DATA TRANSFER VIOLATION
20 DRUM POLICY VIOLATION
21 DEVICE NOT AVAILABLE
22 REGISTER LOADING VIOLATION
23 PRESENT STATUS READ BY AMCP

15 UNDEFINED
16 CONTINUE
17 SEE "DECODE"
18 DISABLE CHECK CODE CYCLE
19 DRUM POLICY
20 POSITION ONLY

POSITION COUNTER (BITS 3 THROUGH 11 NOT USED IN DRUM TSU)

3 TRACK VERIFIED
4 TRACK NUMBER
12 POSITION NOT VALID
13 BUSY
14 WRITE
15 RECORD NUMBER
22 POSITION WITHIN RECORD

REGISTER SELECT

3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
TSU ADDRESS		ENABLE ATTENTION	DISABLE ATTENTION	ENABLE LOAD	SELECT STATUS	SELECT CHECK WORD Ø	SELECT CHECK WORD 1	SELECT POSITION COUNTER Ø	SELECT POSITION COUNTER 1	SELECT POSITION COUNTER 2	SELECT POSITION COUNTER 3	SELECT FUNCTIONAL UNIT #	SELECT HOLDING UNIT NUMBER	SELECT CLASS WORD Ø	SELECT CLASS WORD 1	SELECT WORD COUNT ADDRESS	SELECT CENTRAL MEMORY ADDRESS	SELECT DEVICE ADDRESS	SELECT MAP	SELECT INSTRUCTION

0	0	TSU Ø (DRUM 1)
0	1	TSU 1 (DRUM 2)
1	0	TSU 2 (DISK 1)
1	1	TSU 3 (DISK 2)

A3ES3 REV. B