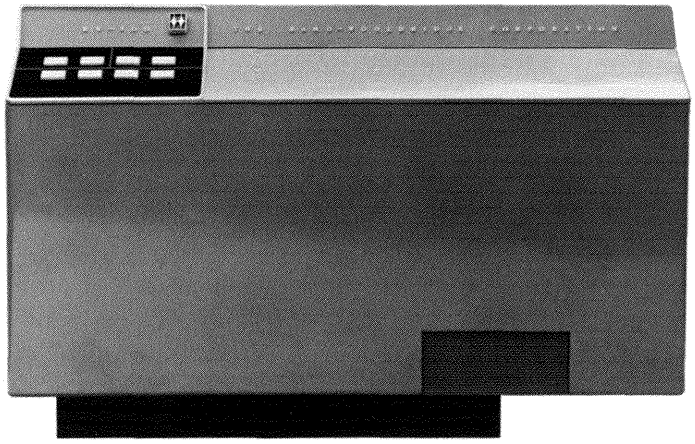
SERIAL NO. 171

RW-300 DIGITAL CONTROL COMPUTER
THEORY OF OPERATION MANUAL



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SECTION 1

GENERAL DESCRIPTION

1-1. PURPOSE.

The objective of this manual is the description of the physical and functional features of the RW-300 Digital Control Computer. General application is described in Section 1. Section 2 provides a brief review of computing system requirements and detail information on the basic circuits of the RW-300. In Section 3, the theory of operation of the RW-300 Computer is provided. This material is presented on the basis of functional groups, individually and as each contributes to processing of each instruction. Operational differences arising from differences in installations are described separately in supplementary publications, as are programming instructions. Appendix A of this manual offers a few definitions generally used in the computing field and a complete list of symbol usage within the RW-300 Computer.

1-2. SYSTEM OBJECTIVES.

The RW-300 Digital Control Computer is a magnetic drum memory, stored program computer for general application in the field of industrial automation. The system is designed principally for the real-time control of processes, and incorporates capability for data logging, test stand operation, and for scientific and engineering calculations.

Functioning principally in a closed-loop control system, the RW-300 Computer accepts continuously variable signals (analog form data) and/or discrete data such as signals from punched tape and on/off devices (digital form data). Input data is converted to a fractional binary system for storage and operation in the Computer. Reconversion to analog output form is effected to provide drive for devices controlling a process and/or for recorders.

Employed as a process controller, the RW-300 offers speed in reading and interpreting instructions and in performing complex calculations, while storing information used to modify control actions, based on changing input conditions. As a data logger, the RW-300 can record and interpret process instrument readings, scan process variables, indicate when a given limit has been exceeded, detect instrument failures, and evaluate recorded data. Similarly, in testing applications, the RW-300 Computer not only records, accumulates, and interprets measured data, but can control test operations.

To facilitate use of the RW-300 for general purpose computation, subroutines

are available for arithmetic operations, common engineering functions, and programming simplification.

To meet the objective of continuous service, the equipment is designed for maximum reliability, being almost wholly transistorized; no component operating at greater than 50 percent of its rated capacity. Only 500 watts input power is required from a 115-vac single-phase source.

1-2a. PHYSICAL FEATURES. The RW-300 Digital Control Computer is housed in a non-purgable, steel desk console, illustrated in figure 1-1. Over-all dimensions of the 645-pound basic unit are: length, 56 inches; height, 36 inches; and depth, 29 inches. For convenient installation, all side panels may be removed, reducing the length and depth each approximately three inches.

Figure 1-1. RW-300 Digital Control Computer

Connections are made to a single-phase, 60-cps, 115-volt power source, and to associated equipment through a row of connectors along the bottom of the back of the Computer.

1-2a(1). Controls. Accessible at the top left of the Computer are the principal operating controls. (Any or all of these controls may be duplicated on a remote operator's panel. See supplementary publications pertaining to the installation under consideration.) The panel is equipped with seven assemblies which are either indicator lights or push buttons with or without associated indicator lights.

Power is applied to the Computer in two discrete steps. Depressing the **POWER ON** button initially produces the standby condition, in which the drum and certain circuitry in the Computer are powered. Approximately two minutes after initial application of line voltage, the drum speed has been established. The **STANDBY** indicator turns off, the **POWER ON** indicator turns on, power is applied to the remainder of the circuitry, and the Computer is ready for operation. Depressing the **POWER OFF** button disconnects the line voltage from the entire unit.

Program control is effected, under normal operation, by the **LOAD, START, STOP,** and **RESUME** buttons. Operation of the Control panel circuitry is described in paragraph 3-7a.

Additional adjustments and facilities required for operation versatility, code checking, and self-testing, are provided by the Test and Maintenance panel, located under the top cover of the Computer. The panel includes: an oscilloscope and indicating lights for the display of the contents of registers and the condition and output of principal flip flops, marginal checking controls and indicators, digital input toggle switches, and track selector plug and sockets.

Through use of the **FETCH** and **EXECUTE** buttons, program execution may be interrupted to permit inspection of register contents. Register contents are displayed on the oscilloscope as two parallel sets of 10 digits each. Clock intensity modulation can be applied through the **CA INT MOD** switch to avoid any ambiguity of flip flop status at a given digit time. A bank of neon bulbs and selector switches comprise the **STATE INDICATORS**, displaying the status of the selected flip flops. Following program interruption, automatic high-speed operation of the Computer is resumed by depressing the **RUN** button.

One-bit digital inputs may be manually introduced on six of the input lines through the **DIGITAL INPUT** toggle switches.

Line voltage is metered, and supply voltages may be metered and/or adjusted using the meters, switches, and potentiometers at left center of the Test and Maintenance panel.

At the extreme left of the panel, a plug and series of eight jacks permit connection of the write amplifiers to one group of eight tracks in order to load programs into drum tracks not available for writing during normal program execution. Any attempt to record on a track to which the write circuits are not connected activates the RECORD ERROR light at the right of the Test and Maintenance panel.

Circuits of the Test and Maintenance panel are described in paragraph 3-7b.

1-2a(2). Internal Construction. Figure 1-2 illustrates the major functional assemblies in the RW-300.

The central storage drum is mounted to the left center of the front of the Computer. Conventional chassis construction and vacuum tube circuitry is used in the power supply and clock generator, shown in the lower part of figure 1-2. The balance of the Computer has been designed around modular construction techniques.

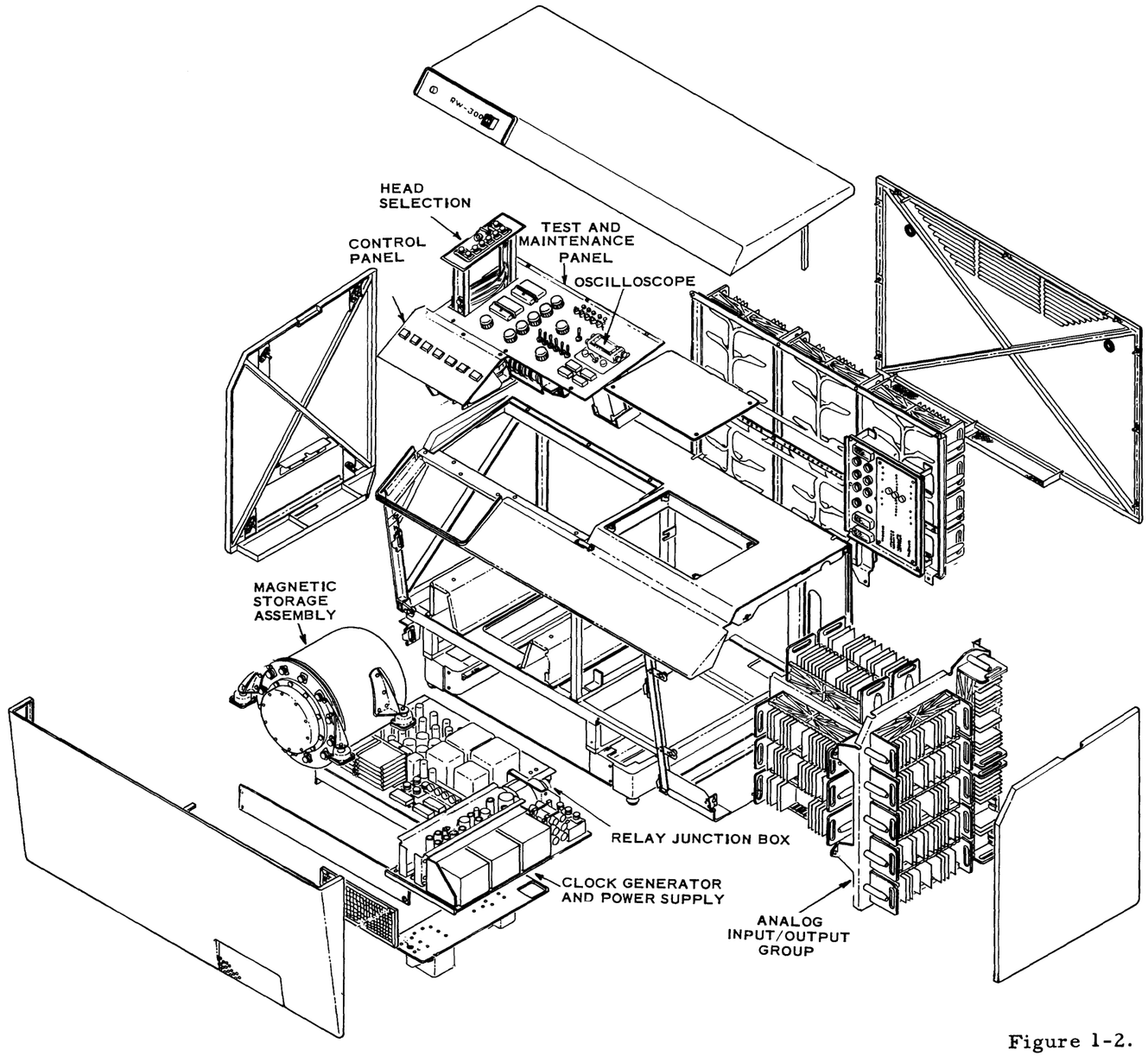


Figure 1-2. Major Assemblies of the RW-300

A typical module is illustrated in figure 1-3. The module frame is molded of high impact styrene with a handle slot in each end piece for convenience in installation and removal of the module from the supporting frame. Grooves on the inside surfaces of the side pieces support the insert cards. On the bottom of the module frame is a micaply board bearing components interconnected by etched wiring. The etched wiring terminates on molded tabs that plug into jacks mounted on the subassembly frames. Inter-module cabling is conventional.

While of a standard size and design, each module is actually an individual unit. However, the modular construction technique is more correctly represented by the insert cards bearing particular circuits which, by variation of input signals, can be used in more than one module.

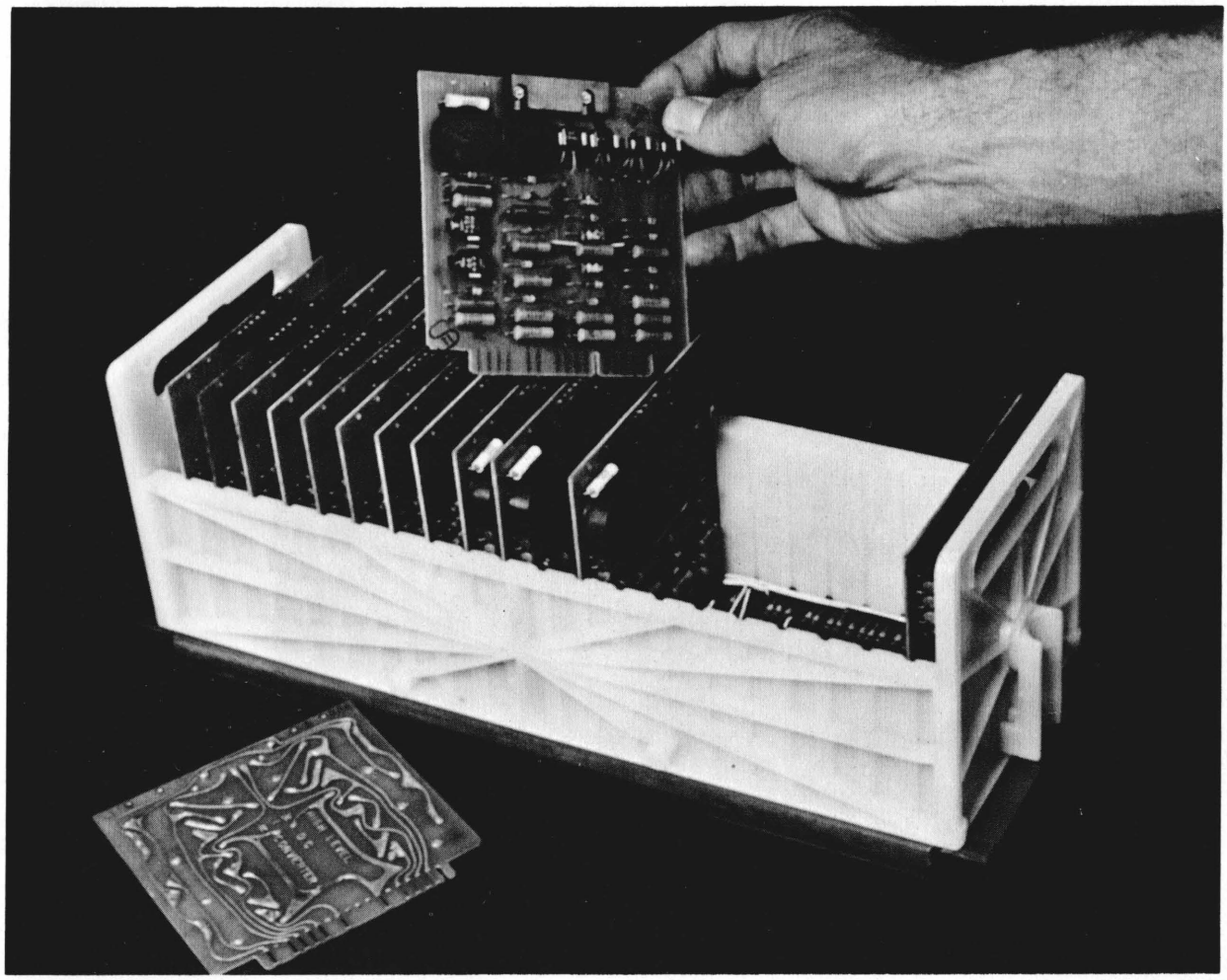


Figure 1-3. Typical RW-300 Module with Insert Card

Fabrication of the insert cards is essentially identical to that of the module boards, as already described. Figure 1-4 provides a detailed view of both sides of a typical card. A connector mounted at the top of the components side of each board provides test points for convenience in testing. The card plugs into a jack on the module board by means of the tab on which the wiring extends. Cards are approximately four and one-quarter inches square.

As indicated in figure 1-4, subminiaturized circuit components combine with semi-conductors to require minimum equipment space. However, for maximum reliability, components are operated well below nominal ratings. The extensive use of semi-conductors prevents undesirable heat generation, thereby avoiding any need for special air conditioning.

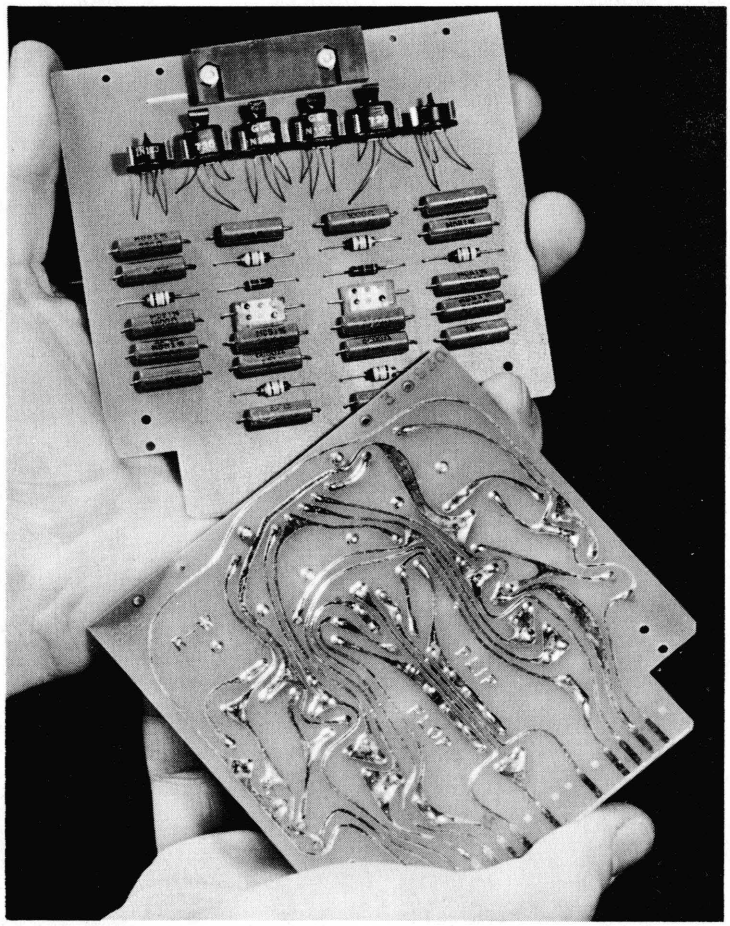


Figure 1-4. Typical Insert Card.

1-2b. FUNCTIONAL FEATURES. The binary computation resulting in process control or in recorded data is accomplished in the arithmetic and control portions of the RW-300 Computer in association with the central storage functions. Conversion of analog data to digital and vice versa is also provided by circuits which can be mounted within the Computer. The signals converted and/or used for computation are supplied by digital or analog equipment external to the Computer.

1-2b(1). External Equipment. RW-300 Computer circuitry permits selection from 540 one-bit digital and 1024 analog input sources and driving 540 one-or 18-bit digital and 36 analog output loads. The Computer can be programmed to generate gating signals selecting the correct group of inputs or outputs.

In an expanded system, digital information may be entered on any of the 30 groups of 18 parallel input lines specified by the program; analog information on one of 4, 8, 16, or 32 groups of 32 parallel input lines each. In addition to two groups of output lines normally reserved for use with typing and/or punching equipment, 30 groups of 18 parallel output lines can be made available in an expanded system. Analog outputs are presented in groups of 12.

Commonly, the digital information is generated by a Flexowriter or similar punched tape reading device, with a speed of approximately 10 characters per second. Each character is represented by a series of holes and spaces in a frame on the tape. Sensing devices in the input equipment present a signal on the corresponding line into the Computer when a hole is sensed. Thus, regardless of whether the holes in a frame represent a decimal digit or some alphabetic or symbolic character, the Computer recognizes the presence or absence of a signal on each of the input lines. Sampling these signals serially, the Computer can store all or as many as instructed by the program. The process is reversed for read-out. The Computer incorporates a delay circuit preventing execution of a digital command prior to completion of the previous digital command.

Lines not required for parallel communication to Flexowriters, typewriters, card readers, or similar equipment can be used to communicate with auxiliary signalling devices. One of the one-bit output lines is used to turn the Flexowriter on and off. The number of input lines of the selected group shifted into the Computer can be limited by program specification, in digits 14 through 18 of the first word of the digital command.

Signals required to actuate printing or punching of the desired character are shifted serially from the A register into an output buffer register for parallel transfer to and/or control of external equipment.

Analog inputs and outputs are not under program control but are established for a particular installation. When relays are used to sample from groups of 32 inputs, the analog input/output circuitry is provided with an automatic counting sequence for such sampling. Inputs are sampled and stored at least once every 8.5 seconds. Outputs are adjusted every 16.7 ms except during the drum revolution in which inputs are sampled. An output can be adjusted from zero to full scale in two seconds.

1-2b(2). Internal Operation. The RW-300 operates internally on binary digits called bits (see paragraph 2-1). Control signals and arithmetic results are generated and used in binary form. Input equipment therefore presents data and program information in binary form, and analog equipment transforms analog data to binary form. Program, necessary constants, and binary data are stored on the central magnetic drum, nine inches in diameter and nine inches long.

The drum is equipped with recording and play-back heads which write and read in a series of tracks. The length of the drum track is magnetized to represent the desired binary pattern, by the magnetic flux produced as recording current passes through the recording head.

Each track accommodates 128 equal sectors, each of which is a Computer word of 20 bits length. The surface of the drum thus offers storage space, in the 63 general storage tracks, for approximately 8000 Computer words. Average access time of general storage is 8.3 ms. Tracks and sectors are numbered; the sector number being recorded in the first seven bits of each sector on the sector number track.

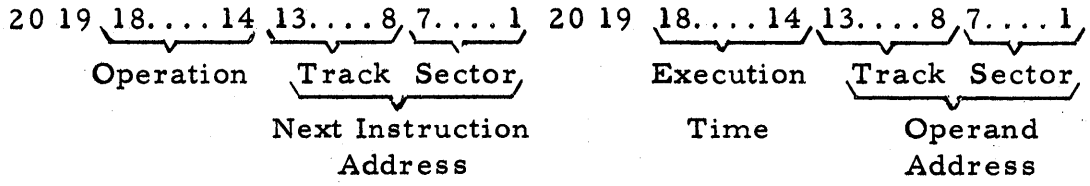
Words stored in tracks 0 through 7 may be modified under program control since writing heads are provided on these tracks. The routine for program loading is stored in track 63. Loss of the loading routine through an attempt to write into this track (when the track selector plug is connected to the tracks 56-61 group) is prevented by circuitry which suspends program execution and illuminates a RECORD ERROR light.

Track 62 is equipped with a write head providing circulation of the same group of 16 words, for fast access (approximately one millisecond) in optimizing a program. Information appearing at the read head is simultaneously recorded in a sector 16 words farther along the track. Five one-word circulating register tracks are provided, each equipped with recording and play-back heads (mounted in a single package for each track) which record in the next successive sector the information passing under the read head. Circulating data can be modified under program control and/or automatically in the process of instruction execution.

Data converted to digital form by the analog input/output circuitry is stored in track 8 (or sequentially in tracks 8 through 15, as required in a given installation) from which it is read by the digital portions of the Computer for arithmetic and control use. Digital data and digital form process control signals generated by the arithmetic and control portions of the Computer for use by the analog portion are stored in track 7. The analog data is read by a separate head from track 7 into the analog converter, under control of the analog portion of the Computer.

Analog data conversion is based on a current weighting/digit sampling technique to establish the digital equivalent of input signals. A stablization loop corrects any error due to circuit drift; while a sampling loop prevents control signal outputs from exceeding the value specified by the digital data, and the digital data from exceeding the value specified by the input signals.

Computer words bearing data consist of 17 magnitude digits, a sign bit, and two space bits. The space bits provide time to turn writing circuits on prior to the appearance of the first bit to be recorded and to turn off these circuits after the last (sign) bit has been recorded. An instruction utilizes two adjacent words, only the first of which is specified in the program. Digit use is shown below. Digit 1 is the least significant digit and appears at the read head first.



In addition to the controls effected by front panel buttons, the RW-300 recognizes and performs commands for arithmetic manipulation; "logical" addition and multiplication -- permitting modification of selected bits within either data or instruction sectors; shifting; magnitude comparison; register contents switching; communication with external digital equipment; program branching; and stop. The 19 individual operations recognized are described briefly in the following paragraphs. Typical contents of principal registers upon completion of certain operations are shown in figure 1-5.

For arithmetic addition, the contents of the A register (the accumulator) are added to the contents of the required drum storage location called (m). The sign of the A register is determined by the signs and magnitudes of (A) and (m). Occurrence of an overflow is sensed internally and the overflow information is stored (in Z2) pending an instruction to transfer on overflow.

In subtraction, the contents of the drum storage location are subtracted from

the contents of the A register by an "add complement" technique. The digit carried out of the sign bit controls completion of the subtraction to change accumulator sign, if necessary, and may be stored as an overflow as in an addition.

Multiplication, in which (A) are multiplied by (m), employs a shifting and adding process. The most significant digits of the product are stored in the A register. The double-length product developed by two 17-bit numbers utilizes the B register, for storage of the least significant digits. The execution time specified in the first word of a multiply instruction determines the number of significant digits. There is no round off.

(A) are divided by (m) by a "shifting and adding complement" process when the divide command is given. The quotient is stored in the A register and the remainder in the B register. The Computer tests for a dividend larger than the divisor and actuates the overflow circuit. The execution time specifies the number of quotient digits plus the test digit time.

Either A or B registers may be loaded from storage, with (m) recorded in the selected circulating register. The A register may be loaded with (-m), if desired.

In commands to store either A or B register, (A) or (B) may be recorded in the desired drum location.

The registers may be shifted; either (A) shifting right or left the number of digits specified by the execution time digits, or both A and B registers shifting simultaneously left the number of digits specified by the execution time digits. In all shifts, the signs of the registers remain the same. Ones shifted left from digit 17 of the A register actuate the overflow circuit. The most significant operand track digits specify the type of shift to be accomplished.

	(m)	Z2	(A)	(B)
ORIGINAL CONTENTS	+01110	0	+10101	+11101
ADD	+01110	1	+00011	+11101
SUBTRACT	+01110	1	+00111	+11101
MULTIPLY	+01110	0	+01001	+00110
DIVIDE	+01110	0	+00001	+10000
LOAD A	+01110	0	+01110	+11101
LOAD B	+01110	0	+10101	+01110
LOAD A NEGATIVE	+01110	0	-01110	+11101
STORE A	+10101	0	+10101	+11101
STORE B	+11101	0	+10101	+11101
SHIFT				
A right 3	+01110	0	+00010	+11101
A left 2	+01110	1	+10100	+11101
AB left 4	+01110	1	+11110	+10000
MERGE	+01110	0	+11111	+11101
EXTRACT	+01110	0	+00100	+11101
COMPARE MAGNITUDE	+01110	0	+00111	+10101
SWITCH				
A→B	+01110	0	+10101	+10101
B→A	+01110	0	+11101	+11101
A↔B	+01110	0	+11101	+10101

NOTE: The sign of the contents is stored as a binary digit; 0 representing plus and 1 representing minus. Registers actually contain 17 magnitude digits and the sign digit. Z2 is the overflow indicator.

Figure 1-5. Typical Contents of Principal Registers.

A and B registers may be cleared (filled with zeros) through use of the shift command.

By transfers on zeros in the A register, on a negative sign in the A register, and on overflow, conditional branching of the program may be effected. Transfer results in obtaining the next instruction from the address specified as the operand address of the transfer instruction.

The logical operators -- "and" and "or" -- are included, in the extract and merge instructions, which form the logical product and sum, respectively, of (A) and (m). The result appears in the A register in both cases.

In the compare magnitude instruction, (m) is subtracted from (A). When (m) are greater than (A), the execution time digits are added to the digits of the next instruction sector, offering program branching at the option of the programmer. The result remains in the A register, however, for any desired processing as data. The original (A) are copied into the B register, and are therefore also available for further processing.

Switching instructions permit copying of (A) into the B register and (B) into the A register, either without disturbing the original data or as a complete exchange of data. The two most significant digits of the operand track number specify the type of switch.

Digital communication is specified by the combination of the operation code digits and the operand address. Inputs or outputs of 18 one-bit combinations or combinations involving six- or eight- bit Flexowriter inputs, as described in paragraph 1-2b(1), can be selected by the digits of the operand address. The A register accepts input digits from a "parallel to serial" circuit and presents output digits to the output buffer register.

The Computer is placed in an idling mode by the stop instruction.

SECTION II

ESSENTIALS OF RW-300 CIRCUITRY

2-1. COMPUTING SYSTEM REQUIREMENTS.

To orient the technician who may have limited knowledge of automatic digital computers, a review of the basic operational concepts and tools is provided in this paragraph. (See also definitions in Appendix A.) The reader already familiar with the general subject may turn directly to the descriptions of the basic circuits of the RW-300 beginning in paragraph 2-2.

The RW-300 is an automatic digital control computer. A computer is a person or device which computes. To be capable of computing, the computer (whether human or machine) must accept input data, must store such data as required, must perform arithmetic operations on the data, and must present the results as output data. Control of each of these functions must also be a computer capability. Primarily, control may be considered implicit in each action. However, input data may contain control information which may require immediate compliance or may require storage for action conditional on other inputs, outputs, or computations. Therefore, a block diagram of general computer capabilities can be shown as in figure 2-1. Signal paths are solid lines and control paths are dashed lines.

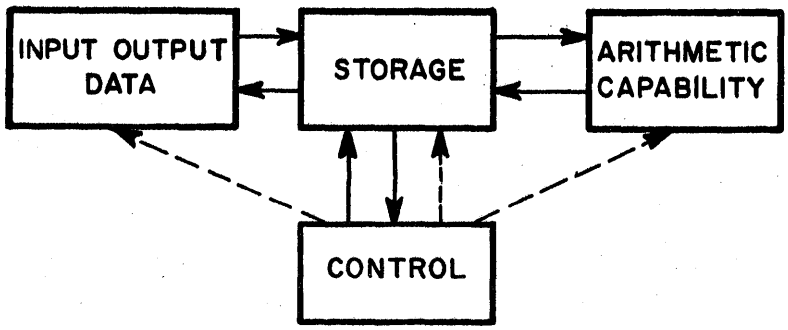


Figure 2-1. General Computer Functions, Block Diagram

An automatic computer is a device capable of performing a sequence of arithmetic operations continuously, without intervention by an operator. Applied to process control, such a computer accepts information on certain process conditions, performs desired computations based on the variations in these conditions, and generates output signals capable of controlling the process inputs and/or conditions within the process. Computers may employ magnetized or photosensitive tapes, disks, or cylinders; punched cards or tape; cathode ray tube faces; or, electrical or acoustic delay lines for program storage. The RW-300 utilizes a magnetic storage drum.

A digital computer performs the required operations internally using discrete numbers. Based on an alternate principle, an analog computer performs arithmetic functions on continuously variable physical quantities. For example, navigation equipment receiving a signal of continuously varying amplitude from its rotating antenna, and receiving samples indicating wind direction and velocity from other electromechanical devices, may be considered an analog computer generating the heading correction signal. Severe computation precision problems can exist in an analog computer designed to compute accurately several quantities, each of which might vary between different limits.

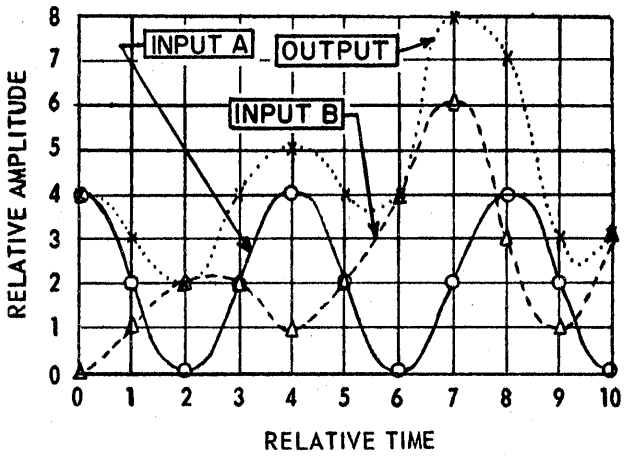
As in manual arithmetic computation, in an automatic digital computer the precision of computation is limited only by the number of significant digits in the input data and the space available for digital manipulation (i.e., manually, the size of the paper; automatically, the word size for which the computer is equipped). Since input data in a process control is analog in nature, the RW-300 can be equipped with special analog input/output conversion facilities, transforming such information to the digital form required for internal computation by the machine.

Analog inputs may be graphed as a continuous function with respect to time as illustrated in the hypothetical example in figure 2-2a. Assume that some input data is varying sinusoidally (represented by solid-line A) while a second input varying randomly (represented by dashed-line B) is effectively modifying the system output (represented as the sum of the input functions by the dotted line). The data may be tabulated as the amplitude of each input and the resultant output at arbitrary times, as indicated in figure 2-2b. The same data will be used to illustrate digital information handling.

A digital computer may operate on the decimal system, such as is usually employed in longhand computation. While not requiring a sensitivity to continuous change in a quantity, such a system must provide a sensitivity to 10 discrete conditions. Circuitry sensing and accurately reproducing one of a set of 10 discrete conditions suffers from reliability problems nearly as severe as those of

an analog machine.

Reducing recognition requirements to the minimum would result in a system in which all data is expressed in terms of on/off conditions, or as a set of binary digits.



a. Data Graphed as Continuous Functions

TIME	INPUT A	INPUT B	OUTPUT
0	4	0	4
1	2	1	3
2	0	2	2
3	2	2	4
4	4	1	5
5	2	2	4
6	0	4	4
7	2	6	8
8	4	3	7
9	2	1	3
10	0	3	3

b. Data Tabulated

Figure 2-2. Graphic Example
Of Analog Functions

2-1a. BINARY NOTATION AND MANIPULATION. Representation of a value in binary form may be understood by a simple analysis of decimal representation. A decimal digit may be considered the multiplying factor for some power of 10, and a

series of such digits is the sum of the product of each factor and its power of 10. For example, the decimal number 273 is 200 + 70 + 3, or $(2 \times 10^2) + (7 \times 10^1) + (3 \times 10^0)$. Similarly, a binary number is a series of digits representing the factors by which each power of two is to be multiplied. The binary number 111 010 represents $(1 \times 2^5) + (1 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (0 \times 2^0)$. Expressed as a decimal number, 111 010 is (32) + (16) + (8) + (0) + (2) + (0), or 58. Decimal and binary representations of the powers of two are provided in figure 2-4, while the binary equivalents of decimal numbers 1 through 7 are listed in figure 2-5. As an illustration, the data tabulated in figure 2-2b has been converted to binary form as shown in figure 2-3.

TIME	INPUT A	INPUT B	OUTPUT
0	100	000	100
1	010	001	011
2	000	010	010
3	010	010	100
4	100	001	101
5	010	010	100
6	000	100	100
7	010	110	1000
8	100	011	111
9	010	001	011
10	000	011	011

Figure 2-3. Binary Representation of Data Tabulated In Figure 2-2b

In order to operate on information originally in decimal form, the Computer must accomplish transformation to binary form. While this is automatic in the system, the representation, which the technician must recognize, can be obtained manually by successively subtracting from the decimal number the highest power of two contained, until a remainder of one (2^0) is reached. Expressed as a binary number, the decimal number 29 therefore becomes $(29-2^4) + (13-2^3) + (5-2^2) + (1)$, or $(1 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$ which is 11 101.

A second representation system, used by some external equipment supplying information to the Computer, is based on powers of eight. Called the octal form, a number so represented can be transformed to a binary number merely by substituting for the octal digits the binary equivalents (see figure 2-5). For example, the decimal number 123 can be represented in octal form as $(1 \times 8^2) + (7 \times 8^1) + (3 \times 8^0)$, or 173. In binary form, the decimal number 123 becomes $(1 \times 2^6) + (1 \times 2^5) + (1 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (1 \times 2^0)$, or 1 111 011. Referring to the table listing binary equivalents of decimal digits

2^n BINARY	2^n DECIMAL	n	2^{-n} DECIMAL	2^{-n} BINARY
1	1	0	1.0	1.0
10	2	1	0.5	0.1
100	4	2	0.25	0.01
1 000	8	3	0.125	0.001
10 000	16	4	0.062 5	0.000 1
100 000	32	5	0.031 25	0.000 01
1 000 000	64	6	0.015 625	0.000 001
10 000 000	128	7	0.007 812 5	0.000 000 1
100 000 000	256	8	0.003 906 25	0.000 000 01
1 000 000 000	512	9	0.001 953 125	0.000 000 001
10 000 000 000	1 024	10	0.000 976 562 5	0.000 000 000 1

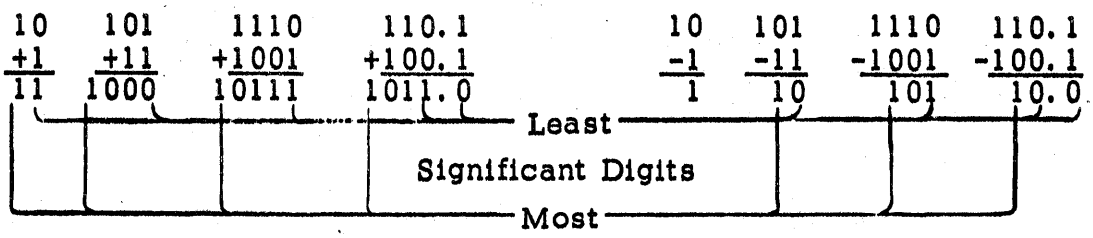
Figure 2-4. Powers of Two

Decimal Digit	Binary Number
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 2-5. Binary Equivalents Of Decimal Digits

and reading the first digit as 001, the binary number can be read directly in octal form and, similarly, an octal number can be read directly as a binary.

Arithmetic manipulation of binary numbers is essentially the same as that of decimal numbers. (Arithmetic manipulation of octal numbers is also similar. However, since such numbers are automatically transformed to binary form by the machine prior to arithmetic functions, no examples of the operation are provided here.) When operating to the base two, 1 + 0 = 1 and 1 - 0 = 1; while, 1 + 1 is represented as 10 or 0 with 1 carried, and 0 - 1 is 1 with 1 borrowed. The least significant digit (that adjacent to the point indicating the change to negative powers of the base) of numbers of more than one digit is added or subtracted first. Some examples are given below. (See also figure 2-3, demonstrating that binary addition of the inputs produces the output.)



An alternate technique for obtaining the difference between two values requires conversion of one of the values to a complement, addition of the complement to the second value, and subtraction of the complement base. Using the decimal form, the method can be illustrated as follows: 29-18 = 11. The complement of 18 is 100 - 18, or 82. 29 + 82 = 111. 111 - 100 = 11. Because producing the complement of a decimal number itself requires subtraction, the complement technique is not considered practical for the decimal form. The technique is widely used in binary computation, since the circuitry employed in electronic computers generates the complement form automatically.

In multiplying binary digits, (1 x 0) = 0, (0 x 0) = 0, and (1 x 1) = 1. In dividing, (1 ÷ 1) = 1 and (0 ÷ 1) = 0. As in the decimal system, division by 0 is undefined. Longhand multiplication and division are the same as in the decimal system, actually a series of additions or subtractions, respectively, and the digital computer performs these operations on a "shift and add" or "shift and add complement" basis.

The arithmetic operations described require circuitry capable of two basic functions: adding and storing. The addition of 1 and 1 requires at least temporary storage of the "carried" digit. The "logic" of an automatic digital computer is therefore concerned with (one-bit) addition and storage operations, which can be extended beyond arithmetic computation into computation control.

2-1b. **LOGICAL ELEMENTS.** Commonly, the temporary one-bit storage needed for the arithmetic operations can be effected in an automatic computer by setting the contacts on relays or changing the states of bi-stable multivibrators. Addition can be accomplished by sampling at some specified instant the state of each of two such storage circuits and using the sample to set the state of two additional circuits, one of which is functioning as an adder and the other as a carried-digit storage.

For example, consider the "on" output of the circuit as a binary 1 and the "off" condition as a binary 0. The input to the adder and to the carried-digit storage might each be gated such that the adder produces a 0 output if both inputs are the same (either 0 or 1) and a 1 output when the inputs are unlike. The carried-digit storage circuit produces a 0 output in all cases except application of two 1 inputs. If the output of C is applied in a feedback return to the input of the adder gating, the subsequent adder output will reflect the carry. The circuits then offer the addition function required for binary manipulation.

Figure 2-6 diagrams the basic circuit. (Only the solid signal lines need be considered at this point in the discussion.)

To provide the gating function needed for the generation of the appropriate output, simple biased diode circuits can be employed. Figure 2-7 illustrates simple gates passing a signal only when both inputs are 1's (example 1), and when either

input is a 1 (example 2). A gate, such as example 1, which requires a 1 signal from both A and B to produce a 1 output is called an "and" gate. Similarly, since the second example produces a 1 output from a 1 signal at either A or B, such a circuit is called an "or" gate. (In the examples, a 1 signal is positive.)

In the language of computer design, these are termed "logical operators". Arithmetic operators are "plus", "minus", "times", and "divided by"; each being symbolized by "+", " - ", " x ", " ÷ ", respectively. Logical operators also are given symbols, although absolute standardization of the symbols has not been established. Although in this manual "+" symbolizes the logical "or", and ". " symbolizes the logical "and", the reader may also encounter these operators symbolized by other devices.

Gates are often shown schematically as a semi-circle with the appropriate symbol inside. A complex gate is conveniently analyzed by setting up a "truth" table, similar to those shown in figure 2-7, listing the conditions necessary to produce a "true" or "1" gate output. The function E in each of the examples may be defined using the input letters and the logical symbols as follows:

"And" gate:	$E = AB$, or $E = A \cdot B$
"Or" gate:	$E = A+B$
"And-or" gate:	$E = AB+CD$

The notation system and the operations derive from a branch of symbolic logic called Boolean algebra, after its originator, George Boole.

In addition to the logical operators already discussed, the "not" operator is employed. The "not" concept in the algebraic derivation is equivalent to the complement concept. That is, in any whole made up of two parts, one part may be called the complement of the other, and one part necessarily is "not" the other part.

Referring again to the circuits employed to effect binary computation, and also to figure 2-6, the bi-stable multivibrator used for storage can demonstrate the "not" operator in its two states. The multivibrator circuit consists essentially of two amplifiers, the output of each being returned to the input of the other such that one is conducting while the other is cut off. A set pulse applied to the input of the cut off stage produces conduction and subsequent cut off of the opposite stage.

The circuit may be considered to have two outputs, which change from a "true" or conducting condition to a "false" or cut off condition. Commonly, the circuit remains in one condition until the required pulse is applied to the alternate input. The two inputs are called "set" and "reset" and are symbolized by the

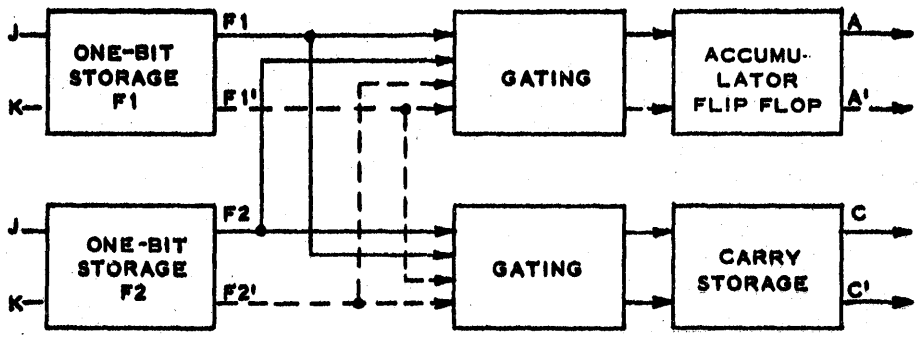
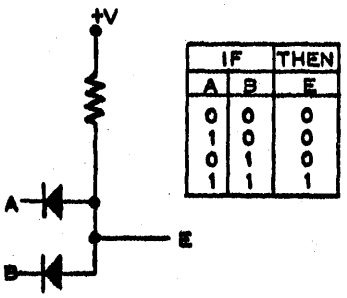
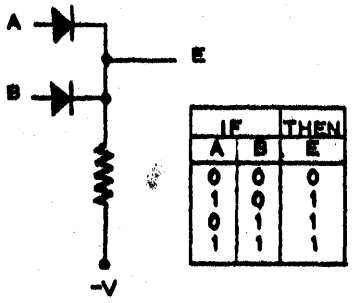


Figure 2-6. Functions (Logical Elements) Required For Binary Manipulation



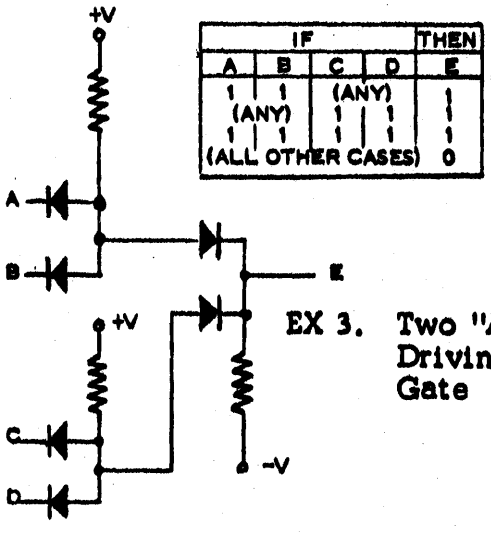
IF		THEN
A	B	E
0	0	0
1	0	0
0	1	0
1	1	1

EX 1. "And" Gate
(True input signals are assumed to be positive.)



IF		THEN
A	B	E
0	0	0
1	0	1
0	1	1
1	1	1

EX 2. "Or" Gate



IF				THEN
A	B	C	D	E
1	1	(ANY)		1
(ANY)		1	1	1
1	1	1	1	1
(ALL OTHER CASES)				0

EX 3. Two "And" Gates Driving an "Or" Gate

Figure 2-7. Typical Diode Gates in Logical Application

letters "j" and "k", respectively. The output of the stage corresponding to the "set" input is called the "normal" output, symbolized by the letter representing the circuit. The output of the stage corresponding to the "reset" input is called the "not" or "complement" output, symbolized by a prime mark following the letter representing the circuit and shown in dashed lines in figure 2-6. (The use of prime marks in this manual is symbolically equivalent to over-score marks sometimes used.) With these logical tools, the computer designer establishes equations representing the conditions which must be met by gating and storage circuits in order to provide the general performance desired. Such equations are called the "logic" of the computer.

2-2. BASIC CIRCUITS.

Binary computation has been shown to require two basic types of circuits: gating and storage. The stored program computer also requires a central storage device, which establishes the requirements for recording and reading circuits. For a magnetic drum storage, circuitry must generate a recording current representing the information to be stored and a detected signal reproducing the recorded pattern. The recording technique selected, in turn, influences the selection of gating and storage circuits.

To avoid some of the limitations of alternate recording techniques, a phase modulation system has been employed in the RW-300. Thus, rather than altering the amplitude of the recording current to represent the difference between the digits 1 and 0, this system changes the phase of the recording current with respect to a stable timing pulse. The signal, as read from the recorded track, is therefore a continuous a-c function. A unique, dynamic flip flop satisfies the resultant requirements, but introduces a "reverse" gating condition. Conventional gating and d-c flip flops are used for certain storage functions, such as read head selection and writing into circulating registers.

The following paragraphs describe the recording technique, the gating structure, basic flip flop and its variations, special purpose flip flops, and the clock pulse.

2-2a. RECORDING TECHNIQUE. The write amplifiers in the RW-300 are designed to produce a continuous a-c function in recording on the magnetic drum surface. The phase of the signal recorded on the drum is inspected with respect to the clock pulse (CA) to determine its phase. The signal representing a series of the same digits (either a 1 or a 0) is virtually a sine wave at 153.6 kc. The basic frequency is determined by the diameter of the drum, the speed at which the drum rotates, and the bit density of which the recording heads are capable.

A series of alternately different digits can be considered as a sine wave at one half the basic frequency. Obviously, the frequency spectrum required by such a recording technique is relatively restricted and therefore can be obtained reliably in transistorized, transformer-coupled circuits. Figure 2-8 shows

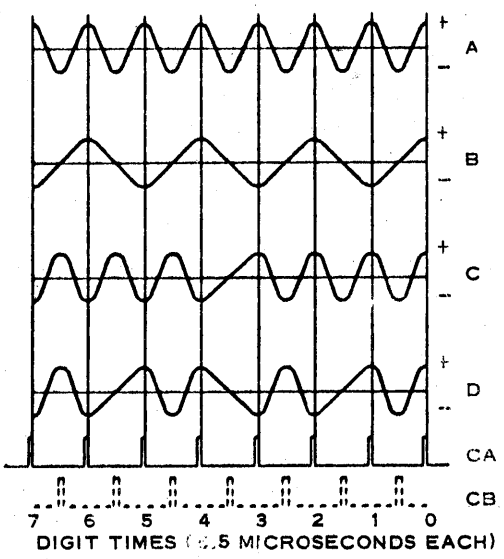


Figure 2-8. Typical Read Head Outputs

idealized waveforms of digits as they might be recorded on the track. Series A demonstrates the waveform of a series of digits which are all alike. Series B demonstrates digits which change from one value to the other in alternate time intervals. Series C illustrates a set of digits which remain the same for four time intervals and then change to the alternate digit; while series D shows a set of digits which remain the same for two time intervals, change to the alternate digit for two time intervals, return to the original state for two time intervals, and then return to the second state for two time intervals.

Identification of a digit as a 0 or a 1 is the responsibility of the clock pulse, CA. The clock pulse occurs at the time indicated by the row of solid line pulses along the bottom of the figure. Assuming that a negative signal is identified as the digit 1 while a positive signal is identified as the digit 0 at clock A pulses, series A may be said to represent the digits 00000000; series B represents 01010101; series C represents 00001111; and series D represents 00110011. Time is represented from right to left on the figure.

Retention of the a-c character of the signal throughout the Computer is accomplished by the use of a supplementary clock pulse, called CB, which occurs at the same rate as the principal clock pulse (CA) but is displaced in time midway between CA pulses. In figure 2-8, the clock B pulses are represented as vertical dashed lines.

2-2b. **DYNAMIC FLIP FLOP.** The a-c pattern recorded on the drum track is, after amplification, used to control a low level dynamic flip flop. Circuit output remains symmetrical with respect to zero voltage, changing phase depending upon input at clock A time, but is shaped to a virtual square wave.

As an aid to circuit analysis, a schematic is provided in figure 2-9. The right half of the circuit should be considered first, ignoring the connection of R into the base of each output transistor. Transistors Q3 and Q4 are connected as a flip flop in which transformer windings form the current path (and load) and capacitors (C) couple changes in conduction of one half into the other half to insure complete saturation during each cycle.

The current drawn through the primary winding flows in one direction through one half of the winding during conduction by one transistor, and in the other direction in the other half of the winding during conduction by the other transistor. The output of the circuit is conventionally coupled into the secondary, which is balanced with respect to ground. The base circuit of each flip flop transistor is driven through an "and" gate. Output from the secondary is applied through one diode while CB pulses are applied through a second diode. With a positive signal from the secondary at one input, and the CB pulse at the other input, the gate drives the transistor which had been cut off during the previous clock interval. Absence of one of these inputs results in application of the -27 volt cut-off bias at the base of the transistor.

Without other control, the circuit as thus far described would change state each clock B time, as the flip flop transistors alternately conducted. Sampled at clock A times, the output would be a series of alternating digits. To set the flip flop to the desired state--reflecting the input signals, the clock A pulse is employed. As with the clock B pulses, CA pulses are applied to "and" gates

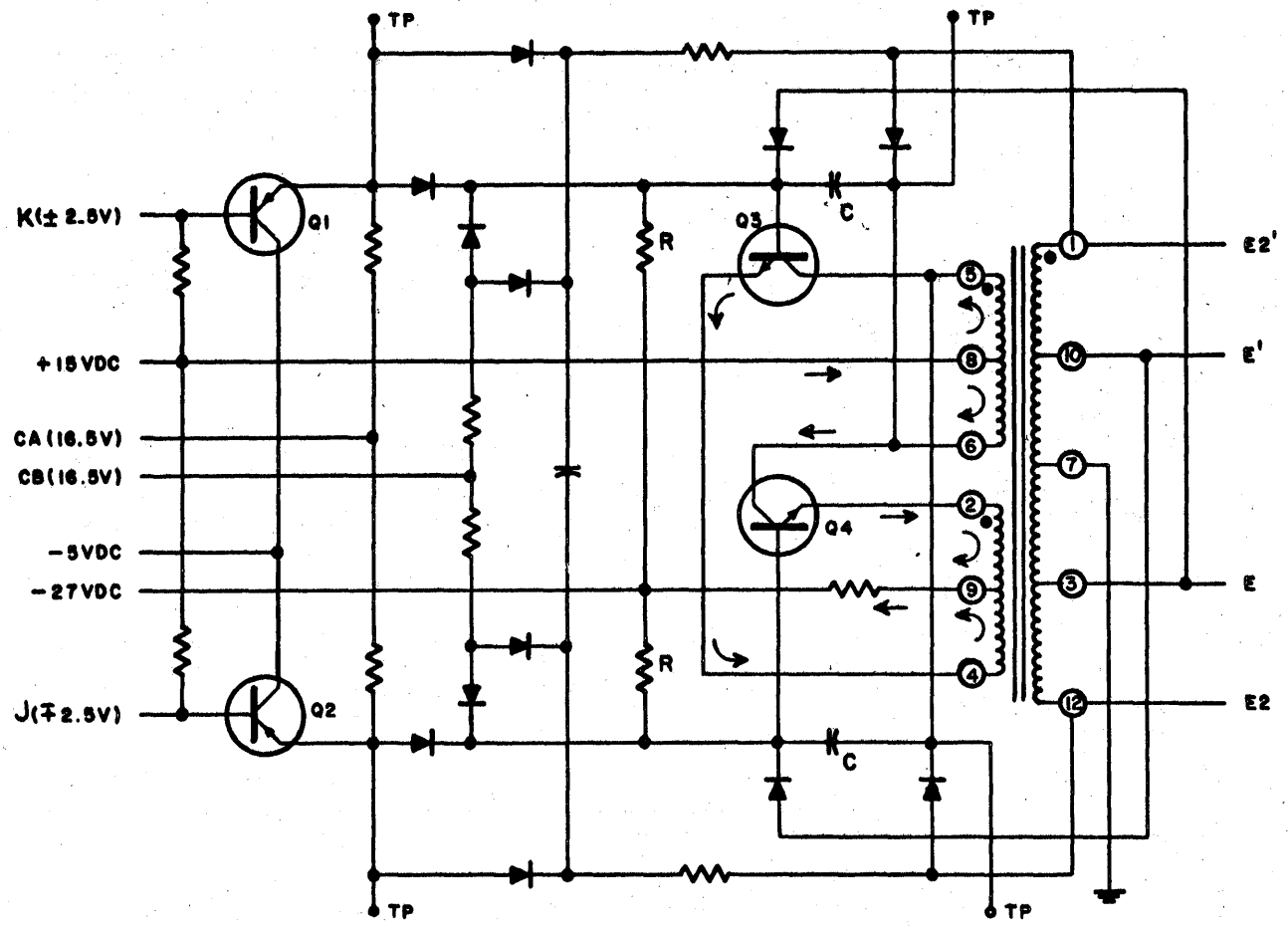


Figure 2-9. Dynamic Flip Flop, Basic Schematic

driving the base of each of the flip flop transistors. Occurring in conjunction with the application of a positive signal from the secondary, CA pulses could similarly produce the alternation of output state. Control of the output state is effected by inhibiting the transfer of the CA pulse during application of true input signals.

The input signals are applied to the base of each of the PNP transistors shown at the left of the schematic. A positive (false) input signal holds the transistor at cut-off. The high impedance of the cut off stage does not absorb any of the CA pulse when it occurs, permitting its transfer to the flip flop input gate. Conversely, a negative (true) input signal drives the input amplifier into conduction, absorbing the CA pulse and inhibiting its transfer. Application of

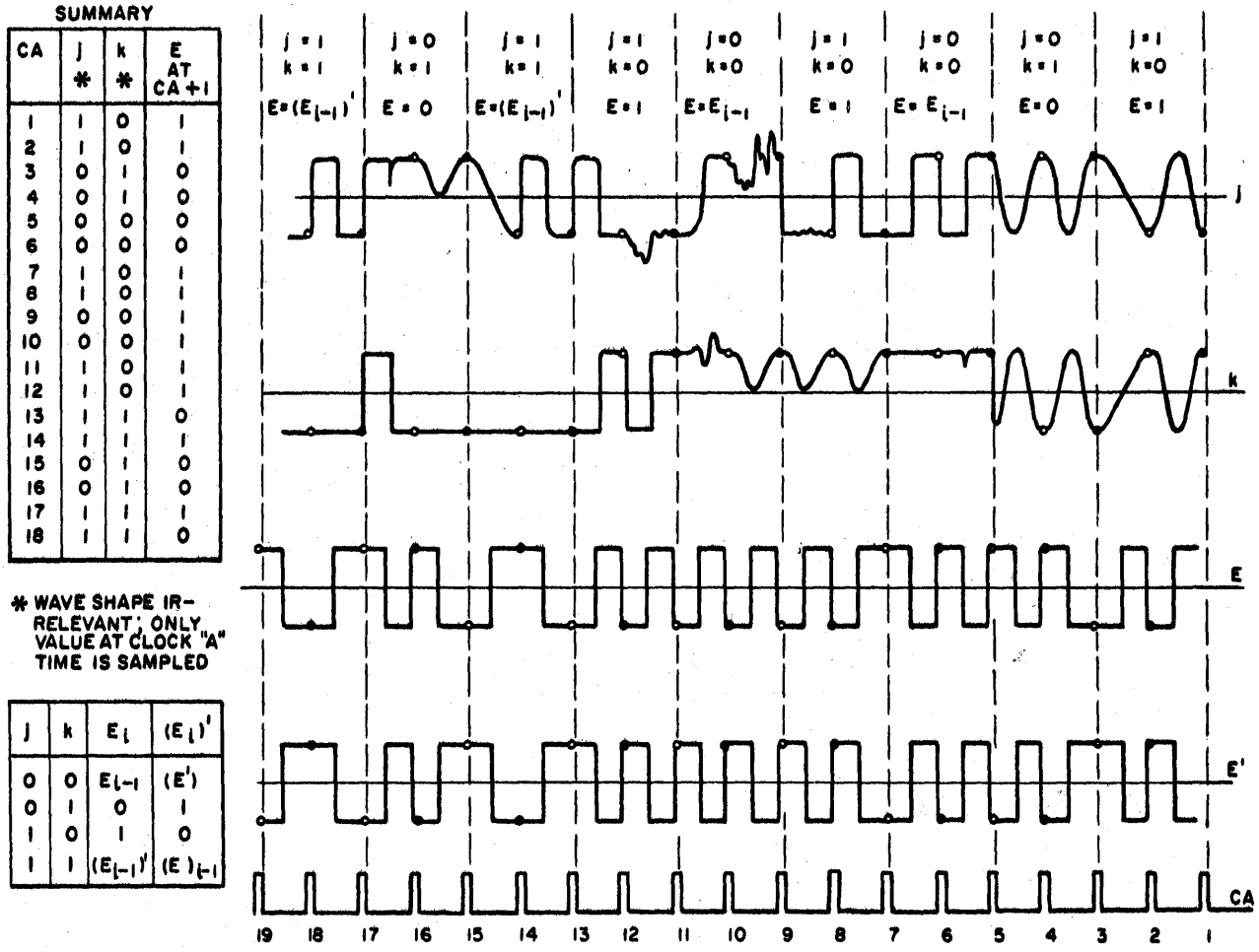


Figure 2-10. Idealized Waveshapes From A Dynamic Flip Flop Under Various Input Signal Conditions

false signals simultaneously to both inputs at clock A time results in a change in polarity of voltage at the secondary terminals since only the previously cut off side of the flip flop would be receiving both the CA pulse and the positive signal from the secondary. However, since the polarity of the output voltage had changed during the previous clock B time, the introduction of two false signals at the input would restore the state of the flip flop to that of the previous clock A time. Similarly, application of true signals to both input transistors at clock A time results in conduction in both and prevention of any change in the state of the flip flop output, from that generated by the previous clock B pulse. Therefore, the state sampled at the clock A time following application of two true input signals will be the reverse of the state sampled during the previous clock A time. The truth table summarizing this operation is provided in figure 2-10. The j side of the circuit is the set side, and corresponds to the E output side. A true (-2.5 volt) signal at j at clock A time produces a true (-2.5 volt) signal at E during the subsequent CA time.

2-2c. GATING STRUCTURE. Gating in the RW-300 complies with what is called two level "and-or" gating. As shown in figure 2-11, signals from two or more flip flops and/or power amplifiers are applied to a first level "and" gate. At least one term applied to a second level "and" gate must be derived from a first level "and" gate. First level "or" gates are driven either by "and" gates or by signals directly from flip flops or power amplifiers. At least one of the inputs to a second level "or" gate is derived from a first level "or" gate. The second level "or" gates minimize the diode back current when many "or" terms are necessary. Such a standardized gating structure affords versatility in application without prohibitive power drain.

In figure 2-7, typical "and" and "or" gates were illustrated. Generally, gates were assumed to have been triggered by d-c inputs, a true signal being represented as a positive voltage. As described in paragraph 2-2b, the output of the dynamic flip flops employed in the RW-300 Computer is an a-c signal, true at -2.5 volts and false at +2.5 volts. Gates admitting such signals are therefore reverse of those illustrated in figure 2-7, and may be summarized as shown in figure 2-12.

The a-c nature of the flip flop output is subject to some distortion resulting from transfer through gates. However, sampled at clock A time, the condition identifying the state (an amplitude no more positive than -2.5 volts) is retained. Hence, regardless of the input waveshape, if at clock A time all inputs are in phase and positive, the gate will present a false signal at its output; while, if all inputs are in phase and negative, the gate will present a true signal at its output.

Out-of-phase signals applied to the "and" gate create a false signal at the value of the most positive input signal, as sampled at clock A time. Out-of-phase signals applied to an "or" gate create a true signal at the level of the

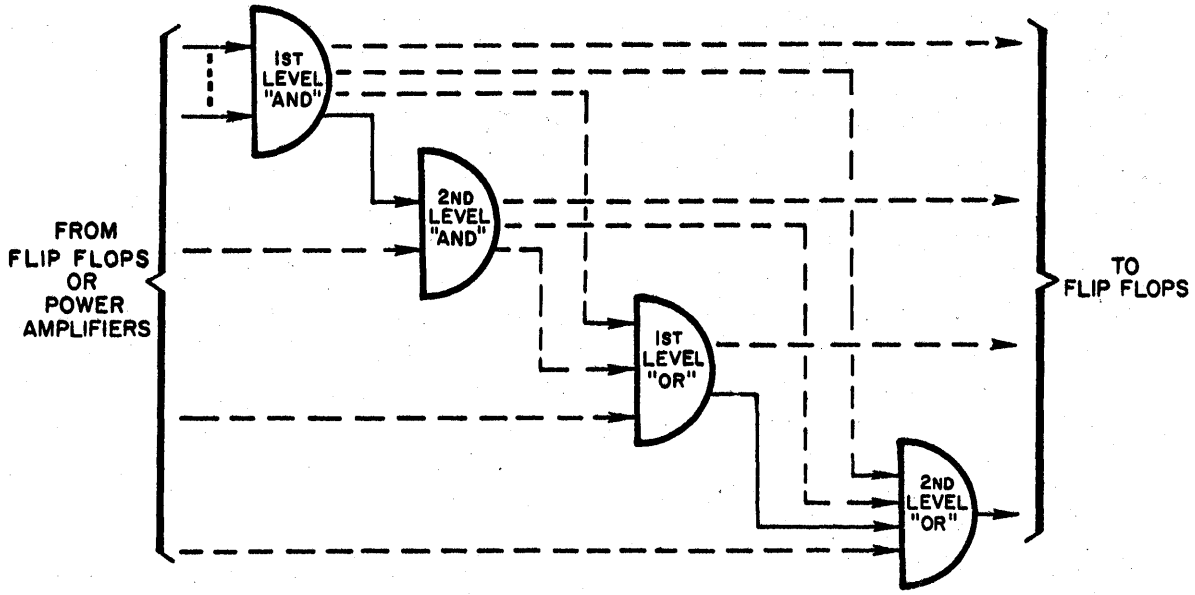
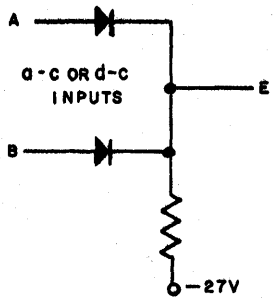
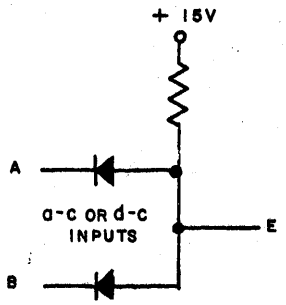


Figure 2-11. Two Level "And-Or" Gating (Required signal paths shown as solid lines; optional paths shown as dashed lines.)



IF		THEN AT CLOCK A
A	B	E
FALSE	FALSE	FALSE +2.5
FALSE	TRUE	FALSE +2.5
TRUE	FALSE	FALSE +2.5
TRUE	TRUE	TRUE -2.5

A. "And" Gate



IF		THEN AT CLOCK A
A	B	E
FALSE	FALSE	FALSE +2.5
FALSE	TRUE	TRUE -2.5
TRUE	FALSE	TRUE -2.5
TRUE	TRUE	TRUE -2.5

B. "Or" Gate

Figure 2-12. RW-300 Gates

most negative input signal, as sampled at clock A time.

Since the gating structure results in driving gates from other gates, as well as from the a-c output of flip flops, and although the truth table shown is valid, additional circuit configurations are required for cases in which the waveform of the gate output must be restricted to dc (see paragraph 3-2b and 3-2c).

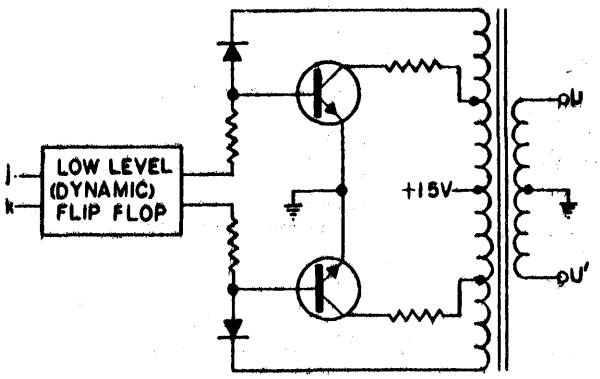
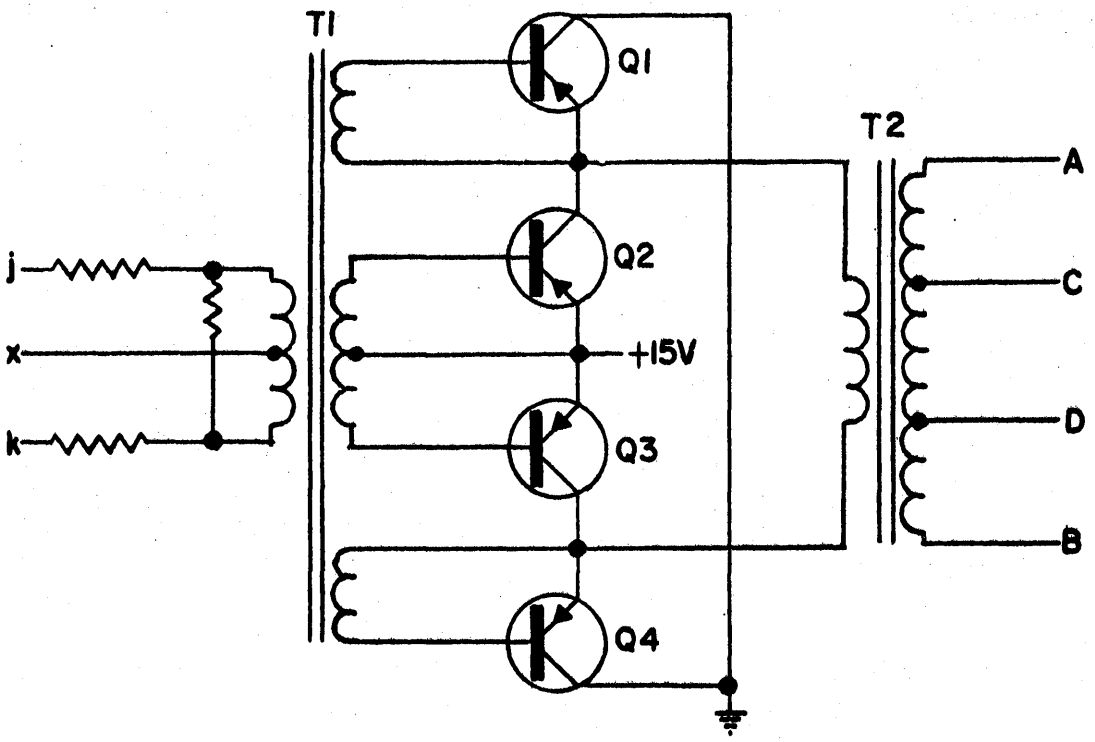


Figure 2-13. High Level Flip Flop, Simplified Diagram

Gates are designed to operate satisfactorily with input signals as low as ±2.5 v. Gate resistors have been selected to insure sufficient hold down voltage under the worst drain conditions, assuming circuit sharing rather than constant maximum drain. No more than eight inputs are applied to any "or" gate to limit source current requirements. Duty cycle and number of gates in a given network determine whether the input signals to the network must be supplied by a low level flip flop (20 ma max.), a high level flip flop (100 ma max.), of a power amplifier (200 ma max.).

2-2d. OTHER BASIC CIRCUITS. In addition to the basic low level dynamic flip flops already described, high level flip flops, read circuits, matrix amplifiers, d-c flip flops, delay flip flops, high level d-c converters, power amplifiers, and write and memory control circuits are employed in the RW-300 Computer. Those utilized in only one functional grouping will be described briefly in conjunction with their use. Those widely employed in the Computer are described in the following paragraphs.

2-2d(1). High Level Flip Flop (Figure 2-13). To satisfy the requirements for greater power output under maximum gating loads, the low level flip flop is wired into a power amplifier to become a high level flip flop, on a single insert card. Two NPN transistors comprising the power amplifier circuit alternately conduct, producing current flow in the correct direction in the primary of the output transformer. Output across the secondary can accommodate a 100 ma drain by associated gating without degradation of the ±2.5 volt a-c signal.



PIN	WRITE CIRCUIT		POWER AMPLIFIER	
	Controlled	Continuous	Push-Pull	Single-Ended
j	Input signal to be recorded	Input signal to be recorded	U output of flip flop	U output of flip flop
k	(Input signal)' to be recorded	--	U' output of flip flop	--
x	WC output of write control circuit	Ground	--	Ground
A	No. 1 head lead	No. 1 head lead	Output signal	Output signal
B	No. 2 head lead (common)	No. 2 head lead (common)	--	--
C	--	--	Ground	Ground
D	--	--	(Output signal)'	Output signal

Figure 2-14. Power Amplifier (Write Circuit), Schematic

2-2d(2). Power Amplifier (Figure 2-14). The power amplifier circuit is packaged with two complete circuits on each insert card. The input may be connected, either push-pull or single-ended, to provide a controlled or continuous signal to the write head when the circuit is utilized as a power amplifier, or to accept a-c or single polarity signals. The table under figure 2-14 lists the connections for various uses. Input signals induce signals on the bases of Q2 and Q3, resulting in an amplified voltage change at the load (the primary of T2). Connection of Q1 and Q4 essentially as emitter followers provides simultaneous current amplification. The desired power amplification is produced as the combined increase in power available at the secondary of T2.

2-2d(3). Delay Flip Flop (Figure 2-15). The basic dynamic flip flop is also used for a delay flip flop by the introduction of a single transistor circuit on the j input which inverts the signal to drive the k input. If a zero is applied to the j input, the output of the flip flop is zero at the next digit time; while, if a one is applied to the j input, the normal output of the flip flop is a one, one digit time later.

2-2d(4). Read Circuit (Figure 2-16). The basic low level dynamic flip flop is also a part of the read circuit accepting the signal from the magnetic storage drum. Output is presented one digit time following the application of input.

The single-ended signal from the drum is applied to the base of an NPN transistor amplifier driving an emitter follower, the load for which is the primary of the input transformer. Transformer output drives a push-pull circuit acting as the clock A inhibitors described in paragraph 2-2b. Biases on the input stages are established to maintain the waveform symmetry while slightly clipping signal peaks.

2-2d(5). High Level D-C Converter (Figure 2-17). Four high level d-c converters, such as shown in figure 2-17, are packaged on a single insert card. These circuits are preceded by gating which converts the a-c signals, from dynamic flip flops, etc., to d-c signals. Resultant d-c input signals to the converter are biased 15 volts above ground, and inverted in the input transistors. The output transistor provides a signal at +15 volts from a true input at Q1, and at +1 volt from a false input at Q1. When generated in response to the condition of the track register (M) flip flops, outputs from high level d-c converters control the transfer of signals through the read head selection unit, and from the circulating registers into the write circuits. (See paragraph 3-2c and 3-3a(4).

2-2d(6). Matrix Amplifier (Figure 2-18). Matrix amplifiers are equipped with only a j input. Output is a low impedance at 20 milliamps. No delay is introduced by this circuit since it responds directly to input signals without reference to the clock pulses. To prevent overloading the transformer wind-

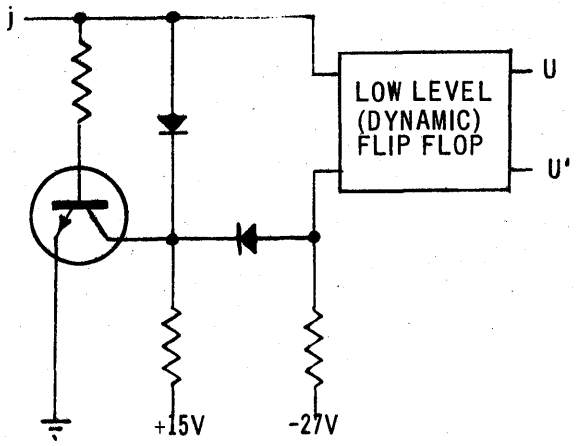


Figure 2-15. Delay Flip Flop, Simplified Diagram

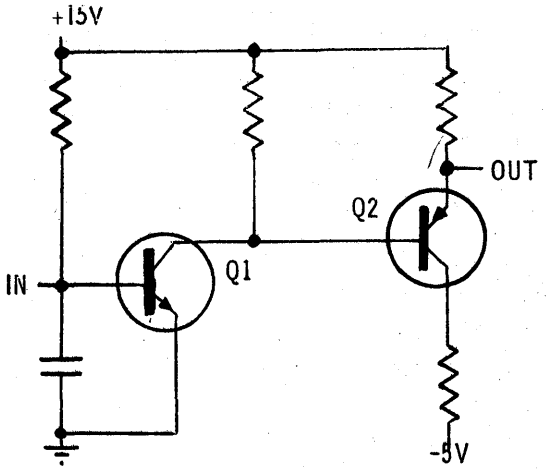


Figure 2-17. High Level D-C Converter, Schematic

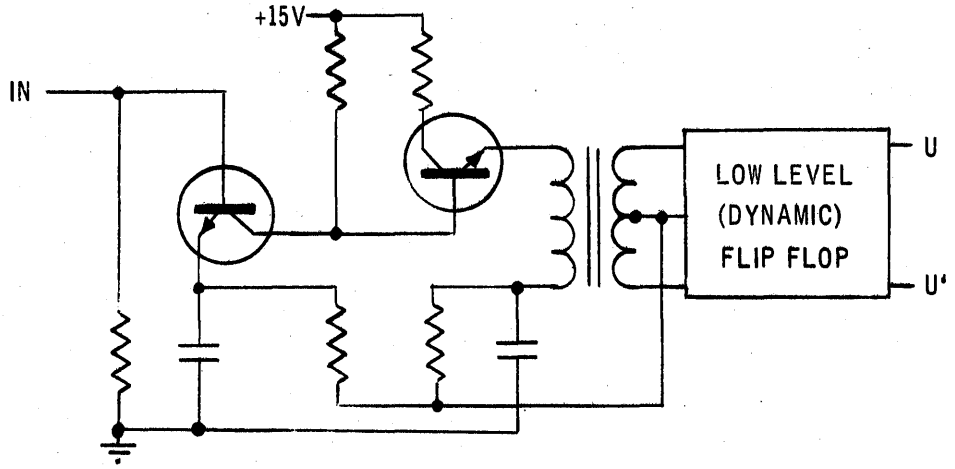


Figure 2-16. Read Circuit, Simplified Diagram

ing, a Z1' term must be included at the input, insuring that the input has an a-c character. The input stage is an emitter follower, driving Q4, a second emitter follower, through an "and" gate introducing Z1, and Q3, an inverter driving one side of the primary of the output transformer. Q4 couples the signal into the emitter of Q2, generating drive for the opposite side of the output transformer primary. Output power is developed between the clock B pulse and the clock A pulse of a bit and therefore can be used only to drive gating for A phase flip flops.

2-2e. CLOCK. Essential to the interpretation of the operation of the circuits in an automatic computer is the timing pulse called the clock. In the RW-300, two clock pulses are employed. The main clock pulse, CA, is responsible for the sampling; while a secondary pulse, CB, is applied to the dynamic flip flop for automatic state changes midway between CA pulses.

Clock pulses are approximately 0.6 microsecond wide, occur at the basic rate of 153.6 kps, and are applied to Computer circuits at a nominal amplitude of + 16.5 volts. Pulses are generated by circuitry on the power supply chassis described briefly in paragraph 3-6. The clock track on the drum bears the sine wave pattern applied to the input gate which triggers the clock generator. Thus, variations in phase of the 60 cps drum power source are reflected in the generation of clock pulses which remain synchronized with bits being read from or recorded on the drum.

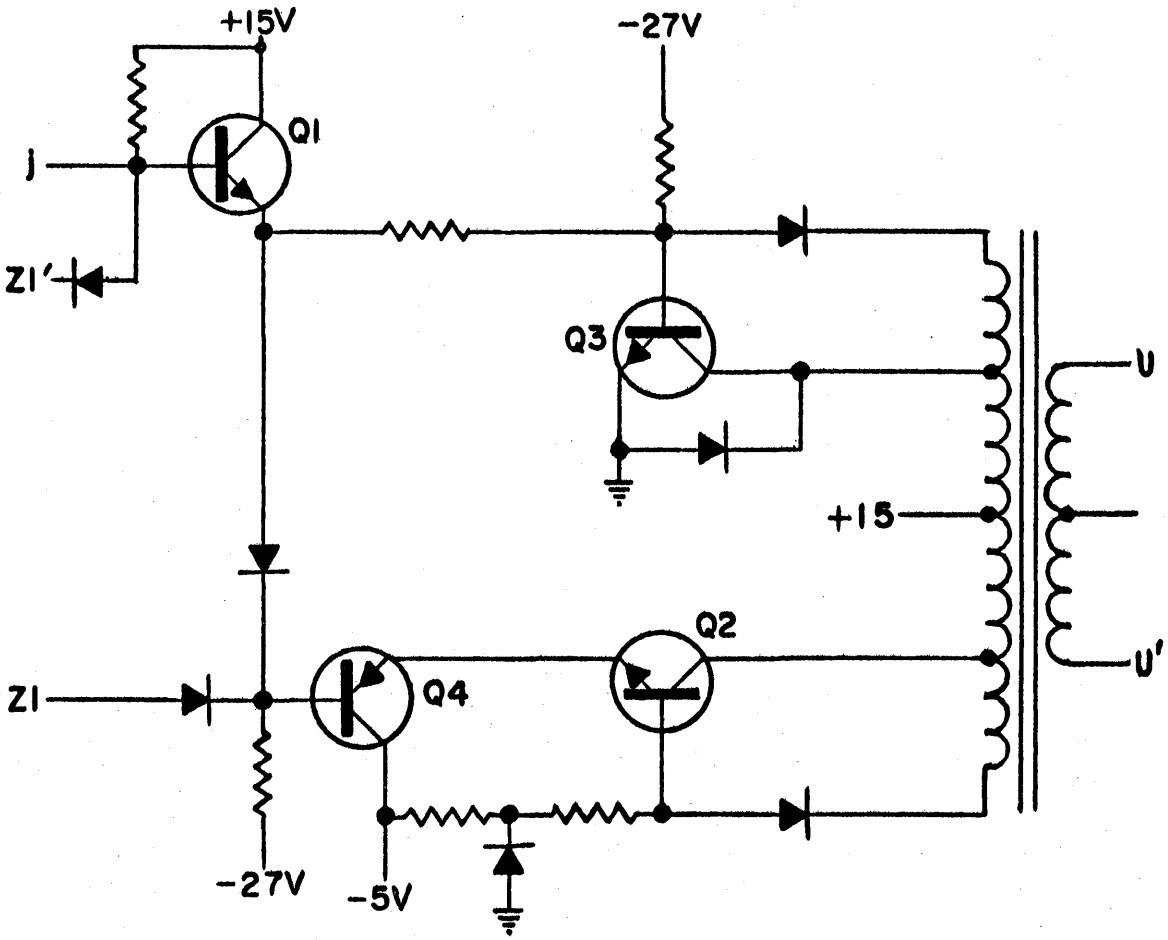


Figure 2-18. Matrix Amplifier, Schematic

SECTION 111

THEORY OF OPERATION OF RW-300 FUNCTIONAL GROUPS

3-1. INTRODUCTION.

The theory of operation of the RW-300 Computer is presented on the basis of the following functional groups:

a. Storage functions, including mechanical features of drum and heads, and head signal selection and recording;

b. Arithmetic and control functions, described on the basis of circuit groups and instruction processing;

c. Digital input/output capabilities and circuits;

d. Analog input/output capabilities and circuits;

e. Clock generator and power supply circuits; and,

f. Test and control group functions.

Each of these groups, except certain of the analog input/output circuits, is or can be mounted on the Computer frame as described in applicable paragraphs. Figure 3-23 should be referenced in following the descriptions of storage, arithmetic, and control functions.

3-2. STORAGE FUNCTIONS.

Central storage in the RW-300 is provided by the magnetic drum and head assembly, in conjunction with read amplifiers and recording amplifiers controlled by head selection circuits. Data and instructions accepted by the Computer, or generated within it, are recorded in tracks or channels on the magnetic surface of the drum. Certain tracks can be recorded only under program loading. Others are recorded only by information from the analog converter. Dual units containing a read head and a write head provide circulation of data on certain tracks, for instant accessibility during instruction processing. The following description of storage functions is therefore organized on the basis of the mechanical features of the drum and heads, the track usage, the head selection circuits (required during reading from general storage tracks), and the recording control system.

3-2a. MAGNETIC STORAGE ASSEMBLY. The magnetic storage assembly consists principally of a magnetic storage drum driven by a synchronous motor, a set of magnetic recording and reading heads, necessary cabling from motor and

heads to drum input connectors, and a housing.

The assembly is shock-mounted to the Computer frame and is located in the left center area, as shown in figure 3-1. (Refer also to the Computer assembly drawing, figure 1-2.)

The series of individually labelled connectors mounted on the front surface of the housing accept the power input for the motor and signal connections for the heads. No accessibility is afforded to the inside of the housing. The self-lubricating bearings in the motor are rated for some 50,000 hours of maintenance-free operation. Head positions are factory-set and should require no adjustment in normal service. Failure of a head or its associated wiring may be corrected through use of one or more of the spares, which also are correctly adjusted and wired to the connectors on the front of the housing. (Refer to supplementary literature for installation and maintenance data.)

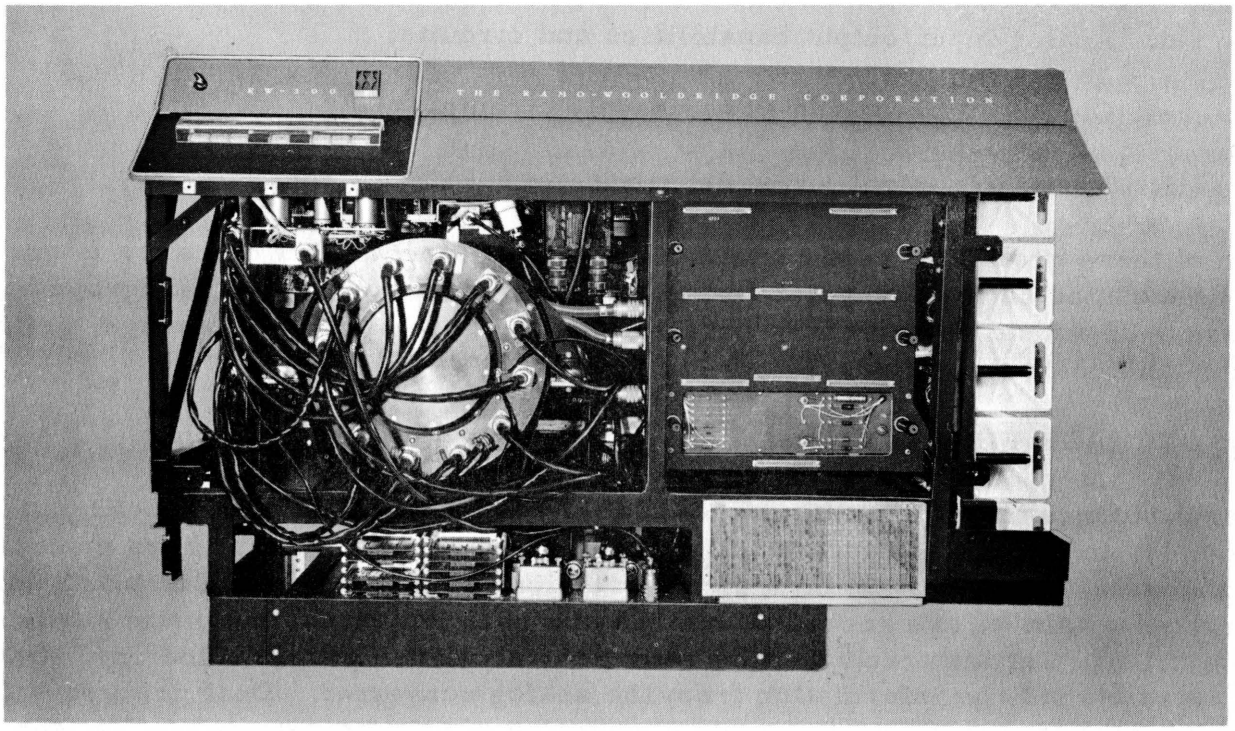


Figure 3-1. RW-300 with Front Panel Removed

The central storage device in the RW-300 Computer is an aluminum drum, nine inches in diameter and nine inches long, spray-coated with magnetic oxide. The drum is driven at 3600 rpm by a 60-cps, dynamically balanced, synchronous motor.

When the POWER ON switch on the Control panel is pressed, a circuit is completed from the 115-vac input through the coil of relay K27, in the Relay Junction Box. Contacts on K27 complete the circuit from the a-c input to one side of the drum motor, applying 220 vac to the motor.

During the two minutes following initial application of power, the motor reaches stable speed and no power is applied to the remainder of the Computer. At the end of the period, controlled by a time delay circuit in the Relay Junction Box, voltage on the motor is dropped to 115 vac for normal operation and power is applied to the remainder of the Computer.

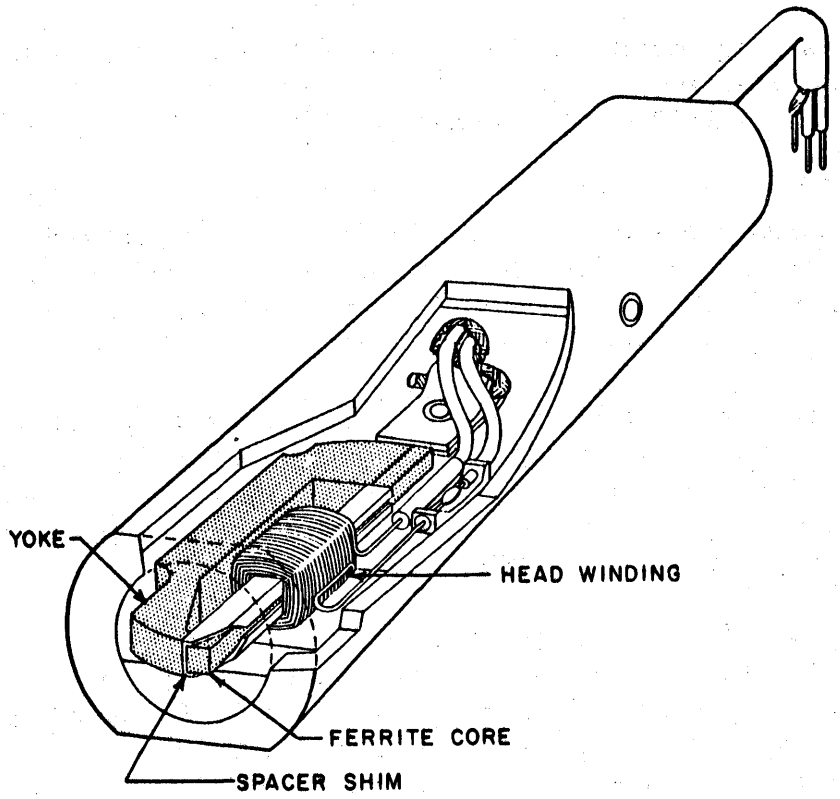
3-2a(1). Heads. Recording upon the drum and reading from the recorded tracks is accomplished by the heads. Each head is effectively a small electromagnet with a 0.001-inch gap in the magnetic field path. This gap is positioned 0.001-inch from the magnetic surface of the drum, permitting the drum surface to complete the magnetic field path. Current changes in the head coil produce changes in the magnetic field and resultant variation in the magnetization pattern on the drum track. Conversely, variations in the magnetization pattern produce changes in induced coil current. Impressing a desired signal pattern on the track is called writing, and detecting the pattern is called reading. The recording pattern employed in the RW-300 is described in paragraph 2-2a.

Two types of heads are employed in the RW-300 Computer: a single unit capable of reading or writing, and a dual head in which one single unit reads while a second simultaneously writes the same material into the adjacent position on the track. Cut-away views of both types of heads are shown in figure 3-2.

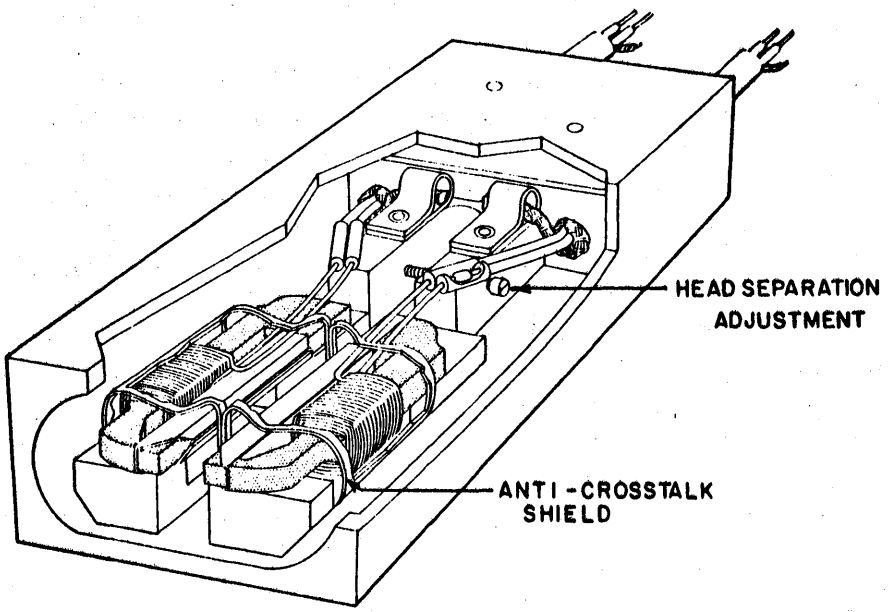
A ferrite bar and yoke, separated at one point by a silver shim, comprise the magnetic path with the desired gap. Ferrite surfaces at the gap are ground to the radius of the drum. In the single unit, the head coil is assembled to the bar. In the dual head, a head coil is assembled to each of the two yokes. Mechanical assembly of either type is completed by filling the cavity between case and unit with soft vinyl.

Nominal performance specifications at clock frequency are tabulated below.

	Single Unit	Each Unit In Dual
Inductance (microhenries)	82	100
Impedance at 200 ma (ohms)	120	160
D-C Resistance (ohms)	1.17	1.34



A. Single Unit Read/Write Head



B. Dual Read and Write Head (One-word revolver)

Figure 3-2. Cut-away Diagram of Heads Used in RW-300 Computer

	Single Unit	Each Unit In Dual
Saturation writing current, peak-to-peak (ma)	225	200
Readback, at 200 ma writing current (millivolts)	183	150
Bit density, per inch, at 3600 rpm	90	90
Track width (inches)	0.051	0.054

Heads are secured to the headmount which is provided with openings in a spiral arrangement, as illustrated in figure 3-3. Each head is individually adjusted for spacing from the drum surface and for peripheral location. The space between the gaps of the dual head is also adjusted for the correct write/read delay.

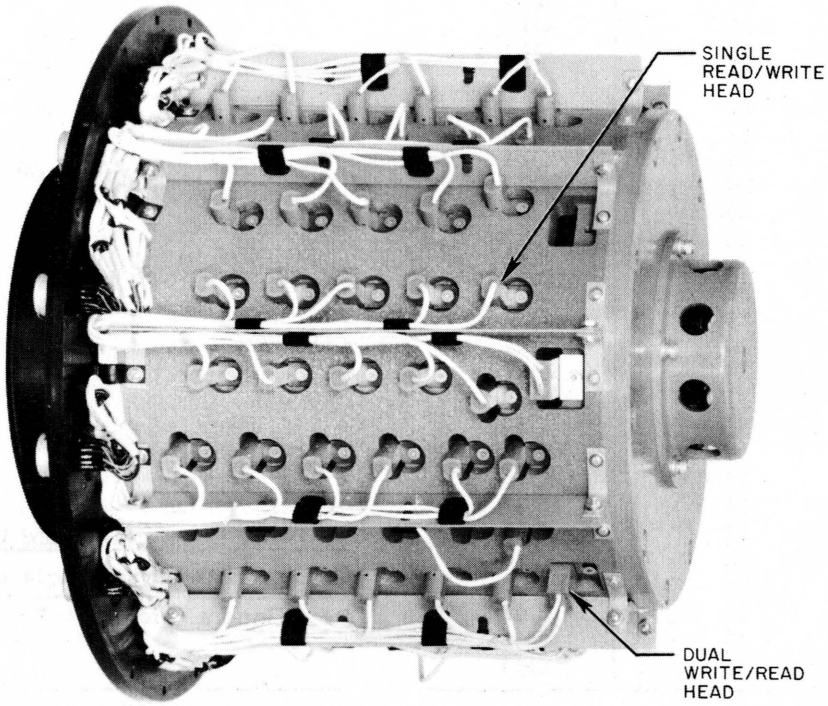


Figure 3-3. Drum Headmount Showing Location of Heads

Tracks With Dual Heads	Signal Designations
A register (19-bit CR)	Q272 Q72
B register (19-bit CR)	Q273 Q73
Y register (20-bit CR)	Q269 Q69
N register (20-bit CR)	Q270 Q70
C register (20-bit CR)	Q271 Q71

Tracks With One Single Head		Signal Designations
Clock		Q65
General storage	9	Q10
	10	Q11
	11	Q12
	12	Q13
	13	Q14
	14	Q15
	15	Q16
	16	Q17
	17	Q18
	18	Q19
	19	Q20
	20	Q21
	21	Q22
	22	Q23
	23	Q24
	24	Q25
	25	Q26
	26	Q27
	27	Q28
	28	Q29
	29	Q30
	30	Q31
	31	Q32
	32	Q33
	33	Q34
	34	Q35
	35	Q36
	36	Q37
	37	Q38
	38	Q39
	39	Q40
	40	Q41
	41	Q42
	42	Q43

Tracks With One Single Head		Signal Designations
General storage	43	Q44
	44	Q45
	45	Q46
	46	Q47
	47	Q48
	48	Q49
	49	Q50
	50	Q51
	51	Q52
	52	Q53
	53	Q54
	54	Q55
	55	Q56
	56	Q57
	57	Q58
	58	Q59
	59	Q60
	60	Q61
	61	Q62
	63	Q64

Tracks With Two Single Heads		
Sector number		Q66 and Q67
General storage	0	Q201 Q1
	1	Q202 Q2
	2	Q203 Q3
	3	Q204 Q4
	4	Q205 Q5
	5	Q206 Q6
	6	Q207 Q7
	8	Q209 Q9
	62 (16-word CR)	Q263 Q63

Tracks With Three Single Heads		
General storage	7	Q8 Q208 Q88

Spare Track Type	Quantity
Dual head, 19-bit CR	1
Dual head, 20-bit CR	1
Clock (single head)	1
Sector number(single head)	2

Spare Track Type	Quantity
GS With One Single Head	7
GS With Two Single Heads	2
GS With Three Single Heads	1
GS (16-word CR)	1

NOTE: Signal designations in the 200 series are normally writing signals (input to the track) while signals designated as Q1 through Q88 are normally read from the track.

Figure 3-4. Typical Magnetic Head Usage and Signal Designations

3-2a(2). Signal Handling. In conjunction with appropriate heads, the surface of the drum serves as a series of concentric recording tracks. Tracks are spaced 0.090-inch center to center (11 to the axial inch). Seventy-two tracks are normally used and approximately fifteen spares are available. Figure 3-4 lists the heads used with each of the tracks and the logical designation for the signal produced by each.

Since the bit storage capacity of a recording track depends upon track length and bit density of which the head is capable, each track in the RW-300 can bear 2560 distinct bits of information. These bit cells are used in 20-digit groups called sectors, which are numbered from 0 to 127. The binary equivalents of numbers 0 to 127 (0000000 to 1111111) are recorded sequentially on the sector number track. Two single reading heads are associated with this track. The first reads the sector number for comparison with the sector specified by a given instruction and for synchronization of certain Computer circuits. The second reads the same sector number 32 sector-times later, making sector identification available to a writing head should the instruction require storage into the sectors of tracks 0-7.

In addition to bearing the number of each sector, the sector number track also offers synchronizing signals for:

a. the digit counter, by means of 1's recorded in bits 13 and 16 of each sector;

b. the analog input/output equipment by means of 1's recorded in bit 20 of all but sector 127; and,

c. external test equipment, by means of an origin pulse in bit 17 of sector 127.

One other Computer synchronization track is provided: the clock track which is provided with a single reading head. Recorded on the clock track is a precisely continuous 153.6 kc sine wave.

Five tracks, called one-word circulating registers, are provided with dual heads which read and record the same information simultaneously. The writing head in the dual unit is separated from the reading head by a distance equal to 17 or 18 bits. Two or three one-bit delays are added by the read-write circuitry to achieve the desired sector delay between reading and writing. Information on these tracks is continuously circulating and therefore immediately available to the Computer circuits. The tracks are used in arithmetic and control operations.

A similar circulation technique is provided in track 62 of general storage.

However, since the delay desired between writing and reading on this track is 16 sectors rather than a single sector, two single heads rather than a dual are used. As a given sector is read, its contents are written immediately into a sector 16-word lengths farther along the track. Identical information is thus available in eight sectors on track 62, and therefore accessible in one-eighth the time required for access to general storage. Circulation of this same information is uninterrupted until new data is written into the track.

Three types of general storage tracks, in addition to the 16-word circulating register, are provided:

a. Eight which are each equipped with two single heads positioned 32 sectors apart, one for reading and one for writing;

b. One or more (see special supplement describing installation under consideration) which communicates with analog input/output equipment, each of which is equipped with two or more single heads used for reading or writing as required; and,

c. As many as 55 which are each provided with a single reading head.

For special program writing, the read heads on the general storage tracks function as writing heads. A track selector arrangement on the Test and Maintenance panel permits writing into tracks 8 through 61 in groups of eight adjacent tracks. Attempts to write into a track other than one of the eight selected cause the Computer to stop and an error light to be illuminated.

The RW-300 can be equipped to permit writing into tracks 8 through 15 under program control in installations not requiring these tracks for communication with analog input/output equipment. An extra write module is then installed within the Computer (see paragraph 3-2c).

To clarify the application of each head, a block diagram of the circuits associated with each is provided in figure 3-5. Arranged at the top of the figure are the symbols for the signals appearing at each head. Signals numbered from Q1 through Q88 are being read from the drum; while those numbered from Q201 through Q273 are being written onto the drum. Since all read heads are reading simultaneously, the signal desired must be gated through a selection circuit or must be applied individually to separate circuits for specific uses.

Signals read from the general storage tracks (Q1 through Q64) appear at the input of the Read Selection unit, which, through application of appropriate control signals, passes only the information from the desired track into an amplifier (R1). The R1 signal and/or its complement R1' are applied to the control circuitry (not detailed in figure 3-5) for further processing.

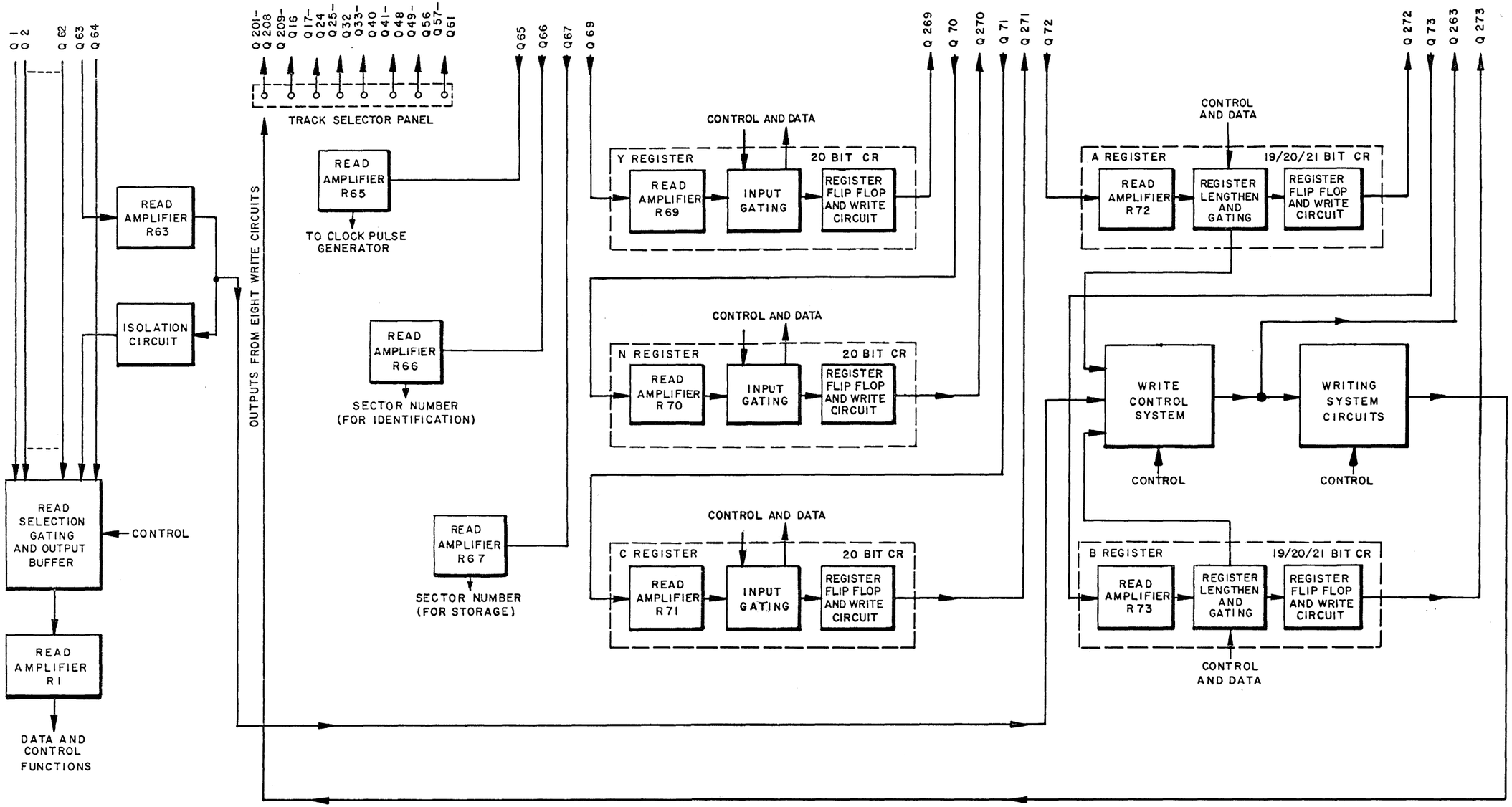


Figure 3-5. Read and Write System, Block Diagram

Signal Q63 read from the 16-word circulating register passes through a read amplifier, the output of which is applied, through an isolating transformer network, to the Read Selection unit and to the write system gating circuits. Subject to modification in the write system gating circuits, the signal becomes Q263 for recording on track 62. Similarly, information to be recorded on the remaining general storage tracks is introduced (from the A or B registers) into the write system gating circuits, through write control circuits selecting the desired one of eight adjacent tracks, to a movable output connector (P2113). Mating P2113 to one of the eight connectors accessible on the Test and Maintenance panel completes the write circuit for a group of eight separate recording signals. Normally, these signals are applied to tracks 0 through 7, each of which is provided with a separate write head.

As indicated in the figure, the clock track signal (Q65) is amplified and wired directly to the clock pulse generator, for synchronization of the power pulses applied to the Computer circuitry.

Outputs of the two heads on the sector number track (Q66 and Q67) contribute to the control functions, as is more fully described in paragraph 3-3a(1).

The storage function of the one-word circulating registers is illustrated in the diagram. Input and output of control and data signals are described in the diagrams and text of paragraph 3-3a(5).

The digital signal (Q88) read from track 7 communicates with the analog input/output circuitry; while analog information in digital form becomes Q209, for recording on track 8. Control of the analog input/output circuit is described in paragraph 3-5.

3-2b. **READ SELECTION.** Illustrated photographically in figure 3-6 is the Read Selection unit. (See also the major assemblies diagram, figure 1-2.) The unit is an assembly consisting primarily of:

a. Diode and resistor gating circuits, an isolating transformer network for Q63 input, and an output buffer stage, all mounted on a large phenolic board;

b. A panel on which are mounted the track selector connectors and a toggle switch;

c. The set of jacks for interconnection between heads, read selection gating, write selection, and power;

d. A subchassis supporting a write protection relay; and,

e. A main supporting frame.

Gating on the Read Selection unit is controlled by the track register. Briefly, tracks are identified as a combination of output signals from the six flip flops comprising the track register. The (logic) symbols for these flip flops are M1 through M6, and the symbols for the outputs of each flip flop are M1 and M1', M2 and M2', M3 and M3', M4 and M4', M5 and M5', and M6 and M6'. Basic circuit description and a schematic of the type of flip flop used in the track register are included in paragraph 2-2.

The combination of M1' M2' M3' M4' M5' M6' represents the identity of track 0; M1' M2' M3' M4' M5' M6 represents track 1; etc., with M1 M2 M3 M4 M5 M6 representing track 63. Each output drives a separate high level d-c converter, described and illustrated schematically in paragraph 2-2d(5), the outputs of which are identified as MD1, MD1', MD2.....MD6'. Selection of track 0 would result in generation of the signals M1' M2' M3' M4' M5' M6' and therefore of outputs MD1' MD2' MD3' MD4' MD5' MD6', which are used to back-bias the diodes in the Read Selection unit. The gating structure is summarized in figures 3-7 and 3-8.

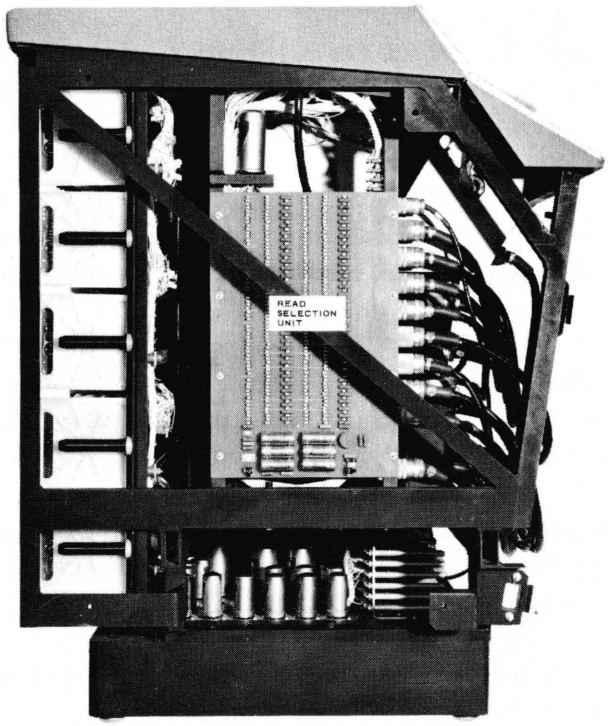


Figure 3-6. Left Side of RW-300 Computer with Side Panel Removed.

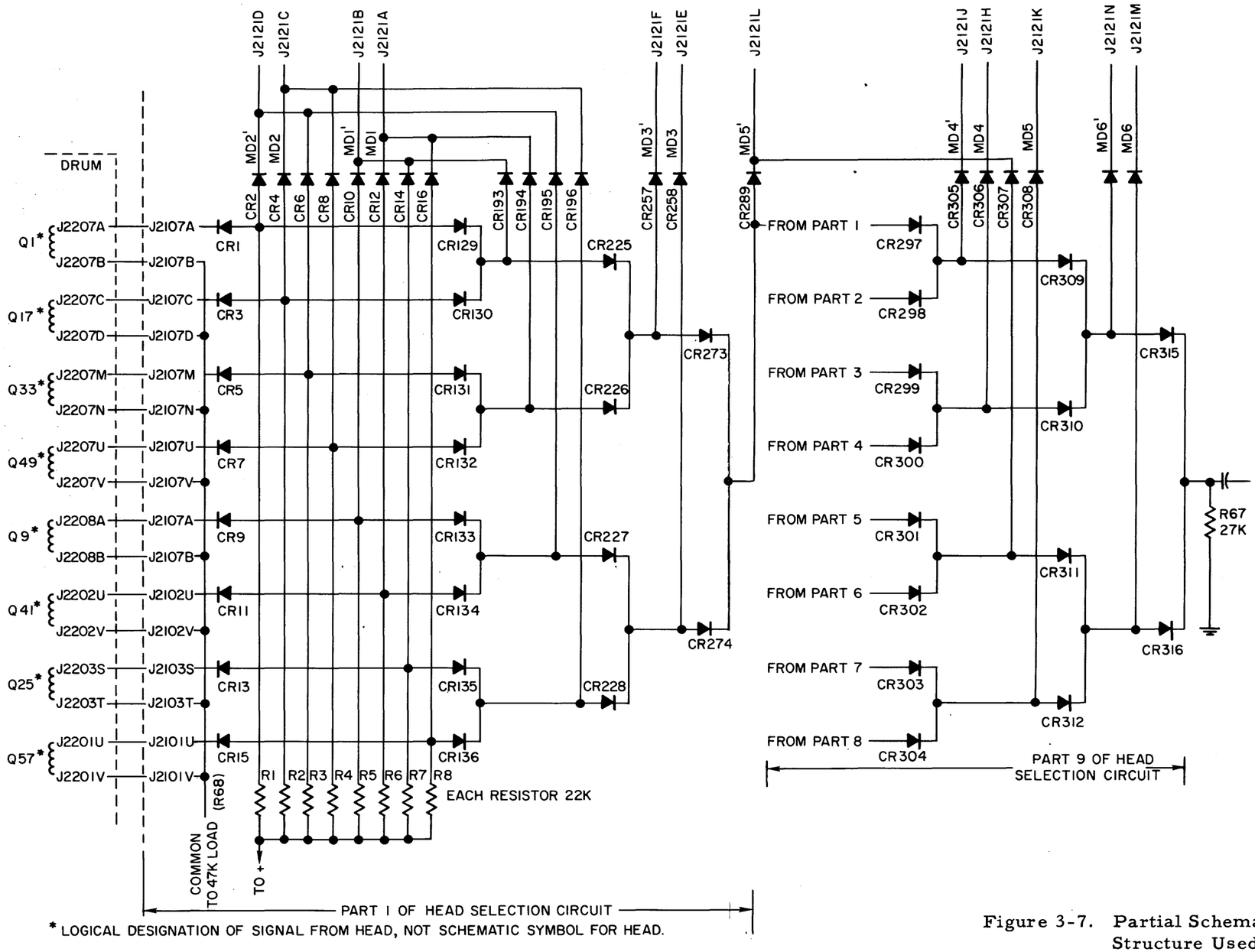


Figure 3-7. Partial Schematic of Gating Structure Used in RW-300 Read Selection Unit

As an example of the gating action, assume track 0 is to be passed to the general storage read amplifier, R1. The signal (Q1) from the track 0 read head is available between pins A and B of J2107. The required control signals (MD1' MD2' MD3' MD4' MD5' MD6') are produced and appear at the connectors as shown in figure 3-7. Resistors R67 and R68 establish equal current drain from the power source by each of the two branches of the conducting circuit. Presence of the MD1' signal, and therefore of no MD1 signal, permits transfer of the Q1 signal but not the Q17 signal to CR193. Similarly, presence of the back-biasing MD1' signal permits transfer of Q1 while Q33 and Q49 signals are shunted through the low impedance MD1 path. The MD3' signal back-biases CR257, permitting transfer of Q1 through CR273. The desired signal is thus passed through the gating circuit while undesired signals are conducted to ground through the control circuits.

Figure 3-7 illustrates only parts 1 and 9 of the gating structure. Parts 2 through 8 are essentially the same as part 1 and the interconnections into part 9 are indicated. Track and control signals applied to all parts are summarized in figure 3-8.

The desired head signal appears across the load resistor (R67) and is capacitively coupled into a class A NPN transistor amplifier. Amplifier output is direct-coupled to the base of an NPN emitter follower which drives read amplifier R1, a basic circuit description of which is included in paragraph 2-2. Distribution of the signal from the read amplifier is described in paragraph 3-3b.

While physically part of the Read Selection unit, the track selector panel (track selector jacks and write protection toggle switch) and write protection relay can be considered functionally part of the write system and are described in paragraph 3-2c.

3-2c. WRITE SYSTEM. The circuits necessary for writing and writing control are incorporated on module 113, located in the top left corner of the rear of the Computer, as shown in figure 3-9. Circulating registers, as indicated in figure 3-5 and described in paragraph 3-2a(2), are continuously recording. Input signals are determined by the instruction being processed and are introduced through the gating. Extra flip flops available in the A and B registers provide the option of circulation of 20 bits as normally required. Without the one-bit delay introduced by this flip flop, each of these registers circulates only 19 bits, thus effecting a one-bit right shift per circulation.

In addition to continuously recording revolver tracks, the arithmetic and control portion of the Computer controls writing into eight tracks of general storage and into the 16-word fast-access revolver. Selection of which group of eight tracks is to be used is manually controlled by the track selector plug and connectors on the Test and Maintenance panel. The analog converter portion of the Computer controls writing into track 8 (or tracks 8 through 15, depending upon the installation).

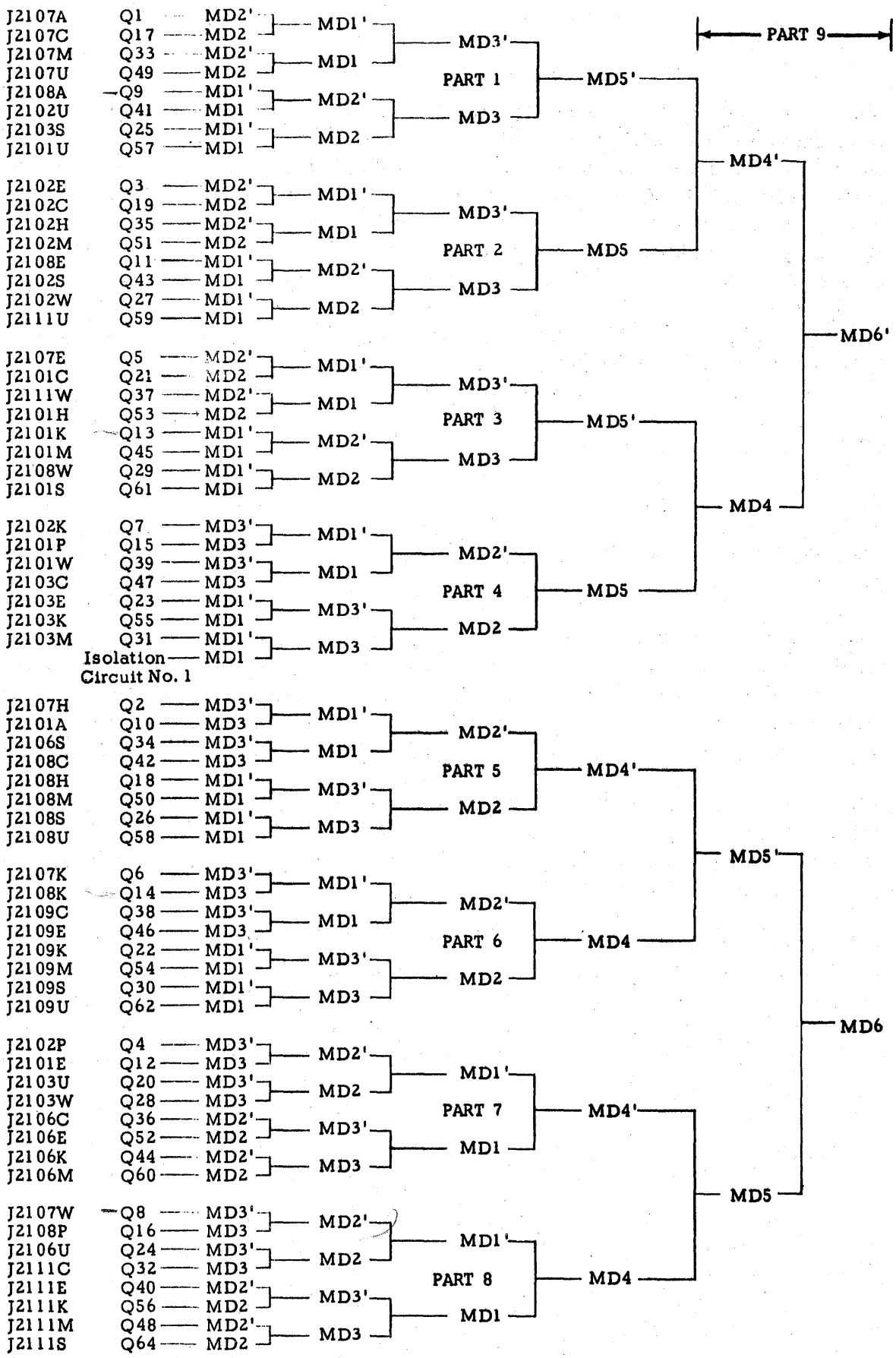


Figure 3-8. Reading Head Selection Gating

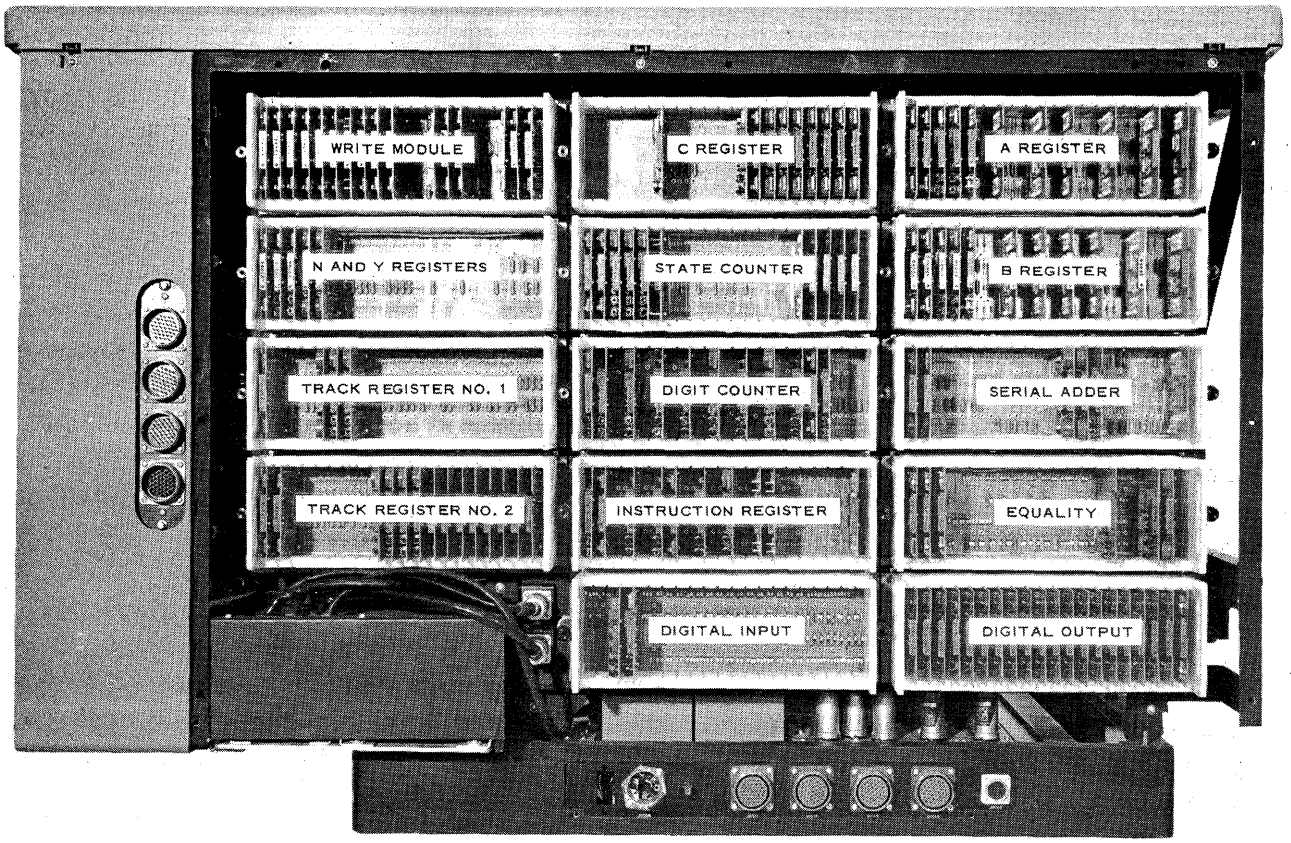


Figure 3-9. Back of RW-300 Computer with Rear Panel Removed to Show Location of Modules.

The signals permitting recording into a general storage track, to which the track selector plug is connected, are generated in response to a "store" instruction. During certain digit times in the processing of the instruction, gating produces an a-c signal which, with respect to the track from which the information to be recorded is read, can be called f_a or f_b. To use the signals to control the general storage write circuits, conversion to d-c is necessary. The desired output is produced through use of a group of signals called f_a*, f_b*, and f_{63}*, which are "anded" with the outputs of the reference flip flop.

The combinations comprising the asterisked function are the complements of the individual signals comprising the normal a-c function and should not be interpreted as the recognition equivalents of other signals. They are used only in the gating driving the high level d-c converters called DCA, DCB, and DC63.

The "anding" of the normal output of the reference flip flop and the f_a signal produces a d-c output which appears at the input of DCA. The manner in which conversion takes place is described below, using the A register in the example. D-C signals controlling writing from the B register and into track 62 are generated using the same technique.

Since the asterisked function, $f_a{}^*$, is generated simultaneously with f_a, it is "anded" with the complement output of Z1, producing a "mirror image" of f_a Z1. The two signals are applied to an "or" gate at the input of a high level d-c converter, illustrated schematically in figure 2-17. During one half of the cycle the diode introducing $f_a{}^*$Z1' conducts, passing the f_a Z1 signal into the transistor; and, during the other half cycle, the alternate diode conducts, passing the $f_a{}^*$Z1' signal. The result is a drop in input level of the converter during the full digit time and a consequent increase in collector potential. The NPN output stage, driven directly by the collector potential, tends to cut off during this condition, producing a +15 volt output level used for write control gates.

During any digit time in which f_a is false, both f_a Z1 and $f_a{}^*$Z1' are false and the input to the d-c converter is driven more positive, dropping the collector potential. Consequently, the output stage conducts, producing an output level of +1 volt.

A similar analysis is valid relative to the generation of d-c signals used to control writing from the B register into general storage or from either register into the 16-word revolver. The latter signal is called DC63 and its components are f_{63} Z1 or $f_{63}{}^*$Z1'.

The use of the signals thus generated is illustrated in figure 3-11, a block diagram of the write control system. The gating indicated at the left of the diagram is conventional d-c gating, such as originally described in paragraph 2-2c. The write control circuits shown as blocks at left center of the diagram are illustrated schematically in figure 3-10. Input from the high level d-c converter is applied in series with a zener diode to the base of an NPN transistor. The circuit may be connected with the emitter grounded; or, alternately, the circuit may be used as an emitter follower. In the first case, the output is called WC', and in the second it is called WC. Since true signals from the high level d-c converters are at +15 volts, the write control circuit, when the emitter is grounded, produces a WC' output of +1 volt. The WC output of the circuit, functioning as an emitter follower, when driven by a true WCj signal of +15 volts, is approximately +8 volts. Conversely, a false or +1 input at WCj produces from the grounded emitter circuit a WC' output of +15 volts and a WC output, from the emitter follower connection, of -5 volts. Four such circuits are mounted on a single insert card.

The system can be explained by examining operation during an instruction to store the A register in one of the general storage tracks to which the track

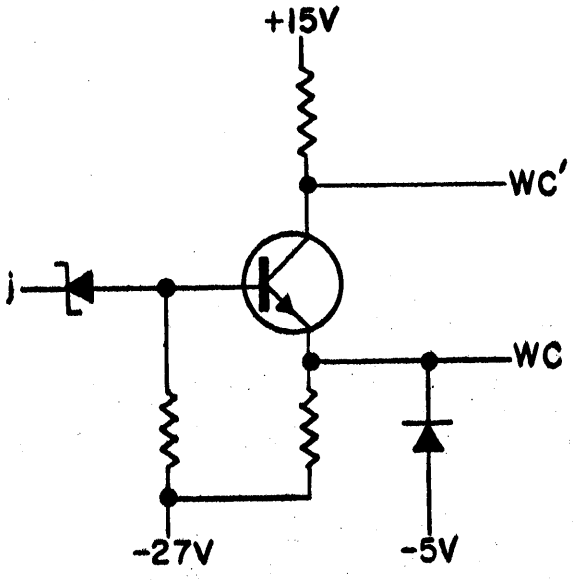


Figure 3-10.
Write Control Circuit, Schematic

selector plug is connected (other than track 62). The true output of DCA produces a 1 volt signal driving the second write control circuit, WC10. This circuit connected as an emitter follower produces a -5 volt bias, applied to a gating network called the memory control portion of the system.

The presence of the -5 volt bias on the memory control input gate permits the transfer of the signal from the A register read circuit to an isolation amplifier circuit which also accepts the output of the B register read circuit if such output has passed the appropriate input gate.

In addition to being applied to the write control circuit, WC9, the DCA signal is "anded" with a DC63 signal and applied to a second write control system. Gating illustrated schematically at the left of figure 3-11 drives an emitter follower which is cut off when DC63 is not present. Since in the example being discussed, the DC63 signal would not be present, write control circuit WC13, driven by the false +1 volt output of the emitter follower, produces -5 volts out.

Output from the read circuit for the 16-word circulating register, R63, would be permitted to pass through the memory control circuit to be applied to the write circuit for track 62, W63. The DC63 signal also drives write control WC16, which generates the signal permitting the output of the isolating amplifier to be transferred into the general storage writing system.

In the case where the contents of either the A register or the B register is to be stored on track 63, conduction in the emitter follower produces a +15 volt signal at WC14 and WC13, resulting in a +8 volt output from WC13, preventing transfer of the signals from the 16-word circulating register read circuit into the writing circuitry and permitting the output of the isolation amplifier to be transferred into the input of W63. The read circuit in all cases is that shown in figure 2-16 and described in paragraph 2-2d(4).

In figure 3-12, the writing circuit system is shown. Since only one of a group of eight tracks may be addressed, under any given position of the track selector plug, the three least significant digits of the track number, as generated by the M flip flops, are used to generate d-c control signals for the writing

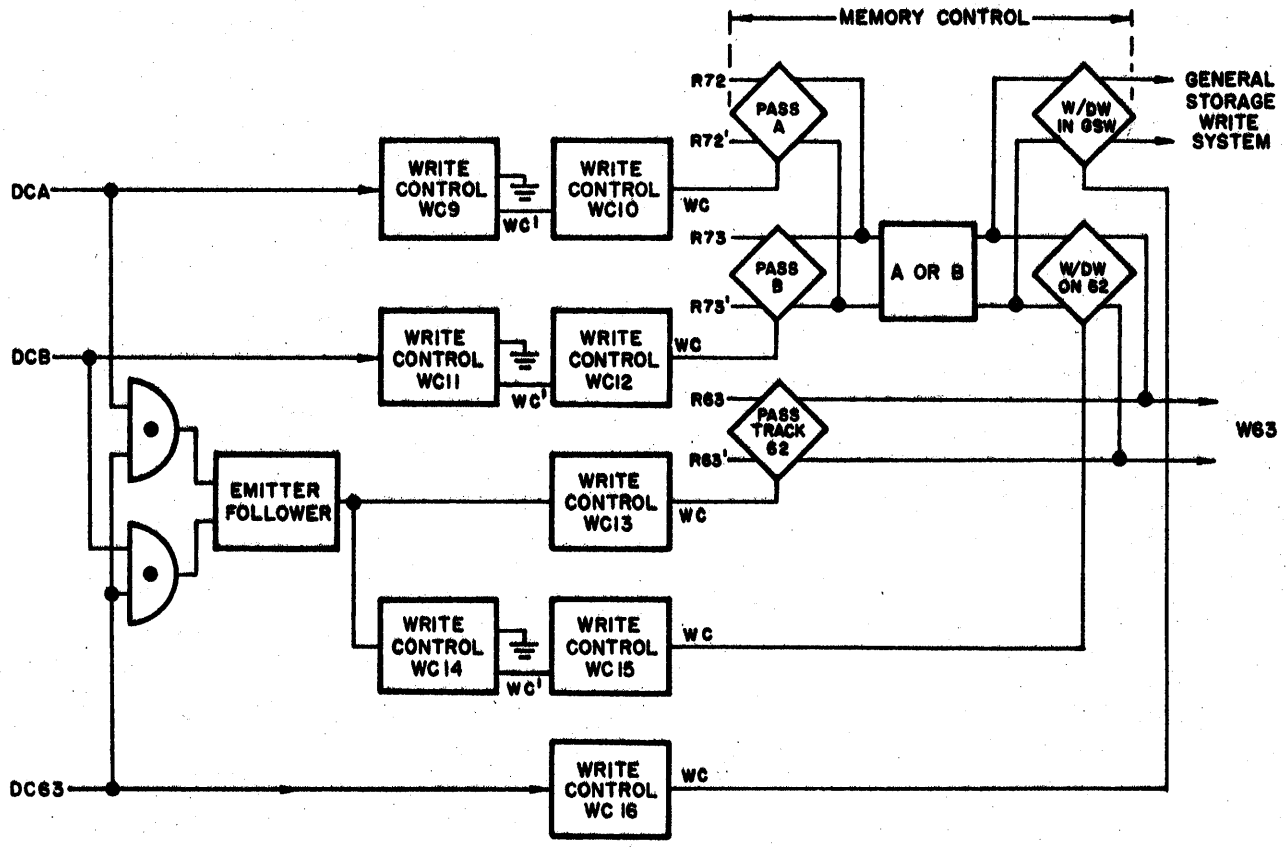


Figure 3-11. Write Control System, Block Diagram

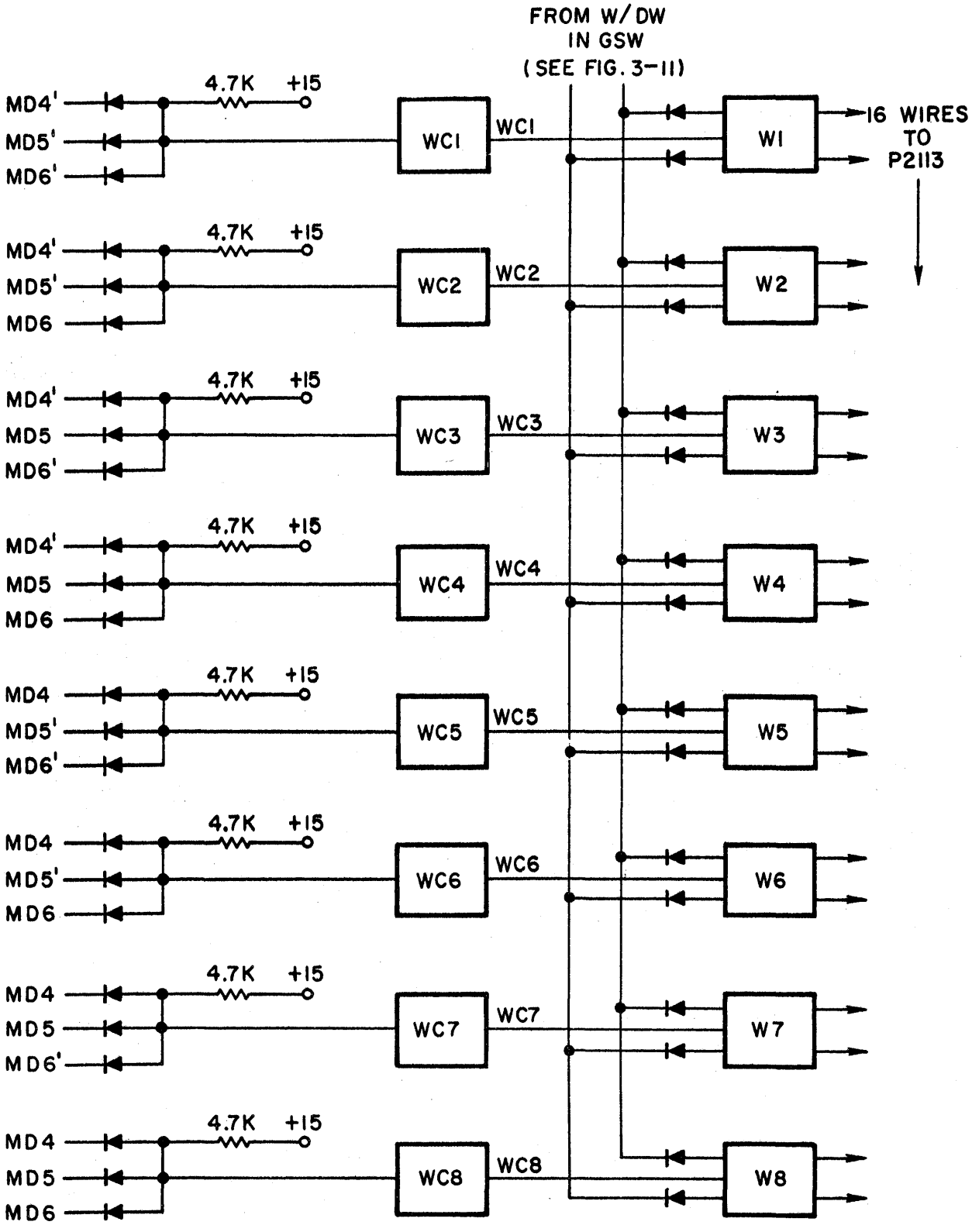


Figure 3-12. Writing Circuits System, Block Diagram

circuits gating. As shown in figure 3-12, the gating accepting these signals is conventional and produces output only when all three signals are present. A true output from one of the associated write control circuits drives one of the write circuits, each of which is a power amplifier, described in paragraph 2-2d(2).

The writing current generated in one of these power amplifiers is transferred through the track selector plug (P2113) and the connector into which it is plugged, to the correct head on the magnetic drum surface. Normally, P2113 is connected to tracks 0 through 7, since each of these is equipped with a separate write head and is therefore normally addressable.

A set of writing plug position identification signals are presented to the track selector plug when mated with each of the jacks. These signals are called Z6, Z6', Z7, Z7', Z8, and Z8'. The signal group identifying each track group, and the selection signals are listed below:

Track Group

0 through 7: Z6' Z7' Z8' identify plug position, M1' M2' M3' are selection signals.
8 through 15: Z6' Z7' Z8 identify plug position, M1' M2' M3 are selection signals.
16 through 23: Z6' Z7 Z8' identify plug position, M1' M2 M3' are selection signals.
24 through 31: Z6' Z7 Z8 identify plug position, M1' M2 M3 are selection signals.
32 through 39: Z6 Z7' Z8' identify plug position, M1 M2' M3' are selection signals.
40 through 47: Z6 Z7' Z8 identify plug position, M1 M2' M3 are selection signals.
48 through 55: Z6 Z7 Z8' identify plug position, M1 M2 M3' are selection signals.
56 through 63: Z6 Z7 Z8 identify plug position, M1 M2 M3 are selection signals.

By virtue of the identification signals produced when the track selector plug is mated into one of the track group connectors, writing into any track other than the group of eight so specified is avoided. However, track 62 may be addressed at any time.

In a store instruction, the identification signals are compared with the track selection signals and the track number compared with the identification for track 62 in order to prevent recording in a track in which it is either impossible or undesirable to write. Should inequality be obtained during this inspection, the RECORD ERROR light is illuminated.

To permit writing into tracks 8 through 15 under program control (normally written into under control of the analog input/output equipment) it is necessary to modify the drive to the RECORD ERROR matrix amplifier J1 and the input to the "store" sector number matrix amplifier, J9. For tracks 0 through 7, the "store" sector number is read from R67 while in the remaining tracks, the "store" sector number is read from R66.

A single pole, double throw toggle switch on the track selector panel is wired in series with the winding of a relay mounted in the read selection unit. The write

circuits for tracks 0 and 7 are connected through contacts on the relay. The relay is placed in open circuit, or off position, prior to starting the Computer in order that any information on these two tracks should not be erased accidentally by a power surge or instantaneous accidental setting of the flip flops to effect an erasure. The switch can be paralleled by one on a remote control panel, if desired.

3-3. ARITHMETIC AND CONTROL FUNCTIONS.

The portion of the RW-300 Digital Control Computer which accomplishes computation is called the Arithmetic and Control unit and comprises the modules listed below (the locations of which are indicated in figure 3-9):

a. Digit counter, module 101, a set of flip flops triggered by clock pulses and counting digit times to synchronize operation of the Computer;

b. State counter, module 102, a set of flip flops controlling the sequence of instruction execution within each Computer operation;

c. Instruction register, module 103, a set of flip flops used primarily to store the binary equivalent of the instruction code number in the instruction being executed;

d. Track register, modules 104 and 105, a set of flip flops and associated high level d-c converters used for track number storage and miscellaneous identification signals;

e. A register, module 106, the accumulator;

f. B register, module 107, the auxiliary circulating register;

g. N and Y register, module 108, in which the next instruction address and operand address, respectively, are circulated;

h. Adder, module 109, matrix amplifiers accepting two sets of digits to be summed and incorporating, in a feedback loop, a flip flop storing the carried digit and another storing the overflow digit;

i. Equality, module 110, which provides the principal condition for advance in the instruction execution; and,

j. C register, module 114, the multipurpose, non-addressable circulating register used for temporary storage, equality inspection, and transfer between other circulating registers and counters.

3-3a. MODULE CIRCUITRY. To explain the operation of the arithmetic and control equipment, the following paragraphs describe the individual circuits comprising the modules listed above. Actual performance requires complex signal paths, changing between digit times and therefore not conveniently presented as block diagrams. Reference should be made to the master functional block diagram, 3-23. Gating for the various flip flops and matrix amplifier insert cards described in conjunction with each module is formed on the module boards and on insert cards.

3-3a(1). Digit Counter (Module 101). The digit counter provides identification of individual digit times or groups of digit times significant to the functional sequence of the Computer. By utilizing nine flip flops, rather than the five which would be required for binary representation of any of the 20 possible digit times, recognition of the necessary digit times is, in most cases, offered by combinations of two or three signals, thus simplifying the gating into Computer circuits requiring digit time synchronization. The digit counter flip flops are T1 through T9. The nine flip flops are interconnected as a counter passing through a total of 14 successive combinations representing the required digit times or digit time groups. The state of each of the flip flops for each of the digit times or digit time groups is listed in figure 3-13. The counting sequence provides that only one of the nine flip flops must change state to effect the change to the next desired digit time or digit time group. Obviously, the nine flip flops are capable of more than 1000 different combinations. However, any initial random setting, while not recognized as a particular digit time, would contain terms producing one of the digit time conditions, thus triggering automatic counting. Counting will synchronize with the drum as a result of the introduction of the signal from the sector number track. As mentioned in paragraph 3-2a, the sector track bears, in the first seven bits of each sector, the number of that sector, expressed in binary form. In bits 13 and 16 of each sector, a "1" is recorded; while, in all sectors other than 127, a "1" is recorded in bit 20. Both the digit counter in the arithmetic and control group and the separate digit counter in the analog input-output equipment use bits 13, 16, and 20 for synchronizing signals.

The counting sequence may be examined by referring to figure 3-13, the table indicating the output of each of the digit counter flip flops. Assume that the flip flops may have randomly achieved the output states listed as digit 1. In order to advance to digit 2, T4 must go true. T4 is designed to go true on the next digit time following the one in which it went false. Similarly, advancing to digit time 3 requires that T3 go from false to true, a condition created by true outputs from either T2 T4 T5 or T1' T5. Since, at digit time 2, T2 T4 and T5 are true, the counter may advance to digit time 3. The sequence of counting may be continued through digit time 8. In order to advance beyond digit time 8, the counter must receive a false T3 signal, which was generated by the T5' output during digit time 8. Advancing beyond the digit time group 9-13 requires that T7 go false. A true signal must be obtained from the sector number track and applied to the k input of T7 in order to step the counter to the digit time 14-16 group. This term

is available at bits 13 and 16 on the sector number track. Should the digit time group 9-13 be set up by a true signal at some other bit in the sector number track (bits 1 through 7, or 20), counting will fail to synchronize on the next successive sector. However, counting automatically synchronizes in one drum revolution or less, following application of clock pulses to the Computer.

The simple recognition signals listed at the right of figure 3-13 are those which can be introduced into the gating for the remainder of the arithmetic and control circuits.

High level flip flops, as described in paragraph 2-2d(1), are necessary for T2, T5, and T7 to satisfy gating requirements resulting from the duty cycle of the circuits. Low level flip flops, described in paragraph 2-2b, are suitable for T1, T3, T4, and T6. They are also used, in conjunction with separate power amplifiers described in paragraph 2-2d(2), to provide the duty cycle required for T8 and T9.

Mounted in the digit counter module is the reference flip flop, Z1, which also accepts the output of the sector number track read circuit. The first true signal to appear at Z1j following synchronization of the Computer sets Z1 true, the status in which it remains as long as power is applied to the equipment. This output can then be used as a reference for the remainder of the Computer. Z1 output is applied to circuits in which it is necessary to convert from the normal a-c signal to a d-c signal, as used in the high level d-c converters associated with the track register and the write control circuitry.

Output of Digit Counter Flip Flops T1	T2	T3	T4	T5	T6	T7	T8	T9	Digit Time or Digit Time Group	Recognition Signal
1	1	0	0	1	1	1	1	1	1	T4'
1	1	0	1	1	1	1	1	1	2	T1 T2 T3' T4
1	1	1	1	1	1	1	1	1	3	T2 T3
1	0	1	1	1	1	1	1	1	4	T1 T2' T3
1	0	0	1	1	1	1	1	1	5	T1 T2' T3'
0	0	0	1	1	1	1	1	1	6	T1' T3' T5
0	0	1	1	1	1	1	1	1	7	T1' T3 T5
0	0	1	1	0	1	1	1	1	8	T3 T5' T7
0	0	0	1	0	1	1	1	1	9-13	T3' T5' T7
0	0	0	1	0	1	0	1	1	14-16	T6 T7'
0	0	0	1	0	0	0	1	1	17	T6' T9
0	0	0	1	0	0	0	1	0	18	T8 T9'
0	0	0	1	0	0	0	0	0	19	T2' T8' T9'
0	1	0	1	0	0	0	0	0	20	T2 T9'
									1-18	T8
									1-17	T9
									18-20	T9'
									2-17	T4 T9
									1-16	T6
									2-18	T4 T8
									1-7	T5
									1-5	T1
									8-13	T5' T7
									1-13	T7
									14-18	T7' T8
									17-20	T6'
									9-16	T3' T5' T6
									4-19	T2'

Figure 3-13. Digit Identification

3-3a(2). State Counter (Module 102). Gross timing in the Computer is effected through the state counter. The state counter consists of three flip flops which are set on the basis of conditions occurring during the execution of the various instructions and which, in turn, produce identification signals advancing the sequence of the execution. Figure 3-14 lists the condition of each of the three flip flops during each of the eight states. Since only three flip flops are employed, all must be used to identify a given state. However, the code representing the conditions required for each state has been established to require a change in the output of only one of the three flip flops to achieve the conditions for the next successive state. A change from state 8 to state 1 requires a change in the output of each of the state counter flip flops. The application of the state counter is detailed in the functional description of instruction execution found in paragraph 3-3b.

High level flip flops, described in paragraph 2-2d(1), are used in conjunction with power amplifiers (write circuits of figure 2-14) to provide output signal levels sufficient to drive the required gates.

3-3a(3). Instruction Register (Module 103). The flip flops which store the instruction code are called the instruction register. Binary digits representing the instruction code in an instruction group--two consecutive sectors, as detailed in paragraph 1-2b(2)--are transmitted through R1, the general storage read amplifier, during digit times 14 through 18 of the second sector of the pair and appear at P1 in the instruction counter, least significant digit first. Each digit is stepped through the instruction counter (P) flip flops. At the end of digit time 18, therefore, the most significant digit of the instruction code is stored in P1 and the least significant digit, in P5.

State Number	Output of State Flip Flops S1	S2	S3	Recognition Signal
1	1	1	0	S1 S2 S3'
2	1	0	0	S1 S2' S3'
3	1	0	1	S1 S2' S3
4	1	1	1	S1 S2 S3
5	0	1	1	S1' S2 S3
6	0	1	0	S1' S2 S3'
7	0	0	0	S1' S2' S3'
8	0	0	1	S1' S2' S3

Figure 3-14. State Identification

The instruction code is established for efficient and non-ambiguous recognition by the set of five flip flops. Since there are only 19 different instructions, only three of these five instruction counter flip flops are necessary to recognize a given instruction. Figure 3-15 provides the list of instructions, abbreviations, decimal code numbers (used in programming by means of a Flexowriter), the output signal from each of the five instruction counter flip flops (which is also the binary code number), and the recognition signal.

When not storing the instruction code, the P flip flops hold the execution time--contained in the corresponding digits of the first sector of an instruction pair. The application of the flip flops is described with respect to functional grouping in paragraph 3-3b.

Low level flip flops, described in paragraph 2-2b, are used in association with power amplifiers, described in paragraph 2-2d(2), for all of the instruction counter flip flops with the exception of P5, which uses a high level flip flop. See paragraph 2-2d(1).

3-3a(4). Track Register (Modules 104 and 105). The multiple functions performed by the six flip flops comprising the track register are detailed in paragraph 3-3b, describing the functional groupings with respect to instruction execution. Principally, the flip flops store, in serial register technique, the track number of the next instruction address or of the operand address. Since the track identification is contained in bits 8 through 13 of the sector, the contents of the drum storage location are shifted into the M flip flops during digit times 8 through 13, least significant digit entering M1 first. Therefore, at the end of digit time 13, M6 contains the least significant digit of the desired track number, while M1 contains the most significant digit of the track number.

In addition to accepting the serial output from other registers, the track register is designed to count down automatically to 00000 from the status stored during the digital input command. During the count down, digital input lines are sampled serially, as described in paragraph 3-4a.

Track register flip flops are also used in the digital communication command to specify input or output functions, type or non-type operation, and/or the address selecting the desired group of input or output lines. Flip flop M1 is used during multiplication and division instructions for miscellaneous digit storage and control, as more thoroughly described in paragraph 3-3b.

The track register also stores the "type of shift" and "type of switch" in these commands.

The d-c gating control needed by the Read Selection unit and write circuits is generated in MD1 through MD6 (and their complements). The basic circuit of the high level d-c converters used

Description	Abbr.	Code Number	Instruction Register Flip Flops P1	P2	P3	P4	P5	Recognition Signal
Add	A	31	1	1	0	0	1	P1 P3' P5
Subtract	S	30	1	1	0	0	0	P2 P4' P5'
Multiply	M	20	1	0	0	0	0	P1 P2' P3'
Divide	D	32	1	1	0	1	0	P1 P3' P4
Load A	LA	35	1	1	1	0	1	P2 P3 P4'
Load A Negative	LN	25	1	0	1	0	1	P1 P2' P5
Extract	EX	05	0	0	1	0	1	P1' P3 P4'
Load B	LB	07	0	0	1	1	1	P2' P4 P5
Store A	SA	36	1	1	1	1	0	P2 P3 P5'
Store B	SB	24	1	0	1	0	0	P3 P4' P5'
Shift	SH	01	0	0	0	0	1	P2' P3' P5
Transfer on Negative	TN	11	0	1	0	0	1	P1' P2 P4'
Transfer on Zero	TZ	13	0	1	0	1	1	P3' P4 P5
Digital Input or Output	DG	06	0	0	1	1	0	P1' P3 P5'
Merge	MG	37	1	1	1	1	1	P1 P4 P5
Compare Magnitude	CM	17	0	1	1	1	1	P1' P2 P3
Transfer on Overflow	TF	12	0	1	0	1	0	P1' P2 P5'
Switch	SW	02	0	0	0	1	0	P2' P3' P4
Stop	SP	00	0	0	0	0	0	P1' P2' P5'

Figure 3-15. Instruction Code

for MD1 through MD6 is discussed in paragraph 2-2d(5).

Application of the high level d-c converters for read head selection is similar to that in the generation of the signals controlling writing from one of the circulating registers into one of the general storage tracks or into track 62, as described in paragraph 3-2c. MD1 is true during the entire digit time in which M1 is true since both M1 Z1 and M1' Z1' are applied to the input of the converter. Hence, although the true signal is a-c in character, and the positive half cycle produces no output from the gate, the negative half cycle of the false complement signal produces gate output and therefore input to the converter.

The MD1' converter is driven by M1' Z1 and M1 Z1'. During the half cycle in which M1 is true, M1' is false. "Anded" to Z1, M1' presents the appropriate false input to the MD1' converter during the half cycle in which M1 is true. During the half cycle in which M1 is positive, the positive half cycle of Z1 prevents the appearance of a true input from M1' to the converter. Thus, while MD1 is true, MD1' is false. These high level d-c converters are mounted in the track register modules. Each of the track register flip flops is a high level flip flop, described in paragraph 2-2d(1).

Installed in module 104 is the matrix amplifier, J1, used as part of the signal necessary to actuate the RECORD ERROR light. J1 checks the three least significant track digits versus the plug position signals, Z6, Z7, and Z8, as described in paragraph 3-2c. The RECORD ERROR indicator is illuminated when any attempt is made to write into an unaddressable track--either the program loading track or one not connected to the write amplifiers.

3-3a(5). A Register (Module 106). Figure 3-16 is a simplified block diagram of the one-word circulating A register. As described in paragraph 3-2a(2), a dual head is used on this track. The signal detected from the track appears at R72, a read circuit such as that described in paragraph 2-2d(4), in which shaping and amplification is accomplished. Further amplification is provided by power amplifier WA1, described in paragraph 2-2d(2). To lengthen the 19-bit A register to 20 bits, an additional high level flip flop, described in paragraph 2-2d(1), is provided. However, this circuit may be bypassed, thus the 19-bit word length automatically accomplishes a one-bit right shift. The principal A register flip flop is a delay type, such as described in paragraph 2-2d(3), which is used to drive the power amplifier applying the writing signal to the circulating register write head.

3-3a(6). B Register (Module 107). The B register, also a 19-bit circulating register employing a dual head, is virtually identical to the A register. Output from B register read circuit R73 can drive directly the principal B register flip flop, a delay flip flop such as described in paragraph 2-2d(3), or can drive register lengthening flip flop BL, a high level flip flop described in paragraph 2-2d(1). Logic cards in association with circuitry on the module board itself, provide the necessary gating.

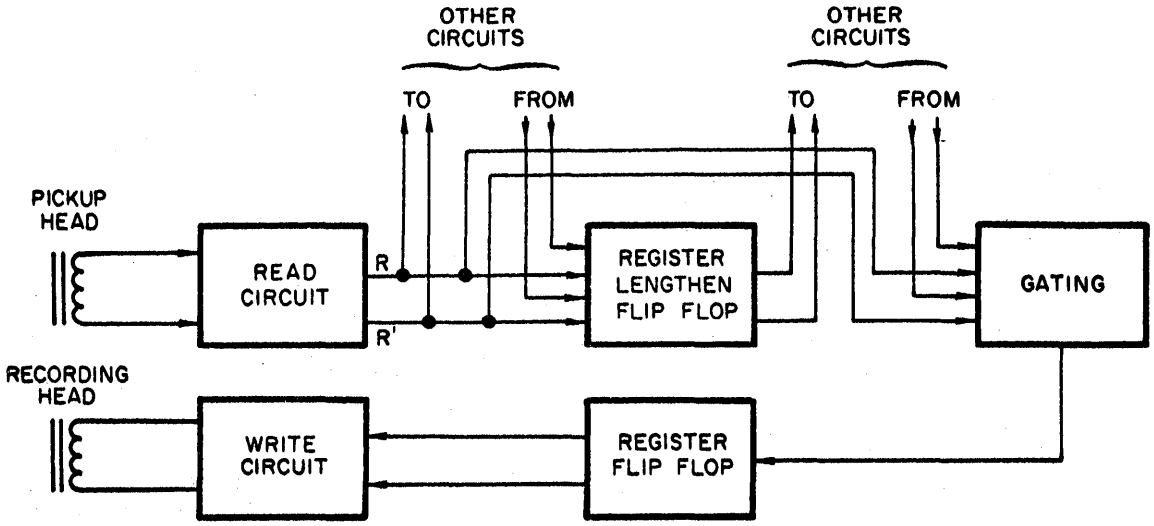


Figure 3-16. Typical 19-Bit Circulating Register, Block Diagram

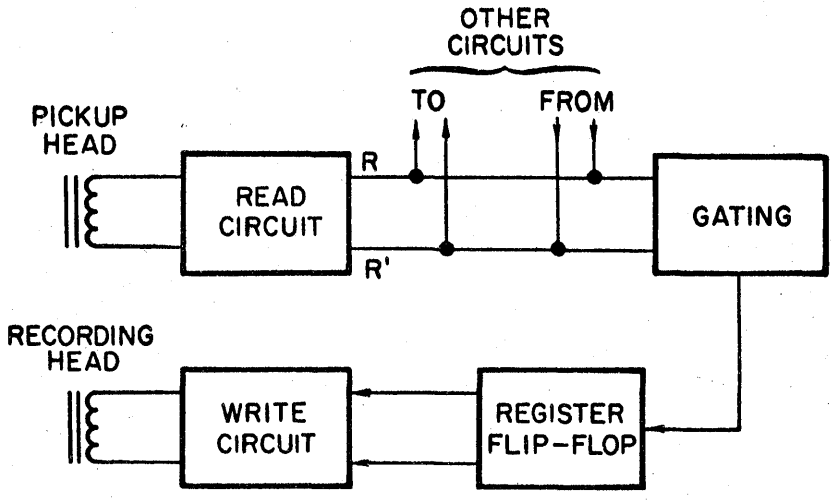


Figure 3-17. Typical 20-Bit Circulating Register, Block Diagram

3-3a(7). N and Y Registers (Module 108). The next instruction address (N) register and the operand address (Y) register are located in module 108. The N register accepts the next instruction address, contained in bits 1 through 13 of the second word of an instruction pair, from general storage read. In state 8, START and LOAD buttons cause a series of 1's or 0's to be recorded in the N register by track register flip flops M1 and M2 to establish the location from which the next instruction is to be read.

The Y register recirculates

a. The operand address;
b. the pseudo address created by the addition of execution time digits to the operand address sector number digits; or
c. the alternate address in a transfer instruction.

Each is a one-word 20-bit circulating register utilizing a dual head and a circuit similar to the simplified block diagram of figure 3-17. Output from the read head drives a read circuit, as described in paragraph 2-2d(4). The read circuit output may be applied to other registers or to the input logic for the register flip flop, a delay type described in paragraph 2-2d(3). The register flip flop drives the associated write circuit, a power amplifier as discussed in paragraph 2-2d(2), and therefore the recording head.

3-3a(8). Serial Adder (Module 109). Arithmetic computation is accomplished in the serial adder circuitry. A simplified block diagram of the adder is offered in figure 3-18. The binary digits to be added are serially presented to the input matrix amplifiers J6 and J7, described in paragraph 2-2d(6). "And" gating accepts the outputs of these two amplifiers for presentation to the carry flip flop, Z4 -- a low level flip flop such as described in paragraph 2-2b--and to the sum flip flop, J8, also a matrix amplifier. The inherent one digit delay in the carry flip flop results in the application of the carry digit to the "and" gates actually performing the summing (at the input of J8) simultaneously with the presentation the next succeeding digit from the adder inputs.

Since a 1 in the most significant bit of each of the numbers being added could result in a carry into a digit position not available, output of the carry flip flop also is used during certain operations to set the gating which drives the overflow indicator flip flop. This latter flip flop is mounted in the equality module.

Since two matrix amplifier circuits are mounted on each such insert card, the extra amplifier (J2) on the card bearing J7 is used to generate the "not track 62" signal which forms part of the drive to the RECORD ERROR indicator.

3-3a(9). Equality (Module 110). The equality flip flop is used to inspect sector numbers relative to the sector required during various phases of instruction processing and to store the "ready" signal associated with digital input/output. The flip flop is set true at digit time 20 (the first bit) of state 1, and is turned off at any inequality in the applied digits during the search for the next instruction address. Sampled at digit time 19 of the sector, the output is set true at the next bit in preparation for inspection of the digits in the next sector number. A similar condition is set up during search for operand addresses and pseudo addresses generated in certain instructions. Also located on the equality module is the matrix amplifier, J9, producing the "store" sector number signal used in store instructions. When the output of J9 designates the "store" sector, equality of the output of J9 and the sector number permits recording, since the desired sector (in tracks 0-7) is then under the writing head.

A low level flip flop, as described in paragraph 2-2b, is used as the overflow indicator Z2, also mounted in the equality module. Set by overflow digits in addition, division, and shift left instruction, Z2 is reset only by a transfer on overflow instruction.

3-3a(10). C Register (Module 114). A 20-bit one-word circulating register called the C register functions as an auxiliary revolver and storage location employed by the Computer in the course of instruction execution. Figure 3-17, the block diagram of the 20-bit circulating registers, applies to the C register as well as to the N and Y registers. A delay flip flop, discussed in paragraph 2-2d(3), a read circuit, described in paragraph 2-2d(4), and a write circuit, in paragraph 2-2d(2), comprise the C register circuitry in conjunction with a dual head revolver track on the drum. The module also supports the read

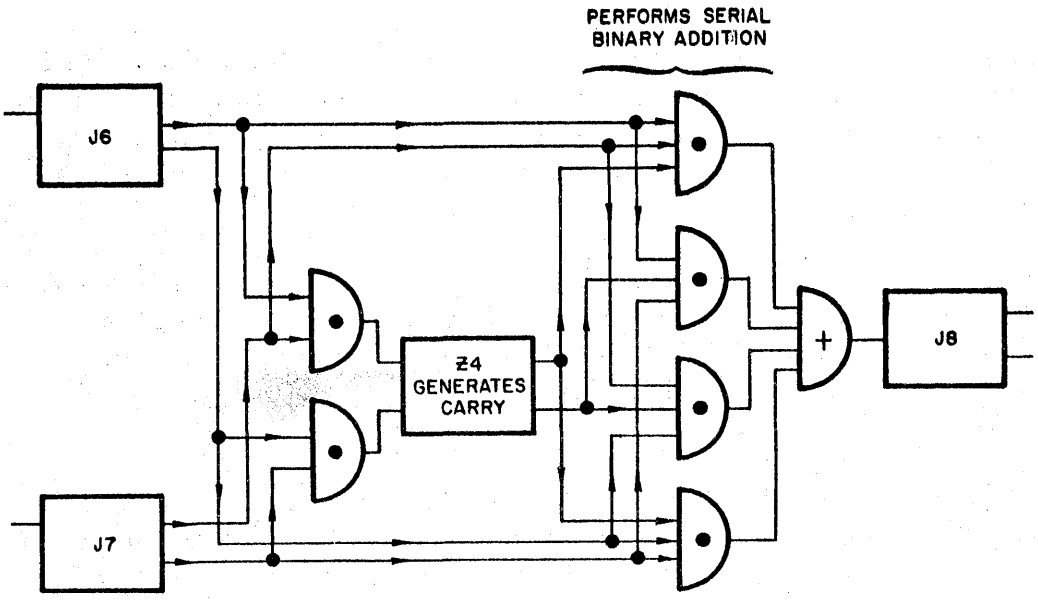


Figure 3-18. Adder Circuits, Simplified Block Diagram

circuits for the analog data head on track 7, the "store" sector number, the sector number, the 16-word circulating register, the general storage, and the clock. Relay drivers RD1, RD2, and RD3 are also located in this module. Their function is described in paragraph 3-4.

3-3b. FUNCTIONAL GROUPING. The application of the circuits described in the previous paragraphs must be explained on the basis of the functions performed by the various circuits in the course of executing each of the instructions for which the machine is designed. Figure 3-23 should be used as an aid to following the descriptions.

3-3b(1). General Conditions. Instructions are executed in a sequence controlled by the state counter. Most instructions are accomplished in sequences of five or six states. However, a total of eight states are available to provide the sequence necessary for certain complex instructions. The change from one state to the next occurs at digit time 19 when required conditions are met. Each state therefore begins at digit time 20 of a sector. The functions performed in each state and the length of time required for completion of the state are as follows:

a. State 1, completed in a minimum of one word time, in which the sector specified as the next instruction address in the previous instruction is located and the track number is stored in the M flip flops, and in which the Computer idles if the **EXECUTE** button has been depressed;

b. State 2, completed in one word time, in which the first word of an instruction pair is read, the information in the M flip flops being used to actuate the gating of the read head selection unit to permit transfer of the operand address into the Y register and of the execution time digits into the instruction counter;

c. State 3, completed in one word time, in which the second word of the instruction pair is read, the next instruction address being stored in the N register, the execution time being shifted into the C register, and the instruction code digits being shifted into the P flip flops;

d. State 4, completed in a minimum of one word time as the operand address is located (instructions not requiring an operand omit state 4 unless the **FETCH** button is pressed) and in which the machine idles if the **FETCH** button has been pressed or if the external digital equipment is not yet ready;

e. State 5, completed in one word time, in which the operand is manipulated and some instructions are completed (see details of individual instructions in subsequent paragraphs);

f. State 6, completed in a minimum of one word time, in which other instructions are completed;

g. State 7, completed in a minimum of one word time, in which the remaining instructions are completed; and,

h. State 8, in which the machine idles if instructed to stop or if START, LOAD, or STOP button has been pressed, or if a RECORD ERROR has occurred.

3-3b(2). All Instructions. To execute any of the 19 possible instructions, listed in paragraph 3-3a(3), the RW-300 must cycle through the first three states. The Computer can be placed in state 1 automatically upon completion of each instruction, or manually by pressing the RESUME or EXECUTE buttons following suspension of automatic instruction processing. During digit times 1 through 7 of state 1, the sector number track and N register outputs are applied to the equality flip flop in order to search for the desired next instruction sector. During digit times 8 through 13, the N register output is introduced in the track register flip flops. M1 initially receives the least significant track number digit, which was stored in bit 8 of the N register. Counting proceeds until, at digit time 13, M6 contains the least significant track number digit.

During digit times 1 through 18, the A and B registers, which may contain the previous instruction data or results, are recirculated at 20-bit lengths. The operand address (Y) register and C register are not recirculating, however. At digit time 19, if the desired sector number has been found, a true output from the equality flip flop is generated. Thus, conditions necessary for the state counter to assume the state 2 configuration are completed (as long as the EXECUTE button has not been pressed). The Computer remains in state 1 until the desired sector is obtained.

During digit times 1 through 13 of state 2, the signals from the M flip flops, now containing the desired track number, drive the high level d-c converters which control the output of the read selection unit. The signal from the required track, therefore appears at the output of general storage read. Simultaneously, this information is recorded on the Y register (the operand address register). The execution time information, stored in bits 14 through 18 of the first word of an instruction pair, is stepped from general storage read into the instruction register (P flip flops) during digit times 14 through 18. During digit times 1 through 18, A and B registers recirculate at 20 bits. At digit time 19, the Computer automatically changes to state 3.

In state 3, the second word of an instruction pair is read and stored. During digit times 1 through 13, the next instruction address is shifted into the N register. During digit times 1 through 5, the execution time previously stored in the instruction register is copied onto the C register. Hence, during

digit times 14 through 18 of state 3, the instruction register receives the new instruction code. During digit times 6 through 18, the C register is recirculated. During digit times 1 through 18, the A, B, N, and Y registers recirculate. At digit time 19, the Computer automatically changes to state 4.

In state 4, variations in the sequence of instruction execution begin. These variations are described in the following paragraphs, with respect to completion of the cycle for each of the possible instructions. Figure 3-23 graphically illustrates instructions processed in each state.

3-3b(3). Instruction 31 (Addition). Instruction 31, represented by the binary code number 11001, accomplishes addition of the contents of the drum storage location specified, to the contents of the accumulator. The sum then appears in the accumulator. The sign of the A register depends on magnitudes and signs of the operands. Addition of two operands of like sign takes a minimum of six word times. Addition of operands of unlike sign may take a minimum of six or seven word times. Contents of the B register are not disturbed.

NOTE

The time to execute an instruction is made up of the necessary manipulations and/or arithmetic time plus the time to find the instruction and the time to find the operand. Each of these search times has been given the minimum value of one in the minimum times cited in these paragraphs.

The search for the operand address takes place in state 4. During digit times 1 through 7, the output of the Y register is compared with the incoming sector number at the equality flip flop. During digit times 8 through 13, the operand address is copied from the Y register into the M flip flops. Equality between operand address and sector number, sampled at digit time 19, represents location of the desired sector and, unless the FETCH button has been pressed, the Computer will automatically go into state 5. At the same time, the carry flip flop is set to zero in preparation for the arithmetic addition. A, B, Y, N, and C registers remain at 20 bits and recirculating during digit times 1 through 18.

Figure 3-19 provides a few examples of addition as mechanized by the Computer. In state 5, the data contained in the desired drum location is copied into the C register during digit times 1 through 17. At digit time 18, the sign of the operand is compared with the sign of the A register. The Computer automatically changes to the subtract function (see paragraph 3-3b(4)) if the contents of the storage location bear the opposite sign from the A register. In this case, at digit time 19, the carry flip flop is set to a one to effect the complement addition. In either case, at digit time 19, the Computer automatically changes to state 6. During digit times 1 through 18, the A, B, C, N and Y registers remain at 20 bits and recirculating.

Arithmetic addition is actually accomplished in state 6 during digit times 1 through 17 as the output from the A register lengthen flip flop is applied to the J6 input of the adder, while the output from the C register is applied to the J7 input of the adder. The sum appearing at the output, J8, is then introduced into the A register flip flop for storage on the A register. (Review paragraph 3-3a(8) which describes the adder circuitry and the carry flip flop.) In digit time 17, the carry flip flop, if set to 1, sets the overflow flip flop, Z2 at digit time 18. At digit time 19, with the completion of the addition, the Computer returns to state 1 automatically.

3-3b(4). Instruction 30 (Subtraction). Instruction 30, the binary code number of which is 11000, effects the subtraction of the contents of the desired storage location from the contents of the A register. The difference appears in the A register while the contents of the B register are undisturbed. Subtraction of two operands of unlike sign requires a minimum of six word-times. Subtraction of operands of like sign may take a minimum of six or seven word-times.

EX.	CONTENTS OF A	CONTENTS OF m	BINARY SUM
1	+11011	+10010	+101101
2	-11011	+10010	-01001
3	+11011	-10010	+01001
4	-11011	-10010	-101101
5	+10010	-11011	-01001
6	-10010	-11011	-101101

LIKE SIGNS (DATA LISTED AS EX. 1, 4, AND 6)

State 5: Set Z4 to 0
State 6: Add (A) and (m), and use sign of (A)

Ex. 1:	Ex. 4:	Ex. 6:
+11011	-11011	-10010
+10010	-10010	-11011
+101101	-101101	-101101
(A) = +01101 with overflow	(A) = -01101 with overflow	(A) = -01101 with overflow

UNLIKE SIGNS (DATA LISTED AS EX. 2, 3, AND 5)

State 5: Set Z4 to 1, change to subtract
State 6: Add Z4, (A), and (m)', and use sign of (A)

If (A) > (m), overflow occurs but is ignored

Ex. 2:	Ex. 3:
1	1
-11011	+11011
+01101	-01101
101001	101001
(A) = -01001	(A) = +01001

If (m) > (A), no overflow; state 7 required

Ex. 5:
1
+10010
-00100
(A) = +10111

State 7: Add 1 in least significant digit to (A)', and complement sign of (A)

Ex. 5 cont:
1
01000
01001
(A) = -01001

Figure 3-19. Addition

As in addition, the search for the operand address is accomplished in state 4. During digit times 1 through 7, the output of the Y register is compared with the incoming sector number at the equality flip flop. The operand address track number is shifted into the M flip flops from the Y register during digit times 8 through 13. At digit time 19, the output of the equality flip flop is sampled. True output causes the state counter to step into state 5, if the FETCH button has not been pressed. The carry flip flop is again set to zero in preparation for arithmetic operations. Twenty-bit circulation is maintained in the A, B, C, N, and Y registers during digit times 1 through 18.

In state 5, the data from the desired drum location is copied into the C register during digit times 1 through 17. The instruction code to subtract produces a comparison between the sign of the drum storage location and that of the A register, at digit time 18. When the signs are unlike, the Computer automat-

ically changes to addition through the setting, at digit time 19, of the carry flip flop to 0. Regardless of the sign, the Computer changes to state 6 at digit time 19. During digit times 1 through 18, the A, B, C, N, and Y registers are 20 bits and recirculating.

During digit times 1 through 18 in state 6, the A, B, C, N, and Y registers remain at 20 bits and recirculating. During digit times 1 through 17, if the Computer has automatically shifted to an add instruction as the result of unlike signs in (A) and (m), the output of the A lengthen flip flop is applied to J6; the output of the C register is introduced into the alternate input for the adder, J7; and the output of the adder, J8, is applied to the A register flip flop during digit times 1 through 17. A 1 out of the carry flip flop at digit time 18 sets the overflow flip flop and the Computer returns to state 1 at digit time 19.

EX.	CONTENTS OF A	CONTENTS OF m	BINARY DIFF.
1	+11011	+10010	+01001
2	-11011	+10010	-101101
3	+11011	-10010	+101101
4	-11011	-10010	-01001
5	+10010	-11011	+101101
6	-10010	-11011	+01001

LIKE SIGNS (DATA LISTED AS EX. 1, 4, AND 6)

State 5: Set Z4 to 1
State 6: Add Z4, (A), and (m)', and use sign of (A)

If (A) > (m), overflow occurs but is ignored

```
Ex. 1:      1          Ex. 4:      1
          +11011                 -11011
          +01101                 -01101
          ------                 ------
          101001                 101001
  (A) = +01001           (A) = -01001
```

If (A) < (m), no overflow; state 7 required

```
Ex. 6:      1
          -10010
          -00100
          ------
  (A) = -10111
```

State 7: Add 1 in least significant digit to (A)', and complement sign of (A)

```
Ex. 6 cont:      1
               01000
               -----
               01001
  (A) = -01001
```

UNLIKE SIGNS (DATA LISTED AS EX. 2, 3, AND 5

State 5: Set Z4 to 0 and change to addition
State 6: Add (A) to (m), and use sign of (A)

```
Ex. 2: -11011      Ex. 3: +11011      Ex. 5: +10010
       +10010             -10010             -11011
       ------             ------             ------
       101101             101101             101101
(A) = -01101       (A) = +01101       (A) = +01101
with overflow      with overflow      with overflow
```

Figure 3-20. Subtraction

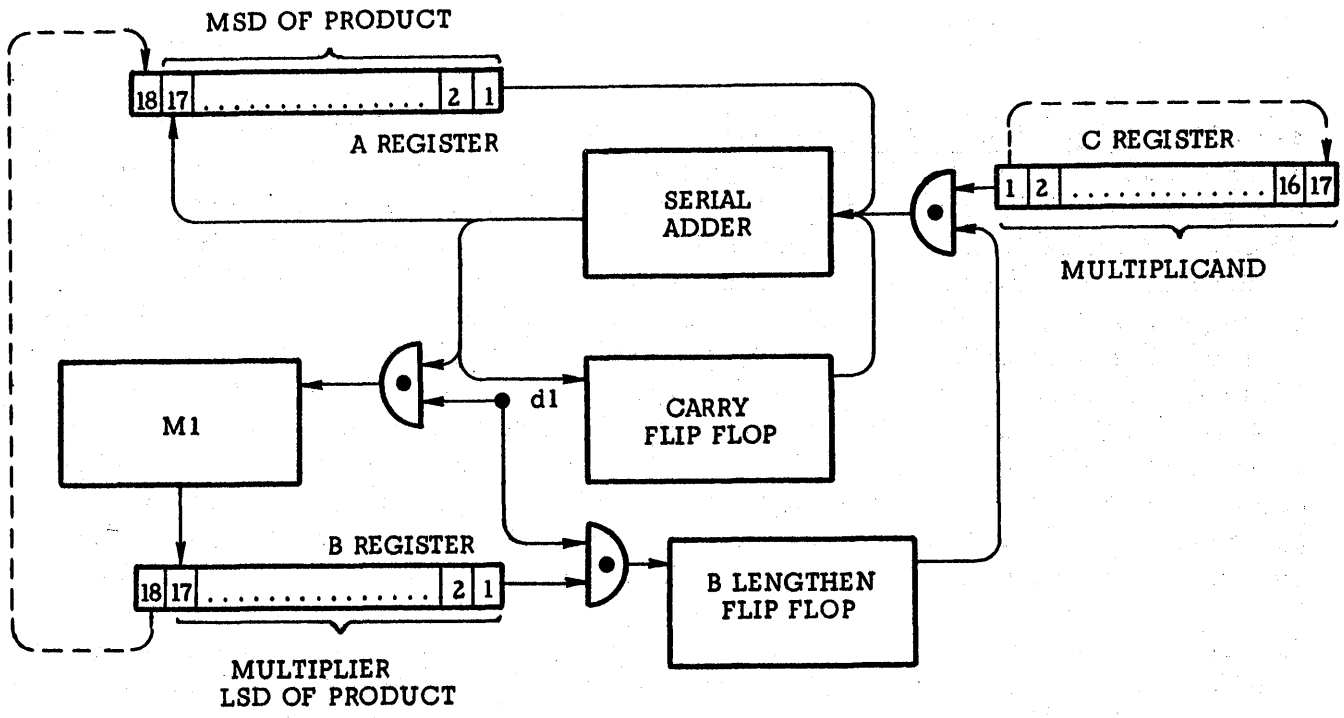
If the Computer remains in the subtract instruction at the end of state 5, the complement output of the C register is applied to J6; the output of the A lengthen flip flop, to J7; and the output of J8, to the A register flip flop. A 1 out of Z4, the carry flip flop, at digit time 18, is ignored. Inspection of the output of the carry flip flop at digit time 19 determines whether the subtraction is complete. When the signs of the operand and the contents of the A register are alike, the overflow flip flop is set to a 1 in state 5, at digit time 19. In state 6, this digit is added to the contents of the A register and the complement of the contents of the drum storage location. When the original contents of the accumulator are greater than the contents of the drum storage location, an overflow digit is created by the end-around carry but is ignored and the Computer returns automatically to state 1. When the original contents of the accumulator are less than the contents of the drum storage location, no overflow digit is created and the Computer changes to state 7. In state 7, a 1 is added to the least significant digit of the complement of the A register and the sum is recorded in the A register. The sign bit of the A register is complemented and the Computer returns to state 1 as the subtraction is completed. The subtraction process is summarized in figure 3-20.

3-3b(5). Instruction 20 (Multiplication). Instruction 20, represented by the binary code number 10000, results in the multiplication of the contents of the A register by the contents of the desired drum storage location. Digits 14 through 18 of the first word of the instruction pair specify the execution time, or the number of multiplier bits to be used. Conventional binary notation is employed; that is, 00001 specifies an execution time of 1, and 10001 specifies an execution time of 17. An execution time of 0 should not be specified. The 17 most significant bits of the product appear in the A register. The B register contains the least significant bits of the product in positions 17 through 17 -q + 1, where q is the specified execution time. There is no round off, and previous contents of the B register are lost. The time required for multiplication of two operands is six word times plus q word times. Thus, minimum time to execute a multiplication is from seven to 23 word times.

The search for the operand address takes place in state 4. During digit times 1 through 7, the output of the Y register is compared with the incoming sector number at the equality flip flop. During digit times 8 through 13, the operand address is copied from the Y register into the M flip flops. Equality at digit time 19 represents location of the desired sector and, unless the FETCH button has been pressed, the Computer will automatically go into state 5. At the same time, the carry flip flop is set to zero in preparation for the arithmetic addition. A, B, Y, N, and C registers remain at 20 bits and recirculating during digit times 1 through 18.

Mechanization of the multiplication function is accomplished by clearing the A register, serially connecting A and B registers, and shifting both right one digit in each of the series of addition operations, the number of which is specified by the execution time. Figure 3-21 summarizes conditions during each of the six word times required to effect a hypothetical multiplication of two five-digit numbers. In this figure, conditions are set up at what might be comparable to the start of state 6 in the RW-300 Computer during a multiplication instruction.

During digit times 1 through 17 of state 5, the multiplier contained in the sector being gated through the Read Selection unit is copied into the B register and the multiplicand circulating on the A register is copied into the C register, least significant digit first. Meanwhile, zeros are entered into the A register starting at the most significant digits. At digit time 18, the sign of the product is recorded in the B register. If the sign of the A register is the same as that from general storage read, a plus (0) is recorded in the B register; while, if the sign of the A register is unlike that from general storage read, a minus (1) is recorded in the B register. The execution time previously stored in the C register is shifted into the adder during digit times 1 through 7 simultaneously with the output of the sector number read. Adder output is recorded on the Y register to set up a pseudo address which limits the number of additions executed during the completion of the instruction. At digit time 19, the Computer automatically changes to state 6.



(A) = 11011 ⟶ C

(m) = 10010 ⟶ B

Execution time = 5

Long hand,

$$\begin{array}{r} 11011 \\ \times\ 10010 \\ \hline 110110 \\ 1101100 \\ \hline 0111100110 \end{array} = \text{product}$$

$(Y) = Y_0 + 5$

Digit time 20 = First bit of state

Sector Number	At Digit Time 20,	(A)	(B)	Least Significant Digit of B
$Y_0 + 1$	State 6	00000	10010	0
$Y_0 + 2$		00000	01001	1
$Y_0 + 3$		11011	00100	0
$Y_0 + 4$		01101	10010	0
$Y_0 + 5$		00110	11001	1
	State 7	11110	01100	
	State 1	01111	00110	

Figure 3-21. Multiplication

Actual multiplication takes place during state 6. Mechanization of the computation utilizes the least significant digit of the multiplier, stored in the B register, to control the addition of the multiplicand to the partial product. Examine figure 3-21 while following the explanation of Computer multiplication. If the least significant digit of the multiplier is a 1, the multiplicand stored in the C register is copied into the A register through the adder during the first word time. The B lengthen flip flop is used to store bit number 1 of the B register, which controls the input of C to the adder. At digit time 1, output from J8 is stored in one of the track register flip flops, M1, to serial-connect the A and B registers. In a multiplication, the register lengthening flip flops are not employed in series between register read and register flip flop circuits, in order to effect the desired right shift. However, since the sign bit must be retained, the B register is lengthened to 20 bits during digit times 17 through 20. At digit time 17, the output of M1 is recorded on the B register, therefore being effectively shifted from the A register to the B register. During digit times 18 through 20, output from the B register lengthening flip flop drives the B register write circuits. Similarly, the sign of the A register is retained by lengthening the A register to 20 bits during digit times 17 through 20.

Right shifting of A and B registers at the end of each word time moves each higher order digit of the multiplier into the bit number 1 position of the B register for control during the next word time. During any word time in which a 0 is stored in bit number 1 of the B register (and therefore in the B lengthen flip flop), the partial product in the A register is right-shifted without addition.

During digit times 1 through 7, the pseudo address created by the addition of the execution time and the sector number is compared with the sector number from R66, at the equality flip flop. At digit time 19 of the sector in which equality is achieved, the Computer changes to state 7.

During digit times 1 through 17 of state 7, the contents of the A register are shifted to the right an additional bit. At digit time 18, the sign of the B register is recorded on the A register. The Computer returns to state 1 at digit time 19.

3-3b(6). Instruction 32 (Division). The binary code number 11010 represents the division instruction, when appearing in the bits 14 through 18 of the second word of an instruction pair in the RW-300 Computer. The contents of the accumulator are divided by the contents of the specified drum storage location in this instruction. The quotient appears in the A register; while, the remainder is recorded on the B register. There is no round off.

Mechanization of the division operation is based on a fractional quotient; the radix point being placed to the left of the most significant digit. Attempts at generating a quotient greater than unity result in setting the overflow flip flop and shifting 1's into the A and B registers. During the first word time of the

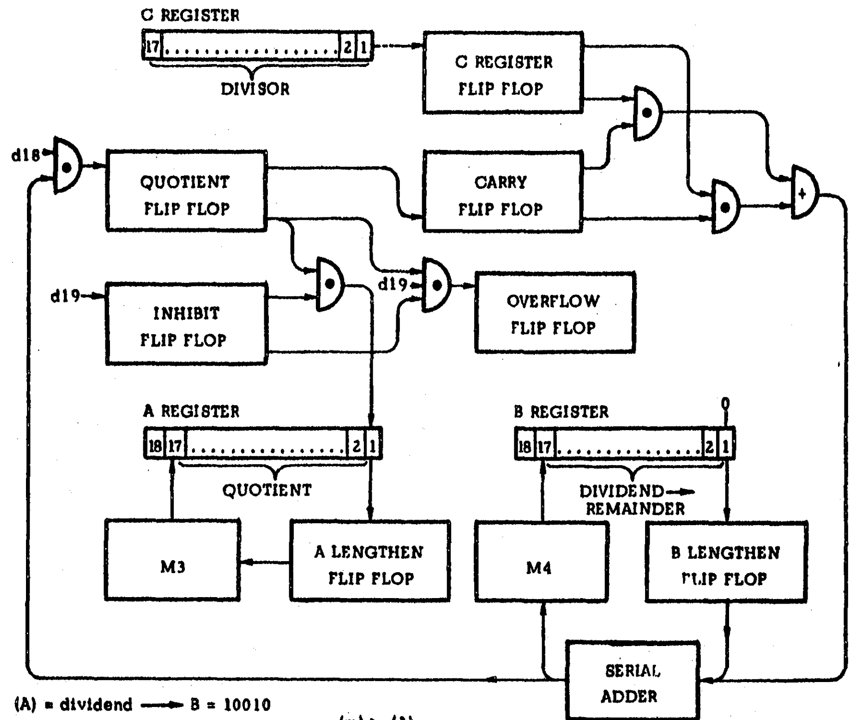
actual division (in state 6), the overflow flip flop is set if (A) > (m). This extra word time must be included, along with the number of quotient digits desired, in the execution time specified by digits 14 through 18 of the first word of the instruction pair. A zero length quotient should not be specified. Division requires six word times plus the execution time, or between 8 and 25 word times.

In state 4 during digit times 1 through 18, A, B, Y, N, and C registers remain at 20 bits and recirculating. The search for the operand address takes place during digit times 1 through 7, as the output of the Y register is compared with the incoming sector number at the equality flip flop. During digit times 8 through 13, the operand address is copied from the Y register into the M flip flops. Equality at digit time 19 represents location of the desired sector and, unless the FETCH button has been pressed, the Computer automatically changes to state 5. At the same time, the carry flip flop is set to zero.

During digit times 1 through 17 of state 5, the divisor is copied from general storage read into the C register, and the dividend appearing in the A register is copied into the B register, least significant digit first. Zeros are entered into the A register starting with the most significant digit. During digit times 1 through 7, the C register, containing the execution time, is shifted into the adder simultaneously with the output of the sector number read. The sum is stored in the next instruction register. At digit time 18, a plus (0) is recorded in B and C registers. If the signs of the dividend and the divisor are the same, a plus (0) is recorded in the A register; while, if the signs are unlike, a minus (1) is recorded in the A register. M2 (one of the track register flip flops), which is used to control the overflow flip flop in state 6, and M1--which stores the quotient digit as its complement output--are set to 0 at digit time 19. The carry flip flop is set to 1 in preparation for the end-around carry in the "shift and add complement" process. The Computer automatically goes to state 6 at digit time 19.

As an aid to understanding the operations performed in a division, the example in figure 3-22 should be considered. Although the data employed in the example each contain only five significant digits, the reader may assume that the remaining 12 more significant digits in the A, B, and C registers at the first digit time 20 of state 6 are zeros.

The contents of each register and of the supplementary control flip flops employed in the division are shown at digit time 20 of the sector $Y_0 + 1$, in the first line of the example table. The quantity (C)' is not actually recorded but can be expected to be generated simultaneously as the digits of (C) are applied to the C register flip flop. In the first word time of state 6, since M2 has been set to 0 and therefore inhibits writing into the A register, a 0 is recorded in the first bit of the A register. During digit times 2 through 17, the A register is recorded through two register lengthening flip flops, AL and M3, thus effecting a one digit left shift per circulation. The sign digit is recorded in bit 18.



(A) = dividend ⟶ B = 10010

(m) = divisor ⟶ C = 11011 (m) > (A)

(A)/(m) = quotient ⟶ A + remainder ⟶ B

Execution time = quotient bits + 1 = 6; therefore, (Y) = Y_0 + 6.

Manually: Right shift and subtract.

```
           .10101  = 5-bit quotient
11011)1001000000
       11011
       100100
        11011
        100100
         11011
         01001  = 5-bit remainder.
```

RW-300: Store sign as most significant digit in A (0 = plus, 1 = minus).

Use sign bits for manipulation, if necessary.

Carry digit from sign bit is complement of the quotient digit.

Adding end-around carry Z4 to C1' (1.00100) produces two's complement of (m).

SECTOR NUMBER	STATE 6	SET M2	(A)	M1'	M1	(B)	Z4 = M1'	(C)	(C)'
Y_0 + 1	d20	0	0--000000	1	0	0--010010	1	0--011011	1--100100
	d18		0--000000	0	1	1--101110			
	d19	1					0		
Y_0 + 2	d20	1	0--000000	0	1	1--101110	0		
	d18		0--000000	1	0	0--010010			
	d19	1					1		
Y_0 + 3	d20	1	0--000000	1	0	0--010010	1		
	d18		0--000001	0	1	1--101110			
	d19	1					0		
Y_0 + 4	d20	1	0--000001	0	1	1--101110	0		
	d18		0--000010	1	0	0--010010			
	d19	1					1		
Y_0 + 5	d20	1	0--000010	1	0	0--010010	1		
	d18		0--000101	0	1	1--101110			
	d19	1					0		
Y_0 + 6	d20	1	0--000101	0	1	1--101110	0		
	d18		0--001010	1	0	0--010010			
	d19	1					1		
State 7	d20	1	0--001010	1	0	0--010010	1		
	d18		0--010101			0--001001			
	d19								
State 1	d20		5-bit quotient			5-bit remainder			

Figure 3-22. Division

Since M1 had been set to 0 in state 5, M1' is a 1 at digit time 20 of the first word time of state 6. Z4 reflects the status of M1'. The resulting carried digit is added, with the complement of the (C), to produce the first partial remainder by the end of digit time 18 of the first word of state 6. A 0 is recorded in the least significant bit of the B register and the difference, formed by adding the dividend and the two's complement of the divisor, is recorded on the B register through two register lengthening flip flops, BL and M4, again effecting the one-bit left shift. In the example shown, the addition generated an overflow from the most significant digit of the register. This signal sets M1. M1' automatically becomes 0. At digit time 19, the status of M1' determines the status of Z4. Also at each digit time 19 of state 6, M2 is set to 1, and the status of the equality flip flop is examined.

In word times following the first, since M2 is true, the complement of the digit generated as the overflow from the B register is recorded in bit 1 of the A register. A left shift is accomplished each word time as the quotient moves into the A register. The sign digit is not shifted but is re-recorded in bit 18 each word time. During word times in which Z4 is 0, the true value of (C) are added to (B) and a similar left shift is provided in recording into the B register. At digit time 19 of the sector equivalent to the pseudo address generated in state 5, the equality flip flop will be true, changing the Computer to state 7.

At digit time 1 of state 7, M1' is recorded in the least significant bit of the A register. The register is left-shifted during digit times 2 through 17. The sign digit is recorded in the A register at digit time 18.

The status of the quotient flip flop, M1', controls the processing of the B register in state 7. If, as in the example of figure 3-22, M1 is false, the contents of the B register are shifted right one digit, by recording into the B flip flop directly from the B read circuit, during digit times 1 through 16. A 0 is recorded in the B register at digit time 17.

When the quotient flip flop is true at digit time 20 of state 7, the contents of the C register are added to the contents of the B register and the result right-shifted into the B register during digit times 1 through 17.

In either case, the sign of the remainder is made equal to that of the quotient by recording from the A register, through AL, into the B register at digit time 18. At digit time 19 of state 7, the Computer returns automatically to state 1.

3-3b(7). Instruction 05 (Extract). The logical intersection or product of the contents of the A register and the contents of the drum storage location is formed through the use of the extract instruction. By storing a mask in a given drum storage location, certain portions of (A) may be eliminated while other portions are retained. For example, the mask 0000011111111111111 could be logically multiplied, by means of the extract instruction, with the second word of an

instruction pair (previously loaded into the A register). Pertinent instruction codes may also be stored as masks. Assume the add instruction were stored as 1100100000000000000. Arithmetic manipulation of the "instructionless" word of the example (appearing in the A register), and the add instruction mask then results in Computer modification of the program on the basis of an appropriate conditional program transfer. The binary code number for the extract command is 00101. The contents of the B register are not affected and the command requires five word times to execute.

The operand address is sought in state 4, and during digit times 1 through 7, the equality flip flop examines the output of the Y register and the output of the sector number read circuit. The contents of the Y register in bits 8 through 13 are copied into the M flip flops. The desired sector, when applied to the equality flip flop, creates a true output which, sampled at digit time 19, actuates the Computer to change to state 5. The Computer remains in state 4 if the FETCH button has been pressed, however. At digit time 19, the carry flip flop is set to 0. The circulating registers are maintained at 20 bits length during digit times 1 through 18.

The extraction takes place in state 5 as the output of general storage read and the output of the A lengthen flip flop are "anded" and re-recorded on the A register. At digit time 19, the Computer returns to state 1.

3-3b(8). Instruction 37 (Merge). Logical addition is also offered for programming flexibility in the RW-300. In this command, represented by the binary code 11111, the contents of the specified drum storage location are merged with the contents of the A register and the result appears in the A register. A minimum of five word times is required for the execution of instruction 37.

During digit times 1 through 7 of state 4, the operand address is located through comparison of the output of the Y register with that of the sector number being read from the track, at the equality flip flop. Equality at digit time 19 represents location of the desired sector and, unless the FETCH button has been pressed, the Computer automatically goes into state 5. During digit times 8 through 13 of state 4, the operand address is copied from the Y register into the M flip flops. During digit times 1 through 18, A, B, Y, N, and C registers remain at 20 bits and recirculating. At digit time 19, the carry flip flop is set to 0.

The merging is accomplished in state 5 as, during digit times 1 through 18, a true output from either general storage read or the A register lengthening flip flop results in the recording of a digit 1 in the appropriate bit of the A register. At digit time 19, the Computer returns to state 1.

3-3b(9). Instruction 35 (Load A). The binary code number 11101 represents instruction 35, in which the contents of the desired drum storage location are

copied into the accumulator. Contents of the B register are not disturbed. A minimum of five word times is required to accomplish the transfer. During state 4, the operand address is located. The sector number being read by R66 is compared, during digit times 1 through 7, with the output of the Y register, in the equality flip flop. During digit times 8 through 13, the operand track number is copied from the Y register into the M flip flops. Unless the FETCH button has been pressed, the Computer automatically changes to state 5 upon generation of a true output from the equality flip flop at digit time 19. A, B, Y, N, and C registers are 20 bits and recirculating during digit times 1 through 18. At digit time 19, the carry flip flop is set to 0. The output from general storage read is applied to the A register flip flopfor recording in the A register, during digit times 1 through 18 of state 5. At digit time 19, the Computer returns automatically to state 1.

3-3b(10). Instruction 25 (Load A Negative). Instruction 25, represented by the binary code number 10101, copies the contents of the drum storage location into the A register, changing the sign of (m). The contents of the B register are not disturbed. Transfer also requires a minimum of five word times.

The Computer searches for the operand address during state 4. In digit times 1 through 7, the output of the Y register and the output of the sector number read amplifier are applied to the equality flip flop. During digit times 8 through 13, contents of the Y register are transferred into the M flip flops. True output from the equality flip flop at digit time 19 represents location of the desired sector and, unless the FETCH button has been depressed, the Computer automatically goes to state 5. The carry flip flop, Z4, is set to 0 at digit time 19. The circulating registers remain at 20 bits during digit times 1 through 18.

During digit times 1 through 17 of state 5, the output of general storage read is copied into the A register. At digit time 18, the complement of general storage read is recorded in the A register. At digit time 19, the Computer returns to state 1.

3-3b(11). Instruction 07 (Load B). Represented by the binary code number 00111, the load B command copies (m) into the B register. The contents of the A register are unaffected. Five word times are required to execute the command.

In state 4, the operand address is sought by the comparison of the output of the Y register with the sector number, during digit times 1 through 7, at the equality flip flop. During digit time 8 through 13, the operand address track digits are shifted into the M flip flops from the Y register. At digit time 19, the output of the equality flip flop is sampled and a true output changes the Computer automatically into state 5 (unless the FETCH button has been pressed). The circulating registers are kept at 20 bits during digit times 1 through 18. At digit time 19, the carry flip flop is set to 0.

As in the load A instruction, during digit times 1 through 18 of state 5, the output of general storage read is recorded on the B register. The Computer automatically changes to state 1 at digit time 19.

3-3b(12). Instructions 36 and 24 (Store A or Store B). Instruction 36, represented by binary code number 11110, copies the contents of the A register into the storage position specified by the command; while instruction 24, binary code 10100, effects such storage of (B). Mechanization of the store command is described in paragraph 3-2c. The contents of the circulating registers are not affected by the copying. A minimum of six word times is required for the instruction, the search for the storage location requiring a minimum of two word times.

Since the write head is positioned 32 sector times ahead of the read head, the search for the storage location is based on the "store" sector number, which is read from the sector number track 32 sector times prior to the sector number read head. Therefore, during digit times 1 through 7 of state 4, the output of the Y register and the "store" sector number read amplifier are presented to the equality flip flop. (If the track selector plug is in a position other than the tracks 0-7 jack, the sector number is used rather than the "store" sector).

If the FETCH button has not been pressed and no recording error has been generated, the Computer automatically goes to state 5 at digit time 19 with true output from the equality flip flop. A recording error illuminates the RECORD ERROR light on the test and maintenance panel and shifts the Computer into state 8, in which it idles. During digit times 8 through 13 of state 5, the operand address is shifted into the M flip flops. The carry flip flop is set to 0 at digit time 19. A, B, Y, N, and C registers are recirculated at 20 bits length.

In state 5, storage of the contents of the specified register is accomplished during digit times 1 through 18, as described in paragraph 3-2c. The computer returns to state 1 at digit time 19.

3-3b(13). Instruction 01 (Shift). Three types of shifts are provided in the RW-300 Computer. The same binary code number, 00001, specifies the instruction to shift, while the two most significant bits of the operand track address designate the type of shift. The number of shifts is specified by the execution time.

The A register may be shifted right by specifying the digits 00 in bits 13 and 12; the A register may be shifted left by specifying the digits 01; and, both the A and B registers may be shifted left by specifying the digits 11. A zero is shifted into position 17 each time the A register is shifted right. The sign remains unchanged. When shifting the A register left, zeros are shifted into position 1. A 1 shifted off the left end of the A register sets the overflow flip

flop. The sign of the register remains unchanged. Shifting both registers left inserts zeros into bit 1 of the B register and shifts digit 17 of the B register into bit 1 of the A register. The signs of both registers remain unchanged. All shifts require four word times plus one word time per shift. Thus, minimum time for this command ranges from four to 38 word times.

No processing is accomplished in a shift instruction in state 4 other than the change to state 5 at digit time 19 and the setting of the carry flip flop to 0. The A, B, Y, N, and C registers remain at 20 bits and recirculate. The change from state 4 to state 5 depends, of course, on the status of the FETCH button. With the FETCH button pressed, the Computer idles in state 4, regardless of instruction.

In state 5, during digit times 1 through 7, the equality flip flop is used to determine whether an execution time of 0 is specified, by setting the equality flip flop with output from the C register read. Output of the C register is applied to the adder with output of the sector read amplifier, to generate a pseudo address which is recorded on the operand address register. The track address, which specifies the type of shift, is stepped into the track register flip flops, M1 and M2, from the Y register during digit times 8 through 13. If both registers are to be shifted left, the signals from M1 and M2 result in storage of digit 17 of the B register in M6. If a 0 shift has been specified, the equality flip flop provides a true signal at digit time 19 and the Computer automatically returns to state 1. If the equality flip flop is false at digit time 19, the Computer transfers into state 6 and the equality flip flop is set to a 1.

When M1 is 0 and M2 is 1, the shift A left command is effected by lengthening the A register to 21 bits by recording through both the A lengthen flip flop and through M3, during digit times 1 through 17. At digit time 1, a 0 is recorded on the A register. The overflow flip flop, Z2, is set to 1 by a 1 in the A register at digit time 17.

The shift A right command, specified by M1 and M2 both being 0, controls the decrease in the length of the A register to 19 bits, by recording directly from the A read into the A write, during digit times 1 through 16, and recording a 0 in the A register at digit time 17.

The digit 1 in both M1 and M2, specifying the shift both A and B left command, results in the increase in the length of both the A and B registers to 21 bits, during digit times 1 through 17, through introduction of the A lengthen flip flop and M3 in the A register circuit and the B lengthen flip flop and M4 in the B register circuit. The digit stored in M6 during state 5 is written into the A register at digit time 1, and a 0 is written in the B register at digit time 1. At digit time 17, the digit in M4 is stored in M6. The equality flip flop examines the pseudo address in the Y register with respect to the sector number during digit times 1 through 7. A true output from the equality flip flop at digit time 19 returns the

Computer to state 1. At digit time 19, inequality, the Computer cycles through state 6 conditions again, the equality flip flop being reset after each digit time 19 sampling.

3-3b(14). Instruction 02 (Switch). Also called the exchange command, the switch instruction copies the contents of one register into the other or completes an exchange of the contents of each register into the alternate register. The binary code 00010 specifies a switch; while the type of transfer is specified by the most significant digits of the operand track number. Five word times are required to accomplish a switch.

During state 4, in a switch instruction, the circulating registers remain at 20 bits during digit times 1 through 18. At digit time 19, if the FETCH button has not been pressed, the Computer automatically goes into state 5, setting the carry flip flop to 0. The information regarding the type of exchange, recorded in the operand track address, is shifted into the M flip flops during digit times 8 through 13 of state 5. At digit time 19, the Computer automatically goes to state 6.

In state 6, during digit times 1 through 18, if the contents of M1 and M2 are both 0, the contents of the A register are copied into the B register through the A lengthen flip flop. If M1 is 0 while M2 is 1, the contents of the B register are copied into the A register, through the B lengthen flip flop. An exchange of the contents of the two registers is specified by M1 M2', and is accomplished by applying the output of the B register read circuit to the input of the A register lengthen flip flop, and the output of the A register read circuit to the input of the B register lengthen flip flop during digit time 1 through 18. At digit time 19, the Computer automatically changes to state 1.

3-3b(15). Instruction 11 (Transfer on Negative). Instruction 11, represented by the binary code number 01001, provides program branching on a negative sign in the A register. During state 4, the circulating registers remain at 20 bits during digit times 1 through 18. At digit time 19, the Computer automatically goes to state 5, unless the FETCH button has been pressed. In state 5 at digit time 18, the sign bit of the A register, delayed by the A lengthen flip flop, is stored in the M1 flip flop. At digit time 19, the M1 flip flop is inspected, a true output transferring the Computer into state 6 and a false output returning the Computer to state 1. During digit times 1 through 13 of state 6, the operand address is copied into the next instruction address register and the Computer returns to state 1 at digit time 19.

3-3b(16). Instruction 13 (Transfer on Zero). Program branching is also provided in the transfer on zero command, binary code number 01011. As in the transfer on negative command, during state 4, the A, B, Y, N, and C registers recirculate at 20 bits, and at digit time 19, the Computer changes to state 5 unless the FETCH button has been pressed. The carry flip flop is set to 0. In

state 5, the output of the A register is shifted into the equality flip flop during digit times 1 through 17. The equality flip flop is set to 0 on any 1 appearing in the A register. Sampled at digit time 19, true output from the equality flip flop transfers the Computer into state 6. Lack of 1 in the A register would result in a false output from the equality flip flop at digit time 19 and the Computer returns to state 1. When transferred into state 6, during digit times 1 through 13, the Computer records the operand address from the Y register into the next instruction register and, at digit time 19, returns to state 1.

3-3b(17). Instruction 12 (Transfer on Overflow). The binary code number 01010 specifies a program branching command in which transfer is accomplished if an overflow has occurred since the last transfer on overflow instruction. The command requires four word times to execute if no overflow has occurred; five word times if a transfer is necessary. During digit times 1 through 18 of state 4, the A, B, Y, N, and C registers recirculate at 20 bits. Unless the FETCH button has been pressed, the Computer automatically goes to state 5 at digit time 19, and the carry flip flop is set to 0. During digit time 19 of state 5, the status of the overflow flip flop is examined and used to transfer the Computer into state 6 if an overflow has occurred or into state 1 if none has occurred. At digit time 19, the overflow flip flop is reset to 0. During digit times 1 through 13 of state 6, the operand address is recorded from the Y register into the next instruction address register. At digit time 19, the Computer returns to state 1.

3-3b(18). Instruction 17 (Compare Magnitude). Instruction 17 offers another option of program branching in association with an arithmetic test. In addition to comparing the absolute magnitudes of (A) and (m), the instruction provides temporary storage of the original (A) in the B register and generates the difference in magnitudes in the A register; thus, permitting further processing of both the original (A) and the new (A). The command accomplishes the program branch through appropriate specification of digits in the execution time bits of the first word of the pair. Instruction 17 subtracts the absolute value of the contents of the drum storage location from the absolute value of the contents of the A register. The binary code number for this command is 01111. If the result of the subtraction is negative, the number specified in the execution time digits is added to the next instruction sector number, resulting in a program branch. If no transfer is necessary, the command requires a minimum of five word times. A transfer adds two word times to the command execution.

During digit times 1 through 7 of state 4, the contents of the Y register are compared with the sector number for equality. If the FETCH button has not been pressed, the Computer automatically goes to state 5 on equality at digit time 19. Since this command requires arithmetic subtraction, the carry flip flop is set to 1 at digit time 19 to provide the necessary end-around carry digit.

In state 5, during digit times 1 through 17, the carry digit, the complement of general storage read, and the output of the A lengthen flip flop are added in the

adder circuitry. The output of the A register lengthen flip flop is also recorded into the B register during digit times 1 through 18. Adder output is recorded on the A register during digit times 1 through 17. At digit time 18, a 0 is written into the A register. If the magnitude of the contents of general storage read is greater than the magnitude of the contents of the A register, the carry flip flop will be storing a 0 at digit time 19 and the Computer automatically goes to state 6. When the magnitude of the contents of general storage read is less than or equal to the contents of the A register, the carry flip flop remains set to 1 and the Computer is shifted into state 1.

At the end of state 5, the A register contains the complement of the difference between the original magnitudes. In order to utilize the actual difference in subsequent computation, the complement of the A register is recorded, through the A lengthen flip flop, into the A register during digit times 1 through 18 of state 6. At digit time 1, a 1 is added in the least significant digit of the A register. At digit time 18, a 1 is written into the A register, setting the contents negative. At digit time 19, the Computer goes to state 7.

In state 7, the execution time, contained in the C register, is added to the contents of the next instruction address register during digit times 1 through 5, assimilating the carries into the next instruction address, digits 6 and 7. During digit times 1 through 7, the output from the adder is recorded on the N register. During digit times 8 through 13, the N register is recirculated. At digit time 19, the Computer returns to state 1.

3-3b(19). Instruction 06 (Digital). Digital inputs/outputs are transferred to/from the A register in response to the digital command (00110 binary). Of the operand "track" address, the most significant bit differentiates between the input and output, and the remaining bits differentiate between groups of input/output lines. Pertinent bits in the first word of the DG instruction pair are tabulated below:

Bit No.	13	12	11	10	9	8	"Track"	Unit
Stored in	M1	M2	M3	M4	M5	M6	Address	Addressed
	0	0	0	0	0	0	0	Flexowriter output
	0	0	0	0	0	1	1	Logging typewriter output
	0	0	0	0	1	0	2	High speed punch output
	0	x	x	x	x	x	2* - 31	One-bit outputs
	1	0	0	0	0	0	32	Flexowriter input
	1	0	0	0	0	1	33	Ferranti reader input
	1	x	x	x	x	x	34*- 63	One-bit inputs

*If a high speed punch is addressed as "track" 2, "tracks" 3, 34, and 35 cannot be used. (See paragraph 3-4.)

The execution time bits are used to specify:

a. in an input instruction, the number of lines to be sampled and

b. in an output instruction, whether the output lines addressed are to be set to a 1 or a 0 (unless the system addresses all 18 lines simultaneously, in which case the execution time is not used).

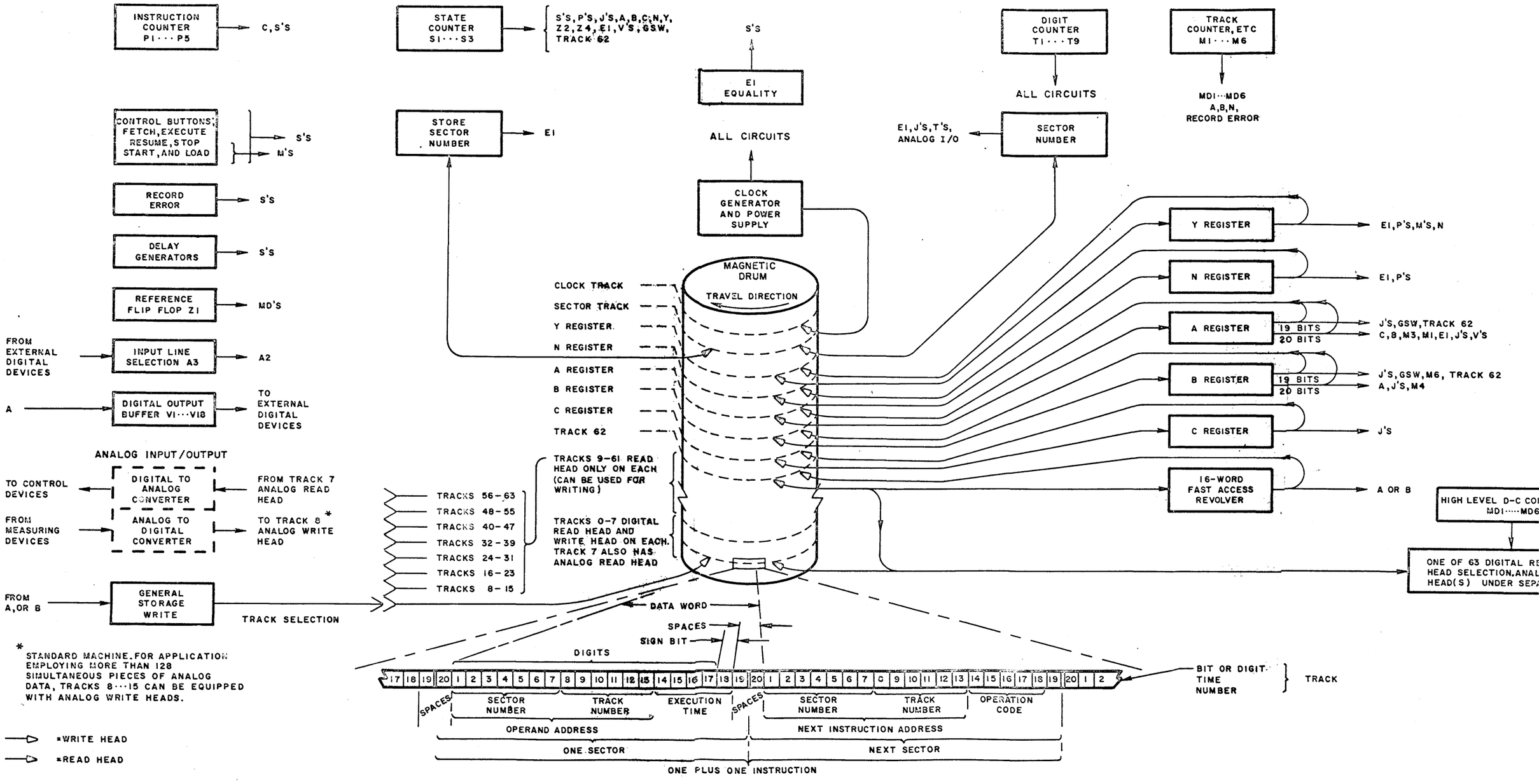
A minimum of six word times is required to execute a digital input instruction. A minimum of five word times is required to execute a digital output instruction.

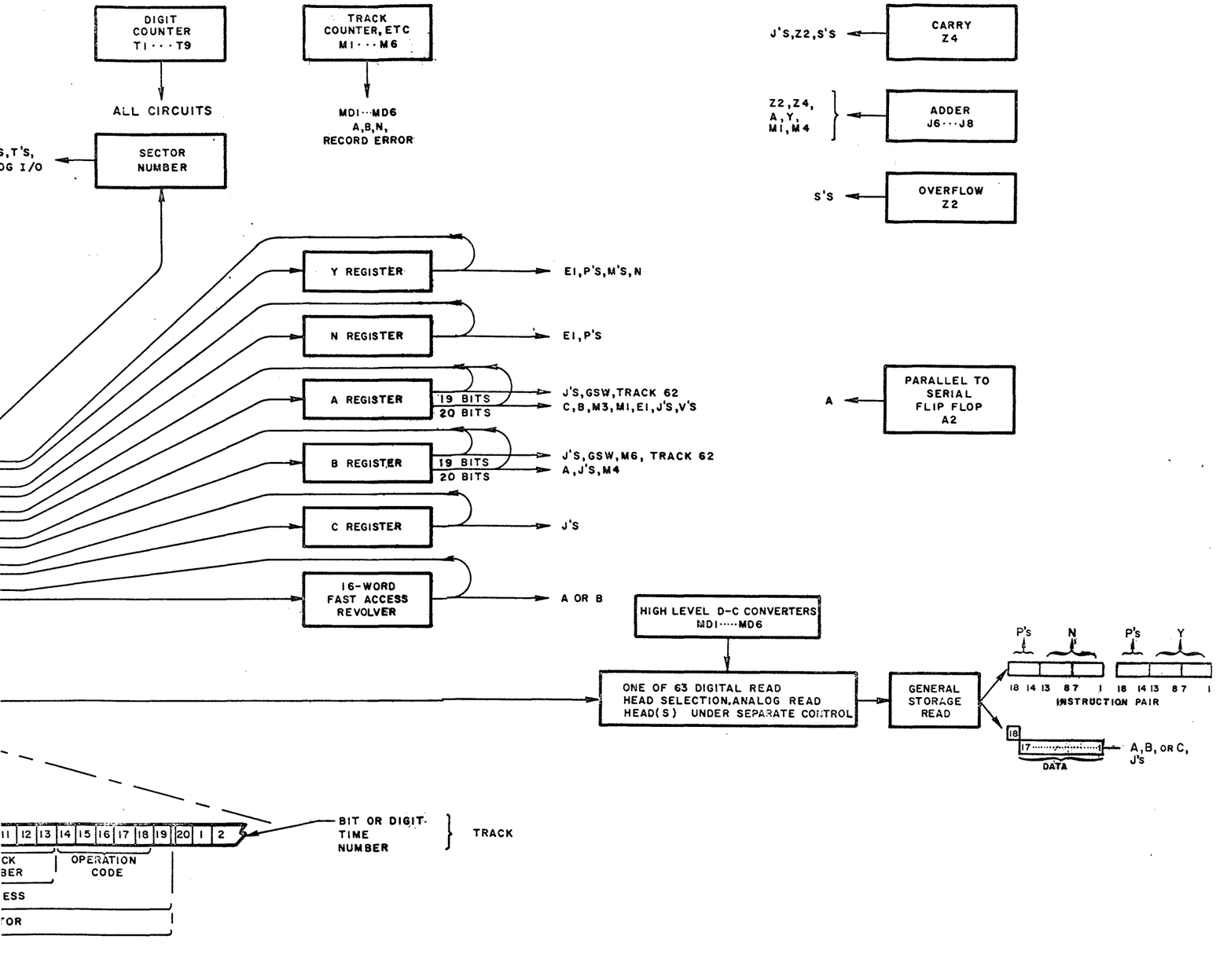
In state 4 of either an input or an output instruction, circulating registers are maintained at 20 bits as in other instructions. At digit time 19, if the FETCH button has not been pressed, and the necessary ready signal has been applied through the equality flip flop, the Computer advances to state 5.

The conditions required for Computer advance to state 5 depend upon whether the instruction orders an input or an output. On an input instruction, the equality flip flop is set by the combination of "track" address and appropriate ready signal from the unit addressed. Simultaneously, if the input is to come from a Flexowriter tape (addressed in track 32), an input line group selection flip flop is set, which sets the relay driver actuating a relay through the contacts of which power is applied to the reader. If a one-bit input is addressed, the line group selection flip flop (A3) is set false, a condition effecting the sampling of the one-bit input lines (during state 6).

At digit time 20 (the first clock pulse) of state 5 of a digital input instruction, the "track" address is transferred from the track register flip flops M2 through M6 into a set of d-c flip flops, V26 through V30, for storage. During digit times 1 through 5, the contents of the C register (the execution time digits) are shifted into track register flip flops M2 through M6. When a Ferranti high speed reader is providing the input, a d-c flip flop is set during state 5 to provide the necessary power transfer relay driver function. At digit time 19, the Computer goes to state 6.

In state 6, during digit times 1 through 18 and digit time 20, the track register flip flops count down, selecting one of the input lines each digit time, for application to the input of the parallel-to-serial flip flop, A2. When M2' M3' M4' M5' M6' = 1, the equality flip flop is set to 1 and the count-down stops. As long as E1 is false, the output of A2 is recorded on the A register, during digit times 1 through 18.


INSTRUCTION COUNTER P1···P5
C,S'S
STATE COUNTER S1···S3
S'S,P'S,J'S,A,B,C,N,Y,Z2,Z4,E1,V'S,GSW,TRACK 62
S'S
E1 EQUALITY
DIGIT COUNTER T1···T9
ALL CIRCUITS
TRACK COUNTER, ETC M1···M6
MD1···MD6 A,B,N, RECORD ERROR
CONTROL BUTTONS: FETCH, EXECUTE RESUME, STOP START, AND LOAD
S'S
M'S
STORE SECTOR NUMBER
E1
ALL CIRCUITS
E1,J'S,T'S, ANALOG I/O
SECTOR NUMBER
RECORD ERROR
S'S
DELAY GENERATORS
S'S
CLOCK GENERATOR AND POWER SUPPLY
REFERENCE FLIP FLOP Z1
MD'S
MAGNETIC DRUM
TRAVEL DIRECTION
Y REGISTER
E1,P'S,M'S,N
N REGISTER
E1,P'S
A REGISTER
19 BITS
20 BITS
J'S,GSW,TRACK 62
C,B,M3,M1,E1,J'S,V'S
B REGISTER
19 BITS
20 BITS
J'S,GSW,M6, TRACK 62
A,J'S,M4
C REGISTER
J'S
16-WORD FAST ACCESS REVOLVER
A OR B
HIGH LEVEL D-C CO MD1·····MD6
ONE OF 63 DIGITAL RE HEAD SELECTION, ANAL HEAD(S) UNDER SEPA
FROM EXTERNAL DIGITAL DEVICES
INPUT LINE SELECTION A3
A2
A
DIGITAL OUTPUT BUFFER V1···V18
TO EXTERNAL DIGITAL DEVICES
CLOCK TRACK
SECTOR TRACK
Y REGISTER
N REGISTER
A REGISTER
B REGISTER
C REGISTER
TRACK 62
TRACKS 9-61 READ HEAD ONLY ON EACH (CAN BE USED FOR WRITING)
TRACKS 0-7 DIGITAL READ HEAD AND WRITE HEAD ON EACH. TRACK 7 ALSO HAS ANALOG READ HEAD
ANALOG INPUT/OUTPUT
TO CONTROL DEVICES
DIGITAL TO ANALOG CONVERTER
FROM TRACK 7 ANALOG READ HEAD
FROM MEASURING DEVICES
ANALOG TO DIGITAL CONVERTER
TO TRACK 8 * ANALOG WRITE HEAD
TRACKS 56-63
TRACKS 48-55
TRACKS 40-47
TRACKS 32-39
TRACKS 24-31
TRACKS 16-23
TRACKS 8-15
FROM A,OR B
GENERAL STORAGE WRITE
TRACK SELECTION
DATA WORD
SPACES
SIGN BIT
DIGITS
17 18 19 20 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 1 2
BIT OR DIGIT TIME NUMBER
TRACK
SPACES
SECTOR NUMBER
TRACK NUMBER
EXECUTION TIME
SPACES
SECTOR NUMBER
TRACK NUMBER
OPERATION CODE
OPERAND ADDRESS
NEXT INSTRUCTION ADDRESS
ONE SECTOR
NEXT SECTOR
ONE PLUS ONE INSTRUCTION
* STANDARD MACHINE. FOR APPLICATION EMPLOYING MORE THAN 128 SIMULTANEOUS PIECES OF ANALOG DATA, TRACKS 8···15 CAN BE EQUIPPED WITH ANALOG WRITE HEADS.
=WRITE HEAD
=READ HEAD



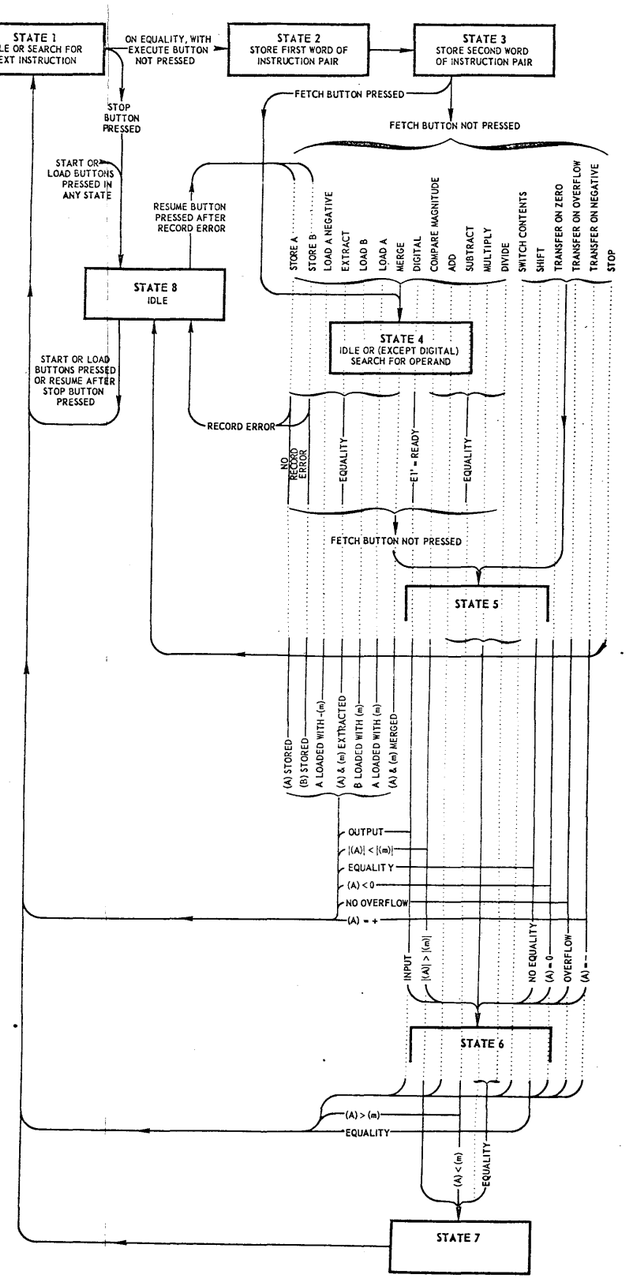


Figure 3-23. Master Functional Diagram

Zeros are written into the A register when E1 is true. At digit time 19, the Computer returns to state 1.

In an output instruction, the equality flip flop is controlled by delay generators, in addition to the "track" address, which impose a fixed delay following execution of a digital instruction to prevent interference by a subsequent digital instruction. A false signal from the appropriate delay generator permits advance of the Computer into state 5 of the digital output instruction.

During state 5, power is transferred, through a d-c flip flop controlling a relay, to the appropriate external unit and the associated delay generator is set to recycle. At digit time 1, the least significant digit of the execution time is stored in V25 to control the output of the Computer. If the LSD is a 1, the one-bit output lines addressed will be set to a 1 and vice versa (for installation exception, see paragraph 3-4b). During digit times 1 through 18 of state 5, the contents of the A register are shifted through the A lengthen flip flop into the output buffer register, V1 through V18. The contents of bit 1 of the A register are ultimately stored in V1. At digit time 19, the Computer returns to state 1.

3-3b(20). Instruction 00 (Stop). Instruction 00 places the machine in an idling mode, in which the contents of all registers recirculate. During state 4, at digit time 19, the carry flip flop is set to 0. During digit time 19 of state 5, M1 and M2 are each set to 1 and the Computer goes into state 8.

During digit time 1 through 18 of state 8, all registers recirculate. The Computer remains in state 8 until externally changed by means of the START, LOAD, or RESUME buttons.

3-4. DIGITAL INPUT/OUTPUT FUNCTIONS.

Digital input and output lines of the RW-300 are specified in groups of 18 lines each, and each group is designated by a "track" number. As used here, the "track" number is simply a means of addressing different groups of input and output lines, and has no bearing on the contents of memory tracks.

"Track" addresses from 0 through 31 are used for digital output lines, while "track" addresses from 32 through 63 are used for digital input lines. When fed into the track register, the most significant bit of the "track" address appears in M1. Thus, a 0 in stage M1 designates a digital output command, while a 1 in stage M1 designates a digital input command.

Digital input and output circuits of the RW-300 can be adapted for use with a wide variety of input and output equipment. Circuits associated with a minimum digital input/output system are located within the Computer, but when the system is expanded, digital input/output circuits are installed in the back of an operator's console or in auxiliary racks. The paragraphs which follow describe digital input

and output capabilities in terms of a maximum, or expanded system. Actually, the number of digital input/output circuits employed will depend upon the requirements of a particular application.

3-4a. DIGITAL INPUT.

Maximum digital input capability is 31 groups of 18 lines each, plus one group of 7 lines. The 7-line group, normally used with a Flexowriter tape reader, is designated L12 through L18. The remaining groups of lines are designated LXX21 through LXX38, where XX designates a "track" number used for input gating logic. While the most significant bit of the operand "track" address distinguishes an input command from an output command, the remaining bits of the "track" address determine whether input is accepted from L12 through L18 or from LXX21 through LXX38.

3-4a(1). Input From the Flexowriter Tape Reader.

When a six-channel tape reader is employed, L13 through L18 are used; for an eight-channel tape reader, L12 through L18 are used. Although only six lines are required for communication between the Flexowriter tape reader and the Computer, a seventh bit may be employed as a parity check. (For parity check, a 1 or 0 must be placed in the seventh channel so that the total number of bits in each character is an odd number. The Flexowriter can be equipped to count the bits in each character to decide if the character is valid.) In the paragraphs which follow, a 6-line input will be assumed.

When in State 4 of a Flexowriter read-in command, the Computer energizes the read clutch of the Flexowriter. The read clutch, LRC, is shown in Figure 3-24. Power is applied to LRC by the following circuits of the Computer: relay-driver RD1 controls relay RDR, and the contacts of RDR apply power to the Flexowriter's read-control magnet. The relay-driver circuit is described in paragraph 3-4c(1).

Punched holes in the paper tape are detected by read feelers which control switches RC1 through RC6 in the tape reader. The switches energize relays in the relay junction box of the Computer if a punched hole is detected in the tape. Thus, when the Computer is in State 4, relays in the relay junction box cause digital input from the tape reader to be applied to input lines L13 through L18. Contact RCC in the tape reader closes when the read feelers are in a position for sensing holes in the tape. RCC energizes relay RCCR in the Computer's relay junction box -- and the contacts of this relay energize a second relay, RCCR'. Designated Z11, a differentiated signal from the contacts of RCCR' is applied to equality flip-flop E1, advancing the Computer to State 5.

Z11 functions as a "ready" signal from the tape reader, holding the Computer in State 4 until all input relays are closed. The sequentially operated relays RCCR and RCCR' provide a time delay that is sufficient to insure that the input relays are

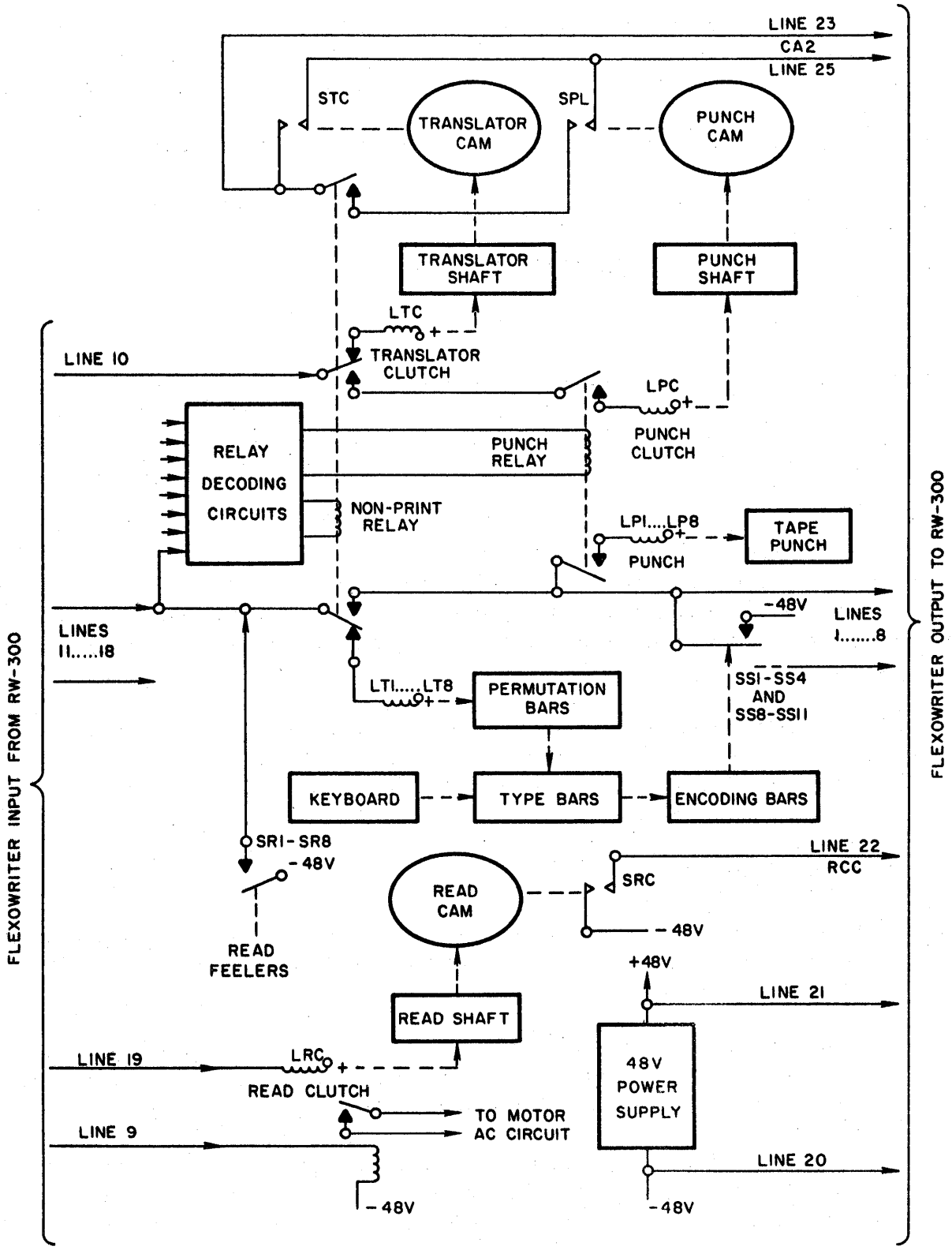


Figure 3-24. Flexowriter, Simplified Connections

closed before the Computer advances to State 5.

Bits from the Flexowriter are read serially into the A register during State 6, as described in paragraph 3-4a(4). The Flexowriter and digital input circuits appear in the block diagram of Figure 3-25. Initially, flip-flop A3 is set true by a Flexowriter input command (a "track" address of 32). A3 is reset when the Computer returns to State 1 after completing the digital input cycle.

Delay-generator D1 prevents interference from a Flexowriter output command which immediately precedes a Flexowriter read-in command. The function of the delay generator is described in paragraph 3-4c(4).

3-4a(2). Input from the Ferranti Tape Reader.

The Ferranti punched-tape reader requires at least 7 input channels (8 if a parity check is required). A Ferranti tape reader is normally connected to input lines designated as L3332 through L3338, and is addressed as "track" 33. (Flip-flop A3 remains reset--A3 is set true only during read-in from a Flexowriter tape reader.)

A "track" address of 33 initiates the read-in cycle for the Ferranti tape reader. When the tape is in a position for reading tape perforations, a signal (Z17) is generated by the tape reader. Z17* causes the input bits to be read into the Computer, and then enables the Computer to procede to the next state after digital read-in.

Tape advance is triggered by V24, a Computer flip flop set true during state 5 of the Ferranti read-in cycle. Without intervening relays, V24 drives a flip flop in the tape reader, causing the perforated tape to advance after read-in. V24 is reset at digit time 20.

3-4a(3). Other Digital Inputs.

A complete description of all possible digital inputs is beyond the scope of this manual. Supplementary publications describe input circuits used with specific installations of the RW-300.

The maximum digital input capacity involves 30 groups of 18 input lines each, or a total of 540 input bits. These 540 input bits are in addition to input bits normally assigned to the Flexowriter and Ferranti tape-reader inputs.

The "track" designations assigned to the input-line groups include addresses 32 through 63. Normally, four of the "tracks" are reserved: "tracks" 32 and 33 are reserved for the Flexowriter and Ferranti tape readers; and "tracks"

*Z17 must be inverted by an amplifier in the Computer. Other input bits from the tape reader are of the correct polarity.

34 and 35 are not usable if provision is made for connecting a high-speed punch to digital-output "track" 2. Thus, if "track" 2 is reserved for a high-speed punch, the maximum digital input capacity is reduced to 28 groups of 18 input lines, or a total of 504 input bits. These 504 input bits are in addition to the Flexowriter and Ferranti tape-reader inputs.

The paragraph which follows describes the technique used for serial read-in of the input bits.

3-4a(4). Digital Read-In.

During digit-time 20 of State 4, the operand "track" address of a digital input command is transferred from the M register to an auxiliary register of flip flops, V26 through V30. As shown in figure 3-25, signals corresponding to the "track" address are applied to the line-group selection logic by flip-flops V26 through V30. For example, a "track" address of 36 would cause input-lines L3621 through L3638 to appear at the output of the line-group selection logic.

Each of the 18 lines from the selected input group pass through a level-changer stage. Next, gating signals developed by the M register cause these 18 input bits to be fed serially into the A register.

In State 5, the execution time digits are shifted from the C register into track-register flip flops M2 through M6. During State 6, these flip flops count down automatically from a status representing the execution time to the 00000 status. Changing once each digit time, the output combinations available from stages M2 through M6 provide a unique pattern for gating one bit into the A register during each digit time.

This parallel-to-serial input conversion is accomplished by the gates shown in the lower right-hand corner of figure 3-25.

Note that Flexowriter input depends upon the A3 term applied to "and" gates accepting L12 through L18, while inputs L21 through L38 require an A3' term. The A3 term is derived from a "track" address of 32, while the A3' term is available because flip-flop A3 is normally reset during State 1.

If an execution time of 18 is specified in the digital input instruction, the count-down sequence of stages M2 through M6 will cause input LXX21 to appear as bit 1 of the A register, LXX22 to appear as bit 2 of the A register, and so on through LXX38, which will appear as bit 18. However, an execution time of 17 causes input LXX22 to appear as bit 1 of the A register, and so on through LXX38, which will appear as bit 17, but LXX21 will be lost. Thus, execution times lower than 18 cause a corresponding displacements of digital input bits in the A register. (Bit displacement as a function of execution time also occurs when inputs L12 through L18 are addressed.)

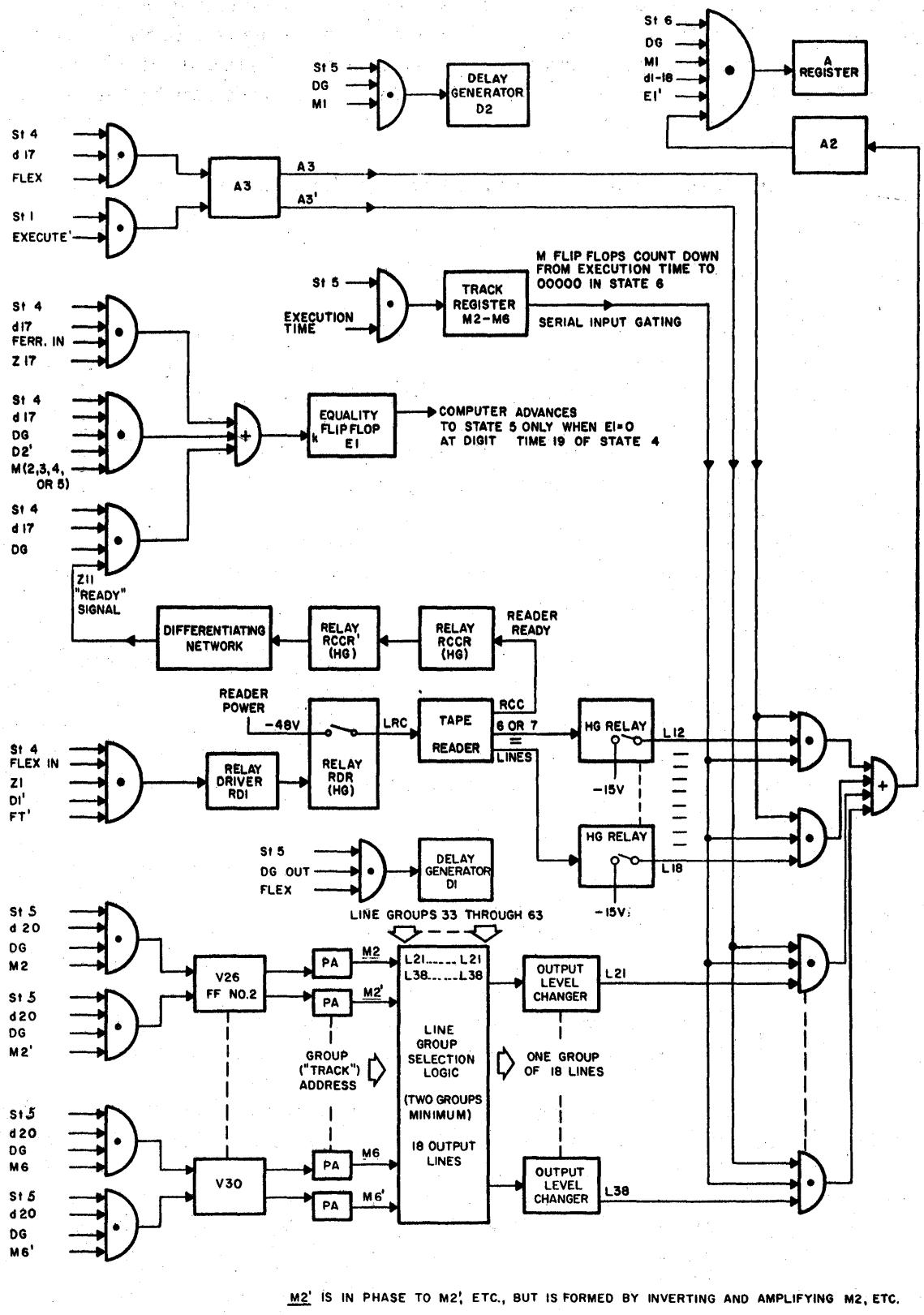


Figure 3-25. Digital Input System, Block Diagram

An executive time of 19 causes input LXX37 to appear as bit 18 of the A register, input LXX21 will appear as bit 2 of the A register, but LXX38 will be lost. However, an "or" combination of LXX21 and LXX22 will appear as bit 1 of the A register. Execution times higher than 19 cause a less coherent displacement of digital input bits because unique reset logic is employed at the input of counter-stage M2 (M2k = State 6, DG, M5', M6'). Thus, execution times of 20 or above should not be used.

Delay-generator D1 delays execution of a Flexowriter input command until 110 milliseconds after a Flexowriter output command.

3-4b. DIGITAL OUTPUT.

Digital outputs from the RW-300 are obtained by connecting output lines to contacts of the Computer's digital-output relays. Depending upon Computer application, output lines may be controlled either individually, or as an 18-line group. The type of line control is fixed by circuit connections made to the coils of the digital-output relays.

As in the case of the digital input lines, digital output lines are designated by "track" number. Again, the "track" number is simply a means of differentiating between groups of digital output lines, and has no bearing on the contents of the memory tracks. The most significant bit of the operand "track" address distinguishes an input command from an output command, and the remaining bits determine which group of output lines is selected.

Output lines are designated DL XX YY, where XX is the "track" address (1 through 31) representing a group of lines, and YY designates a specific line in an output group. Output lines are numbered from 1 through 18.

3-4b(1). Digital Output Relays.

The relays connected to the digital-output lines are of the bi-stable, magnetic latching type. (See figure 3-26.) When voltage is applied between the center tap of a relay coil and one of the outside terminals, the relay armature is set to a position representing a specific binary state. The armature retains this state, even after the voltage is removed. To reverse the binary state of the relay, a reverse magnitization current must be supplied by applying a voltage across the opposite outside terminal and the center tap. The relay remains magnetically latched in this new binary state until a reverse magnetization current is applied. Thus, applying voltage to one half of the relay coil sets the relay output true, and applying voltage to the other half of the relay coil sets the relay output false.

To control a group of 18 output lines simultaneously, the relay connections shown in the lower part of figure 3-26 are used. Under this type of control, all relays of a group are set and reset to correspond to a bit pattern previously stored in

the A register. This mode of operation is called 18-bit output.

For individual control of one or more output lines in an 18-line group, without changing the condition of other lines in the group, the relays are connected as shown in the upper part of figure 3-26. This mode of operation is called one-bit output.

3-4b(2). One-Bit Digital Output.

During State 5 of a digital output command, the contents of the A register are shifted into an output buffer register designated V1 through V18. As shown in the upper part of figure 3-26, the output of the complement side of each buffer-register stage is applied to the coil center taps of the polarized output relays. The output of V1' is connected to the center taps of all line-1 (DLXX01) relays that have been wired for one-bit output; similarly, V2' is connected to the center taps of all line-2 (DLXX02) relays wired for one-bit output; etc.

In the one-bit output mode, the contents of the A register determine which lines of an output group are to be controlled. For example, if line 08 of an output group is the only line of the group to be controlled, a 1 will be contained in bit-position 8 of the A register, and zeros will be in all other bit positions. When the contents of the A register are shifted into the output register, V8 will cause the center tap of all line-8 relays to be at ground potential, while the center taps of all other relays are at -13.5 volts. (In reality, any number of the 18 output lines in a group may be controlled in the one-bit mode.)

Although the contents of the A register determine which output lines are to be controlled, it remains for the contents of the M register to select the appropriate group of output lines. The "track" address is contained in track-register M2 through M6. Terms derived from the M register (V26 through V30) are combined in "and" gates to select the appropriate group of output-line relays. As shown in the upper part of figure 3-26, the relay group address is a gating term for the inputs to a pair of relay-control amplifiers. A pair of relay-control amplifiers--described in paragraph 3-4c(3)--is used with each group of output relays.

Using one-bit output, the type of control imposed on a specific output line is fixed by the execution time associated with the digital-output command. Using an odd number as the execution time places the controlled output line (or lines) in one binary state, while an even-numbered execution time sets the output line to the alternate state. The odd or even execution time determines the status of V25, with complementary outputs of V25 gated into the pair of relay-control amplifiers that drive the selected group of output relays. V25 is a d-c flip flop, type No. 2; paragraph 3-4c(2) contains a description of this circuit.

An odd-numbered execution time causes a 1 to appear in bit 14 of the first word

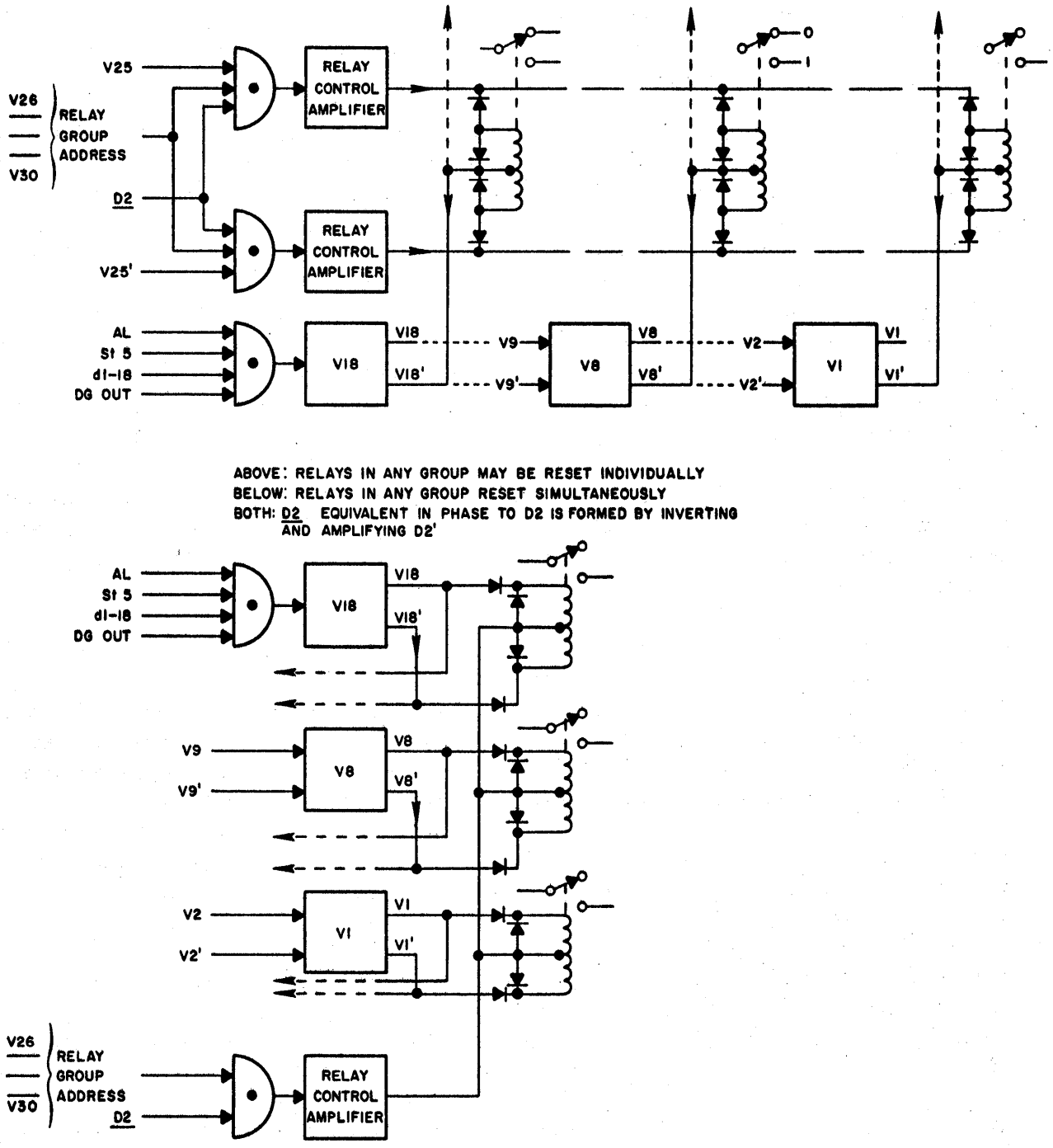


Figure 3-26. Digital Output Systems, Block Diagrams

of the instruction pair, setting V25 true. Under this condition, the pair of relay-control amplifiers shown in figure 3-26 holds the lower terminals of the relay group at 0 volts, and the upper terminals at -13.5 volts. If the center tap of a relay is at ground potential, current will flow through the upper half of the relay coil, and the contacts of the output relay will be set to 1. If, as in an earlier example, bit control were restricted to line 8, center taps of all other relays would be at -13.5 volts, and these relays would not be affected by the voltages from the relay-control amplifiers.

An even-numbered execution time sets V25 false, reversing the polarity of the voltages from the pair of relay-control amplifiers: lower relay terminals are held at -13.5 volts, upper terminals at 0 volts. If the relay center tap is grounded, the lower half of the relay coil is energized, and the contacts of the output relay will be set to 0.

In the upper part of figure 3-26, a $\underline{D2}$ term is shown at the "and" gate connected to the input of the relay-control amplifiers. Derived by amplifying and inverting a D2' signal, $\underline{D2}$ is in phase with, and is the same duration as, a normal D2 signal. The $\underline{D2}$ signal, or rather its complement D2', provides a 12-ms delay to inhibit subsequent digital output commands until output relays are set.

Push buttons located on an operator's console may be connected to relay terminals to provide manual control of the one-bit outputs. Each push button serves as an override control for setting or resetting a relay connected to a specific output line.

3-4b(3). 18-Bit Digital Output.

As in the case of the one-bit digital output command, the contents of the A register are shifted into V1 through V18 during State 5. As shown in the lower part of figure 3-26, complementary outputs of stages in the buffer register are connected to the outside terminals of the polarized output relays.

The outputs of V1 are connected to all line-1 relays that have been wired for 18-bit output; similarly, the outputs of V2 are connected to all line-2 relays wired for 18-bit output; etc.

In the 18-bit output mode, the contents of the A register determine how the 18 relays of an output group are to be set. Selection of a specific output group is determined by the "track" address stored in stages M2 through M6 of the track-address register.

As shown in the lower part of figure 3-26, the relay group address is a gating term for the input to a single relay-control amplifier. Only one relay-control amplifier is required for each group of output lines. When an output group is selected by a specific "track" address, the relay-control amplifier applies

-13.5 volts to the center taps of all relay coils associated with that group.

The coils of the digital-output relays have 0 and -13.5 volts applied across their outside terminals. These complementary voltages, derived from complementary outputs of V-register stages, determine which half of each relay coil will be energized. For example, if V8 was set true by a 1 in bit-position 8 of the A register, current will flow through the lower half of the relay coil, setting the output line to 1. However, if V8 was set false, current will flow through the upper half of the relay coil, setting the output line to 0.

3-4b(4). Output to Flexowriter Printer and Tape Punch.

Eight output lines are reserved for the Flexowriter printer and tape punch. The relays are connected for simultaneous setting and resetting, using circuit connections identical to those employed for 18-bit output. The "track" address of the Flexowriter is 0. If a parity-checking code is used, the eight Computer output relays are connected to the Flexowriter; when no parity check is used, the output relay that controls line 7 is not used.

As shown in figure 3-24, punch coils are designated LP1 through LP8, and print coils are designated LT1 through LT8. Depending upon whether or not parity check is used, either 7 or 8 of these lines are energized in code pattern by the bi-polar output relays of the Computer.

Before a print-out sequence can be initiated, primary power must be applied to the Flexowriter. This is accomplished by a one-bit output of "track" 4. An odd execution time turns the Flexowriter on, and an even execution time turns the Flexowriter off.

Code symbols generated by the Computer are employed to select print-only, punch-only, or print-and-punch modes of Flexowriter operation. These code symbols are transmitted from the Computer to the Flexowriter over the same lines used for transmitting code symbols for print-out. Specific Flexowriter operating commands are recognized by decoding circuits within the Flexowriter.

To initiate a print-out sequence, translator-clutch magnet LTC must be energized, and to initiate a punch-out sequence, punch-clutch magnet LPC must be energized. As shown in figure 3-24, LTC and/or LPC will be energized when the Computer applies power to line 10 of the Flexowriter. Power is applied to line 10 by Computer d-c flip-flop V22 during State 5.

Following print-out or punch-out of the output bits, the Flexowriter's translator cam or punch cam causes a switch closure signal. The switch closure signal, designated CA2, resets d-c flip-flop V22, de-energizing the translator-clutch and punch-clutch magnets.

3-4b(5). Other Digital Outputs.

In addition to provisions for Flexowriter outputs, a group of 5 output lines are normally provided for a logging typewriter, and a group of 7 output lines are usually provided for a high-speed punch. D-C flip-flop V23 controls application of coil current to the decoder of the logging typewriter; and V31 may be included to control application of coil current to the high-speed punch.

As in the case of the flip-flop for Flexowriter control (V22), flip-flops V23 and V31 are set during State 5, and are reset upon completion of the punching or printing cycle.

To summarize, a total of 32 groups of 18 output lines each can be provided as a maximum digital output system. However, two output groups are reserved for the Flexowriter and logging typewriter, and one group is normally reserved for a high-speed tape punch. (Although only one group is actually used for output to the high-speed tape punch, a second group is disabled whenever a high-speed punch is employed.) The remaining 28 groups of 18 lines each provide a capacity of 504 output bits.

Each output group can be connected either as an 18-bit or as a one-bit output group. A description of all possible digital output connections is beyond the scope of this manual.

The "track" designations assigned to the output line groups are 0 through 31. "Track" 0 is used for Flexowriter output, "track" 1 for the logging typewriter, and "track" 2 for the high-speed punch. Attempting to address "track" 3 will cause the Computer to stop in State 4.

Normally, the 18 lines of "track" 4 are connected to provide one-bit outputs. Digit-position 1 of "track" 4 is used to control primary power to the Flexowriter, and digit-position 2 is used to control primary power to the logging typewriter.

3-4c. DIGITAL INPUT/OUTPUT CIRCUITS.

The circuits for a minimum digital input/output system, involving only Flexowriter terminal equipment, are accommodated within the Computer. For an expanded system, digital input/output circuits must be located within an operator's console or in additional racks. Etched circuit cards, modules, and polarized relays of the digital input/output circuits are mounted in digital output assemblies. Digital output assemblies are drawer-type chassis with provisions for standard rack mounting.

Digital output assemblies for one-bit outputs contain an "A" relay chassis with 18 polarized relays. For one-bit output incorporating an override capability, the 18 polarized relays are mounted on a "C" type chassis. For 18-bit outputs,

the 18 polarized relays are located on a "B" type chassis.

A digital output assembly also includes a logic "C" card containing diode gating. One "C" card accommodates three groups of 18-bit inputs.

A module within a digital output assembly contains etched-circuit cards as follows: relay control amplifiers, power amplifiers, emitter-follower level changers, and Ferranti amplifiers.

The paragraphs which follow describe some of the circuits associated with the digital input/output system.

3-4c(1). Relay Driver.

Mounted in the C register module is an insert card bearing three relay driver circuits. RD1 is used in the digital input system to drive the relay applying power to the external reader device. The circuit isolates the changes in gate level from the relay winding and vice versa, and matches the relay input impedance. Each of the three relay driver circuits on the board is an NPN transistor amplifier driven by an "and" gate. Normally conducting, the amplifier is cut off by application of a true input. However, the contacts on the relay providing the circuit load are wired to transfer power to the reader when the winding is de-energized.

3-4c(2). Flip Flop No. 2 (Figure 3-27). A modified d-c flip flop providing a 0 volts false output and a -13.5 volts true output is utilized in the digital input/output systems. Flip flop output is false on both sides for approximately the last half of the clock period. The circuit obeys the following truth table.

Inputs at digit time i		Inputs at digit time i + 1	
j	k	A	A'
0	0	A_i	A_i'
1	0	1	0
0	1	0	1
1	1	Not permitted	

Referring to the schematic of figure 3-27, transistors Q2 and Q5 are the active elements of the basic flip flop circuit. Q3 and Q4 are the output transistors. Q1 and Q6 are the input transistors. Saturation of input and output stages is prevented by diode feedback circuits; while, in the flip flop transistors, saturation is prevented by clamping the conducting base at a voltage slightly above ground, by means of diodes, and resistively limiting emitter current.

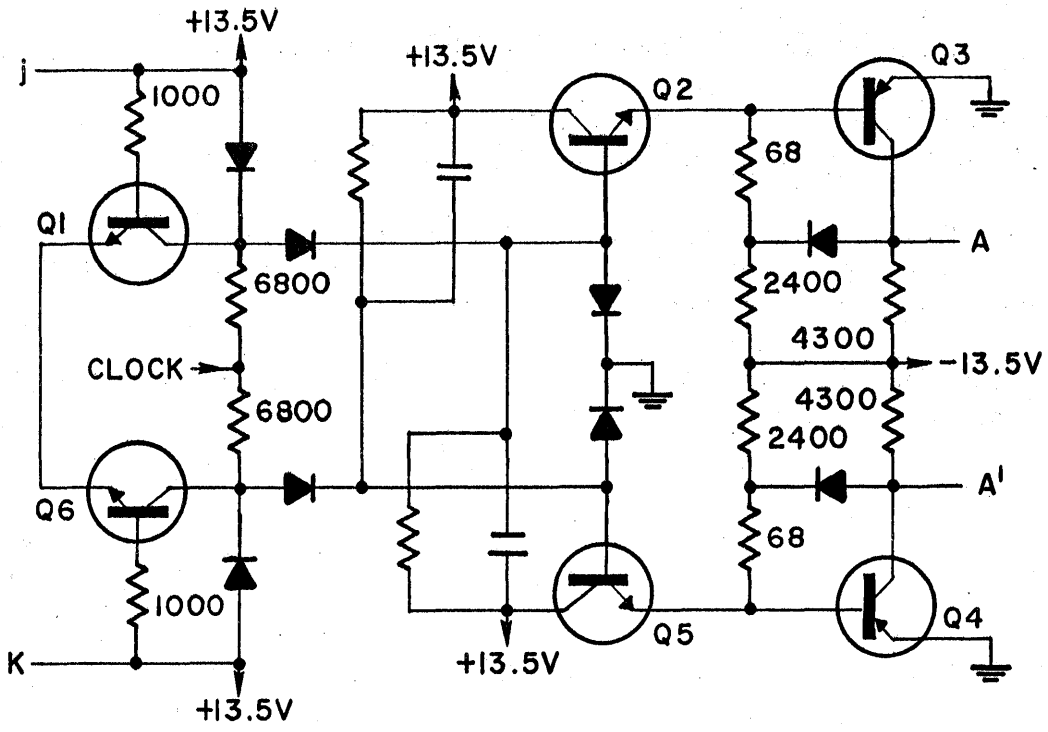


Figure 3-27. Flip Flop No. 2, Schematic

The flip flop action is triggered by transfer of the clock pulse to the cut off side of the flip flop, upon application of a true signal to the associated input stage. Essentially a grounded emitter amplifier, the triggered transistor of the basic flip flop drives the conducting output transistor to cutoff. The transit time of the output signal is thus maximized from conduction to cutoff.

The flip flop is set by holding the input Aj or Ak more negative than -5. 0 volts and absorbing the current from the positive power supply (+13. 5 volts) through the input resistors. Thus the input transistor cut off by a true signal presents a high impedance to the clock pulse, which is therefore transferred to the flip flop. If the input signal is less negative than -4. 0 volts, the input transistor conducts, absorbing the clock pulse.

Cutoff bias on the flip flop transistors is set by clamping each emitter at a voltage slightly below ground (by means of the conducting output transistor) and by using the crossover resistor divider network to set the base voltage farther below ground. The conducting transistor in the flip flop provides the cutoff bias for the output stage transistor. Silicon diodes are used to clamp the conducting base voltage in the flip flop transistors.

3-4c(3). Relay Control Amplifier (Figure 3-28). Illustrated schematically in figure 3-28 is the basic circuit of the relay control amplifiers used in the digital output systems. As indicated, the circuits are provided in pairs. Both circuits on a card may be employed for addressing the same group of relays, in which case the V25 and V25' signals control the output current. The delay generator signal used in driving various relay control amplifiers is power-amplified in order to provide the necessary current for the gating circuits. (This amplified signal is designated D2.)

3-4c(4). Delay Generator. The delay generator circuits inhibit execution of digital commands until external equipment is ready for the required operation. For example, delay circuit D1, associated with Flexowriter type and punch operations, is set to hold its "on" status for 110 milliseconds after its first input actuation pulse. This occurs at state 5 of all commands addressing such equipment. During the 110 milliseconds it is on, that is, for the length of time it takes to perform completely the Flexowriter output operation, D1 inhibits

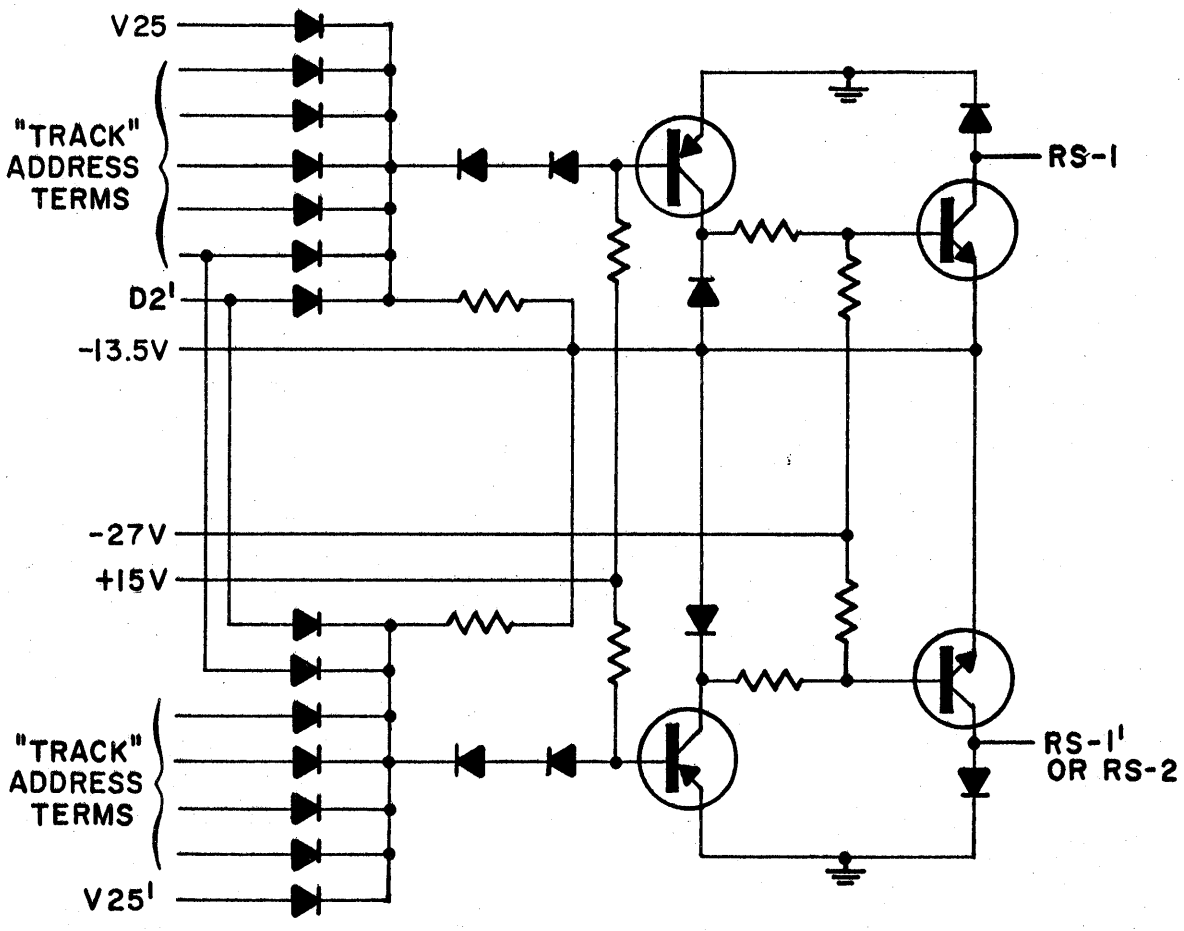


Figure 3-28. Relay Control Amplifier Pair, Schematic

Computer advance to state 5 of any subsequent Flexowriter communication command.

The delay circuit reverses the quiescent state of its output for a specified time period following application of a true pulse to its input. At the end of the time period, the circuit automatically resets and is ready to recycle after 20 microseconds.

The j input is sensitive with respect to ground, so that input voltages below 2.5 volts at 0.4 ma of conventional current at the input terminal are required to trigger the circuit on. Input voltages above +2.5 volts are incapable of triggering the circuit.

Output voltage varies from a false + 2.5 volts to a true -2.5 volts. Both D and D' outputs are available. The D output is normally false (high), becoming true (low) during the delay period; and D' is the opposite and becomes false during the delay period. When false, the D' output is capable of holding up a 28 ma load at +2.5 volts, and the D output can hold up a 4.5 ma load at + 2.5 volts. The false voltage at the D' output varies from +15 volts at no load, to +2.5 volts at full rated load. Similarly, the D output varies between +4.0 volts and +2.5 volts. Therefore, to protect the circuit being controlled by gating involving D or D', an "or" diode is necessary at its input.

The delay generator circuit consists of a d-c flip flop-similar to the flip flop No. 2 circuit described in paragraph 3-4c(2) in which input transistors permit or inhibit transfer of the clock pulse as the flip flop trigger--one side of which is set through a timing circuit. A variable timing resistor, a timing capacitor, and a uni-junction transistor comprise the network which determines the length of the delay interval. This time may be varied from approximately six to 200 milliseconds by varying the setting of the potentiometer.

In the quiescent state, the D output is false and the timing capacitor is essentially uncharged. A true input at clock time triggers the flip flop into its alternate state, providing a true D output and initiating the charge on the timing capacitor connected to the emitter of the uni-junction transistor. The uni-junction breaks down when the charge raises the emitter potential to approximately 56 percent of the total applied voltage, and the timing capacitor is discharged in a very short discharge-to-charge ratio time. The resultant pulse, developed across the timing resistor in base no. 2 of the uni-junction transistor, cuts off the transistor that inhibits transfer of clock pulses to the reset side of the flip flop, thus restoring the circuit to its quiescent condition.

The logic setting the j input of each of the three delay generators in the RW-300 is listed below:

D1j = 0631 4331 M5' M6'
= S1' S2 S3 P1' P3 P5' M1' M2' M3' M4' M5' M6'
= In state 5, on Flexowriter output commands

D2j = 0631 M1' = S1' S2 S3 P1' P3 P5' M1'
= In state 5, on any digital output command

D3j = 0631 4331 M5' M6
= S1' S2 S3 P1' P3 P5' M1' M2' M3' M4' M5' M6
= In state 5, on logging typewriter output commands

3-5. ANALOG INPUT/OUTPUT.

The RW-300 Computer assembly is designed to accommodate the independent subsystem providing analog to digital (A-D) and digital to analog (D-A) conversion. The maximum standard subsystem can process the following inputs and outputs:

a. Up to 1024 analog voltage inputs at high and/or low levels, converting these into binary numbers which are recorded in general storage tracks on the drum; and,

b. Up to 128 binary words, read from track 7 of the drum, converting these into either voltages or currents, as required.

The arithmetic and control portion of the Computer records into the digital to analog track (track 7) and reads from the analog-to-digital track(s).

D-A conversions occur, and outputs are maintained or revised, once each drum revolution (1/60 second) except when A-D conversion is taking place. A-D conversion requires 130 microseconds per input conversion, plus one word time for shifting. All inputs may be sampled and recorded in 2.1, 4.2, or 8.3 seconds, depending on the amount of filtering necessary to reject noise on the input lines. High level inputs require less filtering and therefore are recorded more quickly (when no low level inputs are included).

Linearization, zero suppression, and span scaling are performed numerically within the Computer, eliminating the requirement for external equipment to perform these operations. Low level input lines can be isolated from each other, ground, and the converter, as necessary.

3-5a. SYSTEM FEATURES. The D-A and A-D converters share the use of many circuits in the system. As shown in figure 3-29, the analog input/output system comprises:

a. the analog input switching and amplifying circuitry;

b. the A-D converter;

c. the D-A converter; and,

d. the drift stabilizing circuitry.

3-5a(1). Input Switching and Amplification. Input voltages are switched and amplified as shown at upper left of figure 3-29. A maximum of 32 high speed, high level electronic gates apply the selected signal from groups of up to 32 individual analog inputs. The total inputs which may be handled by the combination of relays and electronic gates, therefore, is 1024. Each low-level input is switched through a separate mercury-wetted contact relay, but one relay is used to switch two high-level inputs. A relay in each group is closed during each A-D conversion.

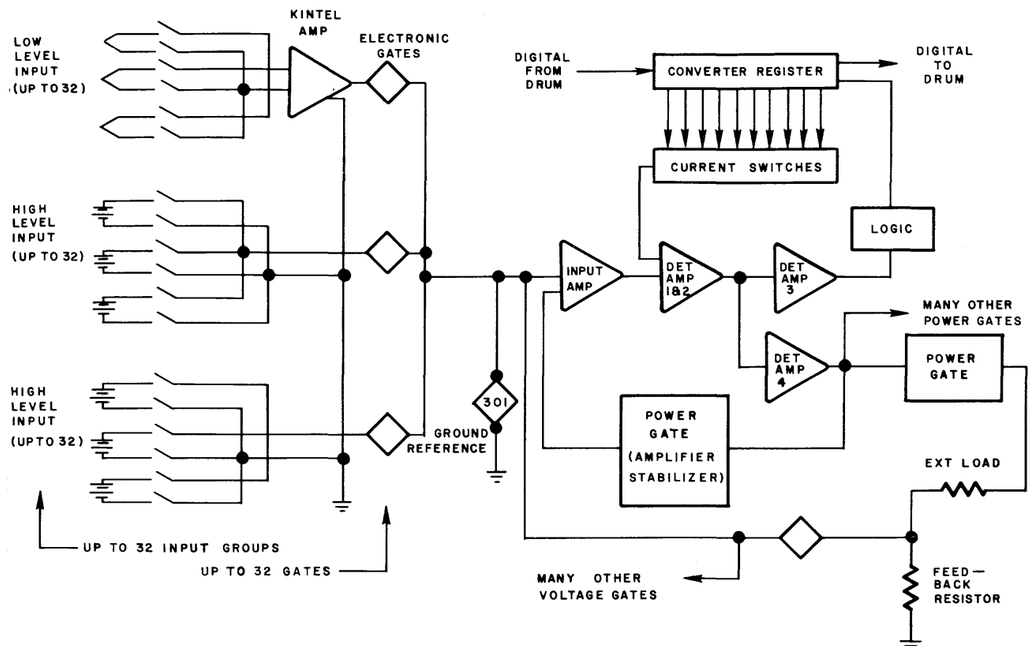
After a closure, a delay allows the amplifiers to reach steady state, and the voltage gates are sequentially activated, until each gate has sampled an analog input. In this manner, up to 32 input conversions are performed in one drum revolution (1/60 second). When these A-D conversions have been completed, a different relay is closed in each group, and, after a delay for amplifier stabilization, the electronic gates again close in sequence to allow another 32 A-D conversions. This sequence continues until all inputs have been sampled, at which time the cycle repeats. The conversions are independent of other Computer operations and continue as long as the system is powered.

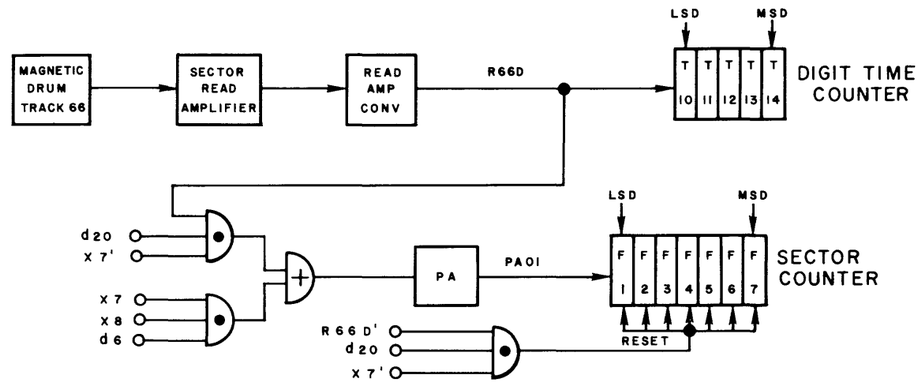
One amplifier is used for as many as 32 low level inputs. Each amplifier gain is fixed and, therefore, all low level signals for this amplifier must be in the same voltage range and polarity. Amplifier gain up to 1000 is available, and the groups of low level inputs in a given installation are arranged to drive amplifiers set to provide the gain needed for greatest measurement accuracy.

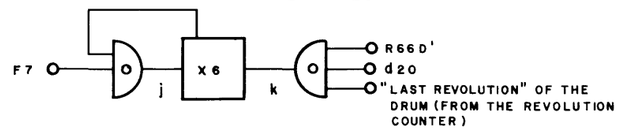
A thermocouple reference junction box can be provided that will electrically isolate each reference junction.

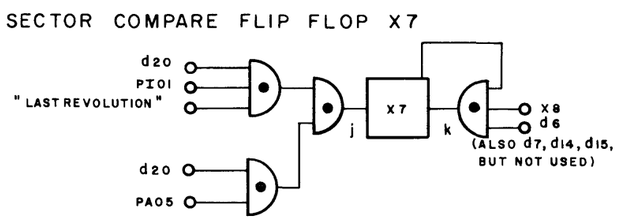
Low level d-c measurements are invariably accompanied by 60 cps a-c pickup. The RW-300 converter takes only 0.13 (milliseconds) per conversion, and since 60 cps is 16.6 ms per cycle, any stray voltages at power frequency are essentially interpreted as dc. The stray may appear in either series or parallel modes. The parallel stray is a common mode signal readily rejected by the floating, differential amplifier. The series stray is equivalent to an a-c signal, in series with the d-c variable that is to be measured, which can be effectively rejected by a low pass filter cutting off all signals above 30 cps.

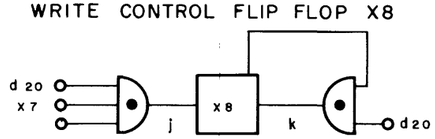
This low pass filter will reduce 60 cps series stray by a factor of 1000. This means that the a-c pickup can be as large as the full scale d-c input, without masking the desired signal. Inherently, the filter used to reject series 60 cps pickup requires a significant time for the output to reach steady state when a d-c signal is suddenly placed on its input. In particular, for the filter described above, the amplifier-filter combination requires about 0.23 seconds (or 14 drum revolutions) to settle out to 99.9 percent of its final value. The standard Computer

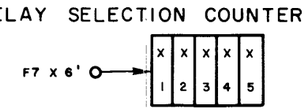


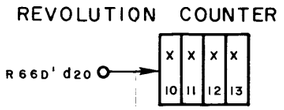












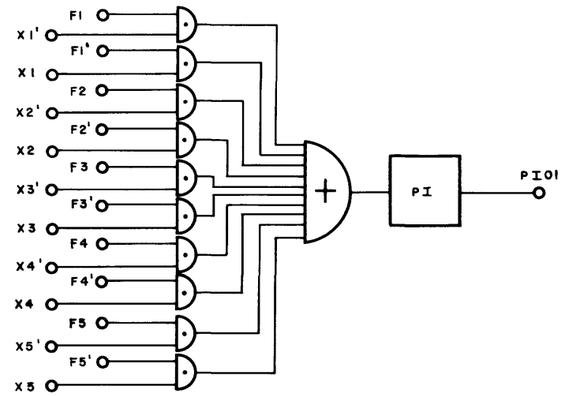


Figure 3-29. Analog Input/Output System, Block Diagram

is arranged such that 14, 6, or 2 drum revolutions delay time may be utilized, thus offering three speed options, depending on the severity of the series stray at a given installation.

Sixty cps stray is not usually a problem for the high level signals, though filtering can be provided in special situations.

3-5a(2). Analog to Digital Conversion. When the input relay and its electronic switch have closed, an analog voltage is presented to the A-D converter (shown at top center of figure 3-29). The output of the input amplifier is fed to detector amplifier 1, where a comparison is made with a test signal from the current switches which, in turn, are controlled by the 10 flip flop converter register. When a conversion is commanded, the first flip flop changes state, thus closing a current switch and causing the current equivalent of -5.12 volts to appear at detector amplifier 1. The voltage at the output of detector amplifier 3 indicates whether the analog input signal current is greater or less than this test signal current.

If the magnitude of the input signal current is greater than the test signal current, the first flip flop in the converter register remains on and the next (second) flip flop is also turned on, adding $\frac{-5.12}{2}$, or -2.56 volts to the -5.12 volts already present at detector amplifier 1, raising the total test signal current to the equivalent of -7.68 volts. This signal is then compared with the input analog signal and the output of detector amplifier 3 is again examined to determine whether the input signal is greater than the test signal.

If the magnitude of the input analog signal is less than the test signal (for example, 7 volts), the last test signal (in this case -2.56 volts) would be turned off by its flip flop in the converter register and the next current signal would be turned on. The next test signal is $\frac{-2.56}{2}$, or -1.28 volts plus the -5.12 volts already present, or -6.40 volts. The comparison sequence continues in this iterative manner until the test signal equals the input signal to one part in 1024; i.e., to an accuracy of one part in 2^{10}. The binary representation of the input signal is indicated by the states of the flip flops in the converter register, and can be recorded on the Computer drum.

An A-D conversion takes one word time (130 microseconds), and the shift into the drum requires the use of another word time, or a total of two word times for the complete sequence.

The analog to digital converter is a single polarity circuit, accurate and stable to 0.1 percent, and capable of being referenced either internally or externally. Full-scale input is 10.23 volts, with least-count transition occurring at +5 millivolt.

3-5a(3). Digital to Analog Conversion. The D-A converter is designed to convert the binary information from the drum to a voltage (0 to 10.23 volts) or

current (up to 5.115 milliamps). The equipment used for a conversion (see figure 3-29) includes the converter register, current gates, detector amplifiers 1 and 2, detector amplifier 4, power gates, feedback voltage gates, and the input amplifier.

When a D-A conversion is to be performed, the binary number is shifted into the converter register. The state of the flip flops control which current switches are turned on, and the resulting current is fed into detector amplifier 1 and 2 for comparison with the voltage of the externally controlled load. If the voltage at the load is equal to the voltage represented by the current switches, detector amplifier 4 will not drive the power gate in either direction.

The power gate supplies a voltage to the external load, maintaining the voltage between conversion intervals. If the voltage at the externally controlled devices is equal to the voltage represented by the current switches, as determined by a comparison at detector 1 and 2 (via the input amplifier and feedback voltage gate), the output of the power gate will not change. Conversely, if the voltage at the load is different from that commanded by the current switches, the power gate is driven (in servo technique) until a null is reached at the detector amplifiers.

Many process controls, such as galvonometer force balance systems, are driven by current rather than voltage. Since the load in this case is a copper coil with a temperature coefficient of 0.4 percent per degree centigrade, a voltage reading across the coil for comparison in the converter would be inaccurate. Instead, a precision feedback resistor is placed in series with the copper coil, and the feedback voltage is taken from the current through this resistor. The output load coil is then served, according to the current, independently of the variations in the coil resistance.

One power gate and one voltage gate are associated with each analog output. These gates are controlled by counters within the input/output subsystem in such a way that the correct output is associated with the converter at the correct time. The RW-300 Computer can serve 36 analog outputs. All outputs are revised every 1/60 second in the RW-300 except when inputs are being converted. The holding circuit holds the output voltage (or current) to 0.1 percent for the 1/60 second possible between revisions. The output signal can be referenced internally or externally.

3-5a(4). Drift Stabilization. The input amplifier and the detector amplifiers are direct-coupled devices and subject to voltage drift with time and temperature unless stabilized. The stabilizing circuitry in the RW-300 converter, as shown in figure 3-29, involves only the addition of voltage gate 301 and the amplifier stabilizer power gate. When the converter is doing neither an A-D nor a D-A conversion, voltage gate 301 is closed, producing a 0 volt input signal, and the register is cleared, resulting in a 0 volt test signal. Any non-zero voltage appearing at the output of detector amplifier 4 is the result of drift, and a compensating signal is added to the input amplifier by means of the amplifier stabilizer power gate.

Thus, all drift is corrected, using only solid state components.

3-5b. FUNCTIONAL GROUPING AND CIRCUIT DESCRIPTIONS. While independent of programming control by the Computer, the analog input/output subsystem must be synchronized with the timing of the storage drum to retain the identity of words recorded on the drum by the A-D circuits and read from the drum by the D-A circuits. The sector number track on the drum controls the synchronization of the analog input/output subsystem as well as that of the computation circuits. However, separate digit counting and sector counting circuits are provided since the digit and sector recognition requirements differ in the two functions. Further, the analog input/output subsystem includes a revolution counter, since input circuit stabilization requires a conversion delay and input sampling must be synchronized based on the delay necessary. All timing function circuits are mounted in modules 413 and 414.

3-5b(1). Digit Time Counter. The digit time counter defines the digits of each sector passing under the read head. Since there are 20 digit times per sector, the digit time counter recycles to zero after a count of 20 and is otherwise a conventional binary counter. The circuit consists of five d-c flip flops of the type described in paragraph 3-4c(1).

The sector identification is recorded in binary numbers in the least significant seven bits of each of the 128 sectors on the sector track. This information is used in the Computer timing, but not in the analog input/output timing. At program sector 127 (bits 1 through 7 are 1's), bit 17 is a 1 to synchronize test equipment. Bits 13 and 16 are always 1's and bit 20 is 1 in all sectors except the last sector (127) of the revolution.

As indicated in figure 3-29, track 66 is read, amplified, and converted into a signal compatible with the d-c logic used in the analog input/output system. The read amplifier converter changes the a-c information recorded on the drum to the d-c logic of the input/output circuit.

The read amplifier converter circuit receives a reference signal from flip flop Z1 on a diode at one input and the complement of the reference signal on a diode at the other input.

Assume that RN (the amplified input signal from the drum) is in phase with Z1. A positive d-c signal is transferred to the transistor base. Since there is an inversion in the transistor from the base to the collector, the output from the collector is a negative signal. Therefore, an in-phase or true signal from the drum produces a -13.5 volts true signal out of the read amplifier converter. In a similar manner, an out-of-phase signal at RN will cause 0 volts false output at the collector of the read amplifier converter transistor.

The digit time counter receives clock pulses, as do all flip flops, and counts

in a binary manner until digit time 13. If R66D (the output of the read amplifier converter) is not a 1 when the five flip flops comprising the counter assume the configuration identified as digit time 13, the counter will wait until a 1 is read in synchronism with the clock pulse. This also occurs at digit time 16. When the counter is in synchronism with the sector track, the counting is continuous. Both d16 and d13 are necessary to eliminate the possibility that the digit time counter will lock in on d20 or one of the sector number identification digits.

3-5b(2). Sector Counter and Control. The sector counter defines the program sector that is under the read head. Since there are 128 words per track on the drum, seven flip flops are required. Sector counter flip flops F1 through F7 are also mounted on timing module no. 1. As shown in figure 3-29, the sector counter is reset to all zeros by digit 20 of sector 127, (assuming that both X7 and X8 are false) thereby providing synchronization. The sector counter counts in a binary manner under the control of digit 20 (R66D and X7') except during an analog to digital conversion. Advance of the counter is controlled by d-c flip flops X7 and X8, which determine the conversion interval. Since the analog inputs are selected by the sector counter, sector extension is required.

Briefly, an A-D conversion takes two word times. Flip flop X7, called the sector compare flip flop, is true during the first word time and until digit 6 of the second word time, thus inhibiting an advance of the sector counter, so that the analog signal is on the input in the second word time as well as the first word time.

Flip flop X7 is turned on during the "last revolution" digit 20 when PI01 is true. PI01 is the command that a conversion is to be made. Power-inverter circuit PI is employed for the comparison between the sector counter output and the relay selection counter, as described in paragraph 3-5b(5). Mechanizing the inverse of the comparison is simpler than mechanizing the comparison itself. The comparisons for the various gate systems, as described in paragraph 3-5b(5), involve only use or omission of the more significant outputs of the relay selection and sector counters.

A true output from PI01 during a last revolution allows sector compare flip flop X7 to become true. At this time, an A-D conversion can be accomplished. PI01 is also mounted on timing module no. 2.

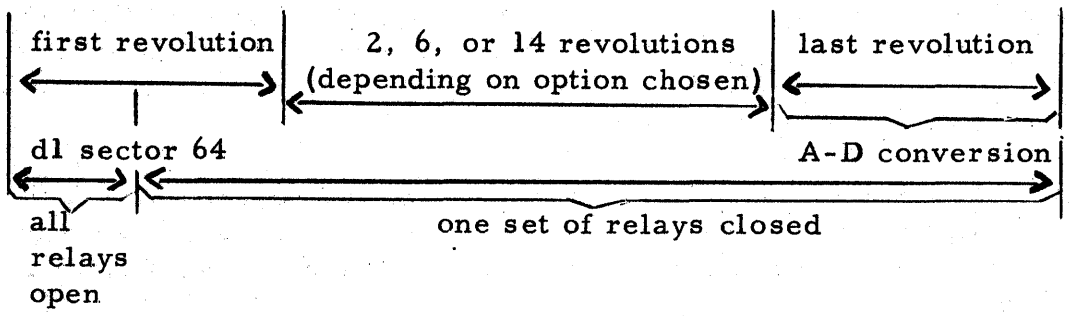
The power inverter is used with logic gates to produce an output, at a lower impedance level, that is logically the inverse of its input. This circuit is used to conserve logical diodes. A true input signal drives the input transistor into cutoff, which drives the second stage into cutoff. The power output stage conducts, its collector dropping to 0 volts, the logical inverse of the input signal. Conversely, a false input drives the input and second stages into conduction and the output stage to cutoff, dropping the output potential to -13.5 volts.

In contrast, PA01, on timing module no. 1, is a power amplifier driving the sector counter flip flops. The power amplifier is used with logic gates to provide an output that is logically the same as its input, but at a lower impedance level. Often a logical function or term must be used in a number of circuits. In such instances, a power gate offers the required signal more economically than does separate formation of the term for each use.

The write control flip flop X8, the second flip flop controlling advance of the sector counter, is true during the second word time of an A-D conversion. When X7 goes false and X8 is true, the analog signal that was just converted is shifted into the drum. X8 is turned on by the true X7 and digit time 20 signals.

3-5b(3). Revolution Counter. The revolution counter establishes the interval of time necessary for the input to the analog amplifiers to stabilize. The counter is stepped by R66D' at digit 20 of sector 127; i. e., one pulse per drum revolution.

A typical conversion sequence occurs during the "first revolution" (X10 = X11 = X12 = X13 = 0). The previously sampled set of analog input relays is dropped out and a new set is pulled in. The transient on the input amplifiers damps out during the remaining revolutions until the "last revolution" (X10 = X11 = X12 = X13 = 1). A-D conversions are recorded during the last revolution only, and the sequence repeats. The sequence is diagrammed below.



If the noise level is high on the low level inputs, 14 drum revolutions are necessary for amplifier stabilization and four flip flops are required in the counter. If the noise level is low, flip flop X13, or X13 and X12, may be omitted. In these cases, six or two drum revolutions occur between "first" and "last" revolutions.

When the last revolution is complete and all A-D conversions for that cycle have been finished, a new set of relays must be selected and the previous set dropped out. To allow time for the former set of relays to drop out before selecting a new set, and thus prevent two input lines from being shorted together, relay control flip flop X6 is provided. X6 is made false from d20 of sector 127 of the last revolution to d1 of sector 64 of the first revolution. When X6 is false, no input relays can be closed, and enough time is allowed for all relays to drop

out before a different set of relays is chosen.

As shown in figure 3-29, X6 is turned on by the most significant digit of the sector counter (F7), and remains on until digit 20 of sector 127 of the last revolution. X6 is a flip flop no. 2 (figure 3-27) mounted in timing module no. 2.

The input relays are divided into as many as 32 groups, and each group may include as many as 32 relays. Electronic switches scan the 32 groups at high speed. One relay in each group can be closed during the first revolution, forming a set of relays. The relay selection counter chooses these sets of relays according to its count. Since there can be 32 sets of relays, the counter has five flip flops, X1 through X5, mounted in timing module no. 2.

The relay selection counter is advanced one count at the same time that the relay gate control flip flop is turned on; i. e., at sector 64 of the first revolution. The new set is chosen by the coincidence of the counter and a true X6 signal. In the standard RW-300, the relay selection counter has five flip flops (for a binary count of 32) with no options. Although fewer than 32 inputs may be used in each group, the relay selection counter completes the total count.

The relay gate contains the logic necessary to interpret the count on the relay selection counter and to close the proper set of relays on the input.

The true or false states of the relay selection counter are applied through diodes in a positive "and" gate, as opposed to the usual negative "and" gates used in the RW-300. When the output of this gate is positive, the appropriate set of relays is closed by a three stage transistor amplifier.

The RG hold down resistors are shunted across the output resistors of the flip flops in the relay control counters. The flip flops draw more current through the smaller collector resistance thus formed, and therefore can handle a greater external load.

The card has an interlock such that if the board is removed, +15 volts is removed from the relay gates to prevent several relay gates from closing simultaneously.

The card also contains part of the test control circuitry, which provides a means to lock the input/output system on a single input.

3-5b(4). Converter and Converter Register. The converter proper consists of the input amplifier, comparison circuits called detector amplifiers 1 and 2, and output amplifiers transferring any difference (resulting from input comparisons) as control to the converter register during A-D conversions or as signal to output circuits during D-A conversions. Module 411 supports the gating and inserts comprising the converter, including the current weighter resistors.

The voltage input amplifier used in the converter system is connected as a 1:4 voltage attenuator and impedance changer. It is a transistorized operational amplifier with an open loop gain of approximately 1400, at 1200 cps. The gain falls to 700 at 80 cps and at 18 kc. Transient response of the circuit produces a final voltage, within ± 0.1 percent, in less than 15 microseconds after a step voltage change. The input is applied to a precision resistor and the compensating power gate output is connected through a second resistor. The summing point is not brought out to an insert pin. Since this point is very sensitive to voltage pick-up, it is protected by a special shield on the back of the insert card. Resistors furnish a negative bias to the summing point so that the power gate can operate at about 5 or 6 volts for normal operation of the input amplifier. The input amplifier is capable of driving a 2500-ohm load over a range of approximately ± 3 volts. Thus it could be used as a bi-polarity A-D converter input as well as the present uni-polarity application.

Two super-beta-connected transistors at the amplifier input minimize the shunting effect of the amplifier input impedance. Two stages contribute to voltage amplification: a common base stage in which the output is in phase with the input, and a common emitter stage producing voltage inversion. Since no inversion is produced in the intervening emitter followers, the output of the over-all circuit is out of phase with the input, and negative feedback is applied through a resistor connected to the input. The output emitter follower supplies the load current at low impedance.

The converter register is a group of 10 flip flops of the type described in paragraph 3-4c(1). In an A-D conversion, each flip flop is set by the output of a current gate actuated by the level on an "add" line.

The positive current gate, weighter resistors, and the positive current gate logic provide the circuitry to switch precision weighted currents into the common "add line". This current is subtracted from the input signal to obtain an error signal.

One of the repeated parts of the three cards noted above is shown in figure 3-30.

The object is to switch a precision current into an add line, or completely cut off the current into the add line. If the junction of R2 and R1 is made negative, the top of the precision 500 k resistor is biased negative, cutting off CR16. Since CR16 is a small silicon diode, the back current is very small. However, if the junction of R2 and R1 is made positive, CR3 is cut off and all the current through the 500 k resistor passes through CR16 to the add line. This current is precision because the 256.6 volts supply is precision, as is the 500 k resistor. Furthermore, the variation in the voltage drop in CR16 is small compared with 256.6 volts.

CR1 and CR2 are back-to-back silicon diodes whose purpose is to limit the voltage excursion at the junction of R2 and R1. The limited excursion reduces the effect of capacitance and allows faster switching.

Diodes CR14, CR13, CR15, and CR20 form the logic for the control of the current switch. If the voltage at CW control 1 is negative, the current switch is biased off, regardless of the action of the other logic. CW1 is used to turn off all current switches for zero stabilization, and also to allow a conversion to take place if under the control of the flip flops.

If both CW1 and CW2 are at ground, the current gate is biased conducting giving a full scale test signal. If CW1 is at ground, and CW2 is negative, the action of

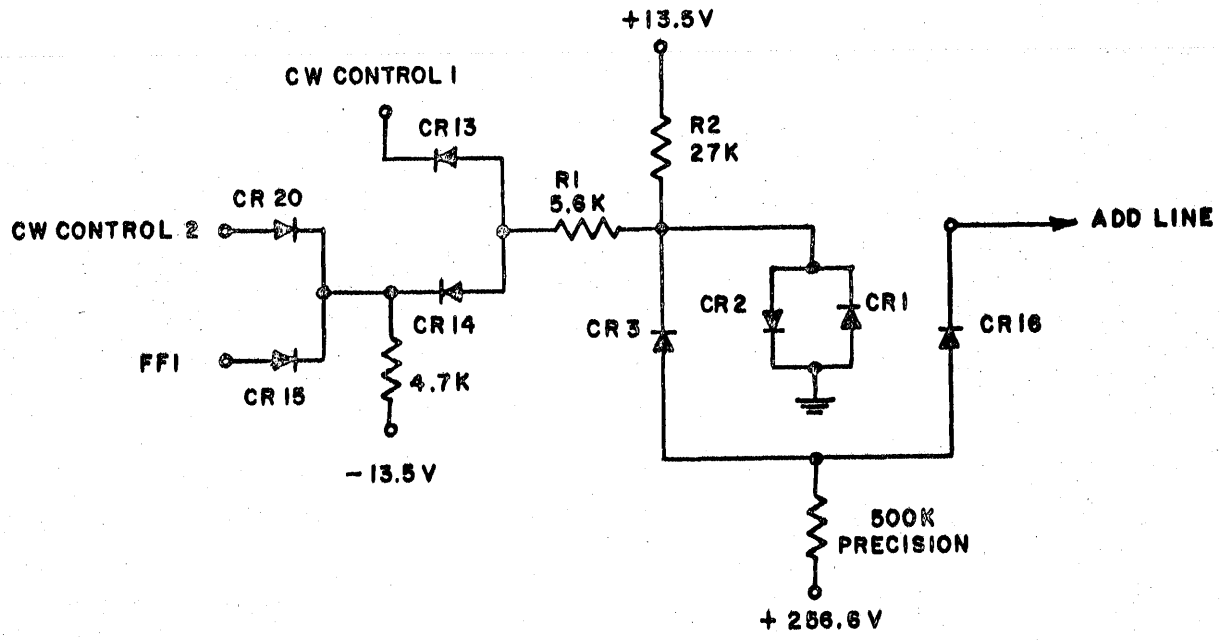


Figure 3-30. Current Conversion Technique, Partial Schematic

the current switch depends on the state of the converter flip flops, as in a D-A conversion.

The reference supply generates the precision 256.6 volts as a standard for analog input/output conversion. The 400-volt supply is dropped through power transistors to form the precision voltage. The base of one power transistor is referenced to three VR tubes, with the reference voltage adjustable through a potentiometer. Constant current through the VR tubes and return for the two zener diodes are each separately transistor-controlled.

A silicon diode compensates for changes (with temperature) in the forward drop of diodes in the current weight gates of the analog to digital converter.

The detector amplifiers amplify the add-line current so it can be used to control either the conversion register, during A-D conversion, or the power gates during D-A conversion. One of each of three types of board terms are used: detector amplifier no. 1 and 2 (DA1 and 2), detector amplifier no. 3 (DA3), and detector amplifier no. 4 (DA4).

DA1 and 2 is an operational amplifier with non-linear feedback. In the linear portion of the operating range, an output voltage is obtained that is proportional to the magnitude of the add-line net current. The feedback causes the add-line voltage change to be very small, thus reducing output of other detector-amplifiers. The emitter of the input stage is connected directly to ground. Therefore, during linear operation, the base is approximately 0.18 volts above ground. Because of an over-all d-c stabilizing feature, the add line is at that potential.

The input (first amplifying) stage of the detector drives the nonlinear feedback. The output voltage of the stage (in its linear operating range) is equal to the net add-line current times 10 k. A transistor isolates the first and second stages of amplification; while diodes form an anti-saturation circuit for the subsequent amplifier stages. Two outputs are provided by this detector. The first is output no. 1 which changes in a negative direction when the add-line net current becomes positive. Output no. 2 changes in a positive direction when the add-line net current becomes positive. Only output no. 2 is used for the A-D, D-A converter. If a bi-polarity converter with both positive and negative current weights were to be constructed using this detector amplifier, both outputs would be utilized.

Detector amplifier no. 3 is used to control the converter register during A-D conversion. The circuit consists of a differential amplifier, one stage of which receives the signal from DA1 and 2, while a constant bias is applied to the base of the second stage by a potentiometer. The output on this detector is furnished in a circuit arrangement that is quite similar to the output circuit of flip flop no. 2.

Detector amplifier no. 4 is also a differential amplifier, used to drive the power gates during D-A conversion. The two outputs have the same phase, one of which provides a low impedance to +15 volts while the other provides a low impedance to -5 volts.

Since the output of DA4 must drive a number of power gates, the DA4 power amplifier, consisting of six emitter followers, is used to provide power gain at the output of detector amplifier no. 4.

3-5b(5). Analog to Digital Conversion Time and Location Control. Four options are available relative to the number of voltage gates at the input. Since a maximum of 32 relays per group may be used, and one drum track can store a maximum of 128 words, the options are known by the number of voltage gates

and the number of tracks necessary. The options are: the 4 voltage gate, 1 track system; the 8 voltage gate, 2 track system; the 16 voltage gate, 4 track system; and the 32 voltage gate, 8 track system. In any case, all voltage gates are sampled during a single drum revolution (the last revolution), and a total of 32 last revolutions are necessary to sample all inputs. The four options will be described separately in the following paragraphs. In all cases, location selection is effected during the first word time after the conversion command is effected, and actual recording is accomplished during the second word time, as indicated in paragraph 3-5b(2).

Since all voltage gates are sampled during each last revolution, four samples must be taken in the last revolution in the 4 voltage gate, 1 track system. Further, the four samples taken must be recorded on the drum in such a way that succeeding samples are recorded in different drum sectors.

The location of a particular sample on the drum is determined by identity between the relay selection counter and five least significant bits of the sector counter. The voltage gate selected is determined by the two most significant bits of the sector counter. Thus, when the relay selection counter is at 00000, an input conversion will be commanded whenever the five least significant bits of the sector counter are 00000, and the four voltage gates will be chosen by the two most significant bits. Then, the first channel will be sampled at sector 0000000 (0), the second at 0100000 (32), the third at 1000000 (64), and the fourth at 1100000 (96). The relay counter is then advanced one count to 00001. When the next four conversions are taken, the two counters are again compared and the conversions are at sector numbers 01, 33, 65, and 97. This sampling procedure continues until the track (track 8) is filled with a total of 4 times 32, or 128 words.

With eight voltage gates to be sampled each last revolution, the converted inputs are recorded into every sixteenth sector on the drum. Since there may be 32 inputs per voltage gate, a total of 32 times 8, or 256 inputs must be accommodated, making two tracks necessary. The location of the sample on the drum is again established by a comparison between the relay selection counter and the five least significant bits of the sector counter. In this case, the most significant bit determines on which track (8 or 9) the sample should be recorded. The four least significant bits determine the track location, allowing eight samples per revolution. The voltage gate in the 8 voltage gate, 2 track system is selected by the three most significant bits of the sector counter.

If the relay selection counter is at 00000, the first eight samples will be converted at the location of track 8, sectors 0, 16, 32, 48, 64, 80, 96, and 112, and the second set at sectors 1, 17, 33, 49, 65, 81, 97, and 113. The samples continue until the track is full and X5 becomes true. The information is subsequently recorded on track 9 (the next track) in a similar manner.

The technique is extended to accommodate a maximum of 1024 inputs, recorded into eight tracks. Figure 3-31 summarizes the circuits involved in each system option.

	Relay Selection	Voltage Gates	Sector Compare	Track Number
4 vgs	X1, X2, X3, X4, X5 X6	F7, F6	F1, F2, F3, F4, F5 X1, X2, X3, X4, X5	X8
8 vgs	X1, X2, X3, X4, X5 X6	F7, F6, F5 X7	F1, F2, F3, F4 X1, X2, X3, X4	X5 X8
16 vgs	X1, X2, X3, X4, X5 X6	F7, F6, F5, F4 X7	F1, F2, F3 X1, X2, X3	X4, X5 X8
32 vgs	X1, X2, X3, X4, X5 X6	F7, F6, F5, F4 F3 X7	F1, F2 X1, X2	X3, X4, X5 X8

	Revolution Counter
4 rs	X10, X11
8 rs	X10, X11, X12
16 rs	X10, X11, X12, X13

Figure 3-31. Summary of Circuits Used in Various Input System Options

The input voltage gate module bears the required number of voltage gates depending upon the input option employed. The voltage gate is a high speed ohmic switch, similar to a single-pole, single-throw contact. This switch has a very linear transmission characteristic and low leakage. The equivalent voltage source at the switch (when closed) is less than one millivolt at 25° C. Because of this voltage offset, this device is used only to switch time level signals at high speeds.

The switch is a modified six diode gate, made conducting by charging a capacitor and permitting it to discharge through a diode. Due to the gating technique, the switch can be on for only about 300 microseconds. The state

of the control signal is brought out from the collector of each of the two transistors for control of other gates.

The data applied to the converter register in an analog to digital conversion is recorded on the drum in the required track (s) during the second word time. The signals driving the write circuits are produced by the power inverters.

3-5b(6). Digital to Analog Conversions. Digital to analog conversion in the RW-300 is performed on every even sector, unless an analog to digital conversion is in process. This indicates that on every even sector, a number from track 7 is read into the converter register, setting up the proper weight from the current switches. The converted number is matched into the output controlled device by the power gate, and the voltage or current at the controlled device is monitored at the detector amplifiers through a voltage gate. The particular output is chosen by the seven bits of the sector counter and X7' (indicating no analog to digital conversion is in process), and this count simultaneously closes the voltage gate and power gate associated with that output.

The RW-300 has 36 outputs, and there are 64 even sectors on the drum. Obviously, some of the numbers read from the drum are converted but not used since there are no output gates associated with these numbers. (These conversions are redundant and have no effect on the equipment.)

Output conversions are taken on every drum revolution except when an analog to digital (A-D) conversion is in progress. Since A-D conversions are taken only during the last revolution of the drum, in extreme cases only one drum revolution can be lost in an output conversion. The power gate can maintain an output to within $\pm$0.1 percent for two drum revolutions (33.2 ms), so this omission is usually negligible. Inasmuch as the maximum number of analog to digital conversions in the last revolution is 32, the other 96 word times are available for digital to analog conversions.

A number requiring D-A conversion is shifted into the converter register at the same time the result of an A-D conversion is being shifted out. However, if a number has been shifted into the register for D-A conversion and an A-D conversion is commanded, the number is cleared out of the register, and the A-D conversion proceeds.

The power gates furnish an analog voltage memory, as well as a means for charging and discharging the memory capacitor. The output of the power gate can drive a 3000-ohm load resistor from 0 to +15 volts, maximum. The holding time is one-thirtieth of a second maximum, which, in the most extreme case, will result in a 20-millivolt output drop if the power gate is energized every one-thirtieth of a second. The average noise is then 10 millivolts or 1 least count. In most cases it will be less than 10 millivolts.

A resistor is provided at the power gate to compensate for the load reflected by the output transistor during output conversion (due to the input resistor of the input amplifier). Hence, the resistor is disconnected from ground during output servo time, and is reconnected to ground through diodes between servo times.

Three output modules, bearing power gates, associated voltage gates, and necessary logic may be installed within the RW-300 Computer assembly.

3-5c. STANDARD SYSTEM OPTIONS. Three sets of options are available in the analog input/output subsystem of a standard RW-300 Computer. The sets are independent of one another and shall be considered separately. The options are easy to implement since they are provided within the standard machine. Many other variations can be effected, but the standard options should cover most cases.

The options will be discussed first, and then the basic limitations of the machine will be itemized so that all changes can be considered as they become necessary.

3-5c(1). Analog Output Option. The digital to analog conversion starts on every even sector time in the RW-300. These conversions occur whether or not an output gate is plugged in for a given channel. Thus, addition of an output channel consists of plugging in a voltage gate, a power gate, one "and" gate, and connecting the output to the Computer.

The output circuits are packaged 12 to a module. Three modules are standard in the RW-300. Any number of modules and voltage gate-power gate pairs may be omitted. Two voltage gates are packaged on each card, making an extra voltage gate necessary for an odd number of outputs.

3-5c(2). Revolution Counter Option. A certain period of time is required for the transient to damp out on the input amplifier-filter combination. The revolution counter counts revolutions of the drum when the input relays have been switched, to provide this settling time. If the noise level is high, more filtering is necessary, and thus more time is required for the amplifier to reach steady state. The standard RW-300 can provide three sampling speeds: 14, 6, and 2 revolutions of the drum, (plus the first and last revolutions in each case).

The three speeds are determined by the number of flip flops in the revolution counter, and a minor change on one of the logic cards. The change in speed does not alter the speed or logic of the input/output operation, but the input/output is idle for a different interval of time for each of the three speeds. A complete conversion of all analog inputs takes 2.13, 4.26, or 8.53 seconds, depending on the number of flip flops in the revolution counter.

3-5c(3). Analog Input Option. The Computer is rarely used with a full comple-

ment of 1024 analog inputs; however, the need for any number of inputs between 1 and 1024 must be anticipated. These input signals may be quite varied with respect to voltage level, and thus a certain degree of flexibility is necessary.

As described earlier and as shown in figure 3-29, the converter scans up to 32 groups of inputs through high speed voltage gates, and each group can be driven by as many as 32 analog inputs each through a mercury-wetted contact relay. In a system employing fewer than the full complement of 1024 inputs, the superior method for applying the inputs to the converter may involve a decrease in the number of groups and/or a decrease in the number of inputs per group (the number of sets of inputs).

There are four standard input systems as described in paragraph 3-5b(5):

a. the four voltage gate, one track system;

b. the eight voltage gate, two track system;

c. the 16 voltage gate, four track system; and

d. the 32 voltage gate, eight track system.

Selection of the system depends upon how the converted numbers are placed on the drum. In the four voltage gate system, four numbers (words) are recorded on the drum during the last revolution. These four words are equally spaced around the drum, for example, at sectors 0, 32, 64, and 96. During the next last revolution, the four gates are again closed in sequence and the conversions are recorded into sectors 1, 33, 65, and 97. This sequence continues for 32 conversions until the track is full (128 words).

In the eight voltage gate, two track system, all voltage gates are sampled during the last revolution (as noted above), but this is a total of eight samples. The words are located equally around the drum, for example, at sectors 5, 21, 37, 53, 69, 85, 101, and 117. The samples at the next last revolution will be recorded at sectors 6, 22, 38, 54, 70, 86, and 102. This procedure continues until the track is full, and then the second track is filled.

In the 16 voltage gate, four track system, a similar sequence is followed.

In the 32 voltage gate, eight track system, the same sequence is followed. However, this time 32 samples are taken during the last revolution. These samples, as before, are equally spaced around the drum, for example, at sector locations 1, 5, 9, 13, 17,...., 121, and 125. During the next last revolution the numbers go in sector locations 2, 6, 10, 14, 18,...., 122, and 126. When this track has been filled (after four last revolutions) the words are recorded into the next track, and so forth until all eight tracks are filled.

Note that in these options, the number of necessary tracks jumps from one to two when the number of input groups is increased from four to eight. But this statement is not strictly true. If, in this case, there are only 16 relays (sets) on all groups, the second track is not necessary because the sequence of recording on the drum (as discussed above) results in filling one track before moving to the next. The input/output system continues to sample sets 17 through 32 and to present the conversions for recording in track 9 (which is not connected). The condition above would be desirable if there were a number of different types of analog inputs, and only a few inputs of each type.

It is also possible to use less than four, eight, 16, or 32 input groups, as the case may be, in the standard system. Although part of each track is filled with zeros, the resulting installation could prove more economical than one requiring the larger number of output amplifiers. The internal logic of the machine recognizes only the four options previously listed. But by decreasing the number of sets of inputs failing to wire a write head, a track can be released for other purposes. Furthermore, all groups for a given option need not be used if the drum space is not at a premium. Thus, the number of input amplifiers is reduced.

The comments above are summarized in figure 3-32. The table shows the maximum number of analog inputs (relays) per group as a function of the number of drum tracks used and the number of input groups. Also indicated is the option as recognized by the internal electronics of the converter.

The information on this chart is expanded in figure 3-33 to indicate the maximum number of analog inputs as a function of the number of tracks and the number of input groups used. Data from figure 3-33 is plotted in figure 3-34 as a quick reference to aid in the choice of an analog input configuration.

The use of these tables can be illustrated with an example. Assume it is necessary to monitor 75 thermocouples, each an input in the range of 0 to 10 millivolts; 40 strain gages, each producing an input in the 0 to 35 millivolt range, and 40 high level inputs at 0 to 10 volts. A maximum of 32 inputs may comprise a group, so there must be at least three groups in the 0 to 10 millivolt range; two groups in the 0 to 35 millivolt range; and two groups in the 0 to 10 volt range. A minimum total of seven groups is necessary. A dot is put at the intersection of 155 inputs and seven groups on figure 3-34. Any combination to the right and above this dot is realizable. In this example, there can be seven groups on two, three, four, six, seven, or eight tracks, or eight groups on five tracks or 10 groups on two tracks, etc. Probably the best combination would be seven groups on two tracks.

Examination of figure 3-33 shows that it is possible to include 224 inputs in the selected combination. Figure 3-32 indicates that there can be 32 inputs per group, and the eight voltage gate, two track system is to be used. If necessary, another group may be added later, providing 256 inputs in eight groups.

Economics is usually the deciding factor in the choice of input configuration.

In some military applications, however, it may be desirable to scan the inputs with minimum inter-sample delay. If this were true in the above example, the 32 voltage gate, eight track system may have been chosen using 20 groups and two tracks. Notice that this combination is realizable, as shown in figure 3-34, and allows a total of 160 analog inputs.

The four voltage gate options are chosen by a simple wiring change on one of the logic cards.

Number of Input Groups

	Number of drum tracks used 1	2	3	4	5	6	7	8
1-4	W 32	X 32	Y 24	Y 32	Z 20	Z 24	Z 28	Z 32
5-8	X 16	Y 32	Y 24	Y 32	Z 20	Z 24	Z 28	Z 32
9-16	Y 8	Y 16	Y 24	Y 32	Z 20	Z 24	Z 28	Z 32
17-32	Z 4	Z 8	Z 12	Z 16	Z 20	Z 24	Z 28	Z 32

W = 4 volt gt, 1 track sys.
X = 8 volt gt, 2 track sys.
Y = 16 volt gt, 4 track sys.
Z = 32 volt gt, 8 track sys.

$$\text{Maximum Total Number of Inputs} = \left[\frac{\text{Inputs}}{\text{group}}\right] \left[\text{Number of groups}\right]$$

Figure 3-32. Maximum Number of Analog Inputs Per Group, Chart

NUMBER OF INPUT GROUPS \ TOTAL NUMBER OF TRACKS USED	1	2	3	4	5	6	7	8
1	32	32	24	32	20	24	28	32
2	64	64	48	64	40	48	56	64
3	96	96	72	96	60	72	84	96
4	128	128	96	128	80	96	112	128
5	80	160	120	160	100	120	140	160
6	96	192	144	192	120	144	168	192
7	112	224	168	224	140	168	196	224
8	128	256	192	256	160	192	224	256
9	72	144	216	288	180	216	252	288
10	80	160	240	320	200	240	280	320
11	88	176	264	352	220	264	308	352
12	96	192	288	384	240	288	336	384
13	104	208	312	416	260	312	364	416
14	112	224	336	448	280	336	392	448
15	120	240	360	480	300	360	420	480
16	128	256	384	512	320	384	448	512
17	68	136	204	272	340	408	476	544
18	72	144	216	288	360	432	504	576
19	76	152	228	304	380	456	532	608
20	80	160	240	320	400	480	560	640
21	84	168	252	336	420	504	588	672
22	88	176	264	352	440	528	616	704
23	92	184	276	368	460	552	644	736
24	96	192	288	384	480	576	672	768
25	100	200	300	400	500	600	700	800
26	104	208	312	116	520	624	728	832
27	108	216	324	432	540	648	756	864
28	112	224	336	448	560	672	784	896
29	116	232	348	464	580	696	812	928
30	120	240	360	480	600	720	840	960
31	124	248	372	496	620	744	868	992
32	128	256	384	512	640	768	896	1028

Figure 3-33. Detailed Chart of Maximum Number of Analog Inputs Per Group

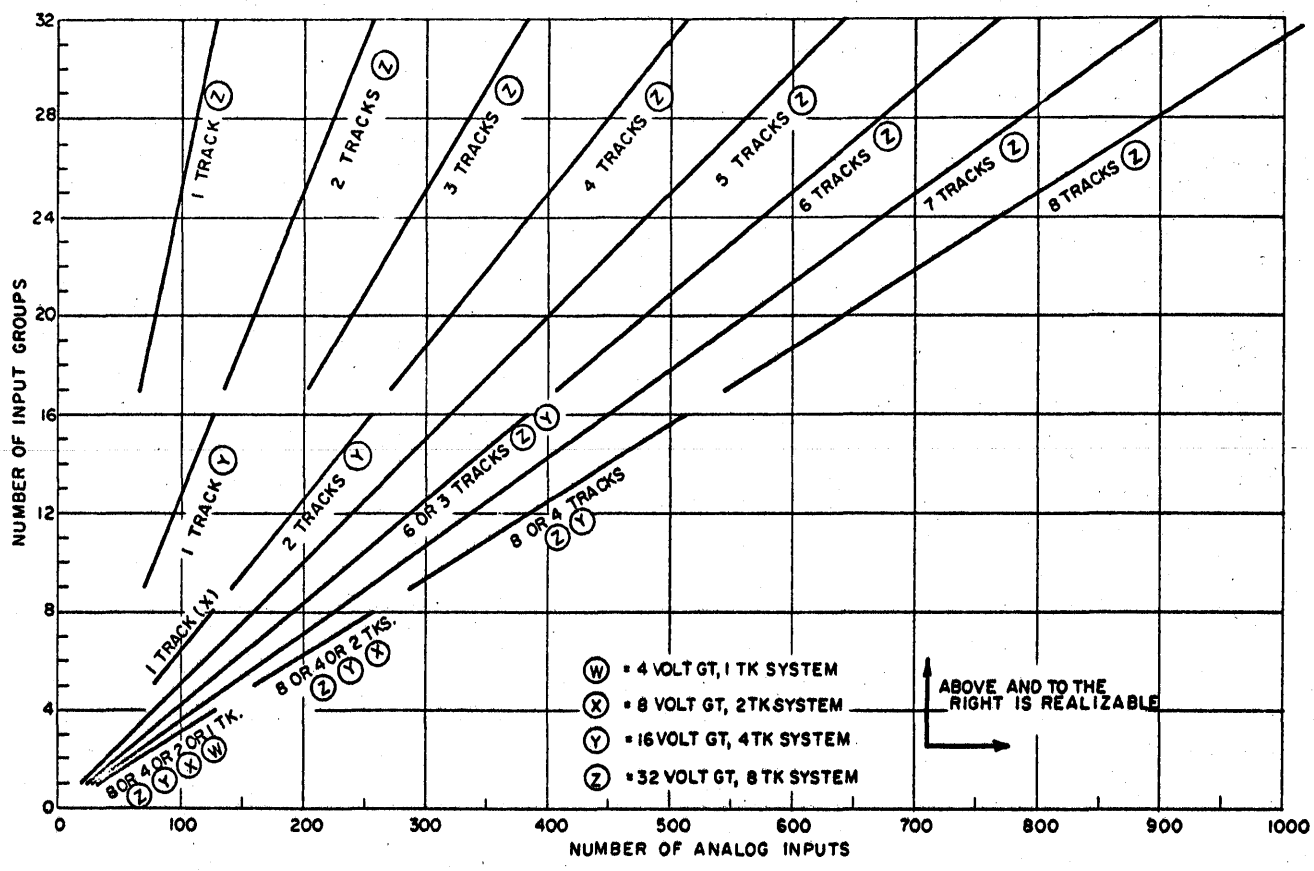


Figure 3-34. Data of Figure 3-33 Graphed

3-5d. NON STANDARD SYSTEMS. The modules in the analog input/output subsystem have been designed so that certain non standard features are possible with no module changes except wiring on the external module connectors. Non standard variations are so extensive that rather than list possible changes, the limitations of the machine are described in this section.

Within limitations, it is possible to convert some inputs every revolution, and other inputs only during the last revolution of each input cycle.

Outputs can be distributed (to some extent) along track 7 without using more than one module for up to 12 outputs.

By control of three flip flops X6, X7, and X8, it is possible to control the input/output system to a large degree. These flip flops have extra diodes in their input gating which makes special control possible.

Provisions exist for adding a flip flop, power amplifier, power inverter, and two universal logic cards (or special inserts) to make non standard provisions possible with standard modules.

Examples of machine limitations are:

a. The converter requires two word times to perform an input conversion and record it on the drum.

b. The converter requires two word times to read a number from the output track and perform an output conversion (update an analog output voltage).

c. A maximum of 64 conversions (input plus output) are possible each drum revolution.

d. An output conversion is not possible during an input conversion time, nor during the word time following an input conversion (when the result of the input conversion is being transferred from the converter register to the drum memory).

e. It is normal to read an output number into the converter register while writing the result of an input conversion, but it is not possible to read an output number into the converter register during an input conversion.

f. Outputs are read from track 7 only during even sector times (F1 = 0) and output conversions occur only during odd sector times (F1 = 1).

g. It is normal to read an output number into the converter register during an even sector time which precedes an input conversion. In this case the conversion register will be reset to 0 at digit 20 of the even word time.

3-6. CLOCK GENERATOR AND POWER SUPPLY.

The various power levels and polarities required internally by the RW-300 Computer are produced by the clock generator and power supplies located on the clock generator and power supply chassis and on the Relay Junction Box. Both chassis are essentially conventional in design, heavily anodized to aid in insulating power transistors and diodes.

3-6a. CLOCK GENERATOR. The clock generator accepts the signal from the clock track on the drum and generates a pulse at +18 volts, 0.6 microseconds wide, for gating in the Computer.

The signal on the clock track is a sine wave recorded to insure precision continuity around the track at the basic frequency of 153.6 kc. The exact frequency is a function of drum speed (3600 rpm) and of the total number of bits a track may store.

Clock track read circuit R65 shapes the clock pulse into a somewhat squared a-c signal. Read circuit output and its complement are coupled into two separate but virtually identical clock pulse generator circuits. Following an input isolation amplifier, each generator consists of a multivibrator, a cathode follower, and an output amplifier.

The signal input stage of the multivibrator is normally conducting. A negative-going pulse from the input amplifier drives the multivibrator into the alternate state, applying a sharply negative-going pulse to a delay line. Reflection from the delay line produces a positive-going pulse which is applied to the signal input stage of the multivibrator, restoring conduction. A zener diode, common to the cathode circuits of both multivibrators, establishes the minimum level at which triggering can occur. Since the signals applied to the clock generator circuits are complements of one another, the common cathode clamp insures that the time between the rise of clock A and the rise of clock B is the same as the time between the rise of clock B and the rise of clock A.

The delay lines control the pulse width to the desired 0.6 microseconds (at mid-amplitude on leading and trailing edges of the pulse). Each delay line is shunted by a diode to minimize ringing. The pulse generated is coupled through a cathode follower to an output power amplifier. Pulse amplitude may be controlled by a potentiometer, on the Test and Maintenance panel, that adjusts the operating point at which the output amplifier functions. Output is developed across the secondary of the transformer, clipped at ground level by diodes, and is restored to an a-c function by a shunt choke. Therefore, the level between clock pulses is approximately -2 volts, preventing any ambiguity in the gating action in the Computer. Time between clock A pulses is nominally 6.5 microseconds; and that between clock A and clock B pulses is exactly one half the time between clock A pulses.

The clock B output is interlocked with respect to the circuit supply voltages (-27 volts and +15 volts). Should clock B drop below approximately +12 volts, the negative-going change is coupled through an integrating capacitor into the base of a feedback circuit transistor, decreasing the current drawn and resulting in interruption of the contacts on a relay and removal of the +15 volt supply from the Computer circuits.

3-6b. POWER SUPPLIES. The regulated power supply for the clock generator circuits is conventional, with the transformer being mounted on the Relay Junction Box. A voltage regulator tube and feedback amplifier control regulation, maintaining constant output at the cathodes of parallel-connected 6080 WA.

The power supplies generating the principal Computer circuitry voltages are transistorized. The regulation technique utilizes a separate transformer winding and an output emitter follower, the base of which is maintained at a constant voltage. Each supply is regulated to within ±1 percent of nominal value. Base voltage is restricted in variation by dropping the input voltage through a series-connected 1500-ohm resistor and zener diode. The variation at the junction of the resistor and diode is only approximately one-fortieth as severe as at the input. By means of a second such diode/resistor regulating network, the variation is further reduced by a factor of 9 or 10 to one.

Actual output voltage is obtained through a separate rectifier circuit. Examining the -27 volt supply first, regulation is introduced at the base of a transistor which drives two tandem-connected power output transistors. A potentiometer (in series with the emitter and four zener diodes) mounted on the Test and Maintenance panel provides adjustment of the level. The -5 volt source is derived from the -27 volt supply by a separate emitter follower. The level at the base of this stage is varied to change the output voltage at the emitter.

The regulated voltage at the base of this transistor is also used to maintain the +15 volt supply output. Coupled through a resistor, any change in regulation signal is applied to the base of a transistor which drives the tandem-connected power output transistors in the +15 volt supply. Output is presented at the contacts on a relay and to the adjustment potentiometer on the Test and Maintenance panel. When the -27 volt source is appropriately negative (no more positive than approximately -18 volts) and the clock B pulse is more positive than approximately +12 volts, current through the relay winding closes the contacts, applying +15 volts to the circuits as required.

A separate but similar transistorized supply is provided on the Relay Junction Box to generate the regulated -13.5 volts required by the relays.

3-7. TEST AND CONTROL GROUP

The test and control group within the Computer provides for three basic types of operation: normal, code check, and testing.

In normal operation, the switches on the Control panel, illustrated in figure 3-35, provide for powering the Computer, loading or starting a program, and stopping and resuming either loading or program execution. Lights within the switch assemblies, plus the STANDBY light, indicate the status of the Computer operation.

For code checking, single instruction operation can be effected through the switches on the Test and Maintenance panel, and register contents may be inspected by means of the display features described in paragraph 3-7c.

Diagnostic testing of the Computer employs the metering and adjustments also located on the Test and Maintenance panel and includes a bank of neon indicators for displaying the condition of the output of certain flip flops, as discussed in paragraph 3-7d.

3-7a. CONTROL PANEL. The circuits associated with the Control panel apply power to the Computer in the proper sequence and provide, with appropriate interlocks, the circuit closures producing the logical signals necessary to control the Computer in automatic operation.

The buttons on the Control panel are **POWER ON, POWER OFF, START, LOAD, STOP,** and **RESUME.** All buttons are spring-loaded momentary contact and/or release and, with the exception of the **POWER OFF** button, are back-lighted with 12 volt lamps which are called by the corresponding button name. The **STANDBY** light has the physical appearance of a button.

Pressing the **POWER ON** button energizes the hold relay in the Relay Junction Box which applies full voltage to the drum motor, the clock power supply transformers, the time delay, and the **STANDBY** light. After approximately two minutes, the heating-type time delay closes, energizing the time delay relay. Power is applied to the d-c low voltage supplies, the **STANDBY** light goes out, and the **POWER ON** light illuminates.

The **START** and **LOAD** buttons control two relays which are connected to assume one of three possible states:

a. **START** relay de-energized, **LOAD** relay de-energized;

b. **START** relay energized, **LOAD** relay de-energized; or,

c. **START** relay de-energized, **LOAD** relay energized.

Initially, neither relay is energized and neither light is illuminated. The Computer idles in state 8, since a series circuit through the normally closed contacts on each relay parallels the **STOP** button contacts. When either **START** or **LOAD** button is pressed, the corresponding relay is energized and is held through its normally open contacts in series with the normally closed contacts on the alternate relay. Should the alternate button be pressed, energizing its relay opens the holding circuit for the first relay, and establishes a similar holding circuit for the alternate. Hence, the light associated with the button last pressed remains on (except following removal of power from the Computer).

The light behind the **STOP** button is controlled as follows. A relay driver whose input logic is S1' S2 S3 Z1 controls a relay with single-pole, double-throw contacts. A true output from the relay driver occurs in state 8, de-energizing the relay and illuminating the **STOP** light. The threshold of relay action is set to

prevent chattering as the Computer cycles between states 1 and 8.

3-7b. TEST AND MAINTENANCE PANEL. Located under the top cover of the RW-300 is the Test and Maintenance panel (see figure 3-35).

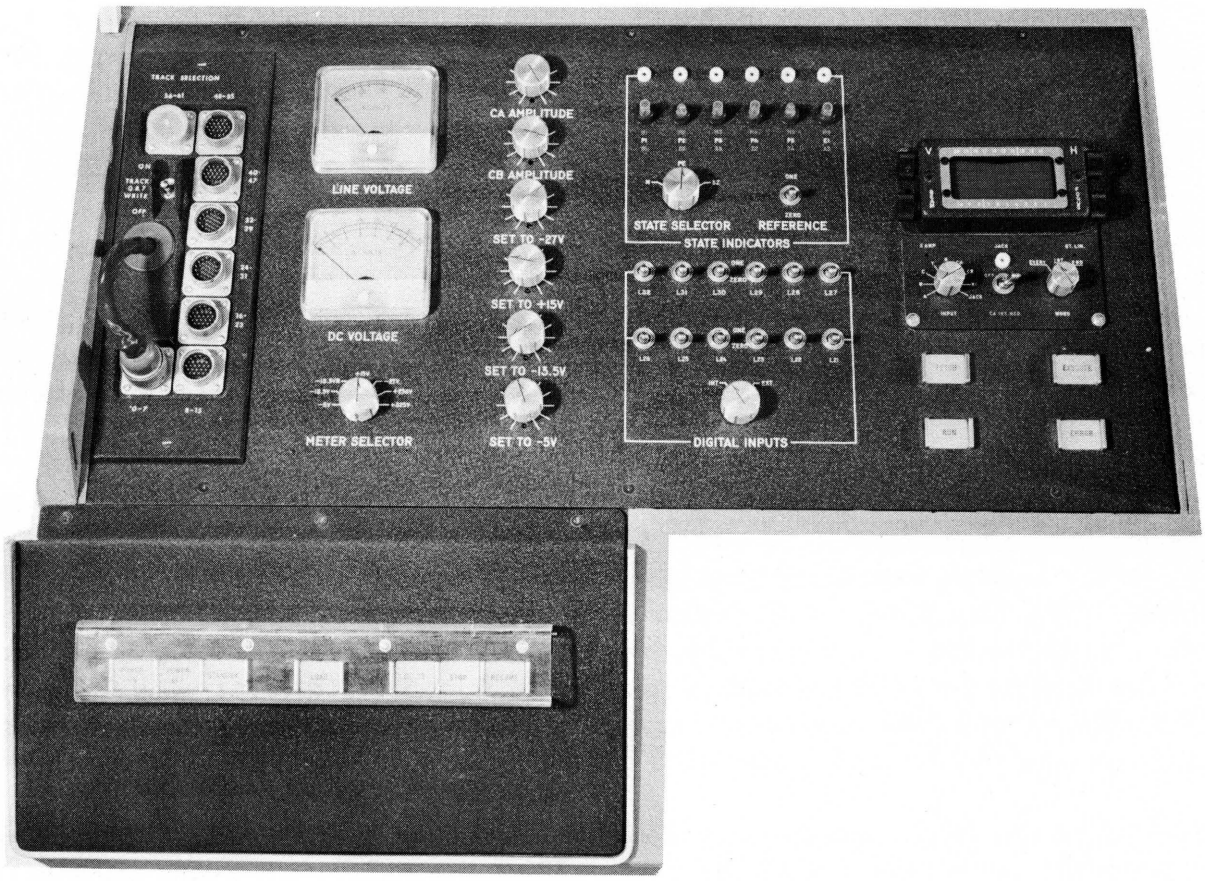


Figure 3-35. Test and Maintenance Panel and Control Panel

Available at this panel are

a. Plug and jack selection of one of eight groups of writable tracks and the switch protecting data on tracks 0 and 7, as described in paragraph 3-2c;

b. Meters, switches, and controls for marginal testing (see paragraph 3-7f);

c. A bank of neon bulbs indicating the condition of the flip flops selected by a switch, and a set of pin jacks at which the output of each flip flop appears for waveshape inspec-

tion through use of the oscilloscope, described in paragraph 3-7d;

d. A set of switches for interrupting digital input lines to apply fixed bias for circuit testing (see paragraph 3-7e);

e. The oscilloscope assembly, including an input selector switch, clock intensification switch, and word display selector switch, as detailed in paragraph 3-7c(2); and,

f. FETCH, EXECUTE, and RUN buttons, and the RECORD ERROR indicator light, operations that are discussed in paragraph 3-7c(1) and 3-2c.

3-7c. CIRCUIT MONITOR. To permit inspection of the contents of the registers, primarily for code checking, operation of the Computer can be interrupted. While the Computer idles, the contents of the selected register can be displayed on the oscilloscope. Control and display constitute the circuit monitor function.

3-7c(1). Fetch and Execute Operations. The contents of the registers are of interest immediately after state 3, in which the next instruction address is shifted into the N register and the execution time for the current instruction is shifted into the C register. The Computer is forced to remain in state 4 by including a term in the state 4 logic which is produced by the FETCH button on the Test and Maintenance panel. The Computer is permitted to pass state 4 by a logic term generated by the EXECUTE button, but can return to automatic processing only by reset of the fetch and execute operations. The RUN button controls the reset.

The circuit for the fetch, execute, and run operation is illustrated in figure 3-36. The RUN switch is in series with the return from the -13.5 volt relay supply. In the automatic operation, the return circuit is completed only through the lamp in the RUN button assembly. A -5 volt source is coupled through the normally closed pairs of contacts on the FETCH and EXECUTE switches and the relay contacts to appear as true FT' and EX' levels at the jacks providing connection into the arithmetic and control portions of the Computer. A +15 volt source is used as the false EX output.

Mechanically, the push buttons are manually set and automatically reset. However, when either FETCH or EXECUTE button is pressed, power is first applied to the associated relay winding, through the normally open pairs of contacts, which pulls the relay contacts into the energized position. Relay current is then drawn through a set of contacts on each relay. Thus, powering the alternate relay by pressing the alternate button opens the first relay winding circuit.

Momentary interruption of the RUN switch de-energizes both relays and restores automatic computer operation. While a given relay is energized, +15 volts appears

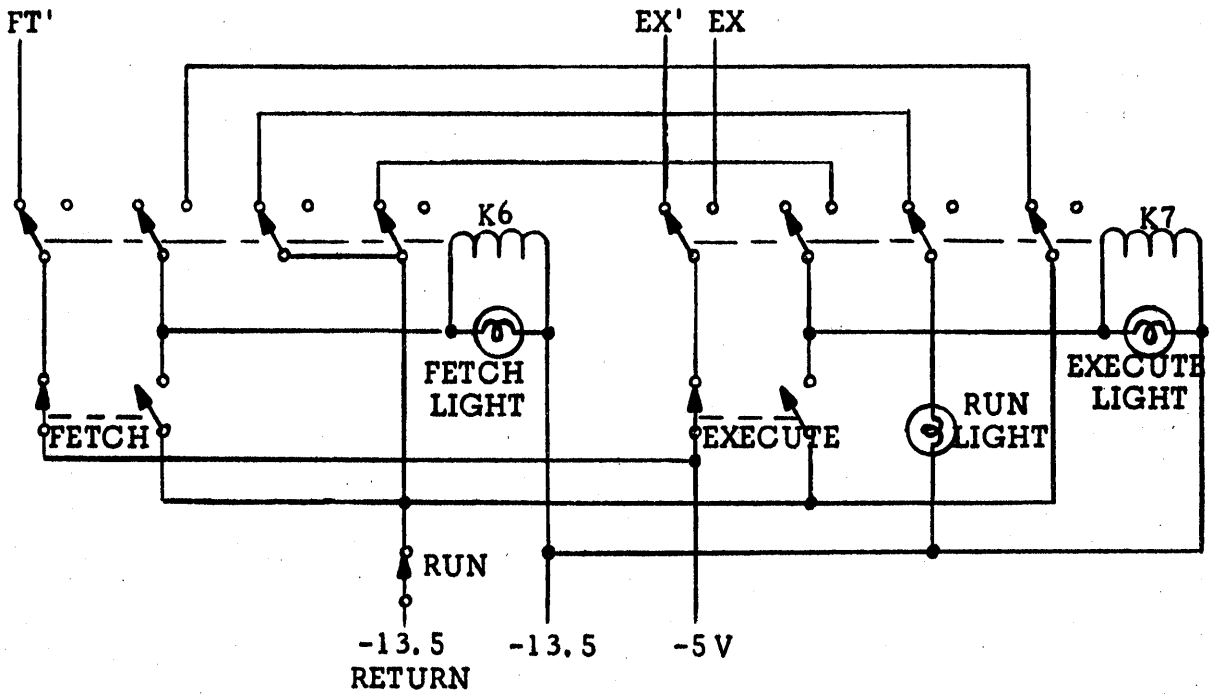


Figure 3-36. Circuit for Suspending Computer Operation, Simplified Schematic

at the complement output line and, in the case of K7, the -5 volt true output appears at the EX line. Single instruction operation of the Computer is thus provided.

3-7c(2). Display Capability. Consisting of an oscilloscope, selection switches, and associated circuitry, the display system included in the RW-300 provides visual observation of

a. The contents of any of the five circulating registers;

b. The next instruction pair after the EXECUTE button is pressed;

c. The operand after the FETCH button is pressed; or,

d. The waveshapes at the output of the flip flops connected to the STATE INDICATORS.

The operation of the oscilloscope assembly is described below with reference to the block diagram of figure 3-37.

The signal available at the input selector switch, from a circulating register, is displayed on the CRT as a lower level trace representing, from right to

left, digits 1 through 10, and an upper level trace representing, from right to left, digits 11 through 20. A downward excursion of the trace, from its baseline, is produced by a "1" digit input. To identify the digit, clock intensification can be introduced. The resulting display consists of 20 bright dots located either on one of the baselines or in the corresponding "1" amplitude positions, depending upon the digit. When a flip flop output waveform is to be displayed, clock intensity modulation may be removed.

The vertical and horizontal amplifiers and the high voltage power supply are furnished with the oscilloscope. To provide the display described above, sweep and sweep control circuitry (in part located on the oscilloscope assembly and in part on the Test and Maintenance panel assembly) is required.

While more efficiently utilizing the CRT face and offering optimum "readability" of the display, the two-level trace requires a two-cycle per word sweep which retraces between digits 10 and 11 and between digits 20 and 1, and a change in vertical positioning bias between these digits.

Since digit 10 is not defined as a single combination of the T flip flops (see figure 3-13), the necessary signals are simulated by using digit group 9-13 and digit 19, respectively, to set Z12, a low level flip flop providing a one-bit delay. Two additional signals are applied with digit group 9-13 to specify digit 9 only. Z12 is reset in digit times 10 and 20 by the Z12 output, thus preventing an output by digit 10 of the Z12j input group.

The vertical bias, required in conjunction with the two-cycle trace to position the display, also aids in preventing an output by any digit other than d9, of the 9-13 group. The output of Z12, true at digit times 10 and 20, is applied to the j input of a d-c flip flop, V19, with the digits 19 and 20 signal, and to the k input of the flip flop with the digits 1-18 signal.

The d-c flip flop is triggered by clock pulses in conjunction with a true (negative at clock time) input signal. The input stage on either side of the circuit is cut off by a true input signal, permitting transfer of the clock pulse to the corresponding side of the flip flop. Triggered to conduction by the clock pulse, this side of the flip flop presents a low (true) output voltage which is maintained until re-triggered by the next clock pulse or until overcome by application of a true signal on the alternate input stage. Absence of a true input at clock time inhibits flip flop triggering.

V19 is therefore set at digit time 20 and reset at digit time 10, and its output is a square wave true (dropping instantaneously) at digit time 20 and false (rising) at digit time 10. Since V19 goes false at digit time 10, it prevents a Z12j input from being created by digits 11 through 13 of the digits 9-13 signal. The principal use of the V19' output is the application to the vertical amplifiers of the oscilloscope, as a positioning bias. An emitter follower isolates the flip flop from

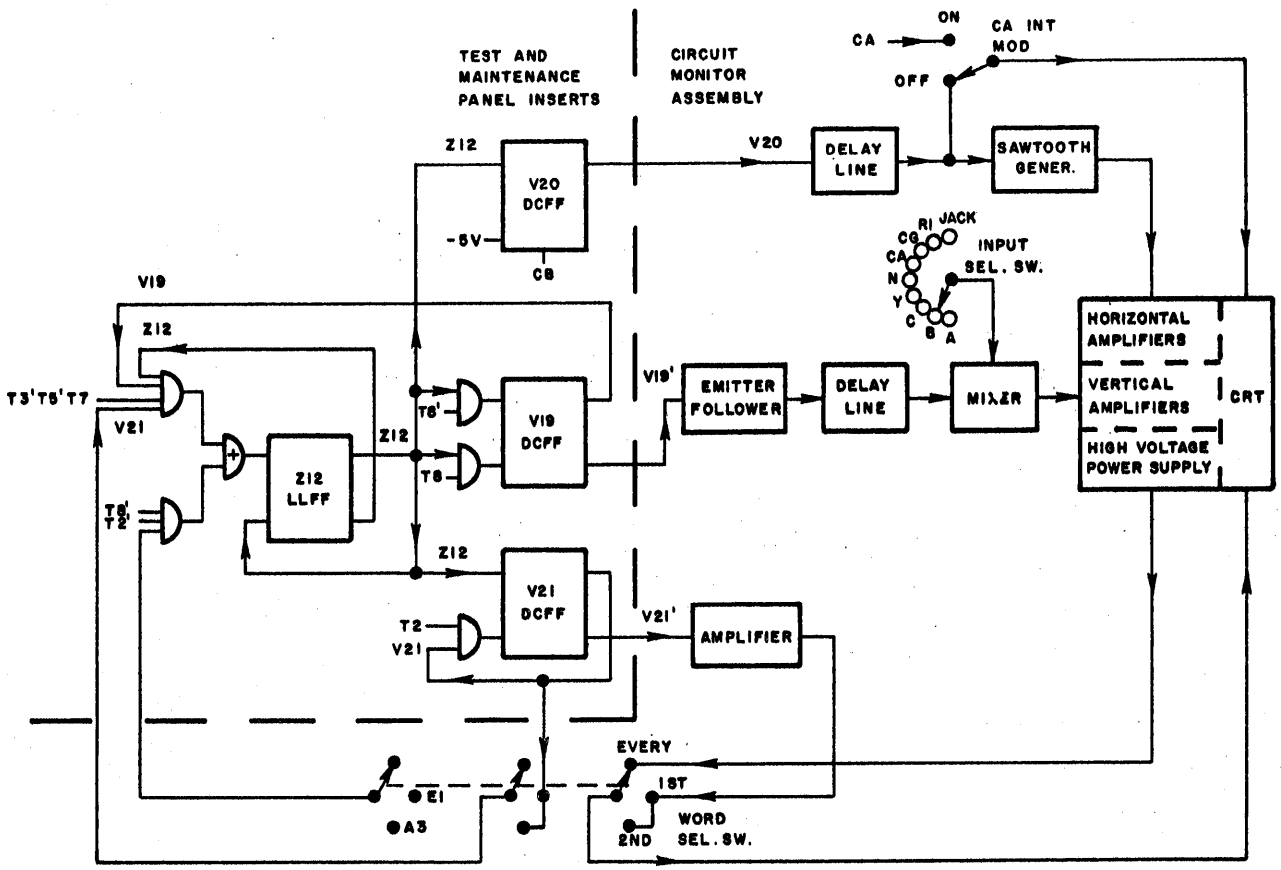


Figure 3-37. Circuit Monitor Display Functions, Block Diagram

the oscilloscope circuitry, preventing reflections from the delay line from triggering V19. The 1.5 microsecond delay line insures that the trace position is not changed until after the digit 10 and digit 20 displays. A resistive network mixes delay line output with signals from the input selector switch.

The circuitry generating the sawtooth waveforms is a modified bootstrap sweep circuit. Current from the -27 volt source charges a capacitor through the sawtooth limiter potentiometer and fixed series resistors, as long as no change in potential occurs at the collector of the input stage of the generator. Output of the stage is clamped by an emitter follower which has a zener diode from collector to ground. Linearity of the rising positive voltage at the emitter is insured by return of a zener diode from emitter to the charging current path, replacing the feedback capacitor generally used.

To retrace between the tenth and eleventh and between the twentieth and the first digits, the generator must be discharged rapidly. The signals representing digit times 10 and 20 are available at Z12 and are applied to another d-c

flip flop, V20. By introducing CA into one half of this flip flop and CB into the other half, the true output from a Z12 input is a negative-going 3.2 microsecond pulse falling at digit times 10 and 20. A delay line also is used between the trigger pulse and the sawtooth generator. The trigger pulse also is available for retrace blanking, applied through the CA INT MOD switch, when the oscilloscope is being used to observe waveforms.

The WORD selector switch implements the observation of next instruction pairs and of the operand. The logic setting Z12 is expanded to select either the first or second words of the instruction pair. To trigger the sweep only on the first word of a pair, after the EXECUTE button is depressed, the coincidence expressed as true output of the equality flip flop-see paragraph 3-3a(9)-which occurs after only one digit 19 per drum revolution, is included in the Z12 input logic by providing E1 at a contact on the WORD selector switch.

The change in display frequency from every word time to once every 128th word time severely reduces the display brilliance. Some compensation is provided by V21. Triggered on by Z12, at one digit 20 time each drum revolution, V21 is true at digit 20 time. But since this signal also resets the flip flop, V21 goes false until the next appearance of the E1 signal. Z12 is restricted to a true output at only one digit 10 time per drum revolution by including V21 as a term in the Z12j input logic. V21 is reset at the first digit 1 time following a true E1 by applying the true output of V21 and the digits 1-3 group signal to the V21k input. The change in level at V21' is coupled into an amplifier and appears at contacts on the WORD selector switch for transfer to the CRT cathode as intensification bias.

To display the second word of an instruction pair, while the EXECUTE button is depressed, an additional input term for Z12j is required. The gating on the A3 flip flop, in the Digital Output module, offers the desired selection. Logic for A3 is

A3j = State 1, Digit 19, EXECUTE, equality.

A3k = State 1, Digit 19.

Since the output of A3 is true in the next digit 19 after equality, the A3 term provides for the display of the second word of the pair.

Display of the operand is automatic after depression of the FETCH button, as described in paragraph 3-7c(1).

Source voltage (115 vac) is applied to the high voltage power supply in the oscilloscope assembly after the initial two-minute delay (when the Computer is powered) to avoid presentation of the non-sweeping beam. The source voltage is removed through an interlock in the lid, thus minimizing power dissipation when the display

is not under observation.

3-7d. STATE INDICATORS. A set of neon indicating lights, test jacks, and selector switches constitute the STATE INDICATORS feature provided on the Test and Maintenance panel of the RW-300.

NOTE

"State" here refers to the condition or signal on the "normal" output line of the flip flop to be examined.

The "normal" output line of each of the flip flops in the track, instruction, and state counters, and of the equality, overflow, carry, and digital holding flip flops are each wired to a terminal on the STATE SELECTOR switch, as shown in the simplified schematic of figure 3-38.

Since the output state of the flip flops represents a change in phase with respect to the reference flip flop, the neon indicator requires both Z1 output and the desired signal. The "and" gate, an amplifier terminated by a step-up transformer, a rectifier, and appropriate bias introduction comprise the neon driver circuit. The dynamic signal from the flip flop being sampled and the a-c signal from the reference flip flop are "anded". A true gate output drives the NPN transistor amplifier, producing an a-c signal across the secondary of the step up transformer. The signal is rectified, biased at -45 volts to insure neon firing, and presented to the neon indicator. Four such circuits are available on each of the two insert cards mounted in the holders on the Test and Maintenance panel assembly.

To display the output wave shape from any of the available flip flops, a patch cord can be connected from any of the test points, provided above the neon indicators, to the jack below the oscilloscope, with the scope INPUT switch in "jack" position.

The output of the reference flip flop can be checked by examining one of the available outputs and introducing alternately Z1 and Z1'. Failure of the neon indicators to reverse condition may indicate malfunction of the reference flip flop.

3-7e. DIGITAL INPUT SWITCHES. The set of switches labelled DIGITAL INPUTS are available to permit manual introduction of one-bit inputs on the lines normally used for Flexowriter inputs. The breakpoint switch interrupts the connections of the lines from the source into the Digital Input module. The individual toggle switches can then apply -5 volts to any of the lines.

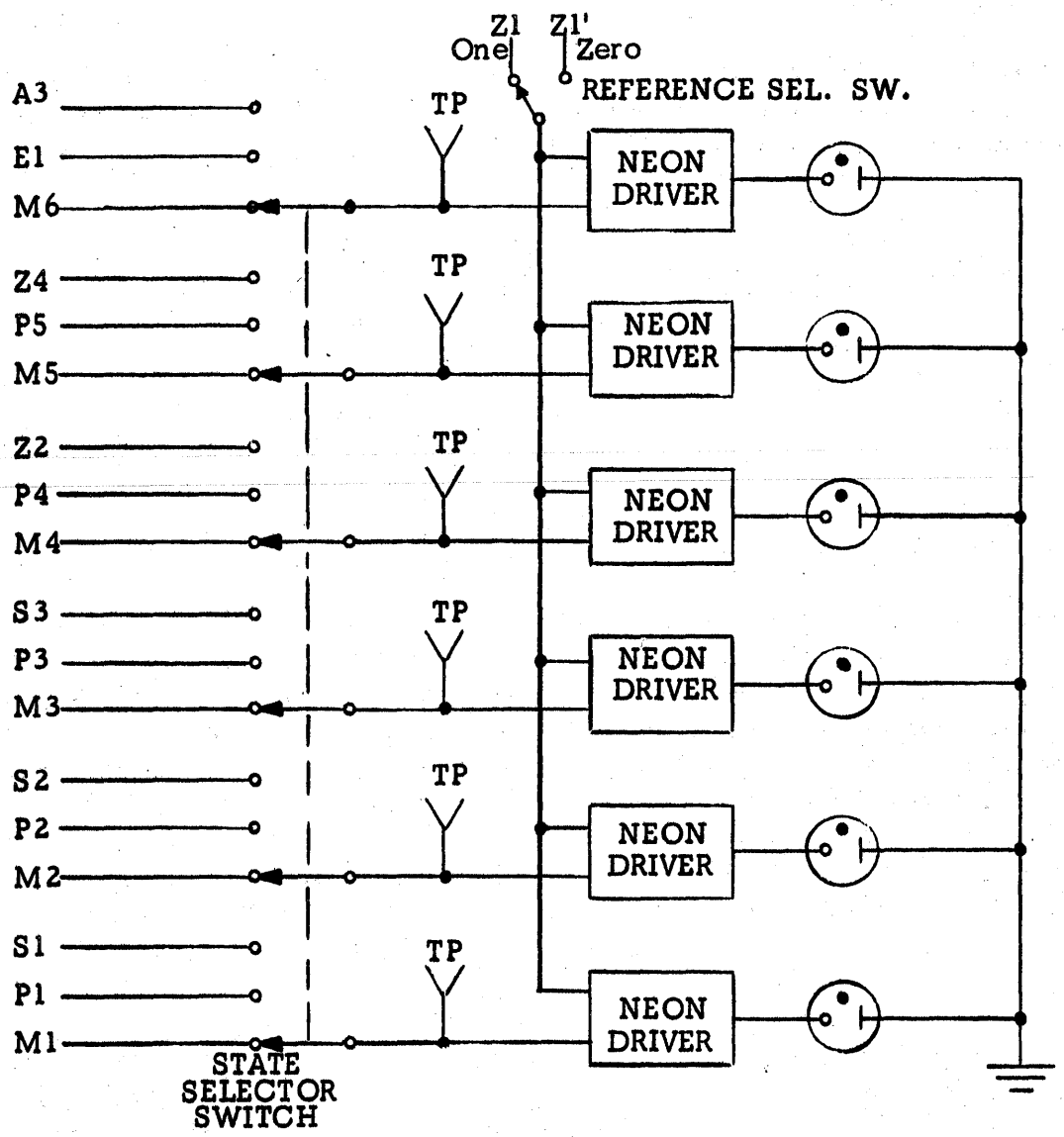


Figure 3-38. State Indicators, Simplified Schematic

3-7f. MARGINAL CHECKING. Marginal supply voltage conditions can be set up to isolate performance discrepancies and aid in preventive maintenance. Computer operation is examined through the use of a set of potentiometers, meters, and a metering selection switch on the Test and Maintenance panel.

Line voltage is continuously metered. Principal flip flop supply voltages can be metered and adjusted by means of the METER SELECTOR switch and appropriate control. Controls for clock signals are in series with the B supply to the output stage of the respective clock generator. Each of the supply voltage controls is in the regulating circuitry for the respective supply.

APPENDIX A

SYMBOLS AND DEFINITIONS

(A): Symbol for "the contents of the A register". Similarly, (B) means the contents of the B register; (m), the contents of the drum storage location; etc.

A1: The logical flip flop for the A register, mounted in insert position 18 on module 106. Input drive may be derived from output of the power amplifier associated with the A register read circuit, from the register lengthening flip flop, or from other Computer circuitry such as the adder. See paragraph 3-3a(5).

A2, A3: A2 is a delay flip flop in insert position 17 on the digital input module, whose output reflects sequential sampling of signals on 18 parallel digital input lines. The status of A3 (set by track address 32) determines whether or not digital input is to be obtained from the Flexowriter. A3 is also mounted in module 111, in insert position 18.

ACCUMULATOR: In the RW-300, the A register functions as the accumulator for arithmetic manipulations. During certain control functions, such as those in which a pseudo address is created, the Y register assumes a non-addressable accumulator feature.

ADDER: A circuit or device forming the sum of two quantities entered into it. A serial binary adder is used in the RW-300. In such an adder, the two binary numbers to be added are each applied, least significant digit first, to gating circuits. Output of one "and" gate drives the carry flip flop. If both input digits are 1's, the carry flip flop is driven to generate a 1 during the succeeding digit time. This carried digit is applied to a set of "and" gates simultaneously with the next higher order of input digits. The "and" gates drive an "or" gate, the output of which reflects the binary sum of the digits appearing at the adder input. Gating and amplification for the adder are provided on module 108. See paragraph 3-3a(8).

AL: A high level flip flop, mounted in insert position 17 of the A register module, used to lengthen the A register to 20 bits.

ANALOG: Representation of numerical quantities by physical rather than symbolic means. See paragraph 2-1 and paragraph 3-5.

"AND", "AND" GATES: The operator by which two binary statements (signals) are logically multiplied. The logical product of each possible combination of true and false statements (signals) is shown below. The logical "and" function is provided when a true statement (signal) is generated only by all true statements (signals). For example, assigning a value to "truth" and an alternate value to "falsity", a circuit is said to provide the "and" operator if and only if an output of the "true" value is produced by applying only

"true" input signals. Such circuits are called "and" gates.

First Statement	Second Statement	"And" Result
False	False	False
False	True	False
True	False	False
True	True	True

Input No. 1	Input No. 2	"And" Output
0	0	0
0	1	0
1	0	0
1	1	1

A REGISTER: Accumulator, principal arithmetic circulating register. Word length may be varied ± 1 bit for contents shifting. See paragraph 3-3a(5).

B: The logical flip flop for the B register, mounted in insert position 18 on module 107. Input drive may be derived from output of the B register read circuit, from the register lengthening flip flop, or from other Computer circuitry such as the adder. See paragraph 3-3a(6).

BASE: The radix in a scale of numerical notation. In the decimal system, the base or radix is 10; in the binary system, the base or radix is two; and, in the octal system, the base or radix is eight. The least significant digit in any number is the product of the digit and the base raised to the zero power. See paragraph 2-1a.

BINARY SYSTEM: A notation and computation system based on only two digits or conditions; i. e., 0 and 1, true and false, high and low, on and off, yes and no. In binary notation, the positions of the digits 0 and 1 in a number designate the power of two by which the individual digit is multiplied. See paragraph 2-1a. Binary digits are called bits.

BL: A high level flip flop, mounted in insert position 17 of the B register module, used to lengthen the B register to 20 bits.

B REGISTER: Second addressable circulating register. Word length may be varied ±1 bit for contents shifting. See paragraph 3-3a(6).

C: The logical flip flop for the C register, mounted in insert position 9 of module 114.

CARRY FLIP FLOP: Z4, a low level flip flop in insert position 7 on the adder module, provides the delay of the carried digit for binary computations in the RW-300. See paragraph 3-3a(8).

CG1 and CG2: Current gate diode circuits, used in A-D and D-A conversion are mounted on boards located in positions 11 and 13 respectively on the converter module.

CIRCULATING REGISTER: In the RW-300, a storage circuit continuously reading and recording the same data on a drum track for fast accessibility. Five one-word circulating registers and a 16-word circulating register are provided.

CL1 and CL2: Current gate input logic circuits, which drive the current gates, are provided on boards located in insert positions 15 and 16 on the converter module.

CLOCK PULSES (CA and CB): Basic timing pulses controlling the sampling and/or transfer of signals in a computer. In the RW-300, CA is the principal clock pulse. CB is a secondary clock pulse at the same amplitude, pulse width, and frequency as CA but occurring, in time, midway between each successive CA pulse. See paragraph 3-6.

COMMAND: The code to which a computer responds with a sequence of operations resulting in performance of an instruction recognized by the programmer. The RW-300 recognizes 19 individual instruction codes, some of which offer more than one option (i.e., code 00001 specifies any of three types of shift, each of which may be from 1 to 17 bits.

COMPLEMENT: In a whole made up of two parts, one part (X) is said to be the "complement" of the other (Y). In Boolean algebra, the complement may be symbolized by the use of a prime mark, or an overscore. Expressed symbolically: $X+Y = 1$, $Y = X'$, $X+X' = 1$. In a flip flop for which the symbol A is used, a true input on the set side produces a true output on the corresponding side and a false output on the alternate side. The side corresponding to the set input is called the normal output (A), while the alternate side is called the complement output (A'). Thus, complements are generated automatically in a flip flop. The complement side will be true when a true input is applied to the reset input of the flip flop but the symbols remain the same as in the first case. An arithmetic complement is formed either by subtracting each digit of the original from the base digit or by subtracting each digit from a digit one unit smaller than the base digit, adding a 1 in the least significant digit of the result and executing all carries.

COUNTER: Generally, a device or circuit which totals digital numbers or permits digital numbers to be increased by additions of one in any column of the number, and which can be reset to zero. Since this definition may extend to adder functions, in the RW-300 a counter is principally a set of flip flops storing a particular field of a machine word (as the instruction code bits), or a set of flip flops logically interconnected to count sequentially in binary or in a special coded binary, either automatically (the digit counter) or conditionally (the state counter).

C REGISTER: Non-addressable 20-bit circulating register used to store units

of information (word fields) during instruction execution. See paragraph 3-3a(10).

CURRENT WEIGHTER RESISTORS: A board mounted in position 12 on module 411 bears the precision resistors necessary for the current weighting technique used in the analog input/output group for conversion.

d1.....d20: Digit times 1 through 20 constitute a sector time in the RW-300. Digit times are generated and remain synchronized through operation of the digit counter described in paragraph 3-3a(1). d1 is the least significant bit of a sector. d19 and d20 are space bit times, during which Computer operations accomplish any required changes.

DA1 and 2: Detector amplifier 1 and 2, accepting error signals during analog to digital conversion and digital to analog conversion.

DA3: Detector amplifier used to amplify error signals during analog to digital conversion.

DA4: Detector amplifier used to amplify error signals during digital to analog conversion. Output drives a power amplifier.

D1, D2 and D3: Delay generators triggered by various digital output commands. The true output on the complement side, existing when no delay is in force, constitutes a term in gating permitting advance of the Computer in digital communication commands. Conversely, true output on the normal side, generated during the delay period, inhibits Computer advance.

DELAY FLIP FLOP: A dynamic flip flop, in the RW-300, which requires only a j-input and which generates a k-input by means of an inverter stage. See figure 2-15.

DELAY GENERATOR: See D1, D2 and D3.

DETECTOR AMPLIFIER: A circuit used in analog to digital or digital to analog conversion, to amplify an error signal. See paragraph 3-5b(4). Output voltage is proportional to net input current.

DIGIT: A symbol in a numbering system. The decimal system employs 10 different digits (0 to 9) while the binary system employs only two different digits (0 and 1).

DIGIT COUNTERS: The RW-300 is equipped with separate digit counters for arithmetic/control and analog input/output functions. See T1...T9 and T10...T14. Once these groups of flip flops are synchronized with the drum, by means of the sector number track, they step sequentially through each pertinent digit

time or digit time group.

DRUM: The central storage device in the RW-300 consisting of a rotating cylinder whose surface is coated with magnetic material responding to the variation in magnetic field created as recording current passes through the head(s). See paragraph 3-2a.

E1: The low level flip flop, mounted in insert position 3 on module 110, which indicates achievement of equality during searches for next instruction, operand, and pseudo addresses. Also used to indicate readiness of external equipment in commands for communication with digital equipment.

END-AROUND CARRY: The digit added in the least significant place to correct the result when performing a subtraction by adding the 9's complement of the subtrahend to the minuend, or when performing an addition by adding the 9's complement of the negative number to the positive number.

EXECUTE BUTTON: A switch and light assembly on the Test and Maintenance panel which actuates an interruption of program execution, placing the Computer in an idling mode to facilitate inspection of the next instruction pair of track sectors. See paragraph 3-7c(1).

F1...F7: A set of d-c flip flops comprising the sector counter which synchronizes operation of the analog input/output group with the arithmetic and control group. F1 is least significant. F1 through F7 are mounted in insert positions 1, 2, 4, 5, 7, 8, and 10, respectively, of timing module no. 1.

f_a and f_a*; f_b and f_b*; f_{63} and f_{63}*: f_a is an a-c signal produced in response to the source (A register) of a signal to be stored. f_a* is a signal made up of the individual complements of the signals comprising f_a. Using f_a and f_a* in combination with Z1 and Z1', a d-c control signal, called DCA is generated and is used to control transfer of the contents of the A register into the writing circuits, during a store A instruction. Similarly, f_b and f_b* are employed in a store B instruction. Generated and used in the same manner, f_{63} and f_{63}* permit recording of (A) or (B) into the 16-word circulating register (track 62). See paragraph 3-2c.

FALSE SIGNALS: See TRUE SIGNALS.

FETCH BUTTON: A switch and light assembly on the Test and Maintenance panel which actuates interruption of program execution, placing the Computer in an idling mode to facilitate inspection of the operand. See paragraph 3-7c(1).

FIELD: A set of digits, not necessarily the same in all instructions, used as a group to constitute a unit of information. For example, the instruction

code field comprises bits 14 through 18 of the second word of an instruction pair in the RW-300.

FIRST REVOLUTION: A reference period used in analog to digital conversion in the RW-300; the period during which input relays are being selected and X10=X11=X12=X13=0.

FIRST WORD: A reference period used in analog to digital conversion in the RW-300; the period during which the conversion begins.
Also, in an instruction pair, the Computer stores the first word as the operand address and execution time of the instruction.

FLIP FLOP: A bi-stable multivibrator circuit having two inputs and two outputs. Inputs consisting of one true signal and one false signal generate a true signal on the output corresponding to the true input, and a false signal on the output corresponding to the false input. Inputs are usually accepted, and outputs are usually sampled, with reference to a timing (clock) pulse. The output sampled during a given clock pulse was generated as the result of inputs accepted during the previous pulse. Hence, a flip flop inherently introduces a delay equivalent to the period from the start of one clock pulse and the start of the next pulse. A flip flop set by a true signal on one input remains set until a true signal is applied to the alternate input and is therefore useful for one-bit storage. True signals applied to both inputs produce ambiguous results. The RW-300 utilizes both d-c and a-c (called dynamic) flip flops. See paragraph 2-2b and 3-4c(1).

FLIP FLOP NO. 2: A modified Eccles-Jordan d-c flip flop, used in the RW-300, producing 0 volts output from a false input and -13.5 volts output from a true input. See paragraph 3-4c(1).

GATE: A circuit accepting two or more inputs and producing a single output (during a timing or sampling pulse) based on "and" and/or "or" logic. See paragraph 2-1b.

H1....H10: The converter register in the analog input/output group. Since analog data is converted to 10-bit words, the register is composed of 10 d-c flip flops. Each flip flop is set by the current weighting network. At the completion of the conversion, the status of each flip flop is shifted sequentially into a sector on one of the analog input tracks on the drum. The flip flops of the converter register are mounted on module 412.

H11: A low level dynamic flip flop, H11 is mounted in position 11 on the analog write module (415) and is used to convert the d-c signals stored in the converter register (H1 through H10) into a-c signals for recording on the drum surface.

HEAD: Electromagnetic device, mounted within 0.001-inch of the surface of the magnetic drum which, when driven by recording current, records the datum as a variation in magnetic flux, and which senses such variations in flux to reproduce the excitation pattern. See paragraph 3-2a(1).

INPUT AMPLIFIER: An impedance matching amplifier from the RW-300 analog input gating into the detector amplifier DA1 and 2, for analog to digital conversion.

INSTRUCTION: In addition to the instruction code, an instruction for the RW-300 specifies the operand address, instruction execution time, and next instruction address. See paragraph 3-3a(3) and 3-3b(2).

J1, J2: Matrix amplifiers J1 and J2 are used to generate the RECORD ERROR signal when an attempt is made to record into any track (except track 62) other than one of the eight to which the Track Selector plug is connected. J1 is mounted in insert position 16 of module 104, while J2 is in position 8 on module 109. See paragraph 3-3a(4).

J6, J7, and J8: Matrix amplifiers, mounted in positions 8 and 9 on module 109, accept the digits to be added in the serial binary adder. See paragraph 3-3a(8). Such amplifiers respond without delay to input signals. Output of J8 is stored either in a register or in a general storage track as the sum of the quantities entered into it. J6 and J7 drive the carry flip flop, whose output is also applied to J8 after the desired one digit delay.

J9: Matrix amplifier, mounted in insert position 2 of module 110, accepting the output of either the sector number read circuit or the "store" sector number read circuit, and generating the signal permitting storage, based on appearance of the sector into which the digits should be recorded under the write head. See paragraph 3-3a(9).

LAST REVOLUTION: A reference period used in analog to digital conversion in the RW-300; the period during which all conversions are completed and X10=X11=X12=X13= 1.

LOAD BUTTON: A switch and light assembly on the Control panel which actuates the Computer to begin program loading. Track 63 bears the loading routine and the LOAD button transfers the Computer into sector 0 of track 63.

LOGIC. The mathematical or logical relationships which must be implemented by circuitry to perform the logical operations of comparing, sorting, selecting, merging, matching, etc. The logic of a circuit is described by a symbolic expression of the input terms and their interrelationships necessary to produce a true output from that circuit. See

logic descriptions for each of the RW-300 circuits, listed in the List of Illustrations. Also refer to "AND", "AND" GATES and "OR", "OR" GATES. Since various combinations of "and" and/or "or" gating are required, in the RW-300, the insert cards bearing the diodes and resistors forming the necessary gates are called "logic" cards and are further identified by decimal numbers.

M1...M6: A set of six multi-purpose high and low level flip flops used primarily as a track number register, in the arithmetic and control group. See also paragraph 3-3a(4).

MD1...MD6 and MD1'...MD6': A set of 12 high level d-c converters driven by track register flip flops M1 through M6, in conjunction with output of the reference flip flop Z1, to produce gating signals for the read head selection unit. The configuration of the a-c outputs of M1 through M6 is converted to comparable d-c biases which permit the output of the head reading the selected track to be transferred into the general storage read circuit, R1. MD4 through MD6 and MD4' through MD6' are used to select one of eight tracks (to which the track selector plug provides a connection) on which information is to be recorded during store A or store B instructions. MD1, MD1', MD2, and MD2' are on module 104; the remainder on module 105; four converters sharing one insert card.

MODULE: In the RW-300, individual circuits are assembled and wired on insert cards. Interconnection between circuits and physical mounting for cards are provided by modules. See paragraph 1-2a(2).

N: The logical flip flop for the N (next instruction) register, mounted in insert position 18 of module 108.

N REGISTER: Non-addressable 20-bit circulating register which stores the next instruction address in the RW-300. See paragraph 3-3a(7).

OPERAND: Any of the quantities entering into or arising from an operation.

"OR", "OR" GATES: The operator by which two binary statements (signals) are logically added. The logical (not arithmetic) sum of each possible combination of true and false statements (signals) is shown below. The logical "or" function is provided when a true statement (signal) is generated by any true statement (signal) in a combination of two or more statements (signals). For example, assigning a value of 1 to "truth" and 0 to "falsity", a circuit is said to provide the "or" operator if an output of the "true" value is produced by applying one or more "true" input signals. Such circuits are called "or" gates.

First Statement	Second Statement	"Or" Result
False	False	False
False	True	True
True	False	True
True	True	True

Input No. 1	Input No. 2	"Or" Output
0	0	0
0	1	1
1	0	1
1	1	1

P1...P5: A set of five high and low level flip flops, located on module 103 in the arithmetic and control group, used to store the digits of the instruction code.

PA01, PA07 and 8, PA11...18: Power amplifier whose input logic establishes the extended word time for an analog to digital conversion. PA01 is wired on one half of an insert card in position 11 of timing module no. 1. The remaining half of the card bears a spare power amplifier, PA02, PA07 and 8, and PA11 through PA18 are mounted on module 417, available for use depending upon the input system used.

PG064...PG086; PG088...PG110; and, PG112...PG126 and PG000...PG006 (Even numbers only): Analog output power gates, each associated with a voltage gate, mounted in output modules. Twelve sets are mounted in each output module. The number of modules used depends upon system requirements.

PG301 and PG302: Circuits furnishing an analog voltage memory. Output voltage range is 0 to +15 volts; holding time one-thirtieth second maximum. Each is associated with a voltage gate, which can be used in the stabilizing loop. Power or voltage gate outputs effect analog control of external devices. PG301 and PG302 are mounted in positions 6 and 5, respectively, on the converter module.

PI01: Power inverter which provides sector comparison for analog to digital conversion. This inverter occupies one half of the insert card (PI02 occupying the remaining half) mounted in insert position 12 on timing module no. 2.

PI03: Power inverter which turns off all current switches in the converter, in the analog input/output group. PI03 shares position 17 on module 411 with PI04.

PI04: Power inverter which in conjunction with PI03 can turn on all current switches in the converter, in the analog input/output group. PI04 occupies one half of the insert card in position 17 on the converter module.

PI08...PI15: Power inverters. The number used depends upon the number of tracks on which converted analog data is to be recorded. Each power inverter drives a write circuit wired to a head on the drum surface. Power inverters and associated write circuits are mounted in the analog write module.

Q1...Q88: The logical symbols for each of the reading heads in the RW-300 Q1 through Q62 read from general storage tracks 0 through 61; Q63 reads from the 16-word circulating register (track 62); Q64 reads from the program loading routine track (track 63); Q65 reads from the clock pulse track; Q66 reads from the sector number track; Q67 also reads from the sector number track but 32 sectors ahead of Q66, in the direction of drum travel; Q69 reads from the Y register, Q70 from the N register, Q71 from the C register, Q72 from the A register, and Q73 from the B register. Q88 reads from track 7 but presents its signal to the analog input/output group for conversion from digital to analog form.

Q201...Q209: The logical symbols for each of the writing heads in the RW-300. Q201 through Q208 record into general storage tracks 0 through 7. Each is a separate, single head unit mounted 32 sectors ahead of the reading head in the direction of drum travel. Q209 is a single unit recording signals converted, by the analog input/output group, from analog to digital form onto track 8. An expanded system may include a write head on tracks 9 through 13. Q269 through Q273 are individual recording heads mounted in dual-unit packages and recording on Y, N, C, A, and B circulating registers, respectively. Each is separated from its reading head by 19 or 20 bits. Q263 is a single head mounted 16 sectors behind its reading head on the 16-word circulating register (track 62).

R1: General storage read circuit, accepting output of the read head selection unit for amplification and shaping, mounted in position 5 on module 114.

R63: Read circuit, in position 4 on module 114, for the 16-word circulating register (track 62).

R65: Read circuit, in position 5 on module 114, for the clock pulse track.

R66: Read circuit (insert position 3 in C register module) accepting directly signals from Q66 on sector number track. Circuit output is used by digit counters in arithmetic/control group and in analog input/output group for synchronization.

R66D: Read amplifier converter in analog input/output group. A-C signals from sector number read circuit, R66, are converted to d-c signals at levels required by the flip flops in the analog group digit counter. The circuit occupies one half of an insert card in position 20 on timing module no. 1.

R67: In position 2 on module 114, the read circuit for Q67 provides the signal used to identify the sector into which information from A and B registers is to be recorded during store A and store B instructions, in tracks provided with separate recording heads (usually tracks 0 through 7).

R69...R73: Read circuits for Y, N, C, A, and B registers, each mounted in the appropriate module.

R88: Read circuit (insert position 1 on C register module) accepting directly the data recorded on track 7 by the arithmetic/control group for conversion by analog group.

R88D: Read amplifier converter in analog input/output group. A-C signals from track 7 analog read circuit, R88, are converted to d-c signals at levels required by the flip flops in the analog group converter register. The circuit occupies one half of an insert card in position 20 of timing module no. 1.

RD1...RD3: Relay drivers sharing insert position 15 on module 114. RD1 drives a relay applying power to a Flexowriter used for digital communication.

REFERENCE SUPPLY: A precision voltage source, at 256.6 volts, for use as a standard for the current switches in the analog input/output group.

REGISTER: Mechanisms and/or circuitry for storing one machine word. In the RW-300, five one-word circulating registers are included. Three (N, Y, and C registers) are fixed length storage. The word length handled by the remaining two (A and B registers) may be varied between 19 and 21 bits to accommodate shifting.

RESUME BUTTON: A switch assembly on the Control panel which actuates restoration of automatic program execution following an interruption resulting from an attempt to record into an "illegal" address.

RUN BUTTON: A switch assembly on the Test and Maintenance panel which actuates restoration of automatic program execution following interruption by either fetch or execute operations. See paragraph 3-7c(1).

S1...S3: A set of three high level flip flops in module 102 comprising the state counter in the RW-300 arithmetic and control group. Outputs of the state counter flip flops are recognized as gross timing signals in the execution of instructions. Instruction execution generates signal conditions controlling input to the state counter flip flops.

SECOND WORD: A reference period used in A-D conversion in the RW-300. The period during which the conversion is completed and the converted word is shifted to the drum. Also, in an instruction pair, the Computer stores the second word as the next instruction address and the instruction

code for the current instruction.

SECTOR: A unit of length on the recording tracks on the RW-300 drum. Track length is divided into 128 sectors. Two successive sectors are used in an instruction pair. A single sector stores a 17-bit data word plus sign.

SECTOR COUNTER: A set of d-c flip flops controlling timing of A-D conversions in the analog input/output group. See paragraph 3-5b(2).

SHIFT: A machine operation equivalent to multiplying or dividing by a power of the base of notation. In a binary computer such as the RW-300, a single digit right shift effectively multiplies the word by 2^1. A single digit left shift effectively divides the word by 2^1. Shifting occurs automatically in arithmetic manipulations where necessary and may be accomplished under programming control through the shift instruction (code 00001) in the RW-300. See paragraph 3-3b(13).

START BUTTON: A switch and light assembly on the Control panel which actuates the Computer to begin automatic program execution at sector 0 of track 0.

STATE: In the RW-300, a state is a unit of gross timing in the execution of an instruction. See paragraph 3-3b(1). Also, a flip flop is said to be in a true or false state when the output signal on the normal side is true or false, respectively.

STOP BUTTON: A switch and light assembly on the Control panel which actuates interruption of automatic program execution and transfers the Computer to an idling mode.

STORAGE: Retention of data and instructions by the Computer, on a temporary or long time basis. Temporary storage may be considered that provided by flip flops and registers. Long time storage is a capacity of a magnetic drum.

SYMBOLIC LOGIC: A formal logic using symbols for non-numerical relationships in order to express such relationships conveniently for analysis. The branch of symbolic logic known as Boolean algebra is employed in the logical design of computing circuits.

T1...T9: A set of nine high and low level flip flops, on module 101, comprising the digit time counter for synchronization in the arithmetic and control group. A special binary code is used to identify pertinent digit times and digit time groups such that only one of the nine flip flops changes state to effect each change in the counting sequence.

T10...T14: A set of five d-c flip flops comprising the digit time counter for the analog input/output group. They are located on timing module no. 1 in

positions 18, 17, 15, 14, and 13, respectively. A conventional binary representation for each digit time is assumed by the five flip flops.

TRACK: A strip on the circumference of the magnetic drum, which is identified with respect to the recording and/or reading heads with which it is associated and which may bear a recorded pattern corresponding to a serial representation of data and/or instructions. See paragraph 3-2a(2).

TRUE SIGNALS: In a system of binary operation, true signals are one of the two possible classes of signals used. True signals are those recognized as having a binary value of 1, as opposed to false signals which are those recognized as having a binary value of 0. The level of a true signal (or binary 1) in the RW-300 is normally no more positive than -2.5 volts. Signals more positive than -2.5 volts are recognized as false (or binary 0's). In the RW-300, a true signal is symbolized by the alphabetic and/or numerical symbols representing the circuit which generated the signal. However, see also COMPLEMENT.

V1...V18: D-c flip flops in module 112 which act as a serial input, parallel output buffer register communicating with external digital output equipment.

V19: A d-c flip flop in the Test and Maintenance panel assembly generating vertical bias for the two-baseline oscilloscope display. See paragraph 3-7c(2).

V20: A d-c flip flop, in the Test and Maintenance panel assembly, generating the trigger signal for the saw-tooth generator in the circuit monitor.

V21: A d-c flip flop in the Test and Maintenance panel assembly controlling the amplifier providing additional display brilliance during circuit monitoring of only one sector during each drum revolution.

VG064...VG086; VG088...VG110; and, VG112...VG126 and VG000...VG006 (Even numbers only): Analog output voltage gates, each associated with a power gate, mounted in the output modules. Twelve sets are mounted in each output module. The number of modules used depends upon system requirements.

VG200...VG231: Voltage gates accepting analog inputs in the analog input/output group. The voltage gates employed are mounted on module 416. The position of individual gates depends upon the system used.

VG301: Voltage gate used to ground the common line for analog inputs, to stabilize against circuit drift, in analog to digital conversion. VG301 occupies one half of an insert card in position 4 on the converter module.

VG302: Voltage gate, in the analog input/output group, presenting an external reference voltage to the reference supply in cases where such an external reference is used. The voltage gate is wired on one half of an insert card in position 4 of the converter module.

VG400...VG403: Spare voltage gates in insert positions 1 and 2 of the converter module for the analog input/output group. Unused in RW-300.

W1...W8: A set of eight write circuits to which the data to be stored on the drum are presented by the arithmetic and control group. Track selection signals from MD4 through MD6 and MD4' through MD6' control transfer of the signal into the desired track. Write circuits are mounted, two per insert card, in module 113.

W63: Write circuit in insert position 12 on module 113, driving the 16-word circulating register.

W69...W73: Write circuits for Y, N, C, A and B registers, each mounted in the appropriate module.

W88: Write circuit sharing insert position 12 on module 113, accepting digital signals generated by the analog input/output group and driving the recording head on track 8, also under analog group circuit control.

WC1...WC16, WC88: Write Control circuits, mounted four per board in module 113, which may be connected either as conventional amplifiers (inverting the signal) or as emitter followers to generate desired gating signals. See paragraph 3-2c.

WRITE CIRCUIT: Current and voltage amplifier producing power amplified sine wave output either for recording on drum tracks or to provide loading capability for widely used signals in arithmetic and control group. Both input and output may be used either single-ended or push-pull. See figure 2-14.

X1...X5: A set of five d-c flip flops comprising the relay selection counter in the analog input/output group. Each combination of states of the flip flops in the counter addresses one set of input relays. Flip flop insert cards for the relay selection counter occupy insert positions 1 through 3, 5, and 6 on module 414.

X6: Relay gate control flip flop in insert position 8 of module 414. This d-c flip flop prevents closure of more than one relay of a set at any one time in an A-D conversion.

X7: The sector compare flip flop in the analog input/output group. A true output from X7 permits conversion of an analog input to digital data. X7 remains

true from the first word time until d6 of the second word time. It is mounted in insert position 19 on timing module no. 2.

X8: The write control flip flop in the analog input/output group. X8 is true during the second word of an A-D conversion and permits recording of converter register contents onto the drum. It is mounted in insert position 20 on timing module no. 2.

X10...X13: A set of d-c flip flops, mounted in positions 13 through 17 of timing module no. 2 in the analog input/output group, comprising the revolution counter, which establishes the delay in which input voltages settle prior to sampling for A-D conversion.

Y REGISTER: Non-addressable 20-bit circulating register which stores the operand address and, in the execution of certain instructions, a pseudo address which determines completion of the arithmetic or control operation. See paragraph 3-3a(7).

Z1: High level flip flop in insert position 20 on module 101, which is set to the digit 1 by the first 1 read from the sector number track after the Computer is actuated. This flip flop remains in the true state as a reference and is combined with track number digits to generate d-c gating signals.

Z2: Mounted in position 6 on module 110, Z2 is set by a carry out of the most significant digit in certain instructions as an indication that overflow has occurred. It is reset by a transfer on overflow instruction.

Z4: The carry flip flop, Z4, is located on module 109 in position 7 and is driven, through gating, by the true outputs of J6 and J7. See paragraph 3-3a(8) and ADDER.

Z6...Z8: Signals identifying the jack into which the track selector plug is connected. These signals are compared to the most significant digits of the track address, and information appearing at the write circuit is transferred to the recording head if the plug position identification matches the track selection signals. Failure of the signals to match illuminates the RECORD ERROR light and transfers the Computer to an idling mode.

Z12: A low level flip flop mounted in the Test and Maintenance panel assembly, Z12 generates a d10 identification signal by delaying digit time group 9-13 and eliminating all but digit time 10, which is used in the circuit monitor display. See paragraph 3-7c(2).

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