TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 990 Computer

16 Input/16 Output TTL Data Module
Depot Maintenance Manual

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PREFACE

This manual provides maintenance instructions for the Texas Instruments 16 Input/16 Output TTL Data Module. The manual also provides the theory of operation for the module. The information in the manual is divided into the following sections:

I. General Description – This section briefly describes the module, including its operation and characteristics.

II. Installation – This section provides instructions for unpacking, inspecting, and installing the module into a Model 990 Computer mainframe or expansion chassis.

III. Operating Instructions – This section provides programming instructions for the module and a description of how the software controls the operation of the module.

IV. Theory of Operation – This section contains detailed block diagrams of the data module, describes the module's interfaces with the Model 990 Computer and a peripheral device, and provides a discussion of the module's operation.

V. Maintenance – This section provides troubleshooting and fault isolation procedures for the module.

Alphabetical Index – The alphabetical index provides an alphabetical listing of key words and concepts within the manual and locates them for easy reference.

Additional information related to the 16 Input/16 Output TTL Data Module may be found in the following documents:

Title	Part Number
990 Computer Family Systems Handbook	945250-9701
Model 990/4 Computer System Hardware Reference Manual	945251-9701
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990 Computer Family Maintenance Drawings	945421-9701 and 945421-9702

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SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

The 16 Input/16 Output TTL Data Module (see figure 1-1) provides a two-way communication path between a Texas Instruments 990 Computer and attached peripheral devices which are operated by or which generate TTL level digital signals. The module may be used in any Communications Register Unit (CRU) port within the CPU chassis, or it may be used in a CRU expansion chassis.

The module provides 16 input and 16 output lines. Each line may be addressed as a single independent binary value or as a member of a group of from 2 to 16 lines. Alternate versions of the module provide 15 normal inputs, 14 normal outputs, an interrupt line, and an interrupt mask. Data module inputs and outputs are negative logic levels that switch between 0 volts and a positive voltage level. Each output is an open collector transistor capable of sinking up to 50 milliamperes at up to 30 volts. Pads are available on the module for installing pull-up resistors or resistor divider networks at each output of the module. Each input is connected to the base of an emitter-follower transistor that operates at TTL levels. Pads for input filter capacitors are also available on the module.

Use of the data module in a simplified control system is shown in figure 1-2. In this example, the computer and the data module combine to sense the level of fluid in a storage tank and to control the operation of an input valve to maintain the fluid level between two prescribed reference levels. When the fluid reaches one of the prescribed references, an interrupt and an

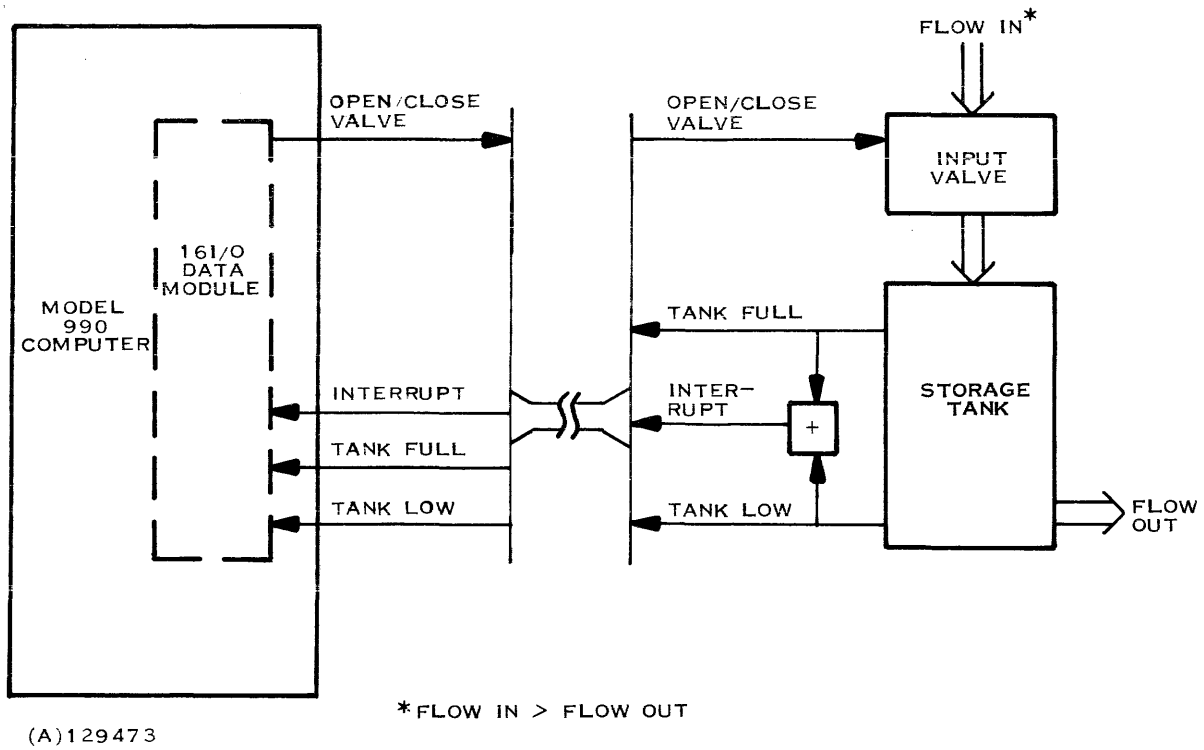


Figure 1-2. Simplified Control System Example

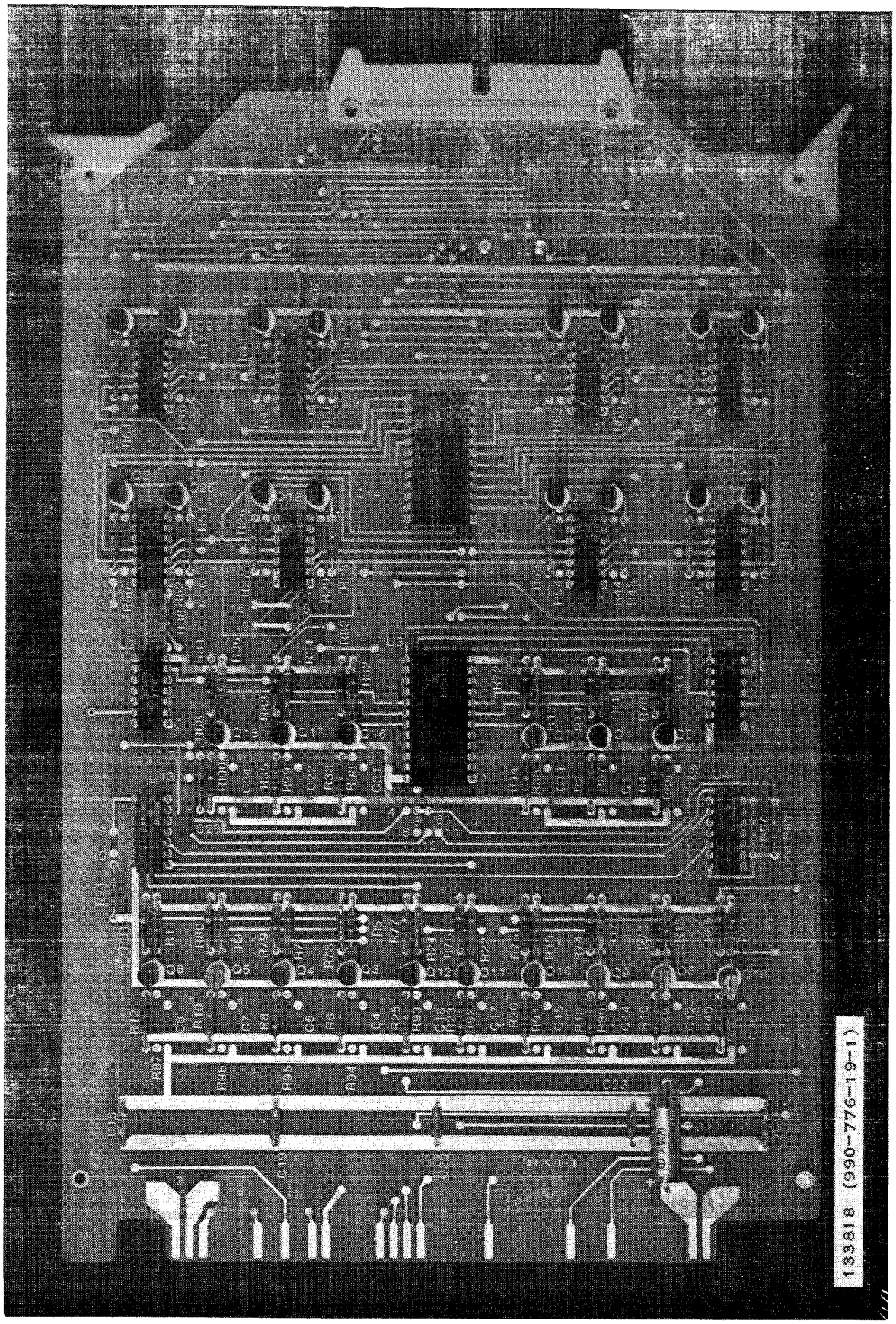


Figure 1-1. 16 Input/16 Output TTL Data Module

indication of which condition (tank low or tank full) caused the interrupt are generated. The service routine handling the storage tank system then uses the input data to develop a control signal that either opens or closes the input valve to rectify the situation.

1.2 EQUIPMENT OVERVIEW

Refer to figure 1-3 for a simplified diagram of the data module. The module contains 16 flip-flops that are used to hold the data supplied by the CPU and destined for some attached device. In the send mode, the CPU supplies output data, a write clock signal, an address that specifies one of the 16 flip-flops, and a module enable signal. All of these controls act to set or clear the selected flip-flop to establish an interface with the attached device. In the receive mode, the CPU provides a select address and a module enable signal to read one of 16 input lines.

The 990 Computer instruction repertoire includes single (SBO, SBZ, and TB) and multiple (STCR and LDCR) bit instructions that exercise the data module in both the send and receive modes. The SBO and SBZ instructions set and clear, respectively, the addressed flip-flop; the TB instruction tests the addressed input line. The LDCR instruction uses address increment logic to load from 1 to 16 of the flip-flops with serial data from the CPU. The STCR instruction uses the address increment logic to store data from 1 to 16 of the input lines in contiguous memory locations.

When the module is wired to report interrupts, 2 of the 16 flip-flops are used to store the interrupt itself and an interrupt mask. When the attached device generates an interrupt, it is recorded in the interrupt flip-flop and the interrupt mask, controlled by the CPU, either enables or disables the transfer of the interrupt to the CPU.

1.2.1 TRANSMIT MODE. In the transmit mode, the CPU supplies an address (CRUBIT12-15) that specifies 1 of the 16 flip-flops, the module enable signal (IMODSELA–), a write clock signal (STORECLK–), and the data bit (CRUBITOUT–). When IMODSELA– and STORECLK– are both TRUE (logic 0), the address decoder uses the address to select one of the 16 flip-flops and the data bit is gated into it, through an open-collector driver, and out on the selected line. See figure 1-3 for the output logic.

1.2.2 RECEIVE MODE. In the receive mode, the CPU supplies the line address (CRUBIT12-15) and the module enable signal (IMODSELA–). The line address is decoded by the multiplexer and, when IMODSELA– is true (logic 0), the input bit is gated through an emitter-follower transistor on the selected line, inverted three times and submitted to the CPU as CRUBITIN–. See figure 1-3 for the input logic.

1.2.3 INTERRUPT RESPONSE. Interrupt handling is selected by wiring the jumper options as shown in Section II. Both types of interrupts (low-to-high and high-to-low) provide 15 normal input lines, 14 normal output lines, an interrupt line, and an interrupt mask. When an interrupt occurs, it is input on line IN15–. The signal is inverted either once or twice (depending upon the type of interrupt the module is wired for), submitted to a differentiating network, and clears the interrupt flip-flop. If interrupts are enabled by the CPU (determined by the interrupt mask), the interrupt is inverted three times and submitted to the CPU as a low signal. See figure 1-3 for the interrupt logic.

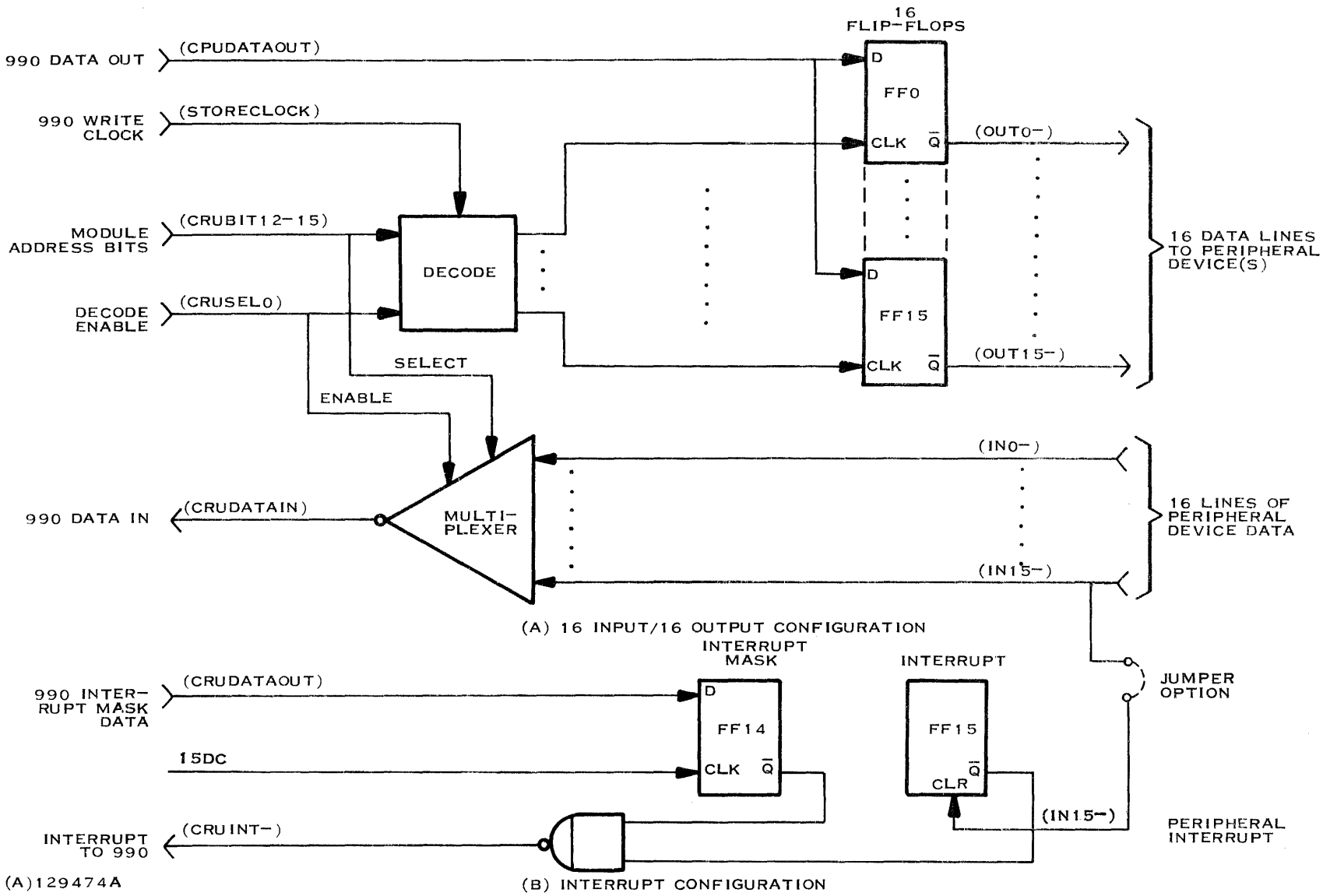


Figure 1-3. Simplified 16 Input/16 Output Data Module Diagram

1.3 PHYSICAL CHARACTERISTICS

The 16 Input/16 Output TTL Data Module is implemented on a double-edge, half-size printed circuit board that can be inserted into any CRU slot of any Model 990 Computer chassis or CRU expansion chassis. It is a double-sided board that measures 7.00 inches by 10.80 inches high, as oriented in figure 1-1. The board is made to be inserted into an 80 contact printed circuit board slot connector located in the backpanel of the chassis (see table 1-1 for the pin assignments). The generalized TTL interface is supplied to external devices through a 40-pin flat cable connector on the rear of the card. The pin assignments for this connector are shown in table 1-2.

1.4 ELECTRICAL CHARACTERISTICS

Table 1-3 lists the logic levels and electrical requirements for the 16 Input/16 Output TTL Data Module.

1.5 MODULE ADDRESS

The location of the module within the computer chassis (or expansion chassis) determines the CRU base address that the module recognizes. Therefore, before selecting a chassis location, determine the address that the software handling routine expects the module to recognize.

Table 1-1. CRU Interface Pin Assignment

Pin Number	Signal Name
P1-14	TLIORES
P1-18	CRUBITOUT
P1-22	STORECLK
P1-32	CRUBIT13
P1-34	CRUBIT15
P1-36	CRUBIT12
P1-38	CRUBIT14
P1-48	IMODSELA
P1-60	CRUBITIN
P1-66	INTERRUPTA
P1-1,2,24,79,80	GROUND
P1-3,4,77,78	+5 Volts

Table 1-2. External Connector Pin Assignment

Pin Number	Signal Name
P2-2	OUT0–
P2-3	OUT1–
P2-4	OUT2–
P2-5	OUT3–
P2-6	OUT4–
P2-7	OUT5–
P2-8	OUT6–

Table 1-2. External Connector Pin Assignment (Continued)

Pin Number	Signal Name
P2-9	OUT7–
P2-10	OUT8–
P2-11	OUT9–
P2-12	OUT10–
P2-13	OUT11–
P2-14	OUT12–
P2-15	OUT13–
P2-16	OUT14–
P2-17	OUT15–
P2-24	IN15–
P2-25	IN14–
P2-26	IN13–
P2-27	IN12–
P2-28	IN11–
P2-29	IN10–
P2-30	IN9–
P2-31	IN8–
P2-32	IN7–
P2-33	IN6–
P2-34	IN5–
P2-35	IN4–
P2-36	IN3–
P2-37	IN2–
P2-38	IN1–
P2-39	IN0–
P2-1,20,21,40	GROUND
P2-19,22	+5 Volts

Table 1-3. 16 I/O TTL Data Module Electrical Characteristics

Specification	Requirement
Peripheral inputs	0.0 to 1.0 volts for logic 1 3.0 to 5.0 volts for logic 0
Module outputs	Open or 3.0 to 5.0 volts for logic 0 0.0 to 0.4 volts for logic 1
Power (from CPU or expansion chassis)	+5 Vdc at -0.53A

SECTION II

INSTALLATION

2.1 GENERAL

This section provides instructions for unpacking, inspecting, and installing a 16 Input/16 Output TTL Data Module.

2.2 UNPACKING

The module is packed in one box and is wrapped in plastic bubble-pack wrapping. Visually inspect the box for signs of damage. Remove the module from the box. Verify that at least three (six for Part Numbers 945145-0002 and 045145-0003) jumpers have been received (the jumpers are plugged into the circuit board for shipping). Do not discard any of the wrapping material until all equipment has been accounted for.

2.3 INSPECTION

Perform the following steps prior to installing the module in a chassis slot:

1. Visually inspect the circuit board for cracks, corrosion, loose components, and loose connectors.

2. Remove all jumpers from their shipping locations.

3. According to the pre-determined requirements for the module, insert the jumpers into the proper sockets. Table 2-1 gives the connections for all possible options.

Table 2-1. Jumper Connections

945145-0001 No Interrupt	945145-0002 One High to Low Interrupt	945145-0003 One Low to High Interrupt	945145-0004 No Interrupt
E5 - E6	E5 - E8	E5 - E8	E5 - E6
E16 - E18	E9 - E10	E9 - E10	E16 - E18
E17 - E19	E6 - E12	E11 - E12	E17 - E19
	E7 - E13	E7 - E13	
	E16 - E18	E16 - E18	
	E17 - E19	E17 - E19	

2.4 INSTALLATION

After defining the location for the data module, checking the jumper configuration, and insuring that the required voltages are available for the module, perform the following steps to install the module in the desired location:

1. Ensure that the chassis power is off.

2. Insert the circuit board, component side up, into the selected slot until the sides of the board slide into the card guides on either side of the slot (one guide is the center card guide, Part Number 945129-0001, which must have been installed before inserting the circuit board).

3. Gently push the board straight in until the card edge connector engages the slotted connector in the backpanel of the chassis.

4. Insert the appropriate cable into the external device connector.

5. Dress the cable out of the chassis (toward the center of a mainframe chassis, toward the bottom of an expansion chassis).

6. Connect the other end of the cable to the desired peripheral device in accordance with the installation instructions for the device.

SECTION III

OPERATING INSTRUCTIONS

3.1 GENERAL

Operation of the 16 Input/16 Output TTL Data Module consists entirely of the programming required to perform the necessary interface with the attached peripheral device. The service routines implemented to handle the interface use the SBO, SBZ, TB, LDCR, and STCR instructions from the 990 Computer instruction repertoire (see the *990 Computer/TMS 9900 Microprocessor Assembly Language Programmers Guide*, Manual Number 943441-9701). All of these instructions require the use of an effective CRU address that addresses bit 0 of the module under consideration. Since the module can be inserted into any of the available CRU chassis locations, and the locations are wired for pre-established addresses, the base address becomes a variable dependent upon the hardware configuration.

3.2 PROGRAMMING

The interface between the CPU and the module consists of 16 addressable I/O bits. The I/O routines written to handle communications with the attached devices vary for each device type. This is due to the differences in the controls accepted and the status returned by the device. Generally, the I/O routine must first establish communications with the device and then proceed to read/write on a character-by-character basis. At the same time, the routine must be prepared for irregular status indicators and, if the 16 I/O TTL board is so wired, be capable of handling interrupts.

The simplified control system example presented in Section I is a case where the single-bit CRU instructions are used to control operation of the data module interface. A service routine of the following type would execute after the computer had been interrupted and the current machine status saved:

```
TANKLO  EQU   0        Define label.
TANKFL  EQU   1        Define label.
OPVALV  EQU   2        Define label.
START   TB    TANKLO   Is fluid level too low?
        JNE   OPEN     If yes, jump to the corrective routine.
        TB    TANKFL   Is the tank full?
        JNE   CLOSE    If yes, jump to the corrective routine.
EXIT    RTWP           Interrupt corrected. Return to the interrupted
                       program and restore status.
OPEN    SBO   OPVALV   Open the input valve to correct the fluid
                       low condition.
```

```
        JMP     START   Return to the start of the routine to see
                        if the problem has been corrected.

CLOSE   SBZ     OPVALV  Close the valve.

        JMP     START   Return to the start of the routine to see
                        if the problem has been corrected.
```

The multiple bit instructions, LDCR and STCR, are typically used in a service routine that handles data groups.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section provides the theory of operation of the 16 Input/16 Output TTL Data Module. A general description of the data module is given in Section I and it should be read first if the reader is not familiar with the basic data module operation. The detailed description in this section is accompanied by timing diagrams and abbreviated logic diagrams. Detailed logic diagrams may be found in the *Model 990 Computer Family Maintenance Drawings Manual*, Manual Numbers 945421-9701 and 945421-9702.

4.2 DATA MODULE INPUT LOGIC

Refer to figure 4-1 for a diagram of the data module input logic, the associated timing diagram, and the pin numbers used on the data module. As shown, the CPU provides the data module with +5 Vdc and a common ground that can be tied in with the peripheral device. The 16 peripheral input lines are applied to the U3 multiplexer via individual emitter-follower transistors. Capacitor pads are provided across the inputs for use when line noise is a problem. When the user program decides to read one of the input lines, the CPU develops address select lines (CRUBIT12-15) which are decoded by the multiplexer (see table 4-1) and a data module enable (IMODSELA–) that combine to select one of the 16 input lines. The input data is inverted three times and passed to the CPU via the CRUBITIN– line. A low (0 to 1 V) or high (3 to 5 V) input signal becomes a high (logic 1) or low (logic 0) logic level, respectively, in the CPU.

4.2.1 MULTIPLEXER. The multiplexer is a 16-to-1 data selector (see figure 4-2) that passes one of its inputs to a output gate each time it is strobed by IMODSELA– from the CPU. The input passed is selected by the CRU address bits, CRUBIT12-15, as shown in table 4-1. Once passed to the output of the multiplexer, the data is gated to the CPU if IMODSELA– = 0.

4.3 DATA MODULE OUTPUT LOGIC

Refer to figure 4-3 for a diagram of the data module output logic, the associated timing diagrams, and the pin numbers used on the module. When a program is required to transfer data from the CPU to an attached peripheral device, the CPU must supply the data module with an output data bit (CRUBITOUT–), destination flip-flop select address (CRUBIT12-15), a data module enable signal (IMODSELA–), and a write clock signal (STORECLK–). The IMODSELA– and STORECLK– signals combine to gate the data bit into the selected flip-flop. The CRUBIT12-15 signals are applied to the U13 address decoder to select the destination flip-flop (see table 4-2). The CPU output bit is inverted and stored in the selected flip-flop and then made available to the attached peripheral after two more level inversions. The result of the three level inversions is that a logic 1 (2.4 V) or a logic 0 (0.4 V) of computer output data becomes a low voltage (0.4 V or less) or an open circuit, respectively, at the peripheral interface.

4.3.1 OUTPUT DECODER. The U13 output decoder is a 4-line-to-16-line decoder. As shown in figure 4-4, it accepts the CRUBIT12-15 inputs and the IMODSELA– and STORECLK– signals. When IMODSELA– and STORECLK– are both low, the decoder reads the inputs and selects the appropriate output line.

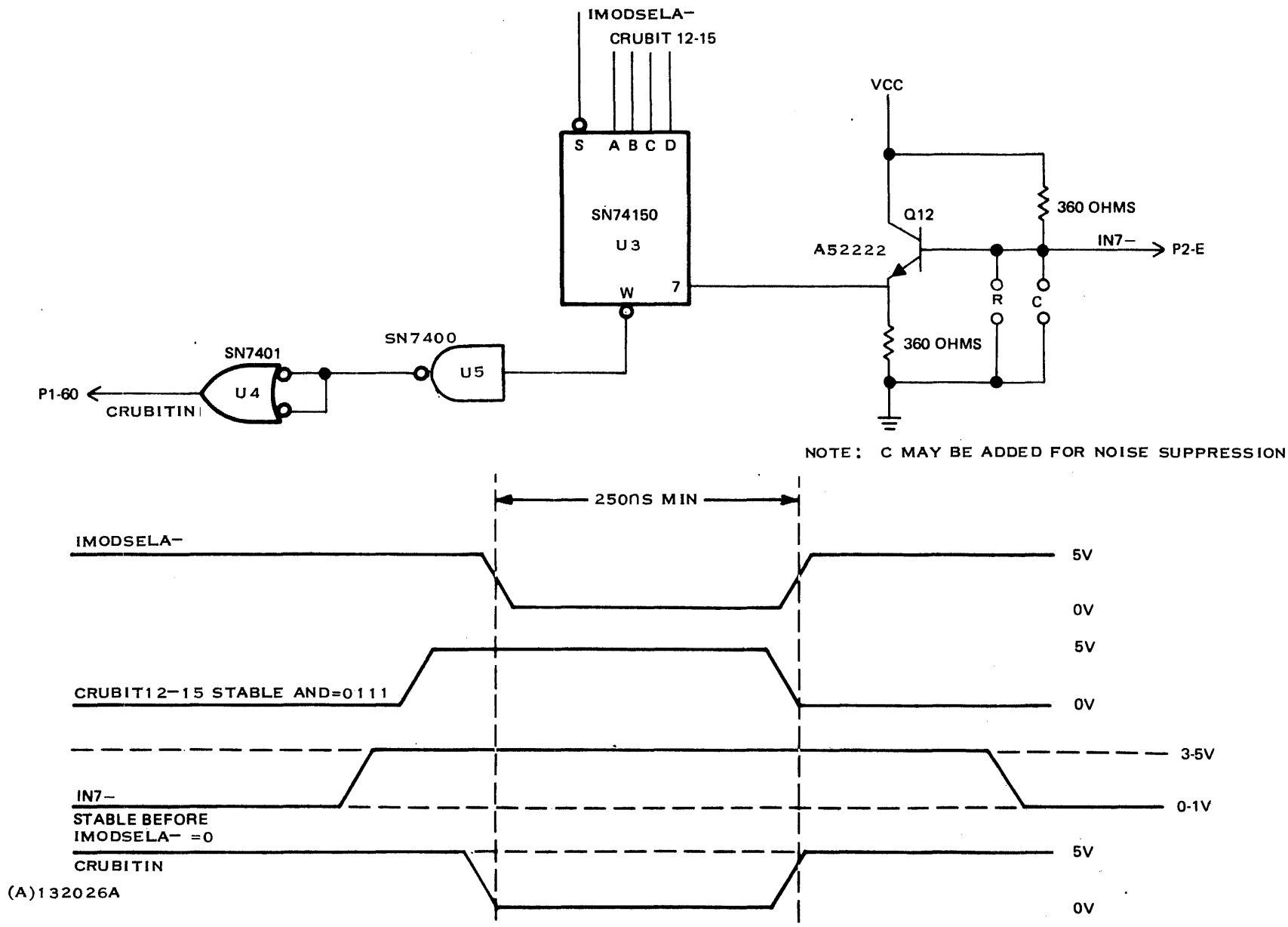


Figure 4-1. Data Module Input Circuit and Timing

Table 4-1. Multiplexer Input Select for CRUBIT12-15

CRUBIT12-15	Input Selected
0000	IN0–
0001	IN1–
0010	IN2–
0011	IN3–
0100	IN4–
0101	IN5–
0110	IN6–
0111	IN7–
1000	IN8–
1001	IN9–
1010	IN10–
1011	IN11–
1100	IN12–
1101	IN13–
1110	IN14–
1111	IN15–

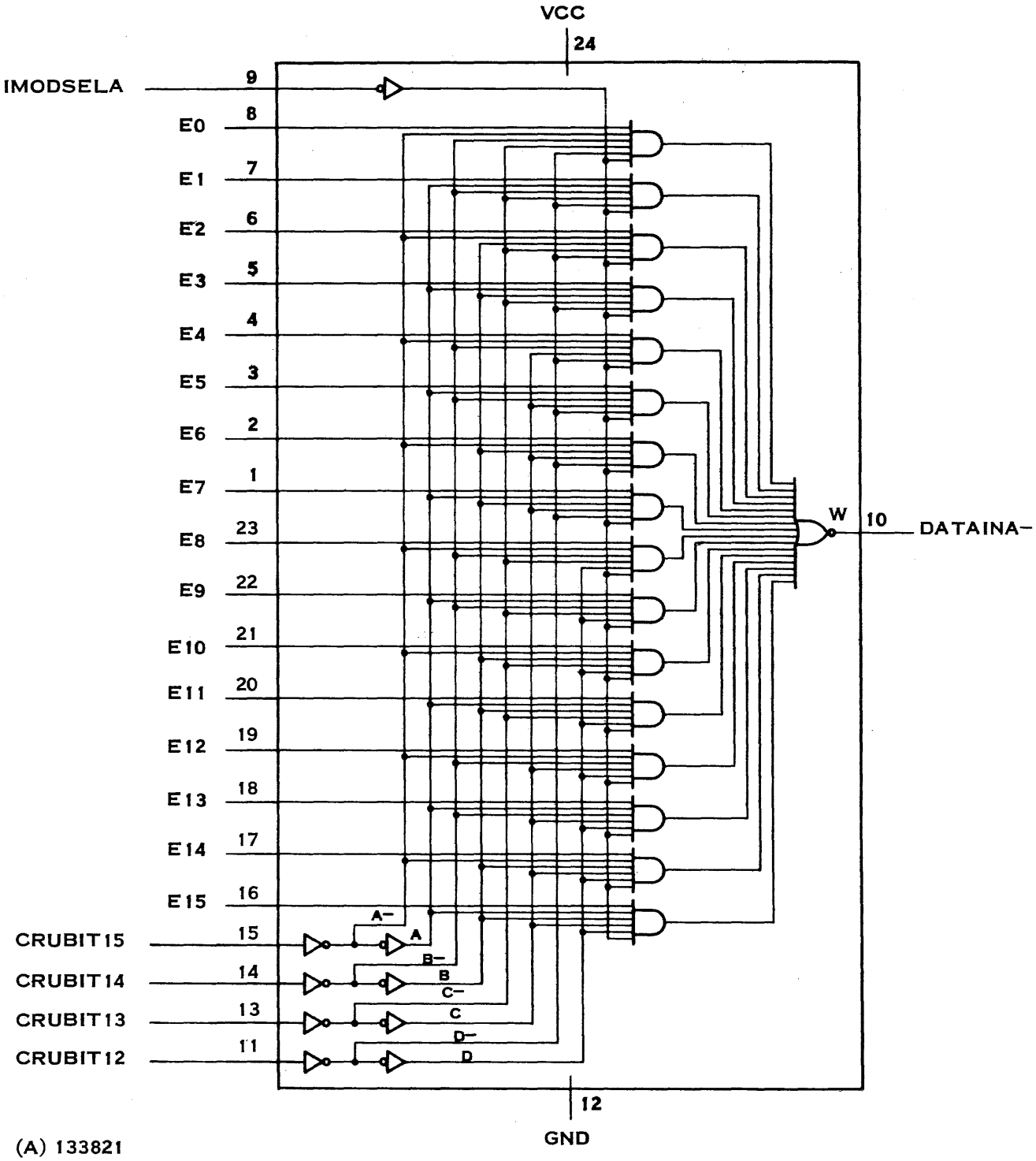


Figure 4-2. Data Selector/Multiplexer

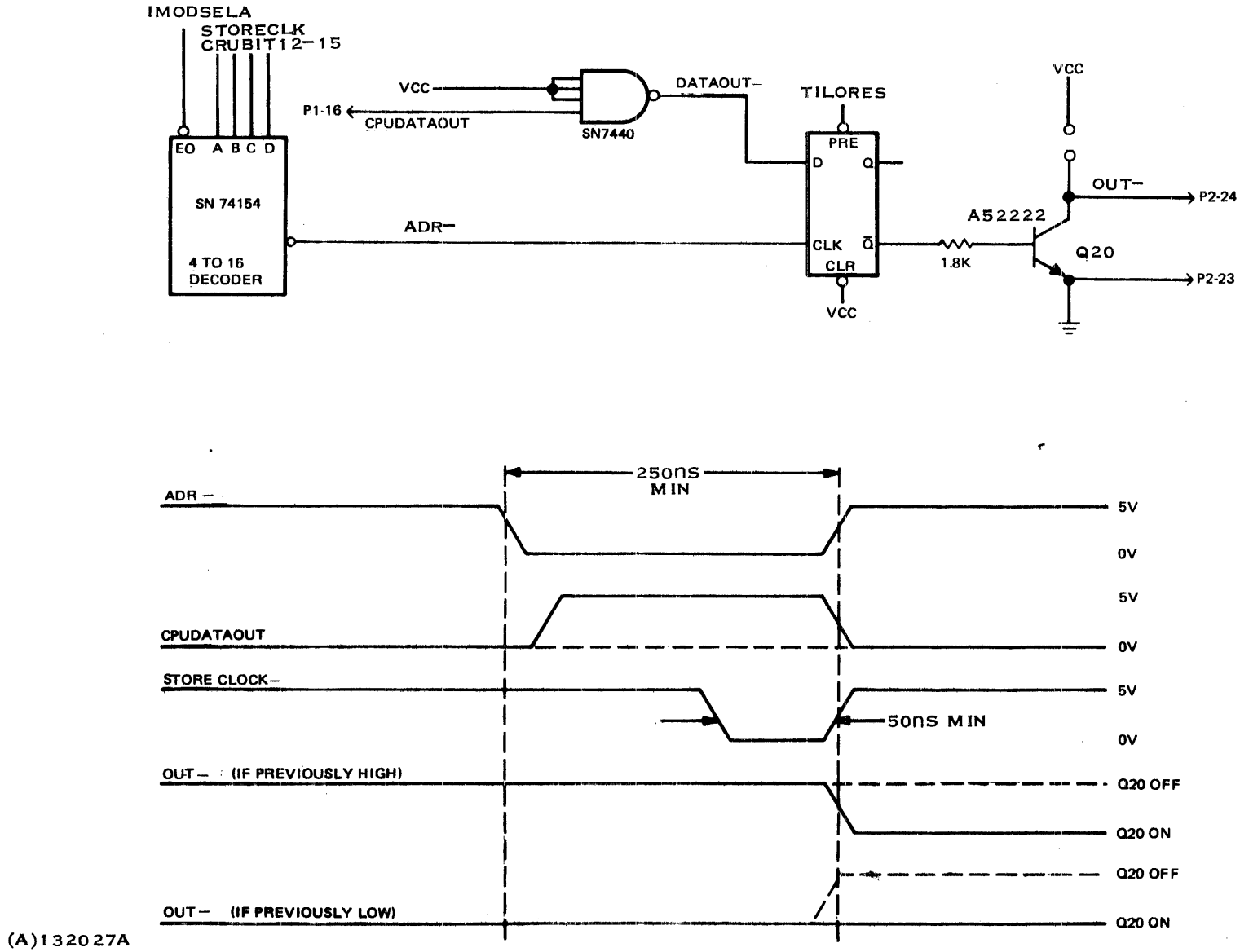


Figure 4-3. Data Module Output Flip-Flop and Timing

Table 4-2. Decoder Output Select for CRUBIT12-15

CRUBIT12-15	Output Selected
0000	OUT0–
0001	OUT1–
0010	OUT2–
0011	OUT3–
0100	OUT4–
0101	OUT5–
0110	OUT6–
0111	OUT7–
1000	OUT8–
1001	OUT9–
1010	OUT10–
1011	OUT11–
1100	OUT12–
1101	OUT13–
1110	OUT14–
1111	OUT15–

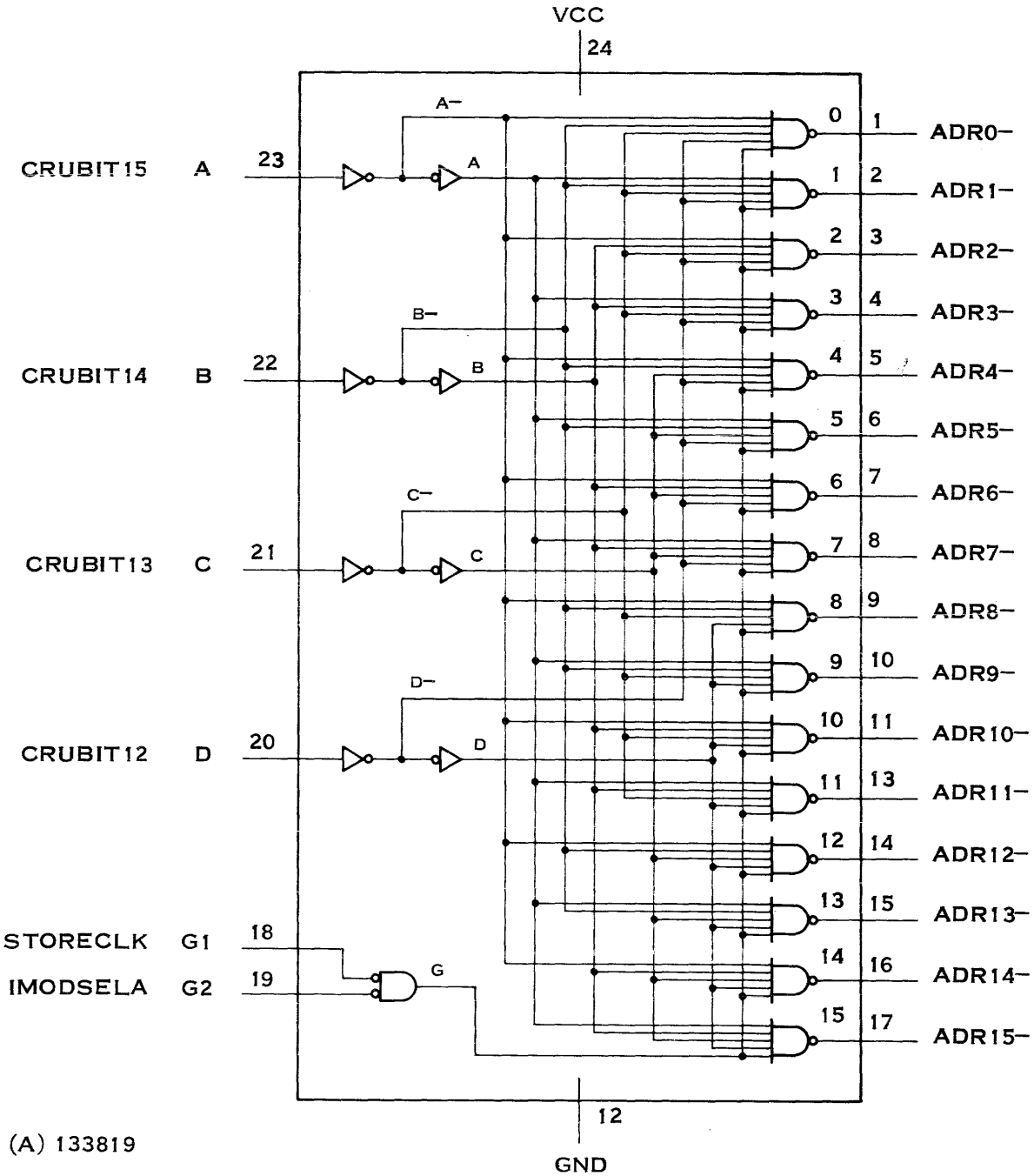


Figure 4-4. 4-Line-to-16 Line Decoder/Multiplexer

4.3.2 **OUTPUT FLIP-FLOPS.** The flip-flops used on the data module are dual D-type positive edge triggered flip-flops with preset and clear as shown in figure 4-5. The CRUBITOUT– is gated into the appropriate flip-flop by the U13 decoder, inverted by the flip-flop and input to the output transistor for the selected line.

4.3.3 **OUTPUT TRANSISTORS.** Each of the output transistors must have some type of pull-up resistor and power supply connected to its collector lead. Pads are provided on the data module for connecting pull-up resistors to the local +5 Vdc power supply. The output transistors are capable of sinking up to 50 milliamperes at up to +30 volts.

4.4 DATA MODULE INTERRUPT LOGIC

Refer to figure 4-6 for a diagram of the two data module interrupt configurations, the associated timing diagram, and the pin numbers used on the data module. The difference between the two interrupt types is that one provides for interrupting the computer on a negative transition of the peripheral interrupt signal, and the other provides for interrupting the computer on a positive transition of the peripheral interrupt signal. When a peripheral interrupt occurs, it is inverted either once or twice, depending on the selected interrupt type, and applied to a differentiating network consisting of C28, R38, and R68. Under steady-state conditions (no interrupt) the voltage divider of R38 and R68 disables the recording of any interrupts by maintaining approximately 2.5 V on the clear input of the interrupt flip-flop.

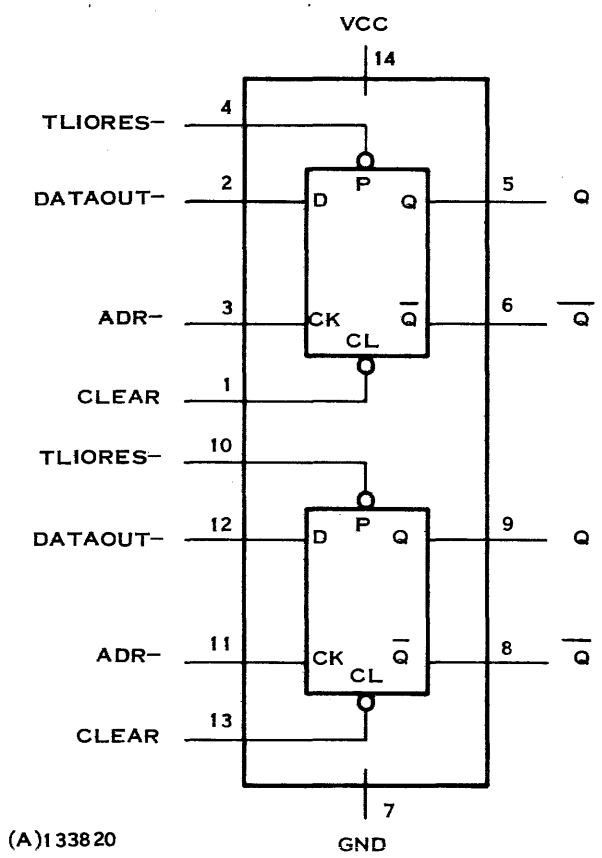
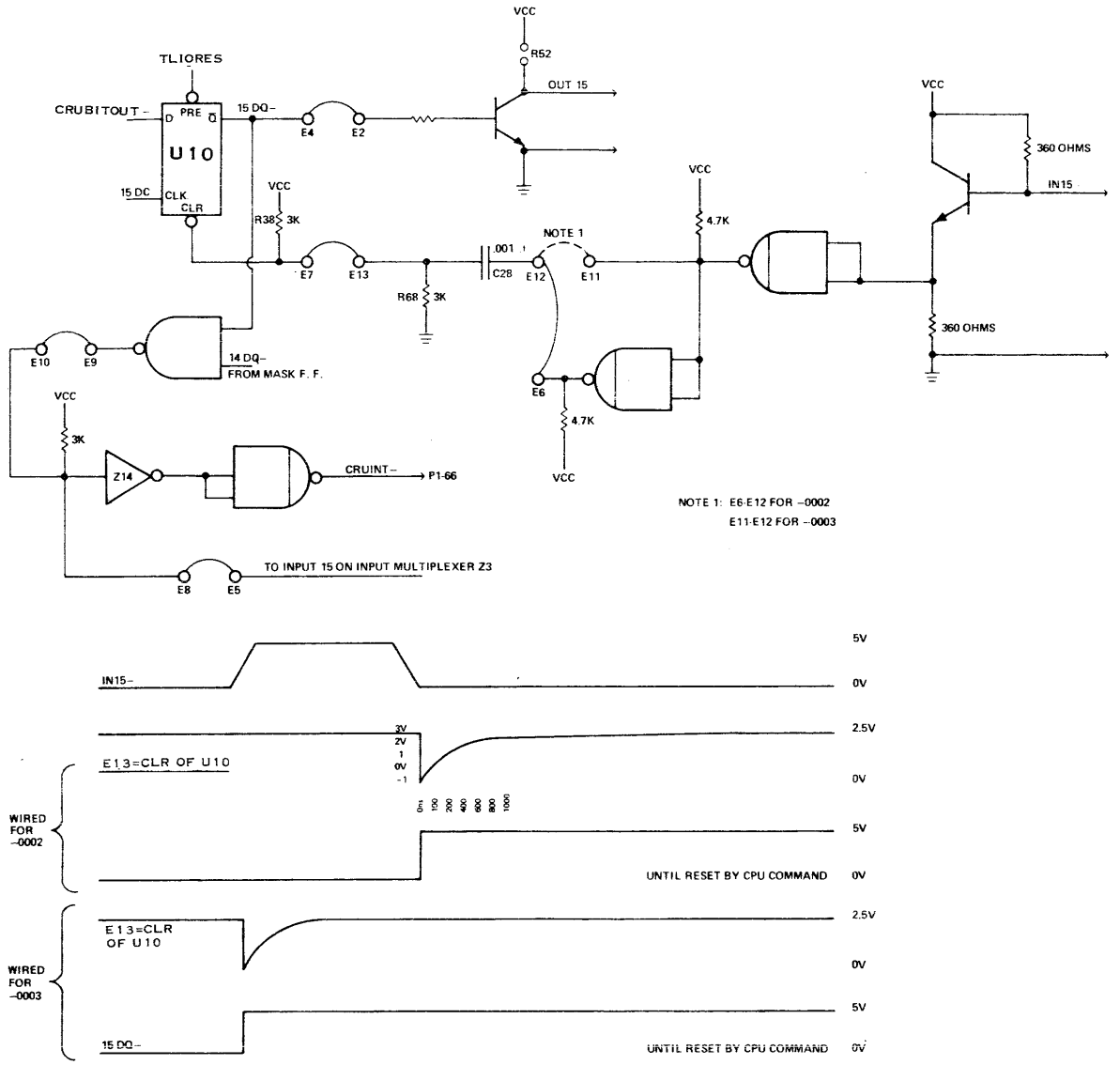


Figure 4-5. Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear



(A)132028A

Figure 4-6. Edge Triggered Interrupt Generation Logic and Signals

When a voltage drop occurs at terminal E13 (due to either a positive or negative transition of the input interrupt, depending on the wired configuration), the voltage spike generated by the differentiating network clears the interrupt flip-flop. If the CPU has enabled the associated interrupt mask, the recorded interrupt is inverted three times and transferred to the CPU as a low active (0.4 V) signal. The CPU will then execute a service routine in response to the interrupt.

In addition to receiving the hard-wired interrupt, the CPU can be programmed to locate the source of the interrupt via the U3 multiplexer. Both the interrupt mask and the interrupt flip-flop can be controlled by the CPU with the normal addressing mechanism discussed for the data module output logic.

SECTION V

MAINTENANCE

5.1 GENERAL

This section describes the depot maintenance philosophy for the 16 Input/16 Output TTL Data Module and provides troubleshooting procedures to allow fault isolation to the component level. Component replacement procedures are described in *Model 990/4 Computer System Depot Maintenance Manual,* Manual Number 945403-9701 and in *Model 990/10 Computer System Depot Maintenance Manual,* Manual Number 945404-9701. The engineering drawings for the 16 Input/16 Output TTL Data Module are found in the *Model 990 Computer Family Maintenance Drawings Manual,* Manual Number 945421-9701 and 945421-9702.

5.2 MAINTENANCE PHILOSOPHY

Depot maintenance for the 16 I/O TTL Data Module is based on the use of a hot mock-up system incorporating a Model 990 Computer, a Model 990 Maintenance Unit, and a dual-trace oscilloscope/digital multimeter, as shown in figures 5-1 and 5-2.

Suspect modules from the field repair facilities are serviced by placing the module on an extender board in the hot mock-up computer chassis. Initial testing is controlled by a diagnostic program read into the computer memory from either a cassette transport located in the Model 990 Maintenance Unit, or a Model 733 ASR/KSR Teleprinter. Resulting error messages are printed by the teleprinter.

Faults are then isolated to the component level by establishing and tracing scoping loops that isolate the circuits indicated by the diagnostic testing.

5.3 SPECIAL TEST EQUIPMENT

The special test equipment required to perform depot maintenance on the 16 I/O TTL Data Module includes:

- Model 990 Computer Hot-Mock-Up System
- Model 990 Maintenance Unit
- Test Connector (Part Number 946760-0001) for use with models 945145-0001 and 945145-0004
- Test Connector (Part Number 946760-0002) for use with models 945145-0002 and 945145-0003.

Operating procedures for the special test equipment are provided in the *Model 990/4 Computer System Depot Maintenance Manual,* Manual Number 945403-9701 and in the *Model 990/10 Computer System Depot Maintenance Manual,* Manual Number 945405-9701. Operating procedures for the oscilloscope/multimeter are contained in the manufacturer-supplied user manuals for the equipment.

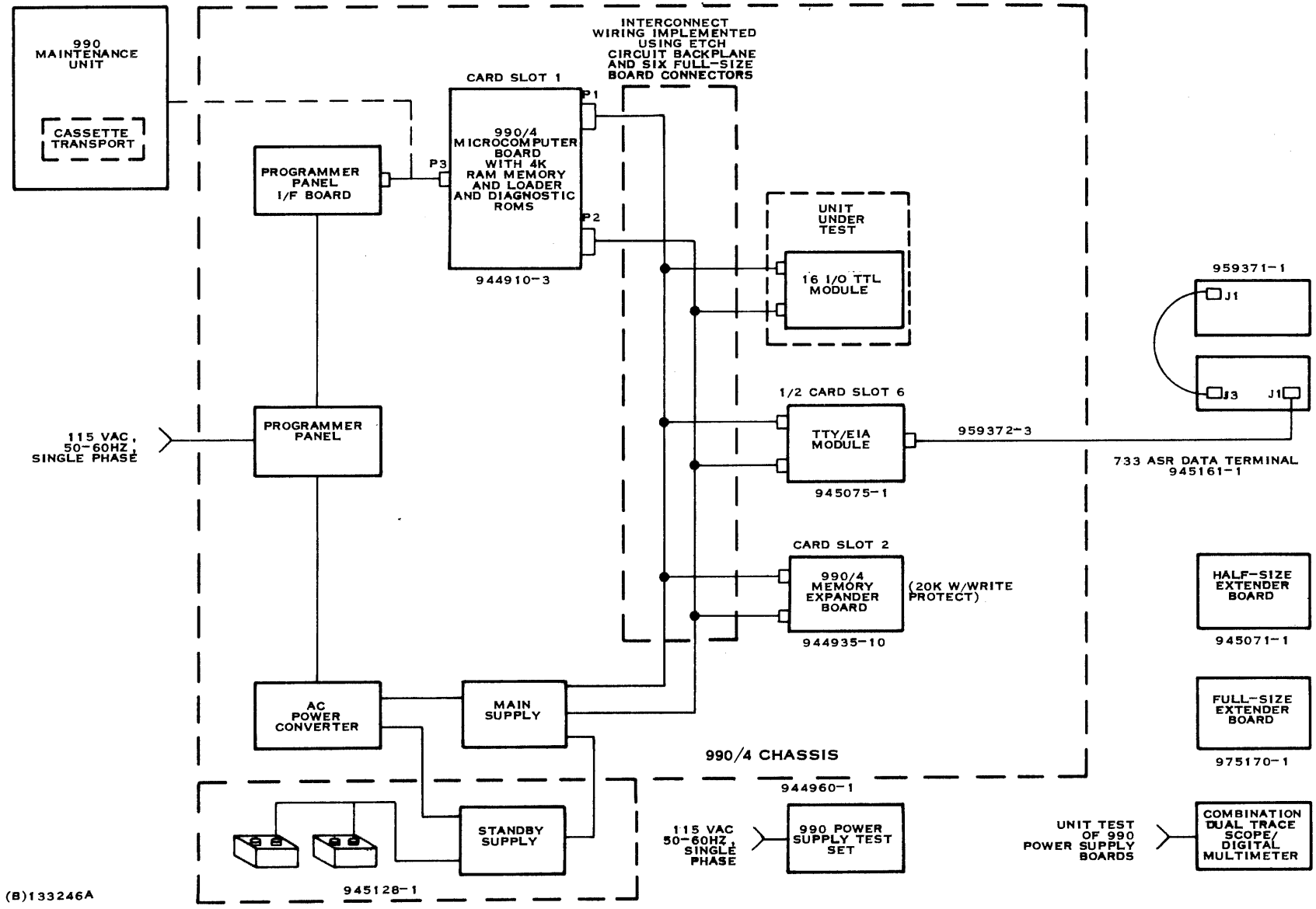


Figure 5-1. Model 990/4 Computer Hot Mock-Up System

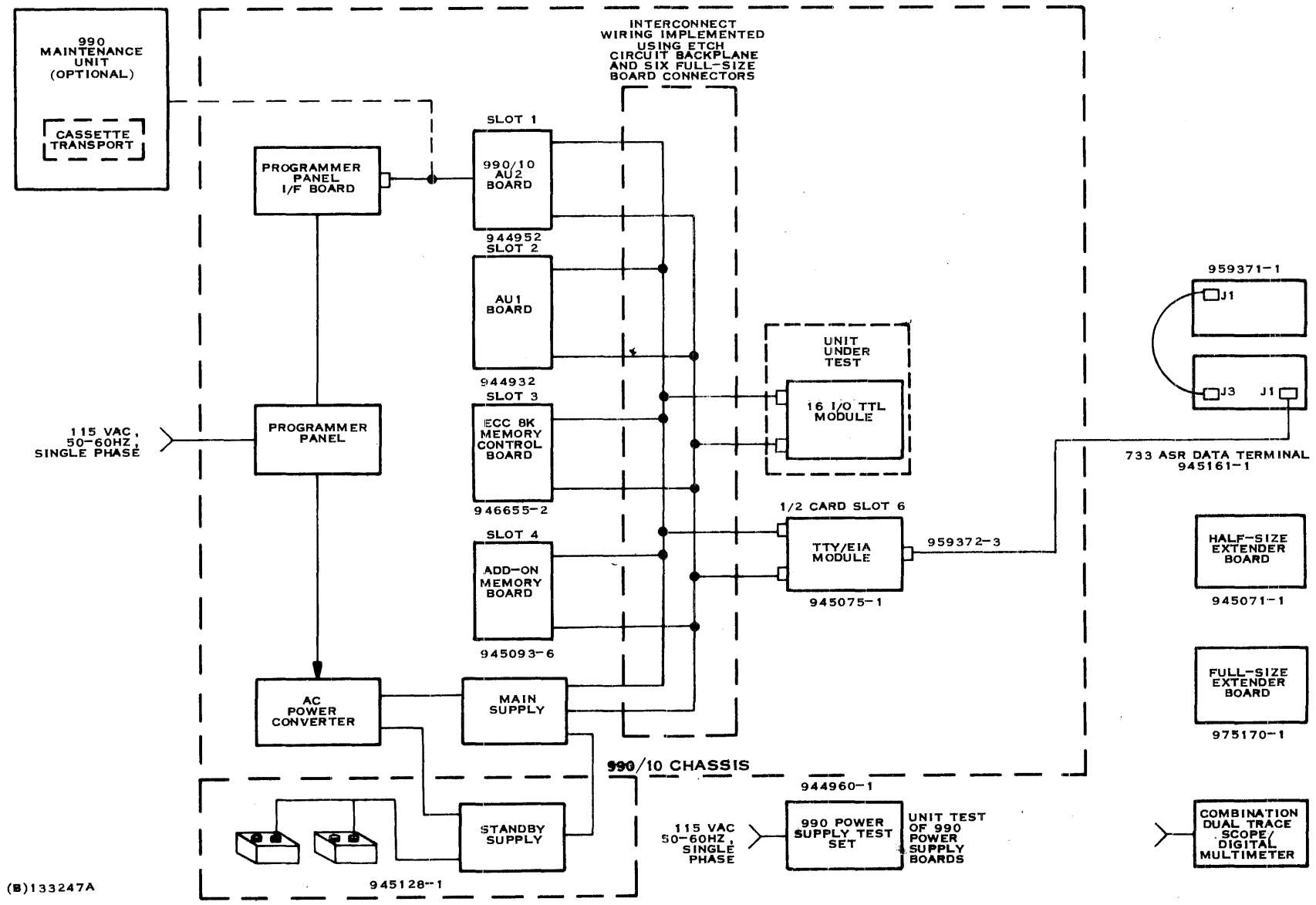


Figure 5-2. Model 990/10 Computer Hot Mock-Up System

5.4 TROUBLESHOOTING PROCEDURES

Upon receipt of a defective data module from a field repair facility, inspect the module for visible signs of damage (loose or missing components, loose or missing jumpers, breaks in the board or etched circuits, foreign material which may have caused short circuits, etc.). If no indications of damage are found, place the module on an extender card in the hot mock-up system and perform the procedures listed in table 5-1.

5.4.1 SCOPING LOOPS. A scoping loop is a short repetitive software program which establishes and maintains a set of conditions in the circuitry under observation so that an error of brief duration may be observed and isolated. Once the malfunction has been discovered, a scoping loop is entered into the hot mock-up computer from the programmer panel on either the computer chassis or the Model 990 Maintenance Unit. The scoping loop permits data to be written into or read from a desired memory location or block of memory locations. Dynamic troubleshooting may then be performed in accordance with the procedures in table 5-1. Table 5-2 provides a reference for tracing each output line circuit, and table 5-3 provides a reference for tracing each input line circuit.

The following scoping loop is used to set a CRU output line to '1' and to read back the corresponding CRU input line. The normal indication is that CRUBITIN– = CRUBITOUT.

Main Memory Location	Machine Code	Comments
1000	C300	MOV 0.12 (Move the CRU base address to register 12)
1002	1D09	SBO 9 (Set CRU output line '9' to '1')
1004	0206	LI 6,>0040 (Load register 6 with 0040_{16})
1006	0040	
1008	0606	DEC 6 (Decrement register 6 by one)
100A	16FE	JNE $-1 (Loop until register 6 = 0)
100C	1F09	TB 9 (Test CRU input line 9)
100E	10F8	JMP $-7 (Go back to the beginning of the loop)
1040	XXXX	Enter the CRU base address.

WP = 1040
PC = 1000

Table 5-1. Test Procedures

Step	Sympton	Probable Cause	Troubleshooting Procedure	Normal Indication	If Abnormal
1	Bad data to device.	Transmit Shift Register	Set up a scoping loop to transmit data to the device.	Output line = 0	Check circuit back for the appropriate line. See table 5-2 for reference designators and pin numbers. Replace components where necessary.
2	Bad data from device.	Link receiver	Actuate terminal.	CRUBITIN = 0 (if input = 1)	Check circuit through to the U3 multiplexer using table 5-3. From U3, check pin U3-10, U5-1,2,3, and U4-8,9,10. Replace components where necessary.
3	No data from device.	Multiplexer, receive buffer	Set up a scoping loop to read back a CRU character.	CRUBITIN = CRUBITOUT	Check circuit back from U4-10 through U5-3 and U3-10. Check back from U3 using table 5-3. Replace components where necessary.
4	Interrupt not received at CPU	Interrupt flip-flop	Set up scoping loop to generate correct signal on IN15–.	INTERRUPTA = 0	Check circuit back from U4-13 through U5-8, U10-6, U4-4 (model 0002 only), U4-1, and Q19. Replace components where necessary.

Table 5-2. Output Line Reference Chart

Line No.	P2 Pin No.	Transistor Ref. No.	Flip-Flop Ref. No.	Flip-Flop Pin No. Data In/Out	CLK Pin No.	Mult. Out
OUT0–	2	Q26	U16	12/8	11	0
OUT1–	3	Q21	U16	2/6	3	1
OUT2–	4	Q27	U17	12/8	11	2
OUT3–	5	Q22	U17	2/6	3	3
OUT4–	6	Q29	U18	2/6	3	4
OUT5–	7	Q28	U18	12/8	11	5
OUT6–	8	Q32	U20	2/6	3	6
OUT7–	9	Q30	U20	12/8	11	7
OUT8–	10	Q14	U1	2/6	3	8
OUT9–	11	Q13	U1	12/8	11	9
OUT10–	12	Q15	U6	2/6	3	10
OUT11–	13	Q20	U6	12/8	11	11
OUT12–	14	Q23	U9	2/6	3	12
OUT13–	15	Q31	U9	12/8	11	13
OUT14–	16	Q24	U10	12/8	11	14
OUT15–	17	Q25	U10	2/6	3	15

Table 5-3. Input Line Reference Chart

Line No.	Transistor Ref. No.	Multiplexer Pin No.
IN0–	Q2	8
IN1–	Q1	7
IN2–	Q7	6
IN3–	Q8	5
IN4–	Q9	4
IN5–	Q10	3
IN6–	Q11	2
IN7–	Q12	1
IN8–	Q3	23
IN9–	Q4	22
IN10–	Q5	21
IN11–	Q6	20
IN12–	Q16	19
IN13–	Q17	18
IN14–	Q18	17
IN15–	Q19	16

This scoping loop may be used to test any input/output line by changing the line designations in the SBO and TB instructions. The scoping loop is entered into the computer from the programmer panel using the following procedures:

1. If the Model 990 Maintenance Unit is being used, set its POWER switch to the ON position and set the MODE switch to the PANEL position. If the programmer panel is part of the computer chassis, proceed to step 2.

2. Set the key switch on the programmer panel to the UNLOCK position.

3. If the RUN LED is lighted, press the HALT/SIE switch to halt the processor and begin execution of the programmer panel code. When the panel is active, the RUN LED is extinguished.

4. Press the CLR switch to clear the panel's display register.

5. Press the ENTER ST (enter status) switch to clear the status register in the TMS 9900.

6. Set up 1000_{16} on the data display LEDs using the data entry switches. This is the memory address where the first instruction of the scoping loop is to be stored.

NOTE

A lighted display LED indicates a logic 1.

7. Press ENTER MA switch to load the memory address value 1000_{16} into the memory address register of the TMS 9900.

8. Press CLR to clear the displays for the next entry.

9. Set up the instruction code $C300_{16}$ on the data LED display using the data entry switches.

10. Press MDE switch to load $C300_{16}$ into memory location 1000_{16}.

11. Press MA1 to increment the memory address value stored in the memory address register and repeat steps 8 through 11 until all instructions and the CRU address are loaded.

12. Press CLR to clear the displays.

13. Enter 1000_{16} into the displays (address of first instruction in the scoping loop).

14. Press ENTER PC to load the value into the program counter.

15. Enter 1040_{16} into displays.

16. Press ENTER WP to enter workspace pointer.

17. Press CLR to clear displays.

18. Press RUN to begin execution of the program. The RUN LED should light to indicate proper operation.

NOTE

If the RUN LED fails to light, return to step 1 and repeat the program setup procedure.

The following scoping loop is used to test all 16 of the output/input lines. As shown, it sends $FFFF_{16}$ out and loops it back on the input lines. The $FFFF_{16}$ value is loaded into the interface by the LDCR instruction from register 2; the 16 bits read back are stored in register 8 by the STCR instruction. The normal indication is that register 2 = register 8. By changing the value at location 1006_{16}, any value (pattern) may be looped out/in. By changing the count operand of the LDCR and STCR instructions, any number of lines may be tested.

The loading procedures for this loop are identical to those for the previous example.

Main Memory Location	Machine Code	Comments
1000	C300	MOV 0,12 (Move the CRU base address to register 12)
1002	04C8	CLR 8 (Clear register 8)
1004 1006	0202 FFFF	LI 2,>FFFF (Load register 2 with $FFFF_{16}$)
1008	3002	LDCR 2,0 (Load the 16 CRU lines with the data in register 2)
100A 100C	0206 0040	LI 6, 0040 (Load register 6 with 0040_{16})
100E	0606	DEC 6 (Decrement register 6 by one)
1010	16FE	JNE $-1 (Loop until register 6 = 0)
1012	C300	MOV 0,12 (Move the CRU base address to register 12)
1014	3408	STCR 8,0 (Load register 8 with the value of the 16 CRU input bits)
1016	10F4	JMP $-11 (Go back to the beginning of the loop)
1040	XXXX	CRU base address.

$PC = 1000_{16}$
$WP = 1040_{16}$

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
- Appendixes - References to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.
- Paragraphs - References to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph is found.
- Tables - References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number:

  Tx-yy

- Figures - References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number:

  Fx-yy

- Other entries in the Index - References to other entries in the index are preceded by the word "See" followed by the referenced entry.

USER'S RESPONSE SHEET

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Depot Maintenance Manual (945407-9701)

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CUT ALONG LINE

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