## Taltonix

## 4023 <br> COMPUTER DISPLAY TERMINAL

SERVICE MANUAL

# Tektronix <br> COMMITTED TO EXCELLENCE 

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## 4023 COMPUTER DISPLAY TERMINAL

SERVICE MANUAL

Tektronix, Inc.

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# INSTALLATION AND OPERATION 

This manual is a part of the following set of documents which describe the 4023 Refreshed Computer Display Terminal:

4023 USERS MANUAL, Tektronix Part No. 070-1621-00.

Contents-An explanation of how to operate and program the 4023.

4023 SERVICE MANUAL, Tektronix Part No. 070-1617-00.

Contents-A comprehensive explanation of the 4023. It includes operation, characteristics, servicing, adjustment, circuit description, and parts lists.

Optional items used with the Terminal are explained in separate manuals.

## INTRODUCTION

The 4023 Computer Display Terminal interfaces between man and computer by permitting inputs through an integral keyboard and providing a display of computer output data. In addition, the Terminal can relay data bi-directionally between peripheral devices and a computer. An Interface Unit must be installed in the Terminal and connected to the computer-either directly or through a modem (modulator-demodulator)-to permit information interchange. The Terminal has the ability to have copies made of its display, via a Hard Copy Unit.

## INSTALLATION

## GENERAL

Installation consists of desk-mounting the Terminal, selecting the proper operating voltage and fuse size, setting the desired strap options, and connecting the Terminal to the computer. These steps are discussed in the following paragraphs.

## MOUNTING THE TERMINAL

Desk-Mounting consists of simply setting the Terminal on a desk or other surface. The air vents on the bottom and sides should be kept free of obstructions to permit air flow through the unit.

A dimensional drawing is provided in Fig. 1-2 as an installation aid.

## CIRCUITRY ACCESS

The display unit cover must be removed to permit access to the Motherboard into which the Terminal Control cards, interface cards, and optional accessory cards are installed. Removing the display unit cover opens a line voltage safety interlock switch, which automatically cuts power when the cover is removed. The switch actuator (located, in the top, left-rear corner) can be pulled up to permit Terminal operation with the display unit cover removed.

## WARNING

> Dangerous voltages exist in the display unit area when the line cord is connected. Servicing should be done only by qualified technicians.

## SELECTING STRAPPABLE OPTIONS

Strappable options are movable wire straps located on circuit cards inside the display unit, Figs. 1-3 and 1-4 show the strap option locations. These straps provide options for the operator and programmer and can be set at the user site by qualified technical personnel. The circuit cards (seven of them) plug into the Motherboard. See Fig. 1-5 for card locations on the Motherboard.


1. Do not remove or install circuit cards while the Terminal power is on.
2. The cards must be installed in the order shown in Fig. 1-5; otherwise, heat is not dissipated properly.

The positions of the straps are dependent upon computer and program requirements, and in some cases, upon user preference. The location and description of the movable strap options for the Keyboard Interface, Control, Timing, and Basic Data Communications Interface cards are shown in Figs. 1-3 and 1-4. Information on cut-strap options can be found in Section 2 of this manual. The Optional Data Communications Interface (021-0112-00) is to be installed in P8. The Standard Data Communications Interface (021-0111-00) is installed in P9. Detailed strappable option information for these two interfaces can be found in their respective manuals.


Fig. 1-2. Physical Dimensions.

## AC Power Sources and Requirements



This Terminal is intended to be operated from a single phase, earth, referenced power source having one current carrying conductor (neutral) at ground (earth) potential. Operation from power sources where both current-carrying conductors are live with respect to earth (such as phase-to-phase on a multiphase system, or across the legs of a 117-234 single phase three-wire system) is not recommended because only the line conductor has overcurrent (fuse) protection within the instrument.

This Terminal is designed to operate from either a 110 or 220 volt nominal line voltage source that has a frequency of 48 to 440 Hz . In addition, any of three voltage ranges for 100 Vac or four voltage ranges for 220 Vác may be selected. Voltage, current and power requirements are listed below.

VOLTAGE, CURRENT, AND POWER REQUIREMENTS

| VOLTAGE <br> RANGE | FREQUENCY | LINE FUSE <br> (slo blow) | INPUT POWER |
| :--- | :---: | :---: | :---: |
| 100,115, <br> 120 | 48 Hz | 2 A | 220 W Max |
| 20, <br> 200,220, <br> 230,240 | 440 Hz | 1.25 A |  |
|  |  |  |  |



BUF-position with BUFFER selection permits a keyboard CR to also generate a linefeed.

IN position permits either a keyboard or computer generated CR to generate a simultaneous linefeed.

OUT position inhibits simultaneous linefeeds with CR, regardless of CR origin.

A. Keyboard Interface Card.

LF position performs a linefeed only upon receipt of a linefeed command.

LF/CR position causes a simultaneous carriage return function upon receipt of a linefeed command.


IN causes wrap-around when moving cursor past 80th character position. OUT disables wrap-around


LOCAL enables line feeds to be generated in LOCAL when transmitting from the Terminal buffer to an auxiliary device. Line feeds are not transmitted to the computer is on line.

IN enables linefeeds to be generated by transmit circuits when operating in LOCAL or ON LINE with BUFFER selected.

OUT prevents linefeeds from being generated at end of a line.


OUT is used when 4023 does not require a prompt character for data transmission from buffer a line at a time.

IN is used when 4023 is to receive a prompt character for data transmission from buffer.


MESSAGE END

The Message End character is the last character sent in a buffer or Read Cursor transmission. The standard END character is strapped to be CR.

Fig. 1-3A \& B. Options on the Keyboard Interface and Control cards that can be selected by strap placement.

BLINK CURSOR
RESET BLINK position causes cursor to blink when RESET key is pressed.

BLINK position causes cursor to blink continuously.


A. Timing Card.

B. Interface Card.

Fig. 1-4A \& B. Options on the Timing and Standard Interface card that can be selected by strap placement.


Fig. 1-5. Motherboard (minibus) connector assignments.

A fuse and a transformer jumper arrangement permit the Terminal to be modified to suit the voltage supply. A tag on the back panel of the Terminal identifies the internal voltage setting for which the Terminal is wired when shipped from the factory. If, for any reason, the jumper arrangement is changed, changing the internal voltage setting, cross out the old setting and write the new voltage setting on a tag. Attach the tag to the rear panel or the line cord.

The fuse is located in the bottom-left corner of the back panel. The Transformer and jumper arrangement are located inside the display unit in the left rear corner (see Fig. 1-6). Removing the display unit provides access to the jumper arrangement. This consists of removing two screws at the top of the rear panel. The display unit cover can be removed. Wiring instructions are shown on the metal protection cover directly above the transformer wiring connectors. See Fig. 1-6.

## WARNING

Dangerous voltages exist at several places inside the display unit. Disconnect the Terminal from the power source before changing transformer connections. (In the event the power was on when the cover was removed, a safety interlock switch disables the power supply. Pulling the switch up allows the Terminal to be operated with the cover off.)

## AC POWER CORD AND GROUNDING REQUIREMENTS

This instrument has a three-wire power cord with a three-wire terminal polarized plug for connection to the power source and safety earth. See Fig. 1-7 for USA standard plugs. The Safety Earth terminal of the plug is directly connected to the instrument frame for electricshock protection. Insert this plug only in a mating outlet with a safety earth contact or otherwise connect the frame of the Terminal to a safety earth system. The color coding of the cord conductors is in accordance with recognized standards as shown below. In other jurisdictions, replace the USA standard plug with a plug that satisfies local authorities.


Fig. 1-6. Location of Transformer wiring connectors.


Fig. 1-7. Transformer terminal jumper arrangement.


Fig. 1-8. Card-edge connector pin assignments.

## SPARE SWITCH (SW1 AND SW2) CONNECTIONS

Connection to SWITCH 1 and SWITCH 2 is provided at pin $Z$ and $X$, respectively. Fig. 1-8 shows location of pins $Z$ and $X$ on the circuit card edge connectors.

Depressing the left side of a switch provides a ground connection for the respective switch; the other position of the switch results in an open circuit.

## SPARE INDICATOR CONNECTION

Connection to spare Indicator 3 is provided at pin 2 of the card-edge connector.

## REAR PANEL CONNECTORS

J190 - HARD COPY CONNECTOR. This is a fifteen pin female connector with signals for sending video out of the 4023. It can be used by the Hard Copy Unit or other devices for connections up to 200 feet ( 15 -foot and 200-foot cables are available).

VIDEO CONNECTORS. The Monitor connection is a 75 -ohm BNC connector for composite video. The number of video monitors to which the 4023 can provide acceptable video depends on the type of monitor, the cable distance to the furthest monitor, and the type of connecting cable used. Single loop-through is used, with a single 75 -ohm termination on the end of the string of monitors.

## CONTROL DESCRIPTIONS

## GENERAL

This information describes the controls that can be manipulated by the operator at the Terminal. These include console switches, alphanumeric keys, and special purpose keys that control cursor positioning, editing, transmission, and other functions.

With the exception of the Power switch, the Display controls, and the Interface controls, all operator controls and indicators are located on the keyboard console. The Power switch and Display controls are on the lower right side of the display unit. The Interface controls are located on the back panel of the display unit.

DISPLAY \& POWER CONTROLS
POWER Provides power ON-OFF control for the Terminal.

BRIGHTNESS

CONTRAST

Adjusts brightness of the characters. Adjust for operator convenience.

Changes the difference in display intensity between white and gray. Adjust for operator convenience.


Fig. 1-9. Power and Display controls.

## REAR PANEL CONTROLS

## (Standard Data Communications Interface only)

## BAUD RATE SELECTOR

ECHO
IN OUT

An eight position rotary switch located on the rear panel that selects one of eight data transfer speeds from the 4023 to the computer.

IN position provides an "echo" that permits data to be displayed when transmitting with the DIRECT/ BUFFER switch in DIRECT. OUT position disables the Terminal's echoing of its own data and would be used when the computer provides an echo of the Terminal transmission.

## CONSOLE CONTROLS AND INDICATORS

Figure 1-11 shows the Terminal controls divided into three basic groups: the Console Controls and Indicators, the Keyboard, and the Function Pad Controls. A brief explanation of the controls in each group follows.

The console includes light-emitting diode indicators (LED's) and rocker switches. Individual descriptions follow.

Power Lamp Illuminated by the +5 V supply when the power switch is turned on.

Indicator 3

Multiple use lamp whose function is determined by the accessories and optional equipment used with the Terminal.


Fig. 1-10. Rear panel.


Fig. 1-11. Keyboard and console.

Wait Indicator
Keyboard Lock Indicator

Switch 1
and
Switch 2

Local/On Line
Switch

Indicates that the computer system cannot accept data from the 4023. Transmission sequence does not occur until the light is extinguished.

Indicates that keyboard entry is inhibited because on of the following is occurring:

1. The 4023 is transmitting a message or a message transmission is pending.
2. The cursor is located in a protected field in which data is not normally changed.
3. The cursor is positioned on a Field Attribute Code.

Two-position rocker switches whose functions are determined by the accessories and optional equipment used with the Terminal.

Two-position rocker switch that performs the following:

LOCAL electrically disconnects the 4023 from the computer. However, the Terminal can still interact with other devices to which it may be

Direct/Buffer Switch
connected. LOCAL is also used for operator familiarization, maintenance, or any other function that the Terminal can perform independent of the computer.

ON LINE permits the 4023 to communicate with the computer. Auxiliary devices connected to the Terminal can communicate with the computer and/or the Terminal.

Two-position rocker switch that provides the following functions:
DIRECT causes keyboard entries to be routed directly to the computer if the Terminal is On Line. If in Local, Keyboard entries are sent directly to any auxiliary devices that may be connected to the Terminal. An echo (either computer or local) condition must exist for keyboard entries to be displayed.

BUFFER position causes keyboard entries to be routed to the Terminal memory for editing, prior to transmitting the data to the computer (if on line), or to a peripheral.

## THE KEYBOARD

The Keyboard's primary function is to act as a source of data for the computer. The display is used to provide a visual representation of the keyboard entries and Terminal/ computer interchange.

The Keyboard has encoded keys that generate ASCII code, and function keys which generate switch closures. Most of the keys are used only for entering data and are designed for single key entry, dual key entry, and triple key entry. Most are familiar with typewriter keys. The 4023 keyboard shown in Fig. 1-9 is equipped to perform as an input for ASCII or TTY codes. ASCII characters are shown on the key caps and are represented by the key code as follows.

Letter keys Unshifted provide lower case; shifted provides upper case.

Number keys Unshifted provides numeral; shifted provides character shown on front surface of key.

Control Character Control character keys that transkeys mit control characters are: ESC, TAB (HT), BACKSPACE (BS), LF, and RETURN (CR). When these keys are pressed, the appropriate control character is transmitted regardless of SHIFT key position.

All others Unshifted (lower) or Shifted (upper) characters as shown on top surface of key caps.

TTY LOCK KEYBOARD ENTRY. Lower case letters (alpha) characters cannot be transmitted when the TTY LOCK key is depressed, regardless of the position of the SHIFT key.

REPEAT ENTRIES. Character transmission occurs when a key is pressed. If the key is held down, a 0.5 second delay (approx.) occurs, after which the character is repeatedly entered at a 10 Hz rate. If CTRL or SHIFT is used with a character key, the original selected code continues to be transmitted as long as the character key is held down, even if CTRL or SHIFT are subsequently released.

CONTROL KEYS. The following keys do not directly enter characters for transmission, but control operation of the keyboard or Terminal. Some of them are used independently, while others are used in combination with other control keys or character keys.

PAGE-ERASE INPUT When pressed alone, causes all unprotected data stored in Terminal memory to be erased, and the cursor moves to the home position. This function is normally used with formatted displays. When pressed while SHIFT is held down, performs a PAGE function. The memory is cleared, the logic is set to initial condition, and the cursor moves to home.

CTRL

SHIFT

TTY LOCK

BREAK

RUBOUT
Not a control key but a character key. When pressed, the RUBOUT ( $127_{10}$ ) character is transmitted. Use of this key is program dependent.

## FUNCTION PAD CONTROLS

This useful, dual-purpose group of controls is located to the right of the keyboard. They provide control over data transmission, editing, cursor positioning, and reset functions. With the NUM LOCK key pressed, these keys function as a numeric pad to aid in entry of numeric data.

A multiple purpose key that performs the following (depending on operating configuration):

1. Blinks the cursor; cursor quits blinking when key is released.
2. Pressing RESET while simultaneously entering a control character will store that control character in Terminal memory.
3. If the optional Rulings Character Set has been installed and selected, pressing RESET causes the standard character set to be reselected.
4. RESET terminates a buffer transmission.
5. Inhibits an $\overline{\mathrm{LCE}}$ condition as long as RESET is held down. (See $\overline{L C E}$ signal description in "Definition of Line Titles" in Section 6.)
6. Clears a Make Copy request (will not terminate a copy in progress).
7. With formatted displays, holding RESET down enables data to be keyed into a protected field: Alpha characters can also be keyed into a non-alpha field.
8. With formatted displays, pressing ERASE TO END with RESET held down, causes erasure of data in a protected field from the cursor position to the end of that field (or the end of the line).
9. When using 4 -line roll-up, pressing RESET allows 4 more lines to roll-up (used with flagged interfaces only).

ERASE TO END

COPY

INS L INS C

With a formatted display, pressing this key when the cursor resides in an unprotected field causes erasure of all data from the cursor location to the end of that field. With no fields contained in a line, data is erased from the cursor position to the end of the line.

With a Hard Copy Unit connected to the Terminal, pressing this key activates the Hard Copy Unit to make a copy (on paper) of the displayed information.

Pressing this key without SHIFT causes an Insert Character function. A SPACE character is entered at the cursor location, and data at the cursor position and to the right of the cursor moves right. Data moved past the right margin is lost. The function repeats if the key is held
down. Pressing with SHIFT causes an Insert Line function. The line where the cursor resides moves down one line, with all lines below doing likewise. Data in the 24th line is lost. The cursor remains stationary and the line where it resides is filled with SPACE (SP) characters. This function also repeats when the keys remain held down.

Pressing this key without SHIFT causes the character at cursor location to be deleted. All characters to right of cursor move left one position. A NUL character resides at the right-most character position on the line. This function also repeats. Pressing with SHIFT causes a Delete Line function. The line where the cursor resides is lost and replaced by the line immediately below. All other lines below also move up one line. The line vacated by the last line moved up is filled with NUL characters. This function also repeats when the keys remain held down.

Pressing this key without SHIFT initiates the Enter transmission sequence. Pressed with SHIFT initiates the Send transmission sequence. (See Operation Descriptions for explanation of Enter and Send.)

CURSOR (Direction Shift) Keys

HOME

NUM LOCK

A group of four non-encoded keys that provide directional movements of left, right, up, and down for the cursor. A momentary push moves the cursor one character or line position in the direction indicated on the key cap. Holding the key causes the function to repeat.

Moves the cursor to the home position. Home is the first character position of the first line. (Also terminates a buffer transmission.)

Pressing this switch enables function Pad keys to be used as a numeric pad. Specific numeric inputs provided by individual keys are embossed on the front surface of the key caps. NUM LOCK must be pressed a second time to restore normal Function Pad Controls.

## OPERATING MODES

## GENERAL

The 4023 is both a transmitting and a receiving device. Standard interface hardware provides Full Duplex only. Full or Half Duplex can be achieved by use of an Optional Data Communications Interface. Data can be transmitted to the computer directly from the keyboard, from the keyboard via the Terminal buffer (memory), or from an optional auxiliary unit. Data received by the Terminal can be displayed, or can control other functions in the Terminal or at auxiliary units.

Data transmitted to the computer can be echoed back to the receiving circuits by the computer, the modem, or by selecting Local Echo at the interface unit. Under Local Echo conditions, data from the keyboard or auxiliary unit is simultaneously sent to the computer and the 4023 receiving circuits. Printable characters from the computer enter the Terminal memory and are displayed. The computer can write anywhere on the screen regardless of fields.

The LOCAL/ON LINE switch must be in the ON LINE position to communicate with the computer. The LOCAL position allows the Terminal to operate independent of the computer. Local operation permits keyboard or auxiliary unit data to be written on the display or otherwise executed by the Terminal.

The Data Entry Modes are: Direct Entry, Buffer Entry, and Buffer Form Fill-out Entry. They function as follows: (Table 2-4 in Section 2 provides a brief description of data transfer in DIRECT and BUFFER.)

## NOTE

The following is a discussion of operation of the standard Terminal. Strappable options and other options can modify the description.

## DIRECT ENTRY

Placing the DIRECT/BUFFER switch to DIRECT sets the Direct Entry Mode. This mode is interactive by character (similar to Teletype). Destination of data depends on the position of the LOCAL/ON LINE switch. In the ON LINE position, data entered from the keyboard (keyed data) is sent directly to the computer. Data from the keyboard is not sent to the Terminal memory for display unless the computer echoes the data, or the modem or the interface unit supplies local echo. Roll-up occurs with a
cursor movement past the last line on the display. When ON LINE, the Direct Entry Mode can operate in full or half duplex (depending on the interface unit used). Placing the LOCAL/ON LINE switch to LOCAL causes all keyboard data to go directly to the auxiliary device (such as a mag storage unit). The data is not sent to the Terminal memory for display, unless a local echo condition exists.

## BUFFER ENTRY

This mode is set when the DIRECT/BUFFER switch is set to BUFFER. Keyed data is stored in memory and is displayed, allowing text editing before data entry. Buffer Entry Mode is used for either non-formatted or formatted operations. When no Field Attribute Codes (FACs) are used, the entire message is transmittable. Video is displayed white on black background with normal intensity. Pressing either the ENTER or SEND key initiates the buffer transmission sequence. As in the Direct Entry Mode, the destination of data is determined by the position of the LOCAL/ON LINE switch.

ENTER KEY ENTRY. Pressing the ENTER/SEND key without SHIFT causes an ETX code (A Message Separator) to store in memory (if display is non-formatted) at the cursor location. Storing the ETX in memory causes a rectangular marker to be displayed at the cursor positiun. The cursor moves rapidly back through the text, seeking either a start of text message (previous Message Separator) or the home position, then sends the stored message. Transmission of data continues until the cursor reaches the ETX code, at which time the Terminal sends an End Code and performs a carriage return. (The End Code can be strapped to be any desired control character. Standard strap setting is for a CR code.)

Fig. 1-12 is an illustration of the 4023 display during a typical 4023/computer entry interchange using the buffer. Assume that the cursor was originally at the home position. The operator keys into the Terminal memory the first line, edits if necessary, then presses the ENTER key. The cursor moves rapidly back through the text, searching for a previously stored Message Separator or the home position, in this case, the home position. Data entry then begins at the home position. Data entry continues to the ETX code that was stored when the ENTER key was pressed, at which time the 4023 sends an End Code and performs a carriage return function.

The first character of the computer response is an LF (line feed) code that positions the cursor down one line. Thus combined with the carriage return executed by the Terminal, the cursor is positioned to the first character position of a new line. Computer response continues. . .


Fig. 1-12. Buffer transmission illustration.

If the software does not provide an ETX at the end of this message, the operator may store a Message Separator by simultaneously pressing the RESET and CR keys. The CR stores but is not executed. This provides a Message Separator between the computer response and the following buffer entry. As with the ETX code, the storing of CR displays a visible retangular block. This Message Separator marks the beginning of text for the next message to be entered by the operator.

SEND KEY ENTRY. The SEND key can also be used to initiate buffer entry. However, it will not store a Message Separator; the message to be sent is controlled by existing Message Separators. As when the ENTER key is pressed, buffer entry is from the preceding Message Separator (or home). If no Message Separator was previously stored at the cursor location prior to pressing SEND, cursor movement continues to the last character position of the last line. The Terminal then transmits an End character and executes a carriage return.

USE OF MESSAGE SEPARATORS. Figure 1-13 shows how the Message Separators can be used to input specific data. Assume that the string of data shown is a computer
response to the Terminal. The operator wishes to input back to the computer a specific line (or lines). Using the cursor position keys, the cursor is positioned to the beginning of the data that is to be input, at which point a CR is stored by simultaneously pressing RESET and RETURN. Next, by using the cursor position controls, the cursor is positioned at the end of the data to be input. Pressing ENTER causes an ETX to store. The data, bracketed by the two message separators (CR and ETX), is then transmitted.

## BUFFER FORM FILL-OUT ENTRY

Any Field Attribute Code stored in memory sets the Buffer Form Fill-Out Mode. When Terminal logic receives the US control character, logic is set to interpret the next character received as being a Field Attribute Code (FAC). This mode is normally used when inputting form information to the computer. Fig. 1-14 illustrates a form that might be used by a bank. The illustrated square symbol that precedes each data field symbolizes the position in Terminal memory occupied by the Field Attribute Code. The Field Attribute Code identifies the data field that follows. If no other field codes appear in the line, the field extends to the end of the line. When no field codes appear in a line


Fig. 1-13. Using Message Separators for selective input.
of data, the input circuits interpret the line as containing normal (transmittable alphanumeric) data.

Note the character that appears in the character space preceding each field. These characters represent the Field Attribute Code and are not normally visible. However, Fig. 1-14 illustrates the codes and the position in memory that each occupies. Fields identified by the code for the ASCII " N " specify that all data extending to the next FAC (or to the end of the line, if no other field codes exist in the line) as protected, non-transmittable data. The operator cannot alter the data, (unless RESET is pressed). This data is normally the form heading information that resembles the source document. Those fields identified by the code for the ASCII "@" character contain data that is transmittable and unprotected. Data in these fields can be altered and transmitted. Both alpha and numeric data can be input to these fields. Fields identified by the code for the ASCII " A " character contain data that is transmittable, non-alpha only. (Only those characters that reside in columns 2 and 3 of the ASCII Code chart can be keyed into a non-alpha field.) Alpha data cannot be entered into these fields from the keyboard unless the RESET key is held down while simultaneously entering alpha data. Those
fields identified by the code for the ASCII " $\Lambda$ " character blank the line up to the next FAC, or the end of line.

## NOTE

The computer can write anywhere regardless of fields.

TRANSMITTING FORM FILL-OUT DATA VIA ENTER. With the form displayed, the operator can key the input data into memory, or change the input data already displayed. If necessary, all input data can be cleared by pressing the ERASE INPUT key, or just one input field can be cleared (or part of an input field can be cleared by using the ERASE TO END key). The operator can use the TAB key to move the cursor from one input field to the next. When all necessary inputs have been keyed into memory, the operator can press the SEND-ENTER key (without SHIFT).

The ENTER transmission sequence is used for normal form up-dating when FAC's are in memory. No ETX is stored when ENTER is pressed. Thus, no matter the cursor position, all input data can be entered. The cursor moves


Fig. 1-14. Typical business form application for Field Attribute Codes.
backward through the text, seeking a previously stored Message Separator or the home position, and the KEYLOCK indicator becomes lighted. When the system is ready to accept the data, the cursor moves through the text, causing transmittable data only to be entered to the computer. When the cursor reaches another previously stored Message Separator or the last line, last character position, an End character is transmitted, and the Terminal transmits the End character and performs a carriage return, positioning the cursor to the left margin on the 24th line. The KEYLOCK indicator goes out, signifying that the transmittable data has been entered.

TRANSMITTING FORM FILL-OUT DATA VIA SEND. Pressing the SEND key in Buffer Form Fill-Out Entry performs functions similiar to the ENTER key, except that all data (non-transmittable and transmittable) is input. The Send transmission function in Form Fill-Out can be used for programming or for storing a newly generated form onto a medium (such as a magnetic storage device) for later call-up.

NOTE
In Form Fill-Out operations, previously stored Message Separators are honored.

## NUL SUPPRESSION

NUL characters reside in memory when the Terminal is turned on, or the screen is erased. NUL's are not transmitted during an Enter or a Send transmission sequence. This causes the transmitted message to be "compacted". If the memory has been entered to a storage medium, it will be read back in its "compacted" state. In other words, because the NUL's were suppressed when reading to the storage medium, no spacing is provided for later read-back to the Terminal. Therefore, where spacing between lines and characters is important (such as with formatted displays), use SP (SPACE) characters as required. The SP character can be transmitted, and when read back to the Terminal, will provide the necessary spaces between lines and characters.

## CHARACTERISTICS

## INTRODUCTION

The characteristics are contained in two parts. The first part consists of an alphabetic listing. The alphabetic listing makes reference to the second part, which contains tabulated information.

The following conditions must be met before all characteristics can be considered valid:

The Terminal must have been adjusted at an ambient temperature between $+20^{\circ} \mathrm{C}$ and $+30^{\circ} \mathrm{C}$.

It must be operating in an environment as specified under Environmental Specification.

Operation must be preceded by a warmup period of at least 20 minutes.

Specified power requirements must be met.

The following tables and illustrations are included immediately after the alphabetic listing of characteristics:
Accessories
Code Effect
Data Coding
Data Transfer
Display (Monitor) Specifications
Editing Specifications
Environmental Specifications
Field Attribute Codes
Physical Specifications
Power Supply Specifications
Reset Key Effects
Strappable Options for the
Standard Terminal
Timing Specifications
Ruling Characters
ASCII Code Chart

Table 2-1
Table 2-2
Table 2-3
Table 2-4
Table 2-5
Table 2-6
Table 2-7
Table 2-8
Table 2-9
Table 2-10
Table 2-11

Table 2-12
Table 2-13
Figure 2-1
Figure 2-2

The following characteristics are contained in the Alphabetic Listing:

| Accessories | Field Attribute Codes (FAC) |
| :---: | :---: |
| Address | Field Attribute Code |
| Arming | Transmission |
| Bit 8 and Bit 9 | Formatted Display |
| Blink Cursor Strap | Full Page Feature |
| Buffer | Hard Copy Mode |
| Buffer Transmission | Home Position |
| Carriage Return | Interface Specification |
| Character Effect on Terminal | Keyboard |
| Character Generation | Keyboard Lock Conditions |
| Character Matrix | Line, Character |
| Characters Per Display | LF DOES CR Strap |
| Characters Per Line | Line Feed |
| Character Size | Local Operation |
| Character Transmission | Memory Specifications |
| Character Transmission of | Message End Strap |
| Field Attribute Co | Message Separator |
| Character Transmission in | Minibus (also Motherboard) |
| Read Cursor O | Monitors |
| Character Type | Non-Alpha Fields |
| Character Writing | NUL's |
| Character Writing Inhibit | Numeric Pad |
| Characters, Lower Case | Operating Features |
| Characters, Ruling | Options, Strappable |
| Clock | Page Full |
| Composite Video | Physical Specifications |
| Console Lock Strap | Position Cursor Operation |
| Control Character | Power Supply Specification |
| Control Character Sequence | Read Cycle |
| Control Character Storage | Read/Write Cycle |
| Control Character Transmission | Prompt Mode Strap |
| CR Does LF Strap | Receive Rate |
| Cursor | Resetting Optional Rulings to |
| Cursor Addressing | Initial Conditions |
| Cursor Reading | Read Cursor Operation |
| Data Transfer | Resetting Home Position |
| Data Transfer Rate | Roll-Up |
| Direct Transmission | Rulings Character Set |
| Display and Logic Timing | Send Transmission Sequence |
| Display Size | Space |
| Display Cycle | Storage, Control Character |
| Display Controls | Strappable Options |
| Display Memory | Timing |
| Display Unit Specifications | Transmission |
| Echo | Transmission, Computer- |
| Editing Specifications | Initiated |
| End Character | Transmission, Cursor Reading |
| Enter Transmission Sequences | Transmission Rate |
| Environmental Specifications | Video |
| EOL LF GEN Strap | Wrap-around |

## ALPHABETIC LISTING

ACCESSORIES. See Table 2-1.

ADDRESS. A display position with reference to a grid of 80 by 24 characters with the 0,0 address being at top left (also known as the first character position). Address is synonymous with Position Cursor and Read Cursor functions.

ARMING. Certain functions at the Terminal require a control sequence whose first character "arms" the Terminal, permitting the next character to perform a function other than what it would do if the Terminal were not armed. ESC is normally used as the arming command. The execution commands are listed under "Character Effect on Terminal." In addition, accessory devices may use other execution commands as explained in the accessory device instruction manual.

## BIT 8 AND BIT 9. See Table 2-3.

BLINK CURSOR STRAP. See Strappable Options, Table 2-12.

BUFFER. See Display Specifications, Table 2-5.

BUFFER TRANSMISSION. See Transmission, Buffer.

CARRIAGE RETURN. Return of cursor to the left margin occurs on receipt of CR or ESC FF; on receipt of LF (if it is strapped on Keyboard Interface Card to also perform a carriage return); by initializing or pressing PAGE-ERASE INPUT key or HOME key; or when wraparound occurs when spacing past the last character position in a line.

CHARACTER EFFECT ON TERMINAL. Terminal recognizes characters contained in ASCII code, except for those not listed in the Code Effect Table. All alphanumeric and ruling characters except space and delete (RUBOUT) result in character writing and subsequent spacing. Space does not write visibly but is stored in memory and causes spacing; delete causes neither writing nor spacing. Control characters and control character sequences are decoded and perform specific functions as shown in Table 2-2. Additional use of control characters or control character sequences may be made by accessory devices connected through circuit cards to the Terminal minibus.

CHARACTER GENERATION. The standard Terminal contains 24 lines of 80 characters each, for a total of

1920 characters. The Terminal uses 262 non-interlaced horizontal sweeps of video to generate the display. Of the 262 lines, 22 lines are blanked. This allows 10 video sweeps per character line, thus a character line can be referred to as 10 video lines. To allow spacing between lines of alphanumeric characters, only 7 of the 10 video sweeps are used (lower case uses 8 video lines). Some of the optional ruling characters use all 10 video sweeps, in addition to filling in the space between ruling characters with video. This permits solid lines to be displayed for charts, graphs, and forms. Fig. 6-3 in the Circuit Description shows the relation between the character generator and the video sweeps. The upper left-hand corner of the display is illustrated, with character position 0,0 being the home position. The crt electron beam sweeps video line 0 of character line 0 , retraces, then sweeps video line 1 of character line 0 , displaying information as commanded by the logic and video circuitry. The beam retraces and continues sweeping, displaying video one sweep at a time. Note that Fig. 6-3 provides an illustration of character generation for both alpha and optional ruling characters.

CHARACTER MATRIX. Characters in columns 2 through 5 of the ASCII code chart use a $5 \times 7$ dot matrix pattern to provide write information to the Terminal logic and video circuits. The lower case and optional ruling characters use a 5 by 8 dot matrix. This matrix is "spread" to a $7 \times 10$ dot matrix for ruling character generation.

CHARACTERS PER DISPLAY. See Display Specifications Table 2-5.

CHARACTERS PER LINE. 80 Characters per line.

CHARACTER SIZE. Limits determined by width and height adjustments. Nominal size, 80 by 120 mils.

CHARACTER TRANSMISSION. Depending upon the operation selected, the code for ASCII or TTY characters can be transmitted from the keyboard in response to a key, in response to a SHIFT and key combination, or in response to a CTRL SHIFT and key combination. RUBOUT sends the code for DEL. BIT 8 is sent normally high, or as determined by the data communication interface in use. The Motherboard can accept any eight-bit combination from accessory units for transmission to the computer.

CHARACTER TRANSMISSION OF FIELD ATTRIBUTE CODES. See Field Attribute Code Transmission.

CHARACTER TRANSMISSION IN READ CURSOR OPERATION. A sequence of characters is transmitted to the computer in response to a control character sequence from the computer. See Read Cursor Operation for details.

CHARACTER TYPE. The standard character type used on the Terminal display is ASCII. Optional ruling characters can be provided to display orthogonal characters for drawing charts, graphs, etc. If the Terminal has the optional rulings ability, the Terminal initializes with ASCII selected, and returns to ASCII in response to a Reset or Clear Page function; program selection for ASCII or rulings characters occurs in response to SI and SO , respectively $\left({ }^{C} \mathrm{~N}\right.$ and ${ }^{C} \mathrm{O}$ from keyboard).

> NOTE
> A superscript " C " (and sometimes "s ") precedes an alpha to designate the simultaneous pressing of the CTRL (and SHIFT) and character keys, when keying control characters for the keyboard.

CHARACTER WRITING (KEYBOARD). The Terminal has writing capability for all ASCII characters. Since TTY is a subset of ASCII, TTY writing capability is included.

CHARACTER WRITING INHIBIT. See Keyboard Lock Conditions.

CHARACTERS, LOWER CASE. Lower case ASCII characters are accepted and written. Lower case letters cannot be transmitted from the keyboard while the TTY LOCK key is depressed.

CHARACTERS, RULING. An Optional character set that, when selected by the proper code, permits ASCII code to select specific ruling characters. This character set is accessed by SO ( ${ }^{\mathrm{C}} \mathrm{N}$ from keyboard). The ASCII character set is reselected by SI (C ${ }^{\text {C }}$ from keyboard). See Fig. 2-2 for illustration of available ruling characters.

CLOCK. See Timing Specifications, Table 2-13.

COMPOSITE VIDEO. Similar to RS 330. Nominal source impedance and termination impedance is 75 ohms. Visible video is two-tone, white and gray.

CONSOLE LOCK STRAP. See Strappable Options Table 2-12.

CONTROL CHARACTER. See Character Effect on Terminal.

CONTROL CHARACTER STORAGE. Control characters keyed in from the keyboard or sent by the computer are not normally stored in Terminal memory; they are simply performed. Control characters (other than ETX) that are computer originated can never be stored. However, control characters can be stored from the keyboard by simultaneously holding down the RESET key when keying in the control character. RESET does not prevent HT, VT, ESC, FS, and US from being executed.

CONTROL CHARACTER TRANSMISSION. Control characters (excluding CR, NUL, and ETX) can be transmitted when stored in memory. When a control character is stored in memory, its position is indicated by a displayed block of about cursor size, at its respective position on the display. CR, LF, and BS are not executed when entered into memory with RESET. Only one-half of the control characters can be displayed. If Bit 1 of the control character is true, then the control character can be displayed.

CR DOES LF STRAP. See Strappable options, Table 2-12.

CURSOR. A seven-by-ten dot matrix which indicates the current writing position.

CURSOR ADDRESSING. See Position Cursor Operation.

CURSOR READING. See Read Cursor Operation.

DATA TRANSFER. See Data Transfer, Table 2-4.

DATA TRANSFER RATE. Interface dependent; limited to a maximum input/output (I/O) rate of 15720 characters per second. However, internal data transfer operations for editing and clear page functions are performed at 94,320 characters per second. This is known as Fast I/O. Fast I/O can be strapped to the input/output by strapping the Fast I/O strap on the Timing card. See Table 2-12 for more strap information.

DIRECT TRANSMISSION. This transmission mode is set when the DIRECT/BUFFER switch is set to DIRECT. Transmission is "direct" from keyboard. If keyboard entries are to be displayed, an echo condition must exist. (See Echo.)

DISPLAY AND LOGIC TIMING. See Table 2-13.

DISPLAY SIZE. See Display Specifications, Table 2-5.

DISPLAY CYCLE. While video is unblanked, data is read from the memory along with memory read cycles, and sent to the character generator, a shift register, and on to the screen as video.

DISPLAY CONTROLS. Operator display controls include brightness and contrast.

DISPLAY MEMORY. See Display Specifications, Table 2-5.

DISPLAY SPECIFICATIONS. Refer to Table 2-5.

ECHO. Consists of executing data at the Terminal as the data is being sent to the computer with DIRECT selected. Echoing can be caused by placing an ECHO command on the minibus, usually from the interface unit.

## EDITING SPECIFICATIONS. See Table 2-6.

END CHARACTER. The last character in a message transmitted from the Terminal buffer. Strappable options on the Control Card allow any ASCII control character to be used as the End Character. Standard End Character is strapped to be CR. See Strappable Options, Table 2-12.

ENTER TRANSMISSION SEQUENCE. Normally used with BUFFER selected to transmit from one character to a full page of characters. Normal Sequence is:

Without Formatted Display

1. Set DIRECT/BUFFER switch to BUFFER.
2. Key in from keyboard necessary information.
3. Position cursor at end of data to be transmitted.
4. Press SEND-ENTER key; response is. . .
a. Message Separator (ETX code) is entered into memory at the cursor location.
b. Cursor moves to the home position or previously stored Message Separator.
c. Cursor moves at selected baud rate over data that is subsequently transmitted.
d. At end of each line a CR is transmitted. LF's can also be transmitted by placement of EOL LF GEN strap on Control Card.
e. Cursor reaches Message Separator, transmits the End character (CR is standard-can be strapped to be
any ASCII control character), and performs a carriage return to position cursor at left margin of last line transmitted.

## With Formatted Display

Same as above except ETX is not entered into memory, and only transmittable data residing between existing Message Separators is transmitted. If no Message Separators reside in memory, all displayed data is input.

Environmental Specifications. See Table 2-7.

EOL LF GEN Strap. See Strappable Options, Table 2-12.

FIELD ATTRIBUTE CODES (FAC). Field Attribute Codes (FAC's) are used to arrange displayed data as to its appearance, its transmission, and its protection. The FAC defines the field on the display and is stored in Terminal memory in the first character position of the field. It is protected from keyboard replacement regardless of the protection status of the field it defines. (Simultaneously pressing RESET will allow another character to be keyed over the FAC. Edit functions such as delete line and delete character will erase FAC's.) The field continues from the location of the FAC until another FAC or the end of the line is encountered.

FIELD ATTRIBUTE CODE TRANSMISSION. When data fields are transmitted, the US control character precedes the Field Attribute Code. US signals the program that the next character is a Field Attribute Code.

FORMATTED DISPLAY. Displayed data that has been specially arranged to resemble (for most purposes) a source document, can be set up through use of Field Attribute Codes. Field Attribute Codes are used to identify data in a line. One FAC can identify from 1 to 79 characters (the FAC occupies a character space in memory). Table 2-8 shows the available FAC's.

FULL PAGE FEATURE. A page full of data can be rapidly entered into memory and displayed by simultaneously holding down the PAGE-ERASE INPUT, SHIFT, and any character key, then, while still holding down the character key releasing the other two keys.

HARD COPY MODE. Permits copying of the Terminal display memory by a Hard Copy Unit. This mode is activated by a COPY switch on the Terminal keyboard, a Hard Copy unit, or by program command (ESC ${ }^{\mathrm{C}} \mathrm{G}$ ).

HOME POSITION. Top left corner of display that corresponds to the first character position on the first line. Cursor moves to that position upon initialization and upon receiving ESC FF. It also moves there by a Clear Page function, Erase Input function, or by pressing the HOME key.

INTERFACE SPECIFICATION. See documentation pertaining to specific interface unit.

KEYBOARD. 64/96 ASCII upper and lower case with auto repeat for any keys held down for more than 0.5 second.

KEYBOARD LOCK CONDITIONS. The keyboard is prevented from inputting to the Terminal buffer under the following conditions:

1. A message from the computer is pending or is in progress.
2. The cursor is positioned over a Field Attribute Code.
3. The cursor is positioned in a protected field.
4. When attempting to enter an alpha character into a non-alpha field.

LINE, CHARACTER. Consists of 80 character spaces. Data lines are made of ten horizontal video sweeps; seven for character display and three for spacing between lines. Some optional ruling characters use all ten video sweeps for character generation.

LF DOES CR STRAP. See Strappable Options, Table 2-12.

LINE FEED. Moves writing beam down one line. Occurs upon receipt of LF from keyboard or program. Standard Terminal configuration performs a line feed upon receipt of a CR. LF can also be strapped to simultaneously perform a CR. See both LF DOES CR and CR DOES LF straps in Table 2-12.

LOCAL OPERATION. Off-line operation used principally for operator training, formatting of data, equipment maintenance, and when data processing functions are with Terminal auxiliary units only. Local operation is selected by the LOCAL/ON LINE switch at the keyboard, and isolates the Terminal from the computer.

MEMORY SPECIFICATIONS. See Display Specifications, Table 2-5.

MESSAGE END STRAP. See Strappable Options, Table 2-12.

MESSAGE SEPARATOR. Storing the ETX or CR codes in memory provides a "message separator" for data entry purposes. Initiating an Enter sequence stores the ETX code at the cursor location. Message Separators are not stored when FAC's reside in memory. However, there are exceptions to this rule. See Table of Reset functions, Table 2-11.

MINIBUS (ALSO MOTHERBOARD). This board makes identical signals available at each of the board-edge connectors. See Dictionary of Line Titles and Wire List in Section 6 for details.

MONITORS. The 75 ohm monitor output connector is located on the Terminal back panel and provides composite video for monitors. The number of monitors to which the Terminal can provide acceptable video depends on the type of monitor, the distance to the furthest monitor, and the type of connecting cable used.

NON-ALPHA FIELDS. Fields into which only those characters listed in columns 2 and 3 of the ASCII Code Chart are normally entered. See ASCII Code Chart in Fig. 2-2.

NUL'S. NUL control characters reside in memory in those character spaces where data is not entered. NUL's are skipped during transmission to decrease transmitting time. Functions such as Clear Page, Erase, Input, Erase to End, Delete Character, and Delete Line enter NUL's into memory.

NUMERIC PAD. The cluster of 12 keys on the right of the keyboard provide a 10 key numeric input pad. This is in addition to their primary functions as explained in individual switch descriptions in Section 1. The NUM LOCK key initializes the numeric functions; NUM LOCK must be pressed again to re-establish the normal functions.

OPERATING FEATURES. Character Generation, Position Cursor, Read Cursor, Field Formatting, and Hard Copy Operation. See individual operating descriptions for details.

OPTIONS, STRAPPABLE. See Table 2-12 for strappable options for the basic Terminal; see Interface Unit documentation for strap options information pertaining to interface units.

PAGE FULL. A condition with BUFFER selected that occurs when line feeding past the 24th line that causes a Terminal busy (TBUSY) signal.

PHYSICAL SPECIFICATIONS. See Table 2-9.

POSITION CURSOR OPERATION. An operating feature initiated by sending FS followed by $X$ and $Y$ address codes. This feature permits cursor addressing to any character position in memory.

POWER SUPPLY SPECIFICATION. See Table 2-10.

READ CYCLE. 636 nanoseconds long.

READ/WRITE CYCLE. 1.9 microseconds long.

PROMPT MODE STRAP. See Strappable Options, Table 2-12.

RECEIVE RATE. Capable of 15,720 characters per second.

RESETTING OPTIONAL RULINGS TO INITIAL CONDITIONS. If the Optional character set has previously been selected, the standard character set is reselected by sending SI ( ${ }^{\text {C }} \mathrm{O}$ from keyboard) or by pressing either the RESET key or the PAGE-ERASE INPUT key at the keyboard.

READ CURSOR OPERATION. See Transmission, Cursor Reading.

RESETTING HOME POSITION. The Terminal resets to home position (top-left of display area) in response to ESC FF from the computer. Home position also occurs when PAGE (Clear Page function), HOME, or ERASE INPUT is entered at the keyboard.

ROLL-UP. Roll-up occurs in DIRECT with a line feed past the bottom line of the display. All lines roll-up one line, with the top line rolling off the page. A new line is then available at the bottom on which to enter new data.

RULINGS CHARACTER SET. An optional character set that provides 32 "ruling" characters for drawing charts, forms, etc. This set is accessed by SO; SI reselects the normal character set. RESET or PAGE from the keyboard also reselects the normal character set.

SEND TRANSMISSION SEQUENCE. Similar to Enter Sequence. Variations are:

1. Initiated by simultaneously pressing the SHIFT and SEND-ENTER keys.
2. No Message Separator Stores at the cursor location.
3. With non-formatted displays, all data is transmitted to computer; unless Message Separators have previously been stored, in which case they are honored.
4. With formatted displays, all data (transmittable and non-transmittable) is transmitted. However, existing Message Separators are honored.

SPACE. The area in a line that is indicative of the respective character position in memory. There are 80 spaces per line and a total of 1920 characters per display.

STORAGE, CONTROL CHARACTER. See Control Character Storage.

STRAPPABLE OPTIONS. Optional operating features which can be selected by connectors within the Terminal. See Table 2-12.

TIMING. See Timing, Table 2-13.

TRANSMISSION. See Transmission sequence in question; Direct, Enter Sequence, Send Sequence, Transmission, and Cursor Reading Transmission.

TRANSMISSION, COMPUTER INITIATED. The computer can initiate transmission of buffer contents via one of two sequences, Send All or Send Transmittable Only. Send All is initiated when the Terminal receives ESC SO. All data whether defined by Field Attribute Codes as transmittable or not, is sent. Send Transmittable Only is initiated when the Terminal receives ESC SI. Data defined by Field Attribute Codes as transmittable, is sent, as is data not defined by a FAC.

TRANSMISSION, CURSOR READING. Data is transmitted as a series of bytes in response to an ESC ] from the computer. The sequence of transmitted data from the Terminal is GS, $\mathrm{X}, \mathrm{Y}, \mathrm{END}$. GS is the ASCII control character that identifies the following two bytes ( X and Y ) as cursor position data. X is the code for the character position in a line ( 0 through $79+32$ ) and $Y$ is the line number ( 0 through $23+32$ ). End is the character that marks the end of transmission and is usually strapped to be CR .

TRANSMISSION RATE. Interface dependent. See documentation pertaining to the specific interface unit. Also see Data Transfer Rate.

WRAP-AROUND. A Terminal feature that causes an automatic carriage return/line feed to be performed when moving the cursor past the 80th character position.

VIDEO. See Composite Video.

TABLE 2-1
ACCESSORIES

| ITEM | TEKTRONIX PART NUMBER |
| :--- | :---: |
| Standard Accessories |  |
| Standard Data Communications Interface | $021-0111-00$ |
| Standard Data Communications Interface Instruction Manual | $070-1613-00$ |
| 4023 Users Manual | $070-1621-00$ |
| Optional Cabinet Colors |  |
| Red | $390-0340-07$ |
| Green | $390-0340-08$ |
| Gold | $390-0340-04$ |
|  |  |
| Optional Accessories |  |
| 4023 Service Manual | $070-1617-00$ |
| Optional Data Communications Interface | $021-0112-00$ |
| 4023 Pedestal (stand only) | $016-0568-00$ |
| Logic Extender Card (includes extender cable kit) | $067-0659-00$ |
| $72-$ Pin Extender Card (includes extender cable kit) | $067-0696-00$ |

TABLE 2-2
CODE EFFECT

| ASCII CONTROL <br> CHARACTER | KEYBOARD KEY <br> COMBINATION | RESPONSE |  |
| :--- | :--- | :--- | :---: |
| ETX $\left(3_{10}\right)$ | $c_{\text {C (normally not keyed }}$ <br> from keyboard) | End Of Text. Functions as a Message Separator when <br> stored in the buffer. It is stored when the computer outputs <br> the ETX to the Terminal as the last character of the <br> computer transmission, or when the operator types CTRL <br> C or presses the ENTER key with non-formatted displays. <br> Storage is suppressed from the keyboard if there are any <br> Field Attribute Codes in memory. |  |
| BEL $\left(7_{10}\right)$ |  |  |  |

TABLE 2-2 (cont)
CODE EFFECT (cont)

| ASCII CONTROL CHARACTER | KEYBOARD KEY COMBINATION | RESPONSE |
| :---: | :---: | :---: |
| SINGLE CHARACTER COMMANDS (cont) |  |  |
| $\text { BS }\left(8_{10}\right)$ <br> Backspace | ${ }^{\mathrm{C}} \mathrm{H}$ | Backspace-a format effector. Moves the cursor to the left one character. If the cursor is already at the left margin, the BS command has no effect. |
| $\begin{aligned} & \text { HT }\left(9_{10}\right) \\ & \text { TAB } \end{aligned}$ | $c_{1}$ <br> or TAB key | Horizontal Tabulate-a format effector. In Buffer mode with formatted displays, HT tabs the cursor one character space beyond the FAC that describes an unprotected field. Used to tab the cursor from one field (any field) into the next input field. If no input field is available, the cursor returns to the Home position. <br> When no Field Attribute Codes are stored (in DIRECT), HT performs a non-destructive direct space, i.e. moves cursor right one space. |
| $\operatorname{LF}\left(10_{10}\right)$ <br> Line Feed | c J or LF key | Line feed-a format effector. In Buffer operations, LF performs a line feed by moving the cursor down one line. It does not affect the horizontal position of the cursor unless strapped to give a CR with LF (see Strappable Options). An LF past the 24th line will cause the screen to roll up one line. If in Direct, LF's can be executed depending on mode configuration (see Strappable Options). |
| $\mathrm{VT}\left(11_{10}\right)$ | $c_{K}$ | Vertical Tab-a format effector. Performs a "back tab" function-the reverse of the HT function. If no input field is found, the cursor goes to the home position. Performs no function in DIRECT. |
| CR ( $13_{10}$ ) <br> Carriage Return | ${ }^{C} M$ | Carriage Return-a format effector. Moves the cursor to the first character position at the left margin. Can be strapped to provide a line feed with carriage return, thus establishing a new line at the left margin. Various effects to and from a CR are provided by strappable options. Can also be stored in memory for use as a Message Separator by having the operator simultaneously press RESET with RETURN. |
| SO ( $14_{10}$ ) <br> Rulings Set Select | ${ }^{\mathrm{c}} \mathrm{N}$ | Shift Out-Selects the optional (rulings) character set. |
| $\operatorname{SI}\left(15_{10}\right)$ <br> Standard Set Select | ${ }^{\mathrm{c}} \mathrm{O}$ | Shift In-Selects the standard character set if the optional character set has previously been selected. |

TABLE 2-2 (cont)
CODE EFFECT (cont)

| ASCII CONTROL CHARACTER | KEYBOARD KEY COMBINATION | RESPONSE |
| :---: | :---: | :---: |
| SINGLE CHARACTER COMMANDS (cont) |  |  |
| $\operatorname{ESC}\left(27{ }_{10}\right)$ <br> Arming Command | ESC key or ${ }^{C S}$ K | First character of a special two-character sequence. ESC "arms" the Terminal to interpret the next character received (regardless of its normal function) as a special control or function. (See ESC BEL, ESC FF, ESC SO, ESC SI, ESC O, and ESC ].) The Character following ESC causes $\overline{\text { CBUSY }}$ to go active for 0.5 sec . Fast response would limit $\overline{\text { CBUSY }}$ to 60 ms . (See ESC Character Delay in Programming Considerations and also FAST RESPONSE strap under strappable options.) |
| $\operatorname{FS}\left(28_{10}\right)$ <br> Set Cursor <br> Addressing Mode | ${ }^{\text {cs }}$ L | Sets the Cursor Addressing Mode. When followed by the proper address codes, the cursor can be positioned to any character position on screen. |
| US ( $311_{10}$ ) <br> Field Separator <br> (Field Attribute <br> Code Substitute) | $\mathrm{cs}_{\mathrm{O}}$ | Performs two functions: <br> 1) Used in Buffer Form Fill-Out transmission sequences as a Field Segregator. The US code precedes the Field Attribute Code on the data string to identify the input data that follows as having been preceded by a FAC in Terminal memory. <br> 2) When the Terminal receives a US code, Terminal logic is set to interpret the next character received as a Field Attribute Code. |

TWO CHARACTER COMMANDS

| ESC BEL | $E^{\prime} C^{\prime} G$ | Used to trigger a hard copy of the displayed data when <br> using a Hard Copy Unit. ESC BEL is the computer <br> addressed equivalent of the COPY button on the Terminal <br> or Hard Copy Unit. The Hard Copy Unit can receive and <br> print video (except for blink) onto paper. Multiple copies <br> can be obtained under program control by commanding a <br> copy to be made and immediately following it with the <br> Read cursor command (ESC ]). The action of making a <br> copy delays the reading of the cursor until the copy is <br> completed. When the Terminal responds with the cursor <br> location, the program can use this as signifying that the <br> copies is ready for another command. |
| :--- | :--- | :--- |

TABLE 2-2 (cont)
CODE EFFECT (cont)

| ASCII CONTROL CHARACTER | KEYBOARD KEY COMBINATION | RESPONSE |
| :---: | :---: | :---: |
| TWO CHARACTER COMMANDS (cont) |  |  |
| ESC FF <br> Clear Page | $E S C{ }^{c} L$ | Clear screen command. Performs same function as PAGE. The screen is cleared, cursor positions to Home and all Terminal logic is initialized. |
| ESC SO <br> Send Page | $E S C{ }^{\text {c }} \mathrm{N}$ | Initiates a send function. Causes all fields, normally transmittable or not, from the beginning to end of text, to be transmitted to the computer. If fields are contained on the display, the Field Attribute Codes are preceded by the US $\left(31_{10}\right)$ character. When transmission of all data is completed (including ruling characters, if any), the cursor resides in the left-most character position on the last line of the message. |
| ESC SI (i.e. <br> Send Transmittable Only) | ESC ${ }^{\text {c }} \mathrm{O}$ | Performs the same functions as ESC S0 with the exception that only transmittable fields are transmitted. (Rulings are not transmittable.) |
| ESC O <br> (Same as ERASE INPUT key) | ESC O | Initiates the clear input sequence. Sets all unprotected data fields to NUL characters. Used in the Buffer Form Fill-Out Mode when it becomes necessary to clear the input data only (does not clear rulings). Do not confuse with the Clear Page Function. If FAC's or rulings are not present, the effect is the same as Clear Page. |
| ESC ] <br> Set Read <br> Cursor Mode | $\begin{aligned} & \text { ESC ] } \\ & \left.(]=93_{10}\right) \end{aligned}$ | Initiates the Read Cursor Mode. Causes cursor coordinates to be transmitted to the computer. |

TABLE 2-3
DATA CODING

| DATA LINK | BITS |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| ASCII DATA LINK |  | $8^{1}$ | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| BINARY TELETYPE |  | $8{ }^{2}$ | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| MOTHERBOARD WITH SEND $\overline{8}$ TRUE |  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| MOTHERBOARD WITH MEMORY NORMAL | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

Normally, Bit 8 is for use internal to the 4023 and is not related to parity or used for binary data. Bit 9 is also for internal use. Bits 8 and 9 together tag the other 7 bits as follows:

| BIT 9 | BIT 8 | Bits 1-7 are: |
| :---: | :---: | :--- |
| 0 | 0 | Normal ASCII Character |
| 0 | 1 | Field Attribute Code |
| 1 | 0 | Alternate Character |
| 1 | 1 | Invalid |

TABLE 2-4
DATA TRANSFER

| SWITCH POSITION | KEYBOARD DATA TRANSFER |  |  | BUFFER DATA TRANSFER ${ }^{3}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | DIRECT |  | BUFFER | DIRECT | BUFFER |
|  | WITHOUT ECHO | WITH ECHO |  |  |  |
| LOCAL | Peripheral | Peripheral and screen | Screen | Peripheral | Peripheral |
| ON LINE | Computer | Computer and screen | Screen | Computer | Computer |

[^0]TABLE 2-5
DISPLAY (MONITOR) SPECIFICATIONS

| CRT | TV type, 12" diagonal measurement. |
| :---: | :---: |
| Screen Size | $10.5{ }^{\prime \prime}$ by $8^{\prime \prime}$. |
| Deflection | Electromagnetic, raster scan. |
| Video | Composite video that can drive 525-line, TV-type broadcast monitors. |
| Character Generator | $5 \times 7$ dot matrix read only memory for upper case; $5 \times 8$ dot matrix read only memory for lower case and optional ruling characters. |
| Refresh Buffer | $2048 \times 9$ bits standard 24 line MOS RAM. $1024 \times 9$ bits optional 12 line MOS RAM. |
| Refresh Rate | 60 Hz for each dot (frame rate equals field rate of 60 Hz ). This can be strapped in Terminal for 50 Hz operation. |
| Intensity | Normal video, 30 foot lamberts; dim video, 15 foot lamberts. |
| Resolution <br> Display Center <br> Display Corner | TV lines measured in accordance with EIA RS-375 and is adjusted for 100 percent. <br> 750 lines. <br> 650 lines. |
| Geometry | Not more than $2 \%$ of active raster height. |
| Retrace and Delay Times <br> Vertical Retrace <br> Horizontal Retrace <br> Horizontal Delay | $900 \mu \mathrm{~s}$ maximum. <br> $7.0 \mu \mathrm{~s}$ maximum. <br> $4.0 \mu \mathrm{~s}$ maximum. |

TABLE 2-6

## EDITING SPECIFICATIONS ${ }^{4}$

| FUNCTION | RESULT |
| :--- | :--- |
| Insert Character | A space is entered at the cursor position. All data from the cursor position moves right, <br> leaving a space at the cursor position. Only the line where the cursor resides is affected. |
| Delete Character | The character where the cursor resides is deleted or replaced by a new character typed <br> from the keyboard. |
| Insert Line | The line where the cursor resides and all lines below move down one line for each key <br> depression. The bottom line is lost. |
| Delete Line | The line where the cursor resides is deleted and all lines below move up one line for each <br> key depression. |
| Erases all unprotected information on the screen and positions the cursor to home. |  |

TABLE 2-7
ENVIRONMENTAL SPECIFICATIONS

| Ambient Temperature | $+10^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$ |
| :--- | :--- |
| Operating | $-40^{\circ} \mathrm{C}$ to $+65^{\circ} \mathrm{C}$ |
| Storage | $5.0 \%$ to $80 \%$ (noncondensing) |
| Humidity | Unless otherwise specified, $+25^{\circ} \mathrm{C}$; humidity not greater than $55 \%$. |
| Inspecting and | to 50,000 feet |
| Testing Conditions | to 15,000 feet |
| Altitude |  |
| Non-operating |  |

[^1]TABLE 2-8
FIELD ATTRIBUTE CODES

| OGIC | TRANSMITTABLE |  |  |  | NON-TRANSMITTABLE |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | UNPROTECTED |  | PROTECTED |  | UNPROTECTED |  | PROTECTED |  |
| DISPLAY <br> EFFECT | ALPHANUMERIC | NON ALPHA | NORMAL | DIM | ALPHANUMERIC | NON ALPHA | NORMAL | DIM |
| White on Black | $\begin{gathered} @ \\ \left(64_{10}\right) \end{gathered}$ | $\begin{gathered} A \\ \left(65_{10}\right) \end{gathered}$ | $\begin{gathered} B \\ \left(66_{10}\right) \end{gathered}$ | $\begin{gathered} C \\ \left(67_{10}\right) \end{gathered}$ | $\begin{gathered} D \\ \left(68_{10}\right) \end{gathered}$ | $\begin{gathered} E \\ \left(69_{10}\right) \end{gathered}$ | $\begin{gathered} F \\ \left(70_{10}\right) \end{gathered}$ | $\begin{gathered} G \\ \left(71_{10}\right) \end{gathered}$ |
| Black on White | $\begin{gathered} \mathrm{H} \\ \left(72_{10}\right) \end{gathered}$ | $\begin{gathered} 1 \\ \left(73_{10}\right) \end{gathered}$ | $\begin{gathered} \mathrm{J} \\ \left(74_{10}\right) \end{gathered}$ | $\begin{gathered} K \\ \left(75_{10}\right) \end{gathered}$ | $\begin{gathered} \mathrm{L} \\ \left(76_{10}\right) \end{gathered}$ | $\begin{gathered} M \\ \left(77_{10}\right) \end{gathered}$ | $\begin{gathered} N \\ \left(78_{10}\right) \end{gathered}$ | $\begin{gathered} 0 \\ \left(79_{10}\right) \end{gathered}$ |
| Blinking | $\begin{gathered} P \\ \left(80_{10}\right) \end{gathered}$ | $\begin{gathered} \mathrm{Q} \\ \left(81_{10}\right) \end{gathered}$ | $\begin{gathered} R \\ \left(82_{10}\right) \end{gathered}$ | $\begin{gathered} S \\ \left(83_{10}\right) \end{gathered}$ | $\begin{gathered} \mathrm{T} \\ \left(84_{10}\right) \end{gathered}$ | $\begin{gathered} U \\ \left(85_{10}\right) \end{gathered}$ | $\begin{gathered} V \\ \left(86_{10}\right) \end{gathered}$ | $\begin{gathered} W \\ \left(87_{10}\right) \end{gathered}$ |
| Blanked | $\begin{gathered} X \\ \left(88_{10}\right) \end{gathered}$ | $\begin{gathered} Y \\ \left(89_{10}\right) \end{gathered}$ | $\begin{gathered} Z \\ \left(90_{10}\right) \end{gathered}$ | $\begin{gathered} {[ } \\ \left(91_{10}\right) \end{gathered}$ | $\begin{gathered} / \\ \left(92_{10}\right) \end{gathered}$ | $\begin{gathered} ] \\ \left(93_{10}\right) \end{gathered}$ | $\begin{gathered} \Lambda \\ \left(94_{10}\right) \end{gathered}$ | $\left(95_{10}\right)$ |

To set up a field from the keyboard, key in US ( ${ }^{C S} \mathrm{O}$ ) followed by one of the FAC's listed above. For example, sending ${ }^{\mathrm{cs}} \mathrm{O}$ followed by H sets up an inverted, alphanumeric field that is unprotected and transmittable.

TABLE 2-9
PHYSICAL SPECIFICATIONS

| Weight | About 46.5 lbs. |
| :--- | :--- |
| Shipping Weight | About 67 lbs. |
|  |  |
| Dimensions | About 12.500 inches. |
| Height | About 17.500 inches. |
| Width | About 27.250 inches. |

TABLE 2-10
POWER SUPPLY SPECIFICATIONS

| Line Voltage Ranges | 115 VAC | 230 VAC |
| :--- | :--- | :--- |
| Low | 90 V to 110 V | 180 V to 200 V |
| Med | 105 V to 126 V | 208 V to 252 V |
| High | 112 V to 136 V | 224 V to 272 V |
| Line Frequency Range | 50 Hz to 60 Hz |  |
| Power Consumption | 220 watts maximum at 125 VAC |  |
| Fuses |  | 2.0 A slo-blow |
| 115 VAC | 1.25 A slo-blow |  |

TABLE 2-11

## RESET KEY FUNCTIONS

The RESET key is a multiple purpose key that performs the following functions, depending on operation:

| Blink Cursor | Blinks the cursor when pressed; cursor quits blinking when key is released. |
| :--- | :--- |
| Control Character Storage | Pressing RESET while simultaneously entering a control character will store that control <br> character in Terminal memory. |
| Keying Into A Protected Field | With formatted displays, pressing RESET simultaneously with a character key will allow <br> that character to be keyed into a protected field; alpha data can be keyed into a <br> non-alpha field. |
| Rulings Character Set Disable | Disables optional ruling character set by reselecting the standard alphanumeric set. | | Buffer Transmission Terminate |
| :--- |
| Pressing RESET while a buffer transmission sequence is in progress will terminate Buffer <br> transmission. |
| ESC Over-Ride |
| Inhibits the effect of a previously received ESC control character during the time RESET <br> is held down. |
| Erase Protected Fields |

TABLE 2-12

## STRAP OPTIONS

There are two types of strap options used in the 4023, Factory and On Site. Factory options are set at the factory and include modifying the board by installing or removing circuit card runs. Factory straps are normally operating configuration straps, that select the standard operation configuration when un-cut. On Site straps are movable wire straps located on the circuit boards. These straps can be moved at the user site by qualified technical personnel.

The Strap Options Table gives the strap name, its function, its location on the board in respect to the nearest integrated circuit, and its type (Factory on On Site). Listing of boards is by assembly number (A1, A2, etc.), and the straps are alphabetized for each assembly. The location of a specific strap on a board is indicated by a number in the IC Location column. This number corresponds to the nearest integrated circuit to which the strap is located. The strap name is also silk-screened on the board next to the strap to aid in locating the strap. The card location on the minibus can be found by referring to Fig. 1-5.

## WARNING

Dangerous voltages exist inside the display unit. Before attempting to change any strap, or remove any circuit card for strap access, turn Terminal power off and disconnect the Terminal from the power source.

Some operating configurations require that more than one strap be set. The following information lists those operating configurations and the straps that must be sent to establish it. Strap name and locations are also given.

| CONFIGURATION | STRAPS | BOARD |
| :--- | :--- | :--- |
| Optional Rulings Character <br> Set Enable | BIT 9 RAMS IN | RAM Board |
|  | RULINGS | Timing Board |
| Optional 12 Lines Enable | ALT SET ERASE INPUT | Keyboard Interface |
|  | ALT SET XMIT | Control Board |
|  | 12 LINE RAM | Ram Board |
|  | 12 LINE DISPLAY | Cursor Board |
|  | 12 LINE LSTY CRS | Cursor Board |
|  | 12 LINE ROLL-UP SET | Cursor Board |
| RoII-Up Operation | 12 LINE ROLL-UP | Edit Board |
| Keyboard Inhibit | NO ROLL-UP | Edit Board |

The following is a listing of all the strap options that are available in the 4023.

RAM BOARD
(A1)
STRAP OPTIONS

| STRAP <br> NAME | IC <br> LOCATION | TYPE: <br> FACTORY <br> or SITE | FUNCTION |
| :--- | :---: | :---: | :--- |
| BIT 8 RAMS OUT | 81 | FACTORY | Standard un-cut. Cut to eliminate BIT 8 RAMS. This <br> inhibits Terminal response to Field Attribute Codes, thus, <br> eliminating Buffer Form Fill-Out Mode. Cut configuration <br> can be used for TTY subsitute operation. |
| BIT 9 RAMS IN | 91 | FACTORY | Standard un-cut. Cut to enable logic use of BIT 9 RAMS. <br> Enabling BIT 9 permits the optional ruling character set to <br> be enabled by control character SO. Standard character set <br> is re-selected by SI. |
| 12 LINE RAM | 245 | FACTORY | Standard un-cut. When cut, and straps on Cursor Board are <br> placed properly, only 12 lines of Data are displayed. |

CURSOR BOARD
(A2)
STRAP OPTIONS

| 12 LINE ROLL-UP | 121 | FACTORY | Standard un-cut. Cut to enable roll-up with 12 lines. |
| :--- | :---: | :---: | :--- |
| 12 LINE LSTY CRS | 111 | FACTORY | Standard un-cut. To enable 12 lines only, cut top strap, <br> then strap center pad to lower pad. |
| 12 LINE DISPLAY | 321 | FACTORY | Standard un-cut. To enable 12 lines, cut top strap, then <br> strap center pad to lower pad. |

KEYBOARD INTERFACE
(A4)
STRAP OPTIONS

| ALT. SET ERASE <br> INPUT | 91 | FACTORY | Standard un-cut prevents Erase Input from erasing the <br> optional ruling characters. However, if the rulings charac- <br> ters are not protected, they can be keyed over. This strap <br> would be cut if the Standard Lowercase ROM were <br> replaced with an alternate ROM. Cutting allows alternate <br> ROM characters to be erased by ERASE INPUT. |
| :--- | :---: | :---: | :--- |
| BRK FUL (Break <br> on Full) | 391 | FACTORY | Standard un-cut. When cut, the Terminal will transmit a <br> BREAK signal on the data link when line feeds, new lines <br> or cursor controls try to move the cursor below the bottom <br> last line. This is called Page Full. |

## KEYBOARD INTERFACE BOARD (cont)

(A4)
STRAP OPTIONS

| STRAP <br> NAME | IC LOCATION | TYPE: FACTORY or SITE | FUNCTION |
| :---: | :---: | :---: | :---: |
| BUSY FUL (Busy on Full) | 371 | FACTORY | Standard un-cut. When cut, the Terminal will not generate a terminal busy ( $\overline{\mathrm{TBUSY}}$ ) signal on page full. |
| CONSOLE LOCK $\overline{\mathbf{S P 2}}-\square$ | $\begin{aligned} & 351 \\ +5 \mathrm{k} & \\ \sum_{i} & \end{aligned}$ | SITE | Standard OUT. When the strap is placed so that one of the other minibus signals is strapped in, its going low will prevent operation of the keyboard. This includes character keys, clear, insert and delete character/line, etc. |


|  |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| CR DOES LF | 29 | SITE | This strap can be positioned to affect the line feed circuits <br> as follows: |  |  |  |  |  |



A low on this line locks out the keyboard

## KEYBOARD INTERFACE BOARD (cont) <br> (A4) <br> STRAP OPTIONS

| STRAP <br> NAME | IC <br> LOCATION | TYPE: <br> FACTORY <br> or SITE | FUNCTION |
| :--- | :---: | :---: | :---: |
| NO KEYBOARD <br> INSTALLED | 9 | FACTORY | Standard un-cut. When cut, the 4023 ignores the <br> KSTROBE input so that 4023 can be used without a <br> keyboard. |
| WRAP-AROUND | 69 | SITE | IN enables wrap-around feature when spacing past the 80th <br> character position. OUT disables wrap-around. |

## EDIT BOARD

(A5)
STRAP OPTIONS

| ROLL-UP <br> OUT <br> IN <br> (Standard) | 301 | FACTORY | Standard un-cut permits roll-up to work in Direct Entry only. Cutting IN strap and strapping the OUT position, disables roll-up. When roll-up is disabled, TBUSY will occur on page full, thus stopping data from the computer without loss (only if connected via a TTY Port). BUSY FUL strap on keyboard Interface Card must not be cut. |
| :---: | :---: | :---: | :---: |
| ROLL 4 <br> IN <br> OUT <br> (Standard) | 101 | FACTORY | Standard un-cut does not affect operation of ROLL circuitry; the Terminal goes busy on page full. When cut and strapped IN, and with the ROLL-UP strap in the standard configuration (IN), the Terminal will not go busy until after 4 lines of roll-up, stopping reception of data from the computer. RESET causes 4 more lines to roll-up. Roll-up 4 only would be used with TTY Port Interfaces. The BUSY FUL strap on keyboard Interface must not be cut. |
| 12 LINE ROLL-UP | 1 | FACTORY | Standard un-cut. When cut, roll-up operates with 12 lines. |

STRAP OPTIONS

| STRAP <br> NAME | IC <br> LOCATION | TYPE: FACTORY or SITE | FUNCTION |
| :---: | :---: | :---: | :---: |
| ALT SET XMIT | 100 | FACTORY | Normally BIT 9 true signifies that the character is part of the Rulings character set and is non-transmittable, regardless of Field Attribute Codes. When this strap is cut, this signifies that an alternate ROM is used for other characters. Their transmission is controlled by BIT 3 of the Field Attribute Code the same as normal alphanumeric data. Unless a special mod is ordered, the alternate set is indistinguishable from the normal character set in Buffer Entry Sequences. |
| AUTO CR AT END | 75 | FACTORY | Standard un-cut permits the Terminal to perform a carriage return at the end of the last line transmitted. (Clears $x$ cursor register only; does not transmit CR.) When cut, the cursor remains at the end of the message when transmission is completed. |
| EOL LF GEN | 1 | SITE | A three-position strap that provides functions according to the following: |

LOCAL-Standard position that causes line feeds to be generated in local when displaying copies of screen data that originates from an auxiliary unit such as a magnetic tape unit. Line feeds are not transmitted to the computer if On Line.

IN-Line feeds are generated by the send circuits when operating either in local or on line.

OUT-Line feeds are never generated at the end of a line.
A set of 7 factory straps that are used to select any of 128 ASCII characters for the "prompt" character. The uppercase $\mathrm{P}\left(80_{10}\right)$ is standard. The prompt character is an output from the computer that follows a line of Terminal input. When the Terminal completes a line of transmission, it performs a carriage return, then stops, awaiting the "prompt" from the computer. The receipt of the Prompt character is a signal to the Terminal to transmit another

$$
\text { B1 - B7-Bit } 1 \text { - Bit } 7
$$

1 - Strap must be between these two pins to select a logical 1 for that bit.
0 - Strap must be between these two pins to select a zero for that bit.
(The Prompt Character causes $\overline{\mathrm{CBUSY}}$ to go active for about 0.5 sec .)

CONTROL BOARD (cont)
(A6)
STRAP OPTIONS

| STRAP <br> NAME | IC <br> LOCATION | TYPE: <br> FACTORY or SITE | FUNCTION |
| :---: | :---: | :---: | :---: |
| FAST RESPONSE | 31 | FACTORY | Strapping the FAST RESPONSE holes, provides a shorter time for $\overline{\text { CBUSY }}$. Time provided is 25 to 60 millisec and would be used with minicomputers or for a test setting. (Standard time for $\overline{\text { CBUSY }}$ is $460 \mathrm{msec} \pm 40 \%$ ). This strap controls the length of $\overline{\mathrm{CBUSY}}$ upon Terminal receipt of a Prompt Character, or an ESC character. |
| PROMPT MODE | 85 | SITE | Two position strap that provides the following: <br> OUT-Standard strap position that sets the logic to not require a prompt from the computer for data transmission. <br> IN-This position requires a prompt character from the computer for each line of buffer data entered to the computer. (See Line Prompt Strap for prompt character.) |
| MESSAGE END <br> $=5$ least signific of the CR Cha |  | SITE | The Message End character is the last character sent in a message transmitted from the Terminal. Any ASCII control character can be strapped. The standard character used is CR. The Message End Character is also the last character sent in a Read Cursor transmission. See strap illustration. Note that only Bits 1.5 of the specific control character are strapped. |
| TAPEFETCH PROMPT | 89 | FACTORY | Standard un-cut. When cut, this will enable the SP2 (TAPEFETCH) minibus line to control the reading of the buffer to the computer, one character at a time (one character per tapefetch). TAPEFETCH is a signal originating from a TTY Port Interface associated with minicomputer paper tape reader control. The Tapefetch prompt operation permits the 4023 to emulate a high-speed reader. |

TIMING BOARD
(A7)
STRAP OPTIONS


TABLE 2-13
TIMING SPECIFICATIONS

| Display and Logic Timing <br> Master Oscillator | $22.008 \pm 0.25 \% \mathrm{MHz}$ crystal oscillator divided as follows: |
| :--- | :--- |
| Video | $11.004 \mathrm{MHz}(22.008 \div 2)$ |
| Character | $1.572 \mathrm{MHz}(11.004 \div 7)$ |
| Horizontal Sweep | $15.72 \mathrm{kHz}(1.572 \mathrm{MHz} \div 100)$ |
| Vertical | 60 Hz retrace: $(15.72 \mathrm{kHz} \div 262)$ <br> 50.06 Hz retrace: $(15.72 \mathrm{kHz} \div 314)$ <br> Input/Output Timing <br> Master Oscillator |



Note: Numbers 32-63 correspond to ASCII decimal code.

Fig. 2-1. Ruling Characters.


* CHARACTER IS PRECEDED BY ESC CHAR TO PERFORM FUNCTION
** WHEN RECEIVED BY TERMINAL, NEXT CHARACTER IS INTERPRETED AS A FAC. WHEN TRANSMITTING BUFFER CONTENTS, US IS TRANSMITTED INSTEAD OF THE FAC

Fig. 2-2. ASCII Code Chart.

## MAINTENANCE

## GENERAL INFORMATION

## INTRODUCTION

Beyond the need for occasional cleaning of the face of the display and other outer surfaces of the Terminal, there is virtually no need for routine servicing of the Terminal. It has no lubrication points, no air filters, and (with the exception of the crt) no vacuum tubes. The solid-state components provide stable operation, with little need for routine adjustment.

However, if a routine schedule and procedure is desired, a one-year interval and the following sequence is recommended. The disassembly and assembly instructions contained in this section should be referred to as necessary.

## DESK-MOUNTING

Desk-mounting consists of simply setting the Terminal on a desk or other surface. See Fig. 3-1. The air vents on the bottom, sides, and back should be kept free of obstructions.


Fig. 3-1. Desk Mounting.

## MOUNTING THE TERMINAL ON THE OPTIONAL PEDESTAL

A pedestal, on which the Terminal can be mounted, can be ordered from Tektronix, Inc. (PN 016-0568-00). Mounting the Terminal on the pedestal is accomplished by lifting the Terminal over the pedestal and installing four machine screws up through the pedestal top to fasten the Terminal in place. Adjust the four feet to a convenient position, and fasten the lock nuts.

## SERVICING PROCEDURE

1. Disconnect the line cord from the power source.
2. Remove the top from the Terminal.
3. Using a vacuum cleaner, remove dust accumulation from within the unit. Use a soft-bristled brush to loosen dust that won't otherwise vacuum out. A soft cloth and a mild soap and water solution can be used to remove any really stubborn dirt.
4. Inspect the interior for broken leads, loose connections, heat-damaged componehts, etc. Correct as necessary. Investigate the cause of any heat-damaged components.
5. Wash the face of the crt, using a soft cloth and a mild soap and water solution.
6. Perform the check-out procedure found in this manual. Perform the adjustment procedure if the check-out procedure indicates that it is necessary.
7. Put the cover back on the Terminal
8. Clean the outside of the Terminal, using a soft cloth and a mild soap and water solution.

## SOLDERED OPTIONS

In addition to strappable options, there are some options that can be selected by soldering or cutting soldered wires. To reduce the possibility of damage to the equipment, these changes should only be made by qualified technicians. These options are found in the Characteristics section. Information on use of these options is provided there.

## TROUBLESHOOTING INFORMATION

Troubleshooting of the Terminal can be done best if the various features of this manual are used to their fullest advantage. These features and recommended usage are listed here.

CONTROLS AND OPERATION. This information ensures operator understanding of the Terminal features and operation.

CHARACTERISTICS. A complete explanation of the Terminal capabilities is contained in the Characteristics, along with explanations of how to put the capabilities into use.

PERFORMANCE CHECK. This provides a rapid means of checking for proper operation in a logical sequence under normal equipment configuration. It can also be used with the options and the interface unit removed, to indicate operating status of the basic Terminal.

ADJUSTMENT. The procedure follows a logical sequence of adjusting the basic Terminal.

CIRCUIT DIAGRAMS AND CIRCUIT DESCRIPTIONS. These diagrams and their associated descriptions provide an understanding of Terminal operation on a circuit as well as component level. The information contained therein is essential to efficient location of trouble.

COMPONENT LAYOUT ILLUSTRATIONS. These appear on the aprons of their respective diagrams in Section 6 and can be used as aids for locating components.

INTERCONNECTING WIRE LISTS. A listing of cables, jacks and plugs, as well as an explanation of their use, is provided in the Diagrams section. Wire colors are also provided, using the standard code for resistors.

SEMICONDUCTOR INFORMATION. An illustration of semiconductors appears in Section 6 just preceding the diagrams, and can be used for pin identification. An integrated circuit test clip is recommended for use in troubleshooting the in-line integrated circuits, since it makes their leads easily accessible.

## TROUBLESHOOTING PROCEDURE

To troubleshoot the basic Terminal, remove all accessory cards and the interface card. Then check operation by doing the Performance Check. Stop where the Terminal fails to respond properly, and troubleshoot the referenced area, using schematics and associated descriptions. Replacement of suspected circuit cards is recommended as a fast means of confirming suspicions. If the Performance Check works satisfactorily in the basic Terminal, install option cards and the interface card one at a time and repeat the Performance Check until it fails. Then troubleshoot the last-inserted option card and the circuits with which it interacts.

Obviously, not all troubles can be revealed by the Performance Check or Adjustment Procedure. However, they should prove beneficial in most cases, and should aid in guiding a technician to the trouble area.

## RECOMMENDED TROUBLESHOOTING EOUIPMENT

A Logic Extender Card, Tektronix Part No. 067-0659-00, is an efficient tool for circuit analysis. This card can be used as an independent plug-in card to make all minibus signals available to the technician, providing level indicators for most of the lines. In addition, it provides a feature for injecting high- or low-level logic signals into the signal lines. The card can also be used as an extender for other circuit cards, and then permits interruption of any or all signals to the card which is attached to it.

Another extender card is available under Tektronix Part No. 067-0696-00. This card can be installed into the minibus to make bus lines available at test points, and can also be used as an extender for cards installed in the minibus.

A -20 V to +400 V dc voltmeter and a 10 MHz frequency-response oscilloscope are recommended test equipment for troubleshooting low-voltage and logic circuits.

## WARNING

Dangerous voltages exist within the Terminal and normal electrical safety precautions should be observed at all times when working around exposed circuits within these units.

The Motherboard can be completely disconnected and the supplies will still come up. However, when troubleshooting the power supply circuits, a resistive dummy-load should be connected in place of the Terminal circuits. This avoids accidental damage to other circuits in the Terminal. Recommended loads are as follows:

| Power Supply | Connector | Load |
| :---: | :---: | :---: |
| +15 V | J 152 | $7.5 \Omega 30 \mathrm{~W}$ |
| -12 V | J 150 | $15 \Omega 10 \mathrm{~W}$ |
| +5 V | J 153 | $0.5 \Omega 100 \mathrm{~W}$ |

## DISASSEMBLY AND ASSEMBLY

## ACCESS TO THE DISPLAY UNIT CIRCUITRY

For access to the circuits within the Terminal, remove the two screws on each side of the cover, and the two in back near the top. Then lift the cover off.

## KEYBOARD INFORMATION

Perform the following procedure to get at the keyboard circuits:

1. Remove the Terminal cover.
2. Remove the three larger screws from the top rear of the keyboard.
3. Remove the three screws from the bottom-front of the keyboard panel.
4. Pull the keyboard forward, then up and out as far as the cables will allow. Then turn the keyboard over.
5. The top surface of the circuit board can be accessed by removing the eight screws that hold the keyboard assembly to the keyboard panel.

Key caps can be removed by pulling them directly away from the keyboard. Use of a large pair of tweezers or a forceps is recommended.

Keys utilize reed switches whose solder contacts are accessible on the underside of the keyboard circuit board. Once the wires are unsoldered, the reeds can be extracted through the holes. Reverse the procedure for replacement.

Groups of keys are installed in assemblies which can be removed once the nuts are removed from the underside of the circuit board.

## CIRCUIT CARD INFORMATION

ACCESS. For access, remove the Terminal cover.

CIRCUIT CARD REMOVAL. The circuit cards plug into the minibus and are held in by circuit card hold-down clamps. Remove these clamps, disconnect the cabling, then pull the card (cards) from the minibus.

CARD WIRING. Each card is assigned an assembly number starting with A1, the RAM card. Fig. 1-5 illustrates the order the card assemblies are inserted into the minibus. Cabling at the Keyboard Interface, Edit, and Control cards use the resistance color code to assure proper connection. The plugs that attach to the afore-mentioned three cards are colored accordingly. For example, the Keyboard Interface (A4), has three yellow plugs attached. The green plug attaches to A 5 ; the blue to A 6 .

POWER SUPPLY CARD REMOVAL. Remove the cables that connect to the power supply circuit card. Unsolder the four wires that connect to the transformer. Then, remove the four screws that attach the card to the switch assembly.

## REAR ASSEMBLY REMOVAL

The rear assembly consists of the power supply and the Motherboard. For disassembly, follow this procedure. Refer to the illustrations in the mechanical parts list as necessary during this procedure.

## 1. Remove the Terminal cover.

2. Disconnect the cabling from the minibus circuit cards. For convenience, it is suggested that you remove all the circuit cards and set them aside.
3. Disconnect P210, P208, P207, and P205 from the Motherboard.

## 4. Remove power switch wiring (see Fig. 3-2):

a. Remove the transformer wiring top cover and disconnect the grey-red-white and grey-red-black wires from the jumper strip.
b. Remove the cover that houses S1001 and disconnect the grey-black-brown and grey-white-brown wires from the NO 1 and NO 2 connections of S1001. Loosen the clamp and pull these wires through the clamp.
c. Disconnect the ground terminal using a $1 / 4$ inch nut-driver or wrench.


Fig. 3-2. POWER switch wiring.
5. Remove the three machine screws that hold the rear assembly to the mainframe. One screw is on the left, near the silk screening for C 1006 ; the other two are on the right side, in line with the rear cable port.
6. Lift up on the assembly, tipping it back and pull the POWER switch wiring through the hole.
7. Lift the rear assembly away from the mainframe.

REAR ASSEMBLY INSTALLATION. The installation procedure is the reverse of the disassembly procedure.

## MONITOR ASSEMBLY INFORMATION

The monitor assembly includes the crt, Deflection and High Voltage Circuit Board, and the mounting brackets. Refer to the Mechanical Parts Lists as necessary during the following descriptions.

MONITOR ASSEMBLY REMOVAL. The monitor assembly is best removed by following this procedure.

## WARNING

The crt may implode if it is scratched or struck severely. Do not handle the crt by its neck. Wear protective clothing and a face shield when handling the crt.

When working around or directly with the crt, adequate electrical safety precautions need to be strictly observed. ALWAYS discharge to ground the High Voltage anode lead before removing the crt. High voltage can exist, even if the Terminal has not been operating for several days. Discharge by using a jumper strap similar to the one shown in Fig. 3-3. CONNECT STRAP TO GROUND FIRST.


Fig. 3-3. Discharging the high voltage anode.

1. Remove the Terminal cover.
2. Remove the logic cards from the Motherboard.
3. Disconnect J112 from the Monitor Circuit board.
4. Remove the four $3 / 8$-inch machine nuts that bolt the monitor to the mainframe.
5. Remove the machine screw near the left rear corner of the monitor circuit card.
6. Gently lift the monitor assembly out from the Terminal mainframe, and set the assembly on a foam rubber pad, being careful not to bump or scratch the crt.

CRT REMOVAL. The easiest and safest procedure for crt removal is to first remove the monitor assembly from the mainframe, then:

1. See WARNING under Monitor Assembly Removal.
2. Disconnect the plug from the rear of the neck by pulling gently and evenly on the plug.
3. Remove the ring magnets from the base of the crt neck by loosening the clamp screw and pulling the magnet assembly off the neck.
4. Remove the deflection coils in the same manner.
5. Remove the High Voltage anode lead by inserting a grounded screwdriver under the rubber grommet (see Fig. 3-3) and pushing when the screwdriver tip makes contact with the wire conductor. This allows one of the wire hooks to be removed from the anode connection. Twist the connector out and up to remove the other anode hook.
6. Remove the four machine screws that hold the monitor to the frame. HOLD THE MONITOR WITH ONE HAND TO PREVENT IT FROM FALLING WHEN THE LAST SCREW IS REMOVED.

MONITOR (CRT) INSTALLATION. Reverse the Monitor disassembly procedure.

DEFLECTION AMPLIFIER AND HIGH VOLTAGE BOARD. This board is best removed with the monitor
assembly removed. Disconnect all the plugs and pull the board up from the plastic tabs, a corner at a time. For installation, plug identification is provided by an illustration beside the board.

## HIGH VOLTAGE TRANSFORMER REMOVAL.

## WARNING

Be sure to discharge the High Voltage anode lead; otherwise, personal injury may result.

1. Remove the monitor assembly from the mainframe.
2. Disconnect P104, P105, and the High Voltage anode.
3. Place the monitor assembly face down on a foam rubber pad.
4. Remove the two nuts that hold the transformer to the bottom of the monitor assembly and remove the transformer.

To install the High Voltage transformer, reverse the above procedure.

## NOTE

After replacement or reassembly of any of the major afore-described Monitor assemblies, perform the display adjustments procedures provided in Section 4.

## SILICON GREASE

Silicon grease is applied to both sides of the mica insulators used with the following components: Q1105, Q1110, Q1112, Q1118. In addition, silicon grease is applied to both sides of the mica insulators used with Q106 and CR103 on the Deflection and High Voltage board.

## POWER TRANSFORMER INFORMATION

The power transformer can be wired for use with 115 V or 230 V nominal line voltage, and can be set for any of several ranges within the nominal setting.

Instructions for connecting the transformer are contained in the Installation Section. Note that the line fuse must also be changed when shifting between 115 and 230 volt operation.

## PERFORMANCE CHECK/ADJUSTMENT PERFORMANCE CHECK

## GENERAL

This procedure (see Table 4-1) can be used under normal operating conditions with all circuit cards installed. Because some checks require that ON LINE be selected, check that the Terminal is not connected to a modem or computer.

Checks are referenced to a circuit card to permit rapid evaluation of incorrect results. In event of an improper response, recheck the step with all optional and interface cards removed from the minibus to determine if the Terminal is at fault.

TABLE 4-1
Performance Check Procedure

| Activity | Results | Check/Adjustment |
| :---: | :---: | :---: |
| Turn Terminal Power On. | Indicator on right of keyboard glows. | Power Supply (Adjustment 1). |
| Wait 30 seconds. | Cursor appears in upper-left hand corner of display-the home position. | Cursor, Timing, Monitor Circuitry, RAM. Check BRIGHTNESS and CONTRAST controls. |
| Adjust BRIGHTNESS and CONTRAST. | Optimum setting is to adjust BRIGHTNESS all the way up, then back down to the point where the field just becomes invisible; then adjust CONTRAST for best viewing. | Timing, Monitor Circuitry. |
| Set switches to LOCAL and BUFFER, then enter a few characters. | Characters are displayed; cursor moves one space after each key actuation. | Keyboard, Keyboard Interface, RAM, Timing, Cursor. |
| Enter a page full of " H " characters by pressing ERASE INPUT SHIFT and H keys. (Hold down H key and release other two keys to fill screen with H characters). | Screen fills with " H " characters (Readjust BRIGHTNESS and CONTRAST if necessary). Note that every character position contains an " H " character. | Keyboard, Timing, Cursor, RAM. |
| Check for 24 lines of characters (12 lines optional). |  | Cursor. |
| Check for 80 characters per line. |  | Cursor. |
| Press ERASE INPUT key. | Screen is erased, cursor positions to home. | Keyboard, Keyboard Interface, Cursor, RAM. |
| Check each written character on the keyboard; including shifted characters. | Characters displayed are same as indicated on top of keycaps. | Keyboard, RAM, Timing. |
| Press the TTY Lock key to place it in its locked position. Press each character key with the SHIFT key released. | All letter characters should be written as upper case. | Keyboard. |

Table 4-1 (cont)

| Activity | Results | Circuit/Adjustment |
| :---: | :---: | :---: |
| Press a character key and hold down. | Characters repeat after an approximate $1 / 2$ second delay. | Keyboard, Keyboard Interface. |
| Key in 73 consecutive characters, then key in one more. | Bell rings when spacing past 73rd character. | Cursor, Keyboard Interface. |
| Check Wrap-around. Move the cursor to the 80th character position; Place DIRECT/BUFFER Switch to DIRECT, then type or space past the 80th character. | If Wrap-around has been enabled by Wrap-around strap, cursor positions down one line and is at the left margin. <br> NOTE <br> Wrap-around capability may not be available on some earlier Terminal models. | Cursor, Keyboard Interface. |
| Reselect BUFFER and check that Wrap-around does not work. |  |  |
| Move the cursor away from the left margin and press the RETURN key. | With CR DOES LF strap option at IN, cursor spaces one line down and moves to left margin. With CR DOES LF strap option at OUT, cursor moves to left margin. With CR DOES LF strap option at BUFFER, cursor spaces one line down and moves to left margin (BUFFER position prevents computer originated RETURNS from generating a LINE feed). | Keyboard Interface, Cursor. |
| Press ${ }^{\text {c }}$ M . | Same as RETURN key. | Keyboard Interface, Cursor. |
| Move cursor away from left margin, then press LF. | With LF DOES CR strap option at LF, cursor moves to next line. With LF DOES CR strap option at LF/CR, cursor moves to left margin of next line. | Keyboard, Keyboard Interface, Cursor. |
| Press ${ }^{\text {c }}$ J. | Same as LF key. | Keyboard Interface, Cursor. |
| Press HOME key. | Cursor positions to home-the first chararacter position on first line. | Keyboard, Keyboard Interface, Cursor. |
| Enter 23 LINE FEEDS (LF's). | Cursor moves to bottom-left corner of display. |  |
| Enter 24th LINE FEED. | Cursor does not move. Display remains stable. | Edit, Cursor. |

Table 4-1 (cont)

| Activity | Results | Circuit/Adjustment |
| :--- | :--- | :--- |
| Set DIRECT-BUFFER switch to |  |  |
| DIRECT. Check that rear panel |  |  |
| ECHO switch is set to IN. Then |  |  |
| enter another LINE FEED. | Displayed information rolls-up; The top <br> line is deleted and a line of NUL's resides <br> in the 24th line. The cursor does not <br> move. With the Edit Card strapped for 4 <br> line ROLL-UP, four LF's can be given <br> before Terminal goes busy. Pressing RE- <br> SET enables four more roll-ups. With the |  |
| NO ROLL-UP strap cut, roll-up cannot <br> occur when line feeding past the bottom |  |  |
| line. |  |  |

Table 4-1 (cont)

| Activity | Results | Circuit/Adiustment |
| :---: | :---: | :---: |
| Press the following keys $\rightarrow \uparrow \leftarrow \downarrow$ | Cursor moves in direction indicated on key cap. | Keyboard, Keyboard Interface, Cursor. |
| Press NUM LOCK to detent then press each of the eleven remaining function controls. | Numeric characters are now displayed as indicated on the front of the keycaps. SEND-ENTER key displays a decimal point. | Keyboard, Keyboard Interface. |
| Press NUM LOCK again to reestablish normal function controls. | Normal Function Controls re-established. |  |
| Obtain a page full of characters. |  |  |
| Press INS C. | Character at cursor location and all characters to right of cursor move one space to right. 80th character is lost. A space resides at the cursor location and the cursor does not move. Hold key down to check repeatability. | Edit, Cursor, RAM, Timing, Keyboard. |
| Move cursor to a new line and press DELC. | Character at cursor location is deleted and all characters to right of cursor move left one space. 80th character position contains a NUL character. Hold key down to check repeatibility. | Edit, Cursor, RAM, Timing, Keyboard. |
| Simultaneously press SHIFT and INS L. | Line where the cursor resides and all lines below the cursor move down one line. The 24th line (12th line optional) is lost. The cursor does not move and a line of SPACE characters is inserted at the cursor location. Hold keys down to check repeatibility. | Edit, Cursor, RAM, Timing, Keyboard. |
| Simultaneously press SHIFT and DEL L. | The line where the cursor resides is deleted, and all lines below the cursor move up one line. A line of NUL characters reside in the 24th line (12th line optional). Hold keys down to check repeatibility. | Edit, Cursor, RAM, Timing, Keyboard. |
| Check buffer transmitting circuits. Switch to ON LINE and then switch the Baud Rate Selector to 300. Obtain a page full of caracters. Move the cursor to the middle of the second line and press ENTER. | A white block (ETX-Message Separator) is displayed at the cursor location; the KEYBOARD LOCK Indicator becomes lighted; the cursor moves to home and begins moving across line 1, transmitting the data until it reaches the end of the line. A CR and LF is performed and transmission continues on line 2 . When cursor reaches stored ETX, transmission stops, a carriage return is performed and KEYBOARD LOCK indicator turns off. | Keyboard, Control; Interface, Cursor; RAM. |

Table 4-1 (cont)

| Activity | Results | Circuit/Adjustment |
| :--- | :--- | :--- |
| Press ENTER, then press RESET. | ENTER begins transmission; RESET <br> terminates transmission, with cursor <br> residing at last character transmitted. | Control, Interface. |
| Press ENTER, then press HOME. | ENTER sequence is terminated with the <br> cursor positioning to HOME. | Control, Cursor, Interface. |
| Delete all lines except for line one. |  |  |
| Simultaneously press SHIFT and | Line one is sent las in ENTER above) <br> SEND. | Keyboard, Control, Interface, Cursor, <br> location. Note that NUL's contained on |
| the remainder of the page are not trans- |  |  |
| mitted. This is indicated by the cursor |  |  |
| moving rapidly to the left margin of the |  |  |
| last line. |  |  |

Table 4-1 (cont)

| Activity | Results | Circuit/Adjustment |
| :---: | :---: | :---: |
| Type both alpha and numeric characters into field. | Alpha and numeric data can be entered into the inverted, unprotected field. | Control, Timing. |
| Move Cursor to beginning of third line, then press ${ }^{\mathrm{Cs}} \mathrm{O}$ followed by Q . | Line blinks from cursor location to the FAC (Field Attribute Code) that defines the next field. | Control, Timing. |
| Try typing alpha-characters into field. | Cannot be done. Bell rings. | Control, Timing. |
| Enter Numeric characters. | Numeric characters can be entered into the blinking field. All characters in columns 2 and 3 of the ASCII code chart can be entered into this field. | Control, Timing. |
| Position cursor over second character in the blinking field, then press ERASE TO END. | Data in blinking field is erased from cursor position to end of blinking field. Cursor resides in first character position of inverted field. | Keyboard Interface, Timing, Cursor, RAM. |
| Press ERASE TO END key again. | Data in inverted field is erased from cursor position to end of line. Cursor resides at end of line. | Keyboard Interface, Timing, Cursor, RAM. |
| Move cursor down to fifth line, then position cursor away from left margin. Key in some characters on that line. |  |  |
| Position cursor to left margin of fifth line, then press ${ }^{\mathrm{Cs}} \mathrm{O}$ followed by $Z$. | Data residing in fifth line becomes blanked. | Timing. |
| Position cursor back to beginning of fifth line, then press DEL C key. | Field Attribute code is deleted. Video in fifth line becomes visible once again. | Edit, Cursor, Timing. |
| Position cursor over the FAC that defines the blinking field, then simultaneously press RESET and a character key. | The FAC is replaced with the character represented by the key pressed. Data that was previously blinking returns to normal. | Timing, Keyboard Interface. |
| Enter a page full of characters. Then, using the FAC code chart (Table 2-8) enter a few protected and unprotected fields at different locations on the display. For field definition, set codes that cause protected fields to blink and unprotected fields to be inverted (Black on White). | Display becomes full of characters. Fields are set as defined by the FAC's. |  |

Table 4-1 (cont)

| Activity | Results | Circuits/Adjustment |
| :---: | :---: | :---: |
| Press HOME, then TAB key. | Cursor goes home, then "tabs" to first character position of the first unprotected field. | Control, Cursor, RAM, Timing. |
| Send the HT control character (press ${ }^{\mathrm{C}}$ ). | Cursor tabs to next unprotected field. | Control, Cursor, RAM, Timing. |
| Send the VT control character (press ${ }^{C} K$ ). | Cursor backtabs to first character position of preceding unprotected field. | Control, Cursor, RAM, Timing. |
| Press the ERASE INPUT key. | Data defined by FAC's as unprotected is erased. Note also that all data not defined by a FAC is erased. | Keyboard Interface, Control, Timing, Cursor, RAM. |
| Type data back into the unprotected fields, then press and release ESC, then press the " $O$ " letter key. | Again, all data residing in unprotected fields is erased. | Keyboard Interface, Control, Timing, Cursor, RAM. |
| Obtain a new page full of characters. Using the FAC code chart (Table 2-8), enter a few transmittable and non-transmittable fields at different locations on the display. As before, set different codes for field identification. | Display becomes full of characters. Fields are set as defined by the FAC's. |  |
| Press ENTER. | No ETX (Message Separator) codes stores at the Cursor location. Cursor moves to HOME and begins sending transmittable data only; skipping the non-transmittable fields. Note that all data not defined by a FAC is transmitted. | Control, Interface. |
| Press ESC, then send SO control character ( ${ }^{\mathrm{C}} \mathrm{O}$ ). | Results are same as for ENTER above. | Control, Interface. |
| Simultaneously press SHIFT and SEND. | All information displayed is transmitted; even non-transmittable fields. | Control, Interface. |
| Press ESC, then send the SI control character ( ${ }^{\mathrm{C}} \mathrm{N}$ ). | Results are same as for SEND above. | Control, Interface. |
| ERASE the page. |  |  |
| Optional ruling characters check. Press ${ }^{\mathrm{C}} \mathrm{N}$. Then press (in sequence) all characters found in columns 2 and 3 of the ASCII code chart. | 32 different ruling characters are displayed. | Timing. |
| Check that ruling character provided by each key is same as shown in Fig. 2-1. |  | Timing. |

Table 4-1 (cont)

| Activity | Results | Circuit/Adjustment |
| :---: | :---: | :---: |
| Press ERASE INPUT key. | Ruling characters cannot be erased via an Erase Input Function (unless the ALTERNATE SET ERASE INPUT strap on Keyboard Interface is cut). | Keyboard Interface. |
| Press ENTER. | Ruling characters are not transmitted (unless ALT SET XMIT strap on Control Card is cut). | Control. |
| Send the SI control character ( ${ }^{\mathrm{C}} \mathrm{O}$ ). Type a few numeric characters. | Normal character set is re-established. | Timing. |
| Select ruling characters once again. Press a few numeric keys to ensure rulings set selection, then press RESET. | Normal character set is re-established by pressing RESET. | Timing. |
| Erase Screen, then press RESET, while entering the SOH control character ( ${ }^{C} A$ ). | A bright block stores at the Cursor location. | RAM, Timing. |
| Check out storage of rest of control characters (Refer to ASCII code chart). | Control characters with Bit 1 high should store (be displayed). Those with Bit 1 low, should not store. | RAM, Timing. |
| ERASE page. | Display erases; normal operation is reestablished. Cursor goes home, PERFORMANCE CHECK COMPLETED. |  |

## ADJUSTMENT

## INTRODUCTION

Adjustment of the Terminal is required only when it ceases to properly perform its intended functions, or after circuit repairs have been made to the power supply or to the monitor circuitry. If an adjustment is to be performed on a routine schedule, an interval of one year is recommended. Adjustment should be preceded by a thorough cleaning and inspection as outlined in the Maintenance Section. Adjustment should be performed in a $+20^{\circ} \mathrm{C}$ to $+30^{\circ} \mathrm{C}$ environment and should be preceded by a twenty minute warm-up period.

## EQUIPMENT REQUIRED

The following equipment is required in this precedure:

1. Variable voltage source that has an output capacity of at least 2 A at 100,110 , or 120 Vac , or at least 1.25 A at 200,220 , and 240 Vac . The instrument output should be variable to at least $\pm 10 \%$ from the stated value.
2. Single trace Oscilloscope with 10 mV vertical sensitivity. Frequency response should include dc to at least 10 MHz .
3. Voltmeter with a range of at least -20 Vdc to +20 Vdc ; accuracy within at least $1 \%$ on all voltage ranges.
4. Common Screwdriver. $1 / 8$ inch tip, non-conductive, at least 10 inches in length, plus handle.
5. Screwdriver, Allen-Type, 3/32 inch tip--non conductive, at least 10 inches in length, plus handle.

## ADJUSTMENT PROCEDURE

## PRELIMINARY

Turn the Terminal power off and remove the line cord from the power source.

## WARNING

Dangerous voltages exist within the Terminal. Normal electrical precautions need to be observed when working within the Terminal while the cover is removed.

## REMOVE THE TERMINAL COVER

At the back-left corner, remove the shield that covers the transformer terminals. It is held in place by two screws. Determine what voltage the transformer is wired for, by comparing the connections against the diagram on the surfaces of the switch (S1001) cover. If a variable ac power supply is available, set it to the voltage for which the transformer is wired. If the indicated supply is not available, record the transformer wiring condition so it can be restored upon completion of the adjustment procedure. Then rewire the transformer connections to agree with the available power supply. See wiring diagram for instructions.

Check the slow blow fuse (2 A for 115 V or 1.25 A for 230 V).

## WARNING

Dangerous voltages exist in the fuse and transformer circuits. Keep the line cord disconnected while working in these areas.

Check the $+5 \mathrm{Vdc}, 15 \mathrm{~A}$ fast blow fuse for proper size.

## DETAILED PROCEDURE

Adjustments include Low Voltage Power Supply and Monitor Adjustments.

## 1. LOW VOLTAGE POWER SUPPLY CHECK/ADJUSTMENT

a. After the preliminary procedure has been completed, connect the line cord to a variable power supply source (auto transformer) which is set to the voltage for which the transformer is wired.
b. Turn the Terminal power switch ON and place the LOCAL/ON LINE switch to LOCAL.
c. Connect the voltmeter reference lead to the ground Test point, TP 12. See Fig. 4-1.
d. Using a voltmeter that has $1.0 \%$ or better accuracy, adjust R 258 to obtain +5.00 V at the +5 V test point. Adjustment and test point locations are shown in Fig. 4-1.


Fig. 4-1. Power Supply Adjustment and Test Point locations.
e. Measure the other power supply voltages as listed in Table 4-2. Test points are shown in Fig. 4-1. Record all voltages in Table 4-3. (Make duplicate copies of Table 4-3 for future use.)
f. Using the test oscilloscope, check that ripple voltages do not exceed those values given in Table 4-2.
g. Change the variable power source to $10 \%$ below the center value for which the transformer is wired.
h. Measure and record the supply voltages, again using Tables 4-2 and 4-3. Then check the ripple of each supply.
i. Change the variable power source to $10 \%$ above the center value for which the transformer is wired.
j. Again measure and record the supply voltages, again using Tables 4-2 and 4-3. Then check the ripple of each supply.
k. Analyze the results. All voltages should be within the specified values. The differences between voltages at center line and either high or low line should not show a regulation larger than that specified in Table 4-3.
I. Set the line voltage to the center voltage for which the transformer is wired.

TABLE 4-2

Power Supply Voltage Limits

| Supply | Test Point | Voltage Limits | Ripple (P-P) | Comments |
| :---: | :---: | :---: | :---: | :---: |
| +5 V | TP 8 | +4.9 to +5.1 | 20 mV | Adjust R258 for +5 V; re- <br> adjust to compromise so that <br> +15 V and -12 V and -5 V <br> supplies are within limits with <br> line voltage at mid-position as <br> well as at high and low limit. |
| +15 V | TP 7 | +14.850 to <br> +15.150 | NOT |  |
| -5 V | TP 10 | -4.9 to -5.1 | 20 mV | ADJUSTABLE |

TABLE 43
Observed Voltages

|  | (A) <br> Center <br> Line <br> Voltage | (B) <br> Low <br> Line <br> Voltage | (C) <br> High <br> Line <br> Voltage | (D) <br> Greater <br> Deviation <br> From (A) | \% Observed <br> Regulation <br> (D) | (A) |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| +15 V |  |  |  |  |  | Regulation <br> Limit |
| +5 V |  |  |  |  |  |  |
| -5 V |  |  |  |  |  |  |
| -12 V |  |  |  |  |  |  |

## 2. TILT CORRECTION

a. Obtain a page full of characters by simultaneously pressing the ERASE INPUT SHIFT and H keys. Hold down on " H " while releasing the other two keys.
b. Check display for tilt. If tilted, loosen the yoke clamp screw and rotate the yoke to level the display. Fig. 4-2 shows component locations.
c. Tighten the clamp screw.

WARNING

Tightening the yoke clamp screws too tight may cause implosion. Tighten just enough to prevent yoke movement.
3. DISPLAY CENTERING
a. Check display for centering.
b. Center display by using ring magnets on yoke assembly. Fig. 4-2 shows component locations.


Fig. 4-2. Monitor Component locations.

## 5. FOCUS ADJUSTMENT

Adjust R107 for best over-all focus.

## NOTE

FOCUS, BRIGHTNESS, and CONTRAST Adjustments all interact. Adjust BRIGHTNESS and CONTRAST for optimum viewing before adjusting FOCUS.

## 6. HEIGHT ADJUSTMENT

a. Adjust Height Control, R124, for a 24 -line height of 4.5 inches ( 12 cm ).

## 7. VERTICAL LINEARITY ADJUSTMENT

Adjust R121 for best vertical linearity. This can be done by checking that the characters in the top line are the same height as the same characters in the bottom line.

## 8. VERTICAL SYNC ADJUSTMENT

a. Turn Terminal Power OFF.
b. Remove P79 from J79, and bend Pin 1 so that P79 can be installed without pin 1; see Fig. 4-3 for illustration.
c. Turn Terminal power back ON.
d. Adjust R116 to the point where the cursor rolls up approximately three rolls every second.
e. Turn power OFF and reconnect pin 1 to J79.
f. Turn power back on and enter a page full of characters. Note Stable display.
g. Height, Linearity and Vertical Sync Adjustments interact. Repeat as necessary, in the order listed.


Fig. 4-3. Configuration of P/J79 for Vertical Sync Adjustment.

# REPLACEABLE <br> ELECTRICAL PARTS 

## PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

## SPECIAL NOTES AND SYMBOLS

X000 Part first added at this serial number
00X Part removed after this serial number

ITEM NAME
In the Parts List, an Item Name is separated from the description by a colon (:) Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

## ABBREVIATIONS

| ACTR | ACTUATOR | PLSTC | PLASTIC |
| :--- | :--- | :--- | :--- |
| ASSY | ASSEMBLY | QTZ | QUARTZ |
| CAP | CAPACITOR | RECP | RECEPTACLE |
| CER | CERAMIC | RES | RESISTOR |
| CKT | CIRCUIT | RF | RADIO FREQUENCY |
| COMP | COMPOSITION | SEL | SELECTED |
| CONN | CONNECTOR | SEMICOND | SEMICONDUCTOR |
| ELCTLT | ELECTROLYTIC | SENS | SENSITIVE |
| ELEC | ELECTRICAL | VAR | VARIABLE |
| INCAND | INCANDESCENT | WW | WIREWOUND |
| LED | LIGHT EMITTING DIODE | XFMR | TRANSFORMER |
| NONWIR | NON WIREWOUND | XTAL | CRYSTAL |


| Mfr. Code | Manufacturer | Address | City, State, Zip |
| :---: | :---: | :---: | :---: |
| 000FA | BALL ELECTRONICS DISPLAY DIVISION | Р О вох 43376 | ST. PAUL, MN 55164 |
| 01121 | ALLEN-BRADLEY COMPANY | 1201 2ND STREET SOUTH | MILWAUKEE, WI 53204 |
| 01295 | TEXAS INSTRUMENTS, INC. |  |  |
|  | SEMICONDUCTOR GROUP | P.O. BOX 5012 | DALLAS, TX 75222 |
| 01963 | CHERRY ELECTRICAL PRODUCTS CORPORATION | 3600 SUNSET AVENUE | WAUKEGAN, IL 60085 |
| 02735 | RCA CORPORATION, SOLID STATE DIVISION | ROUTE 202 | SOMERVILLE, NY 08876 |
| 03508 | GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR |  |  |
|  | PRODUCTS DEPARTMENT | ELECTRONICS PARK | SYRACUSE, NY 13201 |
| 03888 | KDI PYROFILM CORPORATION | 60 S JEFFERSON ROAD | WHIPPANY, NJ 07981 |
| 04009 | ARROW-HART, INC. | 103 HAWTHORNE STREET | HARTFORD, CT 06106 |
| 04222 | AVX CERAMICS, DIVISION OF AVX CORP. | P O BOX 867 | MYRTLE BEACH, SC 29577 |
| 04713 | MOTOROLA, INC., SEMICONDUCTOR PROD. DIV. | 5005 E MCDOWELL RD,PO BOX 20923 | PHOENIX, AZ 85036 |
| 07109 | OAKTRON INDUSTRIES, INC. | 704 30TH STREET | MONROE, WI 53566 |
| 07263 | FAIRCHILD SEMICONDUCTOR, A DIV. OF |  |  |
|  | FAIRCHILD CAMERA AND INSTRUMENT CORP. | 464 ELLIS STREET | MOUNTAIN VIEW, CA 94042 |
| 10389 | CHICAGO SWITCH, INC. | 2035 WABANSIA AVE. | CHICAGO, IL 60647 |
| 11237 | CTS KEENE, INC. | 3230 RIVERSIDE AVE. | PASO ROBLES, CA 93446 |
| 12969 | UNITRODE CORPORATION | 580 PLEASANT STREET | WATERTOWN, MA 02172 |
| 13993 | baLL brothers research corporation | BOULDER INDUSTRIAL PARK | BOULDER, CO 80302 |
| 14433 | ITT SEMICONDUCTORS | 3301 ELECTRONICS WAY P O BOX 3049 | WEST PALM BEACH, FL 33402 |
| 14752 | ELECTRO CUBE INC. | 1710 S. DEL MAR AVE. | SAN GABRIEL, CA 91776 |
| 15238 | ITT SEMICONDUCTORS, A DIVISION OF INTER |  |  |
|  | NATIONAL TELEPHONE AND TELEGRAPH CORP. | P.O. BOX 168, 500 BROADWAY | LAWRENCE, MA 01841 |
| 17954 | MIRATEL, DIV. BALL BROS RESEARCH CORP. | 1633 TERRACE DRIVE | ST. PAUL, MN 55113 |
| 18796 | ERIE TECHNOLOGICAL PRODUCTS, INC. |  |  |
|  | State College division | 1900 W. College ave. | State College, Pa 16801 |
| 22753 | U. I. D. ELECTRONICS CORP. | 4105 PEMBROKE RD. | HOLLYWOOD, FL 33021 |
| 27014 | NATIONAL SEMICONDUCTOR CORP. | 2900 SEMICONDUCTOR DR. | SANTA CLARA, CA 95051 |
| 32159 | WEST-CAP ARIZONA | 2201 E. ELVIRA ROAD | TUCSON, AZ 85706 |
| 32997 | BOURNS, INC., TRIMPOT PRODUCTS DIV. | 1200 COLUMBIA AVE. | RIVERSIDE, CA 92507 |
| 33096 | COLORADO CRYSTAL CORPORATION | 2303 W 8TH STREET | LOVELAND, CO 80537 |
| 50088 | MOSTEK CORP. | 1400 UPFIELD DR. | CARROLLTON, TX 75006 |
| 50522 | MONSANTO CO., ELECTRONIC SPECIAL |  |  |
|  | PRODUCTS | 3400 HILLVIEW AVENUE | PALO ALTO, CA 94304 |
| 50558 | ELECTRONIC CONCEPTS, INC. | 526 INDUSTRIAL WAY WEST | EATONTOWN, NJ 07724 |
| 50579 | LITRONIX INC. | 19000 HOMESTEAD RD. | CUPERTINO, CA 95014 |
| 51284 | MOS TECHNOLOGY, INC., VALLEY FORGE |  |  |
|  | CORPORATE CENTER | 950 RITTENHOUSE ROAD | NORRISTOWN, PA 19401 |
| 52833 | KEYTRONIC CORP., OCR DIV. | SPOKANE INDUSTRIAL PK., <br> P. O. BOX 14687 | SPOKANE, WA 99214 |
| 55292 | LEDCO DIV., WILBRECHT ELECTRONICS, INC. | 240 EAST PLATO BLVD. | ST. PAUL, MN 55107 |
| 56289 | SPRAGUE ELECTRIC CO. | 87 MARSHALL ST. | NORTH ADAMS, MA 01247 |
| 58756 | CTS OF ELKHART INC. | 1142 W. BEARDSLEY AVE. | ELKHART, IN 46514 |
| 59660 | TUSONIX INC. | 2155 N FORBES BLVD | TUCSON, AZ 85705 |
| 59821 | CENTRALAB INC | 7158 MERCHANT AVE | EL PASO, TX 79915 |
|  | SUB NORTH AMERICAN PHILIPS CORP |  |  |
| 71400 | BUSSMAN MFG., DIVISION OF MCGRAW. |  |  |
|  | EDISON CO. | 2536 W. UNIVERSITY ST. | ST. LOUIS, MO 63107 |
| 71450 | CTS CORP. | 905 N. WEST BLVD | ELKHART, IN 46514 |
| 72982 | ERIE TECHNOLOGICAL PRODUCTS, INC. | 644 W .12 TH ST. | ERIE, PA 16512 |
| 73138 | BECKMAN INSTRUMENTS, INC., HELIPOT DIV. | 2500 HARBOR BLVD. | FULLERTON, CA 92634 |
| 75042 | TRW ELECTRONIC COMPONENTS, IRC FIXED |  |  |
|  | RESISTORS, PHILADELPHIA DIVISION | 401 N. BROAD ST. | PHILADELPHIA, PA 19108 |
| 75915 | LITTELFUSE, INC. | 800 E. NORTHWEST HWY | DES PLAINES, IL 60016 |
| 80009 | TEKTRONIX, INC. | P O BOX 500 | BEAVERTON, OR 97077 |
| 83003 | VARO, INC. | P O BOX 411, 2203 WALNUT STREET | GARLAND, TX 75040 |
| 90201 | MALLORY CAPACITOR CO., DIV. OF | 3029 E. WASHINGTON STREET |  |
|  | P. R. MALLORY AND CO., INC. | P. O. BOX 372 | INDIANAPOLIS, IN 46206 |
| 91637 | DALE ELECTRONICS, INC. | P. O. BOX 609 | COLUMBUS, NE 68601 |
| 91836 | KINGS ELECTRONICS CO., INC. | 40 MARBLEDALE ROAD | TUCKAHOE, NY 10707 |
| 96733 | SAN FERNANDO ELECTRIC MFG CO | 1501 FIRST ST | SAN FERNANDO, CA 91341 |


| Ckt No. |  | Serial/Model No. |  | Name \& Description | MfrCode | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Part No. | Eff | Dscont |  |  |  |
| A1 | 670-2197-01 |  |  | CKT BOARD ASSY:RAM | 80009 | 670-2197-01 |
| A1 | 670-3197-01 |  |  | CKT BOARD ASSY:RAM | 80009 | 670-3197-01 |
| A1 | 670-3197-02 | B050000 |  | CKT CARD ASSY: | 80009 | 670-3197-02 |
| A2 | 670-2198-01 | B010100 | B049999 | CKT BOARD ASSY:CURSOR | 80009 | 670-2198-01 |
| A2 | 670-2198-02 | B050000 | B064267 | CKT BOARD ASSY: | 80009 | 670-2198-02 |
| A2 | 670-2198-03 | B064268 |  | CKT BOARD ASSY:CURSOR | 80009 | 670-2198-03 |
| A4 | 670-2301-01 |  |  | CKT BOARD ASSY:KEYBOARD INTERFACE | 80009 | 670-2301-01 |
| A4 | 670-2301-02 |  |  | CKT BOARD ASSY:KEYBOARD INTERFACE | 80009 | 670-2301-02 |
| A4 | 670-2301-03 |  |  | CKT BOARD ASSY:KEYBOARD INTERFACE | 80009 | 670-2301-03 |
| A4 | 670-2301-04 |  |  | CKT BOARD ASSY:KEYBOARD INTERFACE | 80009 | 670-2301-04 |
| A4 | 670-2301-06 | B050000 |  | CKT CARD ASSY: | 80009 | 670-2301-06 |
| A4 | 670-3428-00 |  |  | CKT BOARD ASSY:C.R. | 80009 | 670-3428-00 |
| A5 | 670-2200-03 |  |  | CKT BOARD ASSY:EDIT | 80009 | 670-2200-03 |
| A5 | 670-2200-04 |  |  | CKT BOARD ASSY:EDIT | 80009 | 670-2200-04 |
| A5 | 670-2200-06 | 8050000 |  | CKT BOARD ASSY: | 80009 | 670-2200-06 |
| A6 | 670-2542-02 |  |  | CKT BOARD ASSY:CONTROL | 80009 | 670-2542-02 |
| A6 | 670-2542-04 | 8050000 |  | CKT CARD ASSY: | 80009 | 670-2542-04 |
| A7 | 670-2199-02 |  |  | CKT BOARD ASSY:TIMING | 80009 | 670-2199-02 |
| A7 | 670-2199-03 |  |  | CKT BOARD ASSY:TIMING | 80009 | 670-2199-03 |
| A7 | 670-2199-04 |  |  | CKT BOARD ASSY:TIMING | 80009 | 670-2199-04 |
| A7 | 670-2199-05 | B020545 | B049999 | CKT BOARD ASSY:TIMING | 80009 | 670-2199-05 |
| A7 | 670-2199-07 | B050000 |  | CKT BOARD ASSY: | 80009 | 670-2199-07 |
| A10 | 670-2195-01 |  |  | CKT BOARD ASSY:MOTHER | 80009 | 670-2195-01 |
| A10 | 670-2195-02 | B050000 |  | CKT BOARD ASSY: | 80009 | 670-2195-02 |
| A11 | 119-0374-01 | B010100 | B063619 | KEYBOARD,CMPTR:72 KEY,TTY,ASCII ENCODED | 52833 | 65-0763-01 |
| A11 | 119-0374-09 | B063620 |  | KEYBOARD ASSY: | 80009 | 119-0374-09 |
| A12 | 119-0363-00 | B010100 | B064505 | MONITOR,TV:15 DEG TILT,15VDC,P4 PHOSPH | 17954 | TV-12C7-012-0124 |
| A12 | 119-0363-01 | B064506 |  | MONITOR,TV:15 DEG TILE,15VDC,P4 PHOSPHOR | 80009 | 119-0363-01 |
| A13 | 670-2196-01 |  |  | CKT BOARD ASSY:POWER SUPPLY | 80009 | 670-2196-01 |
| A13 | 670-2196-02 |  |  | CKT BOARD ASSY:POWER SUPPLY | 80009 | 670-2196-02 |
| A13 | 670-2196-03 | B050000 |  | CKT BOARD ASSY: | 80009 | 670-2196-03 |
| A1 ASSEMBLY RAM |  |  |  |  |  |  |
| A1 | 670-2197-01 |  |  | CKT BOARD ASSY:RAM | 80009 | 670-2197-01 |
| A1 | 670-3197-01 |  |  | CKT BOARD ASSY:RAM | 80009 | 670-3197-01 |
| A1 | 670-3197-02 | B050000 |  | CKT CARD ASSY: | 80009 | 670-3197-02 |
| C1 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C21 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C41 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C55 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C65 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C92 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C181 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C202 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C221 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C223 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C224 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C231 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C232 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C245 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C261 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |



| Ckt No. | Tektronix Part No. | Serial/Model No. <br> Eff Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A1 RAM (CONT) |  |  |
| U31 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U41 | 307-0347-00 |  | RES.,FXD,FILM:13 RES NETWORK | 73138 | 899-1-R220 |
| U45 | 156-0032-03 |  | MICROCIRCUIT,DI:4 BIT BINARY COUNTER,SCRN | 07263 | 7493(PCQR) |
| U51 | 156-0125-02 |  | MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| U55 | 156-0150-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U61 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U65 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 $\times 1$ RANDOM ACCESS MEM | 50088 | MK400GP |
| U71 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U81 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U91 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U101 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U111 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U121 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U131 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U141 | 156-0150-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U145 | 156-0269-00 |  | MICROCIRCUIT,DI:DUAL CARRY SAVE FULL ADDER | 80009 | 156-0269-00 |
| U151 | 156-0269-00 |  | MICROCIRCUIT,DI:DUAL CARRY SAVE FULL ADDER | 80009 | 156-0269-00 |
| U155 | 156-0036-02 |  | MICROCIRCUIT,DI:DUAL 4-INPUT NAND BFR,SCRN | 01295 | SN7440(NP3 OR JP |
| U161 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U165 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U171 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U181 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U191 | 156-0179-00 |  | MICROCIRCUIT,DI:1024 X 1 RANDOM ACCESS MEM | 50088 | MK400GP |
| U201 | 156-0177-02 |  | MICROCIRCUIT,DI:DUAL LINE RCVR,SCRN | 01295 | SN75107A(NP3 OR |
| U221 | 156-0177-02 |  | MICROCIRCUIT,DI:DUAL LINE RCVR,SCRN | 01295 | SN75107A(NP3 OR |
| U241 | 156-0062-02 |  | MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE | 01295 | SN7486 |
| U245 | 156-0129-02 |  | MICROCIRCUIT, DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U251 | 156-0062-02 |  | MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE | 01295 | SN7486 |
| U255 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U261 | 307-0366-00 |  | RES.,FXD,FILM: 220 OHM, $2 \%, 15$ RES NETWORK | 91637 | MDP1601221G |
| U265 | 156-0177-02 |  | MICROCIRCUIT,DI:DUAL LINE RCVR,SCRN | 01295 | SN75107A(NP3 OR |
| U281 | 156-0177-02 |  | MICROCIRCUIT,DI:DUAL LINE RCVR,SCRN | 01295 | SN75107A(NP3 OR |
| U291 | 156-0177-02 |  | MICROCIRCUIT,DI:DUAL LINE RCVR,SCRN | 01295 | SN75107A(NP3 OR |
| U301 | 156-0032-03 |  | MICROCIRCUIT,DI:4 BIT BINARY COUNTER,SCRN | 07263 | 7493(PCQR) |
| U309 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U311 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U315 | 156-0140-02 |  | MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT | 01295 | SN7417 (NP3) |
| U321 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U331 | 156-0321-02 |  | MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE | 01295 | SN74S10 |
| U341 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U345 | 156-0043-03 |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U347 | 156-0035-00 |  | MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| U351 | 156-0034-02 |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U355 | 156-0150-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U361 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U365 | 156-0140-02 |  | MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT | 01295 | SN7417 (NP3) |
| U371 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U381 | 156-0140-02 |  | MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT | 01295 | SN7417 (NP3) |
| U391 | 156-0094-00 |  | MICROCIRCUIT,DI:DUAL PERIPHERAL DRIVER | 01295 | SN75451P |
| Y201 | 158-0072-00 |  | XTAL UNIT,QTZ:4.9152 MHZ,0.05\% | 33096 | ORD BY DESCR |


| Ckt No. | Tektronix Part No. | Serial/M <br> Eff | No. Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | A2 ASSEMBLY CURSOR |  |  |
| A2 | 670-2198-01 | B010100 | B049999 | CKT BOARD ASSY:CURSOR | 80009 | 670-2198-01 |
| A2 | 670-2198-02 | B050000 | B064267 | CKT BOARD ASSY: | 80009 | 670-2198-02 |
| A2 | 670-2198-03 | B064268 |  | CKT BOARD ASYY:CURSOR | 80009 | 670-2198-03 |
| C9 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C39 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF + +80-20\%,150V | 59821 | SDDH69J203Z |
| C69 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C101 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C129 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C139 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C151 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C171 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C211 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C239 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C249 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C269 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C309 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C331 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C339 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C371 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| R101 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R119 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R120 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R151 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R271 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| , |  |  |  |  |  |  |
| U1 | 156-0039-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U9 | 156-0047-02 |  |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| U11 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U19 | 156-0034-02 |  |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U21 | 156-0125-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| U29 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U31 | 156-0042-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE,FF,SCRN | 01295 | SN7476(NP3 OR JP |
| U39 | 156-0089-00 |  |  | MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| U41 | 156-0089-00 |  |  | MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| U49 | 156-0089-00 |  |  | MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| U51 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U61 | 156-0145-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U69 | 156-0145-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U71 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U101 | 156-0034-02 |  |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U109 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U111 | 156-0043-03 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U121 | 156-0089-00 |  |  | MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| U129 | 156-0043-03 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U131 | 156-0035-00 |  |  | MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| U139 | 156-0043-03 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U141 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U149 | 156-0125-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| U151 | 156-0125-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| U159 | 156-0221-00 |  |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U161 | 156-0125-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |


|  | Tektronix | Serial/Model No. |  |  | Mfr |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |


| MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| :---: | :---: | :---: |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA+ OR JA+ |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:DUAL 4 INP NOR GATE | 01295 | SN7425 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER | 80009 | 156-0089-00 |
| MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN | 01295 | SN74157(NP3 OR J |
| MICROCIRCUIT,DI:DUAL 4 INP NOR GATE | 01295 | SN7425 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE | 01295 | SN7486 |
| MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| MICROCIRCUIT,DI:DUAL 4 INP NOR GATE | 01295 | SN7425 |
| MICROCIRCUIT,DI:DUAL 4 INP NOR GATE | 01295 | SN7425 |
| MICROCIRCUIT, DI: QUAD 2 INP EXCL OR GATE | 07263 | $74 \mathrm{S86}$ |
| MICROCIRCUIT,DI:QUAD 2 INP EXCL OR GATE | 07263 | 74586 |
| MICROCIRCUIT, DI: QUAD 2-INP EXCL OR GATE | 01295 | SN7486 |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |


| Ckt No． | Tektronix Part No． | Serial／Model No． <br> Eff Dscont | Name \＆Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A4 ASSEMBLY KEYBOARD INTERFACE |  |  |
| A4 | 670－2301－01 |  | CKT BOARD ASSY：KEYBOARD INTERFACE | 80009 | 670－2301－01 |
| A4 | 670－2301－02 |  | CKT BOARD ASSY：KEYBOARD INTERFACE | 80009 | 670－2301－02 |
| A4 | 670－2301－03 |  | CKT BOARD ASSY：KEYBOARD INTERFACE | 80009 | 670－2301－03 |
| A4 | 670－2301－04 |  | CKT BOARD ASSY：KEYBOARD INTERFACE | 80009 | 670－2301－04＊ |
| A4 | 670－2301－06 | B050000 | CKT CARD ASSY： | 80009 | 670－2301－06 |
| A4 | 670－3428－00 |  | CKT BOARD ASSY：C．R． | 80009 | 670－3428－00 |
| C1 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C40 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C90 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C101 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C160 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C180 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C189 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C233 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C350 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C370 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C385 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，$+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C428 | 283－0004－00 |  | CAP．，FXD，CER DI：0．02UF，＋80－20\％，150V | 59821 | SDDH69J203Z |
| C429 | 283－0177－00 |  | CAP．，FXD，CER DI：1UF，＋80－20\％，25V | 56289 | 2C20Z5U105Z025B |
| CR395 | 152－0075－00 |  | SEMICOND DEVICE：GE，25V，40MA | 14433 | G866 |
| CR395 | －－－－－－－－－－ |  | （CR395，－03 AND UP BOARDS ONLY） |  |  |
| CR409 | 152－0141－02 |  | SEMICOND DEVICE：SILICON，30V，150MA | 01295 | 1N4152R |
| Q401 | 151－0254－00 |  | TRANSISTOR：SILICON，NPN | 03508 | X38L3118 |
| Q402 | 151－0302－00 |  | TRANSISTOR：SILICON，NPN | 07263 | S038487 |
| Q403 | 151－0302－00 |  | TRANSISTOR：SILICON，NPN | 07263 | S038487 |
| ． |  |  |  |  |  |
| R71 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R75 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R91 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R159 | 315－0472－00 |  | RES．，FXD，CMPSN：4．7K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB4725 |
| R190 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM，5\％，0．25W | 01121 | CB1025 |
| R335 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM，5\％，0．25W | 01121 | CB1025 |
| R391 | 315－0102－00 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R394 | 315－0102－03 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R394 | －ーカーー－－－－ |  | （R394，－03 AND UP BOARDS ONLY） |  |  |
| R396 | 315－0102－03 |  | RES．，FXD，CMPSN：1K OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R396 | － |  | （R396，－03 AND UP BOARDS ONLY） |  |  |
| R401 | 315－0271－00 |  | RES．，FXD，CMPSN：270 OHM，5\％，0．25W | 01121 | CB2715 |
| R411 | 315－0110－00 |  | RES．，FXD，CMPSN： 11 OHM， $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1105 |
| R412 | 315－0391－00 |  | RES．，FXD，CMPSN：390 OHM，5\％，0．25W | 01121 | CB3915 |
| R413 | 315－0391－00 |  | RES．，FXD，CMPSN：390 OHM，5\％，0．25W | 01121 | CB3915 |
| R414 | 315－0684－00 |  | RES．，FXD，CMPSN：680K OHM，5\％，0．25W | 01121 | CB6845 |
| R415 | 315－0331－00 |  | RES．，FXD，CMPSN：330 OHM，5\％，0．25W | 01121 | CB3315 |
| － |  |  |  |  |  |
| S1－S75 | 260－1393－00 |  | SWITCH，PUSH：SPST，NO KEYBOARD SWITCH | 01963 | M61－0100 |
| S1－S75 | －－－－－－－－－ |  | （S1－S75，260－1393－01（HEAVY DUTY），MAY BE USED |  |  |
| U1 | 156－0035－00 |  | MICROCIRCUIT，DI：SGL 8－INPUT POS NAND GATE | 80009 | 156－0035－00 |
| U9 | 307－0349－00 |  | RES．，FXD，FILM：13 RES．NTWK，1K OHM，2\％，0．12 | 73138 | 899－1－R1K |
| U29 | 156－0043－03 |  | MICROCIRCUIT，DI：QUAD 2－INP NOR GATE，SCRN | 01295 | SN7402 |
| U31 | 156－0058－02 |  | MICROCIRCUIT，DI：HEX INVRTR，SCREENED | 01295 | SN7404 |


| Ckt No. | Tektronix Part No. | Serial/Model No. <br> Eff Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A4 ASSEMBLY KEYBOARD INTERFACE (CONT) |  |  |
| U39 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U41 | 156-0171-02 |  | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U49 | 156-0034-02 |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U51 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U61 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U69 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U79 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U81 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U89 | 156-0032-03 |  | MICROCIRCUIT,DI:4 BIT BINARY COUNTER,SCRN | 07263 | 7493(PCQR) |
| U91 | 156-0047-02 |  | MICROCIRCUIT, DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| U101 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U109 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U129 | 156-0061-02 |  | MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| U131 | 156-0061-02 |  | MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| U139 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U141 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U149 | 156-0171-02 |  | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U161 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U169 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U171 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U179 | 156-0163-02 |  | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| U181 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U189 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U191 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U201 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U209 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U229 | 156-0035-00 |  | MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| U231 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U239 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U241 | 156-0163-02 |  | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| U249 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U251 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U261 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| U269 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U271 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U279 | 156-0032-03 |  | MICROCIRCUIT,DI:4 BIT BINARY COUNTER,SCRN | 07263 | 7493(PCQR) |
| U281 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U289 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U291 | 156-0039-02 |  | MICROCIRCUIT, DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U301 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U309 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U329 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U331 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U339 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U341 | 156-0034-02 |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U349 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U351 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U361 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U369 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U371 | 156-0093-02 |  | MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| U379 | 156-0093-02 |  | MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| U381 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |

$\left.\begin{array}{llllll} & \begin{array}{l}\text { Tektronix } \\ \text { Ckt No. }\end{array} & \begin{array}{l}\text { Serial/Model No. } \\ \text { Eff }\end{array} & \text { Dscont }\end{array}\right]$

|  | Tektronix | Serial/Model No. |  |  | Mfr |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |  |  |  |
| :--- | :--- | :--- | :--- |

A5 ASSEMBLY EDIT

| A5 | 670-2200-03 |  | CKT BOARD ASSY:EDIT | 80009 | 670-2200-03 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A5 | 670-2200-04 |  | CKT BOARD ASSY:EDIT | 80009 | 670-2200-04 |
| A5 | 670-2200-06 | 8050000 | CKT BOARD ASSY: | 80009 | 670-2200-06 |
| C31 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C51 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C71 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C89 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C109 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C129 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C149 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF $,+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C169 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C201 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C231 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C249 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C261 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C279 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C339 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C371 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + $80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C381 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C401 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C431 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C451 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| R90 | 315-0102-03 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R90 | --------- |  | (R90, -04 AND UP BOARDS ONLY) |  |  |
| R295 | 315-0102-03 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R295 | --------- |  | (R295, -04 AND UP BOARDS ONLY) |  |  |
| R489 | 315-0102-03 |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| . |  |  |  |  |  |
| U1 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U9 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U29 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U31 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U39 | 156-0036-02 |  | MICROCIRCUIT,DI:DUAL 4-INPUT NAND BFR,SCRN | 01295 | SN7440(NP3 OR JP |
| U41 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U49 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U51 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U61 | 156-0034-02 |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U69 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U71 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U79 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| U81 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U89 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| U91 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U99 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U101 | 156-0163-02 |  | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| U109 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| U129 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U131 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| U139 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U141 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U149 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |


|  | Tektronix | Serial/Model No. |  |  | Mfr |
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| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |  |  |  |
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| A5 ASSEMBLY EDIT (CONT) |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| U151 | 156-0039-02 | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U161 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U169 | 156-0039-02 | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U171 | 156-0039-02 | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U179 | 156-0041-05 | MICROCIRCUIT,DI:DUAL D.FLIP FLOP | 01295 | SN7474 |
| U181 | 156-0165-02 | MICROCIRCUIT,DI:DUAL 4 INP NOR GATE | 01295 | SN7425 |
| U189 | 156-0129-02 | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U191 | 156-0163-02 | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| U199 | 156-0043-03 | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U201 | 156-0079-02 | MICROCIRCUIT,DI:DECADE COUNTER,SCREENED | 01295 | SN7490A(NP3 OR J |
| U209 | 156-0171-02 | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U229 | 156-0221-00 | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U231 | 156-0034-02 | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U239 | 156-0047-02 | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| U241 | 156-0163-02 | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| U249 | 156-0039-02 | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U251 | 156-0222-02 | MICROCIRCUIT,DI:HEX D LATCH W/CLEAR,TTL | 01295 | SN74174(NP3 OR J |
| U261 | 156-0222-02 | MICROCIRCUIT,DI:HEX D LATCH W/CLEAR,TTL | 01295 | SN74174(NP3 OR J |
| U269 | 156-0221-00 | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U271 | 156-0171-02 | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U279 | 156-0043-03 | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U281 | 156-0129-02 | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U289 | 156-0178-02 | MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE,TTL | 01295 | SN7427(NP3 OR JP |
| U291 | 156-0042-02 | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE,FF,SCRN | 01295 | SN7476(NP3 OR JP |
| U301 | 156-0030-00 | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U309 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U329 | 156-0034-02 | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U331 | 156-0043-03 | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U339 | 156-0030-00 | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U341 | 156-0129-02 | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U349 | 156-0144-00 | MICROCIRCUIT,DI:3-INPUT POS NAND GATE | 80009 | 156-0144-00 |
| U351 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U361 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U369 | 156-0221-00 | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U371 | 156-0061-02 | MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| U379 | 156-0171-02 | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U381 | 156-0034-02 | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U389 | 156-0171-02 | MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,SCRN | 01295 | SN7432 |
| U391 | 156-0034-02 | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U399 | 156-0129-02 | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U401 | 307-0349-00 | RES.,FXD,FILM: 13 RES. NTWK,1K OHM, $2 \%, 0.12$ | 73138 | 899-1-R1K |
| U409 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U429 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U431 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U439 | 156-0093-02 | MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| U441 | 156-0058-02 | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U449 | 156-0093-02 | MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| U451 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U461 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U469 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U471 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U479 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U481 | 156-0034-02 | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U489 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U491 | 156-0145-02 | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U499 | 156-0041-05 | MICROCIRCUIT,DI:OUAL D-FLIP FLOP | 01295 | SN7474 |


|  | Tektronix | Serial/Model No. |  |  | Mfr |  |
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| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |


| A6 | 670-2542-02 |  | CKT BOARD ASSY:CONTROL | 80009 | 670-2542-02 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A6 | 670-2542-04 | B050000 | CKT CARD ASSY: | 80009 | 670-2542-04 |
| C7 | 290-0530-00 |  | CAP.,FXD,ELCTLT:68UF,20\%,6V | 90201 | TDC686M006NLF |
| C9 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C49 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C101 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%$,150V | 59821 | SDDH69J203z |
| C145 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C279 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203z |
| C289 | 283-0004-00 |  | CAP.,FXD, CER DI:0.02UF, $+80-20 \%$,150V | 59821 | SDDH69J203Z |
| C329 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C331 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J2032 |
| C365 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%$,150V | 59821 | SDDH69J203Z |
| C371 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%$,150V | 59821 | SDDH69J203Z |
| C401 | 283-0004-00 |  | CAP.,FXD, CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C419 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203z |
| C445 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C461 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, + 80-20\%,150V | 59821 | SDDH69J203Z |
| C479 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C491 | 283-0004-00 |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| R7 | 315-0103-00 |  | RES.,FXD,CMPSN: 10 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1035 |
| R95 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R101 | 307-0349-00 |  | RES.,FXD,FILM:13 RES. NTWK,1K OHM,2\%,0.12 | 73138 | 899-1-R1K |
| R195 | 315-0102-03 |  | RES.,FXD,CMPSN:1K OHM, 5\%,0.25W | 01121 | CB1025 |
| R395 | 315-0102-00 |  | RES.,FXD,CMPSN:1K ОHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R495 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| u9 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U29 | 156-0163-02 |  | MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411 (PCQR OR DCQ |
| U31 | 156-0072-02 |  | MICROCIRCUIT,DI:MONOSTABLE MV,BURN-IN | 01295 | SN74121 |
| U39 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U41 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U49 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U51 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U59 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U61 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U69 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U71 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA+ OR JA+ |
| 479 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| 481 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| 489 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| 491 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U109 | 156-0043-03 |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U129 | 156-0041-05 |  | MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| U131 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U139 | 156-0178-02 |  | MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE,TTL | 01295 | SN7427(NP3 OR JP |
| U141 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| $\cup 149$ | 156-0043-03 |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U151 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U159 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U161 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U169 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |


|  | Tektronix | Serial/Model No. |  |  | Mfr |  |
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| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |


| U171 | 156-0030-00 |
| :---: | :---: |
| U179 | .156-0035-00 |
| U181 | 156-0058-02 |
| U189 | 156-0039-02 |
| U191 | 156-0041-05 |
| U201 | 156-0129-02 |
| U209 | 156-0047-02 |
| U229 | 156-0041-05 |
| U231 | 156-0047-02 |
| U239 | 156-0030-00 |
| U241 | 156-0058-02 |
| U249 | 156-0035-00 |
| U251 | 156-0035-00 |
| U259 | 156-0030-00 |
| U261 | 156-0058-02 |
| U269 | 156-0030-00 |
| U271 | 156-0047-02 |
| U279 | 156-0035-00 |
| U281 | 156-0061-02 |
| U289 | 156-0030-00 |
| U291 | 156-0129-02 |
| U301 | 156-0043-03 |
| U309 | 156-0039-02 |
| U339 | 156-0034-02 |
| U341 | 156-0061-02 |
| U359 | 156-0129-02 |
| U361 | 156-0129-02 |
| U369 | 156-0030-00 |
| U371 | 156-0043-03 |
| U379 | 156-0093-02 |
| U381 | 156-0221-00 |
| U389 | 156-0163-02 |
| U391 | 156-0221-00 |
| U401 | 156-0093-02 |
| U409 | 156-0145-02 |
| U429 | 156-0093-02 |
| U431 | 156-0093-02 |
| U439 | 156-0093-02 |
| U449 | 156-0058-02 |
| U451 | 156-0058-02 |
| U459 | 156-0145-02 |
| U461 | 156-0093-02 |
| U469 | 156-0145-02 |
| U471 | 156-0145-02 |
| U479 | 156-0163-02 |
| U481 | 156-0058-02 |
| U489 | 156-0093-02 |
| U491 | 156-0145-02 |


| A6 ASSEMBLY CONTROL (CONT) |  |  |
| :---: | :---: | :---: |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA+ OR JA+ |
| MICROCIRCUIT,DI:DUAL D-FLIP FLOP | 01295 | SN7474 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA + |
| MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| MICROCIRCUIT, DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| MICROCIRCUIT,DI:TPL 3-INP \& GATE,SCRN | 07263 | 7411(PCQR OR DCQ |
| MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |


|  | Tektronix | Serial/Model No. |  |  | Mfr |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number


|  |  |  |  | A7 ASSEmbly timing |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A7 | 670-2199-02 |  |  | CKT Board assy:TIMING | 80009 | 670-2199-02 |
| A7 | 670-2199-03 |  |  | CKT BOARD ASSY:TIMING | 80009 | 670-2199-03 |
| A7 | 670-2199-04 |  |  | CKT BOARD ASSY:TIMING | 80009 | 670-2199-04 |
| A7 | 670-2199-05 | B020545 | B049999 | CKT BOARD ASSY:TIMING | 80009 | 670-2199-05 |
| A7 | 670-2199-07 | B050000 |  | CKT BOARD ASSY: | 80009 | 670-2199-07 |
| C11 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C69 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C87 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C90 | 281-0523-00 |  |  | CAP.,FXD,CER DI: $100 \mathrm{PF},+/$-20PF, 500 V | 72982 | 301-000U2M0101M |
| C91 | 283-0107-00 |  |  | CAP.,FXD,CER DI:51PF,5\%,200V | 96733 | R3017 |
| C95 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C98 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C99 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C121 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C159 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF,+80-20\%,150V | 59821 | SDDH69J203Z |
| C169 | 283-0004-00 |  |  | CAP.,FXD,CER DI: $0.02 \mathrm{UF},+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C189 | 283-0107-00 |  |  | CAP.,FXD,CER DI:51PF,5\%,200V | 96733 | R3017 |
| C199 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C221 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF,+80-20\%,150V | 59821 | SDDH69J203Z |
| C251 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C269 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C289 | 281-0546-00 |  |  | CAP.,FXD,CER DI:330PF, $10 \%$,500V | 04222 | 7001-1380 |
| C291 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C296 | 283-0178-00 | B020545 |  | CAP.,FXD,CER DI:0.1UF, +80-20\%,100V | 72982 | 8131N145651 $104 Z$ |
| C390 | 283-0004-00 |  |  | CAP.,FXD, CER DI:0.02UF, +80-20\%,150V | 59821 | SDDH69J203Z |
| C399 | 290-0530-00 | B010100 | B020544 | CAP.,FXD,ELCTLT:68UF,20\%,6V | 90201 | TDC686M006NLF |
| C411 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF,+80-20\%,150V | 59821 | SDDH69J203Z |
| C461 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | SDDH69J203Z |
| C469 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF,+80-20\%,150V | 59821 | SDDH69J2032 |
| C492 | 283-0004-00 |  |  | CAP.,FXD,CER DI:0.02UF,+80-20\%,150V | 59821 | SDDH69J203Z |
| C495 | 283-0203-00 | B020545 |  | CAP.,FXD,CER DI: $0.47 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 72982 | 8131 M 05825 U 0474 M |
| CR91 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR397 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V, 150MA | 01295 | 1N4152R |
| CR399 | 152-0141-02 | B010100 | B020544 | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR496 | 152-0141-02 | B020545 |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR497 | 152-0141-02 | B020545 |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| L90 | 108-0419-00 |  |  | COIL,RF:FIXED,1.1UH | 80009 | 108-0419-00 |
| L189 | 108-0419-00 |  |  | COIL,RF:FIXED,1.1UH | 80009 | 108-0419-00 |
| Q90 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q92 | 151-0190-02 |  |  | TRANSISTOR:SILICON,NPN | 04713 | SM7706 |
| Q94 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q96 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q98 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q199 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q397 | 151-0188-00 |  |  | TRANSISTOR:SILICON,PNP | 04713 | SPS6868K |
| Q398 | 151-0190-02 |  |  | TRANSISTOR:SILICON,NPN | 04713 | SM7706 |
| Q399 | 151-0190-02 | B020545 |  | TRANSISTOR:SILICON,NPN | 04713 | SM7706 |
| R65 | 315-0102-00 |  |  | RES.,FXD,CMPSN: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |


| Ckt No. | Tektronix Part No. | $\begin{array}{ll}\text { Serial/Model No. } \\ \text { Eff } & \text { Dscont }\end{array}$ | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A7 TIMING (CONT) |  |  |
| R75 | 315-0103-00 |  | RES.,FXD,CMPSN:10K OHM,5\%,0.25W | 01121 | CB1035 |
| R79 | 315-0511-00 |  | RES.,FXD,CMPSN: 510 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5115 |
| R81 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R90 | 315-0750-00 |  | RES.,FXD,CMPSN: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB7505 |
| R91 | 315-0221-00 |  | RES.,FXD,CMPSN: 220 OHM,5\%,0.25W | 01121 | CB2215 |
| R92 | 315-0750-00 |  | RES.,FXD,CMPSN:75 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB7505 |
| R93 | 315-0152-00 |  | RES.,FXD,CMPSN:1.5K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1525 |
| R94 | 315-0391-00 |  | RES.,FXD,CMPSN:390 OHM,5\%,0.25W | 01121 | CB3915 |
| R95 | 315-0101-00 |  | RES.,FXD,CMPSN: 100 OHM,5\%,0. 25 W | 01121 | CB1015 |
| R96 | 315-0750-00 |  | RES.,FXD,CMPSN:75 OHM,5\%,0.25W | 01121 | CB7505 |
| R97 | 315-0152-00 |  | RES.,FXD,CMPSN: 1.5 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1525 |
| R98 | 315-0391-00 |  | RES.,FXD,CMPSN:390 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB3915 |
| R99 | 315-0101-00 |  | RES.,FXD,CMPSN: 100 OHM, 5\%,0. 25 W | 01121 | CB1015 |
| R111 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R190 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R191 | 315-0620-00 |  | RES.,FXD,CMPSN: 62 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6205 |
| R192 | 315-0430-00 |  | RES.,FXD,CMPSN: 43 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB4305 |
| R193 | 315-0561-00 |  | RES.,FXD,CMPSN: $560 \mathrm{OHM}, 5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5615 |
| R194 | 315-0361-00 |  | RES.,FXD,CMPSN:360 OHM,5\%,0.25W | 01121 | CB3615 |
| R195 | 315-0620-00 |  | RES.,FXD,CMPSN: 62 OHM,5\%,0.25W | 01121 | CB6205 |
| R196 | 315-0430-00 |  | RES.,FXD,CMPSN: 43 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB4305 |
| R197 | 315-0561-00 |  | RES.,FXD,CMPSN: $560 \mathrm{OHM}, 5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5615 |
| R198 | 315-0361-00 |  | RES.,FXD,CMPSN:360 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB3615 |
| R199 | 315-0101-00 |  | RES.,FXD,CMPSN: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1015 |
| R231 | 315-0102-00 |  | RES.,FXD,CMPSN: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R251 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R252 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R253 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R291 | 315-0221-00 |  | RES.,FXD,CMPSN: 220 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2215 |
| R292 | 315-0680-00 |  | RES.,FXD,CMPSN: 68 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6805 |
| R293 | 315-0222-00 |  | RES.,FXD,CMPSN:2.2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2225 |
| R294 | 315-0221-00 |  | RES.,FXD,CMPSN:220 OHM,5\%,0.25W | 01121 | CB2215 |
| R294 | -----.--- |  | (-02, -03 BOARDS ONLY) |  |  |
| R294 | 315-0431-00 |  | RES.,FXD,CMPSN: 430 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB4315 |
| R294 | ----- |  | (-04 AND UP BOARDS ONLY) |  |  |
| R295 | 315-0152-00 |  | RES.,FXD,CMPSN: 1.5 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1525 |
| R295 | --------- |  | (-02, -03 BOARDS ONLY) |  |  |
| R295 | 315-0561-00 |  | RES.,FXD,CMPSN: 560 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5615 |
| R295 | ---------- |  | (-04 AND UP BOARDS ONLY) |  |  |
| R296 | 315-0221-00 |  | RES.,FXD,CMPSN:220 OHM, 5\%,0.25W | 01121 | CB2215 |
| R297 | 315-0680-00 |  | RES.,FXD,CMPSN: 68 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6805 |
| R298 | 315-0222-00 |  | RES.,FXD,CMPSN:2.2K OHM,5\%,0.25W | 01121 | CB2225 |
| R300 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R301 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R321 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R371 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R389 | 315-0221-00 |  | RES.,FXD,CMPSN: 220 OHM, 5\%,0.25W | 01121 | CB2215 |
| R390 | 315-0102-03 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R390 | --------- |  | (R390, -03, -04 BOARDS ONLY) |  |  |
| R391 | 315-0681-00 |  | RES.,FXD,CMPSN: 680 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6815 |
| R392 | 315-0122-00 |  | RES.,FXD,CMPSN:1.2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1225 |
| R393 | 315-0511-00 |  | RES.,FXD,CMPSN:510 OHM,5\%,0.25W | 01121 | CB5115 |


| Ckt No. | Tektronix Part No. | Serial/Mo <br> Eff | No. Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | A7 TIMING (CONT) |  |  |
| R394 | 315-0561-00 |  |  | RES.,FXD,CMPSN:560 OHM,5\%,0.25W | 01121 | CB5615 |
| R395 | 315-0681-00 |  |  | RES.,FXD,CMPSN: 680 OHM,5\%,0.25W | 01121 | CB6815 |
| R396 | 315-0391-00 |  |  | RES.,FXD,CMPSN:390 OHM,5\%,0.25W | 01121 | CB3915 |
| R397 | 315-0221-00 |  |  | RES.,FXD,CMPSN: 220 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2215 |
| R398 | 315-0182-00 |  |  | RES.,FXD,CMPSN:1.8K OHM,5\%,0.25W | 01121 | CB1825 |
| R399 | 315-0103-03 |  |  | RES.,FXD,CMPSN:10K OHM,5\%,0.25W | 01121 | CB1035 |
| R399 | --- |  |  | (-03, -04 BOARDS ONLY) |  |  |
| R399 | 315-0101-03 |  |  | RES.,FXD,CMPSN: 100 OHM,5\%,0.25W | 01121 | CB1015 |
| R399 | --------- |  |  | (-05 AND UP BOARDS ONLY) |  |  |
| R400 | 315-0331-00 |  |  | RES.,FXD,CMPSN: 330 OHM,5\%,0.25W | 01121 | CB3315 |
| R400 | ----- ----- |  |  | (-03, -04 BOARDS ONLY) |  |  |
| R400 | 315-0221-03 |  |  | RES.,FXD,CMPSN:220 OHM,5\%,0.25W | 01121 | CB2215 |
| R400 | --- |  |  | (-05 AND UP BOARDS ONLY) |  |  |
| R401 | 315-0102-00 |  |  | RES.,FXD,CMPSN: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R489 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R496 | 315-0222-00 |  |  | RES.,FXD,CMPSN:2.2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2225 |
| R496 | ---------- |  |  | (R496, -05 AND UP BOARDS ONLY) |  |  |
|  |  |  |  |  |  |  |
| U1 | 156-0117-00 |  |  | MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER | 80009 | 156-0117-00 |
| U11 | 156-0117-00 |  |  | MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER | 80009 | 156-0117-00 |
| U21 | 156-0117-00 |  |  | MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER | 80009 | 156-0117-00 |
| U31 | 156-0117-00 |  |  | MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER | 80009 | 156-0117-00 |
| U41 | 156-0117-00 |  |  | MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER | 80009 | 156-0117-00 |
| U51 | 156-0034-02 |  |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U55 | 156-0035-00 |  |  | MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| U61 | 156-0039-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U69 | 156-0030-00 | B010100 | B020544 | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U69 | 156-0150-02 | B020545 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U71 | 156-0032-03 |  |  | MICROCIRCUIT,DI:4 BIT BINARY COUNTER,SCRN | 07263 | 7493(PCQR) |
| U81 | 156-0039-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U89 | 156-0118-03 |  |  | MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN | 01295 | SN74S112JP3 |
| U101 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U111 | 156-0129-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U121 | 156-0039-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U131 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U141 | 156-0043-03 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U151 | 156-0034-02 |  |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U161 | 156-0321-02 |  |  | MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE | 01295 | SN74S10 |
| U169 | 156-0039-02 |  |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U171 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U181 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U189 | 156-0150-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U191 | 156-0180-04 |  |  | MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE | 01295 | SN74S00NP3 |
| U201 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U211 | 156-0036-02 |  |  | MICROCIRCUIT,DI:DUAL 4-INPUT NAND BFR,SCRN | 01295 | SN7440(NP3 OR JP |
| U221 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U231 | 156-0035-00 |  |  | MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE | 80009 | 156-0035-00 |
| U241 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U251 | 156-0047-02 |  |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA+ OR JA+ |
| U261 | 156-0221-00 |  |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U269 | 156-0034-02 |  |  | MICROCIRCUIT,DI:DUAL 4 INP NAND GATE,SCRN | 01295 | SN7420(NP3 OR JP |
| U271 | 156-0030-00 |  |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |


| Ckt No. | Tektronix Part No. | Serial/Model No. <br> Eff Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A7 TIMING (CONT) |  |  |
| U281 | 156-0180-04 |  | MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE | 01295 | SN74S00NP3 |
| U289 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U291 | 156-0093-02 |  | MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN | 01295 | SN74LS00 (NP3) |
| U295 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U301 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U311 | 156-0036-02 |  | MICROCIRCUIT,DI:DUAL 4-INPUT NAND BFR,SCRN | 01295 | SN7440(NP3 OR JP |
| U321 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U331 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U341 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U351 | 156-0079-02 |  | MICROCIRCUIT,DI:DECADE COUNTER,SCREENED | 01295 | SN7490A(NP3 OR J |
| U359 | 156-0039-02 |  | MICROCIRCUIT,DI:DUAL J-K MA-SLAVE FF,SCRN | 01295 | SN7473(NP3 OR JP |
| U361 | 156-0043-03 |  | MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN | 01295 | SN7402 |
| U369 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U371 | 156-0062-02 |  | MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE | 01295 | SN7486 |
| U381 | 156-0047-02 |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA+ OR JA+ |
| U389 | 156-0146-02 |  | MICROCIRCUIT,DI: 8 BIT PAR-IN SER OUT SR,SCR | 01295 | SN74165(NP3 OR J |
| U395 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U401 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U411 | 156-0180-04 |  | MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE | 01295 | SN74S00NP3 |
| U421 | 156-0058-02 |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| U431 | 156-0150-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BUFFER,SCRN | 01295 | SN7437(NP3 OR JP |
| U441 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U451 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U461 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U469 | 156-0030-00 |  | MICROCIRCUIT,DI:UAD 2 INPUT NAND GATE |  | SN7400 |
| U471 | 156-0145-02 |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| U481 | 156-0221-00 |  | MICROCIRCUIT,DI:QUAD LATCH | 01295 | SN74175N |
| U489 | 156-0129-02 |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| U491 | 156-0147-00 |  | MICROCIRCUIT,DI:ROM $64 \times 5 \times 7$ CHAR GEN | 80009 | 156-0147-00 |
| U495 | 307-0349-00 |  | RES.,FXD,FILM:13 RES. NTWK,1K OHM,2\%,0.12 | 73138 | 899-1-R1K |
| U499 | 156-0401-00 |  | MICROCIRCUIT,DI:ROM,5X7 LC ALPHA | 80009 | 156-0401-00 |
| Y89 | 158-0081-00 |  | XTAL UNIT,QTZ:22.008MHZ,+/-0.01\% | 33096 | PB3086 |


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| Ckt No. | Tektronix Part No. | Serial/Model No. |  | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | A11 ASSEMBLY KEYBOARD |  |  |
| A11 | 119-0374-01 | B010100 | B063619 | KEYBOARD,CMPTR:72 KEY,TTY,ASCII ENCODED | 52833 | 65-0763-01 |
| A11 | 119-0374-09 | B063620 |  | KEYBOARD ASSY: | 80009 | 119-0374-09 |
| C1 | 290-0536-00 |  |  | CAP.,FXD,ELCTLT:10UF,20\%,25V | 90201 | TDC106M025FL |
| C2 | 283-0003-00 |  |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | 2DDH66J103Z |
| C3 | 283-0003-00 |  |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | 2DDH66J103Z |
| C4 | 283-0003-00 |  |  | CAP.,FXD,CER DI:0.01UF, +80-20\%,150V | 59821 | 2DDH66J103Z |
| C5 | 283-0003-00 |  |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | 2DDH66J103Z |
| C6 | 285-1134-00 |  |  | CAP.,FXD,PLSTC:0.1UF,0.5\%,100V | 50558 | MH12D104J |
| C7 | 283-0175-00 |  |  | CAP.,FXD,CER DI:10PF,5\%,200V | 96733 | TDR43BY100DP |
| C8 | 290-0524-00 |  |  | CAP.,FXD,ELCTLT:4.7UF,20\%,10V | 90201 | TDC475M010EL |
| C9 | 283-0077-00 |  |  | CAP.,FXD,CER DI:330PF,5\%,500V | 59660 | 831-500B331J |
| C10 | 283-0092-00 |  |  | CAP.,FXD,CER DI:0.03UF, +80-20\%,200V | 59660 | 845-534Z5U0303Z |
| C11 | 285-1134-00 |  |  | CAP.,FXD,PLSTC: 0.1 UF, $0.5 \%, 100 \mathrm{~V}$ | 50558 | MH12D104J |
| CR1 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR2 | 152-0186-00 |  |  | SEMICOND DEVICE:GERMANIUM,80V,10PA | 18796 | 1N198 |
| CR3 | 152-0186-00 |  |  | SEMICOND DEVICE:GERMANIUM, 80V,10PA | 18796 | 1N198 |
| CR4 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR5 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR6 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR7 | 152-0186-00 |  |  | SEMICOND DEVICE:GERMANIUM, 80V,10PA | 18796 | 1N198 |
| CR8 | 152-0186-00 |  |  | SEMICOND DEVICE:GERMANIUM,80V,10PA | 18796 | 1N198 |
| CR9 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| Q1 | 151-0302-00 |  |  | TRANSISTOR:SILICON,NPN | 07263 | S038487 |
| Q2 | 151-0410-00 |  |  | TRANSISTOR:SILICON,PNP | 80009 | 151-0410-00 |
| Q3 | 151-0410-00 |  |  | TRANSISTOR:SILICON,PNP | 80009 | 151-0410-00 |
| Q4 | 151-0302-00 |  |  | TRANSISTOR:SILICON,NPN | 07263 | S038487 |
| R1 | ----- ----- |  |  | SELECTED |  |  |
| R2 | 315-0105-00 |  |  | RES.,FXD,CMPSN:1M OHM,5\%,0.25W | 01121 | CB1055 |
| R3 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R4 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R5 | 315-0204-00 |  |  | RES.,FXD,CMPSN:200K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2045 |
| R6 | 315-0475-00 |  |  | RES.,FXD,CMPSN:4.7M OHM,5\%,0.25W | 01121 | CB4755 |
| R7 | ----- ----- |  |  | SELECTED |  |  |
| R8 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM,5\%,0.25W | 01121 | CB6825 |
| R9 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM,5\%,0.25W | 01121 | CB6825 |
| R10 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R11 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R12 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R13 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM,5\%,0.25W | 01121 | CB6825 |
| R14 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R15 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM,5\%,0.25W | 01121 | CB6825 |
| R16 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R17 | 315-0682-00 |  |  | RES.,FXD,CMPSN:6.8K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6825 |
| R18 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R19 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM,5\%,0.25W | 01121 | CB2025 |
| R20 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, 5\%,0.25W | 01121 | CB2025 |
| R21 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R22 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R23 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM,5\%,0.25W | 01121 | CB2025 |


| Ckt No. | Tektronix Part No. | Serial/Mo <br> Eff | No. Dscont | Name \& Description | Mfr Code | Mfr Part Number |
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|  |  |  |  | A11 ASSEMBLY KEYBOARD (CONT) |  |  |
| R24 | 315-0102-00 |  |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R25 | --------- |  |  | SELECTED |  |  |
| R26 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM,5\%,0.25W | 01121 | CB2025 |
| R27 | 315-0333-00 |  |  | RES.,FXD,CMPSN:33K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB3335 |
| R28 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R30 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB2025 |
| R31 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM,5\%,0.25W | 01121 | CB2025 |
| R32 | 315-0204-00 |  |  | RES.,FXD,CMPSN:200K OHM,5\%,0.25W | 01121 | CB2045 |
| R33 | 315-0105-00 |  |  | RES.,FXD,CMPSN:1M OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1055 |
| R34 | 315-0202-00 |  |  | RES.,FXD,CMPSN:2K OHM,5\%,0.25W | 01121 | CB2025 |
| SW1 | 260-1507-00 |  |  | SWITCH,REED:SPST | 52833 | 60-0003-01 |
| Z1 | 156-0393-00 |  |  | MICROCIRCUIT,DI:CLOCK GENERATOR/DRIVER | 80009 | 156-0393-00 |
| Z2 | 118-0001-00 | B010100 | B063619 | MICROCIRCUIT,DI:KEYBOARD ENCODER MOS TECH | 51284 | MCS-1009-012 |
| Z2 | 118-0430-00 | B063620 |  | MICROCIRCUIT,DI:KEYBOARD ENCODER | 52833 | 20-3600-00 |
| Z3 | 156-0129-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP \& GATE,BURN-IN | 27014 | DM8008 |
| Z4 | 156-0061-02 |  |  | MICROCIRCUIT,DI:BCD TO DEC DCDR,BURN-IN | 27014 | DM8842 |
| Z5 | 156-0111-00 |  |  | MICROCIRCUIT,DI:SGL BCD-TO-DEC DEC/DRIVER | 80009 | 156-0111-00 |
| Z6 | 156-0113-03 |  |  | MICROCIRCUIT,DI:QUAD 2 INP NAND GATE,SCRN, | 01295 | SN74LOONP3 |
| Z7 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| Z8 | 156-0047-02 |  |  | MICROCIRCUIT,DI:TP1 3 INP,NAND GATE | 27014 | DM7410NA + OR JA+ |
| Z9 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| Z10 | 156-0145-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| Z11 | 156-0058-02 |  |  | MICROCIRCUIT,DI:HEX INVRTR,SCREENED | 01295 | SN7404 |
| Z12 | 156-0186-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND GATE,SCRN | 01295 | SN7403(NP3 OR JP |
| Z13 | 156-0186-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND GATE,SCRN | 01295 | SN7403(NP3 OR JP |
| Z14 | 156-0145-02 |  |  | MICROCIRCUIT,DI:QUAD 2-INP NAND BFR | 01295 | SN7438 |
| VR1 | 152-0278-00 |  |  | SEMICOND DEVICE:ZENER,0.4W, $3 \mathrm{~V}, 5 \%$ | 04713 | SZG35009K20 |


|  | Tektronix | Serial/Model No. |  |  | Mfr |
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| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |  |  |  |  |
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|  |  |  |  | A12 ASSEMBLY TV MONITOR |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12 | 119-0363-00 | B010100 | B064505 | MONITOR,TV:15 DEG TILT,15VDC,P4 PHOSPH | 17954 | TV-12C7-012-0124 |
| A12 | 119-0363-01 | B064506 |  | MONITOR,TV:15 DEG TILT,15VDC,P4 PHOSPHOR | 80009 | 119-0363-01 |
| C101 | 281-0751-00 |  |  | CAP.,FXD,CER DI:0.01UF,1000V | 17954 | 1-012-0112 |
| C102 | 281-0751-00 |  |  | CAP.,FXD,CER DI:0.01UF,1000V | 17954 | 1-012-0112 |
| C103 | 281-0751-00 |  |  | CAP.,FXD,CER DI:0.01UF,1000V | 17954 | 1-012-0112 |
| C104 | 283-0067-00 |  |  | CAP.,FXD,CER DI:0.001UF,10\%,200V | 59660 | 835-515-Z5D0102K |
| C105 | 285-0898-00 |  |  | CAP.,FXD,PLSTC:0.47UF,10\%,100V | 56289 | LP66A1B474K |
| C106 | 285-0898-00 |  |  | CAP.,FXD,PLSTC:0.47UF,10\%,100V | 56289 | LP66A1B474K |
| C107 | 290-0691-00 |  |  | CAP.,FXD,ELCTLT:500UF,6V | 13993 | 1-012-2158 |
| C108 | 290-0692-00 |  |  | CAP.,FXD,ELCTLT:100UF,50V | 90201 | MTV101N050E1AP |
| C109 | 285-0566-00 |  |  | CAP.,FXD,PLSTC:0.022UF,10\%,200V | 56289 | $192 P 22392$ |
| C110 | 283-0006-00 |  |  | CAP.,FXD,CER DI: $0.02 \mathrm{UF},+80-20 \%, 500 \mathrm{~V}$ | 59660 | 0841545Z5V00203Z |
| C111 | 283-0006-00 |  |  | CAP.,FXD,CER DI: $0.02 \mathrm{UF},+80-20 \%, 500 \mathrm{~V}$ | 59660 | 0841545Z5V00203Z |
| C112 | 290-0693-00 |  |  | CAP.,FXD,ELCTLT:50UF,50V | 90201 | MTV500N050C1FP |
| C113 | 285-1052-00 |  |  | CAP.,FXD,PLSTC:10UF,1\%,100V | 14752 | 230B1B106F |
| C114 | 290-0694-00 |  |  | CAP.,FXD,ELCTLT:200UF,25V | 90201 | MTV201N025E1AP |
| C115 | 290-0695-00 |  |  | CAP.,FXD,ELCTLT:50UF,25V | 90201 | MTV500N050C0SP |
| C119 | 290-0696-00 |  |  | CAP.,FXD,ELCTLT:25UF,50V | 90201 | MTV250N050C0PP |
| C120 | 281-0751-00 |  |  | CAP.,FXD,CER DI:0.01UF,1000V | 17954 | 1-012-0112 |
| C120 | ------- |  |  | (C120, USED ONLY AS REQUIRED) |  |  |
| CR2 | 152-0409-00 |  |  | SEMICOND DEVICE:SILICON, 12,000V,5MA | 83003 | VG12X-1 |
| CR101 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR102 | 152-0141-02 |  |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| CR103 | 152-0613-00 |  |  | SEMICOND DEVICE:RECT,SI,320V,7A | 000FA | 1-021-0360 |
| CR104 | 152-0040-00 |  |  | SEMICOND DEVICE:SILICON,600V,1A | 15238 | LG109 |
| CR105 | 152-0040-00 |  |  | SEMICOND DEVICE:SILICON,600V,1A | 15238 | LG109 |
| CR106 | 152-0040-00 |  |  | SEMICOND DEVICE:SILICON,600V,1A | 15238 | LG109 |
| CR107 | 152-0040-00 |  |  | SEMICOND DEVICE:SILICON,600V,1A | 15238 | LG109 |
| CR108 | ---------- |  |  | (USED ONLY AS REQUIRED) |  |  |
| F101 | 159-0127-00 |  |  | FUSE,CARTRIDGE:2A,125V | 75915 | 256003 |
| L1 | 108-0770-00 |  |  | CHOKE,RF: | 17954 | 6-003-0321 |
| L2 | 108-0771-00 |  |  | COIL,TUBE DEFL: | 17954 | 6-004-0314 |
| L101 | 114-0335-00 |  |  | COIL,RF:VARIABLE, $40-230 \mathrm{MH}$ | 17954 | -1-016-0303 |
| Q101 | 151-0347-00 |  |  | TRANSISTOR:SILICON,NPN | 56289 | 2N5551 |
| Q102 | 151-0508-00 |  |  | TRANSISTOR:UJT,SI,2N6027,TO-98 | 03508 | X13T520 |
| Q103 | 151-0254-00 |  |  | TRANSISTOR:SILICON,NPN | 03508 | X38L3118 |
| Q104 | 151-0349-00 |  |  | TRANSISTOR:SILICON,NPN,SEL FROM MJE280 | 04713 | SJE924 |
| Q105 | 151-0439-00 |  |  | TRANSISTOR:SILICON,NPN | 80009 | 151-0439-00 |
| Q106 | 151-0483-00 |  |  | TRANSISTOR:GERMANIUM,PNP | 17954 | B1182 |
| Q107 | -------- |  |  | (USED ONLY AS REQUIRED) |  |  |
| R101 | 301-0272-00 |  |  | RES.,FXD,CMPSN:2.7K OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB2725 |
| R103 | 301-0823-00 |  |  | RES.,FXD,CMPSN:82K OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB8235 |
| R104 | 301-0104-00 |  |  | RES.,FXD,CMPSN: 100 K OHM, $5 \%, 0.5 \mathrm{~W}$ | 01121 | EB1045 |
| R106 | 301-0104-00 |  |  | RES.,FXD,CMPSN: 100 K OHM, $5 \%, 0.5 \mathrm{~W}$ | 01121 | EB1045 |
| R107 | 311-1597-00 |  |  | RES.,VAR,NONWIR:TRMR,2.5M OHM, $20 \%, 0.25 \mathrm{~W}$ | 58756 | YR8878 |
| R108 | 301-0150-00 |  |  | RES.,FXD,CMPSN:15 OHM, 5\%,0.50W | 01121 | EB1505 |
| R109 | 301-0470-00 |  |  | RES.,FXD,CMPSN:47 OHM,5\%,0.50W | 01121 | EB4705 |


| Ckt No. | Tektronix Part No. | Serial/Model No. |  | Name \& Description | Mfr Code | Mfr Part Number |
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|  |  | Eff | Dscont |  |  |  |
| A12 ASSEMBLY TV MONITOR (CONT) |  |  |  |  |  |  |
| R110 | 301-0821-00 |  |  | RES.,FXD,CMPSN: 820 OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB8215 |
| R111 | 301-0470-00 |  |  | RES.,FXD,CMPSN: 47 OHM,5\%,0.50W | 01121 | EB4705 |
| R112 | 301-0221-00 |  |  | RES.,FXD,CMPSN: 220 OHM,5\%,0.50W | 01121 | EB2215 |
| R113 | 301-0471-00 |  |  | RES.,FXD,CMPSN:470 OHM,5\%,0.50W | 01121 | EB4715 |
| R114 | 301-0151-00 |  |  | RES.,FXD,CMPSN: 150 OHM,5\%,0.50W | 01121 | EB1515 |
| R115 | 301-0823-00 |  |  | RES.,FXD,CMPSN:82K OHM,5\%,0.50W | 01121 | EB8235 |
| R116 | 311-1136-00 |  |  | RES.,VAR,NONWIR: 100 K OHM, $30 \%, 0.25 \mathrm{~W}$ | 71450 | 201-YA5536 |
| R117 | 301-0472-00 |  |  | RES.,FXD,CMPSN:4.7K OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB4725 |
| R118 | 301-0822-00 |  |  | RES.,FXD,CMPSN:8.2K OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB8225 |
| R119 | 301-0104-00 |  |  | RES.,FXD,CMPSN:100K OHM, $5 \%, 0.5 \mathrm{~W}$ | 01121 | EB1045 |
| R120 | 301-0561-00 |  |  | RES.,FXD,CMPSN:560 OHM,5\%,0.50W | 01121 | EB5615 |
| R121 | 311-1133-00 |  |  | RES.,VAR,NONWIR:10K OHM,30\%,0.25W | 71450 | 201-YA5534 |
| R122 | 301-0472-00 |  |  | RES.,FXD,CMPSN:4.7K OHM,5\%,0.50W | 01121 | EB4725 |
| R123 | 301-0151-00 | B010100 | B052916 | RES.,FXD,CMPSN: 150 OHM,5\%,0.50W | 01121 | EB1515 |
| R123 | 301-0560-00 | B052917 |  | RES.,FXD,CMPSN: 56 OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB5605 |
| R124 | 311-1328-00 | B010100 | B052916 | RES.,VAR,NONWIR: 100 OHM, $30 \%, 0.25 \mathrm{~W}$ | 71450 | 201-YA5553 |
| R124 | 311-1308-00 | B052917 |  | RES.,VAR,NONWIR: 250 OHM, 30\%,0.25W | 71450 | 201-YA5550 |
| R125 | 308-0441-00 | B010100 | B052916 | RES.,FXD,WW:3 OHM,5\%,3W | 91637 | CW2B-3R00J |
| R125 | 308-0503-00 | B052917 |  | RES.,FXD,WW:6.8 OHM, $5 \%, 2.50 \mathrm{~W}$ | 91637 | CW2B-D6R800J |
| R126 | 301-0391-00 | B010100 | B052916 | RES.,FXD,CMPSN:390 OHM,5\%,0.50W | 01121 | EB3915 |
| R126 | 301-0681-00 | B052917 |  | RES.,FXD,CMPSN:680 OHM,5\%,0.50W | 01121 | EB6815 |
| R127 | 301-0471-00 |  |  | RES.,FXD,CMPSN:470 OHM, $5 \%, 0.50 \mathrm{~W}$ | 01121 | EB4715 |
| R127A | 315-0152-00 | B020545 |  | RES.,FXD,CMPSN:1.5K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1525 |
| R128 | 301-0272-00 |  |  | RES.,FXD,CMPSN:2.7K OHM,5\%,0.50W | 01121 | EB2725 |
| R129 | 307-0058-00 |  |  | RES.,FXD,CMPSN:5.6 OHM,5\%,0.5W | 01121 | EB56G5 |
| R130 | 308-0459-00 |  |  | RES.,FXD,WW:1.1 OHM,5\%,3W | 91637 | CW2B-1R100J TR |
| R131 | 301-0332-00 |  |  | RES.,FXD,CMPSN:3.3K OHM,5\%,0.50W | 01121 | EB3325 |
| R132 | 308-0239-00 |  |  | RES.,FXD,WW:84 OHM,1\%,3W | 91637 | RS2B-B84R00F |
| R133 | 315-0472-00 |  |  | RES.,FXD,CMPSN:4.7K OHM, 5\%,0.25W | 01121 | CB4725 |
| R133 | --------- |  |  | (R133, USED ONLY AS REQUIRED) |  |  |
| R135 | 315-0223-00 |  |  | RES.,FXD,CMPSN:22K OHM,5\%,0.25W | 01121 | CB2235 |
| R135 | ----- |  |  | (R135, USED ONLY AS REQUIRED) |  |  |
| R136 | 315-0223-00 |  |  | RES.,FXD,CMPSN:22K OHM,5\%,0.25W | 01121 | CB2235 |
| R136 | ---------- |  |  | (R136, USED ONLY AS REQUIRED) |  |  |
| R137 | 315-0333-00 |  |  | RES.,FXD,CMPSN:33K OHM,5\%,0.25W | 01121 | CB3335 |
| R137 | -------- |  |  | (R137, USED ONLY AS REQUIRED) |  |  |
| T2 | 120-0894-00 |  |  | XFMR,POWER:HV | 17954 | 6-003-0320 |
| T101 | 120-0895-00 |  |  | TRANSFORMER,PLS: | 17954 | 1-017-5338 |
| - |  |  |  |  |  |  |
| V1 | 154-0710-00 |  |  | ELECTRON TUBE:CRT,P4 | 13993 | 1-014-0737 |
| VR101 | 152-0149-00 |  |  | SEMICOND DEVICE:ZENER,0.4W,10V,5\% | 04713 | SZG35009K3 |


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| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A13 ASSEMBLY POWER |  |  |
| A13 | 670-2196-01 |  | CKT BOARD ASSY:POWER SUPPLY | 80009 | 670-2196-01 |
| A13 | 670-2196-02 |  | CKT BOARD ASSY:POWER SUPPLY | 80009 | 670-2196-02 |
| A13 | 670-2196-03 | B050000 | CKT BOARD ASSY: | 80009 | 670-2196-03 |
| C22 | 283-0003-00 |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | 2DDH66J103Z |
| C29 | 290-0135-00 |  | CAP.,FXD,ELCTLT:15UF,20\%,20V | 56289 | 150D156X0020B2 |
| C30 | 283-0134-00 |  | CAP.,FXD,CER DI:0.47UF, $+80-20 \%, 50 \mathrm{~V}$ | 72982 | 8131N087Z5U0474Z |
| C43 | 290-0135-00 |  | CAP.,FXD,ELCTLT:15UF,20\%,20V | 56289 | 150D156X0020B2 |
| C45 | 290-0135-00 |  | CAP.,FXD,ELCTLT:15UF,20\%,20V | 56289 | 150D156X0020B2 |
| C52 | 283-0028-00 |  | CAP.,FXD,CER DI:0.0022UF,20\%,50V | 59660 | 0805585Y5SO222M |
| C55 | 283-0028-00 |  | CAP.,FXD,CER DI:0.0022UF,20\%,50V | 59660 | 0805585Y5SO222M |
| C101 | 290-0135-00 |  | CAP.,FXD,ELCTLT:15UF,20\%,20V | 56289 | 150D156X0020B2 |
| C107 | 290-0527-00 |  | CAP.,FXD,ELCTLT:15UF,20\%,20V | 90201 | TDC156M020FL |
| C110 | 283-0000-00 |  | CAP.,FXD,CER DI:0.001UF,+100-0\%,500V | 59660 | 831610Y5U0102P |
| C123 | 281-0525-00 |  | CAP.,FXD,CER DI:470PF,+/-94PF,500V | 04222 | 7001-1364 |
| C204 | 283-0142-00 |  | CAP.,FXD,CER DI:0.0027UF,5\%,200V | 59660 | 875571YEE0272J |
| C209 | 283-0177-00 |  | CAP,,FXD,CER DI:1UF,+80-20\%,25V | 56289 | 2C20Z5U105Z025B |
| C305 | 281-0546-00 |  | CAP.,FXD,CER DI:330PF,10\%,500V | 04222 | 7001-1380 |
| C306 | 283-0177-00 |  | CAP.,FXD,CER DI:1UF,+80-20\%,25V | 56289 | 2C20Z5U105Z025B |
| C307 | 283-0177-00 |  | CAP.,FXD,CER DI:1UF,+80-20\%,25V | 56289 | 2C20Z5U105Z025B |
| C322 | 290-0506-00 |  | CAP.,FXD,ELCTLT:9600UF,+100-10\%,25V | 56289 | 68D10471 |
| C351 | 290-0506-00 |  | CAP.,FXD,ELCTLT:9600UF,+100-10\%,25V | 56289 | 68D10471 |
| - |  |  |  |  |  |
| CR55 | 152-0107-00 |  | SEMICOND DEVICE:SILICON,400V,400MA | 12969 | G727 |
| CR131 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR134 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR141 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR145 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR151 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR153 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR155 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR157 | 152-0198-00 |  | SEMICOND DEVICE:SILICON,200V,3A | 03508 | 1N5624 |
| CR202 | 152-0141-02 |  | SEMICOND DEVICE:SILICON,30V,150MA | 01295 | 1N4152R |
| Q29 | 151-0341-00 |  | TRANSISTOR:SILICON,NPN | 07263 | S040065 |
| Q38 | 151-0341-00 |  | TRANSISTOR:SILICON,NPN | 07263 | S040065 |
| Q53 | 151-0134-00 |  | TRANSISTOR:SILICON,PNP | 80009 | 151-0134-00 |
| Q55 | 151-0341-00 |  | TRANSISTOR:SILICON,NPN | 07263 | S040065 |
| Q109 | 151-0134-00 |  | TRANSISTOR:SILICON,PNP | 80009 | 151-0134-00 |
| Q110 | 151-0342-00 |  | TRANSISTOR:SILICON,PNP | 07263 | S035928 |
| Q241 | 151-0136-00 |  | TRANSISTOR:SILICON,NPN | 02735 | 35495 |
| Q305 | 151-0342-00 |  | TRANSISTOR:SILICON,PNP | 07263 | S035928 |
| Q359 | 151-0302-00 |  | TRANSISTOR:SILICON,NPN | 07263 | S038487 |
|  |  |  |  |  |  |
| R10 | 315-0511-00 |  | RES.,FXD,CMPSN:510 OHM,5\%,0.25W | 01121 | CB5115 |
| R20 | 315-0101-00 |  | RES.,FXD,CMPSN:100 OHM,5\%,0. 25W | 01121 | CB1015 |
| R21 | 315-0510-00 |  | RES.,FXD,CMPSN:51 OHM,5\%,0.25W | 01121 | CB5105 |
| R23 | 315-0153-00 |  | RES.,FXD,CMPSN:15K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1535 |
| R23 | --------- |  | (-01 BOARDS ONLY) |  |  |
| R23 | 315-0512-00 |  | RES.,FXD,CMPSN:5.1K OHM, 5\%,0.25W | 01121 | CB5125 |
| R23 | ----- |  | (-02 AND UP BOARDS ONLY) |  |  |
| R24 | 315-0241-00 |  | RES.,FXD,CMPSN:240 OHM,5\%,0.25W | 01121 | CB2415 |
| R26 | 315-0471-00 |  | RES.,FXD,CMPSN:470 OHM,5\%,0.25W | 01121 | CB4715 |


| Ckt No. | Tektronix Part No. | Serial/Model No. <br> Eff Dscont | Name \& Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | A13 ASSEMBLY POWER (CONT) |  |  |
| R27 | 315-0101-00 |  | RES.,FXD,CMPSN: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1015 |
| R28 | 321-0816-03 |  | RES.,FXD,FILM:5K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816D50000C |
| R29 | 321-0289-03 |  | RES.,FXD,FILM:10K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816D10001C |
| R30 | 321-0135-00 |  | RES.,FXD,FILM:249 OHM, 1\%,0.125W | 91637 | MFF1816G249R0F |
| R31 | 315-0102-00 |  | RES.,FXD,CMPSN: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R32 | 321-0269-00 |  | RES.,FXD,FILM:6.19K OHM, $1 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G61900F |
| R33 | 315-0472-00 |  | RES.,FXD,CMPSN:4.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB4725 |
| R34 | 315-0241-00 |  | RES.,FXD,CMPSN:240 OHM,5\%,0.25W | 01121 | CB2415 |
| R40 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R41 | 315-0512-00 |  | RES.,FXD,CMPSN:5.1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5125 |
| R42 | 321-0226-00 |  | RES.,FXD,FILM:2.21K OHM, $1 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G22100F |
| R43 | 321-0218-00 |  | RES.,FXD,FILM:1.82K OHM, $1 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G18200F |
| R44 | 315-0511-00 |  | RES.,FXD,CMPSN:510 OHM,5\%,0.25W | 01121 | CB5115 |
| R45 | 321-1296-07 |  | RES.,FXD,FILM:12K OHM,0.1\%,0.125W | 91637 | MFF1816C12001B |
| R45 | ---------- |  | (-01 BOARDS ONLY) |  |  |
| R45 | 321-0634-00 |  | RES.,FXD,FILM:84.65K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | CMF55-116D84651C |
| R45 | --------- |  | (-02 AND UP BOARDS ONLY) |  |  |
| R46 | 321-0306-01 |  | RES.,FXD,FILM:15K OHM, $0.5 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G15001D |
| R46 | --------- |  | (-01 BOARDS ONLY) |  |  |
| R46 | 321-0680-00 |  | RES.,FXD,FILM:35.3K OHM,0.5\%,0.125W | 91637 | MFF1816D35301D |
| R46 | --------- |  | (-02 AND UP BOARDS ONLY) |  |  |
| R47 | 311-1276-00 |  | RES.,VAR,NONWIR: 50 OHM, $+1-10 \%, O .5 \mathrm{~W}$ | 32997 | 3329W.L58-500 |
| R47 | --- |  | (-01 BOARDS ONL.Y) |  |  |
| R47 | 311-1277-00 |  | RES.,VAR,NONWIR:100 OHM,10\%,0.5W | 32997 | 3329W-L58-101 |
| R47 | ---------- |  | (-02 AND UP BOARDS ONLY) |  |  |
| R50 | 315-0332-00 |  | RES.,FXD,CMPSN:3.3K OHM,5\%,0.25W | 01121 | CB3325 |
| R51 | 321-0306-01 |  | RES.,FXD,FILM:15K OHM, $0.5 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G15001D |
| R51 | ------- |  | (-01 BOARDS ONLY) |  |  |
| R51 | 321-0634-00 |  | RES.,FXD,FILM:84.65K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | CMF55-116D84651C |
| R51 | ------ |  | (-02 AND UP BOARDS ONLY) |  |  |
| R52 | 321-0816-03 |  | RES.,FXD,FILM:5K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816D50000C |
| R52 | --------- |  | (-01 BOARDS ONLY) |  |  |
| R52 | 321-0634-00 |  | RES.,FXD,FILM:84.65K OHM, $0.25 \%, 0.125 \mathrm{~W}$ | 91637 | CMF55-116D84651C |
| R52 | --------- |  | (-02 AND UP BOARDS ONLY) |  |  |
| R53 | 315-0472-00 |  | RES.,FXD,CMPSN:4.7K OHM,5\%,0.25W | 01121 | CB4725 |
| R54 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R55 | 315-0751-00 |  | RES.,FXD,CMPSN:750 OHM,5\%,0.25W | 01121 | CB7515 |
| R56 | 308-0402-00 |  | RES.,FXD,WW:30 OHM,5\%,5W | 91637 | CW2A-K30R00J |
| R57 | 315-0512-00 |  | RES.,FXD,CMPSN:5.1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5125 |
| R58 | 315-0101-00 |  | RES.,FXD,CMPSN: 100 OHM,5\%,0.25W | 01121 | CB1015 |
| R59 | 315-0101-00 |  | RES.,FXD,CMPSN:100 OHM,5\%,0.25W | 01121 | CB1015 |
| R101 | 301-0750-00 |  | RES.,FXD,CMPSN:75 OHM,5\%,0.50W | 01121 | EB7505 |
| R106 | 315-0150-00 |  | RES.,FXD,CMPSN:15 OHM,5\%,0.25W | 01121 | CB1505 |
| R110 | 315-0472-00 |  | RES.,FXD,CMPSN:4.7K OHM,5\%,0.25W | 01121 | CB4725 |
| R111 | 315-0301-00 |  | RES.,FXD,CMPSN:300 OHM,5\%,0.25W | 01121 | CB3015 |
| R112 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM,5\%,0.25W | 01121 | CB1025 |
| R201 | 315-0102-00 |  | RES.,FXD,CMPSN:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1025 |
| R202 | 315-0100-00 |  | RES.,FXD,CMPSN: 10 OHM,5\%,0.25W | 01121 | CB1005 |
| R203 | 315-0103-00 |  | RES.,FXD,CMPSN:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB1035 |
| R204 | 315-0103-00 |  | RES.,FXD,CMPSN:10K OHM,5\%,0.25W | 01121 | CB1035 |
| R205 | 315-0103-00 |  | RES.,FXD,CMPSN:10K OHM,5\%,0.25W | 01121 | CB1035 |
| R206 | 315-0622-00 |  | RES.,FXD,CMPSN:6.2K OHM,5\%,0.25W | 01121 | CB6225 |


|  | Tektronix | Serial/Model No. |  |  | Mfr |
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| Ckt No. | Part No. | Eff | Dscont | Name \& Description | Code | Mfr Part Number |  |  |  |  |
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|  |  | A13 ASSEMBLY POWER (CONT) |  |  |
| :---: | :---: | :---: | :---: | :---: |
| R207 | 315-0101-00 | RES.,FXD,CMPSN: 100 OHM, 5\%,0. 25 W | 01121 | CB1015 |
| R208 | 308-0244-00 | RES.,FXD,WW:0.3 OHM, 10\%,2W | 91637 | RS2B162ER3000K |
| R209 | 315-0332-00 | RES.,FXD,CMPSN:3.3K OHM, 5\%,0.25W | 01121 | CB3325 |
| R254 | 315-0681-00 | RES.,FXD,CMPSN:680 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB6815 |
| R256 | 321-0181-00 | RES.,FXD,FILM: 750 OHM, $1 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G750R0F |
| R256 | --------1-1-0100 | (-01 BOARDS ONLY) |  |  |
| R256 | 321-0183-00 | RES.,FXD,FILM: 787 OHM, $1 \%, 0.125 \mathrm{~W}$ | 91637 | MFF1816G787R0F |
| R256 | -------- | (-02 AND UP BOARDS ONLY) |  |  |
| R257 | 321-0226-00 | RES.,FXD,FILM:2.21K OHM,1\%,0.125W | 91637 | MFF1816G22100F |
| R258 | 311-1139-00 | RES.,VAR,NONWIR:500 OHM, $20 \%, 0.50 \mathrm{~W}$ | 73138 | 72-43-0 |
| R304 | 315-0511-00 | RES.,FXD,CMPSN: 510 OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB5115 |
| R305 | 315-0470-00 | RES.,FXD,CMPSN:47 OHM,5\%,0.25W | 01121 | CB4705 |
| R306 | 315-0271-00 | RES.,FXD,CMPSN:270 OHM,5\%,0.25W | 01121 | CB2715 |
| R307 | 315-0392-00 | RES.,FXD,CMPSN:3.9K OHM, $5 \%, 0.25 \mathrm{~W}$ | 01121 | CB3925 |
| R307 | -- | (-01 BOARDS ONLY) |  |  |
| R307 | 315-0471-00 | RES.,FXD,CMPSN:470 OHM,5\%,0.25W | 01121 | CB4715 |
| R307 | - | (-02 AND UP BOARDS ONLY) |  |  |
| R341 | 315-0472-00 | RES.,FXD,CMPSN:4.7K OHM,5\%,0.25W | 01121 | CB4725 |
| R356 | 308-0755-00 | RES.,FXD, WW:0.75 OHM, $5 \%, 2 \mathrm{~W}$ | 75042 | BWH-R7500, |
| R358 | 303-0301-00 | RES.,FXD,CMPSN:300 OHM, 5\%,1w | 01121 | GB3015 |
| 452 | 156-0067-00 | MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER | 01295 | MICROA741CP |
| U55 | 156-0067-00 | MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER | 01295 | MICROA741CP |
| U123 | 156-0071-00 | MICROCIRCUIT,LI:VOLTAGE REGULATOR | 04713 | MC1723CL |
| U205 | 156-0067-00 | MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER | 01295 | MICROA741CP |
| VR306 | 152-0175-00 | SEMICOND DEVICE:ZENER,0.4W, $5.6 \mathrm{~V}, 5 \%$ | 04713 | SZG35008 |


| Ckt No. | Tektronix Part No. | Serial/Model No. |  | Name \& Description | Mfr |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | CHASSIS PARTS |  |  |
| C354 | 283-0358-00 | B050000 |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 1.4 \mathrm{KV}$ | 59660 | ORD BY DESCR |
| C356 | 283-0358-00 | B050000 |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 1.4 \mathrm{KV}$ | 59660 | ORD BY DESCR |
| C1006 | 290-0545-00 |  |  | CAP.,FXD,ELCTLT:86,000UF, $+75-10 \%, 15 \mathrm{~V}$ | 56289 | 36D863G015DC2A |
| C1014 | 283-0003-00 |  |  | CAP.,FXD,CER DI:0.01UF, $+80-20 \%, 150 \mathrm{~V}$ | 59821 | 2DDH66J103Z |
| C1144 | 283-0177-00 |  |  | CAP.,FXD,CER DI:1UF, $+80-20 \%, 25 \mathrm{~V}$ | 56289 | 2C20Z5U105Z025B |
| CR1006 | 152-0518-00 |  |  | SEMICOND DEVICE:RECT,SI,50V,27A | 83003 | K019 |
| CR1120 | 150-1001-00 | B010100 | B064715 | LT EMITTING DIO:RED,660NM,100MA MAX | 50522 | MV5024 |
| CR1120 | 150-1050-00 | B064716 |  | LT EMITTING DIO:RED | 50579 | RL-T1 |
| CR1122 | 150-1001-00 | B010100 | B064715 | LT EMITTING DIO:RED,660NM,100MA MAX | 50522 | MV5024 |
| CR1122 | 150-1050-00 | B064716 |  | LT EMITTING DIO:RED | 50579 | RL-T1 |
| CR1124 | 150-1001-00 | B010100 | B064715 | LT EMITTING DIO:RED,660NM,100MA MAX | 50522 | MV5024 |
| CR1124 | 150-1050-00 | B064716 |  | LT EMITTING DIO:RED | 50579 | RL-T1 |
| DS1125 | 150-0134-00 |  |  | LAMP,CARTRIDGE:6.3V,200MA. | 55292 | 72505-03 |
| . ${ }^{\text {c }}$ |  |  |  |  |  |  |
| F1001 | 159-0023-00 |  |  | FUSE,CARTRIDGE:3AG,2A,250V,5 SEC | 71400 | MDX2 |
| F1007 | 159-0038-00 |  |  | FUSE,CARTRIDGE:3AG,15A,32V,FAST-BLOW | 71400 | AGC15 |
| J193 | 131-0274-00 |  |  | CONNECTOR,RCPT,:BNC | 91836 | KC79-67 |
| Q1014 | 151-0515-01 |  |  | SCR:SILICON | 04713 | SCR1256K |
| Q1105 | 151-0337-00 |  |  | TRANSISTOR:SILICON,NPN | 02735 | 61443 |
| Q1110 | 151-0337-00 |  |  | TRANSISTOR:SILICON,NPN | 02735 | 61443 |
| Q1112 | 151-0433-00 | B010100 | B064784 | TRANSISTOR:SILICON,NPN | 80009 | 151-0433-00 |
| Q1112 | 151-0470-00 | B064785 |  | TRANSISTOR:SILICON,NPN | 80009 | 151-0470-00 |
| Q1118 | 151-0337-00 |  |  | TRANSISTOR:SILICON,NPN | 02735 | 61443 |
| R354 | 307-0413-00 | B050000 |  | RES,NTWK,FXD,FI:3.3M OHM,10\%,1W | 03888 | FL1-3304K-10\% |
| R1112 | 308-0570-00 |  |  | RES.,FXD,WW:0.05 OHM,5\%,5W | 80009 | 308-0570-00 |
| R1140 | 311-0095-00 |  |  | RES.,VAR,NONWIR:500 OHM,10\% | 11237 | 41022 |
| R1145 | 311-0467-00 |  |  | RES.,VAR,NONWIR:100K OHM, $20 \%, 0.50 \mathrm{~W}$ | 11237 | 300SF-41334 |
| S1001 | 260-1497-00 |  |  | SWITCH,PUSH:DPDT,10A,250VAC | 01963 | E79-30A |
| S1002 | 260-1490-00 | $B 010100$ | B052959 | SWITCH,TOGGLE: 1 SECT,3 POSN,30 DEG | 10389 | 171-298-129 |
| S1002 | 260-1902-00 | B052960 |  | SWITCH,ROCKER:DPST,16A,250VAC | 04009 | 260011E |
| S1120 | 260-1334-00 |  |  | SWITCH,ROCKER:SPDT,0.5A,125VAC | 22753 | RSW-412 |
| S1121 | 260-1334-00 |  |  | SWITCH,ROCKER:SPDT,0.5A,125VAC | 22753 | RSW-412 |
| S1122 | 260-1334-00 |  |  | SWITCH,ROCKER:SPDT,0.5A,125VAC | 22753 | RSW-412 |
| S1123 | 260-1334-00 |  |  | SWITCH,ROCKER:SPDT,0.5A,125VAC | 22753 | RSW-412 |
| . ${ }^{\text {c }}$ |  |  |  |  |  |  |
| SP1144 | 119-0305-00 |  |  | LOUDSPEAKER,PM:PERMANENT MAGNET,45 OHM,2W | 07109 | 35A45C |
| T1000 | 120-0884-00 |  |  | XFMR,PWR,STPDN: <br> EM161700.DATA 4023 | 80009 | $120-0884-00$ |

## THEORY OF OPERATION

## INTRODUCTION

This section of the manual is designed to aid the technician in understanding the operation of the Terminal. Not only is circuit operation discussed, but wire lists and diagrams are provided to aid in isolating malfunctions.

It is assumed that the person reading this section has a solid understanding of TTL and analog theory. For this reason, circuitry is not discussed on a component basis, except in those cases where, for clarity, specific components are mentioned.

This section is not intended to cover every detail of Terminal operation; however, it does provide sufficient information to enable the technician to isolate the majority of malfunctions to a block of circuitry on a specific card. Those with a good understanding of TTL and analog circuitry should then be able to further isolate the problem to a specific component.

Many Terminal functions encompass circuitry located on two or more cards. The use of a "minibus" makes this type of circuit design practical. For this reason, it is recommended that the material in this section be read in the order given. Information contained herein is intended to provide the first-time reader an over-view of Terminal operation.

Each circuit board or circuit card (circuit cards are those logic cards which are inserted into the minibus) is discussed in general terms. Here you will find the specific circuits and functions performed by each card. This information is followed by schematic descriptions of the circuits and functions previously mentioned. You can pull out and unfold the schematic as you read the schematic description.

The back portion of this section contains signal and wiring information. Signal information provides a description of each signal available to all cards that plug into the minibus. Here you will also find from which card (cards) each signal originates and on which card (cards) the signal is used. Wiring information provides a wiring list and diagram of wiring between major Terminal components.

Semiconductor information is provided in Fig. 6-16. This figure is located just preceding the schematics.

## GENERAL DESCRIPTIONS

Figure 6-14, located at the end of the circuit descriptions, is an over-all block diagram of the Terminal system. Pull-out this illustration and refer to it when reading the following general descriptions.

## KEYBOARD

Provides a data source for the computer and the Terminal. The operation of Keyboard circuitry is discussed first because this is the starting point of the majority of terminal data inputs to the computer. Refer to the Keyboard circuit description for more information.

## TIMING CARD

A good understanding of Terminal timing is a prerequisite to understanding Terminal logic operation. The Timing Card provides master timing signals relevant to the operation of the Terminal. A 22.008 MHz crystal oscillator provides television timing compatibility. This frequency is divided to provide timing signals for making video, and for synchronizing the display and input/output functions to memory.

Minibus data is received and decoded to generate video for the Terminal display, the Hard Copy Unit, and for auxiliary monitors. Field Attribute Codes that contain "video appearance" information are decoded to display video as normal, dim, inverted, blinking, or blanked. Circuitry such as the character generator, cursor generator, cursor blink, horizontal and vertical drive signal generators, 50 Hz and 60 Hz timing, and others are contained on this card. Specific circuits are:

1. Master Oscillator.
2. Display and Input/Output Timing.
3. DMA Control.
4. Video Path.
5. Two Character Delay.
6. Cursor Generator.
7. Blanking Control.
8. FAC Storage.
9. Rulings Spread.
10. ROM ROW Decoders.
11. Unused Sweep Blanking.
12. Scan Next Line.
13. HCU Video.
14. Monitor Video.
The Circuit Description provides more detailed information
on each of the afore-mentioned circuits. on each of the afore-mentioned circuits.

## KEYBOARD INTERFACE CARD

This card provides connection between the Keyboard and the minibus. Data from the Keyboard is detected and synchronized with Terminal memory timing before being entered to the memory or Computer Interface via the minibus. Appropriate incremental commands are generated to move the cursor when keying in data or when using the cursor movement keys. Erase Input, Clear Page, and bell ringing functions are controlled by this card.

The major circuits on this card are given below; they are discussed in the Circuit Description, in the order given:

1. Inputting Keyboard Data.
2. Control Character Decoders.
3. Keygate Generator With Repeat.
4. TSTROBE and CSTROBE Control.
5. Move Cursor Timing.
6. Move Cursor Gates.
7. Carriage Return and Line Feed Circuits.
8. Clear Page and Erase Input Circuits.
a. Initiate.
b. Clear Page Circuit.
c. Erase Input Circuit.
d. Rulings Erase Control.
9. Page Full.
10. Wrap-around.
11. Miscellaneous Circuits and Functions.
a. Bell Circuit.
b. Rubout Suppress.
c. NUL and ETX.

## CONTROL CARD

The majority of circuitry contained on this card is used to control transmission of memory contents. Coded hardcopy commands; erase-to-end functions; and detection of transmittable, numeric, and protected fields are performed by this card. In addition, ESC character decoding and prompt character decoding are performed here. The following circuits and functions are discussed in the circuit description of this card. Refer to the Circuit Description for more information.

1. Control Character Decoding for $\mathrm{SI}, \mathrm{BEL}, \mathrm{CR}, \mathrm{ENQ}$, VT, ETX, SO, ACK, and NUL.
2. ESC Decoder.
3. Prompt Character Decoder.
4. Make Copy Signal.
5. Conditional Transmit/Field Inhibit.
6. Erase to End Control.
7. EOL LF GEN Strap.
8. End Character Generation.
9. Protected Field and Non-Alpha Field Detection.
10. Miscellaneous Circuits and Operations.
a. Send 8 Functions.
b. Alternate Character Set Not Transmittable.
c. $\overline{\mathrm{CPUNT}}$.
d. Cursor Blanking.

## CURSOR CARD

The Cursor Card contains two sets of $X$ and $Y$ registers. One set remembers and controls the cursor location; the other set is used for display functions and is the source of the address for obtaining a character from memory for display. This card provides considerable steering of data between the minibus and the Cursor Register, as well as between the Cursor and Display Registers. Up, Down, Right, Left, and Clear Page functions are performed by this card. The circuits and functions discussed in the Cursor Card Description are given below. See the Circuit Description for information on each circuit.

1. Register Description.
2. Cursor Register Operation.

## 3. Display Register Operation.

a. Register Counting.
b. RAM Addressing.
c. Presetting the Display Registers.
d. RAM Address Multiplexers.
4. Edit Effects on the Registers.
a. Insert Line
b. Delete Line.
c. Insert Character.
d. Delete Character
5. Cursor Addressing and Reading.
a. Cursor Positioning.
b. Cursor Reading.
6. Miscellaneous Circuits.
7. Summary of Register Operations.
a. General.
b. Register Indicators.
c. Examples of Register Counting.
d. Purpose of Cursor Register.
e. Direct Memory Access (DMA) Operation.

## RAM CARD

The RAM Card contains MOS RAMs, which store data for screen display. Timing is provided by the Timing Card; data source is the minibus. Address inputs are BCD 0-79 for $X$ and BCD 0-23 for Y . The RAM Card contains arithmetic logic, which converts each distinct $\mathrm{X}-\mathrm{Y}$ code into the proper RAM address equivalent. Miscellaneous circuits not connected with the operation of the RAM Card are the Initialization Circuit and the 4.9 MHz Crystal Oscillator (used for input/output timing). Circuits and operations discussed in the RAM Card circuit description are given below. See the Circuit Descripiton for more information.

1. Operation of Major Circuits.
a. Selecting the RAM Set.
b. Read/Write Enabling.
c. RAM Refreshing.
d. Read to Minibus Enable.
e. Address Decoding.
f. Sense Amplifiers.
2. Miscellaneous Circuits.
a. Initializing Circuit.
b. 4.9 MHz Crystal Oscillator.

## EDIT CARD

This Card contains control logic for the Edit, Roll-up Read Cursor, Position Cursor, Bit 8 and Bit 9 Set, and Cursor Tab Functions. As with the other circuit cards, no attempt is made to give a component-by-component description of circuit operations. The Edit Card circuits discussed are generalized, with only the functions of specific components that need explaining being discussed. Refer to the circuit description of this card for more information.

## LOW VOLTAGE POWER SUPPLY

The discussion of this schematic explains the generation and regulation of the $+15 \mathrm{Vdc},+5 \mathrm{Vdc},-12 \mathrm{Vdc}$, and -5 Vdc power supplies. Refer to the Power Supply circuit description.

## DISPLAY CIRCUITS

This description is limited to those circuits necessary to operate the display monitor and include the following:

1. Video Amplifier.
2. Vertical Deflection.
3. Horizontal Deflection.
4. Power Supply.
5. Brightness.
6. Focus.
7. Troubleshooting Guide.

## DETAILED DESCRIPTION

## KEYBOARD DESCRIPTION

## GENERAL

Refer to the Keyboard schematic. The keyboard is a source of data for the computer. It attaches to the Terminal which provides interfacing electronics as well as a display screen to display the man-computer interchange. Whether keyboard data is sent "directly" to the computer or is "buffered" (stored in Terminal memory) prior to sending, depends on the type of input/output operation.

CODED CHARACTER GENERATION. The keyboard contains an encoder array that consists primarily of $\mathrm{Z} 2, \mathrm{Z} 1$, and assoicated circuitry. $\mathrm{Z2}$ is a MOS ROM-Type integrated circuit that provides encoding to and decoding from a 10X by 10 Y keyboard matrix. $\mathrm{Z1}$ provides proper timing inputs to $\mathbf{Z 2}$. Other inputs and outputs of $\mathbf{Z 2}$ will be covered in the following. The combined purpose of this circuitry is to generate a coded character output on 7 data line labeled KBIT $1-$ KBIT 7 (KBIT 8 is pulled high to +5 V on the keyboard).

Z2 provides continuous scanning signals ( $X_{1}-X_{10}$ ) to the column inputs of the matrix. Row signals $\left(Y_{1}-Y_{10}\right)$ from the matrix are sampled one at a time by Z2. A full scan of the matrix comprises 90 clock times, with each clock time defining a specific $\mathrm{Xn}-\mathrm{Yn}$ intersection of the matrix.

When a character key is depressed, a switch closure occurs at that $\mathrm{Xn}-\mathrm{Yn}$ intersection. This switch closure is
decoded by Z2, which enables output data on KBIT 1 KBIT 7 that is representative of the bit combination of the character pressed. The STB output enables KSTROBE to accompany the character output.

Generating a character code also triggers repeat character timing within Z2. If the same key is held down for more than 0.3 seconds (the 0.3 seconds time delay is provided on pin 16 of $Z 2$ ), STB is pulsed at a 10 Hz repetition rate, enabling KSTROBE ten times per second. This enables the Terminal to process the character bits at that rate.

The above-stated condition is maintained as long as the keyboard key is held down. Releasing the key ends the KBIT 1 - KBIT 7 and KSTROBE outputs.

Upper-case characters are generated by simultaneously pressing the SHIFT key and the desired character. Depressing SHIFT causes a switch closure at the $X_{3}-\mathrm{Y}_{10}$ junction. Because the SHIFT key causes a ground closure, transistors Q1 and Q2 provide the "switch" for this junction.

The $X_{4}-Y_{10}$ junction of the keyboard matrix is reserved for the CTRL (control) key. Operation in the control mode occurs as long as the CTRL key is depressed, causing KBIT $5-$ KBIT 7 to reflect control character information.

FUNCTION PAD OPERATION. The 12 key cluster at the right of the keyboard provides input codes for Z2. Like the normal character keys, $\mathbf{Z 2}$ decodes their input and sets the data output lines to reflect their specific input. However, pressing a Function Pad Key also sets the B9 output (pin 17). B9 prevents STB from enabling KSTROBE. This prevents the Terminal from responding to KBIT 1 - KBIT 7. However, B9 also provides an enabling voltage (via Z7E) to Z8A and Z8B. This allows B1 - B4 to control the output from decoders $\mathrm{Z4}$ and $\mathrm{Z5}$. The SHIFT signals, SH and $\overline{\mathrm{SH}}$, provide steering for the shiftable outputs from Z4 and Z5.

Note that the low from Z6C also disables the repeat input frequency to Z2. Repeat capability for the special functions is provided by the Terminal logic.

Pressing the NUM LOCK Key enables the Special Function Keys to perform as a numeric pad. Pressing the function pad keys causes the keyboard to output numeric
characters on KBIT 1 - KBIT 7. NUM LOCK disables the Function Decoders Z4 and Z5. It also permits STB to enable KSTROBE from Z6B, and to enable repetition of STB from Z2, should any function key be held down more than 0.3 seconds. NUM LOCK must be depressed again to re-establish the normal function pad controls. Normally, the RESET key activates KRESET. With NUM LOCK pressed, pressing RESET enables the $\mathrm{X}_{10}-\mathrm{Y}_{3}$ junction (on the keyboard matrix) to be shorted by Q 3 and Q 4 . Thus, with NUM LOCK pressed, RESET is able to activate the numeral " 7 ".

## MISCELLANEOUS FUNCTIONS

SHIFT, PAGE, TTY, AND RESET KEYS. SHIFT not only closes the $X_{3}-Y_{10}$ junction on the matrix, but also provides steering for the Page, Insert, and Delete functions. PAGE is combined with outputs from the SHIFT key to determine the function it initiates. Pressing TTY permits only upper-case bit configurations to be structured. Pressing RESET either sets KRESET active or, if NUM LOCK is pressed, causes the bit configuration for the numeral " 7 " to be structured. Pressing BREAK causes the KBREAK signal to go active. This signal is used by the computer interface for computer signaling purposes.

## TIMING CARD

## TIMING

Refer to the Timing Card schematic. Component locations for the Timing Card are provided on the apron of the schematic. Terminal timing can be divided into specific time intervals. Let's look at the display to understand some basic timing principles.

First, we must know what is meant when we refer to a "field". A FIELD is that period of time required for the display beam to "sweep" (deflect from left to right) 262 times, starting at the top and ending at the bottom of the display. See Fig. 6-1. The standard Terminal generates 60 fields each second (a factory strap option enables the Terminal to be compatible with either 60 or 50 Hz line frequency). Thus, the standard Terminal generates a field every 16.67 ms . The VERTICAL DRIVE signal is the negative going pulse that triggers the vertical drive circuitry (on the monitor) 60 times per second. See Fig. 6-2.

As previously mentioned, a field consists of 262 horizontal sweeps of the crt writing beam. However, not all sweeps


Fig. 6-1. Field definition. A video field contains 262 horizontal sweeps. The Standard Terminal is factory wired to generate 60 fields each second.


Fig. 6-2. Field Timing.
are used for displaying data. Twenty-two sweeps are blanked. Vertical retrace occurs during this time.

The HORIZONTAL DRIVE signal triggers the horizontal sweep every $63.6 \mu \mathrm{~s}(16.67 \mathrm{~ms} \div 262=63.6 \mu \mathrm{~s})$. With 22 sweeps blanked, 240 are left for displaying information. This divides into 10 sweeps for each of the 24 lines of characters. Figure $6-2$ shows the duration of HORIZONTAL DRIVE. The negative going pulse is the time alloted for sweep retrace, and is reserved for input/output functions (see Input/Output).

The on time of HORIZONTAL DRIVE ( $46.6 \mu \mathrm{~s}$ ) also corresponds to DISPLAY time. During DISPLAY time data is read from the memory into the Character Generator to
produce video. Video is produced a horizontal sweep at a time with each horizontal sweep divided into 100 character times. A character time corresponds to the repetition rate of the STEP signal $-636 \mathrm{~ns}(63.6 \mu$ s per sweep $\div 100=$ 636 ns per character). Eighty STEP times are reserved for character generation and 20 for input/output and sweep retrace (the sweep is blanked during horizontal retrace for approximately 10 character times).

Each character time can be further divided into dot times. Dot times are the time during horizontal sweep movement when the display beam would be turned on or off in the process of character generation. An 11.004 MHz signal is used to establish a dot time of approximately 45 ns .

Review Fig. 6-2 and note the breakdown from simple to complex; these signals combine and interact on one another to generate video and control when input/output functions occur.

The TTL Video Logic Signal at the output of U269A is an excellent signal to monitor to show in detail what has been described above. This is discussed further in the following character generation description.

## CHARACTER GENERATION

GENERAL. The circuitry in the upper portion of the schematic contains the Character Generator and video control circuits. Timing requirements are supplied by the timing circuits. Figure $6-3$ shows a partial display illustration; Fig. 6-4 shows the TTI. Video Logic Signal that generates the video shown on the display illustration. The following describes the relationship each component of the


Alpha ROM character. Note that the maximum dot area used by an alphanumeric character is $5 \times 7$, this provides spacing between characters and lines.


Ruling character shown uses a $5 \times 8$ dot matrix. When write dot information appears on the perimeter of the matrix, Terminal logic causes the video circuits to repeat the dot, thus providing solid lines with no gaps (See notes \#1 and \#2).
\#1 Ruling character shown causes Terminal to repeat video sweeps 0 and 9 of the character line.
\#2 Ruling character shown causes Terminal to fill space between ruling characters with video.

Fig. 6-3. Partial Display illustration showing character generation in relation to horizontal sweep.


Fig. 6-4. TTL composite video signal.

TTL Video Logic Signal has to the information displayed in Fig. 6-3.

The TTL Video Logic Signal is monitored at the output of U269A. Assume that all 1920 character spaces have been filled with the opening parenthesis character " $($ ".

TTL VIDEO SIGNAL DESCRIPTION. First review the display illustration, Fig. 6-3, then review Fig. 6-4.

Part A-D of Fig. 6-4 is the TTL Video Logic Signal before conversion to its analog counterpart. Oscilloscope sweep speed is $2 \mathrm{~ms} / \mathrm{div}$. Note that 24 separate groups are visible. Each group is representative of one line of characters. The small spacing between groups is representative of the 3 horizontal lines on which no data appears when generating standard characters. Some lower case characters ( $g, j, p, q$, and $y$ ) are one sweep lower, thus allowing only 2 horizontal sweeps to separate them from the next line of characters. The vertical time (field time) is 16.67 ms and includes vertical retrace time.

Increasing the sweep speed to $50 \mu \mathrm{~s} /$ div shows more detail. Part B of Fig. 6-4 shows that each character line of "(" characters is composed of video information on 7 horizontal sweeps, with 3 sweeps for between-line spacing. Some optional ruling characters use all ten horizontal sweeps for character generation.

Part C of Fig. $6-4$ shows the signal at a sweep speed of $5 \mu \mathrm{~s} / \mathrm{div}$. This shows one sweep that contains 80 negativegoing spikes. These spikes command the writing beam to "turn-on" at the respective "dot position" to write the dot. Note the horizontal retrace time of $27 \mu \mathrm{~s}$.

## RETRACE TIMES

GENERAL. Data transmit and receive functions occur during horizontal retrace time. Keyboard inputs are keyed into memory during vertical retrace.

HORIZONTAL RETRACE. Transmitting and Receiving Functions occur during horizontal (sweep) retrace times. This is a period of $27 \mu \mathrm{~s}$ reserved for these functions.

Input/Output (I/O) is limited to one character per horizontal sweep. This allows a maximum local I/O rate of 15,720 characters per second ( 262 sweeps per field $\times 60$ fields per second equals 15,720 characters per second).

The number 206 refers to the preset count on the outputs of the $\div 50$ counter ( U 1 and U 21 ) in the timing circuitry. This count is preset every 50 STEP times. Each horizontal sweep contains two, 50 -count cycles of the $\div 50$ counter. The first 17.5 STEP times every other 50 -count cycle, are used for $1 / O$ timing. Figure $6-5$, parts $A$ and $B$, illustrates the timing signals that control transmit and receive functions.

For I/O functions, the timing circuits sequentially generate the $\overline{R E A D}$, STROBE, $\overline{\text { STORE }}$ and EXECUTE signals. These signals are acted upon by TSTROBE, $\overline{C S T R O B E}, \overline{C P U N T}$, and TBUSY to perform the I/O functions. Individual signal descriptions are given in the Dictionary of Line Titles, this section.

VERTICAL RETRACE. During vertical retrace, $\overline{\text { VSYNC }}$ goes active for 3 sweep times ( $190 \mu \mathrm{~s}$ ) to enable Keyboard entries in to memory.

## CIRCUIT FUNCTIONS

The majority of circuitry can be divided into function blocks that are described below.
22.008 MHz CRYSTAL OSCILLATOR. This is the master timing oscillator that provides timing for Terminal operation. Division by two provides 11.004 MHz pulses for video and field timing.

Display and Input/Output timing is provided by:
A. U11, a $\div 16$ counter that is preset to a count of 9 each time it is loaded. Seven 11.004 MHz clocks generate a load (STEP) signal from Carry Out, pin 15. STEP corresponds to a character time.
B. U1 and U21 provide timing control for the horizontal sweep and the input/output functions that occur during sweep retrace. This counter is preset to a count of 206. 50 clock (STEP) pulses enable a Carry Out signal from U21. This counter (U1 and U21) cycles twice to provide 100 counts before a clock pulse is generated from U141B for the Field Counter. 100 STEP pulses correspond to one horizontal sweep time.
C. U31 and U41 provide field timing. A field is composed of 262 horizontal sweeps. This counter is preset to a count of 125 ( 99 for 50 Hz line voltage) and must receive 131 clock pulses from U141 before the Carry Out line from U41 goes high. This counter also counts twice for each field. Two 131 count cycles enable a high going pulse from U61A. This equals the field rate of $16.67 \mu \mathrm{~s}$.

DMA CONTROL. This circuitry slows down the STEP and STROBE signals during Direct Memory Access (DMA) and refresh operations. $\overline{\text { STEP }}$ changes duration to enable RAMs to be refreshed, or to perform functions such as clear screen, insert and delete line and character.

DMA functions vary in length of time. U359B assures that when a DMA function is completed, normal operation is re-established at the 50th character time of a sweep and not during an I/O cycle.

VIDEO PATH. Video Path includes Data Latches, two Read Only Memory (ROM) chips, Dot Multiplexer (U389), various gating, and the output drivers, Q397, and Q398.

TWO CHARACTER DELAY. The ASCII code for a character to be displayed is read during DISPLAY time. A character is written when the $X$ EQUAL and $Y$ EQUAL signals are true. This signifies that the Cursor Registers agree with the Display Registers. Normal operation is to generate a cursor at this time. However, because it takes two character times to display the character just read, the cursor must also be delayed two character times to assure proper position over the character.

FIELD ATTRIBUTE CODE STORAGE. This circuitry decodes and stores the Field Attribute Code (FAC). The FAC is stored until another FAC, or the end of the line is detected. U381A and U141C are the gates which recognize a FAC. They supply the pulse that clocks the FAC into the Field Register, U401.

BLANKING CONTROL. This circuit inhibits video output during a clear page function and ensures that it is not re-enabled until $\overline{V S Y N C}$ goes true. Data display continues from the top of the page; not from the middle.

CURSOR GENERATOR. When $X$ EQUAL and $Y$ EQUAL are true, the cursor is generated. U341 causes a delay which enables video inverrsion. The field rate is

(B) Transmitting.

NOTE 1..CPUNT precedes data from the interface by $6.36 \mu \mathrm{~s}$.
NOTE 2..Data is read from the minibus into memory during TSTROBE and $\overline{\text { STORE }}$ at STROBE time.
NOTE 3.. $\overline{T B U S Y}$ is asserted by the 4023 when the data is being processed by the 4023. $\overline{C B U S Y}$ is asserted by the computer interface when data is sent to the computer. Both TBUSY and $\overline{C B U S Y}$ are asserted when data is being executed by 4023 and is being sent to the computer.

NOTE 4..When reading the cursor position to the computer, $\overline{\text { CSTROBE }}$ goes active for the duration of STROBE during $\overline{R E A D}$ time. During Buffer Entry or keyboard entry (Direct), $\overline{\operatorname{CST} T R O B E}$ goes active for the duration of STROBE during STORE time. The computer interface sets $\overline{\text { CBUSY }}$ active until the entry is completed.

Fig. 6-5. Input and Output Timing.
divided by 16 to produce the 4 Hz blink. The Cursor Blink Strap controls when the cursor will blink; either continuously or only when the RESET key is pressed.

READ ONLY MEMORY ROW DECODERS. This group of circuitry provides logic for ROM row decoding. U351 is a BCD decade counter that is clocked at the sweep rate. It sequentially counts 10 sweeps to provide BCD outputs for U261, and row selection for ROM A. The ROM B Latch, U261, latches one count behind the ROM A count, thus causing the ROM B dot matrix to "fall" one dot position for some lower case characters. A comparison between ROM row selection is provided by Table 6-1.

Steering provided by gates located at the output of U261, select row codes for lower case or optional ruling characters.

VIDEO BLANKING OF UNUSED HORIZONTAL SWEEPS. The output of this group of gates controls video blanking on specific horizontal sweeps of a line of characters. Table $6-1$ shows that when ROM $A$ is selected sweeps 8 and 9 are blanked; when ROM B is selected, sweeps 0 and 9 are blanked; no sweeps are blanked when generating a ruling character.

RULINGS SPREAD. Cutting the Rulings strap enables the "spreading" of dots between ruling characters.

## MISCELLANEOUS

The remaining circuitry on this card consists of auxiliary video generators for the Hard Copy Unit and external monitors, and various timing logic for control of display and input/output functions.

## KEYBOARD INTERFACE CARD

## INPUTTING KEYBOARD DATA

Refer to the Keyboard Interface schematic. A component locations illustration is provided on the apron of the schematic. Data keyed from the Keyboard is accompanied by KSTROBE. KSTROBE activates the Keygate Circuit, which generates a KEYGATE signal during the next vertical retrace interval. When KEYGATE is generated (during $\overline{\mathrm{VSYNC}})$, data is latched through the Data Input Gates and onto the minibus. KEYGATE also activates $\overline{\text { TSTROBE }}$ and/or CSTROBE (as described in the description of that circuit) to cause the data to be processed by the Terminal and/or the Computer Interface.

TABLE 6-1
COMPARISON OF 10 HORIZONTAL SWEEPS TO ROM ROW SELECTION

| Sweeps per line of chars | BCD Count From U351 | Upper Case ROM A P/N 156-0147-00 | ROM Row Selection |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Lower Case ROM B P/N 156-0401-00 | Optional Ruling ROM B P/N 156-0401-00 |
| 0 | 0000 | 0 | Blanked | $\begin{aligned} & \text { (repeat of }_{\text {ROM row \# } \# \text { ) }} \end{aligned}$ |
| 1 | 0001 | 1 | 0 | 0 |
| 2 | 0010 | 2 | 1 | 1 |
| 3 | 0011 | 3 | 2 | 2 |
| 4 | 0100 | 4 | 3 | 3 |
| 5 | 0101 | 5 | 4 | 4 |
| 6 | 0110 | 6 | 5 | 5 |
| 7 | 0111 | 7 | 6 | 6 |
| 8 | 1000 | Blanked | 7 | 7 |
| 9 | 1001 | Blanked | Blanked | $\begin{aligned} & 7 \text { (repeat of } \\ & \text { ROM row \#7) } \end{aligned}$ |

Note dropping of Lower-case characters one sweep. Lower-case characters, g, j, p, q, and y have tails written on 7th ROM row, thus extending one sweep lower than other alphanumeric characters.

## Theory of Operation-4023 Service

The data placed onto the minibus is also latched through U109 and U209 during STORE and $\overline{\text { STEP }}$ time. With data on the outputs of these latches, it can be decoded by the Control Character Decoders and processed by applicable steering circuitry.

## CONTROL CHARACTER DECODERS

Decoding for the NUL, ETX, BEL, BS, HT, LF, VT, FF, CR, and SI Control Characters is provided by U129 and U131. These characters cause register manipulation, bell ringing, page clearing, and erase input functions to be performed.

Information on the effects of individual control characters can be found in the following circuit descriptions.

NUL, BEL, and ETX-Miscellaneous Circuits and Functions

BS, HT, and VT-Register Control Enabling Circuit
CR and LF-Carriage Return and Line Feed Circuits

SI-Clear Page and Erase Input Circuits

## KEYGATE GENERATOR WITH REPEAT

This circuit is activated by the KSTROBE signal. It generates the KEYGATE signal when keying data from the Keyboard and when using the Position Cursor Controls. It provides a one-time activation of KEYGATE for each KSTROBE.

KEYGATE goes active during vertical retrace time (it is during vertical retrace that VSYNC goes active), between 3 and 19 ms after $\overline{\text { BOUNCE }}$ becomes inactive. $\overline{\text { BOUNCE }}$ is generated when keys such as the edit, erase input, and cursor position keys are depressed. If BOUNCE remains active for more than 300 ms , KEYGATE has a 15 Hz repetition rate for edit and cursor movement functions.

The CONSOLE LOCK Strap prevents KEYGATE from being generated, and would be used when all keyboard inputs are to be inhibited. The KLOCK signal is activated when the cursor is positioned over a FAC (Field Attribute Code) or in a protected field. It prevents KEYGATE from being generated, thus inhibiting keyboard entry into a protected field.

## TSTROBE AND CSTROBE CONTROL

Keyboard data is not acted upon by the Terminal and/or the computer until $\overline{\mathrm{TSTROBE}}$ and/or $\overline{\mathrm{CSTROBE}}$ are
activated. When keying directly to the computer, the DIRECT signal is active (DIRECT-BUFFER switch is at DIRECT). Keyboard data is directed to the Interface Card when KEYGATE enables CSTROBE. In Direct, the Terminal does not process keyboard inputs unless an "echo" condition is provided. This can be provided by either the computer, the modem, or the Interface Card. The ECHO signal is enabled by strap placement on the Interface Card, and enables TSTROBE to be generated when keying data from the Keyboard in Direct.

TSTROBE is controlled in the afore-described manner as long as KLOCK remains false. Whe KLOCK goes true, the only time TSTROBE goes true (when keying in data) is when one of the following is detected by U49A.

1. Keying data with the RESET Key depressed (this permits keying into a protected field and keying over a FAC).
2. VT Control Character.
3. HT Control Character.

## MOVE CURSOR TIMING

This circuitry provides enabling signals at the proper times for the register control signals, CLRX, $\overline{C L R Y}, \overline{U P}$, $\overline{\text { DOWN, }} \overline{\text { LEFT, and }} \overline{\text { RIGHT. The output of U191D is }}$ enabled at EXECUTE time when KEYGATE is active and remains active until the next $\overline{\text { STEP }}$ time. This is the time when the register controls activated by the KLEFT, $\overline{\mathrm{KRIGHT}}, \overline{\mathrm{KUP}}$, and $\overline{\text { KDOWN }}$ inputs are enabled. Note also the $\overline{\mathrm{STEP}}$ and $\overline{\mathrm{EXECUTE}}$ time is also used to clear the X and $Y$ Registers when the HOME key is pressed.

The output from U179A is used to enable other register control gates. The output of these gates go true when enabled by their respective decoded Control Character output from U131. These gates, their outputs, and the Control Character that activates the output are shown in Table 6-2.

TABLE 6-2

| GATE | INPUT CONTROL <br> CHARACTER | OUTPUT |
| :--- | :---: | :--- |
| U389B | HT | $\overline{\text { RIGHT }}$ |
| U361C | BS | $\overline{\text { LEFT }}$ |
| U351B | LF | $\overline{\text { DOWN }}$ |
| U391B | LF | $\overline{\mathrm{CLRX}}$ (LF does CR) |
| U391C | CR | $\overline{\mathrm{CLRX}}$ |
| U351C | CR | $\overline{\text { DOWN }}$ (CR does LF) |

## MOVE CURSOR GATES

The UP, DOWN, LEFT, RIGHT, and HOME keys are non-encoded keys that control cursor positioning by manipulating the count in the Cursor Registers located on the Cursor Card. Pressing the HOME key causes the X and Y Cursor Registers to clear. This positions the cursor to home. The KUP, KDOWN, $\overline{K L E F T}$, and KRIGHT signals increment or decrement the count in the Cursor Registers. The cursor position reflects the count from these registers.

## CARRIAGE RETURN AND LINE FEED CIRCUITS

CARRIAGE RETURN. Decoding CR activates this circuit to enable CLRX. CLRX clears the $X$ Cursor Register, causing the cursor to position to the left margin. The CR DOES LF strap also enables line feeds to be performed when CR's are decoded. This is the standard Terminal configuration.

LINE FEED. Decoding the LF Control Character causes the $\overline{\mathrm{DOWN}}$ signal to be activated. $\overline{\mathrm{DOWN}}$ increments the count in the Y Cursor Register, thus moving the cursor down one line. This circuit can be strapped to also perform a carriage return with line feed if desired. The standard Terminal is strapped not to generate a carriage return with line feed.

## CLEAR PAGE AND ERASE INPUT CIRCUITS

CLEAR DATA INITIATE CIRCUIT. This circuit detects when a decoded (or keyboard input) Clear Page or Erase Input function is commanded. U131 decodes the program commands, FF (Clear Page) and SI (Erase Input). These Control Characters must be preceded by ESC before their respective functions can be initiated (ESC is decoded by the Control Card, which sets $\overline{\text { LCE }}$ active.) Cutting the FF ERASE strap obviates the need to precede FF with ESC. Pressing the PAGE-ERASE INPUT key with SHIFT depressed initiates the Clear Page sequence from the keyboard; pressing PAGE-ERASE INPUT without SHIFT initiates Erase Input.

Whenever one of these functions is to be performed, the output of U261B goes high. The effect of this high-going signal can be found in the description of the Clear Page Control Circuit. Detecting an Erase Input function also enables the output of U51B. The effect of this low-going signal can be found in the description of the Erase Input Control Circuit.

CLEAR PAGE CONTROL. The purpose of this circuit is to enter a DMA (Direct Memory Access) cycle. All data in memory is read onto the minibus a character-at-a-time and, if it is a Clear Page function, it is not written back into memory but is deleted. If an Erase Input function is being performed, all protected data, if any, is written back into memory (more about Erase Input in the Erase Input Control Description).

A high-going signal from U261B enables this circuit. $\overline{D M A}$ is activated and the cursor positions to home by $\overline{C L R X}$ and CLRY signals that clear the Display Registers. $\overline{\text { RIGHT }}$ is activated and $\overline{\text { STEP }}$ signals increment the $X$ Display Register from 0 to 79 (see circuit description of Cursor Card). When the last character of the line is reached (count 79), EOL DIS goes active. $\overline{\text { CLRX }}$ once again goes active as well as $\overline{\mathrm{DOWN}}$, which causes the Y Display Register to increment the count to the next line of characters. The cycle repeats until the last line is reached, at which time LSTYDIS goes active. When the last character of the last line is read onto the minibus, EOL DIS causes $\overline{C L R X}$ and $\overline{C L R Y}$ to position the cursor back to home. $\overrightarrow{D M A}$ goes inactive, and the Clear Page (or Erase Input) sequence is terminated.

ERASE INPUT CONTROL CIRCUIT. This circuit determines which data read from memory in an Erase Input sequence is deleted or read back into memory. Field Attribute Codes (FAC's) define this data as being protected or unprotected. Any character that has $\overline{\text { BIT }} \mathbf{8}$ true is defined as a FAC and is automatically protected. An Erase Input function does not erase FAC's. The Erase Input circuitry monitors $\overline{\text { BIT } 8}$ to determine if the character is a FAC, and if it is, it samples BIT 2 of the FAC for protection status of the data that follows the FAC. Circuit operation is as follows.

Initiating Erase Input sets DMA active. See description of Clear Page and Erase Input Circuit. Also see Edit Card and Cursor Card descriptions for more information on DMA operation. The cursor begins scanning the memory a character at a time, a row at a time. An Erase Input function sets the output of U51B low. This one-sets U251A whose high-going output enables the Erase Input Control Circuit. As the cursor is moved to each character, it is read from memory and placed on the minibus. It is latched through U109 and U209, where it is sampled by the Erase Input Control Circuitry for $\overline{\text { BIT } 2}$ and $\overline{\text { BIT } 8}$ information, as described above. If the character is a FAC, the output of U241A goes high. This enables the Data Output Gates, placing the character back on the minibus. It is then read back into memory at the same location. If BIT 2 of the

FAC defines, as protected, the data that follows, all data up to the next FAC or the end of the line, follows the same cyclical pattern: from memory, to minibus, through U109 and U209, through Data Output Gates, to the minibus, and back into memory. If BIT 2 defines the data as being unprotected, the output of U241A remains low and the data, up to the next FAC, or the end of the line, becomes lost; it is not placed back into memory.

When another FAC is detected, the operation repeats. Again, whether the data the FAC defines is "erased" or not depends on the protection status defined by BIT 2 of the FAC.

RULING ERASE CONTROL. An active $\overline{B I T} 9$ defines the character it is concurrent with as being a rulings character. During an Erase Input operation, it is desirous not to erase these characters. Therefore, when a rulings character is detected it is not erased, but written back into memory as described in the preceding description.

An ALTERNATE SET ERASE INPUT Strap can be cut to permit erasure of alternate character set characters (ruling characters).

## PAGE FULL CIRCUIT

BREAK ON FULL. Note the BRK FUL Strap. The Standard Terminal does not enable a BREAK signal on page full. The strap must be cut to enable to circuit operation as follows:

When receiving information from the computer and the cursor positions to the last line, LSTYCRS goes true. Another line feed past the bottom line causes $\overline{D O W N}$ to go true. At $\overline{E X E C U T E}$ time, $\overline{B R E A K}$ is enabled. This inhibits further received data on some systems. The circuit is reset by clearing the page or by pressing the Home key.

BUSY ON FULL. The output from the Page Full Flip/Flop also inputs to the Busy On Full circuit. The Standard Terminal is set to enable $\overline{\mathrm{TBUSY}}$ on page full. The BUSY FUL strap must be cut to prevent TBUSY from going active on page full.

## WRAP-AROUND CIRCUIT

The wrap-around feature is enabled by the Wrap-around Strap. When in Direct mode, typing or moving the cursor past the 80th character position, causes $\overline{C L R X}$ and $\overline{\text { DOWN }}$
to become enabled. This moves the cursor down one line and to the left margin.

## MISCELLANEOUS CIRCUITS AND FUNCTIONS

BELL CIRCUIT. This circuit is activated from one of three sources; when $\overline{\text { DING goes active, when attempting to }}$ enter keyboard data into a protected field, and when ESC $B E L$ is decoded. Bell ringing occurs during VSYNC time (vertical retrace).

RUBOUT SUPPRESS. Detecting a rubout character $\left(127_{10}\right)$ causes the output of U229 to enable TSUP. This suppresses Terminal response to that character (as long as $\overline{D M A}$ is inactive and the RESET key is not depressed).

NUL AND ETX. Two control characters not previously discussed are NUL and ETX. Either of these characters activates TSUP. However, ETX causes the cursor to space to the right via U341. All control characters cause cursor spacing to the right if RESET is held down. NUL prevents spacing and inhibits Terminal response to that character.

## CONTROL CARD

## GENERAL CIRCUITRY INFORMATION

Refer to the Control Card schematic. A component location illustration is provided on the apron of the schematic. The following descriptions provide basic information on circuitry contained on the Control Card.

CONTROL CHARACTER DECODER. This circuitry decodes the SI, BEL, CR, ENO, VT, ETX, SO, ACK, and NUL Control Characters which are used as follows.

SI Computer-initiated control command that initiates transmission of transmittable data only (SI must be preceded by ESC).

SO Computer-initiated control command that initiates transmission of buffer contents, transmittable and non-transmittable data (SO must be preceded by ESC).

When preceded by ESC, a computercontrolled Make Copy request is initiated.

CR Stored CR and ETX codes are used in Buffer ETX entry as Message Separators.

| NUL | NUL's reside in memory where data is not <br> entered. During Buffer transmission, NUL's <br> are decoded for Null Suppression. |
| :--- | :--- |
| VT | These are decoded but perform no useful <br> function. |
| ACK |  |

ESC DECODER. An ESC Decoder, U251, and associated circuitry, sets LCE active on receipt of the ESC Control Character. $\overline{\mathrm{LCE}}$, plus the next $\overline{\mathrm{TSTROBE}}$, triggers the CPU Delay Response Multi, U31, to enable CBUSY. CBUSY prevents immediate transmission of cursor coordinates following receipt of the closing bracket (]) code that follows ESC.

PROMPT CHARACTER DECODER. Decodes the Prompt character selected by the Line Prompt Straps when transmitting line-by-line. Receipt of Prompt Character also triggers the CPU Delay Response Multi, U31. As with ESC, $\overline{\text { CBUSY }}$ goes active for duration of on time of U31. ( 0.5 second is standard). A lower value resistor can be strapped in to provide an on time of about 50 ms for shorter delay time requirements. Note that the 1 k resistor is already installed.

MAKE COPY SIGNAL. $\overline{M A K E ~ C O P Y ~ i s ~ g e n e r a t e d ~ u p o n ~}$ receipt of ESC followed by BEL. (Note LCE "arms" U339A.) When the Hard Copy Unit begins making a copy, $\overline{H C U} B U S Y$ goes active.

CONDITIONAL TRANSMIT/FIELD INHIBIT. The $\overline{\text { ENTER }}$ signal is enabled as a result of a Send or Enter transmission sequence initiated from the keyboard or under program command from the computer (note that the $\overline{K S E N D}$ and $\overline{K E N T E R}$ signals enable $\overline{B O U N C E})$. The enter sequence initiated from the keyboard causes an ETX code to store at the cursor location; send does not store an ETX. Also, if $\overline{\text { BIT }} \mathbf{8}$ is true, enter sequences will not cause an ETX code to be generated.

ERASE TO END CONTROL. This circuit initiates and stops the Erase to End Function. In BUFFER, Erase to End is inhibited at the end of a line (EOL CRS goes active) or if a FAC(s) is in the line, the function is terminated when the next FAC is detected. With Wrap-around Strap "IN", and DIRECT selected, Erase to End causes a carriage return/line feed to be executed at the end of the line.

EOL LF GEN STRAP. LF (line feed) generation and transmission are dependent on position of this strap. See Strappable Option.

END CHARACTER GENERATION. An End character is generated and transmitted as the last character of a buffer transmission or a Read Cursor operation. The specific End Character is dependent on the position of the End Character Straps. See Strappable Options.

PROTECTED FIELD AND NON-ALPHA FIELD DETECTION. This circuitry located on the lower portion of the schematic, is controlled by $\overline{\text { BIT 1 }}, \overline{\mathrm{BIT}} 2, \overline{\mathrm{BIT} 6}, \overline{\mathrm{BIT} 7}$, and the FA signal (from U201B). The following functions are performed:

1. Inhibits keyboard writing when cursor is located in a protected field ( $\overline{K L O C K}$ goes active).
2. Allows only non-alpha characters to be written in non-alph fields.
3. Rings bell and prevents Terminal from writing data in a protected field and alpha data in a non-alpha field.

## miscelbaneous circuits and OPERATIONS

CURSOR BLANKING. The cursor is blanked when performing an Erase to End function, making a hard copy, performing NUL suppression, when cursor is tabbing over optional ruling characters or through a non-transmittable field, or when seeking a preceding Message Separator after initiating a Buffer transmission sequence.

SEND 8 FUNCTIONS. $\overline{\text { SEND } 8}$ inhibits the following Cursor Card functions:

1. Control Character Decoding.
2. ESC Decoding.
3. FAC Detection. A buffer that contains FAC's will not have the FAC code preceded by the Field Segregator (US) when transmitting.

ALTERNATE CHARACTER SET NOT TRANSMITTABLE. $\overline{\text { BIT } 9}$ true signifies that the character concurrent with $\overline{\text { BIT } 9}$ is an optional ruling character. Normally, ruling characters are non-transmittable, regardless of Field Attribute Codes. Cutting the ALTERNATE SET XMIT strap allows transmission of alternate character set characters.
$\overline{\text { CPUNT. CPUNT }}$ is placed on the minibus by the Interface Unit (full duplex operation) and is used to inhibit data outputs of the Control Card.

## EXPLANATION OF TRANSMISSION CONTROL

GENERAL. The following is a basic description of the transmission sequences that occur as a result of initiating a Send or Enter sequence. The description covers most aspects of a buffer transmission. The circuitry being discussed is found at about the center of the schematic. Due to its complexity and interaction, the circuitry will be discussed by operation.

STATE DESCRIPTIONS. Ten logic states are provided by a State Circuit that consists of a State Register, U381, a BCD decoder (U281), and associated circuitry. Each state controls the outputs and also the state that is set next. These Control States are shown in the Transmission State Diagram, Fig. 6-6 and are explained in Table 6-3.

TABLE 6-3

| State | BCD Output U381 | Decimal Output U281 | Description |
| :---: | :---: | :---: | :---: |
| Initial | 1000 | $\begin{gathered} 8 \\ (\operatorname{Pin} 10) \end{gathered}$ | Initial is obtained by power-up, PAGE, HOME, RESET, and ESC. These conditions return circuitry to the Initial State regardless of preceding state. |
| Left One | 1001 | $\begin{gathered} 9 \\ (\text { Pin 11) } \end{gathered}$ | Obtained when transmission sequence (Enter or Send) is initiated. A $\overline{\text { LEFT signal goes active and is performed at }}$ EXECUTE time. |
| Left Seek | 0000 | $\begin{gathered} 0 \\ (\operatorname{Pin} 1) \end{gathered}$ | $\overline{\text { LEFT }}$ remains active to be performed every EXECUTE until one of the conditions for change of state is obtained. |
| Stuff Right and Up | 0001 | $\begin{gathered} 1 \\ (\operatorname{Pin} 2) \end{gathered}$ | If a Message Separator code (CR or ETX) or the Home Position have not been reached and the cursor is at the left margin, $\overline{\text { HIX }}$ and TSTROBE signals, as well as code for lower case " o ", are set. These signals position the cursor to the right margin at $\overline{\text { STORE }}$ time. $\overline{U P}$ is set to position the cursor up one line at EXECUTE time. |
| Off ETX | 0010 | $\begin{gathered} 2 \\ (\operatorname{Pin} 3) \end{gathered}$ | When cursor is moved back to a preceding ETX or CR code, cursor movement stops. This state sets circuit outputs to move the cursor off the Message Separator code before transmission begins. This is done by setting RIGHT active to be performed at EXECUTE time. Once the cursor is moved off the Message Separator, CSTROBE is set and transmission begins. If cursor moves back to the Home position without encountering a Message Separator, $\overline{\text { CSTROBE }}$ is set immediately. If the Message Separator is in the 80th character position $\overline{C L R X}$ and $\overline{\text { DOWN }}$ go active instead of $\overline{R I G H T}$. |

TABLE 6-3 (cont)

| State | BCD Output U381 | Decimal Output U281 | Description |
| :---: | :---: | :---: | :---: |
| Sending | 0011 | $\begin{gathered} 3 \\ (\operatorname{Pin} 4) \end{gathered}$ | Circuit outputs are set to control data transmission. $\overline{\text { CSTROBE }}$ at $\overline{R E A D}$ time transmits the character. $\overline{\text { RIGHT }}$ at EXECUTE time moves the cursor to the next character. |
| Field Attribute | 0100 | $\begin{gathered} 4 \\ (\operatorname{Pin} 5) \end{gathered}$ | When in transmitting process and a FAC is detected, cursor movement stops on the FAC. If the FAC defines a transmittable field, the circuit generates a US character which is sent via a $\overline{\text { CSTROBE }}$ at $\overline{R E A D}$ time. Transmission continues beginning with the FAC. Should the FAC define a non-transmittable field, no US character is transmitted and transmission of the FAC and all data in that field is suppressed. |
| EOL 1 <br> (CR with LF) | 0101 | $\begin{gathered} 5 \\ (\operatorname{Pin} 6) \end{gathered}$ | When the end of a line is detected, a carriage return/line feed is performed by enabling $\overline{C L R X}$ and $\overline{D O W N}$ to be acted upon at EXECUTE time. If data was transmitted in that line and the end of the line is reached, a CR character is transmitted via $\overline{\text { CSTROBE }}$ at $\overline{\text { STORE }}$ time. |
| $\begin{aligned} & \text { EOL } 2 \\ & \text { (LF) } \end{aligned}$ | 0110 | $\begin{gathered} 6 \\ (\operatorname{Pin} 7) \end{gathered}$ | When the cursor reaches the end of the line in which data was transmitted a LF character is generated and transmitted by $\overline{\text { CSTROBE }}$ at $\overline{\text { STORE }}$ time (see EOL LF GEN Strap). |
| END | 0111 | $\begin{gathered} 7 \\ (\operatorname{Pin} 9) \end{gathered}$ | When the cursor reaches a stored Message Separator at the end of the message, or the last character position of the last line, the End code is transmitted (the specific End character depends on the character selected by the Message End Straps). Performing a $\overline{\text { CLRX }}$ at EXECUTE positions the cursor to the left margin, and the Initial State is set. |



EXAMPLE OF TRANSMISSION CIRCUIT OPERATION. Assume that the information displayed in Fig. 6-7 is to be transmitted to the computer. It contains two lines of information, preceded and ended by Message Separator (CR or ETX) codes. Refer to the transmission state diagram when reading the following.

The Transmission Control Circuitry remains in the Initial State until a transmission sequence is initiated, either from the computer or by the operator at the keyboard. Assume that the cursor was at the end of the message and the operator presses the SEND-ENTER key. An ETX code stores at the cursor location and the cursor begins moving left via $\overline{\text { LEFT }}$ signals at EXECUTE time. When the left margin is encountered, Stuff Right: and Up occurs, being brought about by generating a lower case " o " code and a TSTROBE at STORE time. An $\overline{U P}$ signal is generated and acted upon at EXECUTE time. Cursor movement continues once again to the left until the old ETX code is sensed, at which time cursor movement stops. The Off ETX state is
set to move the cursor off the Message Separator code; transmission then begins with the character following the Message Separator. $\overline{\text { RIGHT signals at EXECUTE }}$ time increment the cursor to the right, with CSTROBE's occuring at $\overline{R E A D}$ time for each character transmitted. When the end of the line is detected, a carriage return/line feed is performed via a $\overline{\text { CLRX }}$ and $\overline{\text { DOWN }}$ at EXECUTE time, and a CR code is set to be transmitted via $\overline{\text { CSTROBE }}$ at $\overline{\text { STORE }}$ time. If an LF is also to be transmitted, it will be valid at $\overline{\text { CSTROBE }}$ in the next STORE time. Transmission of displayed information then continues until the ETX code is encountered, at which time the End code is transmitted. Setting $\overline{\text { CLRX }}$ active causes a carriage return to be performed at the next EXECUTE time. The Initial State is reset.

Further study of the Transmission State Diagram will show the variety of BUFFER transmission operations controlled by the Transmission Control Circuitry.


Fig. 6-7. Data Input described and "Example of Transmission Control Circuit operation."

## CURSOR CARD

## GENERAL

Refer to the Cursor Card schematic. A component location illustration is provided on the apron of the schematic.

## REGISTER DESCRIPTION

The Register chips are 74193 N synchronous 4 -bit up/down counters. The outputs are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held high.

The outputs are programmable; that is, the outputs can be preset to any state by entering the desired data at the data inputs while the Load input is low. The register output changes to agree with the preset data inputs, independent of the up/down count pulses.

The Clear Input pin, which is independent of the Count and Load inputs, forces all outputs to the low level when a high level is applied. The registers are cascaded by using the Borrow and Carry outputs.

The Register Circuitry is divided into circuit blocks to help locate specific circuits that are being discussed. In most cases, individual block descriptions will not be given; circuit operation will be discussed by function.

## CURSOR REGISTER OPERATION

genernal. The Cursor Register includes the Y Cursor Register chips, U39 and U31B and the X Cursor Register chips U41 and U49. The Y Register is incremented at $\overline{E X E C U T E}$ time if $\overline{\text { DOWN }}$ is active. And the count is decremented at EXECUTE time when $\overline{U P}$ is active. Detection of the 24th (or 12th line, optional) inhibits further effects of $\overline{D O W N}$ signals (LSTY CRS goes active). Detection of top line inhibits further effects of $\overline{U P}$ signals (TOPCRS goes active) the $X$ Register increments with $\overline{\text { RIGHT }}$ at EXECUTE time; detection of end of line prevents further $X$ Register increments (EOLCRS goes active). The count from the $X$ Register decrements with LEFT at EXECUTE time; detection of left margin prevents further $X$ Register decrements ( $\overline{\mathrm{LEFT}} \overline{\mathrm{CURS}}$ goes active). The Y Register is cleared with $\overline{\mathrm{CLRY}}$ at $\overline{\text { EXECUTE }}$; the X Register with CLRX at EXECUTE.

## DISPLAY REGISTER OPERATION

REGISTER COUNTING. The Display Register is incremented during DISPLAY time. Every horizontal sweep, at DISPLAY time, the $X$ Display Register is incremented 80 times by the $\overline{\mathrm{STEP}}$ signal. The Y Display Register increments once every 10 horizontal sweeps by the $\overline{\text { DOWN }}$ signal from the Timing Card.

RAM ADDRESSING. The outputs of the Display Register are used to address the RAM (memory) for display. During DISPLAY time, each $\overline{\text { STEP }}$ signal changes the X Display Register to a new character address. The character is read from the RAM, placed on the minibus, and processed by the video circuits on the Timing Card for display. The 80th character position (count 79) triggers the EOL DIS signal from U139B. EOL DIS is delayed one $\overline{\text { DMA }}$ $\overline{\text { STROBE }}$ time before being placed on the minibus. The X Display Register is cleared by $\overline{C L R X}$ and the count begins again. However, the $X$ Display Register is not cleared for two character times after DISPLAY goes inactive. This allows time for $\overline{\mathrm{CLRX}}$ and $\overline{\mathrm{DOWN}}$ functions to be performed. This delay is of primary importance during DMA operation when Edit functions are being performed. (More information on the two-character delay can be found in the description of the "Edit Data Latches" in the Edit Card Circuit description.)

PRESETTING THE DISPLAY REGISTERS. The Display Registers can be preset to one of two preset inputs. Multiplexers U21, U149, and U151 select the preset input count for the Registers. One preset count is the output count from the Cursor Registers. The other set is a preset count established by straps to +5 Vdc and ground. The set selected depends on the state of the $\overline{\mathrm{HIY}}$ and $\overline{\mathrm{HIX}}$ signals.

Note that the Multiplexer enable pins are tied to ground. This permits the Multiplexers to be continually enabled, obviating the need for a load pulse.

Normally, the $\overline{\mathrm{HIY}}$ and $\overline{\mathrm{HIX}}$ signals are inactive. This enables the output from the Display Register Multiplexers to reflect the count set by the +5 Vdc and ground inputs. This provides the preset inputs of LSTYDIS and EOLDIS.

The preset counts from the X and Y Display Multiplexers are used to perform the edit functions and are summarized in the following:

During a Delete Line operation, simultaneously asserting $\overline{U P}$ and $\overline{D O W N}$ "presets" the $Y$ Display Register to the 24th line (LSTYDIS). This occurs 80 times during the Delete Line operation.

During a Delete Character operation, simultaneously asserting LEFT and RIGHT "presets" the $X$ Display Register to the 80th character position on the line (EOLDIS). This function occurs once during the Delete Character operation.

During an Insert Line operation, simultaneously asserting $\overline{U P}, \overline{D O W N}$, and $\overline{H I Y}$ "jams" the Y Cursor Register count into the $Y$ Display Register. This function occurs 80 times during the Insert Line operation.

During an Insert Character operation, simultaneously asserting $\overline{\text { LEFT, }} \overline{\text { RIGHT, and }} \overline{\text { HIX "jams" the } X}$ Cursor Register count into the $X$ Display Register. This function occurs once during the Insert Character operation.

RAM ADDRESS MULTIPLEXERS. The output of Multiplexers U269, U261, and U259 are controlled by

U101 in the Two Character Time Delay circuit. During $\overline{\text { DISPLAY }}$ (and for two $\overline{\text { STEP }}$ times following the trailing edge of $\overline{\mathrm{DISPLAY}})$, and $\overline{\mathrm{DMA}}$ time, these Multiplexer outputs reflect the address count from the Display Registers. During Input/Output time (horizontal retrace) they reflect the count from the Cursor Register. The Cursor Register count is transmitted as data during a Read Cursor operation.

## EDIT EFFECTS ON THE REGISTERS

GENERAL. Edit functions set the DMA mode into operation. DMA operation is a very rapid manipulation of the memory that suspends the normal write/refresh cycles. Edit functions cause the following effects on the Registers, which in turn control the memory.

INSERT LINE. Refer to Fig. 6-8. Initiating this function sets $\overline{D M A}$ active from the Edit Card. The Edit Card also sets $\overline{U P}, \overline{D O W N}$, and $\overline{H T Y}$ active, and at $\overline{S T E P}$ time loads the $Y$ Cursor Register count into the Y Display Register. CLRX clears the X Display Register causing the output count to reflect the left margin position. The output of the Display Register is now the address for the memory. If a character


Fig. 6-8. Inserting a line (assume cursor is in 19 th line).
resides in memory at this location, it is read from memory and latched into the Edit Card. DOWN remains true from the Edit Card causing STEP to increment the Y Display Register, addressing the character on the next line down. If a character resides at this position in memory, it is also read and latched into the Edit Card. A short time later (during the same $\overline{\mathrm{STEP}}$ time) the first character that was latched into the Edit Card, is dumped back onto the minibus to be written back into the memory; but it is written down one line from its original position. The cycle repeats until LSTYDIS is sensed. Any characters in the last line are lost. LSTYDIS causes the Edit Card to simultaneously set UP, $\overline{\mathrm{DOWN}}$, and $\overline{\mathrm{HIY}}$ to jam the Display Register count back to the Cursor Register count. $\overline{\text { RIGHT }}$ goes active for one $\overline{\text { STEP }}$ time to increment the $X$ Display Register one character space to the right.

The above operations continue to repeat in the described sequence until LSTYDIS and EOLDIS are both active. This corresponds to the bottom line and the 80th character position. With the function completed, $\overline{D M A}$ goes false and the cursor address in the Cursor Register once again addresses the RAM. This is the position the cursor was in when the function was initiated. A line of SPACE (SP) characters now reside at the cursor location.

DELETE LINE. Refer to Fig. 6-9. Insert Line also sets $\overline{\mathrm{DMA}}$ active. $\overline{U P}$ and $\overline{\mathrm{DOWN}}$ are simultaneously asserted by the Edit Card to jam the Y Display Register to the bottom line (LSTYDIS). CLRX then causes the count from the Display Register to reflect the first character position on the bottom line; the character at that address is read from memory. If data resides in memory at that location, it is latched into the Edit Card. The Edit Card holds $\overline{U P}$ active so that the Y Display Register can be clocked by STEP signals. Each STEP time the display address moves up one line, latching a new character into the Edit Card latches and a short time later dumping the previous character back onto the minibus to be read back into the memory. However, it is read back into memory at a location that is one line above its old location. This cycle repeats until the $Y$ Display Register count equals the count from the $Y$ Cursor Register. At this time, YEQUAL goes true. $\overline{U P}$ and $\overline{\mathrm{DOWN}}$ are again simultaneously asserted to jam the $Y$ Display Register back to the bottom line (at $\overline{S T E P}$ time). $\overline{\text { RIGHT }}$ is asserted and again at $\overline{\mathrm{STEP}}$ time the $X$ Display Register is increment to the next column of characters. Again, $\overline{U P}$ remains active so that the Y Display Register can be clocked by STEP.

The afore-described process repeats until EOLDIS and YEQUAL go true. At this time $\overline{D M A}$ goes false and the


Fig. 6-9. Deleting a line.

RAM address reflects the count set by the Cursor Registers. A line of 80 NUL characters now reside on the bottom (last) line. The line of data at the cursor location (if any) is "deleted" and all lines below the cursor have moved up one line.

INSERT CHARACTER. Refer to Fig. 6-10A. Inserting a character places a SPACE character at the cursor location. Initiating this function activates $\overline{\mathrm{DMA}}$ from the Edit Card. When the next XEQUAL occurs, $\overline{\text { LEFT }}$ at $\overline{S T E P}$ time decrements the $X$ Display Register one count. The count from the X Display Register reflects the address of the character preceding the cursor. This character is placed on the minibus and latched into the Edit Card. With RIGHT active, $\overline{\text { STEP }}$ increments the $X$ Display Register to the next character position in that line. The character latched into the Edit Card is placed on the minibus, and written back into memory one space to the right. The character that previously resided in that position in memory has been latched into the Edit Card. The cycle repeats itself, moving all characters to the right one space, until EOLDIS is sensed (80th character position). $\overline{\mathrm{DMA}}$ goes inactive and the cursor
reappears. A space character has been entered at the cursor location. If a character has previously been stored in the 80th position, it is lost.

DELETE CHARACTER. Refer to Fig. 6-10B. $\overline{\mathrm{DMA}}$ goes active from the Edit Card and LEFT and RIGHT simultaneously go active to jam the count in the $X$ Display Register to reflect the end of the line. This occurs at STEP time, causing EOLDIS to go active. LEFT remains active and $\overline{\text { STEP }}$ decrements the $X$ Display Register, alternately latching memory contents into and out of the Edit Card. When XEQUAL is sensed, $\overline{D M A}$ goes inactive. All data to the right of cursor is thus shifted left one space, the character at the cursor location is deleted. A NUL character resides in the character position at the end of the line.

## CURSOR ADDRESSING AND READING

GENERAL. Steering of data and register contents is provided by the Cursor Register Card. When performing a Position Cursor or Read Cursor operation, the following occurs.


Fig. 6-10. Inserting and Deleting a character.

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CURSOR POSITIONING. When the Cursor Registers are loaded with $\overline{\text { BIT }} 1$ - $\overline{\text { BIT 7 }}$, the Register outputs reflect the state of the data inputs. This occurs when addressing the cursor to a specific character location. (Specific details on programming the cursor address can be found in the Programming Section of the User's Manual.)

Cursor addressing is initiated when Edit Card circuitry decodes the FS Control Character. Edit Card logic is then set to interpret the next two characters as "position cursor" data. The first character following FS sets $\overline{\mathrm{HIX}}$ active from the Edit Card. This causes that character to be loaded into the X Cursor Register when STORE and STROBE are active. Gates, U111A, U319B, and U11C ensure that the character is a valid $X$ address (not a Control Character). The next character is the $Y$ address. It sets $\overline{\text { HIY }}$ active to load the character into the $Y$ Cursor Register on the next con-current $\overline{\text { STORE }}$ and STROBE signals. Valid $Y$ addresses are checked by U201D and U109B (not a control character or lower case). The count from the X and Y Cursor Register now reflects the new cursor location.

CURSOR READING. When the Edit Card circuitry decodes on ESC ] sequence, it initiates the transmission of the GS Control Character. GS identifies the next two characters that follow as $X$ and $Y$ cursor position information, respectively. When the interface has completed transmission of GS, the trailing edge of CSTROBE enables $\overline{\text { HIX }}$ from the Edit Card. $\overline{\text { HIX }}$ at $\overline{\text { READ }}$ time causes Read Cursor Multiplexers U161 and U169 to sample the X cursor address. This address is placed on the minibus and transmitted. When this byte is transmitted, the trailing edge of $\overline{C S T R O B E}$ enables $\overline{H I Y}$ from the Edit Card: This time, the Y cursor address is placed on the minibus. Information on calculations performed by the program to arrive at the correct cursor address is provided in the Terminal User's Manual.

## MISCELLANEOUS CIRCUITS

Circuitry not previously discussed is used for steering data and control signals, and for the effect of strappable options on the registers. This circuitry is fairly straightforward, so no further discussion on these circuits will be given.

## SUMMARY OF REGISTER OPERATIONS

GENERAL. Logic on the Cursor Card uses VSYNC, $\overline{\text { DISPLAY }}$ and STEP to clear the $Y$ Display Register without a $\overline{\text { CLRY }}$ signal on the minibus. The $X$ Display Register is cleared by a CLRX originating from the Timing Card.

The Cursor and Display Registers will not wrap-around by themselves. When either the high or low limit ( 0 and 79 respectively for X , and 0 and 23 or 11, respectively for Y ) has been reached, the count stops, waiting for the End of line signals to enable a $\overline{C L R X}$ and $\overline{D O W N}$ from the keyboard Interface card. At this time the wrap-around occurs if enabled by the Wrap-around strap located on the Keyboard Interface card. "Register indicators" that control Register counting are:

| EOLDIS | A high true signal that indicates the $X$ <br> Display Register has reached the 80th char- <br> acter position. |
| :--- | :--- |
| EOLCRS | Same as EOLDIS except this one corre- <br> sponds to the Cursor Register. |
| LSTYDISA high true signal from the $Y$ Display <br> Register that corresponds to the bottom <br> character line of the screen. |  |
| LSTYCRSSame as LSTYDIS except this one corre- <br> sponds to the Cursor Register. |  |
| TOPCRS $\quad$The Y Cursor Register outputs this signal <br> when its count indicates the top character <br> line. |  |
| The $X$ Cursor Register outputs this signal <br> when the count indicates the left-most char- <br> acter position. |  |

Examples of Register counting are:
X Display Register When $\overline{\text { STEP }}$ pulses at $\overline{\text { RIGHT }}$ time increment the count to 79, EOLDIS goes active to inhibit the effect of further $\overline{\text { STEP }}$ signals. $\overline{\mathrm{CLRX}}$ must be sent to clear the Register and deactivate EOLDIS. When STEP pulses at LEFT time decrement the count to 0 , LEFTCRS goes active to inhibit the Register's response to further LEFT counts. Incrementing the Register count deactivates LEFTCRS.

X Cursor Register Similar to X Display Register.
Y Display Register When $\overline{\text { STEP }}$ pulses at $\overline{U P}$ time decrement the Register count to reflect the top character line, the Register stops counting. When STEP pulses at $\overline{\text { DOWN }}$ time increment the count to reflect the bottom character line (11 or 23 depending on 12 line option straps), LSTYDIS goes active to inhibit the Register's response to further increments. Sending CLRY deactivates LSTYDIS.

Y Cursor Register

Similar to Y Display Register except Y Cursor Register outputs TOPCRS to reflect the top line count.

PURPOSE OF CURSOR REGISTER. Writing data into the RAM at the address set by the Cursor Register is done when $\overline{\mathrm{HIX}}$ and $\overline{\mathrm{HIY}}$ are inactive This happens with a $\overline{\text { TSTROBE }}$ at STROBE and STORE. However, if $\overline{\text { HIX }}$ is active at STORE, minibus data will be preset into the $X$ Cursor Register. The operation is the same for $\overline{\mathrm{HIY}}$ and the character that addresses the Y Cursor Register. Table 6-4 summarizes data transfer on the minibus and its effects on the Registers.

TABLE 6-4

## DATA EFFECT ON REGISTERS

| $\overline{\text { HIX }}$ | $\overline{\text { HIY }}$ | READ | $\overline{\text { STORE }}$ |
| :---: | :---: | :---: | :---: |
| False | False | Data from RAM <br> at cursor address | Data to RAM <br> at cursor address |
| False | True | Y Cursor Coordi- <br> nates to minibus | To Y Cursor Reg- <br> ister from minibus |
| True | False | X Cursor Coordi- <br> nates to minibus | To X Cursor Reg- <br> ister from minibus |

DIRECT MEMORY ACCESS (DMA) OPERATION.During DMA operation, the Cursor Register count does not change. Its output is used for comparison by the X Display Register. Depending on the Clear Page or Edit function being performed, the following signals perform their function on the Display Register at STEP time: $\overline{U P}, \overline{D O W N}$, $\overline{\text { LEFT, }} \overline{\mathrm{RIGHT}}, \overline{\mathrm{CLRX}}$, and $\overline{\mathrm{CLRY}}$. The action performed by these register control signals occurs in the middle of $\overline{\text { STEP }}$ time. Summary of their operation during DMA time is given in Table 6-5.

TABLE 6-5
OPERATION OF REGISTER CONTROL COMMANDS IN DMA MODE (at $\overline{\text { DISPLAY }}$ and $\overline{\text { STEP }}$ time)

| HIX | $\overline{\text { HIY }}$ | $\overline{\text { UP - } \overline{\text { DOWN }} \text { SIGNALS }}$ |  |  | $\overline{\text { LEFT - }}$ RIGHT SIGNALS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\overline{\mathbf{U P}}$ | DOWN | $\overline{\text { UP AND DOWN }}$ | LEFT | RIGHT | LEFT AND RIGHT |
| False | False | Decrement Y <br> Display <br> Register | Increment $Y$ <br> Display <br> Register | Preset $Y$ Display <br> Register to LSTYDIS (12th or 24th line) | Decrement X <br> Display <br> Register | Increment X <br> Display <br> Register | Preset $\times$ Display Register to EOLDIS |
| False | True |  |  | Transfer $Y$ Cursor Coordinates to $Y$ Display Register |  |  |  |
| True | True <br> or False |  |  |  |  |  | Transfer X Cursor Coordinates to $X$ Display Register |
|  |  | $\overline{\text { DISPLAY }}$ |  | $\overline{\text { DMA }}$ | $\overline{\text { DISPLAY }}$ |  | $\overline{\text { DMA }}$ |

## RANDOM ACCESS MEMORY <br> (RAM) <br> CARD

## INTRODUCTION

Refer to the RAM Card schematic. A component location illustration is provided on the apron of the schematic. The RAM Card contains MOS RAMs which store data for screen display. Timing is provided by the Timing Card, data source is the minibus, and RAM address inputs come from the Cursor Card. Address inputs are BCD 0-79 for $X$ and BCD $0-23$ for $Y$. The RAM Card contains arithmetic logic that converts each distinct $X-Y$ code into the proper RAM address equivalent. Miscellaneous circuits not connected with the operation of the RAM Card are the initialization circuit and the 4.9 MHz Crystal Oscillator.

## OPERATION OF MAJOR CIRCUITS

INTRODUCTION. Data from the memory is placed on the minibus via a "read" operation. Data is placed in memory via a "write" operation.

The RAMs are shown at approximately the center of the schematic. Note the two sets. One set provides storage for the upper 12 lines (Set 2), the other set for the lower 12 lines (Set 1).

SELECTING THE RAM SET. The specific set is selected by the Set Selector and the Upper and Lower Set Enable Gates, U155B and U155A, respectively. When the cursor moves into the 13th line, the output of the U345C changes, disabling U155B and enabling U155A. Thus, the RAM address is "steered" to the applicable set of RAMs. When cut, the 12 LINE RAM strap (in the Read to Minibus Enable Circuit) disables the output amplifiers when moving the cursor past the 12th line.

READ/WRITE ENABLING. The Read/Write input (pin 3) of the RAM is dual purpose. A low at this input tells the RAM that data on pin 11 is to be written into memory at the address determined by the Row and Column Address Inputs. The Chip Enable Input (pin 13) must be low to write (store) into memory.

The Read/Write Input is controlled by the output of U141B. The operation of this gate and associated circuitry can be reviewed in conjuction with the timing diagram provided in Fig. 6-11.

U347 will not allow data to be written unless a $\overline{\text { TSTROBE occurs with } \overline{\text { STORE }} \text { or } \overline{D M A} \text {. Reviewing the }}$ minibus signal descriptions of the remaining inputs to U347 will tell what conditions inhibit writing into memory.


Fig. 6-11. RAM write timing.

Reading is accomplished with the Read/Write Input held high. Data output from the RAM directly follows the application of an address at the Row and Column Inputs.

RAM REFRESHING. The dynamic memory cell used in the RAM will not store data indefinitely. Stored data is "refreshed" in the RAM at the rate of 32 bit locations every $190.8 \mu \mathrm{~s}$. Rewriting is accomplished internally without the need to re-apply external data.

Refreshing is accomplished during both the write cycle (previously discussed) and the Refresh Cycle. During a write cycle the state of the row address (R1-R5) not only determines which row the written character will be stored in, but also refreshes all 32 bits residing in that row. However, writing data into memory does not ensure that each of the 32 possible row addresses is refreshed in the time necessary to retain memory; therefore, Refresh Circuitry is provided.

The refresh cycle is identical to the write cycle except that the RAMs are disabled while the Read/Write Input is pulsed. Disabling the RAMs removes the data output and also prevents data at the Data Input from being written into memory. A refresh cycle consists of 32 address changes and associated write pulses.

The Refresh Circuitry consists of U341B, U321A, U45, U341A, and U321D. Refer to the timing diagram in Fig. 6-11. This is a partial illustration of the timing conditions that occur during horizontal retrace. The period of time between the trailing edge of $\overline{R E A D}$ and the leading edge of $\overline{\text { STORE }}$ is reserved for memory refreshing. During this time, a low $\overline{R E F R E S H}$ signal from U311F enables a high from U321C. This enables the STROBE signal to pulse the output of U141B twice during the low time of REFRESH. Each low-going "write" pulse from U141B refreshes 32 bit locations.

The $\overline{\text { REFRESH }}$ signal is a result of the high from U341B that has been enabled by the trailing edge of $\overline{R E A D}$. The Q output of U341B is inverted by U311F to enable a high from U321C (as previously mentioned) and also disable the SET 1 and SET 2 outputs. Thus the RAMs are disabled for refreshing.

To ensure that each of the 32 RAM rows is refreshed, refresh memory is provided by U45, U341A, and U321D. The high output of U341B enables STEP to pulse the
output of U321A twice during each sweep. This provides two clock pulses for the input of U 45 . U45 is a 4-bit binary counter with outputs to Row Multiplexer, U51. The outputs of U51 are controlled by the level on pin 1. If it is low, (not refresh time) the X1-X4 inputs from the Cursor Card affect the row address; if high (Refresh Time) the U45 outputs affect row address. Row 16 of the Refresh Row Address is provided by U341A and U321D.

In summary, the Refresh Circuitry provides $2 \overline{\text { REFRESH }}$ pulses every horizontal sweep. Thus, the entire memory is refreshed every 16 sweeps. A refresh cycle takes approximately $100 \mu \mathrm{~s}(16 \times 6.36=101.76 \mu \mathrm{~s}$ ).

READ TO MINIBUS ENABLE. This circuitry controls whether or not data read from the RAM's is placed on the minibus. Data is read from the RAM's during a Normal Read operation, Read Cursor operation, and during a DMA operation.

ADDRESS DECODING. The position in which a character is to be written in the RAM or the position that is to be read from the RAM depends on the state of the 5 column and 5 row address inputs. In turn, these address inputs depend on the 7X and 5Y outputs from the Cursor Card.

The outputs from the Cursor Card are binary counts of $0-79$ for $X$ and $0-23$ for $Y$. The position represented by these inputs must be arithmetically decoded into their RAM address equivalent. This is the purpose of the RAM Address Decoding ( $80 \mathrm{Y}+\mathrm{X}$ ) Circuitry.

## SENSE AMPS

These amplifiers are used to amplify data from the RAMs before the data is placed onto the minibus.

## MISCELLANEOUS CIRCUITS

INITIALIZING CIRCUIT. This circuit consists of U371 and associated circuitry. When power is initialized, a momentary low at pin 2 activates $\overline{\text { PAGE }}$ to trigger a Clear Page function. This ensures that tive memory is cleared and the cursor is positioned at home. $\overline{\text { PAGE }}$ also trigger KEYGATE from the Keyboard Interface Card to reset U371A.
4.9 MHz CRYSTAL OSCILLATOR. This oscillator provides 4.9 MHz and $614 \mathrm{kHz}(4.9 \mathrm{MHz} \div 8)$ square waves for interface timing requirements.

## EDIT CARD

## INTRODUCTION

Refer to the Edit Card schematic. A component location illustration is provided on the apron of the schematic. Because the operation of this card and the Cursor and RAM cards are so inter-related, an over-view of Edit Card functional operation is provided. Fig. 6-12 is a Block Diagram of the Edit, Cursor, and RAM Cards.

Assume the operator initiates an edit function. The Edit Card recognizes the function to be performed and, in proper timing order, activates the required Register Control signals ( $\overline{U P}, \overline{D O W N}, \overline{L E F T}, \overline{R I G H T}, \overline{H I Y}, \overline{C L R X}$, etc.). These Register Control signals, together with timing inputs, increment or decrement the registers to obtain data addresses for the RAM card. The data is read from the RAM and latched into the Edit Card for a two-character time delay, before being placed back onto the minibus and read back into memory. The delay time allows time for the X and Y Display Register to increment or decrement (depending on the DMA function being performed) before the character previously read is written back into memory. This provides a new address for the character to be written into memory and is one character to the left, right, up, or down from its original position.

Register Indicators originate as outputs from the Registers on the Cursor Card, and they perform a dual function
on the Edit Card. Not only do they tell the Edit Card when the function is complete, but they also control how the Registers are manipulated by the Register Control Signals to perform the Edit function.

The process of reading data from the RAM into the Edit Card before it is displayed is necessary to perform the edit functions. Normally, data in memory is "refreshed" by refresh circuitry on the RAM card at a rate that ensures memory is sustained. However, during Direct Memory Access (DMA), the normal refresh cycle is suspended. Instead, data is read from and written back into memory at a rate (determined by DMA timing) that ensures that memory is sustained. DMA operation occurs during edit, roll-up, clear page, and erase input functions.

## EDIT CIRCUITS

The Edit circuits are DEL/INS and DMA Latches, Edit Control for Registers, Edit Data Latches, and the Edit Function Complete circuit. They will be discussed in that order.

DEL/INS AND DMA LATCHES. Initiating an Edit function causes $\overline{B O U N C E}$ to go active. $\overline{\text { BOUNCE }}$ enters the Keyboard Interface Card which generates KEYGATE. KEYGATE clocks data into U229, the DEL/INS Latch, at STEP time. When XEQUAL and YEQUAL become true,


Fig. 6-12. Relation between Edit, Cursor, and RAM cards.
the output of U229 is clocked into DMA Latch U129, which is clocked by the high-going output of U241A. (The input to U241A that goes high to enable the high-going output, depends on the edit function being performed.) $\overline{\mathrm{DMA}}$ becomes true, and the Register Control Signals ( $\overline{U P}$, $\overline{\mathrm{DOWN}}, \overline{\mathrm{LEFT}}, \overline{\mathrm{RIGHT}}, \overline{\mathrm{CLRX}}, \overline{\mathrm{CLRY}}$, and $\overline{\mathrm{HIY}}$ ) are set in a combination that performs the commanded Edit function. More detailed information on how these outputs affect the Cursor and Display Registers can be found under "Edit Functions" in the Cursor Card Description.

EDIT DATA LATCHES (TWO CHARACTER DELAY). During Edit operations, two sets of data latches provide a means whereby data can be read from memory, stored in the latches, then re-written back into memory. The data is either deleted, or it is written back into memory one character space to the left, right, up, or down from the position it originally occupied in memory. This function is provided by D Latch 1 and D Latch 2.

DMA goes active for the duration of the Edit function, and causes the Edit Data Latches to be cleared. $\overline{\text { STEP }}$ also changes from a repetition rate of 636 ns to $1.9 \mu \mathrm{~s}$. The $1.9 \mu \mathrm{~s}$ allows time for the following to occur:

1. The cursor address changes.
2. A character is read at that address and latched into D Latch 1.
3. A character is sent from $D$ Latch 2 and read back into a different position in memory.

The next $\overline{\text { STEP }}$ signal addresses a new character to be read from memory and the cycle repeats until the Edit function is completed.

EDIT FUNCTION COMPLETE CIRCUIT. When the high level that clocks U129 ends, the Q output of U29A (Latch Clear and Pulser Flip/Flop) goes high. This high output is clocked into U29B on the trailing edge of STEP. The low $\overline{\mathrm{Q}}$ output then clears the INS/DEL Latch. The DMA Latch is cleared when the Edit function is completed, as indicated by the Register Indicator Signals, EOLDIS, LSTYDIS, XEQUAL, and YEQUAL.

## ROLL-UP CIRCUITRY

GENERAL. Roll-up occurs in Direct mode when attempting to line feed past the 24th line (or 12th line if strapped for 12 line operation). Note that roll-up can be
disabled by cutting the NO ROLL-UP strap, then strapping to ground. The roll-up sequence is to jam the cursor to the top of the screen, perform a Delete Line function, then jam the cursor back to the bottom line. Roll-up is controlled by the Roll-up Set circuit, Roll-up Complete Circuit, and the LSTY CRS Circuit.

ROLL-UP SET. The Roll-up circuitry is "armed" by the DIRECT signal. When LSTY CRS goes active, and DOWN is active, the next $\overline{\mathrm{EXECUTE}}$ time enables $\overline{\mathrm{STEP}}$ to clock a low from U239B through U499A. This enables $\overline{\text { CLRY }}$ from U439B and also triggers a Delete Line function, moving all lines on the display up one line.

ROLL-UP COMPLETE CIRCUIT. When the output of U499 returns high, a low-going signal from U431C clocks U1A in the Roll-up Complete circuit. A high is clocked to the Q output. High levels are now placed on two inputs of U109B. After the Delete Line function is completed, a low pulse from U131A is inverted by U431E to enable a low output from U109B. The Jam Count Flip/Flop, U9B, becomes zero-set, enabling the outputs from the Jam Count Set circuit. This jams the Y Cursor Register back to the bottom line.

LSTY CRS CIRCUIT. This circuit goes into operation at the end of the roll-up function. It inserts a bit content that is latched into the Y Cursor Register by HIY. The 12-Line Roll strap is cut when only 12 lines are used.

ROLL-UP 4 ONLY. When strapped for 4 -line roll-up DIRECT also arms U301C. When the low output from U499 ends, the high-going signal from U431A enables a low from U301C, which clocks the $\div 4$ counter. The fourth roll-up to occur enables a high level from pin 11 of U201 to inhibit further roll-ups. This circuit is reset by clearing the page or by pressing the RESET button.

## READ CURSOR POSITION

This function is performed by the Read Cursor Position circuit. When ESC followed by ] (closing bracket-93 ${ }_{10}$ ) is decoded, a SEND CURSOR ADDRESS signal from U379A triggers the Read Cursor circuitry. The Q output of U169A goes high to enable the GS character bit configuration to be transmitted at the next $\overline{\text { STORE }}$ and STROBE times. STORE enables the GS character; STROBE enables $\overline{\text { CSTROBE. }}$. (See Timing illustration in Fig. 6-4, Part B.) When $\overline{\text { CBUSY }}$ ends and the next $\overline{\text { READ time occurs, }}$ STROBE enables $\overline{C S T R O B E}$ and also clocks the high Q output from U169A to U149B. The high from U149B subsequently enables $\overline{\text { HIX }}$, causing the $X$ Cursor Register
contents to be placed on the minibus and transmitted. Again, when $\overline{\text { CBUSY }}$ ends, STROBE at $\overline{\text { READ }}$ time enables $\overline{\text { HIY }}$, causing the Y Cursor Register contents to be transmitted.

## CURSOR POSITIONING

Sending FS causes the next two characters received by the Terminal to be interpreted as Position Cursor information. When the FS Control Character is decoded by the Decoding Circuit, a low output from the FS Decoder, U379A, enables the Position Cursor circuit. The output of U71B is set to a high level and the next character received by the Terminal sets $\overline{T S T R O B E}$, which subsequently enables $\overline{\text { HIX }}$ from U471D. $\overline{\text { HIX loads the character on the }}$ minibus into the $X$ Cursor Register, whose output changes to reflect the new $X$ Cursor location. The following character sets $\overline{\mathrm{HI}}$ active to strobe the Y address into the Y Cursor Register. The cursor position now reflects the new position.

## CHARACTER DECODING CIRCUIT

This circuit provides decoding for the characters that control Cursor Positioning, Cursor Addressing, Rulings Set, FAC Set, Tab, and Backtab functions. This circuit is divided into three basic operating functions, the 3 MSB (Most Significant Bit) Decoder, the 4 LSB (Least Significant Bit) Decoder, and the Character Detect Gates.

The ESC ] Gate, U279C, is only enabled when ESC precedes the ] character. ( $\overline{\mathrm{LCE}}$ goes active from the Control Card when the ESC character is detected on the minibus.) The remainder of the circuitry provides decoding for the following Control Characters:

## TABLE 6-6

## CONTROL CHARACTER FUNCTIONS

CONTROL CHARACTER

## FUNCTION

FS Sets Position Cursor Operation
HT Initiates Tab Function
VT Initiates Backtab Function
SI Sets $\overline{\text { BIT } 9}$ active to identify $\overline{\text { BITS 1-7 }}$ as a ruling character. With BIT9 active, a ruling character is displayed instead of the normal ASCII character identified by the bit configuration.
SO Deactivates BIT 9
US $\quad$ Sets $\overline{\text { BIT } 8}$ active to identify $\overline{\overline{B I T S}} 1-7$ as a Field Attribute Code.

## BIT 8 AND BIT 9 SET

This circuit performs the functions as described under the SI, SO, and US Control Character descriptions above.

## TAB/BACKTAB CIRCUITS

GENERAL. The Tab circuitry is located at the bottom of the schematic. The main purpose of this circuitry is to provide tabbing for the cursor from one unprotected field to the next in a form Fill-Out operation. Forward-tabbing or backtabbing is provided. These circuits provide no useful function when the DIRECT/BUFFER switch is at DIRECT. Forward tabbing in Direct causes the cursor to space once, then stop; backtabbing in Direct is prohibited.

TABBING. Sending the HT Control Character is one way of initiating the Tabbing function. When in Buffer, and HT is decoded, a low $\overline{T A B}$ signal from U379C one-sets U41B, setting the Q output high. The Terminal goes buys during the Tab function (TBUSY is active). Also, the cursor is blanked by HCUBUSY while the registers are being manipulated. The $\overline{\mathrm{RIGHT}}$ signal goes active to increment the $X$ Cursor Register one count each EXECUTE time. When the Register addresses a character from the RAM that is a FAC, the Protected/Unprotected circuitry checks to see if it is protected or not. If protected, the $X$ Register continues to increment until either an unprotected field or the end of the line is reached. If the end of the line is reached before a FAC is detected, $\overline{C L R X}$ goes active to clear the $X$ Register; $\overline{D O W N}$ increments the $Y$ Register one count; $\overline{\text { RIGHT remains active and the } X \text { Register counts up }}$ once again. The cycle repeats until an unprotected FAC is detected, the $X$ Register increments one more count, then stops. $\overline{T B U S Y}$ and $\overline{H C U B U S Y}$ end, and the cursor is displayed one character past the FAC that defines the unprotected field.

BACKTABBING. When the Terminal receives the VT Control Character, backtabbing occurs. As with Tab, backtabbing is used when Field Attribute Codes reside in memory. However, backtabbing positions the cursor back to the first character position in the preceding unprotected field. The FAC that defines the field that the cursor may reside in is ignored, whether the field is protected or unprotected.

Basically, the backtabbing function operates in reverse of the forward tabbing function. The cursor is blanked by $\overline{\text { HCUBUSY }}$ and $\overline{\text { TBUSY }}$ goes active. Register Control outputs are set to move the cursor to the left and up until an unprotected field is detected. At this time, cursor movement stops. The X Cursor Register is then incre-
mented one count to move the cursor one space to the right of the FAC.

## DISPLAY CIRCUITS

## GENERAL

Refer to the Monitor schematic. The Monitor consists of the following circuits: Vertical, Horizontal, Power Supply, Video, Brightness, and Focus. They will be discussed in that order. Waveforms associated with the circuit are shown in Fig. 6-13.

## VERTICAL

The Vertical circuit provides a raster for the display. The ramp is generated by C105, C106, Q102, R115, and R116. C105 and C106 repeatedly charge up to a point that causes Q102 to conduct. C105 and C106 then discharge through R120 and Q102. Q102 ceases to conduct. The ramp developed by C105 and C106 is applied to the base of Q103. This ramp is felt at the emitter of Q103, where part
of it is picked off by R124 and applied to Q104 to control the current through vertical yoke coils L1 and L2. A vertical drive signal (with a frequency slightly higher than the free-running frequency of C105-C106-Q102) is applied through R113 and C104. As the voltage at the anode of Q102 increases due to the C105-C106 charge, a negativegoing V DRIVE pulse is applied to the gate of Q102 to cause Q102 to go into conduction. Therefore, the frequency of the circuit is slaved to the negative pulse received on the V DRIVE line.

R116 controls the free-running frequency of the circuit by controlling the charge rate of C105-C106, and is adjusted as necessary to permit the V DRIVE signal to control the circuit frequency. Feedback that controls linearity is adjustable by R121. Height can be controlled by R124.

## HORIZONTAL

To obtain a signal appropriate for driving horizontal output transistor Q106, a driver stage consisting of Q105


Fig. 6-13. Display waveforms.

## Theory of Operation-4023 Service

and T101 is used. A positive-going pulse is coupled through R127 to the base of Q105. The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive at the base of Q106, keeping it cut off. As soon as the primary current of T101 is interrupted (due to the base signal driving Q105 into cut off), the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

Q106 acts as a switch that is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage, plus the charge on C113, causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base, which causes the output circuit to oscillate. A high reactive voltage in the form of a half-cycle, negative voltage pulse is developed by the yoke inductance and the primary of T2. The peak magnetic energy that was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, serves to block dc currents through the yoke and to provide " S " shaping of the current
waveform. " S " shaping compensates for stretching at the left and right sides of the picture tube. (Stretching would otherwise occur because the curvature of the crt face and the deflected beam do not describe the same arc.)

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore varies the width of the horizontal scan.

POWER SUPPLY. The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately -160 Vdc , which is coupled through the brightness control to the coaxial grid of the crt (V1).

This same negative flyback pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately +12 kV , +400 V and +34 V , respectively. 12 kV is the anode voltage for the crt; +400 Vdc serves as the source voltage for grids No. 2 and 4 (focus grid) of the crt. The +34 Vdc potential is the supply voltage for the video output amplifier, Q101.

## VIDEO

This circuit consists of a single stage amplifier (Q101) with a gain of about 17 . The wiper of the CONTRAST control picks off a portion of the incoming video signal and applies it through R109 to the base of Q101. The resulting signal from the collector of Q101 is then applied to the cathode of the crt.

## BRIGHTNESS

This passive circuit uses voltage-divider action to determine the control grid voltage, establishing cathode-to-grid bias. (Both the cathode and control grid are referenced to +34 V.) An arc suppression circuit prevents excessive voltage difference from developing between the control grid and other tube elements.

## FOCUS

This is also a passive circuit, using voltage divider action, adjustable control, and arc suppression in a manner similar to the Brightness circuit. Since the circuit is dependent upon crt cathode current for the actual voltage being impressed on the crt elements, the FOCUS setting is highly
dependent upon the BRIGHTNESS and CONTRAST settings.

TABLE 6-7
TROUBLESHOOTING GUIDE

| SYMPTOM | POSSIBLE REMEDY |
| :--- | :--- |
| 1. Screen is dark | Check "A" bus Q106, Q105, CR2 |
| 2. Loss of video | CR105, Q101 |
| 3. Power con- <br> sumption is <br> too high | Check horizontal drive waveform; <br> Check proper placement of horizontal <br> linearity sleeve; Check Q105, Q106 |

## POWER SUPPLY

Refer to the Power Supply schematic. Component locations are provided on the apron of the schematic. The power supply has regulated outputs of $+15,+5,-12$, and -5 volts. All of these supplies obtain their power from conventional, fullwave bridge rectifiers. The -12 and -5 volt supplies are connected in series aiding, with the current source for the -5 volt supply being the -12 volt supply.

All supplies are referenced to the adjustable +15 volt supply, and all supplies use remote sensing. Each supply contains "safety resistors" for supply protection in the event the supply load is disconnected. These resistors and the supply protected are:

| R24 | +15 Volts |
| :--- | :--- |
| R201 | +5 Volts |
| R44 | -12 Volts |
| R10 | -5 Volts |
| R20 | Ground |
| R21 |  |

## +15-VOLT SUPPLY

The +15 Volt supply uses an integrated-circuit regulator. Reference voltage is provided at the top of R256 and is input on pin 6 of U123. Supply adjustment is provided by R258, with the wiper also supplying the reference input for the +5 -Volt supply. 0241 provides drive, while 01105 is the Series-Pass transistor. R207 and R208 are the currentlimiting resistors.

## -12 AND -5 VOLT SUPPLIES

Regulation for these supplies is provided by U55 (-12) and U52 ( -5 ). Reference voltage is supplied by the +15 Volt supply. -12 Volt sensing is applied to pin 3 of U55. Regulation occurs as follows: when the -12 sense line becomes more negative, the potential on pin 6 of U55 also lowers. The base of U357 subsequently becomes more negative, causing its emitter potential to lower. This in turn limits the drive voltage to the Series-Pass Transistor, Q1118, causing current flow through it to decrease. This decreases (makes more positive) the -12 Volt Supply. The opposite occurs when the -12 Volt Sense line goes more positive.

Current limiting for both the -12 and -5 Volt supplies is provided by $055, \mathrm{R} 58$, and R356. When the current through R58 and R356 increases to a point where 0.6 volts is felt at the base of Q55, Q55 turns on. This turns off the drive from Q357, shutting down the supply.

The -5 Volt supply has the sensing voltage applied to the negative input of U52. When the -5 Volt Sense line goes more negative, pin 6 of U252 becomes more positive. This decreases the bias on 053 , bringing the output back to -5 Volts.

## +5 VOLT SUPPLY

The reference voltage for this supply is obtained from the wiper of R258 in the +15 Volt supply. R203 and C209 bring the +5 Volt supply up slowly when power is turned on. Regulation occurs as follows: when the +5 Volt Sensing line becomes more positive, the output of U205 also becomes more positive. This decreases the bias to Q109, which in turn causes the drive from 01110 to decrease. This decreases the current through Q1112, which lowers the +5 Volt supply. A lowering of the voltage on the +5 Volt Sensing line has an opposite effect on the regulator circuitry.

CURRENT LIMITING. Foldback current limiting is provided by Q29, Q38, and associated circuitry. Resistors R40-R43 provide the foldback (decrease) in current as the voltage decreases. Operation is as follows: when the voltage drops to a level that is sufficient to bias Q38 off, O29 turns on. R47 sets the point at which current limiting occurs. The decrease in collector voltage of Q29 biases Q110 into conduction. This limits the drive to Q1112, shutting down the supply.

OVER-VOLTAGE PROTECTION. Over-voltage protection is provided by a "crow-bar" circuit consisting of Q1114, VR306, and Q305. VR306 provides a 5.6 -volt reference to the base of $\mathbf{Q 3 0 5}$. Should the voltage on the emitter increase to 6.2 volts, Q 305 is biased into conduction. When the voltage at the gate of Q1114 increases to approximately 1.2 volts, Q1114 conducts and immediately lowers the +5 volt line to approximately 1 volt. The associated surge of current causes F1007 to open up, removing power from the circuit.

## WIRING AND SIGNAL INFORMATION WIRING

The following interconnecting references are provided to facilitate signal tracing:

Wire List-Provides a listing of signal path by cable number.

Wiring and Block Diagrams (Fig. 6-14 and 6-15)-Shows location and identity of connectors.

Motherboard Diagrams (Fig. 6-17 and 6-18)-Shows connector locations and lists interconnecting lines.

From/To Addresses (contained on the schematics)-Lists source or destination of subject signal. Signals that do not contain a To/From address will have a specific minibus pin number. The signal on that pin number is applicable to the same pins on all cards that can be inserted into the minibus connectors, J1-J9.

Minibus Signal Listing and Descriptions-An alphabetic signal listing of all signals common to the minibus that describes the signal function, also showing the card(s) from which it originates and the card(s) that uses (use) the signal. This information can be found immediately following the wiring information.

## HOW TO USE THE WIRING INFORMATION

In the event of cable trouble, it may be necessary to trace signals from point-to-point through all connectors. Start with the connector and pin number. If it is a harmonica connector, go to that connector in the Wire List. If it is a card-edge connector (minibus signal) go to that connector on the Motherboard diagram. Opposite the connector and pin number is listed the interconnecting point or points.

Example 1. Follow HIY to its destination. Since $\overline{\mathrm{HIY}}$ is a card that inserts into the minibus, its connector is common to pin J on all cards connected to the minibus. To determine if the signal goes elsewhere, look on the Motherboard diagram under minibus pin J. No other points are listed. For more information on $\overline{H I Y}$ refer to the Minibus Signal Listing.

Example 2. Follow MAKE COPY. Again, it is a connection on the minibus. Go to the Minibus Signal Listing and there you'll find that the Control Card and the Keyboard Interface Card generate this signal. Go to the Keyboard Interface schematic and find this signal. Note that the MAKE COPY command from the Keyboard Interface is a result of KMAKE COPY from J45 pin 4. Go to the Wire List and look up J45 pin 4. There you'll determine that $\overline{K M A K E ~ C O P Y}$ is an output from the Keyboard plug, J111. Next look for the MAKE COPY signal on the Control Card. Note that here it is an output of a programmed make copy request. Refer back to the $\overline{M A K E ~ C O P Y}$ signal description and you'll notice that the Timing Card uses this signal. Refer to the Timing Card schematic and find MAKE COPY. Note that it outputs on J 78 pin 7 which connects to J190 pin 13. J190 can be identified by referring to the Connectors and Wiring Diagram. There it is determined that J 190 is the Hard Copy Connector on the back panel of the Terminal.

## WIRE LISTS

The following wire lists provide a listing of wiring between separate assemblies. Each plug or jack is listed by individual pin numbers that show the destination or origination of the signals. The listing is in numeric order beginning with J45, J47, and J48 on the Keyboard Interface.

WIRE LIST FOR
KEYBOARD INTERFACE
J45, J47, \& J48

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire <br> Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly |  |
| Jack | Pin |  |  |  |  |  |
| J45 | 1 | KERASE INPUT | $J 111$ | 4 |  |  | $9-0$ |
|  | 2 | KRESET | J111 | 2 |  |  | 9-13 |
|  | 3 | KCLEAR | J111 | E |  |  | 9-6 |
|  | 4 | KMAKE COPY | J111 | L |  |  | 9-34 |
|  | 5 | $\overline{\mathrm{KUP}}$ | J111 | M |  |  | 9-8 |
|  | 6 | $\overline{\text { KRIGHT }}$ | J111 | C |  |  | 9-4 |
|  | 7 | KHOME | J111 | D |  |  | 9-3 |
|  | 8 | KLEFT | J111 | 14 |  |  | 9-2 |
|  | 9 | KBREAK | J111 | A |  |  | 9-7 |
|  | 10 | KDOWN | $J 111$ | B |  |  | 9.5 |
| J47 | 1 | KSTROBE | J111 | 5 |  |  | 9-02 |
|  | 2 | NO WIRE | Tied high on Motherboard |  |  |  |  |
|  | 3 | KBIT 7 | J111 | N |  |  | 9-05 |
|  | 4 | KBIT 5 | J111 | P |  |  | 9-07 |
|  | 5 | KBIT 6 | J111 | R |  |  | 9-04 |
|  | 6 | KBIT 1 | J111 | F |  |  | 9-12 |
|  | 7 | KBIT 2 | J111 | J |  |  | 9-03 |
|  | 8 | KBIT 4 | J111 | H |  |  | 9-08 |
|  | 9 | KBIT 3 | J111 | K |  |  | 9.06 |
| J48 | 1 | $+5 \mathrm{Vdc}$ | To Speaker |  |  |  | 2-0 |
|  | 2 | BELL | To Speaker |  |  |  | 9-25 |

WIRE LIST FOR
EDIT
J52

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assemby |  |
| Jack | Pin |  |  |  |  |  |
| J52 | 1 | KDEL LINE | J111 | W |  |  | 9-16 |
|  | 2 | KINS CHAR | J111 | Y |  |  | 9-14 |
|  | 3 | $\overline{\text { KDEL CHAR }}$ | J111 | Z |  |  | 9-15 |
|  | 4 | $\overline{\text { KINS LINE }}$ | J111 | X |  |  | 9.17 |

WIRE LIST FOR
CONTROL BOARD
J60

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly |  |
| Jack | Pin |  |  |  |  |  |
| J60 | 1 | KERASE TO END | $J 111$ | 3 |  |  | 9-18 |
|  | 2 | $\overline{\text { KENTER }}$ | J111 | U |  |  | 9-23 |
|  | 3 | $\overline{\text { KSEND }}$ | J111 | 1 |  |  | 9-1 |

WIRE LIST FOR
TIMING CARD
J76, J78, \& J79

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly |  |
| Jack | Pin |  |  |  |  |  |
| J76 | 1 | COMPOSITE VIDEO | J191 | . Center | Conductor |  | 9-1 |
|  | 2 | COMP VIDEO GND |  |  |  |  | 9-2 |
| J78 | 1 | VIDEO CLOCK GND | J190 | 1 |  |  | 9-1 |
|  | 2 | VIDEO CLOCK | J190 | 2 |  |  | 9-2 |
|  | 3 | V DRIVE GND | J190 | 9 |  |  | 9-3 |
|  | 4 | H DRIVE GND | J190 | 3 |  |  | 9-4 |
|  | 5 | HCU COMP VIDEO | $J 190$ | 11 |  |  | 9-5 |
|  | 6 | HCU COMP VIDEO GND | J190 | 12 |  |  | 9-6 |
|  | 7 | MAKE COPY | J190 | 13 |  |  | 9-7 |
|  | 8 | MAKE COPY GND | J190 | 14 |  |  | 9-8 |
|  | 9 | HCU BUSY | $J 190$ | 7 |  |  | 9-N |
|  | 10 | HCU BUSY GND | J190 | 8 |  |  | 9-0 |
| J79 | 1 | VERTICAL DRIVE | $J 112$ | 9 |  |  | 9.1 |
|  | 2 | VERTICAL DR. GND | J112 | 10 |  |  | (shield) 9-1 |
|  | 3 | INTERNAL VIDEO | To Contrast Pot. |  |  |  | 9-2 |
|  | 4 | INTERN. VID. GND | To Contrast Pot. |  |  |  | (shield) 9-2 |
|  | 5 | MONITOR H DRIVE | J112 | 6 |  |  | 9-3 |
|  | 6 | VERT. DR. GND | J112 | 1 |  |  | (shield) 9-3 |

WIRE LIST FOR
KEYBOARD
J111

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire <br> Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly |  |
| Jack | Pin |  |  |  |  |  |
| J111 | 1 | KSEND | J60 | 3 |  |  | 9-1 |
|  | 2 | KRESET | J45 | 2 |  |  | 9-13 |
|  | 3 | KERASE TO END | J60 | 1 |  |  | 9-18 |
|  | E | $\overline{\text { KCLEAR }}$ | J45 | 3 |  |  | 9-6 |
|  | 5 | KSTROBE | J47 | 1 |  |  | 9-02 |
|  | 8 | $\overline{\text { KNUM LOCK }}$ | NO |  |  |  |  |
|  | 14 | KLEFT | J45 | 8 |  |  | 9-2 |
|  | 15 | GROUND | J205 | 1 | (Strapped | Pin S also) | O-N |
|  | 16 | +5 V | J205 | 2 | (Strappe | Pin T also) | 2-0 |
|  | 17 | -12 V | J205 | 4 |  |  | 7-1 |
|  | A | KBREAK | J45 | 9 |  |  | 9-7 |
|  | B | KDOWN | J45 | 10 |  |  | 9.5 |
|  | C | $\overline{\text { KRIGHT }}$ | J45 | 6 |  |  | 9-4 |
|  | D | KHOME | J45 | 7 |  |  | 9-3 |
|  | 4 | KERASE INPUT | J45 | 1 |  |  | 9-0 |
|  | F | KBIT 1 | J47 | 6 |  |  | 9-12 |
|  | H | KBIT 4 | J47 | 8 |  |  | 9-08 |
|  | J | KBIT 2 | J47 | 7 |  |  | 9-03 |
|  | K | KBIT 3 | J47 | 9 |  |  | 9.06 |
|  | L | $\overline{K M A K E ~ C O P Y ~}$ | J45 | 4 |  |  | 9.34 |
|  | M | KUP | J45 | 5 |  |  | 9-8 |
|  | N | KBIT 7 | J47 | 3 |  |  | 9-05 |
|  | P | KBIT 5 | J47 | 4 |  |  | 9-07 |
|  | R | KBIT 6 | J47 | 5 |  |  | 9-04 |
|  | S | GROUND | J205 | (Strapped to Pin 15 also) |  |  |  |
|  | T | $+5 \mathrm{Vdc}$ | J205 | 2 | (Strapped to Pin 16 also) |  |  |
|  | U | KENTER | J60 | 2 |  |  | 9-23 |
|  | V | KBIT 8 | NO WIRE (pulled high on Motherboard) |  |  |  |  |
|  | W | KDEL LINE | J52 | 1 |  |  | 9-16 |
|  | X | KINS LINE | J52 | 4 |  |  | 9-17 |
|  | Y | KINS CHAR | J52 | 2 |  |  | 9-14 |
|  | Z | KDEL CHAR | J52 | 3 |  |  | 9-15 |


| WIRE LIST FOR HIGH VOLTAGE BOARD $J 112$ |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  | Wire Color Code |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly |  |
| Jack | Pin |  |  |  |  |  |
| J112 | 1 | MONITOR H DRIVE GND | J79 | 6 |  |  | (shield) 9-3 |
|  | 2 | +34 V | Brightness Pot |  |  |  | 8-03 |
|  | 3 | -160 V | Brightness Pot |  |  |  | 8.02 |
|  | 4 | BRIGHTNESS VOLT | Brightness Pot Wiper |  |  |  | 8-04 |
|  | 5 | GROUND | J210 | 2 |  |  | $0 \cdot \mathrm{~N}$ |
|  | 6 | MONITOR H DRIVE | J79 | 5 |  |  | 9-3 |
|  | 7 | +15 V | J210 | 1 |  |  | 2-1 |
|  | 8 | CONTRAST VOLTAGE | Contrast Pot Wiper |  |  |  | 9-05 |
|  | 9 | VERTICAL DRIVE | J79 | 1 |  |  | 9-1 |
|  | 10 | VERT DRIVE GND | J79 | 2 |  |  | (shield) 9-1 |

## WIRE LIST FOR

LV POWER SUPPLY J150, J151, J152, J153, J154


WIRE LIST FOR
HIGH VOLTAGE BOARD
J155 and J156


WIRE LIST FOR
CHASSIS WIRING
J190, J191, and DISPLAY CONTROLS

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly | Wire Color Code |
| Jack | Pin |  |  |  |  |  |
| J190 | 1 | VIDEO CLOCK GND | J78 | 1 |  |  | 9-1 |
|  | 2 | VIDEO CLOCK | J78 | 2 |  |  | 9-2 |
|  | 3 | H DRIVE GND | $J 78$ | 4 |  |  | 9-4 |
|  | 7 | HCU BUSY | J78 | 9 |  |  | 9-N |
|  | 8 | HCU BUSY GND | J78 | 10 |  |  | 9-0 |
|  | 9 | V DRIVE GND | J78 | 3 |  |  | 9-3 |
|  | 11 | HCU COMP VIDEO | J78 | 5 |  |  | 9-5 |
|  | 12 | HCU COMP VID GND | J78 | 6 |  |  | 9-6 |
|  | 13 | MAKE COPY | J78 | 7 |  |  | 9-7 |
|  | 14 | MAKE COPY GND | J78 | 8 |  |  | 9-8 |
| J191 | 1 | COMPOSITE VIDEO | J76 | 1 |  |  | 9-1 |
|  | 2 | COMP VID GND | J76 | 2 |  |  | 9-2 |
| ON/OFF <br> Switch | 1 | See LV Power Supply Schematic for distribution |  |  |  |  | 8-01 |
|  | 2 |  |  |  |  |  | 9-18 |
|  | 5 |  |  |  |  |  | 9-8 |
|  | 6 |  |  |  |  |  | 8-02 |
| BRIGHTNESS |  |  |  |  |  |  |  |
|  |  | +34 V | J112 | B |  |  | 8-03 |
|  |  | -160 V | J112 | C |  |  | 8-02 |
|  |  | BRIGHTNESS VOLTAGE | J112 | D |  |  | 8-04 |
| CON- <br> TRAST |  | INTERNAL VIDEO | J79 | 3 |  |  | 9-2 |
|  |  | INTERN VID GND | J79 | 4 |  |  | $\begin{gathered} \hline \text { (shield) } \\ 9-2 \end{gathered}$ |
|  |  | CONTRAST VOLTAGE | J112 | J |  |  | 9-05 |
| SPEAKER |  | $+5 \mathrm{Vdc}$ <br> BELL | $\begin{aligned} & \text { J48 } \\ & \text { J48 } \end{aligned}$ | 1 2 |  |  | $\begin{aligned} & 2-0 \\ & 9-25 \end{aligned}$ |

WIRE LIST FOR
MOTHERBOARD
J200, J201, J202, J203, J204

| Assembly <br> Connectors |  | Signal <br> Name | To or From |  |  | Originating Assembly | Wire Color Code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus |  |  |
| Jack | Pin |  |  |  |  |  |
| J200 | 1 | GND | J155 | 1 |  |  | O-N |
|  | 2 | GND | J155 | 2 |  |  | O-N |
|  | 3 | GND | J155 | 3 |  |  | O-N |
|  | 4 | GND | J155 | 4 |  |  | O-N |
|  | '5 | GND | J155 | 5 |  |  | 0-N |
| J201 | 1 | +15 V SENSE | J152 | 1 |  |  | 2-1 |
|  | 2 | +15 V | J152 | 2 |  |  | 2-1 |
|  | 3 | +15 V | J152 | 3 |  |  | 2-1 |
|  | 4 | +15 V | J152 | 4 |  |  | 2-1 |
| J202 | 1 | +5 V SENSE | J153 | 1 |  |  | 2.0 |
|  | 2 | +5 V | J153 | 2 |  |  | 2.0 |
|  | 3 | +5V | J153 | 3 |  |  | 2.0 |
|  | 4 | +5V | J153 | 4 |  |  | 2-0 |
|  | 5 | +5V | J153 | 5 |  |  | 2-0 |
| J203 | 1 | -12 V SENSE | J150 | 1 |  |  | 7-1 |
|  | 2 | -12 V | J150 | 2 |  |  | 7-1 |
|  | 3 | -12 V | J150 | 3 |  |  | 7.1 |
|  | 4 | -12 V | J150 | 4 |  |  | 7-1 |
|  | 5 | -12 V | J150 | 5 |  |  | 7-1 |
| J204 | 1 | -5 V SENSE | J154 | 1 |  |  | 7-0 |
|  | 2 | -5V | J154 | 2 |  |  | 7-0 |
|  | 3 | $-5 \mathrm{~V}$ | J154 | 3 |  |  | 7-0 |

WIRE LIST FOR
MOTHERBOARD
J205, J207, J208, J210, J213

| Assembly Connectors |  | Signal <br> Name | To or From |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Plug and/ or Jack | Pin | Minibus | Originating Assembly | WireColor Code |
| Jack | Pin |  |  |  |  |  |
| J205 | 1 | GND | J111 | 15 |  |  | O-N |
|  | 2 | +5 V | J111 | 16 |  |  | 2-0 |
|  | 3 | +15 V |  |  |  |  | No Wire |
|  | 4 | -12 V | J111 | 17 |  |  | 7-1 |
|  | 5 | -5 V |  |  |  |  | No Wire |
| J207 | 1 | +5V | To F-P switches and LEDS |  |  |  | 2-0 |
|  | 2 | KEYBOARD LOCK | KEYBOARD LOCK INDICATOR |  |  |  | 9-7 |
|  | 3 | WAIT LED | J207 | 3 |  |  | 9-8 |
|  | 4 | LED \#1 | (SPARE LED) |  |  |  | 9-0-3 |
| J208 | 1 | GND |  |  |  |  | $0-\mathrm{N}$ |
|  | 2 | LOCAL/LINE SW. |  |  |  |  | 9-6 |
|  | 3 | DIRECT/BUFFER SWITCH |  |  |  |  | 9-3 |
|  | 4 | SW \#2 | (SPARE SWITCH) |  |  |  | 9-2 |
|  | 5 | SW \#1 | (SPARE SWITCH) |  |  |  | 9-5 |
| J210 | 1 | +15 V | J112 | H |  |  | 2-1 |
|  | 2 | GND | J112 | E |  |  | O-N |
| J213 | 1 | +15 V |  |  |  |  | No Wire |
|  | 2 | +5 V |  |  |  |  | No Wire |
|  | 3 | GND |  |  |  |  | No Wire |
|  | 4 | -12 V |  |  |  |  | No Wire |

## Theory of Operation-4023 Service

## MINIBUS SIGNAL LISTING AND DESCRIP- RAM C-RAM Card TIONS <br> The following table lists in alphabetic order all signals common to the minibus. The table provides the following information about each signal. <br> CURS C-Cursor Card <br> TIM C-Timing Card

1. The minibus connector.
2. The card or cards that originate the signal.
3. The card or cards that use the signal.
4. A description of the function performed by the signal.

The following acronyms are used in the table to identify the circuit cards:

KBI C-Keyboard Interface Card

CONT C-Control Card
ED C-Edit Card
INTF C-Interface Card

## NOTE

Signals are designated low true by placing a horizontal bar over them. Reading the signals can be enhanced by reading them as in the following example:

The signal designated $\overline{B R E A K}$ can be read "break not."

TABLE 6-8
SIGNAL DEFINITIONS

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| AUXSENSE | 20 |  |  | Status bit line that is reserved for auxiliary devices. The $\overline{H C U}$ BUSY signal may also be used by auxiliary devices if no Hard Copy Unit is connected with its power on. |
| $\begin{aligned} & \overline{\text { BIT } 1} \\ & \overline{\text { BIT } 2} \\ & \overline{\text { BIT } 3} \\ & \overline{\text { BIT } 4} \\ & \overline{\text { BIT } 5} \\ & \overline{\text { BIT } 6} \\ & \overline{\text { BIT } 7} \end{aligned}$ | $\left.\begin{array}{l} 10 \\ T \\ 11 \\ 12 \\ U \\ F \\ 6 \end{array}\right]-$ | KBI C <br> RAM C <br> CURS C <br> ED C <br> CONT C <br> INT C | CONT C CURS C <br> TC INT C | Data to and from the Terminal, peripherals, and the Computer. |
| BIT 8 | 26 | RAM C <br> ED C <br> INT C | ED C <br> CONT C <br> T C <br> INTF C | When true, $\overline{\text { BIT } 1-\overline{B I T ~} 7}$ are designated as a Field Attribute Code. $\overline{\text { BIT } 8}$ is not transmittable. |
| $\overline{\text { BIT } 9}$ | 30 | $\begin{aligned} & \text { KBI C } \\ & \text { ED C } \end{aligned}$ | ED C <br> CONT C <br> TC | When true, $\overline{\text { BIT } 1-\overline{\text { BIT }} 7 \text { are designated as an }}$ alternate ROM character such as a ruling character. $\overline{\text { BIT } 9}$ is not transmittable. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| BOUNCE | 9 | ED C <br> CONT B | KBI C | $\overline{\text { BOUNCE }}$ is produced by ERASE TO END, SEND, ENTER, INS CHAR, DEL CHAR, INS LINE, and DEL LINE. $\overline{\text { KEYGATE }}$ is produced as a response to $\overline{B O U N C E}$. |
| $\overline{\text { BREAK }}$ | L | KBI C | INTF C | Set active from the Keyboard Interface Card as a result of pressing the BREAK key. Can also go active as a result of a Break on page full. This signal is used to signal the computer. NOTE: In some interfaces, $\overline{B R E A K}$ may be pulled up to +15 Vdc Data signals may also be present on BREAK. |
| $\overline{\text { CBUSY }}$ | 1 | CONT C | ED C <br> INTF C | Means the computer interface cannot accept a character. Controls the timing of data transmitted to the computer. |
| $\overline{\text { CLRX }}$ | 35 | KBI C <br> ED C <br> CONT C <br> T C | KBI C <br> CURS C <br> CONT C | Used to clear to zero either the X Cursor or X Display Register. Can go active independent of $\overline{\text { CLRY. }}$ |
| $\overline{\text { CLRY }}$ | 29 | KBI C <br> ED C | KBI C CURS C | Used to clear to zero either the Y Cursor or the Y Display Register. Can go active independent of $\overline{\text { CLRX }}$. |
| $\overline{\text { CPUNT }}$ | C | INTF C | KBI C <br> CURS C <br> CONT C | $\overline{\text { CPUNT }}$ means that data is about to be asserted by the computer interface during the next $\overline{\text { STORE }}$ time. (See Fig. 6-5). It is asserted 0 to 100 ns after the leading edge of $\overline{\operatorname{READ}}$ and is removed just after the end of STORE. Other devices armed to use the STORE interval must hold their data off the minibus until the next $\overline{\text { STORE }}$ time when $\overline{\text { CPUNT }}$ is not true. |
| $\overline{\text { CSTROBE }}$ | 3 | KBI C <br> CONT C | ED C <br> INTF C | Strobes data to the Interface for transmission to the computer. If the origin of the data is the Terminal memory, as in an Enter operation, $\overline{\text { CSTROBE }}$ is a 636 ns pulse coincident with STROBE and either $\overline{R E A D}$ or STORE. (See Fig. 6-5.) If the origin of data is the keyboard, a peripheral, or another Interface, $\overline{\text { CSTROBE }}$ is generated coincident with $\overline{\text { STORE }}$ and STROBE and is 250 ns wide. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| $\overline{\text { CSUP }}$ | K | CONT C | INTF C | Inhibits the computer or peripheral interface from accepting a $\overline{\text { CSTROBE. }} \overline{\text { CSUP }}$ asserted at $\overline{R E A D}$ time inhibits sending of memory contents, as would be done with non-transmittable fields and null suppression. |
| DING | R | CURS C <br> CONT C | KBIC | Causes the bell to ring, and is asserted when the X Cursor Register senses the count of 72 when the operator is keying. Also asserted when attempting to key into a protected field or over a Field Attribute Code. |
| DIRECT | 19 | J208-3 | $\begin{aligned} & \text { KBI C } \\ & \text { ED C } \end{aligned}$ | Originates from the DIRECT/BUFFER switch When DIRECT is selected, this signal is high Keying of data causes CSTROBE to accompany the keyed data. When low (BUFFER selected). keying causes $\overline{T S T R O B E}$ to accompany the keyed data. TSTROBE occurs because the Buffer Mode is selected. Direct with an echo causes both CSTROBE and TSTROBE to accompany the keyed data. Also, when DIRECT is selected, roll-up can occur (if strapped), as can an auto CR/LF function. |
| $\overline{\text { DISPLAY }}$ | D | TIM C | $\begin{aligned} & \text { CURS C } \\ & \text { ED C } \\ & \text { CONT C } \end{aligned}$ | During the time that this signal is active, data on the bus is being read from the RAM into the Character Generator and used to produce video. It roughly corresponds to "not blanking" Control logic can read data on the bus at this time for several purposes (data is valid on the trailing edge of STEP.) Logic can read Field Attribute Codes and detect cursor location to determine whether the cursor is in a protected field. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| $\overline{\text { DMA }}$ | K | KBI C <br> ED C | KBI C <br> CURS C <br> CONT C <br> TIM C <br> INTF C | $\overline{\text { DMA }}$ goes active during Edit, Clear Page and Erase Input functions. During Direct Memory Access (DMA), normal timing is suspended to enable the logic that asserts $\overline{\mathrm{DMA}}$ to have full control of the memory. $\overline{R E A D}$, $\overline{S T O R E}$, EXECUTE, $\overline{R I G H T}$ and $\overline{\text { DOWN }}$ commands cease to come from the Timing Card. STROBE and $\overline{\mathrm{STEP}}$ change repetition rate. $\overline{\mathrm{CLRX}}$, $\overline{\text { CLRY }}, \overline{U P}, \overline{D O W N}, \overline{\text { LEFT }}$, and $\overline{\text { RIGHT control }}$ the Display Register, which in turn addresses the memory. The screen is blanked and the RAM refresh cycle is suspended. The logic that asserts $\overline{\mathrm{DMA}}$ then manipulates data in a write/ read pattern at a speed that ensures data is not lost. |
| DMA STROBE | 33 | TIM C | KBIC <br> CURS C <br> ED C | During $\overline{\mathrm{DMA}}$, this 90 ns pulse switches to a $1.9 \mu$ s period, whose leading edge is used to strobe data from the RAM to the registers. The period before and including the leading edge is DMA Read. The trailing edge of $\overline{\text { DMA STROBE }}$ indicates that a DMA Store period has begun and registers wishing to enter into the RAM should place data on the minibus, until the trailing edge of $\overline{S T E P}$. |
| $\overline{\text { DOWN }}$ | N | KBI C <br> ED C <br> CONT C <br> TIM C | KBI C <br> CURS C <br> ED C | The down counting pulse for the Cursor and Display Registers. Example: a low pulse on $\overline{\text { DOWN }}$ at EXECUTE time will move the cursor down one character line. |
| $\overline{\text { ECHO }}$ | 7 | INTF C | KBI C | Directs the input source (such as the Keyboard via the Keyboard Interface Card) to assert TSTROBE with each CSTROBE to provide a local copy to the Terminal screen of data entered to the computer. $\overline{\mathrm{ECHO}}$ is asserted by the Interface and, depending on the Interface, selected by strap option or rear panel control. |
| $\overline{\text { ENTER }}$ | Y | CONT C | KBI C | Goes active when the Enter of Send sequence of transmission from Terminal memory is in progress. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| EOLCRS | R | CURS C | ED C CONT C | Indicates that the X Cursor Register has reached the end of the line (79th count). When transmitting memory contents to the computer, EOLCRS is sensed to automatically transmit CR's (LF's optional) into the data stream to compensate for their not being stored in memory. CR's (and LF's) are transmitted only at the ends of those lines that contain data. |
| EOLDIS | $\overline{\text { D }}$ | CURS C | $\begin{aligned} & \text { KBI C } \\ & \text { ED C } \end{aligned}$ | This signal goes true when the X Display Register has sensed the End of a line (80th character position). It is used primarily in Direct Memory Access (DMA) operations. |
| EXECUTE | 18 | TIM C | KBI C <br> CURS C <br> ED C <br> CONT C <br> INTF C | This is a master timing signal which occurs during horizontal retrace at counts of 220 and 221 in the $\div 50$ counter on the Timing Card. See Fig. 6-5. During EXECUTE time, the Cursor Registers are mainpulated for LF, CR, UP, DOWN, HOME, etc. If a command has been issued resulting in $\overline{\text { DMA }} \overline{\text { TBUSY }}$ is set immediately at EXECUTE time. |
| $\overline{\text { HCU BUSY }}$ | J | CONT C | $\begin{aligned} & \text { ED C } \\ & \text { TIM C } \end{aligned}$ | This signal indicates that the Hard Copy Unit is busy making a copy of the memory. This signal also blanks the cursor when tabbing during non-transmittable periods of the buffer transmission sequence, and when making a hard copy. |
| $\frac{\overline{H I X}}{\overline{H I Y}}$ | $\begin{aligned} & 13 \\ & \text { J } \end{aligned}$ | ED C CONT C | KBI C <br> RAM C <br> CURS C <br> ED C <br> CONT C | These signals are used along with data to preset (respectively) the X and Y Cursor and Display Registers, or to read them at $\overline{\text { READ }}$ time. |
| HOME | F | KBI C | CONT C | This signal goes active as a result of pressing the HOME key. It causes the X and Y Cursor Registers to be cleared, thus homing the cursor. |

TABLE 6 -8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| KEYGATE | M | KBI C | RAM C CURS C ED C CONT C INTF C | KEYGATE goes true as a result of keying data from the keyboard or by pressing one of the Function Control keys (INS C, INS L, $\rightarrow \downarrow$, etc.) It normally goes true for one $\overline{\text { STORE }}$ time, 3 to 19 milliseconds after BOUNCE has become inactive. If $\overline{B O U N C E}$ stays true for greater than 300 milliseconds, KEYGATE has a repetition rate of 15 Hz to repeat cursor movements. |
| KLOCK | $\bar{N}$ | CONT C | KBI C | Indicator 2 on the console is controlled by this signal. It is used to indicate Keyboard lock conditions, and inhibits TSTROBE. This is how data and Field Attribute Codes are protected from keyboard replacement. |
| LCE | $\overline{\text { B }}$ | CONT C | $\begin{aligned} & \text { KBI C } \\ & \text { ED C } \end{aligned}$ | $\overline{\text { LCE }}$ goes active when the ESC Control Character is detected on the minibus. It indicates the following character (concurrent with $\overline{L C E}$ ) is to be interpreted as a command and is not to perform its normal function. |
| LED 3 <br> (Indicator 3) | 2 |  |  | Spare Indicator. |
| $\overline{\text { LEFT }}$ | w | KBIC ED C CONT C | curs C | Counting signal that decrements the count in the X Cursor Register. Example: A low on $\overline{\text { LEFT }}$ at EXECUTE time moves the cursor left one space. |
| LEFT CRS | L | CURS C | ED C CONT C | When true, it signifies that the cursor is at the left-most position of the display. |
| $\overline{\text { LOCAL }}$ | H | J208-2 | CONT C <br> INTF C | Originates from the LOCAL/ON LINE switch and indicates that the Terminal is logically disconnected from the computer. The associated peripheral devices (if any are connected) can interact with each other in Local Mode. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| LSTY CRS | 32 | CURS C | KBI C <br> ED C <br> CONT C | Indicates that the Cursor Register on the Cursor Card has reached the last character line. The Cursor Card may be strapped to enable this signal to go active with either 12 or 24 line displays. |
| LSTY DIS | 16 | CURS C | $\begin{aligned} & \text { KBI C } \\ & \text { ED C } \end{aligned}$ | Indicates that the $Y$ Display Register on the Cursor Card has reached the last character line. It may also be strapped for either 12 or 24 line displays. |
| $\overline{\text { MAKE COPY }}$ | $\bar{C}$ | KBI C CONT C | TIM C | Directs the Hard Copy Unit to make a copy. |
| $\overline{\text { PAGE }}$ | $\bar{E}$ | KBI C RAM C | KBI C <br> ED C <br> CONT C <br> TIM C <br> INTF C | This signal is asserted by simultaneously pressing the PAGE-ERASE INPUT and SHIFT keys. The signal also goes active when power is turned on. Its function is to erase the memory (protected data as well), and home the cursor. |
| $\overline{\text { READ }}$ | 4 | TIM C | Used on all cards | A synchronizing signal that occurs in the horizontal retrace interval, in counts 208, 209, 210, and 211 of the $\div 50$ counter on the Timing Card. See Fig. 6-5. During this time, the contents of the RAM at the cursor location, are placed on the minibus, regardless of whether the Terminal is On Line, in Local, or Sending. Decoding of data by Terminal logic is done in count 208 when STEP is active. If necessary, this allows $\overline{\mathrm{CSUP}}$ to be asserted in counts 209, 210, and 211. For example, the above would be done to accomplish null suppression. Reading cursor coordinates is also done at this time. |
| RESET | 28 | CONT C | KBI C <br> ED C <br> TIM C | Goes active as a result of the operator pressing the Keyboard RESET key. It is a multi-purpose key that performs the functions listed in the Characteristics Section. |

TABLE 6 -8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| RIGHT | V | KBI C <br> ED C <br> CONT C <br> TIM C | CURS C | Increment signal for the $X$ Cursor and Display Registers. Example: $\overline{\text { RIGHT }}$ at EXECUTE time increments the X Cursor Register. $\overline{\text { RIGHT at }}$ $\overline{\text { STEP }}$ time during $\overline{D M A}$ or DISPLAY, increments the X Display Register. |
| SEND 8 | 27 | INTF C | KBI C <br> ED C <br> CONT C | Indicates that data is being sent as an 8-bit byte (do not add parity). Inhibits Terminal from storing or executing characters while allowing peripherals to use the minibus. |
| SP1(FAST I/O) | 23 | TIM C | KBI C <br> INTF C | Spare minibus line that can be used by interfaces or peripherals. SP1 can be used for Fast I/O. Fast I/O can be strapped on the Timing Card to cause the Input/Output (I/O) sequence to occur not only in the horizontal retrace period of time, but five more times where display usually occurs. During Fast I/O, the screen is blanked. The logical operation of the Terminal is unchanged; however, Fast $\mathrm{I} / \mathrm{O}=94,320$ characters per second, whereas regular $\mathrm{I} / \mathrm{O}=15,720$ characters per second. |
| $\begin{aligned} & \overline{\mathrm{SP2}} \\ & (\overline{\mathrm{TAPEFETCH}}) \end{aligned}$ | P | (TTY PORT INTF C) | CONT C | Signal generated by some TTY Port Interface Cards that provides transmission control. Normally a prompt for the transmission of one character. |
| $\overline{\text { STEP }}$ | 22 | TIM C | KBI C <br> ED C <br> CONT C | A 1.572 MHz signal that provides timing intervals for the horizontal sweep. One horizontal sweep is $63.6 \mu \mathrm{~s}$. $\overline{\text { STEP }}$ divides the sweep into 100 timing intervals of 636 ns . See Fig. 6-5. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| STORE | E | TIM C | KBI C CURS C CONT C ED C INTF C | $\overline{\text { STORE }}$ goes active during counts 218 and 219 of the $\div 50$ counter on the Timing Card. See Fig. 6-5. STORE occurs once every horizontal sweep (every $63.6 \mu \mathrm{~s}$ ) during the horizontal retrace interval. Data to be entered into the RAM from the Keyboard Interface or peripheral, should be on the bus at counts 216 and 217 of the $\div 50$ Counter. At STEP time and count 216, logic determines whether a TSUP should be asserted in count 217. If TSUP is not asserted, at count 217, the bus data is written into memory at the cursor address at count 217. If a CSTROBE has previously been asserted at count 210, the bus data goes to the Interface. Valid on-line combinations of $\overline{\text { CSTROBE }}$ and $\overline{\text { TSTROBE }}$ at $\overline{\text { STEP }}$ time include: |
|  |  |  |  | Lo Lo To Terminal <br> and Computer |
|  |  |  |  |  |
|  |  |  |  | Hi Lo ${ }^{\text {H }}$ To Computer |
|  |  |  |  | Hi Hi Input/Output <br> inhibited |
| Strobe | 21 | TIM C | KBI C <br> CURS C <br> ED C <br> CONT C | A 250 ns master timing signal that is usually timed according to the display memory read/write pulse requirements. At $\overline{R E A D}$ time, it is 636 ns . See Fig. 6-5. It is pulsed in counts 214 and 217 of the $\div 50$ Counter for memory refresh, and count 219 for writing data from the minibus into memory. It is also pulsed continuously at a $1.9 \mu \mathrm{~s}$ rate during the time $\overline{\mathrm{DMA}}$ is active. |
| SW1 and SW2 | $\begin{aligned} & z \\ & x \end{aligned}$ | $\begin{gathered} \mathrm{J} 208-5 \\ \mathrm{~J} 208-4 \end{gathered}$ |  | Spare console rocker switches reserved for use with interfaces and peripherals. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| TBUSY | 8 | KBI C <br> ED C | TIM C | With flagged interfaces, TBUSY controls the timing of data being transmitted to the Terminal. See Fig. 6-5. For operations like Line Feed, Carriage Return, Home, Address Cursor, and transmission of buffer contents, the Terminal does not go busy. A peripheral can also pull down on TBUSY. |
| TOP CRS | $\bar{M}$ | CURS C | ED C <br> CONT C | When true, it signifies that the Cursor Register is at a count that corresponds to the top character line of the display. |
| TSTROBE | 5 | KBI C <br> ED C <br> CONT C <br> INTF C | CURS C <br> ED C <br> CONT C <br> KBI C | When active, $\overline{\text { TSTROBE enables STROBE to }}$ strobe data into the Terminal to be displayed on the screen. It goes true the same time as STORE. See Fig. 6-5. Thus, for data to be decoded, stored, or to address the cursor, TSTROBE must be anded with STROBE at STORE time. |
| $\overline{\text { TSUP }}$ | 17 | KBI C CONT C | KBI C | When active, the Terminal memory response to $\overline{\text { TSTROBE }}$ is suppressed. $\overline{\text { TSUP }}$ is used to prevent entry into memory of incoming data such as CR and LF. If entry is to be suppressed, Terminal logic asserts TSUP during the second character portion of the window (count 217 of the $\div 50$ Counter on the Timing Card) before STROBE becomes true. |
| $\overline{U P}$ | $\bar{H}$ | KBI C <br> ED C <br> CONT C | $\begin{aligned} & \text { CURS C } \\ & \text { ED C } \end{aligned}$ | A counting signal that, when true, allows the count in the Y Cursor Register to be decremented at EXECUTE time. Logic also allows the $Y$ Display Register to be decremented at $\overline{\mathrm{STEP}}$ when $\overline{\mathrm{UP}}$ is true. |
| VSYNC | 34 | TIM C | KBI C <br> CURS C <br> CONT C | A low $190.8 \mu \mathrm{~s}$ signal that correponds to 3 horizontal times during vertical retrace. Its leading edge is 3 horizontal sweeps after the last visible line on the bottom and 18 sweeps before the next visible sweep at the top. |

TABLE 6-8 (cont)
SIGNAL DEFINITIONS (cont)

| Signal | Minibus Pin | Source | Used By | Description |
| :---: | :---: | :---: | :---: | :---: |
| $\overline{\text { WAIT }}$ | 25 | INTF C |  | An output of the Optional Data Communications Interface that signifies a computer transmission is pending or in progress, or a half duplex line is turned with the Terminal in the receive mode. |
| X EQUAL | $\overline{\mathrm{A}}$ | CURS C | EDC <br> TIM C <br> CONT C | When true, it signifies that the $X$ Cursor Register count is equal to the $X$ Display Register count. This signal, along with $Y$ EQUAL is used to generate the cursor. The cursor address is the location in memory where data will either be read from or written to at $\overline{\text { READ }}$ or STORE time, respectively. X EQUAL is valid at the leading edge of $\overline{\text { STEP. }}$ |
| Y EQUAL | 31 | CURS C | ED C <br> CONT C <br> TIM C | Signifies that the Y Cursor Register count is equal to the Y Display Register count. This signal along with $X$ EQUAL is used to generate the Cursor. Y EQUAL is valid on the leading edge of $\overline{\text { STEP. }}$ |
| 614 kHz | B | RAM C | INTF C | Square wave used by the Interface. |
| 4.9152 MHz | 24 | RAM C | INTF C | Square wave used by the Interface. |
| +15 Vdc | 15 |  | INTF C |  |
| $+5 \mathrm{Vdc}$ | S |  | All cards |  |
| $-5 \mathrm{Vdc}$ | $\overline{\mathrm{P}}$ |  | RAM C TIM C | Low voltage power supplies. |
| -12 Vdc | 14 |  | INTF C <br> RAM C <br> TIM C |  |





Fig. 6-16. Semiconductor Information.

| An | － 0 | ${ }^{\circ}$ | ${ }^{\circ}$ | 8 | 品 | $\because$ | － | ： |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 品 | $\because$ | \％ | $\because 0$ | $\cdots$ |  | 品品 |  |  |
|  | $\cdots$ | ${ }^{n}$ | 吅品 | 号 | 0 |  | 促品 | \％ |  |
|  | $\bigcirc$ | － | 品 | 品 | － | － | $\bigcirc$ | － |  |
|  | － | $\cdots$ | \％ | $\bigcirc$ | $\bigcirc$ | 品 | 品 | 品 |  |
|  | 品 | \％ | \％ | 品品 | 品品 | 品品 |  |  |  |
| 部言品品 | 品 | － | $\stackrel{\square}{\square}$ | 品品 | 品 | 品品 |  | 品品 |  |
| －$\quad$ 品 | $\bigcirc$ | ¢00 | 号品 | 品 | 吅品 | － | － | － |  |
| － | 品品 |  | 品品 | 品 | 品品 | － | 品品 | 品品 |  |
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| $\bigcirc$ |  | \％ | $\stackrel{\square}{\square}$ |  |  | 品品 |  | 品品 | \％ |
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| ¢ ${ }^{\text {\％}}$ |  | 品 | 品品 |  | 品品 |  |  | 品品 |  |
|  |  | 品品 |  |  |  |  |  | 兂品品 |  |
| －${ }^{\circ} \mathrm{B}$ | 品品 | 硡品 | \％ | 品 |  | 品 |  | 品品 | ${ }^{3}$ |
|  | $\bigcirc$ | ¢ | － | \％ | 品 | － | \％ | $\bigcirc$ |  |
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|  |  | \％ | 品品 | 品品 | － | \％ |  | 吅品 |  |
| ¢ ${ }^{8}$ |  |  | 品品 |  |  |  |  |  |  |
|  | 㖪品品 |  | 品 |  |  |  |  | 品品 |  |







Fig. 6-20A. Timing Card Component Locations (670-2199-02).


Fig. 6-20B. Timing Card Component Locations (670-2199-03).



Fig. 6-20D. Timing Card Component Locations (670-2199-05).

| CKT \# GRID LOC CAPACITOR |  | CKT \# Grid |  |  | grid loc |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | integrated circuit |  |  | F5 |  |
| c11 | H4 | U1 | н3 |  | G3 |  |
| c69 | H4 | 411 | H2 | U321A | D2 |  |
| c87 | н5 | U21 | н3 | U3218 | E2 |  |
| C90 | H1 | U31 | H4 | U331A | +2 |  |
| c91 | H1 | 041 | G5 | U3318 | ${ }_{\text {F4 }}$ |  |
| c95 | ${ }^{\text {B6 }}$ | U51A | F5 | U3310 | F4 |  |
| c98 | B5 | U518 | B3 | U341 | D5 |  |
| c99 | A5 | U55 | $\mathrm{G}_{5}$ | U351 | B1 |  |
| C121 | H4 | 061 | H4 | U395A | G2 |  |
| C159 | H5 | U61A | G4 | U359A | G2 |  |
| C169 | H2 | U69 A | G5 | பз598 | H4 |  |
| C189 | H1 | U698 | F5 | U3618 | c4 |  |
| C199 | B6 | U69C | ${ }^{\text {H4 }}$ | U361C | c3 |  |
| C221 | н5 | U69D | F4 | U361D | D5 |  |
| C251 | H5 | 471 | D4 | U369 | C4 |  |
| C269 | H5 | U81A | F5 | U369A | G2 |  |
| C289 | D5 | 481 B | D5 | U3698 | B2 |  |
| C291 | H5 | 489 | ${ }^{\text {H1 }}$ | U369D | в3 |  |
| C390 | H5 | U89A | H1 | U369F | c5 |  |
| C399 | E5 | U898 | F2 | U371A | D4 |  |
| C411 | н5 | U101A | G2 | U3718 | E5 |  |
| C461 | H5 | U1018 | ${ }^{\text {G3 }}$ | U371C | D5 |  |
| C469 | $\begin{array}{r}\text { H5 } \\ \\ \\ \hline 6\end{array}$ | U101C | G3 | U371D | C5 |  |
| DIode |  | U101D | ${ }_{\text {E }}{ }^{\text {G }}$ | U381A | D4 |  |
|  |  | U101F | G3 G3 | U3818 | C5 |  |
| CR91 | G2 | U111A | G5 | U381C | C4 |  |
| CR397 | c5 | U1118 | G3 | 4389 | C3 |  |
| JACK |  | U111C | ${ }^{\text {c2 }}$ | U395A | B4 |  |
|  |  | U111D | F4 | U3955 | ${ }^{\text {c5 }}$ |  |
| 376 | B6 | U121B U131A | E4 | U3950 | c5 |  |
| J78 | B6 | U131B | G3 | U401 | ${ }^{\text {c }}$ |  |
|  | E1 | U131C | G2 | U411A | B2 |  |
|  | F1 | U1310 | H4 | U4118 | D4 |  |
|  | G1 D6 | U131E | G3 | U4112 | ${ }^{\text {c }}$ - |  |
| 379 | E6 | U131F | G4 <br> +1 | U421B | c2 |  |
|  | F6 | U141B | H4 | U421C | F4 |  |
| CHOKE, COIL |  | U141C | D4 | U421D | C2 |  |
| L90 | H2 | U1410 | ${ }_{\text {F }} 5$ | U421E | H5 D2 |  |
| L189 | H2 | U151A | F4 | U431A | нз |  |
| transistor |  | U161A | G2 | U431B | E4 |  |
| 090 | G2 | U1618 | G3 | U431C | F4 |  |
| 092 | G2 | U161C | 61 | U441A | ${ }^{\text {G2 }}$ |  |
| 094 | B5 | U169A | G5 | U4418 | D4 |  |
| 096 | B5 | U1698 | G5 | U441C | D4 |  |
| 098 | A5 | U1718 | ${ }^{\text {E4 }}$ | U4410 | D4 |  |
| 0199 0397 | B4 C5 | U171C | E4 | 0451 | D2 |  |
| 0397 0398 | C5 C5 | U1710 | E5 | 0461 | D2 |  |
| Resistor |  | U181A | D3 | U465A | ${ }^{\text {A3 }}$ |  |
|  |  | U1818 | B4 | U465 | 82 |  |
| R65 | H2 | U181C | D4 | U469B | D2 |  |
| R75 | G5 | U1810 | F5 | U469C | c6 |  |
| R79 | F6 | U181E | H1 | U4714 | C6 |  |
| R81 R90 | D2 | U181F | A3 | U471C | ${ }^{\text {c6 }}$ |  |
| R90 R91 | G2 | U189A | D4 H1 | U4710 | F5 |  |
| R91 R92 | ${ }^{\text {G2 }}$ | U1898 | H1 G2 | U481 | c4 |  |
| ${ }_{\text {R93 }}$ | ${ }^{\text {B5 }}$ | U189D | C4 | U489A | c3 |  |
| R94 | B6 | U191A | H1 | U4898 | B3 |  |
| R95 | B6 | U191B | H1 | U4898 | ${ }^{\text {c3 }}$ |  |
| $\mathrm{R}^{\mathrm{R96}}$ | B5 | U191C | C4 | U4991 | ${ }^{\text {c3 }}$ |  |
| R97 | ${ }^{\text {B5 }}$ | U191D | H1 | U495A | B3 |  |
| R98 R99 | A5 B5 | U201A | G4 64 | U4958 | c3 |  |
| R111 | H4 | U201C | F2 | U495D | ${ }^{\text {c }}$ |  |
| R190 | H3 | U201D | G2 | U495E | ${ }^{\text {B3 }}$ |  |
| R191 | B5 | U211A | F4 | U495F U495 | - ${ }^{\text {B3 }}$ |  |
| R192 | B5 | U2118 | E3 | U4995J | C3 |  |
| ${ }_{\text {R193 }}$ | B5 85 | U221A U2218 | E4 | U4995k | 12 |  |
| R195 | ${ }^{\text {A5 }}$ | U221C | F2 | U495L | 13 |  |
| R196 | A4 | U221D | E3 | U495M | D3 |  |
| R197 | B4 | U231A | E3 | U495N | C2 |  |
| R198 | A4 | U241A | E4 | U495R | C2 |  |
| R199 | c5 | U2418 | E4 | U499 | C3 |  |
| R231 | 14 | U241C | F2 |  |  |  |
| R251 | B2 | U2410 | G4 |  |  |  |
| ${ }^{\text {R252 }}$ | B2 | U251A | F4 |  |  |  |
| R253 | B2 | U2518 | F4 |  |  |  |
| R291 | B4 | U251C | A2 | SEmicon | NDUCTOR | information |
| R292 | B5 | U261 | B2 |  |  |  |
| R293 R294 | ${ }^{\text {B5 }}$ | U269A | D5 | number | vcc | gnd Pins |
| R294 R295 | B4 | U2698 | D4 |  |  |  |
| R295 | B4 | U271A | B3 | 7400 | 14 | HIGH |
| R296 | B5 | U2718 | B3 | 7402 | 14 | Low |
| R297 R298 | B5 <br> 85 | U271C | G2 | 7404 7408 | 14 14 | HIGH |
| R298 | B5 B2 | U271D | C5 | 7408 7410 | 14 14 | HIGH |
| R301 | F5 | U2818 | C5 | 7416 | 14 | 7 |
| R321 | G5 | U281C | C4 | 7420 | 14 | HIGH |
| R371 | H5 | U281D | D5 | 7430 | 14 | HIGH |
| R389 | C5 | U289A | в3 | 7437 | 14 | HIGH |
| R390 | E5 | U2898 | B2 | 7438 | 14 | 7 HIGH |
| R391 | c5 | U289C | в3 | 7440 | 14 | 7 High |
| R392 | C5 | U289D | C4 | 7473 | 4 | 11 HIGH |
| R393 | B4 | U291A | B5 | 7486 | 14 | Low |
| R394 | B4 | U2918 | B5 | 7490 | 5 | 10 Low |
| R395 | C5 | U291C | B5 | 7493 | 5 | 10 Low |
| R396 | c5 | U291E | B5 | 74161 | 16 | HIGH |
| R397 | C5 | U291F | B5 | 74165 | 16 | HIGH |
| R398 | C5 | U295C | B4 | 74175 | 16 | 8 HIGH |
| R399 | E5 | U295D | B4 | 74500 | 14 | High |
| R400 | E5 | U301A | F4 | 745112 | - 16 | High |
| R401 | C1 | U3018 | D5 |  |  |  |
| R489 | H5 | U301C | D2 |  |  |  |

$\overline{\square M a}$

| CKT \# | Grid loc | Loc |  | CKT \# | GRID LOC |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CAPACITOR |  | integrated circuit |  | U301D | F5 |  |
| C11 | H4 | U1 | H3 | U311A | G3 |  |
| c69 | H4 | U11 | ${ }_{\text {H2 }}$ | U3118 | G4 |  |
| C87 | H5 | 421 | H3 | U321A | D2 |  |
| c90 | H1 | U31 | H4 | U3218 $\sim$ | E2 |  |
| C91 | ${ }^{\mathrm{H}} 1$ | 041 | G5 | U331A | F2 |  |
| C95 | ${ }^{\text {B6 }}$ | U51A | F5 | U3318 | F2 |  |
| C98 | B5 | U518 | B3 | U331C | F4 |  |
| C99 | A5 | U55 | G5 | U3310 | F4 |  |
| C121 | H4 | U61 | H4 | U341 | D5 |  |
| C159 | H5 | U61A | G4 | 0351 | B1 |  |
| C169 | H2 | U69A | G5 | U359A | G2 |  |
| C189 | ${ }^{\text {H1 }}$ | U698 | F5 | U3598 | H4 |  |
| C199 | B6 | U69C | H4 | U361A | D5 |  |
| C221 | H5 | U69D | F4 | U3618 U361C | ${ }^{\text {c4 }}$ |  |
| C251 | H5 | 471 | D4 | U361D | ${ }_{\text {c }}$ |  |
| C269 | ${ }^{\text {H5 }}$ | U81A | F5 | ${ }^{\text {U369 }}$ | c4 |  |
| C289 | D5 +45 | 4818 | D5 | U369 A | G2 |  |
| C291 | H5 | 489 | H1 | บ3698 | B2 |  |
| C390 | H5 | U89a | H1 | U3698 | ${ }^{\text {B2 }}$ |  |
| C411 | H5 | U89B | F2 | U369F | c5 |  |
| c461 | H5 | U101A | G2 | U371A | D4 |  |
| C469 | H5 | U1018 | ${ }^{\text {G3 }}$ | U3718 | E5 |  |
| C492 | H6 | U101C | G3 | U371C | D5 |  |
| diode |  | U101D | E2 | U371D | C5 |  |
| CR91 | G2 | U101F | G3 | U381A | D4 |  |
| CR397JACK |  | U111A | G5 | U3818 | C5 |  |
|  |  | U1118 | G3 | U381C | C4 |  |
| J76 | B6 | U111C | C2 | U395A | B4 |  |
| J78 | B6 | U111 | F4 | U3958 | B4 |  |
|  | E1 | U131A | F4 | U395C | ${ }^{\text {c5 }}$ |  |
|  | F1 | U1318 | G3 | U395D | C5 |  |
|  | G1 | U131C | G2 | U401 | C4 |  |
| 179 | E6 | U131D | ${ }^{\text {H4 }}$ | V411A | B2 |  |
|  | F6 | U131E | G3 G4 | U411C | G4 |  |
| CHOKE, COIL |  | U141A | H3 | U411D | c2 |  |
| L90 | H2 | U1418 | H4 | U4218 | ${ }_{\text {C2 }}$ |  |
| L189 | H2 | U141C | D4 | U421D | C2 |  |
| transistor |  | U1415 | F5 | U421E | H5 |  |
| 090 | G2 | U1518 | F4 | U421F | D2 |  |
| 092 | G2 | U161A | G2 | U431A | H3 |  |
| 094 | B5 | U161B | G3 | U431C | F4 |  |
| 096 | B5 | U161C | G1 | U4310 | - ${ }_{\text {c }}$ |  |
| 098 | A5 | U169A | F5 | U441A | c3 |  |
| 0199 | B4 | U169B | G5 | U4418 | D4 |  |
| 0397 | C5 |  |  | U441C | D4 |  |
| 0398 | C5 | U1718 | B2 | U4410 | D4 |  |
| RESISTOR |  | U171D | E5 | 0451 | D2 |  |
| R65 | H2 | U181A | D3 | U465A | d2 A |  |
| R75 | G5 | U1818 | B4 | U465 | ${ }^{\text {A }}$ |  |
| R79 | F6 | U181C | D4 | U4698 | D2 |  |
| R81 | D2 | U181D | F5 | U469C | B3 |  |
| R90 | G2 | U181F | ${ }^{\text {A }}$ | U471A | c6 |  |
| R91 | ${ }^{\text {G2 }}$ | U189A | D4 | U47118 | E5 |  |
| R93 | B5 | U1898 | H1 | U471C | C6 |  |
| R94 | B6 | U189C | G2 | U4710 | F5 c4 |  |
| R95 | ${ }^{\text {B6 }}$ | U189D | C4 | U489A | c3 |  |
| R96 | ${ }^{\text {B5 }}$ | U191B | H1 H 1 | U4898 | в3 |  |
| R98 | A5 | U191C | C4 | U489C | c3 |  |
| R99 | B5 | U191D | H1 | U4898 | c3 |  |
| R111 | H4 | U201A | G4 | U491 | c3 |  |
| R190 | н3 | U201B | G4 | U495A | B3 |  |
| R191 | B5 | U201C | F2 | U4958 | C3 |  |
| R192 | B5 | U201D | G2 | U495D | ${ }^{\text {c3 }}$ |  |
| R193 | B5 | U211A | F4 | U495E | B3 |  |
| R194 | B5 | U2118 | E3 | U495F | ${ }^{\text {B3 }}$ |  |
| R195 | A5 | U221A | E4 |  | C3 |  |
| R196 | A4 | U2218 | E4 | U495J | ${ }^{\text {B2 }}$ |  |
| R197 | B4 | U221C | F2 | U495k | 12 |  |
| R198 | ${ }^{\text {A4 }}$ | U221D | E3 | U495L | ${ }^{13}$ |  |
| R199 | ${ }^{\text {c5 }}$ | 1231 A | E3 | U495M | D3 |  |
| R231 R251 | 14 | U241A | E4 | U495R | c2 |  |
| R251 R252 | B2 B2 | U2418 U241C | E4 | U499 | c3 |  |
| R252 | ${ }^{\text {B2 }}$ | U241D | G4 |  |  |  |
| R291 | B4 | U251A | F4 |  |  |  |
| R292 | B5 | U251B | F4 |  |  |  |
| R293 | B5 | U251C | A2 |  |  |  |
| R294 | B4 | 4261 | B2 | SEmico | NDUCTOR | nformation |
| R295 | B4 | U269A | D5 |  |  |  |
| R296 | ${ }^{\text {B5 }}$ | U2698 | D4 |  |  | unused |
| R297 R298 | B5 | U271A | ${ }^{\text {B3 }}$ | number | vcc | gnd pins |
| R300 | ${ }^{\text {B5 }}$ | U271C | G2 | 7400 | 14 | 7 HIGH |
| R301 | F5 | U2710 | ${ }^{\text {c5 }}$ | 7402 7404 | 14 14 | 7 Low |
| R321 | G5 | U281A | F5 | 7404 7408 | 14 14 | 7 HIGH |
| R371 | H5 | U2818 | C5 | 7408 7410 | 14 14 | $\begin{array}{ll}7 & \text { HIGH } \\ 7 & \text { HIGH }\end{array}$ |
| R389 R391 | ${ }_{\text {C5 }}$ | U2810 | D5 | 7416 | 14 | High |
| R392 | ${ }^{\text {c5 }}$ | U289A | в3 | 7420 | 14 | 7 HIGH |
| R393 | B4 | U2898 | B2 | 7430 | 14 | 7 HIGH |
| R394 | B4 | U289C | B3 | 7437 | 14 | $7{ }^{7} \mathrm{HIGH}$ |
| R395 | ${ }^{\text {c5 }}$ | $\mathrm{U}^{2} 289 \mathrm{D}$ | ${ }_{\text {C4 }}$ | 7438 7440 | 14 14 | $7{ }_{7}{ }_{7} \mathrm{HIGH}$ |
| R396 R397 | C5 C5 | U29918 | B5 | 7473 | , | 1 High |
| R398 | C5 | U291C | B5 | 7486 | 14 | 7 Low |
| R401 | c1 | 4291 E | B5 | 7490 | 5 | 10 Low |
| R489 | H5 | U291F | B5 | ${ }_{74163}$ | 5 | 10 LOW |
|  |  | U295C | B4 | 74161 | 16 | HIGH |
|  |  | U295D | B4 | 74165 74175 | 16 | 8 HIGH |
|  |  | U301A | F4 | 74175 | 16 | 8 HIGH |
|  |  | U301B U301C | D5 | 7745112 | 16 | ${ }_{\text {HIGH }}$ |



\begin{tabular}{|c|c|c|c|c|c|c|}
\hline ckt $\#$ \& grid loc \& CKT \# \& grid loc \& CKT \# \& \multicolumn{2}{|l|}{grid loc} <br>
\hline \multicolumn{2}{|l|}{capacitor} \& \multicolumn{2}{|l|}{integrated circuit} \& \multirow[t]{2}{*}{U301D U311A} \& \multicolumn{2}{|l|}{F5} <br>
\hline C11 \& H4 \& U1 \& H3 \& \& $\mathrm{G}^{\text {G }}$ \& <br>
\hline c69 \& H4 \& 011 \& H2 \& U321A \& ${ }^{\text {D2 }}$ \& <br>
\hline C87 \& H5 \& U21 \& H3 \& U3218 \& E2 \& <br>
\hline C90 \& H1 \& U31 \& H4 \& U3318 \& F2 \& <br>
\hline C91 \& H1 \& 041 \& G5 \& U3318 \& F4 \& <br>
\hline C95 \& B6 \& U51A \& F5 \& U3310 \& F4 \& <br>
\hline C98 \& B5 \& U518 \& ${ }^{\text {B3 }}$ \& U341 \& D5 \& <br>
\hline C99 \& A5 \& U55 \& G5 \& U351 \& B1 \& <br>
\hline C121 \& H4 \& 461 \& H4 \& U395A \& G2 \& <br>
\hline C159 \& H5 \& U61A \& G4 \& U359A \& G2 \& <br>
\hline C169 \& ${ }^{\mathrm{H} 2}$ \& U69A \& G5 \& U359B \& H4 \& <br>
\hline C189 \& H1 \& U69B \& F5 \& U3618 \& C4 \& <br>
\hline C199 \& B6 \& U69C \& H4 \& U361C \& c3 \& <br>
\hline c221 \& H5 \& U69D \& F4 \& U3610 \& D5 \& <br>
\hline C251 \& H5 \& 471 \& D4 \& U369 \& C4 \& <br>
\hline C269 \& H5 \& U81A \& F5 \& U369A \& G2 \& <br>
\hline C289 \& D5 \& U818 \& D5 \& บЗ69в \& B2 \& <br>
\hline C291 \& H5 \& 489 \& H1 \& U369D \& B3 \& <br>
\hline C390
c399 \& H5
E5 \& U89A \& H1
F2 \& U369F \& c5 \& <br>
\hline C411 \& H5 \& U101A \& G2 \& U371A \& D4 \& <br>
\hline C461 \& H5 \& U101B \& G3 \& U3718 \& E5 \& <br>
\hline C469 \& H5 \& U101C \& G3 \& U3710 \& c5 \& <br>
\hline C492 \& н6 \& U101D \& ${ }_{\text {E2 }}$ \& U381A \& D4 \& <br>
\hline \multicolumn{2}{|l|}{DIODE} \& U101E \& G3 \& U3818 \& C5 \& <br>
\hline CR91 \& G2 \& U111A \& ${ }_{6}$ \& U381C \& C4 \& <br>
\hline CR397 \& C5 \& U1118 \& G3 \& 0389 \& ${ }^{\text {c3 }}$ \& <br>
\hline CR399 \& E5 \& U1119 \& C2 \& U395A \& ${ }^{\text {B4 }}$ \& <br>
\hline \multicolumn{2}{|l|}{Jack} \& U1110 \& F4 \& U395C \& C5 \& <br>
\hline \multirow[t]{5}{*}{376

78} \& B6 \& U131A \& F4 \& U3950 \& C5 \& <br>
\hline \& ${ }^{\text {B6 }}$ \& ${ }^{\text {U1318 }}$ \& ${ }_{\text {c }}$ \& U401 \& C4 \& <br>
\hline \& E1 \& U131C \& G2 \& U411A \& B2 \& <br>
\hline \& F1 \& U131D \& H4 \& U4118 \& D4 \& <br>
\hline \& G1 \& U131E \& G3 \& U411C
U411D \& ${ }^{\text {G4 }}$ \& <br>
\hline \multirow[t]{2}{*}{J79} \& D6 \& U131F \& G4 \& 44218 \& ${ }^{\text {c2 }}$ \& <br>
\hline \& F6 \& U141A \& \& U421C \& F4 \& <br>
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{CHOKE, COIL}} \& U141C \& D4 \& U421D \& C2 \& <br>
\hline \& \& U1410 \& F5 \& U421E \& H5 \& <br>
\hline L189 \& H2 \& U151A \& F4 \& U421F \& D2 \& <br>
\hline \& H2 \& U1518 \& F4 \& U431A \& H3 \& <br>
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{transistor}} \& U161A \& G2 \& 4318 \& F4 \& <br>
\hline \& \& U161B \& G3 \& $4331{ }^{\text {d }}$ \& -4 \& <br>
\hline 092 \& G2 \& U161C \& G1 \& U4471A \& ${ }^{\text {c }}$ \& <br>
\hline 094 \& B5 \& U169A \& G5 \& U441B \& D4 \& <br>
\hline 096 \& B5 \& U1698 \& G5 \& U441C \& D4 \& <br>
\hline 098 \& ${ }^{\text {A5 }}$ \& U1714 \& E4 \& U441D \& D4 \& <br>
\hline 0199
0397 \& ${ }^{\text {B4 }}$ \& U171C \& E4 \& U451 \& D2 \& <br>
\hline 0398 \& C5 \& U171D \& E5 \& U461 \& D2 \& <br>
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{resistor}} \& U181A \& D3 \& U465D \& ${ }^{\text {B4 }}$ \& <br>
\hline R65 \& \& \& 84 \& U4698 \& D2 \& <br>
\hline R75 \& G5 \& U181D \& F5 \& U469C \& B3 \& <br>
\hline R79 \& F6 \& U181E \& H1 \& U471A \& C6 \& <br>
\hline R81 \& D2 \& U181F \& A3 \& U471B \& ${ }^{\text {E5 }}$ \& <br>
\hline R90 \& G2 \& U189A \& D4 \& U4710 \& F5 \& <br>
\hline R91 \& G2 \& $\cup 1898$ \& ${ }^{H}$ \& $\cup 481$ \& c4 \& <br>
\hline R92 \& B5 \& U189C \& G2 \& U489A \& c3 \& <br>
\hline 893 \& ${ }^{\text {B5 }}$ \& U189D \& ${ }^{\text {c4 }}$ \& U4898 \& в3 \& <br>
\hline R94 \& ${ }^{\text {B6 }}$ \& U191A \& H1 \& U489C \& c3 \& <br>
\hline R95 \& ${ }^{\text {B6 }}$ \& U1918 \& H1 \& U4890 \& c3 \& <br>
\hline R96 \& B5 \& U191C \& ${ }_{\text {c }}$ \& U491 \& c3 \& <br>
\hline R97 \& - ${ }^{\text {A5 }}$ \& U1901A \& H1
G4 \& U495A \& B3 \& <br>
\hline R99 \& B5 \& U2018 \& G4 \& U4958 \& c3 \& <br>
\hline R111 \& H4 \& U201C \& F2 \& U495D \& c3 \& <br>
\hline R190 \& H3 \& U201D \& G2 \& U495E \& B3 \& <br>
\hline R191 \& B5 \& U211A \& F4 \& U4995 \& -83 \& <br>
\hline R192 \& B5 \& U2118 \& E3 \& U495.J \& ${ }_{\text {B2 }}$ \& <br>
\hline R193 \& B5 \& U221A \& E4 \& 4495 K \& 12 \& <br>
\hline R195 \& A5 \& U221C \& F2 \& U495L \& 13 \& <br>
\hline R196 \& A4 \& U221D \& E3 \& U495M \& D3 \& <br>
\hline R197 \& B4 \& U231A \& E3 \& U495N \& c2 \& <br>
\hline R198 \& A4 \& U241A \& E4 \& U495R \& C2 \& <br>
\hline R199 \& C5 \& U2418 \& E4 \& U499 \& c3 \& <br>
\hline R231 \& 14 \& U241C \& F2 \& \& \& <br>
\hline R251 \& B2 \& U241D \& G4 \& \& \& <br>
\hline R252 \& B2 \& U251A \& F4 \& \& \& <br>
\hline R253 \& B2 \& U2518 \& F4 \& \multicolumn{3}{|l|}{\multirow[t]{2}{*}{SEmiconductor information}} <br>
\hline R291 \& B4 \& U251C \& A2 \& \& \& <br>
\hline R292 \& B5 \& 4261 \& B2 \& \& \& <br>
\hline R293 \& B5 \& U269A \& D5 \& \multirow[t]{2}{*}{number} \& vcc \& GND PINS <br>
\hline R294 \& B4 \& U2698 \& D4 \& \& \& <br>
\hline R295 \& 84 \& U271A \& в3 \& 7400 \& 14 \& HIGH <br>
\hline R296 \& B5 \& U2718 \& в3 \& 7402 \& 14 \& 7 LOW <br>
\hline R297 \& B5 \& U271C \& G2 \& 7404 \& 14 \& 7 \% <br>
\hline R298 \& B5 \& U2710 \& C5 \& 7408 \& 14 \& HIGH <br>
\hline R300 \& B2 \& U281A \& F5 \& 7410 \& 14 \& High <br>
\hline R301 \& F5 \& U2818 \& C5 \& 7416 \& 14 \& 7 <br>
\hline R321 \& G5 \& U281C \& C4 \& 7420 \& 14 \& 7 HIGH <br>
\hline R371 \& H5 \& U281D \& D5 \& 7430 \& 14 \& 7 HIGH <br>
\hline R389 \& C5 \& U289A \& в3 \& 7437 \& 14 \& 7 HIGH <br>
\hline R390 \& E5 \& U2898 \& B2 \& 7438 \& 14 \& 7 HIGH <br>
\hline R391 \& C5 \& U289C \& B3 \& 7440 \& 14 \& 7 HIGH <br>
\hline R392 \& C5 \& U289D \& C4 \& 7473 \& 4 \& 11 HIGH <br>
\hline R393 \& B4 \& U291A \& B5 \& 7486 \& 14 \& Low <br>
\hline R394 \& B4 \& U2918 \& B5 \& 7490 \& 5 \& 10 Low <br>
\hline R395 \& C5 \& U291C \& B5 \& 7493 \& 5 \& 10 Low <br>
\hline R396 \& C5 \& U291E \& B5 \& 74161 \& 16 \& HIGH <br>
\hline R397 \& c5 \& U291F \& B5 \& 74165 \& 16 \& HIGH <br>
\hline R398 \& C5 \& U295C \& B4 \& 74175 \& 16 \& HIGH <br>
\hline R399 \& E5 \& U295D \& B4 \& 74500 \& 14 \& HIGH <br>
\hline R400 \& E5 \& U301A \& F4 \& 745112 \& 16 \& HIGH <br>
\hline R401
R489 \& C1

H5 \& | U301B |
| :--- |
| U301C | \& D5 \& \& \& <br>

\hline
\end{tabular}






Fig. 6-22. Keyboard interface Card Component Locations 670-2301-04 and below.

| CKT \# | grid loc | CKT \# | Grid Loc | CKT \# | GRID LOC | CKT \# | GR |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CAPACITOR |  | U41B | F3 | U201C | D3 | U369E | C2 |  |  |
| C1 | A1 | U41C | E4 | U201D | F5 | U369F | C1 |  |  |
| cı0 | A1 | U41D | F4 | U201E | F5 | U371A | E6 |  |  |
| c90 | A1 | U49A | D3 | U201F | F5 | U371B | E6 |  |  |
| C101 | A2 | U49D | E4 | U209 | H3 | U371C | E6 |  |  |
| C160 | A2 | U51A | B2 | U229 | G4 | U3710 | F5 |  |  |
| C180 | A2 | U51B | F5 | U231A | G2 | U371E | E6 |  |  |
| C189 | A2 | U51C | G5 | U231B | G3 | U371F | E6 |  |  |
| C233 | A2 | U51D | D4 | U231C | 15 | U379A | C6 |  |  |
| C350 | A2 | U61A | H2 | U231D | H4 | U379C | E6 |  |  |
| C370 | A3 | U61B | G6 | U239A | H5 | U379D | E5 |  |  |
| C385 | A3 | U61C | E5 | U239B | G2 | U379E | E6 |  |  |
| C428 | A3 | U61D | E4 | U241A | G5 | U381A | D6 |  |  |
| C429 | D5 | U69A | G5 | U241B | G3 | U381B | D6 |  |  |
|  |  | U69C | G4 | U241C | G4 | U381C | D6 |  |  |
| DIODE |  | 479 | A4 | U249A | C3 | U381D | D6 |  |  |
| DIODE |  | U81A | B4 | U249B | G2 | U389A | c3 |  |  |
| CR409 | D5 | U81B | B4 | U249C | B3 | U389B | c6 |  |  |
| JACK |  | U81C | B4 | U249D | D3 | U389C | H4 |  |  |
|  |  | U81D | B4 | U251A | F5 | U389D | D6 |  |  |
| J43 | F6 | 489 | B2 | U251B | E4 | U391A | c3 |  |  |
| J45 | D1 | U91A | C2 | U261B | F4 | U391C | F6 |  |  |
|  | E1 | U91B | B4 | U261C | E4 | U391D | B5 |  |  |
|  | F1 | U91C | G5 | U269 | E5 | U391E | F6 |  |  |
| J47 | G1 | U101A | E4 | U271A | C2 | U481A | F4 |  |  |
|  | H1 | U101B | D5 | U271B | E5 | U481B | F4 |  |  |
| J48 | D6 | U101C | D5 | U271C | C2 |  |  |  |  |
| TRANSISTOR |  | U101D | G1 | U271D | C2 |  |  |  |  |
| 0401 | D5 | U101E | D5 | U279 | B3 |  |  |  |  |
| 0402 | D5 | U101F | D4 | U281A | B2 |  |  |  |  |
| 0403 | D5 | U109 | H3 | U281B | B2 |  |  |  |  |
|  |  | U129 | E3 | U289A | B2 |  |  |  |  |
| RESISTOR |  | U131 | E3 | U289B | B3 |  |  |  |  |
| R71 | A5 | U139A | G3 | U289C | B3 |  |  |  |  |
| R75 | C2 | U139B | F1 | U289D | B3 |  |  |  |  |
| R91 | G5 | U139C | F3 | U291A | B3 | SEMICONDUCTOR INFORMATION |  |  |  |
| R159 | A4 | U139D | G6 | U291B | B3 |  |  |  |  |
| R190 | A5 | U139E | F3 | U301A | H2 | NUMBER | VCC | UNUSED |  |
| R335 | A6 | U139F | G4 | U301B | H2 |  |  | GND | PINS |
| R391 | C3 | U141A | F4 | U301C | H2 | 7400 | 14 |  |  |
| R401 | D5 | U141B | F3 | U301D | H2 | 7402 | 14 |  | LOW |
| R411 | D5 | U141C | E4 | U309A | H2 | 7402 7404 | 14 | 7 |  |
| R412 | C5 | U141D | G4 | U309B | H2 | 7408 | 14 | 7 | HIGH |
| R413 | C4 | U149A | G4 | U309C | H4 | 7410 | 14 | 7 | HIGH |
| R414 | D5 | U149B | F4 | U309D | H 2 H 4 | 7411 | 14 | 7 | HIGH HIGH |
| R415 | D5 | U149C | E4 | U329A | H4 | 7416 | 14 | 7 |  |
| INTEGARTED CIRCUIT |  | U149D | D3 | U329B | C6 | 7420 | 14 | 7 | HIGH |
|  |  | U161A | D4 | U329C | H4 | 7430 | 14 | 7 | HIGH |
| U1 | D2 | U161B | D4 | U329D | H4 |  | 14 |  |  |
| U9A | G2 | U161C | E4 | U331A | G3 | 7432 | 14 | 7 | LOW |
| U9B | D2 | U161D | F4 | U331C | G3 | 7438 | 14 | 7 | HIGH |
| U9D | D1 | U169A | F4 | U3310 | G3 | 7442 | 16 | 11 |  |
| U9E | D2 | U169B | E5 | U339A | G3 | 7473 | 14 | 11 | HIGH HIGH |
| U9G | D2 | U169C | E5 | U339B | F6 | 7474 | 14 | 7 | HIGH |
| U9H | D1 | U169D | E5 | U339C | C4 | 7493 |  | 10 |  |
| U9J | H1 | U171A | F4 | U339D | F5 | 74175 | 16 | 8 | HIGH |
| U9K | F5 | U171B | B2 | U341A | F4 |  |  |  |  |
| U9L | F2 | U171C | C3 | U341B | C4 |  |  |  |  |
| U9M | F4 | U171D | C5 | U349A | H4 |  |  |  |  |
| U9N | F5 | U179A | A5 | U349B | H4 |  |  |  |  |
| U29A | F5 | U179B | C3 | U349C | H4 |  |  |  |  |
| U29B | H2 | U181A | C3 | U349D | H4 |  |  |  |  |
| U29C | C3 | U181B | C1 | U351A | G5 |  |  |  |  |
| U29D | E3 | U181C | B2 | U351B | F6 |  |  |  |  |
| U31A | D5 | U181D | B3 | U351C | F6 |  |  |  |  |
| U31B | D5 | U181E | B4 | U351D | G5 |  |  |  |  |
| U31C | B1 | U181F | E4 | U361A | F5 |  |  |  |  |
| U31D | 15 | U189A | B4 | U361B | D6 |  |  |  |  |
| U31E | H5 | U191A | B4 | U361C | E6 |  |  |  |  |
| U31F | H5 | U191B | B4 | U361D | D6 |  |  |  |  |
| U39A | B5 | U191C | C3 | U369A | E6 |  |  |  |  |
| U39B | E5 | U191D | B4 | U369B | D5 |  |  |  |  |
| U39C | F2 | U201A | B5 | U369C | B3 |  |  |  |  |
| U39D | D3 | U201B | D4 | U369D | E5 |  |  |  |  |



Fig. 6-22. Keyboard interface Card Component Locations 670-2301-04 and below.


| CKT \# | GRID LOC | CKT \# | GRID LOC | CKT \# | GRID LOC | CKT \# | GRID |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CAPACITOR |  | U41B | F3 | U201C | D3 | U369D | E5 |  |  |
|  |  | U41C | E4 | U201D | F5 | U369E | C2 |  |  |
| $\begin{aligned} & \text { C1 } \\ & \text { C40 } \end{aligned}$ | A1 | U41D | F4 | U201E | F5 | U369F | C1 |  |  |
|  | A1 | U49A | D3 | U201F | F5 | U371A | E6 |  |  |
| $\begin{aligned} & \mathrm{C} 40 \\ & \mathrm{C} 90 \end{aligned}$ | A2 | U49D | E4 | U209 | H3 | U371B | E6 |  |  |
| C101 | A2 | U51A | B2 | U229 | G4 | U371C | E6 |  |  |
| C180 | A2 | U51B | F5 | U231A | G2 | U371D | F5 |  |  |
| C189 |  | U51C | G5 | U231B | G3 | U371E | E6 |  |  |
|  | A2 | U51D | D4 | U231C | 15 | U371F | E6 |  |  |
| C350 | A2 | U61A | H2 | U231D | H4 | U379A | C6 |  |  |
| C370 | A3 | U61B | G6 | U239A | H5 | U379C | E6 |  |  |
| C385 |  | U61C | E5 | U239B | G2 | U379D | E5 |  |  |
| C428 | A3 | U61D | E4 | U241A | G5 | U379E | E6 |  |  |
|  | D5 | U69A | G5 | U241B | G3 | U381A | D6 |  |  |
| C429 |  | U69C | G4 | U241C | G4 | U381B | D6 |  |  |
| DIODE |  | U79 | A4 | U249A | C3 | U381C | D6 |  |  |
| CR409 | D5 | U81A | B4 | U249B | G2 | U381D | D6 |  |  |
|  |  | U81B | B4 | U249C | B3 | U389A | C3 |  |  |
| JACK |  | U81C | B4 | U249D | D3 | U389B | C6 |  |  |
| J43 | F6 | U81D | B4 | U251A | F5 | U389C | H4 |  |  |
| J45 | D1 | U89 | B2 | U251B | E4 | U389D | D6 |  |  |
|  | E1 | U91A | C2 | U261B | F4 | U391A | C3 |  |  |
|  | F1 | U91B | B4 | U261C | E4 | U391C | F6 |  |  |
| J47 | G1 | U91C | G5 | U269 | E5 | U391D | B5 |  |  |
|  | H1 | U101A | E4 | U271A | C2 | U391E | F6 |  |  |
| J48 | D6 | U101B | D5 | U271B | E5 | U481A | F4 |  |  |
| RANSISTOR |  | U101C | D5 | U271C | C2 | U481B | F4 |  |  |
|  |  | U101D | G1 | U271D | C2 |  |  |  |  |
| 0401 | D5 | U101E | D5 | U279 | B3 |  |  |  |  |
| 0402 | D5 | U101F | D4 | U281A | B2 |  |  |  |  |
| 0403 | D5 | U109 | H3 | U281B | B2 |  |  |  |  |
| RESISTOR |  | U129 | E3 | U289A | B2 |  |  |  |  |
|  |  | U131 | E3 | U289B | B3 |  |  |  |  |
| R71 | A5 | U139A | G3 | U289C | B3 |  |  |  |  |
| R75 | C2 | U139B | F1 | U289D | B3 |  |  |  |  |
| R91 | G5 | U139C | F3 | U291A | B3 |  |  |  |  |
| R190 | A4 | U139D | G6 | U291B | B3 | SEMICONDUCTOR INFORMATION |  |  |  |
|  | A5 | U139E | F3 | U301A | H2 |  |  |  |  |
| R335 | A6 | U139F | G4 | U301B | H2 | NUMBER | VCC | GND | UNUSED <br> PINS |
| R391 | C3 | U141A | F4 | U301C | H2 |  | Vcc | GND |  |
| R401 D5 |  | U141B | F3 | U301D | H2 | 7400 | 14 | 7 | HIGH |
| R411 D5 |  | U141C | E4 | U309A | H2 | 7402 | 14 | 7 | LOW |
| R412 C5 |  | U141D | G4 | U309B | H2 | 7404 | 14 | 7 |  |
| R413 C4 |  | U149A | G4 | U309C | H4 | 7408 | 14 | 7 | HIGH |
| R414 D5 |  | U149B | F4 | U309D | H2 | 7410 | 14 | 7 | HIGH |
| R415 D5 |  | U149C | E4 | U329A | H4 | 7411 | 14 | 7 | HIGH |
| INTEGRATED CIRCUIT |  | U149D | D3 | U329B | C6 | 7416 | 14 | 7 |  |
|  | D2 | U161A | D4 | U329C | H4 | 7420 | 14 | 7 | HIGH |
| U9A | G2 | U161B | D4 | U329D | H4 | 7430 | 14 | 7 | HIGH |
| U9B | D2 | U161C | E4 | U331A | G3 | 7432 | 14 | 7 | LOW |
| U9D | D1 | U161D | F4 | U331B | F3 | 7438 | 14 | 7 | HIGH |
|  | D2 | U169A | F4 | U331C | G3 | 7442 | 16 | 8 |  |
| U9E | D2 | U169B | E5 | U331D | G3 | 7473 | 4 | 11 | HIGH |
| U9H | D1 | U169C | E5 | U339A | G3 | 7474 | 14 | 7 | HIGH |
|  | H1 | U169D | E5 | U339B | F6 | 7493 | 5 | 10 | LOW |
| U9J | F5 | U171A | F4 | U339C | C4 | 74175 | 16 | 8 | HIGH |
|  | F2 | U171B | B2 | U339D | F5 |  |  |  |  |
| U9M | F4 | U171C | C3 | U341A | F4 |  |  |  |  |
| U9N | F5 | U171D | C5 | U341B | C4 |  |  |  |  |
| U29A | F5 | U179A | A5 | U349A | H4 |  |  |  |  |
| U29B | H2 | U179B | C3 | U349B | H4 |  |  |  |  |
| U29C | C3 | U181A | C3 | U349C | H4 |  |  |  |  |
| U29D | E3 | U181B | C1 | U349D | H4 |  |  |  |  |
| U31A | D5 | U181C | B2 | U351A | G5 |  |  |  |  |
| U31B | D5 | U181E | B3 | U351B | F6 |  |  |  |  |
| U31C | B1 | U181F | E4 | U351C | F6 |  |  |  |  |
| U31D | 15 | U189A | B4 | U361A | F5 |  |  |  |  |
| U31E | H5 | U191A | B4 | U361B | D6 |  |  |  |  |
| U31F | H5 | U191B | B4 | U361C | E6 |  |  |  |  |
| U39A | B5 | U191C | C3 | U361D | D6 |  |  |  |  |
| U39B | E5 | U191D | B4 | U369A | E6 |  |  |  |  |
| U39C | F2 |  |  | U369B | D5 |  |  |  |  |
| $\begin{aligned} & \text { U39D } \\ & \text { U41A } \end{aligned}$ | D3 |  | D4 | U369C | B3 |  |  |  |  |
|  | C4 | U201B | D4 |  |  |  |  |  |  |



Fig. 6-22. Keyboard interface Card Component Locations 670-2301-04 and below.






Fig. 6-24. Control Card Component Locations.
number
7400





Fig. 6-30. Edit Card Component Locations.


Fig, G:28. RAM Card Component Locations




CKT \# GRIO Lo
RESISTOR





## REPLACEABLE MECHANICAL PARTS

## PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

## SPECIAL NOTES AND SYMBOLS

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\begin{array}{ll}
\text { X000 } & \text { Part first added at this serial number } \\
00 X & \text { Part removed after this serial number }
\end{array}
$$

FIGURE AND INDEX NUMBERS
Items in this section are referenced by figure and index numbers to the illustrations.

## INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.
$12345 \quad$ Name \& Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
$\qquad$
Parts of Detail Part
Attaching parts for Parts of Detail Part

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol-- * -- - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

## ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

| " | INCH | ELCTRN | ELECTRON | IN | INCH | SE | SINGLE END |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \# | NUMBER SIZE | ELEC | ELECTRICAL | INCAND | INCANDESCENT | SECT | SECTION |
| ACTR | ACTUATOR | ELCTLT | ELECTROLYTIC | INSUL | INSULATOR | SEMICOND | SEMICONDUCTOR |
| ADPTR | ADAPTER | ELEM | ELEMENT | 1NTL | INTERNAL | SHLD | SHIELD |
| ALIGN | ALIGNMENT | EPL | ELECTRICAL PARTS LIST | LPHLDR | LAMPHOLDER | SHLDR | SHOULDERED |
| AL | ALUMINUM | EQPT | EQUIPMENT | MACH | MACHINE | SKT | SOCKET |
| ASSEM | ASSEMBLED | EXT | EXTERNAL | MECH | MECHANICAL | SL | SLIDE |
| ASSY | ASSEMBLY | FIL | FILLISTER HEAD | MTG | MOUNTING | SLFLKG | SELF-LOCKING |
| ATTEN | ATTENUATOR | FLEX | FLEXIBLE | NIP | NIPPLE | SLVG | SLEEVING |
| AWG | AMERICAN WIRE GAGE | FLH | FLAT HEAD | NON WIRE | NOT WIRE WOUND | SPR | SPRING |
| BD | BOARD | FLTR | FILTER | OBD | ORDER BY DESCRIPTION | SQ | SQUARE |
| BRKT | BRACKET | FR | FRAME or FRONT | OD | OUTSIDE DIAMETER | SST | STAINLESS STEEL |
| BRS | BRASS | FSTNR | FASTENER | OVH | OVAL HEAD | STL | STEEL |
| BRZ | BRONZE | FT | FOOT | PH BRZ | PHOSPHOR BRONZE | SW | SWITCH |
| BSHG | BUSHING | FXD | FIXED | PL | PLAIN or PLATE | T | TUBE |
| CAB | CABINET | GSKT | GASKET | PLSTC | PLASTIC | TERM | TERMINAL |
| CAP | CAPACITOR | HDL | HANDLE | PN | PART NUMBER | THD | THREAD |
| CER | CERAMIC | HEX | HEXAGON | PNH | PAN HEAD | THK | THICK |
| CHAS | CHASSIS | HEX HD | HEXAGONAL HEAD | PWR | POWER | TNSN | TENSION |
| CKT | CIRCUIT | HEX SOC | HEXAGONAL SOCKET | RCPT | RECEPTACLE | TPG | TAPPING |
| COMP | COMPOSITION | HLCPS | HELICAL COMPRESSION | RES | RESISTOR | TRH | TRUSS HEAD |
| CONN | CONNECTOR | HLEXT | HELICAL EXTENSION | RGD | RIGID | $V$ | VOLTAGE |
| COV | COVER | HV | HIGH VOLTAGE | RLF | RELIEF | VAR | VARIABLE |
| CPLG | COUPLING | IC | INTEGRATED CIRCUIT | RTNR | RETAINER | W/ | WITH |
| CRT | CATHODE RAY TUBE | ID | INSIDE DIAMETER | SCH | SOCKET HEAD | WSHR | WASHER |
| DEG | DEGREE | IDENT | IDENTIFICATION | SCOPE | OSCILLOSCOPE | XFMR | TRANSFORMER |
| DWR | DRAWER | IMPLR | IMPELLER | SCR | SCREW | XSTR | TRANSISTOR |


| Mfr. Code | Manufacturer | Address | City, State, Zip |
| :---: | :---: | :---: | :---: |
| 0008k | STAUFFER SUPPLY | 105 SE TAYLOR | PORTLAND, OR 97214 |
| 000CL | TWENTIETH CENTURY PLASTICS | 3628 CRENCHAW BLVD. | LOS ANGELES, CA 90016 |
| 000GG | BALL ELEC DISPLAY DIV. | 1610 P. DELL AVE. | CAMPBELL, CA 95008 |
| 00779 | AMP, INC. | P.O. BOX 3608 | HARRISBURG, PA 17105 |
| 01963 | CHERRY ELECTRICAL PRODUCTS CORPORATION | 3600 SUNSET AVENUE | WAUKEGAN, IL 60085 |
| 02107 | SPARTA MANUFACTURING COMPANY | ROUTE NO. 2, BOX 128 | DOVER, OH 44622 |
| 03614 | BUSSMAN MFG., DIV. OF MCGRAW EDISON CO. | 502 EARTH CITY PLAZA | EARTH CITY, MO 63045 |
| 04713 | MOTOROLA, INC., SEMICONDUCTOR PROD. DIV. | 5005 E MCDOWELL RD,PO BOX 20923 | PHOENIX, AZ 85036 |
| 05574 | VIKING INDUSTRIES, INC. | 21001 NORDHOFF STREET | CHATSWORTH, CA 91311 |
| 05820 | WAKEFIELD ENGINEERING, INC. | AUDUBON ROAD | WAKEFIELD, MA 01880 |
| 06383 | PANDUIT CORPORATION | 17301 RIDGELAND | TINLEY PARK, IL 60477 |
| 06915 | RICHCO PLASTIC CO. | 5825 N. TRIPP AVE. | CHICAGO, IL 60646 |
| 07109 | OAKTRON INDUSTRIES, INC. | 704 30TH STREET | MONROE, WI 53566 |
| 08261 | SPECTRA-STRIP CORP. | 7100 LAMPSON AVE. | GARDEN GROVE, CA 92642 |
| 10389 | CHICAGO SWITCH, INC. | 2035 WABANSIA AVE. | CHICAGO, IL 60647 |
| 12327 | FREEWAY CORPORATION | 9301 ALLEN DRIVE | CLEVELAND, OH 44125 |
| 12881 | metex Corporation | 970 NEW DURHAM ROAD | EDISON, NJ 08817 |
| 13150 | VERNITRON ELECTRICAL COMPONENTS, |  |  |
|  | BEAU PRODUCTS DIVISION | P O Box 10 | LACONIA, NH 03246 |
| 13993 | BALL BROTHERS RESEARCH CORPORATION | BOULDER INDUSTRIAL PARK | BOULDER, CO 80302 |
| 22526 | BERG ELECTRONICS, INC. | YOUK EXPRESSWAY | NEW CUMBERLAND, PA 17070 |
| 22753 | U. I. D. ELECTRONICS CORP. | 4105 PEMBROKE RD. | HOLLYWOOD, FL 33021 |
| 24931 | SPECIALITY CONNECTOR CO., INC. | 2620 ENDRESS PLACE | GREENWOOD, IN 46142 |
| 28520 | HEYMAN MFG. CO. | 147 N. MICHIGAN AVE. | KENILWORTH, NJ 07033 |
| 31781 | EDAC INC. | 20 RAILSIDE RD. | DON MILLS, ONT, CANADA M3A 1 |
| 52833 | KEYTRONIC CORP., OCR DIV. | SPOKANE INDUSTRIAL PK., <br> P. O. BOX 14687 | SPOKANE, WA 99214 |
| 70276 | ALLEN MFG. CO. | P. O. DRAWER 570 | HARTFORD, CT 06101 |
| 70485 | ATLANTIC INDIA RUBBER WORKS, INC. | 571 W. POLK ST. | CHICAGO, IL 60607 |
| 71400 | BUSSMAN MFG., DIVISION OF MCGRAW- |  |  |
|  | EDISON CO. | 2536 W. UNIVERSITY ST. | ST. LOUIS, MO 63107 |
| 71468 | ITT CANNON ELECTRIC | 666 E. DYER RD. | SANTA ANA, CA 92702 |
| 71785 | TRW, CINCH CONNECTORS | 1501 MORSE AVENUE | ELK GROVE VILLAGE, IL 60007 |
| 73743 | FISCHER SPECIAL MFG. CO. | 446 MORGAN ST. | CINCINNATI, OH 45206 |
| 75915 | LITTELFUSE, INC. | 800 E. NORTHWEST HWY | DES PLAINES, IL 60016 |
| 76854 | OAK INDUSTRIES, INC., SWITCH DIV. | S. MAIN ST. | CRYSTAL LAKE, IL 60014 |
| 77250 | PHEOLL MANUFACTURING CO., DIVISION |  |  |
|  | OF ALLIED PRODUCTS CORP. | 5700 W. ROOSEVELT RD. | CHICAGO, IL 60650 |
| 78189 | ILLINOIS TOOL WORKS, INC. |  |  |
| 79963 | SHAKEPROOF DIVISION | ST. CHARLES ROAD | ELGIN, IL 60120 |
| 80009 | ZIERICK MFG. CO. | RADIO CIRCLE P O BOX 500 | MEAVERTON, OR 97077 |
| 83385 | CENTRAL SCREW CO. | 2530 CRESCENT DR. | BROADVIEW, IL 60153 |
| 86928 | SEASTROM MFG. COMPANY, INC. | 701 SONORA AVENUE | GLENDALE, CA 91201 |
| 88245 | LITTON SYSTEMS, INC., USECO DIV. | 13536 SATICOY ST. | VAN NUYS, CA 91409 |
| 91836 | KINGS ELECTRONICS CO., INC. | 40 MARBLEDALE ROAD | TUCKAHOE, NY 10707 |
| 93907 | TEXTRON INC. CAMCAR DIV | 600 18TH AVE | ROCKFORD, IL 61101 |
| 95987 | WECKESSER CO., INC. | 4444 WEST IRVING PARK RD. | CHICAGO, IL 60641 |
| 98278 | MALCO A MICRODOT COMPANY, INC. CONNECTOR AND CABLEDIVISION | 220 PASADENA AVE | SOUTH PASADENA CA 91030 |
| S3629 | PANEL COMPONENTS CORP. | 2015 SECOND ST. | BERKELEY, CA 94170 |


| Fig. \& |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| No. | Part No. | Eff | Dscont | Qty | $12345 \quad$ Name \& Description | Code | Mfr Part Number |
| 1-1 | 390-0340-01 | $\begin{aligned} & \text { B010100 } \\ & \text { B050000 } \end{aligned}$ | B049999 | 1 | COVER,TERMINAL:TOP | 80009 | 390-0340-01 |
|  | 390-0340-06 |  |  | 1 | COVER,SCOPE:TAN | 80009 | 390-0340-06 |
|  |  |  |  |  | *...........(ATTACHING PARTS).......... |  |  |
| -2 | 212-0111-00 |  |  | 4 | SCREW,MACHINE:8-32 $\times 0.25$ INCH,PNH STL ..........*(END ATTACHING PARTS)**......* | 83385 | ORD BY DESCR |
| -3 | 426-0928-01 |  |  | 1 | FRAME,TRIM:GRAY PLASTIC .............*(ATTACHING PARTS)............ | 80009 | 426-0928-01 |
| -4 | 213-0088-00 |  |  | 1 | SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL .........***(END ATTACHING PARTS)**.....** | 83385 | ORD BY DESCR |
| -5 | 334-1555-00 |  |  | 4 | PLATE,IDENT:TRADEMARK | 80009 | 334-1555-00 |
| -6 | 331-0326-01 |  |  | 1 | MASK,CRT SCALE: <br> ...............(ATTACHING PARTS)........... | 80009 | 331-0326-01 |
| -7 | 211-0581-00 |  |  | 4 | SCREW,MACHINE:6-32 $\times 0.375$ INCH,TRH STL *............(END ATTACHING PARTS)*........ | 83385 | ORD BY DESCR |
| -8 | 334-2033-00 |  |  | 1 | PLATE,IDENT: | 80009 | 334-2033-00 |
| -9 | 386-2707-01 | B010100 | B049999 | 1 | PANEL,KEYBOARD: | 80009 | 386-2707-01 |
|  | 386-2707-02 | B050000 |  | 1 | PANEL,KEYBOARD: | 80009 | 386-2707-02 |
|  |  |  |  |  | *..........**(ATTACHING PARTS)*........* |  |  |
| -10 | 212-0001-00 |  |  | 3 | SCREW,MACHINE:8-32 $\times 0.250 \mathrm{INCH}, \mathrm{PNH}$ STL | 77250 | ORD BY DESCR |
| -11 | 211-0537-00 |  |  | 3 | SCREW,MACHINE: $6-32 \times 0.375 \mathrm{INCH}$, TRH STL | 83385 | ORD BY DESCR |
| -12 | 211-0517-00 |  |  | 8 | SCREW,MACHINE:6-32 X 1 INCH,PNH,STL .............(END ATTACHING PARTS)*........ | 83385 | ORD BY DESCR |
| -13 | 337-1882-00 |  |  | 1 | SHIELD,ELEC:POWER SWITCH <br> *.......*****(ATTACHING PARTS) *.....***** | 80009 | 337-1882-00 |
| -14 | 211-0504-00 |  |  | 1 | SCREW,MACHINE: $6-32 \times 0.25$ INCH,PNH STL ********(END ATTACHING PARTS)****** | 83385 | ORD BY DESCR |
| -15 | 260-1334-00 |  |  | 4 | SWITCH,ROCKER:SPDT,0.5A,125VAC <br> *(ATTACHING PARTS)*.......... | 22753 | RSW-412 |
| -16 | 210-0406-00 |  |  | 8 | NUT,PLAIN,HEX.:4-40 0.188 INCH,BRS | 73743 | 12161-50 |
| -17 | 210-0004-00 |  |  | 8 | WASHER,LOCK:\#4 INTL,0.015 THK,STL CD PL | 000BK | ORD BY DESCR |
| -18 | 166-0024-00 |  |  | 8 |  | 76854 | 3-5116-314 |
| -19 | ---------- |  |  | 1 | LAMP,CARTRIDGE:(SEE DS1125 REPL) |  |  |
| -20 | -- |  |  | 3 | LAMP,LED:(SEE CR1120,CR1122,CR1124 REPL) |  |  |
| -21 | 131-0775-00 |  |  | 1 | CONTACT,ELEC:HEX,0.25 INCH W/6-32 1 END | 88245 | 1601-A |
| -22 | ------ |  |  | 1 | KEYBOARD ASSY:(SEE A11 REPL) |  |  |
| -23 | 366-1555-00 |  |  | 1 | .PUSH BUTTON SET:GRAY,KEYBOARD | 52833 | ORD BY DESCR |
|  | 366-1555-01 |  |  | 1 | ..PUSH BUTTON SET:A THRU $Z$ | 52833 | GLWW010199000101 |
|  | 366-1555-02 |  |  | 1 | ...PUSH BUTTON:MARKED "A" | 52833 | GLWW0101A0010101 |
|  | 366-1555-03 |  |  | 1 | ...PUSH BUTTON:MARKED "B" | 52833 | GLWW0101B0010101 |
|  | 366-1555-04 |  |  | 1 | ...PUSH BUTTON:MARKED "C" | 52833 | GLWW0101C0010101 |
|  | 366-1555-05 |  |  | 1 | ...PUSH BUTTON:MARKED "D" | 52833 | GLWW0101D0010101 |
|  | 366-1555-06 |  |  | 1 | ...PUSH BUTTON:MARKED "E" | 52833 | GLWW0101E0010101 |
|  | 366-1555-07 |  |  | 1 | ...PUSH BUTTON:MARKED "F" | 52833 | GLWW0101F0010101 |
|  | 366-1555-08 |  |  | 1 | ...PUSH BUTTON:MARKED "G" | 52833 | GLWW0101G0010101 |
|  | 366-1555-09 |  |  | 1 | ...PUSH BUTTON:MARKED " ${ }^{\text {" }}$ | 52833 | GLWW0101H0010101 |
|  | 366-1555-10 |  |  | 1 | ...PUSH BUTTON:MARKED " 1 " | 52833 | GLWW010110010101 |
|  | 366-1555-11 |  |  | 1 | ...PUSH BUTTON:MARKED "J" | 52833 | GLWW0101J0010101 |
|  | 366-1555-12 |  |  | 1 | ...PUSH BUTTON:MARKED "K" | 52833 | GLWW0101K0010101 |
|  | 366-1555-13 |  |  | 1 | ...PUSH BUTTON:MARKED "L" | 52833 | GLWW0101L0010101 |
|  | 366-1555-14 |  |  | 1 | ...PUSH BUTTON:MARKED "M" | 52833 | GLWW0101M0010101 |
|  | 366-1555-15 |  |  | 1 | ...PUSH BUTTON:MARKED "N" | 52833 | GLWW0101N0010101 |
|  | 366-1555-16 |  |  | 1 | ...PUSH BUTTON:MARKED "O" | 52833 | GLWW010100010101 |
|  | 366-1555-17 |  |  | 1 | ...PUSH BUTTON:MARKED "P" | 52833 | GLWW0101P0010101 |
|  | 366-1555-18 |  |  | 1 | ...PUSH BUTTON:MARKED "Q" | 52833 | GLWW0101Q0010101 |
|  | 366-1555-19 |  |  | 1 | ...PUSH BUTTON:MARKED "R" | 52833 | GLWW0101R0010101 |
|  | 366-1555-20 |  |  | 1 | ...PUSH BUTTON:MARKED "S" | 52833 | GLWW0101S0010101 |
|  | 366-1555-21 |  |  | 1 | ...PUSH BUTTON:MARKED "T" | 52833 | GLWW0101T0010101 |
|  | 366-1555-22 |  |  | 1 | ...PUSH BUTTON:MARKED "U" | 52833 | GLWW0101U0010101 |
|  | 366-1555-23 |  |  | 1 | ...PUSH BUTTON:MARKED "V" | 52833 | GLWW01010000V001 |
|  | 366-1555-24 |  |  | 1 | ...PUSH BUTTON:MARKED "W" | 52833 | GLWW0101W0010101 |
|  | 366-1555-25 |  |  | 1 | ...PUSH BUTTON:MARKED "X" | 52833 | GLWW0101X0010101 |
|  | 366-1555-26 |  |  | 1 | ...PUSH BUTTON:MARKED "Y" | 52833 | GLWW0101Y0010101 |
|  | 366-1555-27 |  |  | 1 | ...PUSH BUTTON:MARKED "Z" | 52833 | GLWW010120010101 |

Fig. \&

| Index <br> No. | Tektronix <br> Part No. | Serial/Mo Eff | el No. | Qty | 12345 Name \& Description | Mfr <br> Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1. | 366-1555-28 |  |  | 1 | ..PUSH BUTTON SET: 1 THRU 9 | 52833 | GLWW010199020801 |
|  | 366-1555-29 |  |  | 1 | ..PUSH BUTTON:MARKED ZERO | 52833 | GLWW010110100101 |
|  | 366-1555-30 |  |  | 1 | ..PUSH BUTTON:GRAY,*/: | 52833 | GLWW010117720802 |
|  | 366-1555-31 |  |  | 1 | ...PUSH BUTTON:MARKED EQUAL OVER MINUS | 52833 | GLWW010110380802 |
|  | 366-1555-32 |  |  | 1 | ..PUSH BUTTON:MARKED + OVER SEMI-COLON | 52833 | GLWW010110370802 |
|  | 366-1555-33 |  |  | 1 | ..PUSH BUTTON:MARKED LESS THAN OVER COMMA | 52833 | GLWW010110340802 |
|  | 366-1555-34 |  |  | 1 | ...PUSH BUTTON:MKD GREATER THAN OVER PERIO | 52833 | GLWW010110350802 |
|  | 366-1555-35 |  |  | 1 | ..PUSH BUTTON:MKD ? OVER / | 52833 | GLWW010110140802 |
|  | 366-1555-36 |  |  | 1 | ..PUSH BUTTON:GRAY,PAGE/ERASE/INPUT | 52833 | GGW0101P3621201 |
|  | 366-1555-37 |  |  | 1 | ..PUSH BUTTON:MKD L BRACE OVER L BRACKET | 52833 | GGWW010110850802 |
|  | 366-1555-38 |  |  | 1 | ..PUSH BUTTON:MARKED ESC | 52833 | GGWW0101E3890701 |
|  | 366-1555-39 |  |  | 1 | ..PUSH BUTTON:MARKED TILDE OVER CARET | 52833 | GGWW010110640802 |
|  | 366-1555-40 |  |  | 1 | ..PUSH BUTTON:MARKED TAB | 52833 | GGWW0101T5990701 |
|  | 366-1555-41 |  |  | 1 | ..PUSH BUTTON:MARKED CTRL | 52833 | GGWW0101C3560701 |
|  | 366-1555-42 |  |  | 1 | ..PUSH BUTTON:MARKED TTY LOCK | 52833 | GGWW0101T4931101 |
|  | 366-1555-43 |  |  | 1 | ..PUSH BUTTON:MARKED SHIFT | 52833 | GGWW0203S5770701 |
|  | 366-1555-44 |  |  | 1 | ..PUSH BUTTON:MKD R BRACE OVER R BRACKET | 52833 | GGWW010110860802 |
|  | 366-1555-45 |  |  | 1 | ..PUSH BUTTON:MARKED BACK SPACE | 52833 | GGWW0101B3211101 |
|  | 366-1555-46 |  |  | 1 | ..PUSH BUTTON:MARKED GRAVE ACCENT OVER AT | 52833 | GGWW010110790802 |
|  | 366-1555-47 |  |  | 1 | ..PUSH BUTTON:MARKED LF | 52833 | GGWW0101L4780701 |
|  | 366-1555-48 |  |  | 1 | ...PUSH BUTTON:MKD VERT DSH OV BACK SLASH | 52833 | GGWW010110870802 |
|  | 366-1555-49 |  |  | 1 | ..PUSH BUTTON:MARKED RUB OUT | 52833 | GGWW2502R4431101 |
|  | 366-1555-50 |  |  | 1 | ..PUSH BUTTON:MARKED BREAK | 52833 | GGWW010183310701 |
|  | 366-1555-51 |  |  | 1 | ..PUSH BUTTON:GRAY RETURN | 52833 | GGWW0905R4450701 |
|  | 366-1555-52 |  |  | 1 | ..PUSH BUTTON:MARKED SHIFT | 52833 | BBWW020255770701 |
|  | 366-1555-53 |  |  | 1 | ..PUSH BUTTON:GRAY,SPACE BAR | 52833 | GGWW120110900000 |
|  | 366-1555-54 |  |  | 1 | ..PUSH BUTTON:GRAY,ERASE TO END/8 | 52833 | GGW0101E2051205 |
|  | 366-1555-55 |  |  | 1 | ..PUSH BUTTON:GRAY,COPY/9 | 52833 | GGWW0101R3770704 |
|  | 366-1555-56 |  |  | 1 | ..PUSH BUTTON:GRAY,RESET/7 | 52833 | GGWW0101C0930704 |
|  | 366-1555-57 |  |  | 1 | ..PUSH BUTTON: | 52833 | GGWW010113771108 |
|  | 366-1555-58 |  |  | 1 | ..PUSH BUTTON:GRAY,ARROW UP/5 | 52833 | GGWW010139050107 |
|  | 366-1555-59 |  |  | 1 | ...PUSH BUTTON:GRAY,DEL L/DEL C/6 | 52833 | GGWW0101D2531108 |
|  | 366-1555-60 |  |  | 1 | ..PUSH BUTTON:GRAY,ARROW LEFT/1 | 52833 | GLWW010139210107 |
|  | 366-1555-61 |  |  | 1 | ..PUSH BUTTON:GRAY,HOME/2 | 52833 | GGWW0101H4690704 |
|  | 366-1555-62 |  |  | 1 | ..PUSH BUTTON:GRAY,SEND ENTER/. | 52833 | GGWW0101S3541108 |
|  | 366-1555-63 |  |  | 1 | ..PUSH BUTTON:GRAY,ARROW DOWN/0 | 52833 | GLWW010139000107 |
|  | 366-1555-64 |  |  | 1 | ..PUSH BUTTON:GRAY,NUM LOCK | 52833 | GGWW0101N5101101 |
|  | 366-1555-65 |  |  | 1 | ..PUSH BUTTON:GRAY,ARROW RIGHT/3 | 52833 | GLWW010139030107 |
| -24 | 118-0031-00 |  |  | 2 | .ACTUATOR ASSY:90Z SGL UNIT,W/MECH ALT ACT | 52833 | 61-0261-09 |
| -25 | 118-0043-00 |  |  | 2 | .ACTUATOR ASSY:SINGLE UNIT | 52833 | 61-0021-03 |
|  | 260-1507-00 |  |  | 72 | .SWITCH,REED:SPST | 52833 | 60-0003-01 |
| -26 | 136-0156-01 |  |  | 1 | CONNECTOR,RCPT,:22/44 PIN,CHASSIS MOUNT | 05574 | 2VH22-1AN5 |
| -27 | 214-0702-00 |  |  | 2 | KEY,CONN PLZN:CKT BD CONN,T SHAPED | 80009 | 214-0702-00 |
| -28 | 200-1476-01 | B010100 | B049999 | 1 | COVER,KEYBOARD:LOWER,PAINTED | 80009 | 200-1476-01 |
|  | 200-1476-02 | B050000 |  | 1 | COVER,KEYBOARD: <br> ..............(ATTACHING PARTS) ${ }^{*+\cdots . . . . . . . . . ~}$ | 80009 | 200-1476-02 |
| -29 | 211-0504-00 |  |  | 3 | SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL **********(END ATTACHING PARTS)******** | 83385 | ORD BY DESCR |
|  | 348-0507-00 | B050000 |  | FT | SHLD GSKT,ELEK:MESH TYPE, $0.25 \times 0.14$ | 12881 | 01-604-1756 |
|  | 407-1865-00 | 8050000 |  | 1 | BRACKET,GASKET:RIGHT,ALUMINUM | 80009 | 407-1865-00 |
|  | 407-1864-00 |  |  | 1 | BRACKET,GASKET:LEFT,ALUMINUM <br> ............"(ATTACHING PARTS)........... | 80009 | 407-1864-00 |
|  | 210-0586-00 | B050000 |  | 2 | NUT,PL,ASSEM WA:4-40 X 0.25,STL **********(END ATTACHING PARTS)******* | 83385 | ORD BY DESCR |
| -30 | 381-0338-00 |  |  | 1 | BAR MOUNTING:VARIABLE RESISTOR,ALUMINUM ..............(ATTACHING PARTS)**........ | 80009 | 381-0338-00 |
| -31 | 211-0507-00 |  |  | 2 | SCREW,MACHINE: $6-32 \times 0.312 \mathrm{INCH}, \mathrm{PNH}$ STL | 83385 | ORD BY DESCR |
| -32 | 366-0128-01 |  |  | 2 | KNOB:THUMBWHEEL | 80009 | 366-0128-01 |
|  | 213-0140-00 |  |  | 2 | .SETSCREW:2-56 $\times 0.94$ INCH,HEX SOC ST | 70276 | ORD BY DESCR |
| -33 | --------- |  |  | 2 | RES.,VAR:(SEE R1140,R1145 REPL) <br> ............*(ATTACHING PARTS) ${ }^{*}$......... |  |  |
| -34 | 210-0583-00 |  |  | 2 | NUT,PLAIN,HEX: $0.25-32 \times 0.312 \mathrm{INCH}, \mathrm{BRS}$ | 73743 | 2x20317-402 |
| -35 | 210-0046-00 |  |  | 2 | WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS | 78189 | 1214-05-00-0541C |



Fig. \&


Fig. \&


Fig. \&

| Index No. | Tektronix <br> Part No. | Serial/Model No. <br> Eff Dscont | Qty | $12345 \quad$ Name \& Description | Mfr <br> Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2-55 | ---------- |  | 1 | TRANSISTOR:(SEE Q1112 REPL) <br> *********(ATTACHING PARTS)* |  |  |
| -56 | 211-0513-00 |  | 2 | SCREW,MACHINE:6-32 $\times 0.625$ INCH,PNH STL | 83385 | ORD BY DESCR |
| -57 | 210-0407-00 |  | 1 | NUT,PLAIN,HEX.: 6-32 $\times 0.25 \mathrm{INCH}, \mathrm{BRS}$ | 73743 | 3038-0228-402 |
| -58 | 210-0457-00 |  | 1 | NUT,PL,ASSEM WA:6-32 $\times 0.312$, STL CD PL | 83385 | ORD BY DESCR |
| -59 | 210-0202-00 |  | , | TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED | 78189 | 2104-06-00-2520N |
| -60 | 210-0803-00 |  | 2 | WASHER,FLAT: $0.15 \mathrm{ID} \times 0.032$ THK, STL CD | 12327 | ORD BY DESCR |
| -61 | 210-0967-00 |  | 2 | WASHER,SHLDR:0.156 ID $\times 0.094 \mathrm{D} \times 0.3750$ | 86928 | 5607-82 |
|  | 210-0910-00 |  | 2 | WASHER,NONMETAL:0.188 ID X $0.313^{\prime \prime}$ OD,TEFLO | 02107 | ORD BY DESCR |
|  |  |  |  | ...........*(END ATTACHING PARTS)**.....* |  |  |
| -62 | 386-0978-00 |  | , | INSULATOR,PLATE:TRANSISTOR,MICA | 80009 | 386-0978-00 |
| -63 | 129-0089-01 |  | 6 | SPACER POST:0.830 L X 0.250,6-32 THD,AL <br> **.........**(ATTACHING PARTS)***....... | 80009 | 129-0089-01 |
| -64 | 211-0581-00 |  | 6 | SCREW,MACHINE:6-32 X 0.375 INCH,TRH STL **********(END ATTACHING PARTS)******** | 83385 | ORD BY DESCR |
| -65 | 214-1781-00 |  | , | HEAT SINK,XSTR:(4) TO-3,AL | 80009 | 214-1781-00 |
| -66 | 343-0469-00 |  | 1 | RETAINER,CKT BD:POLYCARBONATE **********(ATTACHING PARTS) ${ }^{* \ldots * * * * * * * * * * * * *)}$ | 80009 | 343-0469-00 |
| -67 | 211-0507-00 |  | 2 | SCREW,MACHINE:6-32 $\times 0.312 \mathrm{INCH}, \mathrm{PNH}$ STL | 83385 | ORD BY DESCR |
| -68 | 386-2792-00 |  | 1 | PLATE,ALIGNMENT: <br> **********(END ATTACHING PARTS)******** | 80009 | 386-2792-00 |
| -69 | 386-2866-00 |  | 2 | SPRT,CKT BD RET: <br> *.............(ATTACHING PARTS)*.......... | 80009 | 386-2866-00 |
|  | 211-0513-00 |  | 4 | SCREW,MACHINE: $6-32 \times 0.625$ INCH,PNH STL **********(END ATTACHING PARTS)******** | 83385 | ORD BY DESCR |
| -70 | -------- |  | 1 | CKT BOARD ASSY:RAM(SEE A1 REPL) |  |  |
| . 71 | 136-0260-01 |  | 2 | .SOCKET,PLUG-IN:16 CONTACT,RECT SHAPE | 71785 | 133-51-02-075 |
| -72 | 131-0787-00 |  | 15 | .CONTACT,ELEC:0.64 INCH LONG | 22526 | 47359 |
| -73 | --------- |  |  | CKT BOARD ASSY:CURSOR(SEE A2 REPL) |  |  |
| -74 | 131-0787-00 |  | 15 | .CONTACT,ELEC:0.64 INCH LONG | 22526 | 47359 |
| -75 | -------- |  | 1 | CKT BOARD ASSY:KEYBOARD INTFCE(SEE A4 REPL |  |  |
| -76 | 131-0589-00 |  | 21 | .TERMINAL, PIN:0.46 L $\times 0.025$ SQ | 22526 | 48283-029 |
| -77 | 131-0608-00 |  | 14 | .TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD | 22526 | 47357 |
| -78 | 131-0993-00 |  | 3 | .BUS,CONDUCTOR:2 WIRE BLACK | 00779 | 850100-01 |
| -79 | --------- |  | 1 | CKT BOARD ASSY:EDIT(SEE A5 REPL) |  |  |
| -80 | 131-0589-00 |  | 4 | .TERMINAL,PIN:0.46 L $\times 0.025$ SQ | 22526 | 48283-029 |
| -81 | --------- |  |  | CKT BOARD ASSY:CONTROL(SEE A6 REPL) |  |  |
| -82 | 131-0589-00 |  | 3 | .TERMINAL, PIN:0.46 L $\times 0.025$ SQ | 22526 | 48283-029 |
| -83 | 131-0608-00 |  | 22 | .TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD | 22526 | 47357 |
| -84 | 131-0993-00 |  | 7 | .BUS,CONDUCTOR:2 WIRE BLACK | 00779 | 850100-01 |
| -85 | -------- |  | 1 | CKT BOARD ASSY:TIMING(SEE A7 REPL) |  |  |
| -86 | 131-0589-00 |  | 21 | .TERMINAL, PIN:0.46 L $\times 0.025$ SQ | 22526 | 48283-029 |
| -87 | 131-0608-00 |  | 3 | .TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD | 22526 | 47357 |
| -88 | 131-0993-00 |  | 1 | .BUS,CONDUCTOR:2 WIRE BLACK | 00779 | 850100-01 |
| -89 | --------- |  | 1 | CKT BOARD ASSY:MOTHER(SEE A10 REPL) <br> *****......**(ATTACHING PARTS)******** |  |  |
| -90 | 211-0511-00 |  | 6 | SCREW,MACHINE: $6-32 \times 0.500$, PNH,STL,CD PL *............(END ATTACHING PARTS).........* | 83385 | ORD BY DESCR |
|  | - |  | - | .CKT BOARD ASSY INCLUDES: |  |  |
| -91 | 131-0589-00 |  | 33 | .TERMINAL,PIN:0.46 L $\times 0.025$ SQ | 22526 | 48283-029 |
|  | 131-0608-00 |  | 9 | .TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD | 22526 | 47357 |
| -92 | 136-0260-01 |  | 2 | .SOCKET,PLUG-IN:16 CONTACT,RECT SHAPE | 71785 | 133-51-02-075 |
| -93 | 131-1147-00 |  | 9 | .CONNECTOR,RCPT,: 72 PIN | 31781 | 336-072-520-309 |
| -94 | 131-1148-00 |  | 19 | .KEY,CONN PLZN:PLASTIC | 00779 | 67611-6 |
| -95 | 351-0239-00 |  | 1 | GUIDE,CKT BD:MAIN,LEFT \& RIGHT,GRAY PC *.......*****(ATTACHING PARTS)****.....** | 80009 | 351-0239-00 |
| -96 | 210-0457-00 |  | 6 | NUT,PL,ASSEM WA:6-32 x 0.312,STL CD PL $\cdots \cdots \cdots \cdots \cdots$..........nd ATTACHING PARTS)......... | 83385 | ORD BY DESCR |
| -97 | 131-1249-00 |  | 2 | CONTACT,ELEC:QUICK DISCONNECT *............*(ATTACHING PARTS) ${ }^{*}$.......... | 00779 | 41478 |
| -98 | 210-0457-00 |  | 2 | NUT,PL,ASSEM WA:6-32 $\times 0.312, S T L$ CD PL *(END ATTACHING PARTS) | 83385 | ORD BY DESCR |

Fig. \&

| Index <br> No. | Tektronix Part No. | Serial/Mod Eff | Dscont | Qty | 12345 Name \& Description | Mfr <br> Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2-99 | ----- ---- |  |  | 1 | TRANSFORMER:POWER(SEE T1000 REPL) |  |  |
| -100 | 211-0507-00 |  |  | 4 | SCREW,MACHINE: $6-32 \times 0.312 \mathrm{INCH}, \mathrm{PNH}$ STL | 83385 | ORD BY DESCR |
| -101 | 210-0006-00 |  |  | 4 | WASHER,LOCK:\#6 INTL,0.018 THK,STL CD PL | 78189 | 1206-00-00-0541C |
| -102 | 407-1174-00 |  |  | 2 | BRACKET,XFMR:ALUMINUM .........**(END ATTACHING PARTS)******* | 80009 | 407-1174-00 |
| -103 | 131-0775-00 |  |  | 2 | CONTACT,ELEC:HEX,0.25 INCH W/6-32 1 END | 88245 | 1601-A |
| -104 | ---------. |  |  | 1 | TRANSISTOR:(SEE Q1114 REPL) <br> *..........**(ATTACHING PARTS)**......... |  |  |
| -105 | 210-0407-00 |  |  | 1 | NUT,PLAIN,HEX: 6 -32 $\times 0.25$ INCH,BRS | 73743 | 3038-0228-402 |
| -106 | 210-0071-00 |  |  | 1 | ............ (END ATTACHING PARTS)......... |  |  |
| -107 | 342-0136-00 |  |  | 1 | INSULATOR,WSHR:0.812 OD $\times 0.0025$ INCH THK | 04713 | ORD BY DESCR |
| -108 | 210-0202-00 |  |  | 2 | .**********(ATTACHING PARTS)******** |  |  |
| -109 | 210-0586-00 |  |  | 1 | NUT,PL,ASSEM WA:4-40 X 0.25,STL | 83385 | ORD BY DESCR |
| -110 | 210-0851-00 |  |  | 1 | WASHER,FLAT:0.119 ID X 0.375 INCH OD,ST <br> *(END ATTACHING PARTS)****** | 12327 | ORD BY DESCR |
| -111 | ---------- |  |  | 1 | CAPACITOR:(SEE C1006 REPL) ...............(ATTACHING PARTS) ${ }^{*}+\ldots . . .$. |  |  |
| -112 | 211-0511-00 |  |  | 1 | SCREW,MACHINE:6-32 $\times$ 0.500,PNH,STL,CD PL | 83385 | ORD BY DESCR |
| -113 | 210-0457-00 |  |  | 1 | NUT,PL,ASSEM WA:6-32 $\times 0.312, S T L$ CD PL <br> *(END ATTACHING PARTS)******* | 83385 | ORD BY DESCR |
| -114 | 343-0067-01 |  |  | 1 | **(ATTACHING PARTS)****..... |  | 343-0067-01 |
| -115 | 211-0016-00 | B010100 | B064026 | 3 | SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL | 83385 | ORD BY DESCR |
|  | 211-0099-00 | B064027 |  | 3 | SCREW,MACHINE:0.312 FLH, 100 DEG | 83385 | ORD BY DESCR |
| -116 | 210-0851-00 |  |  | 3 | WASHER,FLAT:0.119 ID X 0.375 INCH OD,ST *********(END ATTACHING PARTS)******* | 12327 | ORD BY DESCR |
| -117 | 212-0518-00 |  |  | 2 | SCREW,MACHINE: $10-32 \times 0.312, \mathrm{PNH}, \mathrm{STL}, \mathrm{CD} \mathrm{PL}$ | 83385 | ORD BY DESCR |
| -118 | 210-0273-00 |  |  | 2 | TERMINAL,LUG:0.781 INCH LONG | 79963 | 547 |
| -119 | 348-0004-00 | B010100 | B049999 | 1 | GROMMET,RUBBER:0.281 ID $\times 0.563$ INCH OD | 70485 | 763 |
|  | 348-0063-00 | B050000 |  | 1 | GROMMET,PLASTIC:0.50 INCH DIA | 80009 | 348-0063-00 |
| -120 | 124-0282-00 |  |  | 1 | TERMINAL STRIP,:GROUND | 13150 | 7605-0803-000B |
|  | 210-0203-00 | B050000 |  | 1 | TERMINAL,LUG:SE \#6 <br> ................(ATTACHING PARTS)**......... | **(ATTACHING PARTS)*.........* | 2103-06-00-2520N |
|  | 211-0507-00 | B050000 |  | 1 | SCREW,MACHINE: 6 -32 $\times 0.312 \mathrm{INCH}, \mathrm{PNH}$ STL | 83385 | ORD BY DESCR |
|  | 210-0435-00 | B050000 |  | 1 | NUT,PRESSMOUNT:6-32 $\times 0.344$ OD ...............(END ATTACHING PARTS)*........ | 80009 | 210-0435-00 |
| -121 | 211-0511-00 |  |  | 2 | SCREW,MACHINE:6-32 $\times$ 0.500,PNH,STL,CD PL | 83385 | ORD BY DESCR |
| -122 | 386-2420-01 | B010100 | B049999 | 1 | PANEL,REAR: | 80009 | 386-2420-01 |
|  | 386-2420-03 | B050000 |  | 1 | PANEL,REAR:W/CHASSIS | 80009 | 386-2420-03 |
| -123 | 131-1480-00 | B010100 | B064400 | 2 | LEAD,ELECTRICAL:STRD,22 AWG,3.75 L | 80009 | 131-1480-00 |
|  | 131-1480-01 | B064401 | B064429 | 2 | LEAD,ELECTRICAL:STRD, 22 AWG,3.75 L | 80009 | 131-1480-01 |
|  | 131-1480-02 | B064430 |  | 2 | LEAD,ELECTRICAL:STRD, 22 AWG,3.75 L | 80009 | 131-1480-02 |
| -124 | 179-1091-00 |  |  | 1 | WIRING HARNESS:READOUT | 80009 | 179-1091-00 |
|  | 131-0371-00 |  |  | 12 | .CONTACT,ELEC:FOR NO. 26 AWG WIRE | 98278 | 122-0182-019 |
|  | 179-1947-00 | B010100 | B019999 | 1 | WIRING HARNESS:MONITOR | 80009 | 179-1947-00 |
|  | 179-1947-01 | B020000 | B064429 | 1 | WIRING HARNESS:MONITOR | 80009 | 179-1947-01 |
|  | 179-1947-02 | B064430 |  | 1 | WIRING HARNESS:MONITOR | 80009 | 179-1947-02 |
|  | 179-1944-00 |  |  | 1 | WIRING HARNESS: HEAT SINK NO 1 | 80009 | 179-1944-00 |
| -125 | 131-0621-00 |  |  | 5 | .CONNECTOR,TERM:22-26 AWG,BRS \& CU BE GOLD | 22526 | 46231 |
|  | 131-0792-00 |  |  | 1 | .CONNECTOR,TERM: 18 -20 AWG,CU BE GOLD PL | 22526 | 46221 |
| -126 | 352-0202-00 |  |  | 1 | .HLDR,TERM CONN: 6 WIRE BLACK | 80009 | 352-0202-00 |
|  | 343-0549-00 |  |  | 11 | .STRAP,TIEDOWN:0.091 W $\times 3.62$ INCH LONG | 06383 | PLT1M |
|  | 179-1945-00 |  |  | 1 | WIRING HARNESS: HEAT SINK NO 2 | 80009 | 179-1945-00 |
|  | 131-0621-00 |  |  | 1 | .CONNECTOR,TERM:22-26 AWG,BRS \& CU BE GOLD | 22526 | 46231 |
|  | 131-0792-00 |  |  | 2 | .CONNECTOR,TERM:18-20 AWG,CU BE GOLD PL | 22526 | 46221 |
|  | 334-2192-01 |  |  | 1 | MARKER,IDENT:MKD INT SET FOR 110 V | 80009 | 334-2192-01 |
|  | 334-2193-01 |  |  | 1 | MARKER,IDENT:MKD INT SET FOR 120 V | 80009 | 334-2193-01 |
|  | 334-2194-01 |  |  | 1 | MARKER,IDENT:MKD INT SET FOR 200V | 80009 | 334-2194-01 |
|  | 334-2195-01 |  |  | 1 | MARKER,IDENT:MKD INT SET FOR 220V | 80009 | 334-2195-01 |
|  | 334-2196-01 |  |  | 1 | MARKER,IDENT:MKD INT SET FOR 240V | 80009 | 334-2196-01 |
|  | 334-2558-01 |  |  | 1 | MARKER,IDENT:MARKED 104V,50Hz | 80009 | 334-2558-01 |

Fig. \&

| Index | Tektronix | Serial/Model No. |  |  |  | Mfr |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| No. | Part No. | Eff Dscont | Qty | 12345 | Name \& Description | Code | Mfr Part Number |
| 2 - | 334-2560-01 |  | 1 | MARKER,ID | RKED $110 \mathrm{~V}, 50 \mathrm{HZ}$ | 80009 | 334-2560-01 |
| -127 | 334-2192-01 |  | 1 | MARKER,ID | D INT SET FOR 110 V | 80009 | 334-2192-01 |
|  | 334-2193-01 |  | 1 | MARKER,ID | D INT SET FOR 120 V | 80009 | 334-2193-01 |
|  | 334-2194-01 |  | 1 | MARKER,ID | D INT SET FOR 200 V | 80009 | 334-2194-01 |
|  | 334-2195-01 |  | 1 | MARKER,ID | D INT SET FOR 220 V | 80009 | 334-2195-01 |
|  | 334-2196-01 |  | 1 | MARKER,ID | D INT SET FOR 240V | 80009 | 334-2196-01 |
|  | 334-2558-01 |  | 1 | MARKER,ID | RKED 104V,50Hz | 80009 | 334-2558-01 |
|  | 334-2560-01 |  | 1 | MARKER,ID | RKED $110 \mathrm{~V}, 50 \mathrm{HZ}$ | 80009 | 334-2560-01 |



## ACCESSORIES



| Index <br> No. | Tektronix Part No. | Serial/Model No. Eff Dscont | Qty | 12 | 3 | 5 | Name \& | Description | Mfr <br> Code | Mfr | Part | Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 021-0111-00 |  | 1 | INT | ERFA | CE | C data |  | 80009 | 021 | -0111 | 1-00 |
|  | 070-1613-00 |  | 1 | MAN | UAL, | TE | RVICE |  | 80009 | 070- | -1613 | 3-00 |
|  | 070-1621-00 |  | 1 | MAN | UAL, | TE | SER'S |  | 80009 | 070 | -1621 | 1-00 |


[^0]:    ${ }^{1}$ ASCII Data Link has BIT 8 pulled high on Motherboard.
    ${ }^{2}$ With TTY Port Optional Data Communication Interfaces, BIT 8 can be used for Mark or Space, even or odd parity. With Standard Data Communications Interface asserting SEND 8 causes BIT 8 to be transmitted as received rom the minibus. With SEND 8 not true BIT 8 is used as a mark.
    ${ }^{3}$ As a result of an Enter or Send sequence activated from keyboard or by computer.

[^1]:    ${ }^{4}$ With the exception of Erase Input, the above operations can be performed only from the keyboard.

