Integrated Storage Module

Model 3034

Technical Manual

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v and vi	1
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2-7 through 2-15 (2-16 Blank)	0
3-1 through 3-15 (3-16 Blank)	0
4-1 through 4-39 (4-40 Blank)	0
5-1 through 5-4	0
A-1 through A-8	0
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Title page
Copyright page
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CHAPTER 1

GENERAL DESCRIPTION

1.1 Introduction

The Integrated Storage Module (ISM), Model 3034, is a high density, low power, one megaword (four megabyte) memory module. It is contained on a single 15 by 18 inch printed circuit board therefore occupying only one SelBUS slot in any CONCEPT Computer System. It is a high performance, self-contained memory system. The ISM provides the capability for single-bit error correction and double-bit error reporting. The ISM is designed and manufactured by Gould Inc., Computer Systems Division, Ft. Lauderdale, Florida.

The information in this manual is presented in the following order:

Chapter 1	General Description
Chapter 2	Installation and Operation
Chapter 3	SelBUS Transfers and Operations
Chapter 4	Theory of Operation
Chapter 5	Maintenance

1.2 Features

The significant ISM features are listed below and a brief description of each feature is provided in the paragraphs that follow.

- o Read access time for 600ns to the SelBUS interface
- o Self-contained refresh logic
- o Scrubbing logic
- o Built-in error logger
- o Two deep input buffering
- o 1 Megaword (4 megabyte) storage capacity using 256K DRAMs
- o 4 MW (16MB) addressing capability
- o 64KW (256KB) address recognition boundaries
- o Optional read and lock capability
- o Three module interleaving options
- o Self-contained error correction code (ECC) logic
- o Compatible with existing battery back-up

1.2.1 Read Access Time

Read access time of 600 nanoseconds to the SelBUS Interface is supported. The ISM also provides the following performance capabilities:

- Internal read memory access time of 300 nanoseconds.
- Internal read cycles initiated every 300 nanoseconds.
- Internal write cycles initiated every 300 nanoseconds.
- Internal write halfword or write byte cycles initiated every 600 nanoseconds.

1.2.2 Self-Contained Refresh Logic

A complete refresh cycle is performed every four milliseconds. Each refresh cycle time is 300 nanoseconds.

1.2.3 Self-Contained Scrubbing Logic

Scrubbing logic improves reliability by correcting soft correctable single-bit errors as they occur.

1.2.4 Built-In Error Logger

Nine on-board LEDs make up the error logger. Seven of the LEDs are used for displaying the error correction code (ECC) syndrome bits, and two LEDs are used to display the bank select bits.

1.2.5 Two-Deep Input Buffering

Two-deep input buffering is provided for all cycles except halfword and byte write cycles.

1.2.6 One Megaword Storage Capability Using 256K DRAMs

The maximum storage capacity of the ISM is one megaword (four megabytes). This is achieved by using the 256K dynamic RAM (DRAM).

The 64K DRAM is also supported by the ISM. Maximum storage capacity using the 64K DRAM is 256KW (1MB).

1.2.7 Four Megaword Addressing Capability

The ISM can be programmed to recognize an address range from zero to four megawords (16 megabytes).

1.2.8 64KW Addressing Recognition Boundaries

The ISM can be programmed to recognize addresses in 64KW (256KB) increments over its address range.

1.2.9 Three Interleaving Options

There are three interleaving options available: no interleaving, two-way, or four-way interleaving. The interleaved modules must all contain the same memory capacity. Interleaving improves system performance for cache based CPU systems.

1.2.10 Optional Read and Lock Capability

The read and lock option allows a processor to lock out another processor while it is modifying data in a memory location. This feature can be disabled for optimum performance in single CPU applications. The option can be enabled for proper ISM operation in multi-processor applications.

1.2.11 Self-Contained Error Correction Code (ECC) Logic

On-board Error Correction Code (ECC) circuits correct single-bit errors and detect and/or report double-bit errors.

1.2.12 Compatible with Existing Battery Back-up

The ISM is compatible with the existing battery back-up system supported by Gould. The higher memory capacity of the ISM, and the use of low power logic circuits result in increased reliability, and longer back-up times when compared to existing memory modules.

1.3 Functional Description

The functional description is divided into seven major functional areas as listed below and briefly described in the paragraphs that follow. Detailed descriptions of these functions are provided in Chapter 4, Theory of Operation, of this manual.

1. SelBUS Interface
2. Error Correction Logic
3. Memory Refresh Logic
4. Scrubbing Logic
5. Memory Storage
6. Module Interleaving Options
7. Controls and Indicator Functions

1.3.1 SelBUS Interface

The ISM interface to the system is through the SelBUS Interface. The SelBUS is physically part of the chassis backplane, is completely passive, and contains no active electronic parts.

The data bus is 32 bits wide (one word or four bytes). The address bus uses 24 address bits to select up to four megawords (16 megabytes) of memory.

There are five basic memory transfer types supported on the SelBUS as listed below:

1. Memory Read Transfer (MRT)
2. Memory Write Transfer (MWT)
3. Memory Read and Lock Transfer (MRLT)
4. Memory Write and Unlock (MWUT)
5. Data Return Transfer (DRT)

Each transfer type requires three SelBUS cycles; polling, transfer, and response. By overlapping these cycles the SelBUS attains a transfer rate of one memory transfer every 150 nanoseconds.

1.3.2 Error Correction Code (ECC) Logic

The ISM contains Error Correction Code (ECC) circuitry to correct and report single-bit errors and detect and report double-bit errors. The error correction code adds seven bits to each 32 bit data word.

1.3.3 Refresh

The ISM performs a refresh cycle every 15.6 microseconds. A refresh operation consists of a fullword read to one of the four banks in the ISM, and a Row Address Strobe (RAS) refresh cycle to the remaining three banks. The refresh cycle is transparent to the system operation.

1.3.4 Scrubbing

The scrubbing circuits of the ISM are used only when a refresh operation detects a single-bit error (SBE) condition. The scrubbing circuits perform read and write memory cycles to try to correct the SBE. If the SBE cannot be corrected, the HARD error LED is illuminated. If the SBE can be corrected, the SOFT error LED is illuminated.

1.3.5 Memory Storage

Table 1-1 lists the different ISM storage configurations for the ISM assembly 160-103723-XXX. All module types may be used together in the same chassis.

1.3.6 Module Interleaving

Module Interleaving is a method of mapping contiguous addresses into separate memory modules to permit overlapped memory operation. The ISM may be installed with no interleaving, two-way, or four-way interleaving. Interleaved modules must all have the same memory capacity. There is no modular interleaving performed within an ISM.

Table 1-1. ISM Storage Configurations

ASSEMBLY DASH NUMBER	MEMORY CHIP USED	MEMORY MODULE CAPACITY
-001	256K DRAM	4MB (1MW)
-002	256K DRAM	2MB (512KW)
-003	256K DRAM	1MB (256KW)
-004	64K DRAM	1MB (256KW)

1.3.7 Controls and Displays

The ISM provides individual controls that reset the display, select scrubbing, select the type of error reported, and enable the error correction circuitry.

The ISM contains 14 LED displays. One is used to indicate an incorrect position of several of the controls. An error logger is used to isolate DRAM error conditions. SBE, Soft, Hard, and DBE displays are also provided.

1.4 Physical Description

Each ISM is mounted in the SelBUS logic chassis on either 0.6 inch or .75 inch centers depending on the logic chassis used. Figure 1-1 illustrates the physical location of the functional sections of the ISM. Controls and Indicators mounted on the ISM allow the user to control functions and observe the status of the module. Table 1-2 lists the physical, electrical, environmental, and operational specifications of the ISM.

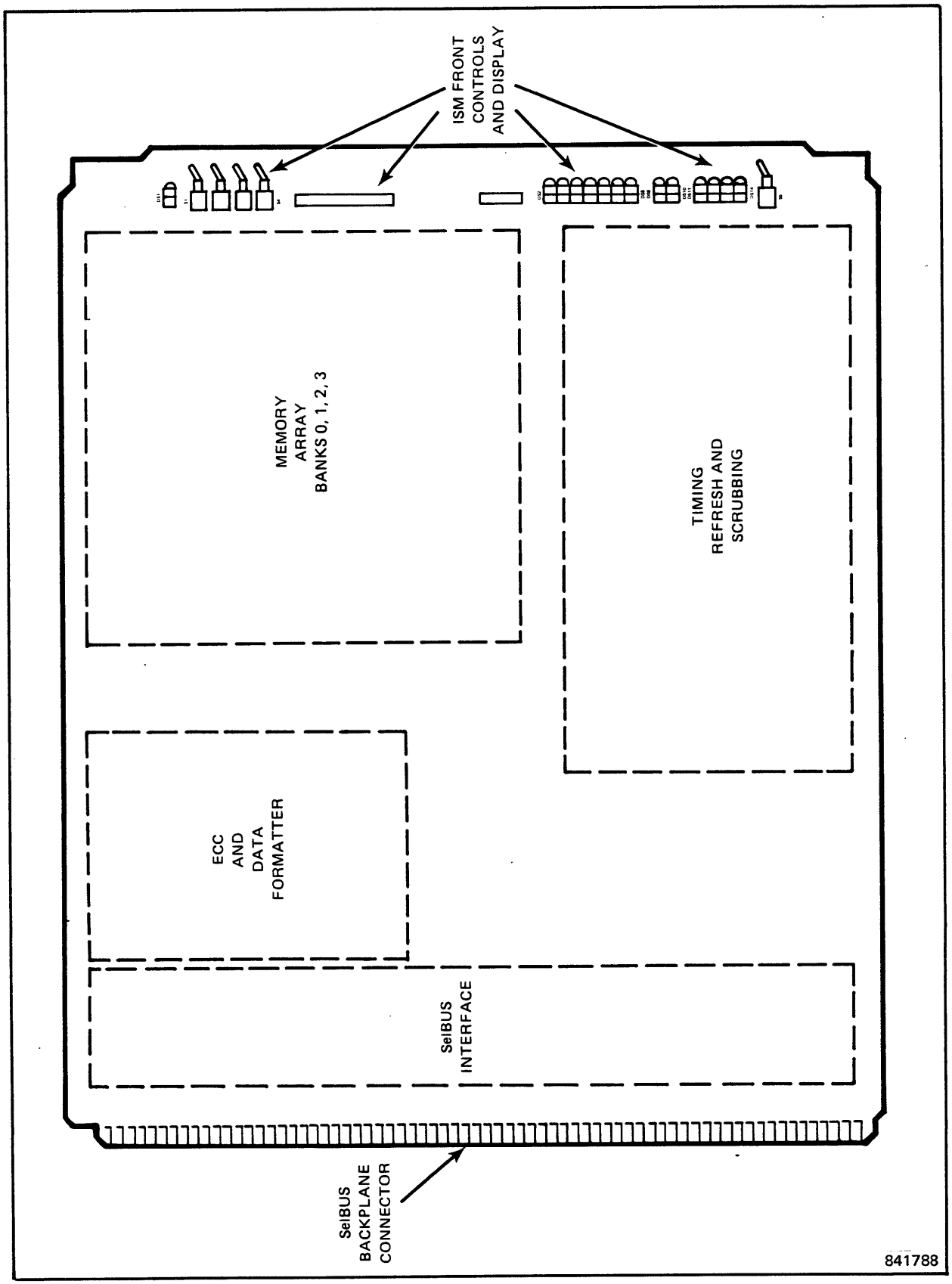

Figure 1-1. ISM Physical Layout

Table 1-2. Integrated Storage Module Specifications

PHYSICAL			
Length	18 inches		
Width	15 inches		
Height	0.4 inch maximum		
Weight	4 lbs.		
ELECTRICAL			
Voltage	+5VDC (2 Supplies)		
Power Dissipation	Voltage (Volts)	Current (Amps) Max.	Power (Watts) Max.
Active	+5VA	6	30
	+5VB	5	25
Idle	+5VA	6	30
	+5VB	3.5	17.5
Battery Backup (+5VB only)	+5VA	--	--
	+5VB	3.5	17.5
ENVIRONMENTAL			
Temperature (Ambient)			
Operating	+50 degrees to +104 degrees Fahrenheit (-10 to +40 degrees Celsius)		
Storage	-40 degrees to +140 degrees Fahrenheit (-40 to +60 degrees Celcius)		
Relative Humidity			
Operating	20 to 80% (non-condensing)		
Storage/Transport	5% to 95% (non-condensing)		
Heat Dissipation/Active	188 BTU per hour		
Heat Dissipation/Idle	162 BTU per hour		
Heat Dissipation/Battery Backup	60 BTU per hour		
Altitude	Up to 10,000 Ft.		

Table 1-2. Integrated Storage Module Specifications (Continued)

OPERATIONAL	
Word Length	39 bits total. 32 data bits plus seven error correction check bits
Capacity	1MW (4MB) using 256K DRAMs 512KW (2MB) using 256K DRAM 256KW (1MB) using 256K DRAM 256KW (1MB) using 64K DRAMs
Access Mode	Random
Read Access Time	Internal 300nsec SelBUS 600nsec
Cycle Time	Fullword Read 300nsec Fullword Write 300nsec Write halfword 600nsec Write byte 600nsec Refresh 300nsec
Modes of Operation	Read fullword Read halfword/selected byte Write fullword Write halfword/selected byte Refresh cycle Scrub cycle
Module Addressing	Jumpers provided for manipulation of the address range.
Error Correction	Error correction check bits generated and stored. Single-bit errors corrected. Double-bit errors detected and reported during normal operation.
Refresh	Each address location refreshed every 4 milliseconds. Sequential address locations refreshed every 15.6 microseconds. A Fullword read used to check for errors. If a SBE is detected, a scrub-cycle is requested.
Scrubbing	Performed when requested. Corrects soft SBE to eliminate accumulation of errors. Reports SBEs as either soft or hard errors.

CHAPTER 2

INSTALLATION AND OPERATION

2.1 Introduction

This chapter describes the installation requirements for the Integrated Storage Module (ISM). The various switches and indicators are illustrated in Figure 2-1. Refer to Chapter 4 (Theory of Operation) for a detailed description of the switches and indicators.

2.2 Installation

ISM's are mounted either horizontally or vertically as required SelBUS logic chassis.

2.3 Operation

There are no operating procedures for the ISM, however, the following controls, indicators, and jumpers should be understood. The operating procedures for the CPU, System Control Panel, and the Operators Console are contained in the appropriate manual.

2.4 Controls

The following on board controls are provided as a means of setting the ISM functions and monitoring certain ISM conditions.

A list of the ISM controls together with their on-board locations, associated logic sheet references, and paragraph in which they are explained is contained in Table 2-1.

2.4.1 Switches

Toggle switches (two position) are located on the front of the ISM to control functions. The normal operating position for all toggle switches is the position shown in Figure 2-1.

2.4.1.1 Display Error Switch (S1)

The normal operating position for this switch is the ON position. This switch controls the error detection LED's on the ISM. With the switch in the ON position, the LEDs are illuminated as required. With this switch in the CLR position, the error logger display will be reset.

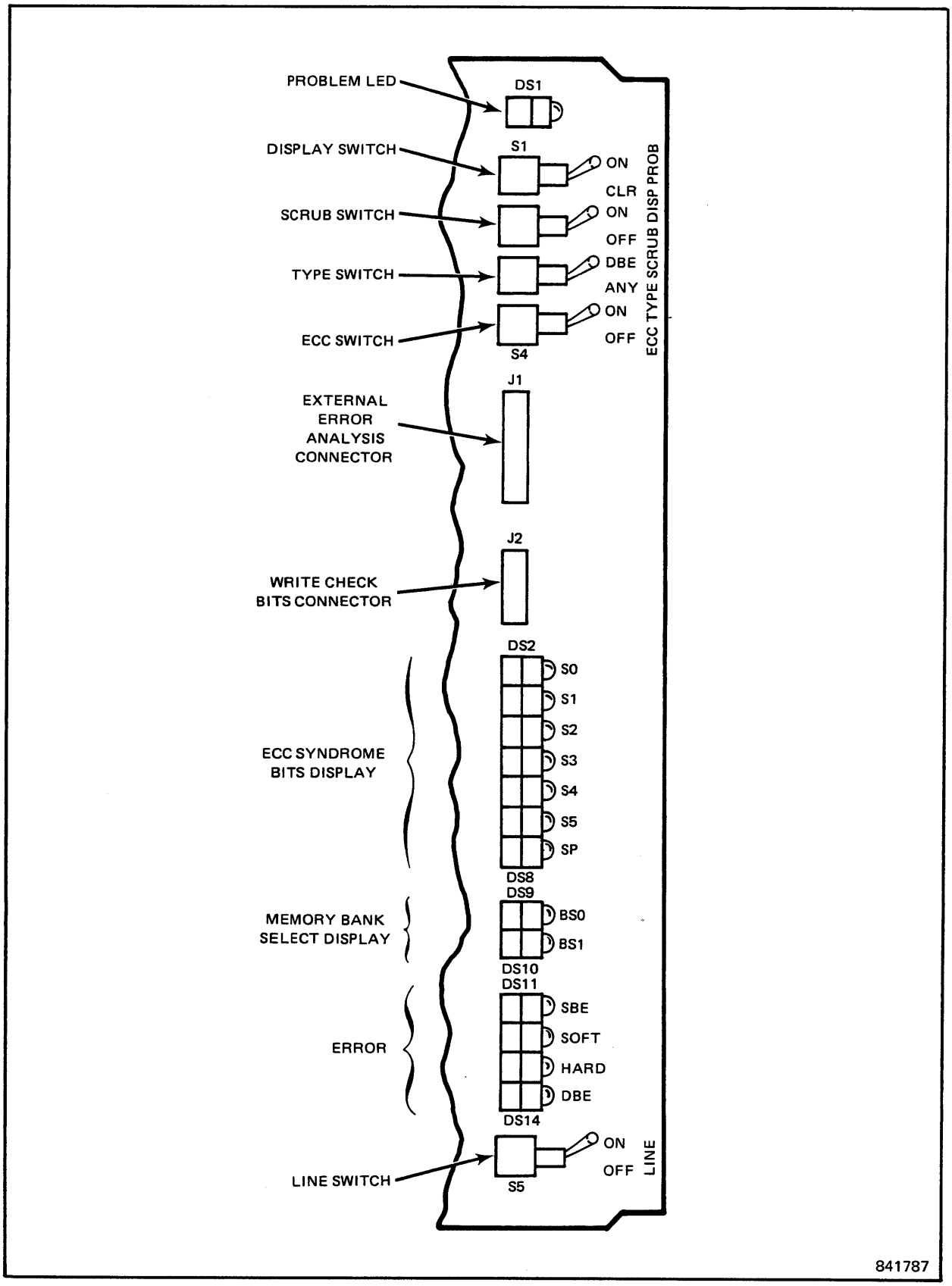

Figure 2-1. ISM Front Controls and Displays

Table 2-1. Controls/Switches

DESCRIPTION/ NOMENCLATURE (POSITIONS)	IDENTIFIER	BOARD LOCATION	LOGIC SHEET	PARAGRAPH
DISPLAY ERROR (CLR/ON)	S1	FRONT	63	2.4.1.1
SCRUB SWITCH (OFF/ON)	S2	FRONT	63	2.4.1.2
ERROR TYPE SWITCH (ANY/DBE)	S3	FRONT	63	2.4.1.3
ECC SWITCH (OFF/ON)	S4	FRONT	63	2.4.1.4
LINE SWITCH (OFF/ON)	S5	FRONT	50	2.4.1.5

2.4.1.2 Scrub Switch (S2)

The normal operating mode for this switch is in the ON position. With the switch in the ON position the scrubbing circuits are enabled if the ECC switch is also on. With the switch in the OFF position, the scrubbing circuits are disabled. The Refresh circuits on the ISM continue regardless of the position of this switch.

2.4.1.3 Error Type Switch (S3)

The normal operating mode for this switch is the DBE position. In the DBE position, only double-bit errors are reported. If the switch is in the ANY position, a single-bit or double-bit error will be reported. If an error occurs, the LERROR signal will be sent on the SelBUS if the LERROR report jumper is enabled.

2.4.1.4 ECC Switch (S4)

The normal operating mode for this switch is the ON position. In the ON position error correction is enabled. If the Scrub switch is also in the ON position, the scrubbing circuits are also enabled.

With the ECC switch in the OFF position, the error correction is disabled. Also, in the OFF position, the scrubbing circuits are disabled since the Scrubbing feature relies on correction cycles for its operation. While in the OFF position write requests by the SelBUS will continue to write the correct syndrome bits. Read requests from the SelBUS will check the syndrome bits and report errors as selected by the LERROR report jumper. (See jumper section.)

2.4.2 Jumpers

There are two basic types of jumpers; hard jumpers and soft jumpers. The following paragraphs describe each type.

2.4.2.1 Soft Jumpers

Soft jumpers are either two pin plug-in assemblies or 16 pin IC jumpr modules. These jumpers are used to set up various system parameters and are intended to be changed in the field. Table 2-2 provides a list of soft jumpers.

2.4.2.1.1 Inhibit (X5 1-4)

These jumpers control which of the four inhibit lines will be set low (true) when inhibits are generated by the ISM. Any combination of inhibit lines may be selected. Refer to Tables 2-3, 2-3A, B, C. Tables 2-4, 2-4A, B provide the Inhibit/Echo jumpering for no interleaving, two-way interleaving or 4-way interleaving when the shared memory enable jumper is installed in the cache control C board.

Table 2-2. Soft Jumpers

DESCRIPTION/ NOMENCLATURE	IDENTIFIER	BOARD LOCATION	LOGIC SHEET	PARAGRAPH
ECHO	X55,6	C19	50	2.4.2.1.2
STARTING ADDRESS	X6-1-6	C28	4	2.4.2.1.3
OFFSET ADDRESS	X6-7-10	E22	4	2.4.2.1.4
READ AND LOCK	X43,4	B21	10	2.4.2.1.5
PRIORITY GENERATION	X2-1-8	A22	9	2.4.2.1.6
PRIORITY RECOGNITION	X3-1-7	A24	9	2.4.2.1.7
ADDRESS INTERLEAVE	X1,1-8	A13		2.4.2.1.8
LDT23 NO ERROR	X5-8	C19	10	2.4.2.1.9
MASTER/SLAVE	X1-2,X3-8	A13, A24	9	2.4.2.1.10
SELBUS CLEAR DISPLAY	X4-1	B21	60	2.4.2.1.11

Table 2-3. Inhibit/Echo Jumper Chart

V6, 32/67, 32/27 (See Note 1)
X5 (C19)

INHIBIT/ECHO	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X					
1		X				X
2			X		X	
3				X	X	X

Table 2-3A. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - No Interleaving/Non-Shared (See Note 1)
X5 (C19)

ECHO ONLY	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X	X	X	X		
1	X	X	X	X		X
2	X	X	X	X	X	
3	X	X	X	X	X	X
	On All Modules Inhibit 0, 1, 2, & 3 Are Driven					

Table 2-3B. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - 2-Way Interleaving/Non-Shared (See Note 1)
X5 (C19)

ECHO/ONLY	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X		X			
1		X		X		X
2	X		X		X	
3		X		X	X	X

Table 2-3C. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - 4-Way Interleaving/Non-Shared (See Note 1)
X5 (C19)

INHIBIT/ECHO	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X					
1		X				X
2			X		X	
3				X	X	X

Table 2-4. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - No Interleaving/Shared (See Notes 2 and 3)
X5 (C19)

ECHO ONLY	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X	X				
1	X	X				X
0	X	X				
1	X	X				X
	On All Modules Inhibit 0 and 1 are Driven					

Table 2-4A. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - 2-Way Interleaving/Shared (See Notes 2 and 3)
X5 (C19)

INHIBIT/ECHO	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X					
1		X				X
0	X					
1		X				X

Table 2-4B. Inhibit/Echo Jumper Chart

32/87, 32/97, V 9 - 4-Way Interleaving/Shared (See Notes 2 and 3)
X5 (C19)

INHIBIT/ECHO	INHIBIT PIN NUMBER				ECHO PIN NUMBER	
	1	2	3	4	5	6
0	X					
1		X				X
0	X					
1		X				X

NOTES

1. It is recommended that Inhibit/Echo zero should be used on modules 0, 4, 8, and C; Inhibit/Echo one be used on modules 1, 5, 9, and D; Inhibit/Echo two be used on modules 2, 6, A, and E; and Inhibit/Echo three be used on modules 3, 7, B and F.
2. These jumpers are applicable for 32/97, 32/87, and V9 when the shared memory enable jumper is installed in the Cache Control "C" board.
3. If an odd number of modules are employed, the odd module must be no-way interleaved.

2.4.2.1.2 Echo (X5 5,6)

These jumpers control which of the two SelBUS echo lines will be set low (true) when an echo code is to be sent by the ISM. Refer to Tables 2-3, 2-3A, B, C and Tables 2-4, 2-4A, B.

2.4.2.1.3 Starting Address (X6 1-6)

These jumpers select the starting address that will be accepted by the module. The selected address must be on a 64KW (256KB) boundary. Refer to Table 2-5.

2.4.2.1.4 Offset Address (X6 7-10)

These jumpers select and automatically calculate the upper address that will be accepted by the module. The selected offset address must be a multiple of 64KW (256KB). Refer to Table 2-6.

2.4.2.1.5 Read and Lock Mode (X4,3,4)

These jumpers enable or disable the ISM read and lock mode. In the enabled mode (X4-4 installed, X4-3 removed) a read and lock request will lock the ISM and prevent it from accepting any additional transfers until a corresponding write and unlock transfer is received. In the disabled mode (X4-3 installed, X4-4 removed) read and lock transfers will be accepted by the ISM without affecting future transfers. All CPU/IPU configurations require that this option be installed.

2.4.2.1.6 Priority Generation (X2 1-8)

These jumpers determine the SelBUS priority generated. A jumper corresponding to the priority assigned to an ISM must be installed. Refer to Table 2-7.

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Table 2-5. Starting Address Jumper Chart

STARTING ADDRESS (WORDS)	JUMPER INSTALLED C28 (X6)					
	1	2	3	4	5	6
0	X	X	X	X	X	X
64KW			X	X	X	X
128KW	X		X	X	X	X
192KW			X	X	X	X
256KW	X	X		X	X	X
512KW	X	X	X		X	X
769KW	X	X			X	X
1024KW	X	X	X	X		X
1280KW	X	X		X		X
1536KW	X	X	X			X
1792KW	X	X				X
2048KW	X	X	X	X	X	
2304KW	X	X		X	X	
2560KW	X	X	X		X	
2816KW	X	X			X	
3072KW	X	X	X	X		
3328KW	X	X		X		
3584KW	X	X	X			
3840KW	X	X				

X Indicates Jumper Installed

Table 2-6. Offset Address Jumper Chart

OFFSET WORDS	JUMPERS INSTALLED IN C28 (X6) PIN 7	PIN 8	PIN 9	PIN 10
64KW	X	X	X	X
128KW		X	X	X
192KW	X		X	X
256KW			X	X
320KW	X	X		X
394KW		X		X
449KW	X			X
512KW				X
576KW	X	X	X	
640KW		X	X	
704KW	X		X	
769KW			X	
832KW	X	X		
896KW		X		
960KW	X			
1024KW	N	O	N	E

X Indicates Jumper Installed

2.4.2.1.7 Priority Recognition (X3 1-7)

These jumpers prevent the ISM from winning the SelBUS poll when processors with higher SelBUS priorities than the ISM are also polling. These jumpers must be installed for all priority levels higher than the ISM and left vacant for all priorities equal to, or lower than the ISM. Refer to Table 2-7.

2.4.2.1.8 Address Interleave (X1, 1-8)

This jumper setting is used to set up the ISM to interleave addresses with other ISM memory modules. ISM options are no interleaving, two-way, or four-way interleaving. The jumpers for X1 are set up using special 16 pin IC modules as listed in Table 2-8.

Table 2-7. SelBUS Priority Jumpers

ISM PRIORITY CODE	INSTALL JUMPERS	
	PRIORITY GENERATION SELECT X 2(1-8) A22	PRIORITY RECOGNITION SELECT X3(1-7) A24
1	X2-1	NONE
2	X2-2	X3-1
3	X2-3	X3-1,2
4	X2-4	X3-1,2,3
5	X2-5	X3-1,2,3,4
6	X2-6	X3-1,2,3,4,5
7	X2-7	X3-1,2,3,4,5,6
8	X2-8	X3-1,2,3,4,5,6,7

2.4.2.1.9 LDT23 No Error Jumper (X5-8)

This jumper, in the enabled position, (X5-8 installed) will allow error information to be sent with a DRT (concurrently, not one clock cycle later). The error signal is sent on the LDT23 address line, and a true (low) condition will mean no error was detected. Current processors do not support this option.

2.4.2.1.10 Master/Slave Enable Jumper

These jumpers are required to enable two ISMs to share the same SelBUS priority. One ISM is the master and the other the slave storage module.

To enable Master/Slave Operation:

1. Master Assembly - remove X4-2, remove X3-8
   Slave Assembly - remove X4-2, install X3-8
2. Install master and slave modules. (Refer to Figure 2-2 for all available board locations.)
3. Install Backplane Jumper Assembly 144-103463-001
4. Both master and slave modules must have the same priority code.

To disable Master/Slave Operation:
Install X4-2, Remove X3-8

Table 2-8. Address Interleave Jumpers

INSTALL GOULD INTEGRATED CIRCUIT MODULE P/N SHOWN BELOW IN POSITION X1 (A13) FOR SELECTED DASH NUMBER OF ASSEMBLY AND INTERLEAVING DESIRED.			
ASSEMBLY DASH NO.	NO INTERLEAVING	2 WAY INTERLEAVING	4 WAY INTERLEAVING
-001 256K DRAM	GOULD P/N 259-700034-001 X1 1-16, 2-15 3-14, 4-13 5-12, 6-11 7-10, 8-9	GOULD P/N 259-700034-000 X1 1-16, 2-10 3-14, 4-13 5-12, 6-11 7-15, 8-16	GOULD P/N 259-700034-009 X1 1-9, 2-10 3-14, 4-13 5-12, 6-11 7-15, 8-16
-002 256K DRAM	SAME AS -001 ABOVE	GOULD P/N 259-700034-006 X1 1-16, 2-9 3-10, 4-13 5-12, 6-11 7-14, 8-9	GOULD P/N 259-700034-007 X1 1-16, 2-9 3-10, 4-13 5-12, 6-11 7-14, 8-15
-003 256K DRAM	SAME AS -001 ABOVE	GOULD P/N 259-700034-004 X1 1-16, 2-15 3-14, 4-10 5-12, 6-11 7-13, 8-9	GOULD P/N 259-700034-005 X1 1-16, 2-15 3-9, 4-10 5-12, 6-11 7-13, 8-14
-004 64K DRAM	SAME AS -001 ABOVE	SAME AS -003 ABOVE	SAME AS -003 ABOVE

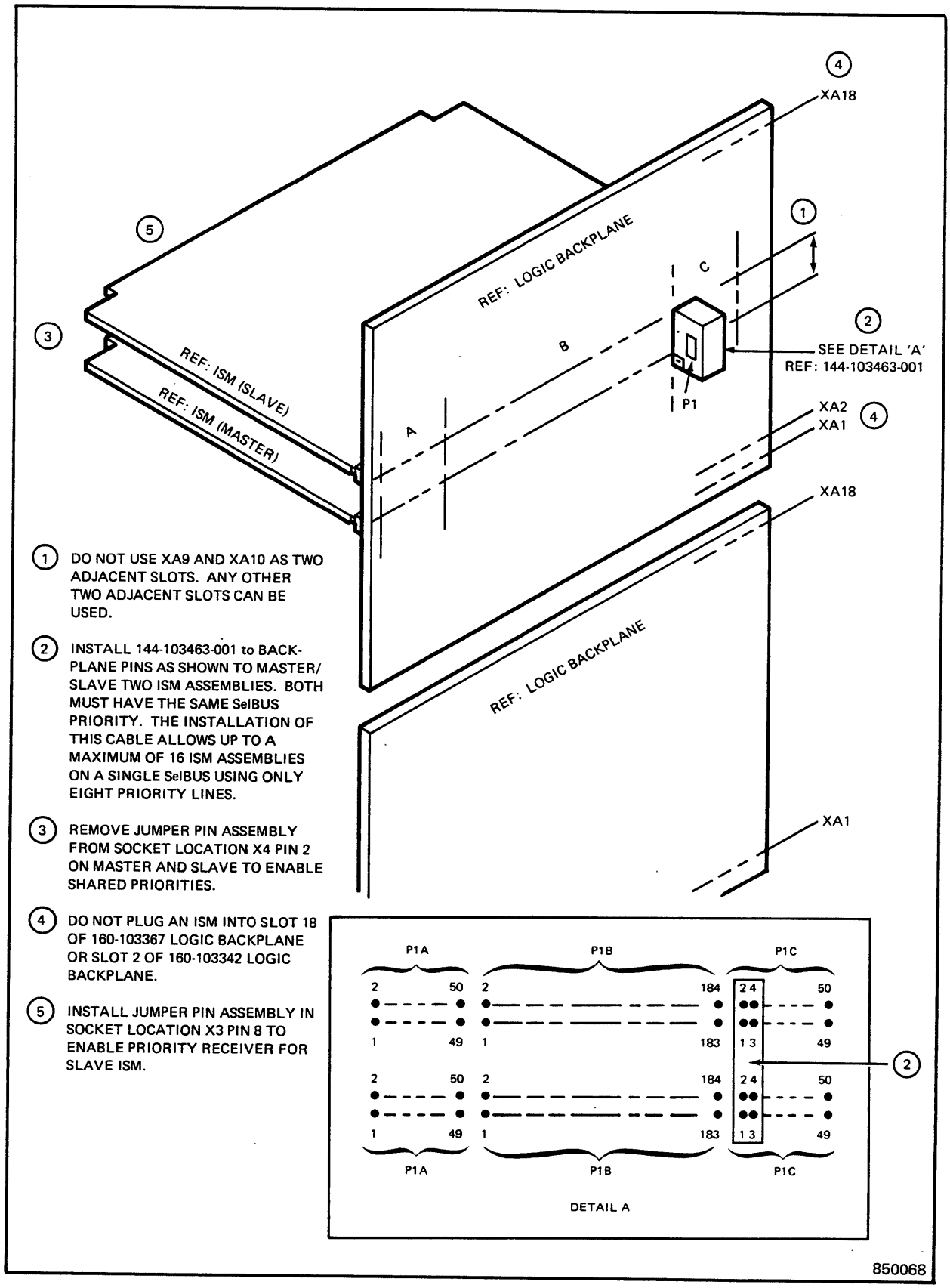


Figure 2-2. Master/Slave Enable

2.4.2.1.11 SelBUS Clear Display (X4-1)

This jumper in the enabled mode (X4-1 installed) allows a SelBUS reset to clear the LED displays on the ISM. The normal operating mode for this jumper is disabled. (X4-1 removed.)

2.4.2.2 Hard Jumpers

Hard jumpers are wirewrapped jumpers normally used for system timing, and are not intended to be changed in the field. Several hard jumpers are used to set up the timing; these hard jumpers are listed in Table 2-9.

2.4.2.2.1 DRAM Type Select (E9-E28)

There are several wirewrapped jumpers to be selected for the DRAM type Address. The configuration of these jumpers is dependent on the particular memory module used. Refer to Table 2-10.

2.4.2.2.2 Memory Bank Decode Select (E1-E8)

These jumpers are used to select the ISM address in order to correspond to the module's storage capability. Refer to Table 2-11.

2.4.2.2.3 RAS Enable (E84)

This jumper is used to enable the Row Address Strobe (RAS). RAS enable (E84) is normally connected to ground (E85), and is disconnected only for test purposes.

2.4.2.2.4 HEDCDLSEL (E37)

This jumper controls a delayed version of the end of cycle signal. It is not normally connected since the signal is permanently connected by board etch to the delay line.

2.4.2.2.5 LTONRASSEL1 (E35)

This jumper controls the turn on time of the RAS signal to the DRAM chips. It is normally connected to E40.

2.4.2.2.6 HTOFFNRASSEL1 (E47)

This jumper controls the turn off time of the RAS signal to the DRAM chips. It is normally connected to E40.

2.4.2.2.7 LTOFFMRASSEL1 (E43)

This jumper controls the turn off time of the RAS signals to the DRAM chips for a 600 nanosecond cycle. It is not normally connected since the signal is permanently connected by board etch.

Table 2-9. Hard Jumpers

DESCRIPTION NOMENCLATURE	IDENTIFIER	BOARD LOCATION	LOGIC SHEET	PARAGRAPH
DRAM TYPE SELECT	E9-28	F18	29	3.4.2.1.1
MEMORY BANK DECODE SELECT	E1-8	F15	28	3.4.2.2.2
RAS ENABLE	E84		51	3.4.2.2.3
HEDCDLSEL	E37	S32	26	3.4.2.2.4
LTONRASEL1	E35	S32	26	3.4.2.2.5
HTOFFNRASSEL1	E47	S32	26	3.4.2.2.6
LTOFFMRASSEL1	E43	S32	26	3.4.2.2.7
LWESTARTSEL	E55	S32	26	3.4.2.2.8
HTOFFECDPLS	E53	S32	26	3.4.2.2.9
HTONECDPLS	E51	S32	26	3.4.2.2.10
HFDBKINSEL	E49	S32	26	3.4.2.2.11
HFDBKSEL	E57	S32	26	3.4.2.2.12
HTONCASSEL	E72	T29	28	3.4.2.2.13
HMUXSEL	E71	T29	28	3.4.2.2.14

Table 2-10. DRAM Type Select Jumpers (E9-E28)

ASSEMBLY DASH NO.	CONNECT JUMPER (wirewrap)
-001	E24-E23, E22-E21, E20-E19, E18-E17, E16-E9, E14-E11, E12-E13, E10-E15, E27-E25
-002	SAME AS -001
-003	SAME AS -001
-004	E26-E23, E24-E21, E22-E19, E20-E17, E18-E9, E16-E11, E14-E13, E12-E15, E27-E28

Table 2-11. Memory Bank Decode Select (E1-E8)

ASSEMBLY DASH NO.	CONNECT (wirewrap)
-001	E8-E6, E7-E5
-002	E8-E2, E7-E5
-003	E8-E2, E7-E1
-004	E8-E4, E7-E3

2.4.2.2.8 LWESTARTSEL (E55)

This jumper controls the turn on time of the Write Enable (WE) signal to the DRAM chips for a 600 nanosecond cycle. It is not normally connected since the signal is permanently connected by board etch to the delay line.

2.4.2.2.9 HTOFFECDPLS (E53)

This jumper controls the turn off time of the HCLKECD pulse which clocks the data read from the DRAM chips. It is normally connected to E50.

2.4.2.2.10 HTONECDPLS (E51)

This jumper controls the turn on time of the HCLKECD pulse which clocks data read from the DRAM chips. It is normally connected to E42.

2.4.2.2.11 HFDBKINSEL (E49)

This jumper controls the signal connected between the delay lines. It is normally connected to E48.

2.4.2.2.12 HFDBKSEL (E57)

This jumper controls the signal connected to the delay line which determines the timing of the feedback signal to the delay line loop. It is normally connected to E48.

For optimum placement of this jumper, refer to the ISM Calibration Specification, 192-103019.

2.4.2.2.13 HTONCASSEL (E72)

This jumper controls the turn on time of the CAS signals to the DRAM chips. It is normally connected to E75.

2.4.2.2.14 HMUXSEL (E71)

This jumper controls the multiplexer time of the address signals to the DRAM chips. It is normally connected to E80.

2.5 Indicators

The following indicators are provided as a means of monitoring ISM conditions. All LED displays are located on the front of the memory module. Refer to Figure 2-1 for LED locations.

2.5.1 Problem LED (Red) (DS1)

This LED is illuminated if any of the switches (S1 through S5) on the ISM are not in their normal position.

2.5.2 Error Logger (Red) (DS2-DS10)

The error logger consists of nine LEDs which display the seven ECC syndrome bits (DS2 through DS8) and the two bank select bits (DS9 and DS10) when any error is detected in a read cycle. The operation of the error logger display is coupled to the setting of the display clear switch. The syndrome error pattern for a hard error will override a soft error already stored in the error logger.

2.5.3 SBE (Green) (DS11)

This LED is illuminated whenever the scrubbing circuits or a SelBUS read transaction detect a single-bit error in memory.

2.5.4 Soft SBE (Green) (DS12)

This LED is illuminated whenever the scrubbing circuits detect a single-bit error which was correctable. The green color of this LED indicates to the user that an acceptable error has occurred.

2.5.5 Hard SBE (Red) (DS13)

This LED is illuminated whenever the scrubbing circuits detect a single-bit error which was uncorrectable.

2.5.6 DBE LED (Red) (DS14)

This LED is illuminated whenever a double-bit error is detected.

CHAPTER 3

SelBUS TRANSFERS AND OPERATIONS

3.1 Introduction

The ISM communicates with the processors on the SelBUS using defined signal conditions which are referred to as Transfers and Transfer Operations.

This chapter covers the following areas:

- SelBUS Protocol
- SelBUS defined Transfer Operations
- SelBUS Timing and Performance for the ISM

3.2 SelBUS Data Priority Transfer System

The ISM uses a transfer system call the SelBUS Data Priority Transfer system to communicate between processors on the SelBUS backplane.

The ISM memory to SelBUS Interface uses 32 data bus lines (LD00-31), 25 address lines (LDT00-23, LDTF), 9 priority lines (LPR00, HPR01-08), 7 transfer proper tag lines (LTX, LMEM, LCNT0-1, LRD, LMLK, LMUNLK), 3 transfer response tag lines (LTA, LUS, LERROR), 2 Echo code lines (LECK0-1), 4 inhibit lines (LINH0-3), and other miscellaneous timing and control lines.

3.3 SelBUS Protocol

Excluding interrupts, which are not used by SelBUS memory processors, there are three basic memory operation types on the SelBUS: write operations, read operations (request only to memory), and data return operations.

The standard protocol for handling each SelBUS operation is basically the same. The steps or cycles are as follows:

1. Check the Inhibit lines (some processors may bypass this function). The ISM does not check the inhibit lines when it needs to poll.
2. Priority polling for access to the SelBUS.
3. Transfer proper (TX).
4. Response (E).

All the above steps can occur concurrently. A different set of lines is used to implement the function described in each step. This allows the bus a rate of one transaction per 150 nanosecond clock period.

Every transaction commences by the processor checking the inhibit lines when applicable to determine if polling can be performed. The processor then asserts its priority. The highest priority processor wins or gains access to the next bus cycle where it will perform the transfer proper (TX). The cycle following the TX is used for reporting exceptions (E) which are responses from the processors.

The TX operations supported by the ISM are defined in Table 3-1. All the transfers, except for the DRT, are transfers to memory.

The E transfer operations supported by the ISM are defined in Table 3-2.

3.3.1 Inhibit Operations

The inhibit lines tell processors on the SelBUS that it is useless to poll for the SelBUS since the ISM is busy or has its buffers full and is unable to accept a transfer. The protocol improves processing efficiency since processors will only poll for the SelBUS for memory processors which can accept transfers.

The inhibit lines are assigned manually for each memory processor. If more than four memory processors reside on a SelBUS, inhibit lines may be shared.

The inhibit lines monitored by all I/O processors are decoded from the echo lines transferred after the last access to memory. This is how processors can determine which inhibit line to test.

Before a standard SelBUS processor polls for a memory write or read transfer, it tests the status of the memory's inhibit lines. If the inhibit line is found FALSE (high) at clock time (Clock 1, just for reference in this explanation) it will poll the bus on the clock period immediately after CLOCK 1. On winning the poll on the next clock (CLOCK 2), the processor sends the memory read or write transfer during the clock period after CLOCK 2, regardless of the state of the inhibit line at CLOCK 2 time.

The ISM (or any memory processor), guarantees that, if the inhibit line is false (high) at any clock time, a memory read or write transfer immediately following the clock time will always be successful, unless a previous transfer sent on the previous clock was a byte or halfword memory read transfer (MRT) or memory read and lock transfer (MRLT).

The above guarantee exists to support processors which wish to communicate with the ISM without ever receiving an unsuccessful response to a transfer request. It should be noted, that for such processors, if it first polls the SelBUS by testing the inhibit line, it must retest the inhibit line immediately before the actual transfer.

Table 3-1. TX Transfer Operations

SelBUS Signals							Transfer Operation (TX) (input/output)
LTX	LMEM	LCNT0	LCNT1	LRD	LMLK	LMUNLK	
L	L	H*	H*	L	H	H	Memory Read Transfer (MRT) (input to memory)
L	L	H*	H*	H	H	H	Memory Write Transfer (MWT) (input to memory)
L	H*	L	L	H*	H*	H*	Data Return Transfer (DRT) (output from memory)
L	L	H*	H*	L	L	H	Memory Read and Lock Transfer (MRLT) (input to memory)
L	L	H*	H*	H	H	L	Memory Write and Unlock Transfer (MWUT) (input to memory)

Notes:
1. LMLK and LMUNLK cannot be low at the same time.
2. An asterisk after a level indicates the condition of that SelBUS signal is a don't care condition for the transfer and is not monitored or driven by the memory module. The normal state of the level is shown for reference only.

Table 3-2. E Transfer Operations

SelBUS Signals			Transfer Operation (E)
LTA	LUS	LERROR	
H	H	H*	Nonpresent Memory Accessed
L	H	H*	Transfer Accepted by Memory
L	L	H*	Transfer Unsuccessful, Not Accepted by Memory
H*	H*	L	Error Transfer (previous DRT from Memory contained an uncorrectable data error)

Notes:
1. An asterisk after a level indicates the condition of that SelBUS signal is a don't care condition for that particular transfer and is not monitored or driven by the memory module.

3.3.2 Priority Polling

The SelBUS data priority transfer system does not involve the use of centralized polling logic. Instead each SelBUS device is equipped with its own priority resolving logic. During a polling period or window (every 150 nanosecond period), any processor that seeks access to the SelBUS will assert its own priority level on the SelBUS while at the same time, checking for the presence of other higher priority levels driven by other processors. For any particular processor, if no other higher priority levels are present at the end of the polling window, the processor has won the polling operation and it will take the next 150 nanosecond period to perform the transfer on the SelBUS.

All processors are assigned a bus priority on the SelBUS. There are 24 priority levels, 23 of which are represented by signals on the SelBUS.

The highest priority level, level zero, is represented by the signal line LPR00. The intermediate levels, priority levels 1 through 22, are represented by the signal lines HPR01-22. The lowest priority level, level 23, is represented by the case when LPR00 and HPR01 through HPR22 are false, (i.e., there are no processors polling the SelBUS).

Priority levels 2 through 23 are assigned to I/O and memory processors. As a rule, the processors with the highest throughput are assigned the highest priorities to accommodate the faster speed in transferring data.

The ISM is designed to only support priority levels 1-8. No other priority levels can be assigned. In the case where more than eight ISMs must be installed, a Master/Slave option is provided to allow sharing of priorities between ISM modules. Refer to Chapter Two (Installation and Operation) for details concerning this option.

3.4 Transfer (TX) Operations

The following paragraphs describe the various transfers performed by the ISM.

3.4.1 Memory Read Transfer (MRT)

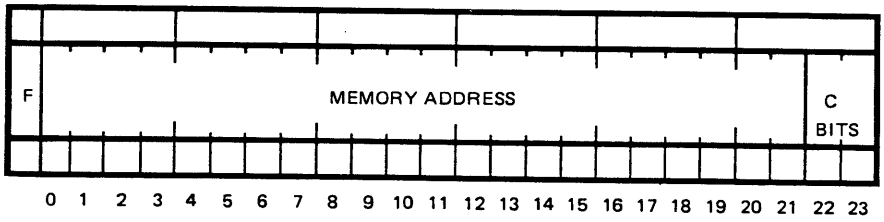
An MRT can originate in any processor on the SelBUS which needs to access memory data. Figure 3-1 illustrates the destination and data bus formats. The SelBUS signal (tag line) configuration for an MRT is defined in Table 3-1.

The memory destination of an MRT is indicated by the 24 bit address on the destination bus and the condition of the memory tag line (LMEM=1). The transfer is indicated as a MRT by the true condition of the read tag line (LRD=1) and the false conditions on the control lines (LCNT0=0 and LCNT1=0).

When the memory has read the location specified by the memory address, the memory generates a data return transfer (DRT) to the requesting device. The DRT is sent only to the SelBUS of the memory module from which the MRT originated.

During the SelBUS transfer cycle immediately following the MRT, the requesting device must monitor the transfer acknowledge (LTA) and the transfer unsuccessful (LUS) tag lines to insure that the memory has received, and will process, the MRT. Refer to Table 3-2 for these signal conditions.

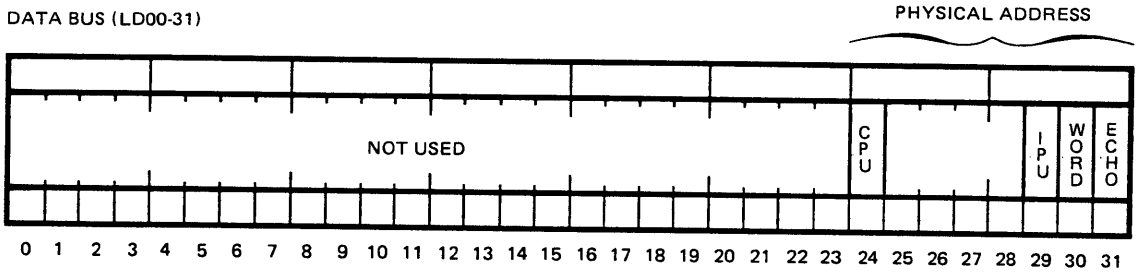
DESTINATION BUS (LDT0-23, F)



MEMORY ADDRESS:

BITS 0 - 23 PROVIDE THE MEMORY ADDRESS OF THE LOCATION TO BE READ.

DATA BUS (LD00-31)



CPU AND IPU BITS:

CPU BIT	IPU BIT	DESCRIPTION
0	X	I/O PROCESSOR IS ORIGINATOR; BITS 25 - 31 SHOULD SPECIFY PHYSICAL ADDRESS OF I/O PROCESSOR.
1	0	CPU IS ORIGINATOR; BITS 25 - 28 NOT USED.
1	1	IPU IS ORIGINATOR; BITS 25 - 28 NOT USED.

WORD BIT:

BIT 30 = 1 SPECIFIES WORD READ IS EVEN; BIT 30 = 0 SPECIFIED WORD READ IS ODD.

ECHO BIT:

BIT 31 = 0 SPECIFIES AN OPERAND FETCH.

BIT 31 = 1 SPECIFIES AN INSTRUCTION FETCH.

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Figure 3-1. MRT Format

The MRT can be used to specify a word, half-word, or byte read. The data read from memory is transferred during the DRT on the data bus and right-justified with zeros in the unused portion of the word. The F-bit (LDTF) and the destination C-bits (LDT22 and LDT23) are used to specify these formats. The decoding of the data bus formats is listed in Table 3-3.

3.4.2 Memory Write Transfer (MWT)

The MWT can originate in any processor on the SelBUS which needs to write memory data. Figure 3-2 illustrates the destination and data bus formats.

The SelBUS signal (tag line) for a MWT is listed in Table 3-1.

The memory destination of the MWT is determined by the 24-bit address on the destination bus and the condition of the memory tag line (LMEM=1). The transfer is identified as a MWT by the false condition of the tag line (LRD=0) and the control lines (LCNT0=0 and LCNT1=0). In a MWT the destination bus contains the memory address and the data bus contains the data (32 bits) to be stored in the memory address.

During the SelBUS transfer cycle immediately following the MWT, the requesting device must monitor the transfer acknowledge (LTA) and transfer unsuccessful (LUS) tag lines to insure that the ISM has received and will process, the MWT. Refer to Table 3-2 for these signal conditions.

The MWT can be used to specify a word, half-word, or byte write. The data to be stored in memory is transferred during the MWT on the data bus and right-justified with zeros in the unused portion of the word. The F-bits (LDTF) and the destination C-bits (LDT22 and LDT23) are used to specify these formats. The decoding of the data bus formats is shown in Table 3-3.

3.4.3 Memory Read and Lock Transfer (MRLT)

A MRLT originates in either a CPU or an IPU. Only three instructions can generate a MRLT: Add Bit in Memory (ABM), Zero Bit in Memory (ZBM), and Set Bit in Memory (SBM). The MRLT SelBUS format is identical to the MRT format illustrated in Figure 3-1 with the additional LMLK signal being low. The SelBUS signal (tag line) configuration for a MRLT is listed in Table 3-1.

The memory destination of the MRLT is indicated by the 24-bit address and the condition of the memory tag line (LMEM=1). The transfer is identified as a MRLT by the true conditions of the read tag line (LRD=1) and the memory lock tag line (LMLK=1) and the false conditions of the control lines (LCNT0=0 and LCNT1=0).

During the SelBUS transfer cycle immediately following the MRLT, the requesting device must monitor the transfer acknowledge (LTA) and the transfer unsuccessful (LUS) tag lines to insure that the memory has received, and will process the MRLT. Refer to Table 3-2 for these signal conditions.

In the MRLT, the destination bus contains the memory address to be read and bits 24 through 31 of the data bus contain the requesting device's physical address.

In normal operating mode, if a double-bit parity error occurs during an MRLT, the ISM will perform an automatic unlock. The ISM will then respond successfully to the next transfer (MRT, MWT, or MRLT) received.

Table 3-3. Data Bus Format Decoding Chart

F-bit	C-bits		Transfer Function
LDTF	LDT22	LDT23	
0	0	0	Fullword Transfer
0	1	0	Fullword or Multiple Word Transfer
0	0	1	Halfword Transfer (Left Halfword)
0	1	1	Halfword Transfer (Right Halfword)
1	0	0	Byte Transfer, Byte 0 (bits 0-7)
1	0	1	Byte Transfer, Byte 1 (bits 8-15)
1	1	0	Byte Transfer, Byte 2 (bits 16-23)
1	1	1	Byte Transfer, Byte 3 (bits 24-31)

3.4.4 Memory Write and Unlock Transfer (MWUT)

The Memory Write and Unlock Transfer (MWUT) originates in the CPU or IPU which issued the MRLT. The MWUT SelBUS format is identical to the MWT format shown in Figure 3-2 with the addition of LMUNLK being low as indicated. The SelBUS signal (tag line) for a MWUT is listed in Table 3-1.

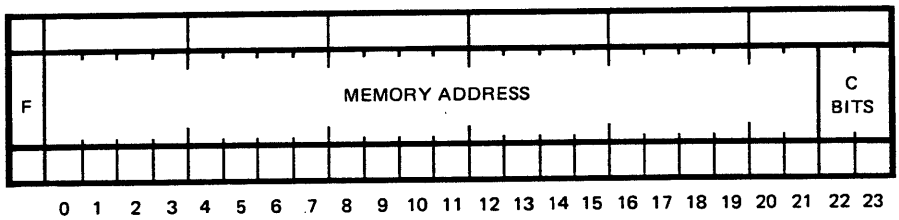
The memory destination of the MWUT is indicated by the 24-bit address and the condition of the memory tag line (LMEM=1). This destination must be identical to the preceeding successful MRLT. The MWUT is identified as a memory write and unlock transfer by the false conditions of the read tag line (LRD=0) and control lines LCNT0=0 and LCNT1=0) and the true condition of the memory unlock tag line (LMUNLK=1). In the MWUT, the destination bus contains the memory address to be written and the data bus contains the 32 bits of data to be written.

The SelBUS interface of the memory board receiving an MWUT is unlocked and is free to accept memory transfers. The MWUT is never unsuccessful.

Every MRLT must have a corresponding MWUT. If a MWUT fault occurs, where the ISM is left locked because an MWUT was never received, the ISM can only be unlocked or cleared by:

1. A system reset.
2. The CPU sending a special MWUT or a special read and unlock transfer (not a defined normal transfer).

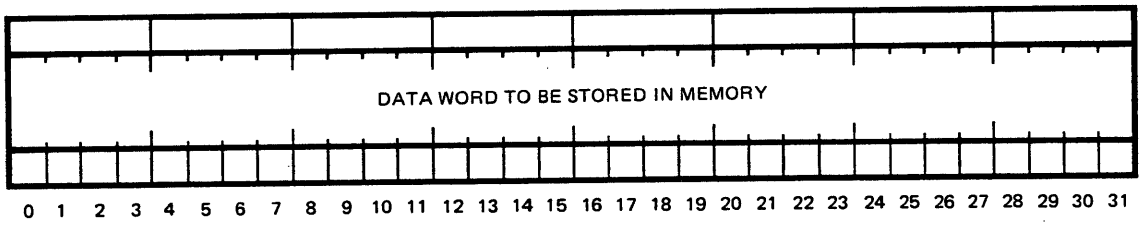
DESTINATION BUS (LDT0-23, F)



MEMORY ADDRESS:

BITS 0 THROUGH 23 PROVIDE THE MEMORY ADDRESS FOR THE LOCATION TO BE WRITTEN.

DATA BUS (CD00-31)



DATA WORD:

BITS 0 THROUGH 31 PROVIDE THE DATA WORD TO BE STORED AT THE ADDRESS SPECIFIED BY THE DESTINATION BUS.

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Figure 3-2. MWT Format

3.4.5 Data Return Transfer (DRT)

The Data Return Transfer (DRT) originates in memory. Figure 3-3 illustrates the DRT format. The SelBUS signal (tag line) configuration for a DRT is listed in Table 3-1.

The destination of the DRT is the original requesting device. This transfer is identified as a DRT by the false conditions of the memory tag line (LMEM=0), the read tag line (LRD=0), and the true conditions of the control lines (LCNT0=1 and LCNT1=1). The requesting device's physical address, contained in data bus bits 24 through 31 during an MRT or MRLT, is returned unaltered in destination bus bits 08 through 15 during the DRT. The data bus contains the data (32 bits) read from memory as the result of an MRT or MRLT.

During the SelBUS transfer cycle immediately following the DRT, the requesting device must monitor the error (LERROR) tag line to determine if the data received contains an uncorrected data error. Refer to Table 3-2 for this signal condition.

3.5 Respond (E) Transfer Operations

The following paragraphs describe the various respond transfer operations performed by the ISM.

3.5.1 Nonpresent Memory Accessed

Refer to Table 3-2 for the signal conditions.

If a TX occurs on the SelBUS to an address not acceptable by the SelBUS processor, the signals LTA and LUS will not be driven by any processor and remain false on the next cycle after the TX transfer.

The destination and data busses are not used for this response.

3.5.2 Transfer Accepted Memory

Refer to Table 3-2 for the signal conditions.

If a TX occurs on the SelBUS and the memory can accept the transfer, it will indicate a successful transfer with LTA true and LUS false on the next cycle after the TX transfer.

The destination and data busses are not used for this response.

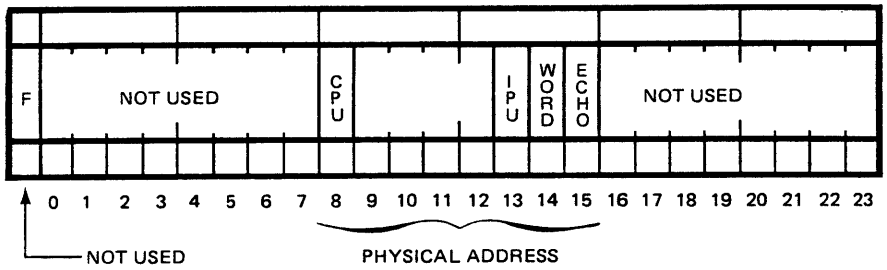
3.5.3 Transfer Unsuccessful

Refer to Table 3-2 for the signal conditions.

If a TX occurs on the SelBUS and the memory cannot accept the transfer, it will indicate an unsuccessful transfer with LTA true and LUS true on the next cycle after the TX transfer.

The destination and data busses are not used for this response.

DESTINATION BUS (LDT0-23, F)



CPU AND IPU BITS:

CPU BIT	IPU BIT	DESCRIPTION
0	X	I/O PROCESSOR IS ORIGINATOR; BITS 25 - 31 SHOULD SPECIFY PHYSICAL ADDRESS OF I/O PROCESSOR.
1	0	CPU IS ORIGINATOR; BITS 25 - 28 NOT USED.
1	1	IPU IS ORIGINATOR; BITS 25 - 28 NOT USED.

WORD BIT:

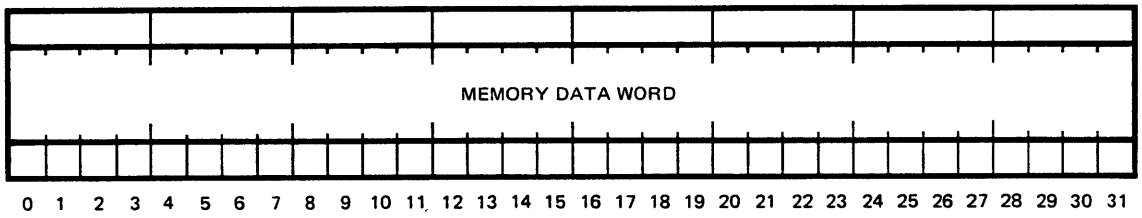
BIT 30 = 1 SPECIFIES WORD READ IS EVEN; BIT 30 = 0 SPECIFIES WORD READ IS ODD.

ECHO BIT:

BIT 31 = 0 SPECIFIES AN OPERAND FETCH.

BIT 31 = 1 SPECIFIES AN INSTRUCTION FETCH.

DATA BUS (LD00-31)



DATA WORD:

BITS 0 THROUGH 31 CONTAIN THE DATA WORD READ.

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Figure 3-3. DRT Format

3.5.4 Error Transfer

Refer to Table 3-2 for the signal conditions.

The E response transfer is only applicable on the next clock cycle after a Data Return Transfer (DRT) is sent by the memory module. If the read cycle which the memory module performed for the DRT transfer found an error condition which has to be reported to the SelBUS, the memory module will transmit the error condition on the next cycle after the DRT transfer.

This condition is reported with the LERROR signal true on the SelBUS.

The destination and data busses are not used for this response.

3.6 ISM Performance and Timing

The SelBUS Interface fastest access time to all read requests (fullword, halfword, byte) is 600 nanoseconds. This value assumes the ISM is initially idle. The 600 nanoseconds include the 300 nanosecond inherent overhead in the SelBUS Interface.

The effect on access time from multiple read requests is summarized in Table 3-4. Maximum system efficiency for reads occurs with at least two ISM boards and with requests perfectly interleaved between the two modules. This is also the case with sequential addressing and ISMs two or four-way interleaved.

Figures 3-4, 3-5, and 3-6 illustrate the response of a single ISM on the SelBUS to various read and write combinations. Note that the maximum word rate in Figure 3-4 corresponds to the non-interleaved case of Table 3-4.

In Figures 3-4, 3-5, and 3-6 the status of the memory inhibit lines are shown for each clock period. A box during a clock period indicates the inhibit line is true (low) on the SelBUS for that period. Note that the inhibit line goes true (low) for at least one clock period when a request is accepted. Note also the condition that transfers can be accepted by the ISM though the inhibit line is low at the previous clock.

The status of the SelBUS line LUS (unsuccessful) is also reflected in Figures 3-4, 3-5, and 3-6. A box during a clock period indicates that if a memory transfer is sent during that clock period, it will not be accepted by the ISM and the LUS signal will be sent on the next clock.

Table 3-4. ISM Access Time Performance

Request No.	Single Memory Module or Requests to one module only (usec.)		Requests Perfectly Interleaved between modules or sequential addressing with 2 or 4 way interleaving (usec.)	
	MRT(x)-DRT TIME	MRT(1)-DRT TIME	MRT(x)-DRT TIME	MRT(1)-DRT TIME
1	.600	.600	.600	.600
2	.750	.900	.600	.750
3	.600	1.200	.600	.900
4	.600	1.500	.600	1.500
5	.600	1.800	.600	1.650
6	.600	2.100	.600	1.800
7	.600	2.400	.600	2.400
8	.600	2.700	.600	2.550

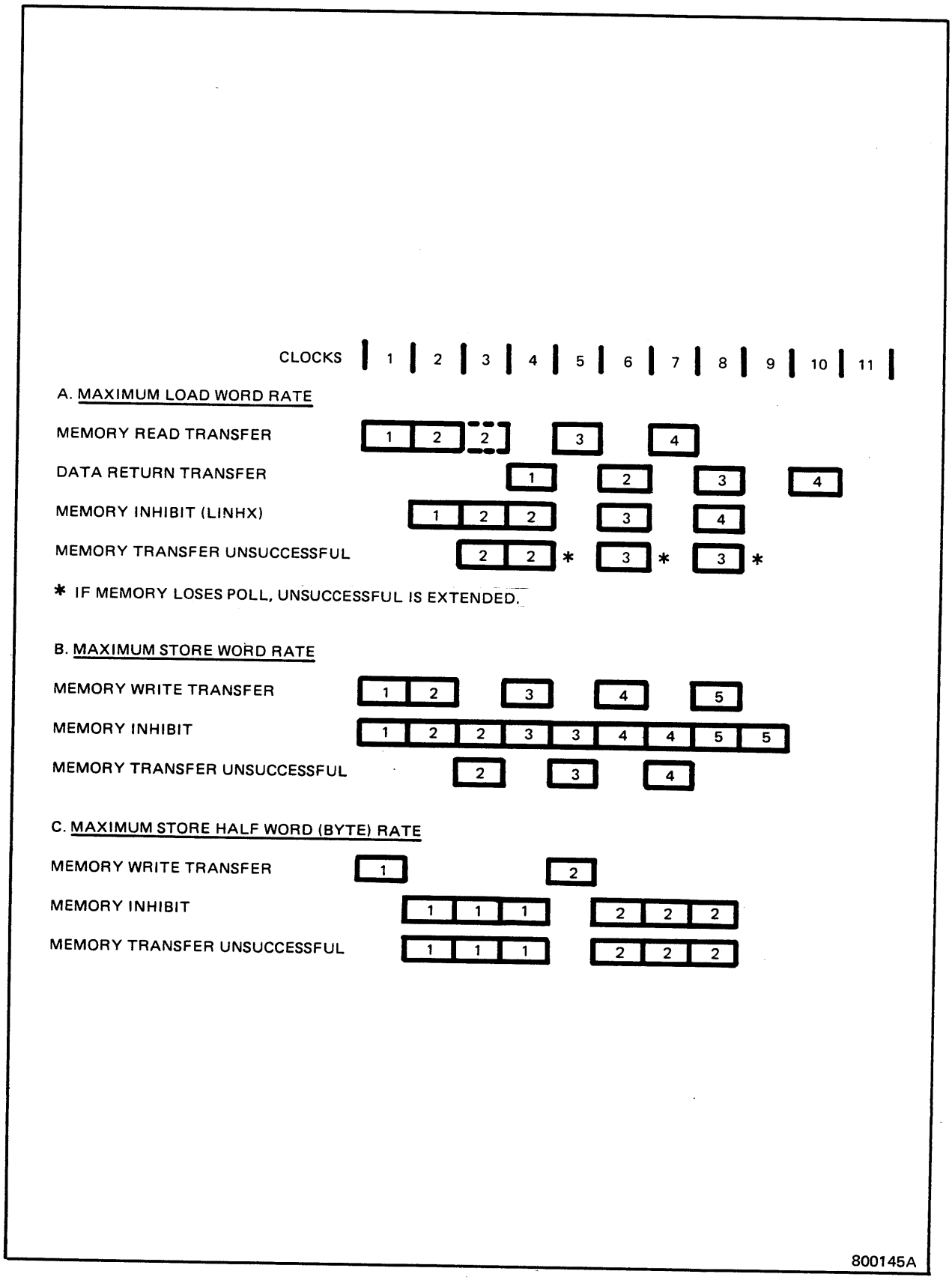


Figure 3-4. Performance Transactions Not Mixed

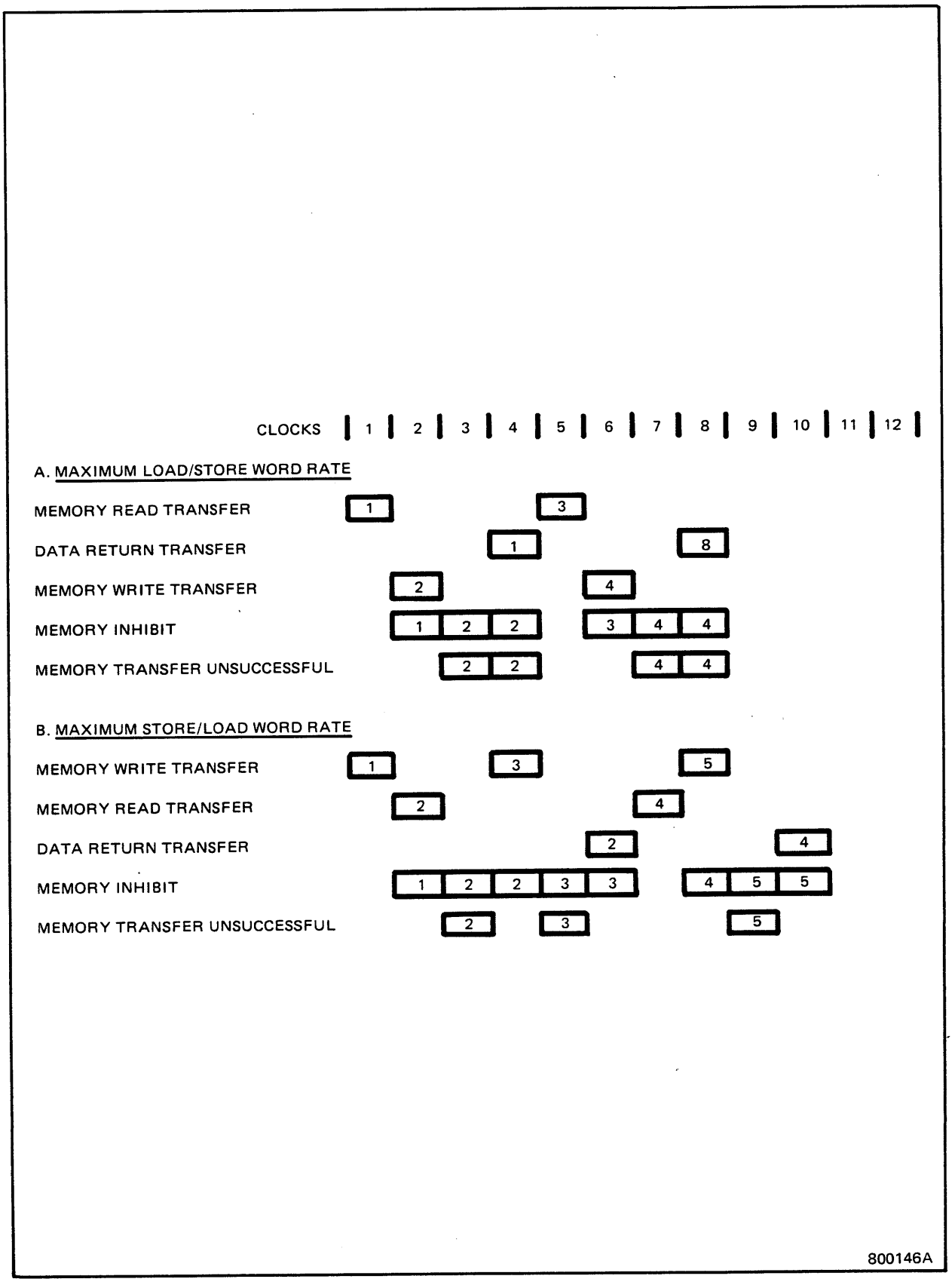


Figure 3-5. Performance Transactions Mixed Load/Store

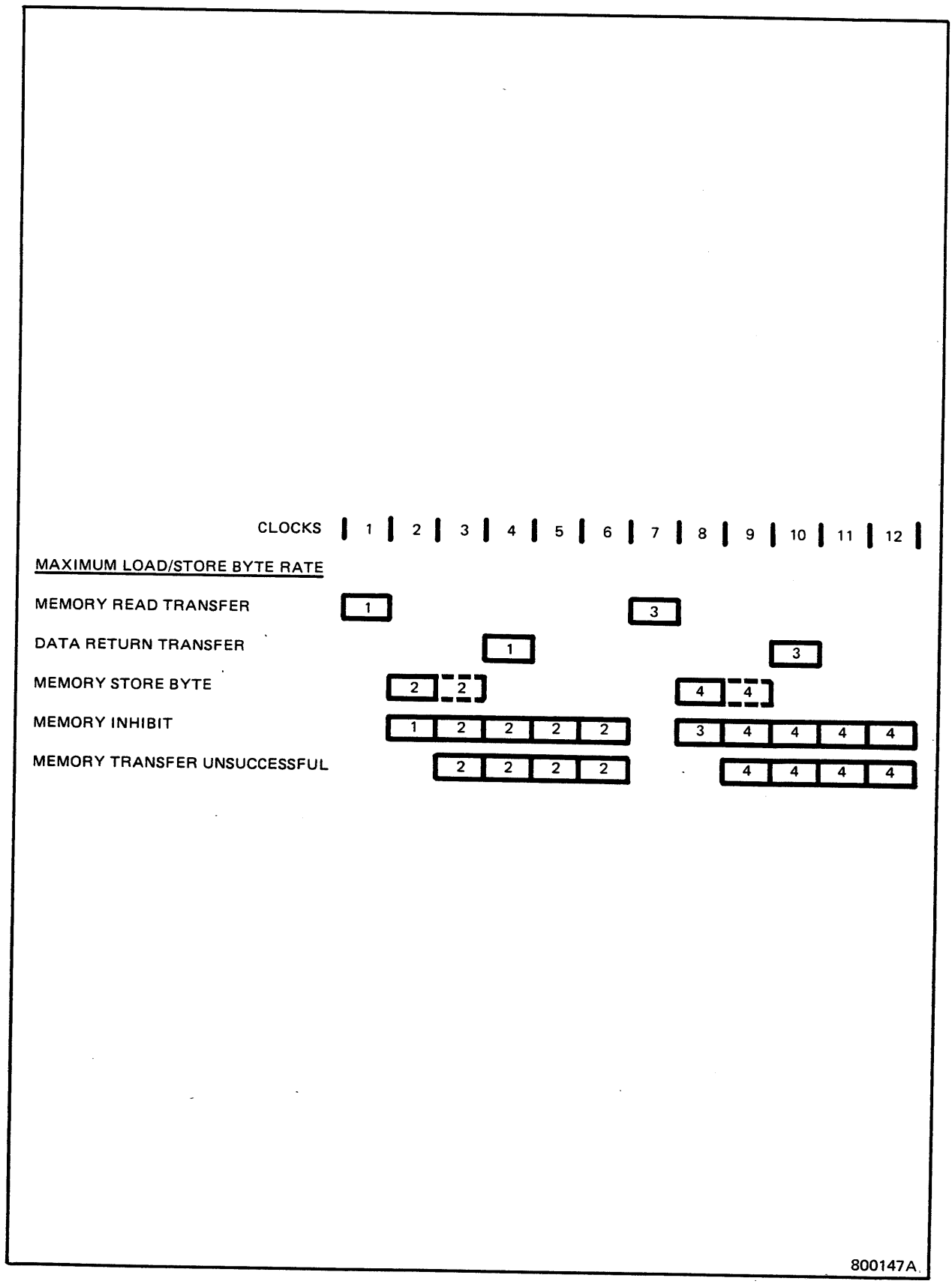


Figure 3-6. Performance Transactions Mixed Load/Store Byte

CHAPTER 4

THEORY OF OPERATION

4.1 Introduction

The theory of operation for the ISM is divided into two levels. The first level is a general theory which describes the overall operation of the memory module. The second level is the detailed theory which describes the ISM logic. Reference to the memory logic diagrams (contained in the ISM drawings manual) is required for the detailed theory of operation.

4.2 Mnemonics

All of the interface signals, and most of the internal ISM signals are referenced by mnemonics throughout the logic explanations. Mnemonic definitions are provided in Appendix A.

4.3 General Theory

The Integrated Storage Module consists of a SelBUS Interface, refresh circuits, scrubbing circuits, error correction circuits, controls, displays, and an external error analysis connector. Figure 4-1 is a simplified block diagram of the ISM. The following paragraphs provide a general description of each block.

4.3.1 SelBUS Interface

The SelBUS interface is responsible for transmitting and receiving all signals to and from the ISM.

4.3.2 Data Formatter and Error Correction

The data formatter and error correction portion of the ISM route the data during read and write cycles. This section also determines the error correction code (ECC) check bits and checks for errors on read cycles from memory.

4.3.3 Memory Storage

The memory storage section contains the DRAM array. The number of DRAMs employed by an ISM is dependent upon the memory storage capability of the individual module.

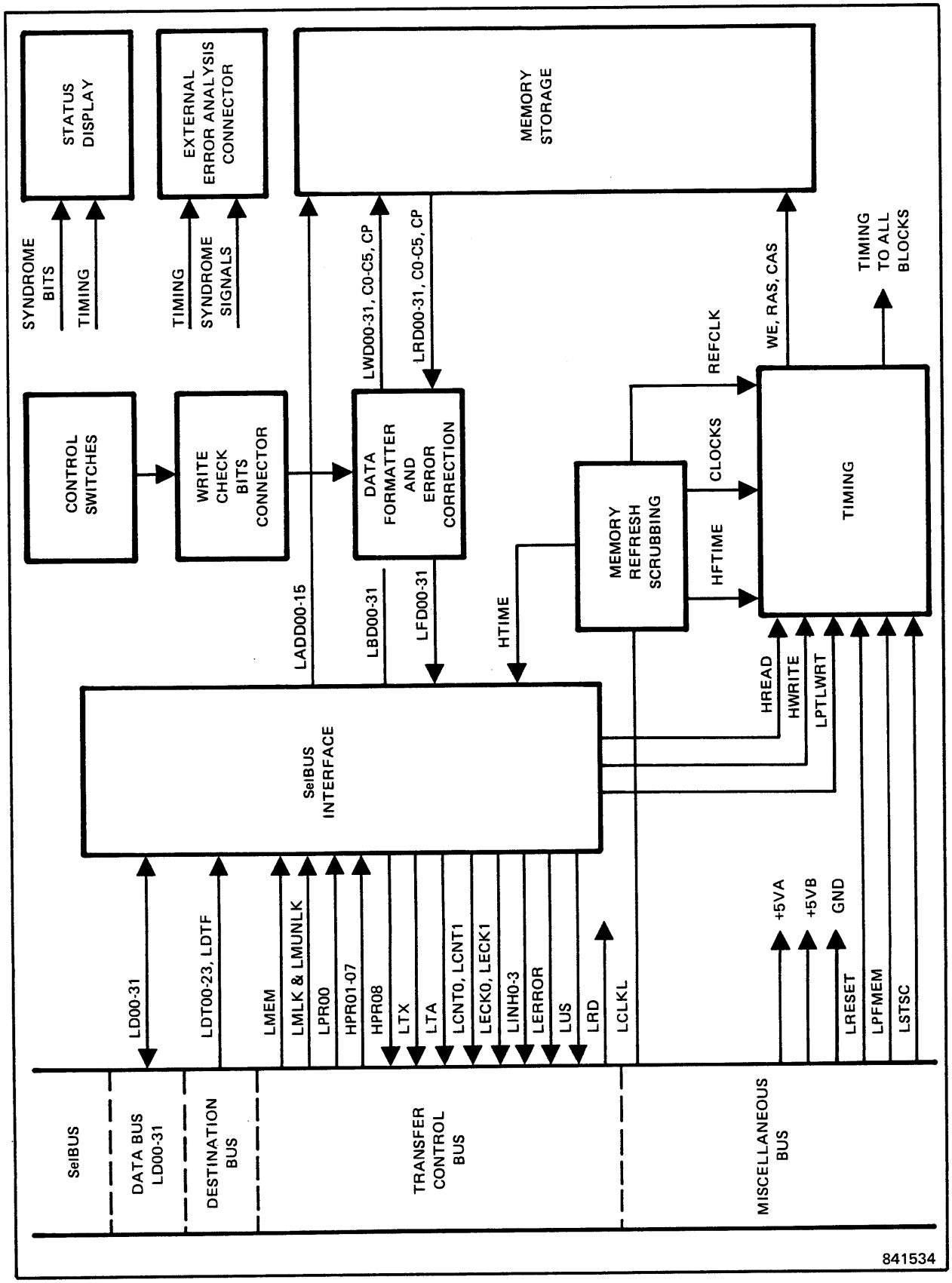


Figure 4-1. ISM Simplified Block Diagram

4.3.4 Timing

The timing section of the ISM is responsible for controlling all functions on the board. The refresh and scrubbing section is actually a timing subsection which continually makes requests for refresh and scrubbing cycles of the DRAM chips.

4.3.5 External Error Analysis Connector

The External Error Analysis Connector allows for error logging externally. This is helpful for maintenance purposes.

4.3.6 Control Switches

The ISM contains Controls (switches) that reset the display, select scrubbing, select the type of error reported, and enables the error correction circuits.

4.3.7 Status Display

There are several on board LED displays which are used to indicate an incorrect position of several of the controls. An LED error logger is used to isolate error conditions. SBE, SOFT, HARD, and DBE LED displays are also contained on the board.

4.4 Detailed Theory

The detailed theory of operation for the ISM is broken into six major topics: memory storage, module address structure, SelBUS interface, timing, refresh and scrubbing, and error correction.

Figure 4-2 is a detailed block diagram of the ISM. Each block contains the sheet(s) number of the logic diagram represented and should be used as a reference in the sections below.

4.5 Memory Storage

The following paragraphs describe the ISM word structure and the DRAM storage circuits.

4.5.1 Dynamic RAM (DRAM) Circuits (Sheets 34-49)

The basic storage element of the ISM is the MOS dynamic random access memory integrated circuit. The DRAM is a dynamic device. It is dynamic in that it requires periodic refresh input in order to retain the stored data.

The DRAMs are organized into four banks of 39 chips, one chip for each of the 32 data bits and one chip for each of the seven error correction code (ECC) bits. Each 256K DRAM is organized into 262,144 by one bit addresses.

4.5.2 Row Address Strobe - RAS (Sheets 51, 28)

The HRAS signal is developed on sheet 51 of the logic diagrams and sent to the RAS bank decode drivers on sheet 28.

The bank address, which is composed of two successive bits, is decoded to determine which of the four sets of banks on the ISM will receive the LRAS signal. When HRAS is received, two row address strobes are applied to the selected set of 39 DRAM chips on the ISM. The LRAS outputs are series resistor terminated and are connected to the two rows of DRAM chips in each bank.

4.5.3 Column Address Strobe - CAS (Sheet 28)

The HRAS signal is applied to a delay line. The output of the delay line is used to form HTONCASSEL. The buffered and inverted outputs are applied to all four sets of DRAM chips in parallel.

Only one of the four banks in the ISM will receive both the LRAS and LCAS signals.

4.5.4 Addressing (Sheets 28-32)

One of the delay line taps is selected by jumpering to provide the multiplexing signal (LMUXADD) to the address selector. Proper address bits are jumpered to the input of the multiplexer inputs. When LMUXADD is high at the select input, it gates the B inputs of the multiplexer to the output address lines which become the row address to the DRAM chips. When the outputs of the selected delay line taps change level, LMUXADD goes low. The column address then appears at the multiplexer outputs.

4.5.5 Write Enable (Sheets 32, 51)

During 300 nanosecond memory write cycles, the Write Enable (LWE) signal remains low for the complete cycle.

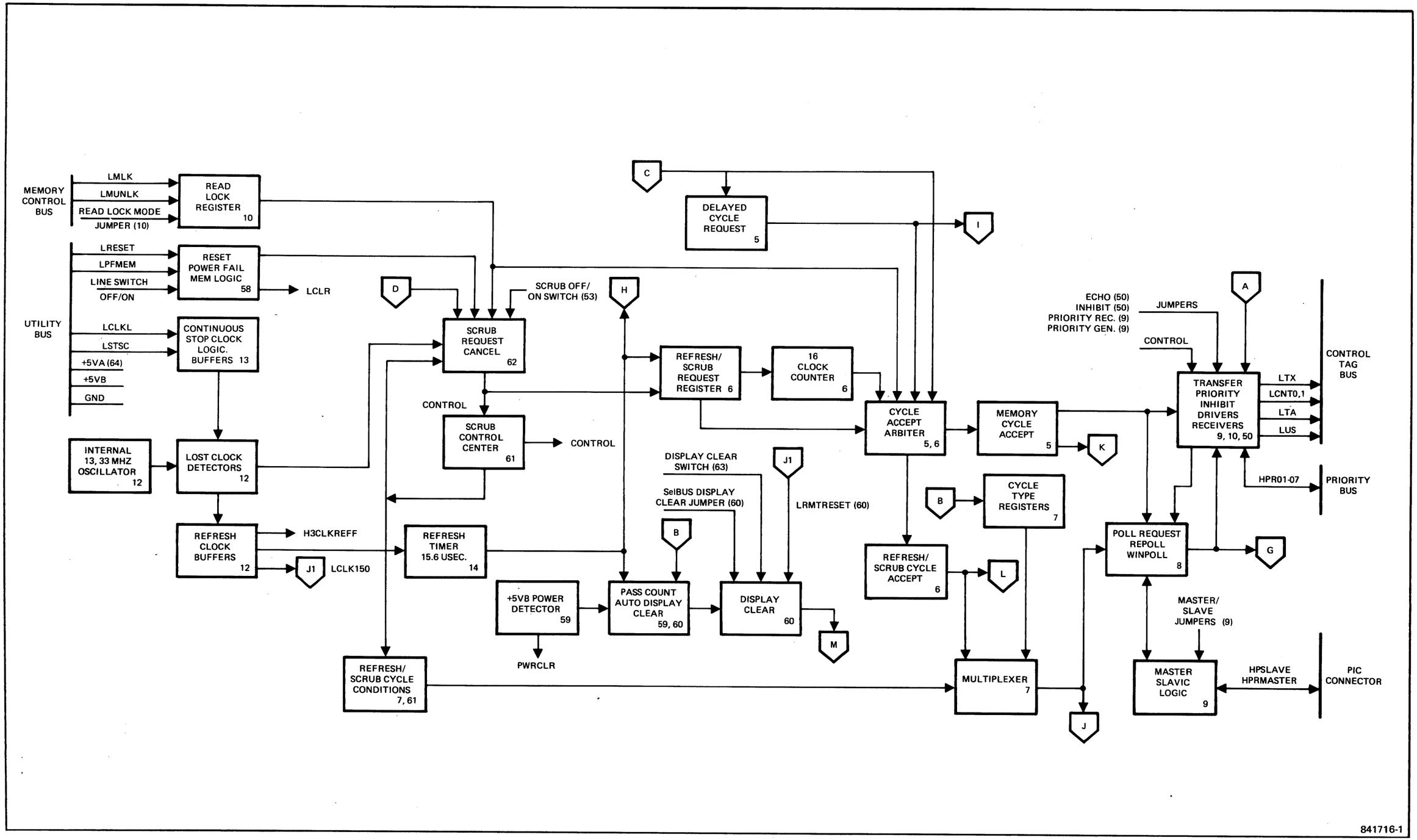
During 600 nanosecond read modify write cycles (write byte or halfword, scrub write), the LWE signal is enabled in the last 300 nanoseconds of the cycle to write the new data into the memory array.

4.6 Module Address Structure

The module addressing structure is described in detail in the following paragraphs.

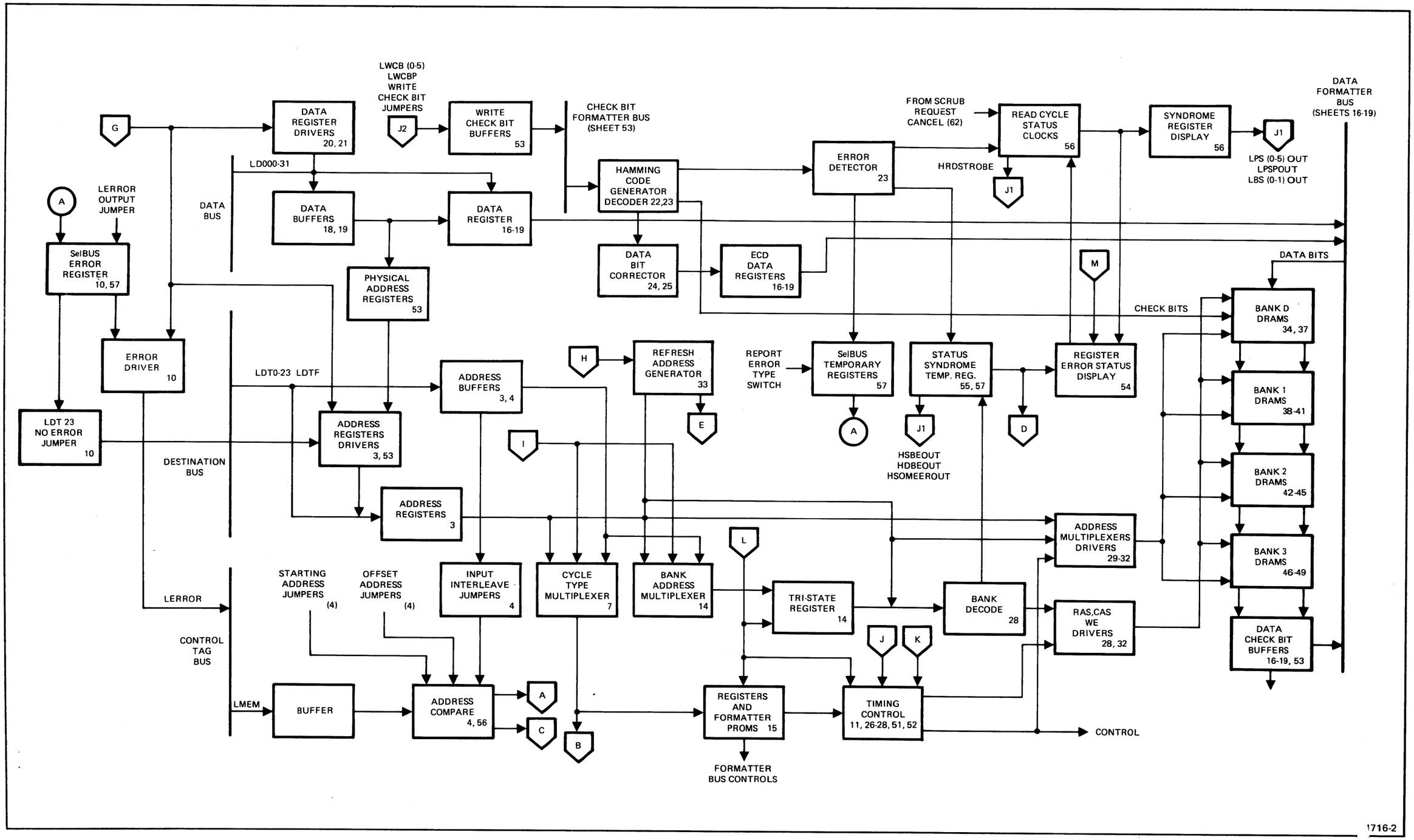
4.6.1 Address Word Structure (Sheets 3, 14, 28 and 29)

The structure of the address word differs between the one Megaword, 512 Kiloword and 256 Kiloword modules as indicated in Table 4-1. Jumpers in the ISM set up the address bits for the different modules. Refer to Table 4-2 for the address bit locations.



ISM Block Diagram (Sheet 1 of 2)

Figure 4-2



ISM Block Diagram (Sheet 2 of 2)

Figure 4–2

Table 4-1. Address Range Bank Locator

160-103723 DASH NO.	MEMORY BANKS			
	BANK 0	BANK 1	BANK 2	BANK 3
-001 1MW 256K DRAM	0XXXXX 4XXXXX 8XXXXX CXXXXX	1XXXXX 5XXXXX 9XXXXX DXXXXX	2XXXXX 6XXXXX AXXXXX EXXXXX	3XXXXX 7XXXXX 8XXXXX FXXXXX
-002 512KW 256K DRAM	0XXXXX 2XXXXX 4XXXXX 6XXXXX 8XXXXX AXXXXX CXXXXX EXXXXX	1XXXXX 3XXXXX 5XXXXX 7XXXXX 9XXXXX BXXXXX DXXXXX FXXXXX	NOT USED	NOT USED
-003 256KW 256K DRAM	XXXXXX	NOT USED	NOT USED	NOT USED
-004 256KW 64K DRAM	X0XXXX X1XXXX X2XXXX X3XXXX	X4XXXX X5XXXX X6XXXX X7XXXX	X8XXXX X9XXXX XAXXXX XBXXXX	XCXXXX XDXXXX XEXXXX XFXXXX

4.6.2 Address Compare (Sheets 4,5,50 and 56)

Jumper assembly X6 is used to select the starting address of the ISM and also to define the high address limit to be compared at the four bit magnitude comparitors.

Jumper assembly X1 is the interleaving jumper which selects the appropriate bits for no interleaving, two way, and four way interleaving options.

When an address match occurs, the HADRSTOP signal is false. The signal LMEM indicates a valid SelBUS transfer to memory.

Table 4-1 is the address range bank locator chart for the ISM. This table assumes the starting address selected is a multiple of the memory module size being used.

Table 4-2. Address Bit Locator

ROW	BANK 0		BANK 1		BANK 2		BANK 3	
	COLUMN		COLUMN		COLUMN		COLUMN	
	K	L	M	N	S	T	V	W
1	0	1	0	1	0	1	0	1
2	2	3	2	3	2	3	2	3
3	4	5	4	5	4	5	4	5
4	6	7	6	7	6	7	6	7
5	8	9	8	9	8	9	8	9
6	10	11	10	11	10	11	10	11
7	12	13	12	13	12	13	12	13
8	14	15	14	15	14	15	14	15
9	16	17	16	17	16	17	16	17
10	18	19	18	19	18	19	18	19
11	20	21	20	21	20	21	20	21
12	22	23	22	23	22	23	22	23
13	24	25	24	25	24	25	24	25
14	26	27	26	27	26	27	26	27
15	28	29	28	29	28	29	28	29
16	30	31	30	31	30	31	30	31
17	C1	C0	C1	C0	C1	C0	C1	C0
18	C3	C2	C3	C2	C3	C2	C3	C2
19	C5	C4	C5	C4	C5	C4	C5	C4
20	--	C6	--	C6	--	C6	--	C6

4.7 SelBUS Interface

The SelBUS physically consists of a multilayer printed wiring board backplane. Table 4-3 contains a list of signals found at connector P1B. Table 4-4 defines the pins on connector P1B used by the ISM.

The SelBUS Interface provides a high speed path between the memory, CPU, and I/O processors. It is a high performance bus that performs at a continuous rate of 26.67 million bytes per second (26.67MB). This rate is derived from the 150 nanosecond master clock, and a 32 bit parallel data path which can transfer four bytes simultaneously.

Table 4-3. SelBUS Pin List (All Signals) (Sheet 1 of 2)

P1B Connector

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	GND	2	GND	63	GND	64	LDT13
3	+5VA	4	+5VA	65	LDT15	66	LDT14
5	LD01	6	LD00	67	LDT17	68	LDT16
7	LD03	8	LD02	69	LDT19	70	LDT18
9	LD04	10	GND	71	LDT21	72	LDT20
11	LD06	12	LD05	73	LDT22	74	NC/GND
13	+5VB	14	LD07	75	LDTF	76	LDT23
15	LD09	16	LD08	77	LREADY	78	GND
17	LD11	18	LD10	79	GND	80	LSYNC
19	GND	20	LD12	81	LCLKE	82	GND
21	LD14	22	LD13	83	GND	84	LCLK
23	+5VB	24	LD15	85	LCLKL	86	GND
25	LD17	26	LD16	87	GND	88	LSTSC
27	LD19	28	LD18	89	+15V	90	+15V
29	LD20	30	GND	91	GND	92	GND
31	LD22	32	LD21	93	GND	94	GND
33	LSCPU	34	LD23	95	-15V	96	-15V
35	LD25	36	LD24	97	LCPUSC	98	GND
37	LD27	38	LD26	99	GND	100	LCLP
39	GND	40	LD28	101	LINH0	102	GND
41	LD30	42	LD29	103	LINH1	104	LRESET
43	+5VB	44	LD31	105	LINH2	106	LCLKOV
45	GND	46	GND	107	LINH3	108	LRTC
47	+5VA	48	+5VA	109	+12VMARG	110	-5VMARG
49	LDT01	50	LDT00	111	GND	112	LPF
51	LDT03	52	LDT02	113	LPFMEM	114	+5VEXT
53	LDT04	54	GND	115	LTRC	116	LMUNLK
55	LDT06	56	LDT05	117	LREFM	118	LERROR
57	LDT08	58	LDT07	119	LECK0	120	LRTRY
59	LDT10	60	LDT09	121	LECK1	122	GND
61	LDT12	62	LDT11	123	LIPUINTR	124	LCHBSY

Table 4-3. SelBUS Pin List (All Signals) (Sheet 2 of 2)

P1B Connector

PIN	FUNC	PIN	FUNC
125	LIPUIPOL	126	LTX
127	LIPUREADY	128	LSIPU
129	LIPUPATTN	130	LTA
131	GND	132	LCNT0
133	LSCPATTN	134	LCNT1
135	LPREF	136	LCPU
137	+5VA	138	+5VA
139	GND	140	GND
141	LPR00	142	LRD
143	HPR01	144	LMEM
145	HPR02	146	GND
147	HPR03	148	LUS
149	HPR04	150	+5VB
151	HPR05	152	LMLK
153	HPR06	154	LIPOL
155	GND	156	LEOIP
157	HPR07	158	LINTR
159	HPR08	160	LIOIN
161	HPR09	162	LEXIN
163	HPR10	164	+5VB
165	HPR11	166	GND
167	HPR12	168	LERRED
169	HPR13	170	LIORST
171	HPR15	172	HPR14
173	HPR17	174	HPR16
175	GND	176	HPR18
177	HPR20	178	HPR19
179	HPR22	180	HPR21
181	+5VA	182	+5VA
183	GND	184	GND

Table 4-4. SelBUS Pin List (ISM Memory Module) (Sheet 1 of 2)

P1B Connector

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	GND	2	GND	63	GND	64	LDT13
3	+5VA	4	+5VA	65	LDT15	66	LDT14
5	LD01	6	LD00	67	LDT17	68	LDT16
7	LD03	8	LD02	69	LDT19	70	LDT18
9	LD04	10	GND	71	LDT21	72	LDT20
11	LD06	12	LD05	73	LDT22	74	
13	+5VB	14	LD07	75	LDTF	76	LDT23
15	LD09	16	LD08	77		78	GND
17	LD11	18	LD10	79	GND	80	
19	GND	20	LD12	81		82	GND
21	LD14	22	LD13	83	GND	84	
23	+5VB	24	LD15	85	LCLKL	86	GND
25	LD17	26	LD16	87	GND	88	LSTSC
27	LD19	28	LD18	89		90	
29	LD20	30	GND	91	GND	92	GND
31	LD22	32	LD21	93	GND	94	GND
33		34	LD23	95		96	
35	LD25	36	LD24	97		98	GND
37	LD27	38	LD26	99	GND	100	
39	GND	40	LD28	101	LINH0	102	GND
41	LD30	42	LD29	103	LINH1	104	LRESET
43	+5VB	44	LD31	105	LINH2	106	
45	GND	46	GND	107	LINH3	108	
47	+5VA	48	+5VA	109		110	
49	LDT01	50	LDT00	111	GND	112	
51	LDT03	52	LDT02	113	LPFMEM	114	
53	LDT04	54	GND	115		116	LMUNLK
55	LDT06	56	LDT05	117		118	LERROR
57	LDT08	58	LDT07	119	LECK0	120	
59	LDT10	60	LDT09	121	LECK1	122	GND
61	LDT12	62	LDT11	123		124	

Table 4-4. SelBus Pin List (ISM Memory Module) (Sheet 2 of 2)

P1B Connector

PIN	FUNC	PIN	FUNC
125		126	LTX
127		128	
129		130	LTA
131	GND	132	LCNT0
133		134	LCNT1
135		136	
137	+5VA	138	+5VA
139	GND	140	GND
141	LPR00	142	LRD
143	HPR01	144	LMEM
145	HPR02	146	GND
147	HPR03	148	LUS
149	HPR04	150	+5VB
151	HPR05	152	LMLK
153	HPR06	154	
155	GND	156	
157	HPR07	158	
159	HPR08	160	
161		162	
163		164	+5VB
165		166	GND
167		170	
169		172	
171		174	
173		176	
175	GND	178	
177		180	
179		182	+5VA
181	+5VA	184	GND
183	GND		

4.7.1 Read and Write Cycle Time (Sheets 7, 15)

The F and C bits along with the control bits are decoded to determine whether the next cycle is a read or write transfer. The decoded outputs, read or write, are then sent to the data formatter PROMs (Sheet 15). Refer to Chapter 3, (SelBUS Transfers and Operations) for a detailed description of read and write transfer operations.

4.7.2 Polling and Transfers (Sheets 8, 9, 20, 21, and 50)

This logic performs priority polling for the SelBUS and enables the bus data out bytes to the SelBUS during a Data Return Transfer (DRT).

When a read cycle is initiated, the signal HFPOLL is generated which allows the ISM to poll the SelBUS. On completion of the polling cycle, if the poll is won the LSBOUTEN signal is generated.

If the poll is lost for a request, a second read cycle is initiated, HWAITPOLL is generated to inhibit the memory. No further memory cycles can be initiated until the poll is won and the first request has been sent on the SelBUS.

If a transfer is sent to the ISM but the ISM is busy and cannot accept the transfer, an unsuccessful (LUS) is issued to the originating device in response to the transfer. Inhibit lines (LINH0-3) are used to notify other devices not to initiate a new SelBUS poll because the ISM is currently busy.

4.7.3 Data Formatter PROMs (Sheets 53, 15, 16-19)

The data formatter is responsible for shifting the data bytes to conform to the SelBUS specification. On the SelBUS, all byte and halfword transfers are right justified and unused bytes are zero filled. During read modify write cycles the data formatter merges the bytes read from memory with the bytes received in the write transfer.

During fullword read and write transfers, the formats are unaltered. For a byte read DRT the addressed byte is selected by the byte three formatter and bytes 0, 1 and 2 are zero filled. For a halfword read DRT, the two addressed bytes (0 and 1 or 2 and 3) are selected by the byte two and byte three formatters and bytes zero and one are zero filled. Refer to Table 4-5 which defines the data formatter PROMs.

When a byte write is received, the byte transferred is always in the byte three position. The formatter loads the byte into its proper position and the remaining three bytes are filled with the data read from the storage module. For example; to write byte one into memory, the byte one formatter selects the byte three output from the write data latches. Bytes zero, two, and three are read from the storage module and clock to buffers for the write portion of the cycle. Halfword write cycles are accomplished in a similar manner. The halfword is received in bytes two and three. The formatter places the bytes in their appropriate positions, and the remaining two bytes (zero and one) are filled with the data bytes read from the storage module.

Table 4-5. ISM Data Formatter PROM (15E22) (Write Cycle Controls) (Sheet 1 of 2)

Hex pin	Address A4 14	A3 13	A2 12	A1 11	A0 10	Data B7 9	B6 7	B5 6	B4 5	B3 4	B2 3	B1 2	B0 1	Hex	Function
0	0	0	0	0	0	0	0	0	0	0	0	0	0	00	
1	0	0	0	0	1	0	0	0	0	0	0	0	0	00	
2	0	0	0	1	0	0	0	0	0	0	0	0	0	00	
3	0	0	0	1	1	0	0	0	0	0	0	0	0	00	
4	0	0	1	0	0	0	0	0	0	0	0	0	0	00	
5	0	0	1	0	1	0	0	0	0	0	0	0	0	00	
6	0	0	1	1	0	0	0	0	0	0	0	0	0	00	
7	0	0	1	1	1	0	0	0	0	0	0	0	0	00	Scrub Cycle
8	0	1	0	0	0	0	0	0	0	0	0	0	0	00	
9	0	1	0	0	1	0	0	0	0	0	0	0	0	00	
A	0	1	0	1	0	0	0	0	0	0	0	0	0	00	
B	0	1	0	1	1	0	0	0	0	0	0	0	0	00	
C	0	1	1	0	0	0	0	0	0	0	0	0	0	00	
D	0	1	1	0	1	0	0	0	0	0	0	0	0	00	
E	0	1	1	1	0	0	0	0	0	0	0	0	0	00	
F	0	1	1	1	1	0	0	0	0	0	0	0	0	00	
10	1	0	0	0	0	0	0	0	0	0	0	1	1	03	Read byte 3
11	1	0	0	0	1	0	0	0	0	0	0	0	1	01	Read right half
12	1	0	0	1	0	0	0	0	0	0	0	1	1	03	Read byte 2
13	1	0	0	1	1	0	0	0	0	0	0	0	0	00	Read word(full/mult.)
14	1	0	1	0	0	0	0	0	0	0	0	1	1	03	Read byte 1
15	1	0	1	0	1	0	0	0	0	0	0	0	1	01	Read left half
16	1	0	1	1	0	0	0	0	0	0	0	1	1	03	Read byte 0
17	1	0	1	1	1	0	0	0	0	0	0	0	0	00	Read word (full)
18	1	1	0	0	0	0	0	0	0	1	0	0	0	08	Write byte 3
19	1	1	0	0	1	0	0	0	0	1	1	0	0	0C	Write right half
1A	1	1	0	1	0	1	0	0	0	0	0	0	0	80	Write byte 2
1B	1	1	0	1	1	0	0	0	0	1	1	0	0	0C	Write word
1C	1	1	1	0	0	0	1	0	0	0	0	0	0	40	Write byte 1
1D	1	1	1	0	1	0	1	0	1	0	0	0	0	50	Write left half
1E	1	1	1	1	0	0	0	1	0	0	0	0	0	20	Write byte 0
1F	1	1	1	1	1	0	0	0	0	1	1	0	0	OC	Write word

Table 4-5. ISM Data Formatter PROM (15E23)
(Read Cycle ECC Output Controls) (Sheet 2 of 2)

Hex pin	Address A4 14	A3 13	A2 12	A1 11	A0 10	Data B7 9	B6 7	B5 6	B4 5	B3 4	B2 3	B1 2	B0 1	Hex	Function
0	0	0	0	0	0	1	1	1	1	0	0	0	0	F0	
1	0	0	0	0	1	1	1	1	1	0	0	0	0	F0	
2	0	0	0	1	0	1	1	1	1	0	0	0	0	F0	
3	0	0	0	1	1	1	1	1	1	0	0	0	0	F0	
4	0	0	1	0	0	1	1	1	1	0	0	0	0	F0	
5	0	0	1	0	1	1	1	1	1	0	0	0	0	F0	
6	0	0	1	1	0	1	1	1	1	0	0	0	0	F0	
7	0	0	1	1	1	1	1	1	1	0	0	0	0	F0	Scrub Cycle
8	0	1	0	0	0	1	1	1	1	0	0	0	0	F0	
9	0	1	0	0	1	1	1	1	1	0	0	0	0	F0	
A	0	1	0	1	0	1	1	1	1	0	0	0	0	F0	
B	0	1	0	1	1	1	1	1	1	0	0	0	0	F0	
C	0	1	1	0	0	1	1	1	1	0	0	0	0	F0	
D	0	1	1	0	1	1	1	1	1	0	0	0	0	F0	
E	0	1	1	1	0	1	1	1	1	0	0	0	0	F0	
F	0	1	1	1	1	1	1	1	1	0	0	0	0	F0	
10	1	0	0	0	0	1	0	0	0	0	0	0	0	80	Read byte 3
11	1	0	0	0	1	1	1	0	0	0	0	0	0	C0	Read right half
12	1	0	0	1	0	0	0	0	0	1	0	0	0	08	Read byte 2
13	1	0	0	1	1	1	1	1	1	0	0	0	0	F0	Read word(full/mult.)
14	1	0	1	0	0	0	0	0	0	0	1	0	0	04	Read byte 1
15	1	0	1	0	1	0	0	0	0	0	1	0	1	05	Read left half
16	1	0	1	1	0	0	0	0	0	0	0	1	0	02	Read byte 0
17	1	0	1	1	1	1	1	1	1	0	0	0	0	F0	Read word (full)
18	1	1	0	0	0	0	1	1	1	0	0	0	0	70	Write byte 3
19	1	1	0	0	1	0	0	1	1	0	0	0	0	30	Write right half
1A	1	1	0	1	0	1	0	1	1	0	0	0	0	B0	Write byte 2
1B	1	1	0	1	1	0	0	0	0	0	0	0	0	00	Write word
1C	1	1	1	0	0	1	1	0	1	0	0	0	0	D0	Write byte 1
1D	1	1	1	0	1	1	1	0	0	0	0	0	0	C0	Write left half
1E	1	1	1	1	0	1	1	1	0	0	0	0	0	E0	Write byte 0
1F	1	1	1	1	1	0	0	0	0	0	0	0	0	00	Write word

4.8 Timing

The following paragraphs describe the various timing functions necessary for ISM operation.

4.8.1 Memory Cycle Accept (Sheet 5, 11)

The Memory Cycle Accept timing logic accepts all of its inputs from internal timing logic areas with the exception of the HME which is generated by the SelBUS logic.

The memory accept logic accepts and starts delayed and normal memory cycles and clears the start cycle. A delayed cycle is a SelBUS request which was accepted by the ISM while it was busy on a current request.

If the ISM is empty and a memory transfer is received, it is routed through and a memory cycle is started (LMCYCSTART). If the ISM is not empty and cannot accept a request, flip-flop HFACCDEL is set to indicate a transfer is stored and waiting to be processed.

The clocks H3CLKBD1, H3CLKBD2, and H3CLKBD3 remain high and retain the data in the address and data formatter registers from the SelBUS when the memory cannot win the poll and performs a DRT transfer onto the SelBUS. The H3 clock memory cycle (H3CLKCYC) clocks data from the SelBUS into memory at the start of each memory cycle. H3CLKADVADR advances the source address.

4.8.2 Refresh Cycle Accept (Sheet 6)

The referesh cycle accept logic accepts and starts the refresh cycle. The HREFREQIN signal sets HFREFLTH to request a refresh cycle. The counter allows a refresh to wait up to 16 clock cycles before it will demand a refresh cycle by generating wait for refresh (LWAITREF).

HFREFREQ will be reset if at any time before the 16 clocks the ISM has an idle period where a refresh cycle can be performed.

4.8.3 Memory Inhibit (Sheets 11, 50)

The memory inhibit logic allows accepted memory read and write cycles to take place and inhibits new accesses to memory once the memory buffers are full.

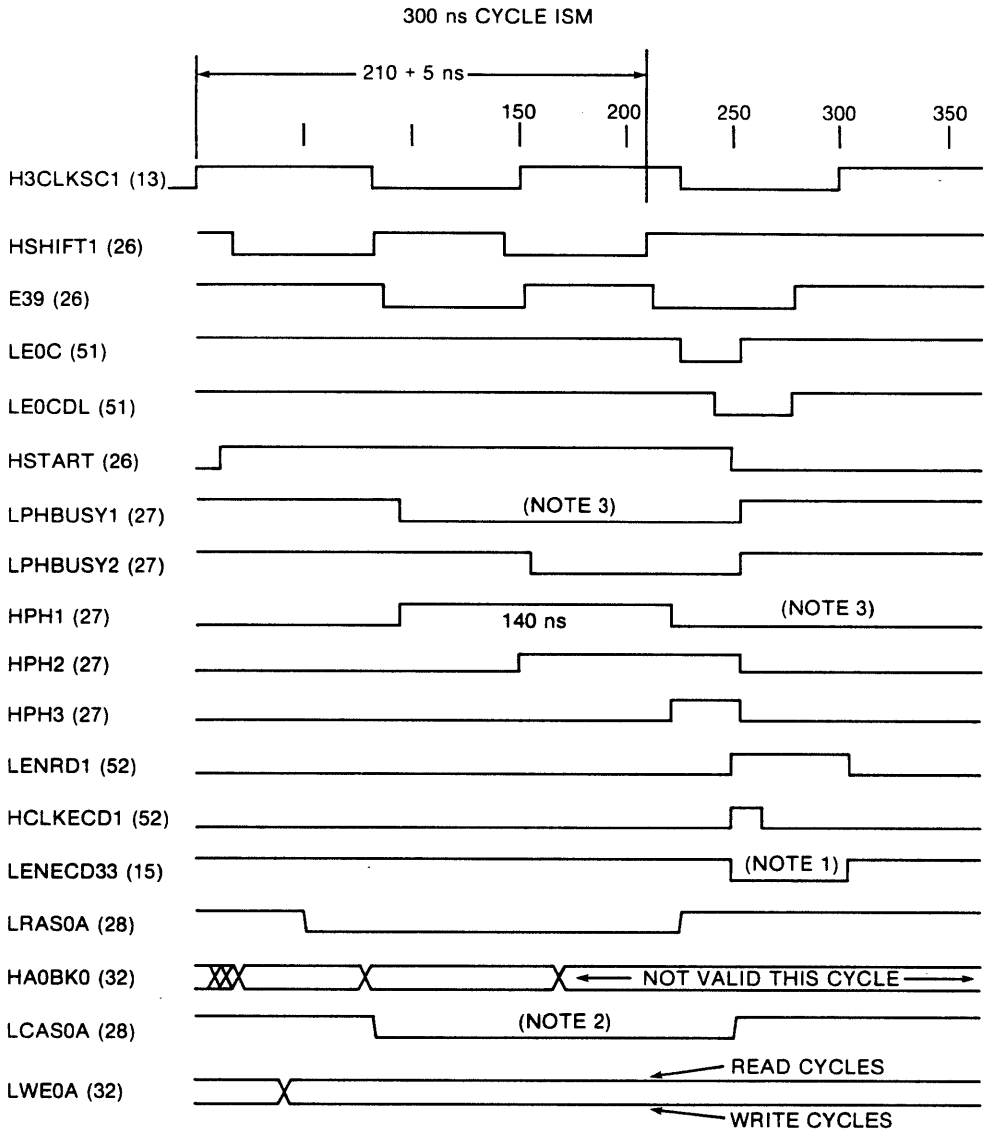
The signals which are responsible for generating the set inhibit (LSETINH) are: power fail (HFPFMEM), delayed cycle (HFACCDEL), and wait lost poll (HWAITPOLL).

4.8.4 Module Reset (Sheet 58)

The ISM module can be reset either through the on board switch S5 or through the LRESET signal located at connector P1B-104.

4.8.5 Phase and Sub-Phase Timing Logic (Sheets 26,27)

The phase timing (Sheet 27), and the sub-phase timing (Sheet 26) provide the timing for the 300 nanosecond read and fullword write cycles (refer to timing diagram Figure 4-3). This same logic provides the timing for the 600 nanosecond byte/halfword write cycles (refer to timing diagram Figure 4-4). The start memory cycle signal (LMCYCSTART) is responsible for generating the HSTART and LSTART signals.



NOTE 1. GOES LOW FOR READ CYCLE ONLY.

2. STAYS HIGH FOR REFRESH CYCLE.

3. MULTIPLY NUMERICAL VALUE OF MNEMONIC BY 70 ns FOR APPROXIMATE EDGE TIMES.

4. NUMBERS IN PARENTHESIS INDICATE ASSOCIATED LOGIC SHEET.

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Figure 4-3. 300 nsec Timing Diagram

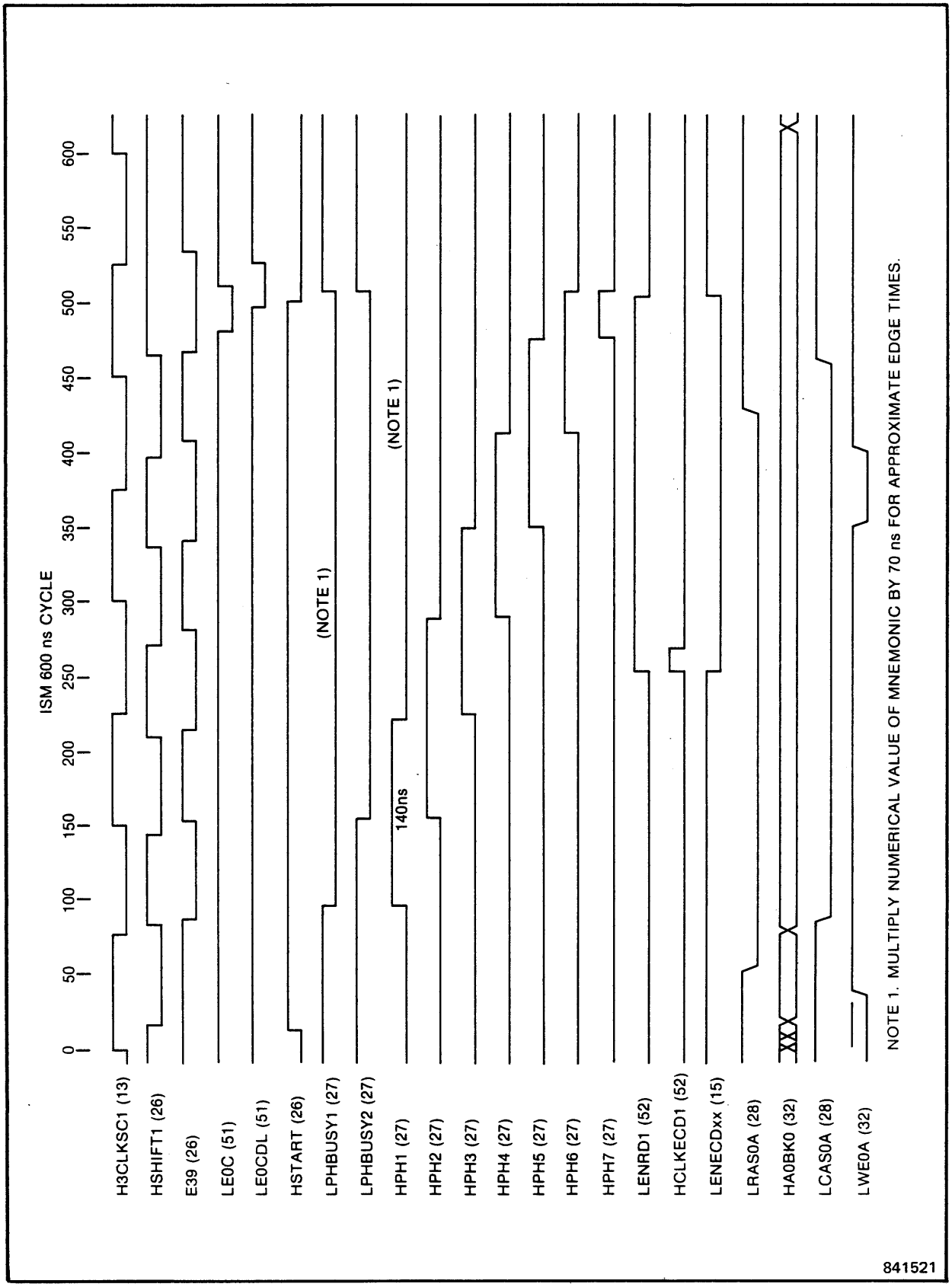


Figure 4-4. 600 nsec Timing Diagram

4.8.6 Continuous Clocks and Power Fail (Sheets 12, 58)

The operation of the ISM is synchronized to the reference signal H3 clock. As their names imply, these clocks run continuously, even in the stop mode.

The power fail signal is synchronized to the H3 clock on board. This signal is true when +5VA power fails and is used to disable the scrubbing circuits.

4.8.7 Stop Clock Clocks (Sheet 13)

The stop clock mode is a test mode that allows the SelBUS clock (LCLKL) to be single stepped through each clock cycle. This test mode is not available unless a development support system is installed. During normal operation of the memory the stop clock clocks operate as continuous clocks.

4.8.8 Formatter Timing (Sheet 52)

The formatter timing circuits control the enable and clocks to the formatter circuits. During read cycles, LENRD gates the read data from the memory arrray. When data is available, HENATECD register is set to hold the corrected data in the formatter bus and HCLKSTAT and HCLKECD signals clock the data into the formatter registers.

4.8.9 Display Clear (Sheets 59, 60)

When +5VB power is turned on, the ISM resets its internal circuits (LPWRCLR). The auto clear display circuits (Sheet 60) are also reset.

The memory contains random data when power is applied and any single-bit errors are corrected by the scrubbing circuits automatically. Double-bit errors in memory are not corrected and remain in the memory module. The display circuits on the front of the ISM will indicate these errors.

It is the responsibility of the program or the operator to write and clear the memory module before reading any locations in the memory. Otherwise, a double-bit error is reported to the SelBUS with the LERROR signal.

The auto clear circuits monitor all memory cycles performed and will automatically clear the LEDs when it detects that no double-bit errors remain in the ISM. The refresh circuits perform a fullword read to all locations in the memory. If a double-bit error (DBE) is detected, a flip-flop is set to indicate a DBE was detected. This flip-flop is reset every time HPASS signal occurs.

4.9 Refresh and Scrubbing

The following paragraphs describe the refresh and scrubbing operations.

4.9.1 Address Generation (Sheet 33)

The address generator holds the next address in memory to be used by the refresh circuits. Twenty address bits are required to perform a fullword read during refresh.

4.9.2 Refresh (Sheets 6, 14, 28)

The refresh logic refreshes one of the 256 rows in each of the banks of the DRAM chips once every 15.6 microseconds. This is equivalent to refreshing the same row address once every 4 milliseconds. Counters count 104 clocks and signal a request for a refresh cycle.

The refresh logic must wait for the completion of a memory cycle before it can initiate a refresh cycle. The 4-bit synchronous binary counter allows the refresh logic to wait a maximum of 16 clocks before forcing a refresh cycle.

The ISM refresh circuits also peforms a full word read to one of the four banks in the ISM. The fullword read is analyzed for correct data and processed with the following criteria and actions.

If no error is detected, no further action is taken. The next sequential address is used for the next refresh cycle.

If a double-bit error is detected, the memory will illuminate the DBE LED display and no further action is taken.

If a single-bit error is detected, the ISM, in normal operation, sets the request scrub flip-flop (sheet 62) which enables the scrubbing circuits to operate as described in the next section.

4.9.3 Scrubbing (Sheets 61, 62)

Scrubbing is a feature in the ISM which corrects soft errors as they occur in the ISM. A soft error is a correctable single-bit error. The scrubbing action prevents single-bit errors from accumulating in the memory which would decrease the reliability of the memory since single-bit errors can convert into double-bit errors if another bit changes in value.

The ISM does not perform a scrub cycle unless it is required by the refresh circuits through the HFREQSCRUB flip-flop (see the previous section). If HFREQSCRUB is true the ISM goes through the scrubbing procedure as follows.

1. The inhibit line LINH0-3 is set true on the SelBUS. This stops additional transfers from being accepted by the ISM.
2. As soon as any current cycles are completed, the ISM performs a 600 nanosecond fullword scrub read modify write cycle. The ISM reads the same location that was refreshed earlier. It checks for incorrect data again.
3. If a single-bit error is detected, it continues with the read modify write cycle and inverts the incorrect bit in the write portion of the cycle (LWE low on the DRAM chip).

   If however, a double-bit error is detected, it disables the read modify write cycle by keeping the write enable LWE signal false. This prevents the uncorrected double-bit error data from being changed. (This feature allows a CPU read to detect a catastrophic double-bit error properly.)

4. Whether or not the read modify write cycle in the above step detects a single or double-bit error, the scrubbing circuits now perform a 300 nanosecond fullword read cycle ("read recheck read" in the timing diagram).
5. The read recheck cycle checks to see if the error that caused the scrubbing has in fact been corrected. If no error is detected during the read cycle, the SOFT LED display is illuminated and the scrub cycle is complete.

   If an error is detected during the read cycle, the HARD LED display is illuminated and the scrub cycle is complete.

Figure 4-5 is a timing diagram illustrating the fastest time for a refresh cycle which has detected a single-bit error. The scrubbing 600 nanosecond cycle and the read refresh cycle are also illustrated.

Figure 4-6 is a flow chart for normal scrubbing 600 nanosecond cycles. The conditions for illuminating the LED displays is also illustrated.

4.10 Error Correction

The ISM contains circuitry to detect and correct single bit errors and detect and report double bit errors. On board LEDs are employed to report these errors. The following paragraphs describe the error correction functions.

4.10.1 Modified Hamming Code Theory (Sheet 66)

The hamming code is a widely used method of generating an internal error correction code. The following paragraphs describe its generation and use within the ISM.

Figure 4-7 shows four signal lines labelled 2^0, 2^1, 2^2, and 2^3 which carry binary bits 1, 2, 4, and 8 to and from a hypothetical storage device which is clocked by LCLK. These lines are listed in the table within Figure 4-7 as signal input. The hamming number for each line is one plus the corresponding exponent of 2 which designates the signal line.

Three parity generator/checkers (PG/Cs) are used, one for each bit in the hamming number. PG/C4 monitors the 2^3 line only since bit 4 is a one only in the binary hamming number for that signal input. PG/C2 monitors the 2^1 and 2^2 lines since bit two in the binary hamming number is a one for the 2^1 and 2^2 signal inputs. PG/C1 monitors 2^0 and 2^2 lines since bit one in the binary hamming number is a one for the 2^0 and 2^2 signal lines. The signal output of each PG/C is stored in a flip-flop when LCLK clocks the word on the signal line into storage. The output of the flip-flop is presented to an AND gate. The AND gates are inhibited during write operations when parity bits are generated, and are enabled during read operations when parity is checked. Parity bits P4, P2, and P1 correspond to the binary hamming number as illustrated in Figure 4-7.

For example, assume that a decimal five is written into storage and odd parity is generated. Column A in the table shows the true and false inputs on the signal lines of each PG/C. PG/C4 stores a one since the 2^3 bit is a zero, PG/C2 stores a zero since it sees only the 2^2 bit as a one, and PG/C1 stores a one since it sees ones in both the 2^0 and 2^2 bits.

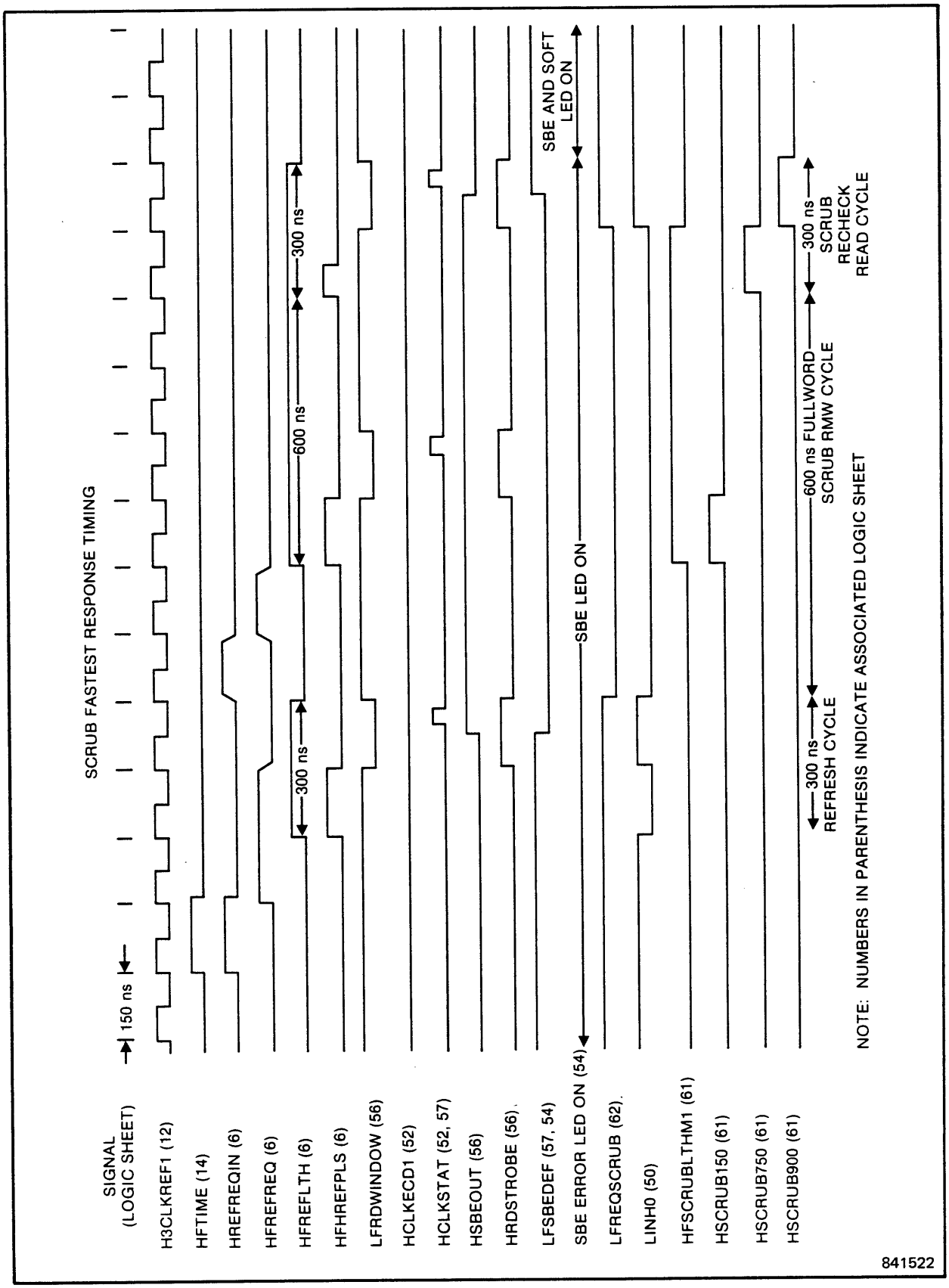


Figure 4-5. Refresh Fastest Time Timing Diagram

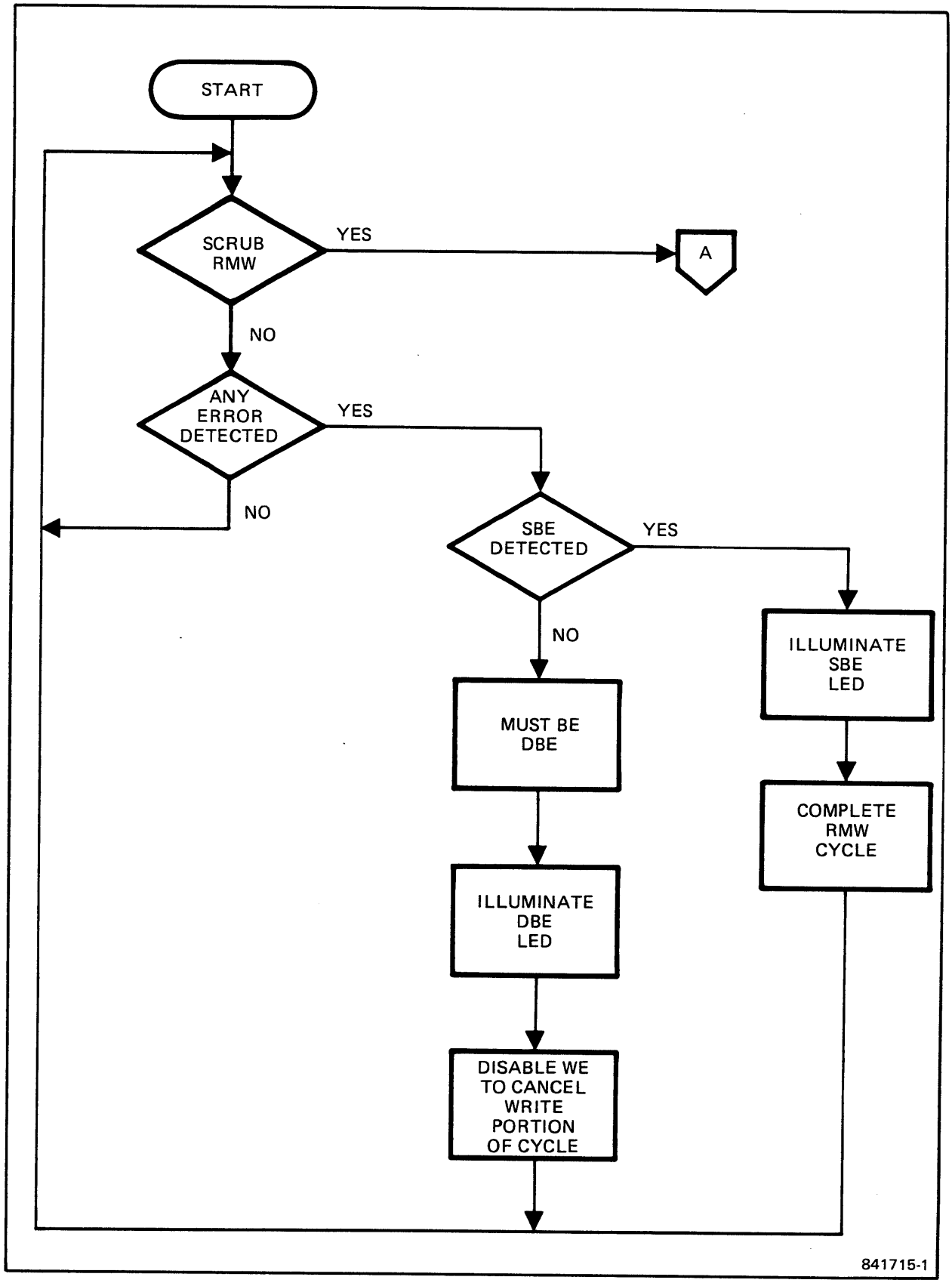


Figure 4–6. Scrubbing RMW Flow Chart (Sheet 1 of 2)

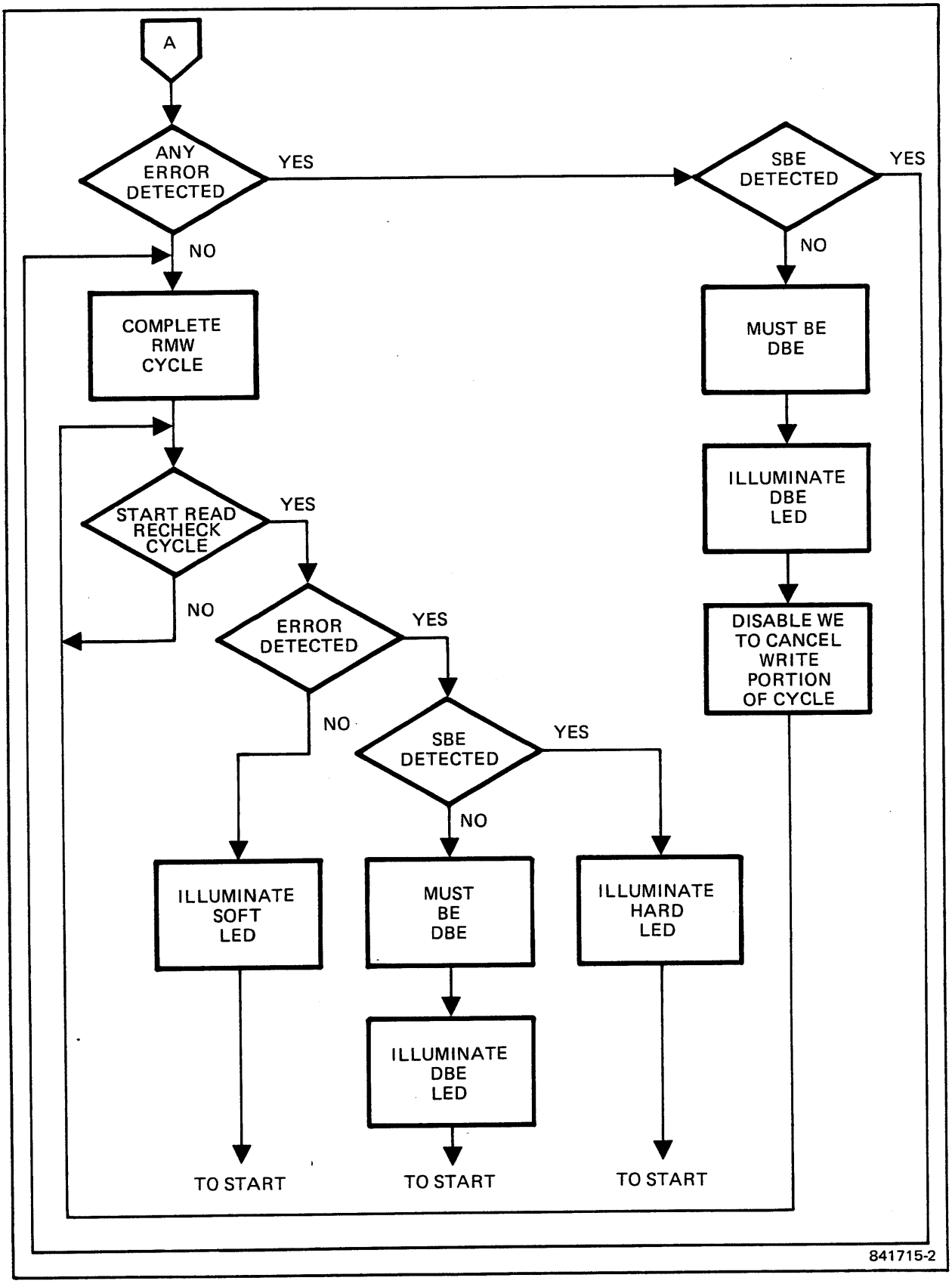
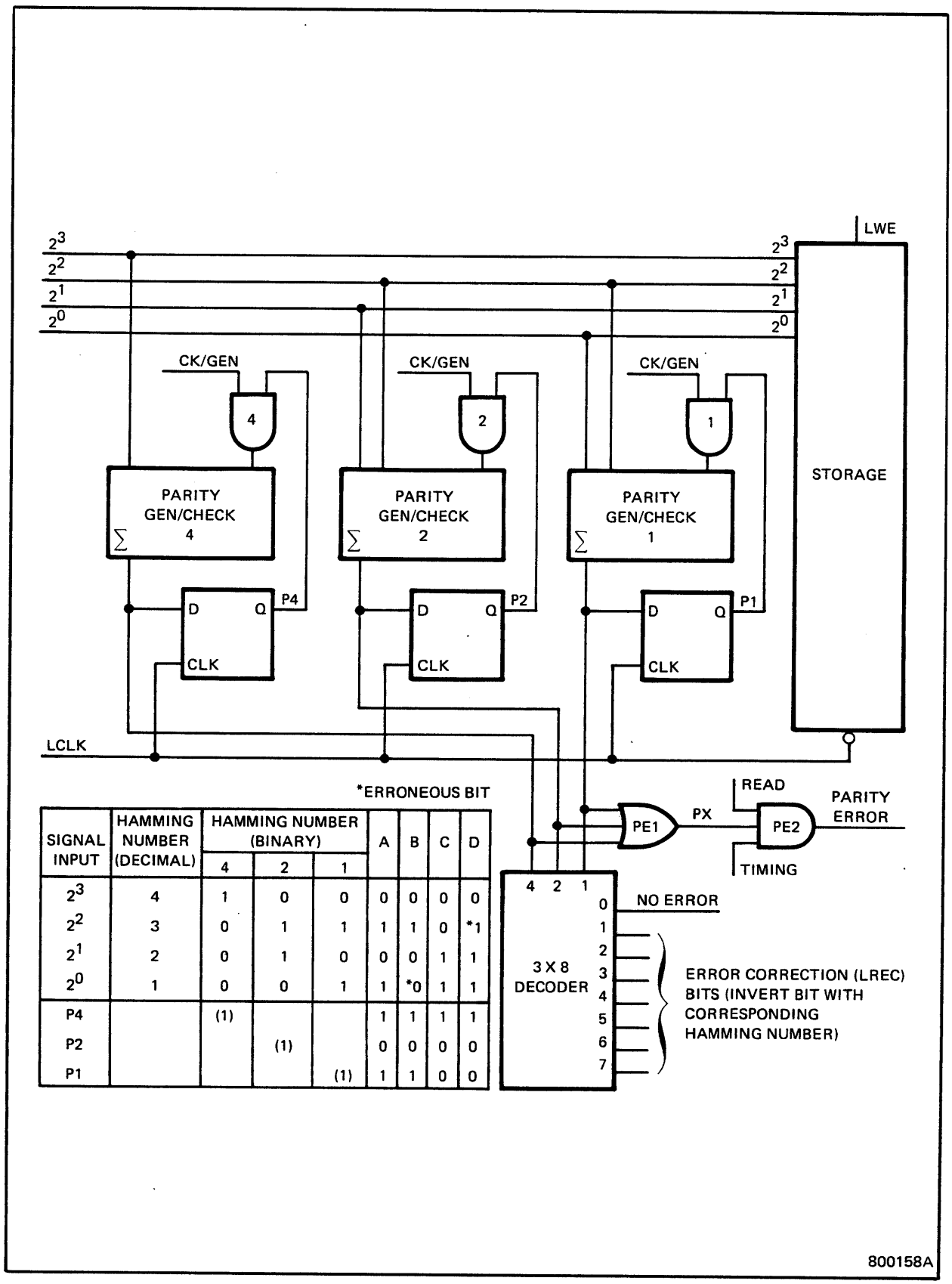


Figure 4-6. Scrubbing RMW Flow Chart (Sheet 2 of 2)



SIGNAL INPUT	HAMMING NUMBER (DECIMAL)	HAMMING NUMBER (BINARY) 4	2	1	A	B	C	D
2^3	4	1	0	0	0	0	0	0
2^2	3	0	1	1	1	1	0	*1
2^1	2	0	1	0	0	0	1	1
2^0	1	0	0	1	1	*0	1	1
P4		(1)			1	1	1	1
P2			(1)		0	0	0	0
P1				(1)	1	1	0	0

Figure 4-7. Modified Hamming Code Block Diagram

In the read operation, AND gates four, two, and one are enabled, allowing the parity bits to be checked when LCLK clocks the word out of storage. Assume that the one in the 2^0 bit is dropped in the storage device as shown in column B. Upon readout and parity check PG/Cs 4 and 2 will not have parity error (PE) outputs since both will correctly detect odd parity. They will both write zeros into the 3 by 8 decoder. PG/C1 will, however, have a PE output and will write one into the decoder since it sees ones in only two bits (2^2 and P1), which constitute even parity. The PE passes through OR gate PE1 and enables AND gate PE2. The output of PE2 can be used to advance a counter and thus accumulate the number of detected parity errors.

The 3 by 8 decoder provides binary to unitary conversion. It decodes the binary hamming code input and puts out a one on the zero output if there is no PE, or it will put out a one on the decimal numbered output line as indicated by the binary input. In the example, where the one in the 2^0 bit has been dropped, binary 1 is decoded and places a one on the 1 output of the decoder. This corresponds to the Hamming number. The output of the decoder is the error correction bit which will place a one in the 2^0 bit when the word is reread. The PE indication will signal the CPU indicating the necessity of a reread operation. The erroneous zero in the 2^0 bit will be inverted to a one by the exclusive OR gate logic.

A second example is as follows: Assume that a decimal 3 is written into storage as indicated in column C of the table. As in the first example, odd parity will be generated and checked. PG/C4 will store a one since it sees only the 2^3 input which is zero. PG/C2 will store a zero since it sees a one in the 2^0 input and a zero in the 2^2 input. PG/C1 will store a zero since it sees a one in the 2^0 bit input and a zero in the 2^2 bit input. Now assume that the 2^2 bit is erroneously changed from a zero to a one when the word is read out of storage and a parity check is made. This is shown in Column D of the table. The AND gates are enabled to allow the parity bits to be checked. PG/C4 will not have PE since it will see only the P4 bit, and it will write a zero into the decoder. PG/C2 and PG/C1 will both detect parity errors by the presence of an erroneous one on the 2^2 line which they both monitor. PG/C2 and PG/C1 will write ones into the decoder. A resulting one on output 3 of the decoder will invert the erroneous one on the 2^2 line which bears Hamming number 3.

4.10.2 Error Correction Code (ECC) Structure (Sheets 22-25, 53)

Figure 4-8 is a simplified block diagram of the parity generation/checking circuitry and the error correction logic for the ISM.

For parity generation/checking and error correction, the 32 bit word is divided in 5 segments. These segments are two, three, four, five, and seven and are composed of eight, seven, or two bits each. The bit composition is defined in Table 4-7. In addition, a sixth segment is composed of check bits C0 through C5 and CP. This sixth segment is not numbered.

The check bits, listed in the left hand column of Table 4-7 are generated and stored during a write cycle. The Xs in the same horizontal row indicate the data bits used in the generation of the check bits. For example, check bit CO is generated by applying the LFDxx bits indicated by Xs in the first row. These parity generator circuits combine in an exclusive OR circuit to compose a 17 input exclusive OR. The output is the write data check bit (LWDC0). It is written into RAM storage with the data bits when LWEx goes true.

LWDC0-5 and LWDCP are generated by the PG/C circuits on sheets 22 and 23.

Table 4-7. Check Parity Matrix

Check Bit	Byte 3								Byte 5								Byte 7	Byte 2							Byte 7	Byte 4														Number of Bits
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	C0	C1	C2	C3	C4	C5	CP	
0		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X							17
1			X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X		X					17
2					X	X	X	X					X	X	X	X					X	X	X	X	X				X	X	X	X			X					17
C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								X											X					19
4	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X												X				18
5									X	X	X	X	X	X	X	X	X								X	X	X	X	X	X	X	X						X			18
P	X			X		X	X		X			X			X	X		X	X		X				X	X	X		X			X							X	18

NOTE: The byte number indicated above corresponds to the binary value of syndrome bits 5, 4, and 3 which the decoder selected for error correction.

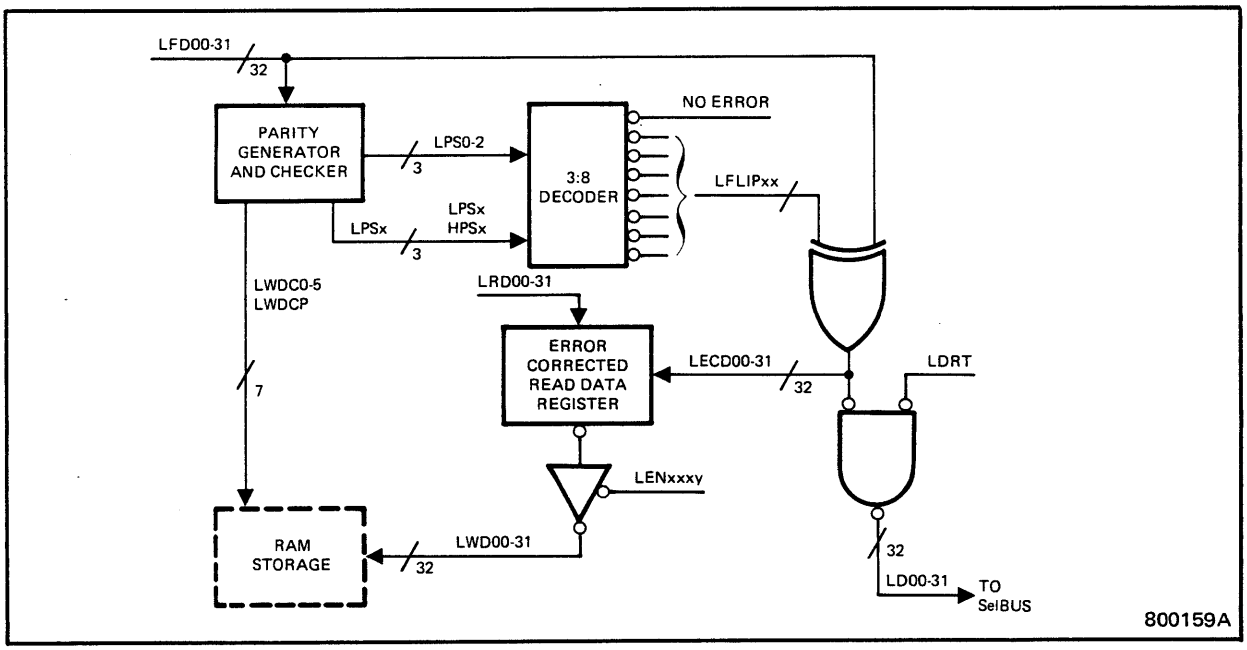


Figure 4-8. Error Correction Simplified Block Diagram

4.10.2.1 Parity Syndrome Check Bits (Sheets 24 and 25)

The PG/C circuits and associated exclusive OR circuits also generate the 11 parity syndrome check bits, LPS0,1,2,3,4,5,P, and HPS2,3,4, and 5. These bits are decoded to produce hamming code error correcting bits when errors are detected in data read from storage. These bits are presented to the decoder circuits on sheets 24 and 25 of the logic diagrams.

LPS0-2 forms a three-bit binary word which is presented to the A, B, and C select inputs of each of the four decoders. The balance of the parity syndrome check bits are applied to the decoder enable inputs (G1, G2A, and G2B). One of the eight outputs of each decoder will be true. The enable inputs to each decoder are arranged to that if no error is detected in the byte, all outputs are high.

Table 4-8 defines how the parity syndrome check bits are decoded. The eight possible binary words formed by LPS0-2 are shown at the head of the columns. The binary words formed by the permutations of the other parity syndrome bits are shown on the left-hand side of each row. For example, if LPS0-2 forms a binary four and LPS3-5 form a binary three, LFD04 is in error and will be inverted. Note that binary 6 is never presented to the enable inputs of the decoders due to the fact that there is no byte 6 decoder.

4.10.3 Error Reporting (Sheet 23)

The following description of the error reporting operation is based on the simplified block diagram provided in Figure 4-8.

Parity syndrome bits LPS0 through LPS5, and LPSP are applied to the parity generator and a NAND gate. If any of the syndrome bits are low, HSOMEERROR is generated from the output of the NAND gate which keeps the signal low. The data signal controls the parity error signal on the SelBUS and when true causes the LERROR signal to be generated on the SelBUS.

Table 4-8. Syndrome Word Decoding Matrix

SYNDROME PATTERN BITS 5,4,3	SYNDROME PATTERN BITS 2,1,0							
	000	001	010	011	100	101	110	111
000	NO ERROR	C0	C1		C2			
001	C3							
010	C4	17	18	19	20	21	22	23
011	00	01	02	03	04	05	06	07
100	C5	25	26	27	28	29	30	31
101	8	9	10	11	12	13	14	15
110								
111	16				24			

If the number of low inputs to the parity generator is odd, the word read from storage contained a single-bit error which has been corrected, and the output HSOMEERROR goes true. If the number of low inputs to the parity generator is even, a double-bit or multiple even bit error is indicated, and the odd parity output HSBEDEF goes true.

Switches S1 through S5 control the displays for error reporting. Refer to Chapter 3 for a detailed description of the control switches.

The displays associated with the error reporting are described in the paragraphs that follow.

4.10.3.1 Error Logger DS2-DS10 (Sheets 55 and 56)

The syndrome bit LEDs S0 through S5 and SP together with the bank select LEDs BS0 and BS1 function as the error logger.

The signal LFRDWINDOW on sheet 56 goes low whenever an internal read cycle occurs in the ISM. The low to high edge of this signal, which occurs 300 nanoseconds after the start of the cycle, is used to generate HCLKSYNDROME to clock an error condition into the error logger on sheet 55.

The error logger is connected to displays DS2 through DS10 which indicate the bank address of the error and the syndrome bit status. The HCLKSTAT signal on sheet 55 temporarily stores the status on each read in registers.

The HCLKSYNDROME, which clocks the error logger, only occurs if the status is to be stored for observation on the displays. The criteria for clocking the error logger is implemented by the logic on sheet 56 and can be described as follows:

Error Condition	Remarks
Hard SBE	Highest priority. First hard error is latched permanently by HCLKSYNDROME. This condition occurs only during the read recheck portion of a scrub cycle.
Soft SBE	First soft SBE condition latched permanently as long as error condition (A) above does not occur. This condition occurs only during the read recheck portion of a scrub cycle.
SBE	The error status for this condition is latched each time it occurs, overriding the previous error status, as long as error conditions (A) or (B) above do not occur.
DBE	The error status for this condition is latched each time it occurs, overriding any previous status, as long as none of the above error conditions occur.

4.10.3.2 Other Status DS11-DS14 (Sheet 54)

The SBE, HARD SBE, SOFT SBE, and DBE LEDs and registers are clocked by LFRDWINDOW whenever an internal read cycle occurs.

No matter what the latched condition is in the syndrome and bank select LEDs (see previous section), the SBE, HARD SBE, SOFT SBE, and DBE LEDs will always be illuminated if an error condition occurs which would illuminate one or more of these LEDs.

4.10.3.3 Sample Display Error Sequence

A sample error sequence is described below to show the operation of the displays.

If a CPU read occurs and a SBE is detected, the SBE LED is illuminated and the syndrome condition latched (assuming the display is blank to start with). If the CPU performs another read to another location and a SBE is again detected, the SBE LED register is clocked again and the new syndrome condition latched (overriding the first SBE).

Then, as the refresh circuits scan the addresses on board, if it detects a SBE it again clocks the SBE LED register, latches the syndrome, and requests a scrub cycle to determine what type of error it is.

During the scrubbing cycle, the ISM first performs a 600 nanosecond cycle to read the data again and rewrite the correct pattern. During the read portion of the 600 nanosecond cycle it checks to verify the SBE and latched the syndrome pattern. The cycle is completed with a write correcting the error.

The ISM then does a recheck read cycle. If an error is detected, the syndrome condition is again latched and the HARD LED is illuminated. This condition will be permanently kept on the LEDs regardless of any future errors detected.

If a SBE or DBE is detected at any time thereafter, the appropriate SBE or DBE LED is illuminated (or left illuminated) but the syndrome is not kept since the higher priority HARD SBE condition has already been recorded.

4.10.3.4 Sample Hamming Code Error Conditions

The following paragraphs describe sample hamming code error conditions and relate them to the syndrome error analysis guide.

Table 4-9 is a syndrome error analysis guide which simplifies analysis of any error clocked into the error logger on the ISM. An explanation of each column in the guide follows:

Column 1 reflects the syndrome code observed in hexadecimal on displays SP (DS8), and S5 (DS7) through S0 (DS2), with S0 being the least significant bit.

Column 2 reflects the parity sum reflected by the code in Column 1, OBE for odd bit error and EBE for even bit error.

If the parity sum (number of ones in column 1) is odd, one or more odd bits are in error. Column 2 indicates OBE for this condition. A single-bit error is a subset of this condition and is the most probable error if an OBE is detected.

If the parity sum of column 1 is even, two or more even bits are in error. Column 2 indicates EBE for this condition. A DBE (double-bit error) is a subset of this condition, and is the most probable error if an even bit error has been detected.

It should be noted that some even bit error conditions may flip a data bit even though the data bit is not in error. For example, if bits 8 and 24 are in error, a hex code of 14 will result and bit 20 will be flipped.

A blank in column 3 indicates that the bit(s) in error are unknown (multiple bit error).

Column 4 indicates the data bit flipped if the ECC switch S4 is in the ON position.

A blank in column 4 indicates no data bit is flipped for that syndrome code. For EBE syndrome codes, two or more bits are in error and the data bit flipped may or may not be the one of incorrect bits.

The error logger can be used to test for bad check bits (in error). This condition can be checked for if a memory test is performed with the ECC switch (S4) in the OFF position. If the memory test indicates no data errors (bits 0-3) but the error logger indicates a single or double-bit error, then the error logger directly indicates the check bits in memory which are bad. For example, a syndrome bit code of 11 would indicate the check bits CP and C0 are bad.

Table 4-9. Syndrome Error Analysis Guide (Sheet 1 of 4)

Syndrome Bit Code (Hexadecimal)	Error Type	Bit in Error	Data bit Flipped If ECC Switch is On
00	None	None	
01	OBE	C0	
02	OBE	C1	
03	EBE		
04	OBE	C2	
05	EBE		
06	EBE		
07	OBE		
08	OBE	C3	
09	EBE		
0A	EBE		
0B	OBE		
0C	EBE		
0D	OBE		
0E	OBE		
0F	EBE		
10	OBE	C4	
11	EBE		17
12	EBE		18
13	OBE	19	19
14	EBE		20
15	OBE	21	21
16	OBE	22	22
17	EBE		23
18	EBE		0
19	OBE	1	1
1A	OBE	2	2
1B	EBE		3
1C	OBE	4	4
1D	EBE		5
1E	EBE		6
1F	OBE	7	7

Table 4-9. Syndrome Error Analysis Guide (Sheet 2 of 4)

Syndrome Bit Code (Hexadecimal)	Error Type	Bit in Error	Data bit Flipped If ECC Switch is On
20	OBE	C5	
21	EBE		25
22	EBE		26
23	OBE	27	27
24	EBE		28
25	OBE	29	29
26	OBE	30	30
27	EBE		31
28	EBE		8
29	OBE	9	9
2A	OBE	10	10
2B	EBE		11
2C	OBE	12	12
2D	EBE		13
2E	EBE		14
2F	OBE	15	15
30	EBE		
31	OBE		
32	OBE		
33	EBE		
34	OBE		
35	EBE		
36	EBE		
37	OBE		
38	OBE	16	16
39	EBE		
3A	EBE		
3B	OBE		
3C	EBE		24
3D	OBE		
3E	OBE		
3F	EBE		

Table 4-9. Syndrome Error Analysis Guide (Sheet 3 of 4)

Syndrome Bit Code (Hexadecimal)	Error Type	Bit in Error	Data bit Flipped If ECC Switch is On
40	OBE	CP	
41	EBE		
42	EBE		
43	OBE		
44	EBE		
45	OBE		
46	OBE		
47	EBE		
48	EBE		
49	OBE		
4A	OBE		
4B	EBE		
4C	OBE		
4D	EBE		
4E	EBE		
4F	OBE		
50	EBE		
51	OBE	17	17
52	OBE	18	18
53	EBE		19
54	OBE	20	20
55	EBE		21
56	EBE		22
57	OBE	23	23
58	OBE	0	0
59	EBE		1
5A	EBE		2
5B	OBE	3	3
5C	EBE		4
5D	OBE	5	5
5E	OBE	6	6
5F	EBE		7

Table 4-9. Syndrome Error Analysis Guide (Sheet 4 of 4)

Syndrome Bit Code (Hexadecimal)	Error Type	Bit in Error	Data bit Flipped If ECC Switch is On
60	EBE		
61	OBE	25	25
62	OBE	26	26
63	EBE		27
64	OBE	28	28
65	EBE		29
66	EBE		30
67	OBE	31	31
68	OBE	8	8
69	EBE		9
6A	EBE		10
6B	OBE	11	11
6C	EBE		12
6D	OBE	13	13
6E	OBE	14	14
6F	EBE		15
70	OBE		
71	EBE		
72	EBE		
73	OBE		
74	EBE		
75	OBE		
76	OBE		
77	EBE		
78	EBE		16
79	OBE		
7A	OBE		
7B	EBE		
7C	OBE	24	24
7D	EBE		
7E	EBE		
7F	OBE		

CHAPTER 5

MAINTENANCE

5.1 Introduction

This Chapter describes the function of the external error analysis connector (J1), and the write check bit connector (J2). Also included in the chapter is a refresh and scrubbing checkout procedure for the ISM.

5.2 Maintenance Philosophy

It is recommended that maintenance be confined to the testing, troubleshooting, and replacement of complete circuit card assemblies. Defective circuit cards should be returned to Gould CSD for repair. The repairs will be made and the circuit card will be returned to the user by the most expeditious method.

5.3 External Error Analysis Connector

The external analysis connector (J1) is designed for use with a logic analyzer for the purpose of recording error syndrome values as they occur. The logic analyzer through J1 will record single-bit, soft single-bit, hard single-bit, or double-bit errors. Refer to Table 5-1 for J1 pin assignment and signal mnemonics with definitions.

5.4 Write Check Bits Connector

The write check bit connector (J2) is used to force memory write cycles to write incorrect syndrome check bits. These incorrect bits are interpreted by the ISM as single-bit or double-bit errors. This allows error conditions to be simulated and verifies correct operation of the refresh and scrubbing circuits on the ISM.

Incorrect check bits are written into memory by grounding one or more pins on J2. This writes the compliment of the correct value of the corresponding check bit into memory.

The order of the check bits in J2 are in the same physical order as the syndrome code LEDs.

The signal pins for J2 are as follows:

PIN	SIGNAL
J2-14	LWCB0
J2-12	LWCB1
J2-10	LWCB2
J2-8	LWCB3
J2-6	LWCB4
J2-4	LWCB5
J2-2	LWCBP

All odd numbered pins on connector J2 are connected to ground.

Table 5-1. External Error Analysis Connector Pin Assignment

Pin Number	Signal Name (Mnemonic)	Definition
J1-2	LRMTRESET	Remote reset signal input. A low will clear the LED display.
J1-4	LCLK150	150 nanosecond clock signal output.
J1-6	HSBEOUT	Single-bit error signal output. A high at error strobe time (HRDSTROBE) indicates a SBE has been detected.
J1-8	HDBEOUT	Double-bit error signal output. A high at error strobe time indicates a DBE has been detected.
J1-10	HSOMEEROUT	Some error signal output. A high at error strobe time indicates an error (SBE or DBE) was detected.
J1-12	HRDSTROBE	Read strobe signal output. This signal is normally low. It goes high for approximately 150 nsec whenever an internal read cycle is performed on the board. The high to low edge (trailing edge) is the error strobe time referred to in this section and it is this edge which should be used to clock the status of the signals. Except for the LCLK150 signal, all output signal conditions will be stable at least 20nsec before and remain stable until at least 150 nsec after error strobe time.
J1-16	LBS(0,1)OUT	Bank select signal output. These signals when clocked indicate the binary value of the bank where the memory read cycle has occurred.
J1-20 thru J1-32	LPS(1-5,P)OUT	Syndrome 0-5, parity signal output. These signals indicate the syndrome bit was detected.
J1-34	LMONITOR	Monitor signal output. When this signal is low, the internal error logger clocks in the status of the syndrome and bank select bits for every internal read cycle in the ISM.
All odd numbered pins of connecter J1 are connected to ground.		

5.5 ISM Refresh and Scrubbing Procedure

The following paragraphs describe the recommended procedure to verify the proper operation of the refresh and scrubbing functions of the ISM.

The procedure assumes that the ISM is plugged into the SelBUS system and performing normal functions. To verify the ISM operation a diagnostic should be run which will perform writes and reads through the entire memory range.

In each step below, the condition of the LEDs are indicated. Unnamed LEDs (except for BS0 and BS1 which reflect the bank addressed) are OFF unless otherwise stated. In all steps, to ground a signal, connect a short jumper from any of the odd numbered pins on J1 or J2 to the signal pin indicated.

Step 1: Start with the ISM running a program with all the switches to the right. All of the display LEDs should be off. If any DBE condition occurs, they should have been cleared by the program being run or by the operator doing a panel clear before running the program.

Step 2: Lamp Test. Ground the following "E" points which are located in front of each LED one at a time: E86 through E100. The corresponding LED should illuminate when the "E" point is grounded. Only E97 through E100 should remain illuminated once grounded. Reset all LEDs.

Step 3: Monitor Check. Ground J1-34. The BS0 and BS1 LEDs should illuminate reflecting the bank addressed being read by the processor. Remove J1-34. Reset the display by using S1 or by grounding J1-2 temporarily.

Step 4: Set Scrub switch (S2) to the OFF position.

Step 5: Create a SBE on the board by grounding J2-2 (SP). LEDs SP, and SBE should illuminate. Since the scrub switch is OFF the SOFT or HARD LEDs should also be off.

Step 6: Set the Scrub switch (S2) to the ON position. LEDs SP, SBE, SBE, and HARD should be illuminated.

Step 7: Remove the jumper from J2-2. LEDs SP, SBE, SOFT, and HARD should be illuminated. Reset the LEDs. After 16 seconds (scrubbing time for the 1MW ISM) no LEDs should be illuminated.

Step 8: Repeat steps 4 through 7 with the remaining check bits on connector J2 (J2-4 through J2-14). The corresponding LED (S1-5, and SP) should be illuminated.

Step 9: Halt the processor. Remove all jumpers from J1 and J2. Reset the LEDs and set all switches to the right. Write all F's (FFFFFFFF) in a location in memory manually. Do a memory read to that location. No parity error should be indicated and correct data should be returned.

Step 10: Set Scrub switch (S2) and ECC switch (S4) to the left. Ground J2-2,6,14 (Hex 51H). Do a memory write (all F's) to the same location used in step 9. LEDs S0, S4, SP, SBE should be illuminated.

Step 11: Do a memory read. No parity error should be detected, and all F's should be read.

Step 12: Set ECC switch (S4) to the right. Read the memory location. Data should be FFFFBFFF (bit 17=0). No parity error detected. The check bit code set up in step 10 above (Hex 51H) corresponds to bit 17 in the check bit matrix.

Step 13: Set Type switch (S3) to the left. Read the same memory location. A parity error should be indicated this time. Set S3 to the right.

Step 14: Set Scrub switch (S2) to the right. After a few seconds (16 seconds maximum) the HARD LED should illuminate.

Step 15: Read the memory location repeatedly. Every few seconds the data in the memory location should be alternated between FFFFBFFF and FFFFFFFF. Bit 17 alternates value as the scrubbing circuits try to correct the SBE by inverting the value. Since the wrong syndrome pattern is always being written into memory, bit 17 is always detected as an error.

Step 16: Remove all jumpers. The SOFT LED should illuminate within 16 seconds.

Step 17: Reset the LEDs. Set all switches to the right. Write all F's (FFFFFFFF) in a location in the memory manually. Do a memory read to that location. No parity errors should be indicated and correct data should be returned.

Step 18: Set ECC switch (S4) to the left. Ground J2-6, 14 (Hex 11H). Do a memory write (all F's) to the same location. Now do a memory read. A parity error should be detected and all F's should be read. The LED DBE should be illuminated.

Step 19: Set ECC switch (S4) to the right. Do a memory read. A parity error should be detected, and FFFFBFFF should be read.

Step 20: Remove all jumpers. Set all switches to the right. Perform a panel clear to all memory. Reset the LEDs. This completes the ISM checkout procedure.

APPENDIX A

MNEMONICS

Mnemonic	Meaning/Remarks
L1CLKCN1	Level 1 clock continuous
H2CLKCN(1,2)	Level 2 clock continuous
L2CLKCN1	Level 2 clock continuous
H2CLKREF	Level 2 clock refresh
L2CLKSC(1,2)	Level 2 clock, stop clock
H3CLKADVADR	Level 3 clock, advance address
H3CLKBD(1-3)	Level 3 clock buffered data
H3CLKCYC	Level 3 clock memory cycle
H3CLKOUTNH(1,2)	Level 3 clock out normally high
H3CLKREF(1-4)	Level 3 clock refresh
L3CLKREF(1,2)	Level 3 clock refresh
H3CLKSC(1-3)	Level 3 clock stop clock
L3CLKSC(1,2)	Level 3 clock stop clock
HA(0-8)	DRAM address bit
HA(0-8)BK(0-3)	DRAM address bit 0-8, bank 0-3
HACCEPT	Accept
HADBOT(1-3)	Address compare low limit (bottom)
HADRCARRY(1,2)	Address carry
HADRTOP(1-3)	Address compare upper limit (top)
LAR0(8-15)	Source address register
LBD(16-31)	Buffered Data Bus

Mnemonic	Meaning/Remarks
HSB(0,1)IN	Bank select in
LBS(0,1)OUT	Bank select out
LCAS(0-3)(A,B)	DRAM CAS lines
LCLK150	150 nanosecond clock
HCLKECD(1,2)	clock error correction data
LCLKL	SelBUS clock late
HCLKSTAT	Clock status
HCLKSYNDROME	Syndrome Clock
HCLR	Clear
LCLR(1,2)	Clear
HCLRSTART	Clear Start
LCLRSTART	Clear Start
LCNT(0,1)	SelBUS control tag lines
LCYCDT(22,23,F)IN	Memory cycle destination bit in
LCYCRDIN	Memory cycle read in
LD(00-31)	SelBUS data bus lines
LDBE	Double-bit error
HDBEDEF	Double-bit error definitely
HDBEOUT	Double-bit error out
LDISPCLR	Display Clear
LDT(00-23,F)	SelBUS destination bus lines
HDT(02-05,20,21,)SEL	Destination bit select
HDT(22,23,F).1	Destination bit buffered
LECD00-31	Error correction data bit
LECK(0,1)	SelBUS Echo lines

Mnemonic	Meaning/Remarks
HENATECD(1,2)	Enable at error corrected data time
LENBD0011	Enable data byte 0 to data byte 0 and byte 1 to data byte 1
LENBD(20,22,30,31,32,33)	Enable data byte 2 to byte 0, byte 2 to byte 2 etc.
LENECD(00,02,03,11,13,22,23,33)	Enable error corrected data byte 0 to byte 0, byte 0 to byte 2 etc.
HENFORWRITE	Enable for write
LENRD(1,2)	Enable read
LENWCB	Enable write check bits
HEOC	End of cycle
LEOC	End of cycle
LEOCDL	End of cycle delayed
LEOCDLSEL.1	End of cycle delayed select buffered
LERROR	Error
HFACCDEL	Flip-flop accept delay
HFANYERSEL	Flip-flop any error select
HFCANSCRUB	Flip-flop cancel scrub
LFCANSCRUB	Flip-flop cancel scrub
LFD(00-31)	Formatter bus data
HFDBESEL	Flip-flop double-bit error select
LFDC(0-5,P)	Flip-flop check bit
HFDISPLAYCLR	Flip-flop display clear
HFDT(02-23,F)	Flip-flop destination bus lines
HFDTBK(2-5)	Flip-flop destination bank lines
HFECCON	Flip-flop ECC on

Mnemonic	Meaning/Remarks
HFENCLKOUTNL	Flip-flop enable clock out normally low
HFHARDSVD	Flip-flop hard saved
LFHARDSVD	Flip-flop hard saved
HFHCYCPLS	Flip-flop first half memory cycle pulse
LFHCYCPLS	Flip-flop first half memory cycle pulse
HFHREFPLS	Flip-flop first half refresh pulse
LFHREFPLS	Flip-flop first half refresh pulse
LFLOCK	Flip-flop lock
HFPFMEM	Flip-flop power fail memory
LFPFMEM	Flip-flop power fail memory
HFPOLL	Flip-flop poll
HFRD	Flip-flop read
LFRDWINDOW	Flip-flop read window
HFREFLTH.1	Flip-flop refresh length buffered
HFREFLTH	Flip-flop refresh length
LFREFLTH	Flip-flop refresh length
HFREFREQ	Flip-flop refresh request
LFREFREQ	Flip-flop refresh request
HFREQSCRUB	Flip-flop request scrub
LFREQSCRUB	Flip-flop request scrub
HFSBEDEF	Flip-flop single-bit error definitely
LFSBEDEF	Flip-flop single-bit error definitely
LFSBESVD	Flip-flop single-bit error saved
HFSCRUBLTHM1	Flip-flop scrub length minus 1 clock
LFSCRUBLTHM1	Flip-flop scrub length minus 1 clock

Mnemonic	Meaning/Remarks
LFSCRUBOFF	Flip-flop scrub off
LFSOFTSVD	Flip-flop soft saved
HFSOMEER	Flip-flop some error
LFSTSC	Flip-flop stop system clock
HFTIME	Flip-flop refresh time
HFULLWRT	Flip-flop full write
LFULLWRT	Flip-flop full write
LINH(0-3)	SelBUS Inhibit lines
LMCYCSTART	Memory cycle start
HME	ME (address compare)
LMEM	SelBUS memory line
HMEMCYCIN	Memory cycle in
LMEMCYCIN.1	Memory cycle in buffered
LMEMHCLR	Low memory or high clear
LMLK	SelBUS memory lock line
LMONITOR	Monitor
LMUNLK	SelBUS memory unlock line
LMUXADD	Multiplex address
LNOSCRUB	No scrub
LOFFLINE	Off line
HPASS	Pass
HPB(0,1)E	Parity bit even
LPFMEM	SelBUS power fail memory line
HPH(1-7)	Phase timing
LPH(1-6)	Phase timing

Mnemonic	Meaning/Remarks
HPHBUSY(1,2)	Phase busy
LPHBUSY(1,2)	Phase busy
LPR00	SelBUS priority line
HPR(1-7)	SelBUS priority lines
HPRMASTER	Priority master
HPRSLAVE	Priority slave
LP(S0-5,P)	Parity Syndrome bits
HPS(1-5)	Parity Syndrome bits
LPS(0-5,P)OUT	Parity Syndrome out
HPS3CTL	Parity Syndrome control
LPS3CTL	Parity Syndrome control
HPTLWRT	Partial write
LPTLWRT	Partial write
HPWRCLR(1-4)	Power clear
LPWRCLR(1-4)	Power clear
HRAS	Row address strobe
LRAS(0-3)(A,B)	Row address strobe DRAM lines
LRD	SelBUS read
LRD2	Read lines buffered
LRD(00-31,C0-C5,CP)	DRAM read data out lines
HRDSTROBE	Read strobe
HREAD	Read
HREFREQIN	Refresh request in
LREPOLL	Repoll
LRESET	Reset

Mnemonic	Meaning/Remarks
LRMTRESET	Remote reset
HSBCLKDIS	SelBUS clock disable
LSBCLKDIS	SelBUS clock disable
HSBEDEF	Single-bit error definitely
HSBEHARDIN	Hard single-bit error in
HSBEOUT	Single-bit error out
HSBEOUTEN	Single-bit error out enable
LSBEOUTEN(1-6)	Single-bit error out enable
HSCRUB150	150 nanosecond scrub
HSCRUB450	450 nanosecond scrub
HSCRUB750	750 nanosecond scrub
HSCRUB900	900 nanosecond scrub
LSCRUB900	900 nanosecond scrub
HSCRUBPTLWRT	Scrub partial write
LSCRUBPTLWRT	Scrub partial write
HSELDLCYC	Select delayed cycle
LSELERROR	Selected error
LSETH0011	Set high bytes 0 and 1
LSETH22	Set high byte 2
HSETINH	Set inhibit
LSETINH	Set inhibit
HSHIFT(1,2)	Shift
HSOMEERROROUT	Some error out
HSTART	Start

Mnemonic	Meaning/Remarks
LSTART	Start
HSTOPACC	Stop accept
LSTOPACC2	Stop accept
LSTSC	SelBUS stop system clock line
LTA	SelBUS transfer acknowledge line
HTOFFECDPLS	Turn off error corrected data pulse
LTOFFMRASSEL	Turn off modify cycle RAS select
HTOFFNRASSEL1	Turn off normal cycle RAS select
HTONECDPLS	Turn on error corrected data pulse
LTX	SelBUS transfer line
LUS	SelBUS unsuccessful line
HWAITPOLL	Wait poll
LWAITREF	Wait refresh

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