



**SDS 930 COMPUTER
CENTRAL PROCESSOR**

Logic Layouts,
Current and History

SDS 900592A

PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG	PAGE	CHG
1		61	A	121		181		241	
2	A	62	A	122		182		242	
3	A	63	A	123		183		243	
4	A	64	A	124		184		244	
5	A	65	A	125		185		245	
6	A	66	A	126		186		246	
7	A	67	A	127		187		247	
8		68	A	128		188		248	
9		69	A	129		189		249	
10		70	A	130		190		250	
11		71	A	131		191		251	
12		72	A	132		192		252	
13		73	A	133		193		253	
14		74	A	134		194		254	
15		75	A	135		195		255	
16		76	A	136		196		256	
17		77	A	137		197		257	
18		78	A	138		198		258	
19		79	A	139		199		259	
20		80	A	140		200		260	
21		81	A	141		201		261	
22		82	A	142		202		262	
23		83	A	143		203		263	
24		84	A	144		204		264	
25		85	A	145		205		265	
26		86	A	146		206		266	
27		87		147		207		267	
28	A	88		148		208		268	
29	A	89		149		209		269	
30	A	90		150		210		270	
31	A	91		151		211		271	
32	A	92		152		212		272	
33	A	93		153		213		273	
34	A	94		154		214		274	
35	A	95		155		215		275	
36	A	96		156		216		276	
37	A	97		157		217		277	
38	A	98		158		218		278	
39	A	99		159		219		279	
40	A	100		160		220		280	
41	A	101		161		221		281	
42	A	102		162		222		282	
43	A	103		163		223		283	
44	A	104		164		224		284	
45	A	105		165		225		285	
46	A	106		166		226		286	
47	A	107		167		227		287	
48	A	108		168		228		288	
49	A	109		169		229		289	
50	A	110		170		230		290	
51	A	111		171		231		291	
52	A	112		172		232		292	
53	A	113		173		233		293	
54	A	114		174		234		294	
55	A	115		175		235		295	
56	A	116		176		236		296	
57	A	117		177		237		297	
58	A	118		178		238		298	
59	A	119		179		239		299	
60	A	120		180		240		300	

NOTES:
1. REVISION LETTERS LISTED INDICATE STATUS OF EACH SHEET OF THIS MULTIPLE SHEET DRAWING.
2. CHECK INDIVIDUAL SHEETS FOR REVISION LETTER AGAINST THIS SHEET BEFORE USING THIS DRAWING.

REFERENCE DESIGNATIONS
ARE ABBREVIATED.
PREFIX THE DESIGNATION
WITH UNIT NUMBER
OR ASSEMBLY DESIGNATION
OR BOTH. (MIL. STD. 16B)


930
PAGE 1
A

SCALE	930	DRAWING NO.	106407	SHEET	A
	DO NOT SCALE DRAWING				
SDS <small>SCIENTIFIC DATA SYSTEMS</small> <small>1100 W. 17th Street, Santa Ana, California</small>		DIAGRAM, LOGIC COMPUTER			
<small>REVISIONS</small> <small>NO.</small> <small>DESCRIPTION</small> <small>DATE</small> <small>BY</small> <small>APP.</small>		<small>106407</small> <small>A</small>			

A/106407

A00	34	C0, C1, C2	46	F1, Fla, F2, F3	65
A0, A1, A2	31	C3 thru C11	47	F1 thru F3 Buffer	61
A3 thru A11	32	C12 thru C20	48	$\overline{F1}$ F3)	60
A12 thru A20	33	C21 thru C23	49		
A21 thru A23	34	C24	50		
A21, A22, A23 Buffer	74	C0 thru C23 Buffer	74		
(A0 ⊕ A1)	72	/C16/, /C17/	82		
(A1 ⊕ A2)	72	C0i thru C23i	75	∅0 thru ∅7	61
(A2 ⊕ A3)	72	/Cm0/ /M0/ thru /Cm23/ /M23/	76	(∅0 Tp Ia)	65
(A00 ⊕ Ix)	35	Cd0 thru Cd23	77	(∅0 T8 Ia)	65
(A21 ⊕ C21)	35	(C10 C11)	74	(∅3 05 06)	35
(A22 ⊕ C22)	35	/C21r/, /C22r/, /C23r/	76	(∅3 Sk)	61
(A23 ⊕ C23)	35	Ck	49	(∅7 03 04 05 06)	35
(Add 1, 2, 3)	53	Clock Distribution	84		
A _{l2} [*] , A _{l2} ^{**}	35	/C1x/	76		
A _{l2} , A _{l2} ^{***} , A _{l2} ^{****}	45	Cp, Cpr	50		
\overline{Anr}	35	/Cpr/	76		
Ar1, Ar1 [*]	35	(Cp Ht)	50	G0	69
Ar3, Ar3 ^{**}	35	Cr3	49	$\overline{G0}$ Ht)	60
Ar3 [*] , Ar3 ^{**1}	45	Cxi, Cxm	49		
		Cz	53		
				Hal, 2, 3	51
B00	44			Ht	68
B0, B1, B2	36	Eax	73	Hx1, 2, 3	51
Bc2, B3, B4, B5	37	E2m0 - E3m2	85	Hx	51
Bc5, B6, B7, B8	38				
Bc8, B9, B10, B11	39	En	69	Ia	71
Bc11, B12, B13, B14	40	End	69	\overline{Ib} /	78
		(En + Ep)	68	\overline{Ie} /	78
Bc14, B15, B16, B17	41	/En + \overline{En} /	81	Ij, Ir, Is	78
Bc17, B18, B19, B20	42	Eod	69	IL	77
Bc20, B21, B22, B23	43	\overline{Eod} /	80	Inr	71
Bc23	44	Eom	69		
B21 [*] , B22 [*] , B23 [*] , Bc23 [*]	74	\overline{Eom} /	76		
Brl, Brl [*] , Brl ^{**}	45	\overline{Eom} / [*]	82		
Bz0	45	(Eom C10 C11 C18 + Kmc)	60		
		Ex	68		

930
PAGE 2
A

SCALE	DATE	REV.	DESCRIPTION	CHK	DATE	APPROVED
DO NOT SCALE DRAWING	106407	A	REV. 5/68			
 DIAGRAM LOGIC COMPUTER			REVISIONS 00407 A			

A106407

Int	68	$\overline{\text{Mgs}}$	81	Pot	69
$\overline{\text{Ir0}}, \overline{\text{Ir1}}, \overline{\text{Ir2}}$	82	$\overline{\text{Mgz}}$	80	$\overline{\text{Pot}}$	76
Iro thru Irl4	79	Mxc	60	$\overline{\text{Pot}}^*$	82
Ix, (Ix $\overline{\text{G0}}$)	70	$\overline{\text{Mxc}}$	78	Pr3	54
Iz0 thru Iz14	80				
		N5 thru N14	78	Q1 thru Q6	64
Ju	73				
Jz0 thru Jz5	62				
Jz6 thru Jz14	63				
		01 thru 06	65	Rad0, Rad1, Rad2	45
		01* thru 06* Buffer	60	Rc	73
		($\overline{02} \overline{04} \overline{05} \overline{06}$)	60	Rde	82
Kd0, Kd1, Kd2	75	(04 05 06)	35	Rd9 thru Rd14	82
Kf1	60	(04 $\overline{05} \overline{06}$)	60	Rf	71
Kf2	60			Rn1, Rn2, Rn3	62
$\overline{\text{Kmc}}$	60	(05 06)	60	Rr1, Rr2, Rr3	62
K0	71	/05/	76	Rsa	45
Kz	53	(05 $\overline{\text{S4}} \overline{\text{S5}}$)	59	Rt	77
		(05 $\overline{\text{S6}} \overline{\text{S7}} \text{Sd2}$)	59	$\overline{\text{Rt}}$	82
		Oc	65	Rti	46
		Of	70	$\overline{\text{Rti}}$	76
		Ofe	53	Rwyl, Rwy2, Rwy3	62
Ls0A, Ls1A, Ls2A	85	Ofi	75	Rx (Rx + Tsr)	46
$\overline{\text{Ls0}}, \overline{\text{Ls1}}, \overline{\text{Ls2}}$	82	Oxc	65	$\overline{\text{Rx}}$	76
$\overline{\text{Ls0}}$ thru $\overline{\text{Ls14}}$	79			R9	82
$\overline{\text{Lz0}}, \overline{\text{Lz1}}, \overline{\text{Lz2}}$	82			$\overline{\text{R9}}$	60
$\overline{\text{Lz0}}$ thru $\overline{\text{Lz14}}$	80				
		P0, P1, P2	54		
		P3 thru P14	55		
$\overline{\text{M0}}, \overline{\text{Cm0}}$ thru $\overline{\text{M23}}, \overline{\text{Cm23}}$	81	sP0, sP1, sP2	54	S1, S2	56
Mit	81	P11 thru P14	75	S3 thru S8	57
$\overline{\text{Mit}}$	80	Pin	69	S9 thru S14	58
Mgs, Mgz	68	$\overline{\text{Pin}}$	76	($\overline{\text{S6}} \overline{\text{S7}} \overline{\text{S8}}$)	59

930
PAGE 3
A

930	106407	A
DIAGRAM LOGIC COMPUTER	930	A
REVISIONS	DATE	APPROVED
A		

A106407

$(\overline{S12} \overline{S13} Sd2)$	59	Xn1, Xn2, Xn3	67
Sc	59	Xn1*, Xn2*, Xn3* Buffer	74
(Sc + Sx 48)	59	Xn1, Xn2, Xn3 Inputs	66
(Sc + Ø1 05 T2)	59	Xw1	66
Sd2	59	Xz1, Xz2, Xz3	52
Sk	72		
Skrz	82		
Sks	74		
\overline{Skss}	60		
$\overline{Skss}/$	78	$[\overline{Yf} (Y0 + \overline{Y9})]$	82
$\overline{Ski}/$	78	Yz1, Yz2, Yz3	52
$\overline{St}/$	76		
$\overline{St}/$	82		
Sxc, Sxp, Sxn	59		

Zrq 80

T0, T1, T3, T5, T7, T8	61
$\overline{T1}/$	78
$\overline{T3}/$	81
Temp*	81
Tp, Tr	61
$\overline{Tpc}/$	76
($\overline{TpEnd} \overline{Sk}$)	61
Trq	82
Ts, Tsm, Tsr	73
Tsm*, \overline{Tsm}^*	79
$\overline{Tsm}/$	76

$[\overline{Wf} (W0 + \overline{W9})]$ 82

SIDS <small>SCIENTIFIC DATA SYSTEMS SANTA ANITA, CALIFORNIA</small>		TITLE DIAGRAM LOGIC COMPUTER	
REV. 1 DESCRIPTION REVISION 3 ALFG.	SHEET 11	DATE 11/1/67	APPROVED [Signature]
SCALE 930	DWG. NO. 106407	SHEET A	DO NOT SCALE DRAWING

A|106407

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		
A																																		
B	FB51	ZB50	ZB50	FB51	ZB50	FB51	FB51	ZB50	IB52	FB51	ZB50	FB51	FB51	ZB50	ZB50	FB51	IB58	FB51	IB58	FB51	IB58	FB51	IB58	IB57	IB57	IB56	IB58	FB51	IB52	ZB50	IB56	IB57	IB58	FB51
C																																		
D																																		
E																																		
F																																		

	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64		
A																																		
B																																		
C																																		
D																																		
E																																		
F																																		

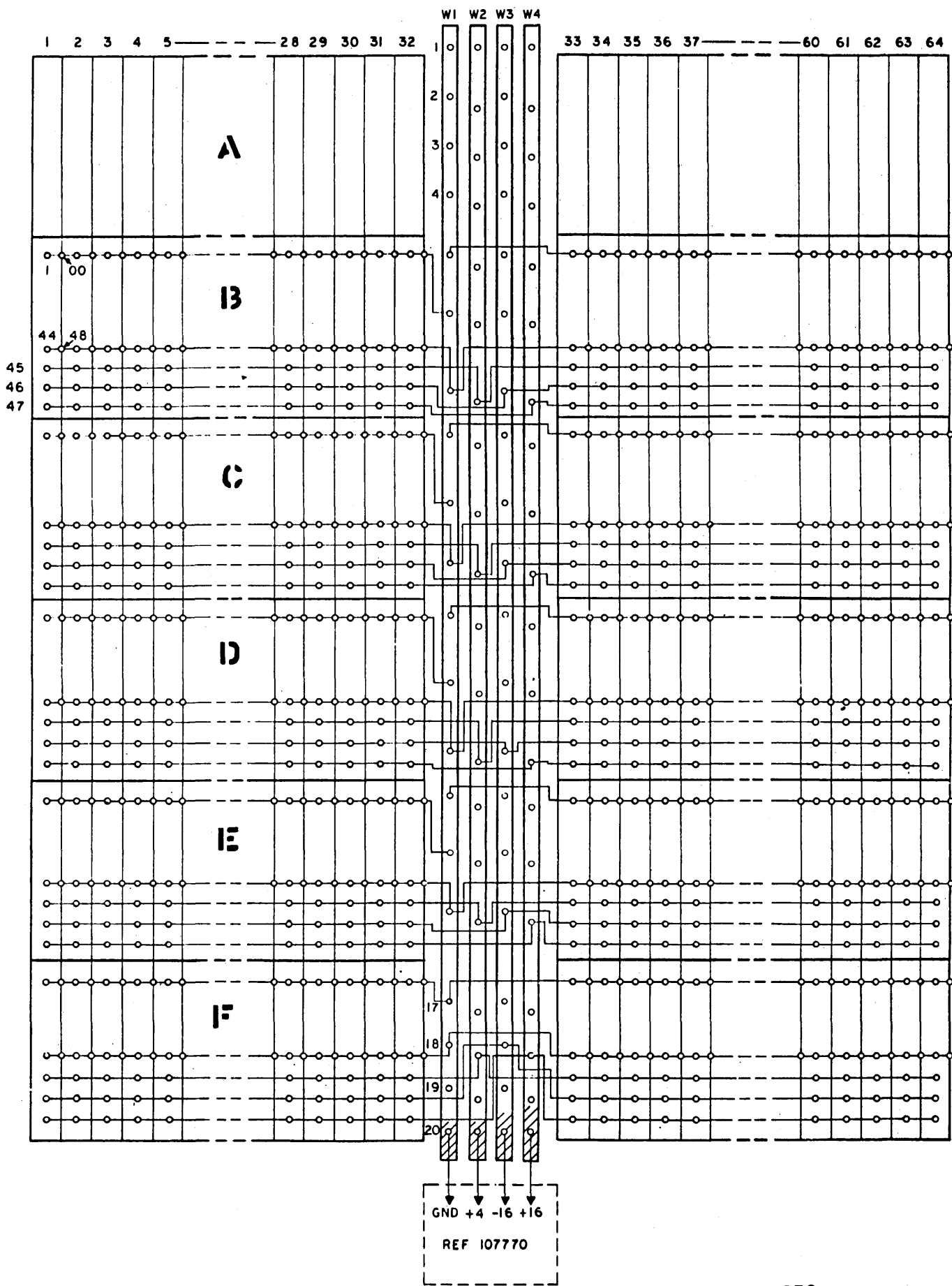
▲ MULTIPLE ACCESSED MEMORY (MAM) OPTION. ▲ USE ZB68 WHEN (MAM) OPTION NOT ADDED. 930 PAGE 5
 ▲ USE ZB52 WHEN 2ND MEMORY CHASSIS NOT ADDED. ▲ PARITY INTERRUPT OPTION. A
 ▲ ADD IF TMCC 'C' AND OR 'D' IS ADDED.

SCALE: 930
 DO NOT SCALE DRAWING
 SHEET: 106407
 PART: A

IBM
 SYSTEMS DIVISION
 3800 N. FIRST ST., SUITE 100
 CHICAGO, ILL. 60642
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 MODEL 106407
 DIAGRAM LOGIC
 COMPUTER

REV.	DESCRIPTION	DATE	BY
1	REL. TO N.F.S.	1/1/71	...

A|106407|



930
PAGE 6
A

REV.		DESCRIPTION		DATE		BY	
A		REL TO MFG					

EDS
SCIENTIFIC DATA SYSTEMS
LANTA, GEORGIA, U.S.A.

DIAGRAM, LOGIC
COMPUTER

930

DWG. NO.
106407

SHEET
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DO NOT SCALE DRAWING


106407 | A

MODULE LIST

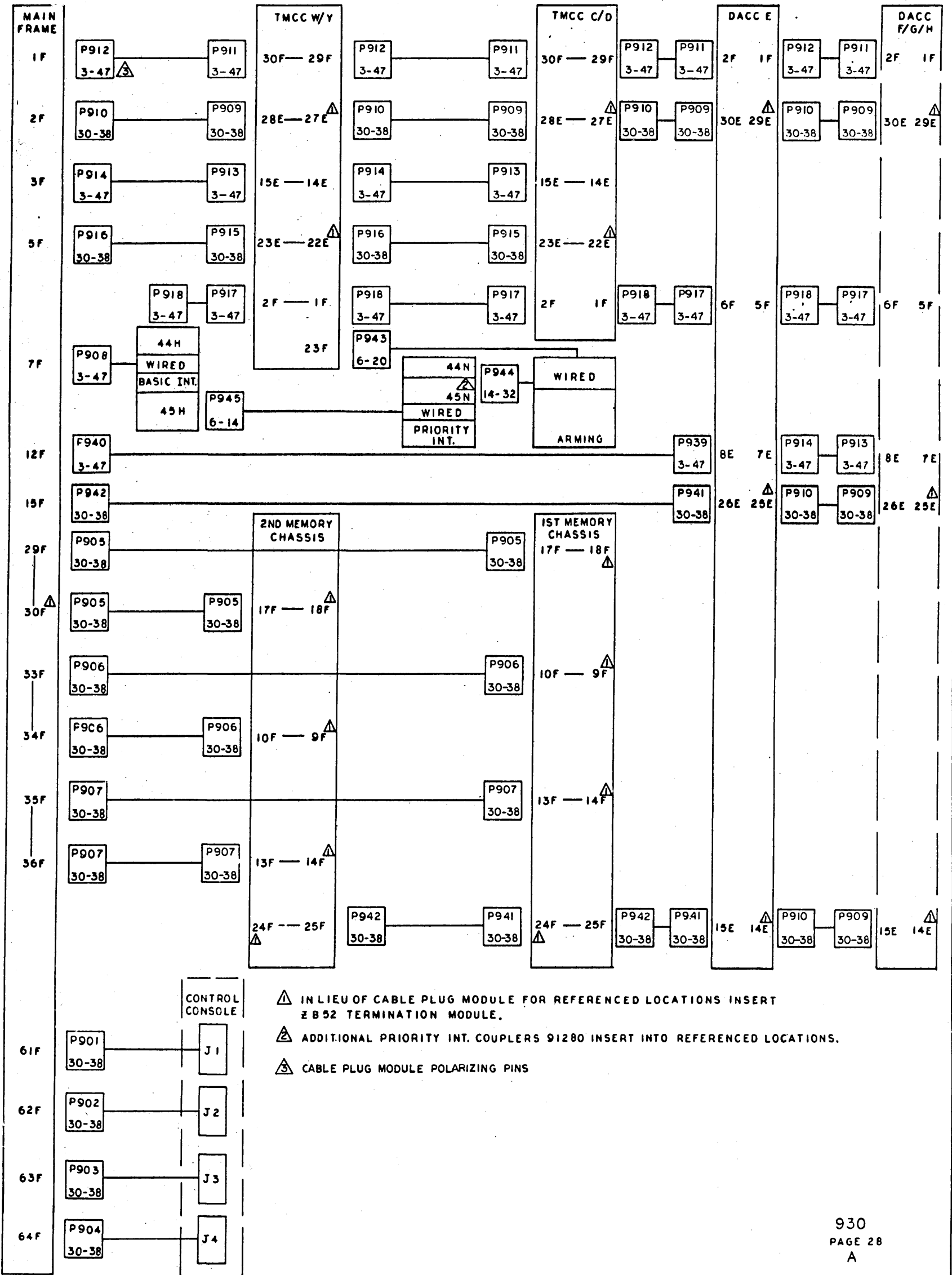
ITEM	DESCRIPTION	MODEL	QTY.
1	DUAL FLIP FLOP	FB51	43
2	TRIPLE FLIP FLOP	FB52	14
3	NAND FLIP FLOP	FB54	34
4	NAND MODULE	IB52	21
5	NAND # 2	IB56	14
6	BAND NAND	IB57	20
7	NAND # 3	IB58	47
8	CABLE DRIVER	AB51	10
9	RECEIVER INV.	AB52	2
10	RECEIVER INV. BUFFER	AB53	1
11	CABLE DRIVER # 2	AB55	13
12	INTERFACE # 8 TO + 4	NB50	4
13	SHIFT REGISTER	DB50	3
14	CLOCK GENERATOR	CB50	1
15	TERM. MOD. (+ 4)	ZB50	20
16	IND. INTERFACE	NB53	2
17	TERM. MOD. CABLE	ZB52	2
18	INTERFACE	NB57	1

ITEM	DESCRIPTION	DESIGNATION	QTY	SUPPLIER CODE SEE INDEX
1	CONNECTOR, SOLDER TAIL 47 CONTACT # 7008-47	J1 THRU J64 B, C, D, E & F	320	82

930
PAGE 7
A

930		106407		A	
DIAGRAM, LOGIC COMPUTER					
					
REVISIONS REV. DESCRIPTION DATE APPROVED A REL TO MFG. 7/78 J.L.B.					

106407 | A



930
PAGE 28
A

930

DIAGRAM LOGIC
COMPUTER




106407

REV.	DESCRIPTION	CHK	DATE	APPROVED
A	REV TO N.E.C.	J4	6/2	GMA

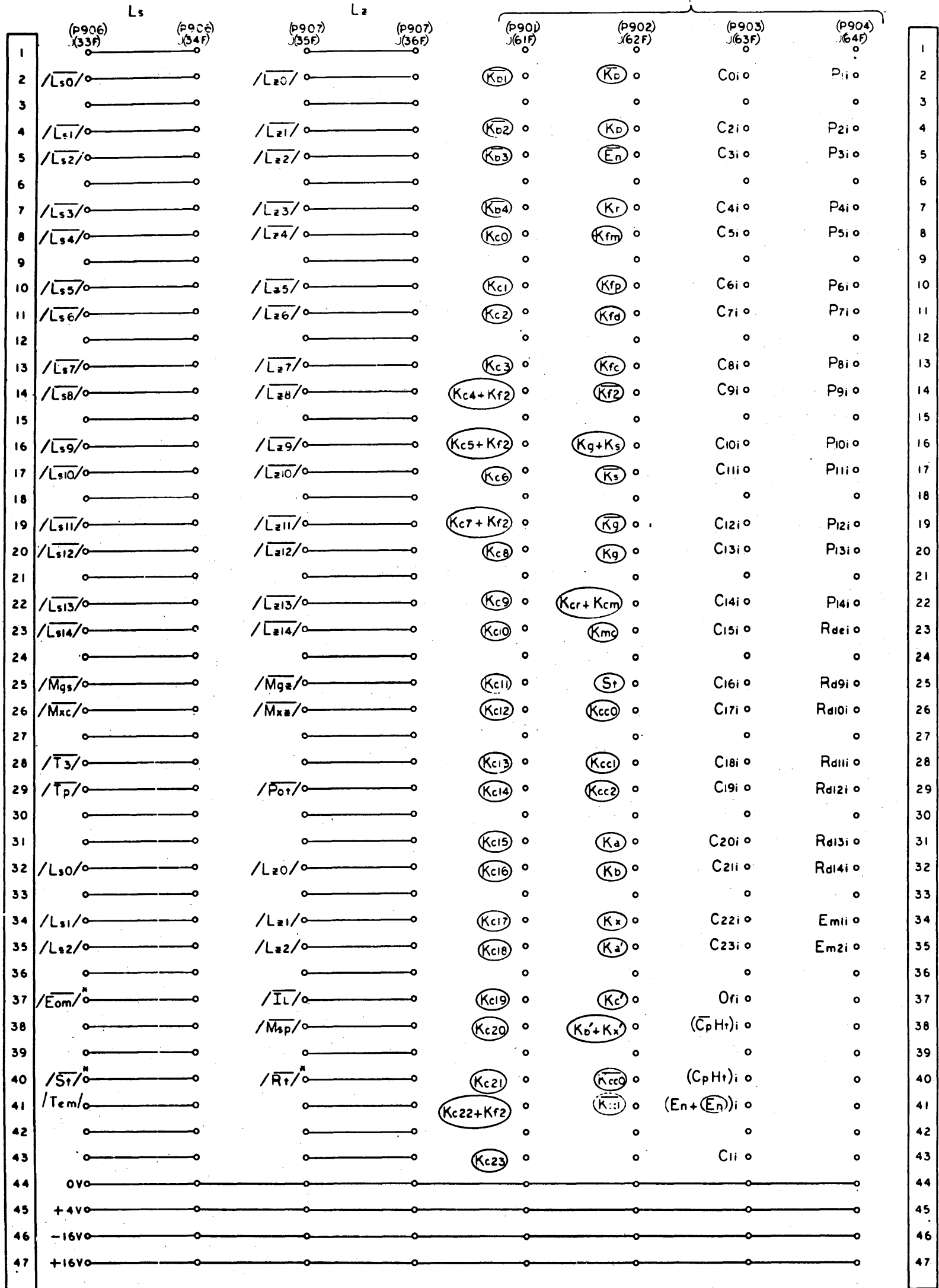
106407 | A

	I/O (P912) J(F)	I/O (P910) J(2F)	I/O (P914) J(3F)	I/O (P916) J(5F)	BASIC Inter. (P908) J(7F)	Z (P940) J(2F)	Z (P942) J(5F)	Z (P905) J(29F)(30F)	
1									1
2	Cd0	/C10/o	/Skrz/o	/C21r/o	(EomC10C11) o	/Rmp/o	/Eod/o	/Cm0//M0/o	2
3			/Koo/o			/Skrz/o			3
4	Cd1	/C11/o	/Kcc1x/o	/C22r/o	Md o	/Kcc0/o	/R1i/o	/Cm1//M1/o	4
5	Cd2	/C12/o	/Kcc2/o	/C23r/o	(S) o	/Kcc1/o	/Sks/o	/Cm2//M2/o	5
6			/Rd9/o		Cpu Parity o	/Kcc1b/o			6
7	Cd3	/C13/o	/Rd10/o	/Cpr/o		/Kcc1a/o	/Tpc/o	/Cm3//M3/o	7
8	Cd4	/C14/o	/Rd11/o	/Rr1/o	I/O Parity o	/Kcc1b/o	*Mga/o	/Cm4//M4/o	8
9									9
10	Cd5	/C15/o	/Rd12/o	/Rr2/o	int. Console 32 ^Δ	/Kcc2/s	/Mxz/o	/Cm5//M5/o	10
11	Cd6	/C16/o	/Rd13/o	/Rr3/o		/Rde/o	/Clock E/	/Cm6//M6/o	11
12			/Rd14/o		/Ioff/o	/Rde/o			12
13	Cd7	/C17/o	/Rde/o	/Rwy1/o	/IL/o	/Rd10/o	/Clock F/	/Cm7//M7/o	13
14	Cd8	/C18/o	/Rd0/ ^Δ	/Rwy2/o	int. Console 33 ^Δ	/Rd11/o	/Clock G/	/Cm8//M8/o	14
15			/Rd1/ ^Δ		/N5/o	/Rd12/o			15
16	Cd9	/C19/o	/Rd2/ ^Δ	/Rwy3/o	/N6/o	/Rd13/o	/Clock H/	/Cm9//M9/o	16
17	Cd10	/C110/o	/Rd3/ ^Δ	/Rx/o	/N7/o	/Rd14/o	/Pot/o	/Cm10//M10/o	17
18									18
19	Cd11	/C111/o	/Rd4/ ^Δ	/Tsm/o	/N8/o	/Iz0/o	/Pr/o	/Cm11//M11/o	19
20	Cd12	/C112/o	/Rd1/ ^Δ	/Tsr/o		/Iz1/o	/Tsr/o	/Cm12//M12/o	20
21			/Rd2/ ^Δ			/Iz2/o			21
22	Cd13	/C113/o	/Rd3/ ^Δ	/Os/o		/Iz3/o	/Sr/o	/Cm13//M13/o	22
23	Cd14	/C114/o	/R9/o	/Clockwy/o	/Sr/**o	/Iz4/o	/C1x/o	/Cm14//M14/o	23
24			/Tr9/o		/Tj/o	/Iz5/o			24
25	Cd15	/C115/o	/Yr(Y0-Y9)/o	/ClockCd/o	/Is/o	/Iz6/o	/C1x/o	/Cm15//M15/o	25
26	Cd16	/C116/o	/Wr(W0-W9)/o	/Pot/o	/Tr/o	/Iz7/o	/C1x/o	/Cm16//M16/o	26
27									27
28	Cd17	/C117/o	/Tr0/o	/Pin/o		/Iz8/o	/C1x/o	/Cm17//M17/o	28
29	Cd18	/C118/o	/Tr1/o	/R1i/o	/N9/o	/Iz9/o	/C17x/o	/Cm18//M18/o	29
30			/Tr2/o		/N10/o	/Iz10/o			30
31	Cd19	/C119/o	/Tr3/o	/Tpc/o	/N11/o	/Iz11/o	/C17x/o	/Cm19//M19/o	31
32	Cd20	/C120/o	/Tr4/o	/Eom/o	/N12/o	/Iz12/o		/Cm20//M20/o	32
33			/Tr5/o		/N13/o	/Iz13/o			33
34	Cd21	/C121/o	/Tr6/o	/Sks/o	/N14/o	/Iz14/o	/Zr4/o	/Cm21//M21/o	34
35	Cd22	/C122/o	/Tr7/o	/C1i/o		/Rd5/ ^Δ	/Zb1/o	/Cm22//M22/o	35
36									36
37	Cd23	/C123/o	/Tr8/o	/C1x/o	/Ti/o	/Rd6/ ^Δ	/Zp1/o	/Cm23//M23/o	37
38	Rt		/Tr9/o	/Sr/o	/Ib/o	/Rd7/ ^Δ	/Zq1/o	/Cm24//M24/o	38
39			/Tr10/o		/Ie/o	/Rd4/ ^Δ			39
40		**/Mit/o	/Tr11/o	/En*(En)/o	/Ski/o	/Rd5/ ^Δ	/Zr1/o	/Mit/o	40
41			/Tr12/o			/Rd6/ ^Δ		Over temp	41
42			/Tr13/o		*C17/o	/Rd7/ ^Δ			42
43			/Tr14/o		*C16/o	/Rd4/ ^Δ		Md	43
44	0V								44
45	+4V								45
46	-16V								46
47	+16V								47

^Δ 9300 only

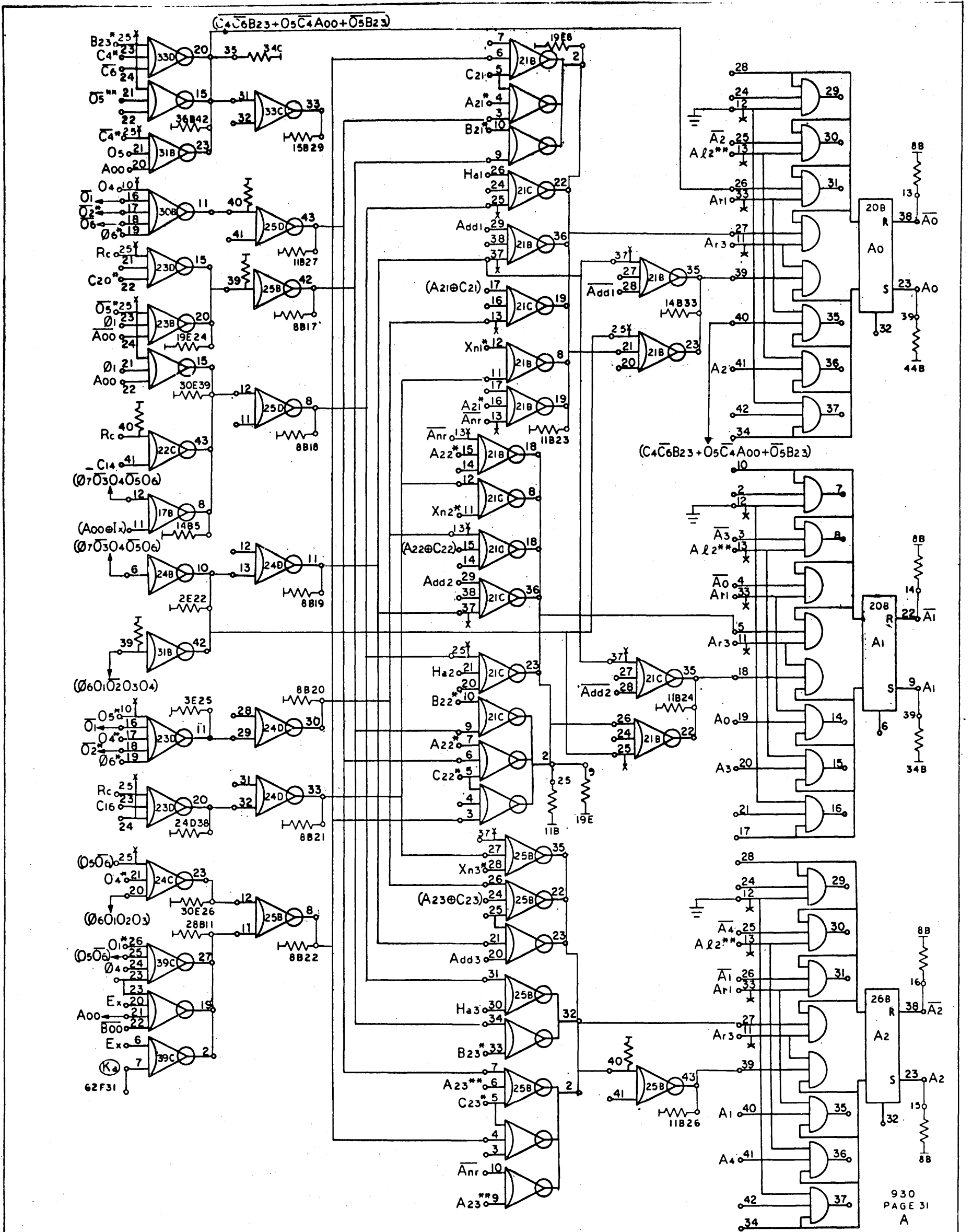
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DIAGRAM, LOGIC COMPUTER		
		
REV	DESCRIPTION	DATE
A	REL. TO 106407	7/8/66
REVISIONS		106407 IA

CONTROL CONSOLE



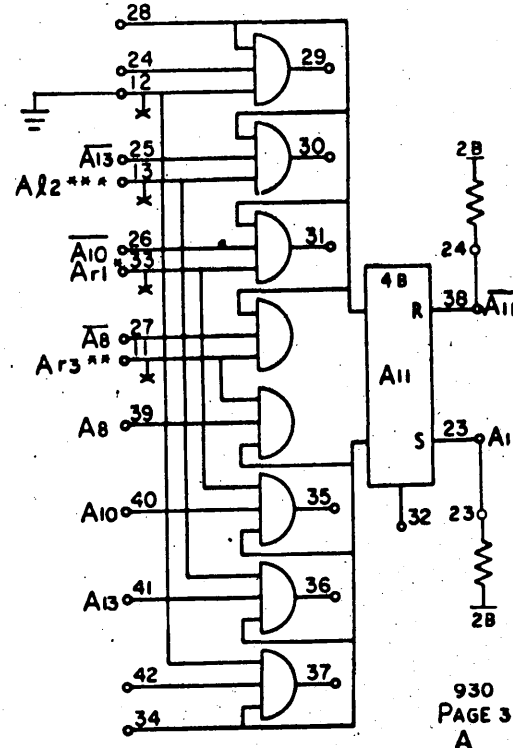
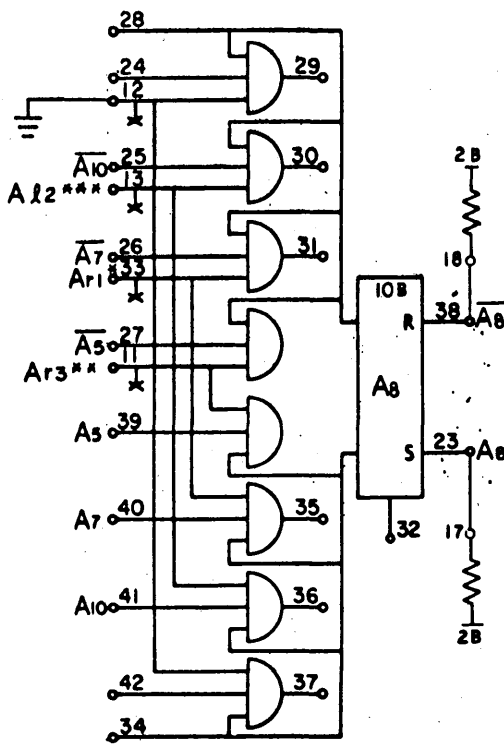
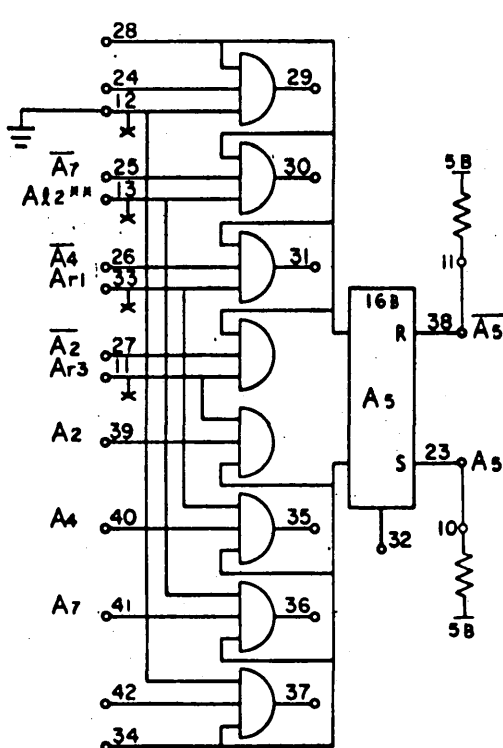
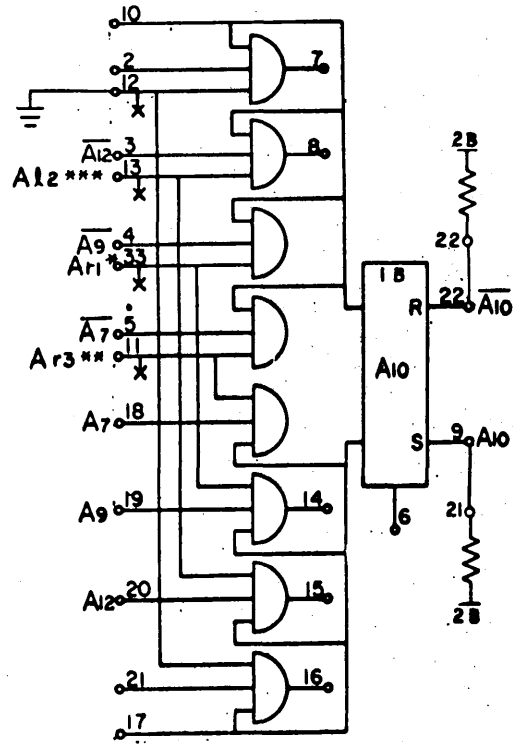
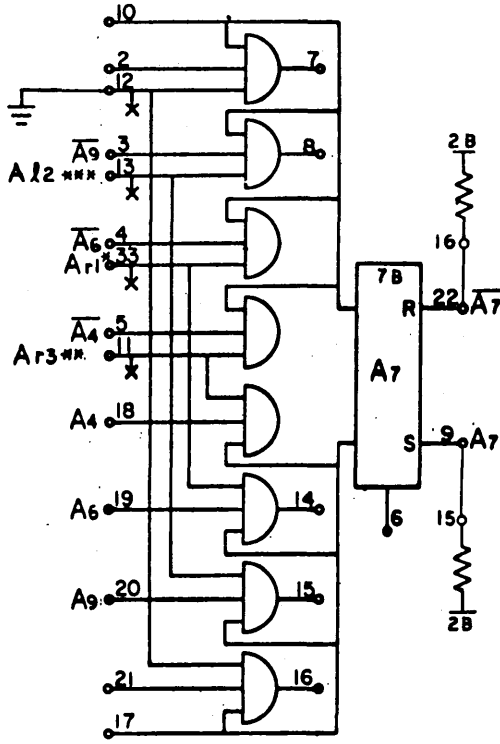
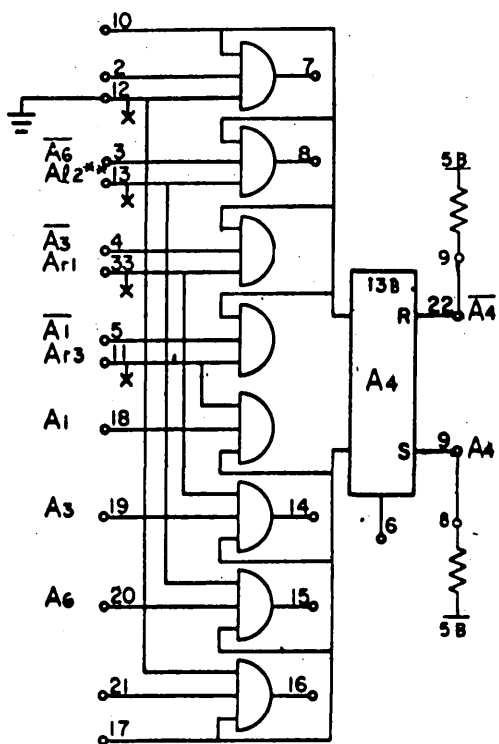
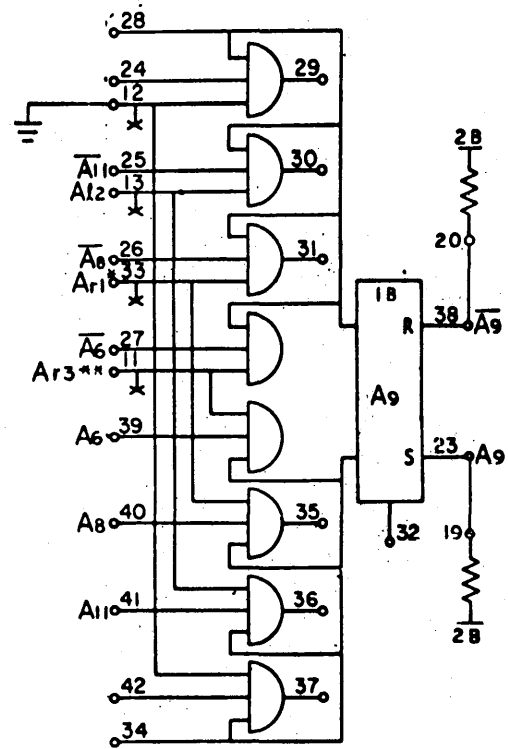
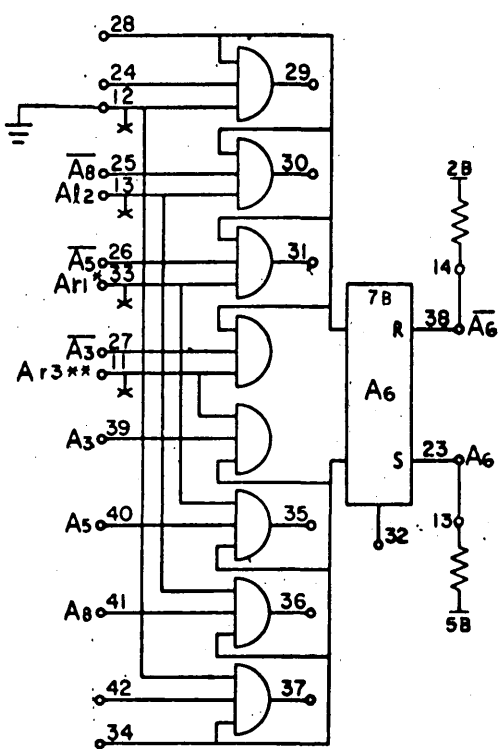
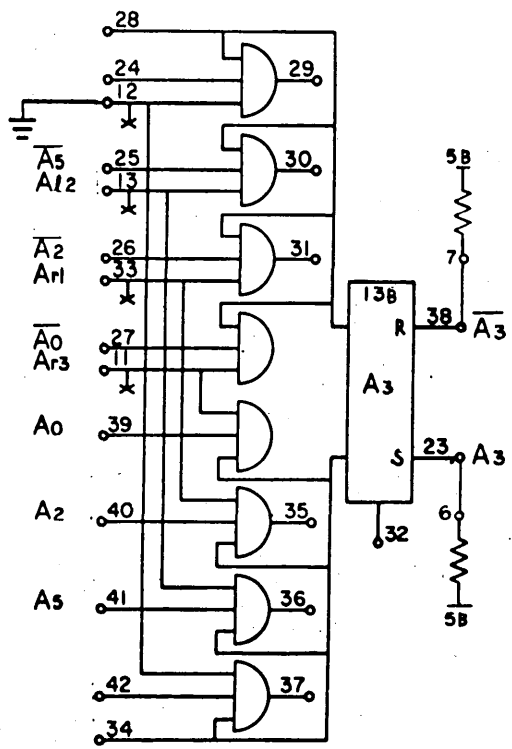
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			2	7/14
			3	2-17-54
DIAGRAM, LOGIC COMPUTER			106407	A

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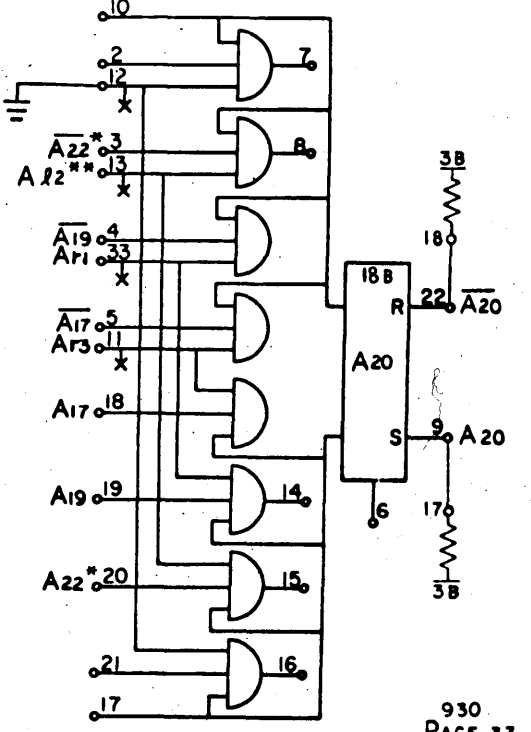
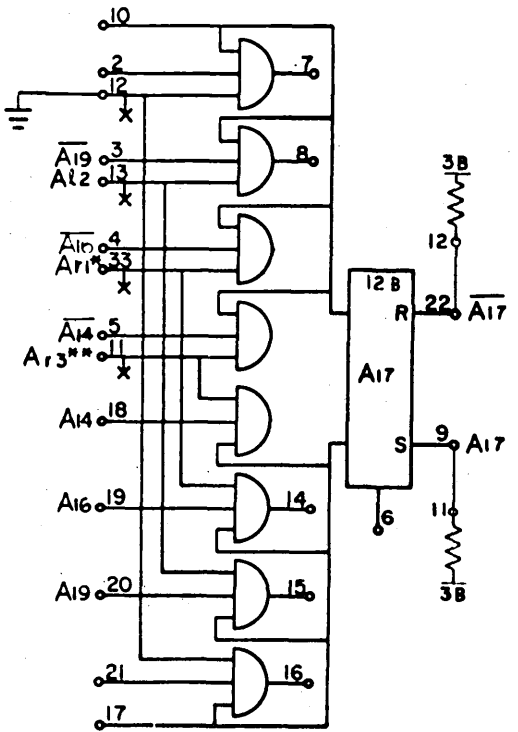
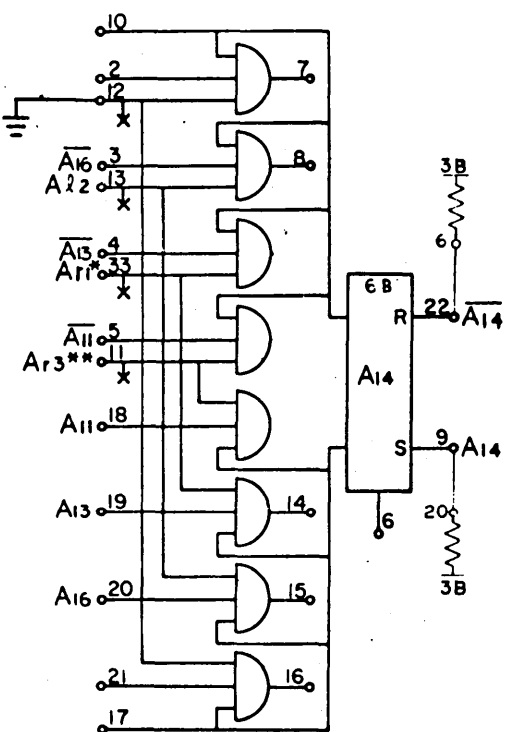
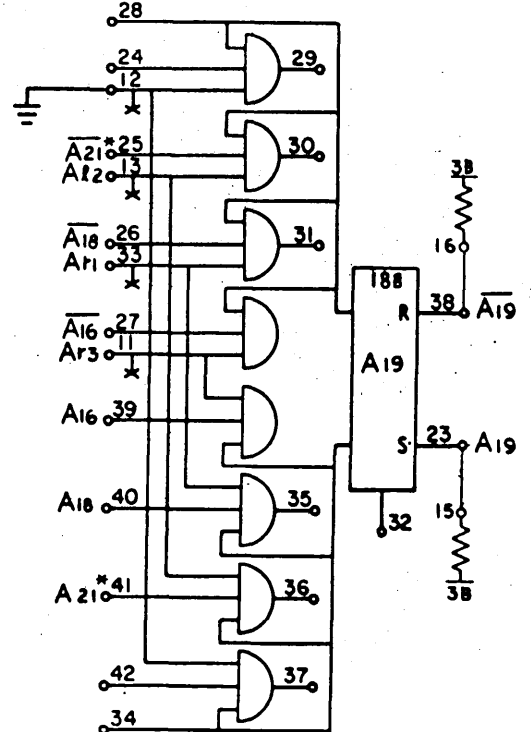
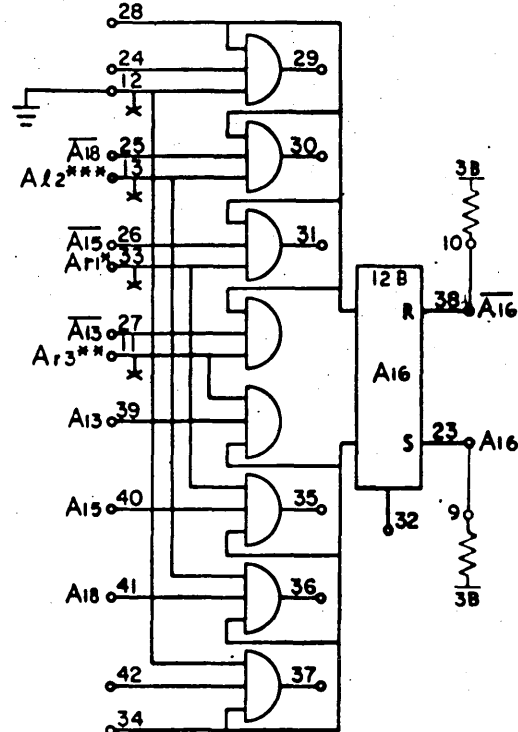
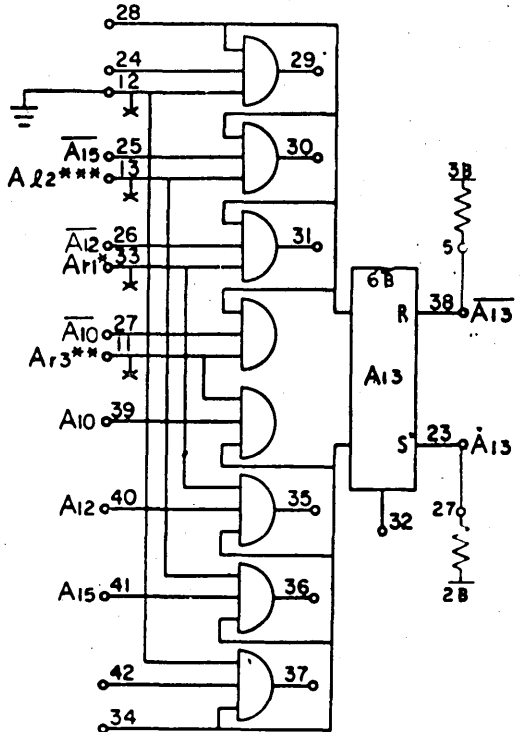
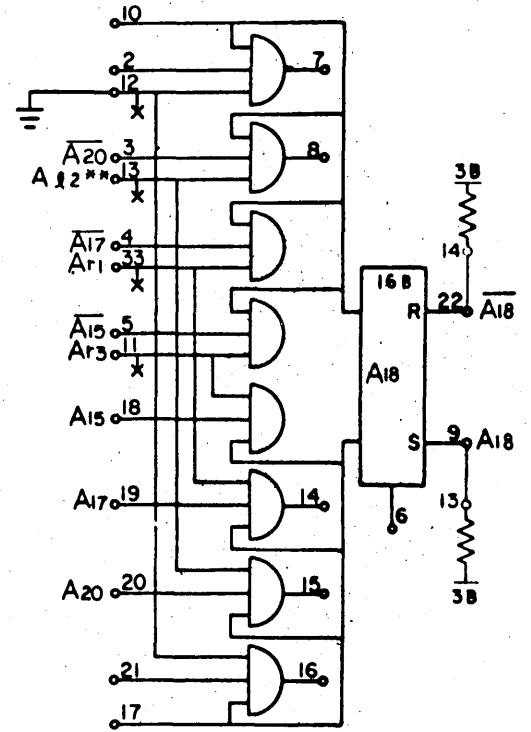
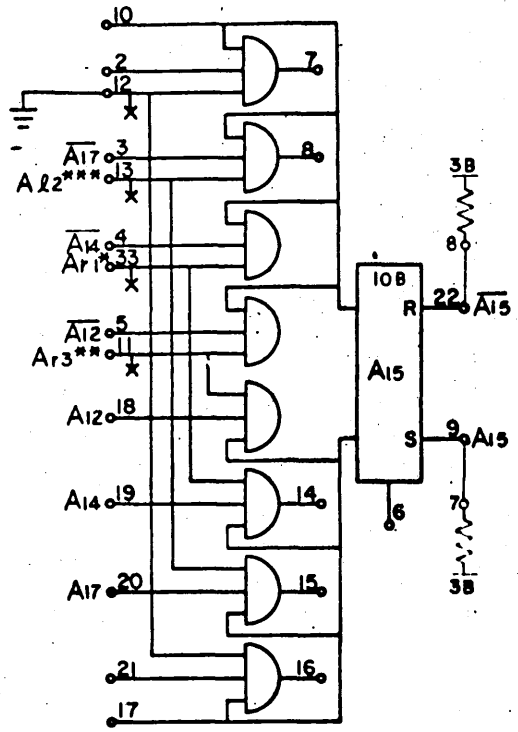
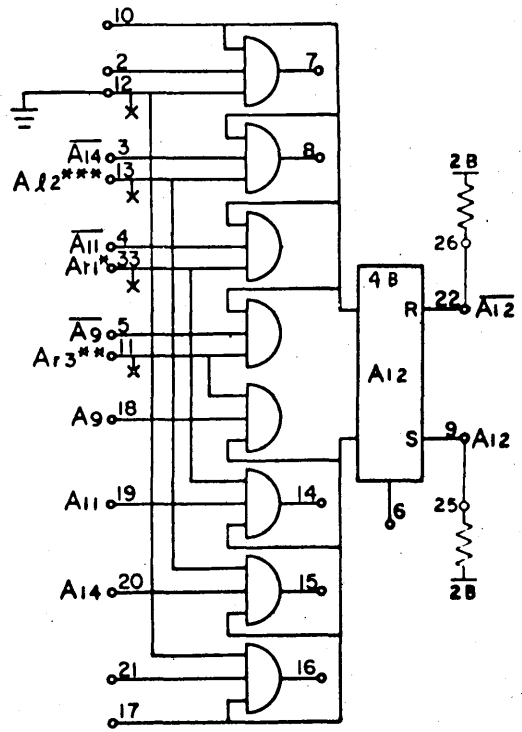
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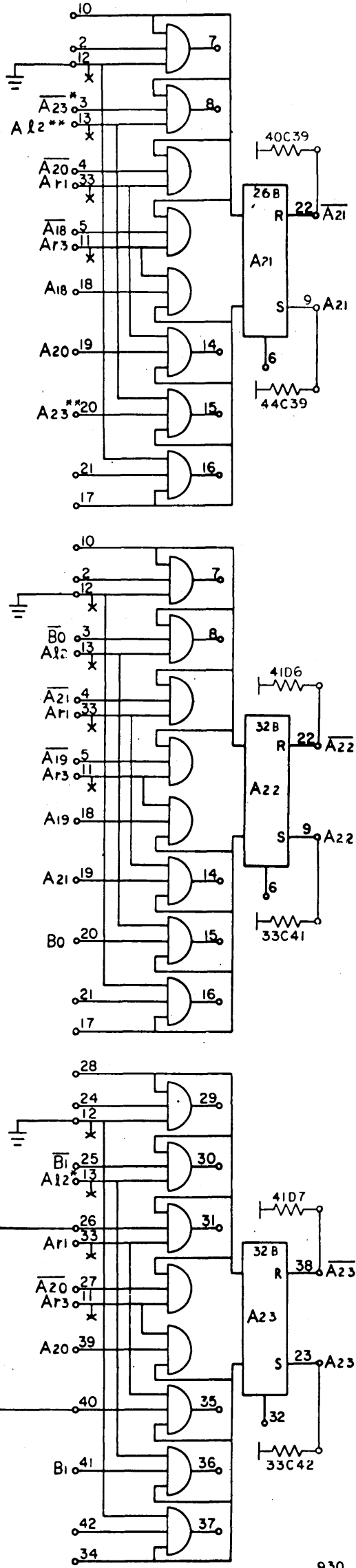
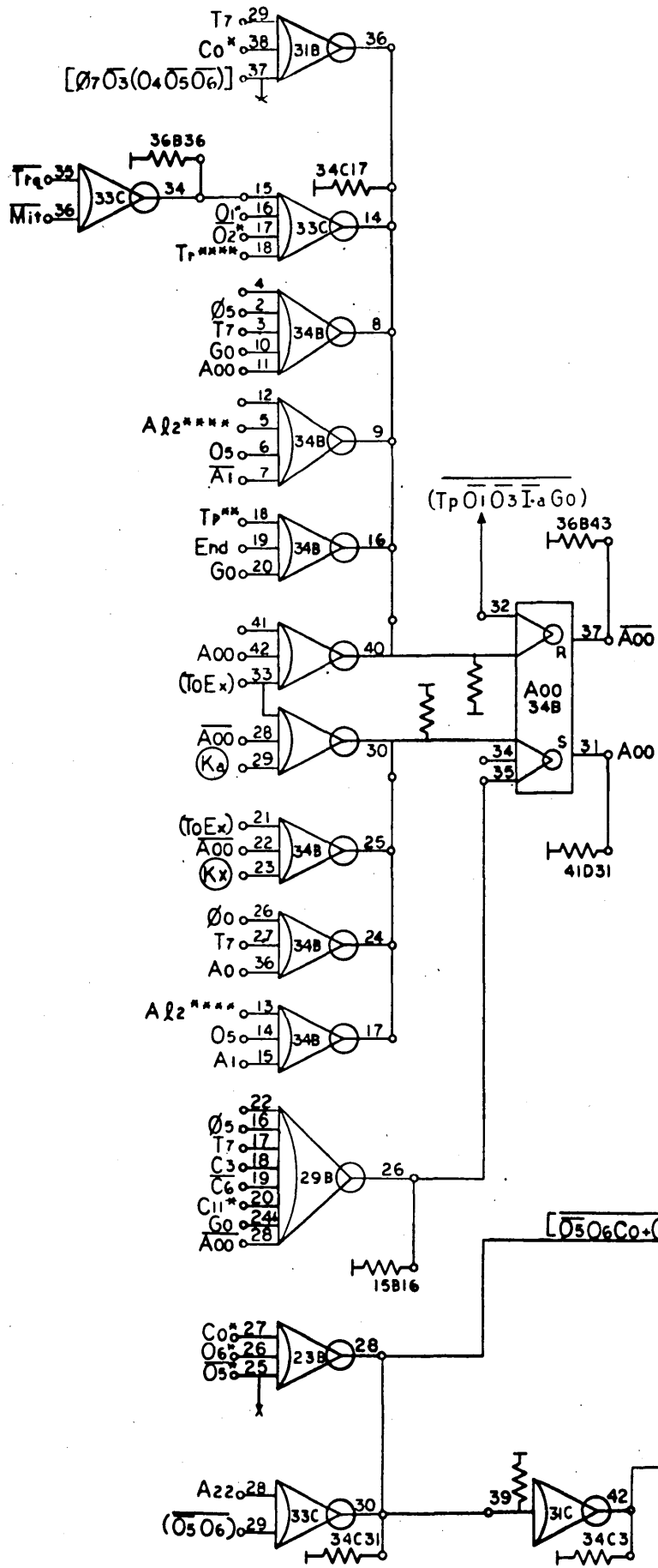
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DIAGRAM, LOGIC
COMPUTER



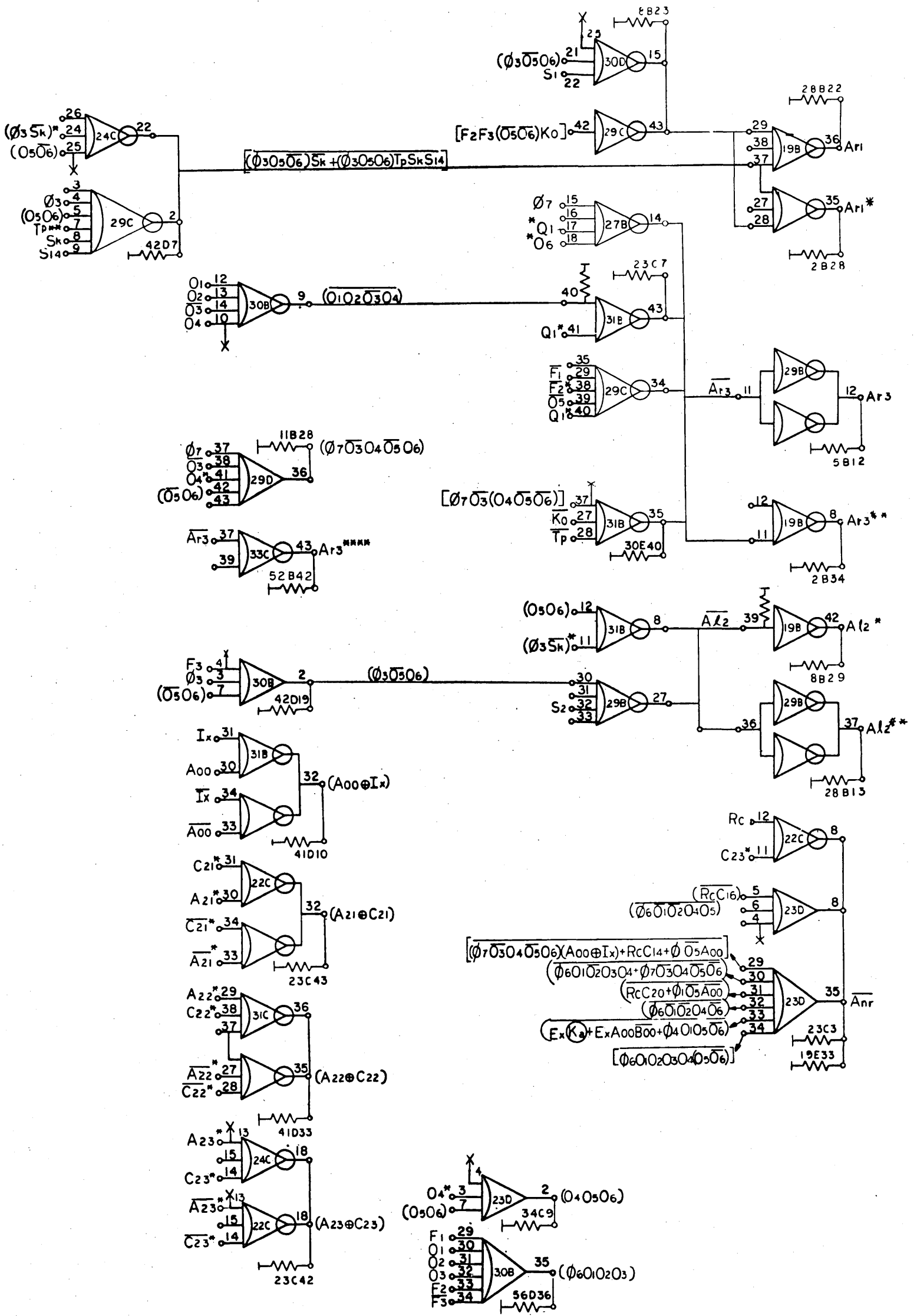
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PAGE 35
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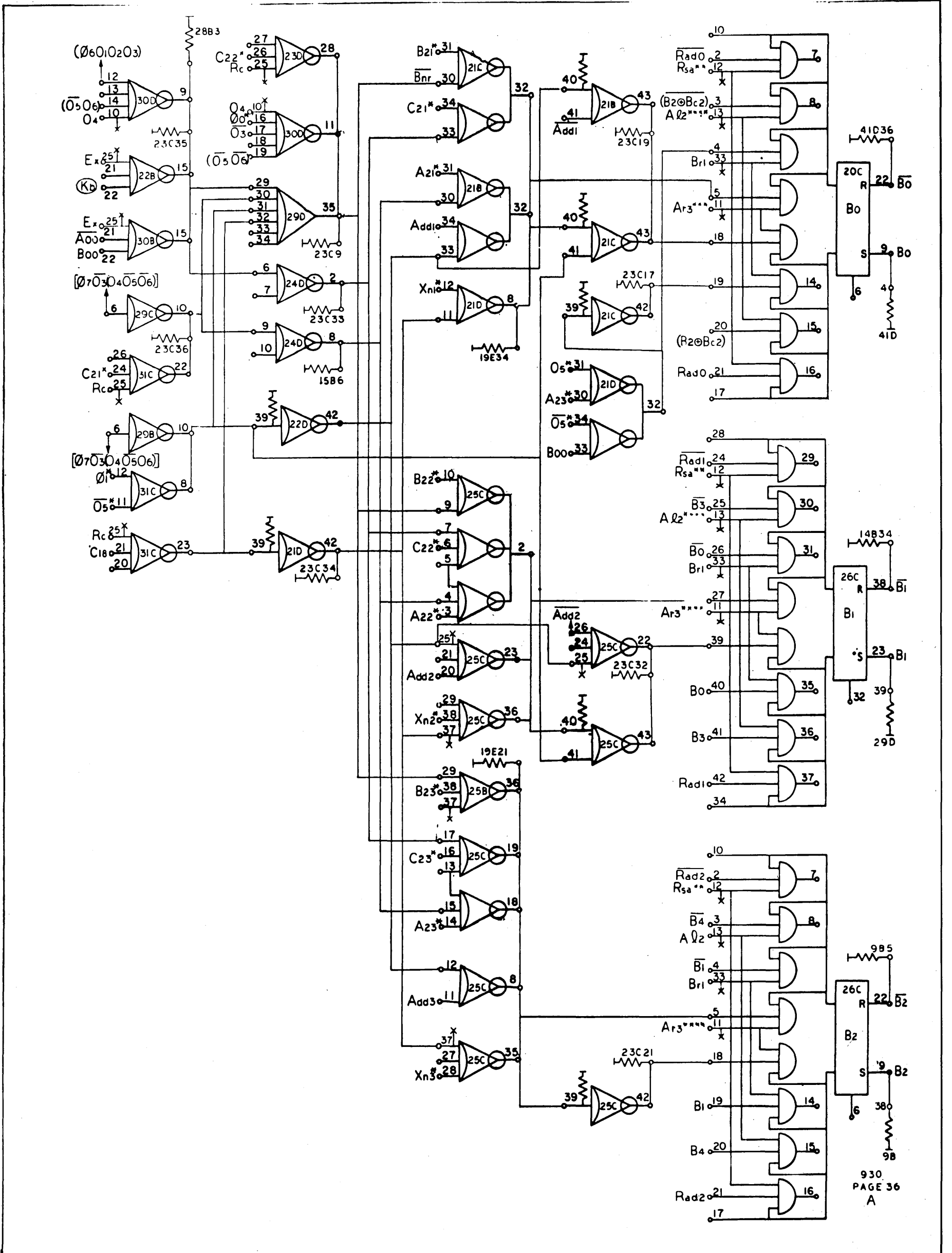
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COMPUTER



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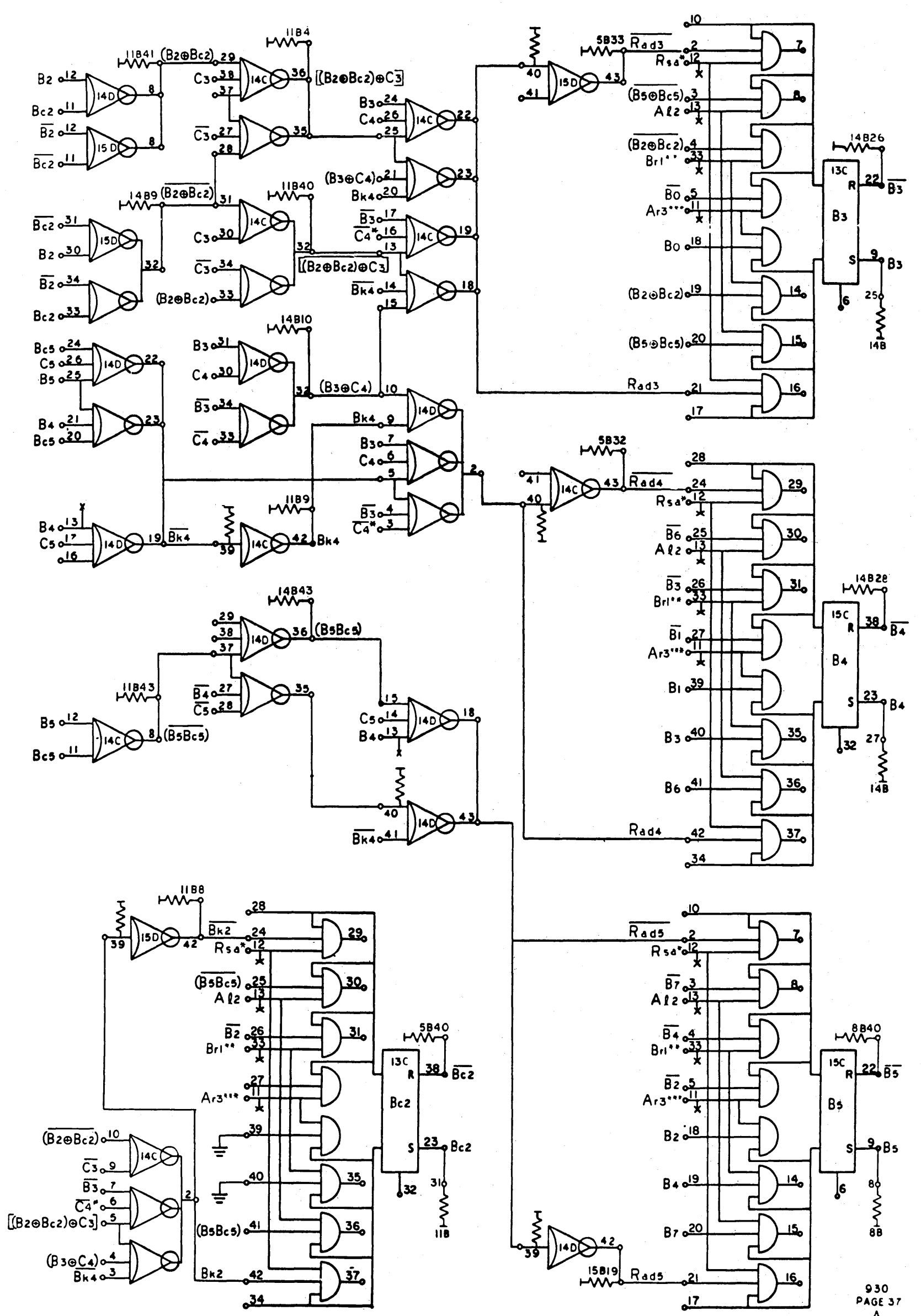
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PAGE 36
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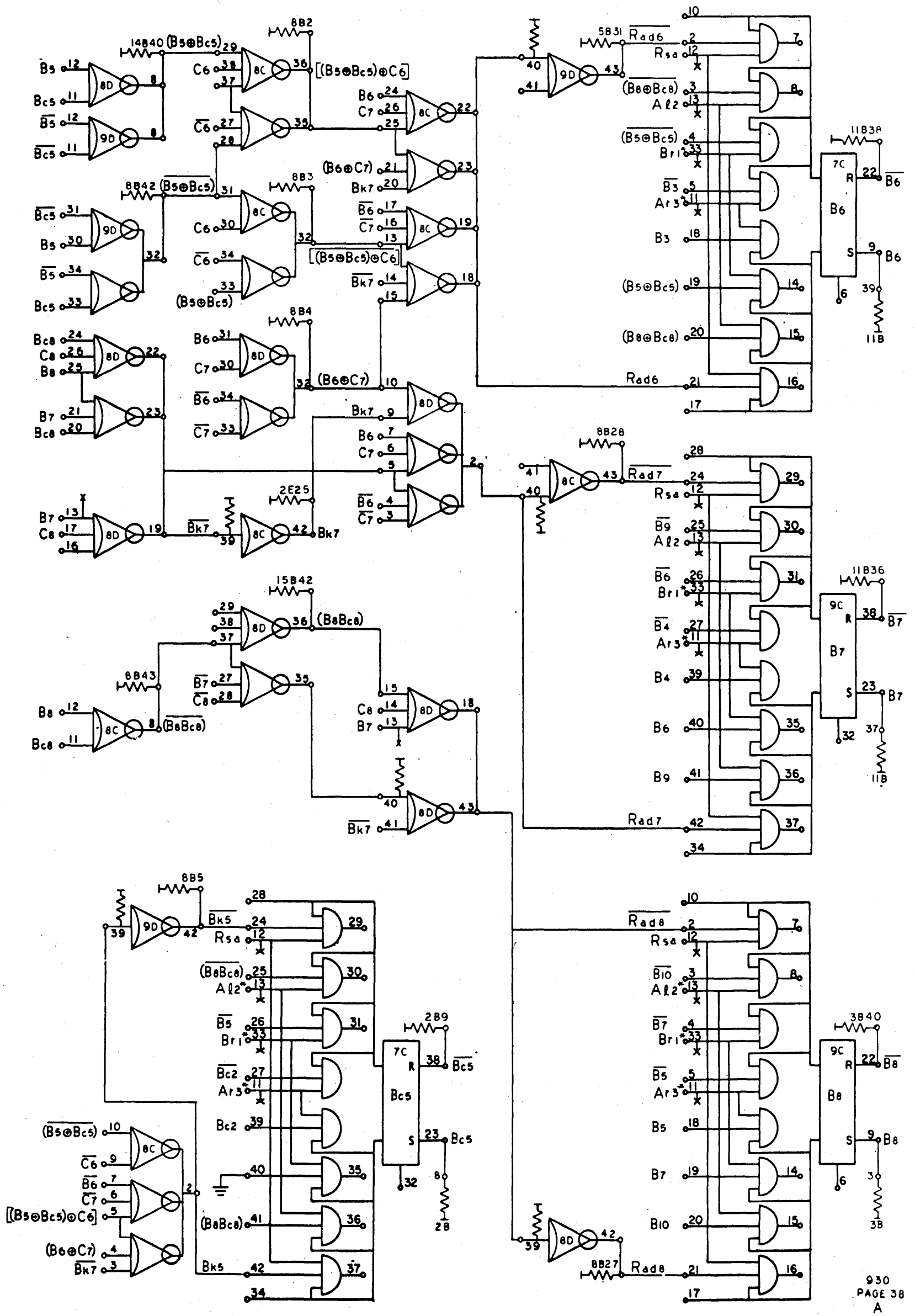


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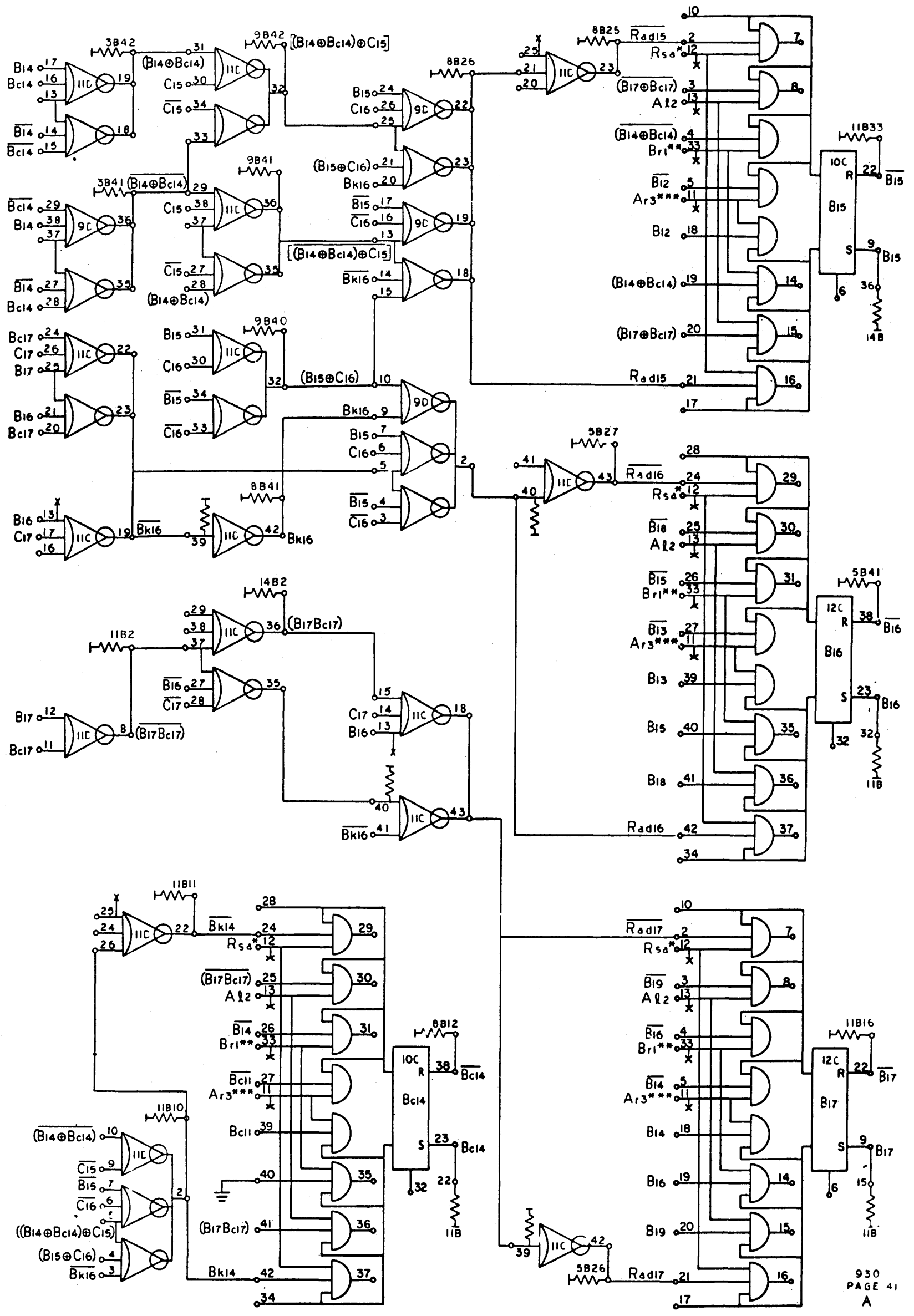
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PAGE 38
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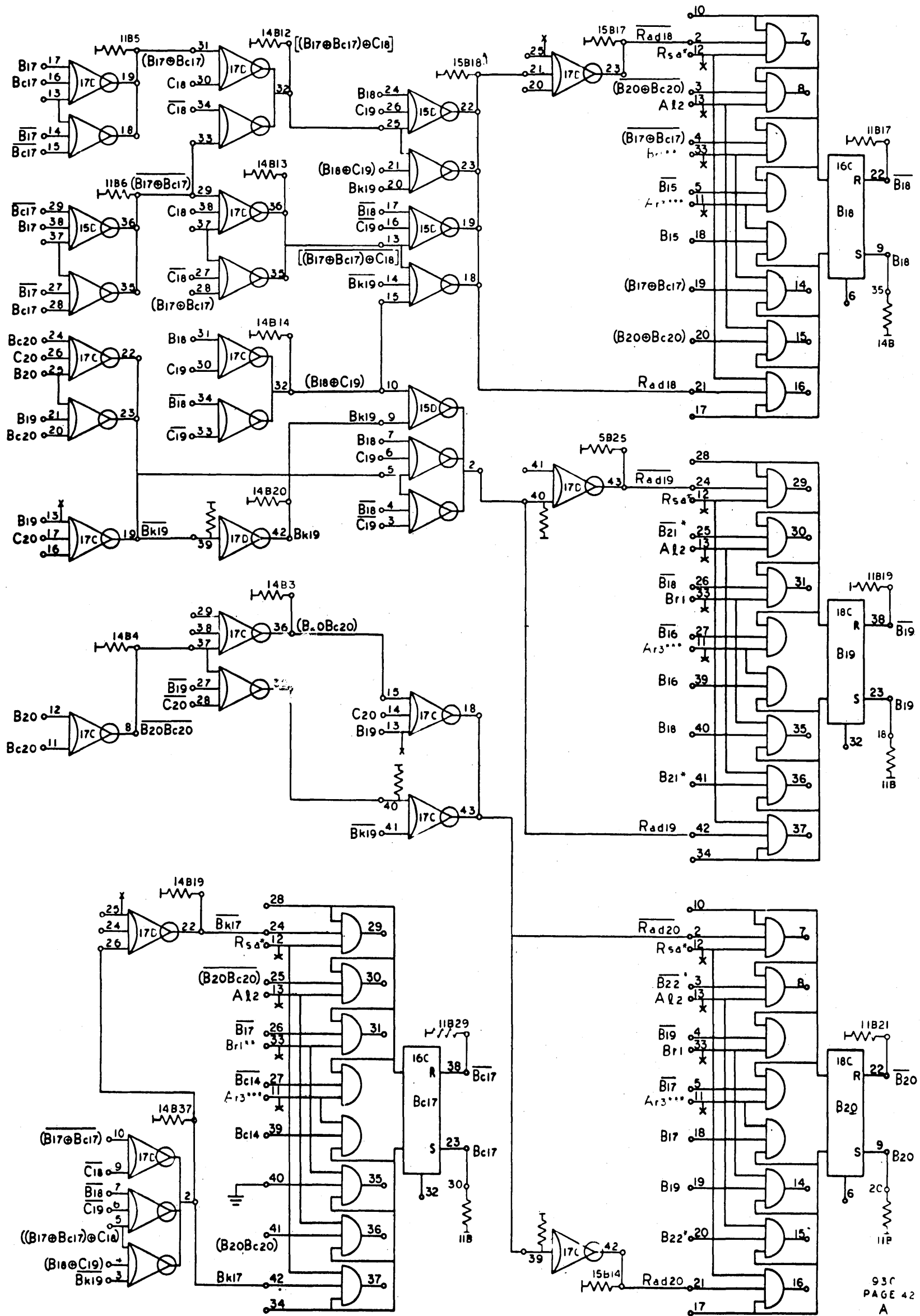
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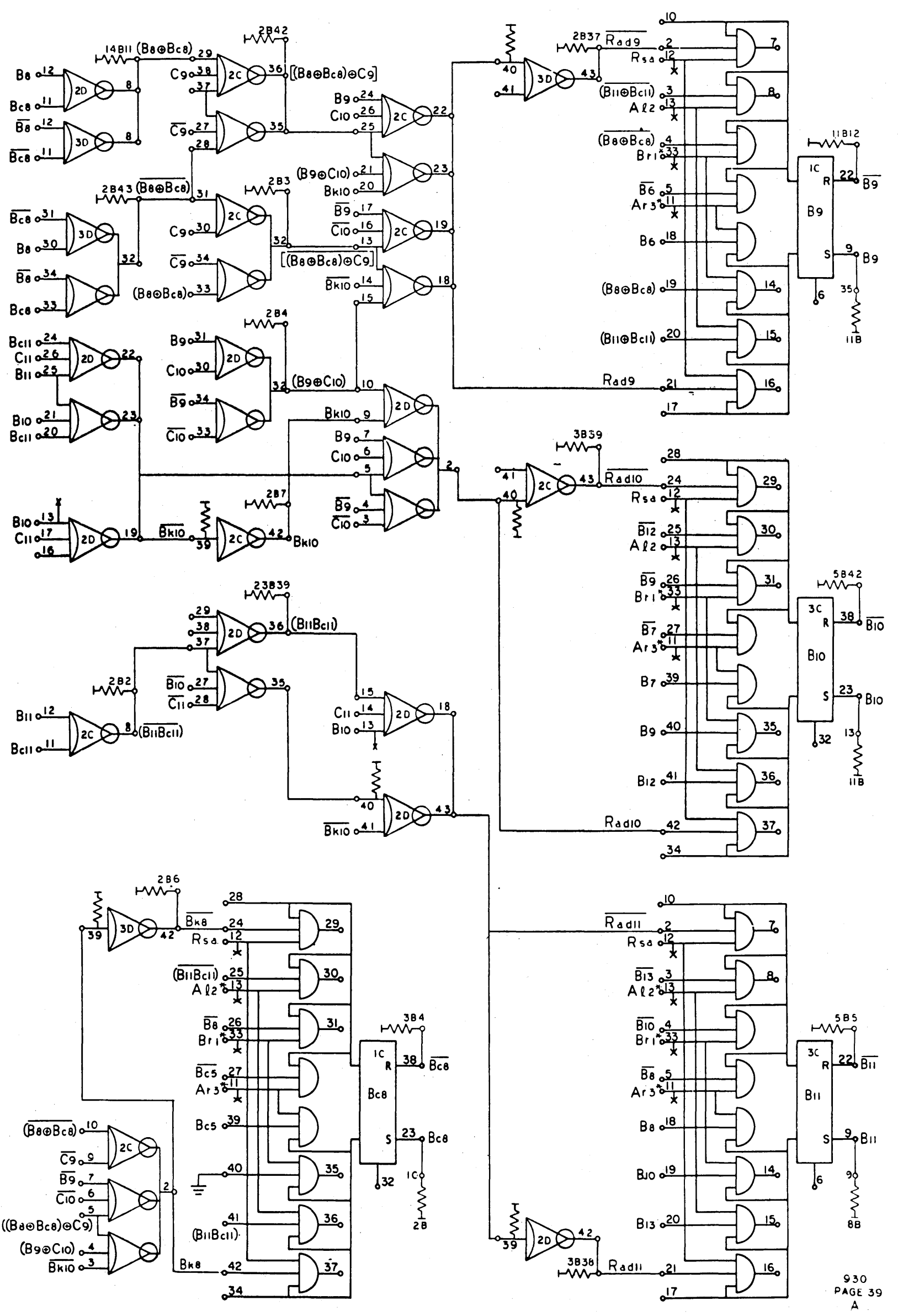
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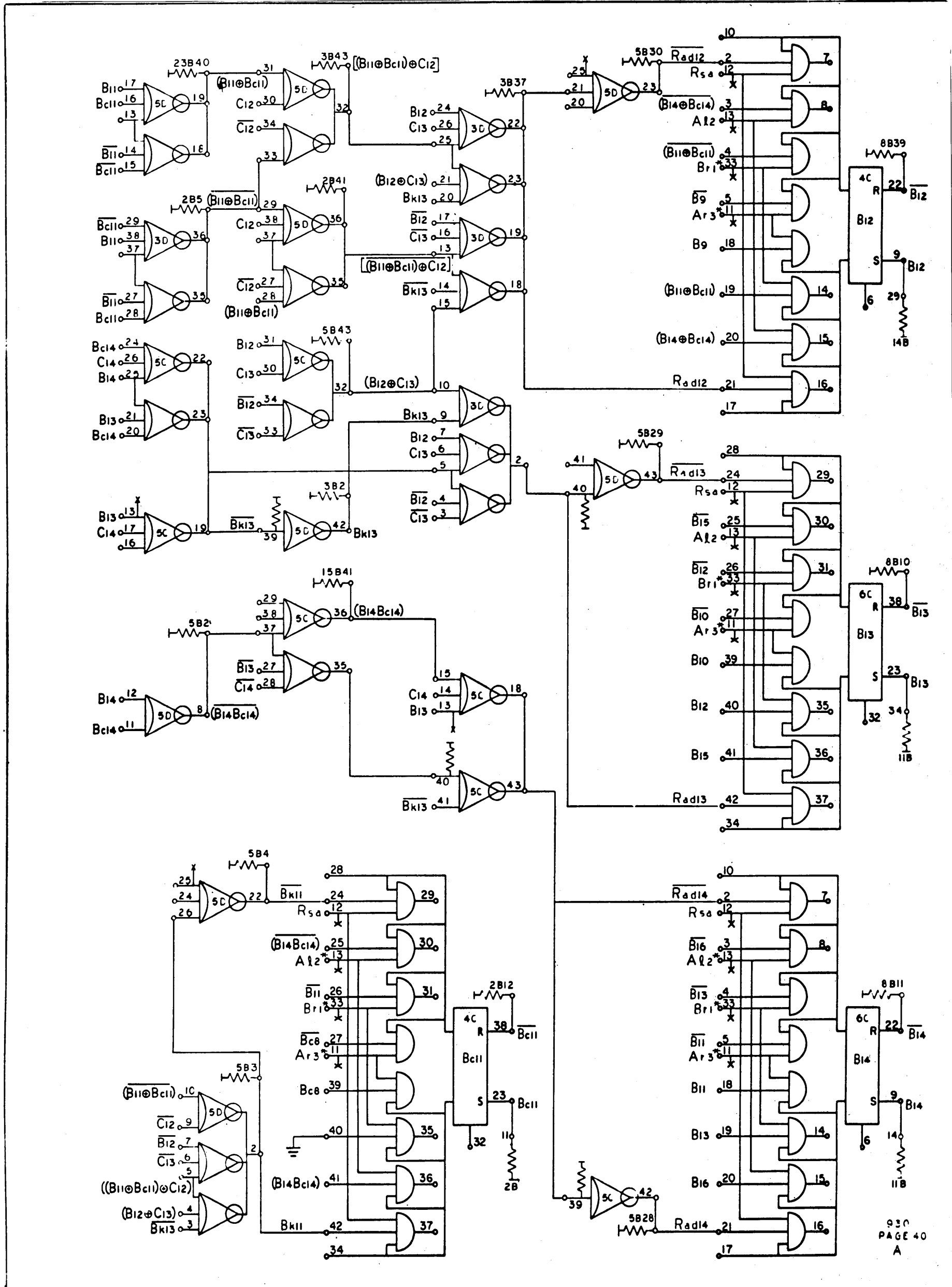
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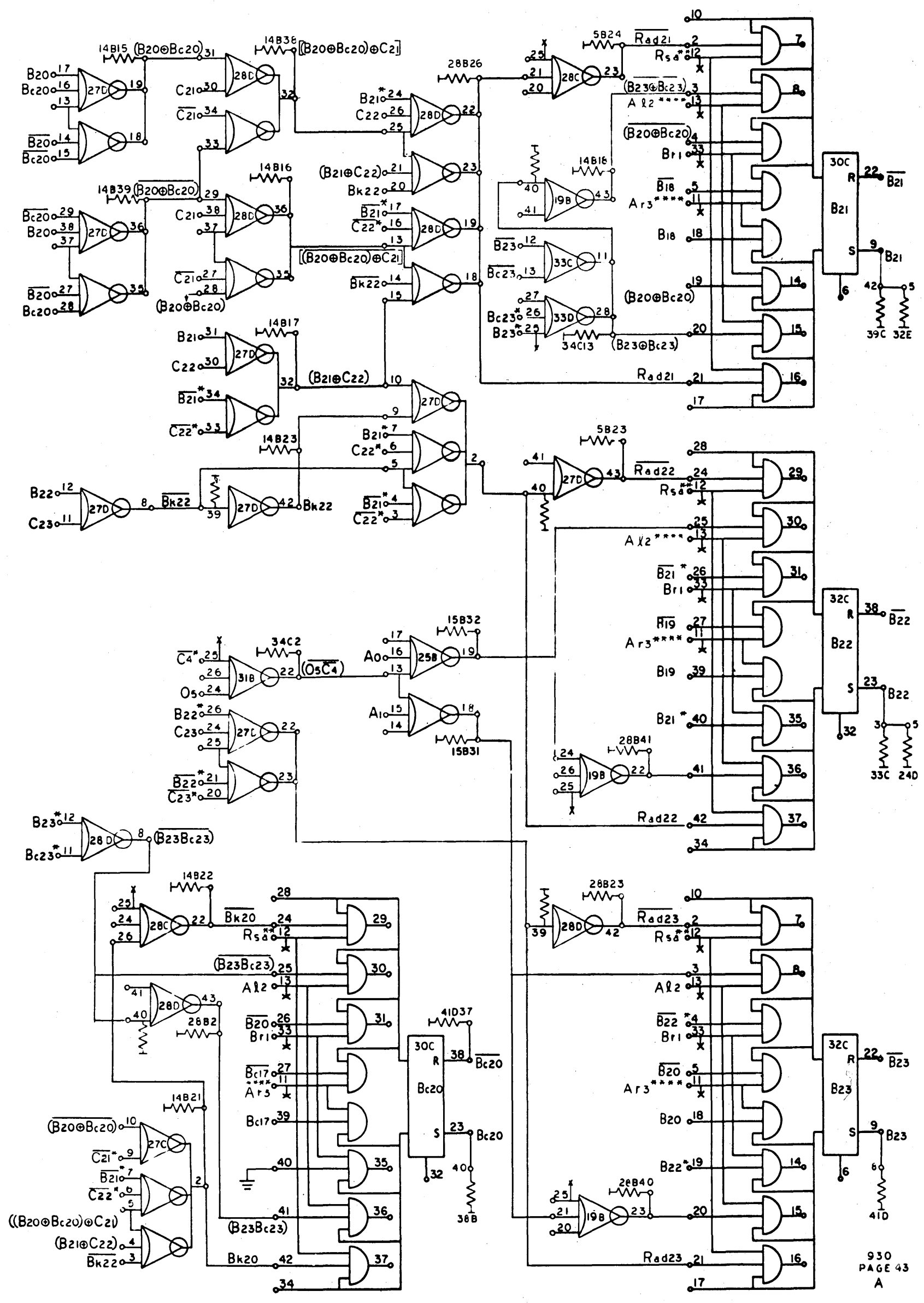
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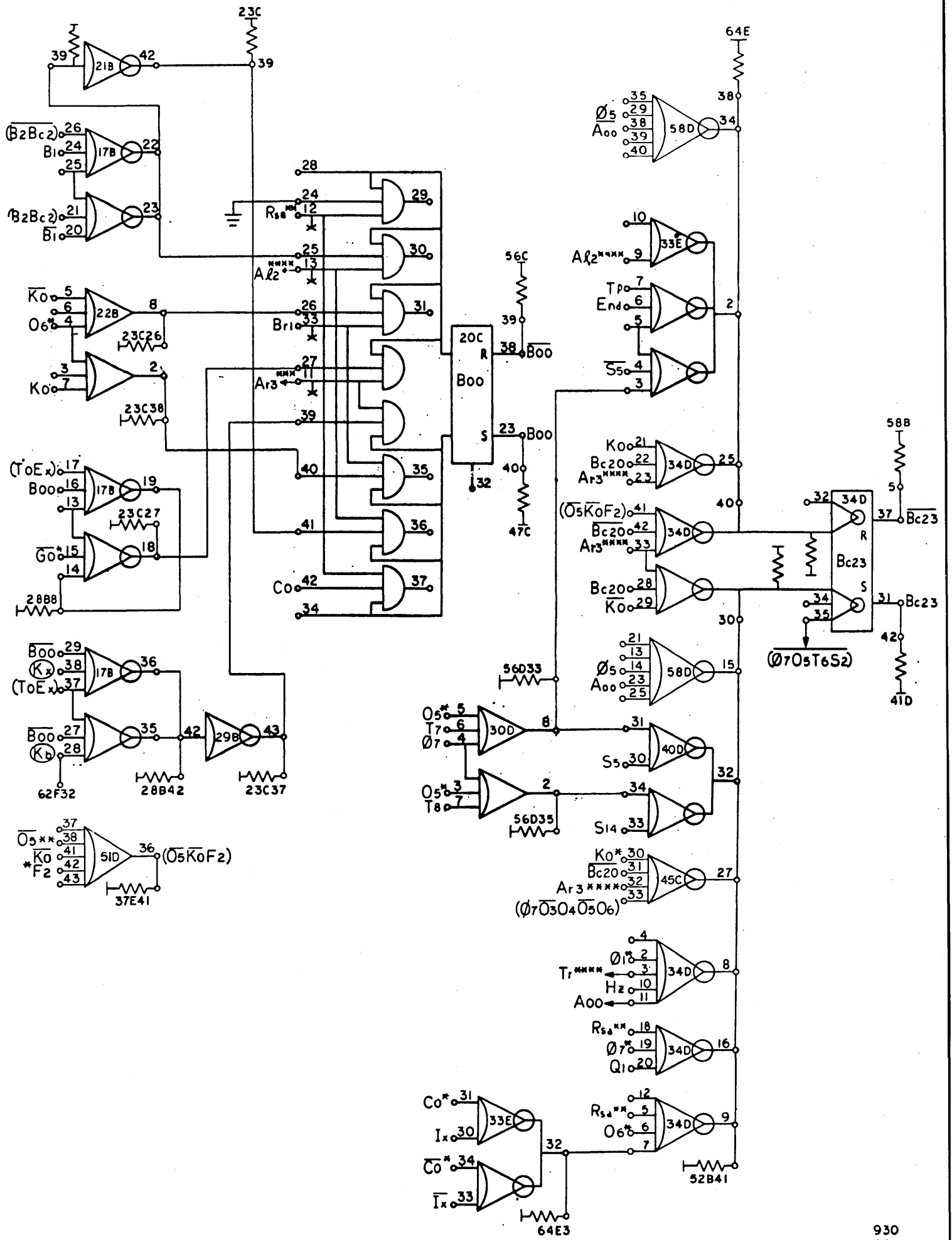
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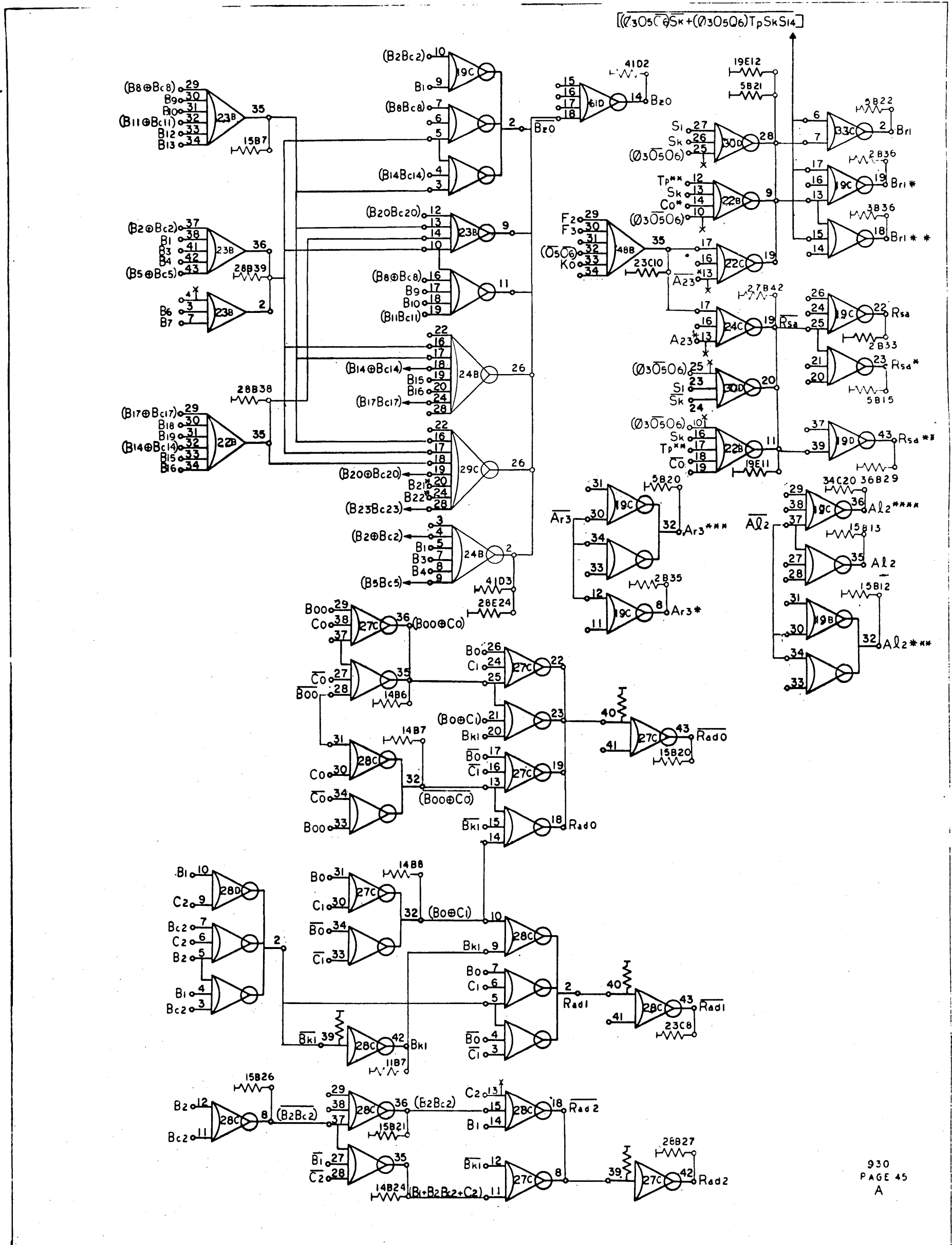


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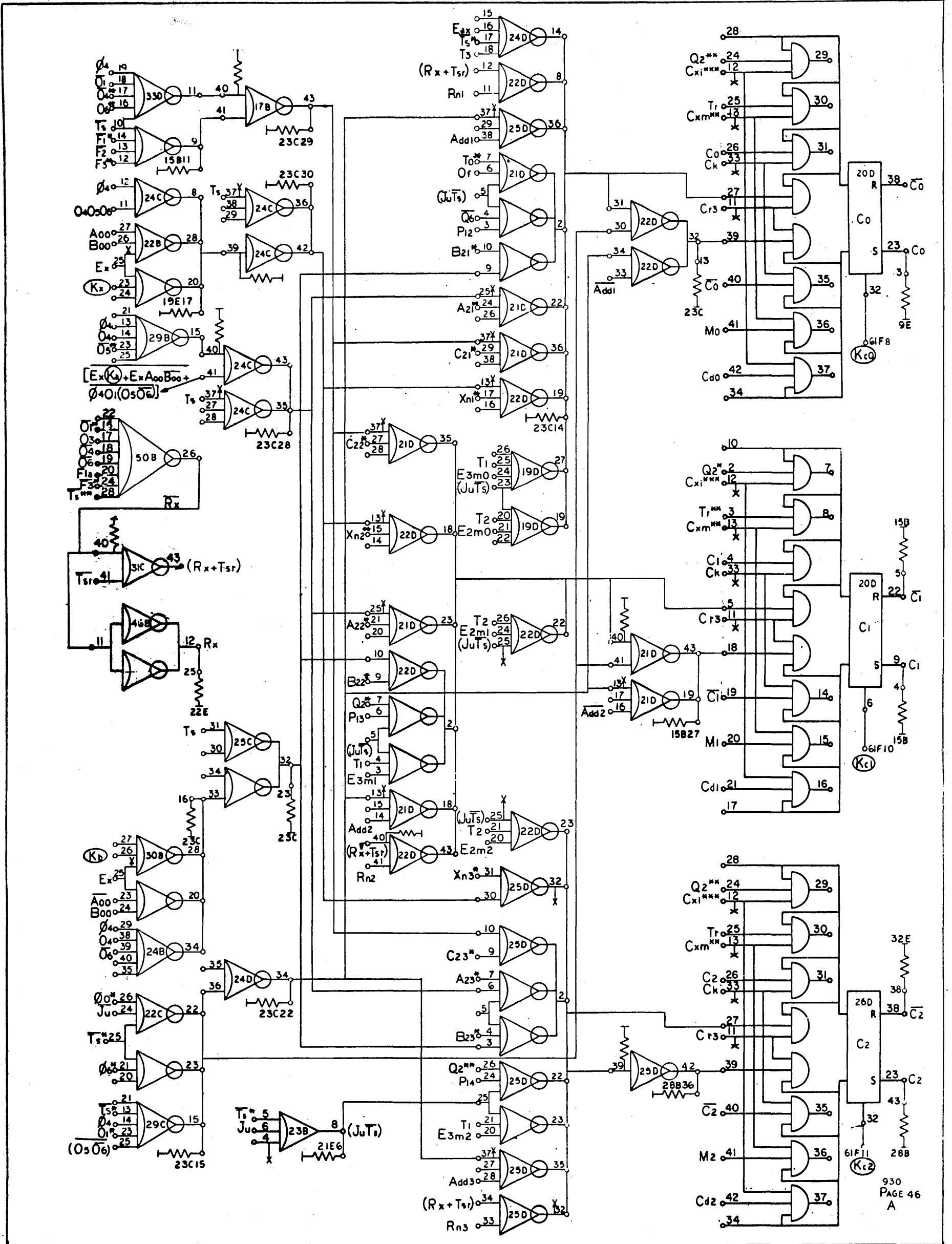
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930	106407	A
DIAGRAM, LOGIC COMPUTER		
<small>Standard Data Systems, Inc., 1400 North 17th Street, Phoenix, Arizona 85016</small>		
REV	DESCRIPTION	DATE
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PAGE 46
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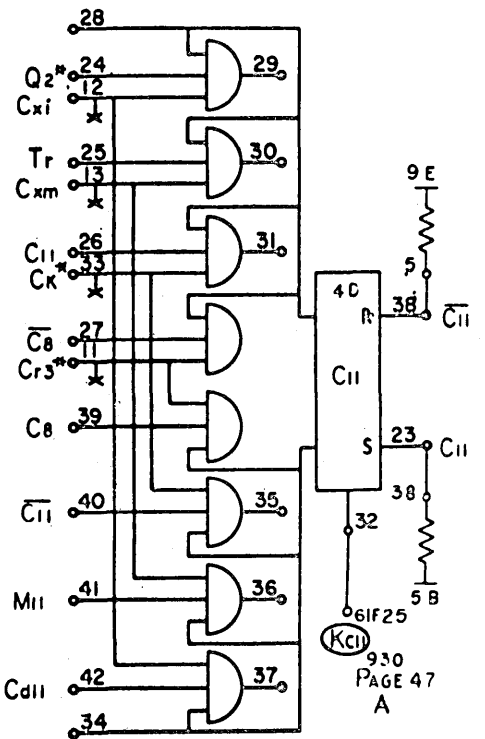
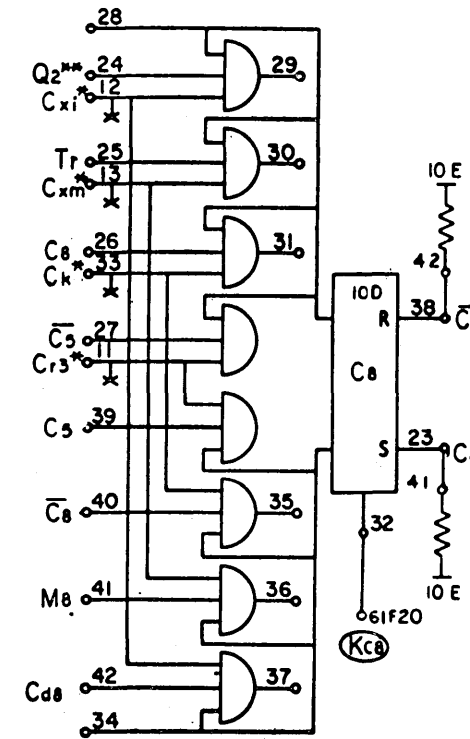
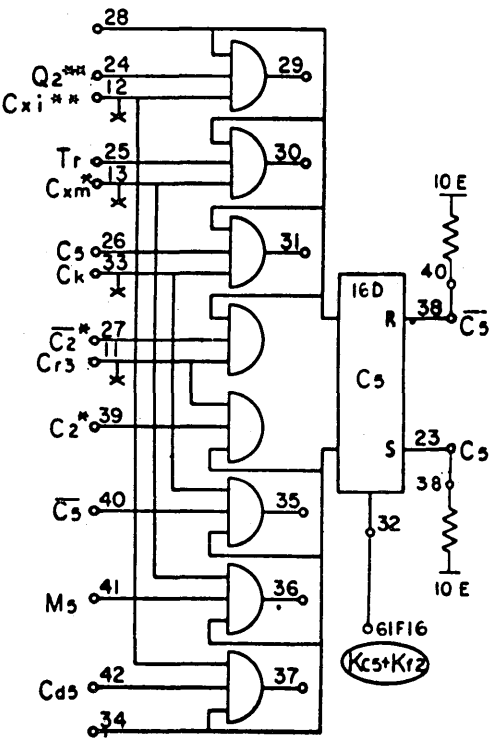
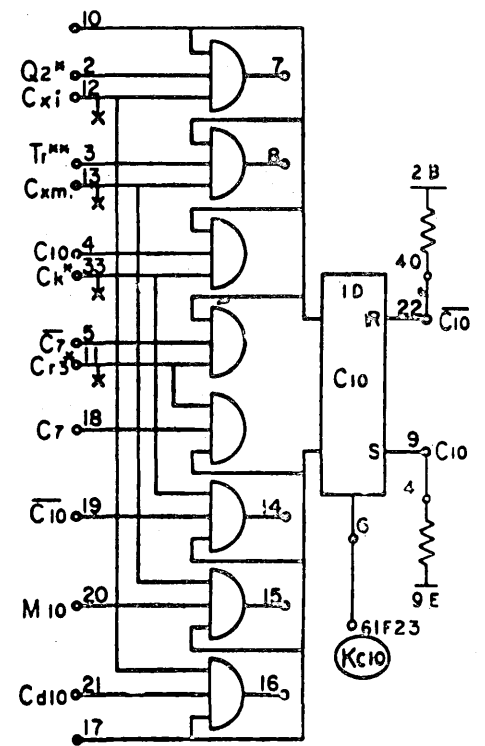
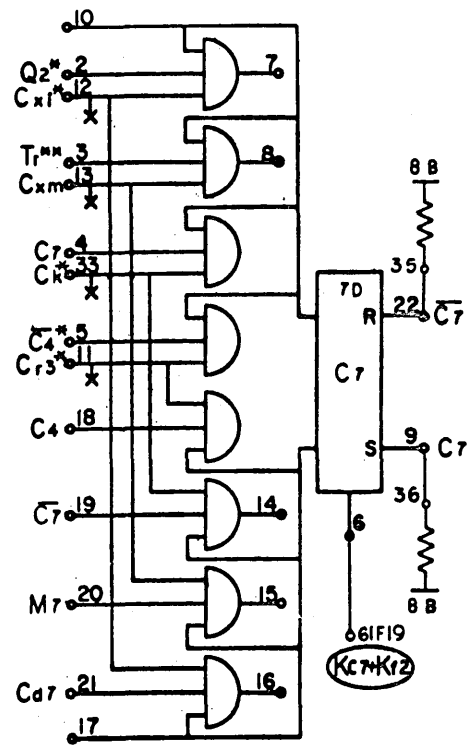
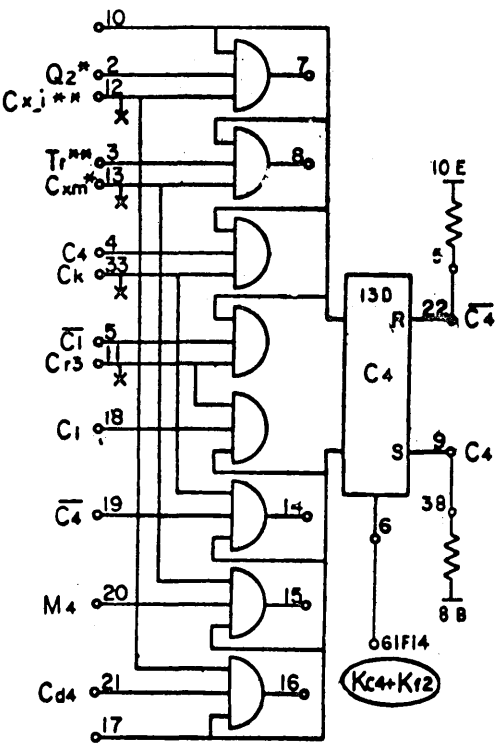
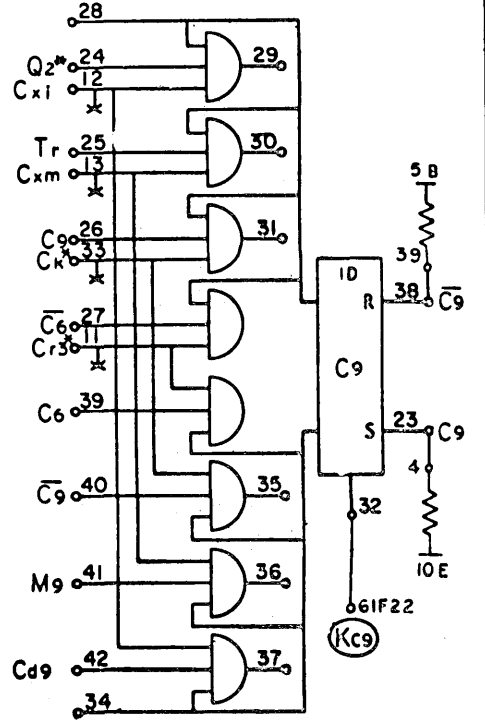
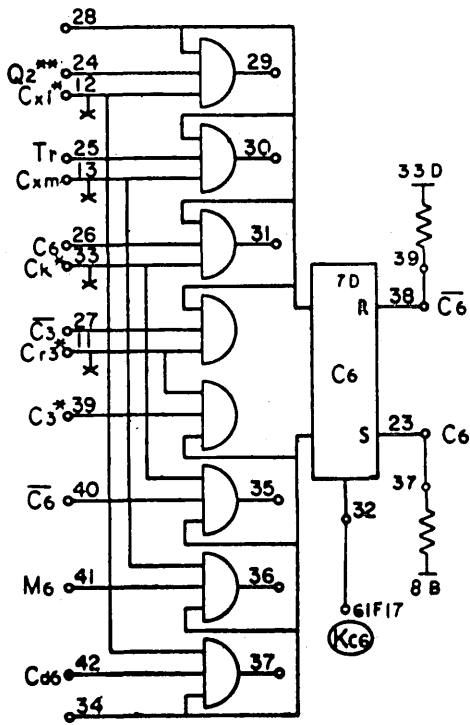
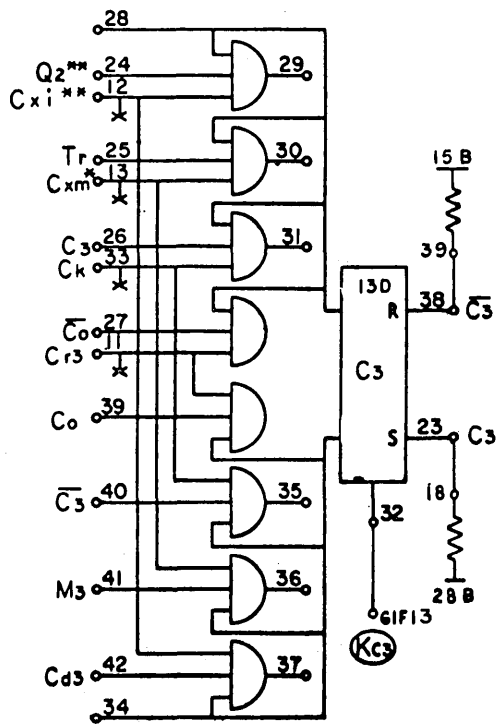
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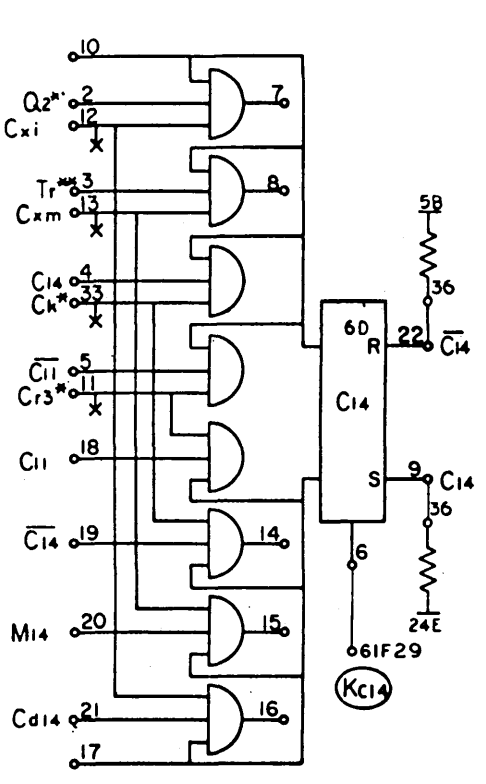
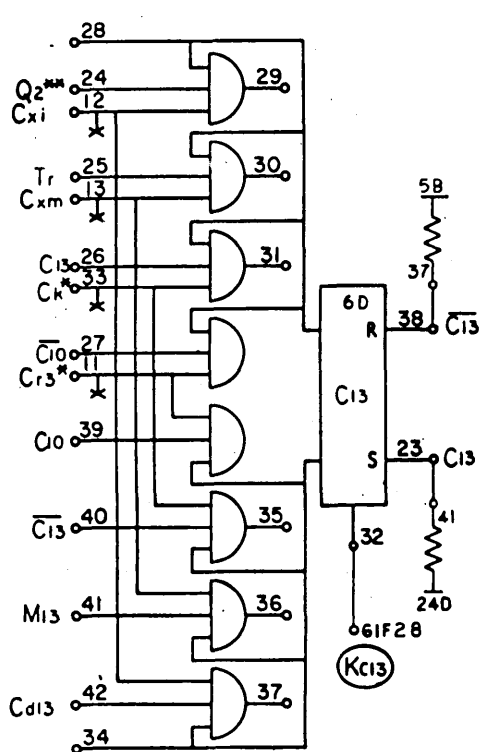
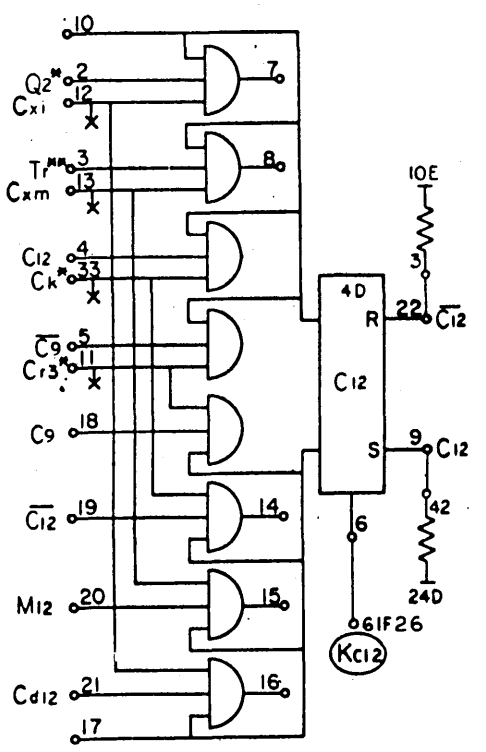
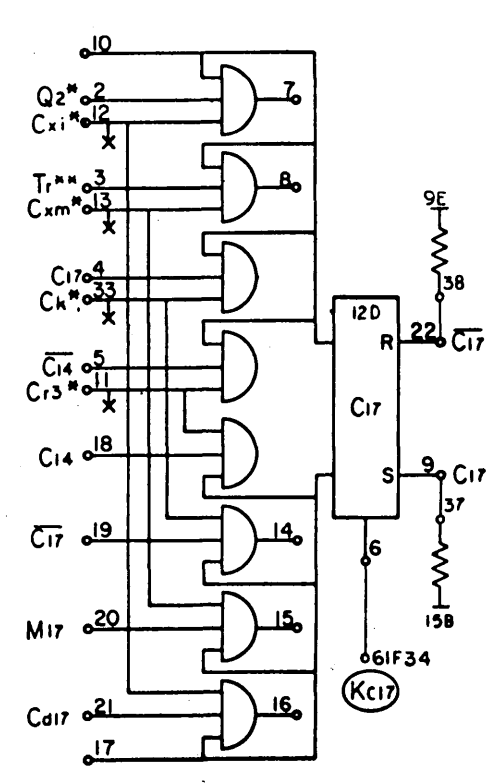
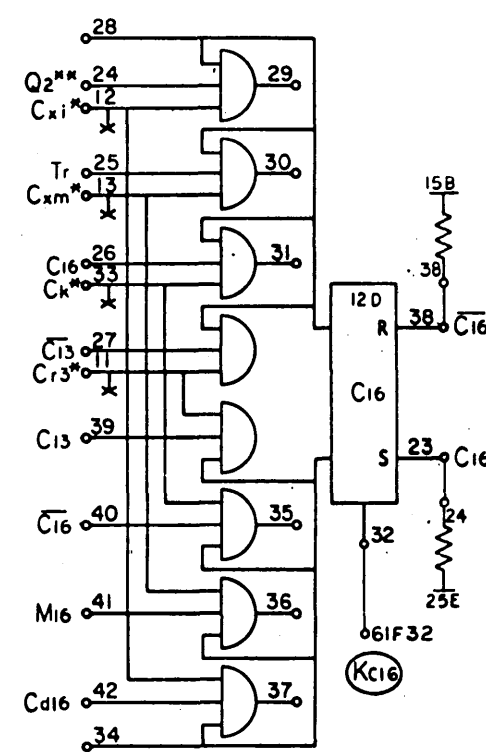
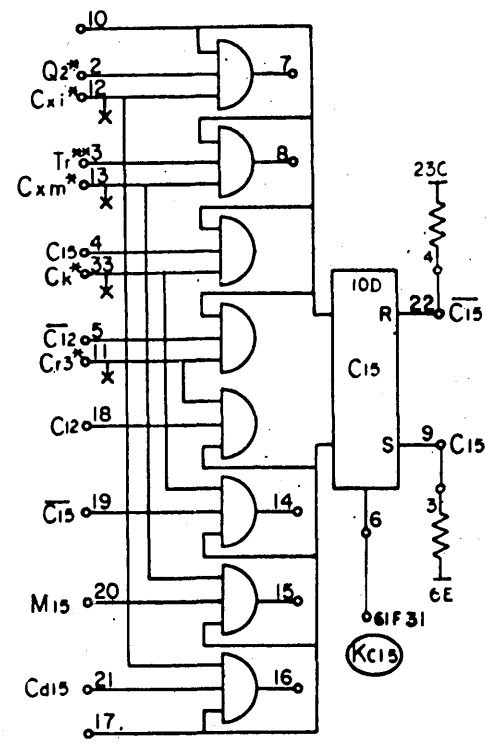
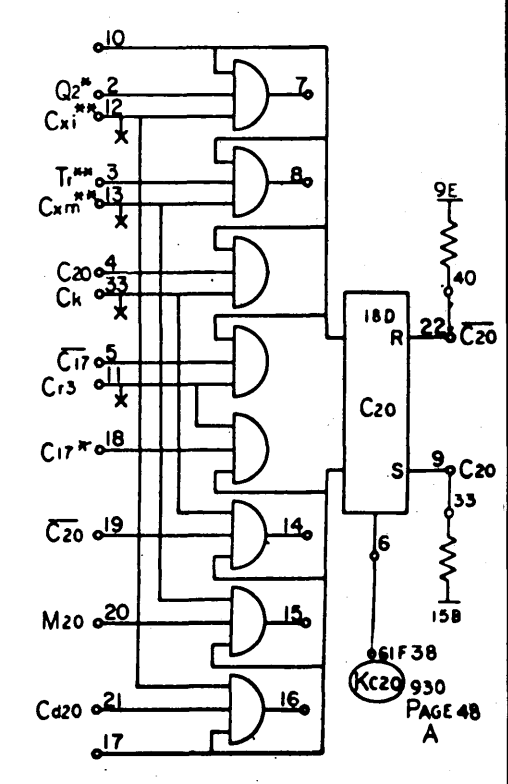
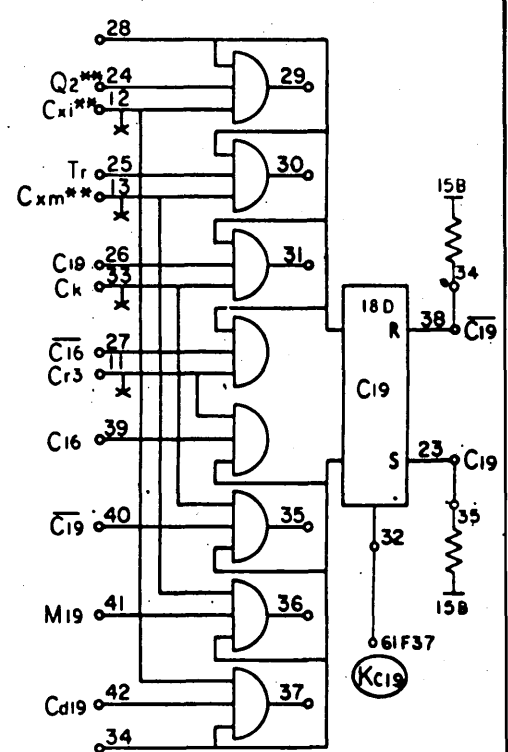
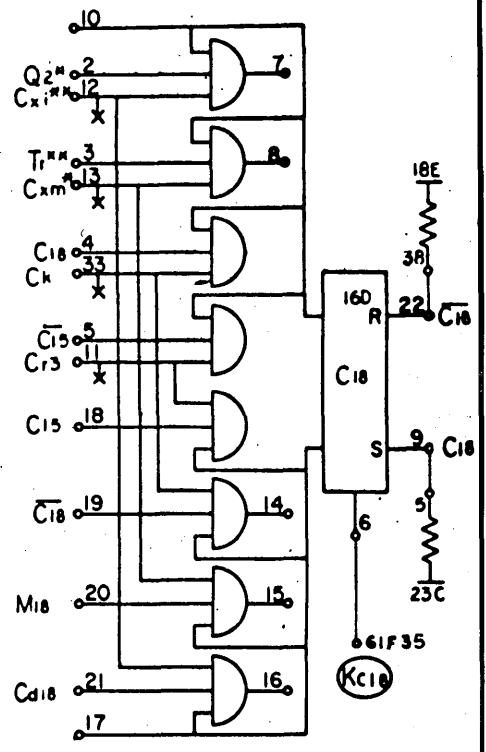


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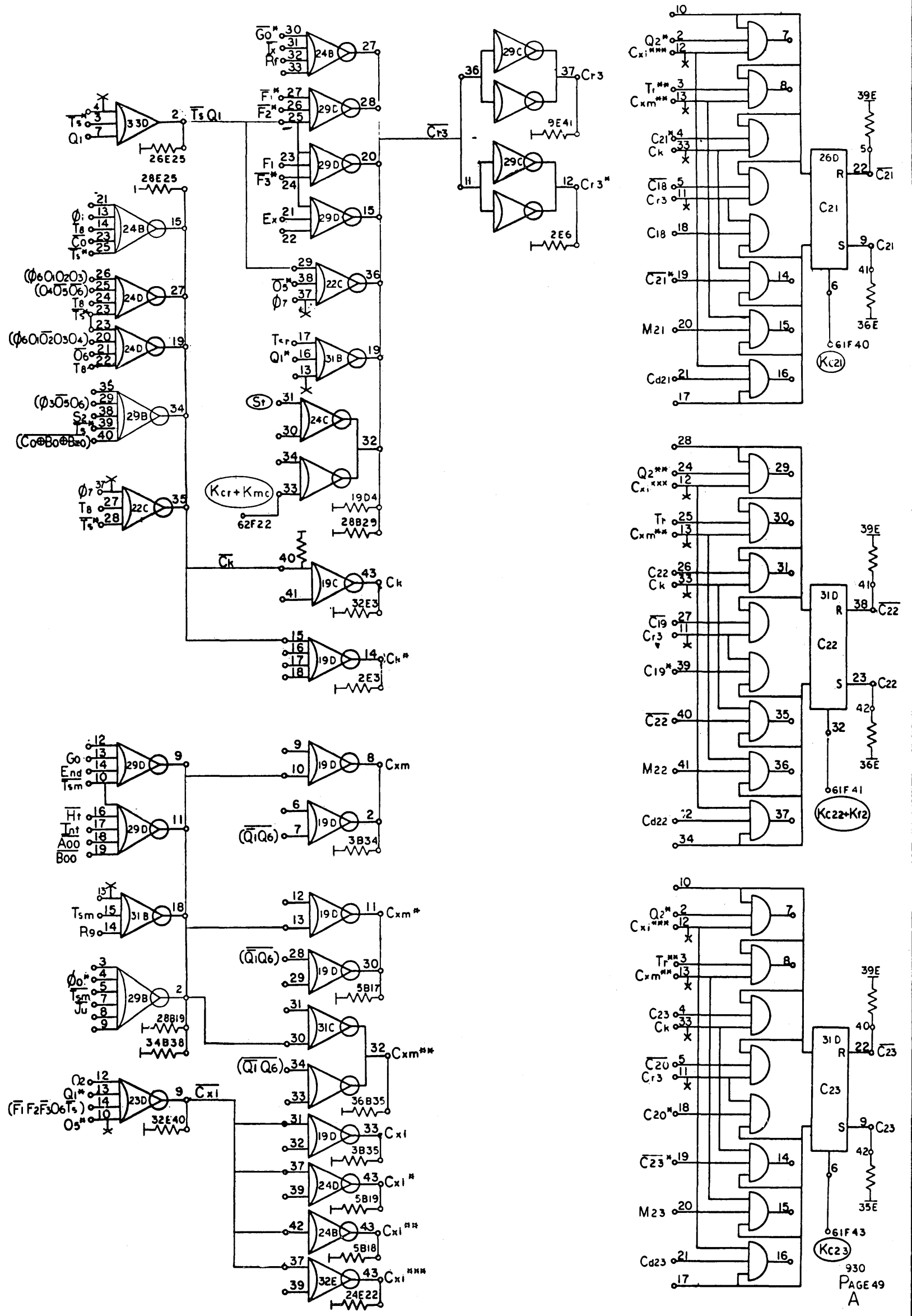
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SYSTEMS SERVICE DIVISION

DIAGRAM, LOGIC
 COMPUTER

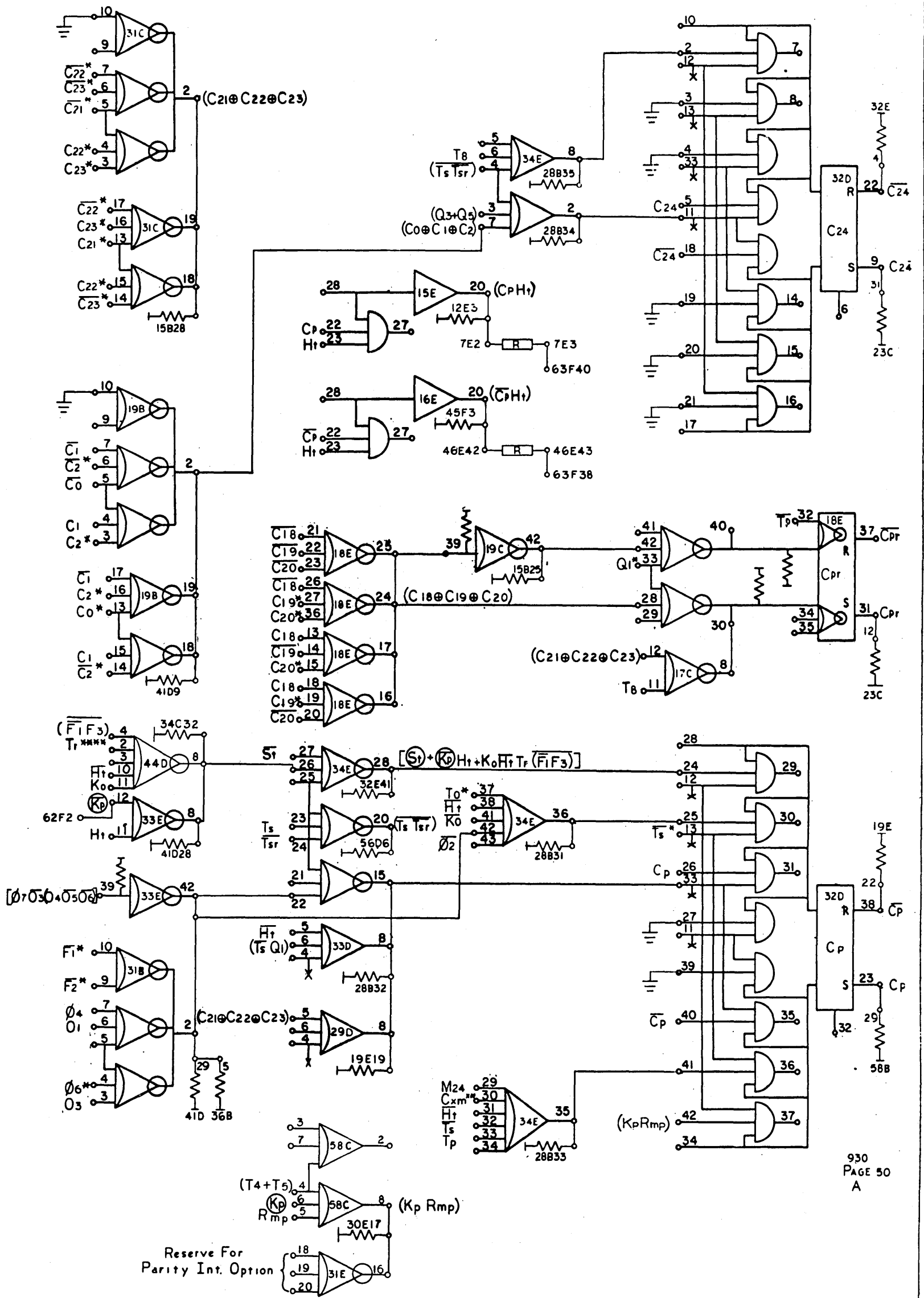
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PAGE 50
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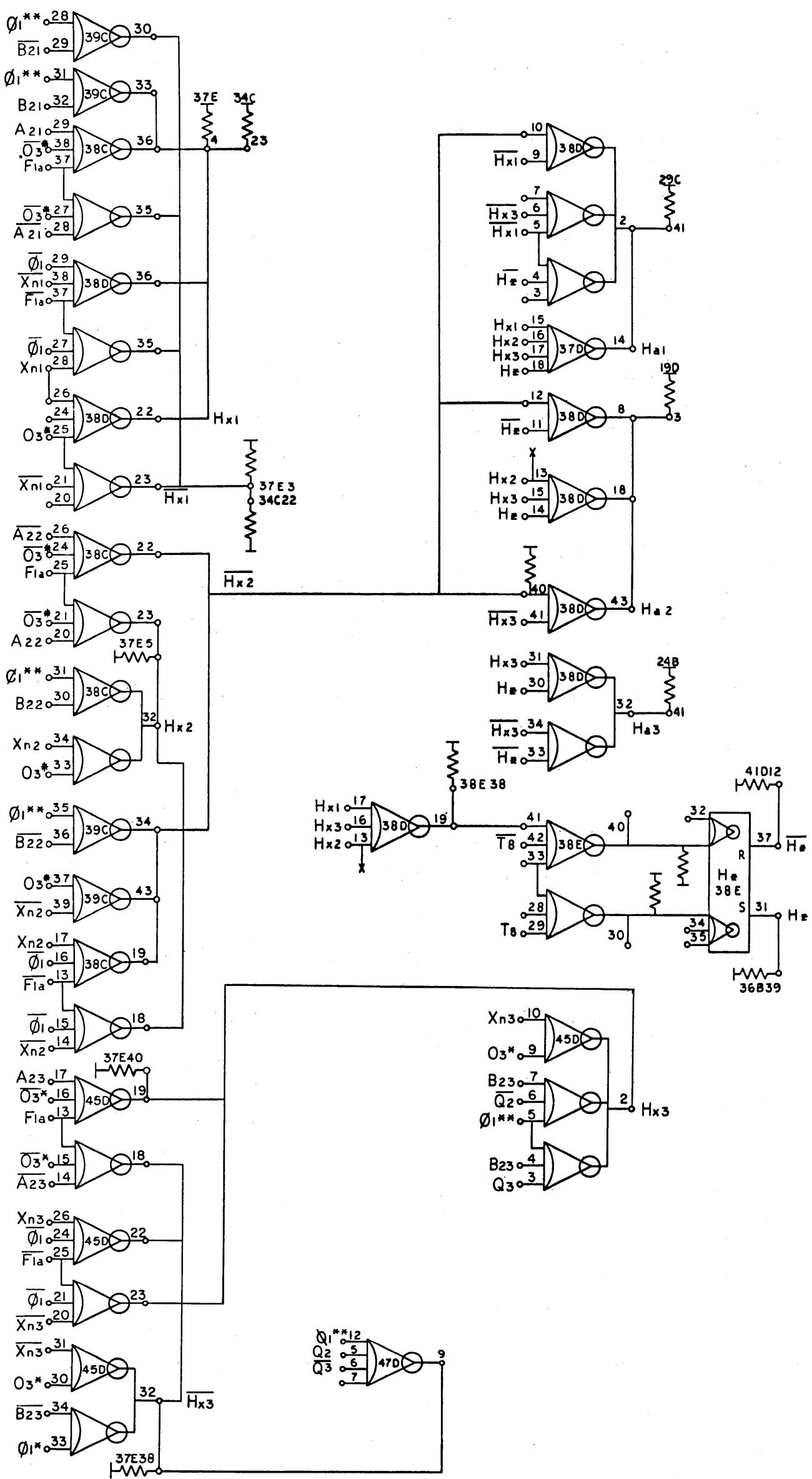
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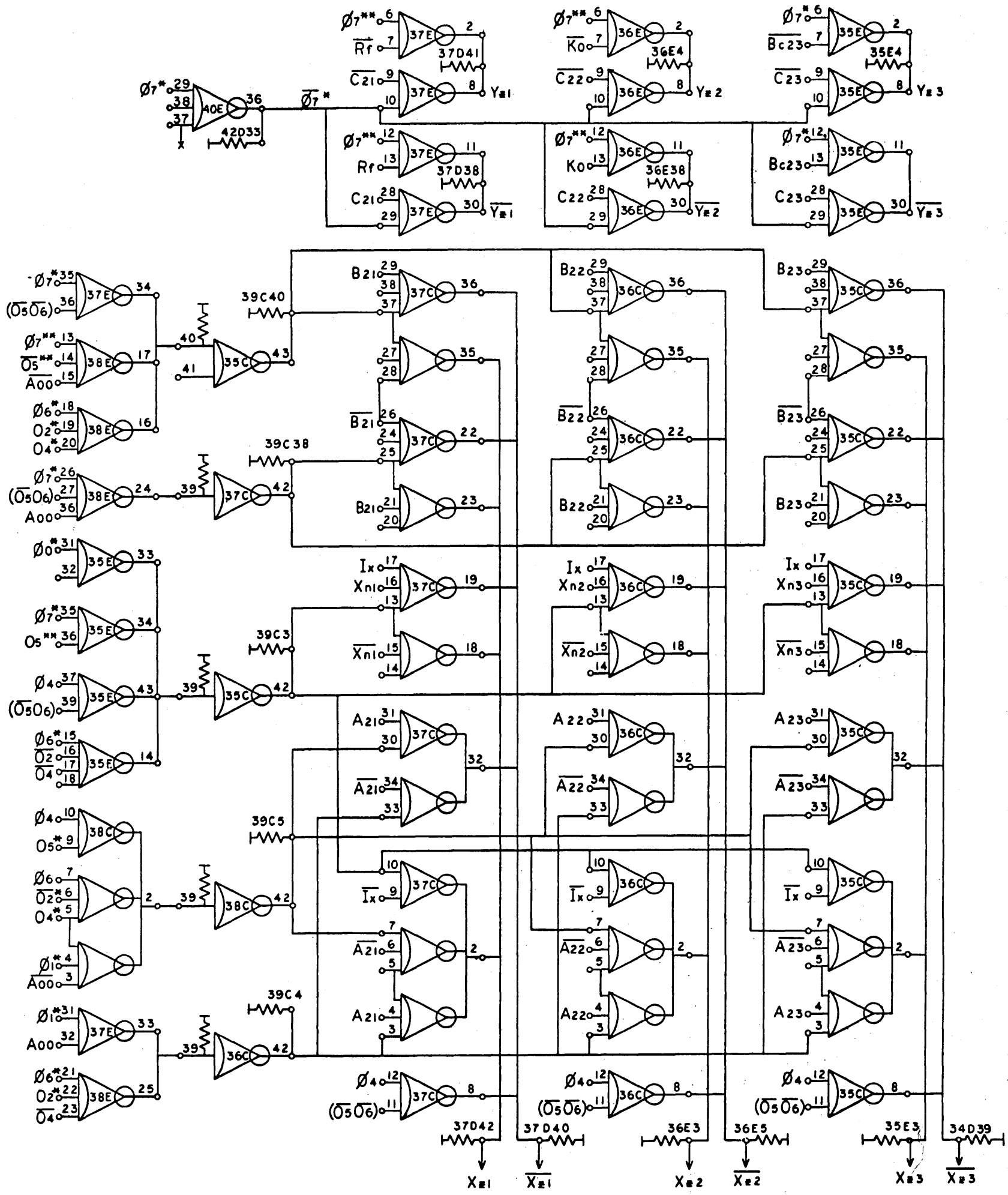


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PAGE 51
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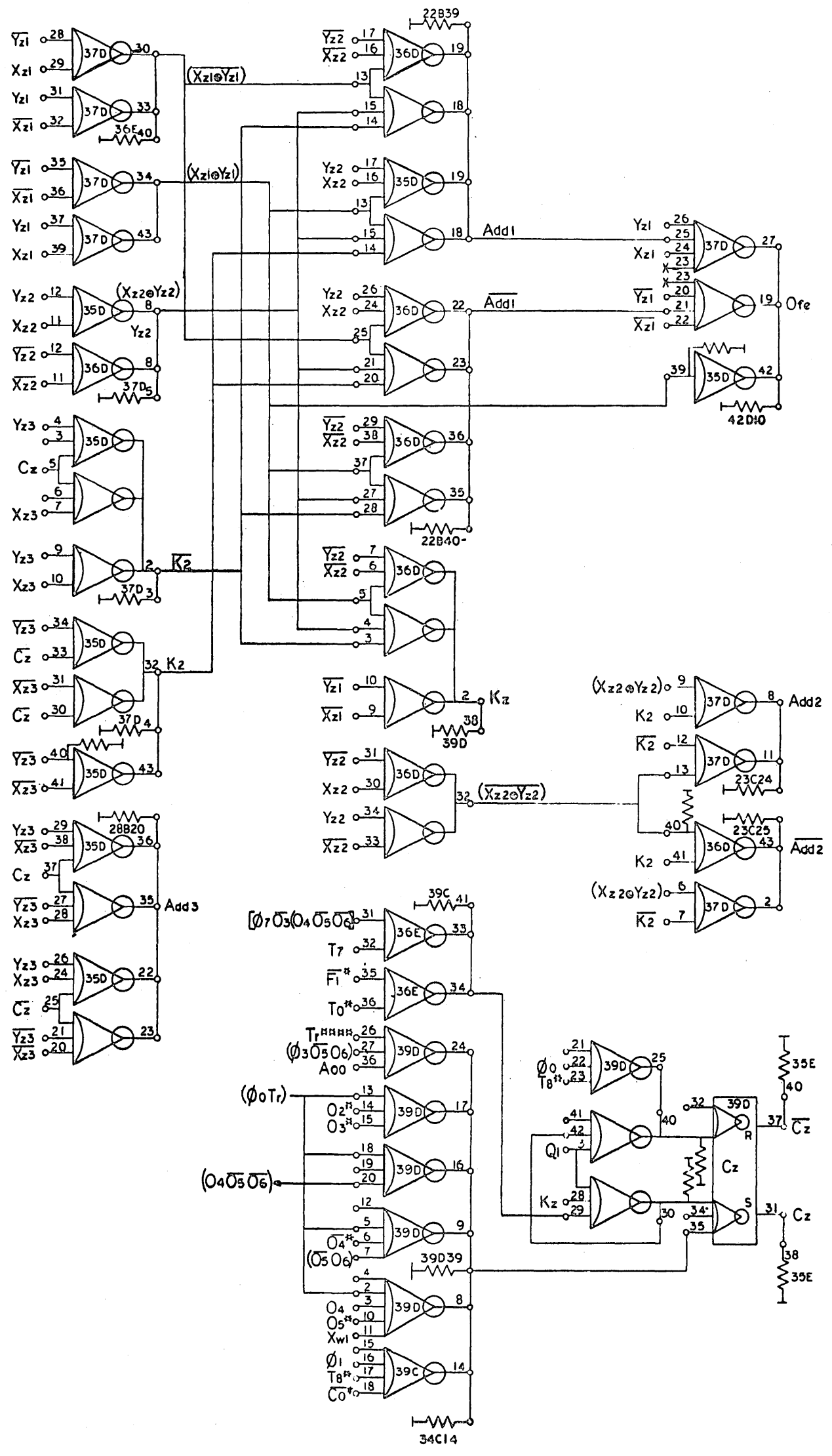
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DIAGRAM, LOGIC COMPUTER		

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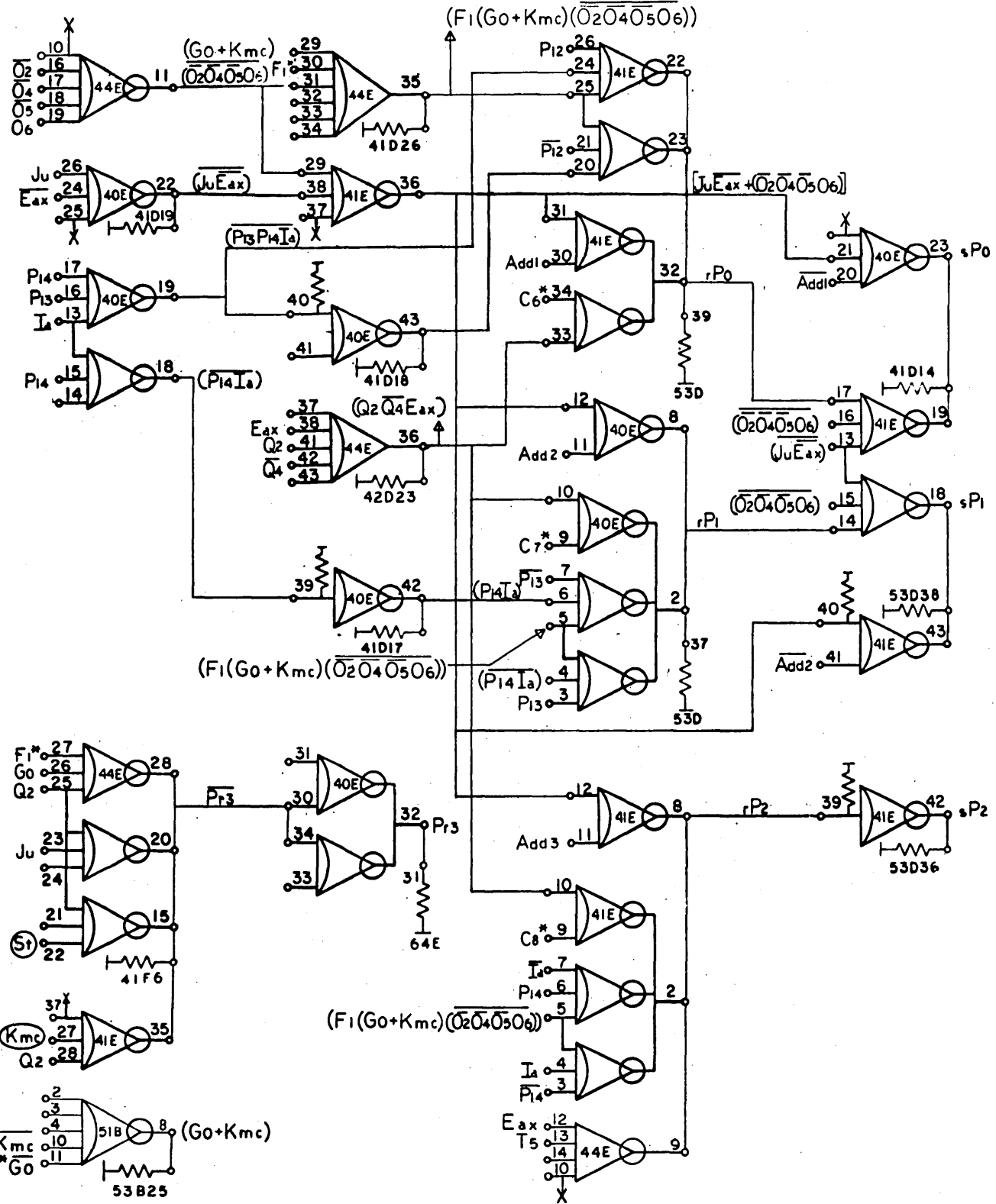
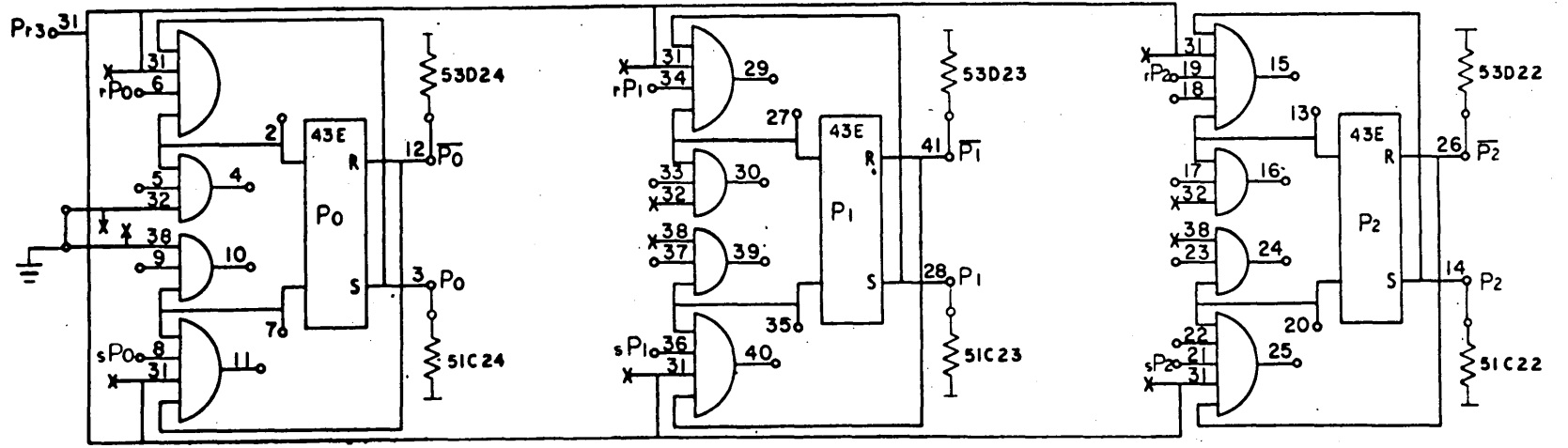
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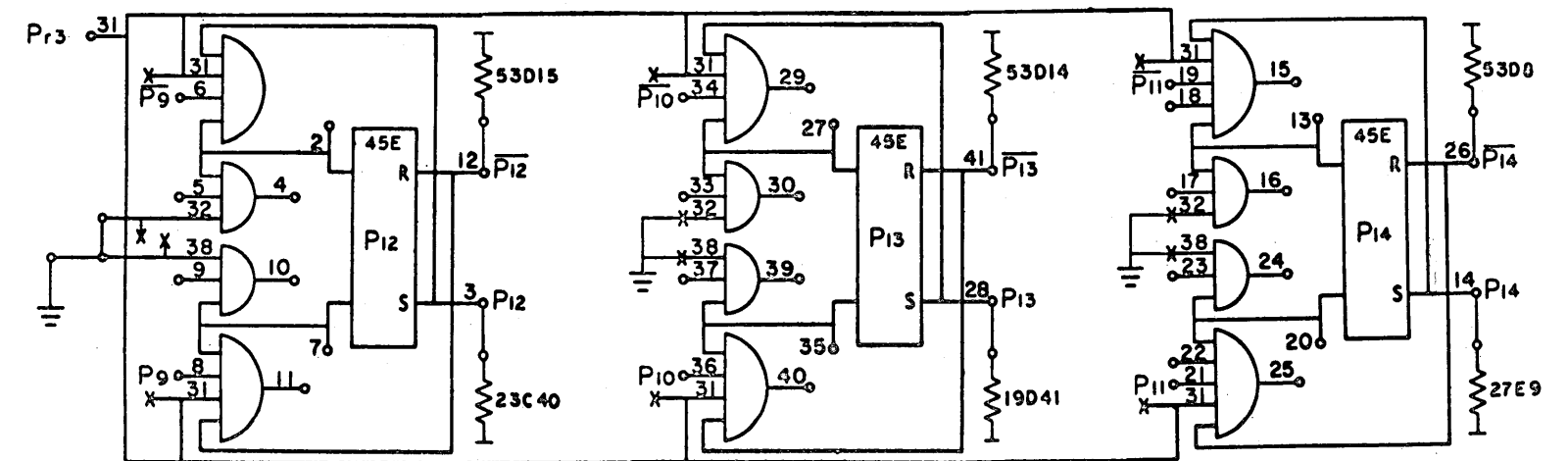
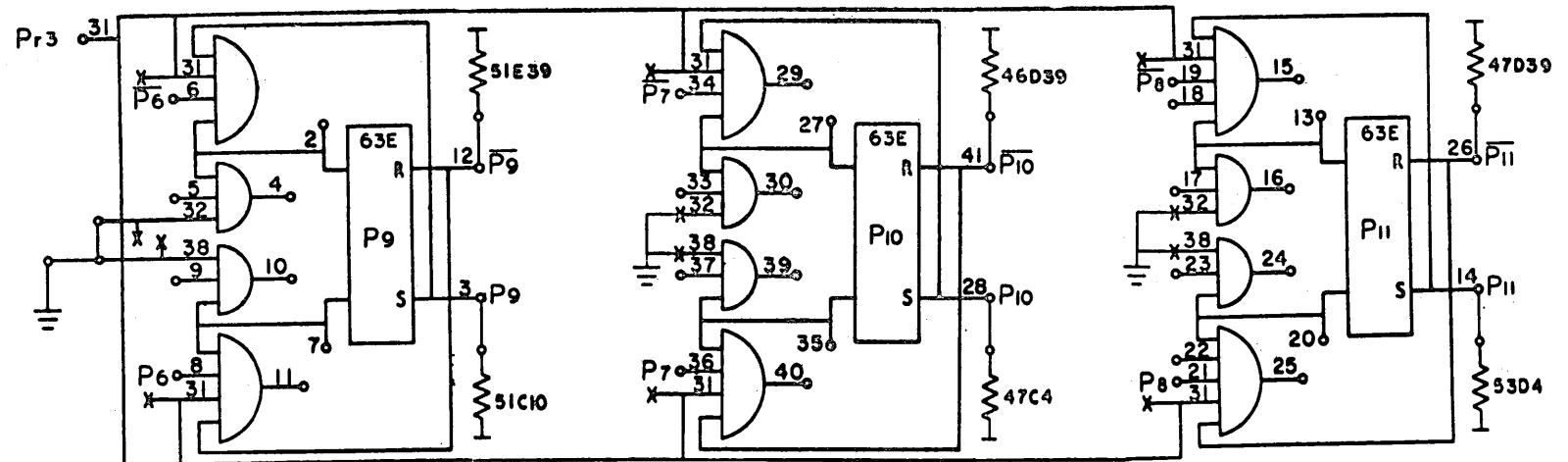
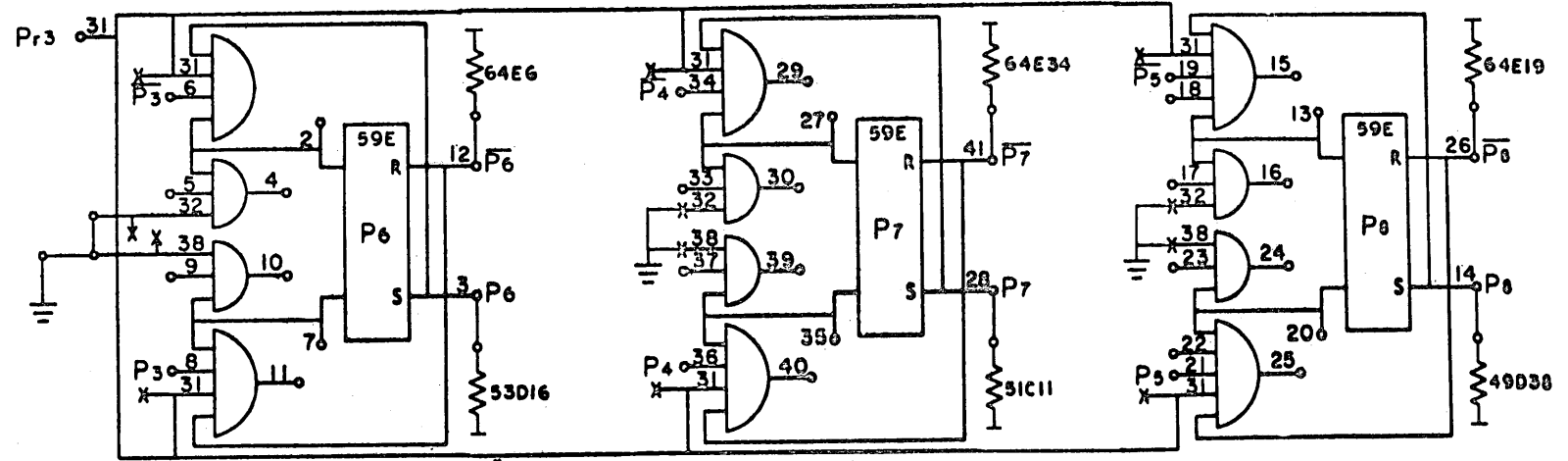
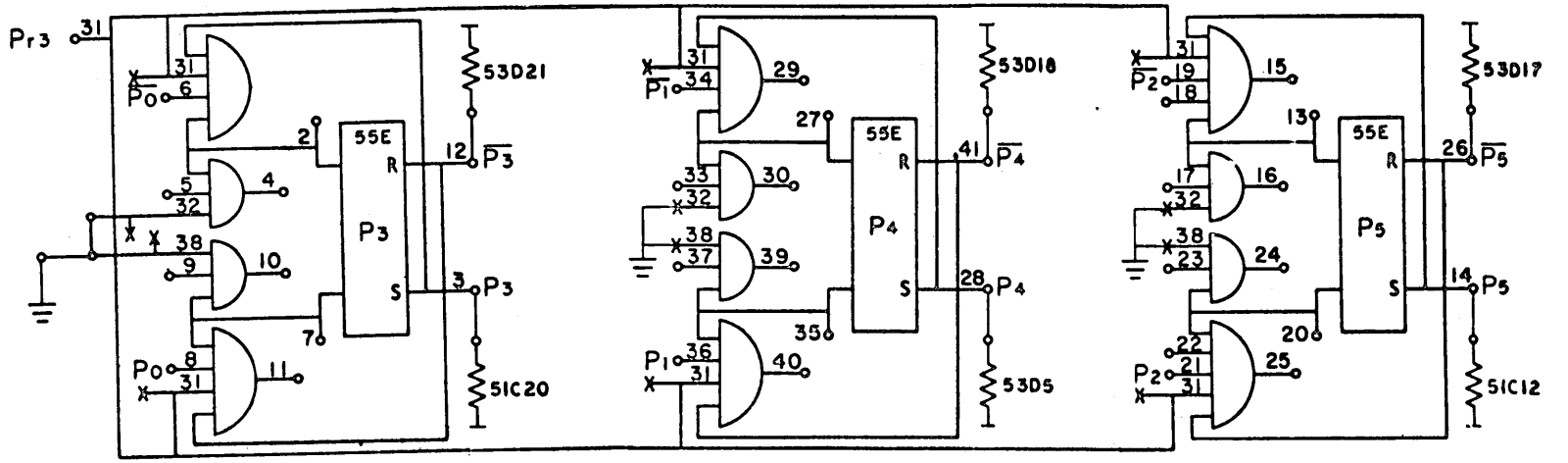


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PAGE 54
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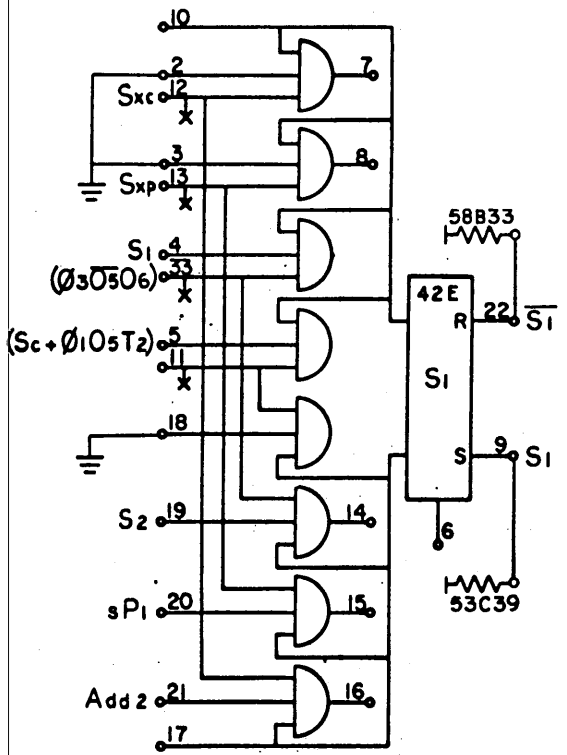
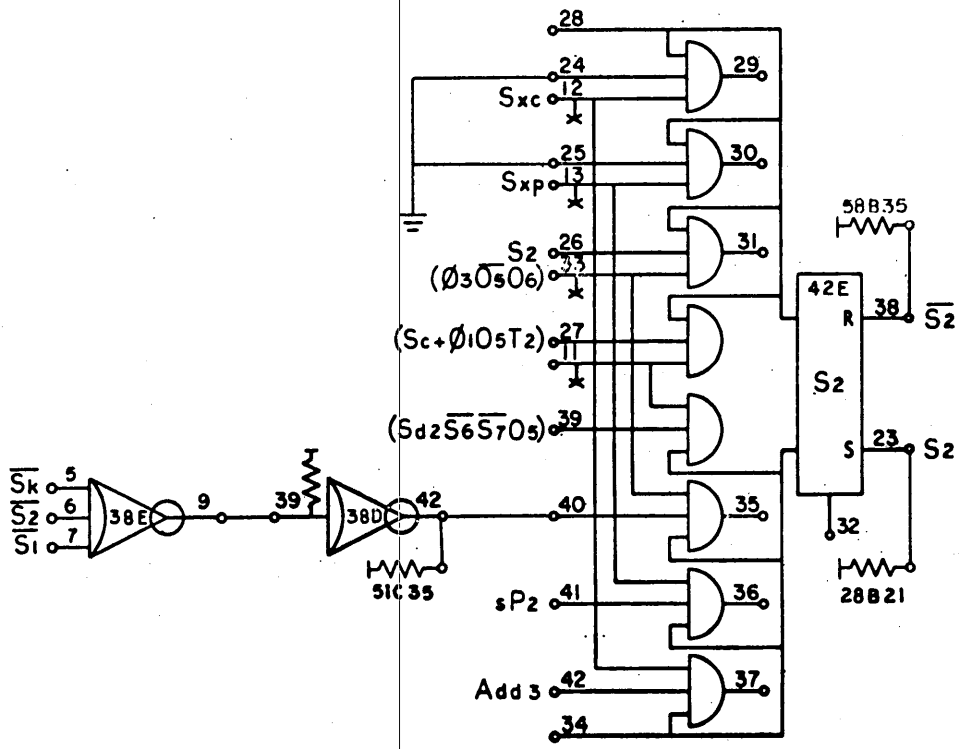
DIAGRAM, LOGIC COMPUTER

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DIAGRAM, LOGIC COMPUTER		
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PAGE 56
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SCANNING DATA SYSTEM
SERIALS, REPRODUCTION, STORAGE

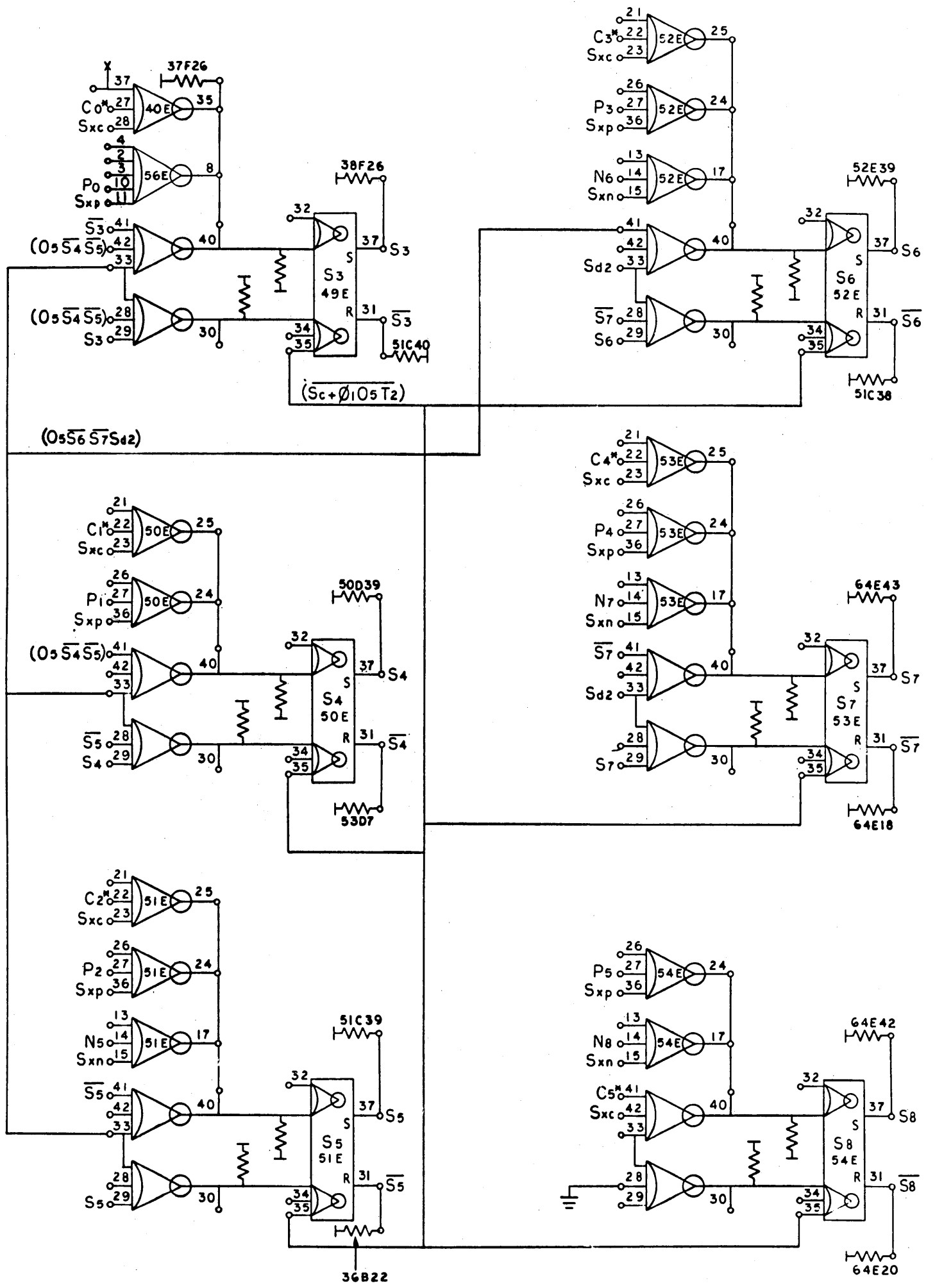
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COMPUTER

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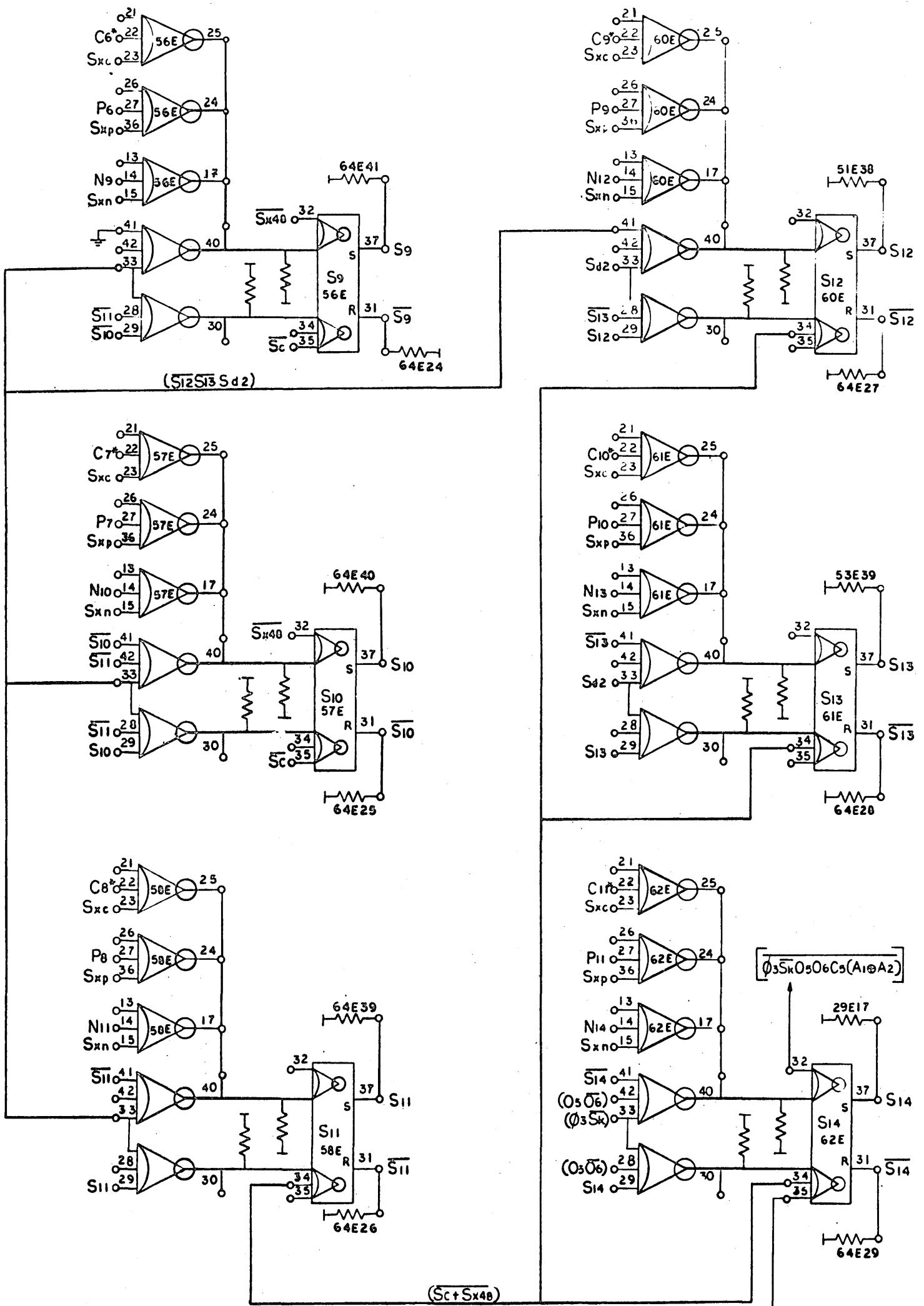
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PAGE 57
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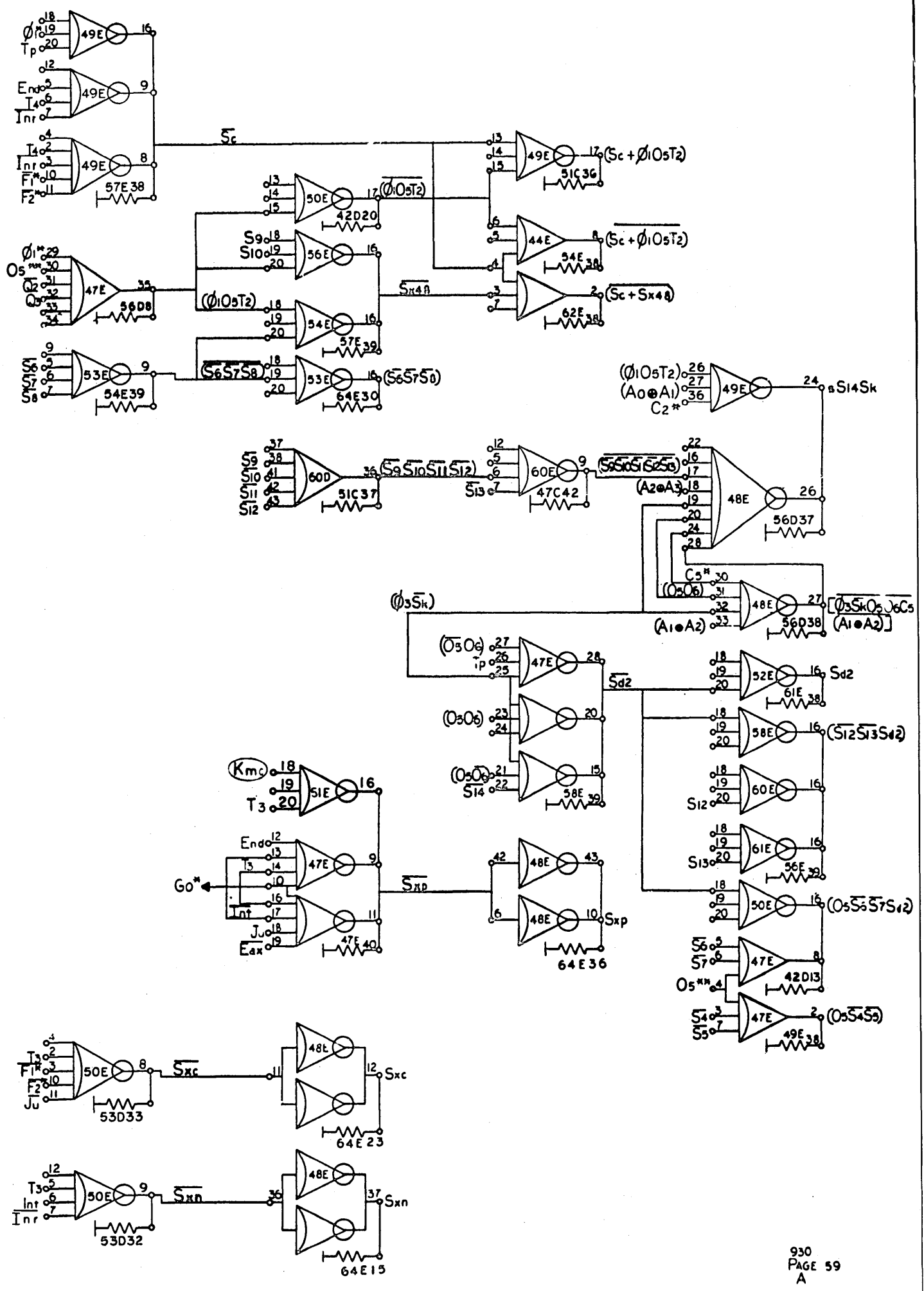
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PAGE 58
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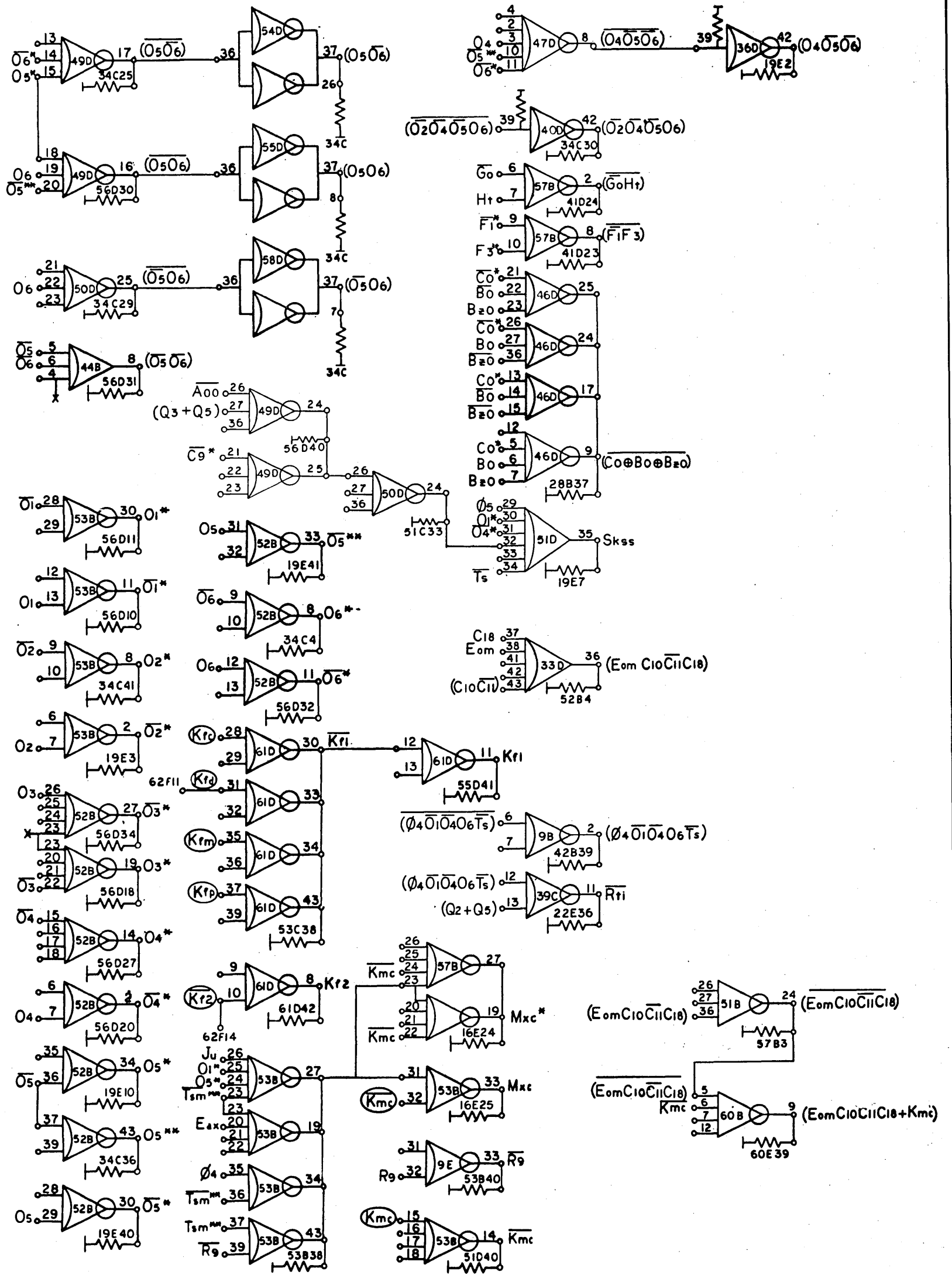
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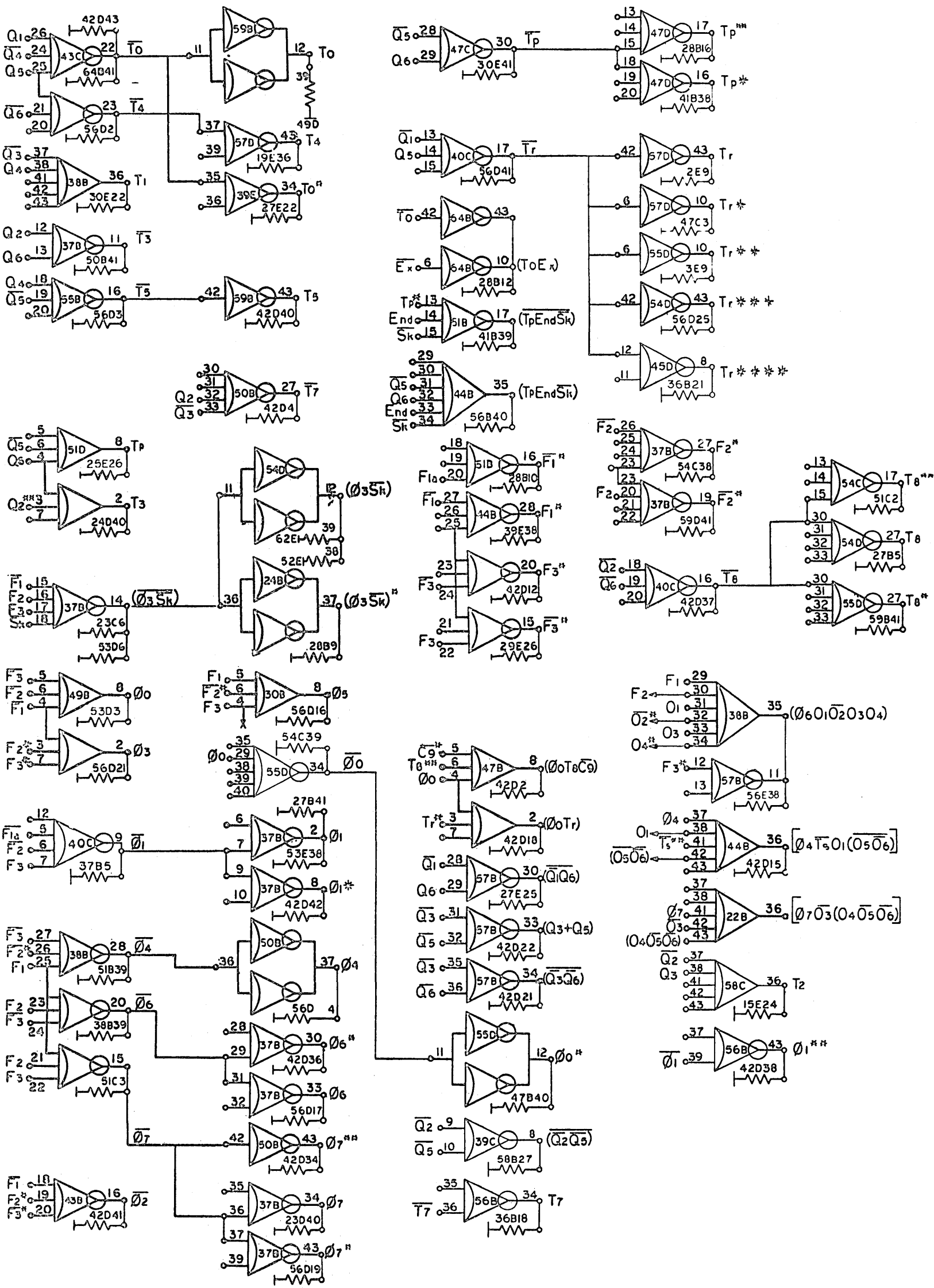


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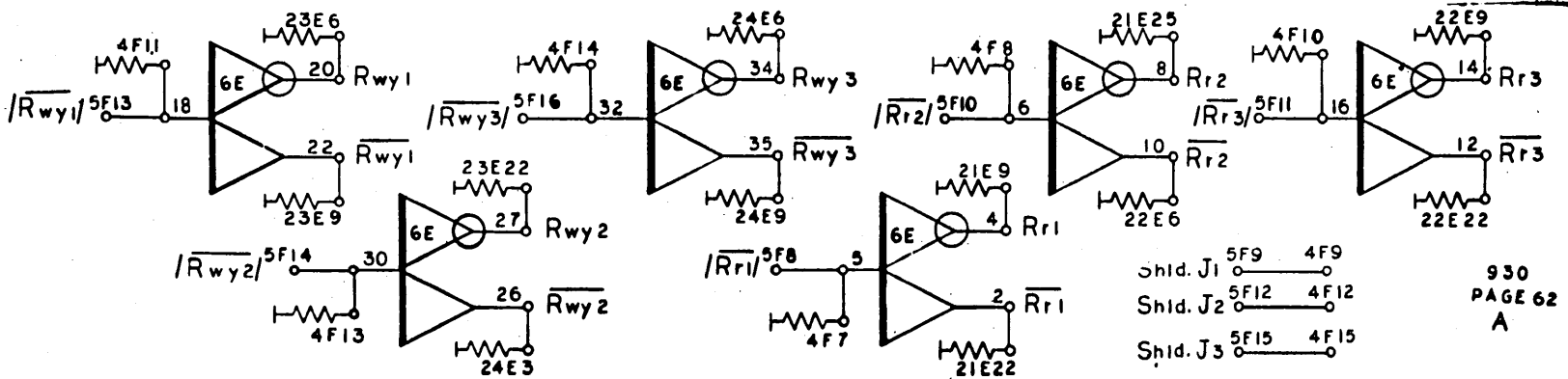
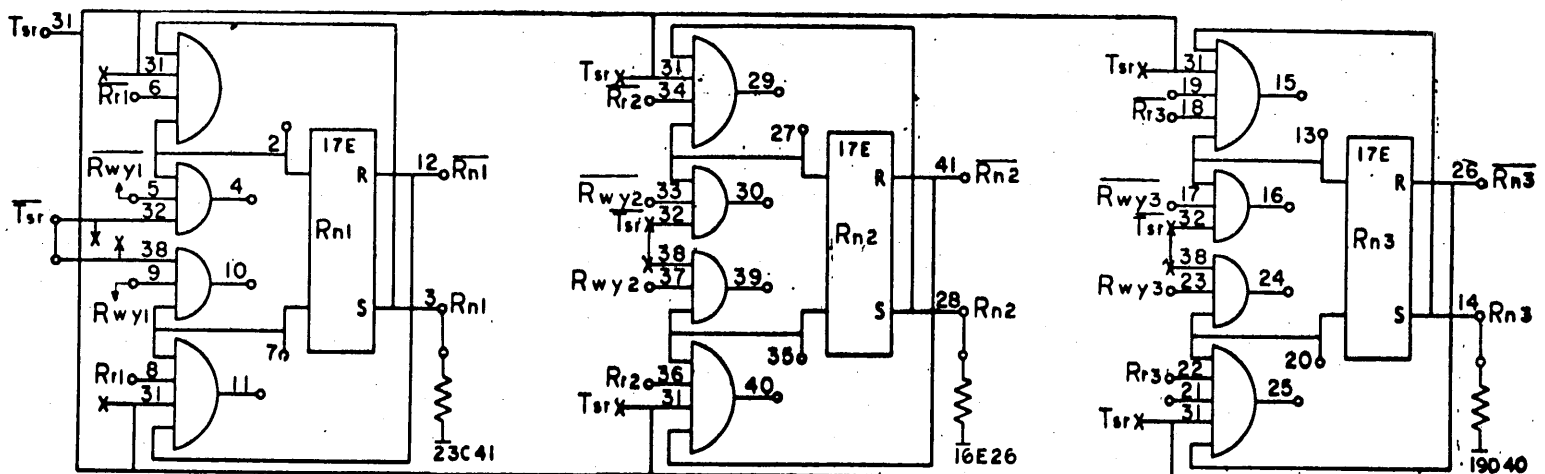
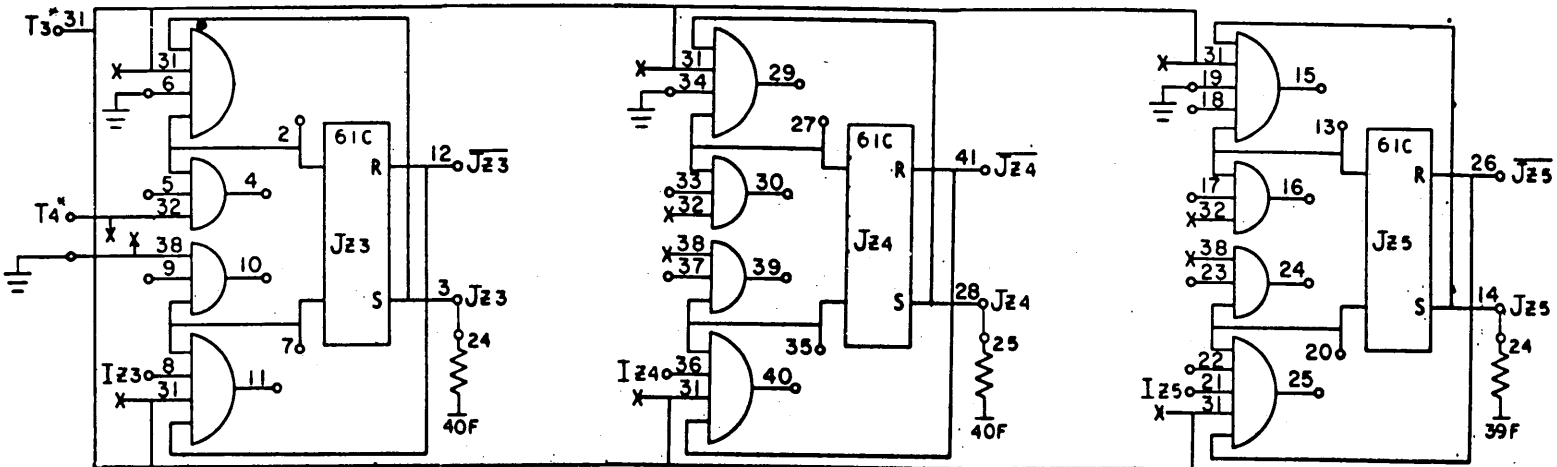
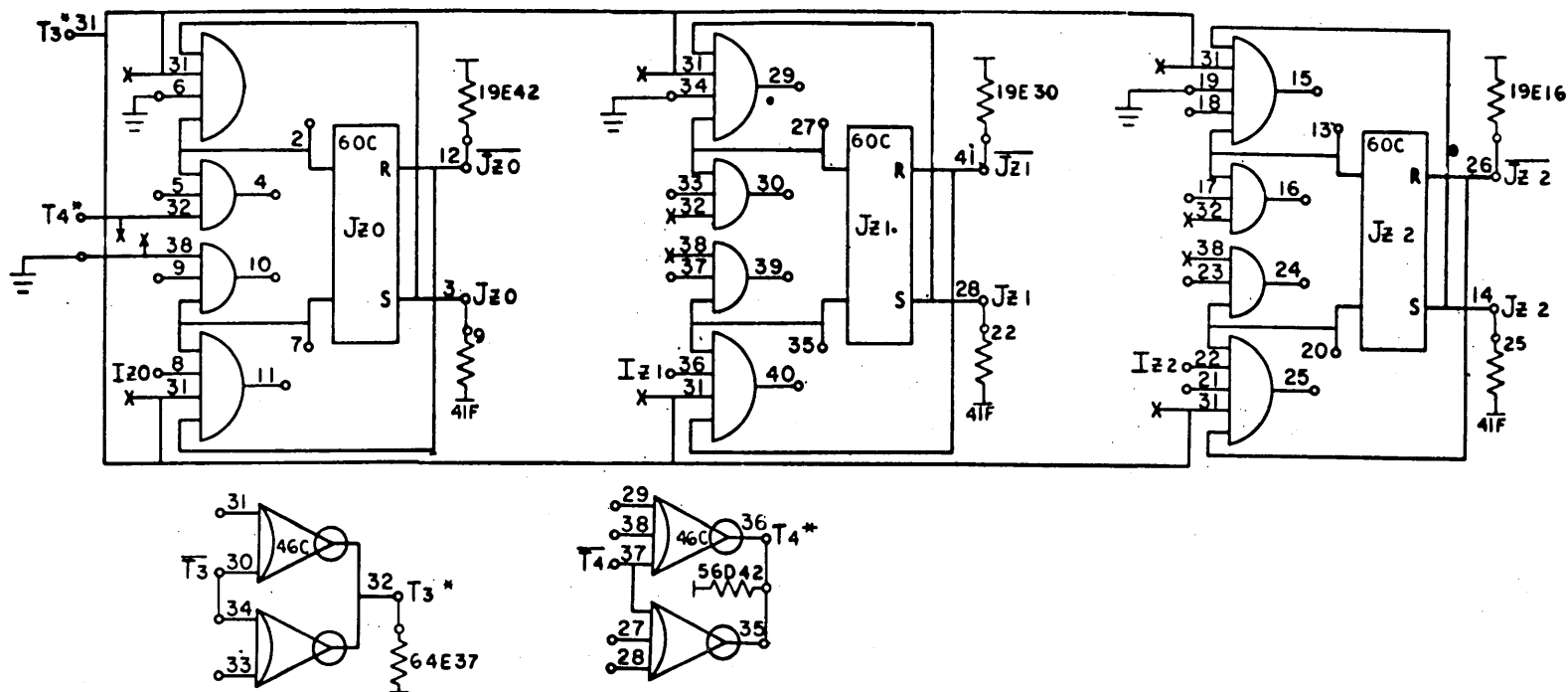
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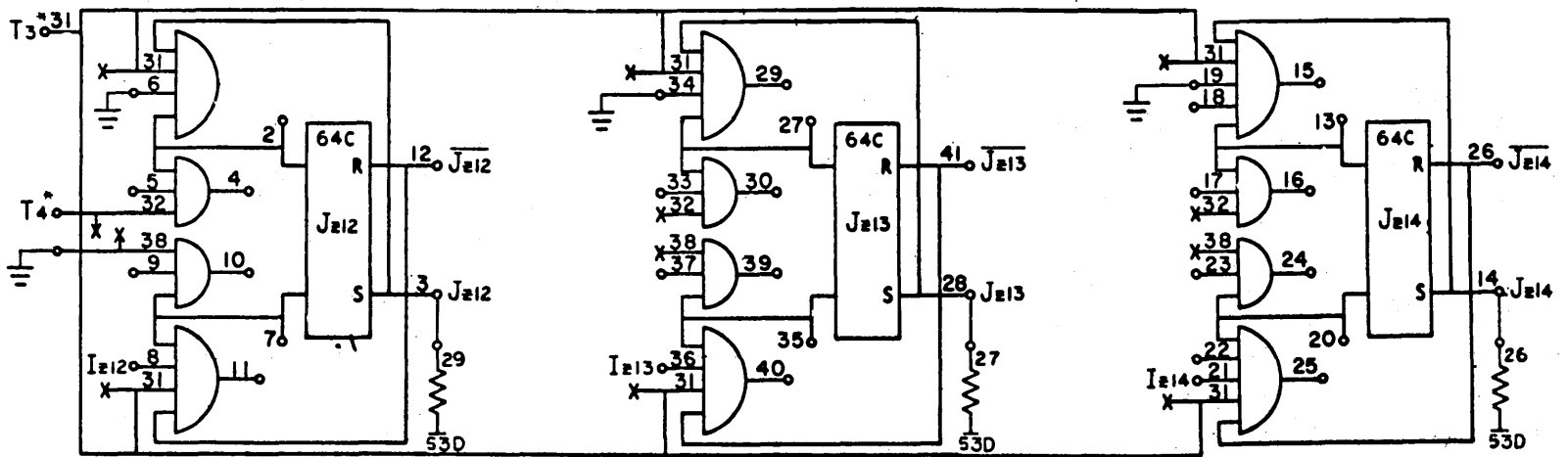
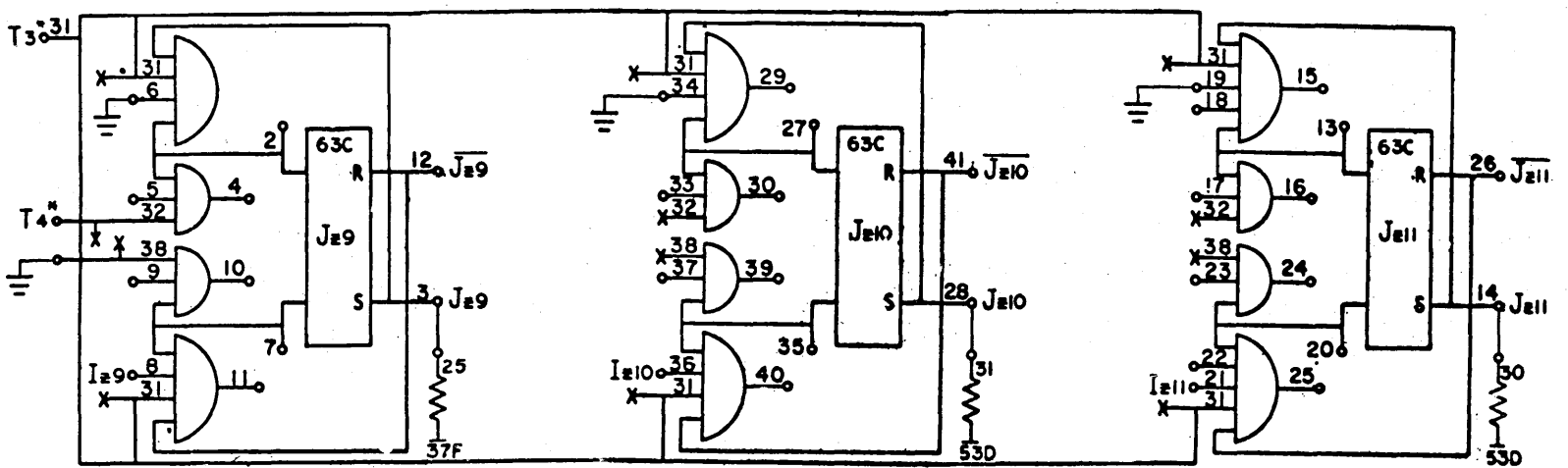
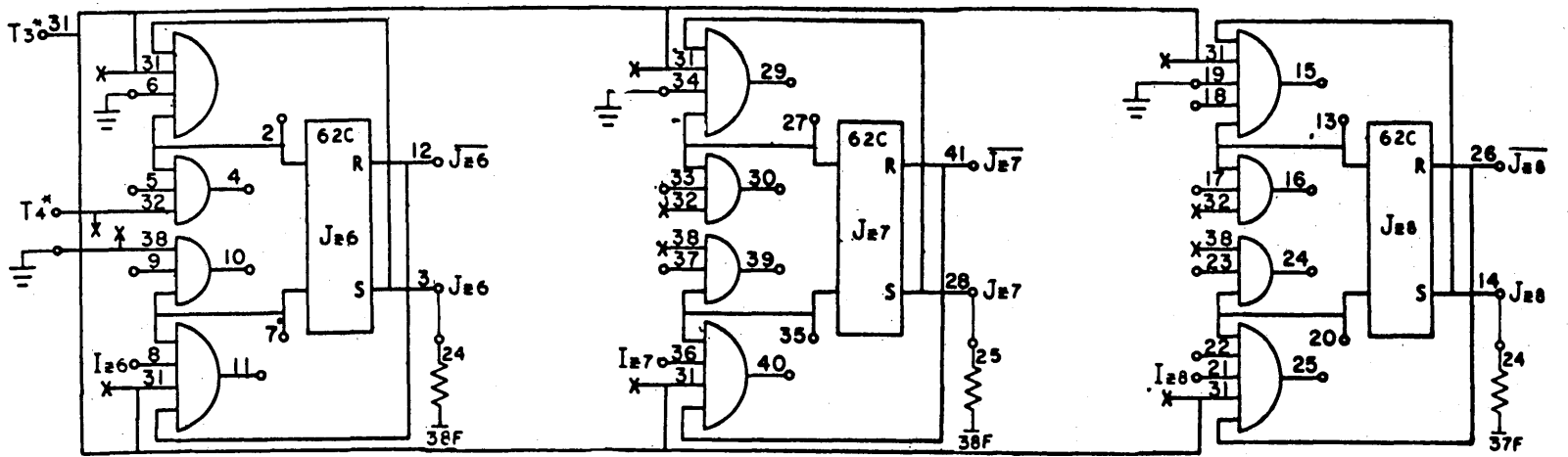
106407/A



930
PAGE 62
A

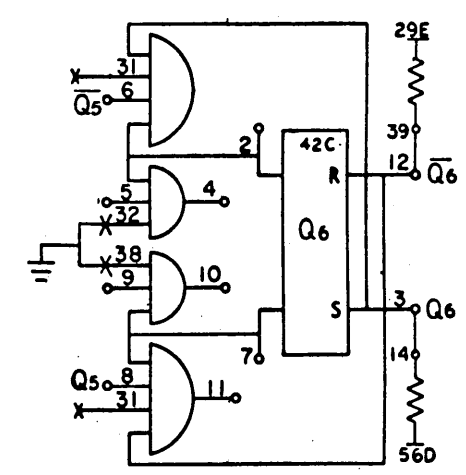
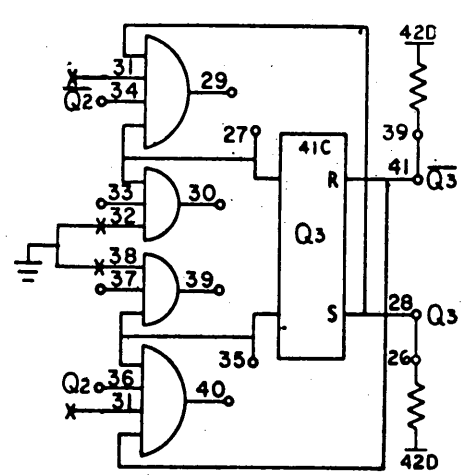
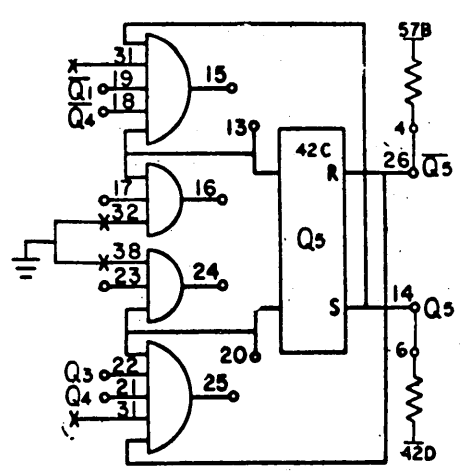
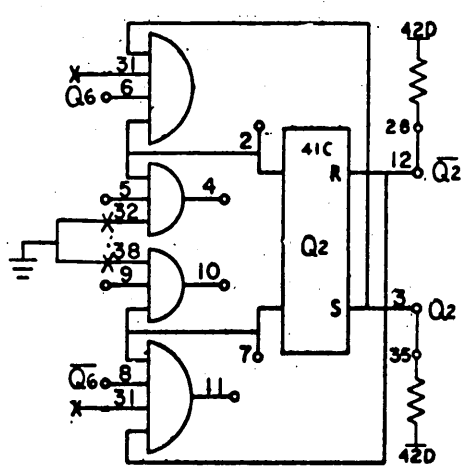
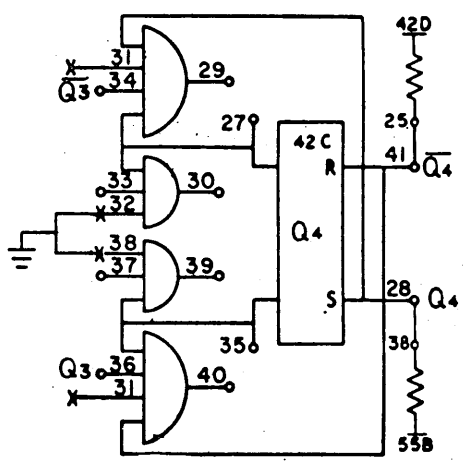
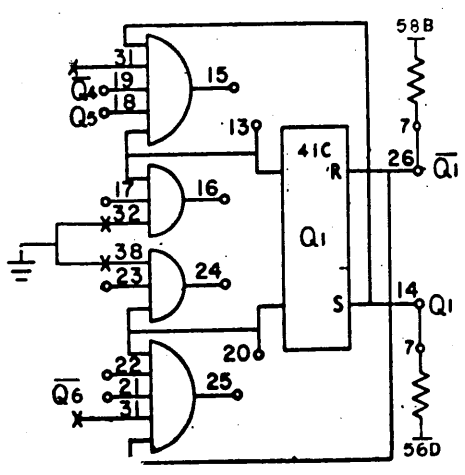
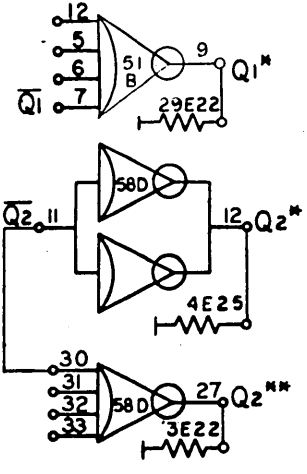
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106407/A



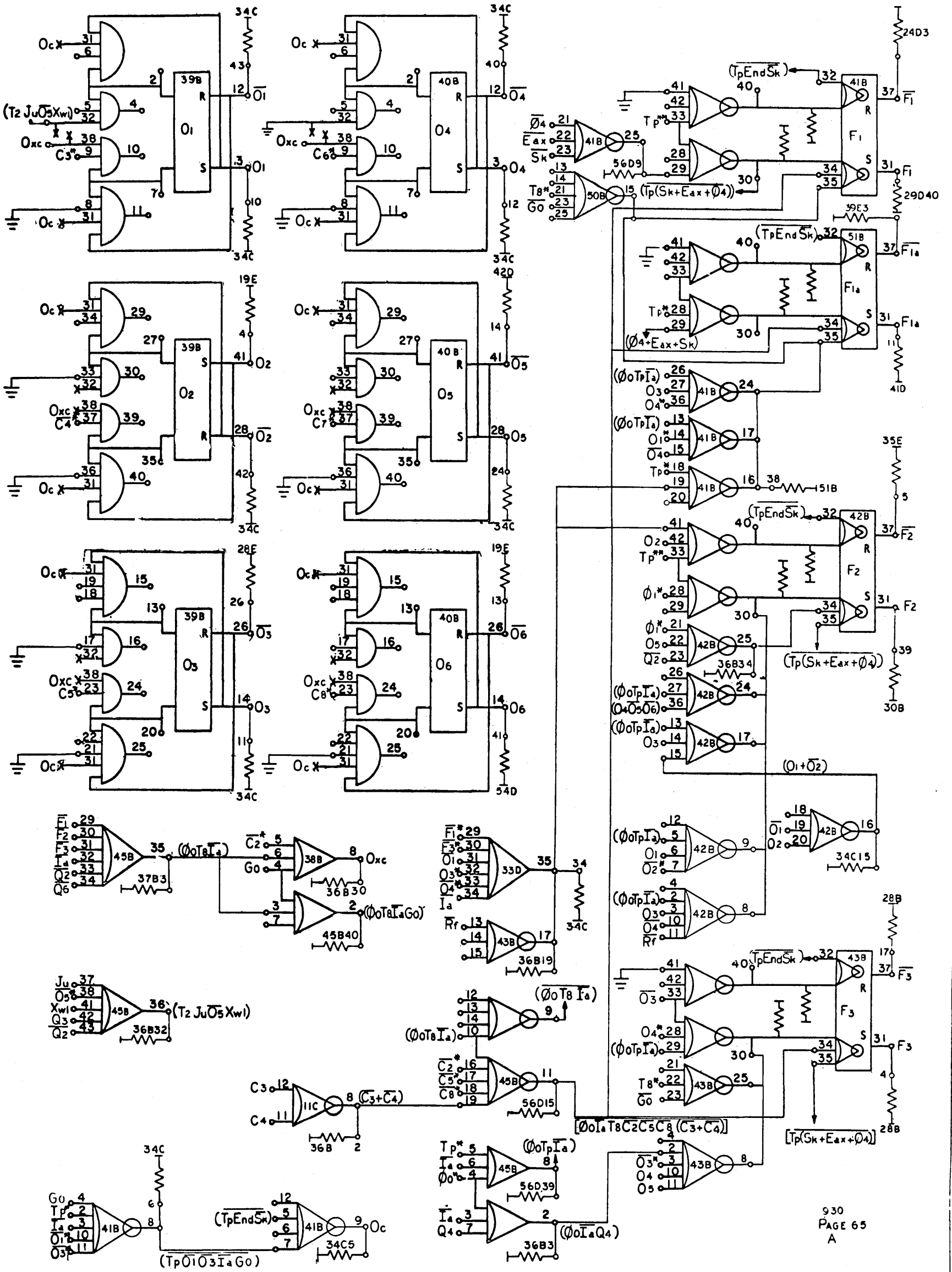
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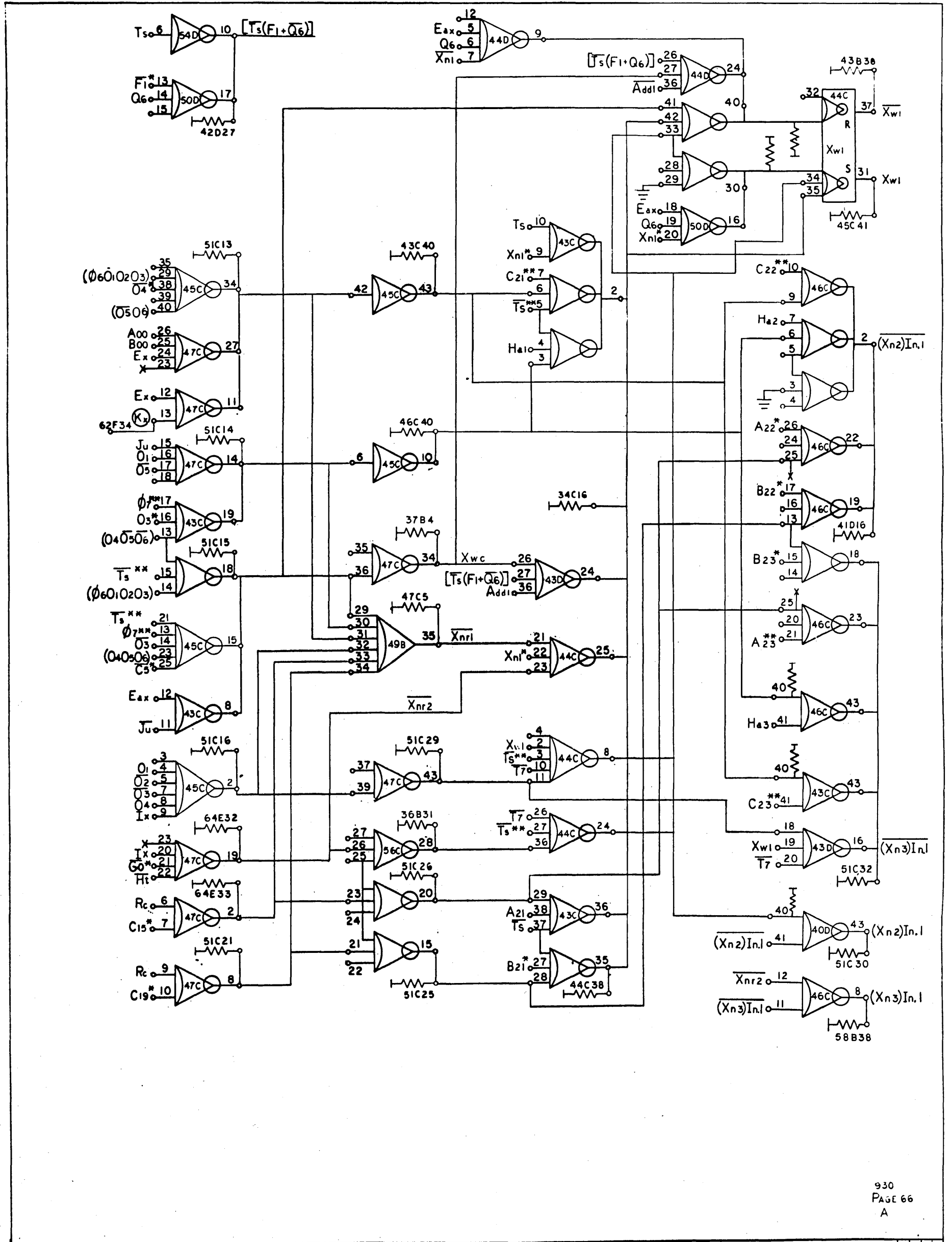
106407/A



930
PAGE 65
A

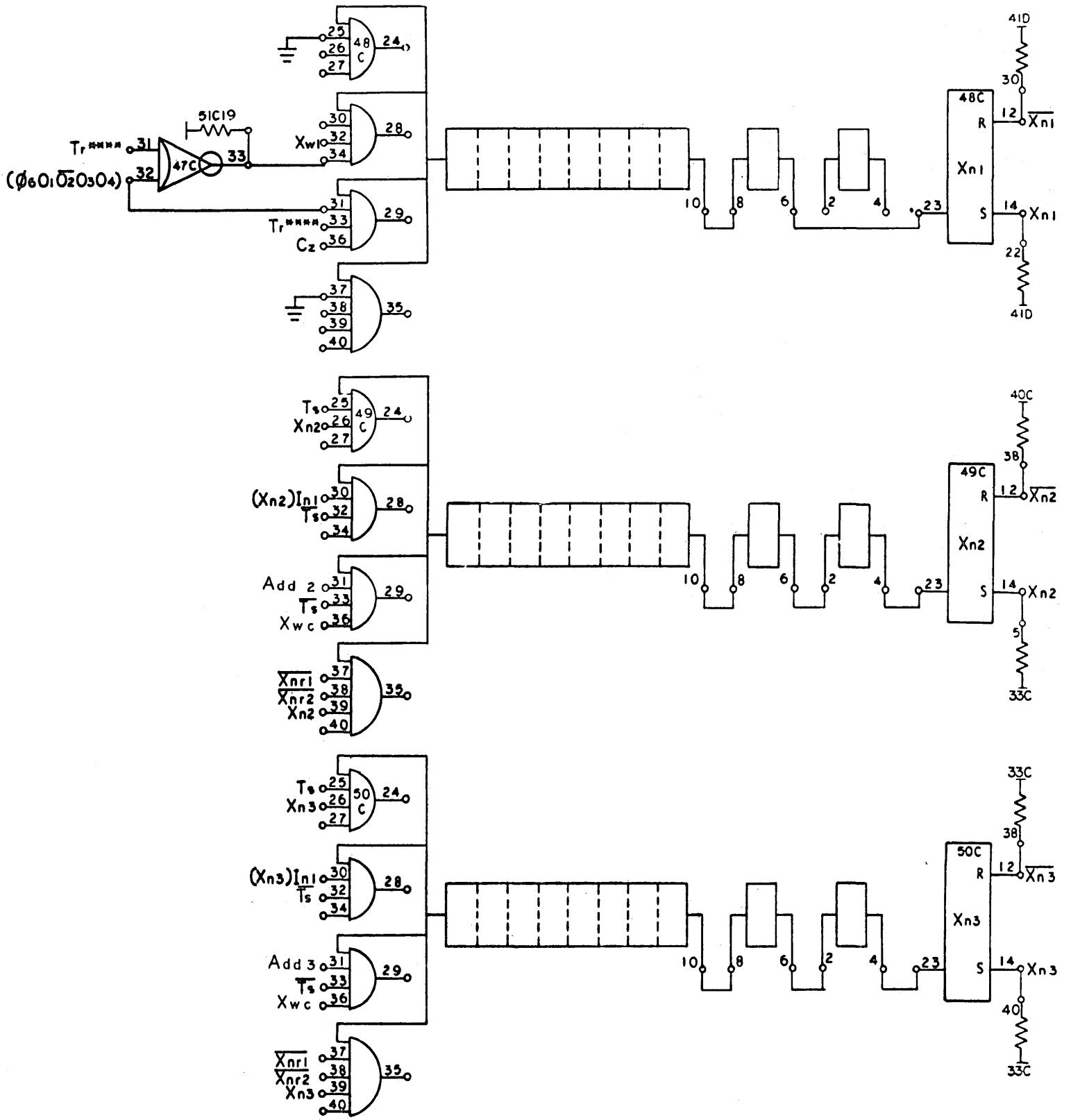
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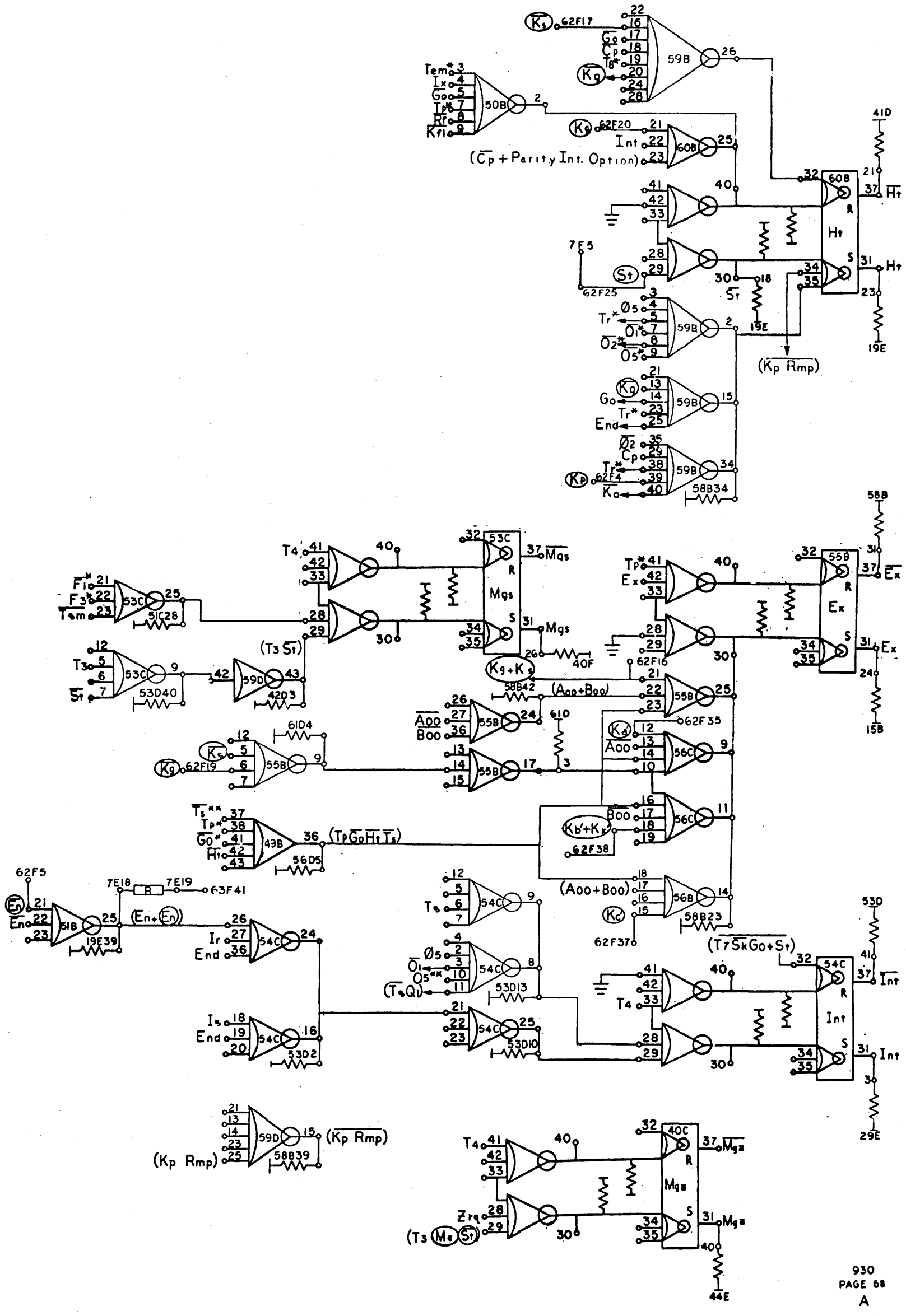


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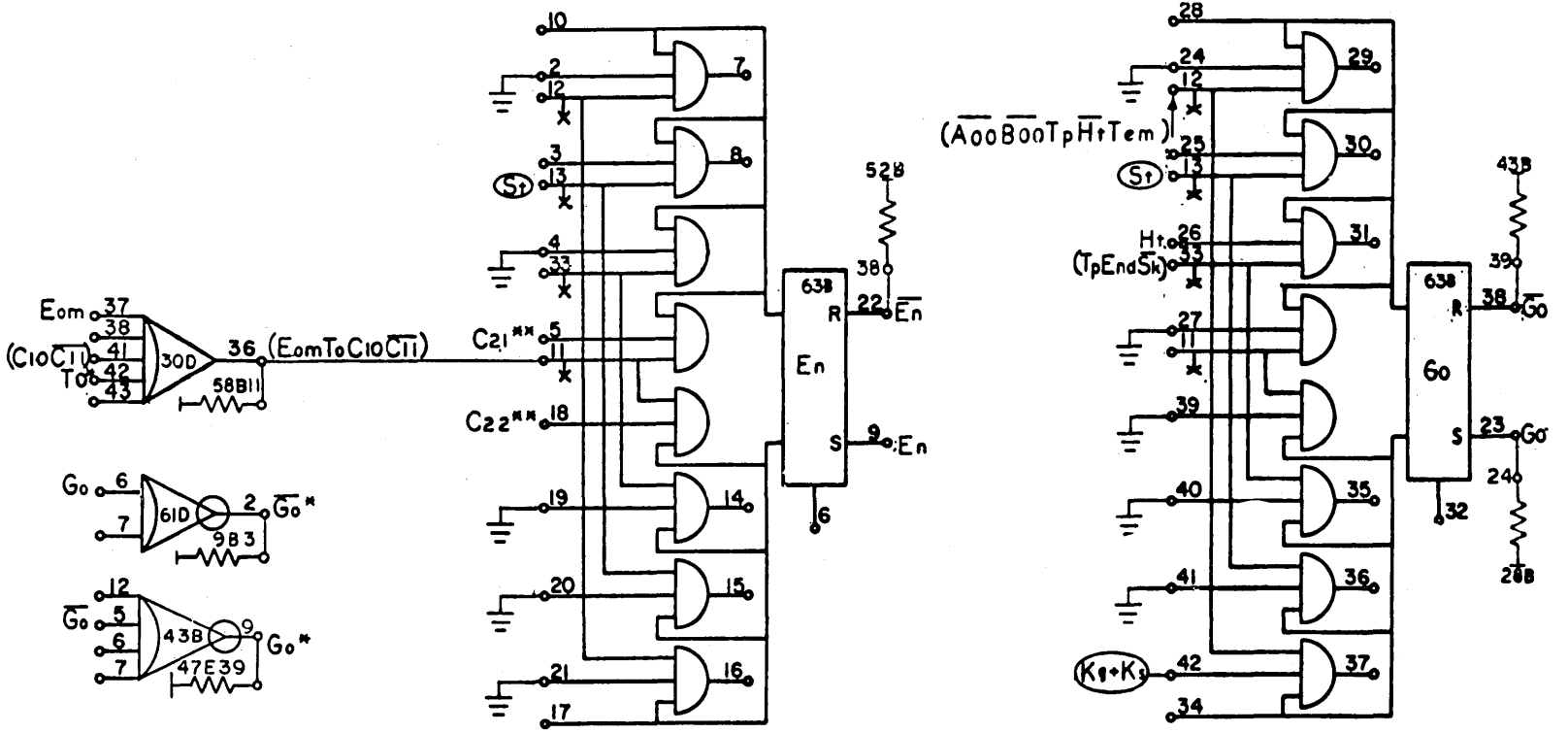
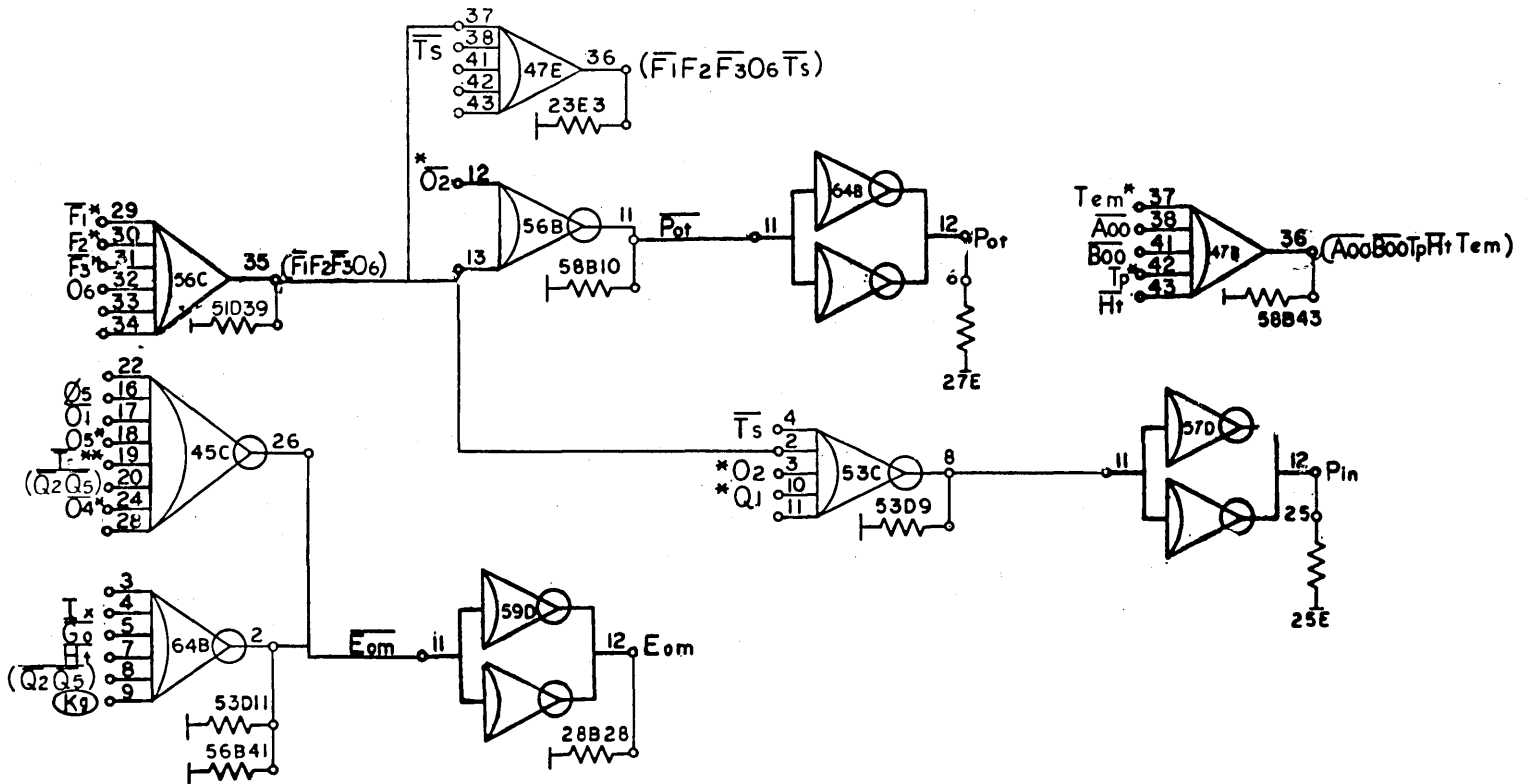
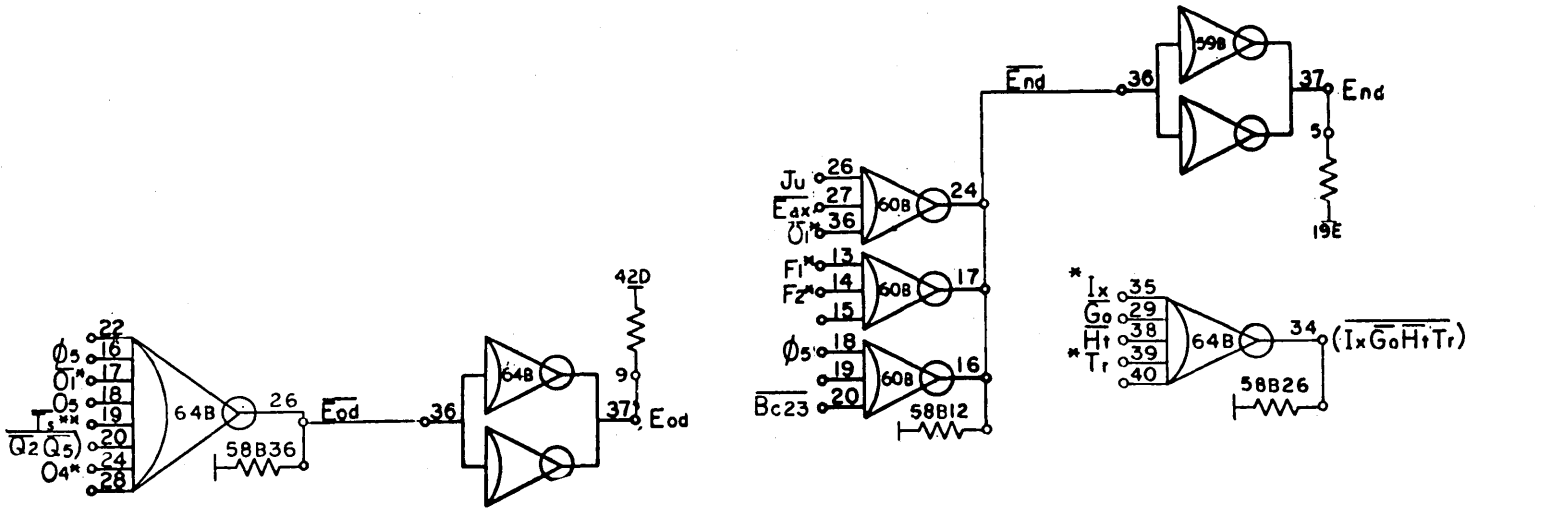


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PAGE 68
A

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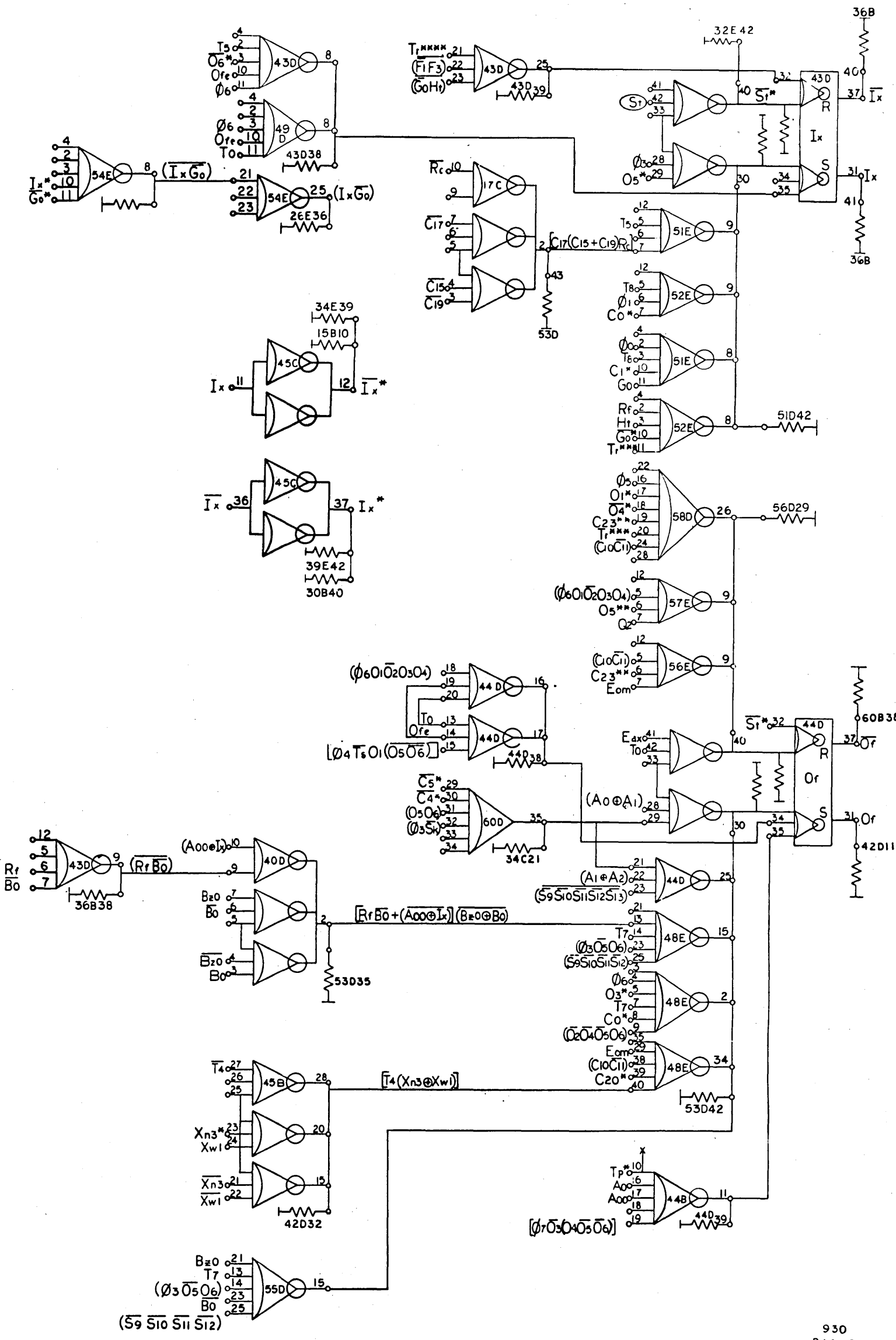
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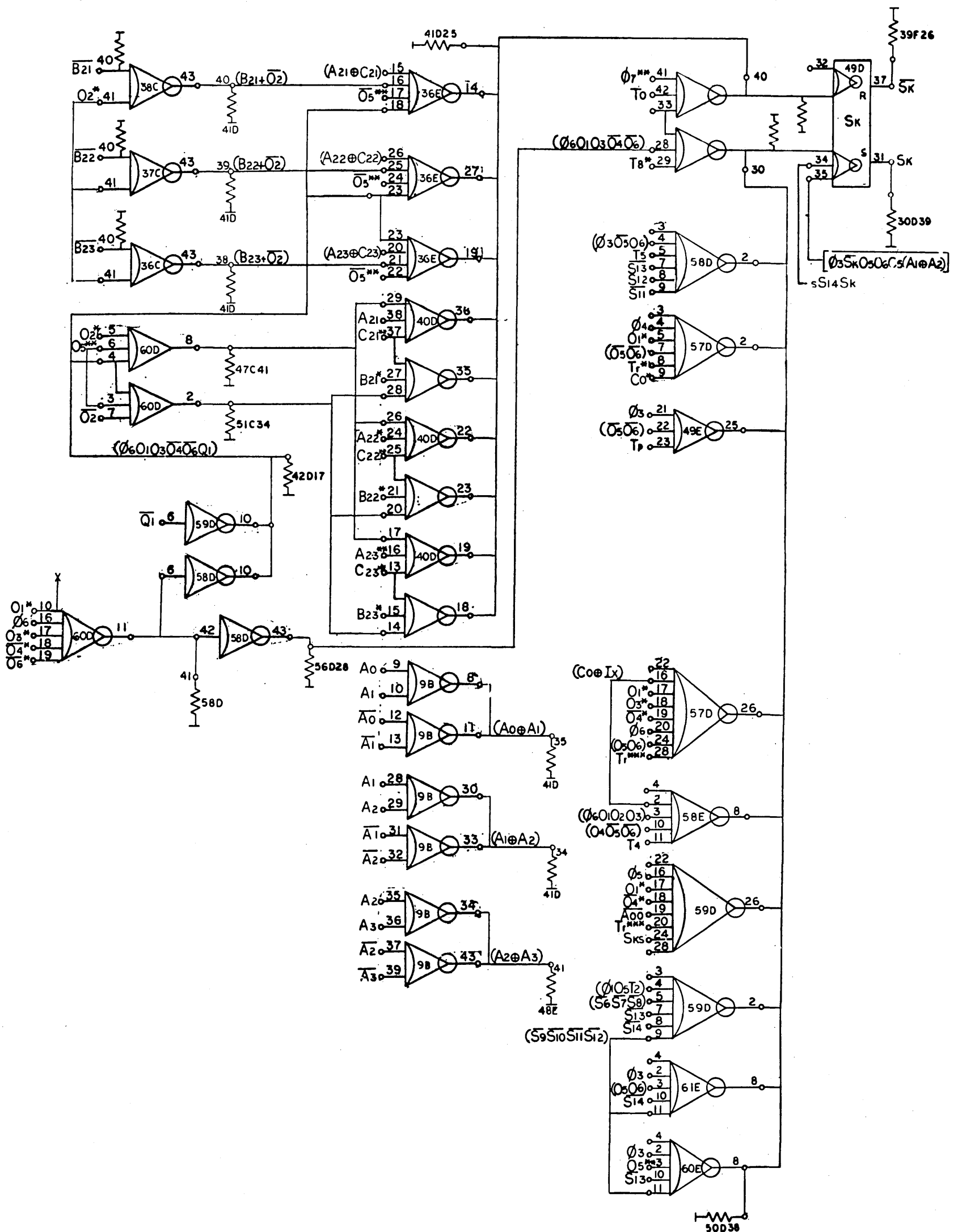
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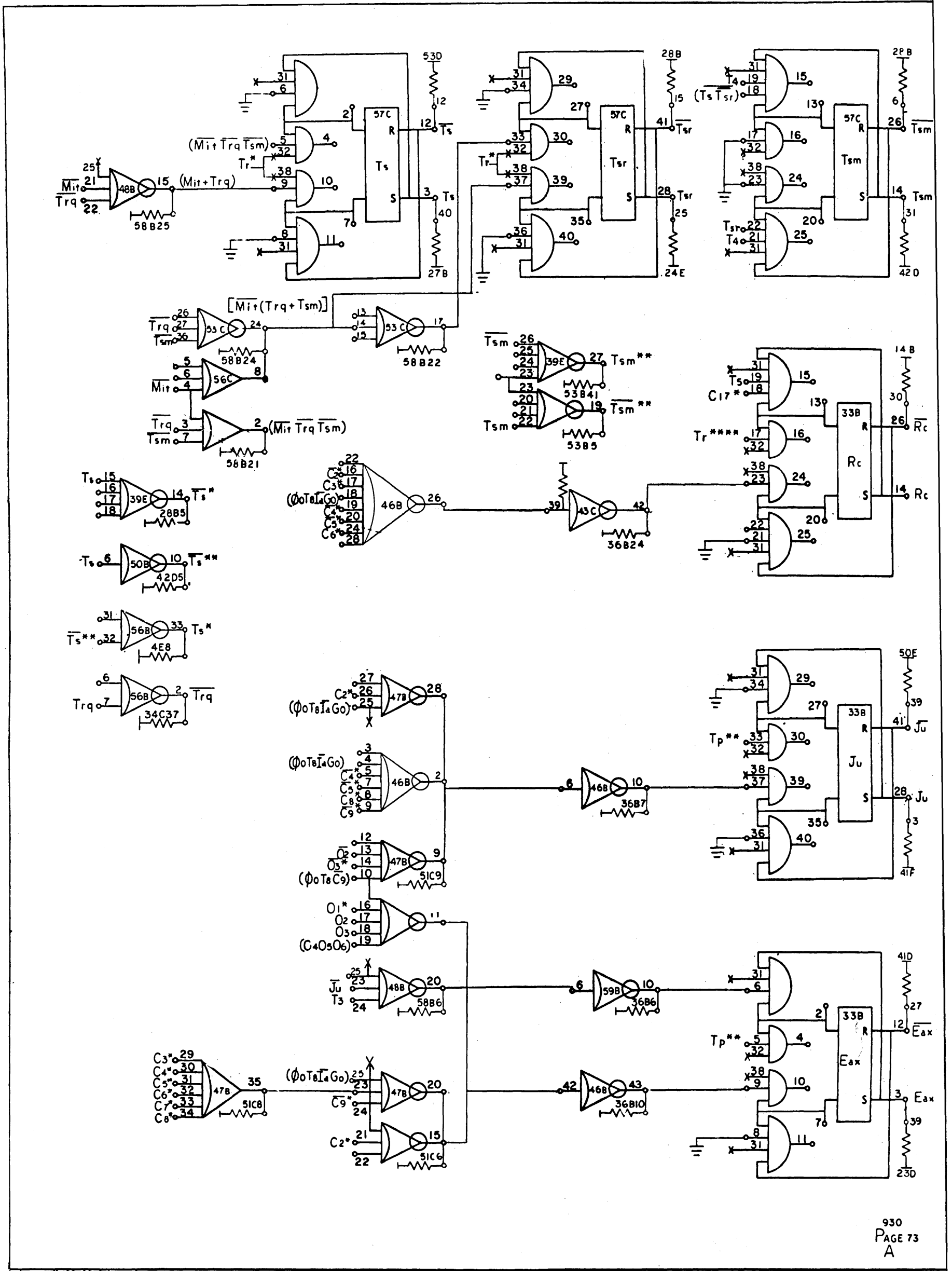
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930
PAGE 72
A

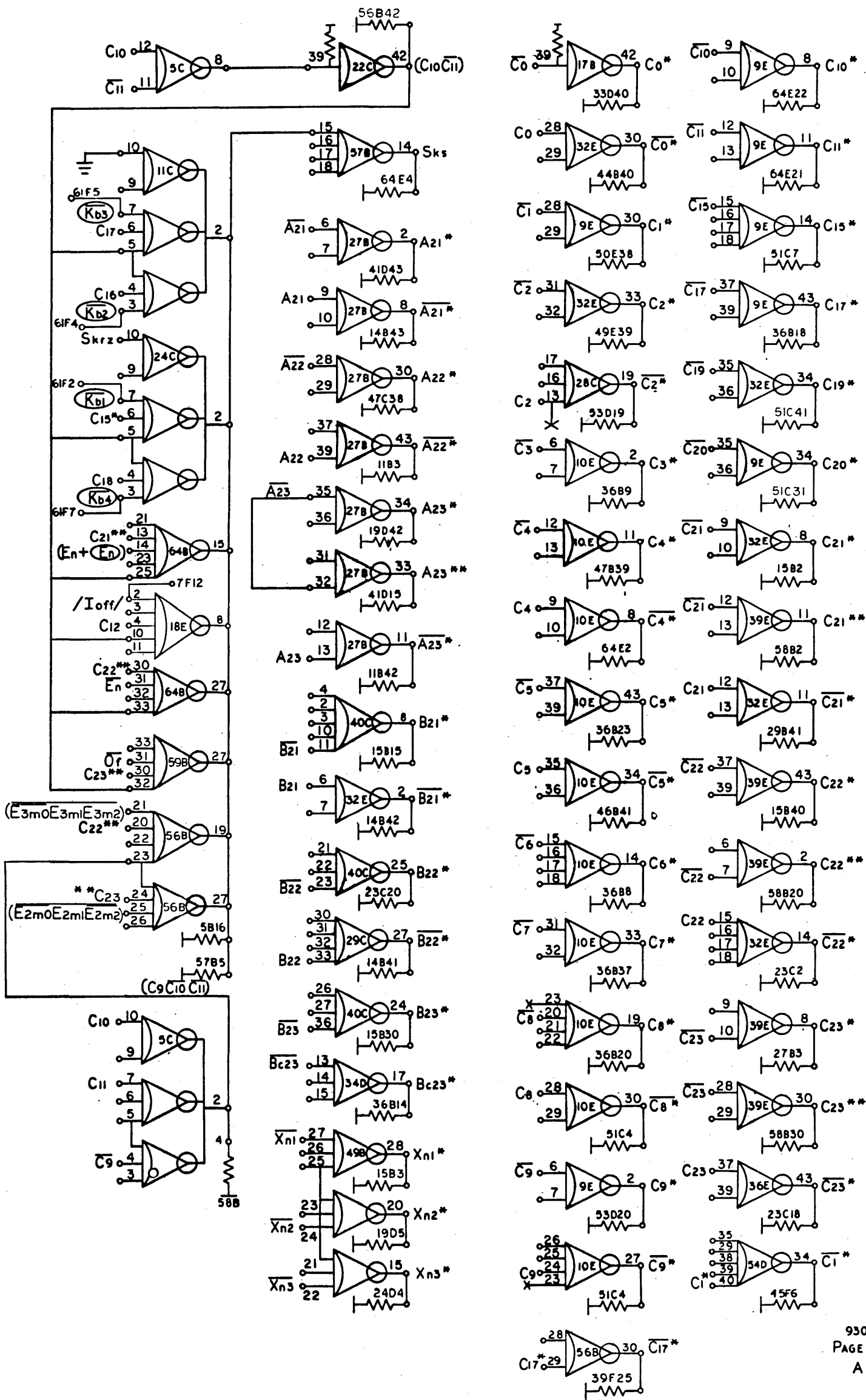
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930
PAGE 74
A

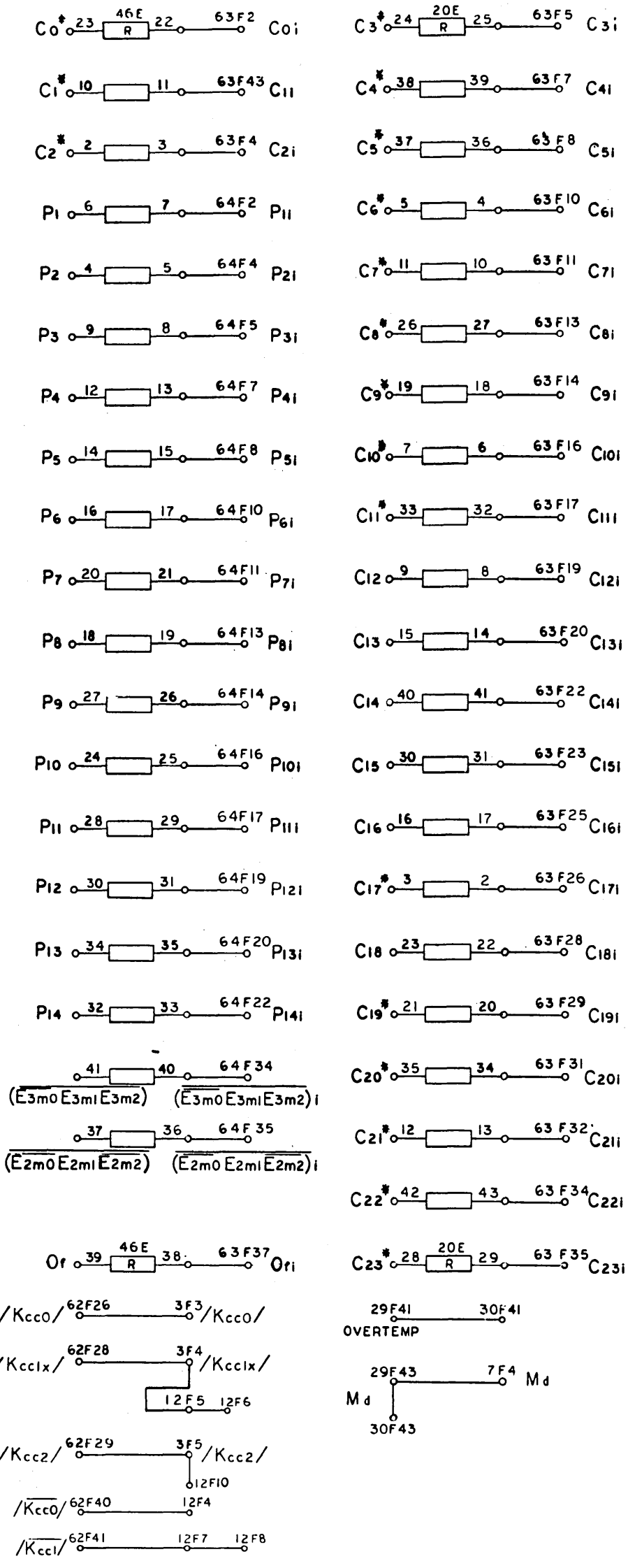
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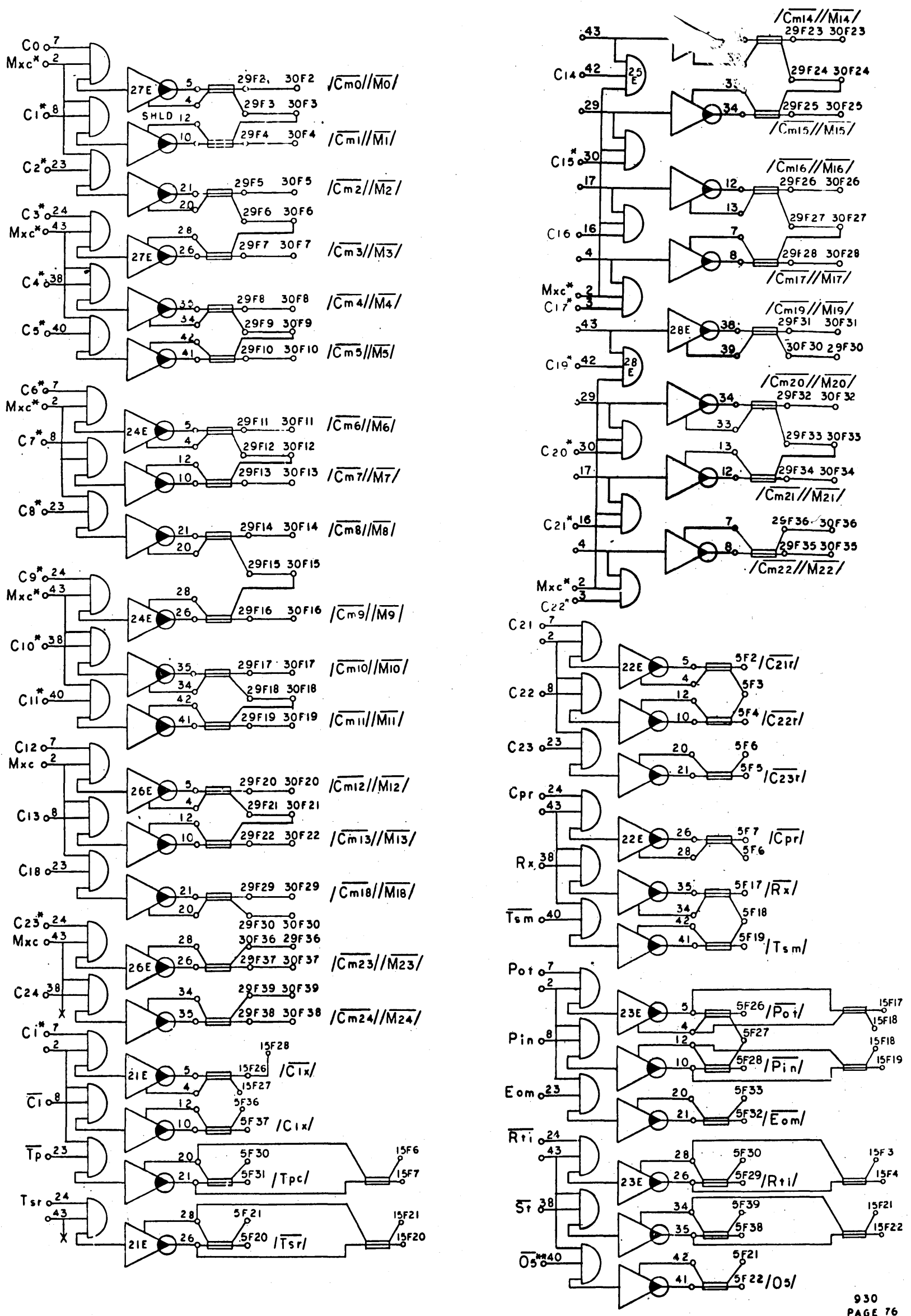
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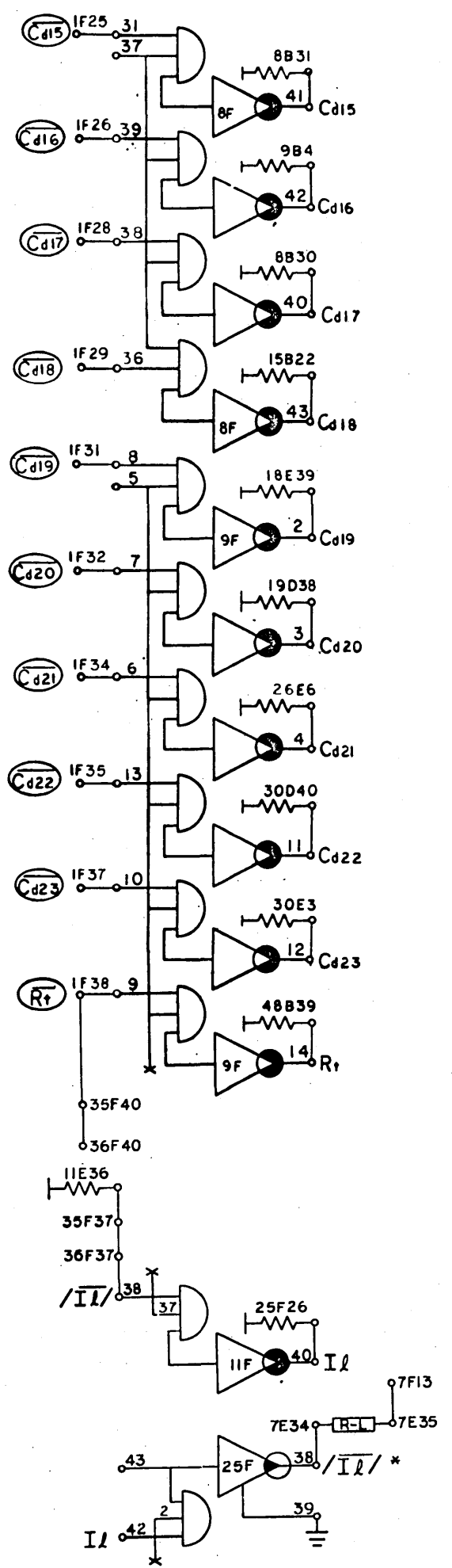
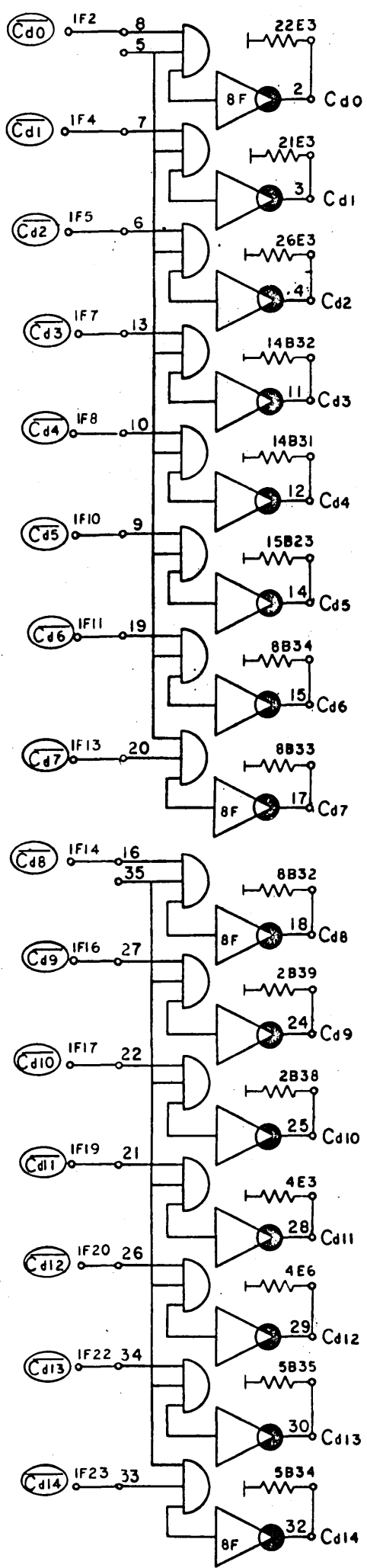
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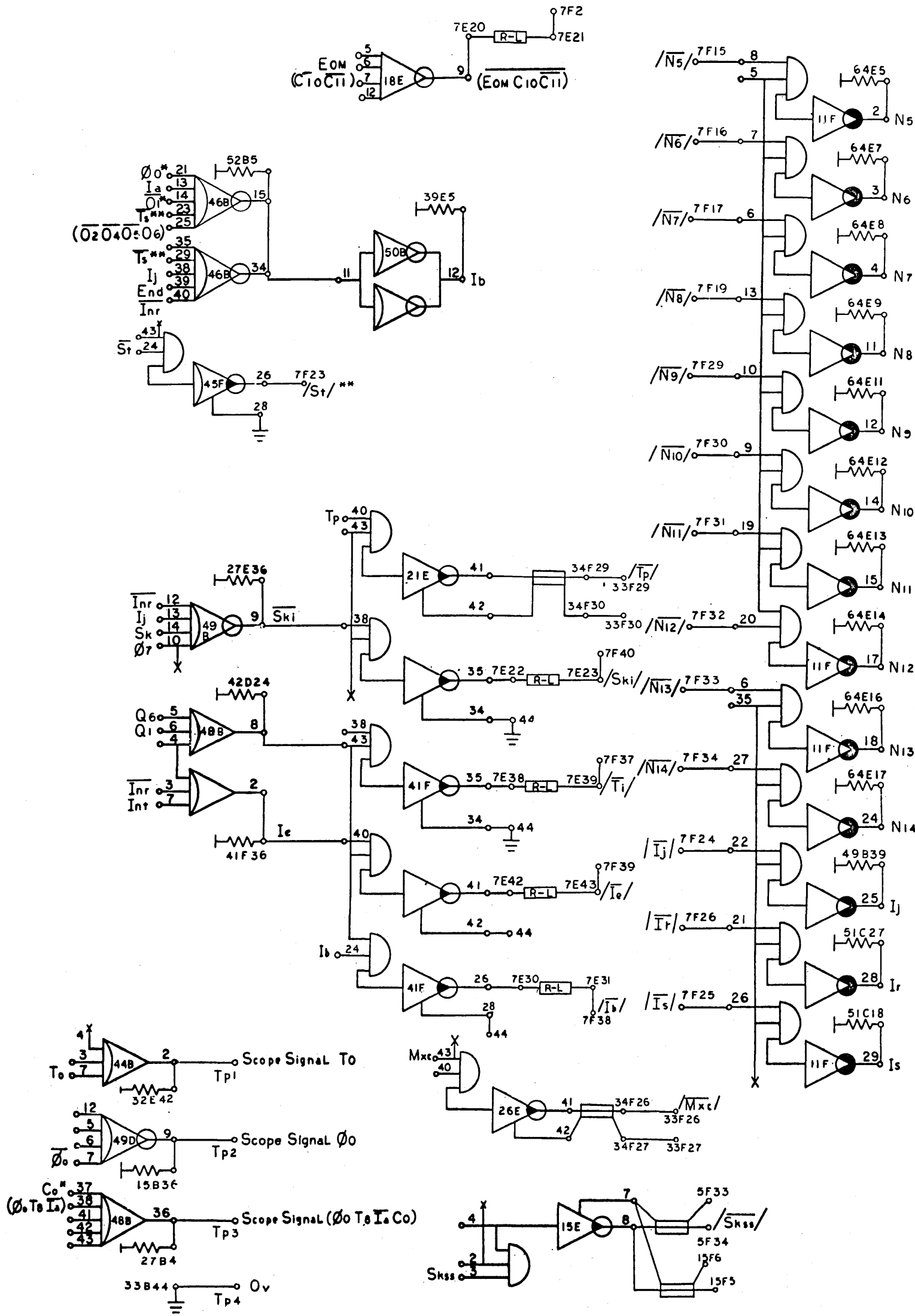
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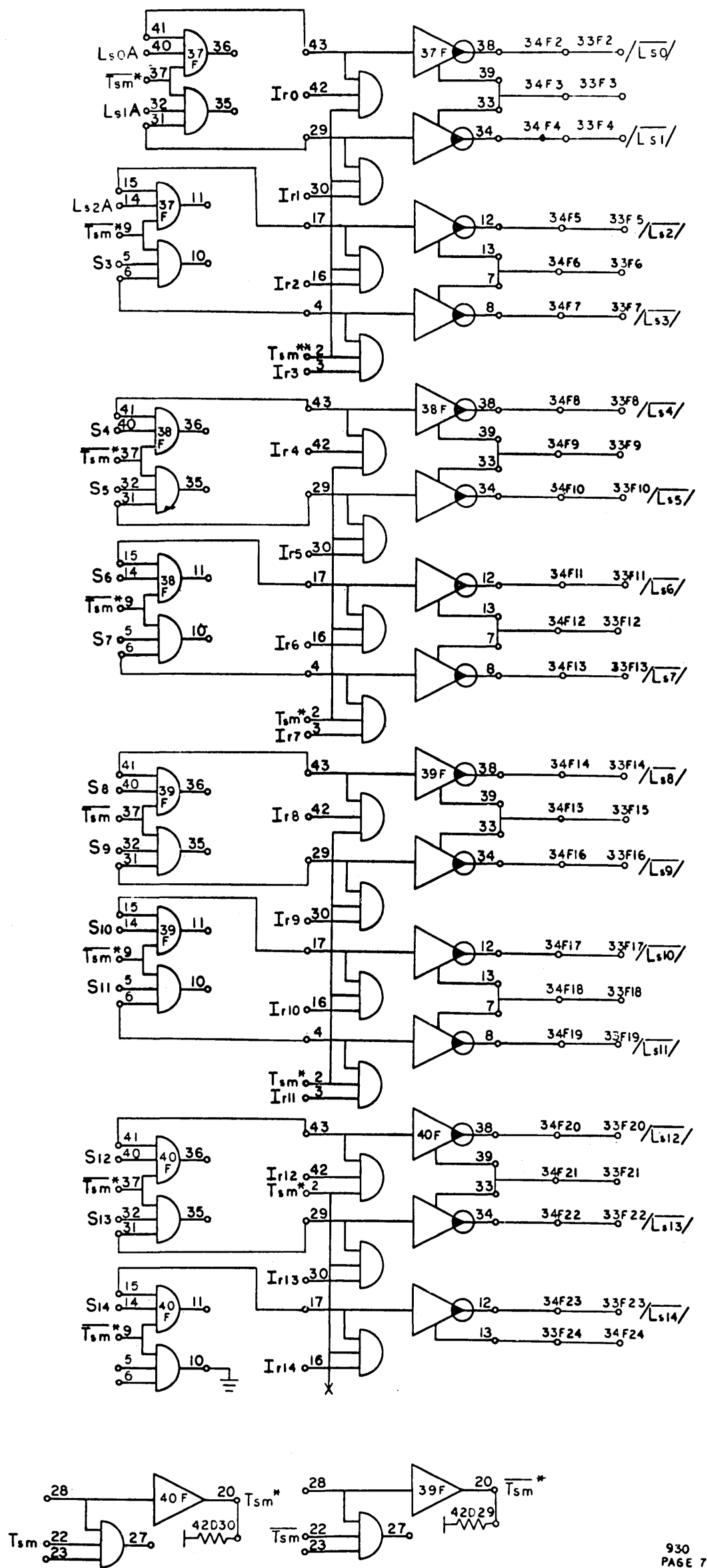
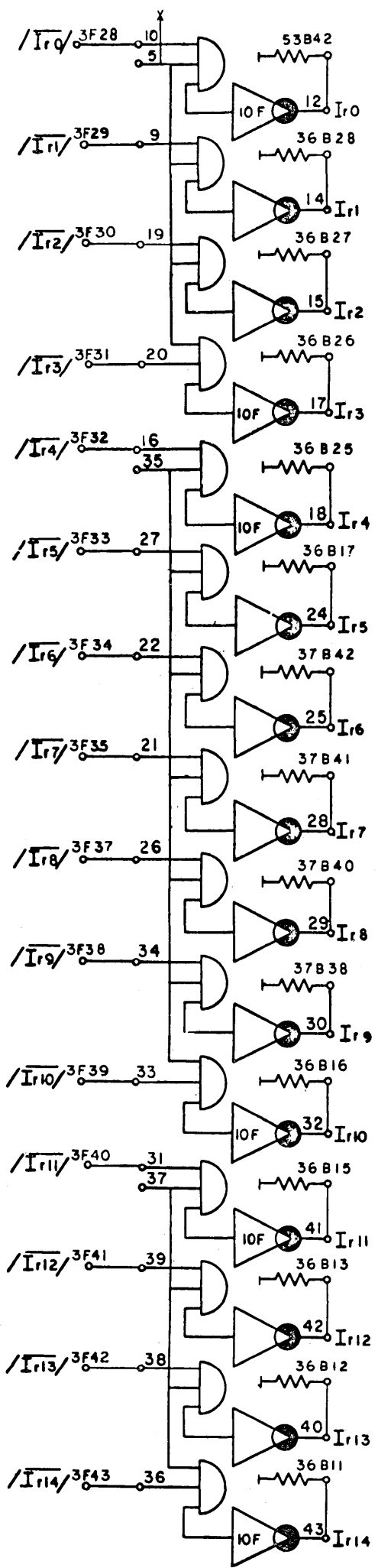
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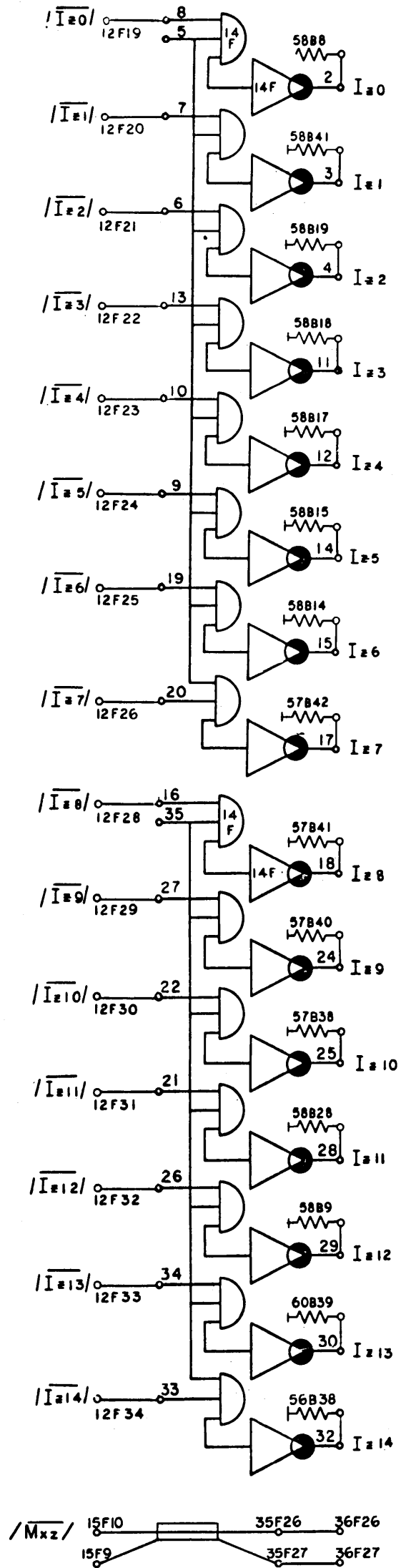
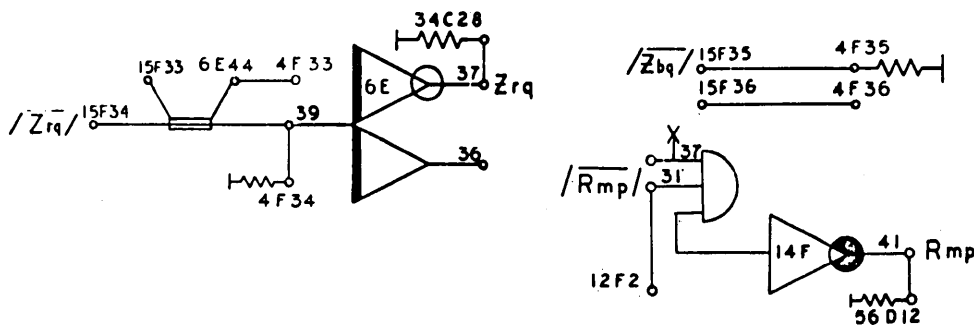
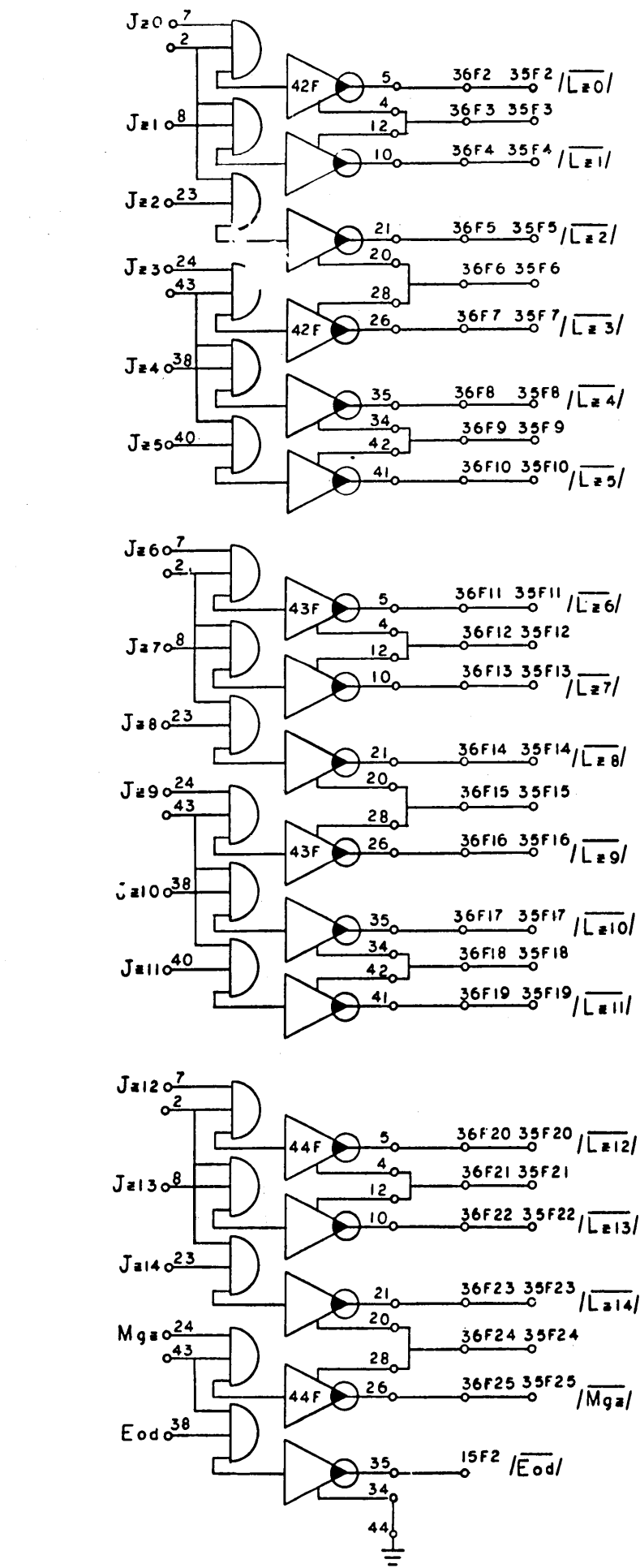
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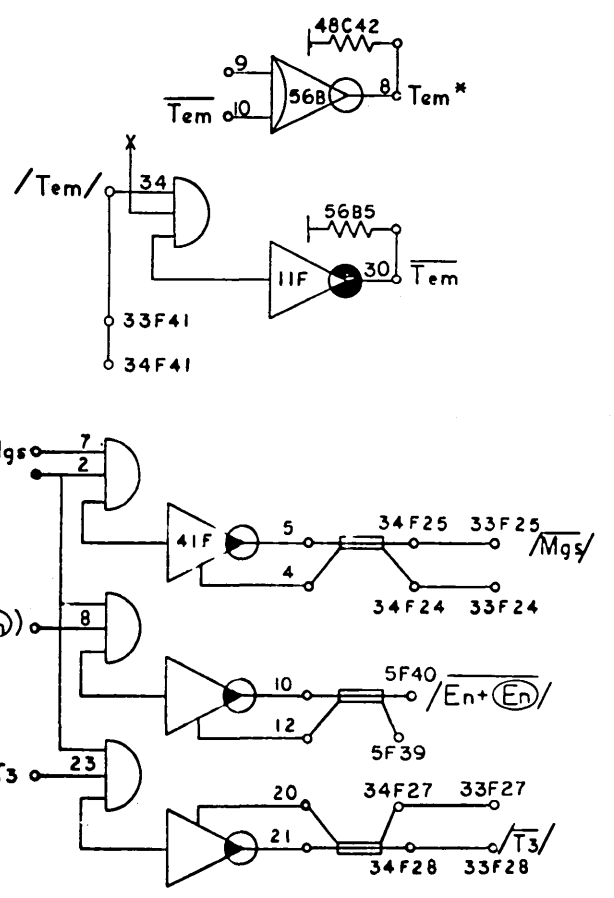
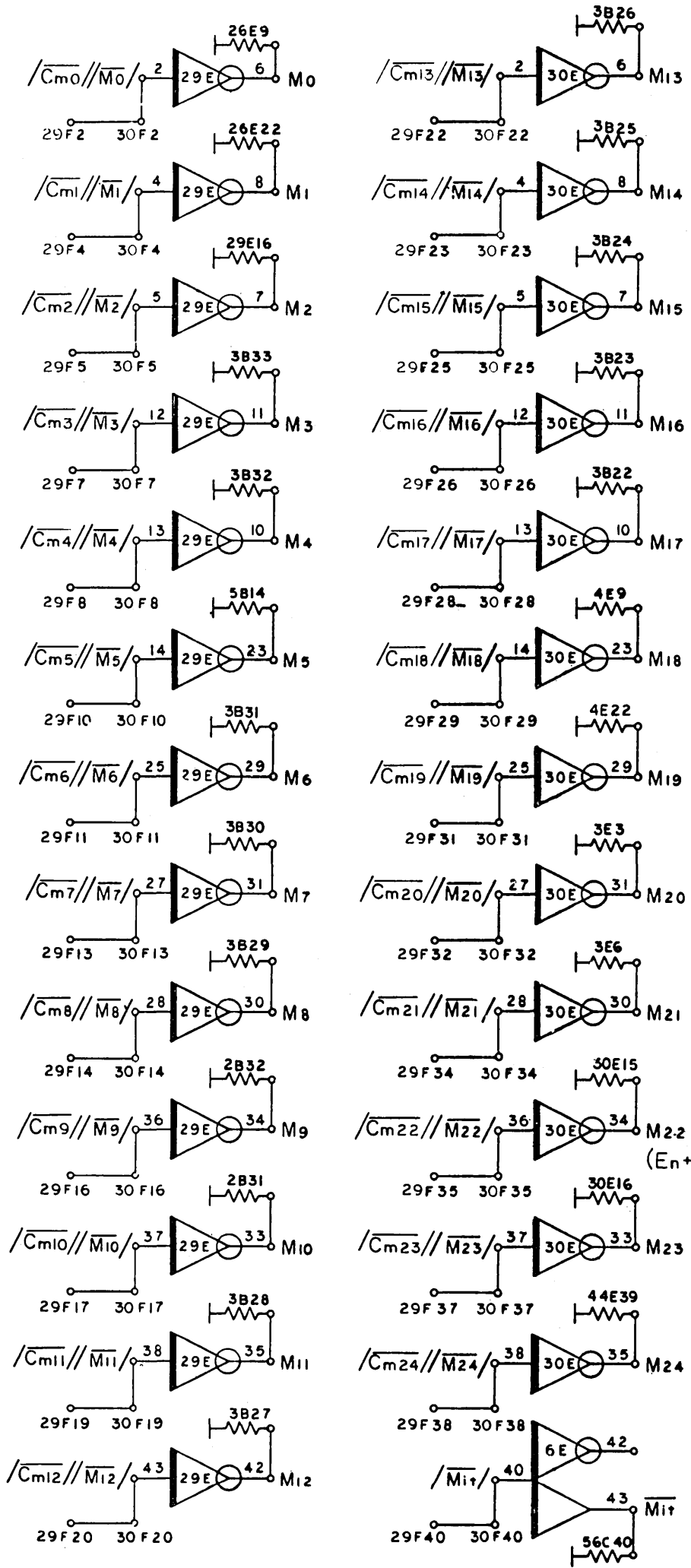
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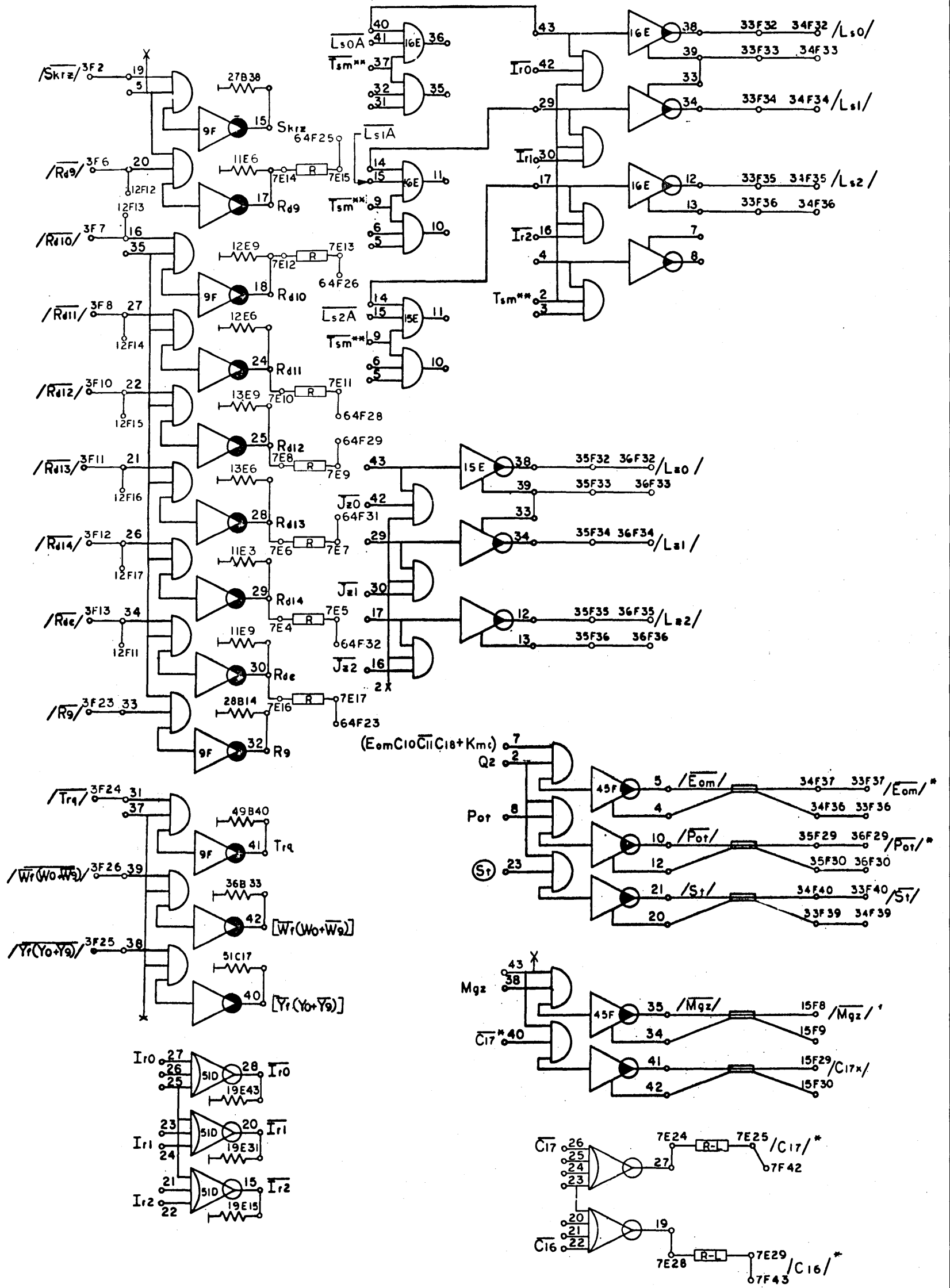
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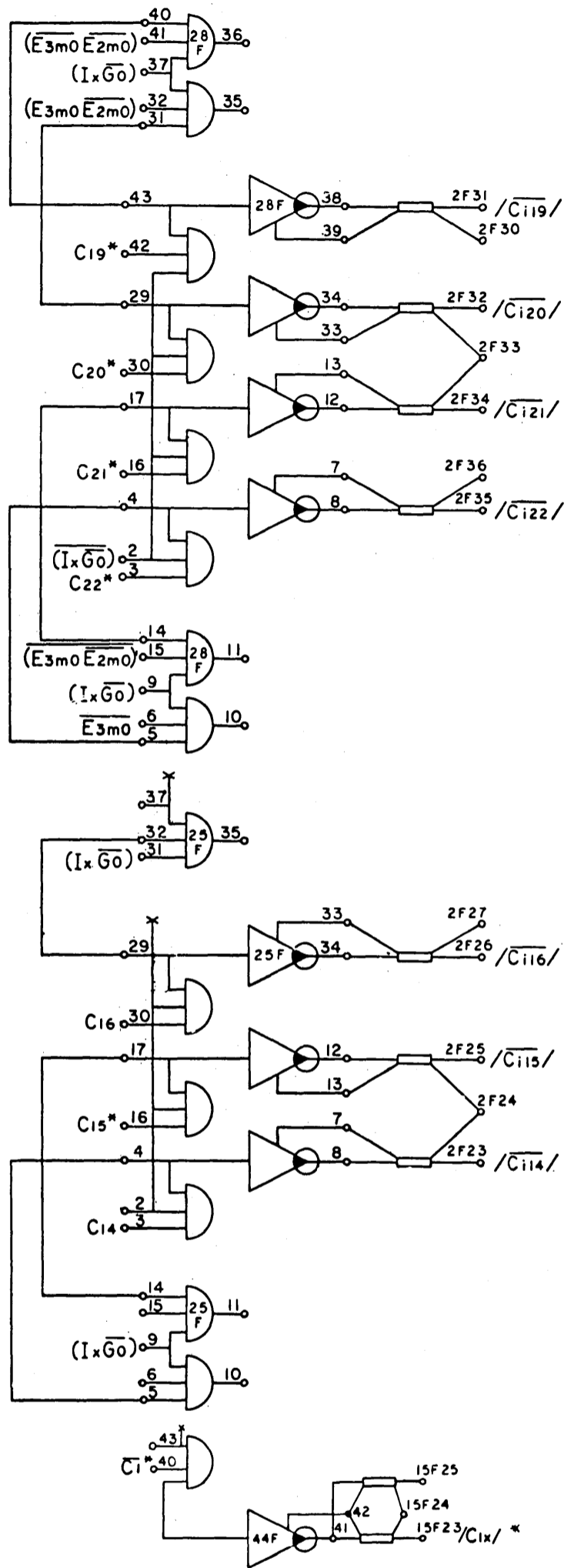
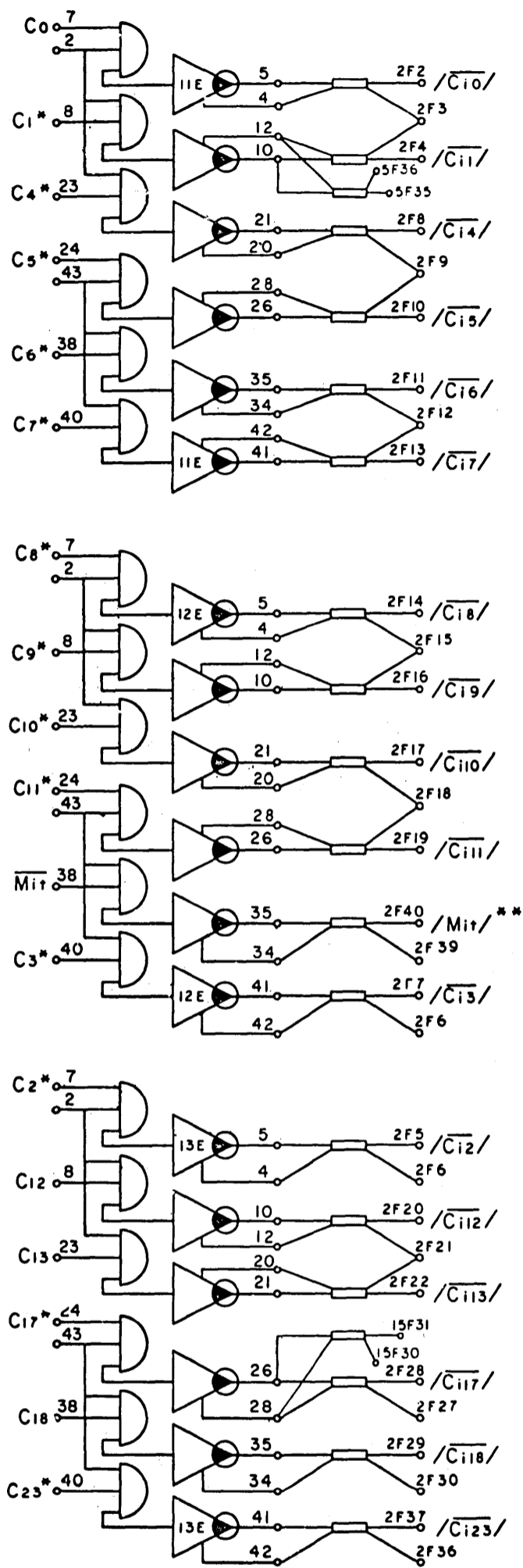
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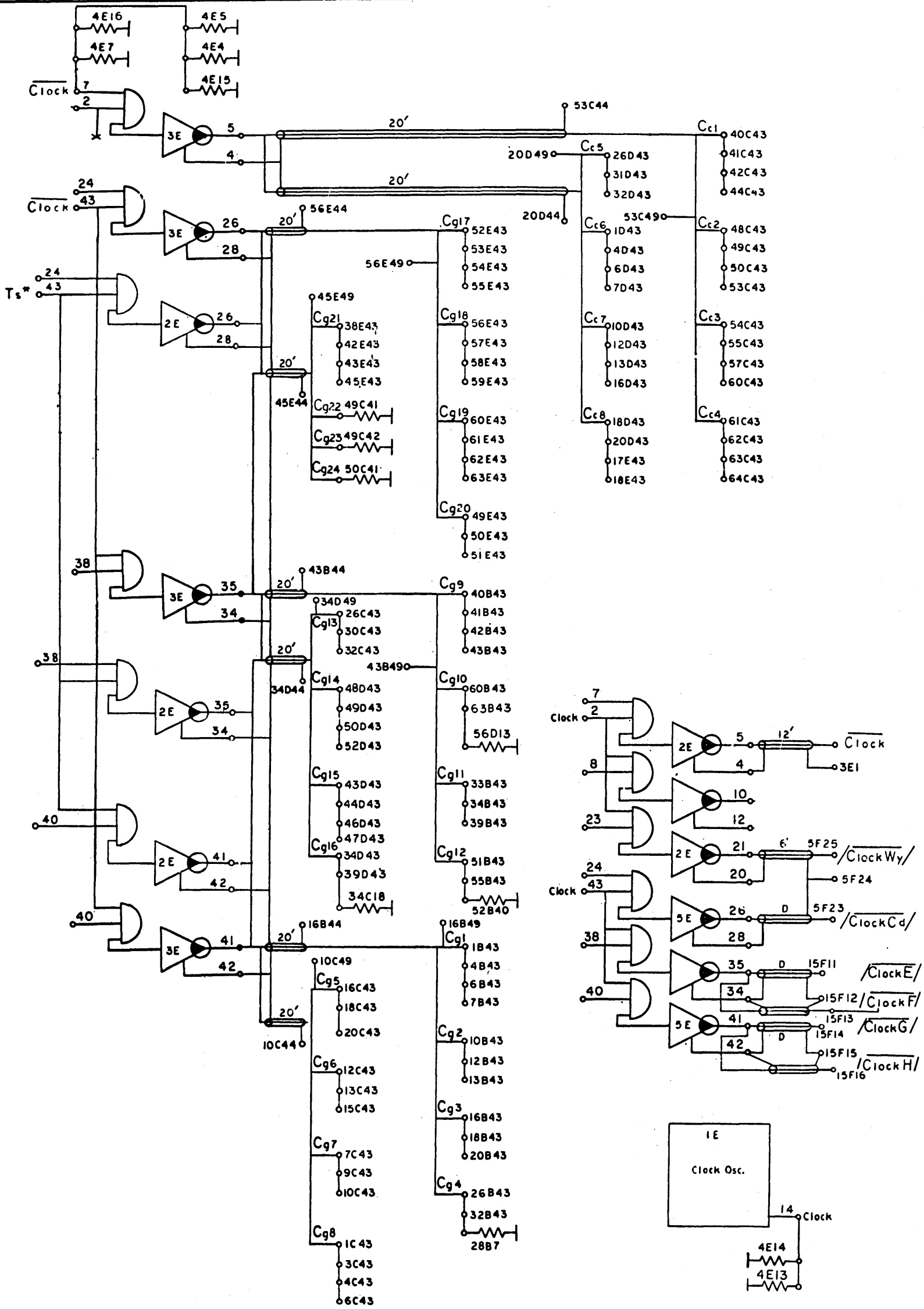
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106407/A



930
PAGE 83
A

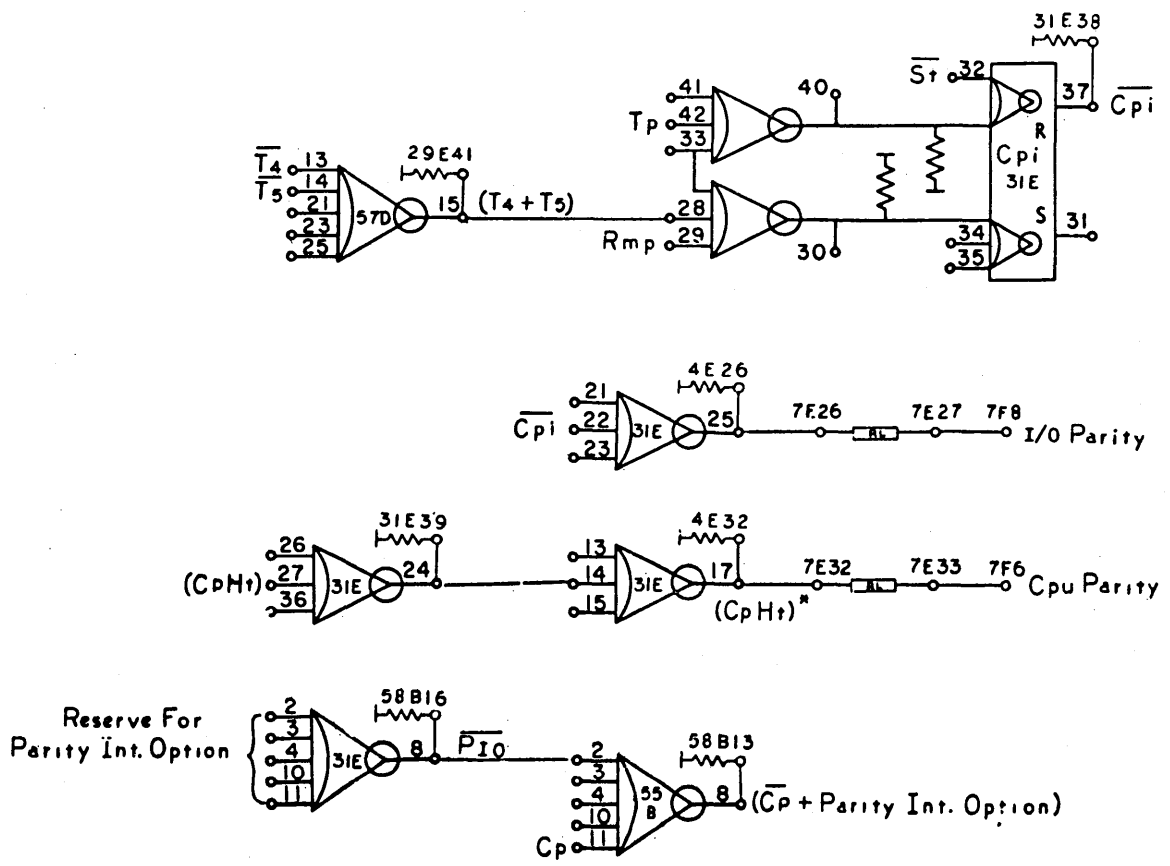
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930
PAGE 84
A

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