H-81-0027

Graphic 8™

COMPUTER GRAPHICS DISPLAY SYSTEM
SERIES 8000

TERMINAL CONTROLLER MAINTENANCE MANUAL

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Federal Systems Group
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Sanders Associates, Inc. reserves the right to modify the products described in this manual and to make corrections or alterations to this manual at any time without notice.

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SAFETY PRECAUTIONS

The following are general safety precautions not related to any specific procedure and therefore do not appear elsewhere in this manual. These are recommended precautions that must be understood and applied during installation or maintenance of the terminal controller.

AVOID LIVE CIRCUITS

Observe all safety regulations at all times. Do not replace components in the terminal controller power panel assembly with power applied.

RESUSCITATION

When working with or near high voltages, be familiar with modern resuscitation methods.

WARNING

Primary power (100 Vac to 240 Vac) is present at the power panel assembly. Line voltage of 115 Vac is present at the power supply.

Always turn off terminal controller and pull power plug before moving any cabinet- or chassis-mounted component.

TERMINAL CONTROLLER PROTECTION

Circuit card assemblies in the terminal controller can be damaged by transient surges.

CAUTION

Always turn off terminal controller before removing or installing any circuit card.

SPECIAL HANDLING FOR MOS DEVICES

MOS devices are subject to damage caused by static charges. Assemblies that contain MOS devices are mapping memories and timing module. When not installed in the card cage, these assemblies should be stored in black Velostat bags with the MOS warning statement printed on the outside of the bag.

CAUTION

Always handle these cards only by the card extractors or by the edges of the connector. Avoid touching the card components or the printed circuit.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Sanders Associates, Inc. GRAPHIC 8™ is a high-performance, intelligent computer graphics terminal system incorporating refreshed raster display technology. It is designed to interface a host computer and to support operator CRT display monitor stations configured with interactive devices, such as keyboards, trackballs, forcesticks, and data tablets. Also, it can produce permanent hard copy records of displayed data.

The GRAPHIC 8 features a dynamic display update via a double refresh buffer memory technique, and supports up to four CRT display monitors. Resolutions of 512 x 512, 640 x 480, 1024 x 768 (interlaced) or 1024 x 1024 (interlaced) are available. Both color and monochrome versions are offered with up to 8 bits per pixel to provide as many as 256 simultaneous colors or monochrome intensities (or 128 plus blink).

The GRAPHIC 8 display processor is a general purpose digital computer with a set of over 400 instructions that controls a variety of functions to reduce the loading on the host computer. In combination with the host computer, the GRAPHIC 8 system permits the user to display digital data in a visual format on the CRT display monitor and to interact with the displayed image by means of keyboards, forcesticks, trackballs, and data tablets. Its high performance and intelligence make it well suited to a variety of applications, such as CAD/CAM, simulation and training, command and control, cartography, and many others.

1.2 COMPONENT DESCRIPTION

The basic GRAPHIC 8 system (figure 1-1) consists of a terminal controller, (figure 1-2) and a monitor. The basic system can be expanded to include a wide variety of options and enhancements.

1.2.1 TERMINAL CONTROLLER. The GRAPHIC 8 terminal controller consists of a rack mountable card cage and a power supply. As shown in figure 1-3, the cards are interconnected by a processor bus or a graphic bus. The size of controller selected is based on the four following major considerations:

1. Color or monochrome
2. Number of simultaneous colors or intensities
3. Resolution of the display image
4. Number of display stations per controller

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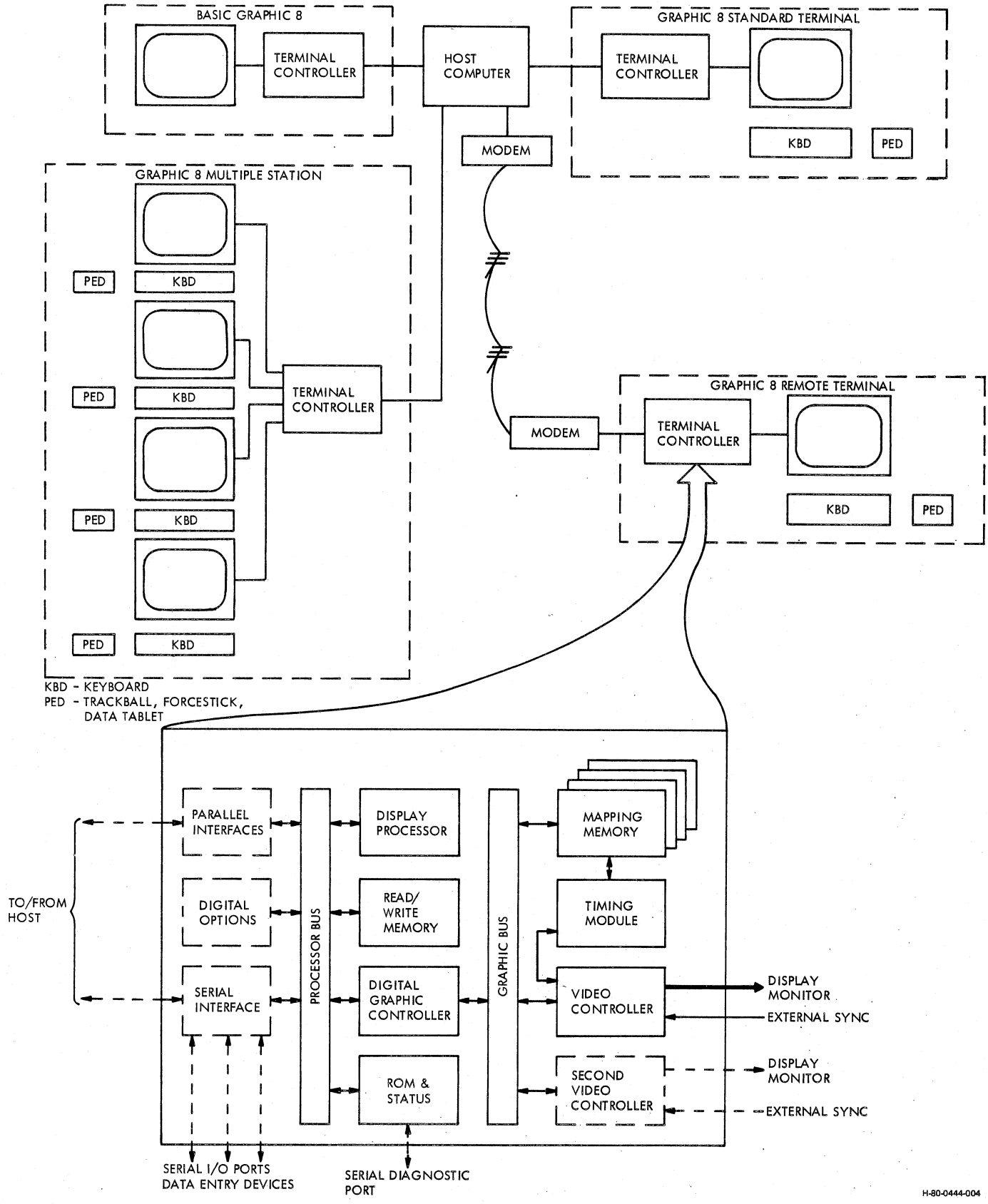
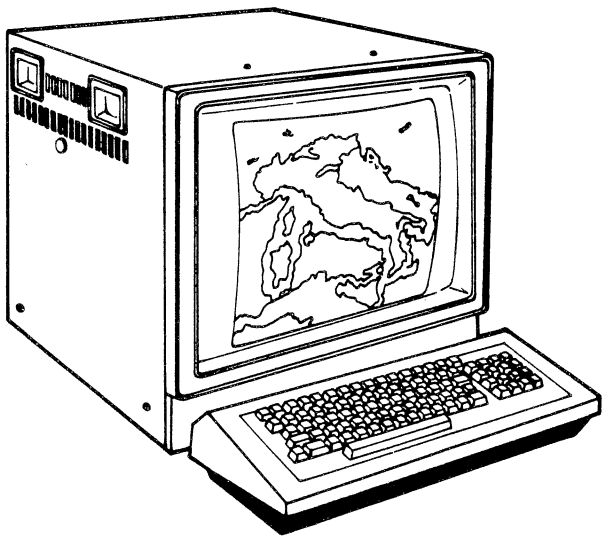
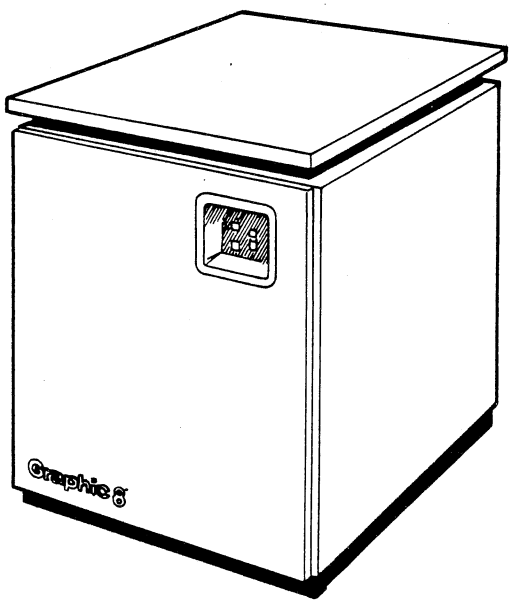


Figure 1-1. Typical GRAPHIC 8 System Configurations



COLOR DISPLAY MONITOR
AND KEYBOARD



TERMINAL CONTROLLER

Figure 1-2. GRAPHIC 8 Terminal Controller and Monitor

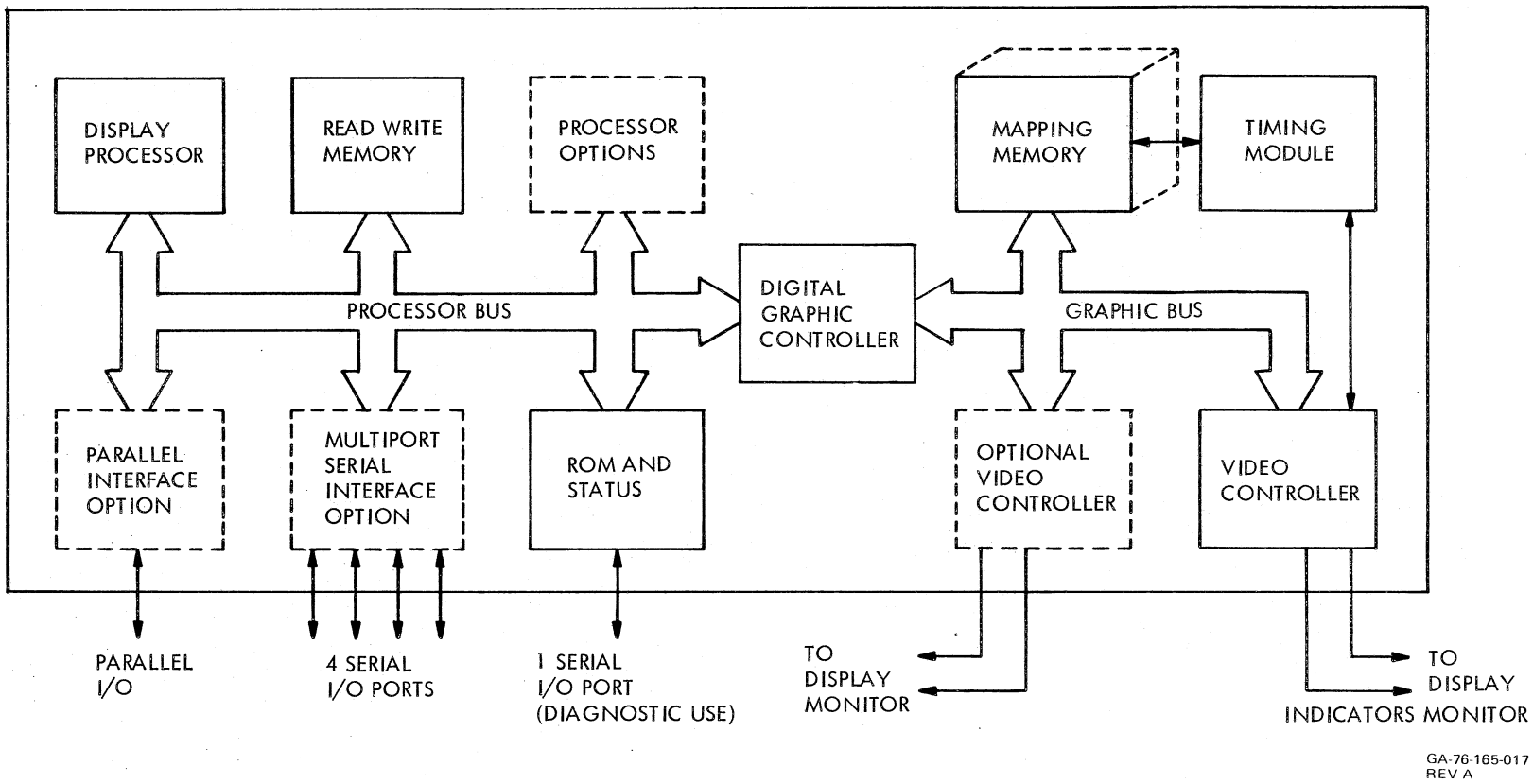


Figure 1-3. GRAPHIC 8 Terminal Controller Organization

The GRAPHIC 8 terminal controller consists of a power supply and a card cage with slots for 17 cards. Six of the slots are for the processor cards, one slot is for the digital graphics controller, one slot is for the timing module, and the remaining nine slots are for the mapping memory and video controller cards.

1.2.1.1 Display Processor. The display processor card is a general purpose digital computer that runs the GCP and acts as master control for all devices connected to the processor bus. It contains multiple high-speed general-purpose registers that can be used as accumulators, pointers, index registers, or auto-indexing pointers in auto-increment and auto-decrement modes. Functions performed by the display processor card include system initialization, interface handling, local data editing, and local generation of simple display images.

Instructions used for the display processor emulate the instruction set for the PDP-11/34® manufactured by Digital Equipment Corporation (DEC®). They are fetched either from the GCP in read-only memory on the ROM and status logic card or from the read/write memory. An 8-bit configuration switch is program readable (used by GCP) from octal location 177774.

1.2.1.2 Read/Write Memory. Locations in the read/write memory are assigned addresses 000000_8 through 777777_8 and are accessed by an 18-bit address on the processor bus and by a 16-bit address and mapping registers on the memory card. The 18-bit address can be used to access the location of a word (16 bits) or of an individual byte (8 bits) as required. Figure 1-4 is the GRAPHIC 8 system memory map.

Each read/write memory card is capable of storing $65,536_{10}$ (64K) sixteen bit words or 128K separately addressable 8-bit bytes. A maximum of two memory cards can be installed in a GRAPHIC 8 system for a total of 128K 16-bit words of memory. The read/write memory card is also available in 16K and 32K word sizes.

NOTE

User refresh programs will not execute in RAM memory in the 24K to 32K area (140000-177777). This area is reserved for Sanders' display processor option software. The option software is loaded from the expansion module or is down-loaded from the host.

1.2.1.3 ROM and Status Logic. The ROM and Status logic card contains the read-only memory in which the GCP used to control the display processor is stored (refer to figure 1-4). Also contained on the card are display status and interrupt logic circuits plus a serial interface port to which a teletypewriter may be connected for diagnostic purposes.

The standard read-only memory provided on the ROM and status logic card contains the GCP firmware. The GCP is approximately 6.6K words (16 bits). Like read/write memory, read-only memory may be accessed to retrieve either 16-bit words or individual 8-bit bytes.

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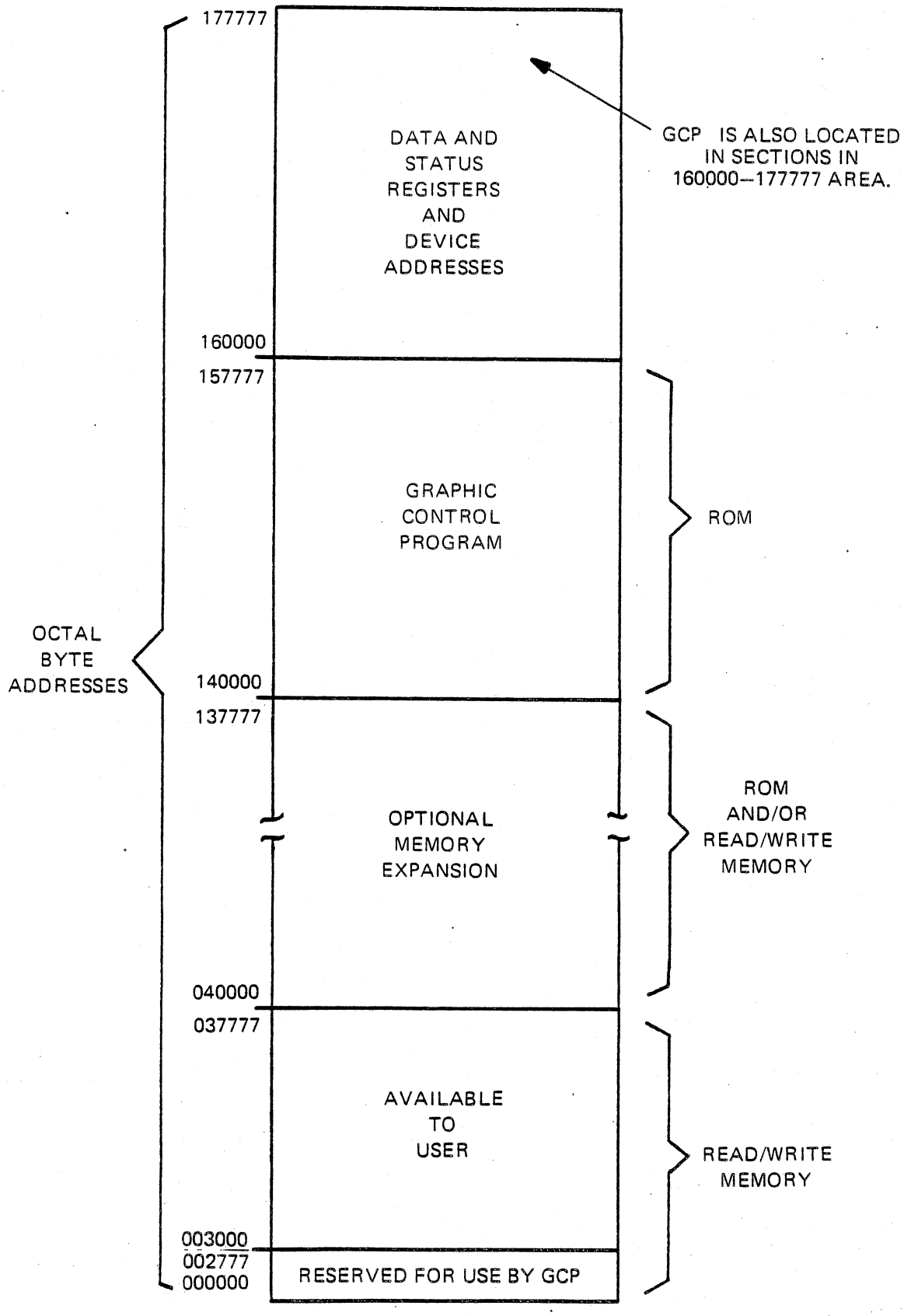


Figure 1-4. GRAPHIC 8 System Memory Map

1.2.1.4 Multiport Serial Interface. The multiport serial interface card contains four serial interface ports that operate in a serial asynchronous mode using RS-232C or TTL voltage levels with standard transmission rates up to 9600 baud. Additionally, the first port can be operated as a full RS-232C asynchronous interface at transmission rates greater than 9600 baud. For GCP applications, the maximum transmission rate supported is 9600 baud. Normally, the host computer is connected to the first port, which is compatible with the standard communication and terminal interfaces supplied by most computer manufacturers. The remaining three ports on the card are used for peripheral devices.

1.2.1.5 Parallel Interface. An optional GRAPHIC 8 parallel interface allows high-speed communications with handshaking and is intended for applications where the GRAPHIC 8 is located in proximity to the host. All parallel interface signals are TTL-compatible. Under program control, the interface operates in either an interrupt driven or a DMA mode. In the latter mode, the interface operates at speeds up to 500,000 16-bit words/second. If a parallel interface card is installed in the terminal controller, GCP assumes that it is connected to the host computer. Therefore, if serial communication with the host computer is desired, a parallel interface card cannot be connected to the processor bus.

NOTE

Normally, if a parallel interface port is used, a single parallel interface card (for the host computer) is installed in the terminal controller. For special applications, however, two parallel interface cards may be installed, but are not supported by the standard Graphic Control Program.

1.2.1.6 Digital Graphic Controller. The digital graphic controller is a microprocessor with more than 50 instructions committed to ROM. It retrieves display update instructions from R/W memory, generates vectors, characters, conics, point plots, and fills, and stores these in mapping memory in raster-scan format. The complete series of sequential instructions that defines any particular display image is referred to as a refresh file.

The digital graphic controller may be considered as a device on the processor bus of the terminal controller. It contains its own set of registers that maintain instruction address, control fetch operations, and perform any branching that may be specified by non-graphic instructions. It also calculates relative data when required, loads data into appropriate registers, and initiates execution of refresh file instructions.

Status bits of the digital graphic controller are maintained by circuits on the ROM and status logic card. These bits plus the graphic controller registers are accessible to the display processor which maintains control over the entire terminal controller.

1.2.1.7 Mapping Memory. The mapping memory contains pixel data in a format which allows display refresh in a raster scan mode. The mapping memory may be configured for various resolutions up to 1024 x 1024 (see figure 1-5) and for interlace or non-interlace refresh. A single memory board can be supplied with a capacity of over four million bits. Up to eight bits can be combined per pixel to provide 256 possible colors or intensity levels.

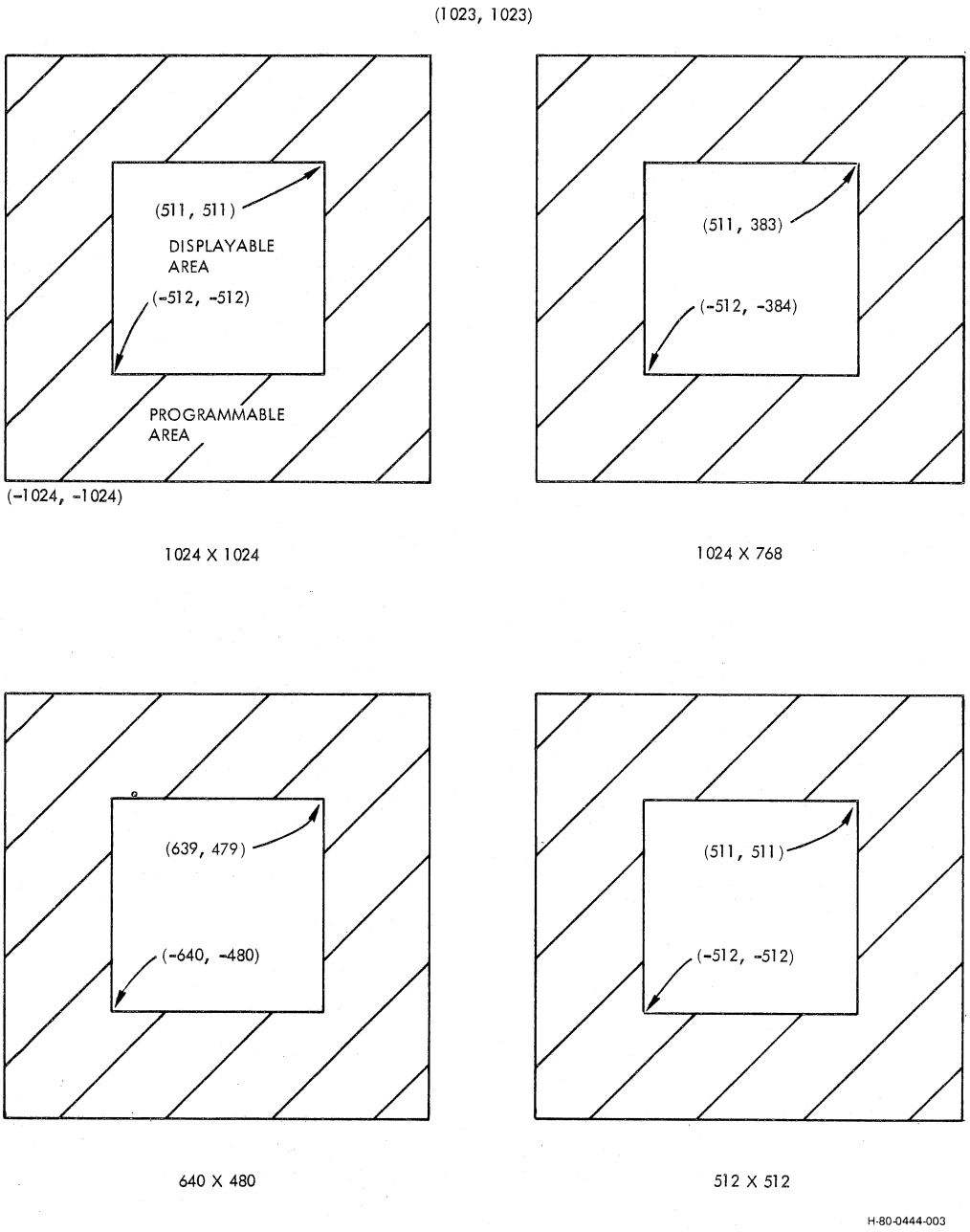


Figure 1-5. Addressable Vs. Displayable Areas for Four Screen Resolutions

A dual mapping memory configuration is for high-speed dynamic update of data. The dual memory concept allows the hardware to clear and update one memory while the second memory is refreshing the display. When the next update occurs, the roles of the two memories are reversed so that the previously updated memory now becomes the refresh memory.

1.2.1.8 Video Controller. The video controller obtains data from the mapping memory and formats it for presentation on the display monitor(s). Outputs are provided as either RGB color or monochrome and as composite video.

External video may be accepted by the video controller and logically ORed with internally-generated video. A single video controller can accomodate up to eight bits per pixel.

The video controller generates one non-destructive, full-screen, crosshair cursor and contains the cursor address registers which are accessible to the user. It controls the split screen function which allows the user to divide the display face into two or three variable-height horizontal bands and fill these bands with data from anywhere in addressable mapping memory. This feature allows the user to simultaneously view up to three separate areas of mapping memory which are not necessarily contiguous.

The video controller contains a 256 x 8-bit word RAM look-up-table (LUT) which allows pseudo-color or pseudo-gray level transformation to be made.

1.2.1.9 Timing Module. The timing module generates all display-related timing signals as well as the necessary synchronization signals for the monitors. On-board switches allow selection for compatible operation with the possible resolutions and refresh frequencies.

1.2.1.10 Character Generation. Character generation is performed by the digital graphic controller. The basic set of characters supplied is a standard set of 96 ASCII characters. When the ASCII code corresponding to the desired character is applied to the read-only memory, the character is drawn at the position determined by the current position for X and Y.

As determined by instructions from the digital graphic controller, characters of three different sizes can be generated. Characters may also be rotated 90 degrees counterclockwise to accommodate vertical writing requirements. Both normal and rotated characters can be made to blink.

Read-only memory for six groups of 16 characters can be added to provide a total of up to 192 standard and special characters that can be produced by the GRAPHIC 8.

1.2.1.11 2-D/3-D Coordinate Converter. The Model 5753 2-D/3-D coordinate converter converts a Sanders graphic display into a three dimensional display capable of independent dynamic manipulation of objects in apparent space. Among the functions provided by the Model 5753 are translation, scaling, rotation, windowing, independent display coordinate mapping, perspective, and zooming with perspective.

The perspective feature is especially useful for realistic viewing of an object. Utilizng perspective, the location of the viewer is defined relative to the image space, and all lines and objects within the image space are then viewed at the proper perspective for that location. The view may be completely orthographic if the viewer does not wish to use the perspective feature.

Objects can be defined within a 64K (X), 64K (Y), by 32K (Z) image space and presented on a 1K by 1K screen or any portion thereof. Translations can be made within the limits of the image space and scaling range is 64 to 1. Rotation can be provided about any axis.

3-D windowing, in conjunction with independent screen coordinate mapping, allows the presentation of any data within a software definable X, Y, Z image space to be presented on the full screen or any portion of the screen. Zooming is accommodated by scaling and changing the user's apparent perspective viewpoint.

Alphanumeric data can be moved about the screen with vector defined data without scaling and rotation.

The 5753 provides for both homogeneous and non-homogeneous matrix operation. Also, transformations of 2-D images can be accomplished including translation, rotation, scaling, and windowing.

1.2.1.12 Data Converter. The model 5744 data converter option transforms incoming floating point binary numbers into displayable numbers. The displayable numbers may be in any of sixteen formats selected by the host. The bi-directional converter also converts the displayed numbers into floating-point binary for transmission back to the host.

The data converter saves host computer time and storage resources by performing these conversions within the graphic terminal. It allows data to be transmitted to and from the host in its most compact form and frees the host programmer from the conversion programming task.

The data converter can perform more than 500 conversions per second, which allows it to be used in high data-rate applications resulting in significant off-loading of the host computer.

The data converter is not supported by the standard Graphic Control Program.

1.2.1.13 EPROM Expansion Module. As options are added to the GRAPHIC 8, the additional software required to handle the options will be stored on the model 7750 expansion module.

The expansion module may contain up to 32K 16-bit words of non-volatile read-only memory (EPROMS). The data may be loaded from the expansion module automatically by pressing the SYSTEM button or when so instructed by the host, depending on the options stored.

1.2.2 INPUT DEVICES. Optional data input devices for the GRAPHIC 8 give the operator two-way interaction with the display and processing system. Input devices available include two types of keyboards; a trackball, a forcestick, and a data tablet. The GCP in firmware can support up to eight keyboards, or eight position entry devices (trackball, forcestick, or data tablet). In addition, a teletypewriter or paper tape reader can be connected to the GRAPHIC 8 for the input of maintenance data.

1.2.2.1 Keyboards. Standard keyboards available for the GRAPHIC 8 are the Model 5783 and Model 5784 keyboards. The keyboards contain a main block of alphanumeric keys plus a matrix and a row of function keys.

The Model 5783 keyboard offers an alphanumeric block of 58 keys. These keys generate standard seven-bit ASCII codes with an eighth (MSB) bit always set to 1. The alphabetic keys generate both upper and lower case codes. A four-by-four matrix of function keys is located to the right of the alphanumeric block and a row of 16 function keys is located immediately above the alphanumeric block. Each function key generates a single eight-bit octal code from 000 to 037.

An added feature of the Model 5784 keyboard is that each function key contains an LED that can be lighted or turned off as required under program control. The Model 5784 also has provisions for additional keys to the basic board. These keys are for future expansion and are located on both sides of the space bar.

The keyboards operate at a rate of 9600 baud and interface to the terminal controller via ports on the multiport serial interface card.

1.2.2.2 Trackball, Forcestick, and Data Tablet. The trackball, forcestick, and data tablet are referred to as PEDs (position entry devices). These devices are used as determined by program control to move a cursor and/or data displayed on the CRT screen. Movement initiated by the trackball is proportional to the speed and direction in which the trackball is rolled. Movement initiated by the forcestick is proportional to the direction and force with which the forcestick is deflected. Movement initiated by a data tablet is proportional to the speed and direction in which the data tablet pen is moved along the data tablet surface. PEDs are connected to the system via ports on the multiport serial interface card(s) in the terminal controller.

1.2.2.3 Maintenance Data Input Devices. A teletypewriter and/or a paper tape reader can be connected to the GRAPHIC 8 to input data for maintenance purposes. The teletypwriter is normally connected to a port on the ROM and status card in the terminal controller while the paper tape reader is connected to one of the ports on a multiport serial interface card. The teletypewriter serves basically as a troubleshooting aid. The paper tape reader is used to load special user or diagnostic programs into the GRAPHIC 8.

1.2.3 OUTPUT DEVICES. The standard output device for the GRAPHIC 8 is the CRT display monitor. A hardcopy unit is available as an optional output device. Using the same signals that go to a standard display monitor, the hardcopy unit can produce a duplicate on paper of any static image displayed on the CRT of the display monitor. Operation of the hardcopy unit is controlled manually.

An optional hardcopy multiplex switch is available. The multiplex switch is capable of interfacing up to four GRAPHIC 8 displays to a single hardcopy unit.

1.2.3.1 Display Monitors. The GRAPHIC 8 offers the user a choice of configuration of eight CRT monitors (four monochrome and four color) to provide the right monitor for the intended application.

Positions on the screen are specified in terms of a matrix containing 2048 coordinates in the X dimension and 2048 coordinates in the Y dimension. Two's complement notation is used to designate the coordinates with location 0, 0 being defined as the center of the screen. Of the 2048 by 2048 addressable locations, the displayable area comprises the field of coordinates centered about the middle of the screen. Refer to figure 1-5 for different screen resolutions.

1.2.3.2 Hardcopy. Both monochrome and color hardcopy devices are available for use with the GRAPHIC 8.

1.3 TERMINAL CONTROLLER PHYSICAL DESCRIPTION

The terminal controller comprises a card cage, a power supply, and two fans. A control panel covers the front of the unit; a protective cover is mounted on the back.

The terminal controller is mounted either in a standard 19-inch equipment rack or in an optional cabinet. In either case, the control panel is removed for access to the terminal controller.

The circuit cards are inserted into the card cage from the front of the terminal controller, and plug into a wire-wrapped backplane. The blower fans, located beneath the card cage and power supply, draw air from the bottom of the unit and discharge the air through the top.

The basic terminal controller contains nine standard circuit cards. Optional cards are inserted as required. Most applications use both the multiport serial interface and the parallel interface cards. Other cards are available to expand the read/write memory or provide special display functions.

Figure 1-6 shows the circuit card order assumed for this manual. The figure indicates the normal locations for a full complement of circuit cards, including the optional interface cards and read/write memory expansion cards.

Table 1-1 lists the physical characteristics of the terminal controller and circuit cards.

The terminal controller can operate with 100V - 120V or 220V - 240V ac input power. An input power control panel (located in a lower front of the equipment cabinet) contains a fuse, a power receptacle, and a removable configuration plug. The configuration plug must be wired for the proper voltages. The power panel contains two outlets. One outlet is live when the circuit breaker is ON. The other outlet is live when the circuit breaker is on and a control signal is applied through a connector (P2) on the power panel.

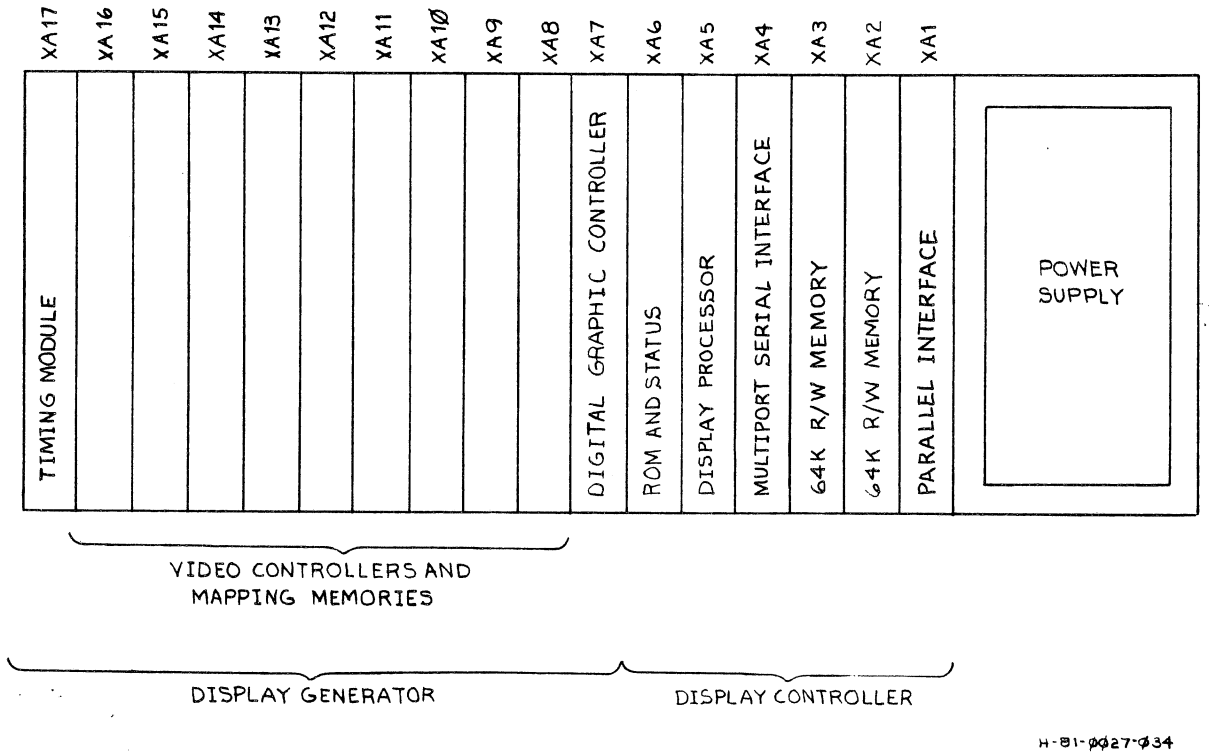


Figure 1-6. Typical Terminal Controller Card Locations

Table 1-1. Physical Characteristics

TERMINAL CONTROLLER	
Height	10.5 inches (26.8 cm)
Width	19.0 inches (48.2 cm) including mounting flanges
Depth	16.0 inches (40.6 cm)
Weight	55 pounds (25 kg) including circuit cards
CIRCUIT CARDS	
Height	12-3/8 inches (31.4 cm)
Width	7-3/4 inches (19.7 cm)

1.4 POWER AND ENVIRONMENTAL REQUIREMENTS

The terminal controller requires 250W of single-phase primary power. The power source must be within six cable-feet of the terminal controller.

The terminal controller fits a 10.5-inch vertical space in a standard 19-inch equipment rack, either directly or on slides. The controller can also be supplied as a stand-alone cabinet unit.

The operating environment temperature range is +15°C (59°F) through +40°C (104°F). The relative humidity should not exceed 90%.

1.5 PERFORMANCE SPECIFICATIONS

Table 1-2 lists the performance specifications for the overall terminal controller and its assemblies where applicable.

1.6 EQUIPMENT IDENTIFICATION

The part number of the terminal controller is a function of its card complement and thus varies from installation to installation. The Sanders identification plate at the rear of the terminal controller carries the part number, voltage rating, current rating, and UL, CSA, and VDE identification.

The part number of the card cage is 5977184.

Nomenclatures and part numbers for the circuit cards are etched on the component side of the cards. Serial numbers are stenciled next to part numbers.

All correspondence and documentation concerning the terminal controller or its assemblies should include full identification data.

1.7 TEST EQUIPMENT REQUIRED

The following equipment (or equivalent) is recommended for maintenance of the terminal controller:

Oscilloscope	Tektronix type 547 with type 1A1 preamplifier
Digital voltmeter	Fluke model 8000A
Multimeter	Triplett model 630
Card extender	Sanders part no. 4171110

1.8 RELATED PUBLICATIONS

Publications relating to the GRAPHIC 8 system are as follows:

PUBLICATION NO.*	TITLE
H-80-0483	GRAPHIC 8 Technical Description
H-80-0444	GRAPHIC 8 Programmer's Reference Manual
H-81-0021	GRAPHIC 8 Fortran Support Package Reference Manual
H-81-0027	GRAPHIC 8 Terminal Controller Maintenance Manual
H-81-0097	GRAPHIC 8 Terminal Controller Maintenance Diagrams Manual

PUBLICATION NO.*	TITLE
H-81-0120	GRAPHIC 8 19-Inch Color Display Manual
H-80-0087	Terminal Controller Power Supply Model MM23-E0647/115
H-79-0350	Model 5753 2-D/3-D Coordinate Converter User's Manual
H-79-0363	Model 5783 Alphanumeric Function Keyboard/Model 5784 Lighted Alphanumeric Function Keyboard
H-78-0044	Model 5786 Trackball/Model 5787 Forcestick Entry Devices Technical Manual
H-81-0129	GRAPHIC 8 Installation Manual

*This column lists the manual's basic number. Revisions are indicated on the cover of the manual by a letter following this basic number.

1.9 MNEMONICS CONVENTIONS

The convention established for naming mnemonics throughout this manual is as follows. In general, terminal controller mnemonics consist of six characters. The first four are an alphanumeric abbreviation of the signal name. The fifth is a sign (+ or -) that indicates the active state of the signal (high or low). The sixth character is an alphabetic code that identifies the source of the signal as follows:

SOURCE CODE	SOURCE
B	Processor bus signal
D	Display processor
F	ROM and status
H	Digital graphic controller
I	Parallel interface
M	Read/write memory
N	Mapping memory
S	Multiport serial interface
U	Timing module
V	Video controller
X	Multiple source

Register and bus mnemonics use the lowest numeric to designate the least significant bit and the highest numeric to designate the most significant bit. For example, in the terminal controller data bus:

DA00-B = LSB
DA15-B = MSG

Power supply mnemonics are as follows:

MNEMONIC	DESCRIPTION
P05V+	+5 Vdc
P15V+	+15 Vdc
N15V-	-15 Vdc
ARET-	Analog ground
DRET-	Digital ground
CGND	Chassis ground

Table 1-2. GRAPHIC 8 Terminal Controller (Model 8XXX) Specifications

GENERAL	
Power Source	115 ± 10 vac 47 to 63 Hz
Power	300 Watts
Temperature Storage	0° to 50°C
Temperature Operating	15° to 40°C
Relative Humidity	10 to 90%
Dimensions:	
Rack Mount Configuration	
Height	10.5 in (26.8 cm)
Width	19.0 in (48.2 cm)
Depth	16.0 in (40.6 cm)
Weight	55 lbs (25 kg) including cards
Equipment Cabinet Configuration	
Height	30 in (76.2 cm)
Width	23 in (58.4 cm)
Depth	30 in (76.2 cm)
Weight	155 lbs (70.3 kg) on four casters
DISPLAY PROCESSOR	
General Purpose Microprocessor	Yes
Word Length	16 bits
Byte Mode	8 bits
Instructions	400 plus
Registers	8
Hardware Stacks	Yes
Automatic Priority Interrupt	Yes
Memory	16 bit words
ROM	8192 words
RAM	65,536 words
Expansion RAM to	131,072 words
INTERFACE OPTIONS (DIGITAL)	
Parallel	16 bits 32 bits (optional)
Serial	RS-232C

GRAPHIC CONTROLLER	
Parallel Microprocessor	16 bits
Display Instructions	50 plus
Synchronized Linkage to Display Processor	Yes
Subroutine Stack	Yes
Display Registers	64 plus
Registers (GP)	4
VECTORS/CONICS	
Line Texture	4
Ellipse	any angle
CHARACTERS	
Font Size	5 x 7 7 x 9
Character Set (STD)	96
User Defined (OPT)	96
Rotation	90° CLK
Sizes	3
Tabular Characters	Auto Text Spacing
Positioning	Random
MAPPING MEMORY	
Addressable Locations	2048 x 2048
Bits/Pixel	2,4,8
VIDEO CONTROLLER	
Blink	Yes
Color or Gray Level	256
Screen Splits	3
Cursor	non-destructive
Terminations	75 ohm
Video	Composite
Displays Max	6

SECTION 2

OPERATION

2.1 GENERAL

This section contains information for operating the GRAPHIC 8 terminal controller. Topics discussed include: controls and indicators, turn-on procedure, and operation in the SYSTEM and LOCAL modes.

2.2 CONTROLS AND INDICATORS

Table 2-1 lists the terminal controller controls and indicators, their locations and functions. Figure 2-1 shows their location on the equipment. Circuit connections for the controls and indicators are shown on the applicable terminal controller diagrams in the Terminal Controller Diagrams Manual (H-81-0097).

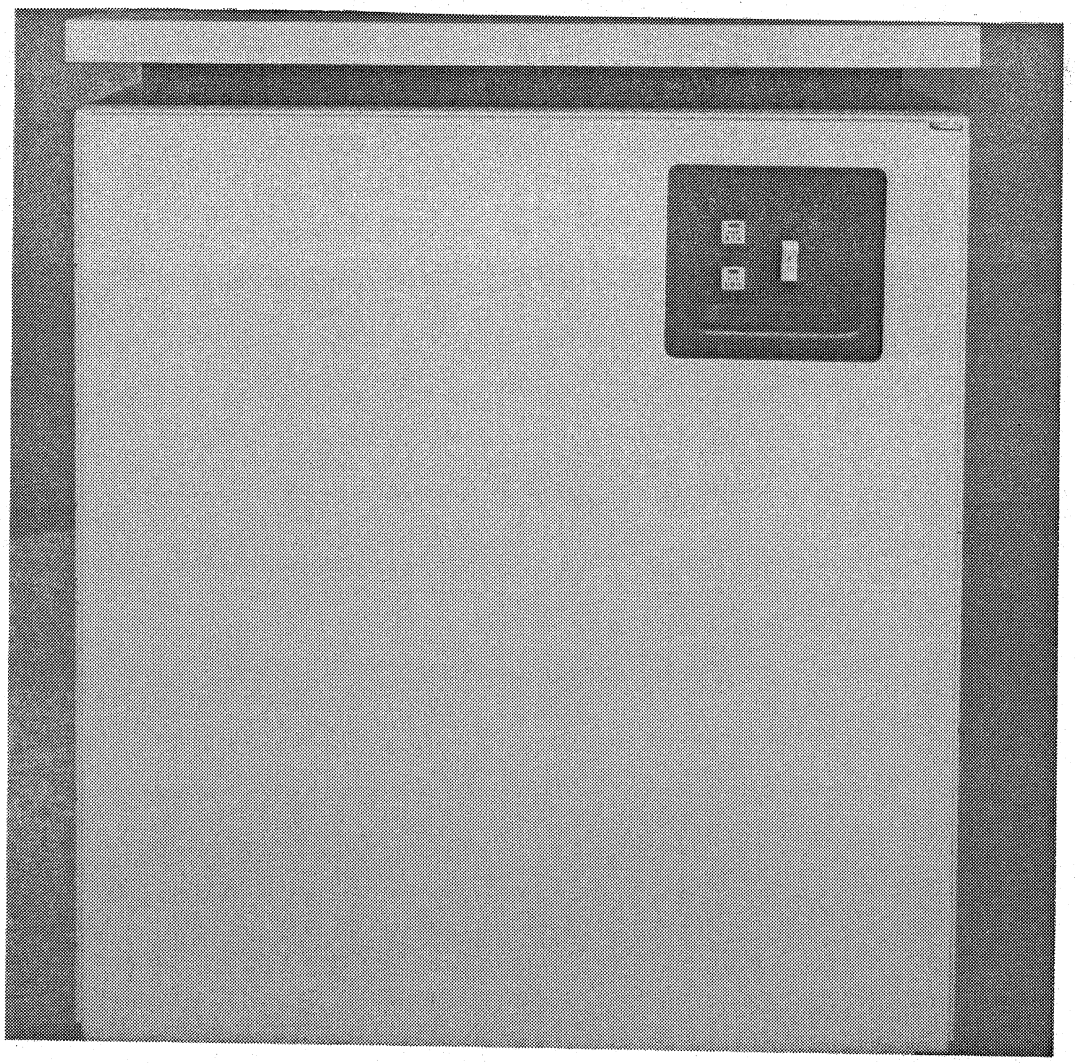
Table 2-1. Terminal Controller Controls and Indicators

NOMENCLATURE	LOCATION	FUNCTION
POWER ON/OFF circuit breaker	Top right of control panel	Energizes/deenergizes terminal controller
RUN/SYS pushbutton	Top right of control panel	Initiates SYSTEM mode (host computer control)
RUN/SYS lamp	In RUN/SYS pushbutton	Indicates display processor card operating
DIS/LOC pushbutton	Top right of control panel	Initiates LOCAL mode (GCP/ operator commands)
DIS/LOC lamp	In DIS/LOC pushbutton	Indicates digital graphic controller card operating

2.3 TURN-ON PROCEDURE

NOTE

Refer to Section 5 for maintenance information if (a) RUN/SYS lamp does not light following power turn-on; (b) host computer subsequently reports terminal controller defective; or (c) terminal controller operation is suspect for any reason.



80-346-015

Figure 2-1. Terminal Controller Controls and Indicators

To turn the terminal controller on, press the 1 side of the POWER ON/OFF circuit breaker. This action lights the RUN/SYS lamp and applies power to the circuit cards.

Delay timers in the circuit cards allow initial power surges to settle, then initialize the terminal controller in the SYSTEM mode. All peripheral devices are reset, and the GCP performs automatic diagnostic tests to verify operation of the basic terminal controller functions.

If the terminal controller is connected to a host computer that is already operating, the controller automatically transmits a performance status report to the computer. If the host computer is not operating, the computer can receive this status report only by initializing the terminal controller as part of its own turn-on procedure. In either case, the host computer's response to the status report is a function of the host computer application software.

2.4 OPERATING PROCEDURES

The terminal controller has two types of operation:

1. Normal Operation: regular controller functions performed in the SYSTEM or LOCAL mode.

2. Checkout: operator test of controller operation.

2.4.1 NORMAL OPERATING PROCEDURES. After normal turn-on, the terminal controller is in the SYSTEM mode; i.e., under host computer control. Pressing the DIS/LOC pushbutton places the terminal controller in LOCAL mode, under GCP control and operator commands. The terminal controller remains in LOCAL mode until it is placed in SYSTEM mode again as described in paragraph 2.4.1.1.

2.4.1.1 SYSTEM Mode Operation. This mode is established when one of the following occurs:

1. When primary ac power is applied to the terminal controller.

2. When you press the RUN/SYS pushbutton.

3. When the terminal controller is in LOCAL mode and you type S on the keyboard.

4. When the terminal controller is in LOCAL mode and you type 157760G RETURN on the keyboard.

5. When an initialize signal comes from the host computer via the parallel interface or the multiport serial interface.

6. When the terminal controller is in the teletypwriter emulation mode (see paragraph 2.4.2.5) and you press function key F13 on the keyboard or the host computer sends octal code 035 (ASCII control character GS Group Separator).

If the terminal controller is already in SYSTEM mode, it can be initialized again by either of the following:

1. A discrete initialize signal from the host computer via the parallel interface or the multiport serial interface.

2. An IZ (initialize) message from the host computer.

Initialization in the SYSTEM mode automatically causes the built-in diagnostic routines to be performed and the results sent in an error status message to the host computer. The diagnostic routines include GO/NO-GO checks of the graphic controller, display processor, read/write memory, 2-D/3-D coordinate converter (if installed), and either the parallel interface or the multiport serial interface (whichever is the device used for communications with the host computer). The error status message also includes a checksum of GCP stored in read-only memory.

In the SYSTEM mode, responses to all operator actions are determined by the application program of the host computer. Control is exercised and data is transferred by means of messages sent between the host computer and the terminal controller. See the GRAPHIC 8 Programmer's Reference Manual, Sanders document H-80-0444.

The host computer application program accesses all display registers and parameters for organization of display images. The initialization sequence enables the associated keyboards so you can enter commands without special action by the host computer.

The GCP handles all internal display interrupts and operator inputs. The GCP performs all housekeeping required for these events, and sends the host computer a message containing all information needed for operational decisions. However, the host computer can preset the terminal controller to transmit only specified signals under specified conditions.

The GCP processes trackball, forcestick, or data tablet inputs without host computer intervention. The GCP detects all PED (position entry device) inputs and either transmits them to the host computer, or uses them to update the position of a predefined PED identifier symbol on the display. GCP processing of PED symbols is controlled by the host computer application program.

GCP also inserts alphanumeric data from the keyboard into the refresh pattern; you can enter and edit a message without host computer intervention. You complete your entry by pressing the RETURN key, and GCP informs the computer that a new message is ready. The application program indicates how alphanumeric inputs are handled by issuing special commands.

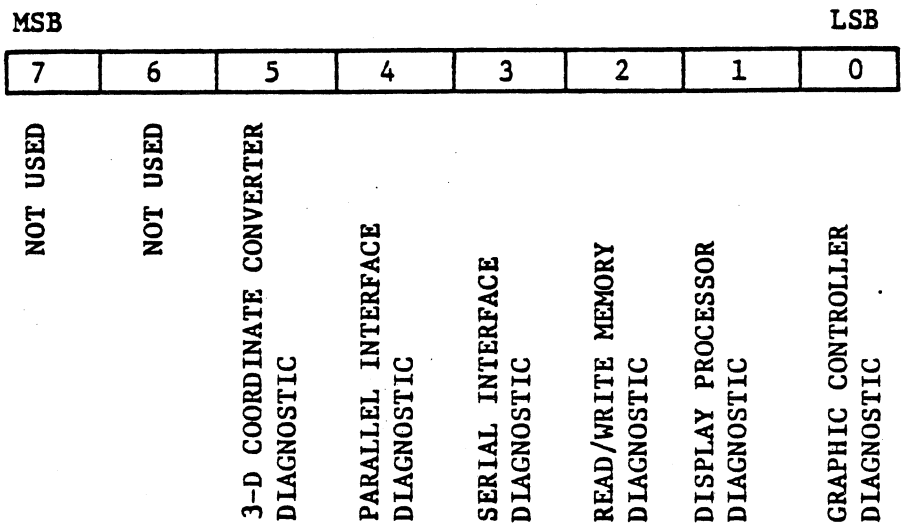
2.4.1.2 LOCAL Mode Operation. After primary power has been applied to the terminal controller, you can initialize the terminal controller in LOCAL mode by pressing the DIS/LOC pushbutton. When you press this pushbutton, the verification test pattern appears on each of the associated display indicators, the terminal controller performs its built-in diagnostic routines, and local mode commands can be executed.

NOTE

When you press the DIS/LOC pushbutton, the built-in diagnostic exercises the complete memory system. For systems containing more than 32K of memory, it may take several seconds before the terminal verification pattern appears. As part of the memory diagnostic, the memory configuration installed in the terminal controller is saved and can be examined if desired. Address 736 contains the RAM configuration word; address 750 contains the ROM configuration word.

2.4.1.3 Verification Test Pattern and Diagnostics. Figure 2-2 shows the verification test pattern that is displayed on each display indicator when the terminal controller is initialized in the LOCAL mode. The pattern remains displayed until terminated by the proper command or until 45 minutes have elapsed since that last performed operation that affected the pattern.

When the system is first initialized in the LOCAL mode, 'XX' appears in the small box in the lower right portion of the pattern. The 'XX' indicates that the code appearing in the same box contains the results of the built-in diagnostic routines that were automatically performed. The diagnostic code is a three-digit octal representation of an eight bit binary code that indicates the results of each diagnostic routine. Bits in the binary code are assigned as follows:



When a diagnostic routine detects a malfunction, the corresponding bit in the error code is set to a 1; if no malfunction is detected, the bit is set to a 0. The octal code displayed in the verification test pattern then tells you the results of all the diagnostic tests. For example, 000 indicates all tests passed, 002 indicates the display processor diagnostic test failed, 030 indicates the serial and the parallel interface diagnostic tests failed, and 077 indicates that all diagnostic tests failed.

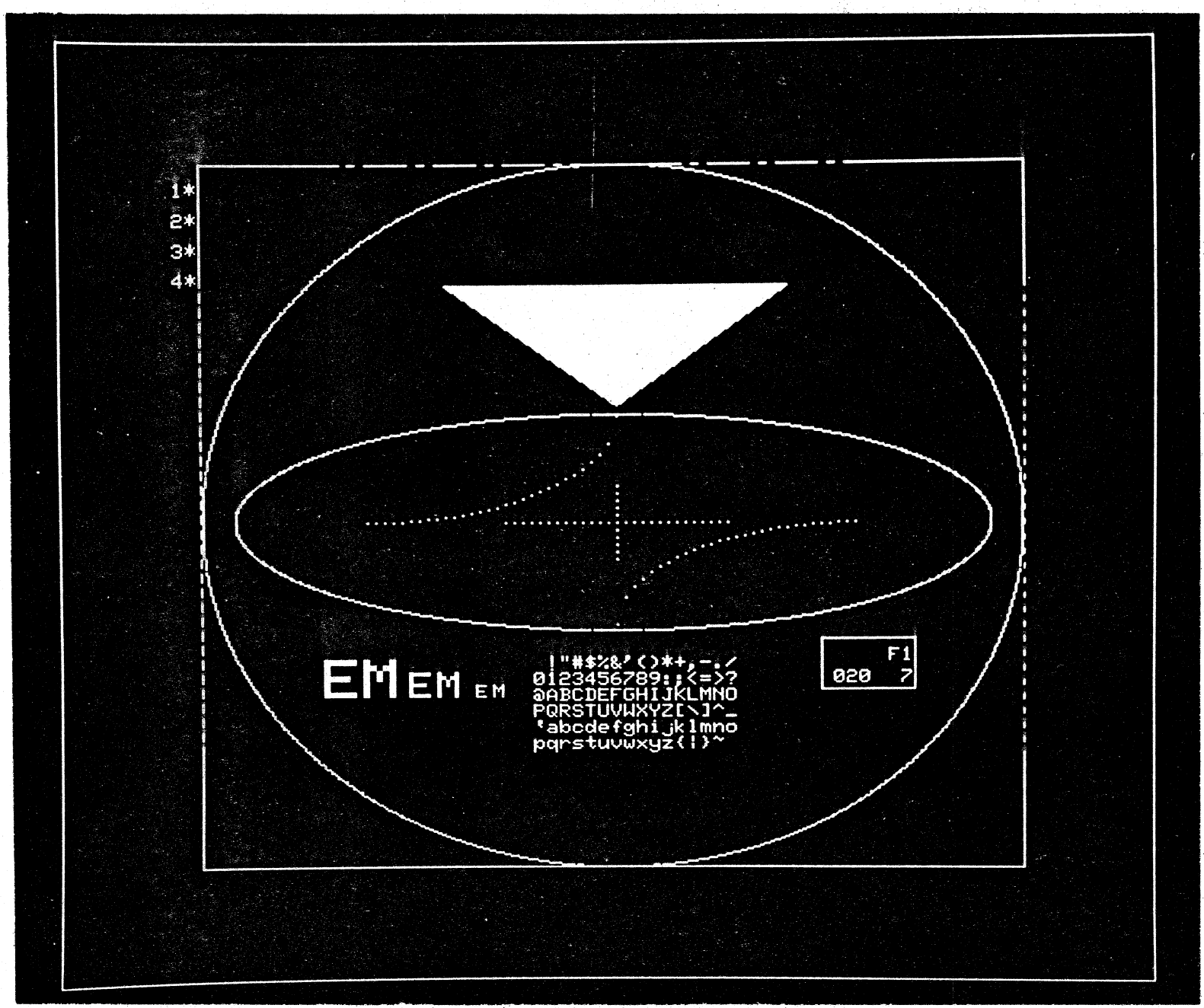


Figure 2-2. Verification Test Pattern

An additional routine performed whenever the GRAPHIC 8 is initialized in the local mode is a checksum calculation based on all GCP stored in read only memory. You can examine the result, which is deposited in memory 500 (octal), as described in paragraph 2.4.2.1.

As soon as the terminal controller receives any input via a serial interface port, the "XX" in the small box is replaced by a code that indicates the port to which the input device is connected. Codes associated with each serial interface port are shown in table 2-2.

When the serial interface port designation is displayed in the small box, the three digit octal code in the box indicates the code last transmitted to the terminal controller. Also, if the code represents a displayable character, the character appears in the upper left corner of the box. If the code does not represent a displayable character, the upper left corner of the box is blank. In systems using SI (shift-in) and SO (shift-out) codes to identify characters in an extended set, the SI character is displayed over the left hand digit of the code and the SO character is displayed over the right hand digit.

The test results box also contains a single-digit real-time clock counter read-out in the lower right corner. This counter increments from 0 through 7 continuously at a 1-Hz rate to confirm operation of the real-time clock timing function.

The numeral in the upper center of the verification test pattern indicates the video controller card to which the display indicator is connected.

Table 2-2. Serial Interface Port Codes

CODE	SERIAL INTERFACE PORT	DEVICE	ASSOCIATED CONNECTOR
F1	3	Keyboard (with function keys)	J5 on multiport serial interface card no. 1
F2	7	Keyboard (with function keys)	J5 on multiport serial interface card no. 2
TT	TTY	Teletypewriter	J2 on ROM and status card
S1, S5	1 or 5	Any	J2 or J3 on multiport serial interface card no. 1 or no. 2
HC	5	Hardcopy	J3 on multiport serial interface card no. 2.

NOTE

No indicator code is provided for ports 4 or 8. These ports are normally used for PEDs which have separate indicators on the test pattern.

Trackball (or forcestick) indicators appear in the upper left corner of the verification test pattern. The "1*" indicator is associated with the device normally connected to serial interface port 4 (J6 on multiport serial interface card no. 1) while the "2*" is associated with the device normally connected to serial interface port 8 (J6 on multiport serial interface card no. 2). These indicators are always displayed on the test pattern regardless of whether or not a trackball or forcestick is connected to the system. If a trackball or forcestick is connected to port 4 or 8, it can be manipulated to move its associated indicator about the screen of the CRT as desired. (See paragraph 2.4.1.5 for data tablet.)

2.4.1.4 Hardcopy Generation. To make a hardcopy of a displayed pattern:

1. Press function key F0 on the keyboard; this action freezes the display.

2. Operate the hardcopy unit manually (see the operator's manual for your hardcopy unit).

2.4.1.5 Data Tablet Testing. You can test the data tablet by pressing function key F1. This causes the 1* and 2* trackball/forcestick indicators to change to 1# and 2#. The 1# and 2# symbols indicate that all messages received via ports 4 and 8 are in data tablet format. (Data tablet messages consist of 10 characters messages, whereas the trackball and forcestick generate 2-character messages.) When you press the data tablet pen switch and move the pen along the active area of the data table surface, the appropriate cursor symbol (1# or 2#) moves at a rate proportional to the movement of the pen. The 1# symbol is associated with the data tablet connected to port 4 and the 2# symbol is associated with the data tablet connected to port 8.

NOTE

Successively pressing function key F1 causes the terminal verification pattern to switch from processing data tablet messages to trackball/forcestick messages and vice versa.

2.4.2 LOCAL MODE COMMANDS. After the GRAPHIC 8 has been initialized in the LOCAL mode and the verification test pattern is no longer required, you can terminate the pattern by pressing the RETURN key on the keyboard. The pattern then disappears and the letters "BØ M" are displayed in the center of the CRT screen as an indication that the system is in the LOCAL MONITOR mode. At this point, you can perform any of several operations that let you monitor or debug a program, transfer control, or communicate with the host computer.

NOTE

Commands are executed when you press the RETURN key on the keyboard.

The following paragraphs discuss commands that can be executed when the system is in the LOCAL MONITOR mode. Table 2-3 is a summary of the commands.

Table 2-3. Local Mode Command Summary

KEYBOARD ENTRY	OPERATION
RETURN	Executes LOCAL mode command or returns system to LOCAL MONITOR level.
nnnnnn/	Displays contents of memory address nnnnnn (octal).
/	Increments memory address counter by two and displays address contents.
^ or ↑	Decrements memory address counter by two and displays address contents.
Bn	Select different memory bank. (BØ 0-32K; B1 32-64K; B2 64-96K; B3 96-128K; and B4 16-32K RAM).
S	Transfers GRAPHIC 8 to SYSTEM mode operation.
T RETURN	Transfers to the verification test pattern.
L RETURN	Loads memory from paper tape reader.
nnnnL RETURN	Loads selected option from expansion module
U RETURN	Unload all options.
O RETURN	Display status of all options loaded.
Q	Decrements contents of display processor Q register by two and displays result. Used with diagnostics to indicate address at which display processor halted.
nnnnnnD RETURN	Directs graphic controller to display refresh file beginning at address nnnnnn (octal).
nnnnnnG RETURN	Transfers control of display processor to program beginning at memory address nnnnnn (octal).
Y RETURN	Calls teletypewriter emulation program. After entering emulation program, function key F0 clears CRT screen. Function key 1 selects full or half duplex operation; receipt of octal code 035 from the host computer or pressing function key F13 transfers GRAPHIC 8 to SYSTEM operating mode.
RUB OUT	Deletes last octal entry from keyboard.

2.4.2.1 Memory Commands. You can display the content of a memory location by typing the octal address (typing of leading zeros is not required) followed by a slash (/). As soon as you type the slash, the content of the memory location is displayed immediately to the right of the address. You can examine successive memory locations by simply pressing the slash key. Each time you press the slash key, the memory address is incremented by two and its content displayed immediately to the right of the slash.

After you have used the slash key to examine the content of a memory location, you can use the up arrow (↑ or ^) key in a similar manner to examine preceding memory locations. Each time you press the up arrow key, the memory address is decremented by two and its content displayed immediately to the right of the slash.

You can change the content of a memory location after you have examined it by typing the new data (typing of leading zeros is not required) before pressing the slash or up arrow key. The new data is displayed to the right of the old data and is automatically substituted when the slash or up arrow key is pressed.

You can examine or change memory locations in other banks via the bank (B) select command. Typing BØ, B1, B2, B3, or B4 changes the memory bank selection to bank Ø, bank 1, bank 2, bank 3, or bank 4 respectively. Below is a table representing the associated virtual and physical addresses for each bank.

Bank Number	Virtual Address	Physical Address	Pages
0*	000000-177777	000000-177777	00-07
1	000000-177777	200000-377777	10-17
2	000000-177777	400000-577777	20-27
3	000000-177777	600000-777777	30-37
4*	100000-177777	100000-177777	04-07

NOTE

*Addresses in the range of 100000-177777 (pages 4, 5, 6, and 7) for bank Ø correspond to ROM and I/O device registers. Addresses in the range of 100000-177777 for bank 4 correspond to RAM.

You can return to the monitor level by pressing the RETURN key. When you press this key, any specified memory content change is completed and the system returns to monitor level as indicated by letters "BO M" displayed at the center of the CRT screen.

2.4.2.2 Displaying a Refresh File. When the system is in the local monitor mode, you can display the contents of a refresh file by typing the starting address of the file (in octal notation) followed by a "D" and then pressing the RETURN key. This command instructs the digital graphic controller to display the entire refresh file that begins at the specified address. Display of the refresh file continues until you press RETURN key again, at which time the system returns to the local monitor level. This command is subject to the bank argument presently displayed.

2.4.2.3 Transfer of Program Control. You can transfer program control from local monitor level to any desired address location in bank Ø by typing the address location in octal notation followed by a "G" and then pressing the RETURN key. The display processor then executes instructions beginning with the instruction at the specified address. Any further operations depend on the program in which control is transferred.

2.4.2.4 Transfer to System Mode. To transfer to the system mode of operation from monitor, level, type "S". This command has the same effect as pressing the RUN/SYS pushbutton on the terminal controller. After transferring to the system mode, operation in the local mode can be reestablished only by a message from the host computer, or by pressing the DIS/LOC pushbutton on the terminal controller, or by pressing CONTROL and SHIFT and RETURN on the keyboard.

2.4.2.5 Teletypewriter Emulation. For purposes of communicating with a host computer, the GRAPHIC 8 can be made to emulate the functions of a teletypewriter. In this mode, the keyboard operates like the keyboard of a teletypewriter and the display indicator serves as the printout device. Scrolling of data on the display indicator is handled on a half-page basis. That is, when the CRT screen is full, the top half of the data is deleted from the display and the bottom half of the data moves up to take its place.

If a parallel interface card is installed in the terminal controller, the graphic control program assumes that communications with the host computer are to be handled over the parallel interface. In this case, teletypewriter emulation signals are transmitted in parallel using only the low order byte (bits 0-7) of the 16-bit interface. If a parallel interface card is not installed, a standard 8-bit serial interface via serial interface port 1 is assumed. In either case, bit 7 is always equal to zero.

You enter the emulation program from the monitor level by typing the letter "Y" followed by RETURN. Full-duplex or half-duplex emulation may then be selected by pressing function key F1, which changes the selection each time it is pressed. The type of emulation selected is indicated by the "TTY F" (full duplex) or "TTY H" (half duplex) that is displayed at the top of the CRT screen at all times during emulation. You can switch between full and half duplex operation at any time during emulation by pressing function key F1. Pressing function key FØ during teletypewriter emulation clears the CRT screen.

Exit from the teletypewriter emulation program occurs when octal code 035 (ASCII control character GS Group Separator) is received from the host computer. This code, which can also be generated by pressing function key F13, immediately causes the GRAPHIC 8 to transfer to the SYSTEM mode of operation. Return to the LOCAL MONITOR level can be achieved only by a command from the host computer, or by pressing the DIS/LOC pushbutton on the terminal controller, or by pressing CONTROL and SHIFT and RETURN on the keyboard.

2.4.2.6 Additional Local Mode Commands. Additional commands that you can use when the GRAPHIC 8 is in the LOCAL mode at the monitor level are the L, U, O, T, Q, and RUB OUT commands. The L command enables the memory to be loaded from a paper tape reader connected to the terminal controller. After the tape has been placed in the reader, loading is initiated by typing the letter "L" followed by RETURN.

NOTE

A paper tape reader may be connected to multiport serial interface card ports 1, 2, or 3 or to the serial interface port on the ROM and status logic card.

You also use the L command to load in options from the expansion module. The option command format is as follows:

nnnnL RETURN

where nnnn is the option number. Valid option numbers are in the ranges of 1 to 3777 and 4001 to 7777.

NOTE

The optional expansion module can store a variety of option types.

The U command is used to unload all options. Typing "U" followed by RETURN unloads all options.

The 0 command is used to detect the presence and status of all loaded options. Typing 0 followed by RETURN causes the display of the first option loaded. Successively pressing the RETURN key causes the display of all other options loaded. The option status is displayed in the following format.

nnnn ss

where nnnn is the option number and ss is the option status

The option status code is as follows:

00	Detected but unloaded
01	Unloaded, checksum error (local)
11	Unloaded, checksum error (system)
02	Unloaded, checksum OK, hardware not present (local)
12	Unloaded, checksum OK, hardware not present (system)
03	Unloaded, checksum OK, self-test = no go (local)
13	Unloaded, checksum OK, self-test = no go (system)
04	Loaded, checksum OK, self-test = go (local)
14	Loaded, checksum OK, self-test = go (system)

You use the T command to recall the verification test pattern when the system is at the local monitor level. This command is executed by typing the letter "T" followed by RETURN. The effect is the same as pressing the DIS/LOC pushbutton on the terminal controller. Pressing RETURN a second time causes the system to return to the monitor level.

The Q command is a special command used for diagnostic and debugging purposes. Whenever a HALT instruction is executed by the display processor, the content of the program counter is stored in the Q register of the display processor. After you have reinitialized the system by pressing the DIS/LOC pushbutton on the terminal controller, you can use the Q command to display the address at which the display processor halted. The Q command is executed by typing the letter "Q". This causes the content of the Q register to be decremented by two and the result displayed to indicate the address of the HALT instruction. Note that the Q command always decrements the content of the Q register by two and displays the result. The result, however, is only meaningful immediately following initialization in the LOCAL mode after a HALT instruction has been executed. After using a Q command, pressing RETURN returns the system to the local monitor level.

The RUB OUT command provides a means of correcting erroneous entries from the keyboard. At any time before a command is executed, pressing RUB OUT causes the last keystroke entry to be deleted. An additional entry is deleted each time the RUB OUT key is pressed.

2.4.3 STANDARD TRANSFER TABLE. ROM addresses 157700 through 157770 (octal) constitute a standard transfer table for certain routines of the graphic control program (GCP). Information identifying the version of GCP installed in the ROM is also contained in these addresses. When the GRAPHIC 8 is operating in the LOCAL mode, you can examine the contents of locations containing information by typing the address of the location followed by a slash. To transfer to one of the GCP routines, the G command should be used as described in paragraph 2.4.2.3. Refer to H-80-0444 for the standard transfer table.

NOTE

When the GRAPHIC 8 is operating in the SYSTEM mode, transfer to one of the GCP routines can be accomplished by using a host-to-GRAPHIC 8 TK message. Refer to H-80-0444 for details.

2.4.4 OPERATOR PERFORMANCE CHECKS. If you suspect a malfunction in the terminal controller or any of its peripherals (or if the host computer reports the terminal controller to be defective), you can perform the following procedure to verify basic system operation. If you do not get the described results, refer to Section 5.

1. Press the DIS/LOC pushbutton to initialize LOCAL mode. Confirm that the verification test pattern (figure 2-2) is present on the display indicator.

2. Confirm that the test results box shows a 000 value (code for all tests passed), with the "XX" error word code displayed in the upper right corner of the box.

3. Confirm that the seconds counter at the lower right corner of the test results box runs continuously through an 8-count cycle (0-7).

4. Confirm that the letter "T" appears in the upper left corner of the test results box.

5. Press one or more alphanumeric keys on the keyboard. Confirm that:

   a. The alphanumeric symbol replaces the letter "T" in the upper left corner of the test results box.

   b. The applicable ASCII value in octal format replaces the test results value below that symbol.

   c. The appropriate source code (table 2-2) replaces the "XX" code.

6. Confirm that a full library of alphanumeric and special symbols is displayed at the lower center of the verification test pattern.

7. Confirm that three different sized sets of "EM" letter pairs are displayed in the lower left quadrant of the verification test pattern.

8. Confirm that the line structure of the overall test pattern conforms with the pattern shown in figure 2-2 with respect to the following:

   a. The corners of the displayed squares are clearly defined right angles, with uniform intensity through the points of congruence in all four corners.

   b. The central portions of the sides of the inner square represent different line structure patterns: solid (bottom), dotted (right), dashed (left), and centerline (top).

   c. The circle and ellipse patterns are smooth and unbroken; the dotted cross and arc segments are as shown in figure 2-2.

   d. The triangle is smooth and complete, as shown in figure 2-2.

9. Confirm that the number of the video controller card associated with a specific display indicator appears in the upper center of the pattern, continuously blinking on and off.

10. Confirm that the trackball/forcestick/data tablet identifier symbols are initially presented in the upper left corner of the pattern, with the applicable symbol moving as appropriate for any PED displacement inputs.

11. In the case of a four-color display, confirm that the proper colors are displayed.

2.5 TURN-OFF PROCEDURE

To turn off the terminal controller, press the O side of the POWER ON/OFF circuit breaker.

SECTION 3

THEORY OF OPERATION

3.1 GENERAL

This section contains the theory of operation for the terminal controller functional circuits. Topics presented are the terminal controller signal/bus structure, and block-diagram level discussions of each standard circuit card assembly. Unique circuit card options are covered in separate manuals (see Appendix A).

3.2 SIGNAL/BUS STRUCTURE

Terminal controller inputs are provided as digital signals from a host computer or peripheral equipment. Except for PHOTOPEN inputs, all inputs are applied to the terminal controller circuits via edge-mounted connectors on the front of one or more interface cards located in the terminal controller card cage.

Terminal controller outputs are applied either as digital signals through the same edge mounted connectors or as analog signals to the associated CRT display indicators (or hard copy unit) through BNC connectors on the front of the video controller card. All interconnections among the various circuit card assemblies are accomplished through backplane wiring (see backplane wiring diagram in H-81-0097). For convenience, backplaning connections common to groups of cards are called buses. The three main terminal controller buses are: the processor bus, raster bus, and power bus.

3.2.1 PROCESSOR BUS. The processor has comprises backplane wiring connections common to the display processor circuit card and all circuit cards that interface with the display processor to perform the digital analysis that creates display files. These cards (the processor subsystem) are located in card cage slots 1A1XA1 through 1A1XA7. The ROM and status card and the digital graphic controller card both have discrete-line backplane connections to circuit cards in the graphic subsystem and therefore occupy specific locations: 1A1XA6 and 1A1XA7, respectively. All other processor subsystem cards interface through the common processor bus connections, and can occupy any card cage slot depending on the interrupt/bus control priority. Table 3-1 lists the standard cards in their preferred priority/arrangement.

Table 3-2 lists the processor bus signals and identifies their basic functions. For convenience, these signals are discussed as three separate buses: the 18-line processor address bus (AD00-B through AD17-B), the 16-line processor data bus (DA00-B through DA15-B), and the 25-line processor control bus.

Table 3-1. Processor Subsystem Cards, Preferred Priority Arrangement

CARD CAGE SLOT	CIRCUIT CARD ASSEMBLY
1A1XA1	Digital Option
1A1XA2	64K Read/Write Memory No. 2 (Optional)
1A1XA3	64K Read/Write Memory No. 2 (Optional)
1A1XA4	Multiport Serial Interface
1A1XA5	Display Processor
1A1XA6	ROM and Status
1A1XA7	Digital Graphic Controller
1A1XA8 through 1A1XA16	Video Controllers and Mapping Memories
1A1XA17	Timing Module

Table 3-2. Processor Bus Signals

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
		PROCESSOR ADDRESS BUS	
57 thru 74	ADnn-B	Address bus bits (AD00-B thru AD17-B)	Selects circuit in which an operation is to be performed.
		PROCESSOR DATA BUS	
13 thru 28	DAnn-B	Data bus bits (DA00-B thru DA15-B)	Carries 16-bit data or control code to or from circuit that was addressed
		PROCESSOR CONTROL BUS	
4, 5, 6*	INLn-B	Interrupt levels 5, 6, 7	Three priority levels for interrupt selection; set by jumpers on each card

*All listed signals are common to all processor subsystem card slots 1A1XA1 through 1A1XA7, except that asterisked signals do not connect to graphic controller 1A1XA7. The asterisked signals pertain mostly to program interrupt handshaking signals. Graphic controller 1A1A7 does not interrupt the processor program directly. Certain of its operations can interrupt the program through status connections to ROM and status card 1A1A6.

Table 3-2. Processor Bus Signals (Cont)

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
7*	IREQ-D	Interrupt request pulse	Produced by display processor at end of each instruction cycle to let any card that is ready to interrupt the program activate its INLn-B output
8*	IENA-D	Interrupt enable	Produced by display processor in response to INLn-B signal to let the requesting card generate an interrupt
9*	IADV-B	Interrupt address valid	Produced by interrupting card to let display processor read interrupt trap address; response to IENA-D
10, 11, 12, 3*	DEV-nB	Device code levels 0, 1, 2, 3 (BCD)	Identifies (by unique BCD code) the card that has control of the bus
31	CLOK-F	10 MHz clock	Master clock for GRAPHIC 8 system
33	BUSB-B	Bus busy	Indicates that bus is under control of some processor subsystem card
36	GRAI+B	Grant input	Lets receiving card gain control of bus (comes as GRAO+B from higher priority card)
35*	GRAO+B	Grant output	Lets lower priority card gain control of bus (goes to that card as GRAI+B)
37	WRIT-B	Write/read control	Activated by card that controls the bus. Low indicates that controlling card is writing to addressed card. High indicates that controlling card is reading from addressed card
38	ADRV-B	Address valid	Indicates ADnn-B address lines are stable; enables address decoder and related logic on addressed card

Table 3-2. Processor Bus Signals (Cont)

CARD PIN	MNEMONIC	SIGNAL NAME	FUNCTION WHEN ACTIVE
39	MEMA-B	Memory acknowledge	Indicates that addressed card has accepted data or has placed data on DAnn-B lines
40*	BYTE-B	Byte/word control	Allows high order byte to be carried on low order byte lines of data bus
41	REST-B	Reset	Resets all circuit card assemblies
42*	BTOM-M	Bus timeout	Indicates that requested data transfer was not completed within normal instruction interval
43*	SYST-B	System mode	Initiates SYSTEM mode
44*	LOCA-B	Local mode	Initiates LOCAL mode
45	TORN-U	Turn-on	Power-up initialize command; activates REST-B sequence
47*	DPRN-D	Display processor run	Lights lamp in SYS/RUN pushbutton
50*	50DB-F	50 kilobaud clock	50 kilobaud I/O clock pulse-train

3.2.2 RASTER BUS. The raster bus comprises backplane wiring connections common to the digital graphic controller card and all circuit cards that interface with the digital graphic controller card to develop digital signals that control the image presented on the display indicator or hardcopy unit. These raster subsystem cards are located in card cage slots 1A1XA8 through 1A1XA17.

Functionally, the term "raster bus" pertains to the digital graphic controller outputs to other raster subsystem circuit cards. This bus includes a 16-bit address bus that carries signals AGxx+H; a 12-bit data bus that carries signals DBxx+H; and certain handshaking signals between the digital graphic controller and the mapping memory. However, the raster bus also carries signals between the video controllers and their respective mapping memories, including an 11-bit address bus that carries signals AVxx+V; an 8-bit data bus that carries signals DCxx-N; and a number of handshaking and timing signals.

3.2.3 POWER BUS. The power bus comprises backplane wiring connections that carry operating power to all card cage slots. Power is distributed through redundant pins to facilitate current flow to and from each card. Table 3-3 lists the common power bus connections.

Table 3-3. Power Bus (Common to All Cards)

CARD CAGE PINS	BUS MNEMONIC	SIGNAL/NAME/FUNCTION
1*, 2* 29, 30 53, 54, 13+, 14+, 71+, 72+	DRET-	Digital ground return (common circuit ground connections on all cards as return for circuits receiving P05V+ power.)
55, 56	P05V+	Positive 5 volts DC
77*, 78*, 97*, 98*, 91+, 92+	ARET-	Analog ground return (common circuit ground for circuits receiving N15V- and/or P15V+ power.)
93, 94	N15V-	Negative 15 volts DC
95, 96	P15V+	Positive 15 volts DC

*These redundant DRET- connections apply only to slots 1A1XA1 through 1A1XA6 in the processor subsystem.

+These redundant DRET- connections apply only to slots 1A1XA8 through 1A1XA17 in the raster subsystem.

3.3 PROCESSOR BUS CONTROL AND TIMING

To perform a program operation, a circuit card seizes control of the processor bus either to obtain data from that bus or to pass data via that bus to some other circuit card. This process involves a handshaking sequence controlled by a grant-signal connection, running as a series string through all cards in the processor subsystem (slots 1A1XA1 through 1A1XA7). This connection configuration means that the GRAO+B (grant output) signal at pin 35 of any slot is connected as the GRAI+B (grant input) signal at pin 36 of the next-higher numbered slot. This connection configuration continues along the card cage from slot 1A1XA1 (highest priority) to slot 1A1XA7 (lowest priority).

A card obtains bus control only when its GRAI+B input is active (high logic level). This normal condition is established by a pullup resistor on the GRAI+B input line of each card, holding that input active unless it is forced low by a preceding higher-priority card that has requested bus control. A card requests bus control by deactivating its GRAO+B output, thereby disabling the GRAI+B input of the next card in sequence which, in turn, lowers the GRAO+B output from that card. The priority string thus begins with the first non-memory card installed in the card cage and continues through digital graphic controller card 1A1A7 (which has lowest priority).

3.3.1 BUS CONTROL LOGIC. Figure 3-1 is a simplified logic diagram of a typical bus-grant circuit which allows any processor bus circuit card to request and gain control of the bus unless inhibited by a higher-priority card. A bus-grant circuit similar to the one shown in figure 3-1 is contained on all processor subsystem cards except the read/write memory cards (which have through-line connections). The exact circuit configuration may differ slightly on individual cards, but the functions illustrated are valid in all cases.

When a function circuit on any card is set up to gain processor bus control, that circuit generates an internal GRAR+ (grant request) signal which is loaded into the GRAB buffer flip-flop by the next 10-MHz CLOK-F pulse. The resultant GRAB $\overline{Q}$ output inhibits the GRAO+ gate, deactivating the GRAO+B output, which serves as the GRAI+B input to the next card on the bus. That low GRAI+B input then inhibits the corresponding GRAO+ gate on that next card, deactivating its GRAO+B output to the next card in sequence, and so on.

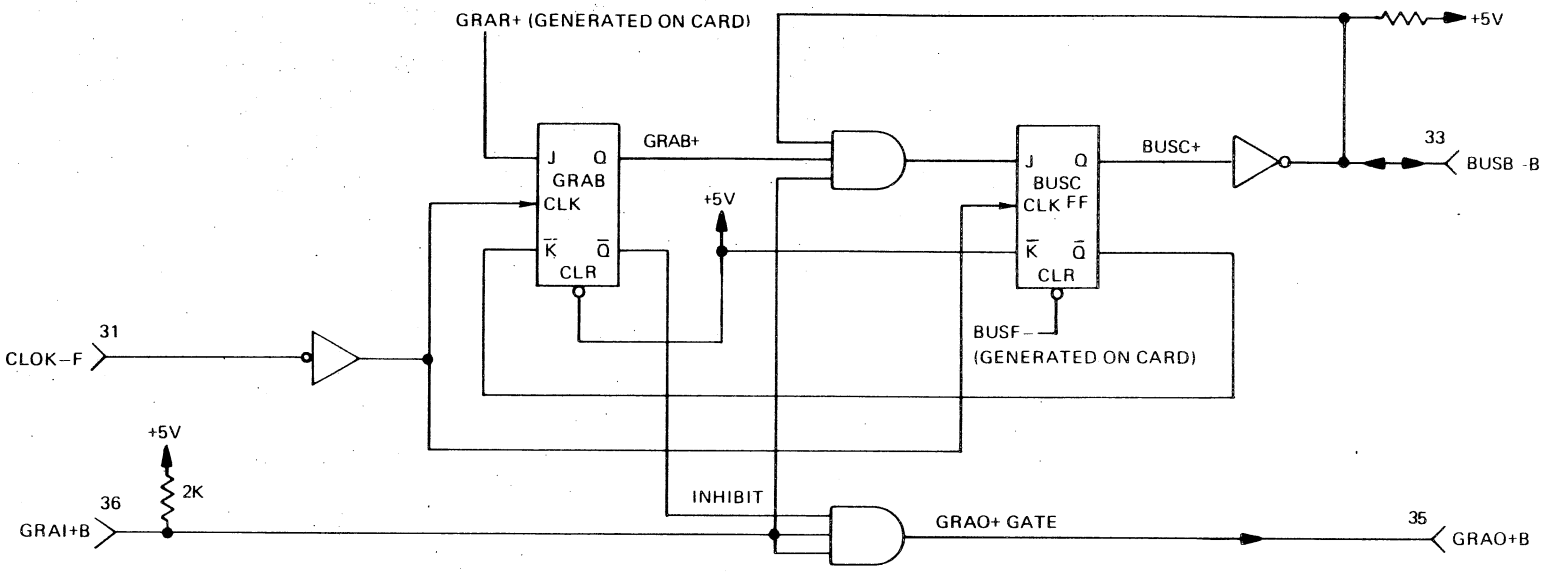
If the GRAI+B input to the card requesting bus control is high and the BUSB-B (bus busy) line currently is not active, GRAI+ gates the GRAB+ flag signal to the BUSC flip-flop, which loads that signal on the next CLOK-F pulse. The resulting BUSC+ output is inverted to activate the BUSB-B control line, informing all other cards that the processor bus is currently under control. At the same time, the BUSC $\overline{Q}$ output is applied as the $\overline{K}$ input of the GRAB flip-flop, resetting that flip-flop on the next CLOK-F pulse (third pulse after GRAB+ is generated). This event removes the inhibit from the GRAO+ output gate, reestablishing GRAO+B output as a high logic level. BUSB-B remains active, however, until the BUSC flip-flop is cleared by a low BUSF- (bus finished) signal. BUSF- is generated internally in the card's function circuit when bus control can be relinquished (i.e., after completion of a read or write cycle).

3.3.2 BUS CONTROL TIMING. Figure 3-2 shows the timing of a typical bus control sequence. In this diagram, signals generated by the display processor are suffixed D, while signals generated by the digital graphic controller are suffixed H.

In figure 3-2, the display processor and the graphic controller simultaneously attempt to gain bus control. Thus, GRAR+D and GRAR+H go high simultaneously, setting the GRAB flip-flops on the two cards. The cross-hatching of the two GRAR+ signals in figure 3-2 designates the periods in which they can be active with respect to the CLOK-F pulse train during the particular bus sequence.

Because of its higher priority location on the bus, the display processor gains bus control first. When the display processor's GRAB flip-flop is set, the resultant low GRAO+B output from that card applies a low GRAI+B to the graphic controller card, thereby inhibiting the conditioning gate for the BUSC flip-flop on that card and preventing that flip-flop from activating the BUSB-B output. The grant ripple timing shown in the GRAO+/GRAI+ signals represents an allowance for gate delays along the bus.

After the GRAB flip-flop on the display processor card is set, the BUSC flip-flop on that card is set by the next CLOK-F pulse, and the BUSB-B output goes low. Internally, the BUSC- signal gates the address of the processor subsystem card that is to be accessed onto the ADnn-B processor address bus.



NOTES: 1.

SIGNAL	FUNCTION (TRUE STATE)
GRAR+ (GRANT REQUEST)	INITIATES BUS REQUEST.
GRAB+ (GRANT REQUEST BUFFER)	SYNCHRONIZES BUS REQUEST.
BUSC+ (BUS CONTROL)	LATCHED GRAB+ ENABLED BY TRUE GRAI.
BUS-B (BUS BUSY)	DISABLES BUS CONTROL UNTIL USAGE IS COMPLETED (HERE OR EXTERNAL).
BUSF- (BUS FINISHED)	TERMINATES BUS CONTROL
GRAI+ (GRANT INPUT)	BUS CONTROL ENABLE FROM HIGHER PRIORITY MODULE.
GRAO+ (GRANT OUTPUT)	BUS CONTROL ENABLE TO LOWER PRIORITY MODULE

2. ALL SIGNALS INTERNAL EXCEPT GRAI+B, GRAO+B, BUSB -B, CLOK-F. BUSB-B IS BIDIRECTIONAL INTERNAL, SOMETIMES EXTERNAL; CLOK-F IS INTERNAL ON ROM AND STATUS CARD.

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Figure 3-1. Bus Grant Circuit, Simplified Diagram

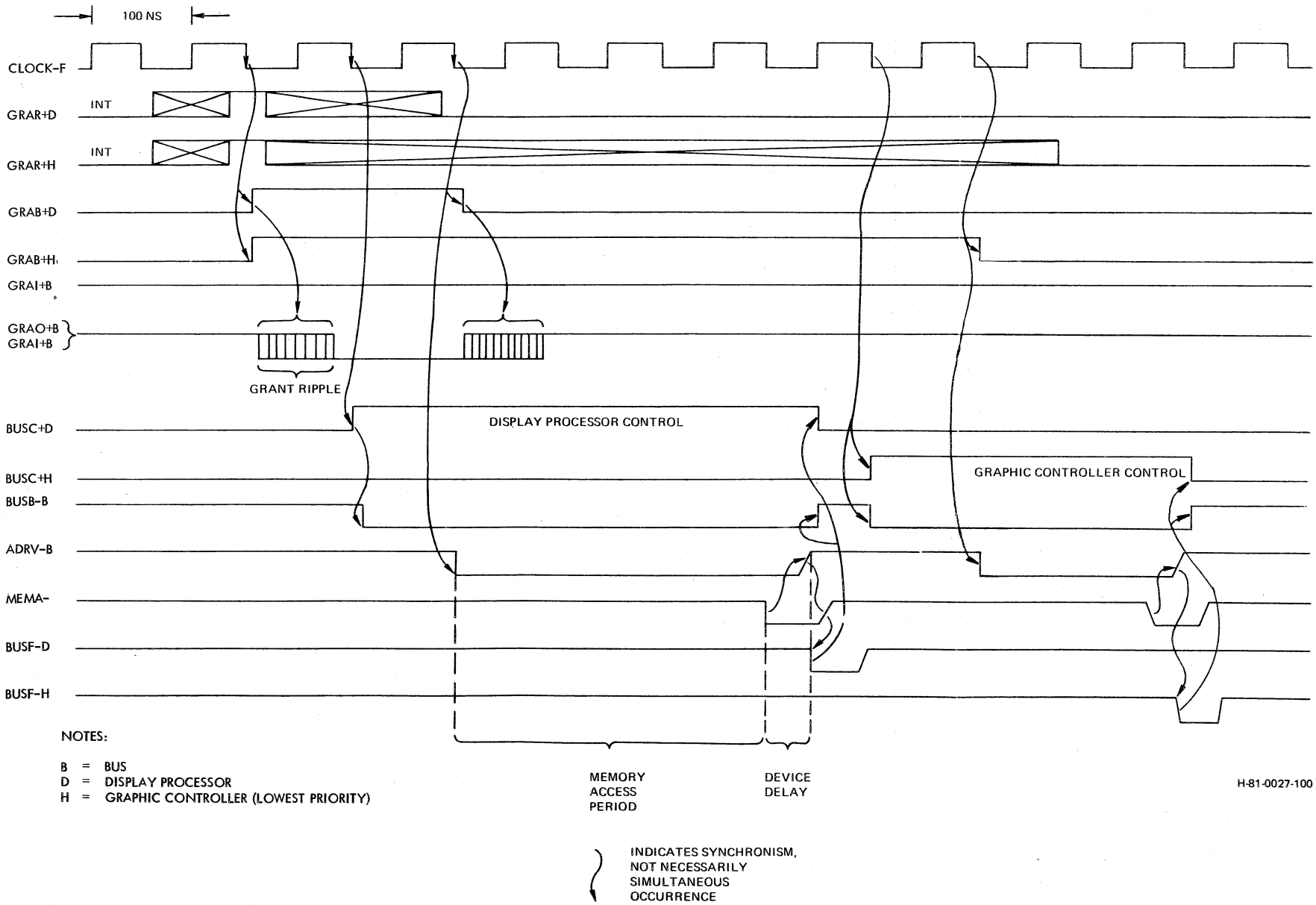

Figure 3-2. Processor Bus Timing

The display processor then generates a low ADRV-B (address valid) output. The delay between activation of BUSB-B and activation of ADRV-B is approximately 100 nanoseconds (i.e., ADRV-B is produced by the same CLOK-F pulse that clears the GRAB flip-flop). ADRV-B initiates operation within the addressed device (read/write memory, ROM and status, interface, or the digital graphic controller).

The addressed device responds by generating a low MEMA-B* (memory acknowledge) signal. The period between activation of ADRV-B and activation of MEMA-B is a function of the addressed device card and can range from a few hundred nanoseconds to seven microseconds. In a READ operation, MEMA-B indicates that the addressed device has placed valid data on the DAnn-B processor data bus. In a WRITE operation, MEMA-B indicates that the addressed device has taken data from the DAnn-B bus. Activation of MEMA-B terminates ADRV-B, whose active period is a function of the addressed device circuit. Following activation of MEMA-B (and, in the case of a read operation, following acceptance of data from the bus), the display processor generates an internal BUSF- (bus finished) signal. This signal clears the BUSC flip-flop in the display processor, terminating BUSB-B and relinquishing bus control.

When the display processor's GRAB flip-flop clears, the GRAI+ input to the digital graphic controller goes high, but the active BUSB-B signal continues to inhibit the conditioning gate for the BUSC flip-flop in the digital graphic controller card (see figure 3-1). If the GRAR+H signal is still active (or has become active again), deactivation of the BUSB-B signal at the end of the display processor's control cycle permits the BUSC flip-flop to be set by the next CLOK-F pulse (see figure 3-2). This condition initiates a digital graphic controller sequence, letting the following CLOK-F pulse set the BUSC flip-flop in the digital graphic controller to reactive the BUSB-B signal. These conditions remain in effect until the digital graphic controller completes its function and activates its BUSF-H to clear its BUSC flip-flop, releasing the BUSB-B processor control line once more.

3.3.3 INTERRUPT LOGIC. Figure 3-3 is a simplified diagram of the interrupt logic contained on all processor subsystem cards that can interrupt the program. The interrupt logic on different cards varies in detail, but the functions shown are common. The interrupt logic operates in conjunction with the bus grant circuit. The associated bus grant circuit is repeated in figure 3-3 to show its control of interrupts. A simplified timing diagram is also included to show approximate time relationships.

A card set up to interrupt the program first generates an initial, high-level interrupt request signal or flag. This flag is the conditioning input to the INTERRUPT flip-flop. Except for a sync-link condition, all interrupts are program-maskable, and the mask must be enabled before the interrupt flag can be generated.

At the end of every instruction cycle, the display processor activates the IREQ-D (interrupt request) control line to sample all interrupt logic circuits to determine their interrupt request status. On any card which has an active interrupt-request flag, IREQ-D both sets of the applicable INTERRUPT flip-flop and gates the resultant INLn-B (interrupt level) signal pulse from the card. In figure 3-3, the INTERRUPT flip-flop activates INL7-B, the highest of three jumper-selectable priority levels.

*MEMA-B (memory acknowledge) is a general response/acknowledge signal, generated by any addressable device/register on the bus. It is not limited to memory accesses.

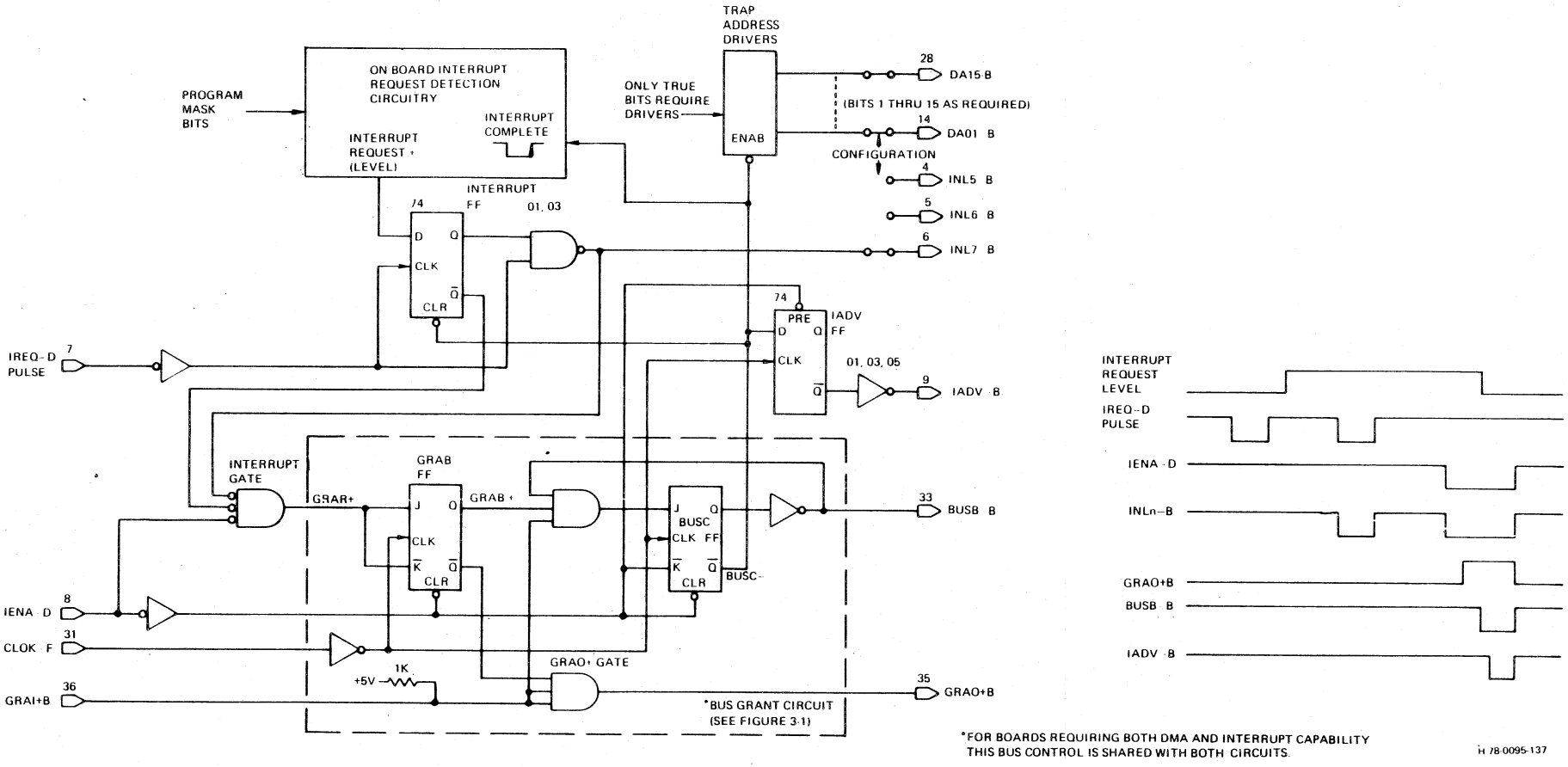

Figure 3-3. Interrupt Logic and Timing

The display processor senses all INLn-B signals simultaneously. If the display processor's program status word (PSW) determines that the interrupt being requested is of a higher priority than the current program operation, the PSW enables an interrupt sequence by (a) forcing the highest activated priority INLn-B lines low (if more than one went active) and (b) activating the IENA-D (interrupt enable) control line to enable the GRAB flip-flop on the card. These conditions (INTERRUPT flip-flop set, INLn-B reactivated, and a low-going IENA-D signal) enable the INTERRUPT gate, activating the GRAR+ flag to the GRAB flip-flop. This flip-flop is set by the next CLOK-F pulse, and its GRAB $\overline{Q}$ output disables the GRAO+ gate to deactivate the GRAO+B output from that card, thus disabling all following lower-priority cards.

If the processor bus is not busy (BUSB-B is high), the conditioning gate is enabled for the BUSC flip-flop on that card, which is set by the next CLOK-F pulse. This, in turn, activates the BUSB-B control line to all other cards on the processor bus, while the low $\overline{Q}$ BUSC flip-flop output enables trap address drivers on the card. These drivers then place the applicable trap address (usually a ROM output accessed by the same signal conditions that caused the original interrupt-request flag) on the DAnn-B data bus for transfer to the display processor as a program branching command. Setting the BUSC flip-flop also clears the INTERRUPT flip-flop and initiates an interrupt complete condition within the interrupt request circuit, deactivating the interrupt-request flag. When the following CLOK-F pulse appears (approximately 10 nanoseconds after BUSB-B goes active), the low $\overline{Q}$ BUSC flip-flop output is loaded into the IADV flip-flop, sending a low IADV-B (interrupt address valid) signal to the display processor as a command to read the trap address. After accepting the trap address, the display processor deactivates IENA-D, clearing the GRAB and BUSC flip-flops to terminate the interrupt cycle on the applicable circuit card.

The display processor then handles the interrupt.

3.4 READ/WRITE MEMORY

This paragraph covers the following versions of the large memory card:

Model	Part No.	Description
7704	1089724G1	64K read/write memory cca
7703	1089724G2	32K read/write memory cca
7702	1089724G4	16K read/write memory cca

The G2 and G4 configurations are depopulated versions of the G1 configuration.

3.4.1 PHYSICAL DESCRIPTION. The large memory circuit card assembly is a 7.75-inch by 12-inch long assembly, fitted with a 98-pin plug that matches the GRAPHIC 8 terminal controller card cage connectors XA1 through XA7 which are commonly wired. The preferred position for the large memory card is the lowest numbered slot available on the processor bus (i.e., slot 1A1A1), with a second card (if used) in the next higher slot. If a 32K or a 16K memory card is used in conjunction with a 64K memory card, the 64K memory card must be in the lower numbered slot. Processor bus control priority is not a concern with these cards.

3.4.2 FUNCTIONAL DESCRIPTION. Each 64K memory card can store up to $65,536_{10}$ 16-bit words (or $131,072_{10}$ separately addressable 8-bit bytes). The 32K memory card can store up to 32,768 16-bit words or 65,536 8-bit bytes. The 16K memory card can store up to 16,384 16-bit words or 32,768 8-bit bytes.

A maximum of two 64K memory cards can be installed in a GRAPHIC 8 system for a combined storage capacity of 131,072 16-bit words or 262,144 8-bit bytes. Each large memory card has its own local oscillator, memory controller, refresh controller, and memory mapping logic.

3.4.3 OPERATION. The large read/write memory cards connect to and are controlled by the processor bus, but do not control that bus. Any applicable circuit card connecting to the processor bus can write data into a specific memory location by seizing control of the bus, placing the desired address on the ADnn-B lines and the desired data on the DAnn-B lines, then placing a low logic level on the WRIT-B (write command) and ADRV-B (address valid) control lines.

Conversely, any applicable circuit card can seize control of the processor bus to read out stored data onto the DAnn-B lines by placing the specific address on the ADnn-B lines and placing a low logic level on the ADRV-B line while leaving WRIT-B high.

3.4.3.1 Memory Organization. The memory card is divided into 4K "pages". Each such page is a 4K word storage area: page 0 = addresses 0 through 4K-1; page 1 = addresses 4K through 8K-1, etc. The 64K memory card has 16 such pages, the 32K memory card has eight pages, and the 16K memory card has four pages.

The G2 configuration of the memory card contains only octal pages 0 through 7. The G4 configuration contains only pages 0 through 3.

Figure 3-4 lists the 32 pages of a 2-card memory. The listing identifies octal-value page numbers and the corresponding octal-value addresses for each page. Note that page 0 is dedicated and cannot be used for general purpose applications. Page 0 contains all the vector trap addresses and certain other reserved functions.

Pages 6 and 7 are a special case. The addresses associated with page 6 are also the addresses associated with the GCP located in ROM on the ROM and status card. An address in the range from 140000_8 through 157776_8 accessess the GCP. However, through a special mapping technique, the display processor can access page 6 of the large read/write memory card. The display processor is the only device that can access page 6.

Similarly, the addresses associated with page 7 are also the addresses associated with devices (device addresses). An address in the range from 160000_8 through 177776_8 accesses a particular device. However, through a special mapping technique, the display processor can access page 7 of the large read/write memory card. The display processor is the only device that can access page 7.

3.4.3.2 Memory Addressing. Typical devices that have access to the memory include the display processor, digital graphic controller, and parallel interface. Only the display processor can use the memory mapping technique and thus gain access to pages 6 and 7. All other devices address the memory directly.

The memory card can be addressed in either of two ways: by 18-bit addressing from any card capable of generating an 18-bit address, or by 16-bit addressing (plus page registers) by the display processor.

Figure 3-5 shows the structure of an 18-bit address. This mode of addressing is called direct addressing. Bit 17 (in conjunction with a switch on the memory card) determines whether card 1 or card 2 is addressed. Bits 15 and 16 select a 16K block (4 pages) on the card. Bits 1 through 14 determine the single address within the selected 16K block. Bit 0 is not really part of the address; it determines the word/byte status.

Direct addressing with an 18-bit address gives access to the total memory, except for pages 6 and 7.

The display processor is a 16-bit device, and thus has direct address to only 32K words of memory (8 pages). The display processor can gain access to memory locations above 32K-1 by memory mapping from memory locations in the range from 4K through 16K-1. This feature involves the use of three page registers.

The memory card contains three page registers, each of which can be preloaded with some particular value consisting of five bits. When the display processor addresses a page register, the five bits stored in that register becomes bits 13 through 17 of the address, as shown in figure 3-6. This feature allows mapping to 32 pages.

OCTAL PAGE #		EFFECTIVE ADDRESSES
	MEMORY CARD 1	
0	RESERVED	000000:017776
1	MAP AREA 1	020000:037776
2	MAP AREA 2	040000:057776
3	MAP AREA 3	060000:077776
4		100000:117776
5		120000:137776
6	GCP (ROM)	140000:157776
7	DEVICE ADDRESSES	160000:177776
10		200000:217776
11		220000:237776
12		240000:257776
13		260000:277776
14		300000:317776
15		320000:337776
16		340000:357776
17		360000:377776
	MEMORY CARD 2	
20		400000:417776
21		420000:437776
22		440000:457776
23		460000:477776
24		500000:517776
25		520000:537776
26		540000:557776
27		560000:577776
30		600000:617776
31		620000:637776
32		640000:657776
33		660000:677776
34		700000:717776
35		720000:737776
36		740000:757776
37		760000:777776

Figure 3-4. Correspondence between Octal Page Numbers and Their Associated Addresses

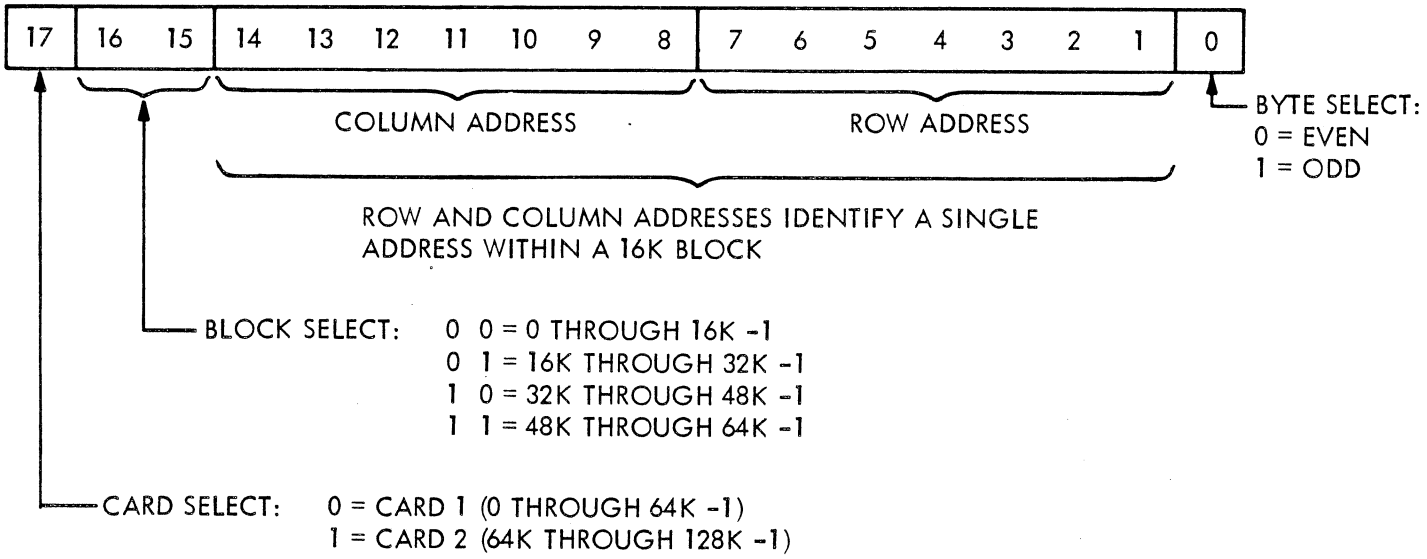

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Figure 3-5. Structure of 18-Bit Address

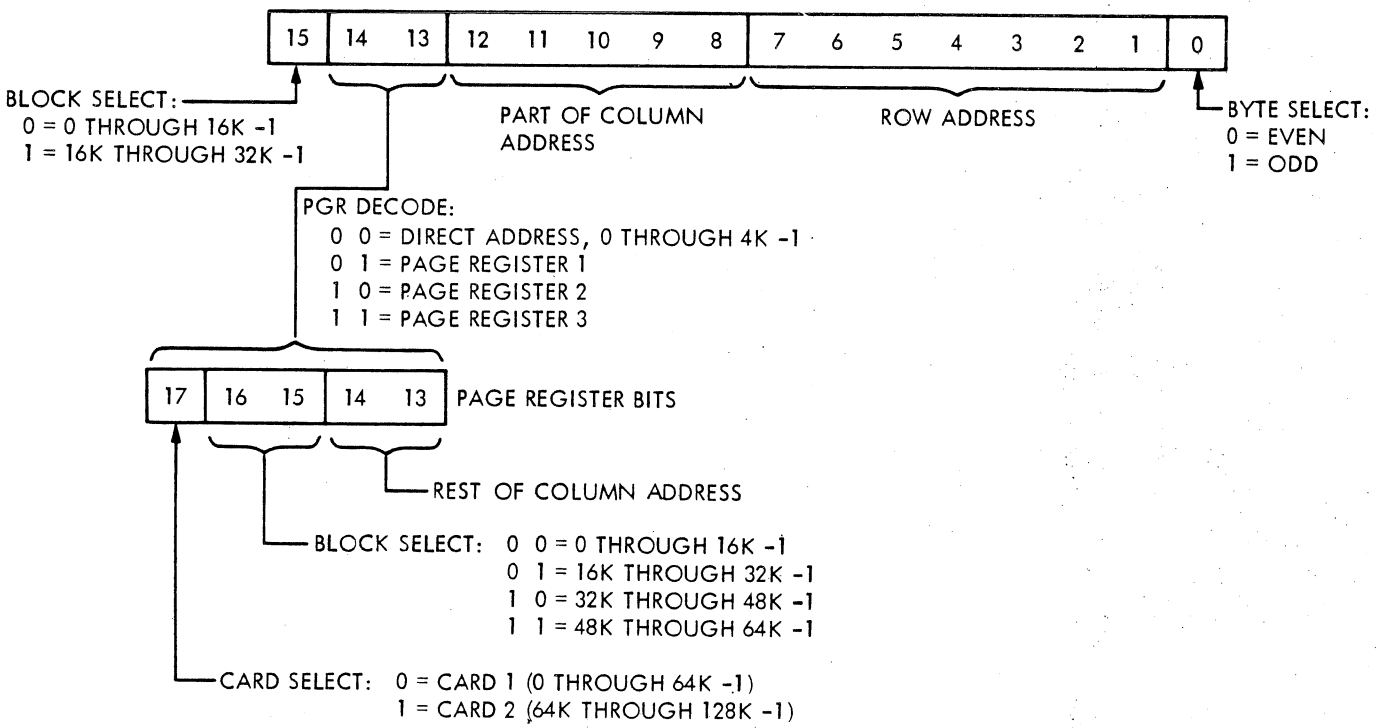

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Figure 3-6. Structure of 16-Bit Address with Memory Mapping

Memory mapping is not invoked when bits 13 through 15 are all zeros; in this case the display processor has direct access to page 0 (memory locations 0 through 4K-1). Memory mapping is not invoked when bits 15 is true (low = logic 1); in this case the display processor has direct access to pages 4 and 5 (memory locations 16K through 24K-1). (In this case pages 6 and 7 are still locked out.)

Memory mapping is invoked only when the controlling device is the display processor, bit 15 is high (logic 0) and bits 13 and 14 are not both zeros. In this case, bits 13 and 14 select one of the three page registers, and bits 1 through 12 constitute part of the final address. The selected page register contributes five additional bits: bit 17 selects the memory card; bits 15 and 16 select a 16K block (4 pages) on the card; and bits 13 and 14 select a predetermined 4K block (1 page) within the 16K block. This is how the display processor gains access to pages 6 and 7 and to memory locations above 32K-1.

However, if the page register is loaded with all zeros, then memory mapping is disabled and the address defaults to the appropriate 4K page in the range from 4K through 16K-1.

3.4.3.3 Example of Memory Mapping. Assume that the page registers are loaded as shown in figure 3-7. In this case, if the display processor addresses map area 1 or 3, it gains access to pages 1 or 3 because page registers 1 and 3 are loaded with all zeros. However, a read/write operation addressed to map area 2 actually reads or writes at the corresponding address on page 14, because page register 2 contains a value of 14.

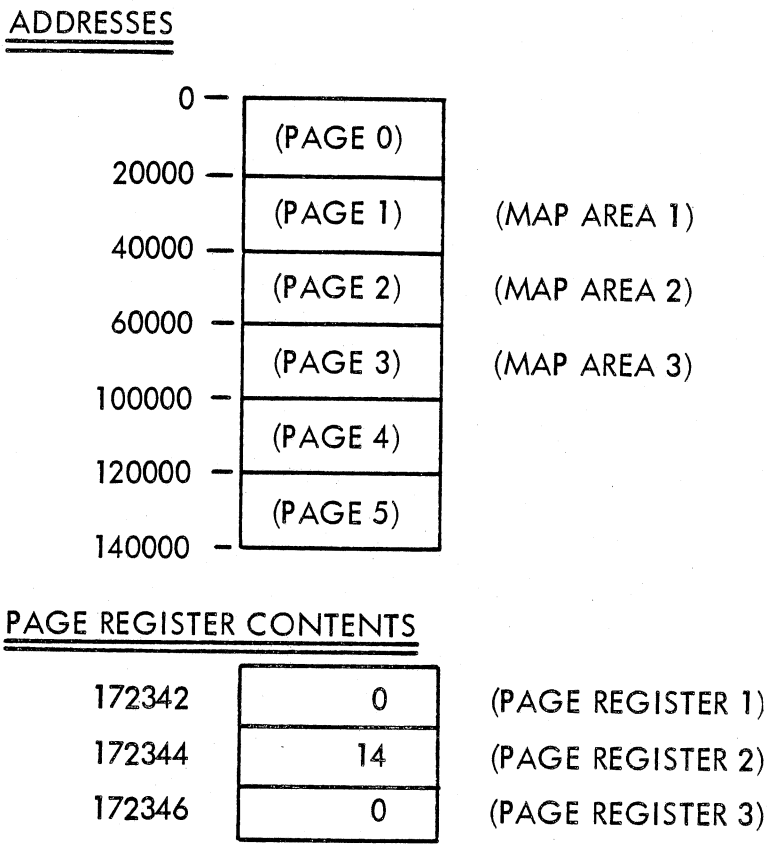

Figure 3-7. Mapping Action

3.4.3.4 PGR Considerations. The graphic controller card's PGR (page register) logic stores and outputs address bits AD16-B and AD17-B, which effectively select one of four 32K memory banks for read/write operations while the graphic controller card has control of the processor bus. The GCP can read or write this register (when the digital graphic controller card is halted) through data bits DA14-B and DA15-B at address 165014_8. Such access requires paying special attention to the handling of digital graphic controller interrupts and to starting and stopping the graphic controller.

All page registers (PGR, PR1, PR2, and PR3) are cleared (to zero value) by activation of a REST-B bus-reset signal following power turn-on, execution of a reset instruction, or receipt of a host-generated initialize command.

3.4.4 OPERATOR CHECKOUT PROCEDURE. Whenever the terminal controller is initialized in the LOCAL mode, the terminal controller performs its built-in diagnostic routines and presents the results of this self-test as part of the verification test pattern. Refer to the programmer's reference manual for details.

As part of the memory diagnostic test, you can examine the memory configuration. Address 000736 contains the RAM configuration word.

1. On keyboard, press RETURN 736/

2. The verification test pattern disappears and the display shows

   000736 / nnnnn

where nnnnn is an octal code that describes the configuration of the installed read/write memory, as follows:

000400 = 16K	017400 = 80K
001400 = 32K	037400 = 96K
003400 = 48K	077400 = 112K
007400 = 64K	177400 = 128K

3.4.5 THEORY OF OPERATION. The large read/write memory card allows the following operations to be performed:

1. Load five bits of data into the page registers.

2. Read a 16-bit word from memory.

3. Write a 16-bit word into memory.

4. Read eight least significant bits from memory.

5. Write eight least significant bits into memory.

6. Read eight most significant bits from memory onto the least significant bit lines of the processor data bus.

7. Write eight least significant bits from the processor data bus into eight most significant bit positions of memory.

When none of these operations is being performed, the memory runs through a continuing program of refreshing itself.

The major circuit blocks shown in figure 3-8 perform the following functions to support these operations.

1. Signal Inverters. The WRIT-B, ADRV-B, and ADnn-B signals are inverted and buffered to match the logic of the card and to allow multiple usage of the signals.

2. Page Register Control Circuits. The page register control circuits recognize when memory mapping is being invoked and which of the threepage registers is being accessed. They also recognize whether the page registers are being accessed for a memory read/write operation, or whether new mapping information is being written into the page registers themselves. The inputs to the page register control circuits are those address bits that make up the address 17234X, the additional address bits that select a single page register, and a read/write instruction.

When new mapping information is being written into the page registers, these circuits also receive data bits DA00-B through DA04-B from the data control circuits.

The outputs from the page register control circuits are address bits P1-P5, which go to the address selection circuits and the data control circuits. Refer to figure 3-6 for the functions of these five bits.

The page registers are cleared by an active low REST-B.

3. Address Selection Circuits. The address selection circuits address the memory array in a two-step operation: first the proper row in memory is selected, then all columns. The intersection of row and column is the location of the individual address.

When direct addressing is invoked, the address selection circuits compile the address from address bits AD01-B through AD17-B. When memory mapping is involved, the address selection circuits compile the address from address bits AD01-B through AD12-B plus bits P1 through P5 from the page register control circuits. When the memory is not being accessed by some external device, the address selection circuits perform the memory refresh operation. A counter in the address selection circuits generates sequential addresses for refresh.

The output from the address selection circuits consists of two groups of seven bits each, the first to select the row, the second the column. The timing of the address selection circuits is controlled by the timing and control circuits.

These row and column bits are applied to all 64 chips in the memory array. The appropriate signals from the timing and control circuits turn on only the appropriate chips to enable that address that was selected by the address selection circuits.

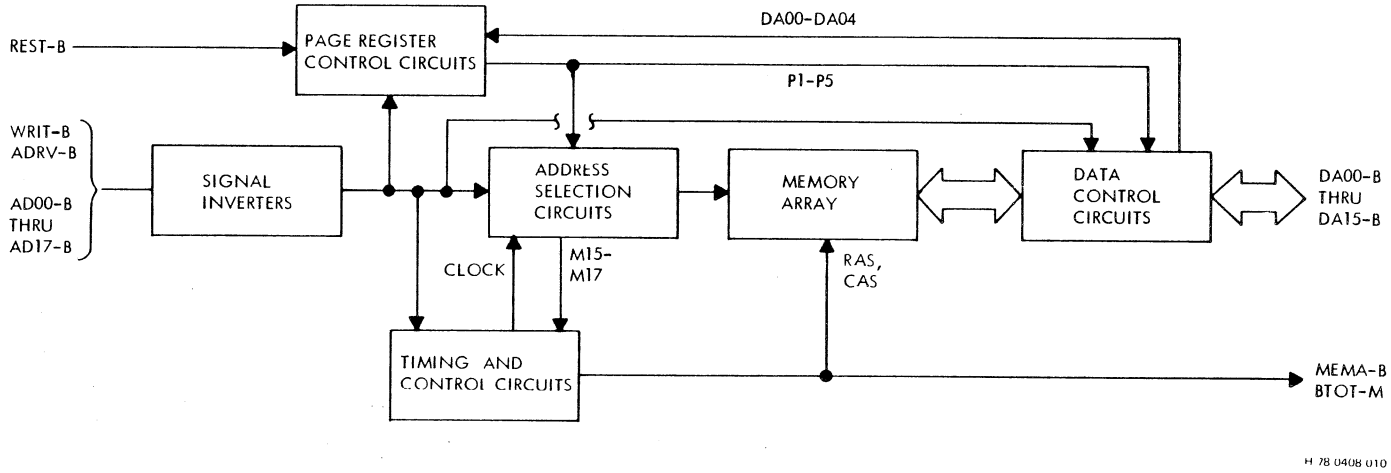

Figure 3-8. Large Read/Write Memory, Simplified Block Diagram

4. Timing and Control Circuits. The timing and control circuits produce the signals that turn on only the selected chips in the memory array that are selected by the address selection circuits. Two turn-on signals, RAS (row address strobe) and CAS (column address strobe), strobe in the row and column address information from the address selection circuits. RAS and CAS go only to selected chips in the memory array, as determined by bits M15 through M17 from the address selection circuits.

The timing and control circuits also generate clocking signals at 10 MHz and 20 MHz that regulate timing throughout the large read/write memory card.

The timing and control circuits also generate the memory acknowledge signal (MEMA-B) at the completion of a memory operation, and the time-out signal BTOT-M if for some reason a memory request does not get serviced.

5. Data Control Circuits. The data control circuits are the interface between the large read/write memory card and the DAnn-B lines on the processor bus. When data is to be written into either the memory array or the page registers, the data control circuits accept the information from the processor bus and pass it to its destination. When data is to be read from the memory array, the data control circuits accept the information from the memory array and pass it to the processor bus.

When the data to be read or written is an eight-bit byte, the data control circuits select the appropriate high/low byte of memory address for connection to the least significant bit lines of the processor data bus.

6. Memory Array. The memory array is organized as a matrix consisting of four rows and 16 columns. Each row represents a word, and each column represents a bit of that word. At the intersection of each row and column, there is a 16K x 1 bit dynamic random access memory device. Therefore, each row represents $16,384_{10}$ 16-bit words. Total storage for the array (four rows) is $65,536_{10}$ 16-it words. Each 16-bit word is divided into two 8-bit bytes by separate read/write control lines, allowing selection of the high or low byte when needed.

3.4.6 DETAILED DESCRIPTION. Refer to figure 3-9 in this section and to engineering drawing 1089726 in Sanders document H-81-0097.

3.4.6.1 Card Power. The read/write memory card receives +5V (P05V+), +15V (P15+), and -15V (N15-) from the terminal controller power supply.

The +5V is filtered and distributed in four discrete fanouts, three of which go to logic devices and one goes to the memory array. The four fanouts are decoupled from each other.

Voltage regulator VR1 and its associated components reduce the +15V input to +12V for the devices in the memory array.

Voltage regulator VR2 and its associated components reduce the -15V input to -5V for the devices in the memory array.

3.4.6.2 Page Register Control Circuits.

1. Page Register Decoder. When ADDRESS VALID (ADRV-B) is true, the register decoder responds to address 17234X, where X has the value 2, 4, or 6. When WRIT-B is also true, one of the three page registers is to receive raw data. When WRIT-B is not true, then the contents of the selected page register are to be made available to the address selection circuits.

2. Read/Write Page Register Control. When the register decoder responds to a page register address, a high at the output of U40D is applied to the A and B inputs of register U9. The 10 MHz clocking signals from the timing and control circuits make this high available at the register QB and QC outputs.

3. Write Selected Page Register. U48B is a 2-line to 3-line decoder. When the read/write page register control QB output is high and WRIT-B is also true, the output of U10B strobes address bits A1 and A2 into U48B. These two bits select one of the three page registers, as follows:

ADDRESS	A2	A1	PAGE REGISTER
172342	low	high	U22 (page register 1 on card 1 or page register 4 on card 2)
172344	high	low	U12 (page register 2 on card 1 or page register 5 on card 2)
172346	high	high	U2 (page register 3 on card 1 or page register 6 on card 2)

NOTE

Page register selection is the same on both cards of a two-card memory, but the memory control circuit on the card not being addressed is inhibited by the read/write inhibit circuit in the timing and control circuits.

The output of U48B clocks the new data into the selected page register. This is how a page register gets loaded with bits D0 through D4 from the data control circuits.

4. Read Selected Page Register. The 15 bits representing the outputs of the page registers are always applied to the page register output multiplexer. The read selected page register circuit, when enabled, determines which set of five bits pass through the multiplexer.

The read selected page register circuit is enabled when the register decoder recognizes a valid address 17234X. Then bits A1 and A2 form a code (as for the write selected page register circuit) through which U38A enables the page register output multiplexer to pass one set of five bits from the selected page register.

When direct addressing is invoked and bit AD15-B is high (bit A15 is low; the desired address is less than 16K), data selector U38A is also enabled. In this case bits A13 and A14 form the code that selects the output of one page register to pass through the multiplexer. However, in this case, the selected page register must have been loaded with all zeroes; otherwise the result will be inadvertent paging.

5. Page Registers. The page registers (U2, U12, U22) are hex D-type flip-flops. Each stores five bits of data (D0-D4) that correspond to memory page numbers, as explained in Section 2. They get loaded as described under Write Selected Page Register and are read as described under Read Selected Page Register.

6. Page Register Output Multiplexer. Devices U1, U11, and U21 constitute five 3-line to 1-line data selectors, one for each bit stored in the page registers. The selected input bits are connected to the outputs in response to the code from the read selected page register circuit.

3.4.6.3 Address Selection Circuits

1. Refresh Address Counter. Devices U26 and U27 comprise a synchronous 7-bit counter that gets clocked every 15 microseconds (66.667 kHz rate). When the read/write memory card is not otherwise engaged, it continually refreshes itself. The refresh address counter steps through its 128 addresses in 2.0 milliseconds, then repeats. Its output consists of refresh address bits R0 - R6, which go to the memory address multiplexer.

2. Comparator. Comparator U4 continually monitors the output of the page register output multiplexer. If the five outputs of the page register output multiplexer (P1 - P5) are all zeroes, the comparator sends a high output to the address gate.

3. Address Gate. The address gate controls the operation of the physical address multiplexer, which determines whether the five least significant bits of the memory address come from the direct address chain (A13 - A17) or from the page register output multiplexer (P1 - P5). A low output from address gate U49A selects P1 - P5; a high output from address gate U49A selects A13 - A17. The output of U49A is high if the output of comparator U4 is high or if DEV1-B is low or if DEV2-B is low or if DEV3-B is high (these last conditions implying that some device other than the display processor is in control of the bus).

The output of U49A is low if the output of the comparator is low (indicating that a non-zero condition was stored in the selected page register) and DEV1-B is high and DEV2-B is high and DEV3-B is low (these last three conditions signifying that the display processor has control of the bus and memory mapping is invoked).

4. Physical Address Multiplexer. Under control of the address gate, the physical address multiplexer (U3, U13) passes either P1 - P5 or A13 - A17 as the five least significant bits of the memory address, M13 - M17. Bits M13, M14 go to the memory address multiplexer. Bits M15, M16 go to the RAS generator in the timing and control circuits. Bit M17 goes to the read/write inhibit circuit in the timing and control circuits.

5. Memory Address Multiplexer. The memory address multiplexer, in response to commands from the memory control circuit in the timing and control circuits, selects seven bits as the address of the memory array. Note that it must make two such 7-bit selections, one before the RAS occurs, the other before CAS occurs. However, during the refresh operation, it makes ony one 7-bit selection (R0 - R6) because refresh does not require a CAS signal.

During a normal memory read/memory write operation (not refresh), the first 7-bit selection consists of bits A1 - A7 from the signal inverters. The second 7-bit selection consists of bits A8 - A12 from the signal inverters plus bits M13, M14 from the physical address multiplexer. M13 can represent either A13 or P1, M14 can represent either A14 or P2, depending on the state of the physical address multiplexer.

The seven outputs of the memory address multiplexer go to the memory array.

3.4.6.4 Timing and Control Circuits. The memory control logic has two modes of operation: read/write memory cycle and refresh cycle. An active ADDRESS VALID signal (logic high at TP5) initiates a read/write cycle. An active REFRESH REQUEST (logic high at TP3) starts a refresh cycle. Each request for memory is serviced, provided the memory is not busy. Neither cycle has priority over the other. A memory cycle cannot be interrupted once it has stated; therefore requests are locked out by a busy signal once a cycle has started.

1. Clock Generator. Master oscillator U7 is a voltage-controlled oscillator with a fixed frequency of 20 MHz. Flip-flop U18 divides the 20 MHz clock frequency to 10 MHz. Single-shot U28A produces 15 microsecond output pulses (66.667 kHz rate) to increment the refresh address counter.

2. Read/Write Inhibit. The function of the read/write inhibit circuit is to prevent read/write operations at specific 4K pages of memory, as determined by the user; this circuit also includes the switch that identifies the memory card as card 1 or card 2 in a 2-card installation.

Device U6 consists of five SPST switches, S1A through S1E. S1A is the card select switch. When switch S1A is off (ON end up), the card responds to addresses from 64K to 128K-1 (card 2). When switch S1A is on (ON end down), the card responds to addresses from 0 through 64K-1 (card 1).

Switches S1B through S1E enable (switch off, ON end up) or disable (switch on, ON end down) 4K memory blocks as follows:

SWITCH	MEMORY ADDRESSES
S1B	28K - 32K-1
S1C	24K - 28K-1
S1D	20K - 24K-1
S1E	16K - 20K-1

When a switch is on (disabling access to memory), the protected area is not accessible by direct addressing. Such an area is still accessible to the display processor through memory mapping.

The inputs to the read/write inhibit circuit are bits A13 - A16, and M17.

Bit M17 is compared with the setting of switch S1A in comparator U16. If the switch output and the bit level are the same, the output of U16 is low and the address is recognized as pertaining to the card. If the switch output and the bit level are different, the output of U16 is low and the memory is inhibited.

When bit A15 is high and bit A16 is low, 2-line to 4-line multiplexer U24A is enabled; bits A13 and A14 then form a code that selects one of the 4K blocks listed above. The output of the multiplexer is compared with the setting of the corresponding block select switch. If both are low, the output of the corresponding section of U5 is high as an input to U16 and the output of U16 goes low, inhibiting memory. If either the output of the multiplexer or the output of the switch is high, memory is enabled.

3. Refresh Request/Inhibit Cycle Gates. This circuit starts a memory cycle (either read/write or refresh) and prevents another input from trying to start a cycle while one is already in progress. It also prevents a read/write cycle from occurring if the address has been locked out by switch S1.

Flip-flop U19A is clocked by the leading edge of the 15 microsecond REFRESH CLOCK pulse from U28A. The high output of U19A is gated through U29C, provided that the output of U17D is also high. If the output of U17D is not high, it means that a cycle is already in progress and refresh is inhibited.

Similarly, gate U10C passes a high ADDRESS VALID signal, provided that the output of U17D is high and the output comparator U16 in the read/write inhibit circuit is also high.

Either a REFRESH REQUEST or an ADDRESS VALID, when the other signals are high, produces a high at the output of U29A, which starts the memory control circuit.

4. Memory Control. The memory control circuit generates the timing signals that trigger the RAS generator, memory address multiplexer, CAS generator, and busy/timeout circuit in the proper sequence. The heart of the memory control circuit is a fourstage ripple counter, U14 and U15.

A high output from U29A in the refresh request/inhibit cycle gates circuit clocks U19B, priming gates U30A and U10A. The same high output from U29A, inverted by U20B, presets flip-flop U18B. The high Q output of U18B passes through gate U17B (the other input to U17B is high at this time) and ripples successively through

U14A, U14B, U15A, and U15B. Each of these flip-flops is clocked by the 20 MHz signal from the timing generator. When U15B clocks high, its low $\overline{Q}$ output disables U17B, so that a low level starts rippling through the counter.

When U14A receives the high input, its $\overline{Q}$ output goes low and triggers the RAS generator circuit through U17A. When U14B receives the high, its high Q output strobes the memory address multiplexer, selecting the CAS address. When U15A receives the high, its high Q output clocks the CAS generator.

Whether or not a CAS signal is generated depends on whether the cycle was started by a REFRESH REQUEST or an ADDRESS VALID signal. If the cycle was started by a REFRESH REQUEST signal, the ADDRESS VALID signal remains low throughout the cycle, keeping U25B in its clear state; further, the D input to U25B is low, thus preventing generation of a CAS signal. If the cycle was started by an ADDRESS VALID signal, the high ADDRESS VALID signal unblocks U25B and the D input to U25B is high, which gets clocked through by the Q output of U15A.

When flip-flop U18B is preset at the beginning of the cycle, its $\overline{Q}$ output is gated through U17D to disable the refresh request/inhibit cycle gates for the duration of the memory cycle. At the end of the cycle (after the high has passed through the ripple counter and been replaced by the rippling low), the $\overline{Q}$ output of U15B goes high and clocks U18B, removing the low from the input of U17D.

At that point in the cycle when the Q output of U15B is still high but the $\overline{Q}$ output of U15A has gone high, the output of U10A goes low to preset U19A. The $\overline{Q}$ output of U19A goes low, clearing U19B. This is the normal or static condition that prevails between memory cycles. A new REFRESH REQUEST changes the states of U19A and U19B; a new ADDRESS VALID signal does not change their states.

Figure 3-10 shows the timing signals associated with memory control.

5. RAS Generator. The function of the RAS generator is to produce either a single low $\overline{\text{RAS}}$n strobe in response to an ADDRESS VALID input or four low $\overline{\text{RAS}}$n strobes in response to a REFRESH REQUEST input.

In the ADDRESS VALID case, gate U30A is disabled by a low input from U19B. When the output of U17A in the memory control circuit goes low, it strobes 2-line to 4-line multiplexer U24. One output of the multiplexer goes low, as determined by the values of bits M15 and M16 from the address selection circuits. The selected low output is gated through U86 to the proper row in the memory array.

In the REFRESH REQUEST case, gate U30A is enabled. When the output of U17A goes low, the output of U30A also goes low and activates all four $\overline{\text{RAS}}$ signals to the memory array. The memory array cells that get refreshed in this case are a function of the output of the refresh address counter in the address selection circuits. If there is no interruption by an ADDRESS VALID input, the entire memory gets refreshed by 128 REFRESH REQUEST cycles in a 2-millisecond period.

6. CAS Generator. The function of the CAS generator is to produce four low $\overline{CAS}$n signals in response to an ADDRESS VALID input, and not to generate any $\overline{CAS}$n signal in response to a REFRESH REQUEST input. The CAS generator consists of flip-flop U25B and four inverters. The action of U25B is described under Memory Control. In the ADDRESS VALID case, the low $\overline{Q}$ output of U25B goes to U17D to disable any further inputs until the operation is complete. The high Q output of U25B also clocks U39A in the read/write lo/hi byte control circuit (part of the data control circuits).

7. MEMA/Timeout Circuit. The MEMA/timeout circuit consists of timer U28B, flip-flops U39B, U25A, and six inverters. The functions of the MEMA/timeout circuit are to generate the MEMA-B (MEMORY ACKNOWLEDGE) signal that indicates the completion of certain activities, and to generate the BTOT-M (BUS TIMEOUT) signal if the memory fails to complete a cycle in response to an ADDRESS VALID input.

When the page register address is detected, the read/write page register control generates the MEMA-B signal to indicate to the display processor that the page register decoder has recognized the page register address 17234X. The high QC output of register U9, inverted by U50B, becomes the MEMA-B signal.

In the ADDRESS VALID case, the high ADDRESS VALID signal starts timer U28B. The low $\overline{Q}$ output of U19B is applied to the D input of U25A. When (during the memory control cycle) the $\overline{Q}$ output of U15A goes high, it clocks U25A. The low $\overline{Q}$ output of U25A, twice inverted, becomes the MEMA-B signal.

When MEMA-B goes low, the device that generated the ADDRESS VALID signal clears that signal. The ADDRESS VALID clears timer U28B and flip-flops U39B and U25A.

If the timer times out (approximately 12 microseconds), the low-to-high transition of the timer $\overline{Q}$ output clocks flip-flop U39B. The low $\overline{Q}$ output of U39B, twice inverted, produces both the MEMA-B and BTOT-M signals. The MEMA-B signal terminates the ADDRESS VALID signal. The BTOT-M signal indicates that the memory cycle was not completed.

In the G1 configuration of the large read/write memory, a jumper is installed from E2 to E3 to disable the preset terminals of U25A and U39B. In the G2 and G4 configurations, the jumper is installed from E2 to E1. If address bit M16 goes high, indicating an address higher than 32K-1, the output of inverter U50F goes low; this low presets U39B and U25A and immediately produces both the MEMA-B and BTOT-M signals, indicating that the memory card does not contain the address specified.

3.4.6.5 Data Control Circuits

1. Data Input/Output Multiplexer. Multiplexers U32, U33, U46, and U47 are tri-state devices. The multiplexers pass processor bus DAnn-B data to the memory banks as the Dnn data bits at all times. When so directed by LO BYTE/HI BYTE signals from the read/write lo/hi byte control circuit, the multiplexers pass the memory output bits Onn to the same processor bus. When the LO BYTE/HI BYTE signals are inactive, the connections between Onn and DAnn-B are at a high impedance level.

Each multiplexer acts as both an input and output register. Each register contains four bits of the 16-bit data word. Operation of the registers depends on the status of the read/write command and the status of the byte select signals.

2. Read/Write Lo/Hi Byte Control. The read/write lo/hi byte control circuit, in response to the levels of the BYTE-B, AD00-B, and WRIT-B inputs, performs the following functions:

BYTE-B	AD00-B	WRIT-B	FUNCTION
H	H	H	Read 16-bit word from memory
H	H	L	Write 16-bit word into memory
H	L	H	Illegal - no response
H	L	L	Illegal - no response
L	H	H	Read 8 LSBs from memory; MSBs on bus = 0
L	H	L	Write 8 LSBs into LSB locations in memory; MSB locations are not altered
L	L	H	Read 8 MSBs from memory onto bus LSB lines; bus MSB lines = 0
L	L	L	Write 8 LSBs from bus into MSB locations in memory; memory LSB locations are not altered

a. Read/Write Decision. The memory write command is a low from U8A (lo byte) and/or U8B (hi byte). When WRIT-B is high (indicating a read operation), the output of U30B is high, and the outputs of U8A and U8B are both high.

Similarly, during a refresh operation, the $\overline{Q}$ output of U19B is low, the output of U30B is high, and the outputs of U8A and U8B are both high.

When WRIT-B is low (indicating a write operation), and the $\overline{Q}$ output of U19B is high (indicating an ADDRESS VALID case), then the output of U30B is low. If BYTE-B is high (indicating a 16-bit operation), then the outputs of U8A and U8B are both low, and 16 bits of data may be written into memory.

If WRIT-B is low (indicating a write operation), and the $\overline{Q}$ output of U19B is high (indicating an ADDRESS VALID case), and BYTE-B is low (indicating an 8-bit operation), then either U8A or U8B has a low output (but not both), depending on the state of the AD00-B signal. If AD00-B is high, the output of U8A is low, permitting writing into the LSB locations in memory. If AD00-B is low, the output of U8B is low, permitting writing into the MSB locations in memory.

b. Lo/Hi Byte Decision. Figure 3-9 shows that, for data flow from the data bus to the memory array, all 16 bits enter the data input/output multiplexer. However, only the eight LSBs go directly from the input/output multiplexer to the memory array. All 16 bits go from the input/output multiplexer through the byte swap multiplexer to the memory array. This arrangement allows the following three possibilities:

- Write 16-bit word into memory
- Write 8 LSBs into LSB locations in memory; MSB locations are not altered
- Write 8 LSBs from bus into MSB locations in memory; memory LSB locations are not altered

Similarly, for data flow from the memory array to the data bus, only the eight MSBs go directly from the memory array to the data input/output multiplexer. However, all 16 bits go through the byte select multiplexer to the input/output multiplexer. This arrangement allows the following three possibilities:

- Read 16-bit word from memory
- Read 8 LSBs from memory; MSBs on bus = 0
- Read 8 MSBs from memory onto bus LSB lines: bus MSB lines = 0

In the write case, when AD00-B is high, the byte swap multiplexer (U36, U37) passes the eight MSBs from the input/output multiplexer to the memory array. When AD00-B is low, the byte swap multiplexer passes the eight LSBs from the input/output multiplexer to the memory array. In either case, the outputs of the byte swap multiplexer go to the MSB locations in memory.

In the read case, the MSB bits from memory (bits D08 - D015) are always supplied to the MSB half of the data input/output multiplexer (U46, U47). All 16 bits from memory are applied to byte select multiplexer (U31, U41, U42, U43). The state of the AD00-B signal determines whether the MSB bits or the LSB bits get applied to the LSB half of the data input/output multiplexer (U32, U33). When AD00-B is high, the LSB bits are selected; when AD00-B is low, the MSB bits are selected.

Putting the bits applied to the data input/output multiplexer onto the data bus lines is a separate operation. When the LO BYTE or HI BYTE signals go low, the data is transferred to the data bus lines. When the LO BYTE or HI BYTE signals are high, the data input/output multiplexer is held in its high impedance state, and the lines are held at a logic high (logic 0) level.

The LO BYTE and HI BYTE signals are controlled by flip-flop U39A and gates U30C, U30D. In the REFRESH REQUEST case, the D input to U39A is high. As a result, both the LO BYTE and HI BYTE lines are high, and there is no output from the data input/output multiplexer.

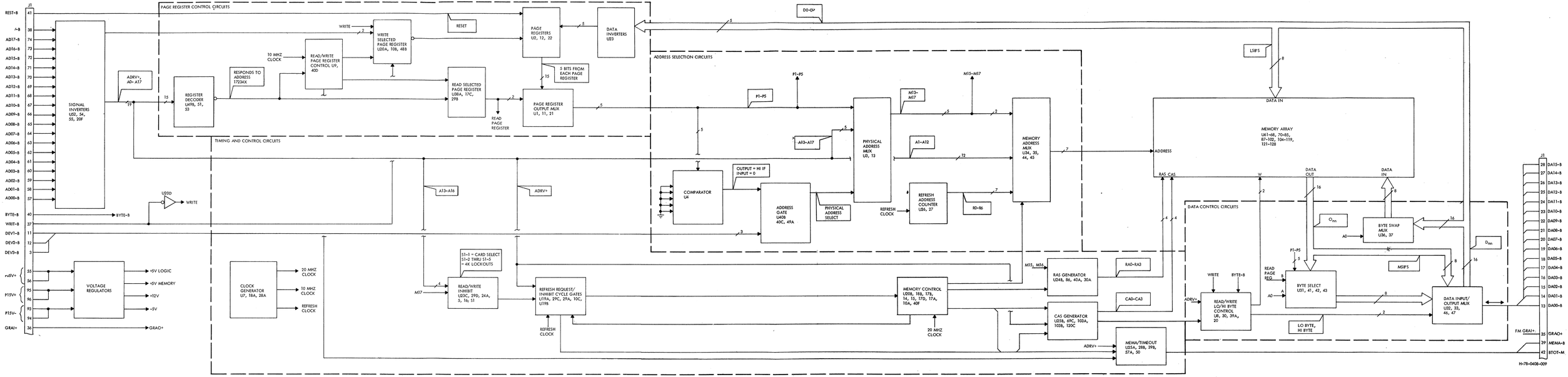

Figure 3-9. Read/Write Memory, Functional Block Diagram

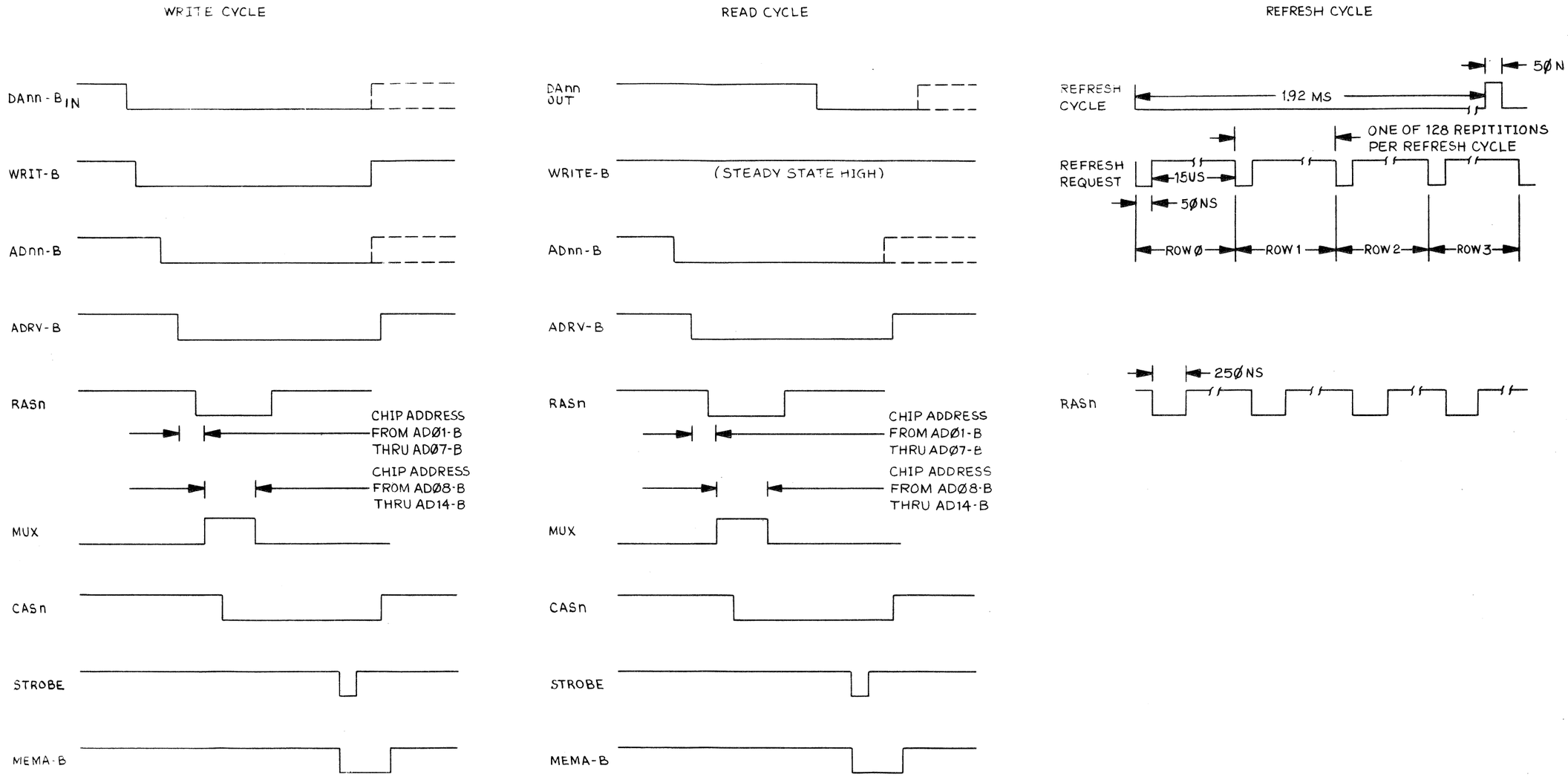

Figure 3-10. Write Cycle, Read Cycle and Refresh Cycle Timing

In the ADDRESS VALID case, the D input to U39A is low; the trailing edge of $\overline{CAS}$ clocks U39A, making the LO BYTE line low. Whether the HI BYTE goes low or not then depends on the state of the BYTE-B input.

c. Reading Page Register Contents. As a special case, an address of 17234X with WRIT-B, AD00-B, and BYTE-B held high reads the contents of the addressed page register. In this case, the low output of U29B applied to the byte select multiplexer puts bits P1 - P5 on the line to the data input/output multiplexer; the other three bits are hard-wired high (logic 0). The low output of U29B also clears flip-flop U39A; the LO BYTE line goes low, placing bits P1 - P5 on the data bus lines. The HI BYTE line also goes low, but because there is no CAS strobe, the memory is not accessed. The MSB bytes are all high (logic 0).

3. Byte Swap Multiplexer. The byte swap multiplexer (U36, U37) is involved only in a memory write operation. Its use is described under Read/Write Lo/Hi Byte Control. When AD00-B is high, the multiplexer passes the eight MSBs to the memory array. When AD00-B is low, the multiplexer passes the eight LSBs to the memory array.

4. Byte Select Multiplexer. The byte select multiplexer (U31, U41, U42, U43) is involved only in a memory read operation. Its use is described under Read/Write Lo/Hi Byte Control. When the B inputs are low, the multiplexer passes bits P1 - P5 (and the associated hard-wired bits) to the LSB portion of the data input/output multiplexer. When the B inputs are high, the output selected depends on the level of the A inputs. High A inputs select the most significant bits from memory; low A inputs select the least significant bits from memory.

3.4.6.6 Memory Array. The individual memory device is a dynamic random access MOS memory circuit, organized as $16{,}384_{10}$ words by 1 bit. The device features multiplexed address inputs, permitting it to be packaged in a standard 16-pin chip. Other features are low power (less than 462 mW active) and fast access time (200 ns maximum).

Each memory chip is configured as a 128 bit by 128 bit cell for addressing purposes. Seven row addresses are latched onto the chip by a low-going $\overline{RAS}$ signal; then seven column addresses are latched onto the chip by a low-going $\overline{CAS}$ signal.

Whenever $\overline{CAS}$ is high, the memory data output lines are held floating in a high impedance state. The output contains a logic 0 or 1 only during the access time of a ready cycle.

Chips that do not receive the $\overline{RAS}$ signal remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

3.5 PARALLEL INTERFACE

NOTE

If your GRAPHIC 8 system contains a parallel interface that has its own technical manual, skip this paragraph and refer to that manual instead.

The parallel interface allows input/output communications between the GRAPHIC 8 system and the host computer. The interface card is designed for easy modification during assembly to accommodate different host computers and applications. For example, host/interface communications pass through buffer gates that can be jumpered to produce the positive logic (active high) conditions used on the parallel interface card. If the host computer uses negative logic (active low) signals, the buffer gates are inverters. If the host computer uses positive logic (active high) signals, the buffer gates do not invert.

Other special requirements are accommodated by convenient jumper selections between lug terminals on the parallel interface card. These jumper selections include: subordinate addressing, word/byte mode selection, interrupt priority, or other special conditions as required.

The basic functions of the parallel interface card are:

1. To pass a system initialization command from the host computer to the GRAPHIC 8 system.

2. To generate a GCP interrupt when the host computer announces that it has output data for the GRAPHIC 8 system.

3. To accept output data from the host and pass it to the appropriate destination in the GRAPHIC 8 system: the display processor for single-word transfers, the read/write memory for multiword transfers.

4. To accept data from the display processor or read/write memory and pass it to the host computer.

5. To generate a GCP interrupt after the host computer accepts a GRAPHIC 8 input (either single word or multiword).

6. To perform internal housekeeping activities, and monitor and report status.

3.5.1 SIGNAL CONNECTIONS. The parallel interface card connects through J1 to all the display processor buses, including the 16-bit DAnn-B data bus, the 18-bit ADnn-B address bus, and all bus control and interrupt lines.

The parallel interface connects to the host computer through a 2-way cable attached to edge-mounted connectors J2 and J3.

Connector J2 receives a 16-bit parallel output data word, OD00+* through OD15+, plus a variety of handshaking signals concerned with host computer output data transfers.** This connector also receives an INIT+ host computer output, representing a system reset command.

Connector J3 passes a 16-bit parallel input data word, ID00+ through ID15+, plus a variety of handshaking signals concerned with host computer input data transfers.

3.5.2 PARALLEL INTERFACE INTERNAL BUSES. The parallel interface contains two internal buses: the 16-bit IOnn+ input/output data bus, and the 16-bit STnn+ status bus.

The IOnn+ bus carries the following signals:

1. ODnn+ data words from the host computer. These signals go either to the DAnn-B processor data bus or to storage registers on the parallel interface card.

2. DAnn-B data words from the processor bus. These signals go to storage registers on the parallel interface card, including the host input data register which, in turn, places the data on the IDnn+ bus for transmission to the host computer.

3. Data stored in various registers on the parallel interface card. These signals go either to the DAnn-B processor bus for distribution to other GRAPHIC 8 circuits, or to the host input register on the parallel interface card for transmission to the host computer on the IDnn+ bus.

The 16-bit STnn+ status bus carries various control and monitoring signals. Certain STnn+ bus bits represent GCP commands that establish the correct logic setup for specific operations. Other bits represent monitoring signals that direct the GCP to sequence from one program function to another.

3.5.3 MAJOR CIRCUITS (See figure 3-12.)

Reset and Timing. An active REST-B input from the display processor is converted to REST+ and REST- signals to establish initial conditions throughout the parallel interface card. Similarly, the CLOK-F clock train from the ROM and status logic card is converted to a CLOK+ pulse train for use within the parallel interface.

*Those input/output signals ending with + can be true in either state, depending on the type of computer used. The parallel interface card gets wired so that all logic true outputs from the host computer are received as high logic levels, and all logic true inputs to the host computer are logic highs up to the point where they enter the input buffer gates.

**Unless otherwise specified, the terms input and output are referenced to the host computer.

Data Multiplexer/Storage. This circuit selects the source for the data on the 16-bit IOnn+ bus. It enables the proper register to store the resultant data; it also causes the associated buffer gates to pass that data when appropriate. The data multiplexer controls operation of the buffer gates, passing ODnn+ output data from the host computer to the IOnn+ bus. The data multiplexer also controls the gating circuits to and from the DAnn-B processor data bus.

The storage registers include:

1. Host input data register. This register receives inputs from the IOnn+ bus; its output goes to the IDnn+ bus as an input to the host computer.

2. Memory address register. This register receives inputs from the IOnn+ bus; its output goes to the ADnn-B processor address bus and represents a specific memory address for a read or write operation.

3. Word count register. This register receives inputs from the IOnn+ bus; its output is a WC≠0 signal that stays active as long as there remains data to be transferred during a DMA (direct memory access) sequence. An LED on the card lights when this register is empty (WC=0) and goes out when this register contains any word count value (WC≠0).

4. Status register. This register receives inputs from the IOnn+ bus and from other circuits. The hardware that makes up this register consists of elements that are actually contained in other circuits. The status register outputs can be read on the IOnn+ bus.

Instruction Decoder. This circuit receives as inputs the AD01-B and AD02-B signals from the processor address bus, and the WRIT+ and ADRV+ signals from the processor control bus. Its outputs are read and write commands that go to different registers in the data multiplexer/storage circuit. A write command tells the addressed register to accept data from the IOnn+ bus. A read command tells the addressed register to place its contents on the IOnn+ bus.

Sequence Decoder. This circuit controls the sequence of input/output transfers between the parallel interface and the host computer.

The sequence decoder is a state counter. It increments from one count to another when it detects different control signals. Each count represents a specific state in the input/output transfer sequence, and is accompanied either by command signals that operate on another circuit, or inhibit signals that prevent further actions until the action in process is completed.

The counting sequence varies, depending on whether the specified operation is an input transfer or an output transfer, and whether the operation is a single-word transfer or part of a DMA sequence. LED indicators DS1 through DS4, mounted on the parallel interface card, give a continuous readout of the count. Figure 3-11 shows the indicator convention.

Figure 3-13 shows different counter sequences for each type of input/output transfer, including single word transfers and DMA transfers. Each state of the sequence decoder is represented by a large circle. The small circles give the count value.

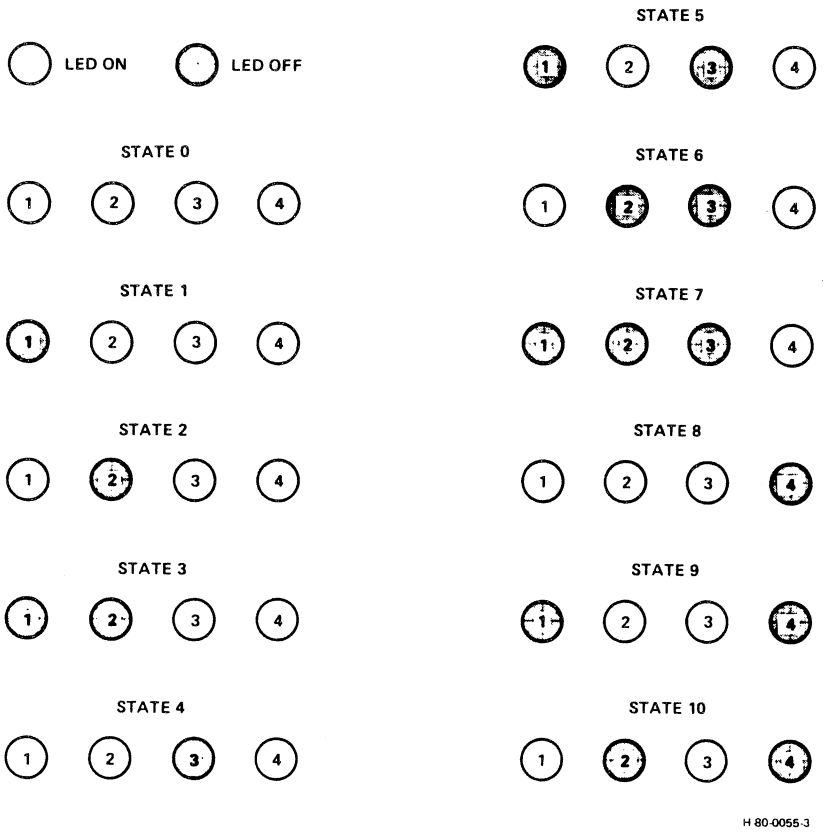

Figure 3-11. Parallel Interface LED Indications

Interrupt and Processor Bus Control. This circuit controls the transfer of data between the parallel interface card and the GRAPHIC 8 processor bus. To perform this function, the circuit monitors the STnn+ status bits and the control lines of the processor bus. Its outputs are timing and enabling signals that:

1. Transfer data to another GRAPHIC 8 card by seizing control of the bus, place the device address and the data on the bus, activate ADRV-B, and wait for the MEMA-B response from the receiving device.

2. Receive data from another GRAPHIC 8 card, steer the data to the appropriate storage register, and generate the MEMA-B response.

The interrupt circuit is triggered by signals from the sequence decoder when single-word input or output transfers are processed, or at the end of a DMA transfer. This circuit interrupts the GCP and sends a trap address to the display processor. The trap address indicates the type of the interrupt condition detected by the sequence decoder, and branches the GCP to the applicable firmware subroutine. Table 3-4 lists the parallel interface interrupt trap addresses.

Table 3-4. Parallel Interface Interrupt Trap Addresses

INTERRUPT	TRAP ADDRESS
Input	120
Output	124
Attention	130

Handshaking Logic. This circuit sends discrete signals to the host computer for handshaking control of all I/O transfers between the parallel interface and the host computer. The circuit consists of an input section and an output section.

1. The output section responds to an active OCTL+ signal from the host computer. After the parallel interface has stored the data from the computer, the handshaking logic sends both an OWR+ signal and an ODR+ signal. The OWR+ signal remains active until the host computer terminates its OCTL+ output. The output handshaking logic also includes an OMR+ signal (a replica of status bit ST00) that can be programmed for unique applications.

2. The input section sends an IWR+ signal to the host computer after valid input data have been placed on the IDnn+ interface bus. When the host computer responds by sending its ICTL+ signal, the input section terminates IWR+ and sends an NDRY+ pulse. The input handshaking logic also includes an IMR+ signal (a replica of status bit ST12) that can be programmed for unique applications.

Initialize Buffer Gates. These circuits convert INIT+ signals from the host computer into low SYST-B signals that go to the display processor to initiate a terminal controller system reset sequence.

3.5.4 OPERATION. The parallel interface performs the following types of operation:

1. Receive single-word output from host computer.

2. Receive DMA transfer from host computer.

3. Send single-word input to host computer.

4. Send DMA transfer to host computer.

In performing these operations, the parallel interface also communicates with the display processor and the read/write memory; it generates GCP interrupts and status signals.

The following paragraphs describe initialization and operation in each of the various modes.

3.5.4.1 Initialization. There are two initialization signals: INIT± from the host computer and REST-B from the display processor.

An active INIT± signal from the host computer enters the parallel interface at J2-47, passes through two or three inverters (depending on the jumper connection at E94) and leaves the parallel interface at J1-43 as a low STST-B that goes to the display processor. The display processor responds by making REST-B low.

A low REST-B signal from the display processor enters the parallel interface at J1-41 and performs the following actions:

1. Clears the interrupt and bus control circuits.

2. Clears the data multiplexer storage registers; memory address and word count go to zero.

3. Clears the sequence decoder; the parallel interface card goes to State 0.

4. Clears the handshaking logic.

In this condition the parallel interface is ready to receive commands and data from either the GCP (over the processor bus) or the host computer (over the interface bus).

3.5.4.2 Status Setup. In its cleared state, the parallel interface is unable to report anything to the GCP. Early in the GCP setup sequence for I/O processing, therefore, the GP8 writes a new status word. This word establishes interrupt enable conditions and any other desired applications (e.g., extended memory address, programmed handshaking requests, etc.). Table 3-6 lists each status bit and its function.

To load the status word into the parallel interface, the GCP places that word on the data bus (DA00-B through DA15-B)*, then places the address for the parallel interface status register on the address bus (AD00-B through AD17-B). See table 3-5.

*Status bits 04, 07, 08, 09, 10 and 15 are read-only bits, not loaded by GCP. They get generated by the parallel interface.

Table 3-5. Parallel Interface
Register Addresses

REGISTER	ADDRESS
Word count	172410
Memory address	172412
Status	172414
Data	172416

The display processor then generates the low BUSB-B, WRIT-B, and ADRV-B signals. These conditions make the instruction decoder in the parallel interface send a WSTA- (write status) command to the data multiplexer/storage logic. The status registers accept and store the bits of the DAnn-B data word, placing them on the status bus to other parallel interface circuits. These status bits remain in effect until the next status update instruction arrives. The parallel interface generates a low MEMA-B to indicate it has recognized its card address.

Table 3-6. Parallel Interface Status Register Bit Description

BIT	IDENTIFICATION	DESCRIPTION
00	OMR+ (output message request) (spare bit #1) (TEST1- OUT)	Program read/write, cleared by processor bus reset. This bit can be programmed as required and presents an OMR+ signal to the host computer. When J2/J3 test strap is connected, this signal triggers the NDRY single-shot.
01	MAR16 (memory address register bit 16)	Program read/write, cleared by processor bus reset. This bit is used in conjunction with standard memory address register outputs (MARnn) to expand DMA addressing capability to 64K words (128K bytes).
02	MAR17 (memory address register bit 17)	Program read/write, cleared by processor bus reset. This bit is used in conjunction with standard memory address register outputs (MARnn) to expand DMA addressing capability to 128K words (256K bytes).
03	MODE+ (DMA I/O mode)	Program read/write, cleared by processor bus reset. When set (bit = 1), indicates input operation (word transfers from GRAPHIC 8 to the host computer). When cleared (bit = 0), indicates output operation (word transfers from host computer to GRAPHIC 8). The GCP writes this bit before a DMA sequence after decoding message header instructions, and leaves it unchanged until the DMA sequence is completed.

Table 3-6. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
04	DMAC+ (DMA complete)	Program read-only, cleared by processor bus reset or by start of DMA sequence. Normally set condition (bit = 1) is cleared when sequence decoder activates status bit 08 (word count ≠ 0) and remains cleared until the write-status clock signal triggered by end of DMA sequence finds status bit 08 returned to normal inactive state (word count = 0). Also receives set command with activation of input interrupt request (IINT-) from sequence decoder (effective only if status bit 08 is low and sequence decoder is not at State 0).
05	OWR+ (output word received)	Program read/write (set only), cleared by processor reset. The sequence decoder sets this bit to acknowledge receipt of host-output data announced by an active OCTL± (output control) handshaking signal from host computer before each output-word transfer. When set, the OWR+ bit sets up the I/O transfer timing logic for output-transfer operation and triggers a 150-nanosecond ODR± (output data received) pulse to the host computer. This bit is cleared when status register bit 07 is deactivated by termination of OCTL± in response to either OWR± signal or associated ODR± pulse.
06	EOUT+ (enable output interrupt)	Program read/write, cleared by processor bus reset. This bit can be programmed as required to enable (set) or mask (reset) output interrupts initiated by host computer announcement of output data. When set (bit = 1), this bit enables generation of GCP output interrupt when the sequence decoder is stepped to State 9 by an initial OCTL± handshaking signal from the host computer or following completion of a DMA output-transfer sequence.
07	SYOC+ (synchronized output control)	Program read-only, cleared by processor bus reset. This bit is set following detection of an active OCTL± (output control) output from the host computer, and remains set until that OCTL± signal is deactivated. While set (bit = 1), SYOC+ establishes output-transfer setup conditions and releases OWR-generation and certain interrupt generation functions; when reset (bit = 0), SYOC+ clears OWR+ signal (bit 05) and same interrupt functions.

Table 3-6. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
08	WC≠0 (word count ≠ zero)	Program read-only, cleared by processor bus reset. This bit reflects the sign bit of the word count register and is set whenever that register is loaded with any two's complement value designating an absolute number of DMA-block words remaining to be transferred. It is cleared when the word count register is incremented to zero value, indicating that all DMA block words have been transferred.
09	ATN1+ (attention #1)	Program read-only. ATN1+ reflects the state of a host computer signal called ATN1±, and allows the host computer to provide any applicable handshaking condition or timing signal. For some host computers, ATN1+ is associated with a host-initiated interrupt triggered on circuits added to the standard parallel interface.
10	ATN2+ (attention #2)	Program read-only. ATN2+ reflects the state of a host computer signal called ATN2±, and allows the host computer to provide any applicable handshaking condition or timing signal. For some host computers, ATN2+ is associated with a host-initiated interrupt triggered on circuits added to the standard parallel interface.
11	Spare attention interrupt enable	Program read/write, cleared by processor bus reset. Spare can be programmed as required. Not used for the standard interface card, this bit is normally reserved as an enabling bit for any attention-interrupt circuit that might be added as a circuit modification for a specific host computer.
12	IMR+ (input message request) (spare bit #2) (TEST2- OUT)	Program read/write, cleared by processor bus reset. This bit can be programmed as required and presents an IMR± signal to the host computer. When J2/J3 test strap is connected, this signal enables/inhibits reset of OWR flip-flop.
13	IWR+ (input word request)	Program read/write, cleared by processor bus reset. For single-word input transfers, the GCP loads the input data word into the host input data register, then sets this IWR+ bit to announce data availability. For DMA input transfers, the parallel interface bus control logic initiates a memory transfer to DAnn-B data to the IDnn± interface bus, then sets this IWR+ bit. In either case, the sequence decoder clears this IWR bit when the host computer activates its ICTL± handshaking signal to confirm data receipt.

Table 3-6. Parallel Interface Status Register Bit Description (Cont)

BIT	IDENTIFICATION	DESCRIPTION
14	EINP+ (enable input interrupt)	Program read/write, cleared by processor bus reset. EINP+ can be programmed to enable (set) or mask (reset) GCP input interrupts initiated by host computer command for input data. When set (bit = 1), EINP+ enables generation of a GCP input interrupt when the sequence decoder is stepped to State 7 by activating the ICTL+ handshaking signal from the host computer for each single-word input transfer, or following the final input transfer of a DMA input-transfer sequence.
15	INR+ (input busy)	Program read-only, cleared by processor bus reset. When high, INR+ indicates a transfer of GRAPHIC 8 data to the host computer is in process. The bit goes active when status bit 13 (IWR+) is set, indicating that DAnn-B data have been loaded into the host input data register and are available on the IDnn+ interface bus. The INR+ stays active until the host computer terminates the ICTL+ handshaking signal to announce receipt of the data word.

3.5.4.3 Single Word Output Transfers. Output transfers are either single word transfers (comprising commands to the GCP) or multi-word transfers (comprising complex instructions or data).

Table 3-7 shows the sequence of events for single-word output transfers; refer also to figures 3-13 and 3-14.

Table 3-7. Single-Word Output Transfer Sequence

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
Places 16 bits of data on ODnn+ interface data bus, activates OCTL+ line.	Change from State 0 to State 9, primes interrupt circuit.	Sends regular IREQ-D pulse.
	On receipt of IREQ-D, sends INLx-B to display processor (if status bit ST06 was previously set). Changes from State 9 to State 10.	Receives INLx-B, generates IENA-D.
	Seizes processor bus, sends INLx-B, sends trap address 000124_8, sends IADV-B.	Reads trap address, terminates IENA-D

Table 3-7. Single-Word Output Transfer Sequence (Cont)

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
	Releases bus.	Stores the address of the next instruction it was going to execute. Branches to output interrupt handling subroutine. Sends data read instruction to parallel interface.
	Passes ODnn± data to DAnn-B processor bus.	Reads data. Sends new status word to parallel interface with bit ST05 set.
	Sends OWR± and ODR± to host computer.	
Terminates ODnn± and OCTL±.	Terminates OWR±, changes from State 10 to State 0.	

At this point the host computer could initiate another output transfer, using the same procedure.

NOTE

If the GCP leaves parallel interface status bit ST06 high, each new word initiates a new GCP interrupt sequence, as described in table 3-7. For some applications, however, GCP deactivates status bit ST06 and simply monitors the state of status bit ST07 to determine when the next OCTL± condition occurs. The GCP then performs the same sequence.

3.5.4.4 DMA Output Transfers. In the case of a multi-word transfer, the first word is a message header, describing the function of the message. The second word normally contains the GCP memory address argument for the message string. The third word is the word count, specifying the number of words in the remainder of the output message.

Table 3-8 shows the sequence of events; refer also to figure 3-13.

Table 3-8. DMA Output Transfer Sequence

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
Sends OCTL$\underline{+}$ and first word as in table 3-7.	Passes first word to display processor as in table 3-7.	Reads header of output message, makes DMA decision. Responds as in table 3-7.
Sends OCTL$\underline{+}$ and second word as in table 3-7.	Passes second word to display processor as in table 3-7. Stores address in its memory address register.	Tells parallel interface to store the data in its memory address register. Responds to host computer as in table 3-7.
Sends OCTL$\underline{+}$ and third word as in table 3-7.	Passes third word to display processor as in table 3-7. Stores two's complement value of word count in its word count register. WC$\neq$0 goes high, status bit ST08 goes high. NOTE This completes the setup for DMA operation.	Tells parallel interface to store the data in its word counter register.
Sends OCTL$\underline{+}$ and next data word.	Bypasses interrupt loop. Changes from State 0 or State 10 to State 1. Status bit ST04 goes low. Seizes control of processor bus. Changes from State 1 to State 2. Places contents of memory address register on ADnn-B bus; connects ODnn$\underline{+}$ to DAnn-B bus. Initiates low ADRV-B on processor control bus.	

Table 3-8. DMA Output Transfer Sequence (Cont)

HOST COMPUTER	PARALLEL INTERFACE	DISPLAY PROCESSOR
	Changes from State 2 to State 3. Status bit ST05 goes high, activating OWR+ and ODR+ handshaking signals to host computer.	
	Increments memory address register by two, increments word count register by one, and changes from State 3 to State 10.	
Deactivates OCTL+	Status bit ST07 goes low, OWR+ terminates. Changes from State 10 to State 0.	
	NOTE This sequence repeats until the host computer has sent the number of words specified in the setup instructions. When the parallel interface word count register returns to zero, status bit ST04 goes high, initiating another interrupt to the display processor.	
	Sends INLx-B, sends trap address 000124_8, sends IADV-B to display processor.	Reads trap address, terminates IENA-D.
	Releases processor bus.	Recognizes that DMA sequence is complete, resumes normal operation.

3.5.4.5 Single Word Input Transfer. Input transfers are either single word transfers or multi-word transfers.

Table 3-9 shows the sequence of events for single-word input transfers; refer also to figures 3-13 and 3-15.

Table 3-9. Single-Word Input Transfer Sequence

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
Places data word on DAnn-B lines, sends write data instruction.	Stores DAnn-B word in input data register, connected to IDnn+ interface bus.	
Places new status word on DAnn-B bus; bits ST03 and ST13 high. Sends write status instruction.	Loads status word into status register. Sends IWR+ handshaking signal to computer. Status bit ST15 goes high. Parallel interface remains in State 0.	Sends ICTL+ when ready to accept input data.
	Changes from State 0 to State 5. Sends NDRY+ pulse (150 ns) to computer, clearing IWR+. Changes from State 5 to State 6.	Reads IDnn+, deactivates ICTL+.
	When ICTL+ is deactivated, status bit ST15 goes low, parallel interface changes from State 6 to State 7. If status bit ST14 is high, sends interrupt to display processor, then changes to State 0. Interrupt trap address is 000120_8.	
Reads trap address. Executes parallel interface read status. If status bit ST15 is low, sequence is complete.		

At this point the display processor could initiate another input transfer, using the same procedure.

3.5.4.6 DMA Input Transfers. In the case of a multi-word transfer, the first word is a message header, the second word is the source address, and the third word is the word count.

Table 3-10 shows the sequence of events; refer also to figure 3-13.

Table 3-10. DMA Input Transfer Sequence

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
Sends first word as in table 3-9.	Passes first word to host computer as in table 3-9.	Reads first word as in table 3-9.
Sends second word as in table 3-9.	Passes second word to host computer as in table 3-9.	Reads second word as in table 3-9.
Sends third word as in table 3-9.	Passes third word to host computer as in table 3-9.	Reads third word as in table 3-9.
Places read/write memory start address on DAnn-B lines; executes write address instruction. If address bits AD16 and AD17 are required, loads these into status register as status bits ST01, ST02 with a separate write status instruction.	Loads start address into its memory address register (and status register if needed).	
Places two's complement of remaining word count on DAnn-B lines; executes write word instruction.	Loads word count value into word count register. WC≠0 goes high.	
Places new status word on DAnn-B lines; executes write status instruction. Status bit ST03 is high.	Changes from State 0 to State 1. Bypasses interrupt loop. Seizes control of processor bus.	
	Changes from State 1 to State 2. Places contents of memory address register on ADnn-B lines. Connects DAnn-B response from memory to IDnn+ lines. When memory sends MEMA-B, parallel interface sends IWR+ to host computer.	

Table 3-10. DMA Input Transfer Sequence (Cont)

DISPLAY PROCESSOR	PARALLEL INTERFACE	HOST COMPUTER
	Changes from State 2 to State 3, increments memory address register by two, increments word count register by one. Changes from State 3 to State 4, waiting for host computer to respond to IWR±.	Activates ICTL± handshaking line.
	Changes from State 4 to State 5. Sends 150-ns NDRY± pulse to host computer, terminates IWR±. Changes from State 5 to State 6.	Terminates ICTL±.
	If WC≠0, goes back to State 1.	
	If WC=0, changes from State 6 to State 7. Sends input interrupt to GCP, returns to State 0.	

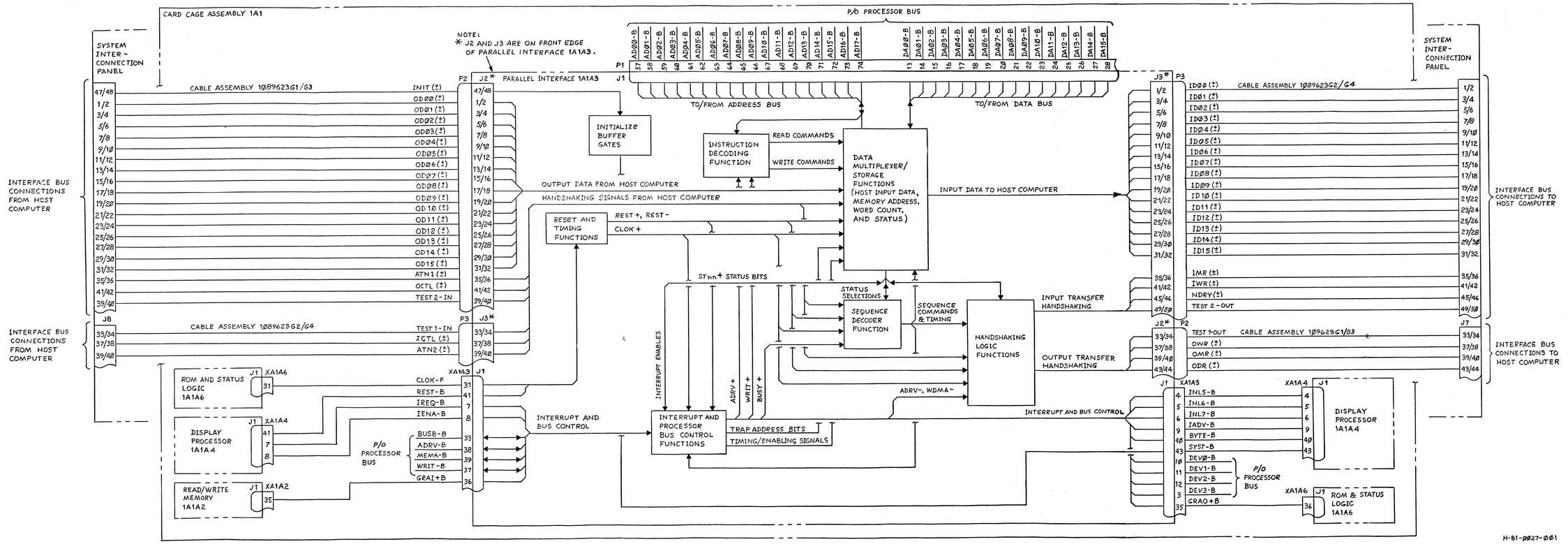

Figure 3-12. Parallel Interface Block Diagram

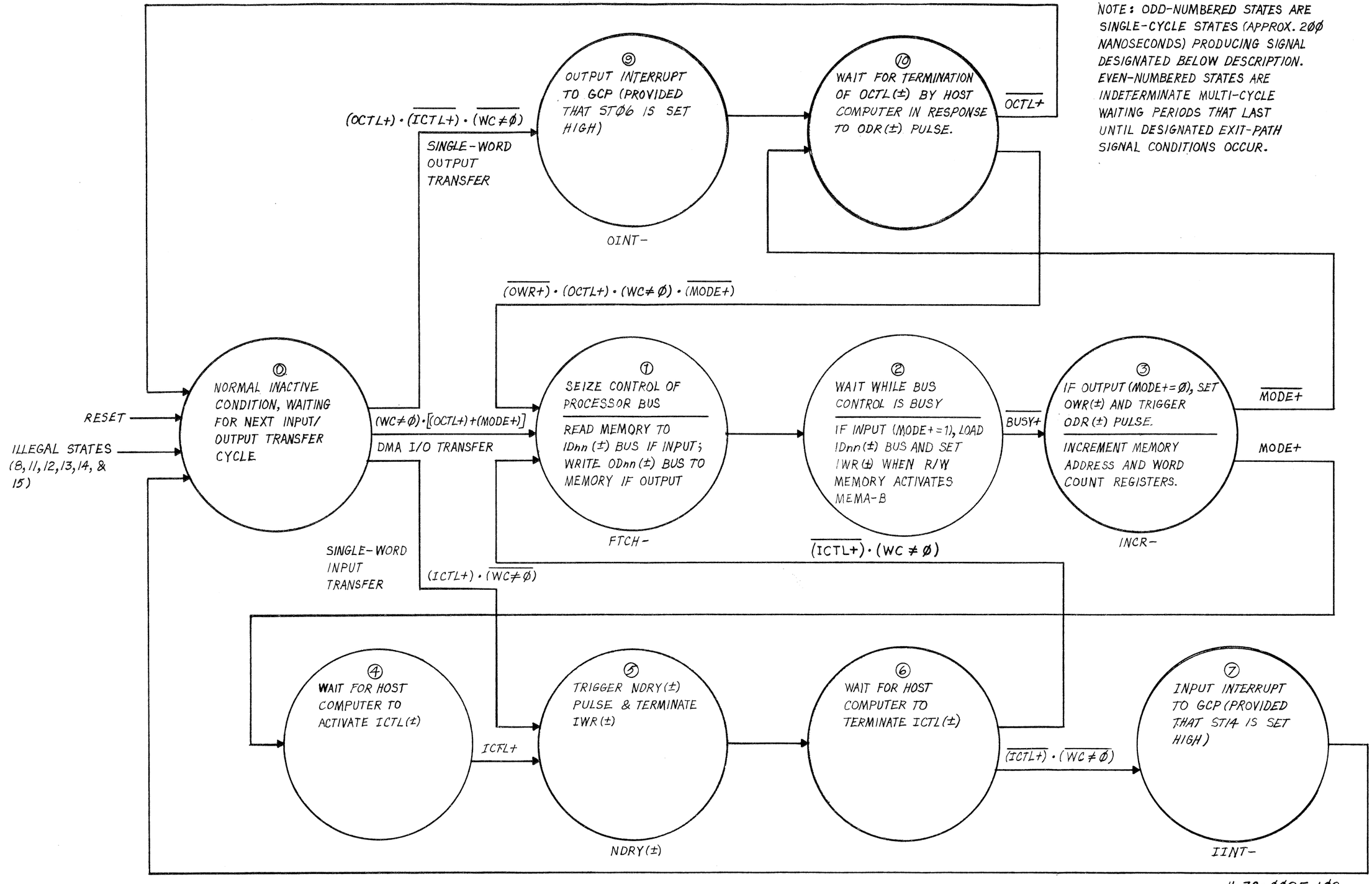

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Figure 3-13. Parallel Interface State Diagram

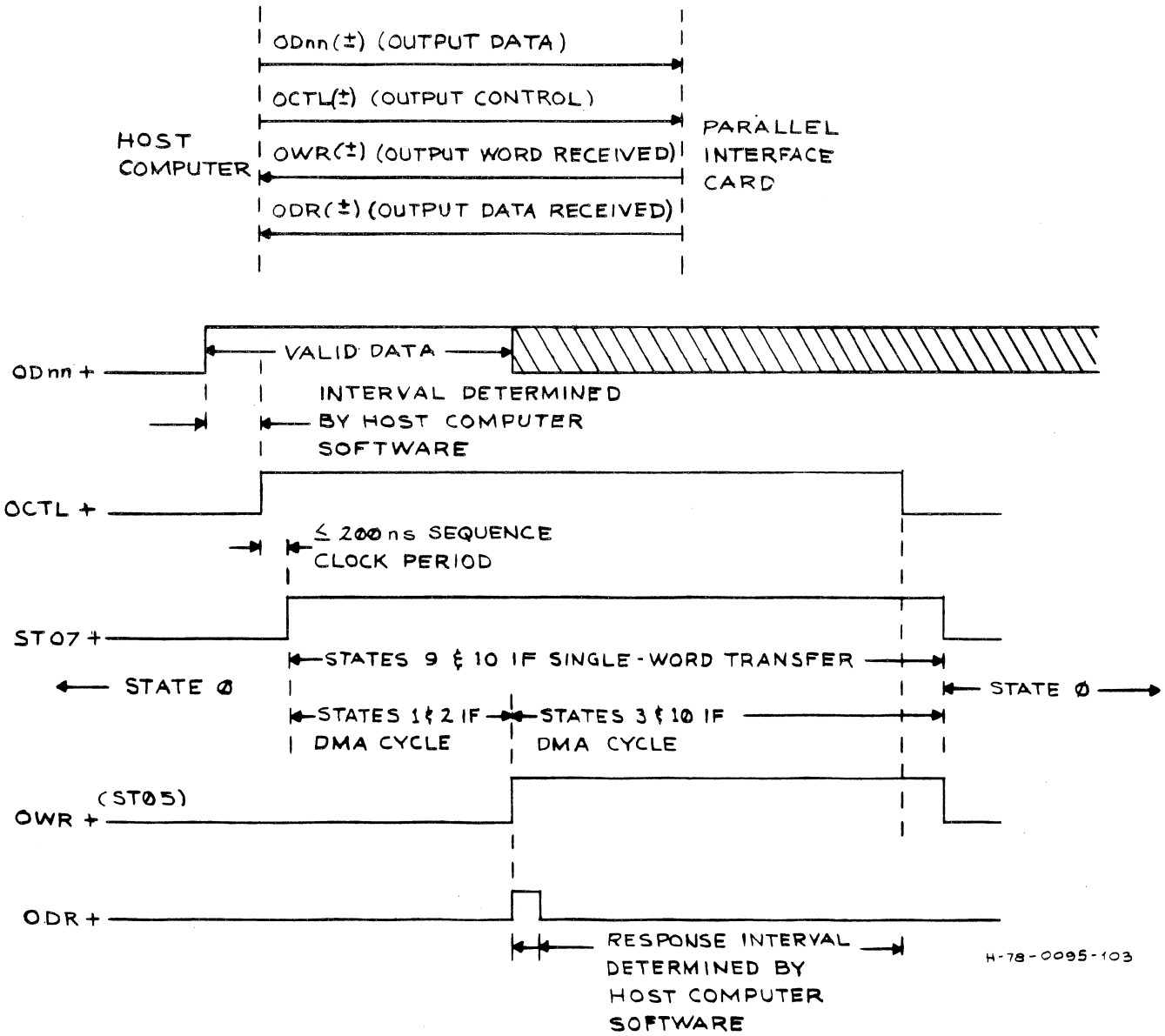


Figure 3-14. Parallel Interface Output Transfer, Timing Diagram

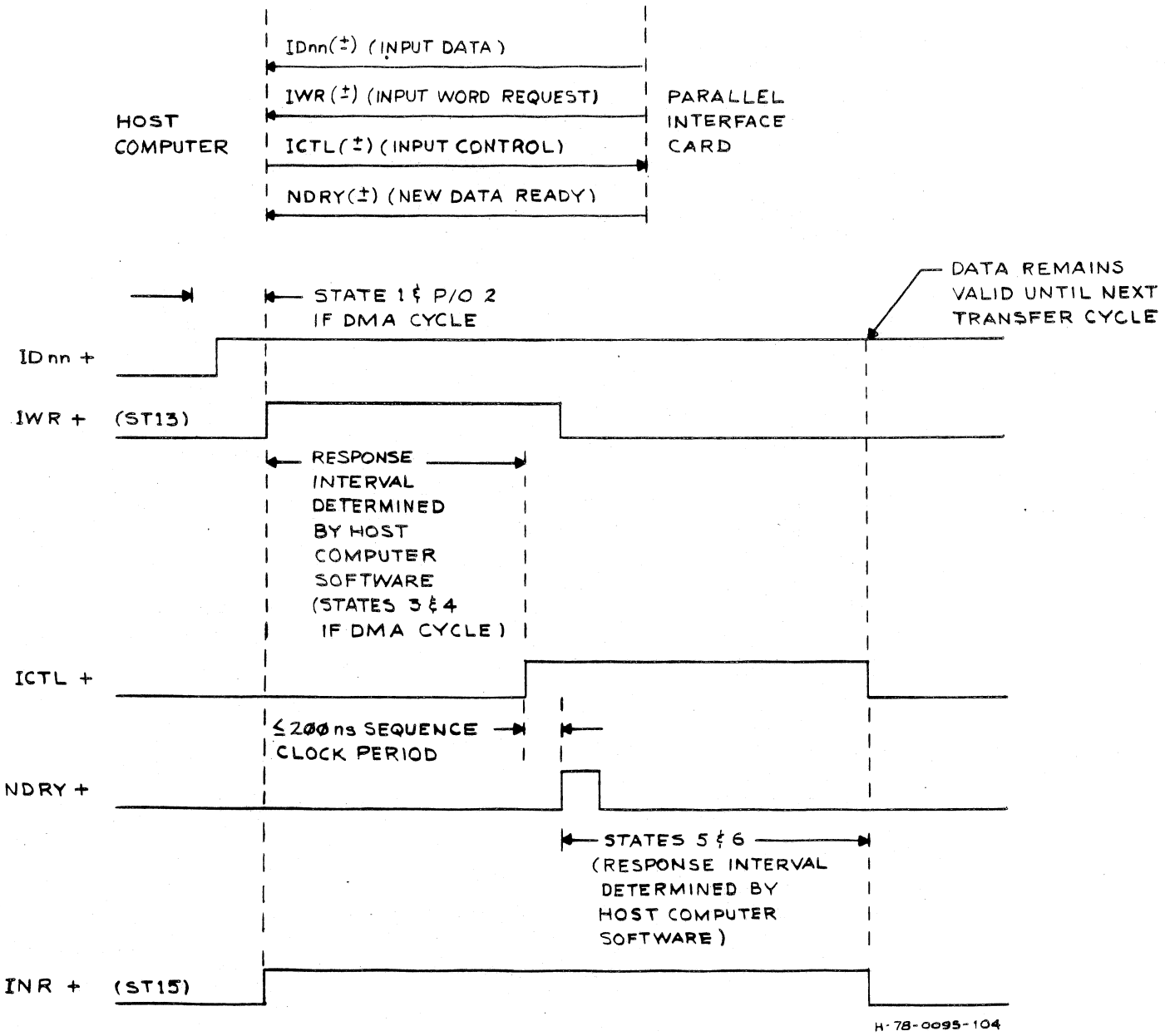


Figure 3-15. Parallel Interface Input Transfer, Timing Diagram

727-J5-PORT 3

3.6 MULTIPORT SERIAL INTERFACE

The multiport serial interface is an optional circuit card that provides four separate interface channels for communications between the terminal controller (which uses parallel data) and up to four peripheral equipments that use serial data. Such equipment might be a host computer, communications modem, high speed tape reader, alphanumeric and function keyboards, or position entry devices (trackball/forcestick/data tablet).

Each communication channel is called a "port", which refers both to a connector on the front edge of the card and to the associated channel circuitry. Each port handles input transfers from the connected peripheral equipment to the terminal controller, and output transfers from the terminal controller to the external equipment.

The ports are designated 1 through 4. The port 1 circuitry can handle simple asynchronous I/O transfers and full RS-232-C communications. Ports 2, 3, and 4 handle only simple asynchronous I/O transfers. See figure 3-17.

Each port contains a universal asynchronous receiver/transmitter (UART). The port 1 channel connects to two edge-mounted connectors: J2 and J3. Connector J2, a 26-pin connector, handles all RS-232-C data and handshaking control lines needed for synchronous or asynchronous operation, in full-duplex or half-duplex modes. Connector J3, a 10-pin connector, handles asynchronous serial data transfers. Connector J3 supplies operating power ($\pm$15V, +5V and ground return), three discrete signal lines (serial input, serial output, and reader-enable confirmation), and shielded return lines for the three discrete signals. (The shields are connected together.) The I/O lines on J3 have a standard configuration for RS-232-C, but can be reconfigured for TTL logic levels.

Ports 2, 3, and 4 connect to the same type of 10-pin I/O connector as J3. The connectors for ports 2, 3, and 4 are J4, J5, and J6 respectively. The I/O lines for ports 2, 3, and 4 have a standard configuration for RS-232-C but can be reconfigured for TTL logic levels.

Each UART (see figure 3-16) contains:

1. A receiver shift register, which accepts serial character data inputs on a discrete line from the external equipment and produces various condition signals.

2. A receive buffer register, which holds the received character data until an associated control circuit requests parallel format readout.

3. A transmit buffer register, which accepts parallel character data output from the terminal controller processor bus and produces a busy/empty signal.

4. A transmitter shift register, which can be commanded to accept the data stored in the transmit buffer register and shift it out serially on a discrete line to the external equipment.

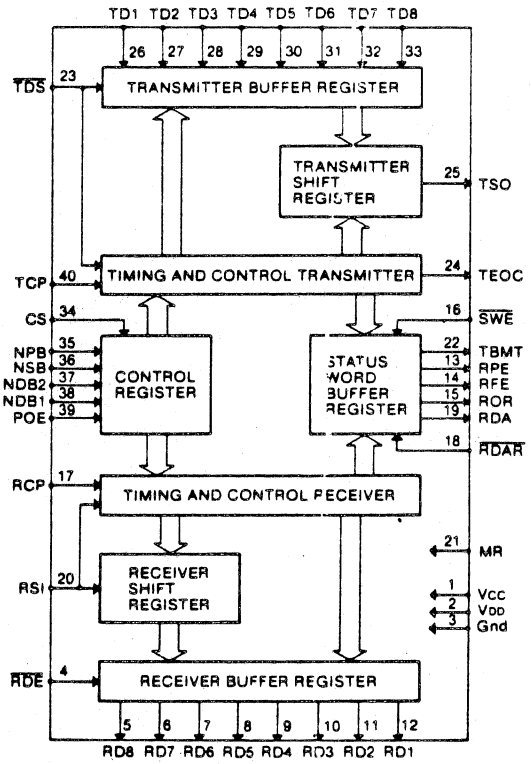


Figure 3-16. UART Functional Block Diagram

3.6.1 MAJOR CIRCUITS

Address Decoder. This circuit recognizes when the serial interface is being addressed by another card in the terminal controller. Address bits AD06-B through AD17-B make up the card address code: $1765XX_8$.*

Bits AD03-B through AD05-B select channels 1 through 4.

Bits AD01-B and AD02-B select one of the four UART register functions for the addressed channel.

Table 3-11 lists the 16 addresses for the serial interface card. Table 3-11 also contains the following information.

1. The register mnemonics.

2. The vector trap addresses sent to the display processor when the serial interface generates an interrupt.

*When the expand switch (U19-S8) is closed, the card address becomes $1766XX_8$. GCP at present does not support this address.

Table 3-11. Multiport Serial Interface Devices

CARD	PORT	OCTAL ADDRESS	REGISTER MNEMONIC	VECTOR TRAP ADDRESS RECEIVE	VECTOR TRAP ADDRESS TRANSMIT	ASSOCIATED EXTERNAL DEVICE	CARD CONNECTOR
	1	176500	RSR1	300		Communicator 1	J2 or J3
		176502	RDB1, PCR1			(RS-232-C 1,	
		176504	TRS1		304	asynchronous)	
		176506	TDB1				
	2	176510	RSR2	310		Spare	J4
		176512	RDB2				
		176514	TSR2		314		
		176516	TDB2				
	3	176520	RSR3	320		Keyboard 1	J5
		176522	RDB3				
		176524	TSR3		324		
		176526	TDB3				
	4	176530	RSR4	330		PED 1	J6
		176532	RDB4			(trackball,	
		176534	TSR4		334	forcestick, or	
		176536	TDB4			data tablet)	

3. The type of external equipment that may be connected by each interface port. The GCP always assumes that this is the type of equipment that is connected to a given port.

NOTE

The device address switches on the serial interface card let you change the port identification on a card. For example, you could connect two keyboards and a hardcopy unit to a single serial interface by identifying the channels as ports 3, 5, and 7. See Section 4 for instructions.

Devices Switches. Switches U19 and U39, consisting of eight SPST switches each, perform the following functions:

1. They configure the serial interface ports to accommodate specific peripheral devices.

2. U19-S8, when closed, changes the card address from 1765XX to 1766XX.

3. U39-S7, when open, disables the DTRY+ function at connector J2.

Table 3-12 lists the device assignments for each port. When setting up these assignments, do not use the same switch settings for more than one port; only the lowest numbered port will respond to the device.

Table 3-12. Serial Interface Port Device Assignments

DEVICE	PORT 1 (U19) S1	S2	S3	PORT 2 (U19) S1	S2	S3	PORT 3 (U39) S1	S2	S3	PORT 4 (U39) S1	S2	S3
Communicator (RS-232-C)	On*	On*	On*	-	-	-	-	-	-	-	-	-
Keyboard #1	On	Off	On	On	Off	On	On*	Off*	On*	On	Off	On
PED #1	On	Off	Off	On	Off	Off	On	Off	Off	On*	Off*	Off*
Hardcopy	Off	On	On	Off	On	On	Off	On	On	Off	On	On
Keyboard #2	Off	Off	On	Off	Off	On	Off	Off	On	Off	Off	On
PED #2	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
Spare #1	On	On	Off	On*	On*	Off*	On	On	Off	On	On	Off
Spare #2	Off	On	Off	Off	On	Off	Off	On	Off	Off	On	Off

*These are the nominal switch settings. Unless otherwise specified by the customer, switches are set to these positions at the factory.

Read/Write Decoder. This circuit responds to the selected address code and the states of the WRIT+ and ADRV+ signals to generate specific command signals at specific times. These command signals control the actions of other circuits throughout the serial interface card.

Mask Register. This circuit responds to the selected address code and the state of input data bit ID06+. When this bit is high, the mask register puts a high on one of eight lines that go to both the priority encoder and the status register.

This circuit lets the programmer determine which conditions will and will not cause interrupts to be generated.

Status Register. This circuit receives the eight lines from the mask register, plus the TRYX+ and DRYX+ signals from each of the four UARTs. The register is addressed by three bits from the address decoder and strobed by RIOR- from the read/write decoder. The output of the status register consists of four bits (OD04+ through OD07+) which, after inversion, go back to the display processor card on the terminal controller data bus. (Bits OD04+ and OD05+ are low.) The bits tell the display processor the current status of the serial interface.

Interrupt Status Register. This circuit receives the eight lines from the mask register and is clocked by any of the DRYX+ or TRYX+ signals from the four UARTs. The eight outputs from this register go to the priority encoder.

Priority Encoder. This circuit decodes the eight lines from the interrupt status register. If one of the mask register bits is active, the priority encoder sets the FLAG+ lines to the bus control circuit, generating an interrupt.

The 3-line coded output of the priority encoder is latched by the GRAB+ signal and passed to the reset decoder and the trap address encoder.

Bus Control Circuit. The bus control circuit operates as described in paragraph 3.3

Reset Decoder. This circuit decodes the latched output of the priority encoder to reset the interrupt status register.

Trap Address Encoder. This trap address encoder is a multiplexer. The switched inputs are twelve DSXX+ signals from the device switches, which identify the type of device connected to each port of the serial interface. Two outputs from latch U58 select three bits as the output of the trap address encoder. The BUSC- signal strobes the trap address encoder, making those three bits available as output bits OD03+, OD04+ and OD05+.

In addition, bits OD00+ and OD01+ are low, and a third output from latch U58 passes as bit OD02+. After inversion, these bits go back to the display processor on the terminal controller data bus.

Baud Rate Generator and UARTs. Baud rate generator U79 is a clock generator with a fundamental frequency of 5.0688 MHz. The nominal output frequency (fT) is 153.6 kHz, corresponding to a baud rate of 9600.

The fT signal goes to the UARTs for ports 2, 3, and 4. The fT baud rate can be changed by changing the jumpers at the T-terminals of the baud rate generator. Refer to Section 4 for details.

The fR output of the baud rate generator goes to the UART for port 1. The nominal frequency for this terminal is also 153.6 kHz, corresponding to a baud rate of 9600. The fR baud rate can be changed by changing the settings of switches S4 through S7 on chip U80. Refer to Section 4 for details.

Each UART performs all the receiving and transmitting functions associated with asynchronous data communications. External connections give control over duplex mode, baud rate, data word length, parity mode, and the number of stop bits. The following paragraphs describe its operation.

The clock frequency is always 16 times the baud rate.

1. Transmitting. The UART is reset at power turn-on. Under these conditions, TBMT (transmitter buffer empty) and TSO (transmitter serial output) are both high.

When TBMT is high, the data bits may be set. The bits ID00+ through ID007 are applied to the UART's TR-terminals and strobed in by the WDBX- pulse at the $\overline{\text{TDS}}$ terminal. At this time TBMT goes low, indicating that the data bits buffer register is full and unable to accept additional data.

If the transmitter shift register is still sending previously loaded data, TBMT remains low. If the transmitter shift register is empty, or when it is through sending the previous character, the data in buffer register is loaded immediately into the transmitter shift register and data transmission starts. TSO (transmitter serial output) goes low and TBMT goes high.

If new data is loaded into the transmitter buffer register at this time, TBMT goes low again and stays low until the present transmission is completed.

Data transmission proceeds in this manner: start bit, data bits, parity bit (if selected), and the stop bit(s). If TBMT is low, transmission of the next character begins immediately. If TBMT is high, the transmitter is completely at rest.

2. Receiving. The UART is reset at power turn-on. Under these conditions, RDA (receiver data available) is low.

Data reception starts when the serial input line (RSI) goes low. The first bit received is a start bit, and must remain low for at least one-half a bit time. After the start bit has been received and verified, data transmission proceeds in this manner: data bits received, parity bit received (if selected), and stop bit(s) received.

If the transmitted parity bit does not agree with the received parity bit, the RPE (received parity error) line is set high. If no parity mode is selected, RPE is held low.

After a full character has been received, RDA goes high. At this time a low RDBX- signal at the UART's $\overline{\text{RDE}}$ terminal enables the outputs at the RR-terminals. The received data (0D00+ through 0D07+), after inversion, goes onto the terminal controller data bus.

If a character is transferred into the receiver buffer register before the previous character was read, the ROR (receiver overrun) output goes high.

A low RDYX- pulse must be applied to the UART's $\overline{\text{RDAR}}$ (receiver data available reset) terminal to clear RDA.

3. Options. Switches S1 through S3 of chip U80 give you the option to select certain features with respect to the port 1 UART only.

When switch S1 is open, no parity bit is sent on transmission; the stop bit follows the last data bit. No parity bit is expected during receiving; the stop bit(s) must follow immediately after the last data bit. The RPE signal is held low. The NDB1 (number of data bits per character) line is held high, and in conjunction with the high NDB2 line selects 8 bits per character.

When switch S1 is closed, the parity circuit is enabled for odd or even parity, depending on the setting of switch S2, and the number of bits per character is 7.

When switch S1 is closed, an open switch S2 selects even parity; closing switch S2 selects odd parity.

Switch S3 selects the number of stop bits. Opening switch S3 selects two stop bits; closing switch S3 selects one stop bit.

Status Multiplexer. The status multiplexer detects any parity error condition or receiver overrun condition in the UARTs and reports such an error by a 3-bit code when addressed.

Readers Enable Register. These flip-flops are preset by the SREX- signals from the read/write decoder and produce the RENX- signals that allow an automatic external device (such as a tape reader) to advance to its next cycle. The circuit is cleared by the start bit when the external device sends a word.

Break and Loopback Decoders and Multiplexer. These circuits are used during tests of the serial interface card. When the break decoder is turned on, it causes a continuous SPACE on the data line, simulating the BREAK key of a teletypewriter.

When loopback decoder is turned on, its output signal LDXX+ causes the gate in the UART RSI lines to accept the data that was sent on the UART TSO lines. This feature makes it unnecessary to use external test plugs when making loopback tests.

The multiplexer, when addressed, reports the status of these devices in the form of four bits, OD00+ through OD03+.

Receiver Status Register. This circuit is involved only when transmitting to a device connected to the port 1 J2 connector. When programmed by two IDXX+ instruction bits, it activates the DTRY+ (data ready) and/or RQTS+ (request to send) lines, and reports its status in the form of three bits, OD01+ through OD03+.

3.6.2 OPERATION

3.6.2.1 Definitions of Bits. In general, communications between the display processor and the serial interface takes place in the form of "register words". Before the serial interface can pass data from an external device to the terminal controller data bus, the display processor must have prepared the serial interface to receive such data. Similarly, before the serial interface can pass data from the data bus to an external device, the display processor must have prepared the serial interface to transmit such data.

In addition, the display processor can read the status of the serial interface at any time by sending an appropriate read instruction; the serial interface responds in the form of a register word that contains the desired information.

1. Transmitting. Before the serial interface can pass data from the data bus to an external device, the display processor must prepare the serial interface to transmit such data.

The display processor sends a TSRn (transmit status register) word to one of the addresses listed in table 3-11. To do this, the display processor places the appropriate instruction on the data bus, places the appropriate address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

The following instructions are possible:

Data bit 00, when active, enables the break decoder, causing the affected channel to send a continuous SPACE on the data line, simulating the BREAK key of a teletypewriter.

Data bit 02, when active, enables the loopback decoder, bypassing the external device and connecting the UART output of the affected port to the UART input.

Data bit 06, when active, allows an interrupt to be generated when the UART sends a word to the external device and is ready to accept another word.

After the serial interface has been set up to transmit, the display processor sends the data to be transmitted in the form of a TBDn (transmit data buffer) word, to the appropriate address (see table 3-11). To do this, the display processor places the appropriate data on the data bus, places the address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

Data bits 00 through 07 contain the information to be passed to the external device.

2. Receiving. Before the serial interface can pass data from an external device to the data bus, the display processor must prepare the serial interface to pass such data.

This display processor sends a RSRn (receive status register) word to one of the addresses listed in table 3-11. To do this, the display processor places the appropriate instruction on the data bus, places the appropriate address on the address bus, then activates the address valid signal ADRV- and the write command WRIT-.

The following instructions are possible:

Data bit 00, when active, causes the SREX- signal to be generated, which places a ground on the RENX- pin of the addressed port. This ground is automatically cleared when the external device sends a start bit to the serial interface.

Data bit 01, when active, sets the DTRY+ (data terminal ready) line of the port 1 26-pin connector. It applies to port 1 only.

Data bit 02, when active, sets the RQTS+ (request to send) line of the port 1 26-pin connector. It applies to port 1 only.

Data bit 06, when active, allows an interrupt to be generated when the UART receives a word from the external device, and is waiting for that word to be read by the display processor.

After the serial interface has been set up to receive, the external device sends its data word. If the interrupt circuit was primed during set-up, the serial interface sends an interrupt to the display processor. The display processor then sends a RDBn (receive data buffer) command. To do this, the display processor places the appropriate address on the address bus, and activates the address valid signal ADRV-, leaving WRIT- high.

The serial interface responds by sending a 16-bit message, as follows:

Data bits 00 through 07 contain the word received from the external device.

Data bit 12, if active, indicates a parity error in the received data. This bit applies only to communications received through connector J2 of port 1.

Data bit 14, if active, indicates an overrun error (a new word was received from the external device before the display processor read the preceding word).

Data bit 15 becomes active if either data bit 12 or data bit 14 is active.

3. Reading Status. The display processor can read the conditions of the transmit function by sending a TSRn message to one of the addresses listed in table 3-11 with the WRIT- line held high. The serial interface responds by sending the status of bits 00, 02, and 06 as they were set up. In addition, bit 07, if active, indicates that the transmit data buffer in the addressed UART is empty and ready to accept another word.

The display processor can read the conditions of the receive function by sending a RSRn message to one of the addresses listed in table 3-11 with the WRIT- line held high. The serial interface responds by sending the status of bits 01, 02, and 06 as they were set up. In addition:

Bit 07, if active, indicates that the UART has a word in its receive data buffer, waiting to be read.

Bit 09, if active, indicates that the external device has set its DATA SET READY line.

Bit 12, if active, indicates that the external device has set its CARRIER line.

Bit 13, if active, indicates that the external device has set its CLEAR TO SEND line.

Bit 14, if active, indicates that the external device has set its RING INDICATOR line.

NOTE

Bits 09, 12, 13, and 14 apply to connector J2 of port 1 only.

3.6.2.2 Typical Receive Sequence. The serial interface waits in an idle condition until the external device sends a serial word. The UART stores the received word in its receive data buffer and activates its RDA terminal. The DRYX+ signal goes to the interrupt status register and the status register. If the interrupt circuit had been set up, the serial interface generates an interrupt to the display processor, at the same time sending the vector trap address for the device that causes the interrupt.

If the interrupt circuit is not set up, the display processor detects the data ready condition the next time it reads status and discovers bit 07 active.

Either way, the display processor sends a RDBn command. The serial interface responds by sending the data, accompanied by the MEMA-B signal to indicate that the data is stable on the bus. After the display processor reads the data, it terminates ADRV- and the serial interface terminates MEMA-B.

3.6.2.3 Typical Transmit Sequence. The GCP initiates output transfers by placing the 8-bit character data code on the low order byte lines of the data bus, activates the WRIT-B line, places the serial interface address on the address bus, and activates the ADRV-B line.

The character data goes to all four UARTs. The address decoder decodes the port selection code and sends a WDBX- (write data bit) command to the one appropriate UART; this command goes to the UART TDS terminal. The UART responds by sending the output message (one start bit, eight data bits, and one or two stop bits) to the external device; the TBMT (transmitter buffer empty) signal goes low when the data is strobed into the UART and goes high when the character has been sent to the external device.

If interrupt enable bit 06 has been previously set, the serial interface sends an interrupt back to the GCP when TBMT goes high. This interrupt reports completion of the transfer and readiness to transmit another character. The interrupt response sequence produces an appropriate trap vector address, which causes the program to branch to the appropriate data handling subroutine for the selected port.

If the interrupt is disabled (bit 06 cleared), the display processor can read the transmit status word directly to determine if the transmitter ready bit (bit 07) has been set.

3.6.2.4 Modem Operation. Modem operation is only through connector J2 of port 1. Modem operation is generally used for long-distance transfers (via telephone line or rf links). For asynchronous operation, the message code structure is the same as for local asynchronous transfers: a start bit, up to eight data bits, and one or stop bits.

Modem operation protocol requires that:

1. The external device send an active DSRY+ (data set ready) signal to the serial interface.

2. Th GCP set bit 01 of the RSR1 status instruction, to keep the DTRY+ (data terminal ready) signal to the external device high.

The serial interface is always ready to receive data from the external device. However, transfers from the GCP to the external device require that the serial interface send an active RQTS+ (request to send) signal and wait for a CLTS+ (clear to send) reply from the external device.

The external device sends a high CARR+ (data carrier detect) signal to the serial interface as long as detection circuits in the external device find no fault with the quality of the data from serial interface.

The external device produces a RING+ signal that is available to the display processor as status bit 14.

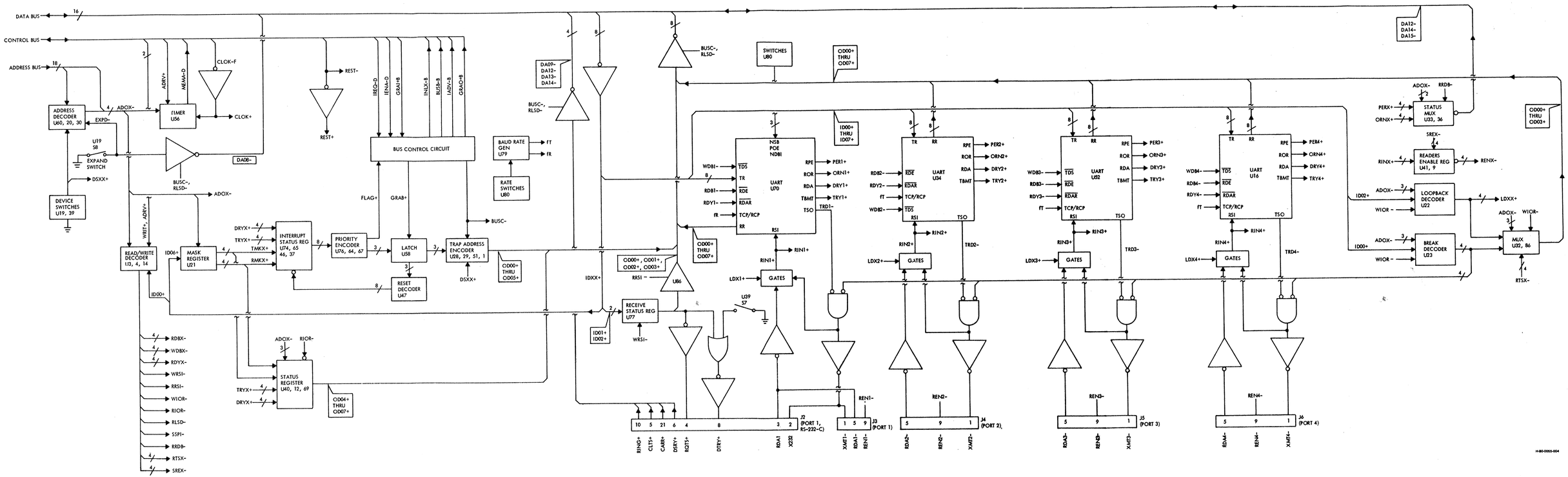


Figure 3-17. Serial Interface, Block Diagram

3.7 DISPLAY PROCESSOR

The display processor (figures 3-18 and 3-19) comprises six logic circuits: input/output, instruction, control, central processing, interrupt, and timing/ miscellaneous. These circuits, which together to emulate a PDP-11 type minicomputer (figure 3-20) are described in the following paragraphs.

Input/Output (I/O) Logic. The I/O logic is the primary interface between the display processor and other circuit cards connected to the processor bus. Input information (data or instruction) for the display processor is applied to the I/O logic on the data lines (DAnn-B) of the processor bus. The I/O logic routes the information to the instruction logic or central processing logic, as appropriate. Similarly, information from the display processor (data or address) intended for other circuit cards is routed from the central processing logic, through the I/O logic, to the processor bus. If it is data, the output information is placed on the processor bus data lines; if it is an address, the information is placed on the processor bus address lines (ADnn-B).

Instruction Logic. This circuit accepts instruction information from the I/O logic, then decodes the data to determine (a) the processor registers to be used and (b) the starting address of the microroutine that will execute the instruction. As required, the decoding operation is modified by decode control inputs from the control logic and by condition code data from the central processing logic. The resulting register selection data goes to the central processing logic while starting address data goes to the control logic.

Control Logic. This circuit determines the specific microinstruction, or series thereof, necessary to execute the macro-instruction decoded by the instruction logic. This is accomplished via a microcontrol program located in a read-only memory (ROM). Execution of an instruction is initiated by application of an address from the instruction logic to identify the proper starting location in the microcontrol program ROM. A counter then causes sequential microcontrol ROM locations to be accessed as necessary to generate the required microinstructions. Simultaneously, decode control signals required for instruction execution are generated and sent to the instruction logic.

The control logic also accepts microcontrol ROM starting locations from the interrupt logic so that microjumps to an interrupt-handling microroutine can be performed. When microroutine execution is required, the control logic sends an enable signal to the interrupt logic which responds by returning the microroutine starting location (microjump address) to the control logic.

Control Processing Logic. This circuit, which contains a 16-bit microcontroller, performs the actual data processing. In response to (a) microinstructions from the control logic, and (b) register select signals from the instruction logic, the microcontroller operates on input data received from the I/O logic and generates output data or an address that is applied to the I/O logic. The central processing logic also generates: (a) condition code signals that are sent to the instruction logic and (b) interrupt priority signals that control interrupt logic operations. As a maintenance aid, the central processing logic generates a DPRN-B (display processor run) signal to indicate that the display processor is operating. This signal lights indicator DS1 on the display processor card and the RUN indicator on the terminal controller front panel.

Interrupt Logic. This circuit monitors: (a) three levels of interrupts (INL5-B through INL7-B) from other circuit cards connected to the processor bus, (b) BTOM-M (bus timeout) signals from the read/write memories, and (c) LOCA-B (local mode) and SYST-B (system mode) commands from interface cards and pushbutton switches. Response to these interrupts is determined by interrupt priority signals from the central processing logic. When an interrupt of higher priority than the display processor is received and the control logic generates a microjump enable signal, the interrupt logic sends a microjump address to the control logic. This microjump address specifies the starting location in the microcontrol ROM of the required interrupt handling microroutine.

Timing and Miscellaneous Logic. This circuit controls the timing and coordination of all display processor functions, monitors status signals on the processor bus, applies status and control signals to the processor bus, and controls initialization of all terminal controller circuit cards.

Timing signals are derived from the CLOK-F (master clock) input from the ROM and status logic card. Normally, this is a 10-MHz signal generated by a ROM and status card circuit, but an optional external clock signal may be used.

Processor bus status signals monitored by the timing and control logic include IADV-B (interrupt address valid), MEMA-B (memory acknowledge), and GRAI+B (grant input). This signals synchronize display processor operations with those of other circuit cards, and indicate when processor bus control has been seized by another card.

When processor-bus control is seized by the display processor, the timing and miscellaneous logic applies bus status and control signals to the bus. These signals include ADRV-B (address valid), WRIT-B (write), BUSB-B (bus-busy), BYTE-B, IENA-D (interrupt enable), IREQ-D (interrupt request); DEVn-B (device code), and GRAO+B (grant output) signals.

Initialization of all terminal controller circuit cards occurs each time primary power is applied to the controller. Applying primary power causes the output channel card to send a TORN-O (turn on) pulse to the timing and miscellaneous logic which then initializes the other display processor circuits and applies a REST-B (reset) pulse to the processor bus to initialize all other terminal controller cards.

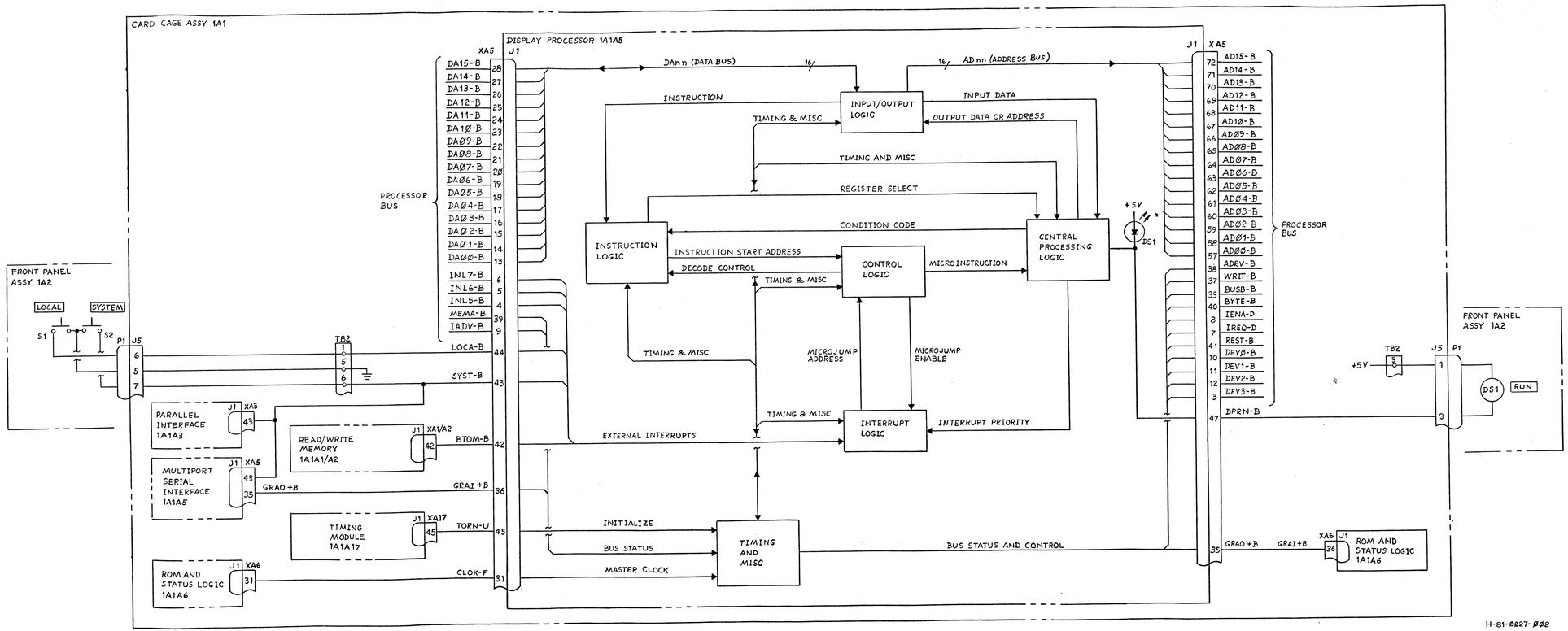


Figure 3-18. Display Processor Block Diagram

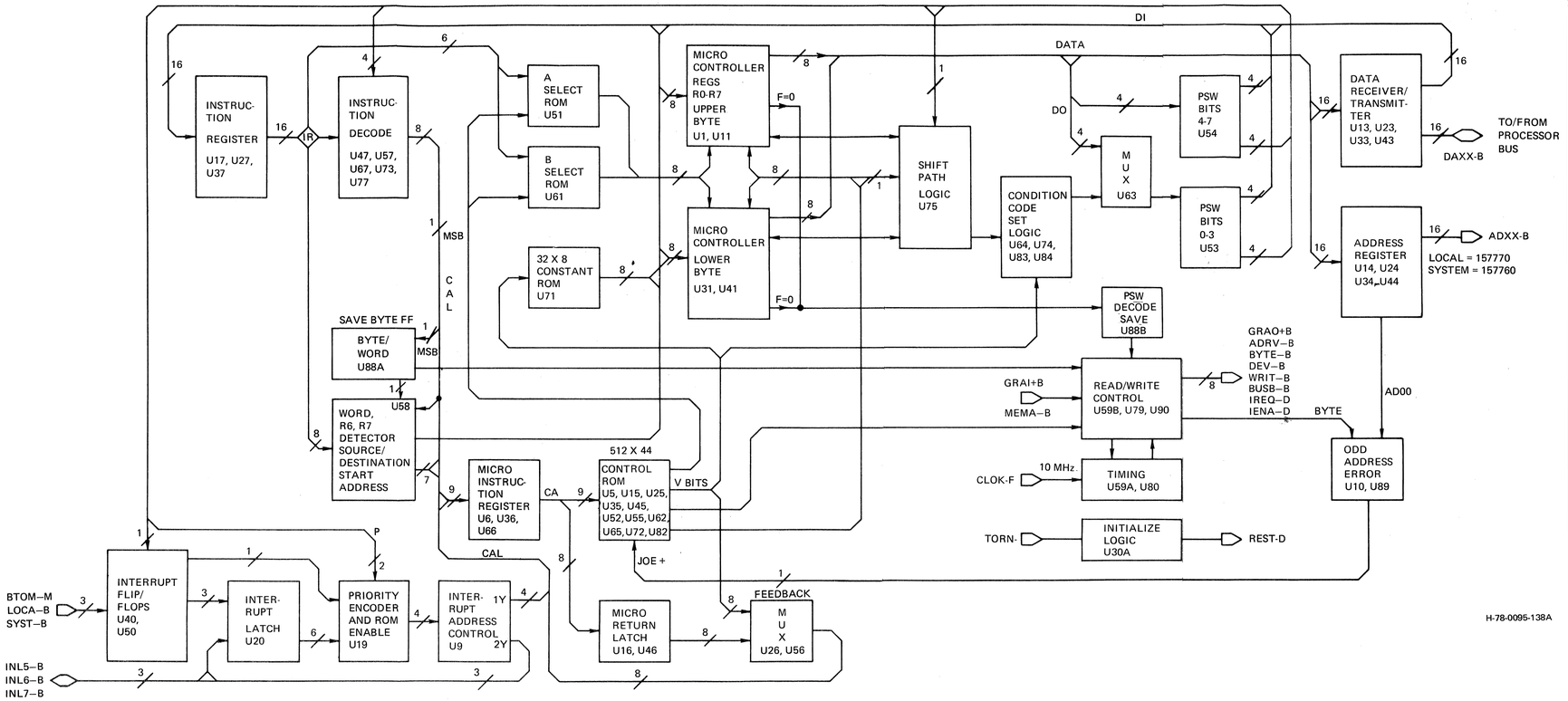


Figure 3-19. Display Processor, Functional Block Diagram

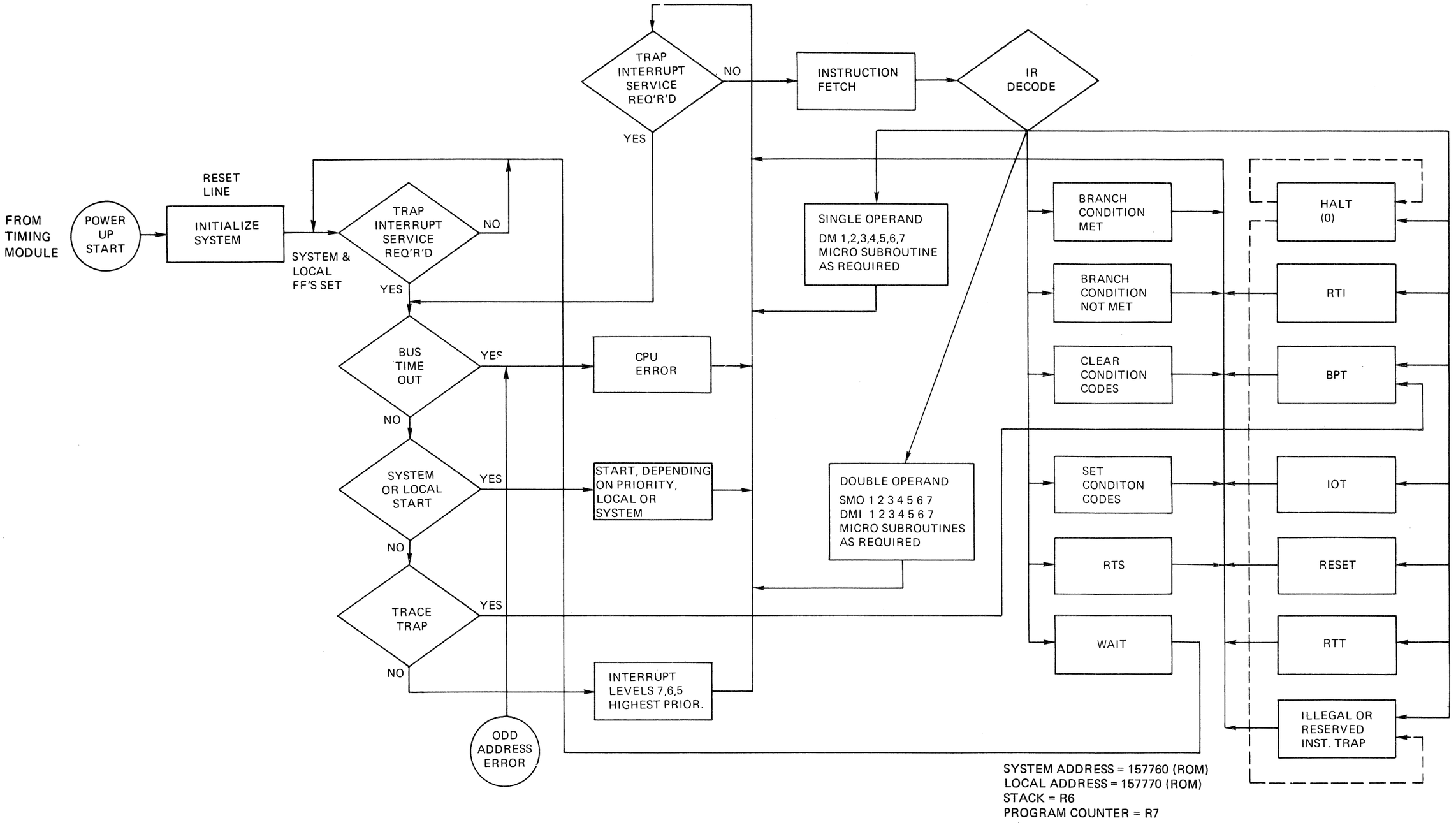


Figure 3-20. Display Processor Flow Diagram

3.8 ROM AND STATUS CARD

The ROM and status card (figures 3-21 and 3-22) contain the ROM-stored GCP macrocontrol programs used by the digital graphic controller and display processor.

The ROM and status card also contains a serial I/O communication circuit that interfaces to external equipment through connector J2. This circuit communicates with a teletypewriter to facilitate diagnostic communications. However, the design is adaptable to a variety of asynchronous-mode, serial-transfer equipments.

The ROM and status card also contains interrupt/monitor status circuits that receive various signals from the digital graphic controller and video controller. These circuits inform the display processor of the status of the signals, with some critical inputs causing program interrupts for immediate processing.

Major circuits of the ROM and status card are as follows:

DAnn-/IDnn+ Buffer/Inverter Input Gates. These gates pass the low-order byte on DAnn-B processor data bus to the 8-bit IDnn+ input data bus. This permanently enabled connection provides GCP access to a universal asynchronous receiver/transmitter (UART) device for serial output transfers to: (a) teletypewriter or other external equipment, (b) an I/O status register to enable/inhibit the UART's I/O communication interrupts, and (c) a display mask register to enable/inhibit other interrupt signals applied to the ROM and status card by other circuits.

ENRM. This circuit enables ROM control logic which:

1. Enables an applicable 2K bank of ROM storage devices (RR00- through RR03, respectively).

2. Enables the ROM output as a 16-bit data word to the processor bus data lines.

3. Enables the ROM high byte output to the low order processor bus data lines.

4. Enables the ROM low byte output to the low order processor bus data lines.

5. Generates a 300 ns delay for memory acknowledge.

ENRG. This circuit enables register control logic which controls:

1. Mask register read/write

2. Sense buffer read

EIOR. This circuit enables serial I/O control logic which selects addressed registers with read/write functions.

ROM Circuit. This circuit stores macrocontrol programs used by the display processor and digital graphic controllers. The full ROM storage circuit comprises four separately addressed rows of 4-bit preprogrammed storage devices, with the four devices in each row producing a full 16-bit output word for each address within its address range.

The address decoder controls ROM row selection by activating only one row-read enabling signal (RR00- through RR03-) at a time. The address decoder also provides 8-bit byte selection by enabling or inhibiting the storage devices pertaining to the low-order byte data. If the LSEL- (low select) control signal is active, the low-order bits are enabled; if that signal is inactive, only the high-order bits are enabled.

Byte Select Multiplexer. This circuit passes high-order byte outputs from the program ROM to the low-order lines on the output-data bus when enabled by a low HSEL- (high select) command from the address decoder. This condition occurs when the BYTE-B (processor bus byte mode control) signals and byte selector address bit AD00-B both are low.

High-Order Byte ODnn+/DAnn- Data Output Gates. These gates, when enabled by a low HBYT- command from the address decoder, pass high order 8-bit byte from the program ROM to the high order lines of the processor data bus. When enabled by a low RRDB- (read reader data buffer) signal from the serial I/O register decoder, they pass the activity state of an OERR- (overflow error from receiver register) output from the UART to processor bus data lines DA15-B from DA14-B.

Low-Order Byte Data Output Gates. These gates, when enabled, pass the eight LSBs of the ODnn+ lines to the corresponding low order DAnn- data lines on the processor bus. This transfer includes any of the following:

1. Eight LSBs of any ROM word (word or byte addressed).
2. Eight MSBs of any ROM word (byte addressed only).
3. An 8-bit parallel data word from the UART as an input transfer from peripheral serial communication equipment.
4. Status bits from the serial I/O UART status register for an input or output transfer.
5. An 8-bit parallel word from the program loaded display mask register.
6. A 4-bit parallel word from the display sense buffer.
7. An 8-bit parallel word from the trap vector address encoder that defines a trap vector which contains a start address of the appropriate interrupt handling subroutine for any of the nine interrupt conditions.

Register Control Logic. This circuit decodes the processor bus address lines together with ENRG- from the address decoder to:

1. Display mask register - read/write
2. Display sense buffer - read.
3. Generate EIOR - enables the serial I/O control logic.
4. Generate 600 ns delay for memory acknowledge.

Serial I/O Control Logic. This circuit decodes the processor bus address lines, together with EIOR- from the register control logic, to establish full communication with the UART. The data includes:

1. Reader status register - read/write.

2. Reader data buffer - read.

3. Transmitter status register - read/write.

4. Transmitter data register - write.

Display Mask Register. This circuit stores eight bit of program-selected data to enable/disable the corresponding inputs to an interrupt storage register. The display mask register is accessed by a 177662_8 address, which activates either a WMSK- (write mask) signal from the register control logic if the WRIT-B processor bus line is low, or an RMSK- (read mask) output if the WRIT-B line is high. The WMSK- signal loads the IDnn+ data word into the display mask register, enabling or disabling the program interrupt conditions. Activation of the RMSK- signal reads out the last stored value of these mask signals for status analysis. Table 3-13 lists the mask bits and their effects.

Table 3-13. Display Mask Register Bits

DAnn-B BIT	ASSOCIATED INTERRUPT CONDITION/SIGNIFICANCE
00	Not used.
01	Graphic controller refresh file program halted.
02	X-axis or Y-axis display vector overflow detection.
03	Real time clock (60-Hz interrogation rate).
04	Not used.
05	Not used.
06	Not used.
07	Not used.

Sense/ODnn+ Buffer Gates. These circuits, when enabled by a low RSEN- (read sense) signal from the TTY command decoder as the result of a read command addressed to location 177660_8, pass graphic controller signal GCRE-H (request enable) and BYTE-B (character byte) status signals as a 4-bit data word to the DAnn-B processor bus (see table 3-14).

Table 3-14. DAnn-B Processor Bus Data Word

DAnn-B BIT	SOURCE	SENSE CONDITION WHEN SET TO LOGIC "1"
04	GCRE-H	Graphic controller display refresh sequence halted.
05	BYTE-B*	Second character of text pair currently is addressed by graphic controller refresh program.
06		Not used.
07		Not used.

*Activating the BYTE-B signal does not generate a program interrupt sequence; each of the other three sense bits interrupts the GCP when enabled by the mask register bits.

Interrupt Status Register. Depending on (a) enable/disable status of the mask signals produced by display mask and (b) I/O status registers, this register confirms or ignores activation of nine different input interrupt signals (see table 3-15).

Table 3-15. Interrupt Status Register Input Signals

SIGNAL	ACTIVATION CONDITION/SIGNIFICANCE
HALT-H	Graphic controller display refresh sequence halted.
DRDY-	Data ready condition in UART receive buffer register (input word to be read).
TBRE-	Transmitter buffer register empty condition in UART (ready to accept next output transfer character from processor data bus).
RTCK-0	Real time clock pulse signal from output channel card.

Sync Storage Register. This circuit, when enabled by a low STAT+ command from the interrupt/processor bus control logic, stores the current logic state of eight mask enabled status bits from the interrupt status register.

Priority Encoder. If the LINK+ output from interrupt/processor bus control logic is low, the priority encoder activates a 3-bit code giving the octal identification of the highest valued input from the sync storage register (see table 3-16). The priority encoder ignores lower priority inputs occurring simultaneously with, or after, activation of any higher priority input; but responds to any following higher priority input. When an input is active, the priority encoder produces a FLAG- output to the interrupt/processor bus control logic, maintaining this steady state output as long as the associated sync storage register input remains active.

Table 3-16. Priority Encoder Trap Address Values

	PRIORITY ENCODER VALUE (OCTAL)	MEMORY TRAP ADDRESS (OCTAL)	INTERRUPT HANDLING SUBROUTINE
	0	140	Execution of halt refresh instruction by graphic controller
	1	144	X-axis/Y-axis position data overflow (offscreen)
	2	060	Received serial data ready for input
LINK+ inactive	3	064	Output serial data transmitted (ready for next character load)
	4		Not used
	5		Not used
	6	100	Real time clock pulse
	7		Not used
LINK+ active	X	170	Sync link execution

Interrupt Trap Vector Address Encoder. If the LINK+ output from the interrupt control logic is low, this encoder circuit responds to coded inputs from the priority encoder by producing an 8-bit output word specifying the trap address of the subroutine that handles the interrupt condition that triggered an active FLAG- signal (see table 3-16). When the LINK+ signal is high, the trap vector address encoder produces SYNC LINK address 170_8, regardless of the priority encoder output state. In all cases, the trap address is placed on the ODnn+ output data bus for transfer (via the low order byte ODnn+/DAnn- data output gates) to the DAnn-B processor data bus.

Interrupt Register Reset Decoder. This circuit responds to coded inputs from the priority encoder by clearing the storage cell in the interrupt status register associated with the input signal that triggered an active FLAG- output from the priority encoder.

Interrupt Control Logic. This circuit initiates an interrupt-processing sequence in response to activation of (a) nonmaskable LINK-H link interrupt commands from the digital graphic controller or (b) unmasked FLAG- interrupt signals from the priority encoder. In either case, the sequence begins with activation of the IREQ-D interrupt request signal from the display processor at the end of the instruction cycle during which the FLAG- input or the LINK-H input goes active.

If the FLAG- input is the trigger signal, activation of IREQ-D places an active low on the INL5-B interrupt priority line.* If the LINK-H input is the trigger signal, the IREQ-D input produces an active low logic level on the INL7-B interrupt-priority line.* The circuit then waits until the display processor card responds to INLn-B with an active low IENA-D interrupt enable. If the interrupt cycle was triggered by FLAG-, STA+ is activated and halts transfer of interrupt signals from the sync storage register to the priority encoder. This means that the priority encoder cannot change state until the announced interrupt condition is processed, ensuring that the established trap address output from the interrupt trap vector address encoder remains valid. If the interrupt cycle was triggered by LINK-H, however, LINK+ is activated to (a) inhibit the priority encoder, and (b) condition the interrupt trap vector address encoder to produce the 170_8 trap address associated with sync link operation.

When the ROM and status card receives an active GRAI+B input, the interrupt control logic deactivates its GRAO+B output to inhibit the graphic controller card from seizing control of the processor bus. Simultaneously, the interrupt control logic activates BUSC-, BUSB-B, and DEV1-B. Internally, BUSC- enables the interrupt trap vector address encoder (transferring the selected trap address code onto the ODnn+ output data bus) and enables the low order byte ODnn+/DAnn- data output gates to pass the trap address code to the DAnn-B processor data bus. Simultaneously, if the interrupt condition is a FLAG-triggered sequence, the interrupt control logic activates an interrupt reset signal to keep (a) the sync storage register inhibited, and (b) cause the interrupt reset decoder to produce a 1-of-8 output code that clears the interrupt status register storage cell that created the FLAG- signal.

Externally, BUSB-B prevents other processor bus circuit cards from seizing control of the bus during the remainder of the interrupt-handling sequence. The active DEV1-B signal informs the memory card that the bus controller for the coming operation is the ROM and status card, thereby inhibiting the memory-mapping circuits normally used when the display processor is in control.

One CLOK+ pulse period later, the interrupt control logic activates a low IADV-B signal that directs the display processor to examine the valid interrupt trap address word now on the DAnn-B processor bus data lines. The same CLOK+ pulse then deactivates BUSB-B and DEV1-B, in turn deactivating the ODnn+/DAnn- enabling logic, releasing the sync storage buffer, and terminating the enabling condition of the interrupt reset decoder.

The subsequent termination of the IENA-D input allows the control logic to return to its normal quiescent state, deactivating STAT+ or LINK+, as applicable. If this cycle was triggered by FLAG-, termination of STAT+ and IRST- reenables the sync storage register. If any lower priority interrupt signals were loaded into the interrupt status register during the completed sequence, this same sequence is repeated to handle the lower-priority interrupt condition.

If the cycle was triggered by LINK-H, termination of LINK+ reenables the priority encoder and the interrupt trap address encoder to respond to any interim or subsequent interrupt inputs.

*The designated FLAG- and LINK-H priorities are the standard jumper selections. Actually, either IREQ-D loaded interrupt condition can be jumpered to the INL5-B, INL6-B, or INL7-B lines in any desired combination.

Memory Acknowlege Generator. This circuit places an active low on the MEMA-B processor bus control line after completion of an instruction operation setup. For ROM readouts, this condition occurs within 300 nanoseconds (i.e., three 10-MHz CLOK-F pulsetrain periods) after activation of the RDRM- (read ROM) enabling signal to the ODnn+/DAnn- output enabling logic. For serial I/O data transfers through the UART or write/read registers, this condition is delayed an additional 300 nanoseconds by routing the applicable outputs from the register control logic to the timing delay circuit.

Universal Asynchronous Receiver/Transmitter (UART). This device services a full duplex serial communication channel through connector J2. The UART accepts serial data from a teletypewriter (or other serial communication equipment) and converts it to an 8-bit parallel word on the ODnn+ output data bus for passage to the DAnn-B processor data bus. Conversely, the UART accepts 8-bit parallel data from the IDnn+ input data bus and transmits it in serial format to the external equipment.

The UART sends two transfer operation signals to the interrupt sense/status mask register. One signal is the low DRDY- (data ready) applied after the UART has placed a received word in its internal receive data buffer register. The other signal is the low TBRE- (transmit buffer register empty) that goes low after the last output word has been passed to the internal serial transmit circuit, and the UART is ready to accept a new word from the IDnn+ bus for transfer to the external equipment.

These outputs initiate program interrupt sequences, producing trap addresses to branch the program to the appropriate handling subroutine for the I/O transfers. Note that these interrupts can be masked by program control of the I/O status register, which monitors DRDY- and TBRE- signals for direct readout by the program when applicable.

I/O Status Register. This circuit stores (a) program-selected values of DA00-B and DA06-B data bits (written to address 177560_8) as external equipment reader enable/inhibit and receive interrupt enable/inhibit commands, and (b) the value of data bit DA06-B (written to address 177564_8) as a transmit interrupt enable/inhibit command. The I/O status register sends an RDEN- (reader enable) signal to the external equipment if DA00-B is loaded as a logic low at 177560_8; this signal is cleared when the external equipment sends a serial input word to the UART. The stored DA06-B values are reproduced as RMSK+ (receive mask) and TMSK+ (transmit mask) signals, respectively. These signals are applied to the interrupt status register as conditioning signals for the storage cells receiving DRDY- and TBRE- interrupt signals from the UART. Consequently, the stored value of the two mask bits determines whether the GCP is interrupted when either UART readiness signal becomes activated.

Under program control, the I/O status register passes output data bits OD04+ through OD07+ to the DAnn-B processor data bus to identify the current I/O communication status. Two data values are possible: one when the program calls for a readout of receiver status (address 177560_8); the other, when the program calls for a readout of transmitter status (address 177564_8). In either case, bits 04 and 05 are always inactive. Bit 06 identifies the current value of the corresponding interrupt enable/inhibit bit (receive or transmit) in the I/O status register. Bit 07 identifies the current value of the corresponding

transfer-operation output (DRDY- or TBRE-) from the UART. The display processor program can therefore be coded to inhibit I/O interrupts, but to maintain communication with the external I/O equipment by reading out the monitor circuits as part of a service loop in the program sequence. Tables 3-17 through 3-20 summarize the programming capabilities for I/O communication through the serial-interface connector J2.

Input Conditioning Logic and Gating. This circuit passes the serial RDAT+ (received data) signal from the external equipment to the UART. The conditioning logic incorporates jumper options for adapting the UART's receiver input line to teletypewriter outputs (the standard 20 mA current loop selection), TTL logic levels, or RS-232C logic levels.

Output Conditioning Logic and Gating. This circuit passes the UART's serial transmitter output signal to the external equipment. The conditioning logic incorporates jumper options to adapt the UART's output to the standard teletype-writer 20 mA current loop, RS-232C communication signals, or TTL logic level.

Baud Rate Generator. This circuit supplies common receive mode and transmit mode clock train signals to the UART, using the selected countdown of a free running crystal controlled oscillator. The standard setting is a rate of 110 baud. Other jumper-selected rates for user equipments cover common industry I/O rate choices; i.e., 300, 1200, 1800, 2400, 4800, or 9600 baud. Note that the UART clock input lines can be jumped to a 50-kiloword output from the independent system clock circuit.

Table 3-17. TTY Receive Status Register (Address 177560_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00	Reader enable	Program read/write, cleared by system reset. When set, this bit establishes an active low RDEN- reader enable signal on pin 9 of I/O connector 1A1A6J2 to advance the associated external equipment to the next transfer cycle (if applicable). This bit is cleared when a serial data START bit is received from the external equipment, and must be rewritten as part of the data read sequence for each character.
06	Receiver interrupt enable	Program read/write, cleared by system reset. When set (the normal condition), this bit allows a program interrupt to be generated whenever the DRDY- (data ready) signal from the UART goes active.
07	Receiver ready	Program read only, cleared by system reset. This bit is set when the UART device accepts a character code from the external equipment and stores that data in its receive data buffer. The bit is cleared when the program reads the receive data buffer. If bit 06 has been set, setting this bit generates a program interrupt.

Table 3-18. TTY Transmit Status Register (Address 177564_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
06	Transmitter interrupt enable	Program read/write, cleared by system reset. When set (the normal condition), this bit allows a program interrupt to be generated whenever the UART activates its TBRE- output following transfer of the last loaded character into its internal shift register for transmission to the external equipment.
07	Transmitter ready	Program read only, set by system reset. This bit is cleared when the program writes new data into the UART, then is reset after the UART transfers that parallel data to its serial output shift register, presenting the first bit to the external equipment (meaning the UART is ready to accept another character from the program).

Table 3-19. TTY Receive Data Buffer (Address 177562_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00 through 07	Received data	Program read only. These bits contain the latest received serial character data stored by the UART as input from the TTY (or other J2-connected external equipment). If the applicable character code length is less than eight data bits, the unused high order bits are inactive (logic 0).
14	Overrun error	Program read only, cleared by system reset. This bit is set when the UART detects a data-overrun condition (i.e., receipt of a new character code from the external equipment before the GCP has read out the last character). This bit is updated each time a new character code is received from the external equipment.
15	Error	Program read only, cleared by system reset. This bit is set when the UART overrun error flag (bit 14) is set. This bit is cleared when the overrun error bit is cleared.

Table 3-20. TTY Transmit Data Buffer (Address 177566_8) Bit Descriptions

DAnn-B BIT	NAME	FUNCTION DESCRIPTION
00 through 07	Transmit data	Program write only. These bits are the character data codes loaded into the UART's transmit data buffer by the program for transfer to the J2-connected external equipment.

System Clock. This circuit generates the 10 MHz (CLOK-F) system clock frequency used by all processor bus circuit cards as the basic timing signal for system operations. The free running clock circuit generates CLOK-F (also available on the ROM and status card as CLOK+/CLOK-) by dividing the output of a 20 MHz crystal oscillator. The system clock circuit also produces a 50KB-F output available for use by other processor bus cards.

Voltage Filters. These devices are inductive pi-network that filters that smooth and isolate the +15V, -15V, and +5V lines to the external communications equipment.

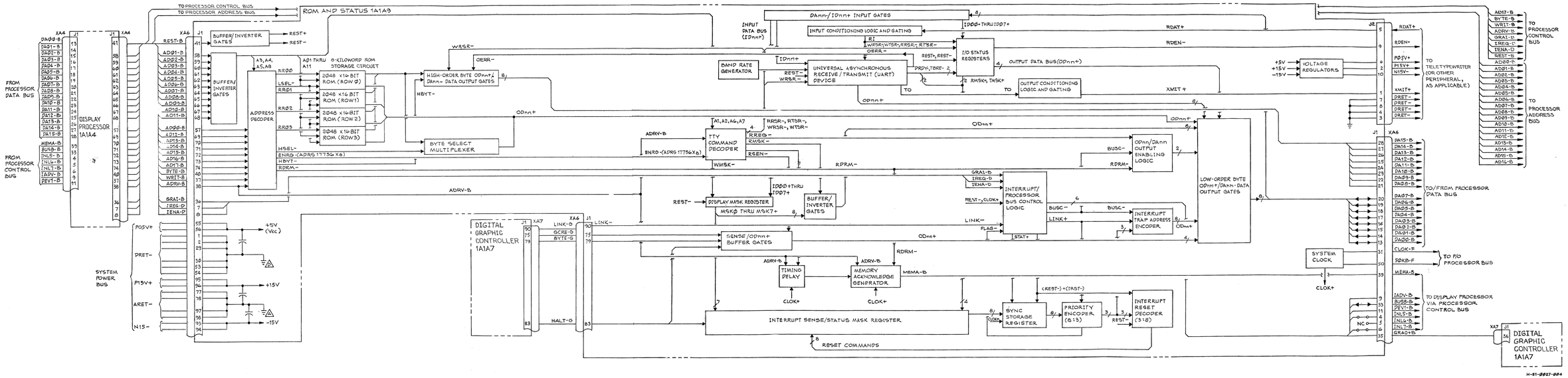


Figure 3-21. ROM and Status Card, Block Diagram

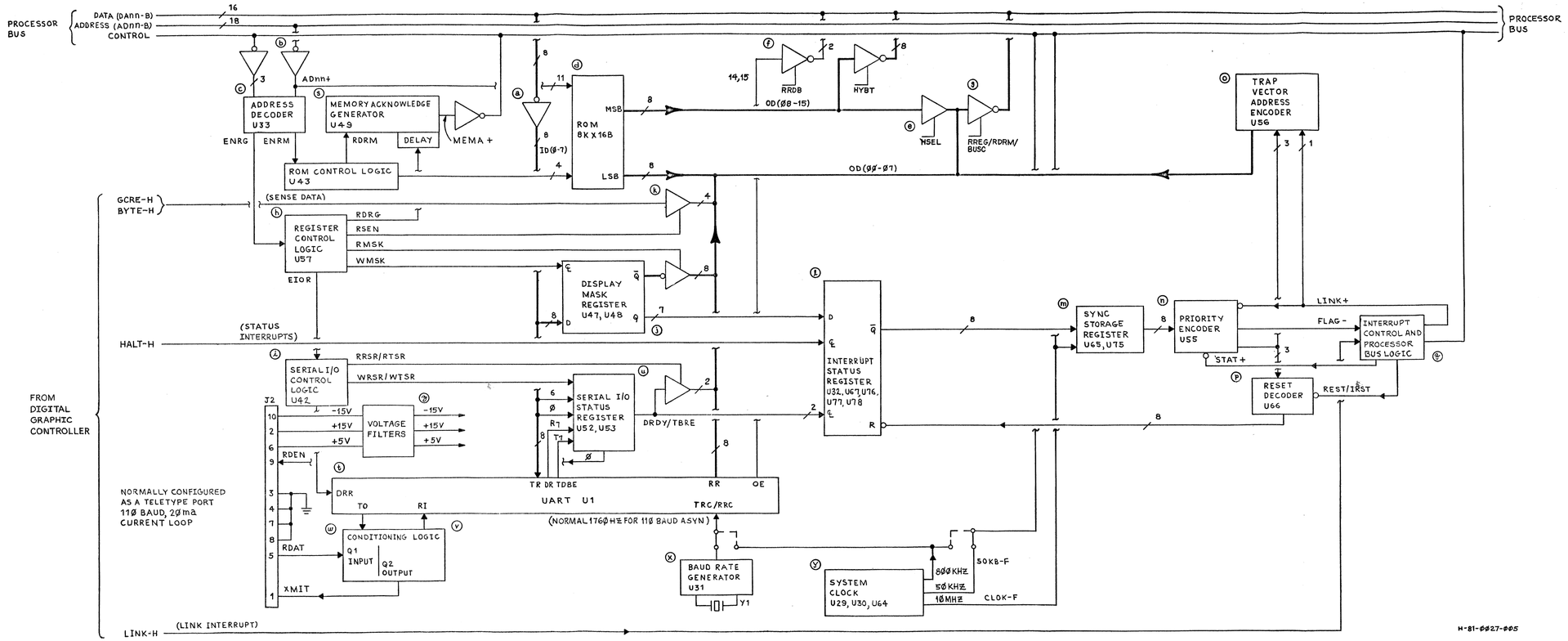


Figure 3-22. ROM and Status Card, Functional Block Diagram

3.9 DIGITAL GRAPHIC CONTROLLER

3.9.1 PHYSICAL DESCRIPTION. The digital graphic controller is an eight-layer printed circuit card, 7-3/4 by 12 inches. It is always located in slot XA7 of a basic GRAPHIC 8 configuration.

The digital graphic controller connects to the backplane through a 98-pin connector (P1). On the front end of the card are two 40-pin connectors, J1 and J2. These connectors allow the digital graphic controller internal buses, program counters, and other signals to be monitored, using a logic analyzer, for debugging purposes. A four-pin connector, J3, is mounted near the center of the card. This connector allows the bus control signals to be brought out separately when an optional, second display processor is added to the GRAPHIC 8 system.

An LED mounted on the front of the card indicates whether the digital graphic controller is busy or looping through a wait routine.

3.9.2 APPLICATION. The digital graphic controller generates the images to be displayed on the GRAPHIC display monitor. The images may consist of vectors, conics, fills, point plots, text, or "pure" raster data obtained from a host computer using the MOVE PIXEL DATA instruction.

The digital graphic controller also controls the display parameters. These include the use of split screen, the point of origin for each split screen segment, the number of lines displayed per segment, cursor enabling and positioning, and selecting which pixel mapping memory is to be displayed.

3.9.3 FUNCTIONAL DESCRIPTION. The digital graphic controller receives its clock signal from the ROM and status card, and other control signals (turn-on reset, vertical access enable) from the timing module. The digital graphic controller receives operational information and instructions from the display processor, and communicates with the display processor through interrupts. The digital graphic controller also receives status information from the video controller and the mapping memory card(s).

The digital graphic controller sends operational information and instructions to the video controller that cause the video controller to pan, scroll, selectively blink, selectively blank, or otherwise alter any or all of a 2048-by-2048 bit memory map. The digital graphic controller also sends updated pixel information to the mapping memory card(s) continuously, under program control. The instructions and pixel information that the digital graphic controller sends to the video controller and the mapping memory card(s) depend on the instruction it receives from the read/write memory in the form of a refresh file. Usually, the display processor instructs the digital graphic controller when to access the refresh file. However, the digital graphic controller can also communicate with the read/write memory as a DMA (direct memory access) device, independently of the display processor. The digital graphic controller can also communicate directly with the host computer. Figure 3-23 shows the relationship of the digital graphic controller to other elements of the GRAPHIC system.

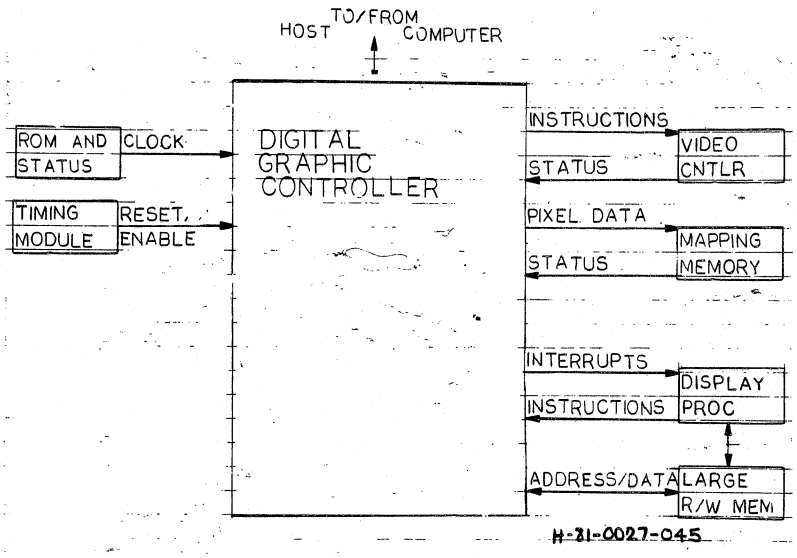


Figure 3-23. Relationship of Digital Graphic Controller to Other Elements of the Graphic 8 System

The execution of a refresh file begins when the display processor halts the digital graphic controller. This is usually done using a HALT, a FUNS (function stop), or a system RESET instruction. The display processor then checks the sense register (address 177660) on the ROM and status card to ensure that the digital graphic controller has halted. (The LED on the front of the digital graphic controller card should go out. This indicates that the digital graphic controller is looping through a three-word wait routine, pending instructions from the display processor.) If the halt bit of the sense register is true, the display processor then writes the program counter (165006) to the digital graphic controller. This causes the digital graphic controller to fetch the contents of the corresponding address in read/write memory. This address contains the starting instruction of the refresh file. Since the digital graphic controller uses 18-bit addressing, it can access a refresh file from any location in the read/write memory not reserved for other functions. (In a dual memory system, there are 256K byte locations. With 18-bit addressing, 2^{18} = 256K).

Once execution of a refresh file has begun, the display processor cannot access the digital graphic controller registers. If the display processor does try to access the digital graphic controller while it is running, a bus timeout will result and the instruction will be ignored. All communications between the display processor and the digital graphic controller must be handled through halts or interrupts. The digital graphic controller can issue three types of interrupts: halt, link, or overflow.

Halt and link interrupts are generated upon receipt of HALT or LINK instructions from the display processor. An overflow interrupt is generated when the address the digital graphic conroller calculates for a pixel lies outside the programmable 2048-by-2048 bit area of the memory map. An overflow interrupt, therefore, can only occur as a result of a relative instruction. All interrupts

from the digital graphic controller are generated through the ROM and status card. This allows the display processor to set the mask registers on the ROM and status card, to determine which interrupts it will respond to.

The digital graphic controller can operate in two different modes. The first mode allows the digital graphic controller to execute all of the graphic orders that are instruction-compatible with the GRAPHIC 7 system. The second mode allows the digital graphic controller to execute all of these same graphic orders plus those that are exclusive to the GRAPHIC 8 system. The mode used is set under program control; as a result, any program should be written so that it executes entirely in one mode.

3.9.4 BLOCK DIAGRAM DESCRIPTION. See figure 3-24. The digital graphic controller consists of the following functional blocks:

1. Processor bus control
2. Processor input/output (I/O) and byte swap registers, and sign extend multiplexer
3. Memory address register (MAR) and address decoder
4. Instruction decoder
5. Sequence multiplexer
6. Read-only memory (ROM) sequencer
7. Control ROM
8. Microcontroller
9. Random access memory (RAM) registers
10. 16-bit by 16-bit multiplier
11. Character ROM
12. Raster bus control
13. Raster MAR
14. Raster I/O data registers

The processor bus control logic seizes control of the processor control bus (GRAPHIC 8 C BUS) whenever the digital graphic controller is ready to perform a program operation. Program operations may include obtaining a graphic order, obtaining data vital to the graphic order, or writing pixel data into read/write memory.

The processor I/O and byte swap registers latch data from the processor data bus (GRAPHIC 8 D BUS) during a digital graphic controller register write or data fetch operation. The sign extend multiplexer extends the I/O receiver register for arithmetic operations, format character data, or passes data unchanged, as directed by the control ROM.

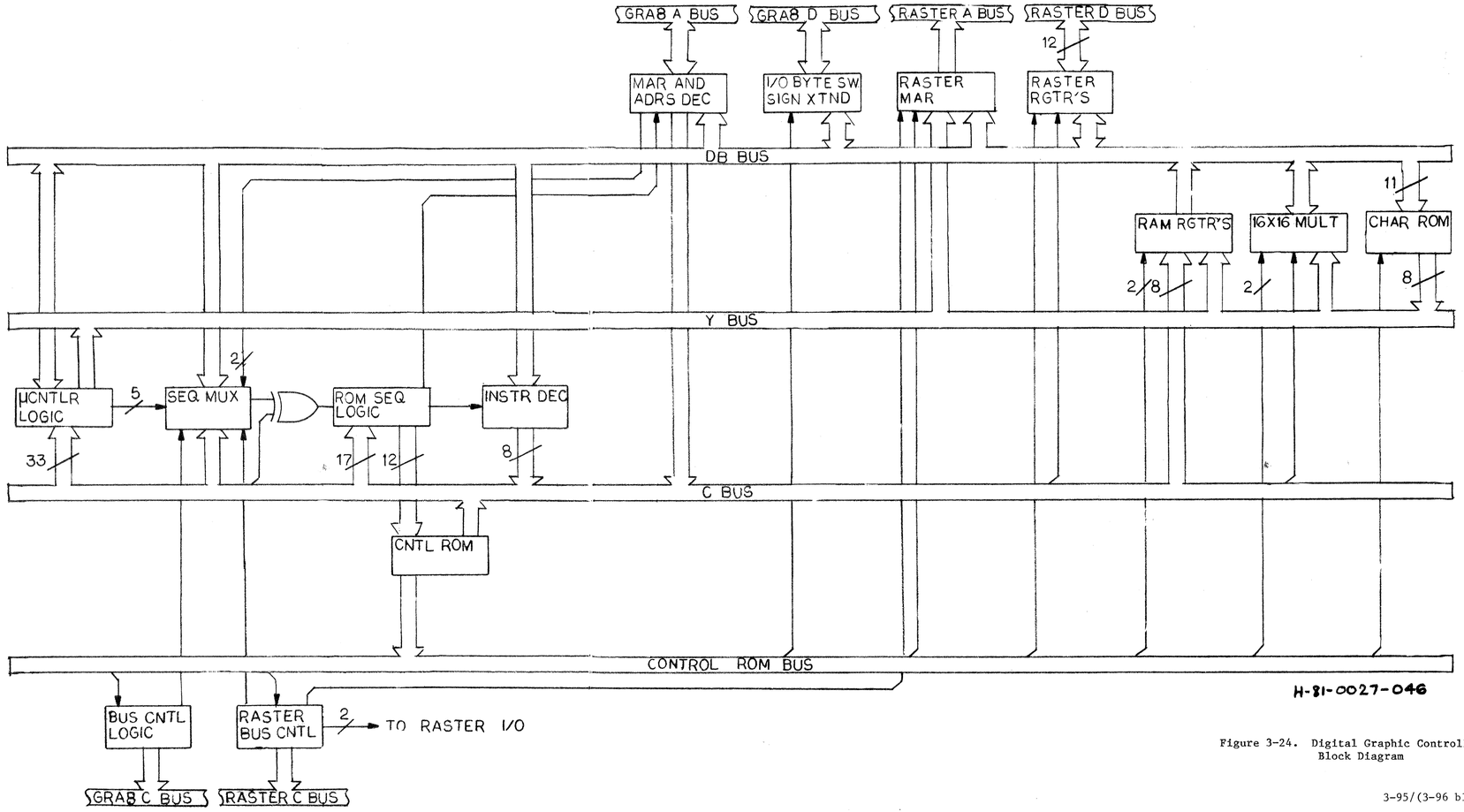


Figure 3-24. Digital Graphic Controller, Block Diagram

The MAR (memory address register) is enabled onto the processor address bus (GRAPHIC 8 A BUS) when the digital graphic controller seizes control of the processor control bus. The MAR latches the 18-bit addresses used by the digital graphic controller. Address decoding is done in two stages: The first stage checks the most significant bits in the MAR for the unique address of the digital graphic controller. The first stage will enable the second stage of address decoding only if this address is valid. The second stage of address decoding then decodes the function or operation to be implemented from the least significant bits in the MAR.

The instruction decoder is essentially a table of starting addresses for all of the graphic orders that the GRAPHIC 8 system can execute. When enabled by the ROM sequencer, the instruction decoder decodes instruction data enabled onto the digital graphic controller internal data bus (DB BUS) by the processor I/O.

The sequence multiplexer allows the ROM sequencer logic to test flag bits and to make branch decisions affecting program operation depending upon the results of the test.

The ROM sequencer logic controls the sequence of execution of the microinstructions stored in the control ROM. The ROM sequencer uses 16 instructions to select the address of the next microinstruction to be executed. Four of the instructions are conditional; their effect depends only on the instruction. Nine of the instructions have effects that are partially controlled by external, data-dependent conditions. Two of these instructions have effects that are partially controlled by the contents of an internal register/counter. One instruction provides for testing of both a data-dependent condition and the contents of an internal register/counter.

The control ROM contains the microinstructions needed to execute all of the graphic orders defined for use in the GRAPHIC 8 system. The control ROM uses an 80-bit-wide field to define these microinstructions.

The microcontroller performs the arithmetic and logical operations needed to execute a graphic order, as instructed by the control ROM. Shift control, carry select, and look-ahead carry circuits on the digital graphic controller card assist the microcontroller.

The digital graphic controller RAM registers can be divided into six groups: processor registers, function registers, sense and mask registers, functional control registers, display control registers, and configuration registers. The RAM registers are accessible by program control only if also assigned an octal code and only if the digital graphic controller is halted.

The 16-bit by 16-bit multiplier is a multifunction arithmetic device capable of performing multiplication with or without product accumulation. The multiplier produces a 32-bit product that is used by the digital graphic controller for conic generation and polygon fills.

The character ROM stores the data needed to produce alphanumeric characters. Each character is allotted 16 locations in the ROM, to allow shifting of characters. Because of the structure of the microcode used to store the characters, 5 x 7 and 7 x 9 characters fonts may be used interchangeably.

The raster bus control circuit enables the digital graphic controller to access locations in the mapping memory for pixel data read or write operations. The raster bus control circuit initiates a bus request whenever function bits are loaded into the raster MAR. The bus request is enabled onto the raster control bus (RASTER C BUS).

The raster MAR stores both the address of the display the pixel data is to be written to and the function to be executed. The digital graphic controller can execute three raster functions: read pixel, write pixel, and write 64 bits (for writing more than one pixel at a time). The function bits and display select bits are loaded separately from the pixel address so that they need not be reloaded every time the digital graphic controller calculates a new pixel address. The raster MAR enables the pixel address onto the raster address bus (RASTER A BUS).

The raster I/O data registers latch data to or from the digital grapic controller during pixel data read or write operations. The pixel data is enabled onto the raster data bus (RASTER D BUS).

3.9.5 DETAIL OPERATION. See drawing 5977182 in the maintenance diagrams manual (H-81-0097). The following paragraphs describe the makeup and operation of each of the blocks in figure 3-24 in more detail.

3.9.5.1 Processor Bus Control. The processor bus control logic consists of grab request flip-flop U48B, bus control flip-flop U48A, byte flip-flop U39, fetch busy flip-flop U43A, address valid flip-flop U74B, and write flip-flop U56B.

A bus request is initiated by asserting RB5, which is inverted by U71B and gated into U48B on the next clock pulse, via NOR gate U49D. The output of U48B becomes the input to U48A, provided the bus is not busy and the grant in line (GRAI+B) is true. (These signals are gated through AND gate U62A.) When these conditions are met, the output of U48A (BUSB-B) is gated onto the bus on the following clock pulse, via NOR gate U63B. The digital graphic controller then assumes control of the bus. (A simplified schematic diagram of the bus grant circuit is shown in figure 3-1.)

If the digital graphic controller is to perform a byte operation, RB64 must be asserted along with the bus request signal, RB5. Then, when U48B is set, U39 will also be set. The output of U39 (BYTF-B) is gated onto the bus when bus control is obtained, via NOR gate U63A.

When the digital graphic controller assumes control of the bus, the output of U48A sets U43A. Fifty nanoseconds later, U74B is clocked and its output asserted. The output of U74B (ADRV-B) is gated onto the bus via NOR gate U63D. The memory address register (MAR) is also enabled onto the processor address bus when the digital graphic controller asserts BUSB-B.

If the digital graphic controller is to perform a write operation, U56B will be clocked when the output of U43A goes true. This enables the processor I/O transmit registers (U14 and U21) onto the processor bus before ADRV-B is asserted, via programmable logic array U57.

If the digital graphic controller is to perform a read operation, the output of U43A holds U56B preset. Since BUSB-B and ADRV-B are already true, this will enable AND gate U69A when the memory acknowledge line (MEMA-B) also goes true. The output

of U69A is passed through NOR gate U61B as the load register instruction, LD INSTR REG. Thus, MEMA-B becomes the clock that allows LD INSTR REG to latch data into the processor I/O receive registers (U5 and U7).

MEMA-B is also the signal used to terminate any bus control action. On the next clock pulse after receiving MEMA-B, ADRV-B is removed, forcing BUSB-B to be removed and thus ending the cycle. (A timing diagram of the processor bus control cycle is shown in figure 3-2.)

3.9.5.2 Processor Input/Output (I/O). The processor I/O consists of receive registers U5 and U7, byte swap register U12, transmit registers U14 and U21, and sign extend multiplexer U4 and U11. The receive, byte swap and transmit registers are all octal flip-flops; the sign extend multiplexer is made up of two programmable logic arrays.

U5 latches the upper eight-bit byte (DA8 through DA15) from the processor data bus. U7 latches the lower eight-bit byte (DA0 through DA7). U12 also latches the eight upper bits. This ensures that, for any cycle, the upper byte can be read into the lower byte without shifting. The enables (ENA lines S3 and S5) for U5, U7, and U12 are under ROM control and are developed via a 1 of 10 decoder (U81). The enables are also applied to U4 and U11, via AND gate U62C.

The outputs of U5, U7, and U12 become the inputs to U4 and U11. U4 and U11 extend bit 10 or bit 5 of the receive registers, as controlled by control ROM bits 3 or 4 (ROMC lines RB3 and RB4). Sign extensions are carried to bit 15. The outputs of U4 and U11 are enabled onto the digital graphic controller internal data bus as DB0 through DB15.

U14 latches the upper eight-bit byte (DB8 through DB15) from the digital graphic controller internal data bus. U21 latches the lower eight-bit byte (DB0 through DB7). The clock for U14 and U21 (STR line T8) is under ROM control and is developed via a 3-line to 8-line decoder (U18). The enable for U14 and U21 (ENA DATA OUT-) is developed via a programmable logic array (U57) and is valid only when the digital graphic controller is performing a write operation, as discussed previously. The outputs of U14 and U21 are enabled onto the processor data bus as DA0 through DA15.

3.9.5.3 Memory Address Register (MAR) and Address Decoder. The MAR consists of three octal flip-flops, U34, U41, and U45. The address decoder consists of micro-destination decoder U19, programmable read-only memories (PROMs) U20 and U26, stop flip-flop U56A, and start flip-flop U38.

U34 latches the lower eight-bit byte (DB0 through DB7) from the digital graphic controller internal data bus. U41 latches the upper eight-bit byte. U45 latches the two most significant bits (MSB), or bank bits, and is loaded only when bank boundaries (in the digital graphic controller RAM registers) are crossed. The clock for U34 and U41 (STR line T13) is under ROM control and is developed via a 3-line to 8-line decoder (U18). The clock for U45 (STR line T1) is also under ROM control and is developed by a second 3-line to 8-line decoder (U24). U34, U41, and U45 are enabled by the output of bus busy flip-flop U48B. The outputs of U34, U41, and U45 are enabled onto the processor address bus as AD0 through AD17.

U26 is the first stage of the address decoder. U26 decodes the digital graphic controller address. It is addressed by the upper nine bits (AD9 through AD17) of the processor address bus. U26 will output only if the address on these nine bits

is an octal 165 and the ADRV-B line is asserted. The output of U26 enables the second stage of the address decoder, U20.

U20 is addressed by bits AD1 through AD8 of the processor address bus. U20 decodes these bits to determine the function the digital graphic controller is to perform. These functions may include reading from or writing to a digital graphic controller register, halting the digital graphic controller through a FUNS (function stop) instruction, or starting the digital graphic controller through either a FUNC (function continue) instruction or writing the display program counter.

When any addressable digital graphic controller register is accessed for a read operation, U20 outputs a memory acknowledge signal (MEMA-B) and enables U19. The MEMA-B and the enable for U19 are developed via programmable logic array U57. The MEMA-B is further passed through flip-flop U74A and inverted by NAND gate U63C, before being placed on the processor bus.

The output of U19 is the starting address of the function to be performed.

The least significant bit (LSB) to both U20 and U19 is the WRIT-B signal output of U57, which is low for write operations.

Writing the FUNS, FUNC, or program counter registers is an asynchronous operation. Some of the graphic orders (for example, a clear memory, or CLRM) can take up to 40 milliseconds, while the display processor will time out after only 2.4 microseconds if it does not receive a response to its request when attempting to halt the digital graphic controller. Therefore, start and stop flip-flops are used to temporarily store the halt request, so that the digital graphic controller will stop when the current graphic order is completed. The outputs of these flip-flops become inputs to the sequence multiplexer (U42, U47, and U55). Before the digital graphic controller decodes a new instruction, it checks the state of U56A to see if a FUNS (165040) has been written. If it has, the digital graphic controller enters a wait loop that checks the status of the start and digital graphic controller address flags.

Writing the FUNC register (165036) will cause U20 to output a MEMA-B and instruct the digital graphic controller to continue executing the refresh file.

Writing the display program counter (165006) will cause U20 to set MEMA-B, latching the data into the processor I/O receive registers and setting the start flip-flop, U38.

3.9.5.4 Instruction Decoder. The instruction decoder consists of PROM U10, switch S1-4, mode register flip-flop U73A, and buffered tri-state output driver U86.

U10 is enabled by the MAP- output of the ROM sequence (U46). U10 decodes bits DB6 through DB15 of the digital graphic controller internal data bus. These bits were enabled onto the bus from the processor I/O receive registers, via the sign extend multiplexer.

Switch S1-4 allows the execution of a refresh file to be interrupted. If S1-4 is open, the two active-high chip enables on U10 (CE3 and CE4) are pulled up to +5V, and no interrupts are allowed. If S1-4 is closed, the next vertical access enable signal (VAEN-U) will disable U10. The VAEN-U is passed through flip-flops U31B and U31A. The low output of U31A is applied to U10 via S1-4. The low output of U31A is

also applied to the sequence multiplexer (U42, U47, U55). This forces the digital graphic controller to trap to an OFE or OFF condition.

The outputs of U10 and the LSB output of U86 form the branch address to the ROM sequencer. The mode bit will be a logic 0 when the digital graphic controller is initialized, whether at turn-on or when instructed by the display processor. The mode bit will be a logic 1 when the MODE instruction is used.

Mode 0 is the GRAPHIC 7 mode, and allows the execution of all the graphic orders used in a GRAPHIC 7 system. All existing GRAPHIC 7 programs can be run on the GRAPHIC 8 system in this mode. However, mode 0 does not allow the use of any features peculiar to the GRAPHIC 8 system. In mode 0, the digital graphic controller decodes the GRAPHIC 8 instructions as an NOP (no operation). Unpredictable operation may result. Mode 1 is the GRAPHIC 8 mode.

3.9.5.5 Sequence Multiplexer. The sequence multiplexer consists of three 1-line to 8-line decoders, U42, U47, and U55; and polarity select gate U85A. The sequence multiplexer is under ROM control.

The inputs to the sequence multiplexer are used as flags when testing for branch conditions. Control ROM bits RB29, RB30, and RB31 select which one of eight inputs to a particular decoder will be tested. Control ROM bits RB1, RB32, and RB33 select which decoder will be enabled. The outputs of the decoders are passed to the ROM sequencer (U46), via exclusive OR gate U85A. U85A allows the sequencer to test either state of a flag. U85A is controlled by ROM bit RB63.

A definition of all the branch condition bits can be found in the GRAPHIC 8 programmer's reference manual (H-80-0444).

3.9.5.6 ROM Sequencer. The ROM sequencer logic consists of bipolar microprogram controller U46. A block diagram of the controller is shown in figure 3-25. Table 3-21 lists the function of each of the inputs and outputs shown on the block diagram.

U46 contains a four-input multiplexer that selects either the register/counter, direct input, the microprogram counter, or the stack as the source of the next microinstruction address.

The register/counter consists of 12 edge-triggerd flip-flops with a common clock enable. When its load control line ($\overline{RLD}$) goes low, new data is loaded into the register on a positive clock transition. The direct input data lines (D_i) supply the data for loading the register/coutner. The register/counter can be also loaded with a number, N, and used as a 12-bit down counter. The zero result is available as a microinstruction branch test criterion. Thus, when the counting loop terminates, the sequence will have executed exactly N+1 times. This ensures efficient iteration of microinstructions.

The direct input data lines are the second source of inputs to the multiplexer. This source is used for branching.

The microprogram counter (uPC) consists of a 12-bit incrementer followed by a 12-bit register. With the carry in line (CI) to the incrementer tied high, the microprogram register is loaded with the current Y output word plus one on each succeeding clock cycle. Thus, microinstructions are executed in sequence.

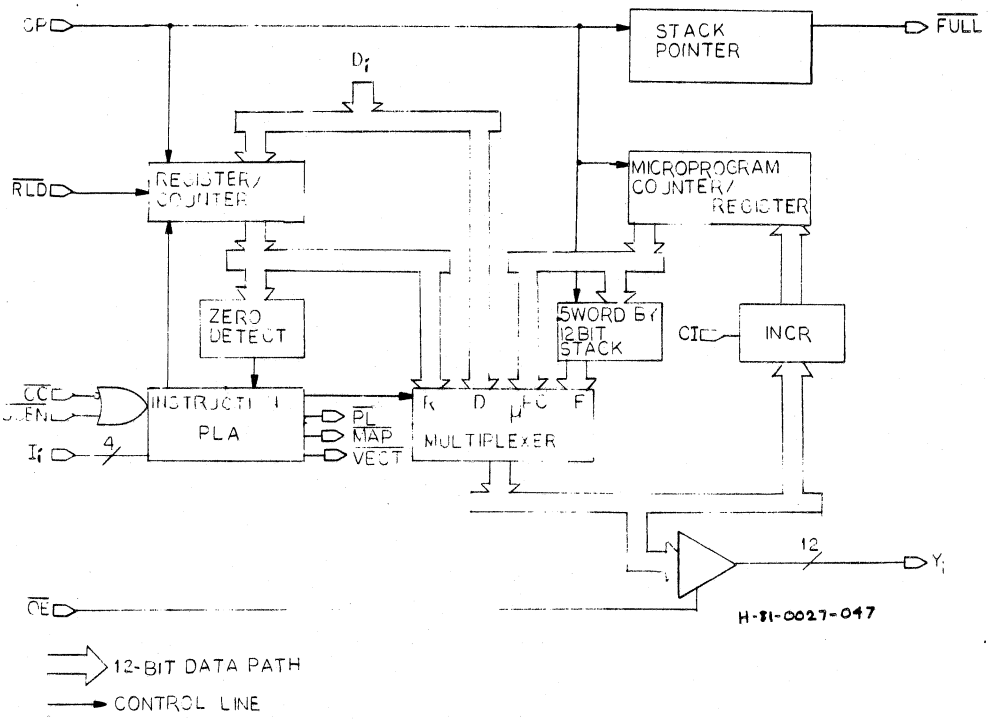


Figure 3-25. ROM Sequencer, Block Diagram

The 5-word by 12-bit stack provides return address linkage when executing microsubroutines or loops. The stack contains a built-in pointer that always points to the last file word written. During system initialization, it is important that the stack pointer be cleared. This is done using a microinstruction word that loops on itself until the digital graphic controller VAEN-U line is low. Refer to the programmer's reference manual (H-80-0444) for a list of the microinstructions available with the ROM sequencer that are implemented in the GRAPHIC 8 system.

U46 provides tri-state Y outputs. These outputs are controlled by switch S1-5. The ROM sequencer normally operates with S1-5 closed, but S1-5 can be switched open to provide external control, if desired, when testing the digital graphic controller card. The outputs of U46 are latched by two hex D-type flips, U37 and U30. The outputs of U37 and U30 are passed to the control ROM.

3.9.5.7 Control ROM. The control ROM consists of 10 bipolar read-only memories: U52, U53, U54, U65, U66, U67, U77, U78, U79, and U84. Switches S1-6, S1-8, and S2-1 through S2-8 can be set for different strapping configurations, to allow the use of alternate ROM devices.

Table 3-21. ROM Sequencer, Input and Output Functions

MNEMONIC	NAME	FUNCTION
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D0 is the LSB.

I_i	Instruction Bit i	Selects one of sixteen instructions for the microprogram controller.
$\overline{CC}$	Condition Code	Used as a test criterion. Pass test is a low on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	When this signal is high, $\overline{CC}$ is ignored and the microprogram controller operates as though $\overline{CC}$ were always true.
CI	Carry In	Low-order carry input to incrementer for program counter.
$\overline{RLD}$	Register Load	When this signal is low, it forces the loading of the register/ counter.
$\overline{OE}$	Output Enable	Tri-state control of Y_i outputs.
CP	Clock Pulse	Triggers all internal state changes on a low-to-high transition.
Y_i	Microprogram Address	Address to microprogram memory. Y_0 is the LSB; Y_{11} is the MSB.
$\overline{FULL}$	Stack Full	Indicates that five items are already on the stack.
PL	Pipeline Address Enable	Selects branch address field of control ROM as a direct input source.
$\overline{MAP}$	Map Address Enable	Selects the instruction decoder as a direct input source.
$\overline{VECT}$	Vector Address Enable	Selects the address decoder as a direct input source.

The control ROM field is 2K by 80 bits wide. Setting the appropriate configuration switches allows the ROM to be expanded to 4K by 80 bits. The outputs of the control ROM (bits RB1 through RB80) define all the graphic orders that the digital graphic controller can perform. The true state of all the control ROM bits is low. Refer to the GRAPHIC 8 programmer's reference manual (H-80-0444) for a description of the function of each of the control ROM bits. The firmware for the digital graphic controller control ROM was assembled using the Advanced Micro devices (AMD) assembler software package.

The control ROM is also used to generate the interrupts required for communication between the digital graphic controller and the display processor and other GRAPHIC 8 devices. Control ROM bits RB17 through RB19 are applied as inputs to 3-line to 8-line decoder U58; U58 decodes the particular interrupt or control signal implemented from these bits. The interrupt outputs of U58 are latched into hex D-type flip-flop U27. Control ROM bit RB20 is also latched into U27 directly. The

outputs of U27 are then enabled onto the GRAPHIC 8 system processor bus on the next clock pulse.

3.9.5.8 Microcontroller. The microcontroller consists of four cascaded four-bit microprocessor slices, U8, U16, U28, and U35. A block diagram of a single four-bit slice is shown in figure 3-26. Table 3-22 lists the function of each of the inputs and outputs shown on the block diagram.

Table 3-22. Microprocessor Slice, Input and Output Functions

MNEMONIC	NAME	FUNCTION
A_{0-3}	RAM A Address Bits 0 to 3	Contain the address of the RAM word appearing at the RAM A output port.
B_{0-3}	RAM B Address Bits 0 to 3	Contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ and $\overline{CP}$ inputs are low.
$\overline{WE}$	Write Enable	When high, inhibits writing data into the RAM. When low, enables data at the Y input/output port to be written into RAM, in conjunction with CP low.
DA_{0-3}	External Data Bits 0 to 3	Can be selected as one of the ALU operand sources; DA_0 is the LSB.
$\overline{E_A}$	Enable RAM A	When high, selects DA_{0-3} as the ALU R operand. When low, selects the RAM A output.
DB_{0-3}	Data Bus Input/Output line 0 to 3	Under control of the $\overline{OE_B}$ input, the RAM B output port can be read directly on these lines, or input data on these lines can be selected as the ALU S operand.
$\overline{OE_B}$	RAM B Output Enable	When low, enables the RAM B output onto the DB_{0-3} lines. When high, disables the RAM B output tri-state bus buffers.
C_n	Carry In	Input to the microprocessor slice as part of a lookahead carry scheme.
I_{0-8}	Instruction Inputs 0 to 8	Select the operation the microprocessor is to perform.
$\overline{IEN}$	Instruction Enable	Tied low. Enables the $\overline{WRITE}$ output and allows the Q register and sign compare flip-flop to be written.

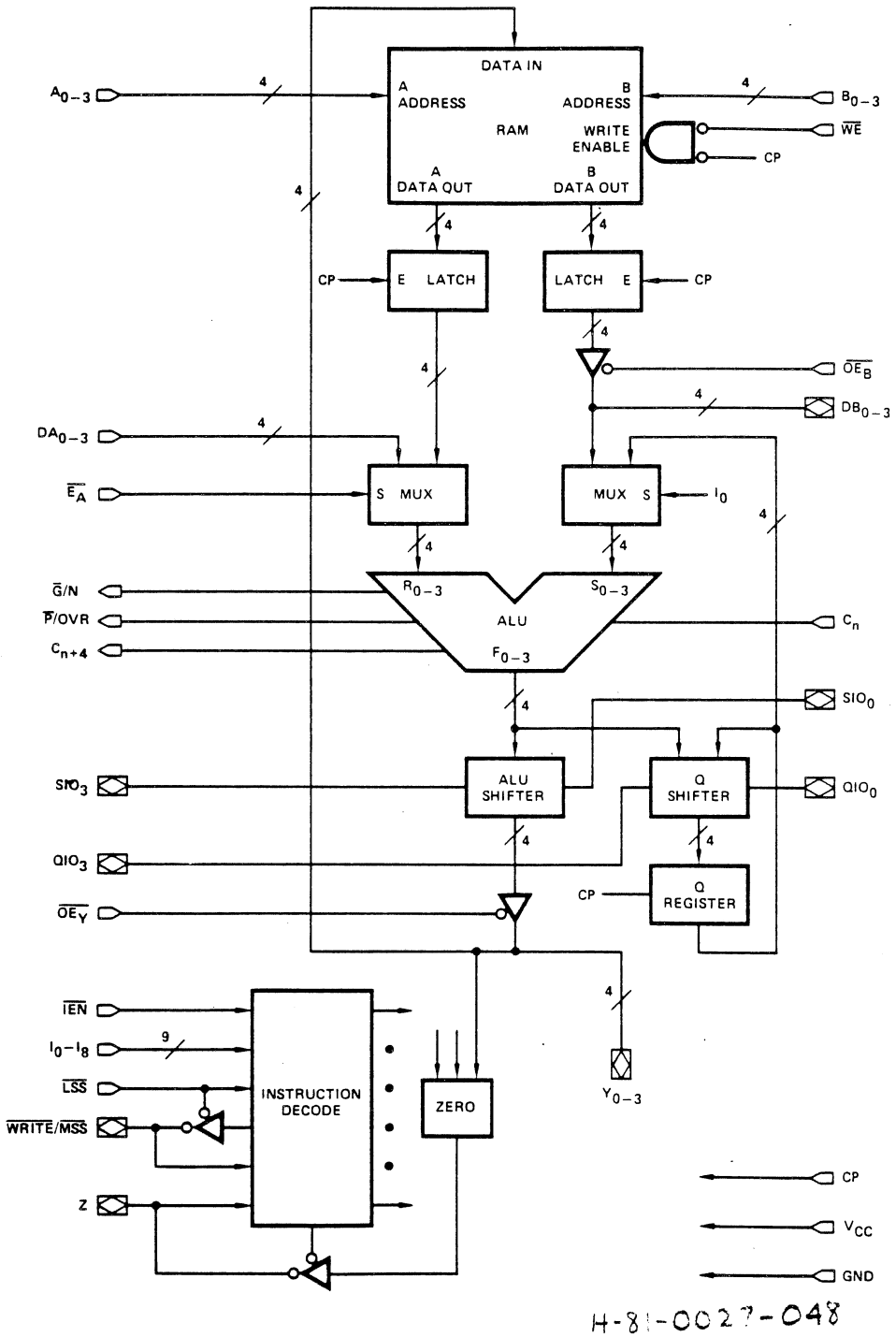


Figure 3-26. Microprocessor Slice, Block Diagram

C_{n+4}	Carry Out	Output from the microprocessor slice as part of a lookahead carry scheme.
$\overline{G}$/N	Carry Generate/Negative	A multipurpose pin that indicates the carry generate function at the LSS and IS slices and the sign of the ALU result of the MSS slice.
$\overline{P}$/OVR	Carry Propagate/Overflow	A multipurpose pin that indicates the carry propagate function at the LSS and IS slices and the conventional two's complement overflow signal at the MSS slice.
Z	Zero	An open-collector input/output pin. When high, generaly indicates that the Y_{0-3} outputs are all low. For some special functions, Z is used as an input pin.
SIO_0, SIO_3	Shift Input/Output Lines	Bidirectional serial shift input/output lines for the ALU shifter. During a shift up operation, SIO_0 is an input and SIO_3 is an output. During a shift down operation, SIO_3 is an input and SIO_0 is an output.
QIO_0, QIO_3	Shift Input/Output Lines	Bidirectional serial shift input/output lines for the Q shifter. Operate similarly to SIO_0, SIO_3.
$\overline{LSS}$	Least Significant Slice	When tied low, programs the slice to act as the least significant slice of an array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE/MSS}$. When tied high, programs the slice to act as the most significant slice and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE/MSS}$	Write/Most Significant Slice	The $\overline{WRITE}$ output appears on this pin when $\overline{LSS}$ is tied low. The $\overline{WRITE}$ signal is low when an instruction that writes data into the RAM is executed. When LSS is tied high, $\overline{WRITE/MSS}$ is an input pin. Tying the pin high then programs the slice to act as an intermediate slice. Tying it low programs the slice to act as the most significant slice.

Y_{0-3}	Y Bus Input/Output	Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
$\overline{OE_Y}$	Y Output Enable	When low, enables the ALU shifter output data onto the Y_{0-3} lines. When high, disables the Y_{0-3} tri-state output buffers.
CP	Clock Input	A low-to-high transition will clock the Q register and sign compare flip-flop. When enabled by $\overline{WE}$, Data will be written into the RAM when CP is low.

Each microprocessor slice contains a 16-word-by-16-bit, two-port random access memory (RAM) with latches on both output ports; a high-performance arithmetic logic unit (ALU) with ALU shifter; a multipurpose Q register with Q shifter; and a nine-bit instruction decoder. Multiplexers at the ALU inputs allow various pairs of source operands to be selected. The source operand pairs may be selected, in any combination, from two external and two internal sources.

The RAM can read any two words addressed at its A and B address ports simultaneously, and output these words via the respective output ports. If the same address is applied to both address ports, the data at the A and B output ports will be identical. Control ROM bits RB65 through RB68 are applied to all four microprocessor slices as the A address bits; control ROM bits RB59 through RB62 are used as the B address bits. The data written into the RAM can be external data from the microprocessor Y input/output port or internal data from the ALU shifter, enabled onto the Y input/output lines. Data from the RAM can be held in the latches at the output ports if the clock input (CP) is low, or read out directly via the microprocessor DB input/output port if the tri-state output enable line ($\overline{OE_B}$) is low. The RAM data outputs are applied to the multiplexers at the ALU inputs.

One multiplexer selects either external data (control ROM bits RB65 through RB68, RB69 through RB72, RB73 through RB76, or RB77 through RB80) or the RAM A output port as the source of one of the ALU operands. The operation of this multiplexer is controlled by the enable A ($\overline{E_A}$) input, control ROM bit RB49. The other multiplexer selects either the RAM B output port, the DB input/output port, or the Q register as the source of the second ALU operand. The $\overline{OE_B}$ and I_0 lines (control ROM bits RB48 and RB50) conrol the operation of the second multiplexer.

The ALU can perform seven arithmetic and nine logical operations on the two, four-bit operands input from the multiplexers. The ALU also accepts a carry in input (C_n). The C_n lines to the most significant slice (MSS), U8, and the intermediate slices (IS), U16 and U28, are developed via lookahead carry generator U17. The C_n line to the least significant slice (LSS), U35, is developed via programmable logic array U36. The output of U36 is also applied as an input to U17. The ALU generates a carry out output (C_{n+4}), as well as carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) outputs. These outputs are needed to complete the lookahead

carry scheme. The ALU also generates two status outputs: negative (N) and overflow (OVR). The C_{n+4} output of slice U8 is latched into flip-flop U23, along with the Z output line from all the slices, to indicate microcontroller ALU status (ALUSTAT Z) to the sequence multiplexer (U42, U47, U55). The C_{n+4} outputs of the other slices are not used.

The $\overline{G}/N$ and $\overline{P}/OVR$ outputs of slices U16, U28, and U35 are applied as inputs to U17. The $\overline{G}/N$ output of slice U8 is applied as an input to shift control logic array U6. (The $\overline{P}/OVR$ output of U8 is not used.) U6 develops the serial shift inputs (SIO_0, SIO_3, QIO_0, and QIO_3) for the MSS and LSS ALU and Q shifters. U6 is controlled by control ROM bits RB44 through RB47.

The four-bit output of the ALU (F_0 through F_3) is passed to the ALU shifter and the Q register.

The ALU shifter can pass the ALU output unaltered, shifted up one bit position, or shifted down one bit position. Both arithmetic and logical shift operations can be performed. The ALU shifter also allows the sign input (SIO_0) to be extended across slice boundaries, through the Y input/output lines. The ALU shifter includes a cascadable, five-bit parity generator/checker for ALU error detection. The operation of the ALU shifter is controlled by the instruction inputs to the microprocessor slice.

The Q register is an auxiliary four-bit register used primarily for multiplication and division operations. The Q register can also be used as an accumulator or holding register. The shifter at the Q register input allows the contents of the Q register to be shifted one bit position up or down. However, only logical shifts can be performed. The operation of the Q register and shifter is controlled by the instruction inputs to the microprocessor slice.

The instruction decoder accepts instruction inputs I_0 through I_8 (control ROM bits RB50 through RB58) and generates the internal control signals needed for operation of the microprocessor slice. The instruction enable ($\overline{IEN}$) and least significant slice ($\overline{LSS}$) inputs and the write/most significant slice ($\overline{WRITE/MSS}$) input/output lines are used to condition and enable instruction decoder operation.

3.9.5.9 RAM Registers. The RAM registers consist of four, 256-word-by-4-bit, static random-access memories, U9, U15, U22, and U29.

Control ROM bits RB34 through RB40 are used as the first seven address inputs to the RAM registers; RB41 or an output of octal D-type flip-flop U13 is used as the eighth address input. (Other outputs of U13 may also be present as the first seven address inputs to U22.) These inputs select the row/column address of any data element contained in the RAM 32 x 32 memory array.

Digital graphic controller Y bus bits Y_0 through Y_{15} are used as the data inputs to the RAM registers. Y_0 through Y_3 are input to U29, Y_4 through Y_7 are input to U22, Y_8 through Y_{11} are input to U15, and Y_{12} through Y_{15} are input to U9. Since the chip select inputs ($\overline{CS_1}$ and CS_2) are tied to their appropriate active-state voltage levels, the RAM registers are always enabled. Data is clocked into the RAM registers whenever the write enable line ($\overline{WE}$) is low. This low is supplied by a timing pulse (STR line T9), developed via 3-line to 8-line decoder U24 under ROM control.

The RAM register outputs are enabled onto the digital graphic controller internal data bus, as bits DB0 through DB16, when the output enable line ($\overline{OE}$) is low. This low is supplied by ENA line S7, developed via 1 of 10 decoder U81 under ROM control.

Refer to the GRAPHIC 8 programmer's reference maual (H-80-0444) for a description of the address, size, and number of bits used for each of the digital graphic controller RAM registers.

3.9.5.10 16-Bit by 16-Bit Multiplier. The 16-bit by 16-bit multiplier is contained on a single chip, U1.

The multiplier and multiplicand data for U1 are loaded into X and Y input registers. Y bus bits Y0 through Y15 are loaded into the X input register; internal data bus bits DB0 through DB15 are loaded into the Y input register. X_0 and Y_0 are the least significant bits and X_{15} and Y_{15} are the most significant bits. Each register is clocked by its own clock input. Both clock inputs are developed via programmable logic array U2. The X input clock also clocks the U1 output register. The Y input register port is bidirectional; the first 16 bits (the least significant product, or LSP) of product data are also passed out via this port.

The numerical system used for multiplication in the digital graphic controller is unsigned magnitude. The output contents can be added to or subtracted from the next product, or the accumulate function can be disabled for multiply only.

Control ROM bit RB21 is applied to U1 as the accumulation control input, ACC. When ACC is high, the contents of the output registers are added to the next product generated and their sum is stored back into the output registers at the rising edge of the clock input. When ACC is low, multiplication without accumulation is performed and the next product generated will be stored into the output registers directly. The ACC signal is loaded into an ACC register at the rising edge of either clock input. The ACC signal is valid over the same period that the input data is valid. Since the subtraction control input (SUB) is tied low, addition is always performed instead of subtraction when ACC is high.

The LSP and most significant product (MSP) output buffers on U1 are disabled when the tri-state least and most control lines (TSL and TSM) are high. These are direct, non-registered control signals. The output drivers on U1 are enabled when TSL and TSM are low. These enables are supplied by ENA lines S8 and S9, respectively. The ENA S8 and S9 lines are developed via 1 of 10 decoder U81, under ROM control. Since the preload control line (PREL) to U1 is tied low, the multiplier output registers will be enabled whenever S8 and S9 are low.

The data outputs of U1 (P_0 through P_{31}) are enabled onto the digital graphic controller internal data bus in two 16-bit bytes. P_0 is the least significant bit and P_{31} is the most significant bit. The 32-bit product is divided into the LSP (P_0 through P_{15}) and the MSP (P_{16} through P_{31}). The product generated is loaded into the output registers on the rising edge of the clock input.

3.9.5.11 Character ROM. The character ROM consists of a 2K-by-8-bit, programmable read-only memory, U36.

U36 is enabled by the Y output enable (OE_Y) from the microcontroller. U36 can also be enabled by the ENA S1 line. This signal is developed via 1 of 10 decoder U81, under ROM control. The S1 line is active low, and is inverted by NAND gate U33B before being applied to the second chip select (CS_2) of U36. (The other chip select, CS_1, is tied to its active-state voltage level, so that CS_2 will control operation of the ROM.)

The digital graphic controller internal data bus bits (DB0 through DB010) are applied to U36 as address bits A0 through A10. The address applied to the character ROM is generated using the ASCII code of the character and the sign extend multiplexer (U4 and U11). The sign extend multiplexer shifts the ASCII code four places to the left and sign extends the LSB of the ASCII code four places to the right. If the address is even, the digital graphic controller will increment through the ROM character table; if the address is odd, the digital graphic controller will decrement through the table.

If a shift out character is desired, a zero is inserted for the MSB (DB011) of the character address. DB011 is applied to the third chip select input (CS_3) of U36. This forces the addressing to the extended character set, provided the digital graphic controller has been optionally equipped for extended characters. The extended character set is physically located on a second character ROM, U3. When installed on the digital graphic controller circuit card, U3 can only be enabled by the combination of the OE_Y signal and a zero on DB011.

Once the character ROM has been enabled and the character address applied, the digital graphic controller scans each line of the ROM character table for bits that are set. When it finds a set bit, the digital graphic controller performs a store-to-pixel-memory operation. It then continues scanning until the LSB of the character ROM flags the end of the character. The character is output onto the digital graphic controller Y bus as bits Y0 through Y7.

3.9.5.12 Raster Bus Control. The raster bus control logic consists of bus busy flip-flop U73B, flip-flop U32B/U33C, row address strobe (RAS) flip-flop U32A/U33D, column address strobe (CAS) flip-flop U40A/U40B, read/write flip-flop U39B, bus cycle timeout counter U25, and tri-state buffered output U50. A timing diagram of raster bus control is shown in figure 3-27.

When the digital graphic controller performs a write pixel operation, it first checks U73B to see if a bus cycle is in progress. If the BUS BUSY output of U73B is high, indicating no bus cycle is in progress, the digital graphic controller loads the raster MAR and initiates a raster bus request. (The pixel data was written into the raster I/O transmit registers beforehand.) U73B will be cleared on the next clock pulse, indicating that the digital graphic controller has seized control and the bus is now busy.

The raster bus request sets U32A/U33D. The output of this flip-flop enables the raster MAR row address registers (U51, U59, and U72), via NAND gate U60B. These registers latch the pixel Y address. The complement of this output, via NAND gate U80A, is used to hold the raster MAR column address registers (U64, U76, and U83) disabled. Thus, only one 16-bit pixel address segment is enabled onto the bus at a time. The row address enable is delayed 60 nanoseconds by delay line DL1, inverted by NAND gate U80C, and output as the row address strobe (GRAS-H) via U50. This strobe clocks the address information on the bus into the mapping memory. The addressed device then responds with a row memory acknowledge (GRMK+B), indicating that it has latched the address information.

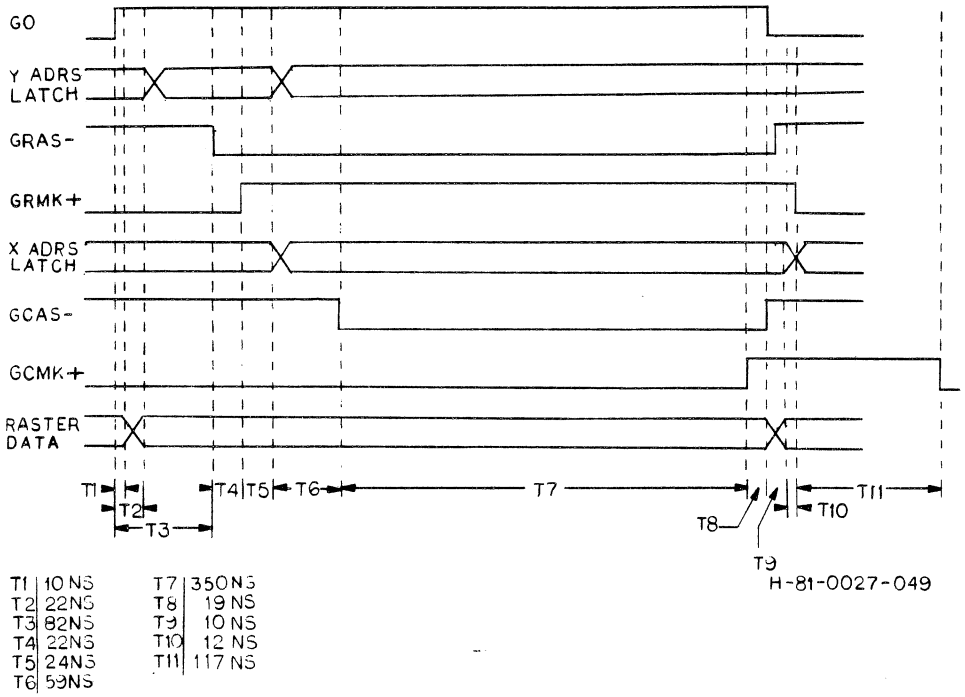


Figure 3-27. Raster Bus Timing Diagram

GRMK+B is passed via U50 and NAND gate U60C, and sets U40A/U40B. The output of this flip-flop disables the raster MAR row address registers and enables the raster MAR column address registers. This removes the first 16-bit address segment from the bus and puts the second 16-bit address segment out to the mapping memory. The column address enable is delayed 59 nanoseconds by delay line DL2, inverted via NAND gate U80B, and output as the column address strobe (GCAS-H) via U50. The addressed device then responds with a column memory acknowledge (GCMK+B) indicating that it has latched the address information.

GCMK+B is passed via U50 and NAND gate U60A, and resets U32A/U33D. This flip-flop in turn resets U40A/U40B, which starts counter U25. U25 is preset to a count of eight, and will count up to its maximum count (15) in 2.4 microseconds. When U25 reaches its maximum count, its output goes true and set U32B/U33C. The output of this flip-flop then sets U73B on the next clock pulse, removing the BUS BUSY signal. The RAS, CAS, pixel address and pixel data are then removed from the bus when the flip-flops are cleared.

U39B is set by Y bus bit Y3 when the function bits are loaded into the raster MAR. U39B is clocked by a timing pulse (STR line T14) developed via 3-line to 8-line decoder U24, under ROM control. U39B controls whether the digital graphic controller will perform a read or a write operation during the raster bus cycle.

3.9.5.13 Raster MAR. The raster MAR consists of six octal D-type flip-flops: U51, U59, U64, U72, U76, and U83.

The raster MAR is clocked by timing pulses (STR lines T3, T14, and T15) developed via 3-line to 8-line decoders U18 and U24, under ROM control.

The raster MAR receives its inputs from the digital graphic controller internal data bus (bits DB0 through DB010) and Y bus bits Y0 through Y10). U51 is used to store the bits that define which display is selected. Four bits are presently used; one bit is available for future expansion. U64 is used to store the bits that define the function to be executed.

When the digital graphic controller is performing a read- or write-pixel-to-memory operation, U51, U59, and U72 latch the Y (or row) address of the pixel and U64, U76, and U83 latch the X (or column) address. Each row/column address is 16-bits long. Since the digital graphic controller raster address bus (AG00+H through AG15+H) is only 16 bits wide, the row and column address segments are multiplexed out to the mapping memory cards. The Y address is always enabled onto the bus first. The X address is not enabled until the mapping memory responds with a row memory acknowledge (GRMK+B). This handshaking is described in more detail in the foregoing paragraph.

When the digital graphic controller addresses a video controller card, the data bits input to U51 will all be zeros. All the GRAPHIC 8 video controllers decode this as their own unique address, and respond to the digital graphic controller to indicate that they are ready to accept configuration data. Bits DB0 through DB3 are then used to select which specific video controller will be configured with the new data.

3.9.5.14 Raster I/O Data Registers. The raster I/O data registers consist of four octal D-type flip-flops, U75, U82, U89, and U90; and read/write flip-flop U39B. U75 and U82 are the raster I/O data receive registers; U89 and U90 are the raster I/O data transmit registers.

For a read-from-pixel-memory operation, the GRAPHIC 8 raster data bus bits (DB00+B through DB11+B) are applied as inputs to U75 and U82. The outputs of U75 and U82 are enabled onto the digital graphic controller internal data bus as bits DB0 through DB011. U75 and U82 are enabled by ENA S2 line. The ENA S2 line is developed via 1 of 10 decoder U81, under ROM control.

For a store-to-pixel-memory operation, the digital graphic controller internal data bus bits are applied as inputs to U89 and U90. These data bits are clocked into U89 and U90 by a timing pulse (STR line T5) developed via 3-line to 8-line decoder U18, under ROM control. The outputs of U89 and U90 are enabled onto the GRAPHIC 8 raster data bus as bits DB00+B through DB11+B.

U39B controls the operation of the raster I/O data registers and is set when the raster MAR function bits (AG11 through AG15) are set. The output of U39B clocks U75 and U82, via NOR gate U61. The output of U39B is also used to enable U89 and U90, via NAND gate U33A.

During turn-on, U39B is initialized to the read state. This allows the digital graphic controller to read the GRAPHIC 8 configuration register, located on the timing module circuit card, before beginning any operation.

3.10 MAPPING MEMORY

3.10.1 PHYSICAL DESCRIPTION. The mapping memory is an 8-layer printed circuit card, 7-3/4 by 12 inches. It is located in the region of slots XA8 through XA16 of the basic GRAPHIC 8 configuration. The mapping memory connects to the backplane through 98-pin connector P1.

3.10.2 APPLICATION. One or two mapping memory cards may be used per display. When one mapping memory card is used, the digital graphic controller and the video controller must share access to it. When two mapping memory cards are used, the video controller can read data from one while the digital graphic controller is updating the other. When the update is complete, the two controllers exchange ownership of the mapping memories. Dynamic pictures can be created by switching back and forth between the two mapping memories.

The mapping memory stores pixel (picture element) data for the raster scan display of the GRAPHIC 8 system. Two models of mapping memory are available:

Part no. 5977176 has a 16K by 64-bit RAM
Part no. 5802554 has a 64K by 64-bit RAM

Each point of light on the display corresponds to a location in memory; the range of memory resolution is from 512 by 512 locations to 2048 by 2048 locations, depending on the architecture selected. Memory resolution is factory set by configuration switches and jumpers in accordance with the customer's requirements.

Pixel color is also a function of data stored in the mapping memory, and may require 1, 2, 4, or 8 bits per pixel, depending on the selected configuration. The number of different colors possible at any given instant is a function of the bits per pixel.

Number of colors = 2^n where n = bits per pixel.

When n = 1, the colors available are black and white. When n = 8, 256 colors are available. One of the bits may be used as a blink bit; however, this divides the number of colors available by two.

3.10.3 FUNCTIONAL DESCRIPTION. The mapping memory performs four types of operations:

1. Memory read by the video controller.
2. Memory refresh by the video controller.
3. Memory write by the digital graphic controller.
4. Memory read by the digital graphic controller.

The video controller operations have the highest priority.

Figure 3-28 shows the relationship of the mapping memory to the other elements of the GRAPHIC 8 system. During a memory read by the video controller, the mapping memory receives address information from the video controller, and responds by returning pixel data and acknowledge signals. During a memory refresh by the video

controller, the mapping memory receives an instruction from the video controller and responds by performing the refresh operation and returning acknowledge signals.

During a memory write by the digital graphic controller, the mapping memory receives address information and pixel data from the graphic controller, and responds by writing the data into memory and returning acknowledge signals. During a memory read by the digital graphic controller, the mapping memory receives address information from the digital graphic controller and responds by returning pixel data and acknowledge signals.

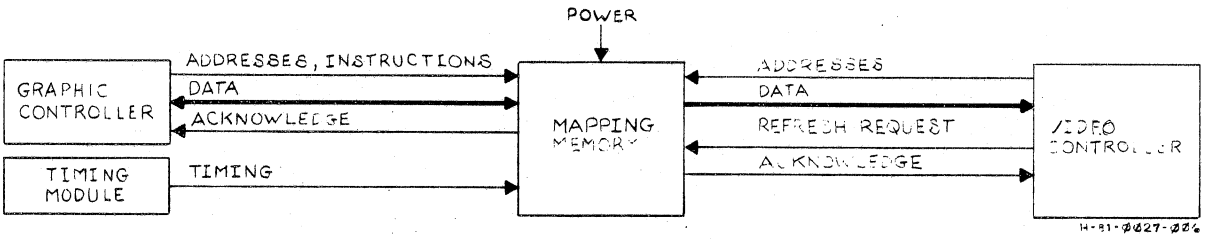


Figure 3-28. Relationship of Mapping Memory to Other Elements of the GRAPHIC 8 System

3.10.4 BLOCK DIAGRAM DESCRIPTION. See figure 3-29. The control logic and the address/instruction latch and decode circuits operate together to produce timing and control signals that control the operations of the other circuits. The address/instruction latch and decode circuit also produces the addresses for the memory matrix.

The memory matrix consists of 64 chips (either 16K or 64K) organized as eight rows and eight columns. The digital graphic controller can write into memory; both the digital graphic controller and the video controller can read from memory.

The video output format logic is a shift register that is configured as a function of system architecture. Its possible configurations are:

1. A single 64-bit shift register.

2. Two 32-bit shift registers.

3. Four 16-bit shift registers.

4. Eight 8-bit shift registers.

The output data stream from the shift register becomes the input data stream to the video controller.

The data select multiplexer reads a single pixel from the memory matrix, where a single pixel may consist of 1, 2, 4, or 8 bits of information. The number of bits per pixel is set by switches and jumpers at the factory and is not changeable in the field. The multiplexer output goes to the digital graphic controller.

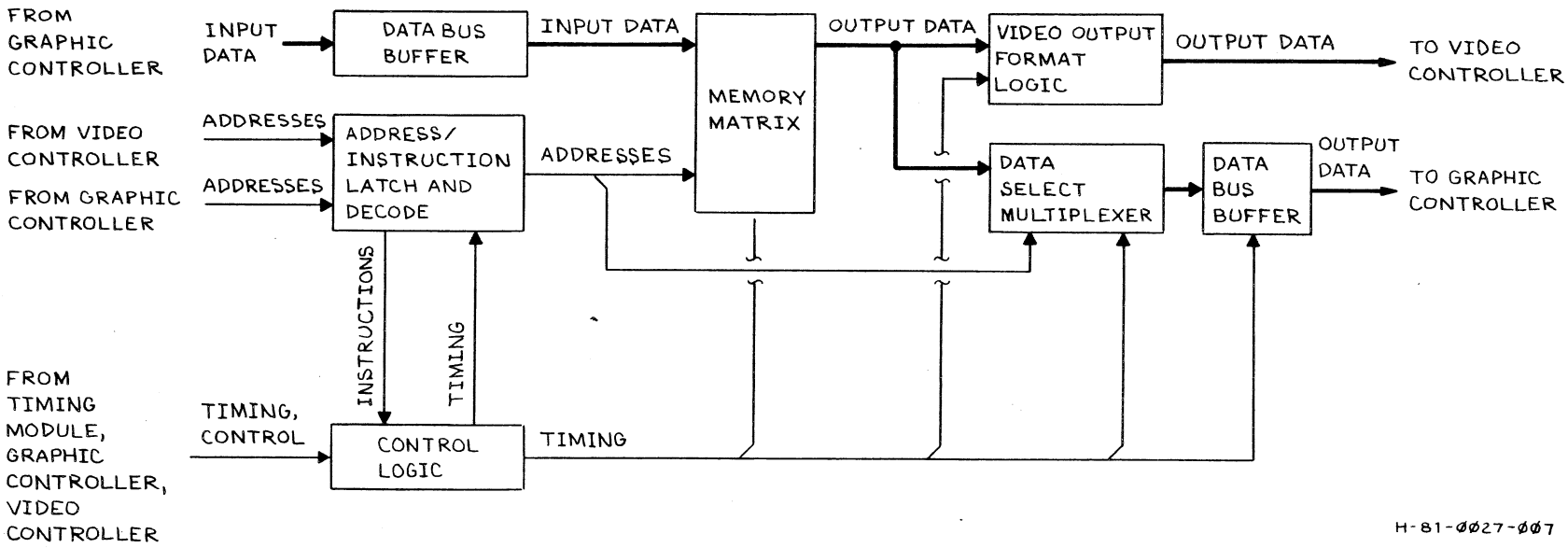


Figure 3-29. Mapping Memory Block Diagram

3.10.5 DETAILED OPERATION. The following paragraphs describe in more detail the makeup and operation of each of the blocks of figure 3-29.

3.10.5.1 Control Logic. The control logic (see figure 3-30) produces a number of timing and control signals (S0 through S19) and acknowledge signals in response to inputs from the timing module, digital graphic controller, video controller, and certain circuits on the mapping memory card itself.

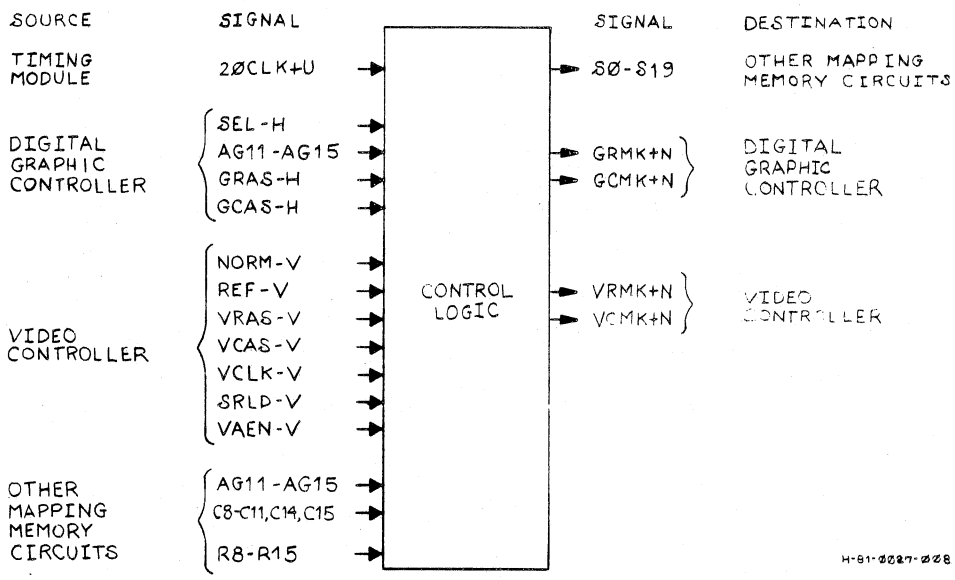


Figure 3-30. Mapping Memory Control Logic Inputs and Outputs

Table 3-23 describes the functions of each of these input and output signals.

Table 3-23. Mapping Memory Control Logic Input and Output Signals

SIGNAL	DESCRIPTION INPUT SIGNALS
20CLK+U	20 MHz square wave from timing module.
SEL-H	Select signal from digital graphic controller. In conjunction with the settings of configuration switches U132 EE through HH lets the digital graphic controller define and select either mapping memory A or mapping memory B. This signal is of no import in a single-memory system. The function of this signal can be overridden by the NORM-V signal from the video controller.
GRAS-H	Row address strobe from the digital graphic controller. This signal, inverted, becomes S0. Used during digital graphic controller read or write operations.
GCAS-H	Column address strobe from the digital graphic controller. This signal, inverted, becomes S1. Used during digital graphic controller read or write operations.
NORM-V	Normal signal from the video controller. When active (low), overrides the effect of the SEL-H signal from the digital graphic controller, giving the video controller first crack at the mapping memory.
REF-V	Refresh signal from the video controller. On receipt of this signal, the mapping memory refreshes itself. This signal appears a certain number of times (0 through 7) during the display vertical retrace period; the number of REF-V pulses is determined by switch settings on the video controller. This signal leads to the production of timing signals S6, S7, S12.
VRAS-V	Row address strobe from the video controller. This signal, inverted, becomes S3. Used during video controller read operations.
VCAS-V	Column address strobe from the video controller. This signal, inverted, becomes S4. Used during video controller read operations.
VCLK-V	Clock signal from the video controller. This signal, inverted, becomes S16. Used during video controller read operations.
SRLD-V	Shift register load from the video controller. This signal, inverted, becomes S17. Used during video controller read operations.
VAEN-V	Vertical access enable from the video controller. This signal defines a time window during which signal S18 may occur.

Table 3-23. Mapping Memory Control Logic Input and Output Signals (Cont)

SIGNAL	DESCRIPTION
	INPUT SIGNALS
AG11-AG15	Address bits from the digital graphic controller. These bits are used to address to correct display (i.e., the correct pair of memory cards)
C8-C10	Column address bits from the column address latches containing clipping information.
C11, C14, C15	Column address bits from the column address latches containing instructions relative to read, write, or read-modify-write operations. These signals contribute to the generation of S9, S11, S13.
R8-R10	Row address bits from the row address latches containing clipping information.
R11-R15	Row address bits from the row address latches containing instructions relative to write operations. These signals contribute to the generation of S9.
	OUTPUT SIGNALS
S0	Clock pulse to the graphic row address latch.
S1	Clock pulse to the graphic column address latch.
S2	Output enable to both the graphic row address latch and the graphic column address latch.
S3	Clock pulse to the video row address latch.
S4	Clock pulse to the video column address latch.
S5	Output enable to both the video row address latch and video column address latch.
S6	Clock pulse to the refresh row address counter.
S7	Output enable to the refresh row address counter.
S8	Input select to the 2-line to 1-line multiplexer.
S9	Output enable to the write enable PROM.
S10	Output enable to the CAS PROM.
S11	Output enable to the multiplexer PROM.
S12	Four lines of row address strobes ($\overline{RAS}$) to the memory matrix.

Table 3-23. Mapping Memory Control Logic Input and Output Signals (Cont)

SIGNAL	DESCRIPTION OUTPUT SIGNALS
S13	Transmit/receive signal to the bidirectional data buffer.
S14	Chip enable to the bidirectional data buffers.
S15	Load to the 64-bit video data latch.
S16	Clock pulses to the video data shift register and 8-bit pixel latch.
S17	Shift/load control to the 64-bit video data shift register.
S18	Output enable to the 8-bit pixel latch.
S19	Clock pulse to the 8-bit read-modify-write latch.
VRMK+N	Row acknowledge signal to the video controller.
VCMK+N	Column acknowledge signal to the video controller.
GRMK+N	Row acknowledge signal to the digital graphic controller.
GCMK+N	Column acknowledge signal to the digital graphic controller.

3.10.5.2 Address/Instruction Latch and Decode. See figure 3-31. The address/instruction latch and decode circuits receive as inputs:

1. Addresses AG00-AG15 from the digital graphic controller.
2. Addresses AV00-AV10 from the video controller.
3. Timing signals S0-S11 from the control logic.

The address/instruction latch and decode circuits produce the following outputs:

1. Memory adress $\overline{AA0}$-$\overline{AA7}$ and $\overline{BA0}$-$\overline{BA7}$.
2. Column address strobes $\overline{CAS00}$-$\overline{CAS07}$, which strobe the column addresses into the correct memory chips in the memory matrix.
3. Write enable signals $\overline{WE00}$-$\overline{WE07}$, which let the digital graphic controller write data into the proper memory chips in the memory matrix.
4. Multiplexer data signals MUX00-MUX15, which go to the data select multiplexer.
5. Miscellaneous signals (AG11-AG15, C8-C11, C15, R8-R15) that go to the control logic.

Table 3-24. Memory Options and Configuration Switch Settings

OPTION	MEMORY SIZE Y	MEMORY SIZE Y	BITS PER PIXEL	SHIFT REGISTER	SWITCH SETTINGS A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X
					64K MEMORY																							
1	2048	2048	1	1 @ 64 bits	O	C	O	O	O	C	O	C	O	O	O	C	O	O	C	C	C	O	C	O	C	O	C	O
2	1024	2048	2	2 @ 32 bits	O	O	C	O	O	C	O	C	O	O	O	C	O	O	O	C	C	O	C	O	O	C	C	O
3	2048	1024	2	2 @ 32 bits	O	O	C	O	O	C	O	O	O	O	C	C	O	O	O	C	O	C	C	O	C	O	C	O
4	1024	1024	4	4 @ 16 bits	O	O	C	O	O	C	O	O	O	C	O	C	O	O	C	O	O	C	C	O	O	C	C	O
5	512	1024	8	8 @ 8 bits	O	O	C	O	O	O	C	O	O	C	O	C	O	O	O	O	O	C	C	O	O	C	O	C
6	1024	512	8	8 @ 8 bits	O	O	C	O	O	O	O	O	O	C	O	O	O	O	O	O	O	C	O	C	O	C	C	O
					16K MEMORY																							
7	1024	1024	1	1 @ 64 bits	C	O	O	O	O	C	O	O	C	O	O	C	O	O	C	C	O	C	C	O	O	C	C	O
8	512	1024	2	2 @ 32 bits	C	O	O	O	C	O	O	O	C	O	O	C	O	O	O	C	O	C	C	O	O	C	O	C
9	1024	512	2	2 @ 32 bits	C	O	O	O	O	C	O	O	C	O	O	O	O	C	O	C	O	C	O	C	O	C	C	O
10	512	512	4	4 @ 16 bits	C	O	O	C	O	O	O	O	C	O	O	O	O	C	C	O	O	C	O	C	O	C	O	C

C = closed
O = open

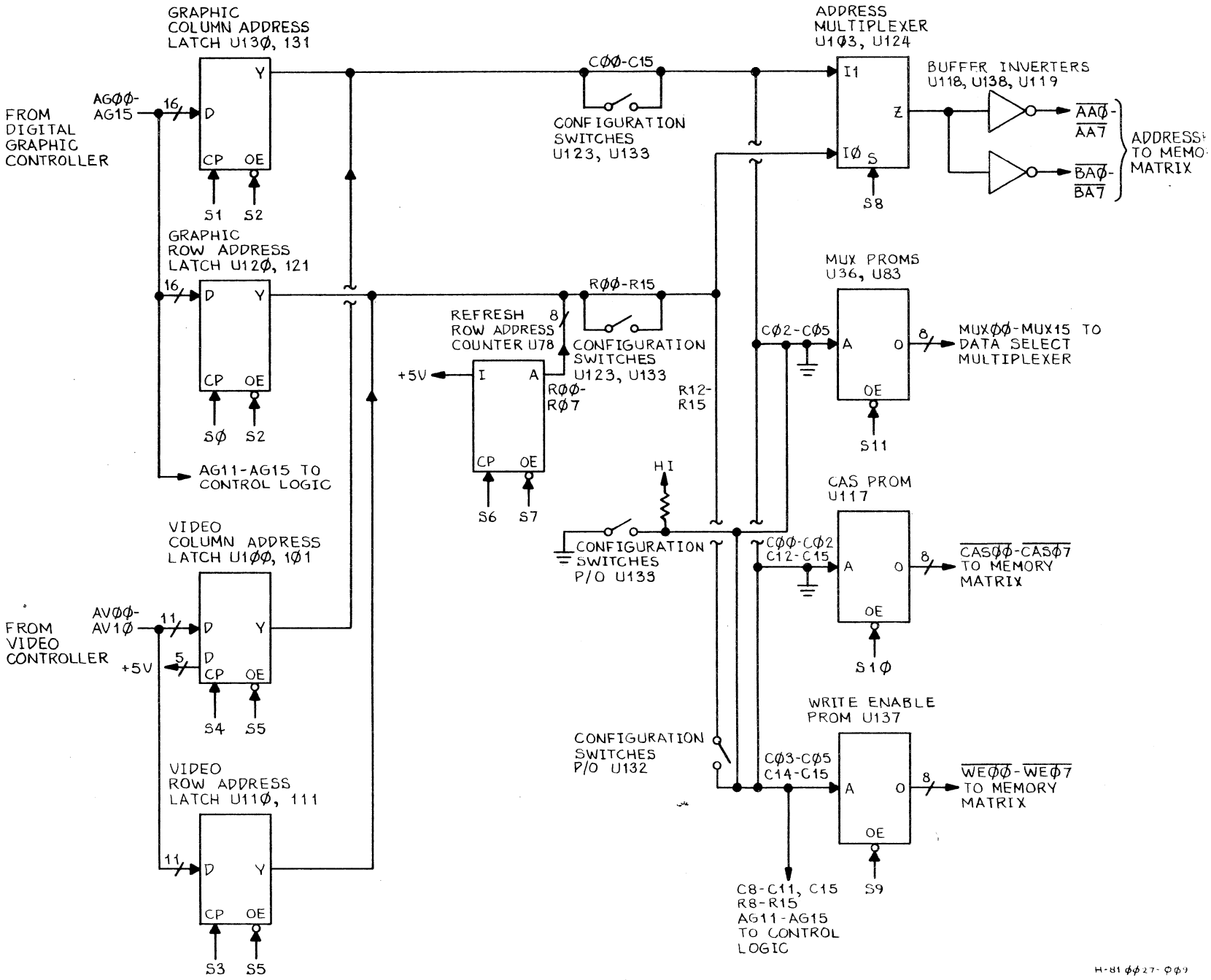


Figure 3-31. Address/Instruction Latch and Decode, Block Diagram

Timing signals S2, S5, and S7 are mutually exclusive. The outputs of the column address latches and row address latches (C00-C15 from R00-R15) can represent any of their three inputs.

During a refresh cycle, row address information (R00-R07) comes from the refresh row address counter, which is enabled by S7 and clocked by S6. Each memory location must be refreshed at least once every two milliseconds, or the memory data will be lost. In practice, refresh cycles occur approximately every 15 microseconds. At the end of a video refresh cycle, the row address counter increments in preparation for the next video refesh cycle.

The configuration switches establish the shape of the memory array to conform with the system configuration and memory configuration. The configuration switches are set at the factory and should not be changed in the field. Table 3-24 defines the options available and the configuration switch settings for those options.

Signals S8 from the control logic selects either the I0 (row addresses) or I1 (column addresses) as inputs to the address multiplexer. The selected signals are inverted and buffered and go to the memory matrix as the memory address signals, $\overline{AA0}$-$\overline{AA7}$ and $\overline{BA0}$-$\overline{BA7}$.

During any memory operation, the column address strobes are generated by CAS PROM U117 in response to the column address inputs. PROM outputs are enabled by timing signal S10. The PROM outputs are $\overline{CAS00}$ through $\overline{CAS07}$.

During memory write operations, the write enable signals are generated by write enable PROM U137 in response to the column address inputs. PROM outputs are enabled by timing signal S9. The PROM outputs are $\overline{WE00}$ through $\overline{WE07}$.

During memory read operations by the graphic controller, memory data outputs are applied as the inputs to a data select multiplexer. The select signals that operate the data select multiplexer are the MUX00 through MUX15 signals from the MUX PROMs U36, U83 in the address/instruction latch and decode circuits. The MUX PROMs generate the MUX00 through MUX15 signals in response to the column address inputs. PROM outputs are enabled by timing signal S11. The configuration switches associated with this circuit determine whether the system supports one or two displays, and identify the display as shown in table 3-25.

Table 3-25. Display Select Switch Settings

	SWITCH SETTINGS										
DISPLAY	AA	BB	CC	DD	II	JJ	KK	LL	MM	NN	
1	O	O	O	O	O	O	O	C	C	O	
2	O	O	O	O	O	O	C	O	C	O	
3	O	O	O	O	O	C	O	O	C	O	
4	O	O	O	O	C	O	O	O	C	O	
5	O	O	O	O	O	O	O	C	O	C	C = closed
6	O	O	O	O	O	O	C	O	O	C	O = open
7	O	O	O	O	O	C	O	O	O	C	
8	O	O	O	O	C	O	O	O	O	C	
1 and 2	O	C	O	C	O	O	C	C	C	O	
3 and 4	C	O	C	O	C	C	O	O	C	O	
5 and 6	O	C	O	C	O	O	C	C	O	C	
7 and 8	C	O	C	O	C	C	O	O	O	C	

3.10.5.3 Memory Chain. The memory chain includes the bidirectional data bus buffer, memory matrix, data select multiplexer, and read-modify-write circuit, as shown in figure 3-32.

Bidirectional data bus buffer U2 receives data from the digital graphic controller or sends data to the digital graphic controller, according to the state of timing signal S13. The buffer is enabled by timing signal S14.

The memory matrix consists of 64 chips, organized as two banks of 32 chips each. Each chip contributes one bit to the 64-bit output of the total memory.

The 16K and 64K memory chips have different pin connections, as follows:

PIN	16K CHIP	64K CHIP
1	-5V	No connection
8	+12V	+5V
9	+5V	Address bit 7

These inputs are satisfied by jumper connections on the mapping memory card. Do not change these jumpers in the field.

The data select multiplexer is a 64 line-to-8, 4, 2, or 1 line selector with 3-state outputs. Signals C00, C01, and MUX00 through MUX15 select the signals to be passed.

The read-modify-write circuit is used to modify the contents of specific words of memory. The circuit operates as follows:

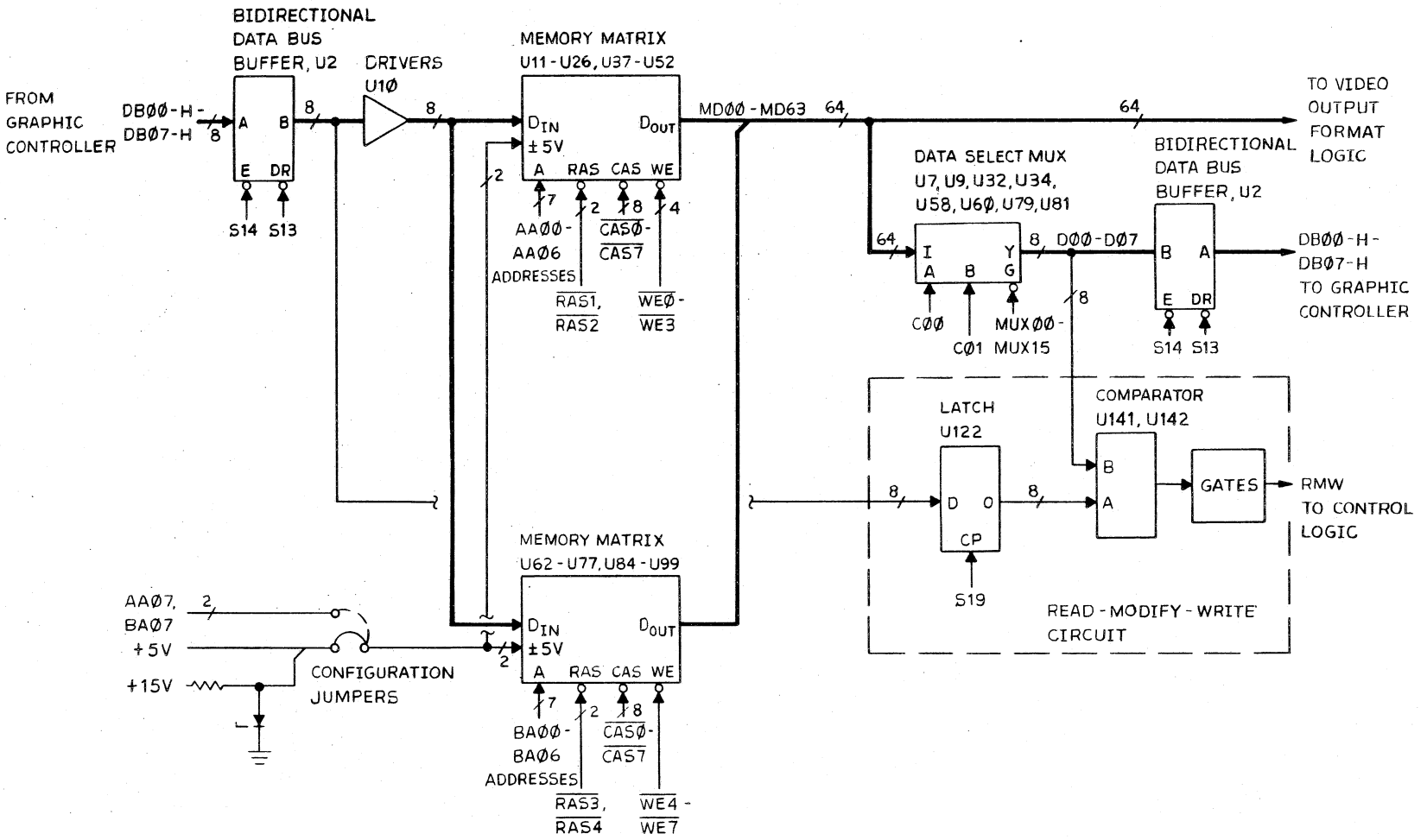
1. Input data is applied to the memory matrix D_{IN} pins and to the latch in the read-modify-write circuit; the row address is applied to the memory address pins at the same time.

2. The $\overline{RAS}$ strobes the row address into all memory chips; timing signal S19 clocks the latch, transferring the input data to the comparator.

3. The column address is applied to the memory address pins.

4. The CAS strobes the column address into the correct memory chips. $\overline{WE}$ is held high, so the memory output is applied through the data select multiplexer to the comparator. (The bidirectional data bus buffer is disabled.)

5. If the data in memory has a higher priority than the data in the latch, no further action is required and the memory returns the GCMK signal to the digital graphic controller. If the data in the latch has a higher priority than the data in memory, the bidirectional data bus buffer is enabled and the data out of the memory is disabled. $\overline{WE}$ is made low and the data present on the data lines is written into memory, overriding the data previously stored there. The memory returns the GCMK signal to the digital graphic controller.



H-81-ØØ27-Ø1Ø

Figure 3-32. Memory Chain Block Diagram

The decision to override or let stand is made in the comparator. Comparator output is the RMW (read-modify-write) signal that goes to the control logic.

3.10.5.4 Video Output Format Logic. See figure 3-33. This circuit receives the 64-bit data output of the memory matrix and presents the data to the video controller during a video read operation. The form of the data presentation is a function of the system configuration.

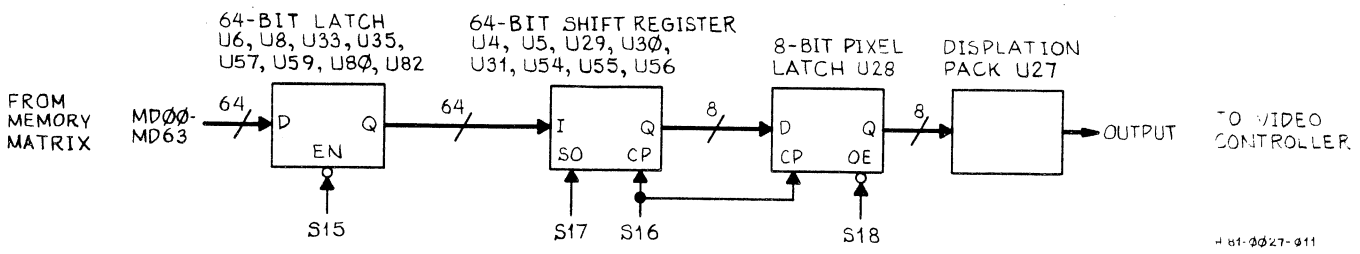


Figure 3-33. Video Output Format Logic Block Diagram

All 64 bits of memory data are applied to the 64-bit latch, which is loaded by timing signal S15. When needed, the data is loaded into the shift register, timing signal S17 enables SHIFT OUT and timing signal S16 clocks the data to the 8-bit pixel latch. Timing signal S18 enables the output of the 8-bit latch, passing the byte to the displation pack.

The displation pack is selected at the factory as a function of the system configuration and has 1, 2, 4, or 8 output lines, corresponding to the number of bits per pixel. Each data transfer from the mapping memory to the video controller consists of 64 bits, but represents 64, 32, 16, or 8 pixels. Although the shift register is loaded with 64 bits, the effective organization of the shift register is also a function of the system configuration. See table 3-26.

Table 3-26. Video Output Format Configurations

NUMBER OF BITS/PIXEL	SHIFT REGISTER ORGANIZATION	SHIFT REGISTER CLOCK PULSES	OUTPUT LINES TO VIDEO CONTROLLER
1	one 64-bit register	64	1
2	two 32-bit registers	32	2
4	four 16-bit registers	16	4
8	eight 8-bit registers	8	8

Figure 3-34 shows how the data moves from the shift register through the displation pack to the video controller for each of these cases (assuming that the 8-bit pixel latch is transparent).

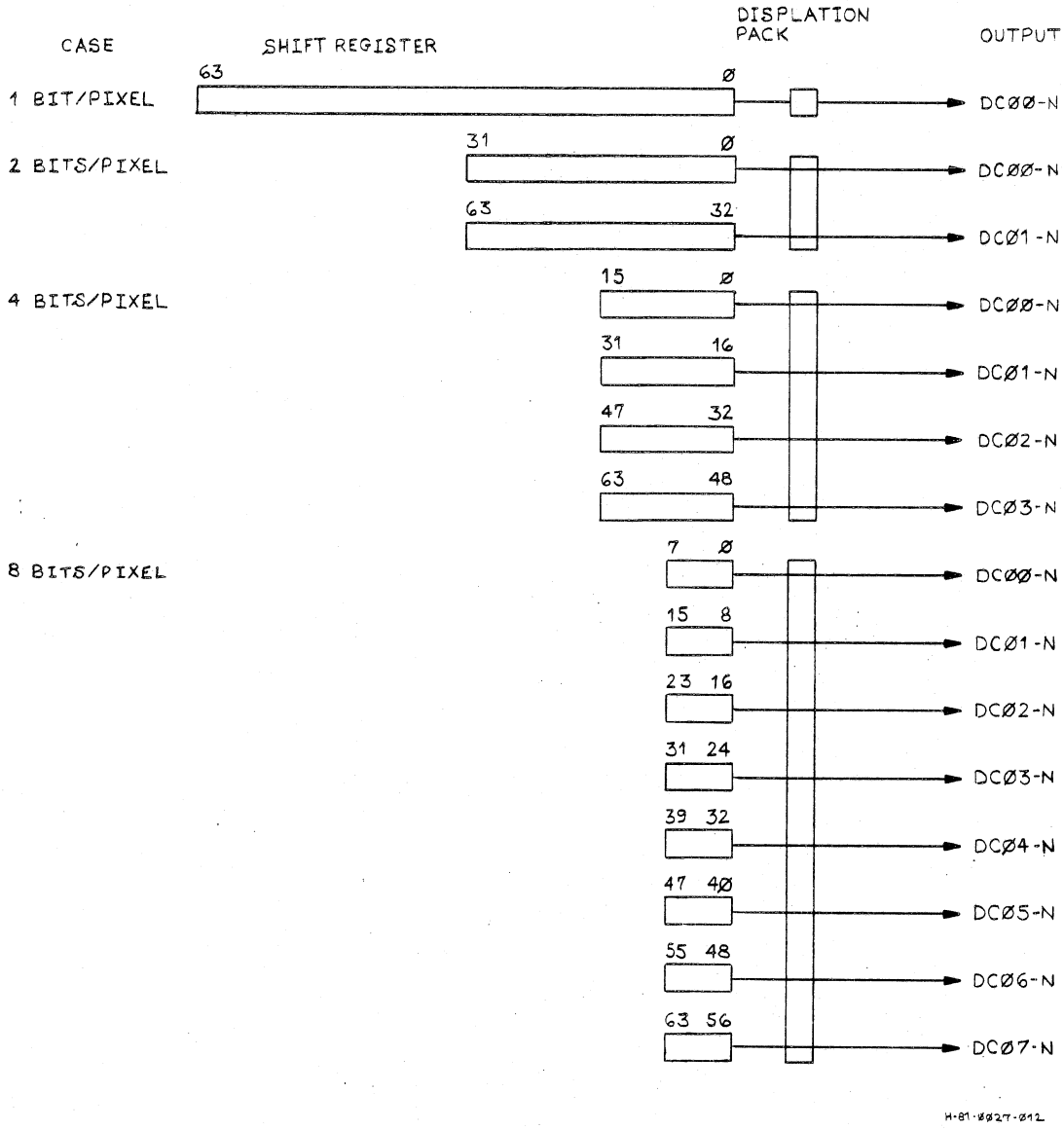


Figure 3-34. Video Output Format Configurations

3.10.6 OPERATING SEQUENCE. The following paragraphs describe the sequence of events for a refresh cycle, a video controller read cycle, a digital graphic controller write cycle, and a digital graphic controller read cycle.

3.10.6.1 Refresh Cycle. See figure 3-35. Signal REF-V from the video controller is applied to the control logic and the refresh row address counter. A CYCLE flip-flop in the control logic sets, causing the REFRESH flip-flop to set. The refresh row address counter supplies a row address to the memory matrix. The row of memory cells is refreshed when the memory row address is present and the control logic sends a $\overline{RAS}$ signal to the memory matrix. The acknowledge signal VRMK+V, goes to the video controller to terminate the refresh cycle; it also resets the flip-flops in the control logic. The refresh cycle typically takes place in an elapsed time of approximately 400 nanoseconds.

3.10.6.2 Video Read Cycle. See figure 3-36. The video controller puts a row address on the address bus and sends signal VRAS. The mapping memory control logic loads the row address latch and sends VRMK back to the video controller. The video controller responds by putting the column address on the address bus and sending VCAS. The control logic loads the column address latch.

After the row address data is latched, the control logic lets the row address be presented to the memory matrix via the address multiplexer. The control logic sends RAS to the memory matrix to select the addressed row.

After the column address data is latched, the data is presented to the memory matrix via the address multiplexer; these bits come from the configuration switches. Bits C12-C15 are applied to the CAS PROMs which generate the proper column address strobes and apply them to the memory matrix. The control logic then sends VCMK back to the video controller to terminate the read cycle; this signal also latches the memory output (MD00-MD63) into the 64-bit latch in the video output format logic. Subsequently the data is clocked out of the video output format logic to the video controller by a series of VCLK pulses from the video controller. A typical video read cycle takes 500 nanoseconds.

3.10.6.3 Graphic Controller Read Cycle. See figure 3-37. The graphic controller puts the row address on the address bus and sends GRAS. The mapping memory control logic loads the row address latch and sends GRMK back to the graphic controller. The control logic lets the latched row address be presented to the memory matrix.

The graphic controller puts the column address on the address bus and sends GCAS. The mapping memory control logic loads the column address latch, then generates the RAS and CAS signals to strobe the address into the memory matrix. the memory data appears at the memory output and is passed through the data select multiplexer and the bidirectional data bus buffer to the graphic controller. The control logic sends GCMK back to the graphic controller to terminate the cycle. Typical graphic controller read cycle time is typically 600 nanoseconds.

3.10.6.4 Graphic Controller Write Cycle. See figure 3-38. The graphic controller puts data on the data bus. The graphic controller also puts the row address on the address bus and sends GRAS. The mapping memory control logic loads the row address latch and sends GRMK back to the graphic controller. The control logic lets the latched row address be presented to the memory matrix.

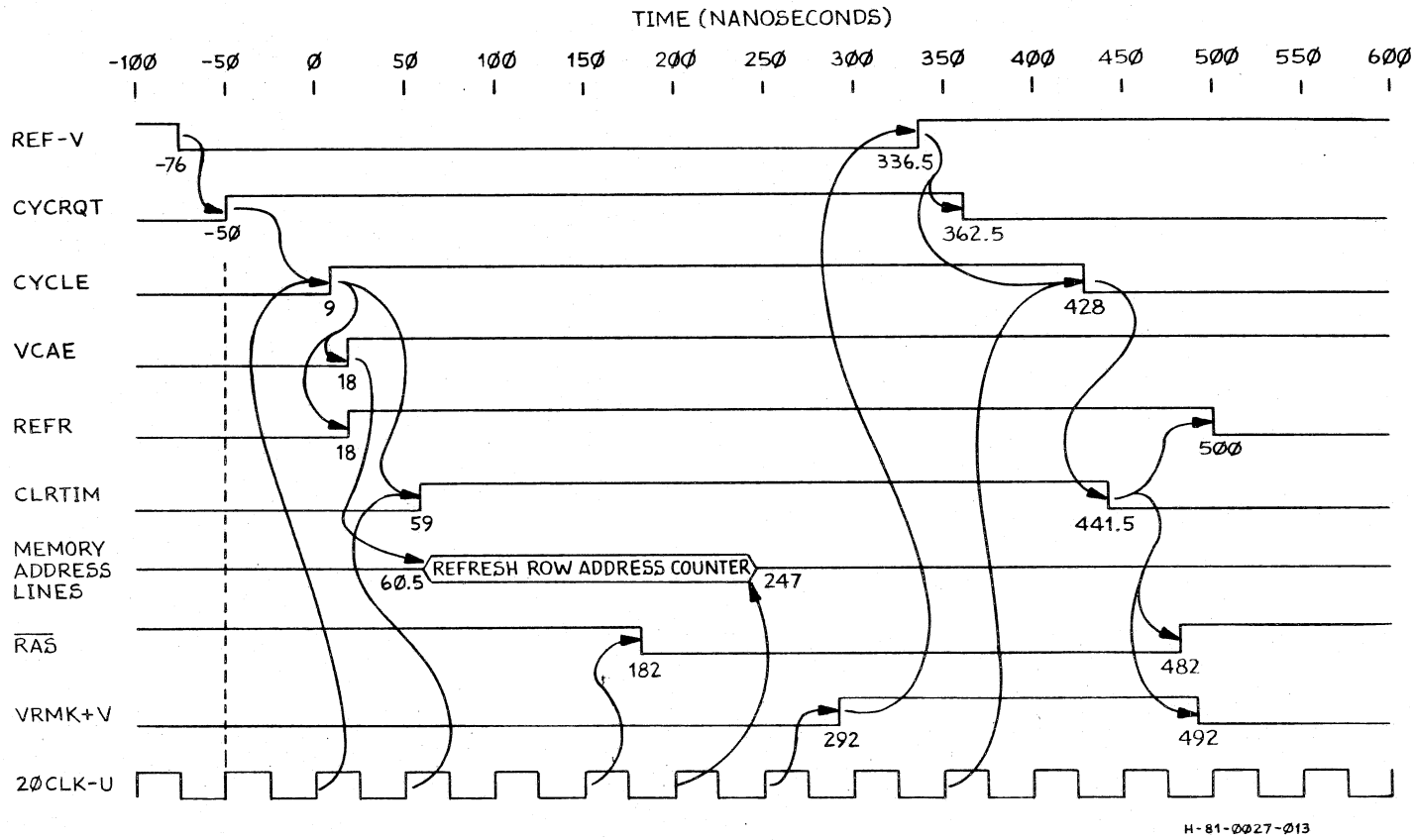


Figure 3-35. Refresh Cycle, Sequence of Events

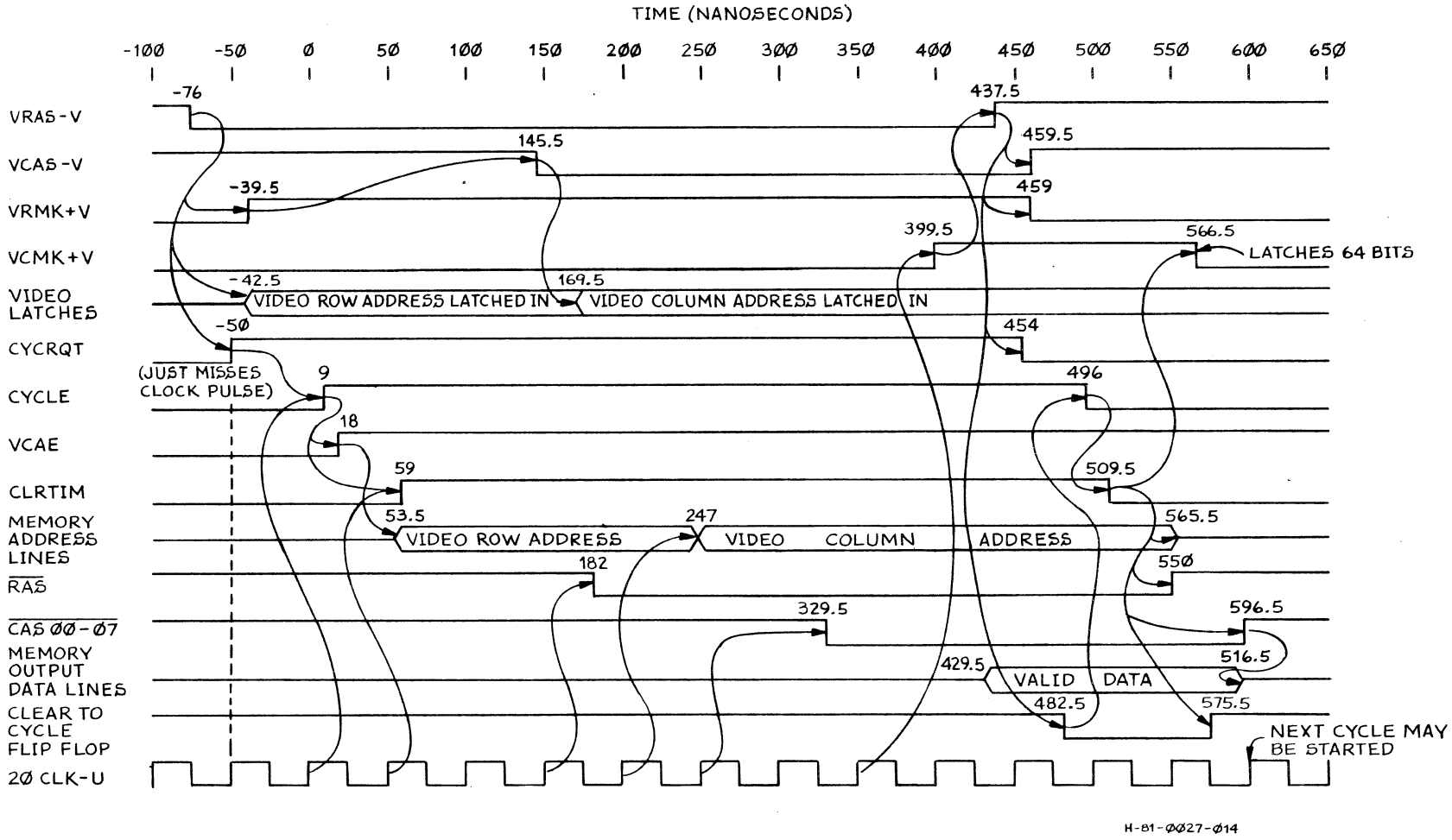


Figure 3-36. Video Read Cycle, Sequence of Events

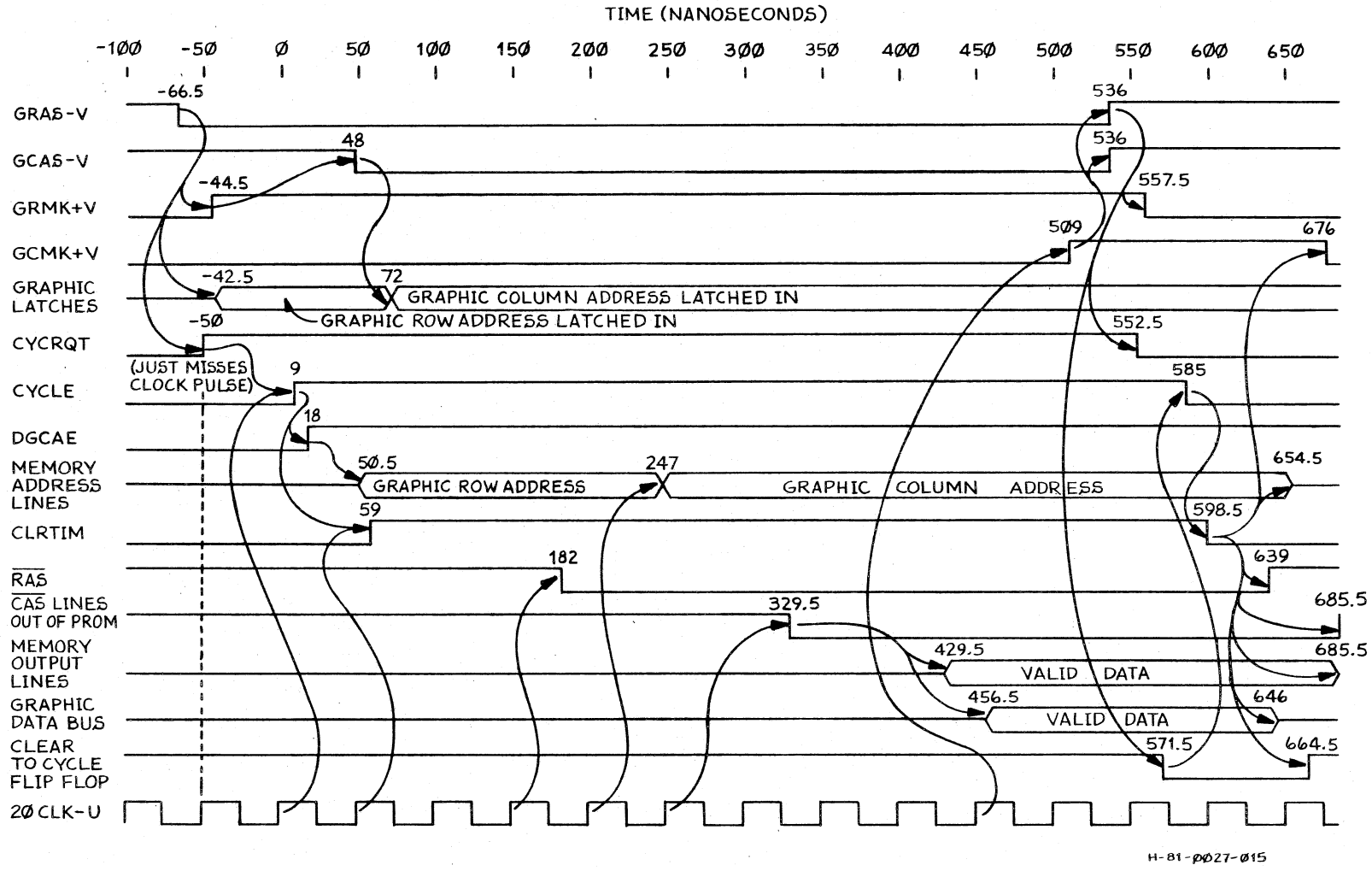


Figure 3-37. Graphic Controller Read Cycle, Sequence of Events

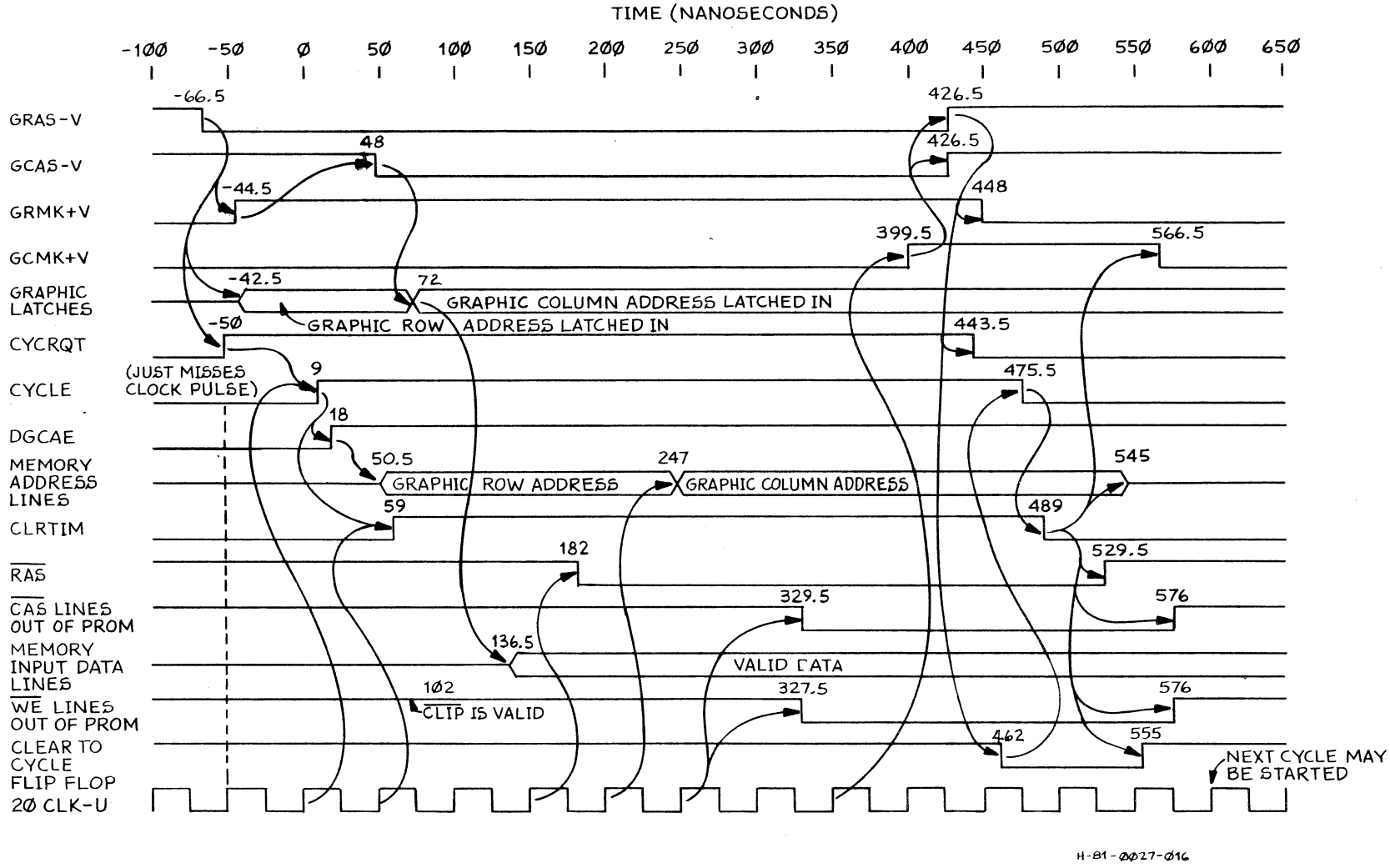


Figure 3-38. Graphic Controller Write Cycle, Sequence of Events

The graphic controller puts the column address on the address bus and sends GCAS. The mapping memory control logic loads the column address latch, then generates the RAS and CAS signals to strobe the address into the memory matrix. At the same time that it generates CAS, the control logic generates write enable ($\overline{WE}$) to enable memory write. The control logic sends GCMK back to the graphic controller to terminate the cycle. A typical graphic controller write cycle takes 500 nanoseconds.

3-11 VIDEO CONTROLLER

3.11.1 PHYSICAL DESCRIPTION. The video controller is an 8-layer printed circuit card, 7-3/4 by 12 inches. It is located in the region of slots XA8 through XA16 of a basic GRAPHIC 8 configuration.

The video controller connects to the backplane through a 98-pin connector (P1). On the front edge of the video controller are seven BNC connectors, J1 through J7. Their functions are as follows:

J1	External video in
J2	Composite video #1 out
J3	Composite video #2 out
J4	Composite video #3 out
J5	Composite video #4 out
J6	Composite video #5 out
J7	Composite video #6 out

3.11.2 APPLICATION. One video controller is required for each interactive display terminal. If the display terminal is monochrome, only one composite video signal goes from the video controller to the display. If the display is color, three composite video signals go from the video controller to the display.

As a special case (optional), the video controller can be configured to drive two display terminals. In such a case, all six composite video out signals could be used.

3.11.3 FUNCTIONAL DESCRIPTION. The video controller receives timing signals from the timing module. The video controller receives operational information and instructions from the digital graphic controller during the display vertical retrace time. The video controller retrieves data from the mapping memory card. The outputs of the video controller are the composite video signals that drive the display indicators. The video controller also supplies refresh timing signals to the mapping memory. Figure 3-39 shows the relationship of the video controller to the other elements of the GRAPHIC 8 system.

Commands from the graphic controller can cause the video controller to pan, scroll, selectively blink, selectively blank, or otherwise alter any or all of three non-contiguous sections of a 2048-by-2048 bit memory map.

A non-destructible full-screen crosshair cursor can be positioned to correlate with any point in the memory map. The cursor is hardware-generated. Its color or intensity contrasts with the background video.

The video controller can accept a synchronized external video input and mix that input with the graphic video in the composite video output.

3.11.4 BLOCK DIAGRAM DESCRIPTION. See figure 3-40. The video controller is reset to its initial condition by a VAEE-U (vertical access enable extension) signal from the timing module. This signal coincides with the display vertical retrace time. During this period the graphic controller can access the parameter RAM, the status register, and the video path look-up table.

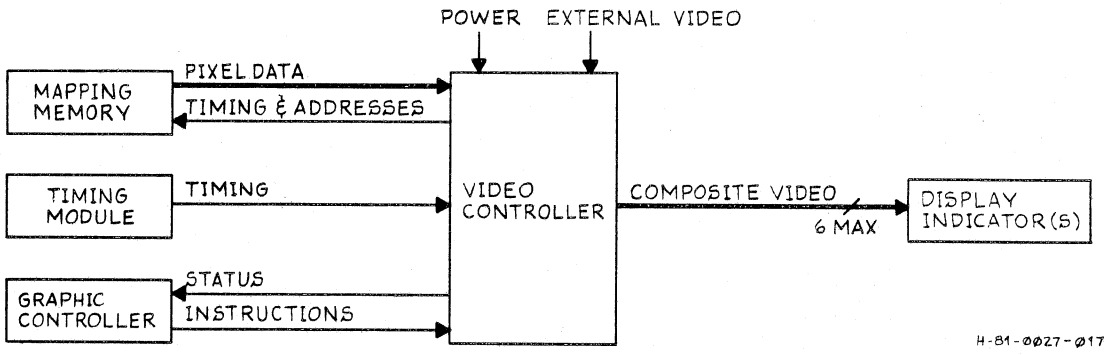


Figure 3-39. Relationship of Video Controller to Other Elements of the GRAPHIC 8 System

The parameter RAM contains information for three display presentations, cursor coordinates, and PHOTOPEN strike coordinates.*

The status register contains read/write control information for memory selection, memory operation, video blink enable, PHOTOPEN search, and a PHOTOPEN strike indicator bit. The PHOTOPEN search information forces a reference white at the display indicator.

The video path look-up table is a 256-by-8 bit RAM operating at transposed ECL (emitter-coupled logic) levels. It is read by the pixel data from the mapping memory. The output of the look-up table goes to the digital-to-analog converters as display data.

The sequence controller controls the hardware that presents a single horizontal scan of displayable data on the display indicator. The sequence controller operates at a clocking period of 150 nanoseconds (approximately 6.67 MHz), developed from the 20CK+U (20 MHz) signal from the timing module.

For each horizontal scan, the sequence controller performs the following major actions:

*Even though PHOTOPEN is not currently used in the GRAPHIC 8 system, the hardware has provisions for PHOTOPEN support.

@Transposed ECL logic 1 = +4.04V, logic 0 = +3.4V.

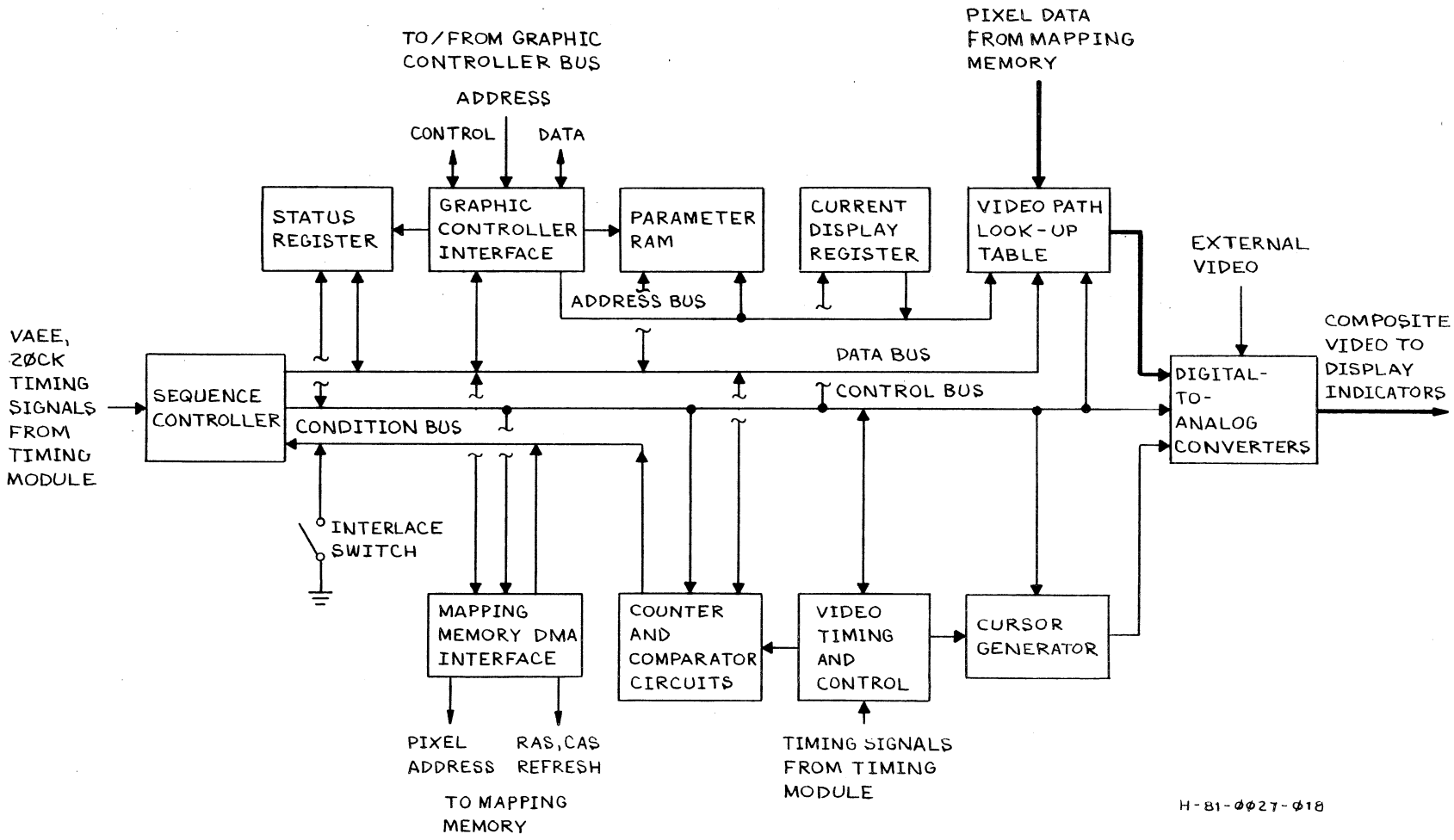


Figure 3-40. Video Controller Block Diagram

1. It interprets the parameter register contents for the initial scan of any displayed area of pixel memory.

2. It modifies the parameters for the next scan of any displayed area.

3. It fetches pixel data from the mapping memory and shifts the pixel data into the DAC holding register.

4. In case of a PHOTOPEN interrupt, it transfers the X and Y PHOTOPEN coordinates into the parameter RAM.

The sequence controller includes seven 32-by-8 bit ROMs that produce the data and control signals that initiate and implement these actions. The sequence controller increments the ROM addressses sequentially unless a branch condition forces a jump to a particular address.

The current display register determines which section of three split screens is being displayed. The current display register is controlled by the sequence controller. Its outputs include the two most significant bits for addressing the parameter RAM.

The mapping memory interface performs two principal functions:

1. It retrieves pixel data from the mapping memory to refresh the display (the retrieved pixel data goes to the look-up table).

2. It generates the REF- (refresh) signals to refresh the mapping memory.

Data retrieval from the mapping memory is a DMA (direct memory access) operation. The mapping memory interface includes two DMA controllers with their associated address registers, address counters, and word counter.

The video timing and control circuits perform the following functions:

1. They generate timing signals that clock various video controller operations.

2. They synchronize PHOTOPEN pulses to the video data rate and generate the PHOTOPEN interrupt.

The counter and comparator circuits make up a high speed data controller that operates at clock rates of up to 45 MHz. The data handled by these circuits is at ECL levels. The primary function of these circuits is to generate the real time addresses of pixel data in the video path. Other functions include accommodating PHOTOPEN strikes and loading the shift register in the mapping memory. Switch settings on the video controller card determine the length of the shift register: 8, 16, 32, or 64 bits.

The cursor generator generates a crosshair on the display that contrasts in color and intensity to the surrounding area of the display.

The interlace switch selects either interlaced or non-interlaced operation.

The DAC circuits select the data that is to be displayed and send the selected signals to the display indicator.

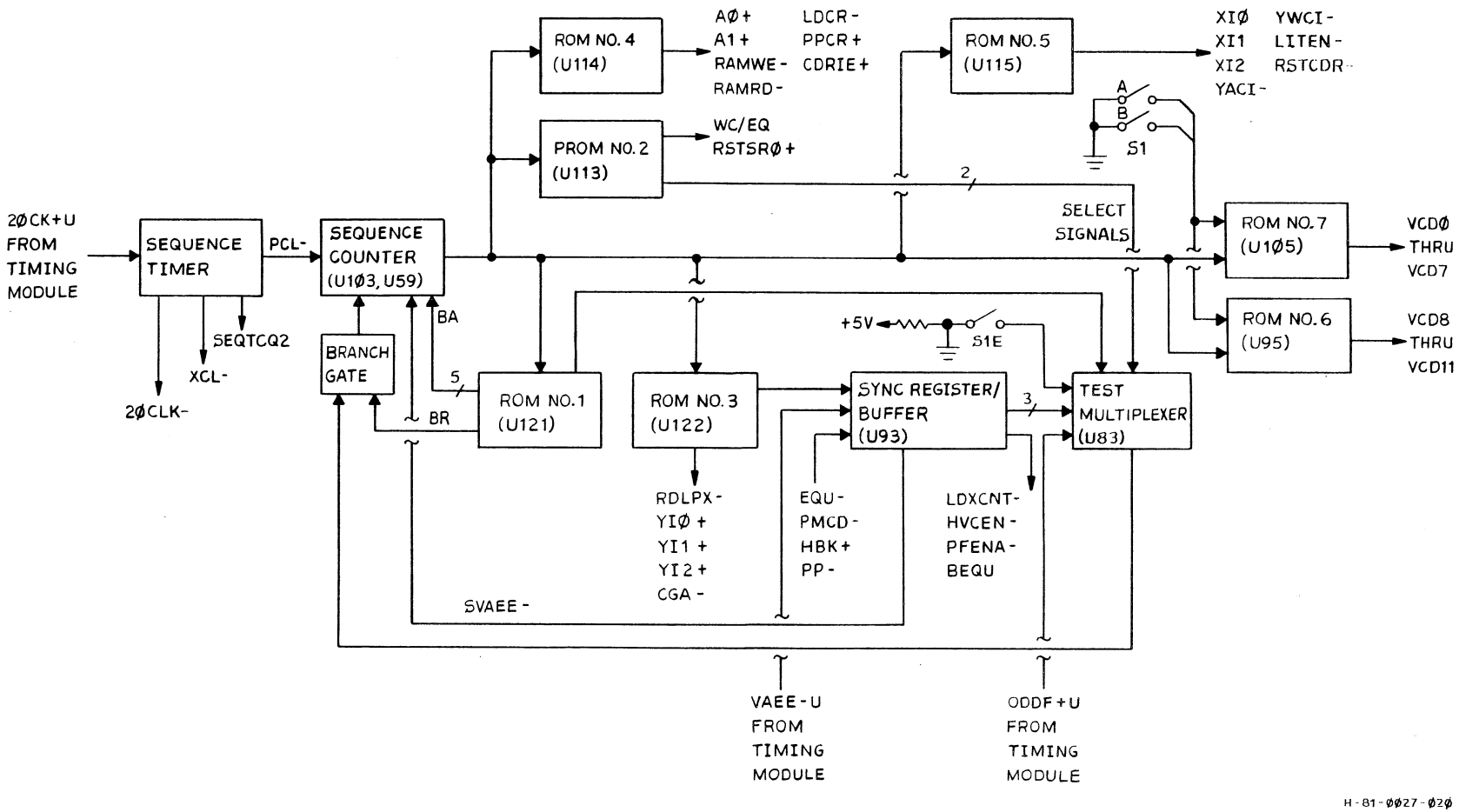


Figure 3-41. Sequence Controller Block Diagram

3.11.5 DETAILED OPERATION. The following paragraphs describe in more detail the makeup and operation of each of the blocks of figure 3-40.

3.11.5.1 Sequence Controller. The sequence controller consists of a sequence timer, sequence counter, sync register and buffer, test multiplexer, and seven 32-by-8 bit ROMs, as shown in figure 3-41.

The sequence timer is a module-3 counter, clocked by the 20 MHz 20CK+U signal from the timing module. Figure 3-42 shows its output waveforms.

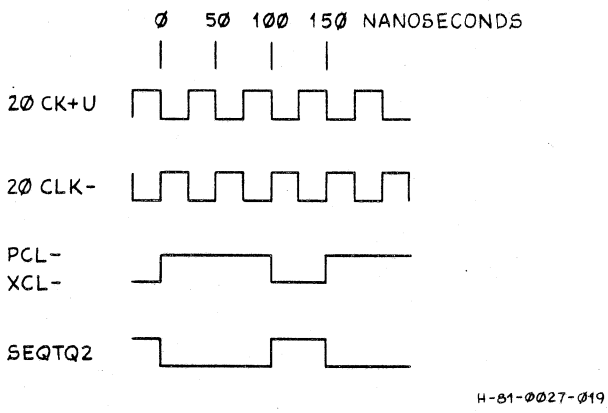


Figure 3-42. Sequence Timer Waveforms

The sequence counter resets to zero on receipt of the VAEE-U signal from the timing module, buffered to become SVAEE-. Thereafter the sequence counter advances one count on each PCL- pulse unless driven to a jump address.

ROMs #2, #3, and #4 are always enabled. ROM #2 produces four output signals:

1. WC/EQ (word count/equality) goes to the current display register circuit.

2. RSTSR0 (reset status register bit 0) goes to the status register circuit.

3. BCC0 and BCC1 are select signals that go to the test multiplexer. (Signal BCC2 goes from ROM #1, when enabled, to the test multiplexer.)

ROM #3 produces eight output signals:

1. PFEN- (pixel fetch enable) is buffered to become PFENA-, which has wide distribution. When PFEN- is high, ROM #5 is disabled.

2. LCXCNT- (load X count, buffered) goes to the counter and comparator circuit.

3. HVCEN- (high speed video circuits enable) goes to the counter and comparator circuit.

4. RDLPX- (read light pen X address) clocks status register bit zero.

5. YI0+, YI1+, and YI2+ (control Y DMA) go to the Y DMA controller in the mapping memory interface.

6. CGA- (cursor generator arm) goes to the cursor generator.

ROM #4 produces seven output signals:

1. A0+, A1+ go to a latch in the current display register circuit and are put on the address bus to drive the parameter RAM.

2. RAMRD- (RAM read) and RAMWE- (RAM write enable) go to the parameter RAM circuit.

3. LCDR- (load current display register) goes to the counter and comparator circuit.

4. PPCR+ (PHOTOPEN/cursor register) and CDRIE+ (current display register increment enable) go to the current display register circuit.

ROM #1 is disabled only when a PP- (PHOTOPEN) interrupt occurs. When enabled, ROM #1 supplies five BA (branch address) signals to the parallel inputs of the sequence counter. If the branch gate output goes low, the sequence counter loads the current branch address and counts from that value. When ROM #1 sets the BR signal high, it also enables the test multiplexer. Depending on the state of the selected multiplexer signal, the branch gate output may or may not go low. The signals selected by the test multiplexer are:

1. BEQU- (buffered EQU-) from the 12-bit comparator in the counter and comparator circuit.

2. INL+ (interlace), which reflects the setting of interlace switch S1E.

3. ODDF+U (odd field) from the timing module.

4. SFD- (buffered pixel memory control done, PMCD-) from the pixel memory control circuit in the mapping memory interface.

5. WC=1 (word count = 1) from the Y DMA controller in the mapping memory interface.

6. SHBK (buffered horizontal blank, HBK+), which is the inversion of HBLK-U (horizontal blank) from the timing module.

7. Ground

When a PHOTOPEN interrupt occurs, the outputs of RAM #1 are all forced high, forcing a program branch to the PHOTOPEN interrupt routine, address 31 of the sequence controller.

ROM #5 is enabled only when the PFEN- output of ROM #3 is high. When enabled, ROM #5 produces seven outputs:

1. XI0+, XI1+, XI2+ (control X DMA) go to the X DMA controller in the mapping memory interface.

2. YACI- (Y address count carry-in) and YWCI- (Y word count carry-in) go to the Y DMA controller in the mapping memory interface.

3. LITEN- (literal enable) enables ROMs #6 and #7.

4. RSTCDR- (reset current display register) resets the current display register.

ROMs #6 and #7, when enabled by LITEN- from ROM #5, generate a 12-bit literal number that can go to the parameter RAM, the status register, or the X and Y DMA controllers in the mapping memory interface.

3.11.5.2 Graphic Controller Interface. The graphic controller interface consists of data bus transceivers U9, U21; PLA (programmable logic array) U128; device select switch S3; and supporting logic elements as shown in figure 3-42A.

The graphic controller interface accepts control, address and data information from the graphic controller, generates control signals that affect the operation of the video controller, and passes data and response signals back to the graphic controller.

The data bus transceivers are enabled when their E terminals are low. They transmit data from the video controller card to the data bus when DR is high, accept data from the data bus when DR is low. DR is high when AG15+H is low and vice versa.

Address switch S3 is the video controller card selector, needed when the GRAPHIC 8 system contains more than one video controller card. The switch has eight sections, of which only one section is closed (see table 3-27). Bits AG00+H through AG07+H contain card select information. When one of these bits is high and matches the switch setting, a high card select signal passes to the PLA.

PLA U128 develops the following output signals:

1. RS- (read status) and WS- (write status) go to the status register.

2. WELUT- (write enable look-up table) goes to the look-up table.

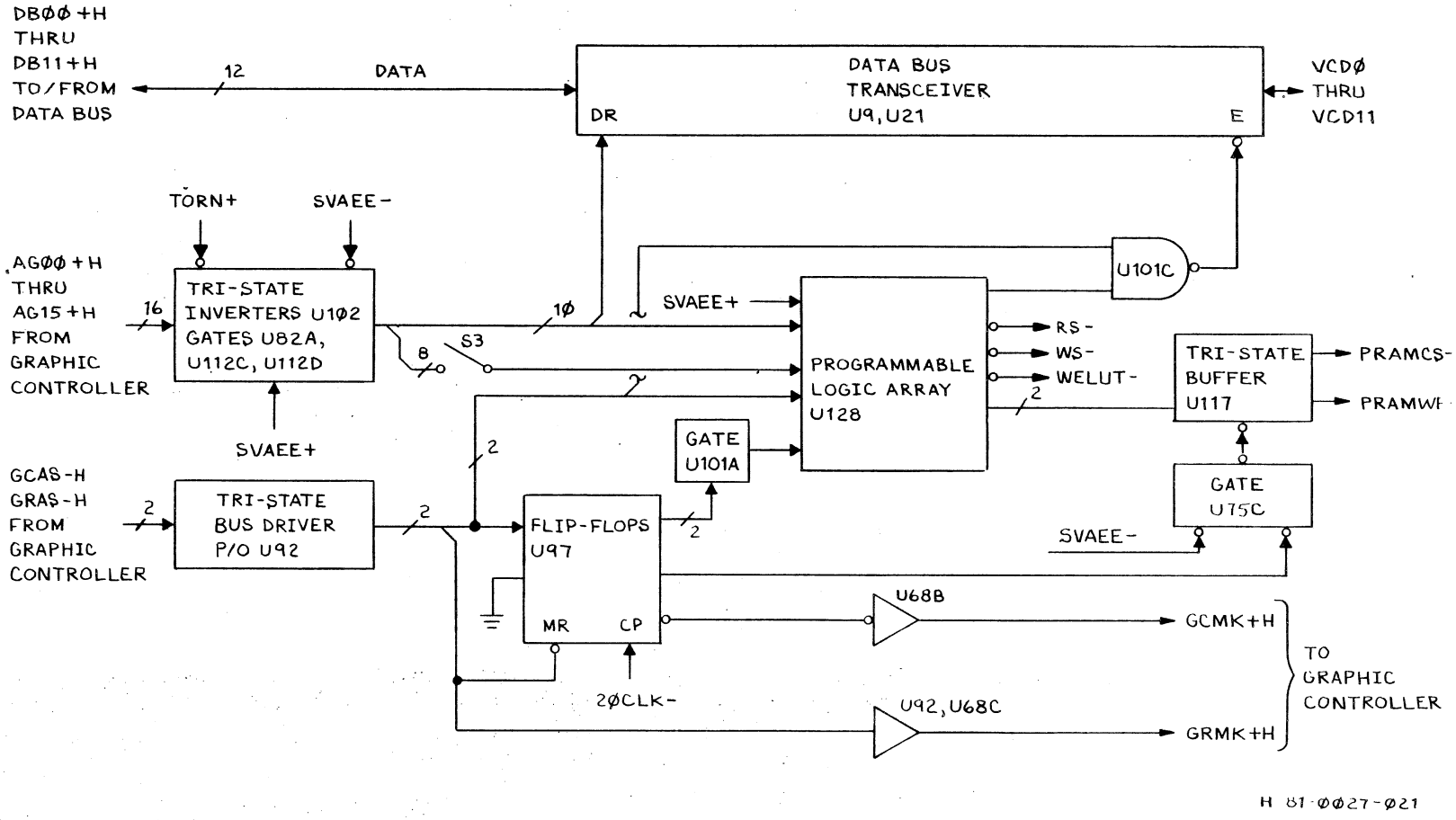


Figure 3-42A. Graphic Controller Interface, Block Diagram

3. PRAMCS- (parameter register chip select) and PRAMWE- (parameter register write enable) go to the parameter register.

Table 3-27. Video Controller Card Select

SWITCH SECTION	CARD	1	2	3	4	5	6	7	8	
A		C	0	0	0	0	0	0	0	
B		0	C	0	0	0	0	0	0	
C		0	0	C	0	0	0	0	0	
D		0	0	0	C	0	0	0	0	0 = open
E		0	0	0	0	C	0	0	0	C = closed
F		0	0	0	0	0	C	0	0	
G		0	0	0	0	0	0	C	0	
H		0	0	0	0	0	0	0	C	

Quad flip-flop U97 is a timing device. GRAS-H (row strobe) from the graphic controller clears the flip-flop. GCAS-H (column strobe) from the graphic controller is loaded into the first of three cascaded flip-flops in U97. Subsequent 20 MHz clock pulses cause GCAS-H to ripple through. After the first shift, gate U101A is enabled, passing a signal to the PLA. After the second shift, the video controller card sends GCMK+H (column acknowledge) back to the graphic controller. The video controller card sends GRMK+H (row acknowledge) back to the graphic controller immediately on receipt.

3.11.5.3 Parameter RAM. The parameter RAM circuit consists of a 16-by-12-bit memory (devices U96, U106, U116) and RAM control multiplexer U107. The parameter RAM stores parameter data (VCD0 through VCD11) at addresses specified by address bits A0 through A3. See figure 3-43.

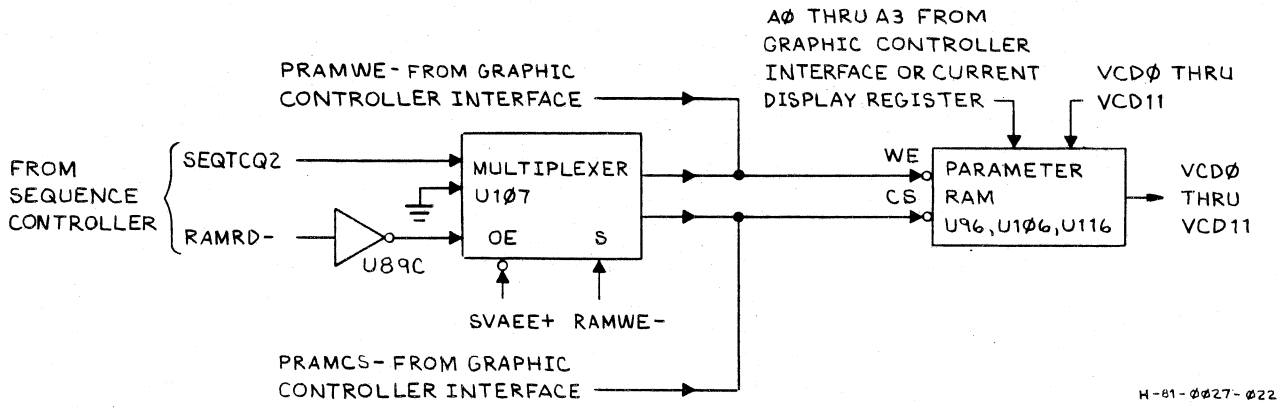


Figure 3-43. Parameter RAM, Block Diagram

The RAM control multiplexer accesses the parameter RAM for either reading or writing. A low SVAEE+ enables the multiplexer. A low RAMWE- signal selects the A inputs (SEQTCQ2), producing a low PRAMCS- (parameter RAM chip select) and low PRAMWE- (parameter RAM write enable). A high RAMWE- signal selects the B inputs (ground and RAMRD), producing a low PRAMCS- but a high PRAMWE-.

NOTE

PRAMCS- and PRAMWE- can also come from the graphic controller interface.

PRAM locations 0, 1, 2, 3, contain the parameters for display split 0; locations 4, 5, 6, 7 contain the parameters for display split 1; locations 8, 9, 10, 11 contain the parameters for display split 2; locations 12, 13 contain the X, Y cursor coordinates; and locations 14, 15 store the PHOTOPEN strike coordinates.

3.11.5.4 Status Register. The status register circuit consists of flip-flops U86, U124; bus driver U92; and LED DS3, as shown in figure 3-44.

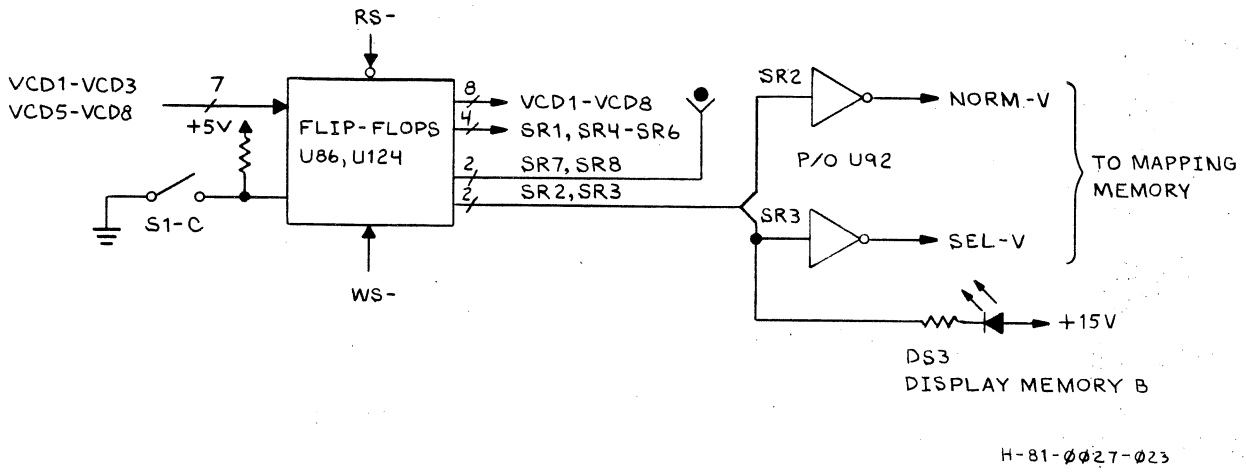


Figure 3-44. Status Register, Block Diagram

The flip-flops have two types of outputs. The VCD outputs are tri-state signals, because they go to a shared bus. The SR outputs are at TTL levels; they go on dedicated lines.

A low WS- (write status) signal clocks the input signal states into the flip-flops. Switch S1-C in conjunction with switches S2-G and S2-H controls the video blink circuit. When S1-C is open, blinking is enabled; when S1-C is closed, blinking is disabled.

A low RS- (read status) signal enables the flip-flop tri-state outputs. The SR outputs are always enabled. Outputs VCD0-VCD8 go on the VCD bus. The SR outputs are distributed as follows:

1. SR1 goes to the DAC circuits.

2. SR2 inverted becomes the NORM-V (normal) signal to the mapping memory.

3. SR3 inverted becomes the SEL-V (select) signal to the mapping memory; when SR3 goes low, the DISPLAY MEMORY B indicator lights on the video controller card.

4. SR4 goes to the video blink enable circuit, part of the look-up table function.

5. SR5 and SR6 go to the cursor generator circuit, part of the DAC function.

6. SR7 and SR8 are not used.

The functions of the video controller status bits are described in table 3-28.

Table 3-28. Video Controller Status Bits

BIT	DESCRIPTION
SR0	When set, indicates a PHOTOPEN strike has occurred. This bit is read only by the digital graphic controller.
SR1	The digital graphic controller can set this bit high to force a reference white. The digital graphic controller can read this bit.
SR2	The digital graphic controller writes this bit. When set low, status bit SR3 determines which mapping memories are accessible to the video controller and digital graphic controller. When high, all mapping memories are accessible to the video controller.
SR3	The digital graphic controller writes this bit. If SR2 is low, a low SR3 makes memory A accessible only to the digital graphic controller (for writing) while memory B is accessible only to the video controller for display refresh. Conversely, a low SR2 and high SR3 lets the digital graphic controller write to memory B while the video controller has access to memory A for display refresh.
SR4	The digital graphic controller writes this bit. When set high, allows the displayed video to blink at a 1.5 Hz rate.

Table 3-28. Video Controller Status Bits (Cont)

BIT	DESCRIPTION
SR5	The digital graphic controller writes this bit. When set high, allows the cursor to be displayed.
SR6	The digital graphic controller writes this bit. When set high, allows the cursor to blink at a 7.5 Hz rate.
SR7	Not used.
SR8	Not used.

3.11.5.5 Current Display Register. The current display register consists of synchronous 4-bit counter U46, latch U104, and supporting logic as shown in figure 3-45. The current display register output (address bits A2, A3) goes to the parameter RAM.

The current display register keeps track of which split screen segment is being displayed. The parameters for split 0 reside in PRAM locations 0-3; those for split 1 are in PRAM locations 4-7; and those for split 2 are in PRAM locations 8-11.

The current display register is initialized to 0 (split 0) at the beginning of each display field. The current display register is allowed to increment only when the number of lines for the current split is initially zero or has been reduced to zero.

Counter U46 is reset to zero by a low RSTCDR- (reset current display register) signal from the sequence controller. The counter loads a count of zero under either of the following conditions:

1. BEQU- low and WC/EQ low and CDRIE high and counter output QA low and counter output QB high.

2. WC/EQ high and WC=1 high and CDRIE high and counter output QA low and counter output QB high.

Both the CET and CEP inputs must be high for the counter to count. The CET signal is CDRIE, the CEP signal is the output of gate U62C. When enabled, the counter counts on PCL- clock pulses from the sequence controller.

The QA and QB outputs of the counter or the PPCR+ signal from the sequence controller go to latch U104 as address bits A2 and A3. Address bits A0 and A1 from the sequence controller also go to the latch. The latch transfers inputs to outputs on receipt of a latch clocking signal from the sequence controller; a low SVAEE+ is the output enable signal.

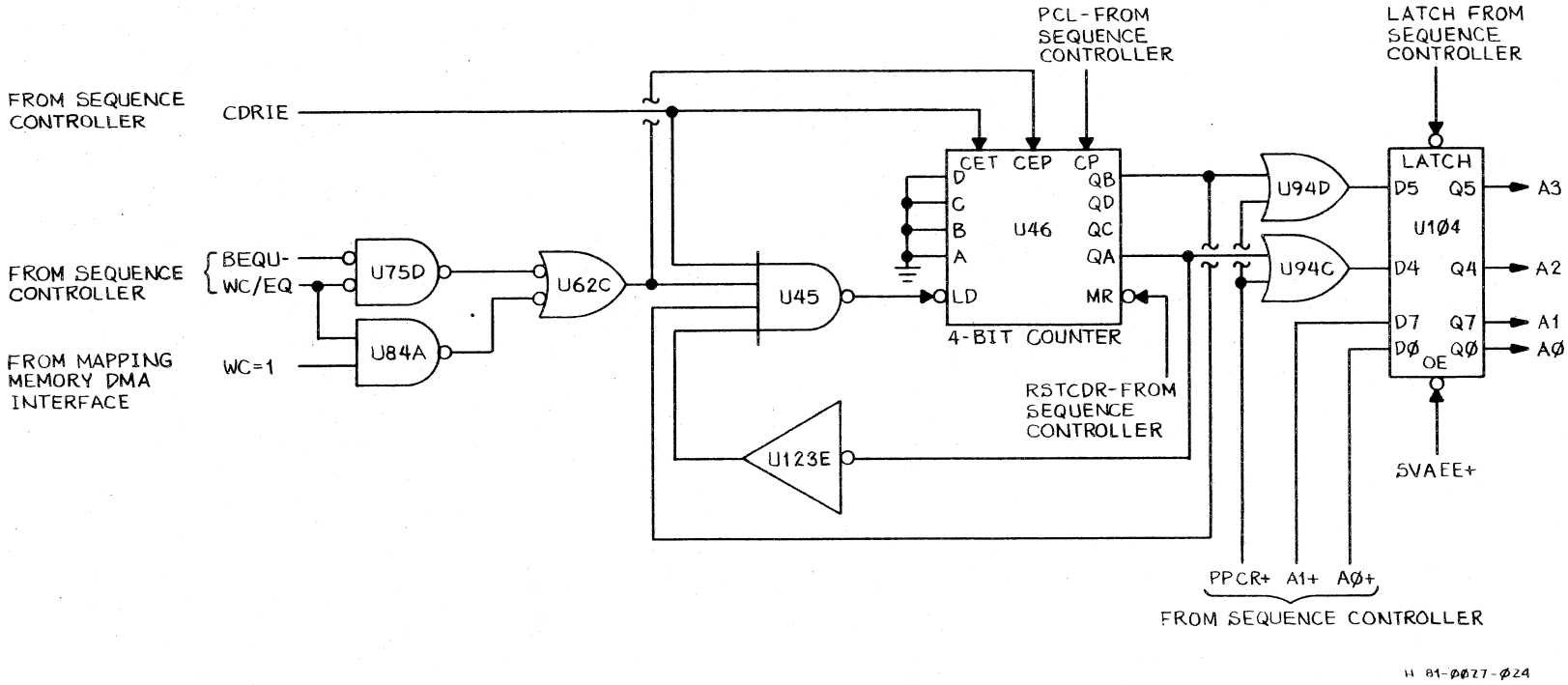


Figure 3-45. Current Display Register, Block Diagram

3.11.5.6 Mapping Memory Interface. The mapping memory interface consists of the six distinct but related circuits shown in figure 3-46. The mapping memory interface performs the following functions:

1. During horizontal retrace (screen blanked), the refresh control circuit ses the REF-V (refresh) control line to the mapping memory. This signal causes the mapping memory to refresh itself. The mapping memory sends back a VRMK+N (row acknowledge) signal after refreshing each row of cells. The refresh control circuit sets PMCD- (pixel memory control done) after the selected number of refresh cycles is completed. The number of refresh cycles per horizontal sweep is selectable from 0 to 7 by setting switches S1F, S1G, S1H; see table 3-29. LED DS2 lights while refresh is taking place; LED DS1 lights at the end of the refresh cycle. In practice, both LEDs should appear to be lit.

Table 3-29. Switch Settings for Number of Refresh Cycles per Horizontal Sweep

	0	1	2	3	4	5	6	7	
S1F	C	C	C	C	O	O	O	O	
S1G	C	C	O	O	C	C	O	O	C = closed
S1H	C	O	C	O	C	O	C	O	O = open

2. During the horizontal display time, the fetch control circuit sends VCASD-V (column address strobe), VRAS-V (row address strobe), and addresses to the mapping memory. The RAS-CAS sequence causes the mapping to load data into its 64-bit holding latch, where it is directly available to the video controller as a function of the PMSRLD and VCLK signals. When shifted out of the memory, the data goes through the video controller's mapping memory interface to the look-up table as signals PD0- through PD7- (pixel data bits). Bit DC07 is related to the blinking function. Switches S1C, S2G, and S2H enable or disable blinking as follows:

	ENABLE	DISABLE
S1C	open	closed
S2G	open	closed
S2H	closed	open

3. During the vertical retrace time, the digital graphic controller can write data into the look-up table. The DCxx signals from the mapping memory are open during this interval. The Ax signals from the digital graphic controller become the PDxx signals to the look-up table.

3.11.5.7 Video Path Look-Up Table. See figure 3-47. The video path look table is a 256-by-8 bit RAM operating at ECL levels (logic high = 4.1V, logic low = 3.4V). The device can be written into when WE (write enable) is low. When the BS (block select) line goes high, all the RAM outputs are read as zeros, forcing the display screen to go to black.

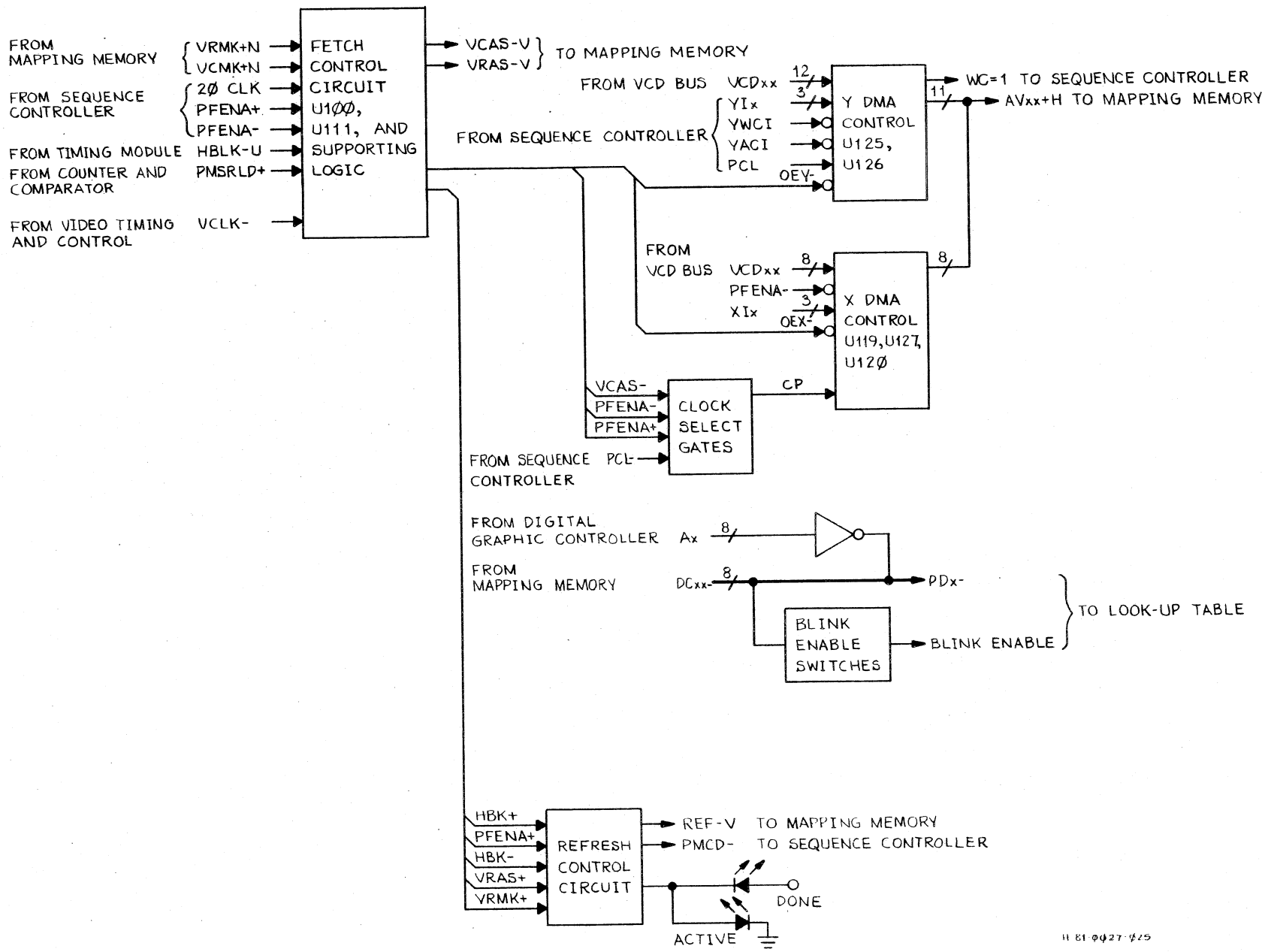


Figure 3-46. Mapping Memory Interfaced, Block Diagram

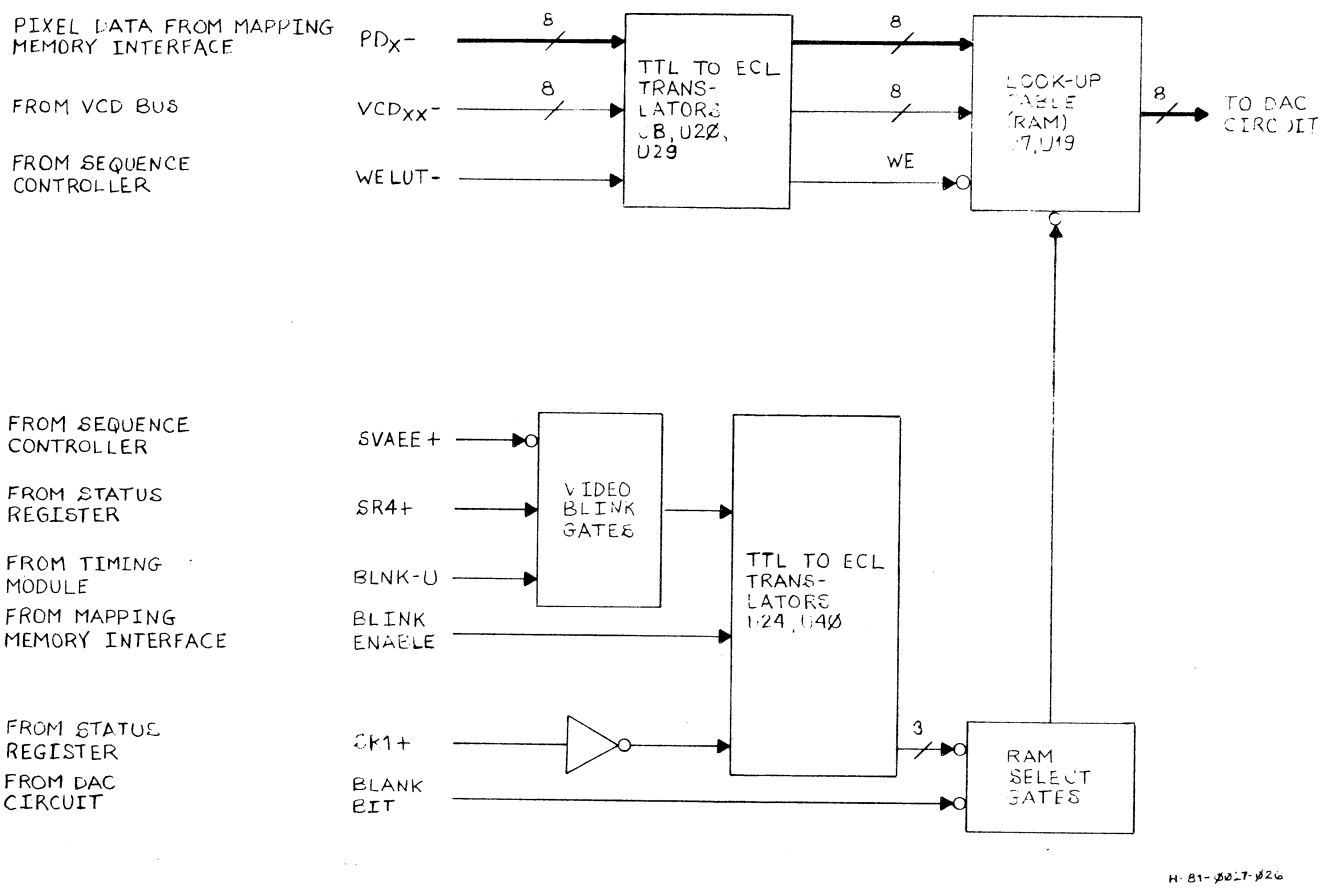


Figure 3-47. Video Path Look-Up Table, Block Diagram

During the vertical retrace period, the digital graphic controller can write data into the look-up table. The address information from the digital graphic controller appears on the PDx lines. The data from the digital graphic controller appears on the VCDxx lines, accompanied by a low WELUT- (write enable look-up table). At the same time, the high SVAEE+ (vertical access extended enable) makes the BS line low.

During the horizontal trace period, pixel data from the mapping memory interface appears on the PDX lines. These signals address the look-up table for read-out; the output data goes to the DAC circuit.

When blinking is invoked, the following conditions prevail:

1. SVAEE+ is low.

2. SR4+ from the status register is high.

3. The blink pixel bit from the mapping memory interface is low.

4. The BLNK-U (blink) signal from the time module controls the state of the BS line, causing the output of the look-up table to alternate between its normal color/intensity value and black.

3.11.5.8 Video Timing and Control. The video timing and control circuit generates various timing and control signals. Figure 3-48 shows the inputs and outputs. Figure 3-49 is the timing diagram. Table 3-30 lists the functions of the output signals.

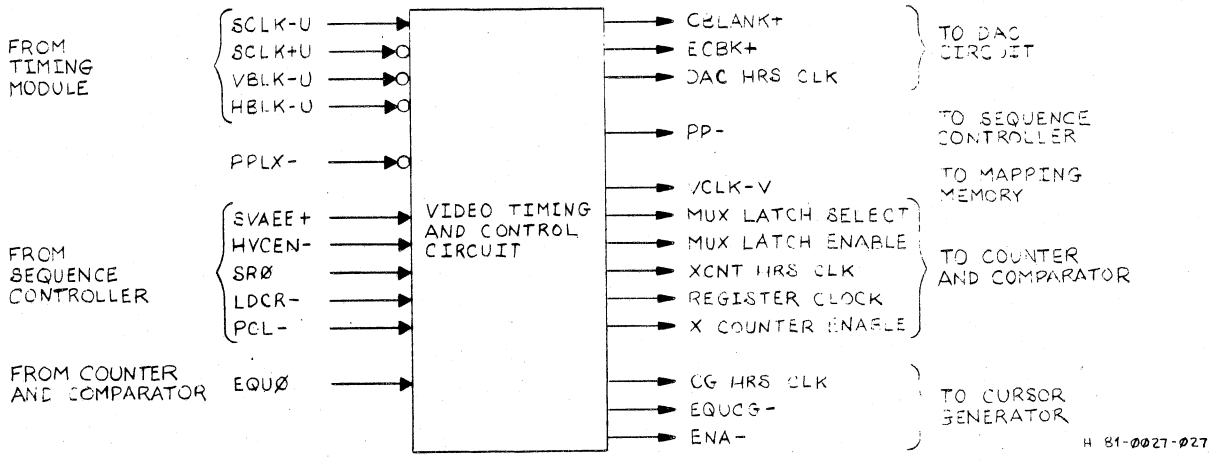


Figure 3-48. Video Timing and Control Circuit, Inputs and Outputs

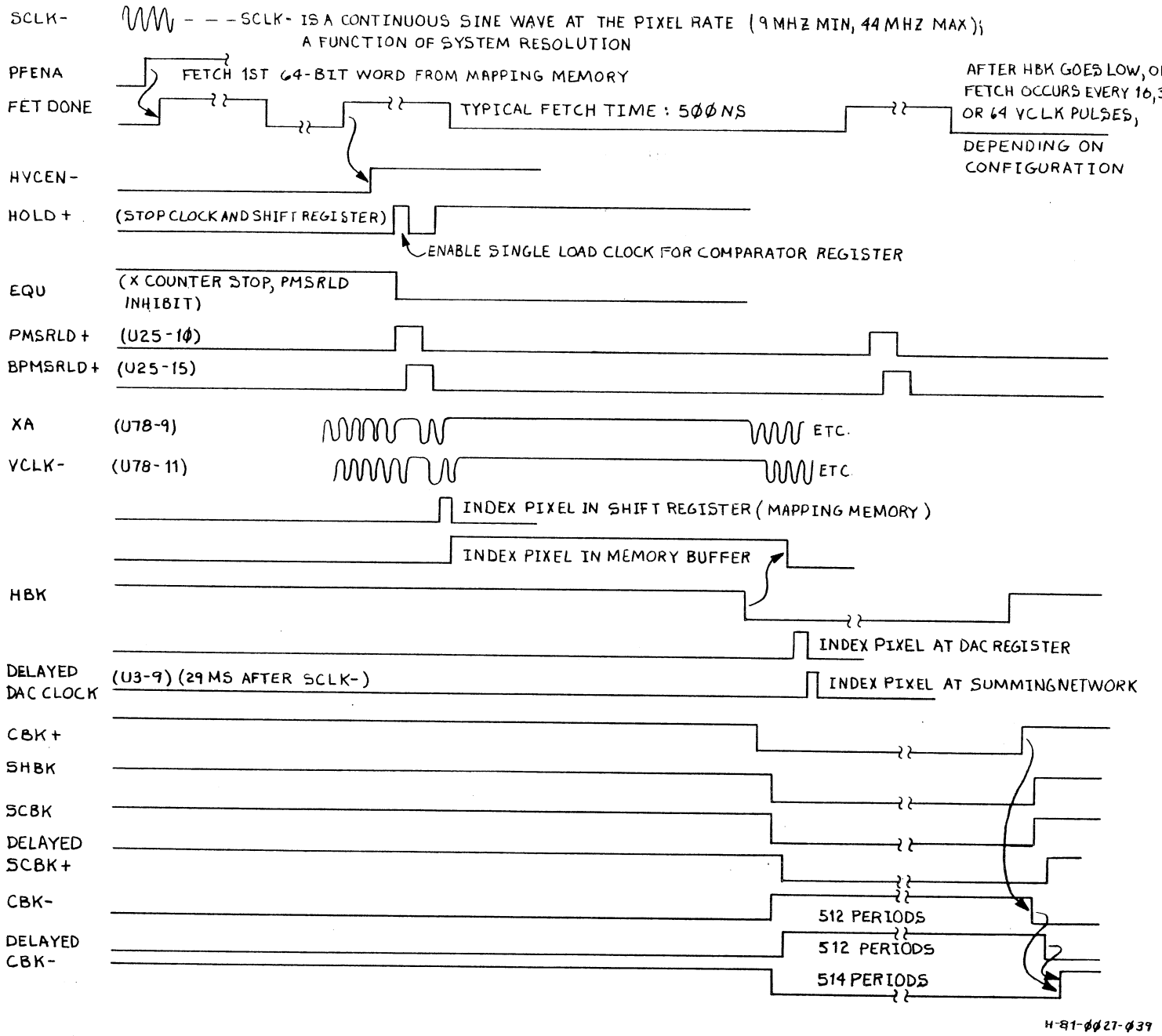


Figure 3-49. Video Timing and Control, Timing Diagram

Table 3-30. Video Timing and Control Output Signal Functions

SIGNAL	DESTINATION	FUNCTION
CBLANK+	DAC circuit	Enables output drivers to pass data to the display indicator(s). CBLANK = composite blanking
ECBK+	DAC circuit	Enables inputs to DAC register.
DAC HRS CLK	DAC circuit	Applied through delay line to clock DAC register.
PP-	Sequence controller	Becomes PPINT (PHOTOPEN interrupt)
VCLK-V	Mapping memory	Clocks 64-bit shift register and 8-bit output latch (mapping memory timing signal S16)
Mux latch select	Counter and comparator circuit	Selects input to multiplexer latch
Mux latch enable	Counter and comparator circuit	Enables output of multiplexer latch
XCNT HRS CLK	Counter and comparator circuit	Clock pulses for X counter
Register clock	Counter and comparator circuit	Clock pulses for comparator register
X counter enable	Counter and comparator circuit	Enables X counter
CG HRS CLK	Cursor generator	Clock pulses for vertical crosshair generator
EQUCG-	Cursor generator	Conditions vertical crosshair generator
ENA-	Cursor generator	Clears vertical crosshair generator

3.11.5.9 Counter and Comparator Circuit. The counter and comparator circuit consists of the elements shown in figure 3-50. The primary function of this circuit is to generate the real-time addresses of pixel data in the video path.

Circuit operation is generally as follows:

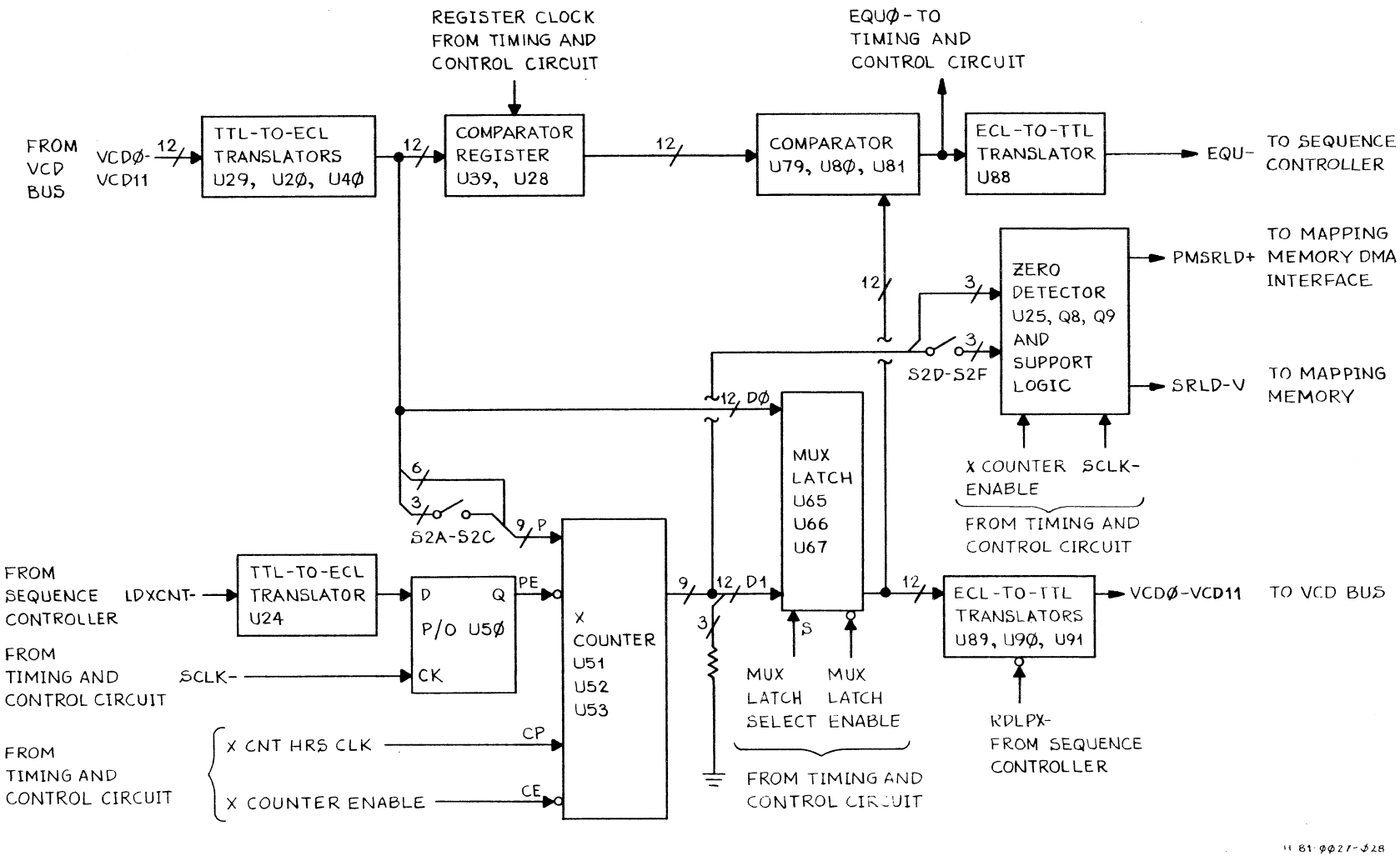


Figure 3-50. Counter and Comparator Circuit

1. At the start of a horizontal sweep, a LDXCNT- (load X counter) command causes the X counter to load a truncated address that corresponds to the starting address of a 64-bit string of pixel data in memory. The same value (not truncated) goes to the comparator register.

NOTE

The pixel string is not necessarily 64 bits long; switches S2A through S2C in this circuit plus other switches as defined in table 3-31 determine the length of the pixel string.

2. The X counter is then enabled and clocked at a rate of up to 44 MHz until the X counter output matches the comparator output (the mux latch is normally transparent).

3. When the comparison is exact, the comparator develops the EQUO- and EQU- (equality) signals. The X counter stops. The X cursor coordinate is loaded into the comparator. The X counter is incremented as necessary (two or three times) until the first pixel to be displayed is indexed at the input of the look-up table. The X counter then waits for horizontal unblanking to occur, then resumes counting.

Any EQU- signal generated after the X cursor data is loaded in the comparator causes the position of the vertical cursor crosshair to be displayed. Any X counter output that has a total of zero in the least significant three to six bits causes generation of PMSRLD (pixel memory shift register load). PMSRLD goes to the mapping memory as SRLD to load the 64-bit shift register, and is also used at the mapping memory interface to initiate a data fetch.

In the case of a PHOTOPEN strike, the mux latch is made not transparent; it holds the X coordinate of the PHOTOPEN strike. A subsequent RDLPX- (read light pen X coordinate) command enables the stored data to be put on the VCD bus, stored in the parameter RAM, and subsequently read by the digital graphic controller. A status bit is set in the status register to indicate the presence of PHOTOPEN data.

The status bit is cleared immediately following the vertical retrace period, whether or not the digital graphic controller has read the PHOTOPEN data.

Table 3-31. Pixel Memory Shift Register Length

SWITCH NO.	8 BITS	16 BITS	32 BITS	64 BITS	
S2A	C	C	O	O	
S2B	C	C	C	O	
S2C	C	O	O	O	
S2D	O	O	C	C	C = closed
S2E	O	O	O	C	O = open
S2F	O	C	C	C	
S1A	C	O	C	O	
S1B	C	C	O	O	

3.11.5.10 Cursor Generator. The cursor generator circuit consists of two flip-flops (U4A, U4B) and supporting logic as shown in figure 3-51. This circuit generates a crosshair on the display that contrasts in color and intensity to the surrounding area of the display.

Circuit operation is generally as follows:

1. A high ENA- at the start of each horizontal retrace period clears the vertical crosshair generator. When status bits SR5+ and SR6+ are both high, a low CCLK-U (cursor clock) from the timing module clears both the horizontal and vertical crosshair generators.

2. The vertical crosshair appears once per horizontal sweep, always at the same place with respect to the start of the sweep. The CG HRS CLK signals clock the state of EQUCG- into flip-flop U4B. When EQUCG- goes low, CV+ appears as a high pulse once per horizontal sweep to represent the vertical crosshair.

3. When CGA- (cursor generator arm) is low, PCL- signals from the sequence controller clock the state of EQU- into flip-flop U4A. When EQU- goes low, CV+ appears as a high for one whole sweep that represents the horizontal crosshair.

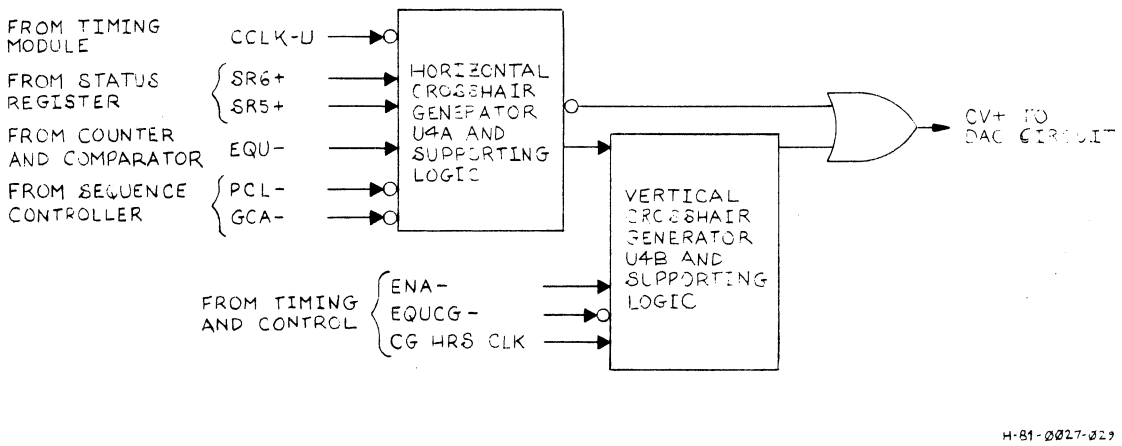


Figure 3-51. Cursor Generator Block Diagram

3.11.5.11 DAC Circuits. The DAC (digital-to-analog converter) circuits consist of the elements shown in figure 3-52. The DAC circuits perform the following functions:

1. They select the data that is to be displayed, from among the following sources: the outputs of the video path look-up table, the outputs of the cursor generator, a reference white condition (during PHOTOPEN search), or external video.

2. They send the selected signals to the display indicator at the proper amplitude to set the color and intensity values in the display indicator.

Operation is generally as follows:

1. For pixel data, cursor data, or reference white to be displayed, the signal ECBK+ (composite blank) must be low. When ECBK+ is low, the outputs from the video path look-up table are gated into the DAC register, clocked out of the DAC register by DAC HRS CLK, and passed to the resistor networks. Cursor data, when present, is exclusive-OR gated with the look-up table data to provide the necessary contrast. Status bit SR1+, when set, forces the reference white. The output of the reference black detector enables the video mixers, so during this interval external video can be displayed. External video, when present, appears at output connectors J3, J5 and J7.

2. When ECBK+ goes high, the data/cursor select logic and select gates are disabled, producing a reference black. The DAC resistor network combines reference black with CBLANK+ to produce the proper blanking at the display indicator. Shortly after reference black and CBLANK+ are combined, the CSYNC+ signal is added to the network. This signal produces a sharp negative pulse on the composite video lines that synchronizes the display indicators (horizontal retrace).

3.11.5.12 OPERATING SEQUENCE. Figure 3-53 is a flow diagram of video controller operations.

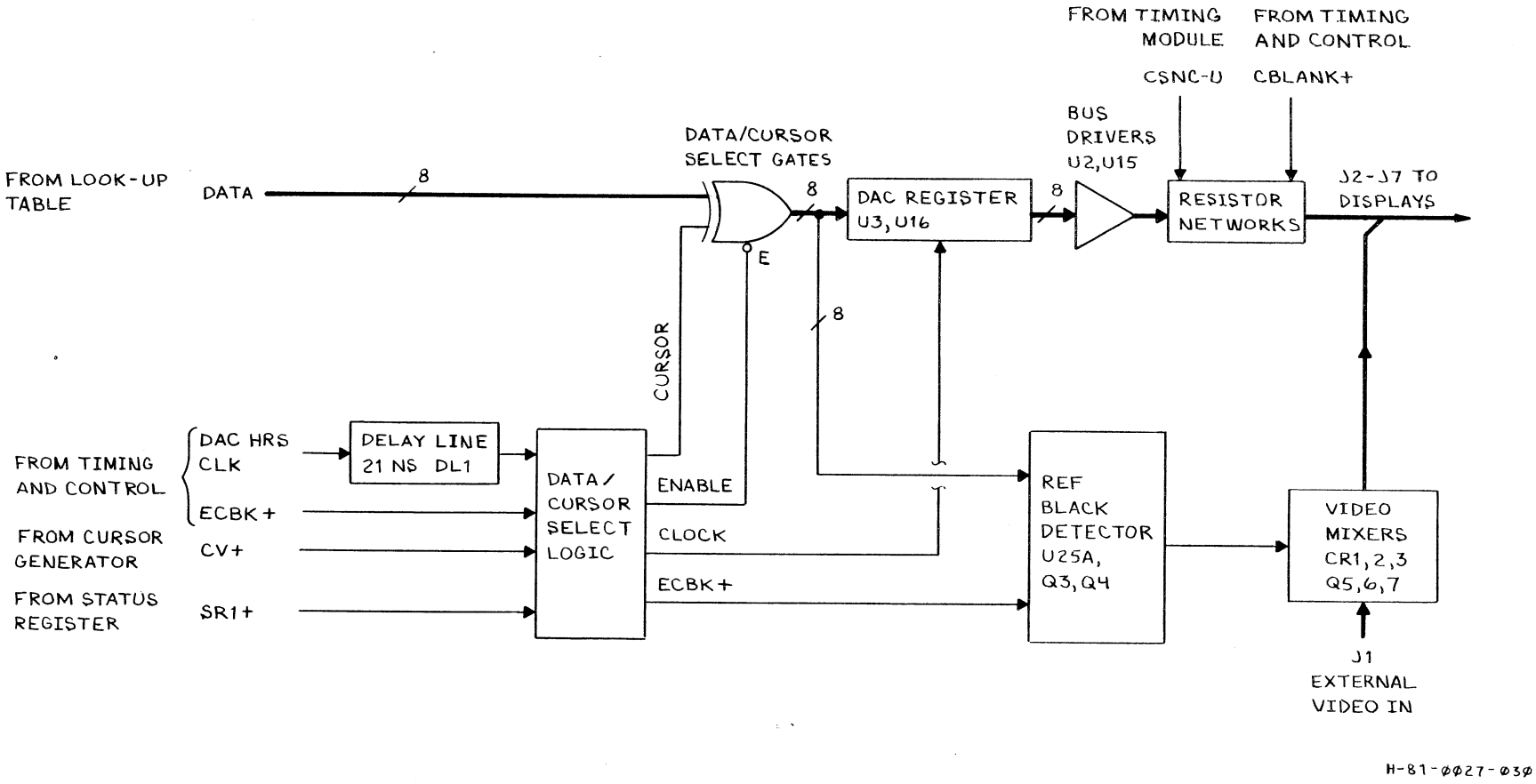


Figure 3-52. DAC Circuits, Block Diagram

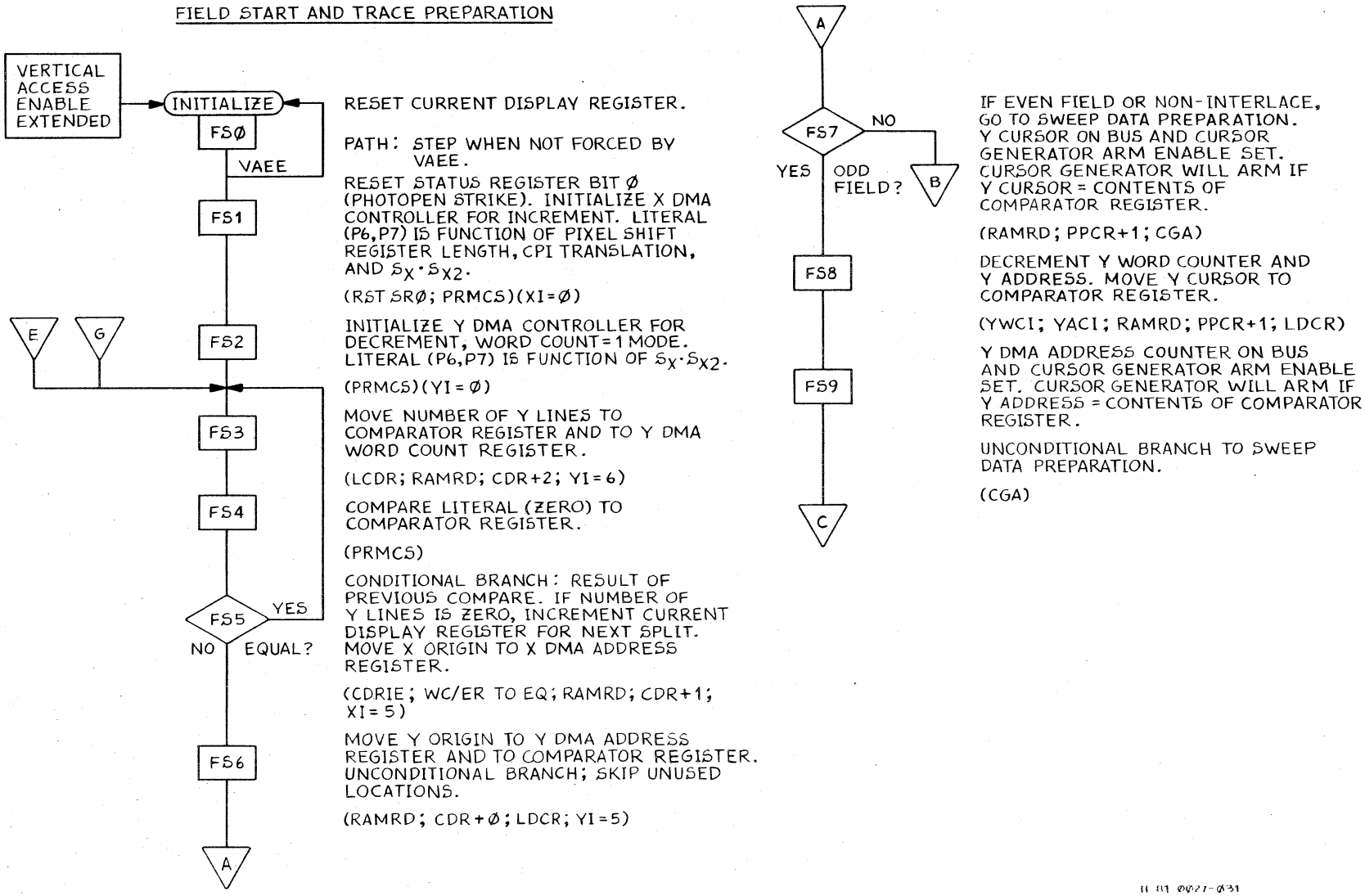


Figure 3-53. Video Controller Flow Diagram (Sheet 1)

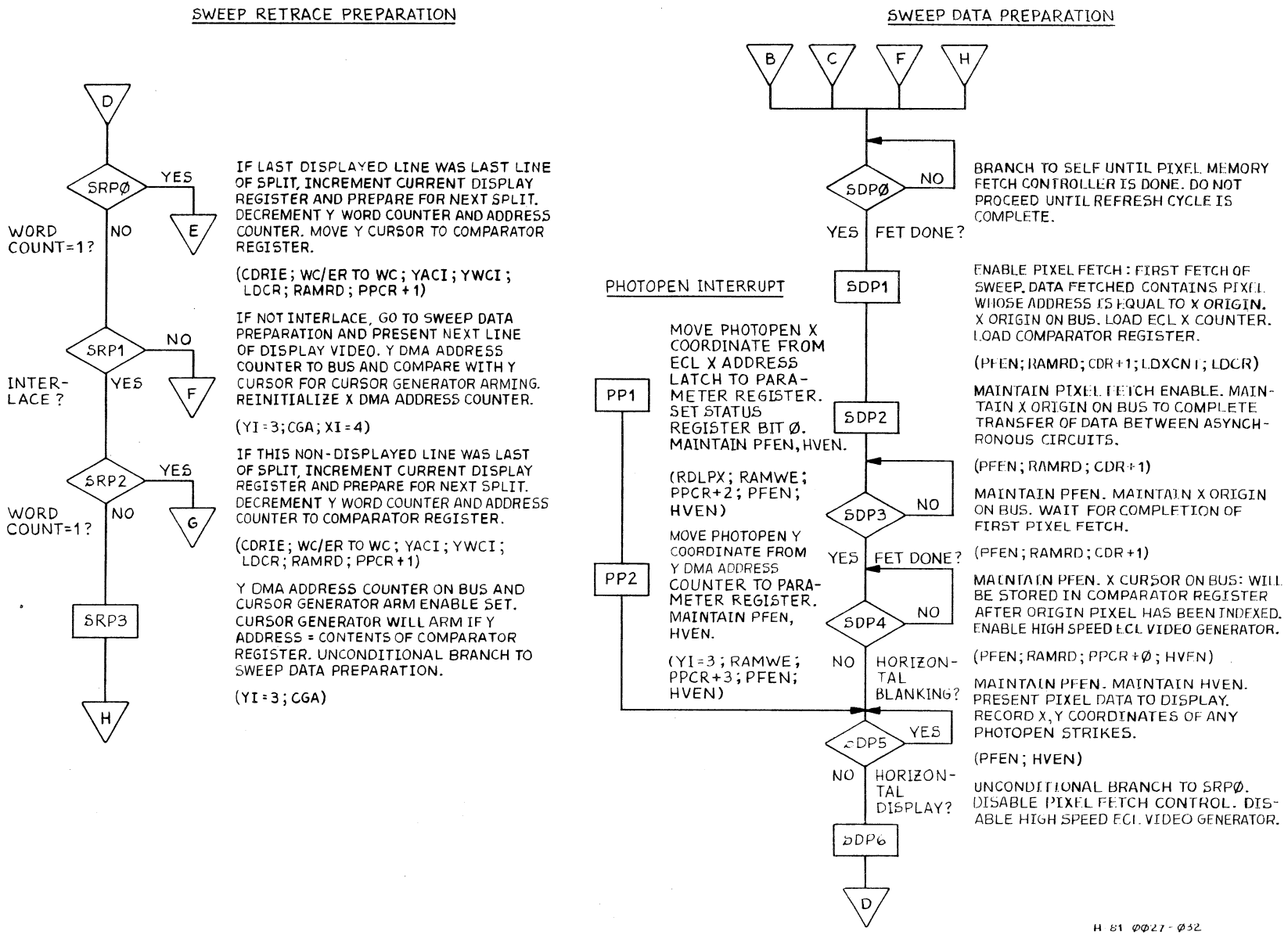


Figure 3-53. Video Controller Flow Diagram (Sheet 2)

3.12 TIMING MODULE

3.12.1 PHYSICAL DESCRIPTION. The timing module is a 4-layer printed circuit card, 7-3/4 by 12 inches, located in slot A17 of the terminal controller.

The timing module connects to the backplane through 98-pin edge connector P1. On the front edge of the timing module are seven BNC connectors, as follows:

J1	VIDEO 2 IN
J2	VIDEO 2 OUT
J3	VIDEO 1 IN
J4	VIDEO 1 OUT
J5	CSYNC
J6	HSYNC
J7	VSYNC

Five DIP switches on the timing module control system resolution, configuration, synchronization, and the type of BNC outputs. Table 3-32 describes the switch settings.

Table 3-32. Configuration Switch Settings

	U6	U10	U12	U30	U37
S1	SYSTEM TYPE				
S2	BITS/PIXEL	X-Y RESOLUTION	SYNC POLARITY	PLL REF	
S3					
S4	MEMORY		NOT USED	BNC OUTPUT SELECT	CLOCK RESOLUTION
S5	FIELD	BANK SELECT	SCREEN RESOLUTION		
S6	SIZE				
S7	NO. OF VIDEO	ODD FIELD ENA	PIXEL PLANES PER MEMORY	NOT USED	INTERLACE SELECT
S8	CONTROLLERS	NOT USED			

3.12.2 APPLICATION. See figure 3-54. The timing module generates the timing signals that control the presentation of the image on the monitor. The timing module is configurable (by switches and adjustments) to meet the non-interlace timing requiremnts of EIA RS-343A at resolutions of 512 x 512 and 640 x 480.

The timing module also generates system functions such as bus synchronization and line rate clocks, and a power-up initialization signal.

The timing module also contains the system status register and two auxiliary video amplifiers.

3.12.2.1 Monitor Timing. All timing functions relating to monitor operation are generated by a single closed-loop frequency divider chain with appropriate feedback. Timing signals include:

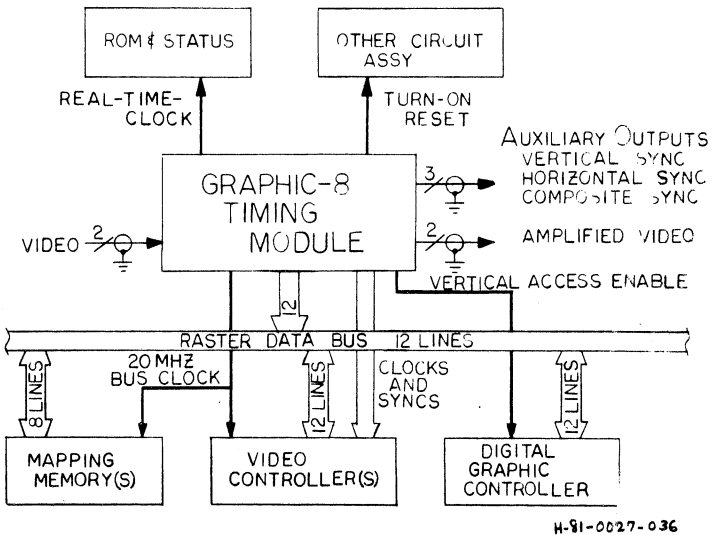


Figure 3-54. Timing Module Functional Application

Horizontal blanking	HBK
Serration	SER
Vertical blanking	VBK
Pixel clock	SCLK
Composite sync	CSNC
Cursor blink clock	CCLK
Video blink clock	BLNK

3.12.2.2 System Functions. The timing module generates the following system timing signals:

20 MHz bus clock	20CK-U
Power turn-on reset	TORN-U
Real time clock	RTCK-U
Vertical access enable	VAEN-U

The timing module generates the following signals used only by the video controller:

Vertical access extended enable	VAEE-U
Odd field signal	ODDF-U

The system status register on the timing module consists of 12 dual in-line switches and tri-state bus drivers. The bus driver outputs appear on the raster data bus during the first complete vertical sweep (16-20 us) after power turn-on. The bits on the raster data bus are identified as follows:

Raster data bus bits	DB00 through DB11

The signals at J5 (CSYNC), J6 (HSYNC), and J7 (VSYNC) are dc-isolated and have an output impedance of 75 ohms. Signal polarity is individually controlled by the switches on the timing module.

Other than operating power, the only input to the timing module is 6.3 Vac, used by the real time clock circuit. The timing module contains pull-up resistors for the raster bus control lines.

3.12.3 FUNCTIONAL DESCRIPTION

3.12.3.1 Input Power. All input voltages are filtered at the edge connector. The +5V lines are decoupled throughout the timing module, and the ±15V lines are filtered at their points of usage.

3.12.3.2 Real Time Clock. See figure 3-55. The real time clock is generated from the line frequency by a step-down transformer and a zero-crossing detector. The step-down transformer is located in the power supply.

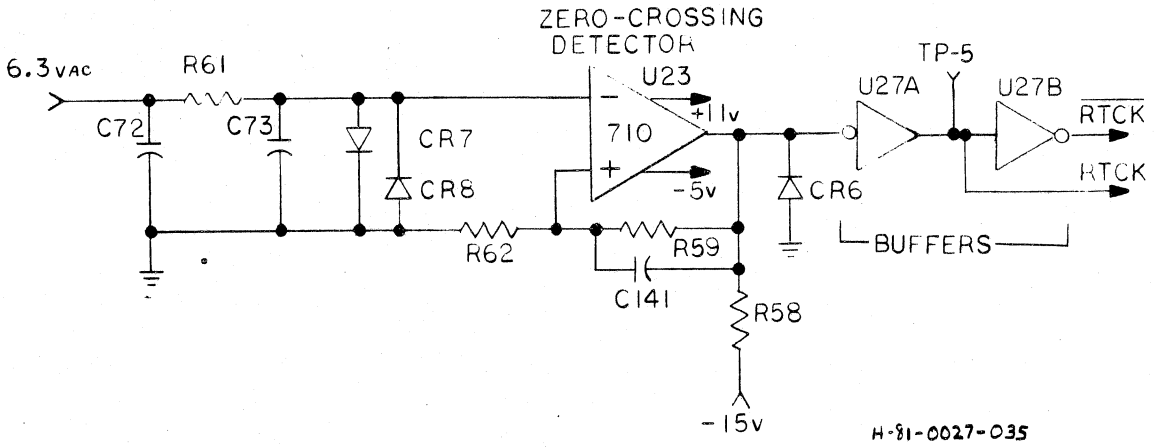


Figure 3-55. Real Time Clock Circuit

Zero-crossing detector U23 changes polarity (inversely) as the input signal passes through zero. C141 reduces ringing through this region. CR6 limits the output to positive excursions. Buffers U27A, U27B supply both phases of RTCK.

3.12.3.3 Turn-On Reset Generator. See figure 3-56. When power is applied to the terminal controller, single-shot U3 generates a 500 ms pulse TORN-U that is distributed throughout the system. The system can also be reset by an external reset signal (EXTR-).

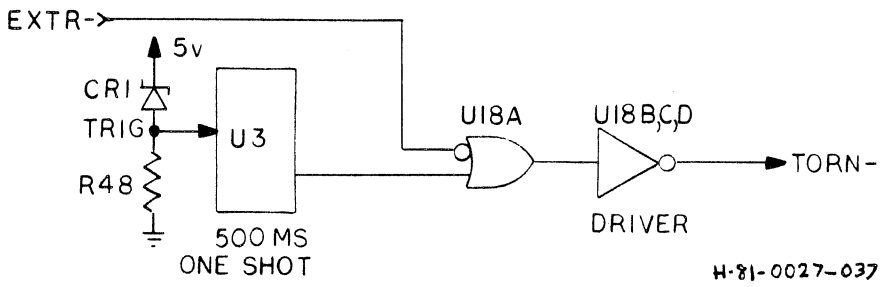


Figure 3-56. Turn-On Reset Generator

3.12.3.4 20 MHz Oscillator. See figure 3-57. Crystal-controlled oscillator U46 produces a 20 MHz TTL level square wave with a frequency tolerance of 0.01%.

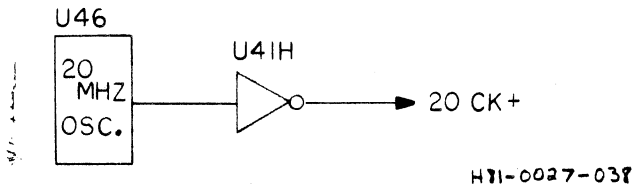


Figure 3-57. 20 MHz Oscillator

3.12.3.5 Auxiliary Video Amplifiers. The video amplifiers are variable gain differential amplifiers with emitter follower outputs. The gain of VIDEO #1 is set by R22; R16 sets VIDEO #2. The output of VIDEO #2 is also coupled to a sync separator through a level shifter to remove screen video. These amplifiers have gains in the range from 0.4 to 3.0; both drive 75-ohm loads. Figure 3-58 shows internal and external connections.

3.12.3.6 System Configuration Register. The system configuration register consists of a bank of switches selected by VAEN- and TORN-. The output of these switches goes to the system raster data bus and remains on the bus for two monitor refresh periods after initial system turn-on. Figure 3-59 shows the switch settings that can be held in the system configuration register. Figure 3-60 shows how the configuration switch information gets onto the data bus.

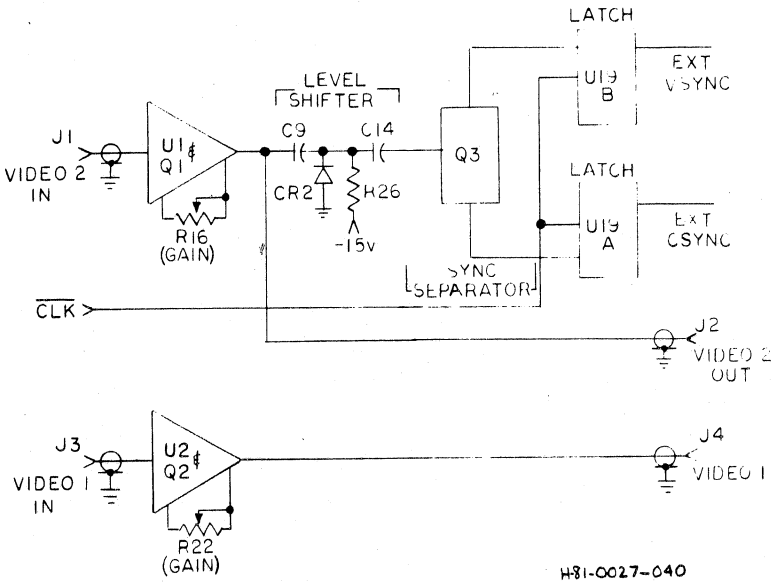


Figure 3-58. Video Amplifiers

8100 8200	0 1	SYSTEM TYPE
2 BITS 4 BITS 8 BITS	01 10 11	BITS PER PIXEL
2048X2048 1024X2048 2048X1024 1024X1024 512X1024 1024X 512 512X 512	001 010 011 100 101 110 111	MEMORY FIELD SIZE
1 2 3 4	00 01 10 11	NUMBER OF VIDEO CONTROLLERS
512X 512 640X 480 1024X 768 1024X1024	00 01 10 11	SCREEN RESOLUTION
1BIT/BD 2BIT/BD 4BIT/BD 8BIT/BD	00 01 10 11	PIXEL PLANES / MEMORY
DB11 — S8 — U12 DB10 — S7 — U12 DB09 — S6 — U12 DB08 — S5 — U12 DB07 — S8 — U6 DB06 — S7 — U6 DB05 — S6 — U6 DB04 — S5 — U6 DB03 — S4 — U6 DB02 — S3 — U6 DB01 — S2 — U6 DB00 — S1 — U6		SWITCH AND RASTER DATA BIT

H-81-0027-041

0 = SW CLOSED
1 = SW OPEN

Figure 3-59. Configuration Switch Settings

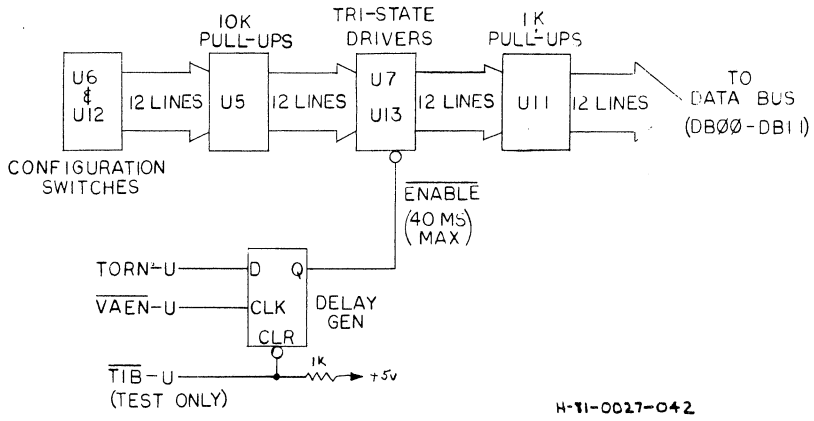


Figure 3-60. System Configuration Register

3.12.3.7 Ramp Generator. The ramp generator (U54, R45, C38) is an integrator with a transfer function $V_{OUT} = -1/RC \int V_{IN} dt$. R43 and R46 make up a variable gain configuration of operational amplifier U54. C35 and R43 filter all high frequency input functions.

3.12.3.8 Sample and Hold. U29 and C19 make up the sample and hold circuit. Ramp generator output is sampled by VSYNC and held by C19. This voltage goes to the VCO. Figure 3-61 shows the ramp generator and the sample and hold circuit.

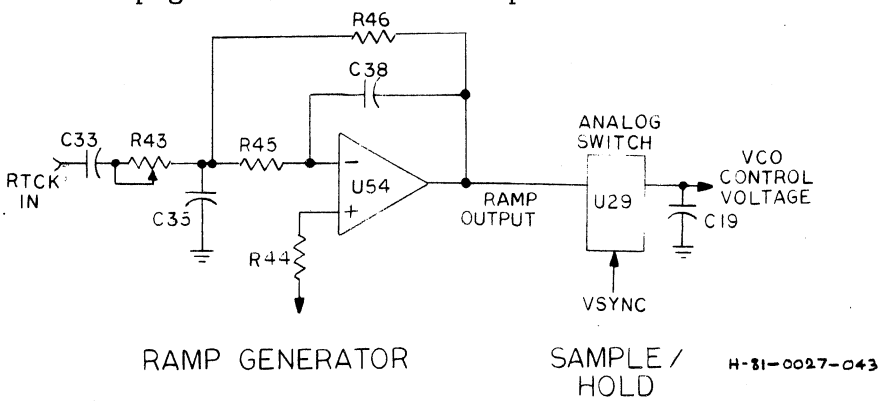


Figure 3-61. Ramp Generator and Sample and Hold Circuit

3.12.3.9 VCO. The voltage-controlled oscillator consists of Q7, C22, C23, C24, C25, L2, and Q4. The voltage on the gate of Q4 changes the output capacitance and the frequency of the circuit. The output is coupled through common base amplifier Q5, emitter follower Q6, and buffer U41H to the pixel clock prescaler.

3.12.3.10 Pixel Clock Prescaler. This circuit consists of DIP switch U37 and binary counter U36. Switch U37 selects the output frequency; see figure 3-62 and table 3-33. The selected frequency goes to the function count prescaler. U16 is an ECL driver that sends the selected frequency to other cards in the terminal controller as SCLK- and SCLK+.

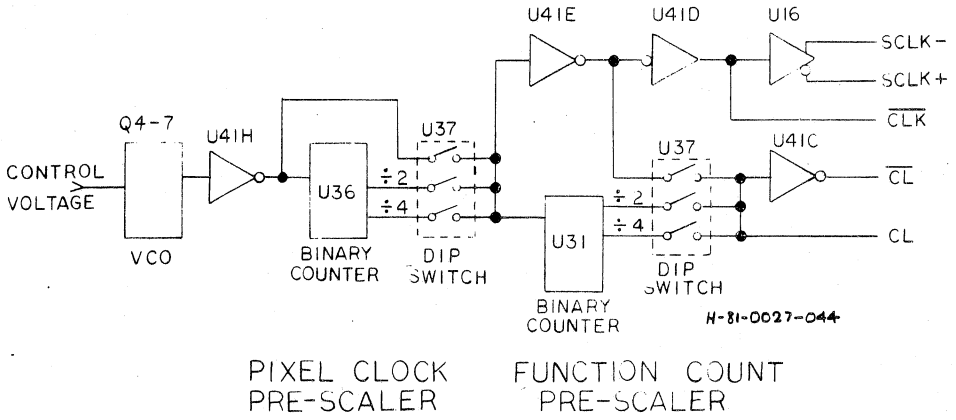


Figure 3-62. VCO, Pixel Clock Prescaler, and Function Count Prescaler

Table 3-33. Output Frquencies

LINE FREQ	RESOLUTION	PIXEL CLOCK PRESCALER FREQUENCY	FUNCTION COUNT PRESCALER FREQUENCY
60 Hz	512 x 512	22.38 MHz	11.19 MHz
60 Hz	640 x 480	25.67 MHz	6.42 MHz
50 Hz	512 x 512	18.65 MHz	9.35 MHz
50 Hz	640 x 480	21.39 MHz	5.35 MHz

3.12.3.11 Function Count Prescaler. This circuit consists of DIP switch U37 and binary counter U31. Switch U37 selects the output frequency; see figure 3-62 and table 3-33. The selected frequency goes to other cards in the terminal controller as CL and $\overline{CL}$.

3.12.3.12 Raster Syncs and Blanks. Raster syncs and blanks are produced by binary counters and digital comparators whose outputs set or reset the function registers. See figure 3-63. The outputs from these registers are:

H BLANK	$\overline{VBLK}$
HSYNC	VSYNC
$\overline{HSYNC}$	$\overline{VAEN}$
HBLK	VAEEP
SERRATION	VDRIVE
	$\overline{VDRIVE}$

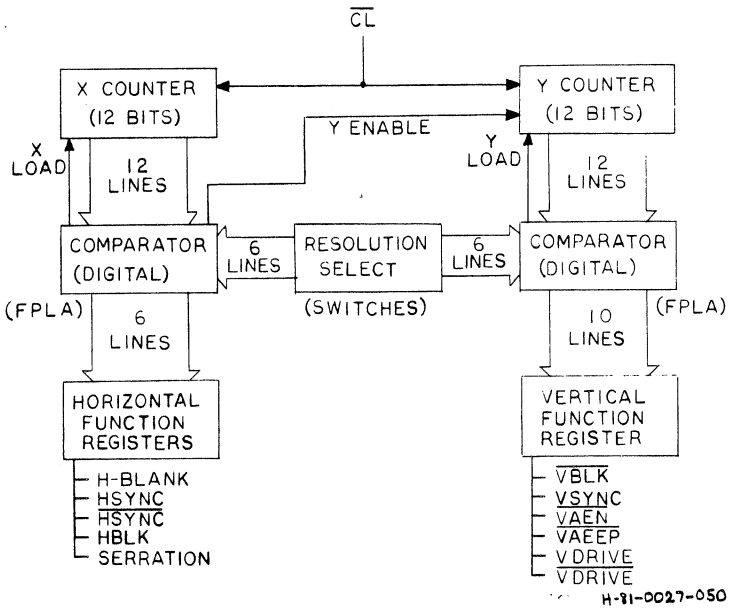


Figure 3-63. Raster Syncs and Blanks

Event timing of each of these signals is controlled by the resolution select switches. See table 3-34.

Table 3-34. Event Timing

FUNCTION	512 x 512	640 x 480
Set H BLANK	256	160
Reset H BLANK	336	206
Set HSYNC	266	166
Reset HSYNC	298	184
Set SERRATION	98, 266	63, 166
Reset SERRATION	124, 292	76, 179
Set $\overline{\text{VBLK}}$	512	480
Reset $\overline{\text{VBLK}}$	555	519
Set VSYNC	515	483
Reset VSYNC	518	486
Set $\overline{\text{VAEN}}$	512	480
Reset $\overline{\text{VAEN}}$	553	517
Set $\overline{\text{VAEEP}}$	512	480
Reset $\overline{\text{VAEEP}}$	554	518
Set VDRIVE	512	480
Reset VDRIVE	521	589

The X counter (figure 3-63) runs through its complete cycle each time the Y counter increments by 1. U28, U34, and U40 make up the X counter; U32, U33, U38 make up the Y counter. The X comparator consists of U22 and U26; the Y comparator consists of U21, U25, U20, and U24. The X register consists of U45 and U39; the Y register consists of U44, U49, and U43. All signals are synchronized by clock $\overline{CL}$. The VSYNC signal goes to the VCO to lock the oscillator phase, thus ensuring a stable raster.

The odd field enable signal ODDF is produced by gating $\overline{HSYNC}$ and SERRATION with VSYNC reset; gate output sets odd field register U48B. The register is reset by gating HSYNC and SERRATION with VSYNC reset.

The CSYNC signal is produced by gating HSYNC, $\overline{VDRIVE}$, and SERRATION with VSYNC. During the VDRIVE period, serration pulses are provided for sync; during all other times HSYNC pulses are provided for sync. During the middle of the VDRIVE period, VSYNC causes an inversion of the sync information.

The VAEE signal goes high on the leading edge of H BLANK (if $\overline{VAEEP}$ is high) and resets when $\overline{VAEEP}$ goes low.

3.12.3.13 Line Drivers and Polarity Select. The CSYNC, HSYNC, and VSYNC signals appear at J5, J6, and J7 of the timing module card, at an impedance level of 75 ohms. Three sections of configuration switch U12 can be set to produce either an inverted or a non-inverted output at these connectors.

3.12.3.14 Video Blink Clock and Cursor Clock. The cursor clock CCLK is created by dividing VSYNC by 8 in U50. The video blink clock is created by dividing VSYNC by 40 in U50 and U55.

SECTION 4

INSTALLATION

4.1 ENVIRONMENTAL CONSIDERATIONS

The terminal controller is designed to operate in an ambient temperature range of 15°C to 40°C (59°F to 104°F), and a relative humidity not exceeding 90%.

The terminal controller can be mounted in a 10.5-inch vertical space of a standard 19-inch equipment rack, either directly or on optional slide assemblies. The terminal controller can also be mounted in the equipment cabinet (Sanders part number 5976104), which also accommodates a system interconnect panel and a power panel assembly.

4.2 EQUIPMENT CABINET

The equipment cabinet is a four-wheeled, semi-portable equipment rack with the following approximate dimensions:

Height	Width	Depth
30 inches (76.3 cm)	23 inches (58.4 cm)	30 inches (76.2 cm)

When the equipment cabinet contains the terminal controller, system interconnect panel, and power panel assembly, they are arranged as follows:

The terminal controller is accessible from the front of the cabinet, and is installed in the upper half of the cabinet.

The power panel assembly is accessible from the front of the cabinet, and is installed in the lower half of the cabinet.

The system interconnect panel is accessible from the rear of the cabinet, and is installed in the lower half of the cabinet.

The cabinet has doors on both front and back. The front door is hinged on its right side, and is held shut by a magnetic latch. The front door has a cut-out to give access to the terminal controller controls and indicators. The rear door is hinged on its left side, and is held shut by a magnetic latch.

A cut-out in the bottom of the cabinet, below the system interconnect panel, is the entryway for power and signal cables.

4.3 POWER PANEL ASSEMBLY

The standard power panel assembly is Sanders part number 5976122. This power panel assembly is usable with prime power voltages of 100 Vac, 120 Vac, 220 Vac, and 240 Vac.

The power panel assembly contains a circuit breaker (CB1) in the prime power lines; a programmable power transformer; a line filter assembly; a 15-pin connector (J3) for voltage configuration; a power contractor (K1); and a duplex 110 Vac power outlet (J1, J2).

Outlet J1 is live when the circuit breaker on the power panel assembly is ON. Outlet J2 is live when the circuit breaker is ON and relay K1 is energized. Relay K1 is energized by a control signal at connector P2 on the power panel.

The power cord is Belden type 17612 (length 6 feet 7 inches, or 2 meters). The first step in installation is to connect an appropriate power connector to this power cord. The three lines in the power cord are color-coded as follows:

Light blue for the neutral line

Brown for the high line

Green/yellow for safety ground

The power cord is soldered to terminals on the line filter. The line filter suppresses transients that may appear on the primary power line. The output of the line filter goes to the circuit breaker.

The circuit breaker opens if the current at 115V exceeds 10A or if the current at 220 V exceeds 5A.

The high line output of the circuit breaker goes to pin 1 of connector J3 (brown wire) and to pin 3 of connector J3 (light blue wire). The neutral line output of the circuit breaker goes to pin 2 of connector J3 (tan wire) and to pin 4 of connector J3 (dark blue wire).

The mating connector P3 contains jumper connections that set up the primary windings of the power transformer to match the input voltage. Connector P3 is wired as shown in table 4-1.

Table 4-1. Connector P3 Configurations

G-CONDITION	INPUT VOLTAGE	JUMPERS INSTALLED
G1	100 Vac	1 to 6; 3 to 7; 10 to 13 to 15; 11 to 12 to 14
G2	120 Vac	1 to 5 to 8; 3 to 7 to 9; 10 to 13 to 15; 11 to 12 to 14
G3	220 Vac	2 to 6; 4 to 9; 7 to 8; 10 to 13 to 15; 11 to 12 to 14
G4	240 Vac	2 to 5; 4 to 9; 7 to 8; 10 to 13 to 15; 11 to 12 to 14

Connections from J3 to the transformer primary winding are as follows:

From J3-5 to T1-C (white)

From J3-6 to T1-A (white)

From J3-7 to T1-E (white)

From J3-8 to T1-D (white)

From J3-9 to T1-F (white)

The output from the transformer secondary winding (110 Vac) goes back to connector J3 as follows:

From T1-1 to J3-10 (light blue)

From T1-2 to J3-11 (brown)

The 110 Vac lines go from connector J3 to the duplex output box connector J1 as follows:

From J3-13 to J1-N (light blue)

From J3-12 to J1-L (brown)

The ground pin of the duplex output box is connected to the outlet box mounting stud.

The 110 Vac lines go from connector J3 to the power contactor K1 as follows:

From J3-15 to K1-8 (light blue)

From J3-14 to K1-7 (brown)

The 110 Vac lines go from power contactor K1 to duplex output box connector J2 as follows:

From K1-4 to J2-N (light blue)

From K1-3 to J2-L (brown)

The power contactor control signal goes from connector P2 to power contactor K1 as follows:

From P2-1 to K1-5 (red)

From P2-3 to K1-6 (black)

From P2-2 to K1 mounting stud (shield)

4.3.1 ALTERNATIVE POWER PANEL ASSEMBLY. The alternative power panel assembly (Sanders part number 5976121) is usable if the prime power is 110 Vac. The alternative power panel contains a filter, a circuit breaker, a relay, and a duplex outlet box. The power cord is Belden type 17612 with the original power connector left on.

Outlet J1 is live when the circuit breaker on the power panel assembly is ON. Outlet J2 is live when the circuit breaker is ON and power contactor K1 is energized. The power contactor is energized by a control signal at connector P2 on the power panel.

4.4 SYSTEM INTERCONNECT PANEL ASSEMBLY

The system interconnect panel (Sanders part number 5976105) provides a convenient means of connecting the terminal controller to the host computer, to the displays, and to other peripheral devices (keyboards, position entry devices, PHOTOPENs).

The panel assembly consists of a panel with cutouts and a number of cable assemblies with connectors; some of the connectors are secured to the panel at their respective cutouts.

Figure 4-1 shows typical wiring between the terminal controller and the system interconnect panel and lists the part numbers of the cable assemblies. Note that figure 4-1 shows the back side of the interconnect panel assembly.

4.5 CONNECTIONS TO BE MADE AT INSTALLATION

4.5.1 TERMINAL CONTROLLER MOUNTED IN EQUIPMENT CABINET. If the terminal controller and equipment cabinet are ordered at the same time, the terminal controller is shipped from the factory installed in the equipment cabinet, and all connections between the terminal controller and the system interconnect panel are already made.

For other situations, refer to figure 4-1.

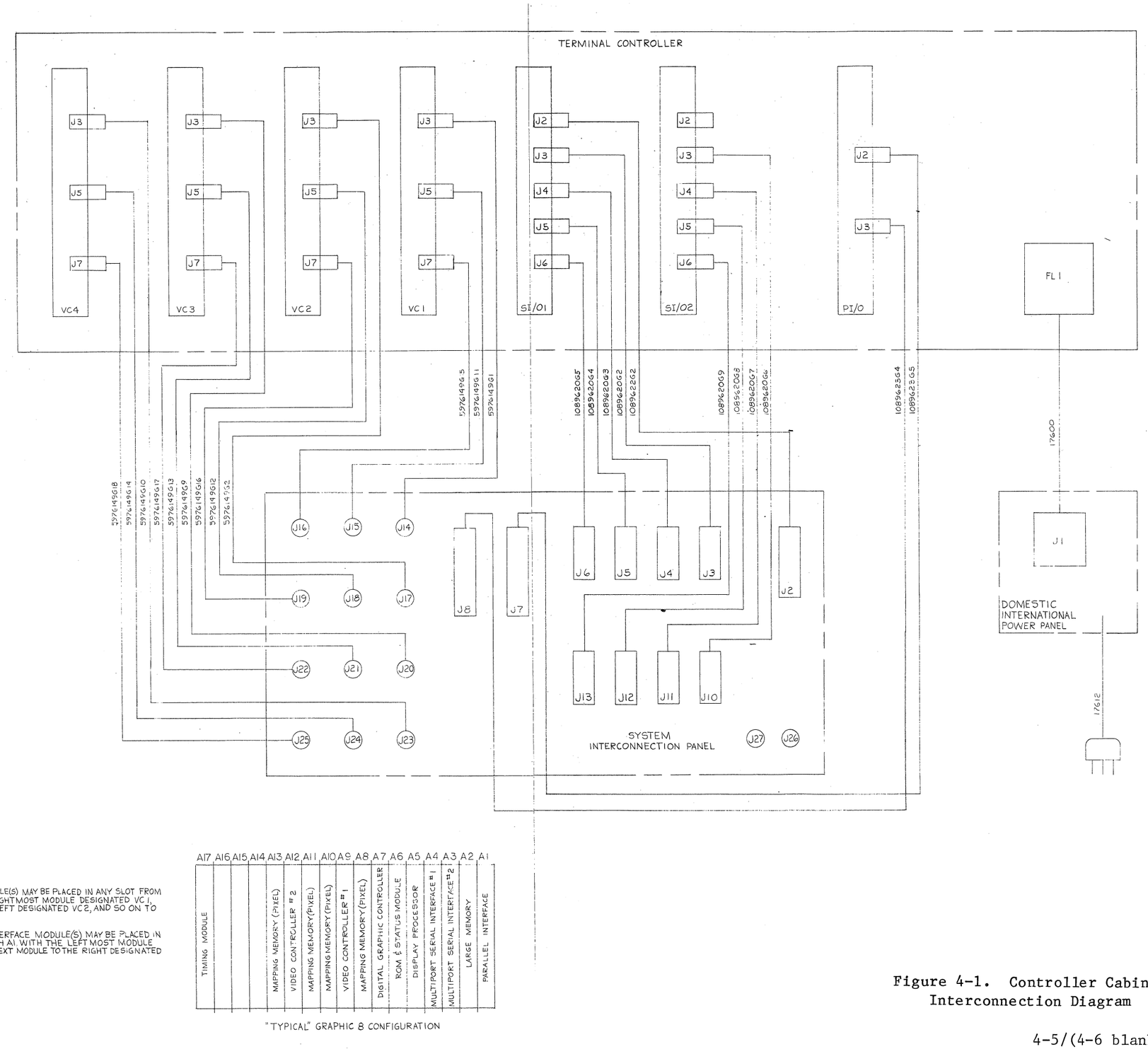
Connections between the system interconnect panel and other devices are a function of the individual installation. Refer to the top assembly drawing for your installation. In general:

1. Connections to the host computer are made by cables from J1 and J8 of the system interconnect panel to the appropriate point in the host computer. If the parallel interface is not Sanders model no. 5712 (part number 1086802), then the cables needed to connect between the system interconnect panel and the host computer may be supplied with the parallel interface. If the parallel interface is Sanders model no. 5712, then the interconnecting cables are the customer's responsibility.

2. If the GRAPHIC 8 system does not contain a parallel interface, and communications with the host computer are through the multiport serial interface, then the cable needed to connect between the system interconnect panel and the host computer is the customer's responsibility. The cable would normally be connected to the J2 connector on the system interconnect panel, but in some cases could be connected to J3.

3. If the GRAPHIC 8 system includes one alphanumeric keyboard, the keyboard shall connect to J5 on the system interconnect panel. However, if the associated display indicator pedestal contains an accessory panel, the keyboard may plug into that accessory panel, from whence another cable leads to J5 on the system interconnect panel.

4. If the GRAPHIC 8 system includes two alphanumeric keyboards and two serial interface cards, the second keyboard connects (either directly or through an accessory panel) to J12 on the system interconnect panel.



2. THE VIDEO CONTROLLER MODULE(S) MAY BE PLACED IN ANY SLOT FROM A8 THROUGH A16, WITH THE RIGHTMOST MODULE DESIGNATED VC1, THE NEXT MODULE TO THE LEFT DESIGNATED VC2, AND SO ON TO VC3 AND VC4.

1. THE MULTIPORT SERIAL INTERFACE MODULE(S) MAY BE PLACED IN ANY SLOT FROM A4 THROUGH A1 WITH THE LEFT MOST MODULE DESIGNATED SI/01 AND THE NEXT MODULE TO THE RIGHT DESIGNATED SI/02

"TYPICAL" GRAPHIC 8 CONFIGURATION

Figure 4-1. Controller Cabinet Interconnection Diagram

5. If the GRAPHIC 8 system includes two alphanumeric keyboards and only one serial interface card, the second keyboard connects (either directly or through an accessory panel) to J4 on the system interconnect panel; the serial interface card must be modified (as described in table 3-12) to make its port 2 appear to be port 7.

6. If the GRAPHIC 8 system includes one position entry device (trackball, forcestick, or data tablet), the PED shall connect to J6 on the system interconnect panel. However, if the associated display indicator pedestal contains an accessory panel, the PED may plug into that accessory panel, from whence another cable leads to J6 on the system interconnect panel.

7. If the GRAPHIC 8 system includes two PEDs and two serial interface cards, the second PED connects (either directly or through an accessory panel) to J13 on the system interconnect panel.

8. If the GRAPHIC 8 system includes two PEDs and only one serial interface card, the second PED connects (either directly or through an accessory panel) to J4 on the system interconnect panel; the serial interface card must be modified (as described in table 3-12) to make its port 2 appear to be port 8.

9. If the GRAPHIC 8 system includes one PHOTOPEN, it connects to J26 on the system interconnect panel. However, if the associated display indicator pedestal contains an accessory panel, the PHOTOPEN may plug into that accessory panel, from whence another cable leads to J26 on the system interconnect panel.

10. If the GRAPHIC 8 system includes two PHOTOPENs, the second one connects (either directly or through an accessory panel) to J27 on the system interconnect panel. In this case the customer must specify an additional cable, part number 5976150G1, to connect from the system interconnect panel to the PHOTOPEN 2 connector on the terminal controller.

11. Connectors J14 through J16 on the system interconnect panel are exact replicas of connectors J3, J5, J7 of the video controller card #1. Similarly J17 through J19 on the system interconnect panel correspond to J3, J5, J7 of video controller card #2; J20 through J22 pertain to video controller card #4, and J23 through J25 pertain to video controller card #4.

12. Connector J2 on the ROM and status card (usable with a teletypewriter, paper tape reader, keyboard, PED, or even the host computer) does not have a comparable connector on the system interconnect panel. Any connection must be made directly to the connector on the edge of the ROM and status card, using a cable with suitable connectors.

4.5.2 TERMINAL CONTROLLER WITHOUT EQUIPMENT CABINET. If the terminal controller is purchased without the equipment cabinet (as for rack mounting or installation in a display console), and if the system interconnect panel is not procured, then connections between the terminal controller, the host computer, and the peripheral devices must be made directly to connectors on the terminal controller.

If the GRAPHIC 8 system includes a parallel interface, the cables from the host computer go to connectors J2 and J3 on the edge of the parallel interface card. J2 accepts output data and control signals from the host computer. J3 carries input data and control signals to the host computer. Table 4-2 lists and identifies the pins in parallel interface connectors J2 and J3 for the model 5712 parallel interface.

Table 4-2. Parallel Interface I/O Connectors, Pin Assignments

JACK/PIN	SIGNAL	JACK/PIN	SIGNAL	JACK/PIN	SIGNAL
J2-1	ODO0(±)	J2-34	SPARE	J3-17	IDO8(±)
J2-2	DRET-	J2-35	ATN1(±)	J3-18	DRET-
J2-3	ODO1(±)	J2-36	DRET-	J3-19	IDO9(±)
J2-4	DRET-	J2-37	OWR(±)	J3-20	DRET-
J2-5	ODO2(±)	J2-38	DRET-	J3-21	ID10(±)
J2-6	DRET-	J2-39	OMR(±)	J3-22	DRET-
J2-7	ODO3(±)	J2-40	DRET-	J3-23	ID11(±)
J2-8	DRET-	J2-41	OCTL(±)	J3-24	DRET-
J2-9	ODO4(±)	J2-42	DRET-	J3-25	ID12(±)
J2-10	DRET-	J2-43	ODR(±)	J3-26	DRET-
J2-11	ODO5(±)	J2-44	DRET-	J3-27	ID13(±)
J2-12	DRET-	J2-45	SPARE	J3-28	DRET-
J2-13	ODO6(±)	J2-46	SPARE	J3-29	ID14(±)
J2-14	DRET-	J2-47	INIT	J3-30	DRET-
J2-15	ODO7	J2-48	DRET-	J3-31	ID15(±)
J2-16	DRET-	J2-49	*IMR(±)	J3-32	DRET-
J2-17	ODO8(±)	J2-50	SPARE	J3-33	*SPR1-
J2-18	DRET-			J3-34	SPARE
J2-19	ODO9(±)	J3-1	IDO0(±)	J3-35	IMR(±)
J2-20	DRET-	J3-2	DRET-	J3-36	DRET-
J2-21	OD10(±)	J3-3	IDO1(±)	J3-37	ICTL(±)
J2-22	DRET-	J3-4	DRET-	J3-38	DRET-
J2-23	OD11(±)	J3-5	IDO2(±)	J3-39	ATN2(±)
J2-24	DRET-	J3-6	DRET-	J3-40	DRET-
J2-25	OD12(±)	J3-7	IDO3(±)	J3-41	IWR(±)
J2-26	DRET-	J3-8	DRET-	J3-42	DRET-
J2-27	OD13(±)	J3-9	IDO4(±)	J3-43	SPARE
J2-28	DRET-	J3-10	DRET-	J3-44	DRET-
J2-29	OD14(±)	J3-11	IDO5(±)	J3-45	NDRY(±)
J2-30	DRET-	J3-12	DRET-	J3-46	SPARE
J2-31	OD15(±)	J3-13	IDO6(±)	J3-47	SPARE
J2-32	DRET-	J3-14	DRET-	J3-48	SPARE
J2-33	*SPR1-	J3-15	IDO7(±)	J3-49	*SPR2-
		J3-16	DRET-	J3-50	SPARE

*Signals used only in test operation using input to output (J3 to J2) loop cable.

If the GRAPHIC 8 system does not include a parallel interface, the cable from the host computer goes to connectors J2 or J3 on the edge of the serial interface card, or (in some cases) to connector J2 on the ROM and status card. In addition, peripheral devices (keyboard, PED) connect directly to the appropriate connector on the edge of the serial interface card. (Refer to table 3-12.) It is imperative that the serial interface card be configured to match each port to the type of device connected to it. Table 4-3 lists and identifies the pins in serial interface connectors J2 through J6.

Table 4-3. Multiport Serial Interface I/O Connectors, Pin Assignments

JACK/PIN	SIGNAL		JACK/PIN	SIGNAL	
J2-1	CGND	PORT 1	J3-9	REN1-	PORT 1
J2-2	SPARE		J3-10	N15V	
J2-3	X232-				
J2-4	TSCK+		J4-1	XMT2-	PORT 2
J2-5	RDA1-		J4-2	P15V+	
J2-6	SPARE		J4-3	DRET-	
J2-7	RQTS+		J4-4	DRET-	
J2-8	RSCK+		J4-5	RDA2-	
J2-9	CLTS+		J4-6	P05V+	
J2-10	SPARE		J4-7	DRET-	
J2-11	DSRY+		J4-8	DRET-	
J2-12	SPARE		J4-9	REN2-	
J2-13	SPARE		J4-10	N15V-	
J2-14	DGND				
J2-15	DTRY+		J5-1	XMT3	PORT 3
J2-16	CARR+		J5-2	P15V+	
J2-17	SPARE		J5-3	DRET-	
J2-18	SPARE		J5-4	DRET-	
J2-19	RING+		J5-5	RDA3-	
J2-20	SPARE		J5-6	P05V+	
J2-21	SPARE		J5-7	DRET-	
J2-22	SPARE		J5-8	DRET-	
J2-23	TXCO+		J5-9	REN3-	
J2-24	SPARE		J5-10	N15V-	
J2-25	SPARE				
J2-26	SPARE		J6-1	XMT4-	PORT 4
			J6-2	P15V+	
J3-1	XMT1-	PORT 1	J6-3	DRET-	
J3-2	P15V+		J6-4	DRET-	
J3-3	DRET-		J6-5	RDA4-	
J3-4	DRET-		J6-6	P05V+	
J3-5	RDA1-		J6-7	DRET-	
J3-6	P05V+		J6-8	DRET-	
J3-7	DRET-		J6-9	REN4-	
J3-8	DRET-		J6-10	N15V-	

The J2 connector on the ROM and status card is identical to connectors J3 through J6 of the serial interface.

Display indicators connect to J3, J5, J7 on the edge of the video controller card. Refer to the technical manual for your display indicator for the method of making connections.

PHOTOPENs connect directly to PHOTOPEN connector J1 and J2 on the terminal controller card cage.

4.6 SWITCH AND JUMPER SELECTIONS

Some of the circuit cards in the terminal controller contain jumper terminals and/or switches to allow selection of operating characteristics that differ from those normally preselected at the factory.

4.6.1 DISPLAY PROCESSOR. Terminals E39 and E40 let the display processor recognize instruction 0 as a halt instruction or as an illegal instruction, as follows:

STATUS	JUMPER CONFIGURATION
Instruction 0 = halt	E39 to E40 jumpered (normal configuration)
Instruction 0 illegal	E39 and E40 open

4.6.2 READ/WRITE MEMORY. Confirm that switches are set and jumpers installed as shown in table 4-4.

Table 4-4. Read/Write Memory Switches and Jumpers

MEMORY CONFIGURATION	S1 SWITCH POSITIONS		JUMPER CONNECTIONS	
	CARD #1	CARD #2	CARD #1	CARD #2
16K	S1-1 thru S1-5 ON	N/A	E2-E3	N/A
32K	S1-1 ON S1-2 thru S1-5 OFF*	N/A	E2-E3	N/A
64K	S1-1 ON S1-2 thru S1-5 OFF*	N/A	E1-E2	N/A
96K	S1-1 ON S1-2 thru S1-5 OFF*	S1-1 OFF S1-2 thru S1-5 OFF*	E1-E2	E2-E3
128K	S1-1 ON S1-2 thru S1-5 OFF*	S1-1 OFF S1-2 thru S1-5 OFF*	E1-E2	E1-E2

*These switch positions allow access to all available memory. To mask out undesired memory blocks, set corresponding switch to ON.

4.6.3 ROM AND STATUS CARD. This card contains jumper terminals that allow reconfiguration of 15 different parameters, as described in table 4-5.

Table 4-5. ROM and Status Card Jumper Configurations

FEATURE	JUMPER CONFIGURATION
Sync link interrupt level	
Level 7	E1 to E4 (normal configuration)
Level 6	E2 to E4
Level 5	E3 to E4
Display status interrupt level	
Level 5	E3 to E5 (normal configuration)
Level 6	E2 to E5
Level 7	E1 to E5
Transmit data select	
TTY, RS-232C, or 20 mA current loop	E7 to E8 (normal configuration)
TTL	E7 to E6
Receive data termination	
TTY	E35 to E36 (normal configuration)
TTL	E9 to E10; E35 to E36 open
20 mA current loop	E9 to E11; E35 to E36 open
RS-232C	No jumper at E35, E36, E9
Receive/transmit data	
TTY	E12 to E13 open (normal configuration)
TTL or RS-232C	E12 to E13
Word length select	
5 bits	E14 to E17 to E19
6 bits	E14 to E19
7 bits	E17 to E19
8 bits	E14 and E17 open (normal configuration)

Table 4-5. ROM and Status Card Jumper Configuration (Cont)

FEATURE	JUMPER CONFIGURATION
Receive/transmit parity	
Checked and generated	E16 to E19
Disabled	E16 open (normal configuration)
Parity select	
Odd	E18 to E19
Even	E18 open (normal configuration)
Number of stop bits	
2 stop bits	E15 to E19
1 stop bit	E15 open (normal configuration)
Receive/transmit frequency select	
110 baud	E20 to E22; E23 to E25 to E26 to E27 (normal configuration)
300 baud	E20 to E22; E24 to E26 to E27
1200 baud	E20 to E22; E26 to E27
2400 baud	E20 to E22; E23 to E25 to E27
4800 baud	E20 to E22; E23 to E24 to E27
9600 baud	E20 to E22; E23 to E27
50K baud	E20 to E21
System clock mode	
Internal clock	E28 to E29 (normal configuration)
External clock	E29 open
Address selection	
16K to 24K	E44 to E32
20K to 28K	E30 to E32
24K to 32K	E31 to E32

Table 4-5. ROM and Status Card Jumper Configuration (Cont)

FEATURE	JUMPER CONFIGURATION
Status logic enable	
Enabled	E33 to E34 (normal configuration)
Disabled	E33 open
Trap address memory locations	
0 - 8K	E37, E38, E39, E40 open (normal configuration)
8K - 16K	E39 to E40
16K - 24K	E37 to E38
24K - 32K	E37 to E38; E39 to E40
50K/800K baud select	
50 kHz	E42 to E43 (normal configuration)
800 kHz	E41 to E43

4.6.4 MULTIPORT SERIAL INTERFACE. This card contains both jumper terminals and DIP switches that allow reconfiguration of 14 different parameters, as described in table 4-6.

Table 4-6. Multiport Serial Interface Parameter Selections

FEATURE	CONFIGURATION
Device address select	
Standard address (1765XX)	U19-S8 OFF (normal configuration)
Expanded address (1766XX)	U19-S8 ON

Device assignments

Refer to table 3-12.

Table 4-6. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION			
Word length select	Port 2	Port 3	Port 4	
5 bits	E43 to E44, E45 to E46	E33 to E34, E35 to E36	E53 to E54, E55 to E56	
6 bits	E45 to E46	E35 to E36	E55 to E56	
7 bits	E43 to E44	E33 to E34	E53 to E54	
8 bits (normal configuration)	E44, E46 open	E34, E36 open	E54, E56 open	
Parity select	Port 2	Port 3	Port 4	
Parity enabled (normal configuration)	E49 to E50	E39 to E40	E59 to E60	
Parity disabled	E50 open	E40 open	E60 open	
Odd parity	E47 to E48	E37 to E38	E57 to E58	
Even parity	E48 open	E38 open	E58 open	
Stop bit select	Port 2	Port 3	Port 4	
1 stop bit (normal configuration)	E51 to E52	E41 to E42	E61 to E62	
2 stop bits	E52 open	E42 open	E62 open	
Transmit levels	Port 1	Port 2	Port 3	Port 4
RS-232 (normal configuration)	E9 to E10	E12 to E13	E30 to E31	E23 to E24
TTL	E10 to E11	E13 to E14	E31 to E32	E24 to E25
Receive levels	Port 1	Port 2	Port 3	Port 4
TTL	E5 to E6	E15 to E16	E19 to E20	E26 to E27
RS-232	E5 open	E15 open	E19 open	E26 open

Table 4-6. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
F_t baud rate (all ports, asynchronous)	
NOTE: E63 to E64 and E65 to E66 are connected for all baud rates.	
9600 baud (normal configuration)	E68 to E67; E69, E71, E73 open
50 baud	E68 to E67 to E69 to E71 to E73
75 baud	E68 to E69 to E71 to E73
110 baud	E68 to E67 to E71 to E73
134.5 baud	E68 to E71 to E73
150 baud	E68 to E67 to E69 to E73
300 baud	E68 to E69 to E73
600 baud	E68 to E67 to E73
1200 baud	E68 to E73
1800 baud	E68 to E67 to E69 to E71
2000 baud	E68 to E69 to E71
2400 baud	E68 to E67 to E71
3600 baud	E68 to E71
4800 baud	E68 to E67 to E69
7200 baud	E68 to E69
19200 baud	E68 to E67

F_r baud rate (port 1 only)	U80-S4	U80-S5	U80-S6	U80-S7
50	On	On	On	On
75	Off	On	On	On
110	On	Off	On	On
134.5	Off	Off	On	On

Table 4-6. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION			
F_r baud rate (port 1 only) (Cont)	U80-S4	U80-S5	U80-S6	U80-S7
150	On	On	Off	On
300	Off	On	Off	On
600	On	Off	Off	On
1200	Off	Off	Off	On
1800	On	On	On	Off
2000	Off	On	On	Off
2400	On	Off	On	Off
3600	Off	Off	On	Off
4800	On	On	Off	Off
7200	Off	On	Off	Off
9600 (normal configuration)	On	Off	Off	Off
19200	Off	Off	Off	Off
Number of stop bits (port 1)				
1 stop bit	U80-S3 on			
2 stop bits	U80-S3 off			
Parity (port 1 only)				
Parity disabled	U80-S1 off			
Parity enabled	U80-S1 on			
Odd parity	U80-S2 on			
Even parity	U80-S2 off			

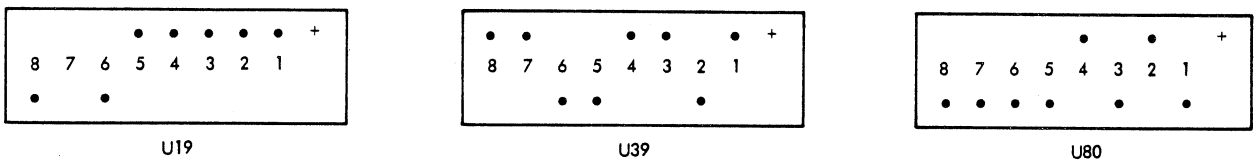
NOTE

If parity is disabled, there are eight data bits. If parity is enabled, there are seven data bits.

Table 4-6. Multiport Serial Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Data terminal ready (port 1 only)	
Circuit enabled	U39-S7 on
Circuit disabled	U39-S7 off
Interrupt level select	
Level 5	E1 to E3
Level 6 (normal configuration)	E2 to E3
Level 7	E4 to E3

Figure 4-2 shows the normal switch positions for the standard port configuration. The + mark on the switch indicates the ON side. The dots in the figure indicate the side of the switch that is pushed down.



H-80-0055-008

Figure 4-2. Serial Interface, Normal Switch Positions

4.6.5 PARALLEL INTERFACE. The model 5712 parallel interface card contains 105 terminals that allow you to customize the card for special installations. Most of the terminals (E1 through E43 and E49 through E66) plus an 2.35 by 6.5 inch (6 by 16.5 cm) unused area are for use with additional integrated circuit elements, which can interface with devices that have unique signal definitions, signal polarities, handshaking requirements, and/or driver/receiver and line matching requirements.

The remaining terminals let you change certain operating parameters, as described in table 4-7.

Table 4-7. Parallel Interface Parameter Selections

FEATURE	CONFIGURATION
Register address select	
First card, address 17241X (normal configuration)	E96 to E99
Second card, address 17243X	E98 to E99

Table 4-7. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Register address select (Cont)	
Third card, address 17245X	E97 to E99
Fourth card, address 17247X	E95 to E99
Interrupt trap address select	
First card (normal configuration)	E87, E88 open; E47, E45 open
Second card	E87 to E88, E46 to E47; E45 open
Third card	E87 to E88, E44 to E45; E47 open
Fourth card	E87 to E88, E44 to E45, E46 to E47
Word vs byte mode	
Word mode (normal configuration)	E90 open
Byte mode	E89 to E90
Polarity of INIT signal from host	
Low (INIT-) produces SYST-B	E93 to E94
High (INIT+) produces SYST-B	E92 to E94
SYST-B inhibited	E91 to E94
Interrupt priority level	
Level 6 (normal configuration)	E83 to E85
Level 5	E84 to E85
Level 7	E86 to E85
Clock speed	
CLOK-F (10 MHz) (normal configuration)	E100 to E101
Clock rate divided (for long distance interface)	Open E100 to E101. Connect E100 to input of a suitable divider. Connect divider output to E101. (Divider may be added to the parallel interface card or located externally with connections made through unused backplane connections).

Table 4-7. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Output data enable ODEN- signal from host	
ODEN- enabled	E102 to E103
ODEN- disabled	E102, E103 open
Input data enable function	
Ground enable to input drivers	E104 to E105
Ground enable not required	E104, E105 open
Additional integrated circuit connections	
NOTE: These connections allow additional integrated circuits to be added to the card.	
Connect attention interrupt enable to IC	E48
Accept interrupt requests from IC	E67
Connect resets to IC	E68
Connect fixed logic high to IC	E69
Connect +5V to IC	E70 through E78
Connect -15V to IC	E79
Connect ARET- to IC	E80
Connect +15V to IC	E81
Accept reset from IC	E82
Card device select	
Normal configuration is:	
DEV0-B high	E112, E113 open
DEV1-B low	E114 to E115

Table 4-7. Parallel Interface Parameter Selections (Cont)

FEATURE	CONFIGURATION
Card device select (Cont)	
DEV2-B high	E116, E117 open
DEV3-B active	E110 to E111
Device codes for second, third, and fourth cards can be created by connecting E112 to E113, E116 to E117, or both.	

4.6.6 OTHER CARDS. Switches and jumper selections on the digital graphic controller, mapping memory, video controller, and timing module establish the system configuration. These selections are set at the factory in accordance with the customer's requirements and should not be touched in the field.

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains the maintenance philosophy, test equipment required, troubleshooting instructions, adjustments, and repair information.

5.2 MAINTENANCE PHILOSOPHY

The maintenance philosophy for the terminal controller is to limit repairs to replacement of plug-in circuit cards and chassis-mounted components. This approach reduces system down-time if a failure occurs. Field repair of circuit cards is not recommended because of their complexity. Testing them requires special factory-level test equipment.

If you encounter a failure, try to isolate the failure to a specific circuit card, then replace that card and make any required adjustments. If the system resumes normal operation, the card that you took out is defective. Return that card to Sanders for repair. Send us also a description of the symptoms that led you to the failed card.

5.3 TEST EQUIPMENT REQUIRED

The following equipment (or equivalent) is recommended for maintenance of the terminal controller:

Oscilloscope	Tektronix type 547 with type 1A1 preamplifier
Digital voltmeter	Fluke model 8000A
Multimeter	Triplett model 630
Card extender	Sanders part no. 4171110

5.4 TROUBLESHOOTING INSTRUCTIONS

Follow the steps indicated in figure 5-3. Pay attention to the cautions of sheet 1 of the figure.

5.4.1 BUILT-IN DIAGNOSTICS. When the terminal controller is initialized in the SYSTEM mode, it executes a set of diagnostic routines that test the GO/NO GO status of certain circuit cards. If a NO GO is detected, the terminal controller sets a bit in the diagnostic error word, and an error message containing the error word is sent to the host computer. The message indicates the diagnostic routine that failed, but does not specifically state how the routine failed.

When you initialize the terminal controller in the LOCAL mode, it executes the same set of diagnostic routines, then executes the terminal verification pattern. The results of the diagnostic routines are displayed in the left field of the readout box as an octal number with the letter T above it (the letter T means that the 3-digit code is the result of the diagnostic routines).

If all tests pass, the 3-digit number is 000, assuming all cards are installed. If any card is not installed, the bit for that card is set, producing an error indication.

If more than one test fails, and sequencing through the remaining tests does not stop, the readout is the sum of all the failed tests. For example, if the terminal controller does not contain a 3D coordinate converter, and both the memory and the graphic controller diagnostics fail, the readout is 045.

The following paragraphs describe the diagnostic routines.

Serial Interface Diagnostic. This test verifies initialization of the status registers.

Parallel Interface Diagnostic. This tets verifies initialization of the hand-shaking circuits and status registers.

Display Processor Diagnostic. This test verifies execution of a branch instruction, an interrupt sequence, and single-word, double-word, and triple-word instructions from the instruction set.

Memory Diagnostic. This test verifies the ability to write and read at each memory location. (During this test, any data already contained in a memory location is temporarily stored in a general purpose register, then restored to its location.)

Graphic Controller Diagnostic. This test verifies that:

1. Each display register is initialized.

2. The graphic controller is in its proper state.

3. The display processor can start a refresh sequence.

4. The graphic controller can start, run, access memory, perform refresh functions, and stop.

3D Coordinate Converter Diagnostic. This test verifies the 3D coordinate converter's ability to write and execute a simple instruction.

5.4.2 TERMINAL VERIFICATION PATTERN. The terminal verification pattern can be used with up to two display indicators and a full complement of peripherals. The pattern verifies proper operation of the terminal controller and display indicators. Each area of the verification pattern has a specific function: either executing a system parameter or providing a visual indication for fault isolation.

5.4.2.1 Character Verification. The character area of the test pattern displays the character repertoire, including alphanumerics and special symbols. In addition, the letters EM are displayed in three different sizes.

5.4.2.2 PED Manipulation. A set of numerals and asterisks should appear at the upper left corner of the screen. The numerals indicate the PED assigned to the symbol. There may be up to eight symbols present, depending on the input device configuration as set on the display processor.

5.4.2.3 Polygon Fill. The triangle directly below the monitor number will cycle through all available colors in the particular configuration.

5.4.2.4 Point Plot. All point plot instructions are used to build the geometric plot in the center of the screen.

5.4.2.5 Overflow Indicators. Various full-screen vectors will appear in the test pattern if X or Y overflow interrupts occur unexpectedly or if they fail to occur when they are expected. See figures 5-1 and 5-2.

5.4.3 ADDITIONAL HINTS. The circuit cards that connect to the processor bus (cards in slots XA1 through XA7) can be installed in other arrangements than that shown in figure 5-3. However, the following rules must be followed:

1. All read/write memory cards should be installed in consecutive slots.

2. Those cards that can seize the processor bus should be installed in consecutive slots, to maintain the integrity of the grant bus. If there is a gap between such cards, you effectively get two grant buses in parallel, with subsequent interference when two cards want the bus at the same time. If it is necessary to separate such cards, you must connect the grant out connection (pin 35) of the higher priority card (lower numbered slot) across the gap to the grant in connection (pin 36) of the next lower priority card (higher numbered slot). For this type of connection, use Sanders part number 47067, daisy-chain jumper.

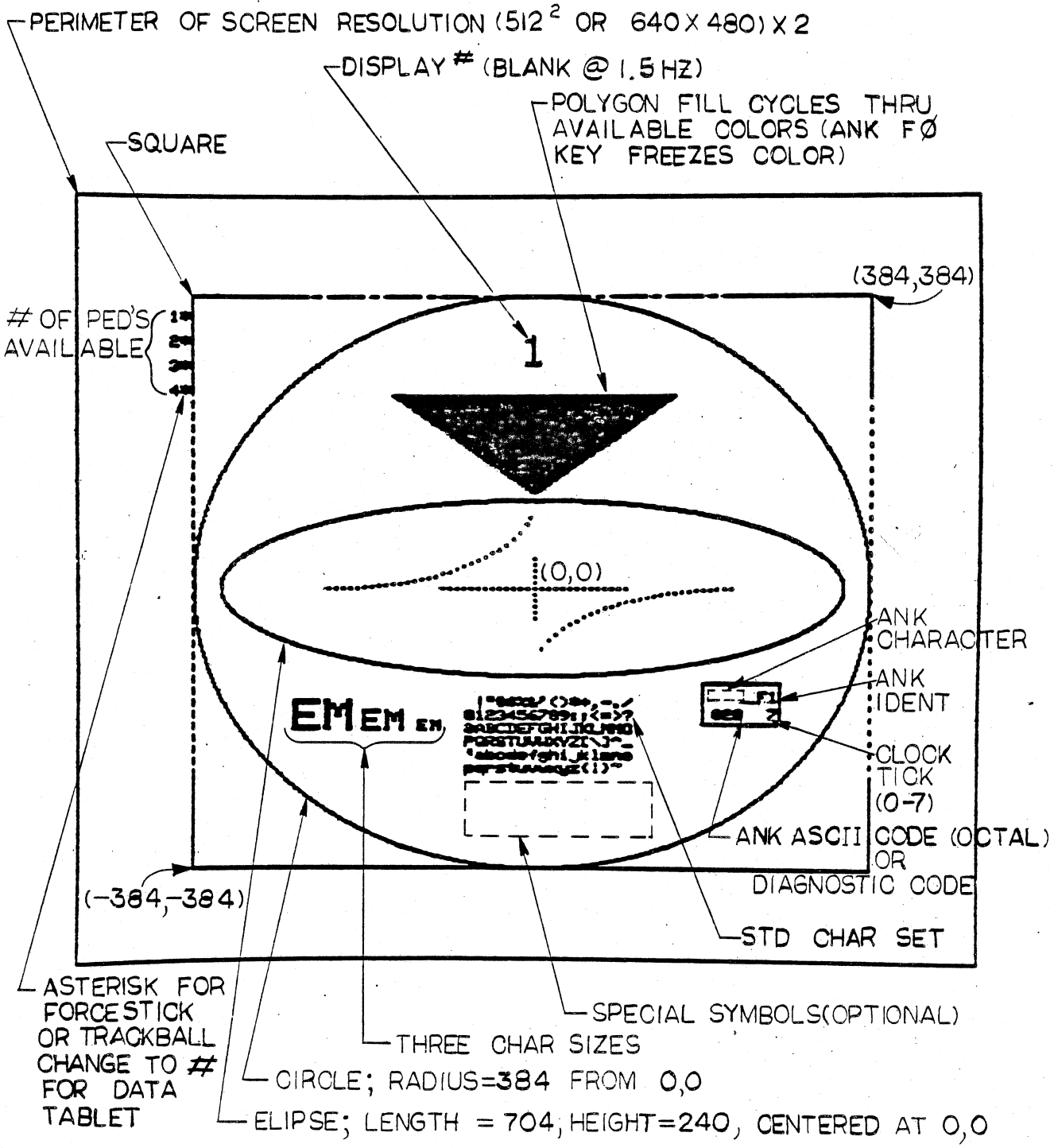


Figure 5-1. Verification Test Pattern

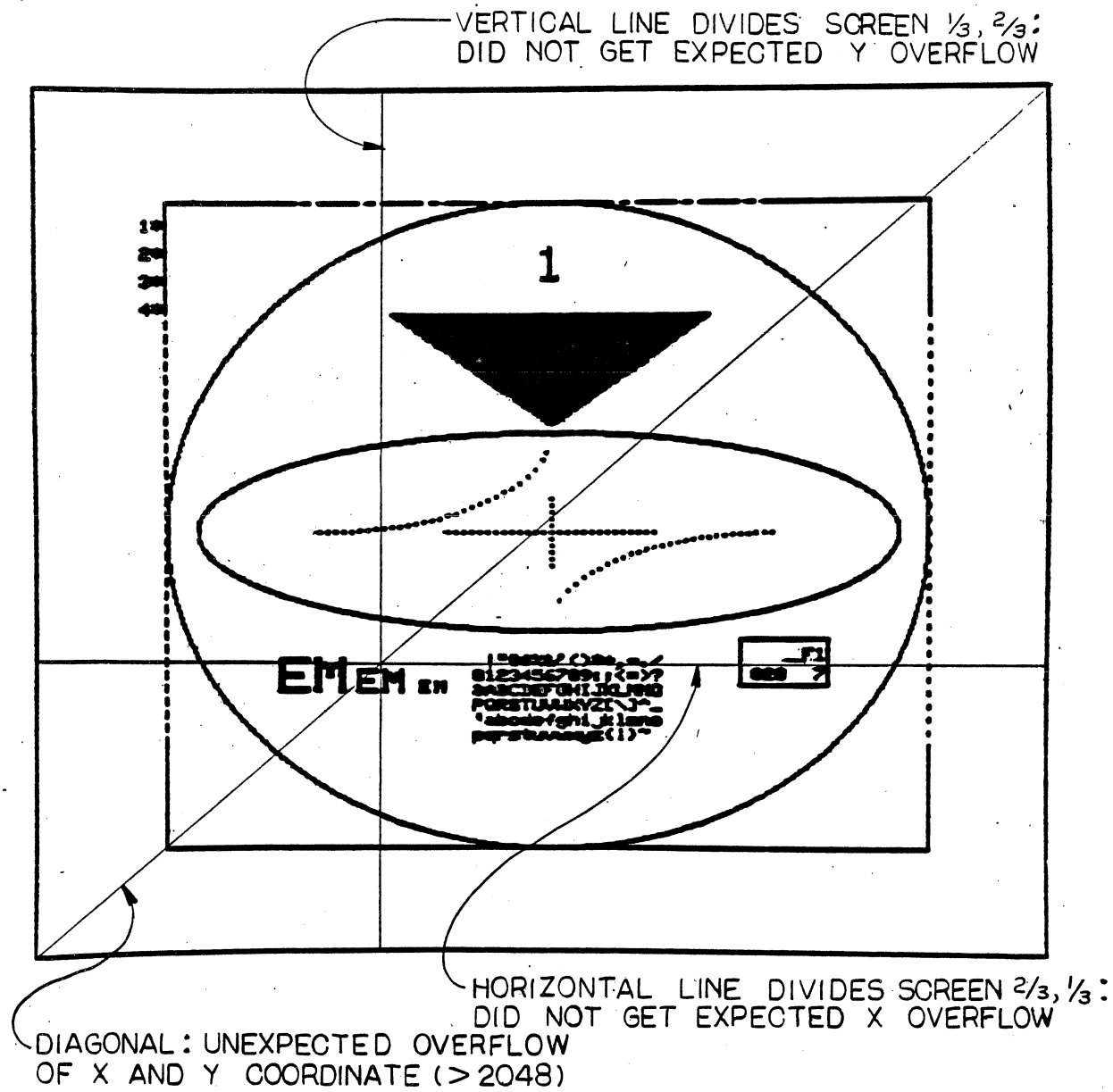
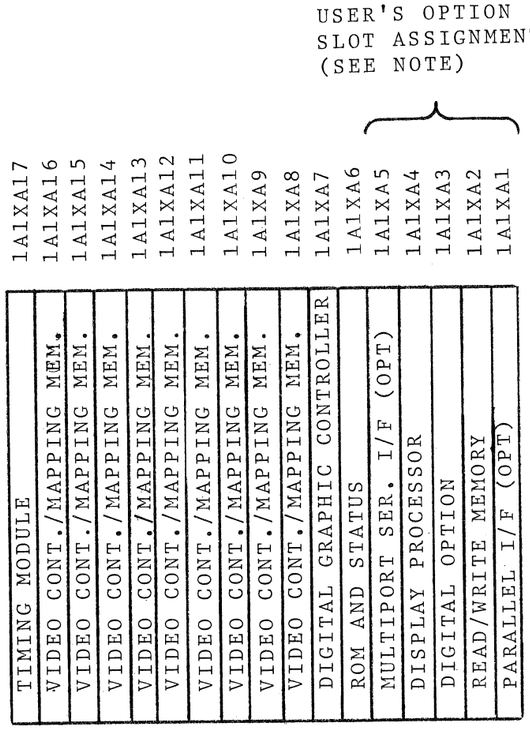


Figure 5-2. Verification Test Pattern



WARNING

TERMINAL CONTROLLER OPERATES ON 110 VAC POWER. ASSOCIATED POWER CONTROL PANEL MAY HAVE 220 TO 240 VAC INPUT.

CAUTION

ALWAYS TURN TERMINAL CONTROLLER OFF BEFORE REMOVING OR INSERTING CIRCUIT CARDS.

MAPPING MEM, LARGE MEM, AND TIMING MODULE CONTAIN MOS DEVICES. WHEN NOT IN USE, STORE THESE CARDS IN STATIC-PROOF CONTAINERS.

NOTE

The backplane wiring for the card cage is identical for card slots 1A1XA1 through 1A1XA5, making the designated card placement for those slots arbitrary. Except for the read/write memory cards, the cards in these eight slots can be interchanged to reassign processor bus control priorities as desired, with the bus control priority grant function being passed in card slot sequence from the highest-priority slot (1A1XA1) toward the lowest-priority card (graphic controller 1A1XA7). Relocatable cards must be placed in adjacent slots (1A1XA5, 1A1XA4, 1A1XA3, etc., in that order); leaving any one of these slots vacant would break the priority chain, which could result in unit malfunction. The read/write memory cards are passive circuits that are accessed by the processor bus but do not seize bus control. The grant signal is passed directly through a read/write memory card.

NOTES

1. Technical Manuals for Display Indicators:

   Mitsubishi C6911, C6912 and C3910

2. Technical Manual for Model 5783/5784 Keyboards: H-79-0363.

3. Technical Manual for Model 5781 PHOTOPEN: H-78-0042.

4. Technical Manual for Model 5786 Trackball/ 5787 Forcestick: H-78-0044. For SIMPLE-2 Data Tablet, see Talos Manual 50114-1.

5. Technical Manual for Model 631 Dunn Color Hardcopy Unit.

   Technical Manual for Model 4632 Tektronix Hardcopy Unit.

6. For Software instructions, see G8 Program Reference Manual.

7. Alignment Procedures:

   Timing Module, Paragraph 5-5.

8. Technical Manuals for Power Supplies:

   Model MM23-E0647/115
   H-80-0087

   If other models are used, appropriate manuals will be provided.

9. Before replacing a board, check switch settings against the configuration document.

H-81-0027-091

Figure 5-3. Troubleshooting Flow Diagram (Sheet 1 of 4)

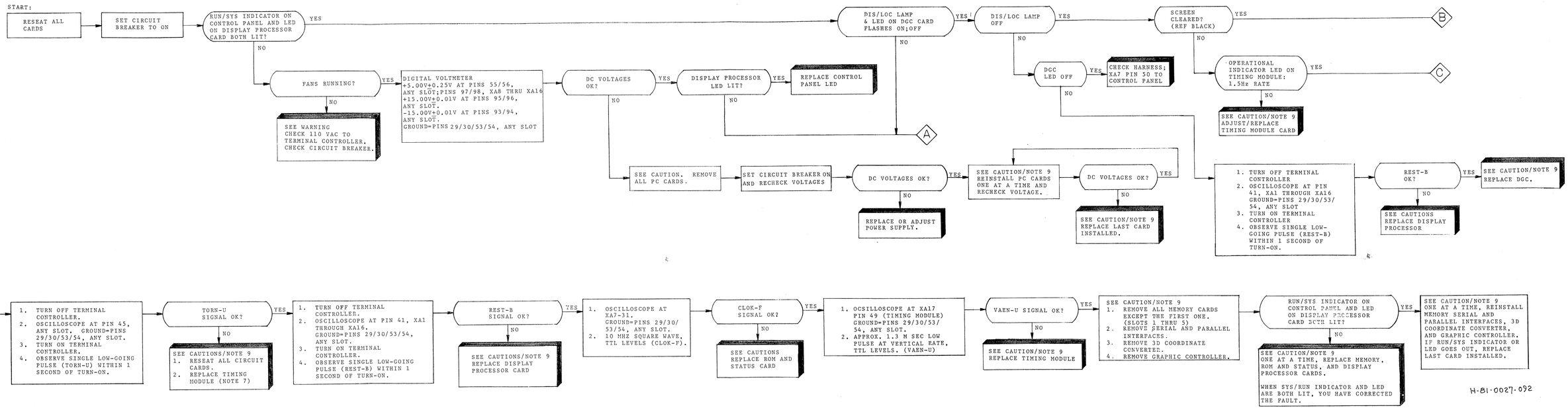


Figure 5-3. Troubleshooting Flow Diagram (Sheet 2 of 4)

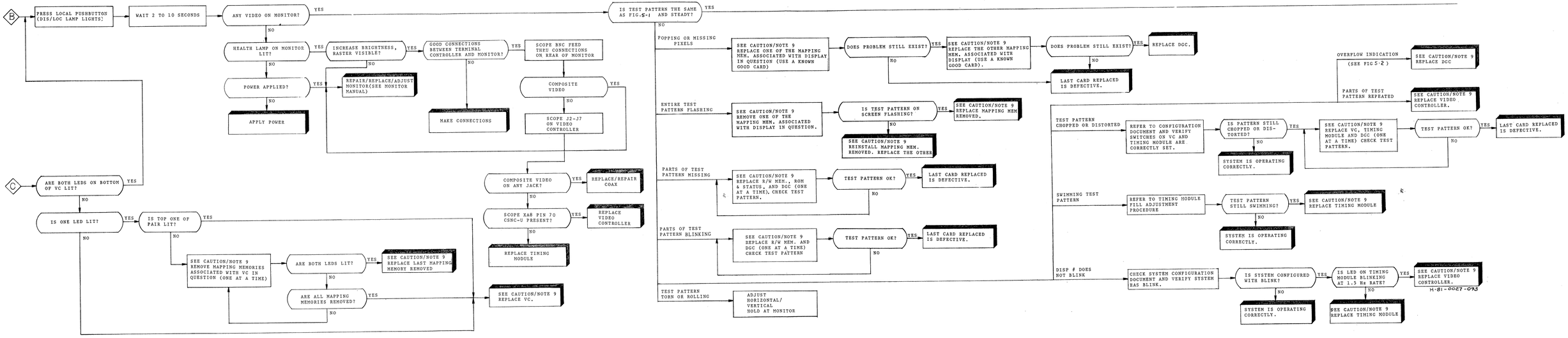


Figure 5-3. Troubleshooting Flow Diagram (Sheet 3 of 4)

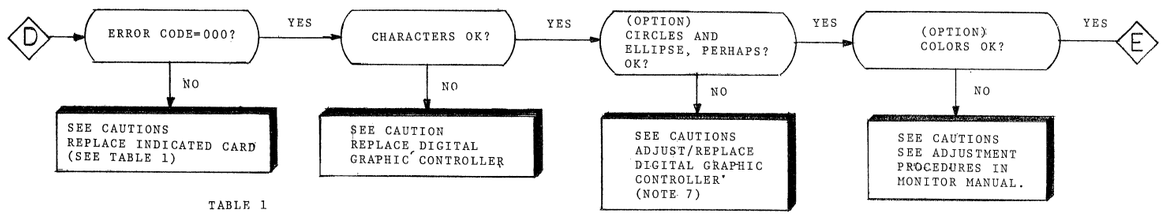


TABLE 1

ERROR CODE IS 3-DIGIT CODE THAT REPRESENTS THE FOLLOWING 8-BIT BINARY CODE.

FIRST DIGIT MSB		SECOND DIGIT			THIRD DIGIT		LSB
7	6	5	4	3	2	1	0

- NOT USED
- NOT USED
- 3D COORDINATOR CONVERTER
- PARALLEL INTERFACE DIAGNOSTIC
- SERIAL INTERFACE DIAGNOSTIC
- READ/WRITE MEMORY DIAGNOSTIC
- DISPLAY PROCESSOR DIAGNOSTIC
- GRAPHIC CONTROLLER DIAGNOSTICS

WHEN A DIAGNOSTIC ROUTINE DETECTS AN ERROR, THE BIT CORRESPONDING TO THAT TEST IS SET TO A 1. IF NO ERROR OCCURS, IT IS SET TO 0.

IF SYSTEM DOES NOT CONTAIN ONE OF THESE CARDS, THE DIAGNOSTIC ROUTINE CONSIDERS IT AN ERROR AND SETS THE ERROR BIT; E.G., IF 3-D COORDINATE CONVERTER IS NOT USED, THEN SECOND DIGIT OF ERROR CODE IS 4 OR LARGER.

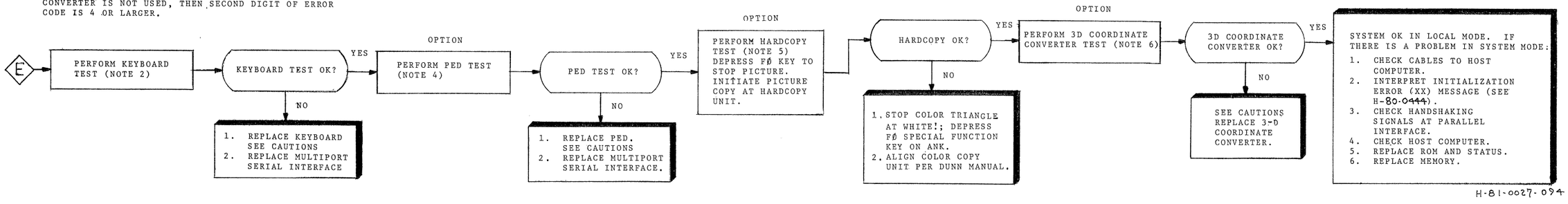


Figure 5-3. Troubleshooting Flow Diagram (Sheet 4 of 4)

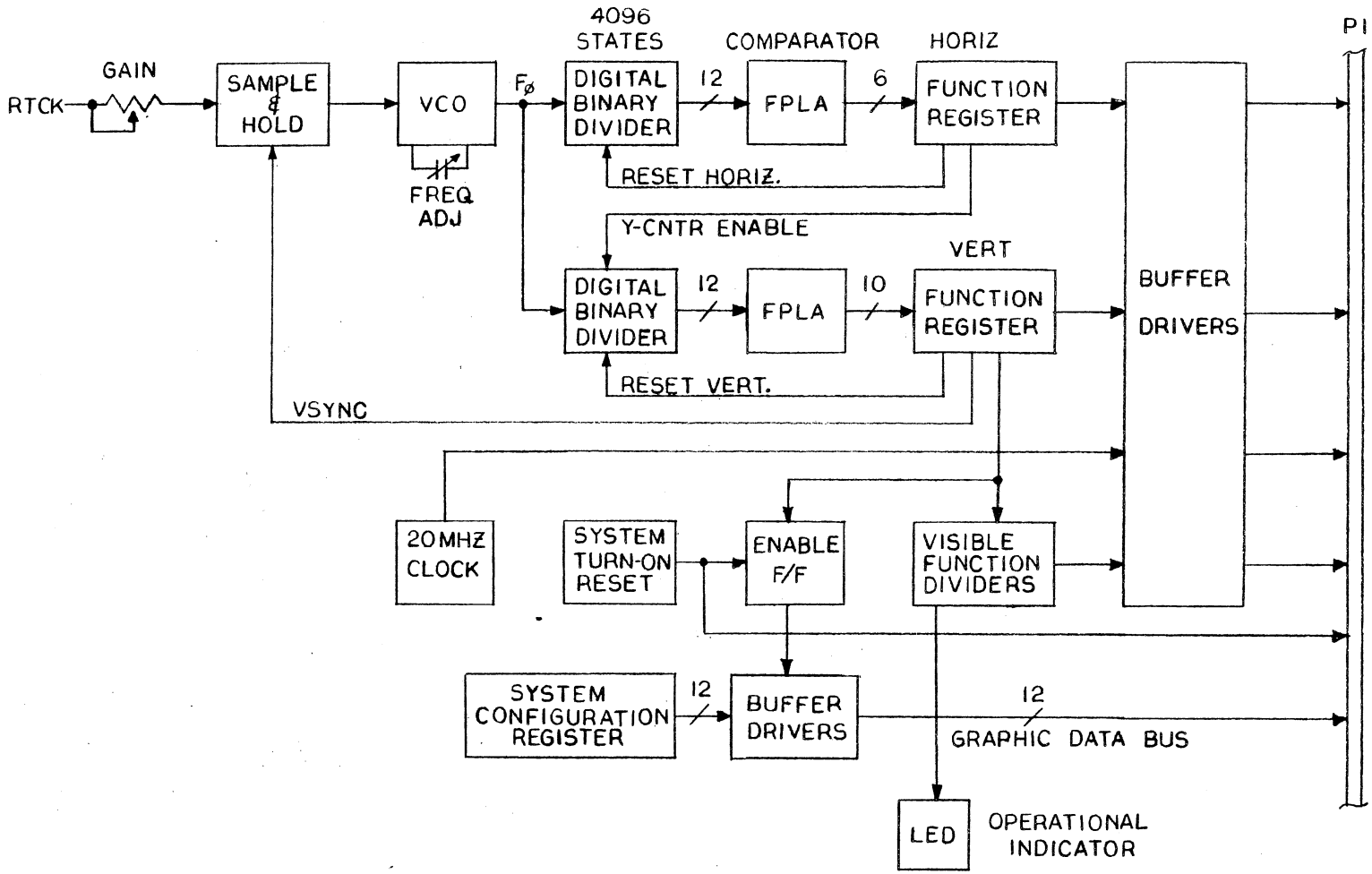


Figure 5-4. Timing Module

5.5 ADJUSTMENTS

The timing module is the only card in the terminal controller requiring adjustment. The timing module is basically a phase-locked loop that locks to the line frequency or an external input. The line frequency may be 50 Hz or 60 Hz. Figure 5-4 shows the basic operation of the timing module.

The VCO frequency is approximately 45 MHz. Binary dividers reduce this frequency to VSYNC, which is phase-locked to the line frequency.

A light-emitting diode on the edge of the timing module blinks at a rate of 1.5 Hz, indicating that VSYNC is present and functioning correctly. If this indicator is either off or steady on, there is a problem with the phase-locked loop. Blinking at a rate slower than 1.5 Hz indicates improper lock, or that the line frequency is lower than 60 Hz.

Before adjusting the timing module, check that the configuration switches are properly set (refer to drawing 5977170 in H-81-0097).

Adjust the timing module as follows:

1. Set gain potentiometer R43 fully counterclockwise (maximum gain).

2. Open switch U30-S2.

3. Adjust offset potentiometer R42 for -8V at TP6.

4. Using oscilloscope, observe waveform VSYNC at J7. Sync internally and observe pulse output. The signal on the oscilloscope should have a pulse duration of 90 us at the line frequency. Adjust C24 for the most stable display. (Pulse period is 16.6 ms for 60 Hz line, 20 ms for 50 Hz line.)

5. Change oscilloscope sync to line. Adjust C24 to minimize movement of the signal on the oscilloscope.

6. Close switch U30-S2. The signal displayed on the oscilloscope should lock and be stable.

7. On second trace of oscilloscope, observe signal at TP6. This signal should be a triangular-shaped wave, centered around -8V, with a peak-to-peak amplitude of approximately 1V. The VSYNC waveform should track about midway on the rising edge of the triangle.

8. Adjust R42 as necessary to center VSYNC on the rising edge of the triangle. Leave R43 set for maximum gain.

9. Verify operation of all I/O signals against table 5-1.

Table 5-1. Timing Module

PIN/ TERM.	SIGNAL NAME	DESCRIPTION
P1-1 P1-2 P1-3 P1-4 P1-5 P1-6	DB00+H DB01+H DB02+H DB03+H DB04+H DB05+H	Bidirectional data line, exclusively raster bus, TTL levels, timing module output configuration switch settings to these lines for a short period after TORN goes high.
P1-7 P1-8 P1-9 P1-10 P1-11 P1-12	DB06+H DB07+H DB08+H DB09+H DB10+H DB11+H	Bidirectional data line, exclusively raster bus, TTL levels, timing module output configuration switch settings to these lines for a short period after TORN goes high.
P1-43 P1-44 P1-46 P1-48	GCMK+H GRAS-H GCAS-H GRMK+H	Timing module provides only a pull up to these bus signals.
P1-37	EXTR-	TTL level input. When this signal is low, TORN-U will be low and a system reset will result.
P1-33	6.3 VAC	6.3 volt RMS sine wave derived from the AC power source.
J1	VIDEO 2 IN	Video input to a wideband variable gain amplifier.
J3	VIDEO 1 IN	Video input to a wideband variable gain amplifier.
P1-31	20CK+U	TTL square wave 50% duty cycle $\pm$5% at 20 MHz.
P1-52	RTCK-U	TTL square wave 50% duty cycle $\pm$5% at AC line rate.
P1-45	TORN-U	TTL pulse which is low for approximately 500 ms after power turn on. Signal then goes high and remains so until system power down or EXTR- active low input.

Table 5-1. Timing Module (Cont)

PIN/ TERM.	SIGNAL NAME	DESCRIPTION
P1-27 P1-28	SCLK-U SCLK+U	ECL square wave 50% duty cycle at pixel rate (balanced output).
P1-25 P1-26	SHLD SHLD	Grounding point for SCLK-U and SCLKT-U bus strip shield.
P1-36	CCLK-U	TTL square wave 50% duty cycle at approximately 3.5 Hz.
P1-40	BLNK-U	TTL square wave 50% duty cycle at 1.5 Hz.
P1-15	ODDF+U	TTL square wave 50% duty cycle at one half the vertical rate.
P1-47	VAEE-U	TTL pulses active low for approximately 1250 usec at the vertical rate.
P1-49	VAEN-U	TTL pulses active low for approximately 1250 us at the vertical rate.
P1-69	VBLK-U	TTL pulses active low for approximately 1250 usec at the vertical rate.
P1-73	HBLK-U	TTL pulses active low for 7 us at the horizontal rate.
P1-70	CSNC-U	TTL pulses derived from H SYNC, V-DRIVE, SERRATION, and VSYNC signals.
J5 J6	CSYNC HSYNC	AC coupled TTL line driver output, polarity is determined by a switch setting.
J7	VSYNC	AC coupled TTL line driver output, polarity is determined by a switch setting. Alternately VDRIVE can be routed to this output by a switch setting.
J2	VIDEO 2 OUT	Amplified video output.
J4	VIDEO 1 OUT	Amplified video output.

5.6 REPAIR

Repair consists of replacing circuit cards or chassis-mounted electrical assemblies suspected of being faulty, based on the troubleshooting analysis (figure 5-3).

CAUTION

Always turn off terminal controller before removing or installing any circuit card.

Always turn off terminal controller and pull power plug before removing any chassis-mounted component.

5.6.1 CIRCUIT CARD REPLACEMENT. To remove a circuit card assembly, grasp the two card extractor handles, exert outward pressure to disengage the card from its connector, and pull straight out of card cage.

Before installing a circuit card assembly, verify the part number of the card. Insert the card (component side to the left) into its slot in the card cage. Engage it with its connector by exerting firm inward pressure.

5.6.2 CHASSIS-MOUNTED COMPONENTS. Chassis-mounted assemblies are secured with standard mounting hardware, and can be removed and replaced using common hand tools.

Refer to the appropriate separate manual for maintenance of the terminal controller power supply.

5.6.3 SPECIAL HANDLING FOR MOS DEVICES. MOS devices are subject to damage caused by static charges. Assemblies that contain MOS devices are the mapping memories and timing module. When not installed in the card cage, these assemblies should be stored in black Velostat bags with the MOS warning statement printed on the outside of the bag.

CAUTION

Always handle these cards only by the card extractors or by the connector. Avoid touching the card components or the printed circuit.

APPENDIX A

RELATED PUBLICATIONS

The following listed publications apply to options that may be added to a GRAPHIC 8 system. The manual number listed in the manual's basic number. Revisions are indicated on the cover of the manual by a letter following this basic number.

MANUAL NO.	TITLE
H-79-0350	Model 5753 2-D/3-D Coordinate Converter User's Manual
H-79-0450	Model 7750 Expansion Module Technical Manual
H-78-0115	Model 5716 Parallel Interface to SEL32; HSD-9132
H-78-0343	Model 5719 Parallel Interface to Data General NOVA and ECLIPSE
H-79-0353	Model 5721 Parallel Interface, NTDS Slow
H-79-0354	Model 5722 Parallel Interface to Honeywell 516 DMC
H-79-0363	Model 5783 Alphanumeric Function Keyboard/Model 5784 Lighted Alphanumeric Function Keyboard
H-78-0044	Model 5786 Trackball/Model 5787 Forcestick Entry Devices Technical Manual

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