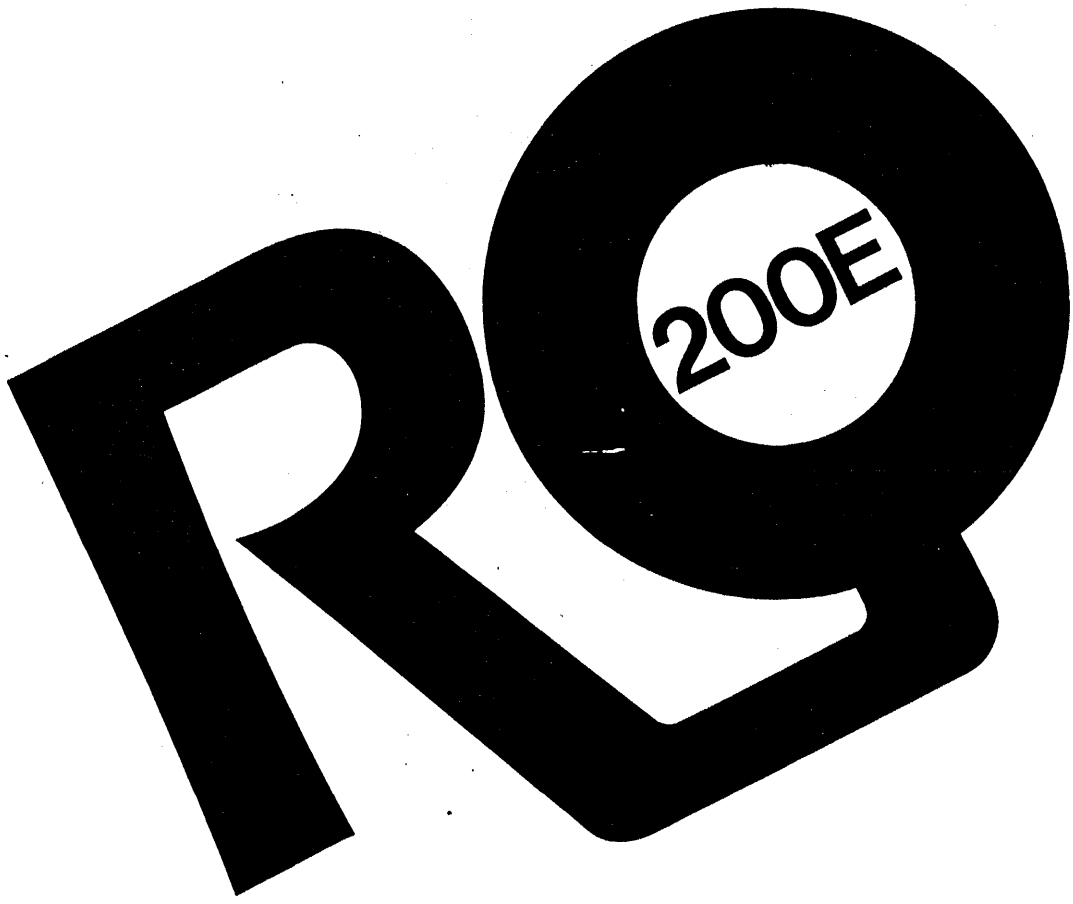
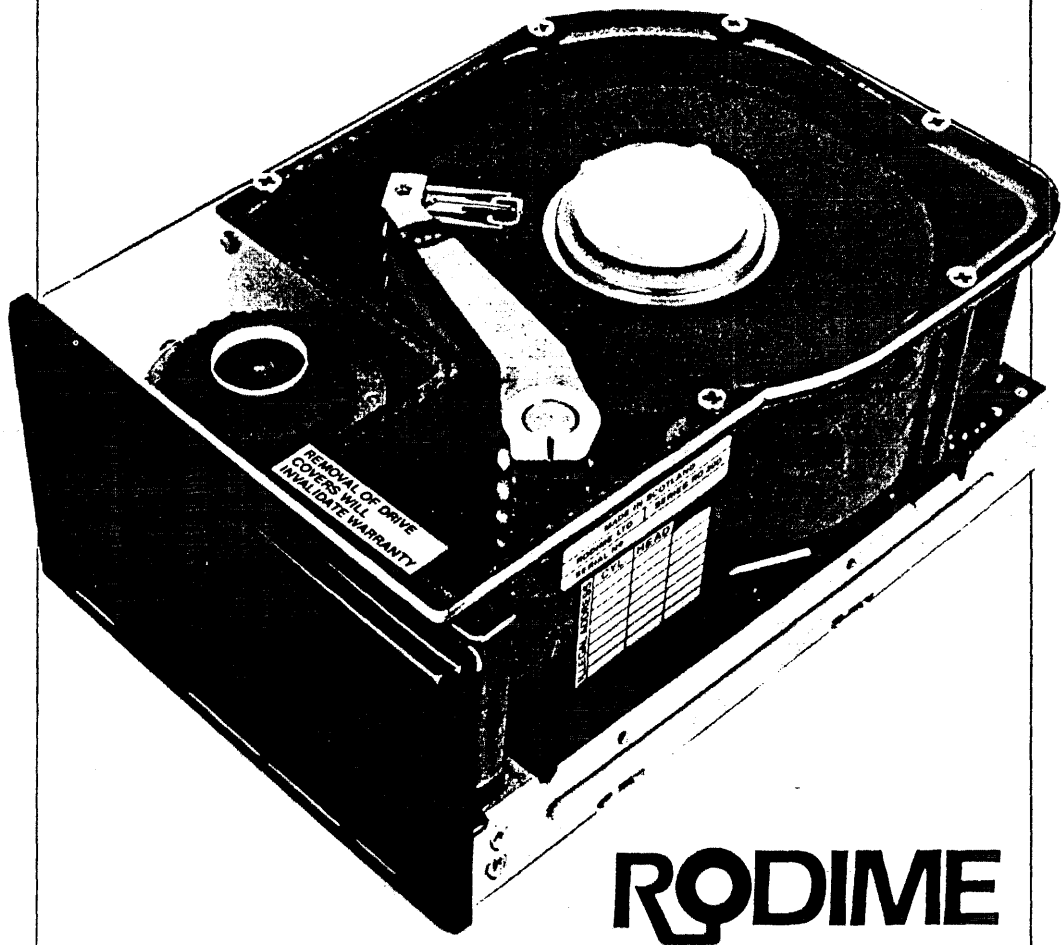
RODIME 200E series 5¼ winchester disk drive
user manual



RODIME 200E series 5¼ winchester disk drive user manual P/N USM0038 Revision A



RODIME

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The purpose of this manual is to provide the user of the RO 200E series disk drive with more technical help and information than is available in the product and interface specifications. However it should be emphasised that these latter documents, PRO-0033 and INT-0034 are definitive. Rather, this manual gives practical advice on drive usage as well as engineering background on function and design.
Part A: User Guide introduces the drive in section 1 and lists controller suppliers. Section 2 gives information on installation into a system. Powering up the drive, description of fault codes and assistance in trouble-shooting are given in section 3 while section 4 is devoted to repair and maintenance.

Part B: Product Description is aimed at providing a technical introduction to the drive design. Sections 5 to 9 deal with the mechanical configuration, the function of the electronic circuitry and features of the microprocessor firmware.

Two appendices list patents applied for and a recommendation to controller designers of a write-precompensation scheme.

Further help is readily available from Rodime customer support engineering and this can be obtained by contacting either the appropriate Sales Office, or by direct contact with the main plant in Glenrothes.

Rodime's dedicated policy is to ensure customer satisfaction with both the product and its service and in order to maintain this, any suggestion for improvement to this manual or our service is welcome and should be made directly to me at the Rodime Plant in Glenrothes.
Rodime — right from the beginning.

Malcolm F. Dudson
DIRECTOR OF MARKETING

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PART A
user guide

1. INTRODUCTION

1.1 General

The Rodime RO 200E series of 5¼ inches (130mm) Winchester disk drives provides fast access data storage for use with small business computers, terminals and microprocessor based systems. There are four models in the series, RO 201E, RO 202E, RO 203E and RO 204E containing 1, 2, 3 and 4 magnetic disks respectively and ranging in total data storage from 13 to 53 Megabytes. The drive outline is shown in figure 1.

The drive is a microprocessor based device which receives and transmits MFM (modified frequency modulation) data, seeking the appropriate track in response to step commands across the disk control interface. The drive is soft sectored and is connected to the host system via a disk controller which is responsible for formatting, MFM encode and decode to NRZ, block address decode, CRC generation and verification and so on. Typical format schemes with 256 data bytes per sector and 32 sectors per track can realise an efficiency of about 80% giving formatted capacities up to about 42 MB.

Dimensions, mounting details and voltage requirements (DC voltage only) are the same as standard 5¼ inches floppy disk drives. The microprocessor is responsible for the control of the stepper motor used for head positioning. Fast seek times are achieved by means of programmed velocity profiles and microstepped velocity feedback damping routines. Automatic thermal compensation has been designed into the head positioning mechanism. A brake is provided as standard for the main DC disk motor and this permits shipment of the Rodime drive in a terminal or system provided it has been mounted in accordance with the correct procedure (see section 2). A further solenoid brake for the actuator can be supplied as an optional extra. The microprocessor also monitors certain fault conditions in the drive and should one

occur, flashes the corresponding fault code on a red LED indicator on the front panel.

A significant feature of the RO 200E-series is that boards are interchangeable without the use of oscilloscopes or other setting up equipment. This is made possible by the fact that there are no select-on-test components and no adjustments on the boards whatsoever. This, of course, in addition gives added reliability which is further emphasised by the fact that there are no mechanical adjustments.

Several engineering features are subject to patent application and these are listed in Appendix 1.

1.2 Specifications

Full specifications of the RO 200E series disk drive are given in two documents:-

PRO-0033 (Product specification)
INT-0034 (Interface specification)

A summary of the important performance parameters is given below:-

Product specifications

Models:	RO 201E, 202E, 203E, 204E,
Disks	: 1, 2, 3, 4
Heads	: 2, 4, 6, 8
Unformatted capacity (M bytes)	: 13.33, 26.66, 40.00, 53.33
Formatted capacity (typical)	
Per drive (M bytes)	: 10.49, 20.97, 31.45, 41.94
Per track (bytes)	: 8192
Per sector (bytes)	: 256
Sectors per track	: 32
Cylinders	: 640
Transfer rate (M bits/s)	: 5
Seek times (ms) (including settling)	
Track to track	: 8
Average	: 55
Maximum	: 130

Average latency (ms)	: 8.3
Flux reversals per inch (max)	: 10,200
Tracks per inch	: 600
Rotational speed (r.p.m.)	: 3600
Power requirements (DC only)	: 5V (±5%) at 0.65A typical
(see para 2.5)	: 12V (±5%) at 2A typical (10%, 4A motor start)
Dimensions (inches)	: 8.00 x 5.75 x 3.25
Operating environment	: 10° C to 50° C 10%RH to 85%RH (non-condensing)
Vibration	
Operating	: .006 inch displ., 5-60 Hz 1g pk accln., 60-500 Hz
Non-operating	: .040 inch displ., 5-30 Hz 2g pk accln., 30-500 Hz
Shock	
Operating and non-operating (without transit lock)	: 3g pk, less than 10ms, max 2 per second.
Non-operating (with transit lock)	: 30g pk, less than 10 ms, max 1 per 10 second
Interface	: ST506 variant of SA1000 (see section 1.3 and 1.4)

1.3 Connectors The RO 200E drive interfaces to host systems via the ST506 interface which has become an accepted standard for 5¼ inch Winchester disk drives. There are separate connectors for data (in MFM code), for control lines and for DC power. The connector positions are shown ing Figure 1 and the connectors themselves are defined in Figures 2, 3, and 4. The corresponding control, power and data interfaces are given in Figures 5 and 6. A chassis ground tab is also provided. The convention for control is that a TTL logical zeros is true and a TTL logical one

is false. Up to four drives may be connected to a host system and each drive is provided with a four-hole switch for selection. The control lines may be daisy-chained but the data lines must be radially (individually) connected to the host (see section 2).

Control signals for the drive are provided via a 34 pin edge connector (P1/J1). The pins are numbered 1 through 34 with the even pins located on the solder side of the board. Pin 2 is located on the end of the board connector closest to the DC power connector and is labelled. A key slot is provided between pins 4 and 6. The recommended mating connector is AMP ribbon connector A/N 88373-3.

Radial connection of read/write data signals is provided via a 20 pin edge connector (P2/J2). The pins are numbered 1 through 20 with the even pins located on the solder side of the board. The recommended mating connector is AMP ribbon connector A/N 88373-6.

DC power is provided by a 4 pin AMP Mate-N-Lok connector (P3/J3) P/N 350211-1 mounted on the component side of the board. The recommended mating connector is AMP P/N 1-480424-0 utilising AMP pins P/N 350078-4.

A ground connection is provided via a "Faston" connector AMP P/N 61664-1 located on a metal stand-off on the chassis between the power and control signal connectors. However, the DC and chassis grounds are common on the drive and the use of the "Faston" connector is not essential. Wiring should be in accordance with Figure 5. The frame ground of the host system should be properly earthed.

1.4 Controllers The following 5¼ inch Winchester Disk Controllers are known to operate with the RO 200E series disk drive. In general, any controller which will operate with the RO 100 and RO 200 series disk drives will also operate with the RO 200E series disk drive. However, the controller must be able to address up to 640 cylinders and set the STEP interval in the

range 5 μs to 5 ms. Further information is available from the Rodime Marketing Department or from the controller manufacturers themselves..

Xebec S1410 : Microcomputer Systems Corp, PO Box 512, 432 Lakeside Drive, Sunnyvale, California 94086 (408) 773 4200, (408) 735 1340.

Western Digital WD 1000 : Western Digital Corp, Newport Beach, California 9266 (714) 557 3550.

DTC 510, DTC 520 : Data Technology Corp, 2775 Northwestern Parkway, Santa Clara, California (408) 4960434.

Konan — David Junior : Konan Corp, 1448N 27th Avenue, Phoenix, Arizona 85009 (800) 528 4563

1.5 Illegal Address Map

Each drive is accompanied by a map indicating the addresses of sectors which should not be used. This map (label) is fixed to the base casting wall. These illegal sectors have been identified during unit test in the factory and contain a repeatable disk defect, greater than one bit in length. No such illegal address will exist in cylinders 0, 1 and 2.

An illegal address is specified by cylinder, head and sector. It should be noted that the format used for this purpose is 33 sectors of 256 bytes each. The maximum number of illegal addresses is:-

Model Number	201E	202E	203E	204E
Max number of illegal addresses	4	8	12	16

2. INSTALLATION

2.1 Shipping lock

The stepper motor shipping lock is a label fixed to the top cover of the drive and covering a plastic pulley on the stepper motor shaft, thus preventing movement of the read/write heads across the disk surfaces.

This label must be removed prior to power-on.

Warning: Once the label is removed the stepper motor shaft should never be rotated by hand since this could lead to head/disk damage.

Note: This label is not present on units which are fitted with the automatic stepper motor lock. This lock also releases on application of 12V.

2.2 Step rate

The drive can accept step pulse intervals over a range from 5 μs to 5 ms. If the interval is in the range 5 μs to 130 μs, then the drive is operated in the ramped seek mode. The seek operation will begin if 32 step pulses have been received or 180 μs has elapsed since the last step pulse was received. In this mode of operation, the access times will vary with step interval. The access times quoted in paragraph 1.2 are for a step interval of 10 μs. If the step interval is in the range 130 μs to 5 ms, then the drive step rate will vary with step interval. Consequently. the access times are not specified.

2.3 Mounting

Side brackets with tapped holes are provided with each drive and permit base or side mounting, see Figure 7. These brackets are fixed to the drive chassis via shock-absorbing grommets. The drive may be oriented in any axis. When installing into an enclosure at least 0.1 inch clearance must be maintained around the entire drive to allow vibration isolation and to prevent obstruction of the breather filter and the creation of ground loops.

2.4 Multiple drive configuration

Up to four drives may be connected to one host in a "daisy-chain" fashion. A 4-pole drive select switch is fixed to each drive, (See Figure 1). To identify a drive as number 1, close the first pole of this switch nearest the terminator pack.

Similarly for drives 2, 3 and 4. Only one pole should be in the closed position. All "daisy-chained" drives should have the line terminator pack removed except for the last drive in the chain. All drives are supplied for single usage, that is, pole 1 is closed and the terminator pack is present. (See Figure 1).

Note that, in the multiple drive configuration all data interface lines are radially connected to the host. Figure 8 shows a four drive configuration.

2.5 Power requirements

The drive requires DC voltages only.

VOLTAGE	CURRENT		
	Typ	Max	Peak During Power-up
+5V ± 5%	0.65A	0.75A	
+12V ± 5%	2.0A	2.4A	4A

No damage will result if power is applied or removed in any order. However, to avoid tripping the fault detection circuitry two conditions must be met:

2.5.1. 5V risetime must not exceed 1 second.

2.5.2. 12V must follow the 5V within 5 seconds if the 5V is applied first.

2.5.3. When checking the power supplies, the following loads should be used:

For the 12V supply, the power-up current may be measured using a standard load of 3 ohms in series with 1 mH and the operating current may be measured using 5 ohms in series with

1mH. With a 7 ohm resistive load on the 5V supply and the above loads on the 12V supply, noise and ripple should not exceed 100 mV peak to peak up to 500 Hz and 50 mV peak to peak from 500 Hz to 5 MHz.

In operation, the maximum rate of change of the 12V load due to the disk drive is 8A/ms.

2.6 Indicators

Two red LED's fixed to the master electronics board are visible through the facia when they are illuminated.

2.6.1. The "Power-On" LED is on when the drive is READY with no error condition present. It is also used to indicate fault conditions in the drive.

2.6.2. The "Select" LED is on when the drive is selected by the host provided the "Power-On" LED is on.

The "Power-On" LED is positioned closest to the centre of the facia. Note that this LED will not come on if the condition 2.5.1, 5V risetime, is not met since the microprocessor will not receive an initial reset.

3. FAULT FINDING

3.1 Front panel fault codes

The "Power-On" LED is used to flash error messages should certain fault conditions arise on the drive. A four bit binary code is used (long flash = logical 1, short flash = logical 0) with the most significant bit occuring first:

e.g. short, short, long, short = 2 (0010)

Fault Code 1 (0001) : No index track data burst.

Fault Code 2 (0010) : No Flag zero

Fault Code 3 (0011) : Motor speed outside ±1% tolerance at end of power-up sequence.

Fault Code 4 (0100) : Motor speed outside ±10% tolerance in normal operation.

Fault Code 5 (0101) : Flag zero stays TRUE.

Fault Code 6 (0110) : STEP received while WRITE GATE is TRUE.

Fault Code 7 (0111) : WRITE FAULT.

Fault Code 8 (1000) : Not used.

Fault Code 9 (1001) : Not used.

Fault Code 10 (1010) : No index.

Fault Code 11 (1011) : Motor not up to speed.

Fault codes 1, 2, 3, 5, 10 and 11 are monitored during the initial power-up sequence of the drive. The remaining codes, namely 4, 6 and 7 are constantly monitored during normal operation. All fault codes are latched by the processor and the drive must be restarted to clear. Codes 3, 4, 10 and 11 generate an interface WRITE FAULT as do those fault conditions leading to code 7.

3.2 Fault codes at power-up

From power-on to drive READY the microprocessor performs a number of checks and calibrations on the drive. Should any of these checks fail the drive will not come READY and the microprocessor will flash the appropriate fault code on the front panel. The power-up routine is shown in Figure 19.

3.2.1. Codes 10, 11. The microprocessor checks for an INDEX pulse (Hall sensor output) from the DC motor. If this does not occur during a period of 8 seconds, then fault code 10 is displayed. Since this condition is likely to be the result of the DC motor not starting, the microprocessor attempts to reduce head/disk static friction during the period of 8 seconds by moving the positioner.

Note that a WRITE FAULT condition removes power from the DC motor thus preventing thermal damage.

The DC motor speed is then checked to within ±1% of 3600 rpm. Each check takes one motor revolution and during this time the power-on LED is flashed at intervals of approximately 0.5 second. If the processor does not see 4 consecutive speed samples correct to ±1% within 25 seconds it will display fault code 11.

3.2.2. Codes 5, 2. When the speed check is successfully completed, WRITE FAULT interrupts are enabled. The microprocessor then begins the recalibration of the actuator to track zero. The exact routine is shown in Figure 20. Two possible fault codes may occur. If flag zero does not go false within 25 steps towards the centre of the disk, fault code 5 will be displayed. After going false, if flag zero cannot then be set true within 800 steps in the out direction, fault code 2 is displayed.

3.2.3. Codes 1, 3. After calibrating the actuator to track zero, the processor initiates the routine for selecting the correct INDEX pulse (see section 6.6 for an explanation of INDEX). The actuator is moved to track −2 to find the index data burst on head Ø and so select the corresponding Hall sensor phase, thus establishing INDEX. Failure to complete this operation, results in fault code 1 provided link A is present and is ignored if link A is cut. The actuator is then re-positioned on track zero and a final check made on the DC motor speed, again to ±1%. Should this fail, fault code 3 is displayed.

At the successful completion of the power-up routine, READY and TRACK ZERO are both set true and the head selects are enabled.

3.3 Fault codes during operation

During normal operation of the drive, fault codes 4, 6 and 7 may be displayed.

3.3.1. Codes 4, 6. While the processor is waiting for a step pulse from the interface it continuously monitors the DC motor speed. Should the speed vary from nominal by more than +10% or −5%, fault code 4 will be displayed. The processor will not allow a step pulse to be received while WRITE GATE is true. This is considered to be a catastrophic controller fault. The drive returns WRITE FAULT status and displays fault code 6.

3.3.2. Code 7: WRITE FAULT. On receipt of a WRITE FAULT interrupt from the drive's hardware detection circuitry the processor latches this condition, delays for 2 seconds and samples the hardware input to check if the WRITE FAULT condition still exists. If it does, fault code 7 is displayed. If not, the processor enters the power-up routine thus setting the actuator to track zero. See Figure 21.

In the above sense, fault code 7 represents a static WRITE FAULT status. There are nine fault conditions which cause. WRITE FAULT to be true. One is defined above in 3.3.1. These are related to read/write heads, namely:

- no write current in any head when WRITE GATE and DRIVE SELECTED are both true
- more than one head selected
- no write data transitions when WRITE GATE is true

One relates to the DC supply, namely:

- 12V supply lower than about 10.0V

The remaining four are abnormal motor conditions as detailed by fault codes 3, 4, 10 and 11.

In practice, it is likely that the vast majority of WRITE FAULT conditions are caused by power supply transients. Thus, the 2 second delay and re-check allows a fast transient to be recognised but the condition is not latched if the re-check is successful. The controller will receive TRACK ZERO and READY status and can repeat the command which had to be interrupted.

3.4 Fault diagnosis

A table showing likely causes of the fault codes is given below. The simplest action to take is that of replacing either the master board or the motor speed board and verifying if the fault code persists. However, a set of diagnostic routines is presented which determine more accurately the cause of each fault code. A voltmeter or oscilloscope and the "TRACKER" exerciser (see section 3.5) are needed for this investigation. The causes of fault conditions other than those given by the fault codes may be more difficult to trace. In practice, the most likely sources of trouble are (a) power supplies not meeting specification and (b) step rates outside the drive constraints (section 9.1). This presumes that the host controller meets the requirements of the Rodime interface specification INT-0034.

In any event, it should be verified that **the shipping label is removed,** the connectors are clean and properly attached, the interface terminator is present or absent according to the configuration, the drive chassis is clear of any system metalwork, the DC power lines are short twisted pairs and data and control cables are preferably shielded and do not run close to high current switching circuits.

3.4.1. For each fault code a possible cause is indicated in the Fault Table by a letter. This is used in the Diagnostics Table for idenfification.

Fault Table

Fault Code	Possible Causes	Action
1	A: Faulty flag zero position	Contact service organisation
	B. Fault in data burst detection circuitry	Replace master board
	C: Fault in head Ø or pre-amp board	Contact service organisation or replace pre-amp board
	D: Data burst erased	Rewrite with "TRACKER"
2,5	E: Transit lock label not removed/faulty stepper lock option (if fitted)	Remove label/check stepper lock solenoid
	F: Connector fault between motor speed board and stepper motor/flag zero assembly	Check connector and/or replace motor speed board
	G: Short circuit between motor speed board and casting	Reassemble board
	H: Faulty flag zero transducer	Contact service organisation
	J: Fault in stepper motor control circuitry	Replace master board
	K: Fault in stepper motor control circuitry	Replace motor speed board
	L: Faulty stepper motor	Contact service organisation
	M: Defective positioner assembly	Contact service organisation

Fault Code	Possible Causes	Action
3,4, 10,11	N: Brake failure	Replace
	P: No 12V supply	Check supply/ connector
	Q: Faulty DC motor/ Hall element	Contact service organisation
	R: Faulty motor speed board	Replace
6	S: Controller/Interface fault	Check controller/ connector
	T: Faulty master board	Replace
7	U: Faulty master board	Replace
	V: Faulty pre-amp board	Replace
	W: 5V and/or 12V too low	Check supply

3.4.2 A numbered set of checks is given for each fault code displayed on the front panel. The action after each test is indicated by a number or a letter. The number refers to another check, normally the next, shown for that fault code in this table. The letter refers to the determined cause as given in the previous table.

Diagnostics Table

Fault Code	Procedure	Test is faulty? Yes	No
1	1. Cut link A to let drive become ready.		2

Fault Code	Procedure	Test is faulty? Yes	No
	2. Use "TRACKER" to check on IC9/14 that flag zero switches between tracks 2 and 5.	A	3
	3. Use "TRACKER" to re-write date bursts, replace link and retest.	4	D
	4. Replace master board, re-write data bursts and retest.	C	B
2,5	1. Check if transit lock label is removed. /Check stepper lock Solenoid (if fitted).	E	2
	2. Remove connector J8 from motor speed board and check for 14 ohm between J8/6 and J8/7, J8/8 and J8/9.	3	4
	3. Check J8 crimp joints.	F	
	4. Check for diode between J8/11 and J8/10.	5	6
	5. Check J8 crimp joints.	F	H
	6. Check beneath motor speed board for shorts to casting.	G	7
	7. Replace master board and retest.	8	J
	8. Replace motor speed board and retest.	M	K
3,4 10,11	1. Check brake operation.	2	3
	2. Check 12V supply.	P	N
	3. Change link on motor speed board to use spare Hall element.	3	Q

Fault Code	Procedure	Test is faulty? Yes	No
	4. Replace motor speed board and retest.	Q	R
6	1. Check interface cables/ controller.	S	T
7	1. Test 12V to be in range 11.4V to 12.6V. Test 5V to be in range 4.75V to 5.25V.	W	2
	2. Replace master board and retest.	V	U

3.5 'TRACKER' exerciser

Rodime has developed a hand-held exerciser, the "TRACKER" which simulates a host controller and allows the user to exercise any 5¼ nch Winchester disk drive which operates via the ST 506 interface. It is a useful tool for checking a drive which is believed defective or which has been repaired. The "TRACKER" comes complete with interface connectors for data and control and with a 5V supply connector. It basically comprises a keypad for parameter and instruction input and six LED's for response.

It will perform the following commands:

- Recalibrate.
- Seek track Ø to 1023.
- Select head Ø to 7.
- Continuous seek between two tracks.
- Key selectable step rate (30 us to 25 ms in 100 us increments).
- Seek demonstration routine (random, planet satellite).
- Write pattern select (1F, 2F, DB Hex).
- Write/erase for one revolution.

- Write/erase for one surface (head).
- Continuous write.
- Check index track - 2.

This device would typically be used with an oscilloscope and allows actuator and head/media verification, for example.

It may be purchased direct from Rodime, and customers wishing to do so should contact the plant in Glenrothes or the appropriate Sales Office.

4. REPAIR AND MAINTENANCE

There is no preventative maintenance and there are no adjustments on the drive. Field repair is restricted to brake and board replacement and selection of the spare Hall sensor. Repair to the module can only be effected by use of Rodime special tooling and Class 100 clean room conditions. USERS ARE REMINDED THAT REMOVAL OF THE MODULE COVERS WILL RENDER WARRANTY VOID.

4.1 Tools

The tools required for field repair consist of:

- Supadriv screwdriver, number 1.
- Pozidriv screwdriver, number 2.
- Box spanner, ¼ inch AF.
- Hex driver (Allen) 5/64 inch.
- .015 inch feeler gauge.
- "TRACKER" exerciser (Optional).

4.2 Procedure

Access to the brake, pre-amplifier board and motor speed board is achieved firstly by removing the facia, then the master board and finally the side brackets.

4.2.1 **Master board replacement (time 5 minutes).** Using number 1 Supadriv, remove 4 screws holding facia and remove from drive. Using 5/64 inch Allen key remove the five (5) screws securing the board to the drive, and carefully lift the board free of the drive.

Disconnect the flat cable connector from the motor speed board.

Reassemble the replacement board in the reverse order ensuring that the pre-amp connector mates correctly with the pre-amp board, and the flat cable connector is correctly polarised.

4.2.2 **Brake replacement (time 10 minutes).** Remove the master board as described in 4.2.1 but do not disconnect the flat cable from the motor speed board. Disconnect the brake connector from the motor speed board.

Remove the two screws securing the brake to the casting using the number Pozidriv screwdriver, and remove brake..

Position the replacement brake and refit the screws loosely.

Place the .015 inch feeler gauge between the motor rotor and the brake pad and push the brake body such that the plunger fully depresses against its spring. Ensure that the centre line of the brake lines up with the motor centre and lock the screws. Reconnect the brake connector.

Reconnect the power connector ensuring correct polarisation.

Power up the drive with the master board lying alongside and check that the brake does not contact the motor rotor.

Power off and check that the stopping time is in the range 5 to 8 seconds.

Refit the master board as described in 4.2.1.

4.2.3 **Motor speed board replacement (time 10 minutes).** Remove the master board as described in 4.2.1.

Remove the three screws and stand-off securing the mounting brackets to the casting and carefully remove the side brackets.

Disconnect the brake, DC motor and stepper motor from the motor speed board.

Unscrew the rear stand-off and remove the motor speed board.

If the spare Hall element is to be connected this is achieved by removing the link on the motor speed board and reconnecting it as shown in Figure 9.

Reassemble the motor speed board in the reverse order ensuring correct polarisation of connectors, check that the ground contact is correctly positioned between the motor speed board and the casting.

4.2.4 **Pre-amplifier board replacement (time 30 minutes).** Remove the master board and side brackets as described in 4.2.1. and 4.2.3.

Desolder the flexible cables from the pre-amp board using solder wick and a fine tipped soldering bolt (maximum temperature 300°C). Care must be taken to minimise the heating of the flexible cables.

Remove the two (2) screws securing the pre-amplifier board to the casting and remove the pre-amp board.

Fit the replacement board to the casting using three (3) nylon washers behind each screw position.

Place the flexible cables over the pins on the board and solder using a fine tipped bolt.

Complete the reassembly as described in 4.2.3.

4.2.5 **Verification.** The Rodime hand-held "TRACKER" exerciser is a useful tool for verification of a repaired drive prior to final systems use. This device is more fully described in Section 3.5.

4.3 Spares holding.

It should be emphasised that the following figures are recommendations only and that it will be up to each individual customer to decide upon the appropriate spares holding.

Description	Part No.	Drives on site		
		1-99	100-250	>250
Master board assembly	ASY 5118	1	2	5
Speed board assembly	ASY 5083	1	1	2
Pre-amp board assembly	ASY 5116	1	1	1
Failsafe brake assembly	ASY 2072	1	1	2

Other spare parts such as bracket/facia assemblies, terminator packs, ground tabs and consumable items such as warning labels are also available.

4.4 Purchase of spares

Spare parts for use as a customer spares holding may be purchased directly from Rodime or from Rodime appointed distributors.

Spares may also be purchased on an exchange basis under which Rodime will supply a new or refurbished sub-assembly making a financial allowance on the returned unit.

Price lists may be obtained from Rodime, its sales offices or authorised distributors.

4.5 Repair services Rodime operates a repair service under which drives will be repaired for a standard service charge.

For drives which are out of warranty when this service is required, Rodime should be informed in writing of the suspected defect. If the drive is to be returned, a Return Authorisation number will be given. The drive should be packaged in the original shipping container and returned to Rodime or to the distributor from which the drive was purchased together with a full description of the fault condition.

If the original packaging has been mislaid, a suitable container may be purchased from Rodime or the distributor.

Rodime cannot assume any responsibility for damage incurred to the drive during the shipment and insurance is the responsibility of the customer.

Rodime will return the goods carriage collect and a charge will be made for any shipping container which Rodime may have to provide.

Further details of this service may be obtained from Rodime or its authorised distributors.

4.6 Return of drives under warranty Rodime Terms and Conditions of Trade include a warranty for a period of twelve months from date of shipment. The procedure for return of drives under warranty is as follows:-

If the drive fails within the first five days of operation please contact immediately the Marketing Department at Rodime or the distributor from whom the drive was purchased.

In the event of other problems Rodime, or the appropriate distributor, should be informed in writing of the suspected defect. If the drive is required to be returned a Return Authorisation Number will be given and the drive should be returned pre-paid. The same procedure as in 4.5 above applies.

If on examination the drive is proved defective under terms of the warranty, the drive will be repaired or replaced, at Rodime's sole discretion and returned to the customer at no charge. If the defect is found to be due to mis-handling or other causes, the drive will be treated as a standard repair and charged accordingly. If, on examination, no fault is found, the drive will be returned at the customer's expense. Rodime reserve the right to make a charge for testing and handling under these circumstances.

PART B
product description

5. MECHANICAL DESIGN

5.1 General

The important performance and reliability aspects of the RO 200E disk drive mechanical design may be summarised as follows:-

- Up to four disks in "mini-floppy" size compatible unit.
- Designed for easy assembly of heads and disks.
- Minimum number of components to maximise reliability.
- Two chamber principle with heads/media in one and actuator mechanisms in the other.
- Low inertia positioner for reliability and fast access.
- Geometry designed to minimise head yaw.
- Drive components designed to compensate for thermal head/disk movement.
- DC brushless motor with ferrofluidic seal and integral ventilated hub.
- Breather filter positioned to equalise pressure across DC motor bearing.
- Air flow designed to locate drive components upstream from re-circulating filter and downstream from heads/media thereby creating an optimum purge cycle.

5.2 Rotary actuator

The positioning system consists of a stepper motor which drives a tensioned steel band via a pulley. The band in turn moves a drive arm which is attached to a shaft. The shaft rotates in a bearing system and moves the head arms across the disk. Simplicity of components ensures easy assembly and reduces failure risk.

The two phase stepper motor operates in a fractional-step mode under microprocessor control (0.45° per track).

5.2.1 **Stepper Load.** The positioner has low inertia to provide

fast seek times (maximum velocity 7000 tracks per second) from the available stepper motor power.

5.2.2 **Yaw.** The geometry of the positioning system restricts head yaw to a range of only 8°. The distribution of this angle is chosen such that the ratio of yaw angle to linear disk speed is approximately the same at outermost and innermost tracks.

5.2.3 **Bearings.** The actuator system utilises two half-shielded deep groove ABEC 3 ball bearings arranged in a back-to-back configuration with a dimensional axial preload of 5 lbf for optimum stiffness.

5.2.4 **Band.** The drive band geometry is designed to give symmetry of movement and to minimise band radii and flexing angles. The band is etched from stainless steel with a typical tensile strength of 250K psi. There is a safety factor of approximately 40 between the breaking stress of the band and the dynamic peak tension.

End stops restrict over-travel should control be lost and will prevent read/write heads from either striking the disk hub or coming off the disk.

5.2.5. **Flag zero.** Track zero is defined from a combination of a particular stepper motor phase (one of eight) and a flag mounted on the drive arm. This flag is set up, using a special assembly fixture to switch on opto-interrupter (track zero transducer) mounted on the base casting. The flag is set to switch between tracks 3 and 4. Track zero requires the flag to be true (transducer interrupted) **and** the correct stepper phase to be selected. Note that the opto-interrupter and drive components are in the sealed lower chamber and hence protected from contamination and accidental handling damage.

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5.3 Head/track positioning accuracy

The requirements of the positioning system are (a) that tracks do not touch and (b) that an acceptable signal to noise ratio is obtained when the same track is overwritten. Broadly speaking, the first condition determines the maximum track pitch error. In the case of the RO 200E drive it relates mainly to the static stepper motor accuracy. The second condition relates to the repeatability of the positioning system. Thus given a specification for the repeatability tolerance the required mean (static) step accuracy of the motor can be determined for a given track density.

5.4 Airflow and filters

The airflow generated by disk rotation causes air to flow from the disk chamber through an aperture into the drive chamber and to return via a recirculating filter. This flow system ensures equalisation of temperature during warm up by moving air over all components. By positioning the recirculating filter upstream from the heads and the drive components downstream from the heads optimum purge conditions can be achieved. The disk hub is designed to ventilate the inter disk spaces from both ends thus ensuring adequate air flow across the disks.

The breather filter situated on the top cover is positioned on the disk rotational axis. This compensates for atmospheric changes and maintains a pressure balance across the DC motor bearings reducing the risk of ingress of contaminants. The breather filter is 99.97% efficient to 0.5 um particles and the time taken to equalise pressure is less than one second.

The recirculating filter is positioned in the drive chamber upstream from the disk chamber. This ensures that any particles generated by moving parts are retained by the filter and prevented from contaminating the disk chamber. The recirculating filter is 99% efficient to 0.5 um particles giving a purge time of 12 seconds.

5.5 Thermal compensation

The positioning mechanism is designed to compensate automatically for head to track mispositioning caused by thermal effects. The thermal loop in the disk chamber (motor hub, disk, head flexure, head arm, shaft, bearings, bearing housing and base casting) causes the read/write head to move outwards from track centre as temperature rises. By careful design of geometry and materials, the thermal loop in the drive chamber (stepper motor, band, drive arm, shaft, bearings, bearing housing and base casting) causes a counter rotation of the actuator thereby maintaining the heads on track centre. See Figure 12.

The resulting misposition is about 1 uin per 1°C temperature change. It is estimated that this would be about 8-10 uin per °C in the absence of this compensation mechanism.

5.6 D.C. motor and brake

The motor is a brushless 2-phase external rotor DC motor with integral hub and commutation effected by Hall sensor. A spare Hall sensor is provided in each motor. The motor uses preloaded ABEC 7 bearings and is balanced in two planes to better than 0.25 gm cm. A ferrofluidic seal is fitted above the top bearing. The disk hub is grounded to the master electronics board via the motor shaft and a button contact.

The brake is a plunger solenoid designed to stop the motor in 5 seconds and to provide a restraining torque during handling. The brake pulls in at 12V and holds off at 5V.

6. MASTER ELECTRONICS BOARD

The master electronics board layout and schematics are given in Figures 23 and 26 (a) – (d). This board provides the following circuit functions:-

- read data channel and interface
- write data interface
- drive control interface
- fault detection
- stepper motor control circuit

In addition the master board provides DC power distribution and control to the motor speed control board and the pre-amplifier board. The interconnections between the various boards are illustrated in Figure 13.

6.1 Read data channel

Read data from the pre-amplifier board is received differentially on the lines RD+ and RD–. The 592 video amplifier, IC1, amplifies the readback signal by a factor of 20. Components R7, R8, C6, C7, L1, L2, C53, L5, L6 form a fifth order low pass Butterworth filter with a characteristic frequency of 4.5 MHz. The second 592, IC2, is configured as a differentiator and transforms the peaks of the readback pulses to zero crossings which are detected by the zero-crossing detector, IC3.

The output signal on IC3 pin 1 is high when the input signal is positive and low when negative. IC3 pin 10 provides a negative pulse of duration 100 ns for every zero-crossing on the input signal. These two signals are used as the data and clock inputs to the D-type flip-flop, IC4. This connection provides a time domain filter which will reject zero-crossings occuring at less than 100 ns intervals.

The exclusive-or gate IC5 generates a pulse for every edge output from IC4 pin 5 using the delay generated by the series connection through the elements of IC6 and IC7.

The signals ±MFM READ DATA are transmitted to the host for decode.

Figure 14 illustrates a typical readback signal at various stages in the read channel. Figure 15 shows read/write data timings.

6.2 Write data interface

Write data from the host is received on the lines ±MFM WRITE DATA. This differential signal is transmitted to the pre-amplifier board as the single ended signal WDI using the line receiver IC7.

The signal WRITE GATE from the host is inverted and transmitted to the pre-amplifier board as R/W.

Precompensation of write data is recommended and a preferred scheme is shown in Appendix 2. The compensation applies to the centre bit of each five bit pattern. The amount of compensation should be 10 to 12 ns and it is recommended it be applied to all cylinders.

6.3 Drive control interface

All input lines on the control interface are terminated by a 220 ohm resistor to +5V, and a 330 ohm resistor to logic ground. The input line receivers and output line drivers are 74LS244 buffers with tri-state outputs.

6.3.1. **Input lines.** WRITE GATE and HEAD SELECT Ø, 1, 2, are hard wired to their appropriate circuits on the master electronics boards. DIRECTION IN and STEP are connected to input pins on the 8049 microprocessor, since the control of the stepper motor is achieved totally through firmware.

6.3.2. **Output lines.** SEEK COMPLETE, TRACK ZERO and READY are generated by the 8049 microprocessor. INDEX is derived by dividing the output from a Hall sensor on the drive motor by 2, since two pulses occur per revolution of the motor. The width of the output pulse is set to approximately 200 µs before transmission. WRITE FAULT is set true if any of the drive fault conditions occur, as described in section 3.3. DRIVE SELECTED is set true if the DRIVE SELECT signal from the host corresponds with the drive select switch setting on P9, and if the drive is READY.

6.4 Fault detection

Two modes of fault detection are used in the drive. One is implemented in the microprocessor firmware and is described in section 3. The other, which is implemented in hardware, is described in this section. Three drive faults are detected.

6.4.1. **Write Unsafe (WUS).** This signal is transmitted from the pre-amplifier board and is gated through an exclusive OR gate with R/W. It is high when a pre-amplifier write fault has been detected or when the pre-amplifier is in the read mode.

6.4.2. **Low +12V rail.** IC9 pin 4 has a 4.3V reference voltage level established from D3. IC9 pin 5 monitors the +12V rail and when it drops to 10.0V, IC9 pin 2 will go low. This condition is wire OR'ed with the Write Unsafe condition, and when low, signals a hardware WRITE FAULT to the microprocessor.

6.4.3. **Low +5V rail.** IC9 pin 13 will go high if the +5V rail is less than 4.3V. In this condition, RST will be low which will hold the microprocessor in a Power-up reset state. Also WCR will be high which will turn off the write current on the pre-amplifier board.

6.5 Stepper motor circuitry

Stepper motor control is achieved totally by firmware in the 8049 microprocessor. See section 9.1. Eight lines from the microprocessor control the stepper motor drive circuits on the master electronics board. Figure 16 illustrates the connection between the microprocessor, the drive circuits and the stepper motor via the motor speed control board.

The stepper motor has a two phase bipolar winding configuration and a velocity sensor mounted externally. The windings are driven by constant current drivers mounted on the motor speed control board.

The magnitude and direction of current is controlled by the circuits on the master electronics board. The direction control is direct from the microprocessor using the signals APH and BPH. The magnitude can be set at one of two levels, high or low, and is defined by the singals AVR and BVR. Using these four signals, an 8 step switching sequence can be obtained as shown in Figure 18.

The velocity feedback from the velocity sensor is used for damping and is picked up from one of two coils depending on cylinder number (VFA and VFB). It is added or subtracted, true or inverted, depending on the step in the switching sequence and direction of travel. This is controlled by four lines from the microprocessor AFB, AFB/, BFB and BFB/.

The signal VDS defines which velocity sensor coil is used, and also switches REDUCED WRITE CURRENT (RWC) on the pre-amplifier board. The transition occurs at cylinder 210.

A position settled signal, POK, is derived from a window comparator monitoring the velocity feedback, and is used by the microprocessor to determine SEEK COMPLETE.

6.6 Index

INDEX is an interface signal used to mark a fixed reference point relative to the disk. The Rodime drive does not have a separate INDEX transducer but instead uses the output of the Hall sensor inside the DC motor. This sensor output is a square wave which has a 50% duty cycle and makes 4 transitions in one disk revolution. This is then divided by two and used to trigger a monostable which gives a 200 us pulse once per disk revolution.

This hardware scheme results in a non-unique INDEX that is one of two each 180° apart. Normally this would not be significant since INDEX should only be used during a drive format. However, some controllers require a unique INDEX for reading.

The following procedure is used to ensure the INDEX is always unique. A special data pattern is written by head Ø on one half of track –2 during drive manufacture. At power-up a comparison is made between the Hall sensor output and the data burst and a unique index is selected. If the data burst is not found on track –2, the drive will display fault code 1. Since the uniqueness of the INDEX signal

is only relevant to certain controllers provision has been made to ignore this fault code. Cutting link A will cause the drive to ignore the loss of the data pattern. Section 9.2 gives details of features designed to protect track –2 from accidental overwrite.

6.7 Links

There are two user definable links on the master board close to the microprocessor.

Link A. This link is cut to circumvent the fault caused by the loss of the INDEX calibration track. See section 6.6.

Reset link. When this link is inserted, J2 pin 5 is connected to the RESET pin on the microprocessor. This will allow an interface RESET if J2 pin 5 is held at less than 0.5V for a minimum of 12.5 μs, then returned to 3.8V minimum. Note that the microprocessor has an internal pull-up of 200 Kohm on this line.

7. PRE-AMPLIFIER BOARD

The pre-amplifier board layout and schematics are shown in Figures 24 and 27. This board provides a means of connection for up to eight read/write heads: Two SSI 117 monolothic integrated read/write circuits provide the following functions:

- pre-amplification of read data
- write amplifiers
- head selection
- write fault detection

Each circuit can support four read/write heads.

RDX and RDY are the differential read data signal lines to the master electronics board.

HSO and HS1 select 1 of 4 heads on each circuit.

HS2 and HS2/ select which circuit is active.

WUS is the write unsafe signal which is low when the chip is writing normally. The high (unsafe) level will be caused by:-

(a) Head input shorted to ground.
(b) Head input shorted to centre tap.
(c) Head inputs shorted together.
(d) Head input open.
(e) Centre tap open.
(f) No write data transistions.
(g) No write current.
(h) Any combination of above.
(i) Chip is in read mode.
(j) Chip is disabled (HS2, HS2/).

Certain lines have been mentioned in the text. These are defined as follows:

- WDI is the WRITE DATA INPUT line.
- R/W is the read/write mode select line.
- RWC is the reduced write current line.
- WCR is the write current return line which can turn off the write current.

8. MOTOR SPEED CONTROL BOARD

The motor speed control board layout and schematic are given in Figures 25 and 28. This board provides the following circuit functions:-

- DC motor speed control.
- stepper motor drive circuits.
- solenoid brake power supply.
- track zero transducer power supply and output termination.

8.1 Drive motor speed control

Speed control of the drive motor is achieved using a phase-locked loop (P.L.L.) technique. The drive motor rotates at 3600 rev/min and generates two feedback pulses per revolution from an internal Hall effect IC. This results in a

120 Hz feedback signal which is phase-locked to a reference signal generated from the microprocessor crystal oscillator on the master electronics board. A speed variation of less than 0.1% is achieved.

The Address Latch Enable (A.L.E.) signal from the microprocessor is used as the reference. This signal (REF CLK), frequency 733 KHz, is divided by 6144 using IC1 and IC2 to give a 120 Hz input to the phase/frequency detector IC3. The other input to IC3 is the feedback signal from the motor Hall sensor.

The output signal on IC3 pin 8 is a DC voltage proportional to the phase difference between the two input signals. R4, R18, C2 and IC4 form the electronic compensation network that ensures the stability of the control loop. The resultant signal on IC4 pin 7 drives the motor via the emitter followers Q1 and Q2, and the power amplifier Darlington transistors Q3 and Q4.

A two phase drive motor is used, and commutation between the two phases is accomplished using the Hall IC output. This signal, and its inverse, alternatively enables either Q3 or Q4, depending upon the phase of the commutation cycle.

The Hall sensor signal is also sent to the master electronics board, where it is divided by 2 and used as the drive INDEX signal. A spare Hall sensor output is provided, and in the event of output failure, the spare may be connected by wire link selection.

8.2 Stepper motor drive circuit

Current in the windings of the stepper motor is controlled by two constant current drivers IC5 and IC6. The magnitude of the current is controlled by AVR, BVR, and the direction by APH, BPH. The stepper windings are connected between ACA and ACB, BCA and BCB.

The signals AOF and BOF hold the drivers in an off condition until the spindle motor is up to speed during the power-up sequence.

8.3 Brake Power is supplied to the solenoid brake initially from the +12V rail until it pulls in and the DC motor is up to speed. Thereafter, power is supplied from the +5V rail via diode D3 to reduce running power dissipation.

8.4 Track zero transducer The resistor R18 is a bias resistor for the LED in the opto-interrupter. A nominal forward current of 30 mA is supplied. The resistor R17 is a pull-up resistor for the photo-transistor which is connected in the open-collector output configuration.

9. MICROPROCESSOR

The microprocessor used in the RO 200E series is a member of the 8048 family of single chip processors. The particular type used is the 8749, an EPROM version with 2048 bytes of internal program memory and 128 bytes of RAM. The microprocessor cycles at 11 MHz, giving an instruction time of 1.36 μs.

The processor has three main functions:-

- stepper motor control.
- interface handling.
- track positioning monitoring.

It also indirectly controls the DC spindle motor since the 733 KHz ALE signal output from the processor is used as a reference frequency for the P.L.L.

9.1 Stepper motor control

Four interface signals are used to control the stepper motor.

STEP. This input signal is used in conjunction with DIRECTION IN to move the stepper motor. It is connected to the 8749 T1 pin. This is a special input to the microprocessor which is used to clock an internal 10 bit counter. This counter is reset prior to each seek. Once the

first STEP pulse is received the processor issues stepper motor phase changes until the number of changes equals the value in the counter. At this point the seek is terminated and SEEK COMPLETE is set true after final step damping.

DIRECTION IN. This input is connected directly to an I/O pin of the processor. It defines the direction of motion of the stepper motor. Once the first STEP of any seek has been received the microprocessor samples this input and internally stores the result. The input is then ignored until the next seek.

SEEK COMPLETE. This status line is driven by a S-R flip-flop. STEP resets the flip-flop false. It is set true with an output from the microprocessor.

TRACK ZERO. This status line is driven directly from the microprocessor. It will be set true when the read/write heads are positioned with correct stepper motor phase over track zero, false otherwise.

Velocity feedback is obtained from a tachometer fitted to the endcap of the stepper motor. This feedback is employed (a) to assist in the control of the motor whilst is is slowing down on the final approach to the desired track and (b) to control the settling when the motor reaches the desired track. This results in settling time being greatly reduced from that which could be obtained under open loop conditions.

An important additional benefit gained from the use of velocity feed-back is that the microprocessor can examine a digitised velocity signal to ensure that the positioner assembly is fully settled before setting "SEEK COMPLETE" status.

All step pulses are buffered by the microprocessor. Two factors determine the stepping rate of the head assembly.

- the interface step rate.
- the length of the seek.

Stepper rate is defined as follows:-

a) Input Step Rate 5 μs to 130 μs.

Seek Length (N)	Stepper Rate
$N < 5$	Slow (1 ms)
$5 \leq N < 32$	Moderate accn/decn ramps
$32 \leq N < 150$	Fast accn/moderate decn ramps
$150 \leq N < 639$	Fast accn/fast decn ramps

b) Input Step rate 130 μs to 900 μs.
Stepper rate = 1 ms.

c) Input Step Rate 900 μs to 5 ms.
Stepper rate = variable.

d) Input step rate greater than 5 ms may cause seek errors.

In the ramped mode of operation the maximum step rate to which the stepper motor accelerates is 7000 steps/second. The acceleration/deceleration ramps chosen are based on the length of seek required. This choice ensures optimum access times with defined settling performance.

In the ramped seek mode (ie, for input step rates in the range 5 to 130 μs) the microprocessor will move the positioner assembly before all the step pulses have been received in accordance with the following conditions:-

a) More than 31 step pulses have been received

or

b) 180 μs has elapsed since the last step pulse was received

After moving off, and as further step pulses are input, the microprocessor makes decisions about acceleration and deceleration on the move. This also ensures that access times are minimised.

'Soft' endstop protection is also provided by the microprocessor. An internal track counter which is dynamically updated means that the processor is aware of how close the mechanical assembly is to the mechanical endstops at any point in a seek. This means that if a seek is requested to an illegal cylinder number, the microprocessor ramps down the stepper motor and stops at the last legal cylinder number attainable in the direction requested (ie, stops at cylinder Ø if a seek is attempted to a negative track and at cylinder 639 if a seek to a cylinder > 639 is requested).

This protection operates for all legal step rates in any direction.

In the event of a failure in the velocity damping system, resulting in an undefined settling performance, the microprocessor will initiate an auto-recal prior to settling seek complete.

9.2 Protection of index selection track

Protection of track –2 is considered to be of prime importance and a number of safeguards have been built into the firmware.

9.2.1. All interface controlled seeks beyond track zero are prohibited by the microprocessor.

At the end of each seek and before SEEK COMPLETE is issued a check is made. If either of the following conditions is detected then an auto-recal will be executed.

(a) Flag zero is detected and the internal track counter is not at zero.

(b) The track counter is at zero and flag zero is not true.

APPENDIX 1

Patents

European Application Number	US Application Number	Title
81305976	332003	"Read-Write Head Thermal Compensation System."
82302197	373281	"Method and Apparatus for Controlling a Stepper Motor."
82303263	391010	"Generation of Unique Index Mark from the Commutation of DC Brushless Motor."
82303262	391150	"Damping of Stepper Motor using Non-Active Windings."
	388165	"Ventilation System for Computer Disc Drive Hub Assembly."

APPENDIX 2

Write Data Pre-Compensation Scheme

Data sequence leftmost bit written first			Required write pre-compensation of centre bit
00	0	10	EARLY
00	0	11	EARLY
00	1	10	LATE
00	1	11	LATE
01	1	00	EARLY
01	1	01	EARLY
10	0	00	LATE
10	0	01	LATE
10	1	10	LATE
10	1	11	LATE
11	1	00	EARLY
11	1	01	EARLY

APPENDIX 3

Format Recommendations

1.0 The following sections describe the general formatting recommendations for the RO 200E series disk drives.

2.0 **Encoding.** It is recommended that data be written on the disk using an MFM encode. The algorithm to convert from NRZ data to MFM data is as follows:-

For a "1" write a flux transition in the middle of the bit cell; for a "0" write a flux transition at the start of the bit cell except when a "0" follows a "1".

3.0 **General Requirements.** The format of the data recorded on the disk is totally a function of the host controller. The two most common formats allow 32 x 256 byte sectors or 16 x 512 byte sectors to be written on each track. A soft sectored format should be used. The start of each sector is identified by a unique byte which is written on the disk. This byte is normally an invalid MFM code (eg. Hex A1 with a missing clock bit). This unique byte is used to flag the start of the sector address field (containing the physical sector address) and also to flag the start of the sector data field.

4.0 **Sector Format Example.** An example of a recommended format for a 256 byte sector is given in Figure A. A full description of each item is given below:-

1. **Inter Sector Gap.** (15 bytes of Hex "4E"). Tolerance gap to allow for disk speed variations.

2. **Sync Field.** (13 bytes of "00"). Provides VFO lock-on prior to data retrieval. The minimum number of bytes is dependent on VFO lock up performance of host data separator.

3. **Address Mark.** (1 byte of Hex "A1" with missing clock). Identifies beginning of address field.

4. **Address Mark. I.D. Field Identifier** (1 byte Hex "FE") Identifies with previous address mark the beginning of the address field.

5. **Cylinder Address.** (1 byte, "0" to Hex "FF"). The most significant bits in the Head Address field (6) can be used to represent the most significant bit of the Cylinder Address.

6. **Head Address.** (1 byte, "0" to "7").

7. **Sector Address.** (1 byte, "0" to Hex "1F").

8. **Address ECC.** (3 bytes). Available for ECC check of the address field.

9. **Gap.** (2 bytes "00"). Allows write turn-on time when updating the sector data field.

10. **Sync Field.** (13 bytes of "00"). Provides VFO lock-on prior to data retrieval.

11. **Address Mark.** (1 byte of Hex "A1" with missing clock). Identifies beginning of data field.

12. **Address Mark Data Field Identifier** (1 byte Hex "F8"). Identifies with previous address mark the beginning of the data field.

13. **Data.** (256 bytes of data).

14. **Data ECC.** (3 bytes). Available for ECC check of the data field.

15. **Gap.** (2 bytes of "00"). Allows write turn-off time when updating the sector data field.

5.0 **Index Gap.** The gap at the beginning of index allows for head switching recovery, so that sequential sectors may be read without losing a complete disk revolution. Minimum length is 12 bytes, Hex pattern "4E". Normal recommendation is 16 byte lengths.

6.0 **Speed Tolerance Gap.** This gap at the end of the last physical sector (before index) provides a spindle speed tolerance buffer for the whole track. A full track format routine begins and ends with detection of index. It is usually a Hex pattern "4E", and the actual number of bytes depends on media speed during the format operation.

7.0 **Sector Interleaving.** It is possible to interleave sectors to improve data throughput during typical read/write operations by allowing multiple sector transfer within a single revolution.

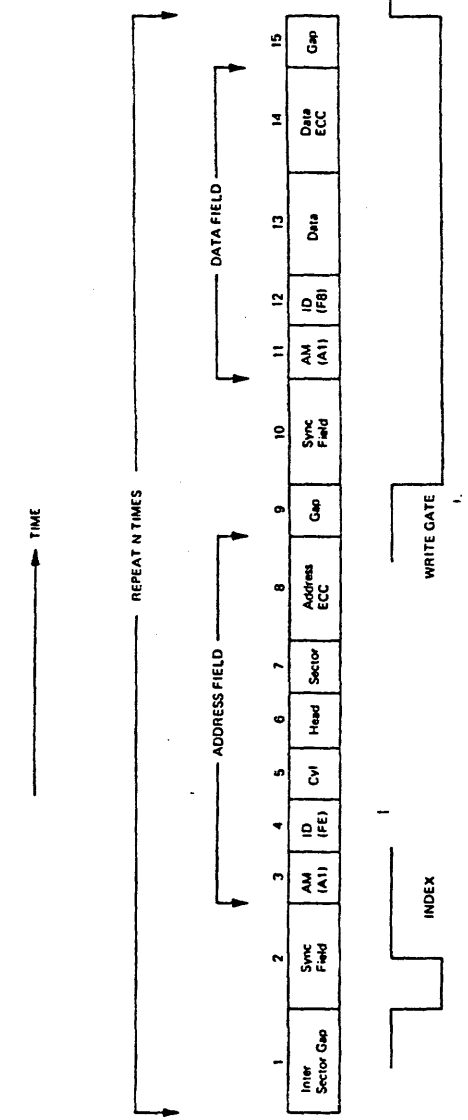


FIGURE A - SECTOR FORMAT

FIGURE 1

Drive outline showing connector positions

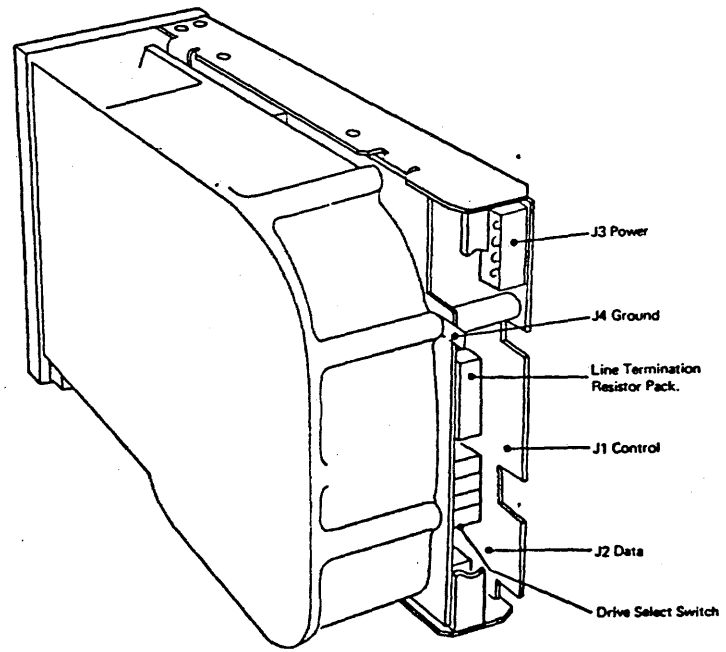


FIGURE 2
J1 Connector — Control

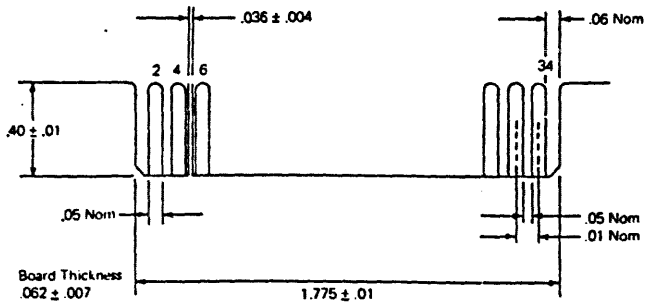


FIGURE 3
J2 Connector — Data

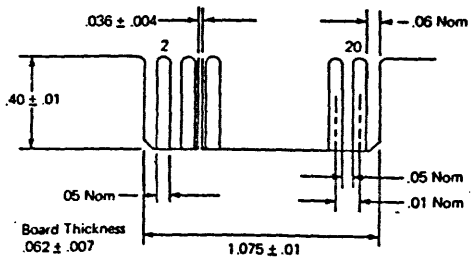


FIGURE 4
J3 Connector — Power

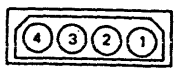


FIGURE 5
Control and power bus

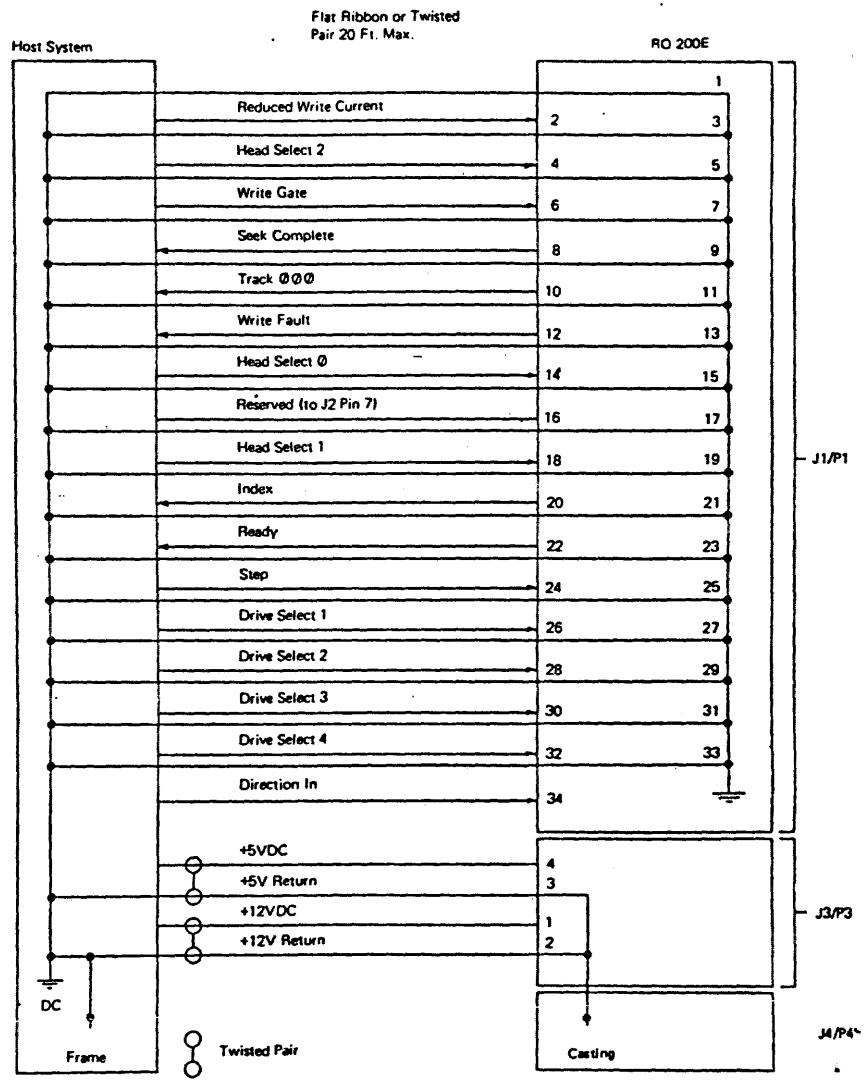


FIGURE 6
Data bus

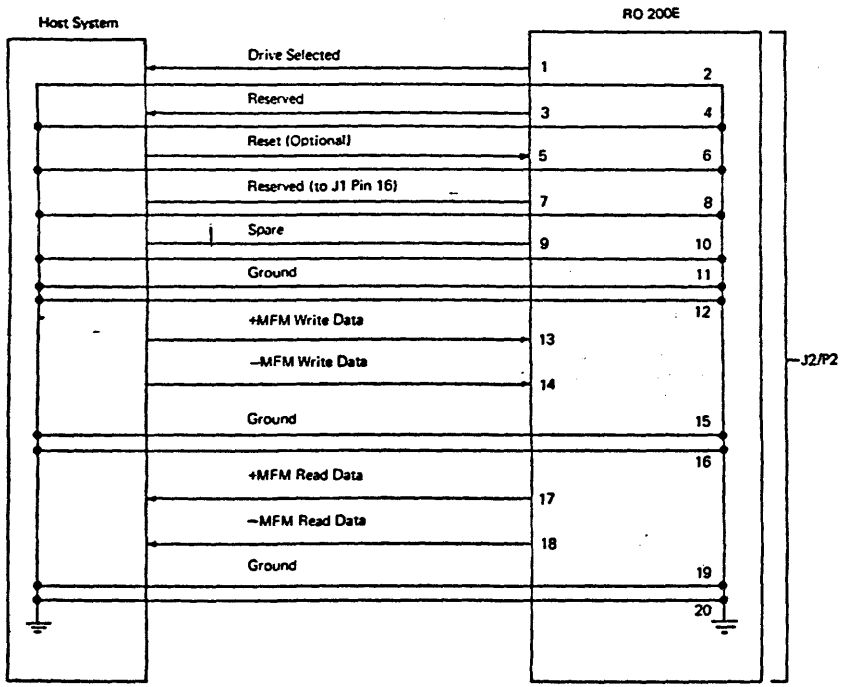


FIGURE 7
Mounting details

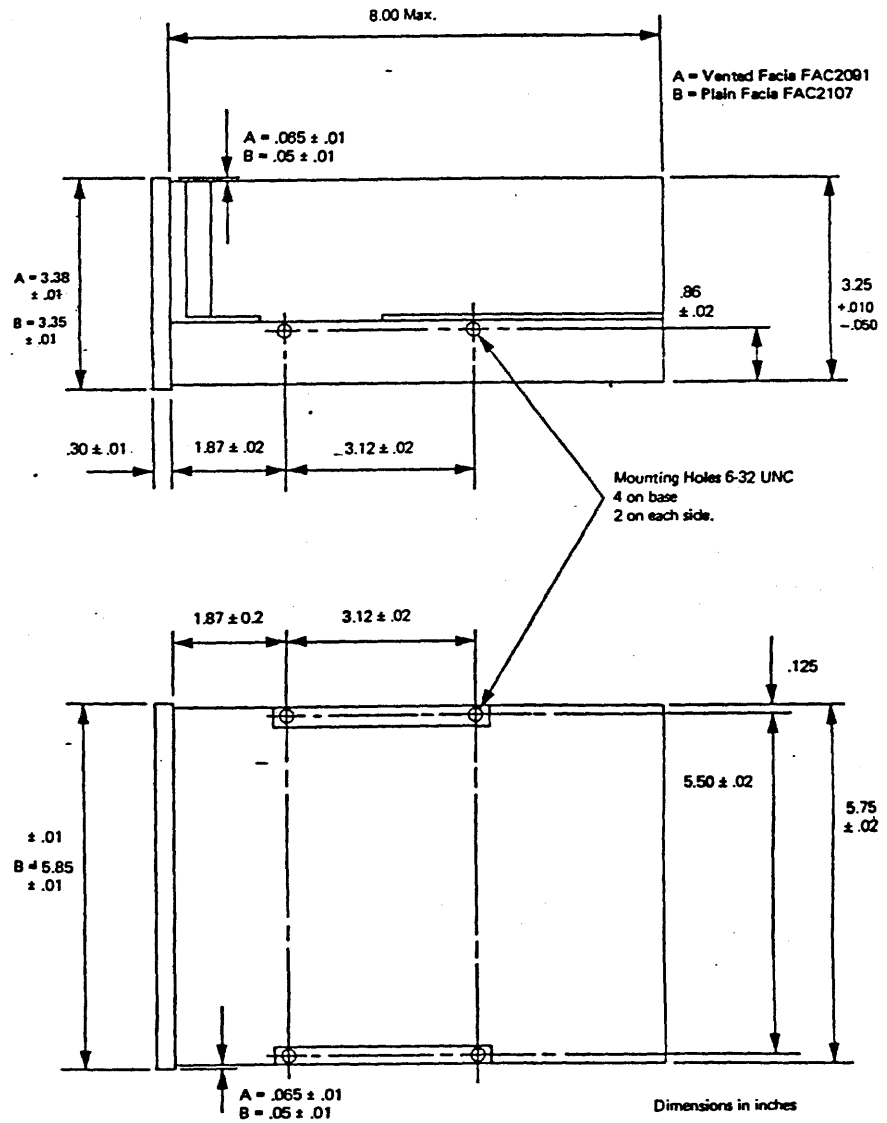
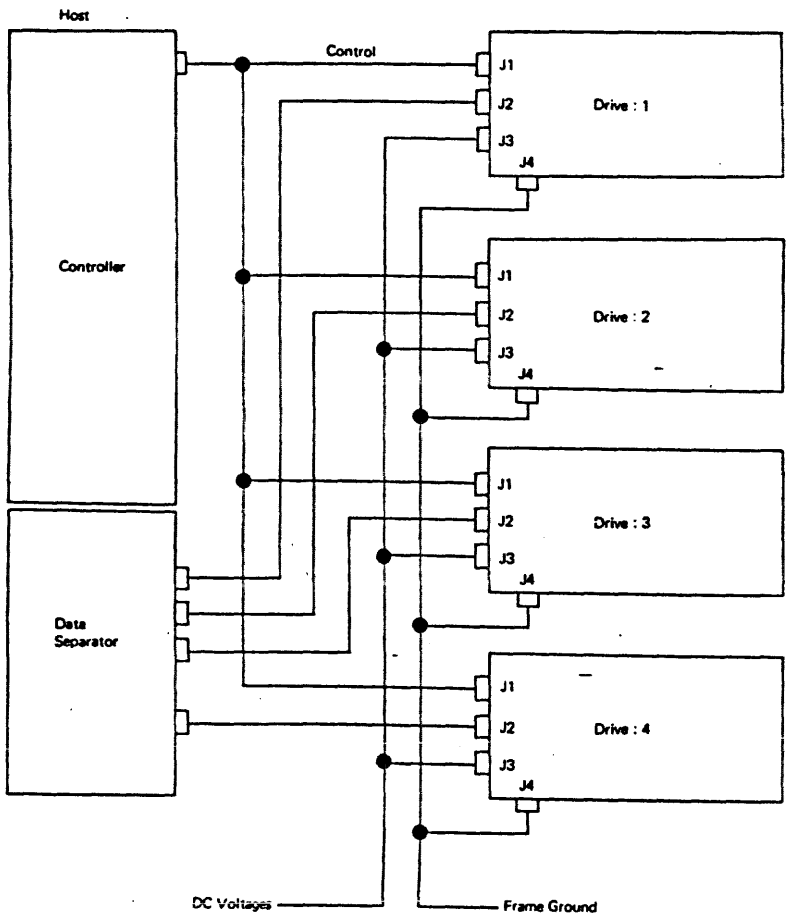


FIGURE 8
System with 4 drives



RODIME

FIGURE 9
Wiring of spare hall sensor

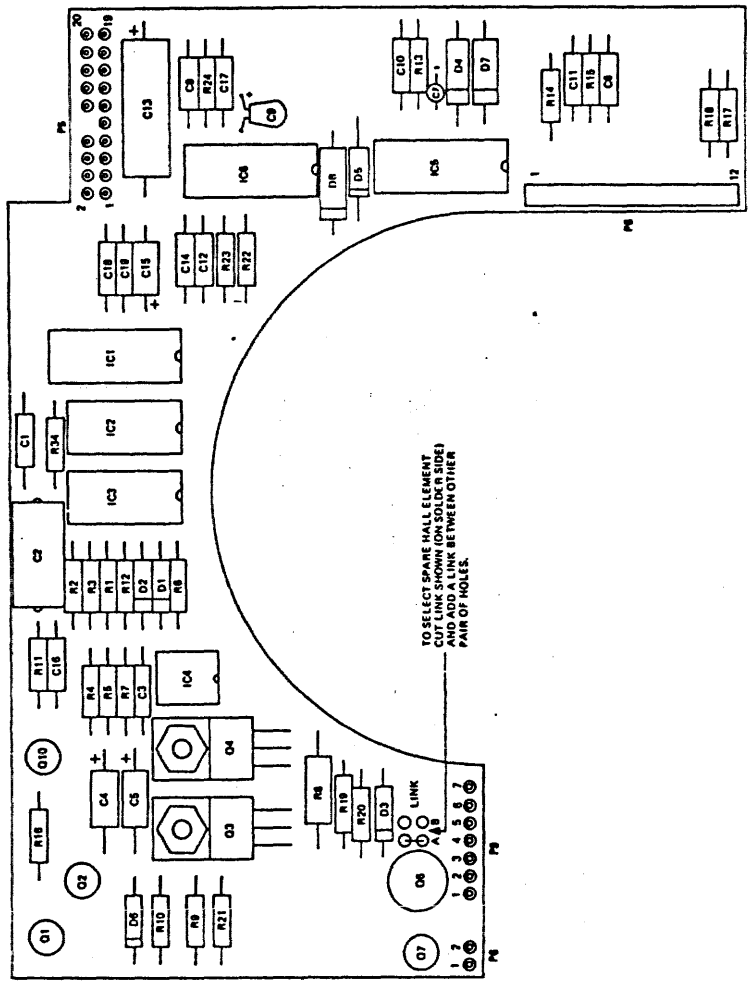


FIGURE 10
Non-planar section of RO 204E

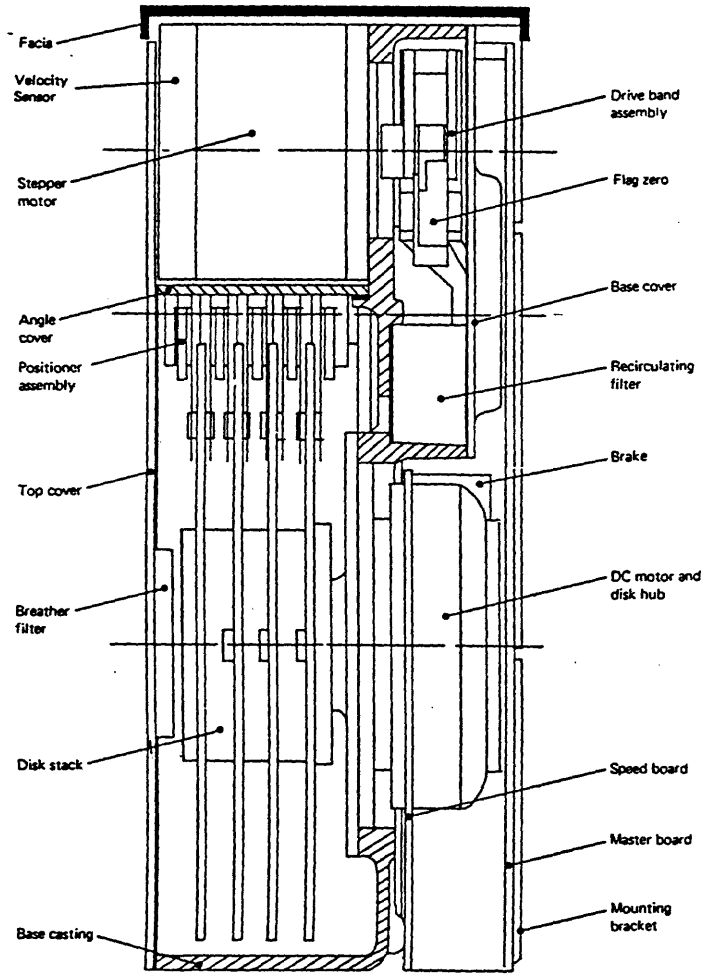


FIGURE 11
Air flow and filter system

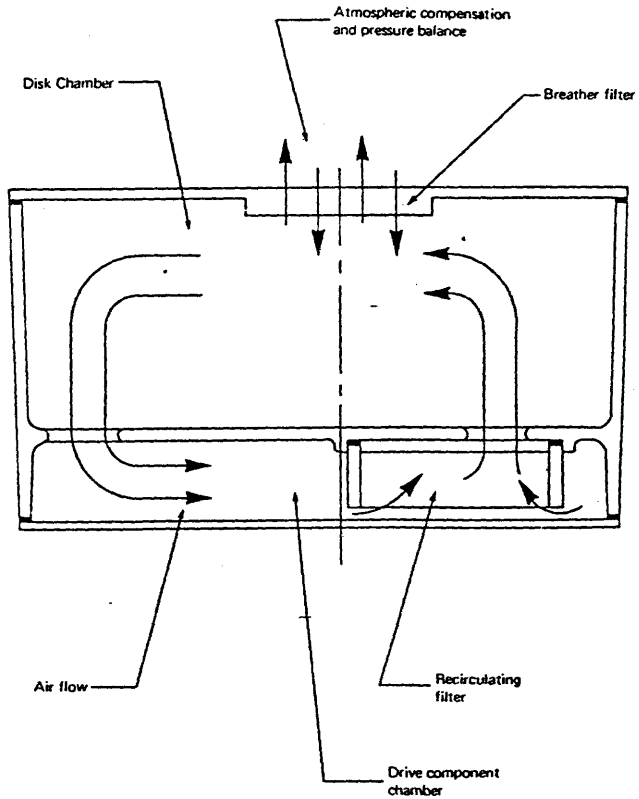
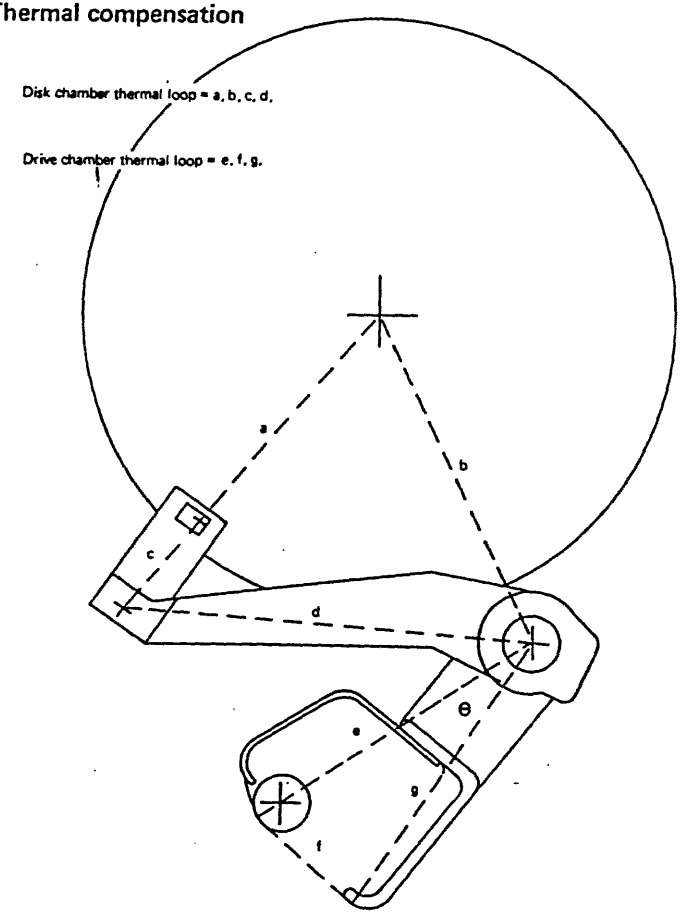


FIGURE 12
Thermal compensation



for a given temperature rise

$\Delta c < \Delta a, \Delta b$ and Δd therefore r/w gap tends

to move outward from track centre

but $\Delta e > \Delta f$ and Δg : therefore angle θ tends

to decrease causing a clockwise rotation of the r/w gap back towards centre

RODIME

FIGURE 13
Board interconnections

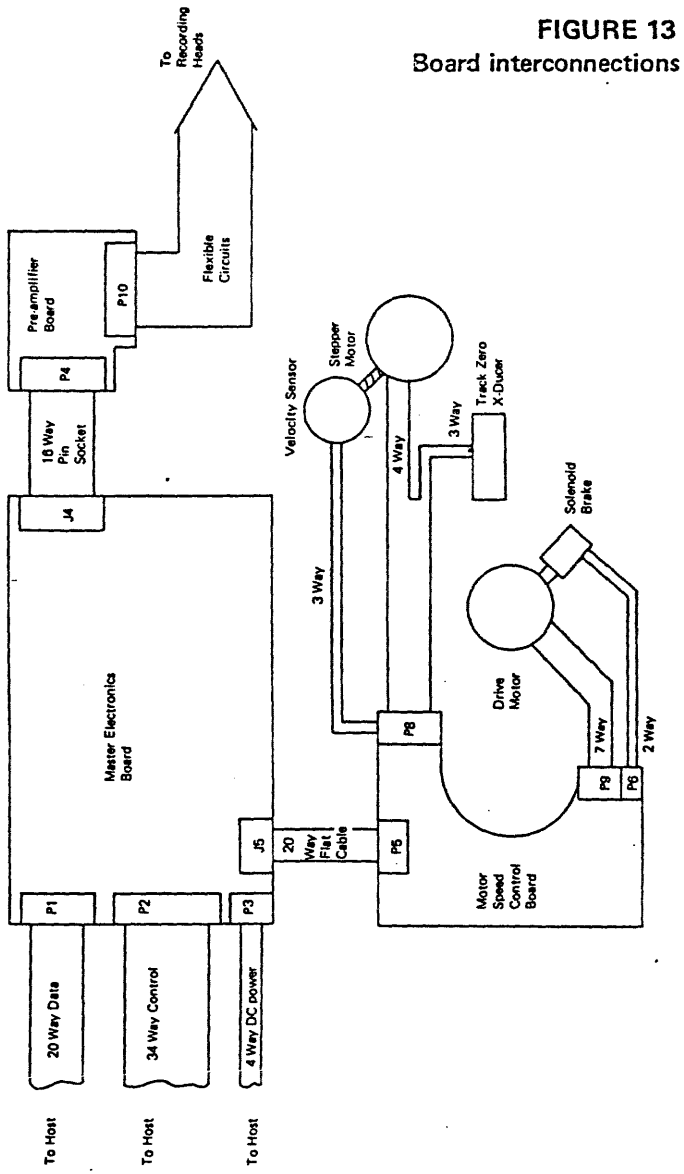


FIGURE 14
Read channel signals

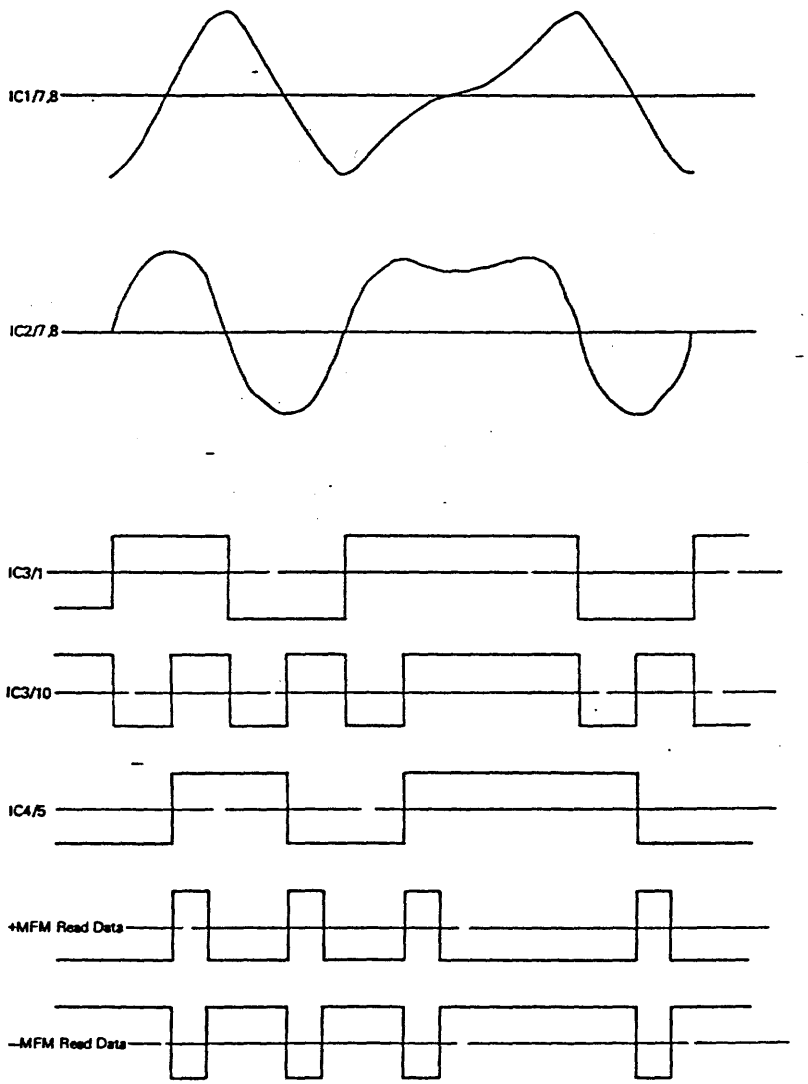
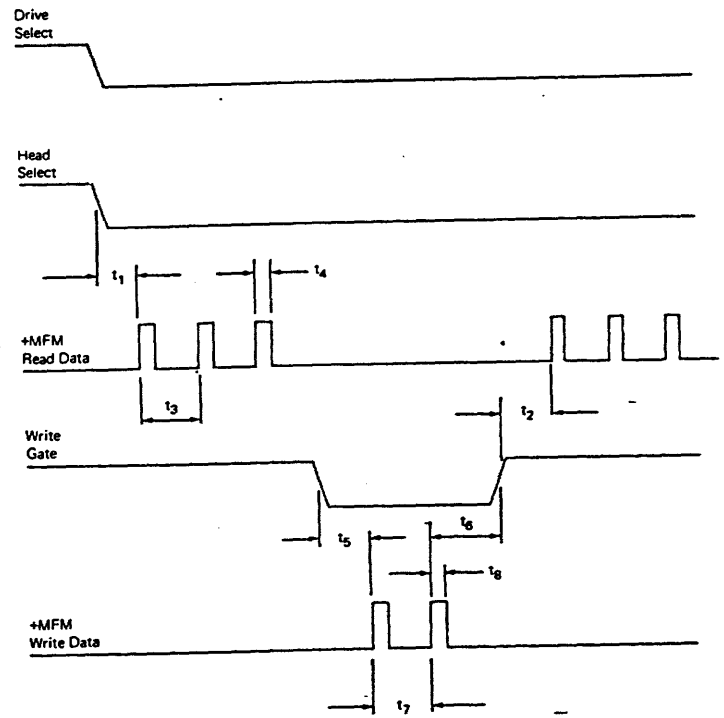


FIGURE 15
Read/Write data timing



Label	Description	Min	Typ	Max	Units
t_1	Select to Read Data			5	us
t_2	Write to Read Recovery			5	us
t_3	Read bit cell		200		ns
t_4	Read Data pulse width	25		200	ns
t_5	Write Gate true to Write Data			400	ns
t_6	Write Data to Write Gate False			400	ns
t_7	Write bit cell		200		ns
t_8	Write Data pulse width	25			ns

FIGURE 16

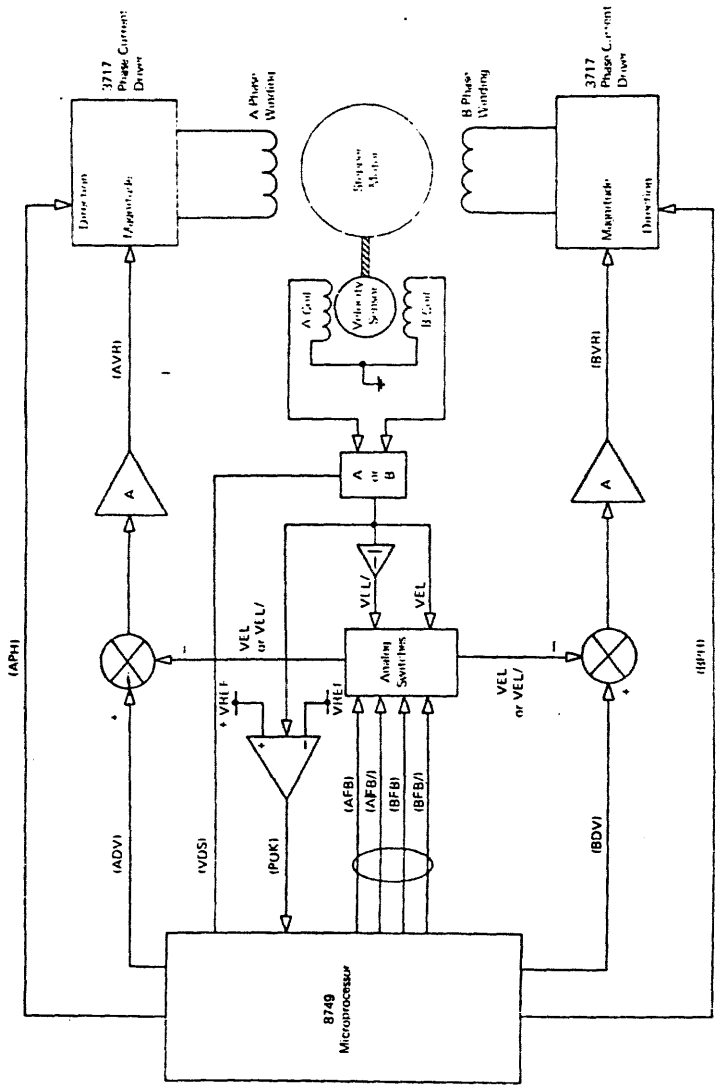
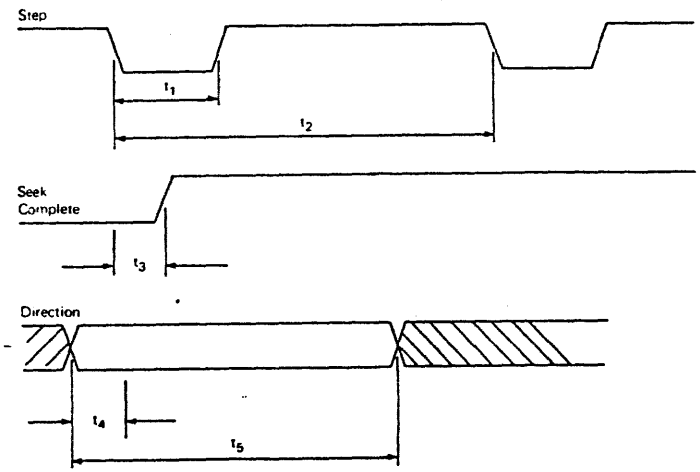


FIGURE 17
Step pulse timing



Label	Description	Min	Typ	Max	Units
t_1	Width of Step pulse	0.5			us
t_2	Time between Step pulses	5		5000	us*
t_3	Time from first Step to Seek Complete False		40		ns
t_4	Direction set to first Step	0			ns
t_5	First Step to direction change (for overlap seek)	150			us

FIGURE 18
Stepper Winding Switching Sequence

↑ ≡ High Current +VE Direction
↓ ≡ High Current –VE Direction
↑ ≡ Low Current +VE Direction
↓ ≡ Low Current –VE Direction

Step	A Phase Current	B Phase Current
1	↑	↑
2	↑	↓
3	↑	↓
4	↓	↓
5	↓	↓
6	↓	↑
7	↓	↑
8	↑	↑
1	↑	↑

FIGURE 19
Power-up flow chart

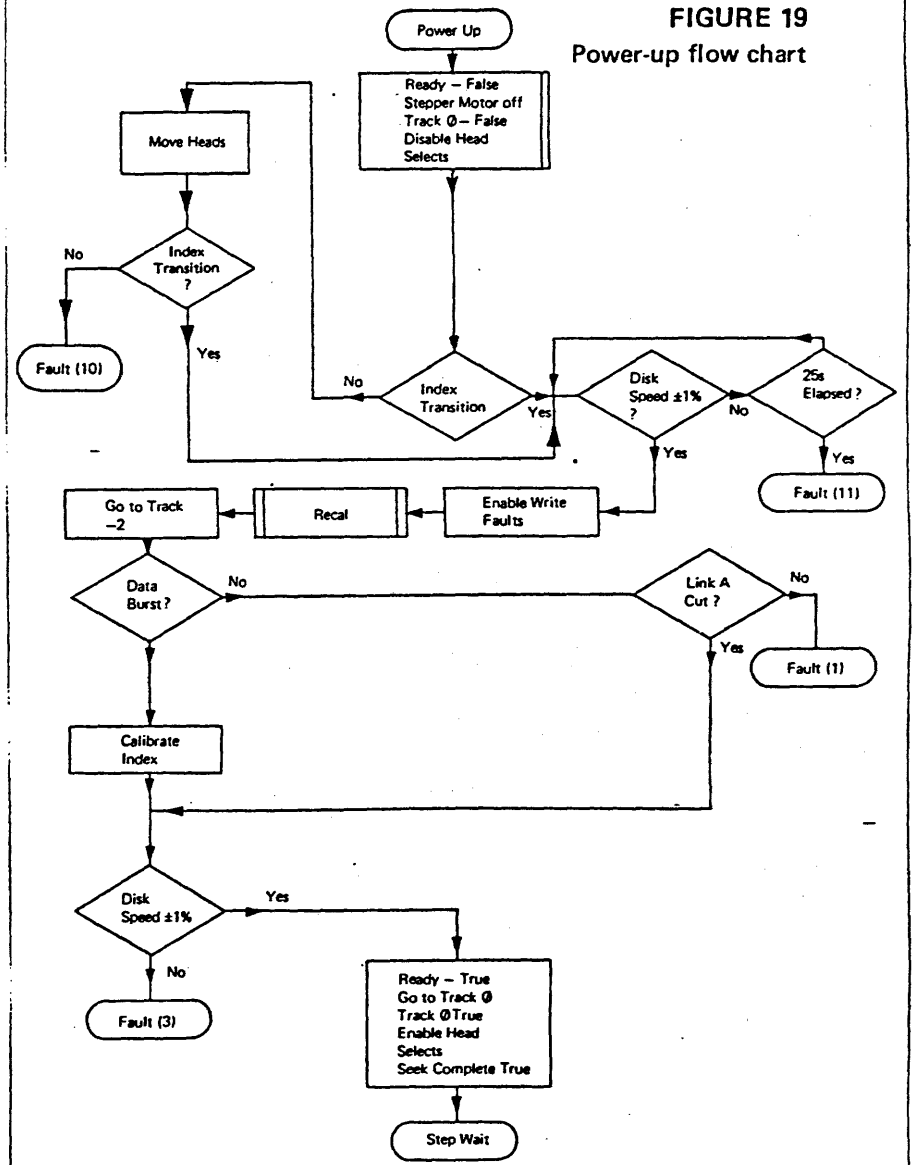


FIGURE 20
Recalibration flow chart

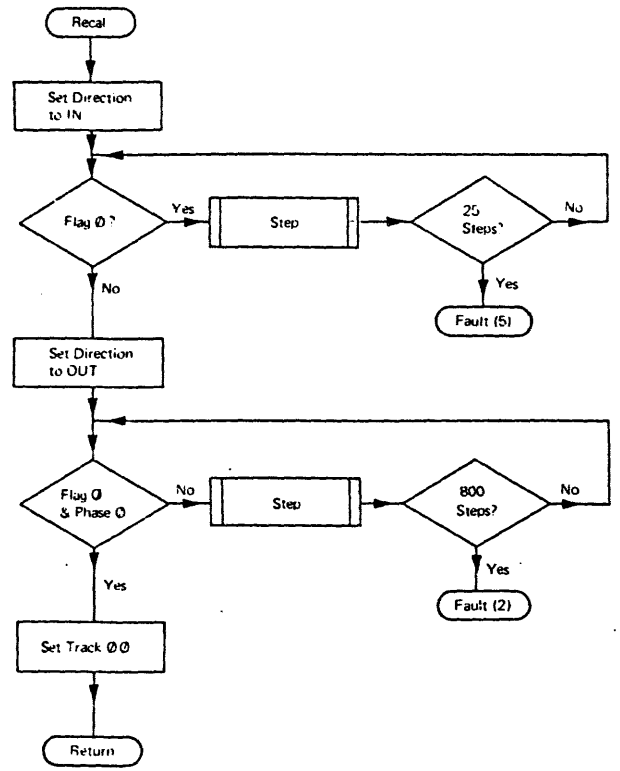


FIGURE 21
Write fault flow chart

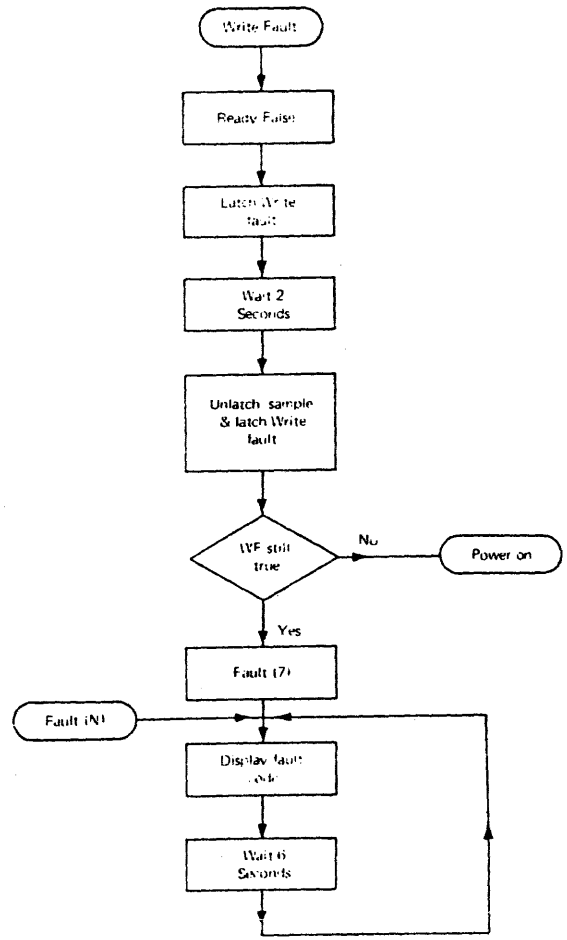


FIGURE 22(a)
Step wait loop

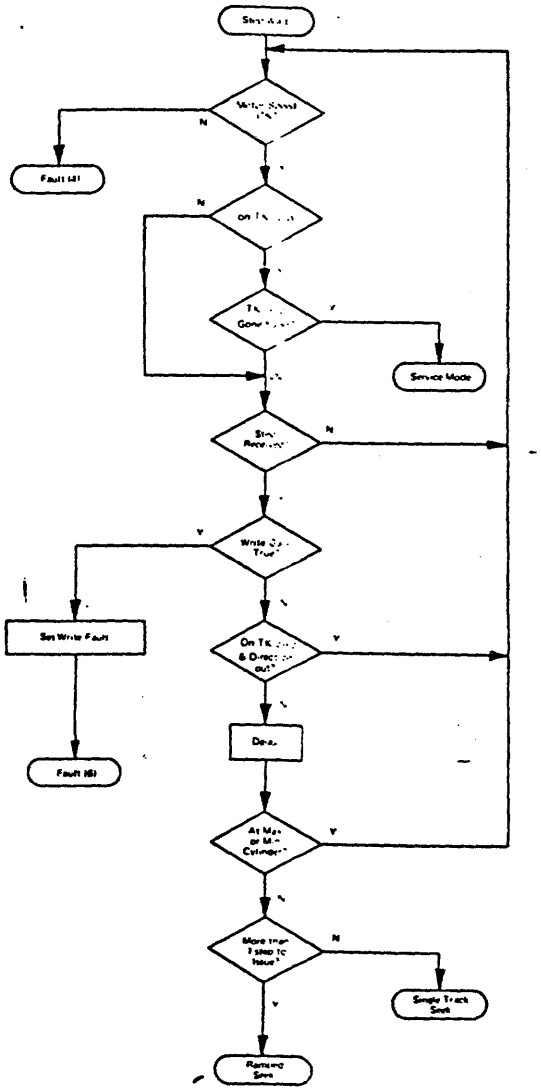


FIGURE 22(b)
Single Track Seek and Slow Mode

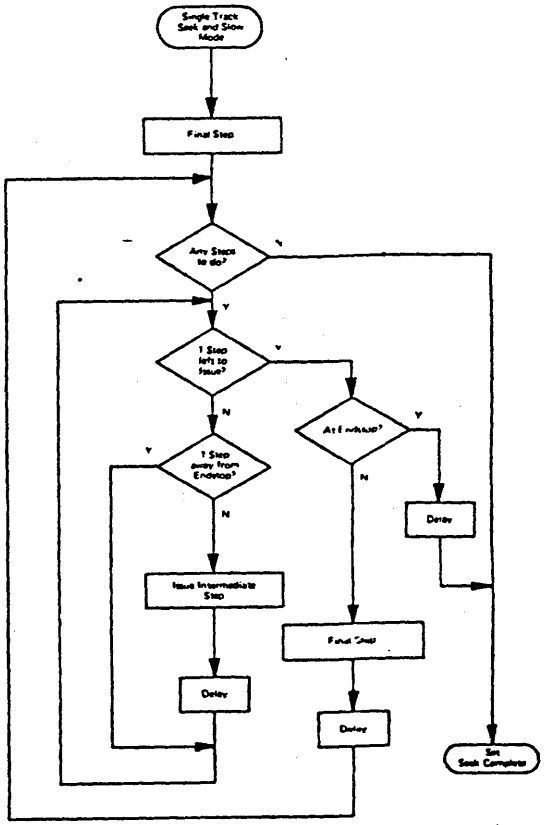


FIGURE 22(c)
Ramped Seek Routes

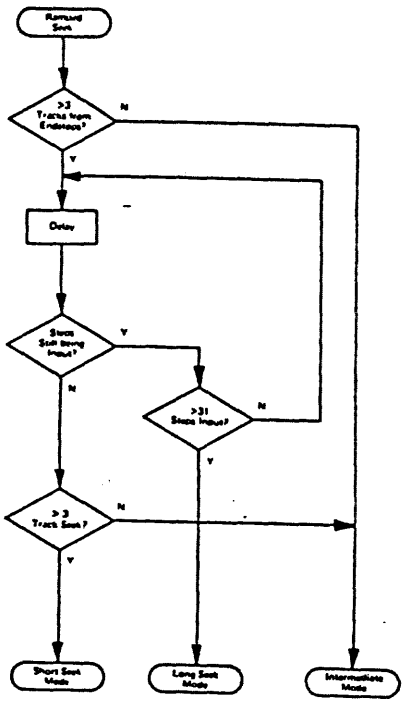


FIGURE 22(d)
Final Step Routine

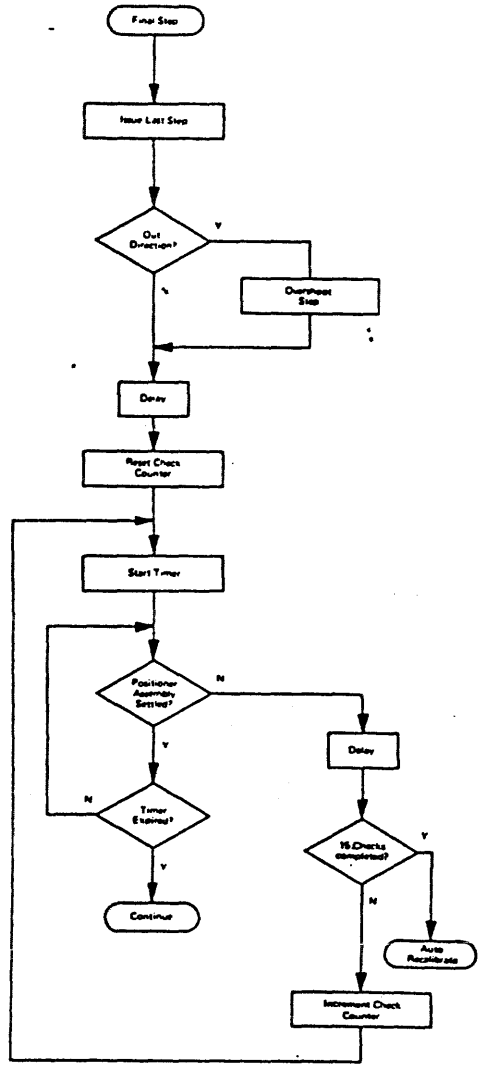


FIGURE 22(e)
Adaptive Settling Routine

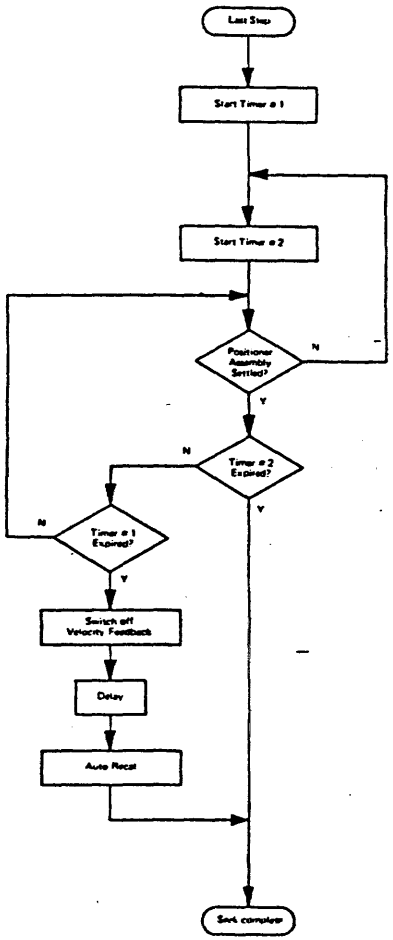


FIGURE 23
Master Electronics Board Assembly

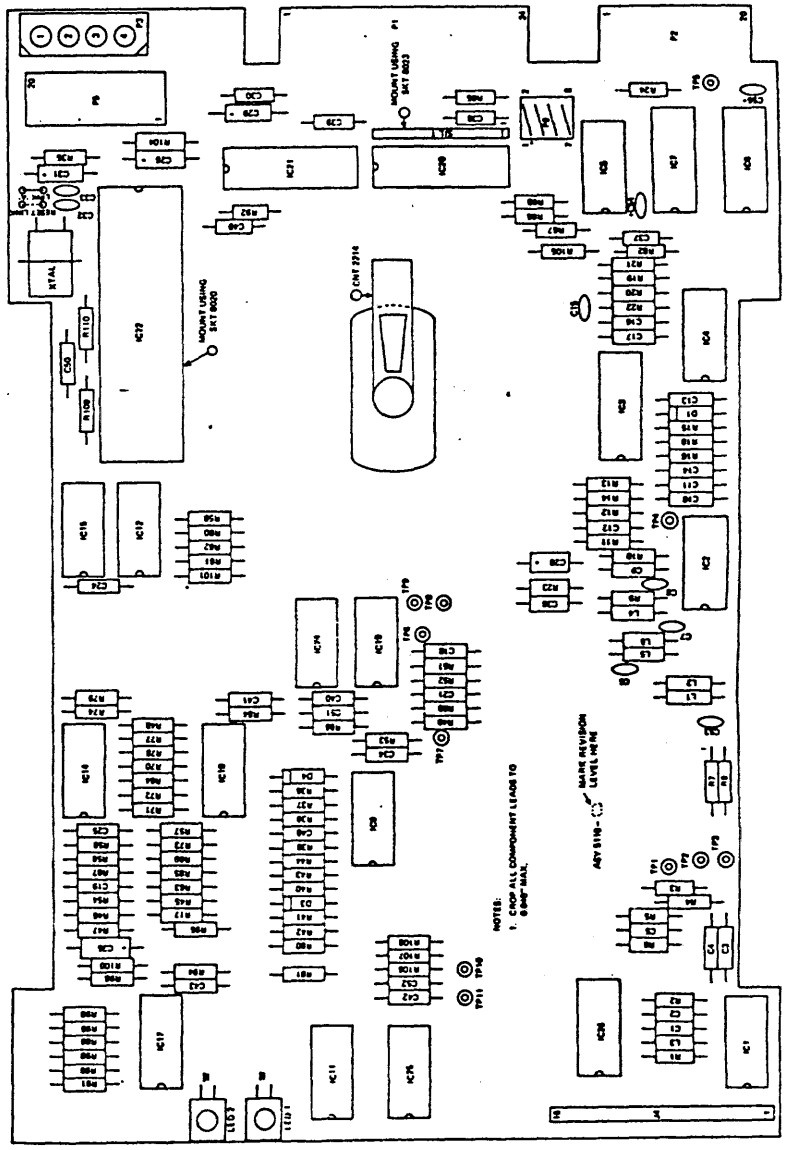
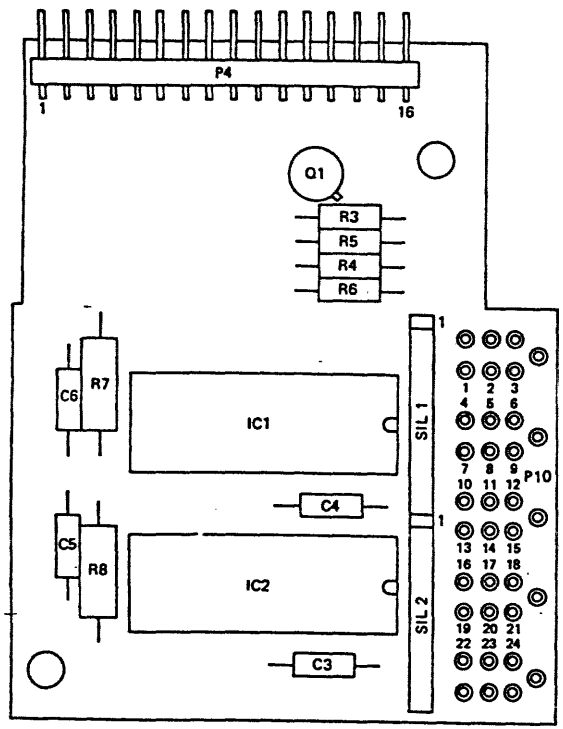


FIGURE 24
Pre-amplifier Board Assembly



1. MAXIMUM COMPONENT HEIGHT ABOVE PCB TO BE 0.25".
2. CROP ALL COMPONENT LEADS TO 0.040" MAX.

FIGURE 25
Motor Speed Control Board Assembly

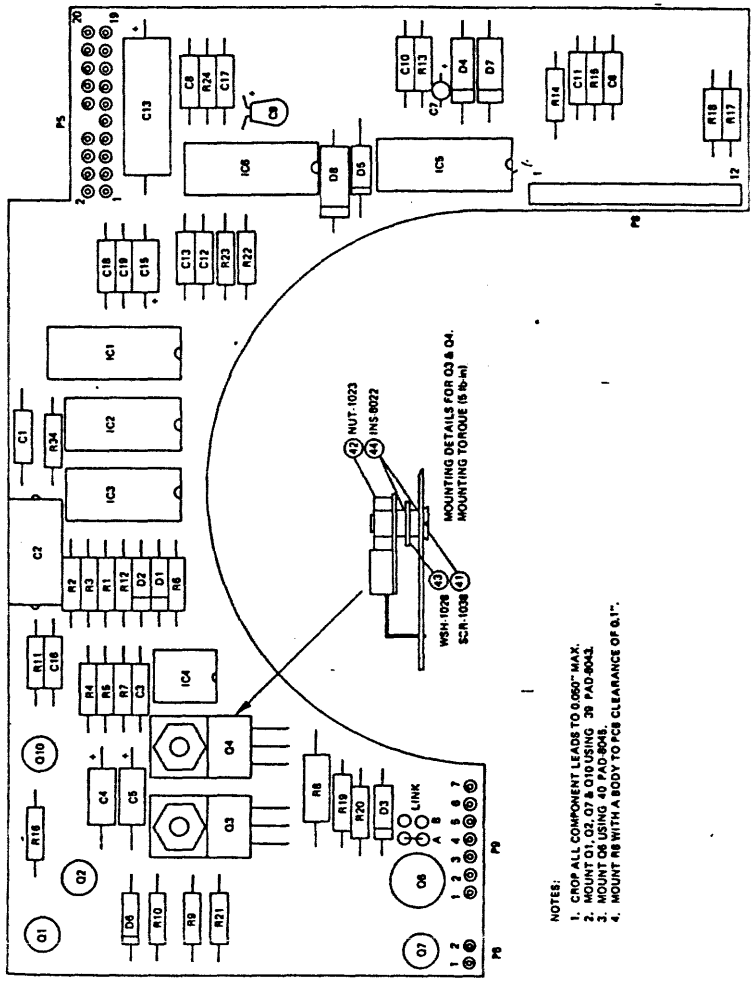


FIGURE 26(a)
Schematic Master Electronics Board

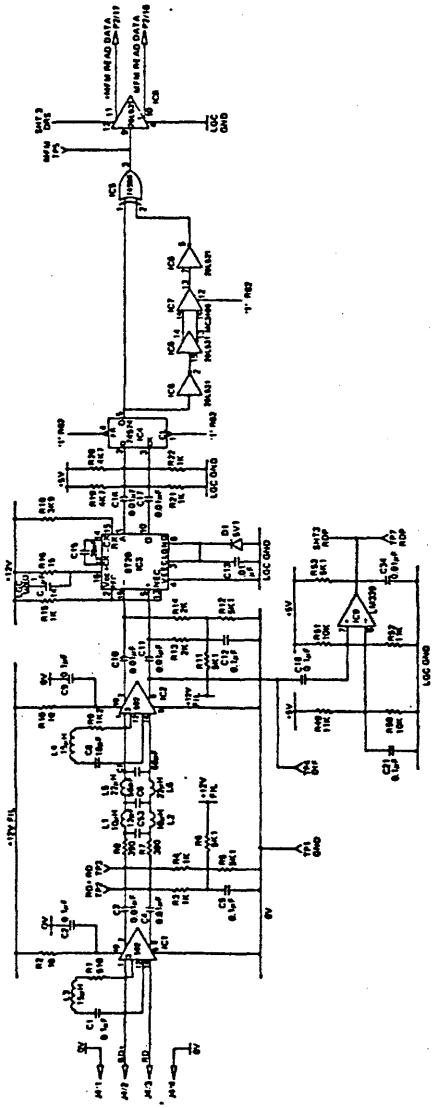


FIGURE 26(b)
Schematic Master Electronics Board

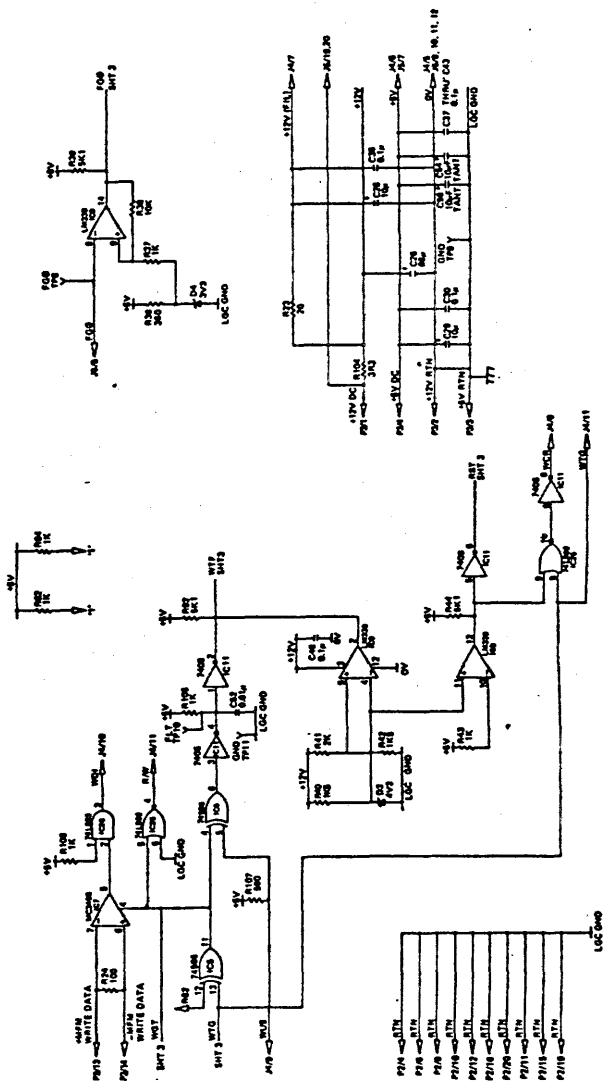


FIGURE 26(c)
Schematic Master Electronics Board

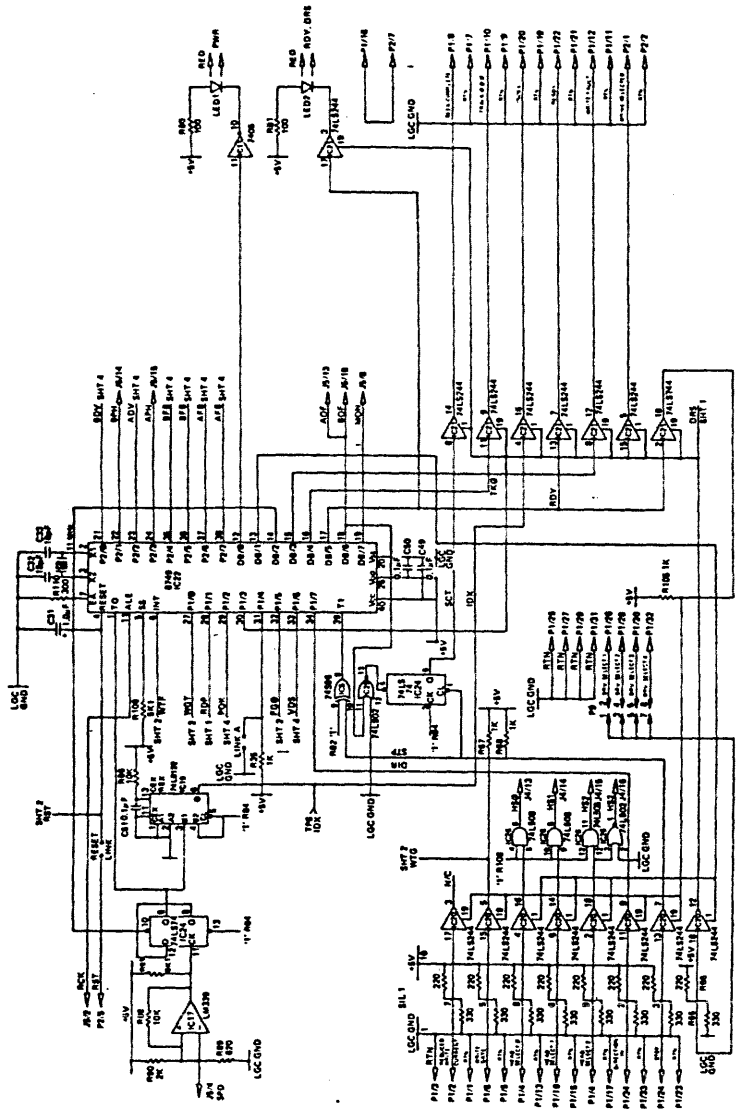


FIGURE 26(d)
Schematic Master Electronics Board

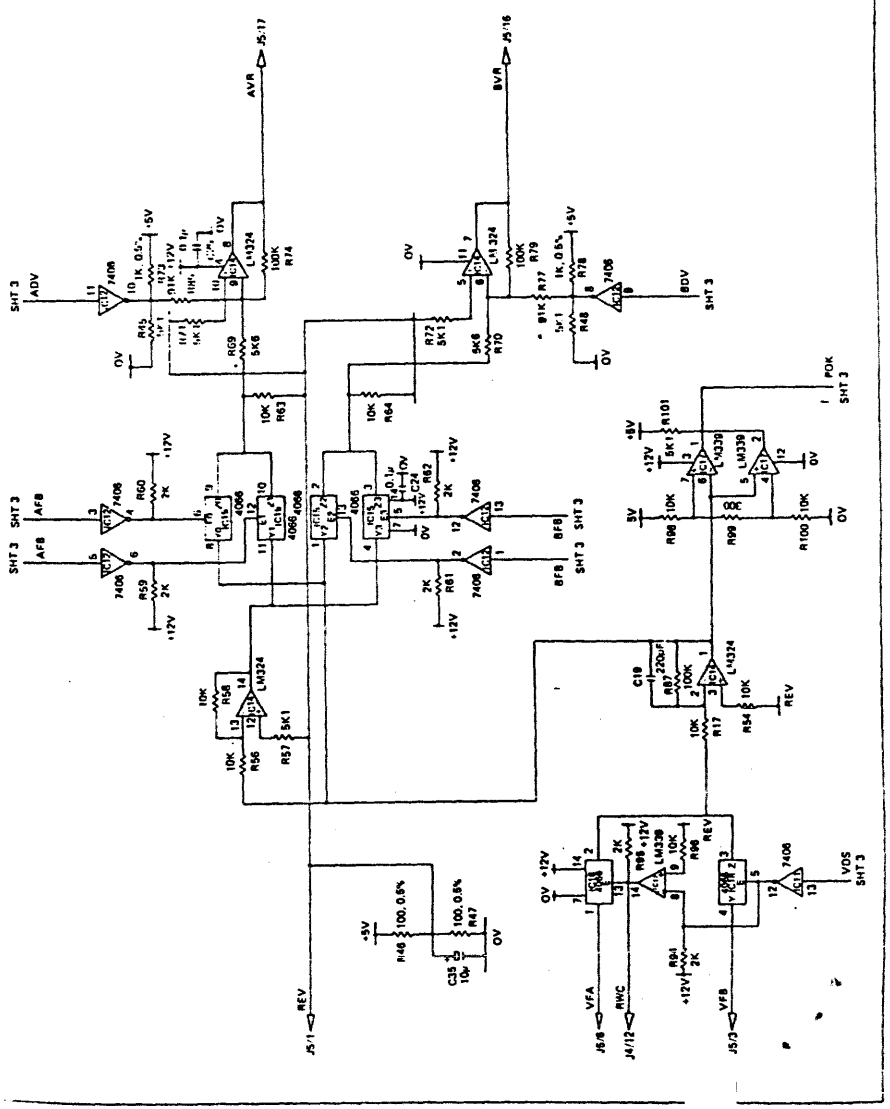


FIGURE 27
Schematic pre-amplifier board

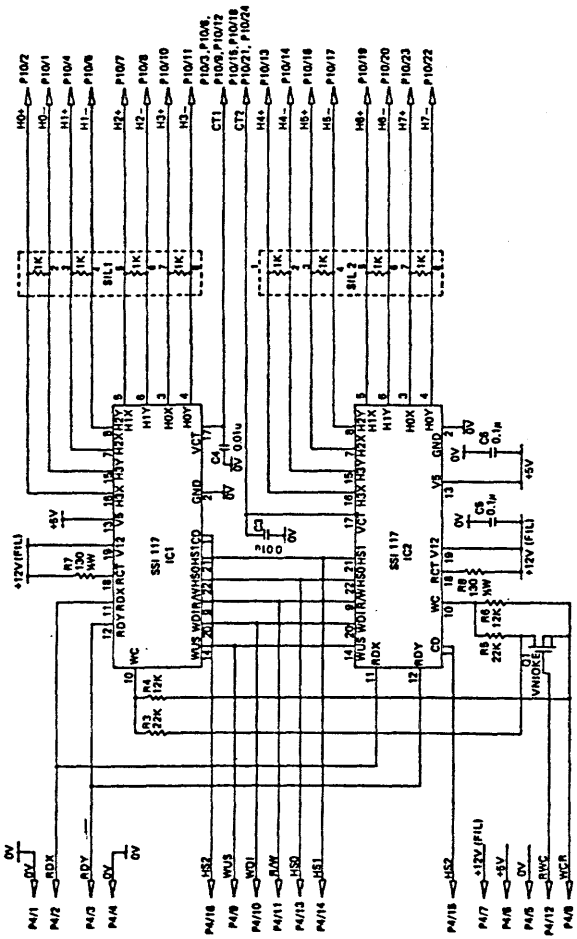


FIGURE 28
Schematic motor speed control board