United States Patent [19]

Graham et al.

[11] **Patent Number: 4,819,153**

[45] **Date of Patent: Apr. 4, 1989**

[54] **MICROPROCESSOR CONTROLLED RIGID DISK FILE SUBSYSTEM**

[75] Inventors: **Randolph H. Graham**, Fremont; **Bruce R. Peterson**, San Jose; **Richard J. Blackborow**, Cupertino, all of Calif.

[73] Assignee: **Plus Development Corporation**, Milpitas, Calif.

[21] Appl. No.: **741,588**

[22] Filed: **Jun. 5, 1985**

[51] **Int. Cl.**[4] **G06F 1/00**; G11B 5/012

[52] **U.S. Cl.** **362/200**; 360/99.08; 360/75; 360/77.04; 360/78.05

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 360/75, 97-99, 77

[56] **References Cited**

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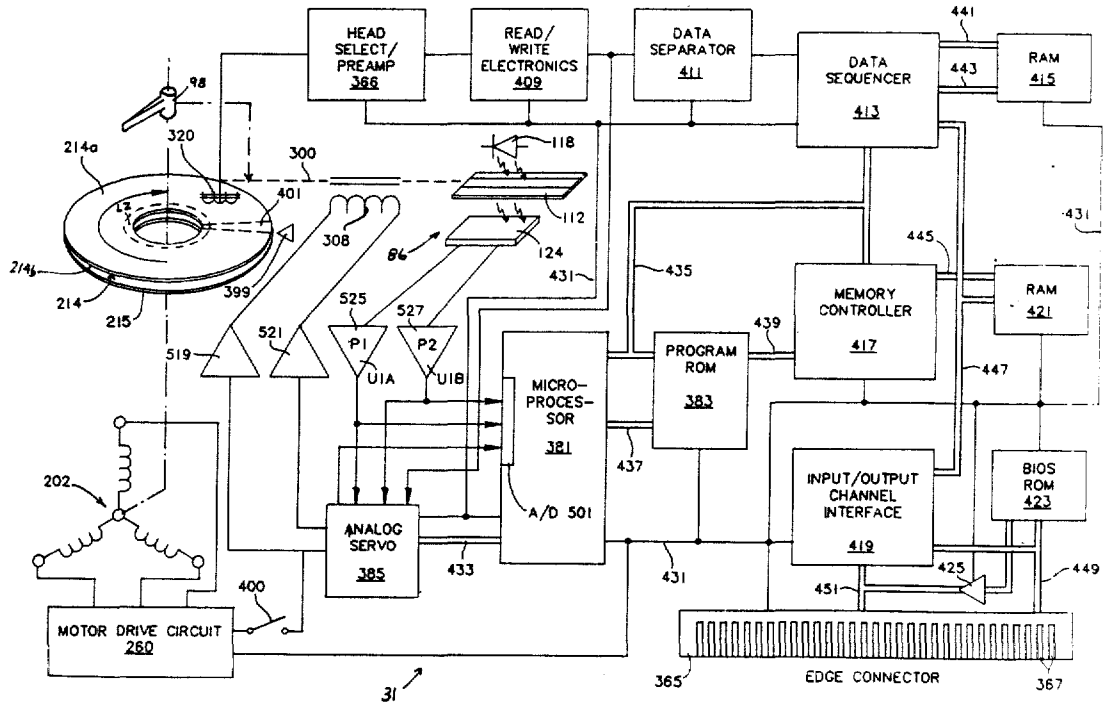
Primary Examiner—Gary V. Harkcom
Assistant Examiner—Christopher H. Lynt
Attorney, Agent, or Firm—David B. Harrison

[57] **ABSTRACT**

An improved control system for a disk file includes head position control circuitry including at least one servo loop for controlling an electromechanical head positioner relative to a rotating data storage disk, a data controller for controlling reading and writing of data blocks from and to a storage surface of the disk, an interface circuit for connecting the disk file directly to data, address and control buses of a host computer, and a single microprocessor programmed to supervise operations of the head position control circuitry, data controller and interface circuit.

38 Claims, 21 Drawing Sheets



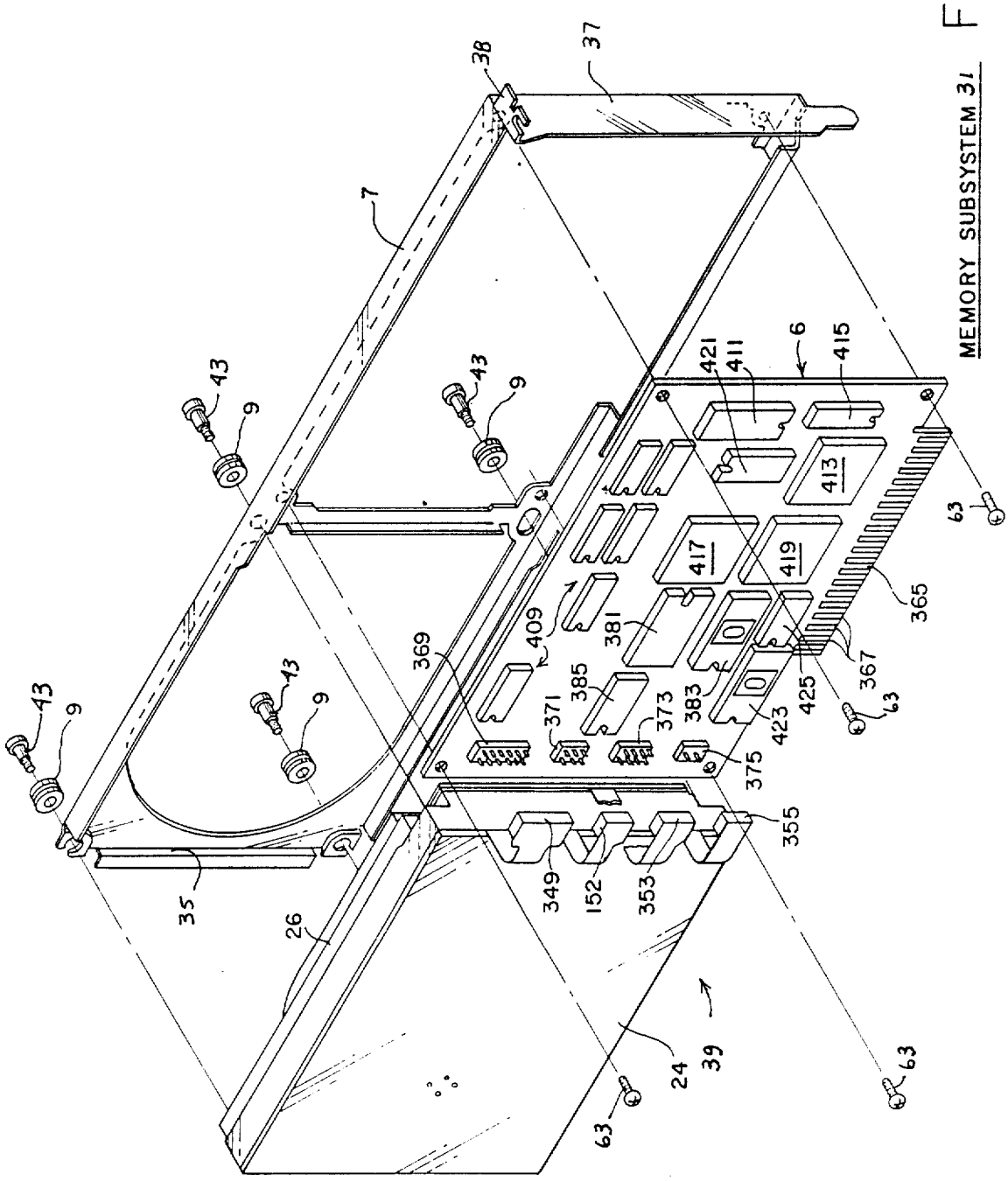

MEMORY SUBSYSTEM 31
38
37
7
43
9
6
421
411
415
413
417
419
409
381
369
385
371
373
383
423
425
367
365
63
375
355
349
152
353
35
26
24
39

FIG. 1

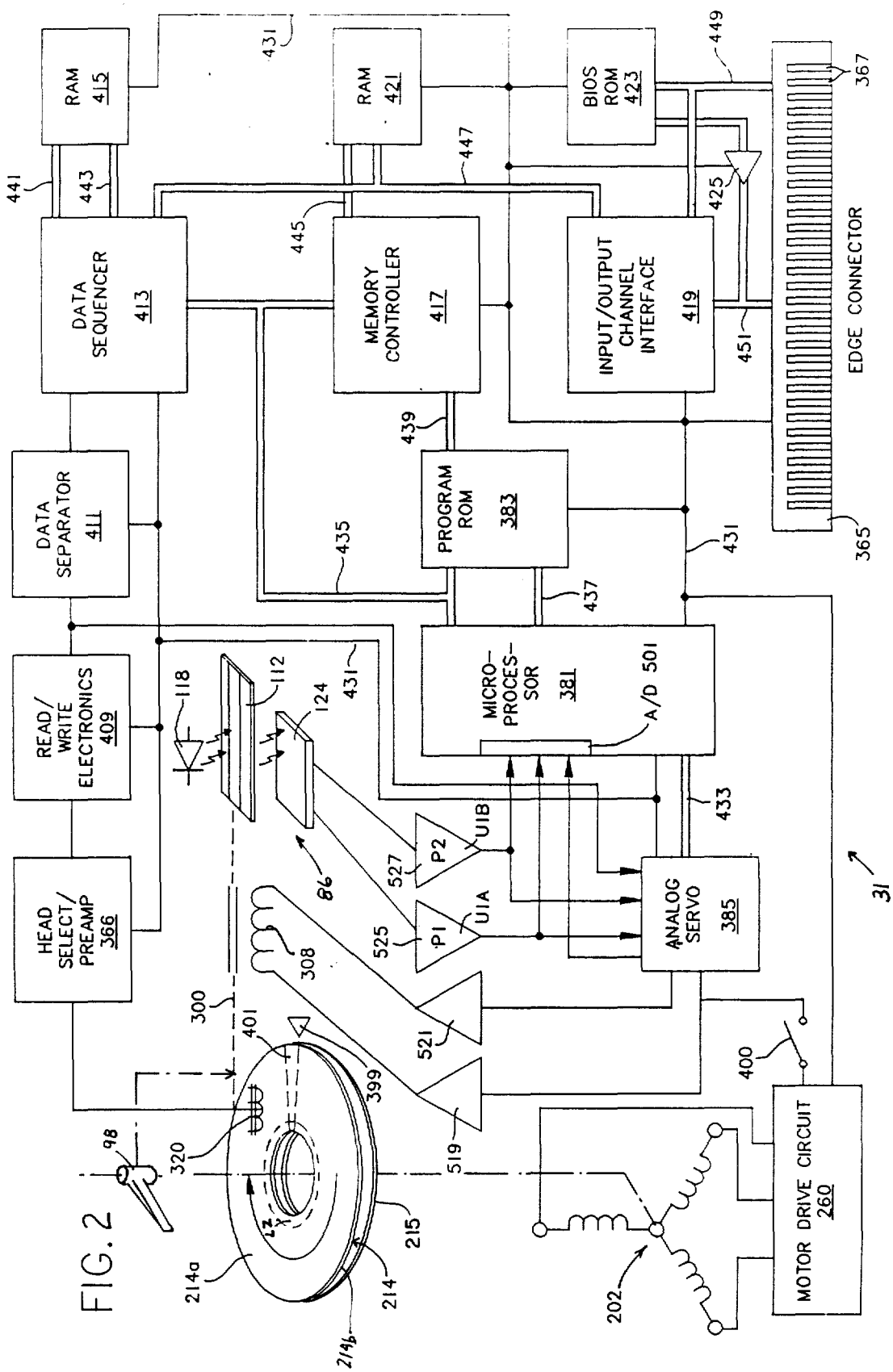

RAM 415
RAM 421
BIOS ROM 423
DATA SEQUENCER 413
MEMORY CONTROLLER 417
INPUT/OUTPUT CHANNEL INTERFACE 419
EDGE CONNECTOR
DATA SEPARATOR 411
PROGRAM ROM 383
READ/WRITE ELECTRONICS 409
MICRO-PROCES-SOR 381
A/D 501
HEAD SELECT/PREAMP 366
ANALOG SERVO 385
MOTOR DRIVE CIRCUIT 260
P1
P2
U1A
U1B
31
86
98
112
118
124
214
214a
214b
215
300
308
320
399
400
401
202
425
431
433
435
437
439
441
443
445
447
449
451
365
367
521
525
527
519

FIG. 2

FIG. 3

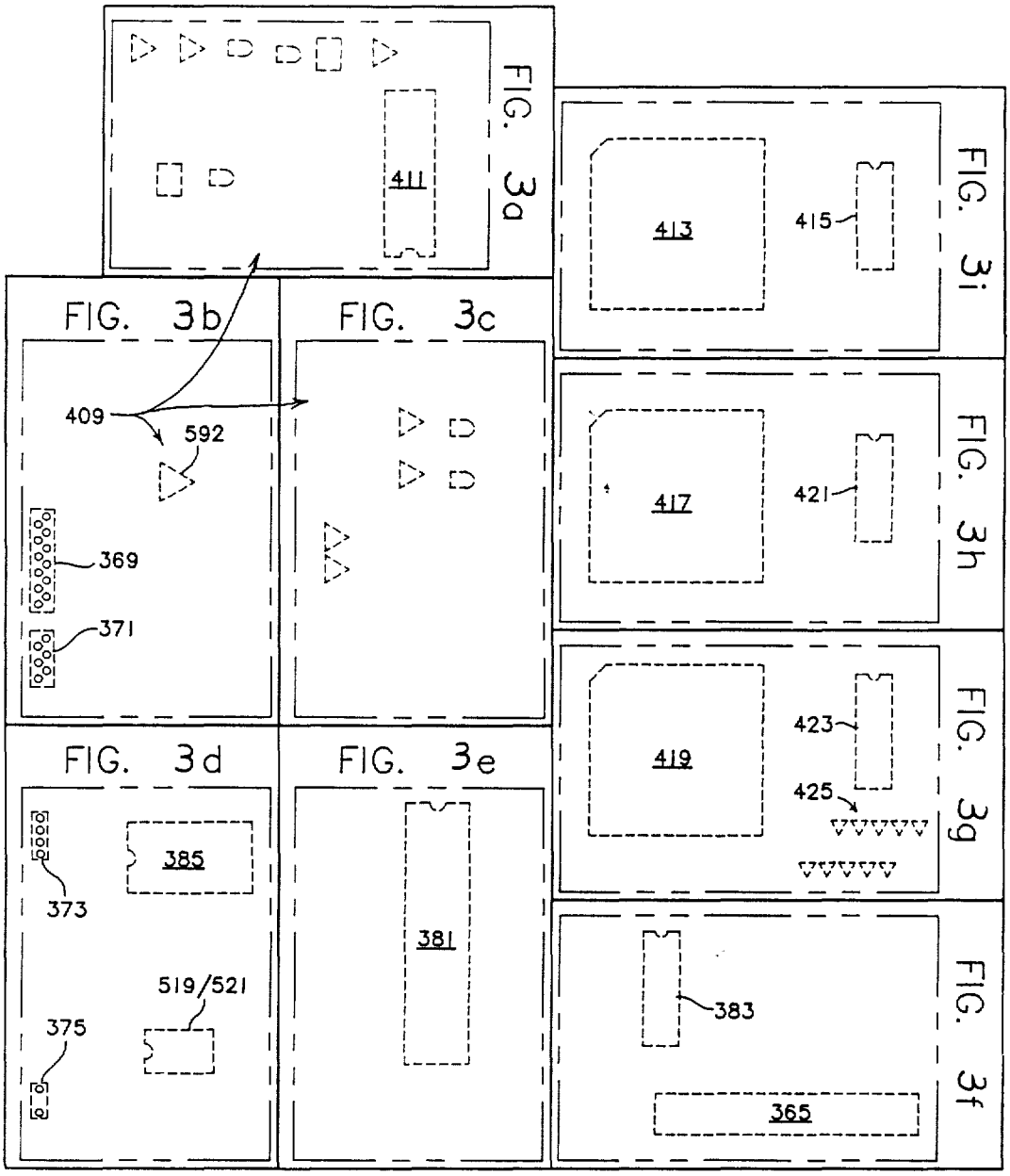


FIG. 3a
411
FIG. 3i
413
415
FIG. 3b
409
592
369
371
FIG. 3c
FIG. 3h
417
421
FIG. 3d
373
385
519/521
375
FIG. 3e
381
FIG. 3g
419
423
425
FIG. 3f
383
365

FIG. 3a

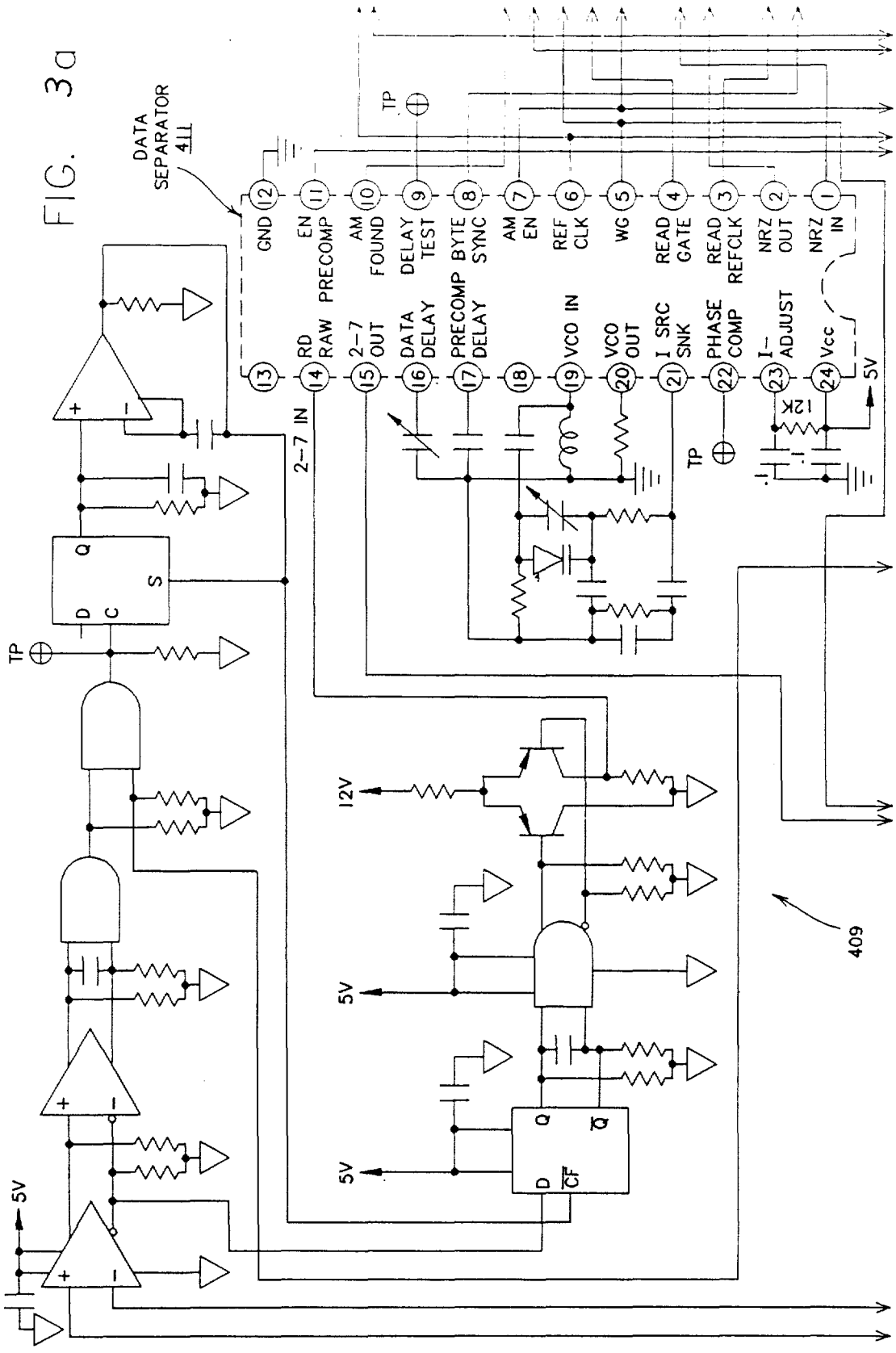
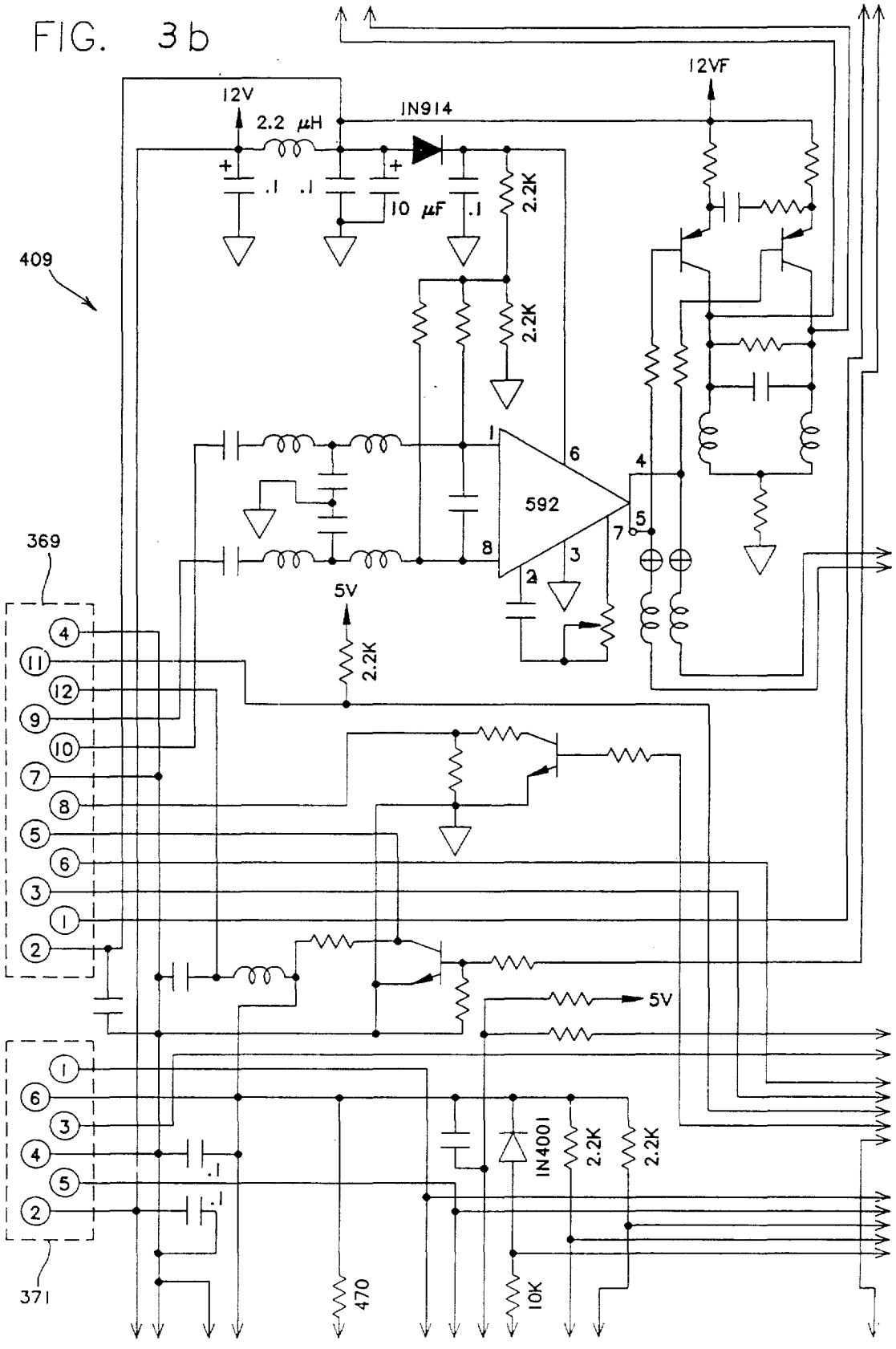

DATA SEPARATOR 411
GND
EN PRECOMP
AM FOUND
DELAY TEST
BYTE SYNC
AM EN
REF CLK
WG
READ GATE
READ REFCLK
NRZ OUT
NRZ IN
RD RAW
2-7 OUT
DATA DELAY
PRECOMP DELAY
VCO IN
VCO OUT
I SRC SNK
PHASE COMP
I- ADJUST
Vcc
2-7 IN
TP
5V
12V
12K
409

FIG. 3b


12V
2.2 μH
IN914
12VF
.1
.1
10 μF
.1
2.2K
2.2K
409
592
1
6
4
5
7
8
3
2
5V
2.2K
369
4
11
12
9
10
7
8
5
6
3
1
2
5V
1
6
3
4
5
2
.1
.1
IN4001
2.2K
2.2K
371
470
10K

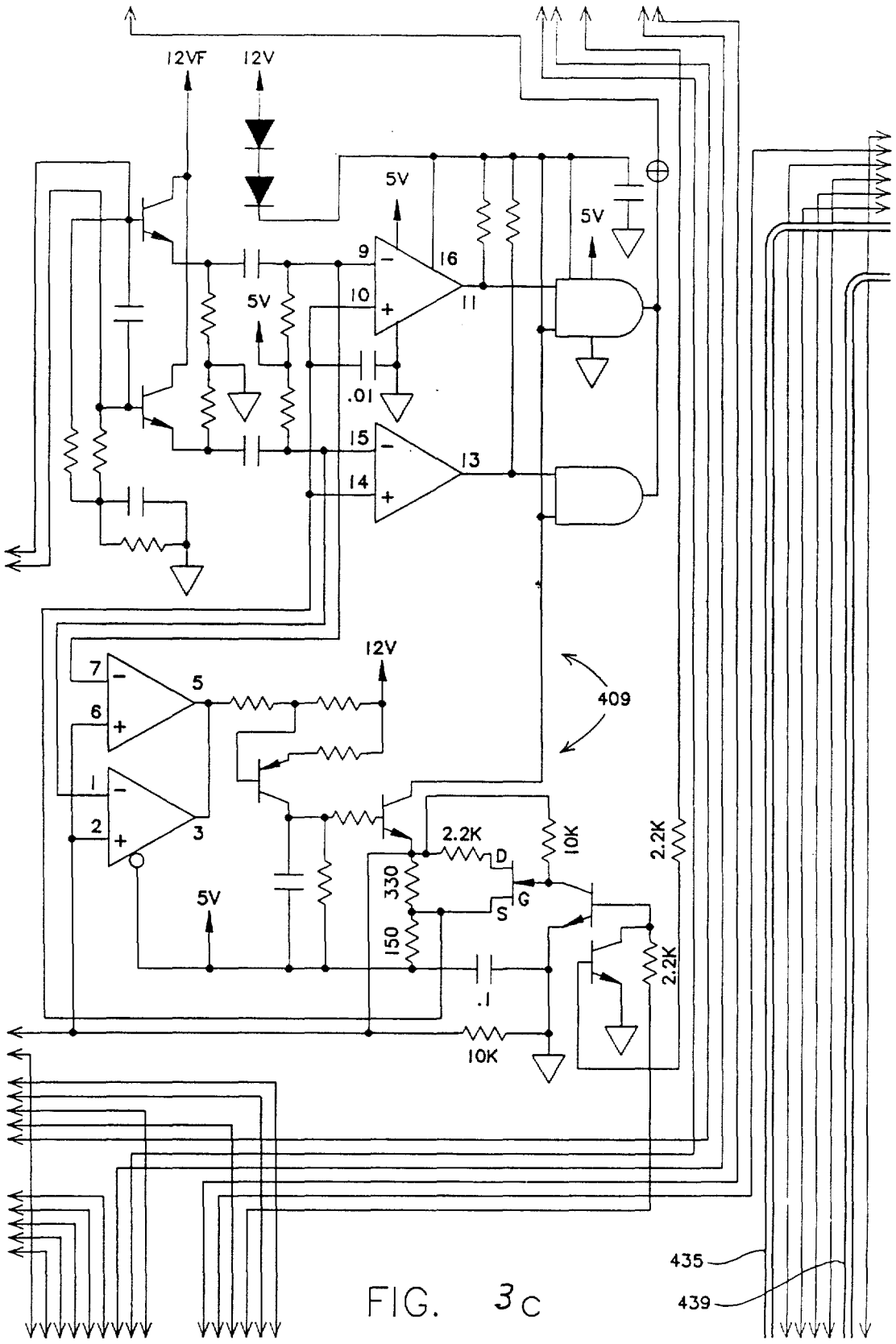

12VF
12V
5V
5V
5V
9
10
16
11
.01
15
14
13
12V
7
6
5
1
2
3
409
2.2K
10K
2.2K
330
150
D
G
S
5V
.1
2.2K
10K
435
439

FIG. 3C

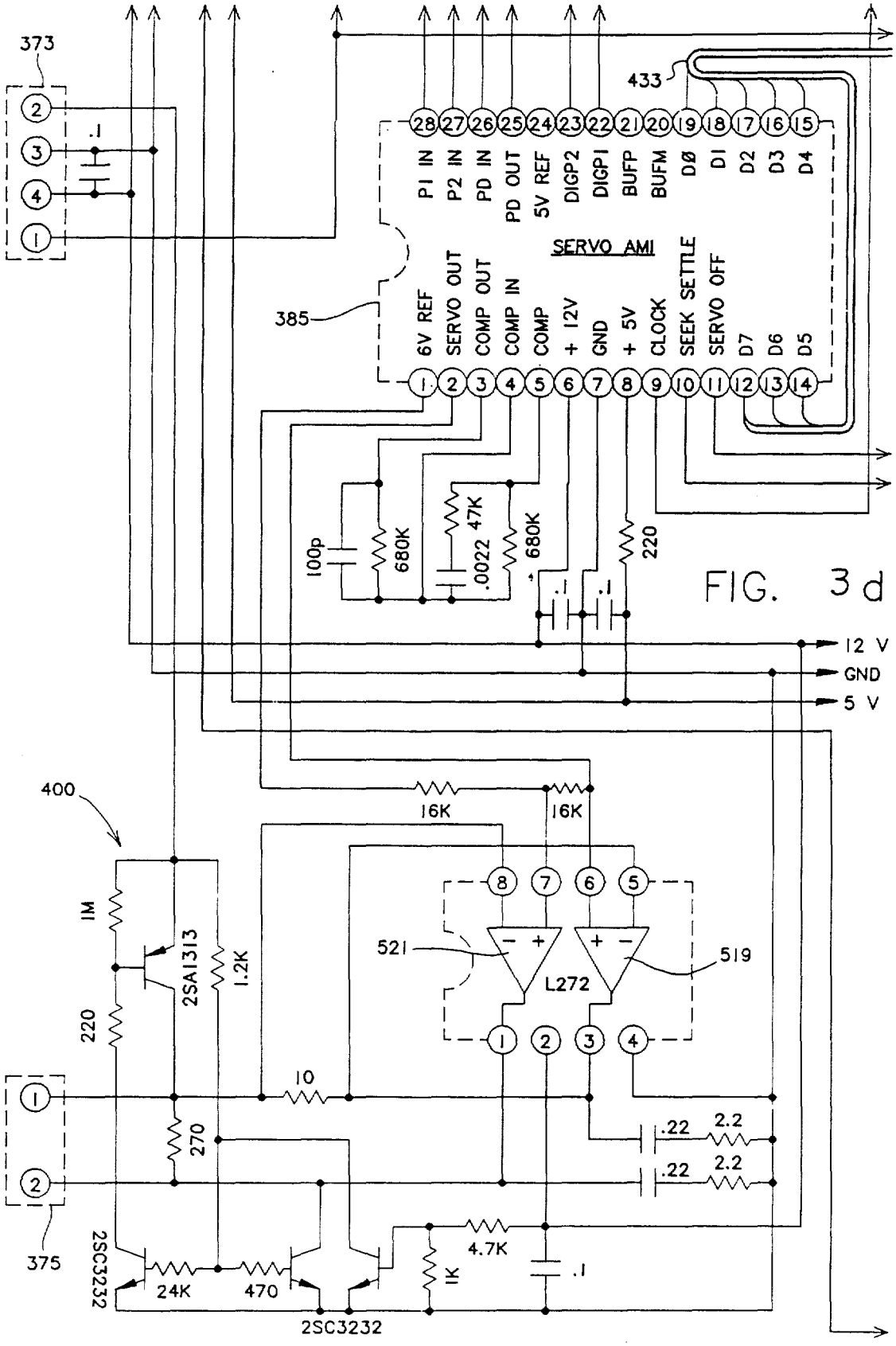

373
433
385
SERVO AMI
P1 IN
P2 IN
PD IN
PD OUT
5V REF
DIGP2
DIGP1
BUFP
BUFM
D0
D1
D2
D3
D4
6V REF
SERVO OUT
COMP OUT
COMP IN
COMP
+ 12V
GND
+ 5V
CLOCK
SEEK SETTLE
SERVO OFF
D7
D6
D5
100p
680K
47K
.0022
680K
220
.1
.1
12 V
GND
5 V
400
16K
16K
1M
2SA1313
1.2K
220
521
519
L272
10
270
.22
2.2
.22
2.2
375
2SC2232
24K
470
4.7K
1K
.1
2SC3232

FIG. 3d

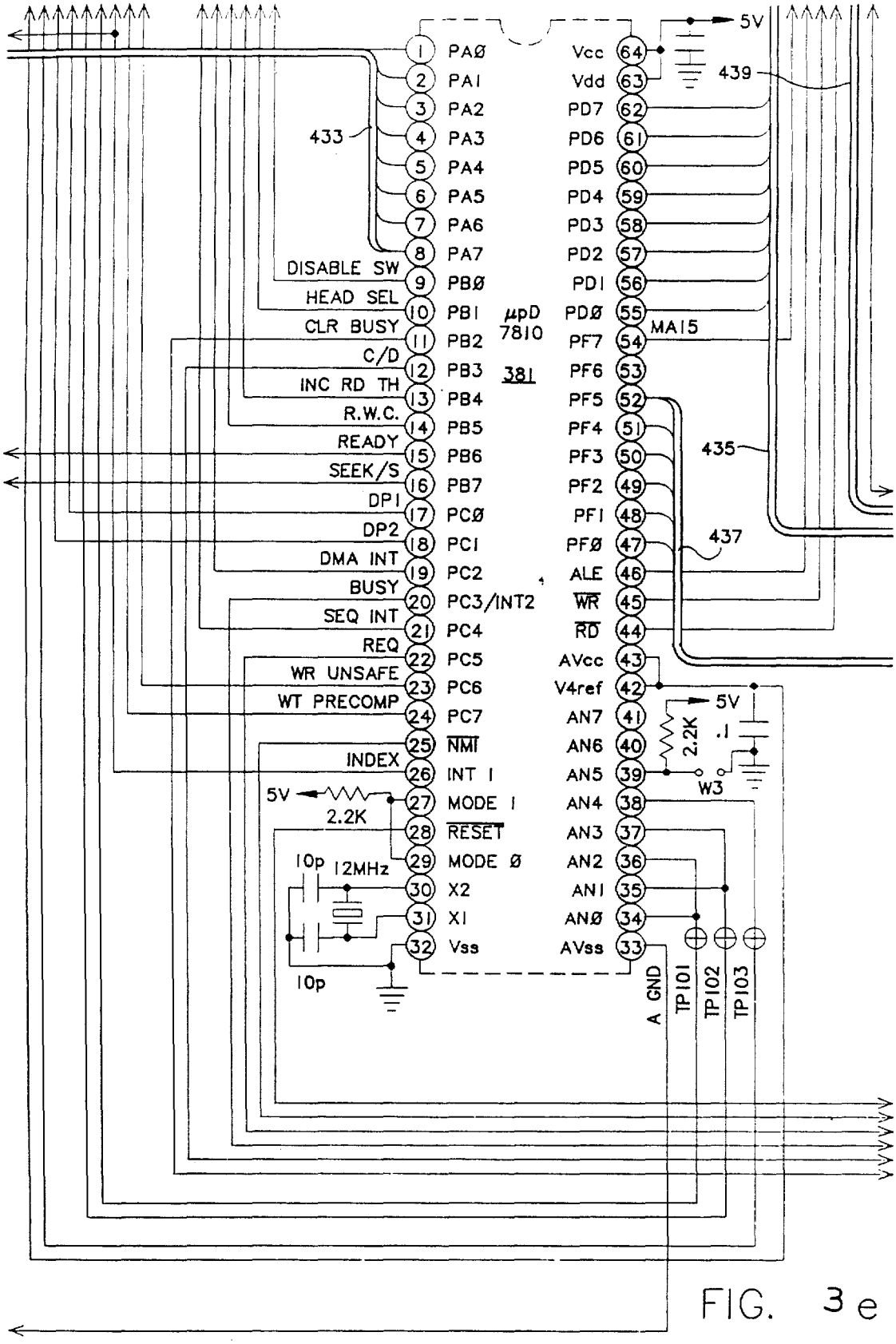
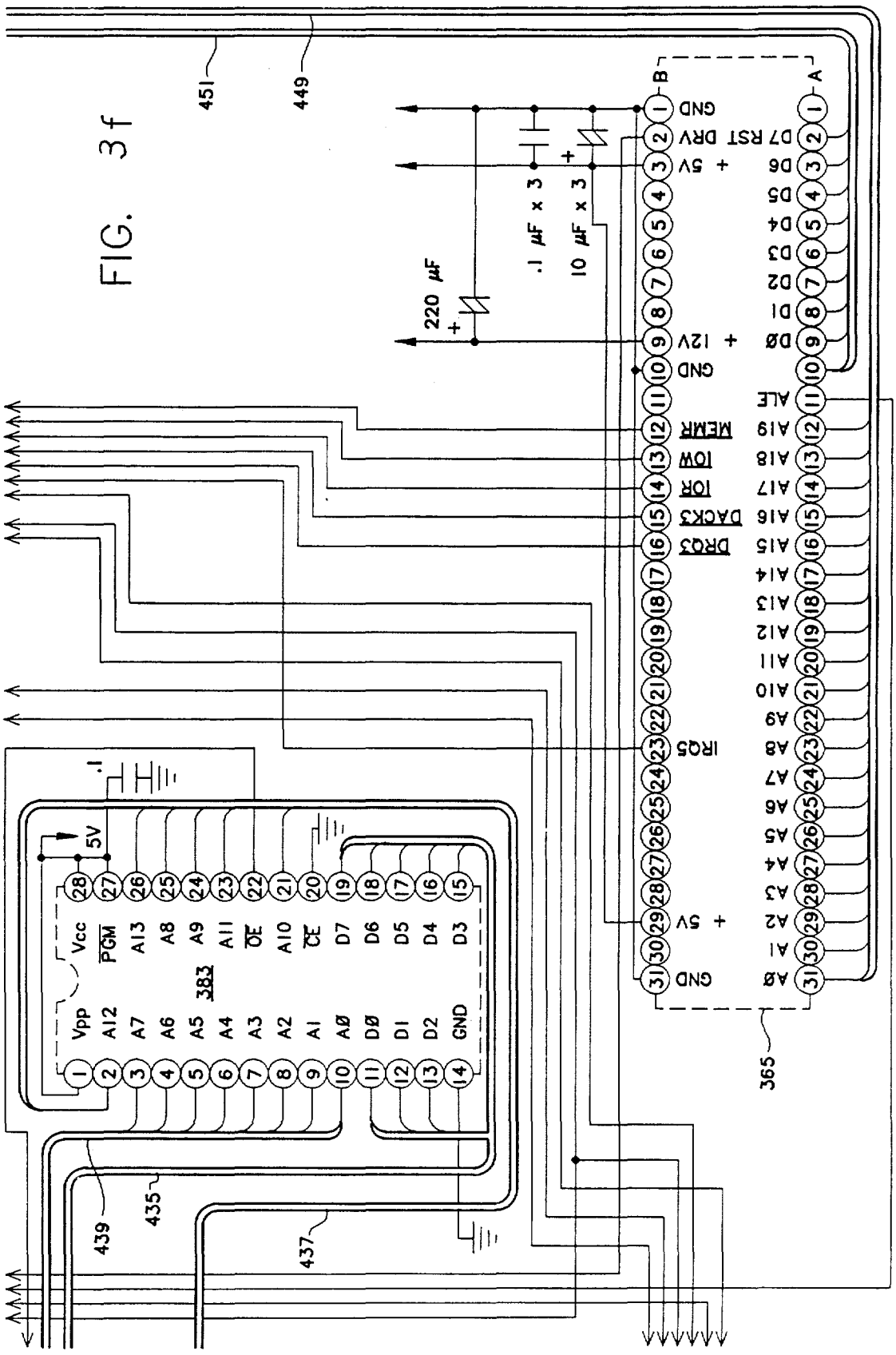

5V
439
433
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3/INT2
PC4
PC5
PC6
PC7
NMI
INT 1
MODE 1
RESET
MODE 0
X2
X1
Vss
Vcc
Vdd
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
PF7
PF6
PF5
PF4
PF3
PF2
PF1
PF0
ALE
WR
RD
AVcc
V4ref
AN7
AN6
AN5
AN4
AN3
AN2
AN1
AN0
AVss
μPD 7810
381
DISABLE SW
HEAD SEL
CLR BUSY
C/D
INC RD TH
R.W.C.
READY
SEEK/S
DP1
DP2
DMA INT
BUSY
SEQ INT
REQ
WR UNSAFE
WT PRECOMP
INDEX
MA15
435
437
2.2K
.1
W3
10p
12MHz
A GND
TP101
TP102
TP103

FIG. 3e

FIG. 3f


451
449
GND
D7 RST DRV
+ 5V
D6
D5
D4
D3
D2
D1
D0 + 12V
GND
ALE
A19 MEMR
A18 IOW
A17 IOR
A16 DACK3
A15 DRQ3
A14
A13
A12
A11
A10
A9
A8 IRQ5
A7
A6
A5
A4
A3
A2 + 5V
A1
A0 GND
365
220 µF
.1 µF x 3
10 µF x 3
.1
5V
Vcc PGM A13 A8 A9 A11 OE A10 CE D7 D6 D5 D4 D3
Vpp A12 A7 A6 A5 383 A4 A3 A2 A1 A0 D0 D1 D2 GND
439
435
437

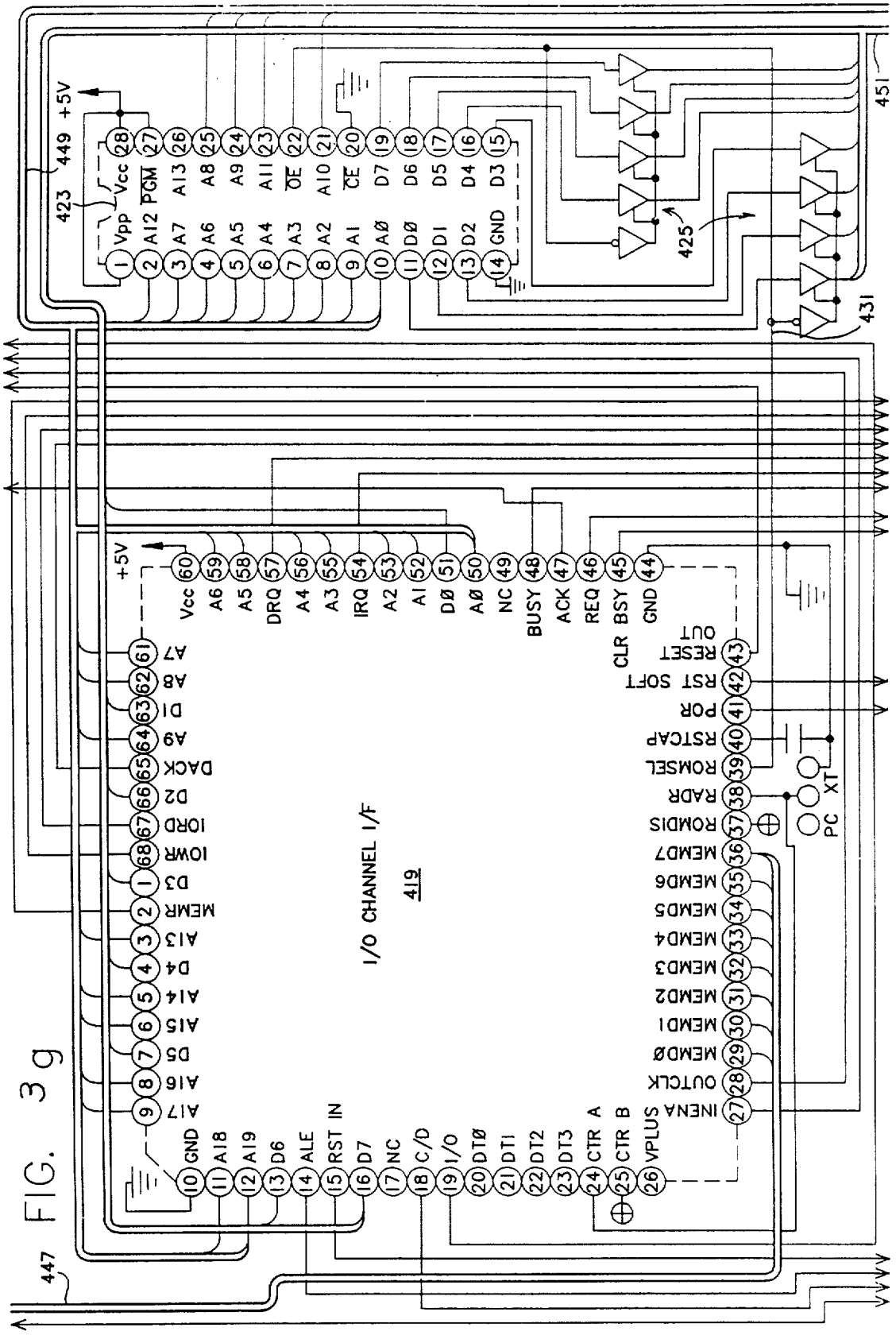

+5V
449
423
451
425
431
447
I/O CHANNEL I/F
419
Vpp
A12
A7
A6
A5
A4
A3
A2
A1
A0
D0
D1
D2
GND
Vcc
PGM
A13
A8
A9
A11
OE
A10
CE
D7
D6
D5
D4
D3
A7
A8
DI
A9
DACK
D2
IORD
IOWR
D3
MEMR
A13
D4
A14
A15
D5
A16
A17
GND
A18
A19
D6
ALE
RST IN
D7
NC
C/D
I/O
DT0
DT1
DT2
DT3
CTR A
CTR B
VPLUS
Vcc
A6
A5
DRQ
A4
A3
IRQ
A2
A1
D0
A0
NC
BUSY
ACK
REQ
BSY
GND
CLR
RESET OUT
RST SOFT
POR
RSTCAP
ROMSEL
RADR
ROMDIS
MEMD7
MEMD6
MEMD5
MEMD4
MEMD3
MEMD2
MEMD1
MEMD0
OUTCLK
INENA
PC XT

FIG. 3g

FIG. 3h

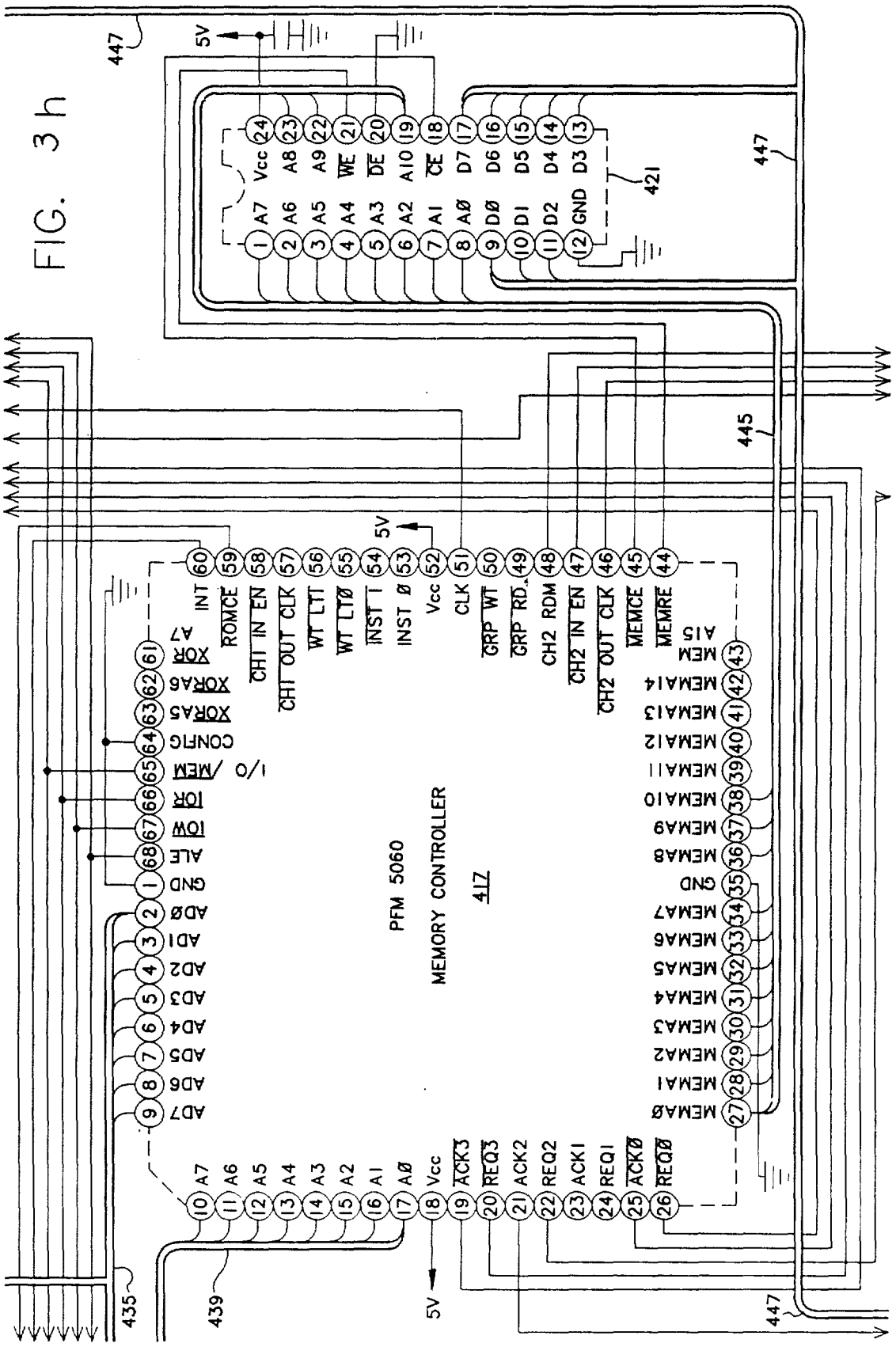
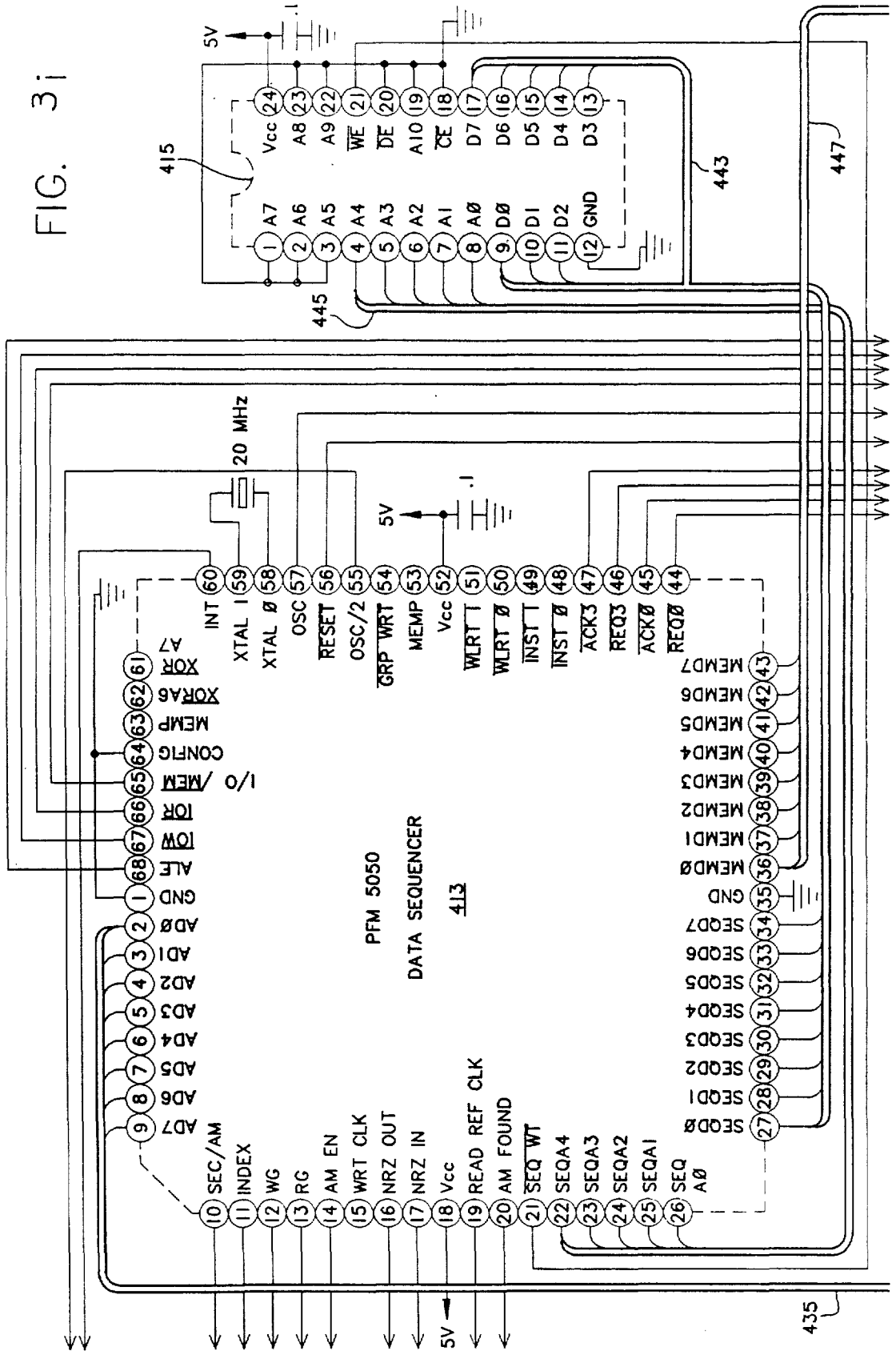

PFM 5060
MEMORY CONTROLLER
417
421
445
447
435
439
5V
Vcc
A7
A6
A5
A4
A3
A2
A1
A0
D0
D1
D2
GND
D3
D4
D5
D6
D7
WE
OE
A10
A9
A8
INT
ROMCE
CH1 IN EN
CH1 OUT CLK
WT LT1
WT LT0
INST 1
INST 0
CLK
GRP WT
GRP RD
CH2 RDM
CH2 IN EN
CH2 OUT CLK
MEMCE
MEMRE
A15
MEMA14
MEMA13
MEMA12
MEMA11
MEMA10
MEMA9
MEMA8
MEMA7
MEMA6
MEMA5
MEMA4
MEMA3
MEMA2
MEMA1
MEMA0
XOR A7
XOR A6
XOR A5
CONFIG
I/O / MEM
IOR
IOW
ALE
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
ACK3
REQ3
ACK2
REQ2
ACK1
REQ1
ACK0
REQ0

FIG. 3i


5V
.1
415
Vcc A8 A9 WE OE A10 CE D7 D6 D5 D4 D3
A7 A6 A5 A4 A3 A2 A1 A0 D0 D1 D2 GND
443
447
445
20 MHz
INT XTAL 1 XTAL 0 OSC RESET OSC/2 GRP WRT MEMP Vcc WLRT 1 WLRT 0 INST 1 INST 0 ACK3 REQ3 ACK0 REQ0
MEMD7 MEMD6 MEMD5 MEMD4 MEMD3 MEMD2 MEMD1 MEMD0
A7 XOR XORA6 MEMP CONFIG I/O /MEM IOR IOW ALE GND AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
PFM 5050
DATA SEQUENCER
413
SEC/AM INDEX WG RG AM EN WRT CLK NRZ OUT NRZ IN Vcc READ REF CLK AM FOUND SEQ WT SEQA4 SEQA3 SEQA2 SEQA1 SEQ A0
SEQD7 SEQD6 SEQD5 SEQD4 SEQD3 SEQD2 SEQD1 SEQD0
435

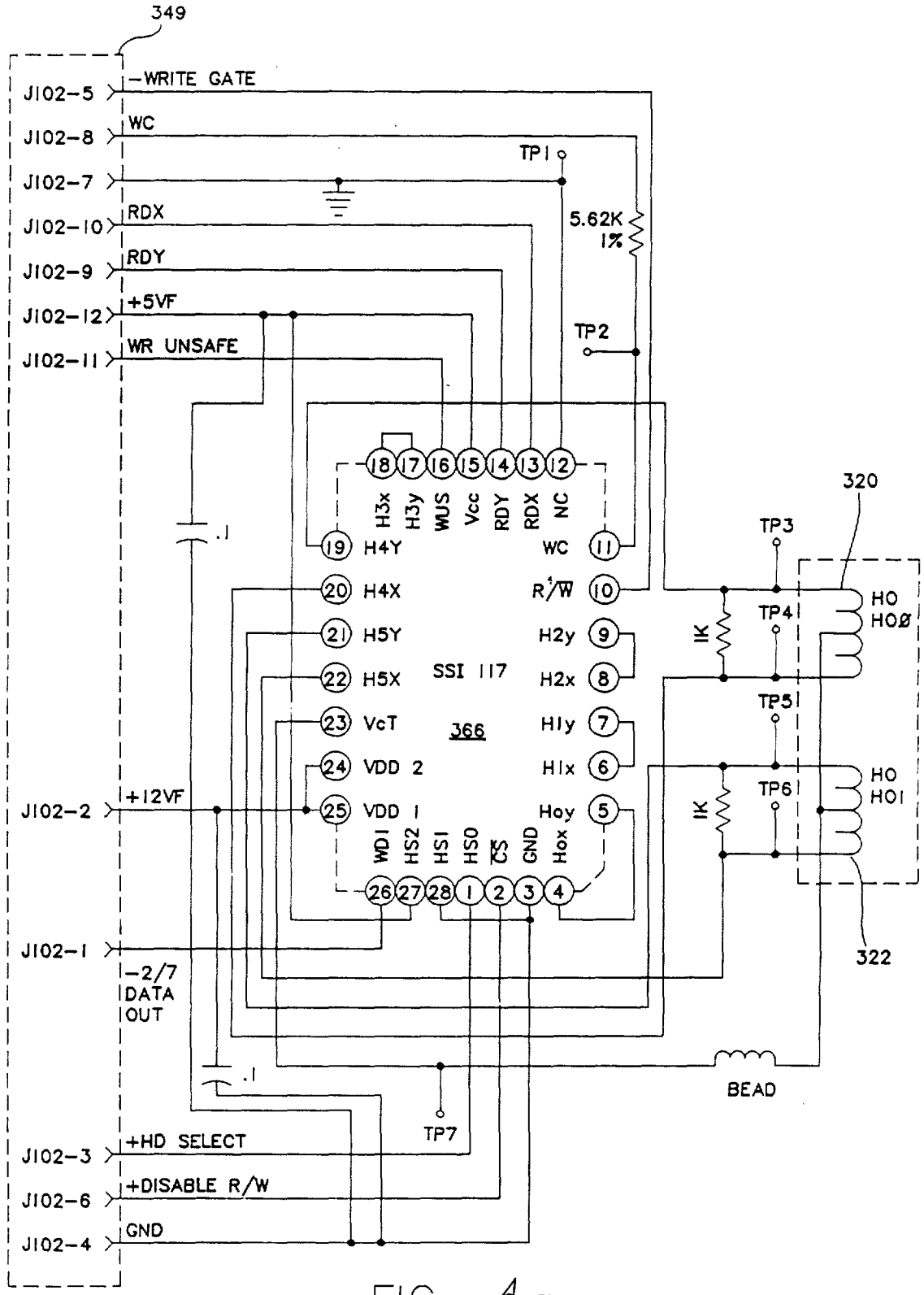

349
J102-5
-WRITE GATE
J102-8
WC
J102-7
J102-10
RDX
J102-9
RDY
J102-12
+5VF
J102-11
WR UNSAFE
TP1
5.62K 1%
TP2
18 17 16 15 14 13 12
H3x H3y WUS Vcc RDY RDX NC
19 H4Y
20 H4X
21 H5Y
22 H5X
23 VcT
24 VDD 2
25 VDD 1
WC 11
R/W 10
H2y 9
H2x 8
H1y 7
H1x 6
Hoy 5
SSI 117
366
WD1 HS2 HS1 HS0 CS GND Hox
26 27 28 1 2 3 4
.1
320
TP3
TP4
TP5
TP6
1K
HO
HOØ
HO1
322
BEAD
J102-2
+12VF
J102-1
-2/7 DATA OUT
TP7
J102-3
+HD SELECT
J102-6
+DISABLE R/W
J102-4
GND

FIG. 4a

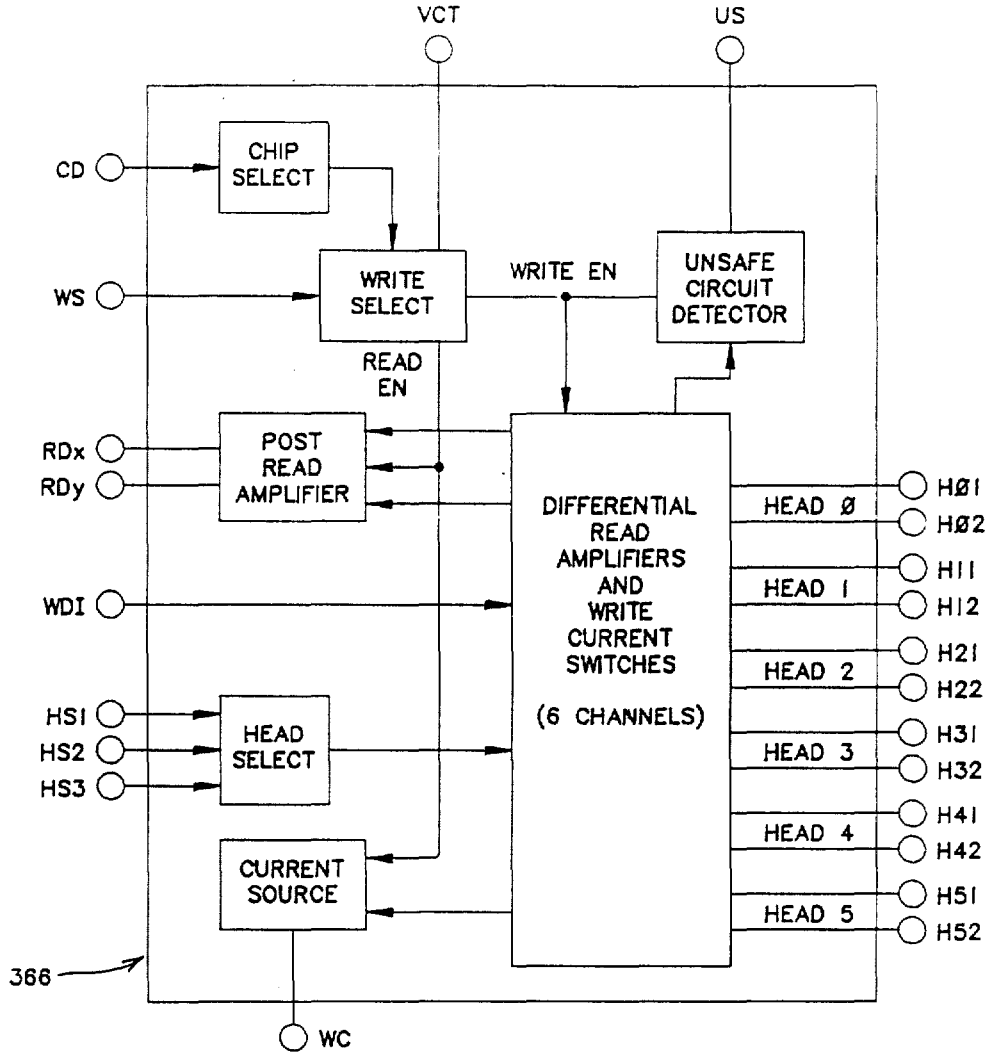

VCT
US
CD
CHIP SELECT
WS
WRITE SELECT
WRITE EN
UNSAFE CIRCUIT DETECTOR
READ EN
RDx
RDy
POST READ AMPLIFIER
DIFFERENTIAL READ AMPLIFIERS AND WRITE CURRENT SWITCHES
(6 CHANNELS)
HEAD Ø
HEAD 1
HEAD 2
HEAD 3
HEAD 4
HEAD 5
HØ1
HØ2
H11
H12
H21
H22
H31
H32
H41
H42
H51
H52
WDI
HS1
HS2
HS3
HEAD SELECT
CURRENT SOURCE
366
WC

FIG. 4b

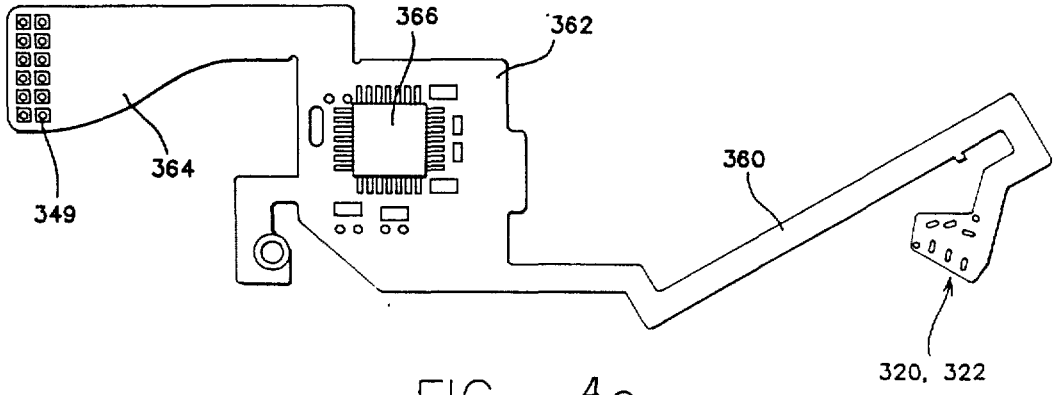

366
362
364
349
360
320, 322

FIG. 4c

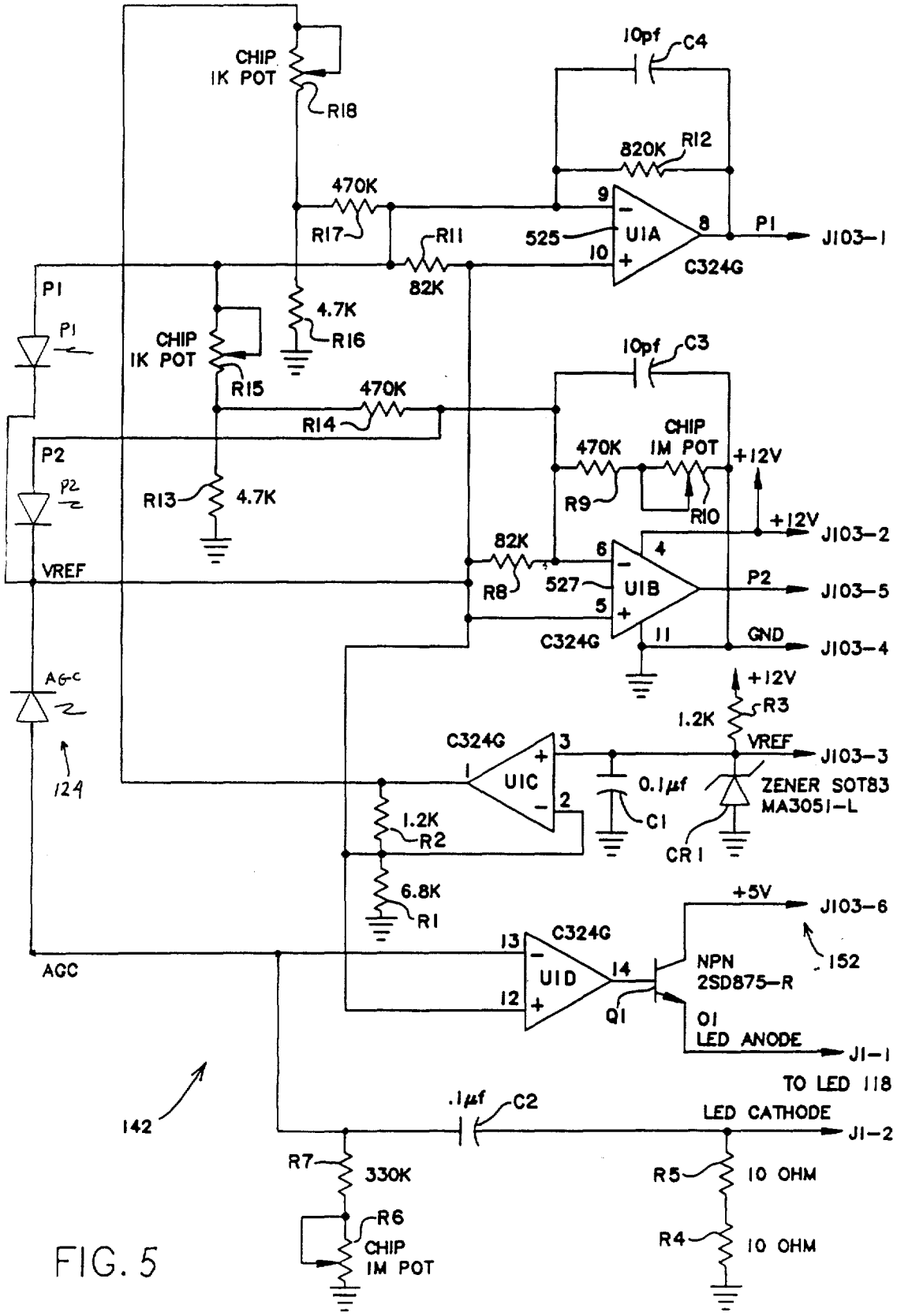
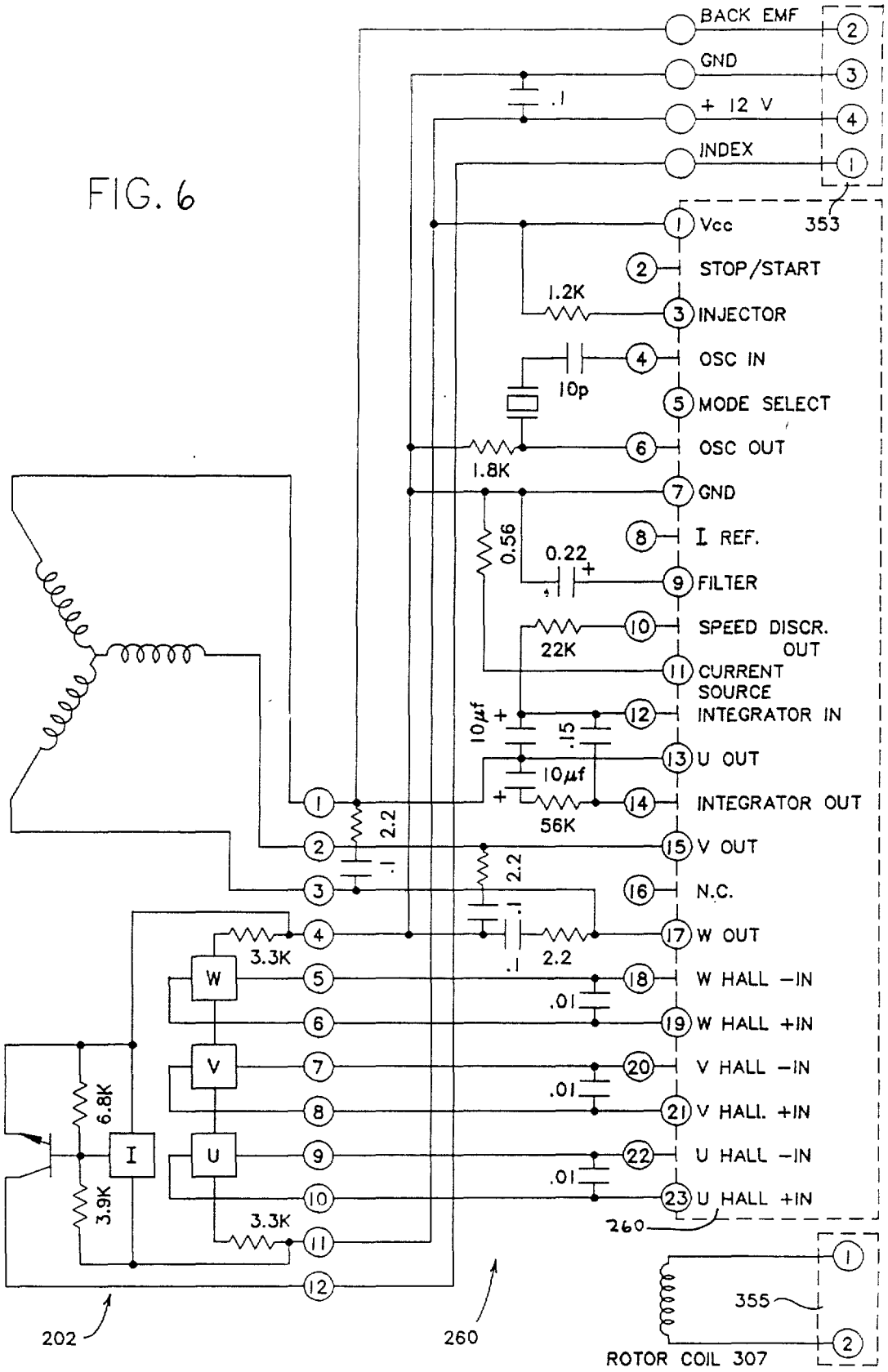

CHIP
1K POT
R18
10pf
C4
820K
R12
470K
R17
R11
525
U1A
C324G
P1
J103-1
82K
4.7K
R16
CHIP
1K POT
R15
10pf
C3
470K
R14
CHIP
1M POT
470K
R9
R10
+12V
P2
R13
4.7K
+12V
J103-2
82K
R8
527
U1B
P2
J103-5
VREF
C324G
GND
J103-4
AGC
+12V
R3
1.2K
C324G
U1C
VREF
J103-3
0.1μf
C1
ZENER SOT83
MA3051-L
CR1
1.2K
R2
6.8K
R1
+5V
J103-6
152
C324G
U1D
NPN
2SD875-R
Q1
01
LED ANODE
J1-1
TO LED 118
AGC
142
.1μf
C2
LED CATHODE
J1-2
R7
330K
R6
CHIP
1M POT
R5
10 OHM
R4
10 OHM

FIG. 5

FIG. 6


BACK EMF
GND
+ 12 V
INDEX
.1
353
Vcc
STOP/START
1.2K
INJECTOR
OSC IN
10p
MODE SELECT
OSC OUT
1.8K
GND
I REF.
0.56
0.22
FILTER
SPEED DISCR. OUT
22K
CURRENT SOURCE
INTEGRATOR IN
10μf
.15
U OUT
10μf
INTEGRATOR OUT
56K
2.2
.1
V OUT
2.2
.1
N.C.
3.3K
W OUT
.1
2.2
W HALL −IN
.01
W HALL +IN
V HALL −IN
.01
V HALL +IN
U HALL −IN
.01
U HALL +IN
3.3K
6.8K
3.9K
W
V
U
I
260
202
260
355
ROTOR COIL 307
HA13426

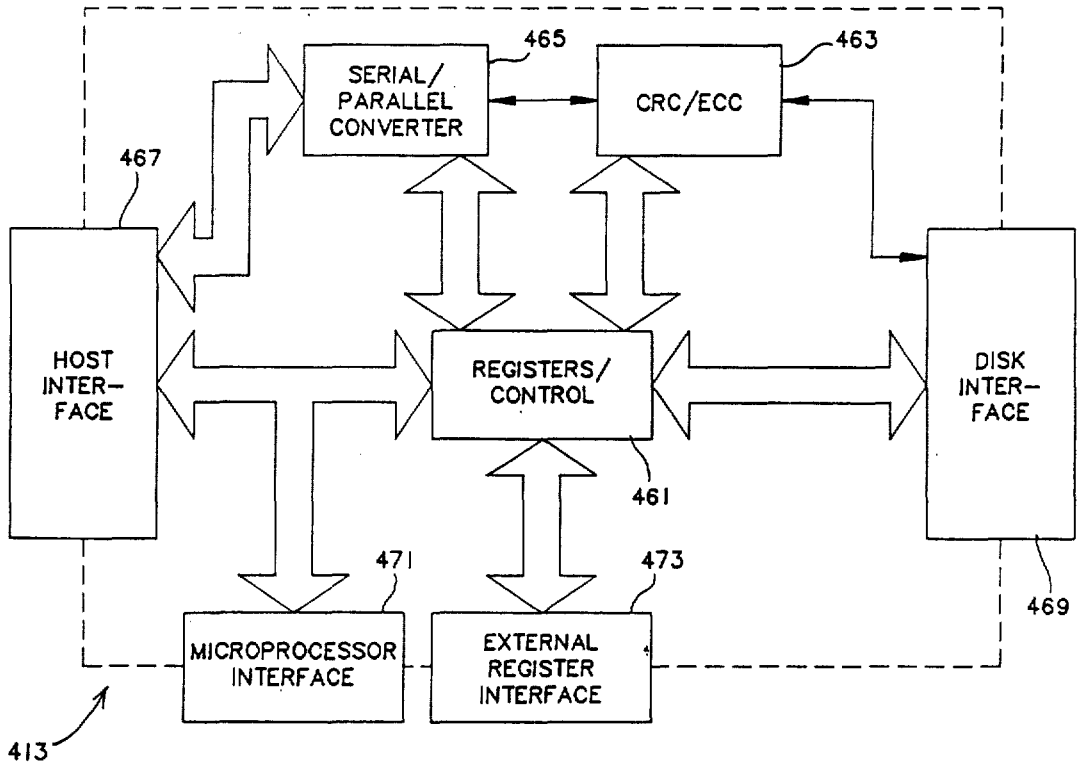

SERIAL/
PARALLEL
CONVERTER
465
CRC/ECC
463
467
HOST
INTER-
FACE
REGISTERS/
CONTROL
461
DISK
INTER-
FACE
469
471
473
MICROPROCESSOR
INTERFACE
EXTERNAL
REGISTER
INTERFACE
413

FIG. 7

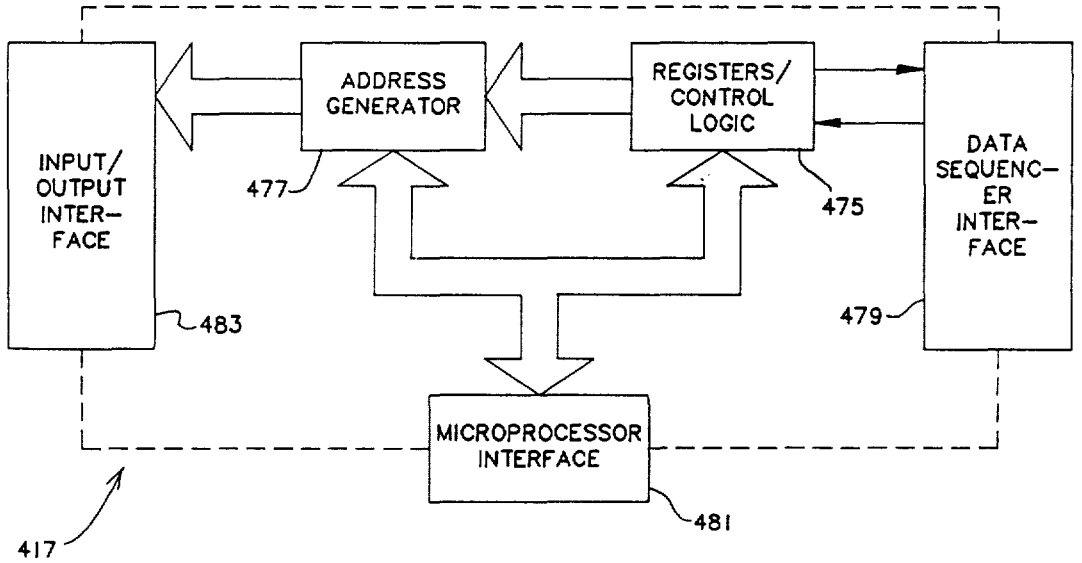

ADDRESS
GENERATOR
REGISTERS/
CONTROL
LOGIC
INPUT/
OUTPUT
INTER-
FACE
477
475
DATA
SEQUENC-
ER
INTER-
FACE
483
479
MICROPROCESSOR
INTERFACE
481
417

FIG. 8

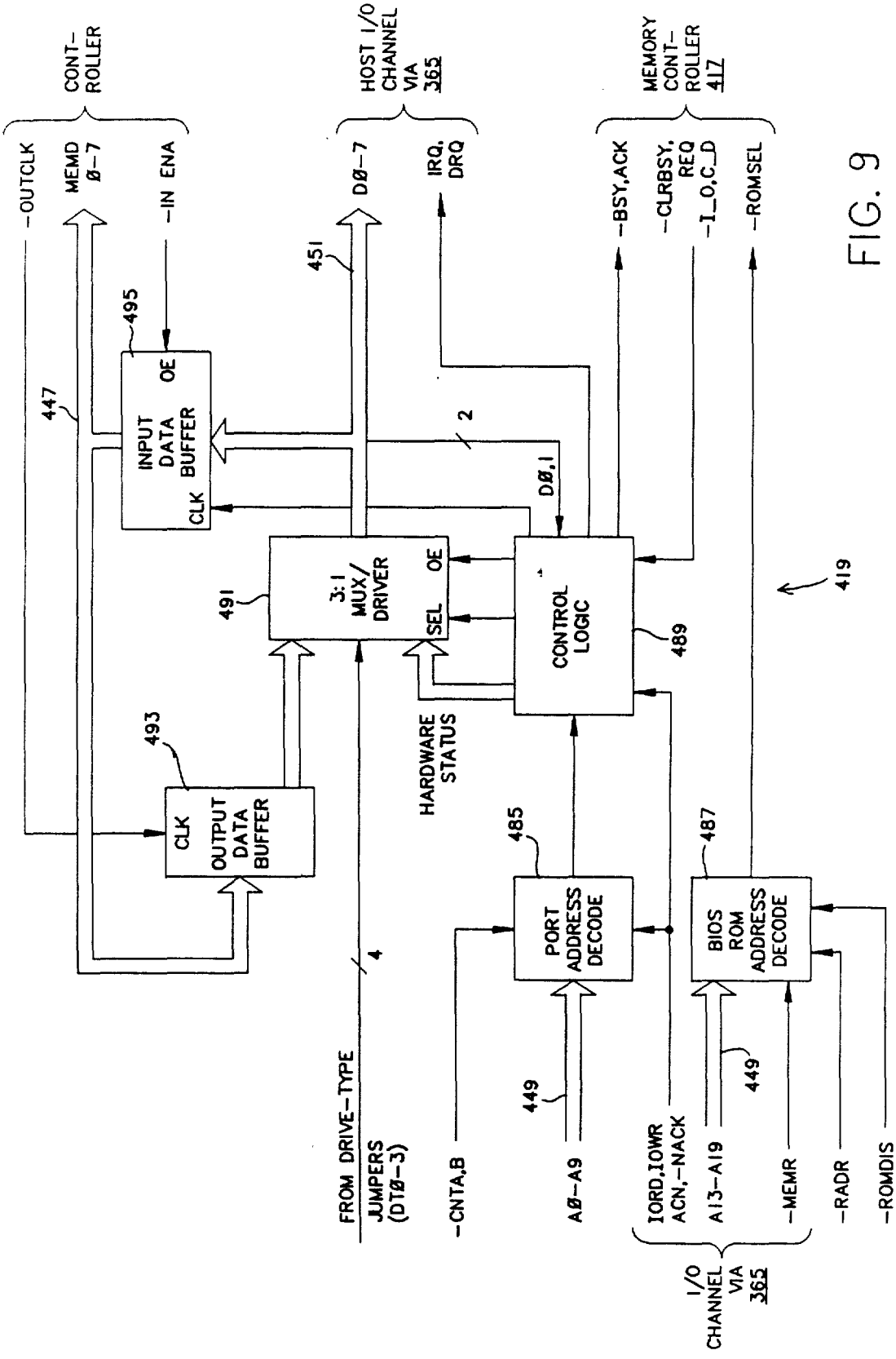

CONT-ROLLER
HOST I/O CHANNEL VIA 365
MEMORY CONT-ROLLER 417
-OUTCLK
MEMD Ø-7
-IN ENA
DØ-7
IRQ, DRQ
-BSY,ACK
-CLRBSY, REQ
-I_O,C_D
-ROMSEL
447
451
495
OE
INPUT DATA BUFFER
CLK
2
DØ,1
491
3:1 MUX/ DRIVER
OE
SEL
CONTROL LOGIC
489
419
493
CLK
OUTPUT DATA BUFFER
HARDWARE STATUS
485
487
PORT ADDRESS DECODE
BIOS ROM ADDRESS DECODE
4
449
449
FROM DRIVE-TYPE JUMPERS (DTØ-3)
-CNTA,B
AØ-A9
IORD,IOWR ACN,-NACK
A13-A19
-MEMR
-RADR
-ROMDIS
I/O CHANNEL VIA 365

FIG. 9

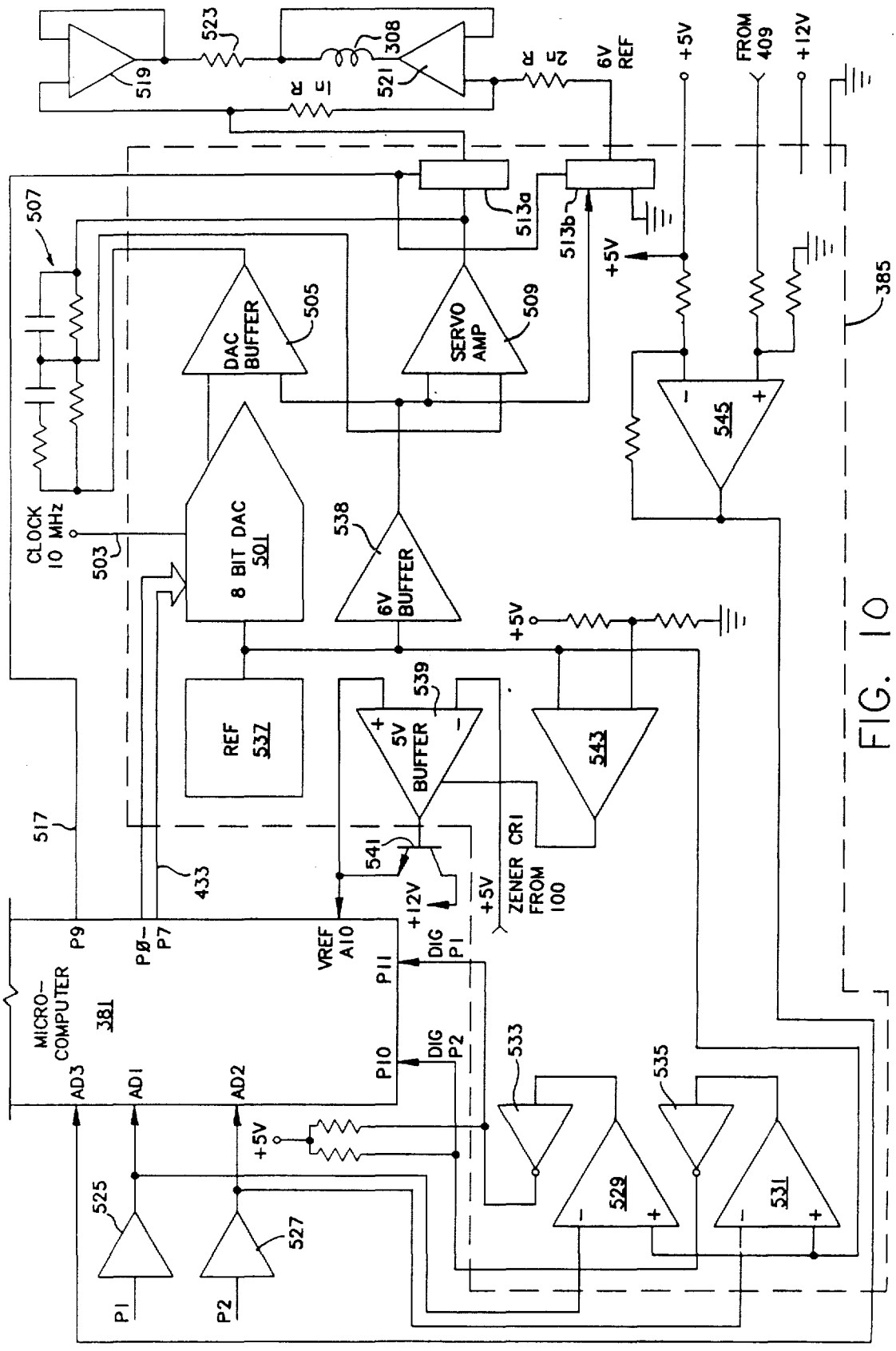

519
523
308
521
6V REF
+5V
FROM 409
+12V
507
513a
513b
385
DAC BUFFER
505
SERVO AMP
509
545
CLOCK 10 MHz
503
8 BIT DAC 501
538
6V BUFFER
REF 537
539
5V BUFFER
543
517
433
541
+12V
ZENER CR1 FROM 100
MICRO-COMPUTER 381
P9
P0-P7
VREF A10
P11
P10
DIG P1
DIG P2
AD3
AD1
AD2
533
535
529
531
525
527
P1
P2

FIG. 10

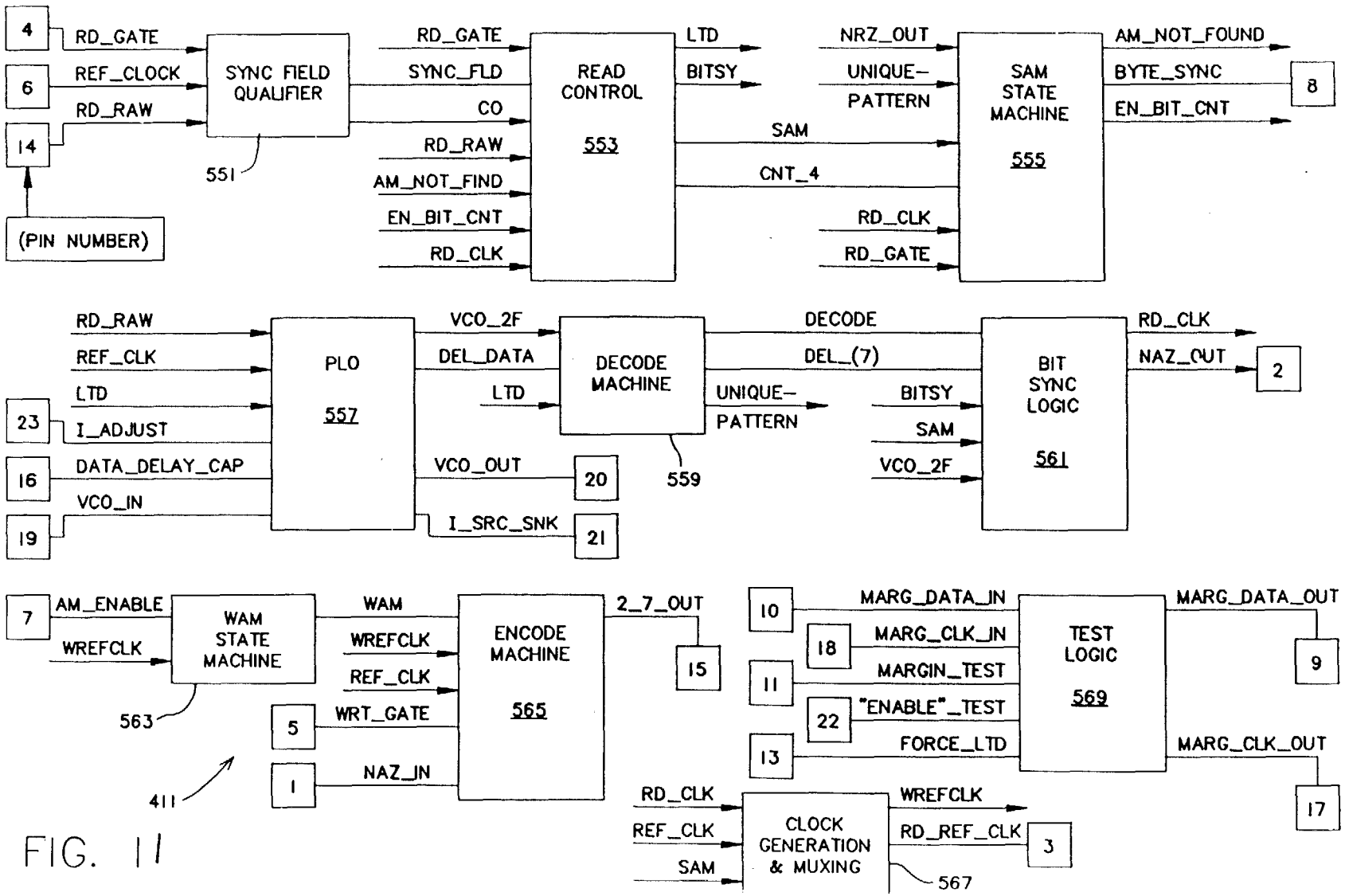

4
RD_GATE
6
REF_CLOCK
RD_RAW
14
(PIN NUMBER)
SYNC FIELD QUALIFIER
551
RD_GATE
SYNC_FLD
CO
RD_RAW
AM_NOT_FIND
EN_BIT_CNT
RD_CLK
READ CONTROL
553
LTD
BITSY
SAM
CNT_4
NRZ_OUT
UNIQUE-PATTERN
RD_CLK
RD_GATE
SAM STATE MACHINE
555
AM_NOT_FOUND
BYTE_SYNC
EN_BIT_CNT
8
RD_RAW
REF_CLK
LTD
23
I_ADJUST
16
DATA_DELAY_CAP
19
VCO_IN
PLO
557
VCO_2F
DEL_DATA
LTD
VCO_OUT
20
I_SRC_SNK
21
DECODE MACHINE
559
DECODE
DEL_(7)
UNIQUE-PATTERN
BITSY
SAM
VCO_2F
BIT SYNC LOGIC
561
RD_CLK
NAZ_OUT
2
7
AM_ENABLE
WREFCLK
WAM STATE MACHINE
563
411
WAM
WREFCLK
REF_CLK
5
WRT_GATE
1
NAZ_IN
ENCODE MACHINE
565
2_7_OUT
15
10
MARG_DATA_IN
18
MARG_CLK_IN
11
MARGIN_TEST
22
"ENABLE"_TEST
13
FORCE_LTD
TEST LOGIC
569
MARG_DATA_OUT
9
MARG_CLK_OUT
17
RD_CLK
REF_CLK
SAM
CLOCK GENERATION & MUXING
567
WREFCLK
RD_REF_CLK
3

FIG. 11

SEQUENCER IN SOFT SECTOR MODE

INDEX MARK 399 — 18 IDENTICAL SECTORS 568 BYTES PER SECTOR — INDEX MARK

RE-WRITTEN DURING WRITE UPDATE

FIELD	POST INDEX GAP	ID PRE-AMBLE	ID SYNC BITE	ID MARKER BYTE	ID DATA FIELD	ID ECC	ID POST-AMBLE	DATA PRE-AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	DATA FIELD	DATA ECC	DATA POST-AMBLE	INTER-SECTOR GAP	PRE-INDEX GAP
SEQ-CNT	149	12	1	1	4	2	3	12	1	1	512	6	3	10	1 *
SEQ-VAL	33	FF	62	FE	AS REQ'D	AS REQ'D	33	FF	62	F8	33	AS REQ'D	33	33	33
SEQ-STATE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MODE	START	RESTART												LOOP	HOLD

POST INDEX GAP BREAKDOWN

PURPOSE:	SERVO WEDGE	INDEX DRIFT
# OF BYTES:	130	19

ID FIELD BREAKDOWN

MEANING:	CYLIN-DER HIGH	CYLIN-DER LOW	HEAD	SECTOR
# OF BYTES:	1	1	1	1

INTER-SECTOR GAP USAGE

PURPOSE:	WRITE UPDATE LOSS	SPEED TOLER-ANCE	AM SEARCH RESTART PAD
# OF BYTES	3	5	2

* 43 BYTES NOMINAL

FIG. 12

MICROPROCESSOR CONTROLLED RIGID DISK FILE SUBSYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to rigid, non-removable disk media based data storage subsystems for use with digital computing equipment. More particularly, the present invention relates to a rigid, non-removable disk media based data storage subsystem in which a single microprocessor supervises and controls track seeking and following operations as well as data controller and host computer bus interface functions.

REFERENCE TO RELATED PATENTS AND APPLICATIONS

The following U.S. Patents and co-pending patent applications are pertinent to the present disclosure:

U.S. Pat. No. 4,396,959 for Data Transducer Position Control System for Rotating Disk Data Storage Equipment;

U.S. Pat. No. 4,419,701 for Data Transducer Actuator Control System for Rotating Disk Data Storage Equipment;

U.S. Pat. No. 4,516,177 for Rotating Rigid Disk Data Storage Device;

U.S. Pat. No. 4,639,798 for Disk Drive Having Two Interactive Electromechanical Control Subsystems;

U.S. Pat. No. 4,647,997 for Aerodynamic Latch for Disk File Actuator;

U.S. Pat. No. 4,703,176 for Optical Encoder Assembly;

U.S. Pat. No. 4,712,146 for Compact Head and Disk Assembly.

Small non-removable, rigid disk data storage subsystems have typically involved at least three separate elements: a head and disk assembly including control electronics; a controller for controlling the transfer of data to and from the host computer buses and the storage surface; and an interface enabling the subsystem to operate effectively at a bus level data transfer environment of a host computing system. Recently, the controller and interface have been merged into a single package, typically a plug-in circuit card for plugging into the backplane or "mother board" of the host computing system. The plug-in controller/interface card has then been connected by cables to the head and disk assembly control electronics.

There are drawbacks to the use of separate control electronics for the head and disk assembly and for the controller/interface. For example, the head and disk assembly control system has not been tightly coupled to the data controller. The use of separate microprocessors has not effectively utilized the processing power available, and has led to duplication of circuitry and process inefficiencies. In voice coil actuated head and disk assemblies, instantaneous perturbations, such as bumps which knock the head off of track have not been signalled immediately to the data controller, thereby leading to the writing of data off of track centerline and corrupting data stored in adjacent tracks.

A heretofore unsolved need has arisen for a small, modular control for a disk file subsystem in which the head and disk assembly is tightly coupled to the controller/interface so that the number of circuit elements is reduced, and so that process and control path efficiency is greatly enhanced, and so that the space and electrical

requirements for the overall subsystem may be made very small and compact.

SUMMARY OF THE INVENTION WITH OBJECTS

A general object of the present invention is to provide a rigid, non-removable disk media based data storage subsystem in which a single microprocessor supervises and controls track seeking and following operations as well as data controller and interface functions so as to overcome the limitations and drawbacks of the prior art.

An object of the present invention is to couple a head and disk assembly tightly to a disk file controller/interface via the use of a single supervisory microprocessor.

Another object of the present invention is to employ a single supervisory microprocessor for a disk file subsystem in a manner which enables known tasks to be carried out far more efficiently than heretofore.

One more object of the present invention is to provide an overall control subsystem for a disk file which is substantially entirely formed and carried on a single very small printed circuit card module.

Yet one more object of the present invention is to provide a more positive bump detection mechanism to ensure the integrity of data during data transfer and storage operations of a disk data file subsystem.

Still another object of the present invention is to provide an improved time interval based position dependent track seeking servo system.

One more object of the present invention is to provide improved and more efficient control signal paths for the single supervisory microprocessor in a disk file subsystem.

In accordance with the present invention, an improved control system for a disk file including a head and disk assembly and a controller/interface includes a control subsystem, a controller/interface and a single programmed microcomputer.

The control subsystem controls the position of a head of the assembly relative to a rotating data storage disk of the assembly to cause the head to move to a commanded track of a multiplicity of available concentric data tracks formed on a storage surface of said disk during track seeking operations and to cause the head to remain in substantial centerline alignment with the commanded track during track following operations.

The controller/interface connects the disk file to a host for receiving commands and data to be stored from the host, controls the storing and retrieving of data from the disk surface via the head, reports disk file status and conditions to the host, and controls the sending of retrieved data to the host via the interface.

The programmed control microprocessor operatively controls operations of the control subsystem (which may be a voice coil actuator controlled by a servo or a stepping motor with or without microstep track centering adjustment based on a wedge servo) and operations of the controller/interface so as to coordinate operations of the controller/interface with the control subsystem.

In one aspect the improved control system comprises at least one servo loop which is closed through the microprocessor.

In another aspect the improved control system comprises a plurality of servo loops: a main servo loop including a polyphase position sensor mechanically linked to the head for providing coarse servo control data and

track boundary determination data, and a fine servo loop including centerline offset information read by a head from the disk data surface when the microprocessor is in its main program loop and receives data from the main servo loop and data from the fine servo loop in order to maintain the head in substantial centerline alignment with the commanded track during track following operations of the head and disk assembly.

In one more aspect control data for the microprocessor is passed from the host through control registers of the data sequencer thereby eliminating a need for a separate control bus between the microprocessor and the host system.

In a further aspect the improved control system includes an aerodynamically released shipping latch for latching the head in a safe region relative to the disk and further includes an electronic return spring including a sensor for sensing loss or removal of power from the disk file and a switch circuit for thereupon connecting voltage induced in a winding of a spindle motor rotating by virtue of kinetic energy stored in the disk ordinarily rotated by the motor, to an electromechanical head mover, so as to move the head to the safe region of the disk surface before the disk ceases to rotate sufficiently to maintain headflight.

In one more aspect of the present invention, the improved control system includes a bump detector for automatically inhibiting any writing to the disk surface in the event of detection of a physical perturbation which tends to move the head out of centerline alignment of a data track.

In still one more aspect of the present invention, an improved servo control system is provided for controlling track seeking operations in a data storage file. The file includes a nonremovable data storage disk rotating at a predetermined angular velocity and an electromagnetic voice coil actuator for moving a data transducer head among selected ones of a multiplicity of concentric data tracks formed on a data storage surface of the disk. The electromagnetic voice coil actuator is under the control of a programmed digital processor during the seeking operation, wherein the processor commands the actuator to move the head from a known departure track location to a known destination track location by commanding a current to pass through the coil of the actuator. The improved track seeking system includes:

a relative track determination mechanism for determining and signalling digitally a particular track of a group of adjacent tracks over which the transducer head is instantly located during a track seeking operation,

a timer for repeatedly signalling elapse of a fixed time interval throughout the track seeking operation, the time interval being selected to be less than the time required for the transducer head to traverse a group of adjacent tracks during the highest transducer head seek velocity portion of the track seeking operation,

a look-up table containing prestored position information of the desired position at which the transducer head should be located for each signalled time elapse during the track seeking operation,

and wherein the programmed digital processor being responsive to each time elapse sent by the timer for thereupon receiving the relative track determination signalled by the relative track determination mechanism, for reading the look-up table to derive desired head transducer position, for comparing actual transducer head position at each signalled time elapse with the prestored position information, for calculating a position correction value in the event of a discrepancy, and for applying the position correction value to the electromagnetic voice coil actuator to urge actual head transducer position into correspondence with desired head transducer position during each elapsed time interval of the seek operation.

In yet a further aspect the relative track determination mechanism of the improved servo control system includes an optical encoder and a comparator for generating digital phase quadrature signals.

These and other objects, advantages and features of the present invention will be more fully understood and appreciated by considering the following detailed description of a preferred embodiment presented in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the Drawings:

FIG. **1** is an exploded isometric and somewhat diagrammatic view of a compact, modular disk file subsystem including a control system in accordance with the principles of the present invention.

FIG. **2** is an electrical block diagram of the disk file subsystem and control system illustrated in FIG. **1**.

FIGS. **3***a* through **3***i* are nine sheets of drawing which together set forth a single electrical circuit schematic of a control circuit for a disk file subsystem of the type illustrated in FIGS. **1** and **2**. FIG. **3** is a layout plan for the nine sheets of FIGS. **3***a* through **3***i* and explains how these sheets should be arranged together in order to provide the overall single electrical schematic.

FIGS. **4**A, **4**B and **4**C comprise respectively an electrical circuit schematic, block diagram and flexible circuit substrate for mounting and connecting a two channel monolithic read/write and head select circuit which is mounted within the head and disk assembly shown in FIG. **1**, and which is plug-connectible with the read and write electronics depicted in detail in FIG. **3**.

FIG. **5** is an electrical circuit schematic and block diagram of an optical encoder subassembly mounted within the head and disk assembly shown in FIG. **1**, and which is plugconnectible with the analog servo electronics depicted in FIG. **3**.

FIG. **6** is an electrical circuit schematic and block diagram of a spindle motor driver module externally mounted on casting of the head and disk assembly and which is plugconnectible with the circuitry shown in FIG. **3**.

FIG. **7** is a block diagram of the structure of a data sequencer included within the circuitry shown in FIG. **3**.

FIG. **8** is a block diagram of the structure of a memory controller included within the circuitry shown in FIG. **3**.

FIG. **9** is a detailed block diagram of the structure of an input/output channel interface included within the circuitry shown in FIG. **3**.

FIG. **10** is a detailed schematic and block diagram of the structure of an analog/digital servo circuit included within the circuitry shown in FIG. **3**.

FIG. **11** is a block diagram of a data separator element included within the circuitry shown in FIG. **3**.

FIG. **12** is a diagram of track formatting followed in the disk file subsystem depicted in FIG. **1**.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Overview of Subsystem 31

A unitized, modular miniature disk file subsystem **31**, incorporating the control system of the present invention, is illustrated in exploded overview in FIG. **1**. The subsystem **31** includes a frame **7** which occupies a single expansion or accessory slot of a popular personal computer, such as the IBM Personal Computer *tm*. The frame includes a vertical alignment and support lip **35** at its distant end, and it includes a support plate **8** at its near end, as viewed in FIG. **1**. The support plate **8** also includes a flange **38** enabling the entire subsystem **31** to be securely fastened to the personal computer in conventional fashion.

A modular, miniature head and disk assembly **39** is attached to the frame via shock absorbing grommets **9**. Anchor bolts **43** secure the assembly **39** and frame **7** together through the grommets **9**. The head and disk assembly includes plastic insulative covers **24**, **26** on both major surfaces of the assembly. These covers prevent other accessories and peripheral circuit boards as may be plugged into the personal computer adjacent to the subsystem **31** from having their components shorted out by coming into contact with the underlying metal surfaces of the head and disk assembly **39**. The compact head and disk assembly **39** is described in detail in the referenced U.S. Pat. No. 4,712,146 entitled: "Compact Head and Disk Assembly", the disclosure of which is hereby incorporated by reference into this specification at this location.

Four flexible circuit substrates extend from the head and disk assembly **39**. These substrates may be conductive traces formed upon thin, flexible mylar film, or they may be thin and flat wire cables. In any event, one leads to a jack **349** for connecting internal head read/write electronics with an external read/write channel, another lead to a jack **152** for connecting in internal optical encoder subassembly with an external analog/digital servo element, another leads to a jack **353** for connecting a spindle motor control module with power supply and associated circuitry, and a final one leads to a jack **355** from a coil of a rotary head positioning actuator within the head and disk assembly **39** to connect to the external drive electronics, being part of the analog/digital servo element.

A small double sided printed circuit card **6** carries all of the electronics required for the control system of the present invention (except for the circuits within the head and disk assembly which have already been mentioned). Four screws **63** anchor the four corners of the circuit card **6** to the frame as suggested by the explosion lines in FIG. **1**.

The circuit card **6** includes a conventional edge connector region **365** having properly aligned connection traces **367** for engaging corresponding contact pins of an accessory or peripheral circuit card connector of the personal computer (host system) in which the storage subsystem **31** is installed and connected solely via the traces **367** formed on the edge connector region **365**.

Four plugs **369**, **371**, **373** and **375** are provided on the circuit card for receiving respectively the jacks **349**, **152**, **353** and **355**, previously described. These plugs enable the circuitry inside the head and disk assembly to be connected to the circuitry carried on the circuit card **6** and to be supplied with power from the host system via the edge connector **365**.

Electronics Overview

The following major circuit elements are contained on the printed circuit card **6** generally in the positions indicated in FIG. **1**. (These circuit elements are interconnected in accordance with the architectural overview of FIG. **2** and in accordance with the detailed connection diagram made up of FIGS. **3***a* through **3***i* as arranged in accordance with FIG. **3** to form a single schematic.)

Microcomputer 381 and Program Memory 383

A single programmed, sequential state monolithic microcomputer **381**, sometimes referred to as a "microprocessor", provides overall control of the subsystem **31**. The microcomputer **381** is preferably a type **7810**, manufactured by NEC Corporation, of Japan, or equivalent. The microcomputer **381** includes a single central processing unit (CPU) and a single arithmetic logic unit (ALU), as well as other internal supporting architecture. It executes only one instruction at a time.

The type 7810 is a single chip, five volt, eight bit microcomputer including an internal analog to digital converter having eight multiplex-selectable analog inputs. The analog to digital converter operates continuously by converting whatever voltage appears at a selected input into a digital value which may be read at any time by the microcomputer **381** under program control.

The microcomputer **381** also includes a **256** by eight bit RAM, multifunctional timer/event counters, general purpose serial and parallel interfaces and input/output ports, and maskable and non-maskable interrupt capability. The microcomputer **381** may also control external memory directly, and requires an external program memory for containing the instructions which it is to execute in carrying out the supervisory functions of the control system of the present invention. Each instruction cycle requires one microsecond, and the basic clocking frequency for the microcomputer **381** is 12 MHz. The software controlled functions of the microcomputer **381** are discussed in greater detail subsequently herein.

The microcomputer **381** utilizes a multiplexed bus structure, so that the same electrical lines may carry both address information and data information, at different times. These times alternate, so that in one machine cycle, a bus may be carrying addressing information, and at the next cycle, the same bus may be carrying data information, and so forth.

The 256 byte random access memory within the microcomputer **381** is used as a stack and provided all of the general purpose registers required for operations of the microcomputer.

An eight kilobyte external read only program memory **383** is connected to the microcomputer **381**, and it contains the instructions which the microcomputer **381** will execute during operations of the disk file subsystem **31**. These instructions are presented as a listing at the end of this specification.

The microcomputer **381** is the heart of the control system and has two overall tasks: it supervises and controls radial head position via an electromagnetic voice coil actuator **300** of the head and disk assembly **39** via servo control loops, and it responds to commands from the host computer system by initiating and monitoring

transfers of blocks of data to and from the host and the disk data storage surfaces via the controller/interface.

It is important to remember that throughout the data read/write operations and data transfer operations the microcomputer **381** is monitored the progress of such operations and it is simultaneously controlling the track following head position servo loop so that it is tightly servoing the head **320** at the centerline of the track at which data is being read or being written.

Track Positioning and Following Servos

The subsystem servo performs two functions: First, it must hold read/write data transducer heads in alignment with the centerline of each data track during track following operations. Second, it must be able to perform track seeking operations which cause the head **320** to be moved rapidly and accurately from a known departure track location to a desired destination track location. All servo operations are controlled and supervised by the microcomputer **381** which controls the current which passes through the coil **308** of the voice coil actuator **300**.

An analog/digital servo circuit **385** is connected to the microcomputer **381**, and the circuit provides circuit elements which are required to carry out servo control loop functions in data track seeking and track following operations of the head and disk assembly. This monolithic circuit **385** is explained in greater detail in conjunction with FIG. **10** hereinafter.

An optical encoder assembly **86** is provided inside the head and disk assembly **39**. This encoder **86** includes a moving scale **112** having a multiplicity of spaced apart radial microlines. An infrared light emitting diode **118** causes light to pass downwardly through the microlined scale and through an underlying stationary masked photodetector array **124**. The array **124** responds to relative light levels indicative of position of the scale **112** and with the aid of the overlying mask converts the light levels into two phase shifted signals P1 and P2 which are in phase quadrature.

These phase signals are converted to voltages by current to voltage converters **525**, **527** of the encoder assembly **86** and are then supplied as analog values to the analog to digital converter within the microcomputer **381**, and also to the analog/digital servo chip **385** which converts the analog P1 and P2 values into digital values and returns them digitized to the microcomputer **381**.

The circuitry of the encoder is set forth and discussed herein in greater detail in conjunction with FIG. **5**. An optical encoder assembly suitable for use with the disk file subsystem **31** of the present invention is described in the referenced U.S. Pat. No. 4,703,176 entitled: "Optical Encoder Assembly", the disclosure of which is hereby incorporated by reference into this this specification at this location.

The analog/servo chip **385** and related circuitry converts digital values received from the microcomputer **381** into driving currents and applies these currents through bidirectional dribing amplifiers **519** and **521** to the winding **308** of the rotary actuator, symbolized in FIG. **2** by the broken line carrying reference numeral **300** and interconnecting a symbolic data transducer head **320**, and the moving scale **112**. The direction and magnitude of current passing through the coil **308** determines the direction and velocity of the head **320** in moving among concentric data tracks formed on the data storage major surface **214a** of a single data storage disk **214**. While a rotary actuator **300** is presently preferred, a linear voice coil actuator would also work satisfactorily with the control system of the present invention.

Storage Disk 214

The disk **214** (and disk **215** in a **20** megabyte version of the subsystem **31**) includes two major data storage surfaces **214a** and **214b** coated with a suitable magnetic data storage material. Each data storage surface **214***a,b* provides storage room for a multiplicity of concentric data storage tracks, there being some **614** logical tracks available per data surface. Some **12** additional spare tracks are provided at the outer periphery of the disk surface **214***a,b* to be used in place of tracks having media defects, so that the first tracks required by the host's operating system for directory purposes will be free of any media defects, and thereby be reliable in all cases.

An inner landing zone region LZ is provided so that the ferrite slider head **320** comes into actual contact with the data surface **214***a,b* and subjects it to possible abrasion only in the landing zone region LZ. Each concentric data track nominally holds approximately **10,416** bytes, and is divided into eighteen data sectors, seventeen of them being for storage of useful data and one of them being held in reserve in the event that a media defect renders any one of the other seventeen unusable. Each data sector contains approximately 568 bytes, including **512** bytes of useful data and the remainder being sector address headers, error correction, speed tolerance gap fillers, etc.

An index marker **399**, generated by motor driver circuitry **260** controlling a spindle motor **202**, marks the location in time for a narrow, approximately **200** microsecond (130 byte wide), single servo sector **401** prerecorded with track centerline information for each data track upon one or more data storage surfaces **214***a,b* of the disk **214**.

The disk **214** rotates at a substantially constant angular velocity, and the time period for each revolution is nominally 16.67 milliseconds. The motor driver circuitry is illustrated in FIG. **6** and includes an integrated circuit motor driver, such as type HA 13426, provided by Hitachi America, Ltd., 707 W. Algonguin Road, Arlington heights, Ill. 60006, or equivalent. This integrated circuit includes a flange which is directly mounted to the base casting for the head and disk assembly **39**. The spindle motor **202** is Y wound and it generates three phase commutation signals by Hall effect transducers U, V and W responsive to a small permanent magnet in the armature of the motor **202**, which are used by the integrated circuit to generate the necessary phases to drive the motor **202**, as is conventionally known and understood.

A fourth Hall effect transducer X generates and puts out a once per revolution index signal on an index line. The microcomputer **381** monitors the index line from the motor control **260** and times the interval between each index marker **399** to be sure that the disk **214** is rotating at proper angular velocity, and it takes the subsystem **31** out of service in the event that disk rotation is determined to be improper.

Two radially offset, time staggered bursts are provided for each concentric data track within the servo sector **401**. The transducer **320** reads the first burst and its amplitude value is sampled and sent to and digitized by the microcomputer **381**. The transducer **320** then

reads the second burst and its amplitude value is sampled and sent to and digitized by the microcomputer **381**. Differences in the digitized amplitude values are used by the microcomputer **381** to calculate centerline offset correction values which are stored and combined with a digitized position value and then used to generate correction currents sent to the coil **308** in order to maintain the head **320** in centerline alignment with each track during track following operations.

The **614** tracks are divided into five contiguous zones, there being four zones of **128** tracks each and one inner zone of **102** tracks each. Track centerline data is acquired and stored for the tracks of each zone, and this data is used for initial correction whenever the actuator has placed the head **320** at a track within the zone. A zone timer is set for each zone, and times out after a predetermined interval, requiring that new centerline information for the zone be obtained before read/write operations will be permitted. These architectural features and operations of the fine servo loop and track zones are explained in further detail in the referenced U.S. Pats. Nos. 4,396,959, 4,419,701 and 4,516,177, the disclosures of which are hereby incorporated by reference into the specification at this location.

Aerodynamic Shipping Latch **98** and Electronic Return Spring **400**

An aerodynamically released spring biased shipping latch **98** is defleted by airflow generated by rotation of the disk **214**. This latch **98** includes a member which engages the rotary actuator **300**, thereby locking the head **320** at a landing zone position whenever disk rotation is insufficient to generate an air bearing effect upon which the head **320** "flies" (in accordance with well-known Winchester technology).

In order to be sure that the actuator **300** returns the head **320** to the landing zone, an electronic return spring, symbolized by the switch **400** in FIG. **2** is provided in the subsystem **31**. When power is lost or intentionally removed from the subsystem **31**, this fact is sensed, and the operation of the spindle motor **202** is reversed: i.e. it becomes a generator, and the electrical energy it generates, due to the kinetic energy stored in the rotating disks **214**, **215**, is switched to the coil **308** of the rotary actuator **300**. So long as there is disk rotation, the electrical energy generated thereby is sufficient to return the head to the inner landing zone LZ of the disk **214** and keep it there so that the spring-biased latch **98** reengages the actuator **300** and thereby retains the head at its inner landing zone. The dynamics of the latch **98** and the electronic spring return **400** are designed so that the head **320** is returned to the landing zone LZ in good time before the latch **98** reengages.

Further details of the aerodynamic shipping latch **98** are set forth in the referenced U.S. Patent No. 4,647,997 for Aerodynamic Latch for Disk File Actuator, the disclosure of which is incorporated into this specification at the present location.

A significant feature provided by the combination of the aerodynamic latch **98** and the electronic return spring **400** is that the bias force applied to the actuator by a conventional mechanical return spring (and which must be continuously overcome during disk file operation) is eliminated completely. This means that the actuator **300** operates with less power consumption, a consideration to be made when drawing all of the power of the subsystem **31** from the accessory socket of the personal computer host system.

Read/Write Channel

The overall read/write channel includes a head select and preamp circuit **366** which is carried on a flexible circuit substrate within the head and disk assembly **39** and which is described further herein in connection with FIGS. **4***a*, **4***b* and **4***c*. The channel also includes read/write electronics **409** schematically illustrated in FIGS. **3***a*, **3***b* and **3***c*, and a data separator **411**, described hereinafter in connection with FIG. **11**. The data separator **411** encodes and decodes the data bits to and from an encoding format, such as **2,7** code, which is used in the actual record and playback process on the disk storage surface **214***a,b*.

Controller/Interface

The controller/interface of the control system for the disk file subsystem **31** includes a programmable data sequencer **413** having its own data sequencer random access memory **415**, a memory controller **417**, an input-/output data buffer random access memory **421** addressed by the memory controller **417** for temporarily storing data sent from and to the data sequencer **413** and the data sent from and to an input/output channel interface **419**.

A BIOS (basic input/output system) read only memory **423** is associated with the input/output channel interface **419**, and it contains basic input output program routines which are accessed and executed directly by the host CPU whenever its operating system wishes to make use of the subsystem **31**. Actually, the BIOS memory **423** is not required for operation of the subsystem **31**, and its inclusion is a matter of convenience for the user, thereby enabling the subsystem **31** to be plugged directly into a personal computer host system without requiring the user to add any software driver routines to the operating system which are needed in order to use the subsystem **31**.

The BIOS memory **423** may also include a collection of error and status condition routines which are used by the operating system of the host system to determine and indicate to the user the status and/or error condition of the disk file subsystem **31** from time to time. An eight bit tri-state bus driver **425** is interposed in a data bus between the BIOS ROM **423** and the input/output channel interface **419** and edge connector **365** so that the BIOS program routines from the ROM **423** may be transferred via the host bus to the host CPU and executed whenever the operating system addresses the BIOS memory **423**.

System Buses

A control bus **431** extends throughout the printed circuit card **6**. This bus, shown symbolically in FIG. **2** as a single line, is actually many different lines. Not all lines extent to all elements. For purposes of convention, unless a bus line is a data bus or an address bus, it is considered to be a control bus line. Thus, the data and address buses shown symbolically in FIG. **2** for ease of understanding and in more detail in FIGS. **3***a* through **3***i* define by omission each of the lines making up the overall control bus.

An eight bit unidirectional data bus **433** enables the microcomputer **381** to send digital actuator control values to the analog servo chip **385**. Digital data passes over the bus **433** from the microcomputer **381** to the analog servo **385** wherein it is converted to analog val-

ues and sent to control the position of the rotary actuator during track seeking and following operations.

An eight bit time-multiplexed data and address bus **435** interconnects the microcomputer **381**, the program memory **383**, the data sequencer **413** and the memory controller **417**.

A six high order bit (A8–A13) address bus **437** interconnects the microcomputer **381** and the program memory **383**. The low order eight address bits (A0–A7) for the program memory **383** are sent by the microcomputer **381** over the data/address bus **435** during address time to the memory controller **417** where they are latched and held in order to be sent over an address bus **439** to address the program memory **383**.

A five bit address bus **441** and an eight bit data bus **443** interconnect the data sequencer **413** and its dedicated small random access memory **415** which stores at most only 32 bytes.

The input/output random access memory buffer **421** is addressed via an eleven bit address bus **445** from the memory controller **417**, while an eight bit data bus **447** connects the data sequencer **413** and the input/output channel interface **419** with the buffer memory **421**. The buffer memory **421** provides temporary input/output data storage and functions as a sector buffer, holding a maximum of two sectors of data which are in the process of being stored or retrieved from the data surface of the disk **214**, in addition to all status and control information which passes between the host and the subsystem **31**.

A thirteen bit address bus **449** extends between the edge connector **365**, the BIOS ROM **423** and the input-/output channel interface **419**; and, an eight bit data bus **451** connects the BIOS ROM **423** with the interface **419** and edge connector **365** via the tri state bus driver **425**.

Data Sequencer 413

The data sequencer **413** is a monolithic large scale integrated circuit containing seven internal functional blocks, as shown in FIG. 7. These blocks include a registers/control logic block **461**. This block **461** contains **32** eight bit internal control registers and associated control logic. The registers may be individually written to initialize the parameters that control data transfer, and individually read by the microcomputer **381** in order to obtain status information about sequencer command execution. This block **461** includes disk address registers for storing cylinder, head and sector identification data, status, etc., for the data block to be handled. The microcomputer **381** issues commands to the sequencer **413** by writing to these registers.

An error correction code/cyclic redundancy check logic block **463** generates and checks error correction code (ECC) or cyclic redundancy check (CRC) bytes appended to the data and identification fields respectively of each sector. This block eanbles use of either a standard CCITT **16** polynomial CRC or a programmable ECC. The particular polynomial may be up to **64** bits long and is determined at initialization time by values written into the registers/control block **461**.

A serial/parallel conversion block **465** enables parallel data from the host to be serialized for the disk. This logic is implemented with high speed shift registers which effect the necessary format translation between parallel and serial data.

A host interface block **467** connects the sequencer to the buffer memory **421** via the data bus **447**. The DMA memory controller **417** provides the addresses in the buffer memory **421** to which the data is to be transferred via the address bus **445**.

A disk interface block **469** provides logic to generate and receive control signals such as read gate, write gate, address mark enable, etc., and it also passes the serial data to and from the disk via the data separator **411** and the read/write circuits **409** and **366**.

A microcomputer interface **471** enables the microcomputer **381** to read and write the internal control registers of the block **461** to control operations of the sequencer **413** and to monitor its status.

An interface **473** to the external random access memory **415**, via the address bus **441** and the data bus **443** provides access to 32 format parameter registers. These format paramter registers specify the size and content of the fields within each data sector on the disk. There are two registers for each field. One specifies the number of bytes in the particular field, and the other specifies the actual value contained in that field.

A monolithic integrated circuit, product code OMTI PFM **5050** Programmable Data Sequencer, available from Scientific Microsystems, Inc., 339 N. Bernardo Ave., Mountain View, Calif. 94043, is the presently preferred implementation of the data sequencer **413**.

The function of the data sequencer **413** is to monitor the serial data stream coming from the data separator **411** in order to locate the precise sector of a track at which data is to be transferred. Once a sector address coming in from the data surface is determined by the sequencer **413** to correspond with the correct sector identification, data read or write operations are then carried out.

In the case of a read operation, the sequencer transfers the data from the correctly identified disk sector (**512** bytes) to the sector buffer **421** where it may then be passed through the interface to the host. In the case of a write operation, the sequencer transfers 512 bytes of data from the host (stored in the sector buffer **421**) through the write path and into the data region of the properly identified sector in the correct track on the selected disk surface **214***a,b*.

The sequencer **413** is preprogrammed to carry out these transfers on a single sector basis. The microcomputer **381** servos on track while waiting until the sequencer has completed its operation before it executes any other commands. Once the transfer of a sector of data is completed, a completion signal is sent by the sequencer to the microcomputer **381**. The microcomputer **381** then checks status registers within the sequencer **413** to be sure that no errors have occurred. In the case of a read, the microcomputer **381** then programs the memory controller **417** to transfer the 512 bytes of data from the buffer **421** through the interface **419** to the host. The microcomputer **381** then continues to servo on track while waiting for that transfer to be completed successfully.

Memory Controller 417

The memory controller **417** is a low power monolithic integrated circuit for managing the flow of data between the data sequencer **413** and the buffer memory **421**, and between the buffer memory **421** and the interface **419** and host computer. It controls the transfer of 512 byte blocks of user data stored on and retrieved from the selected data surface **214***a,b*, and it also controls the transfer of command and status bytes to and from the microcomputer **381**. Fundamentally, the func-

tion of the memory controller **41** is to generate addresses which are sent to the buffer memory **421** via the address bus **445**. It also resolves service request contentions during multiple block data transfers between the host and the subsystem **31**, when data blocks are being moved through the buffer **421**.

Three channels of the memory controller **417** are used by the subsystem **31**, and word count registers and address registers are provided internaly for each of the channels. The microcomputer **381** programs the controller with the address from or to which data is to be transferred, the number of bytes to be transferred, and the direction of the transfer. With these parameters loaded into the controller **417**, it then executes the transfer.

FIG. **8** sets forth a conceptual diagram of the structure of the memory controller **417**. Inside the memory controller **417** a registers and control logic block **475** contains the write and read registers for each channel. The write registers may be individually written in order to initialize the parameters that control data transfer. Read registers are available and may be individually read by the microcomputer **381** in order to obtain status information about data block movement command execution.

An address generator **477** generates and puts out addresses to the buffer memory **421** via the address bus **445**. These addresses locate the data to be transferred to the disk via the data sequencer **413** or to the microcomputer **381** or to the input/output interface **419**. In the event of a block transfer the address generator **477** operates automatically to increment the address value to point to the next location in the buffer **421** until the entire block of data for the selected sector is transferred.

A data sequencer interface **479** connects the registers and control logic block **475** with appropriate control lines of the data sequencer **413** via the system control bus **431**.

A microprocessor interface **481** enables the microcomputer **381** to read status registers and to write the control registers in order to monitor and control block data transfers. The memory controller **417** also is used to demultiplex (latch) program addresses for the program memory **383** from the address/data bus **435**, and these addresses, initiated under the control of the microcomputer **381**, are applied to the program memory via the interface **481** and the address bus **439**.

Finally, an input/output interface **483** enables the memory controller **417** to control the operations of the input/output channel interface **419**.

A monolithic integrated circuit, product code OMTI PFM 5060 Four Channel Memory Controller, available from Scientific Microsystems, Inc., 399 N. Bernardo Avenue, Mountain View, Calif. 94043 is the presently preferred implemenation of the memory controller **417**.

The memory controller **417** is preprogrammed to control the transfer of information, i.e. both data blocks and command and status bytes between the subsystem **31** and the host system. In this regard, the controller **417** handles and coordinates the passing data blocks and control and status bytes back and forth across the interface **419** with the host system. Once a sequence of control bytes has been received from the host, (typically six successive bytes sent to one of four predetermined logical ports to which the subsystem is programmed to respond), these bytes are then transferred to the microcomputer **381**.

There is no data path directly between the microcomputer **381** and the buffer memory **421**. In order for the microcomputer **381** to receive command bytes and to send out status bytes to the host via the buffer memory **421**, it is necessary that such bytes pass through the data sequence **413**. In order to write a byte to the buffer memory **421**, the microcomputer **381** sets up the third channel of the memory controller **417** for writing and points to the address of the buffer **421** to which the byte is to be written. Then, the microcomputer **381** writes the byte to a register address within the data sequencer **413**, and the byte is thereupon automatically transferred to one buffer address by coordinated automatic action of the sequencer **413** and the controller **417**. A similar, but 2-step procedure is followed to move a byte of data from the buffer **421** into the internal random access memory of the microcomputer **381**. A prefetch is used after setting up the controller **417** by the microcomputer **381** to place the first byte into the sequencer **413**. A fetch is then used to move the byte from the sequencer **413** into the processor's internal random access memory. Fetches are then used to transfer all remaining bytes of the sequence.

The memory controller **417** passes data back and forth with the host on a byte by byte handshake basis. Once a block of data, usually a **512** byte sector amount, has been passed successfully, completion of the transfer is signalled to the microcomputer **381**.

The host computer normally handles data block transfers from and to the subsystem **31** on a direct memory access basis wherein after the six command bytes have been passed to the subsystem **31**, the host central processing unit (CPU) relinquishes the data bus and data is directly transferred into the active memory of the host under the control of a host memory controller. Byte-by-byte data transfers are used between the storage subsystem **31** and the host for command and status bytes on a programmed input/output basis, wherein such bytes pass through the accumulator register of the host. Such transfers may be used for data blocks but would take far more time and greatly impair the speed advantages normally associated with rigid disk data storage devices.

Input/Output Channel Interface 419

The input/output channel interface **419** is implemented as a special purpose low power VLSI monolithic circuit. This circuit **419** provides all of the circuitry necessary for interfacing the controller elements **413, 417, 381** and related circuitry of the Winchester disk subsystem **31** to the input/output channel bus of a selected host computer, such as the IBM Personal Computer TM . The circuit **419** provides a buffered data path to the host input/output channel, and it provides address decoding for access to eight host input/output address ports, address decoding for access to the external BIOS memory **423** via the buses **449** and **451**, and circuitry for control of host bus interrupts and DMA transfers.

As seen in FIG. **9**, the circuit **419** includes a port address decode block **485** which decodes address lines **A0-A9** from the host I/O channel in order to enable selection of eight input/output ports: four write ports and four read ports (of which only three are used). Two user accessible address select input pins -CNTA and -CNTB are provided to change the address range of the host's input/output ports to enable the use of multiple

storage subsystems **31** in the same host personal computer.

A BIOS memory address decode block **487** decodes address lines A13 through A19 from the host I/O channel to give a ROM select signal -ROMSEL for enabling reading of the external BIOS memory **423**. An address select input pin -RADR is provided to change the address range of the BIOS memory **423**. An input pin -ROMDIS is also provided to disable decoding of the BIOS address entirely.

A control logic block **489** contains logic circuitry to control the host input/output port register reads and writes, data block transfers to and from the host and interrupts sent to the host. This block includes two internal flip-flops which control whether the host will be interrupted at the completion of a command, and also whether the transfer of data to the host will be by direct memory access through a host memory controller, or not. These bits are set by bits D0 and D1 of a control word written by the host into one of the write ports of the control logic block, and control the logic levels on an interrupt request line IRQ and a data memory request line DRQ extending to the host. A data acknowledge signal -DACK is received into the control logic block **489** from the host to indicate receipt of a data byte and thereby signal the readiness of the host to receive another data byte.

A 3:1 Multiplex/Driver block **491** enables one of three different host input/output read ports to be read on the host input/output channel by the host. These ports include an output data buffer **493** (Port 0) which latches data on the bus **447** from the buffer memory **421** and puts out the data to the host through the block **491** and the data bus **451** on a byte-by-byte handshake basis. The multiplex/driver block **491** also selects a hardware status register (Port 1) located in the control logic **489** which thereupon indicates to the host the state of the various control signals inside of the input/output circuit **419**, and also a drive type register (Port 2), also within the control logic **489**, which enables the host computer to read the value of four inputs which specify the type of disk drive in use. Although a fourth read port (Port 3) is available, it is not used by the subsystem **31**. An input data buffer **495** latches data on the bus **451** from the host and puts out data to the buffer memory **421** on the bus **447** on a byte by byte handshake transfer basis.

Servo Circuit 385

A low power monolithic analog and digital integrated circuit **385** is provided for the analog/digital servo circuit. Its internal architecture is depicted in FIG. **10**. This chip **385** includes the circuitry required to carry out digital to analog conversions to provide control current to the actuator power drivers **519**, **521** for track following and seeking operations. The servo circuit **385** also performs a peak detection function upon the read signal immediately following the index marker **399** when the head **320** reads the servo bursts. The peak detection function enables the microcomputer **381** to determine track centerline information from the radially offset, time staggered servo bursts.

The servo functions are carried out by sending an analog direct current through the rotor coil **308** of the moving actuator asembly **300**. The direction (polarity) of the current passing through the coil determines the direction, whether in or out radially on the disk, of head movement. The electromagnetic motion of the head actuator assembly **300** is controlled by the microcomputer **381** which monitors coarse position information generated by the optical encoder assembly **86** and by the fine position information derived from the single servo sector **401** via the read and write channel.

FIG. **10** diagrams the circuitry of the servo circuit **385** within its environment of the microcomputer **381**, optical encoder **86**, and rotor coil **308**.

Beginning with the eight bit servo data bus **433** from the microcomputer **381**, digital data enters an eight bit digital to analog converter **501**. The digital to analog converter is a switch-capacitor design and uses a 10 MHz clocking signal which is supplied over a line **503**. The analog output from the DAC **501** is buffered in an operational amplifier DAC buffer **505** and then passes through an external phase lead filter **507** which provides servo loop phase compensation in combination with an internal track following servo amplifier **509**. A switching circuit **513** operating in response to a signal from the microcomputer **381** via a servo off control line **517** enables current to be removed entirely from the rotor coil **308** under the control of the microcomputer **381**.

Two external driver amplifiers **519** and **521** are used to drive current through the coil **308**. A voltage (either the phase compensated output of the amplifier **509** during track following or the seek amplifier **511** output) is applied directly to the non-inverting input of the amplifier **519** and is applied to one end of a voltage dividing network comprising resistors having a two to one resistance ratio. A common node of the network is connected to the non-inverting input of the amplifier **521**. The network is also connected at its other lower resistance end to a six volt reference voltage, so the actual voltage between three and nine volts put out to the amplifier **519** is proportioned about the reference voltage when it reaches the input of the amplifier **521**.

For example, when a three volt potential is applied to the amplifier **519**, three volts appears at its output. At the same time a four volt potential appears at the input and output of the amplifier **521**. A one volt difference is then present across a ten ohm sense resistor **523**. A one volt drop across the 10 ohm resistor **423** creates a current flow of **100** milliamps which passes through the rotor coil **308** from left to right in FIG. **10**, and causes it to move the actuator assembly **300**. When the voltage at the input of the amplifier **519** is e.g. nine volts, only eight volts appears across the amplifier **521**, causing a 100 ma current in the opposite direction to flow.

The voltage drop across the resistor **523** is sensed by both amplifiers **519** and **521** at inverting inputs thereof, and is used, in combination with the control voltage applied to the non-inverting inputs, to control the magnitude and direction of current passing through the coil **308**. The driving amplifiers **519**, **521** supply a maximum of approximately **100** milliamperes to the coil **308**, in either direction of current flow.

Two current to voltage converters **525** and **527** in the optical encoder subassembly **86** convert the light-induced phase currents P1 and P2 into analog voltages. Outputs from these converters **525** and **527** enter the microcomputer **381** analog to digital conversion ports and also enter the servo circuit **385**, as shown in both FIGS. **2** and **10**. Two comparators **529**, **531** in the circuit **385** monitor the P1 and P2 voltages and develop digital track crossing signals which are returned to the microcomputer via two inverting amplifiers **533**, **535**, also inside the circuit **385**. By generating the digital track crossing signals, the microcomputer **381** is able to monitor coarse head position during track seeking oper-

ations more efficiently than if it has to convert the P1 and P2 signals to digital values first.

A voltage reference element **537** provides a reference voltage to appropriate nodes of the circuit elements within the chip **385** as shown in FIG. **10**. A six volt buffer **538** provides a reference six volts to each of the DAC buffer **505** and the servo amplifier **509**. The six volt reference enables the DAC to be varied in its output in a range between three and nine volts over **256** equal increments.

A five volt zener reference from the optical encoder assembly **86** passes through a buffer amplifier **539** and an external transistor **541** before being put into the reference voltage input Vref of the analog to digital circuit within the microcomputer **381**. When the zener voltage from the encoder **86** drifts with temperature changes, these small changes are also tracked by the digital to analog converter of the microcomputer **381**.

The analog servo chip **385** works primarily with a twelve volt power supply, while the microcomputer **381** works with a five volt power supply. A comparator circuit **543** monitors the five volt bus within the servo chip **385**. If the five volt reference is lost at the chip **385**, the comparator **543** shuts off the buffer **239**, thereby preventing the microcomputer **381** from becoming damaged because the Vref port is being forced to ground potential. It should be noted in this regard that all of the outputs of the servo circuit **385** leading directly to the microcomputer **381** are open collector or are output protected, so that the micrcomputer **381** is thereby protected against the failure of the chip **385** or any of its elements.

The chip **385** also includes a detector amplifier **545** which is directly connected to the read/write channel in order to receive the sector servo bursts prerecorded in the single servo sector **401**. The peak voltage levels of the read/write channels are translated by the amplifier **545** into levels more suitable for the analog to digital converter input port AD3 of the microcomputer **381**, driven by the output of the amplifier **545**.

Optical Encoder Circuit **86**

As depicted schematically in FIG. **5**, an integrated circuit (U1) contains four operational amplifiers U1A, U1B, U1C, and U1D. The amplifier U1A is a current to voltage converter and functions as the P1 amplifier **525**. It has an inverting input connected to the anode of the upper photocell P1 of the photodetector array **124**. The amplifier U1B is also a current to voltage converter and functions as the P2 Amplifier, having an inverting input connected to the anode of the lower photocell P2 of the photodetector array **124**. A negative feedback circuit comprising a capacitor C4 and a resistor R12 adjusts the frequency response and gain of the P1 converter U1A, and a similar but adjustable network of capacitor C3 and series resistors R9 and R10 adjusts the frequency response and gain of the P2 converter U1B.

A reference voltage Vref is derived from a 12 volt supply bus from the host computer through a network comprising a series resistor R3 and a 5.0 volt zener diode CR1. The zener regulated 5.0 volts is applied to the non-inverting input of an operational amplifier U1C. A resistance network of resistors R2 and R1 provides at a common node a feedback path to an inverting input of the amplifier U1C and a reference voltage Vref which connects to the common cathode substrate of the photodetector array **124** via a connector. The values of the resistors R1 and R2 establish the voltage present at the output of the amplifier U1C. This output voltage is supplied to two adjustable networks: the first network comprising the resistors **R16**, **R17** and **R18** for controlling the operation of the converter U1A, and the second network comprising the resistors **R13**, **R14** and **R15** for controlling the operation of the converter U1B. Resistors **R18** and **R15** are individually adjustable so that the electrical characteristics of the photocells **P1** and **P2** respectively may be individually controlled and equalized in terms of voltage output over the range of light to dark. These two adjustments **R18** and **R15** also enable each photocell **P1** and **P2** of the encoder **86** to be trimmed and to accomodate the particular gap between the scale **112** and and the masked detector array **124** without loss of current amplitude between the maxima of light and dark conditions at each photocell.

An automatic gain control (AGC) cell of the array **124** is connected to an inverting input of an operational amplifier U1D via a connector. The non-inverting input of the amplifier U1D is connected to a driver transistor **Q1** which in turn supplies current from a 5 volt bus of the host equipment to the anode of the LED light source **118**. The cathode of the light source **118** is connected through two current limiting resistors **R4** and **R5** to ground. A series network of resistors **R6** and **R7**, in combination with the current put out by the AGC photocell controls the current put out by the operational amplifier U1D and actually applied to the LED **118** through the driver transistor Q1.R6 is adjustable to control quiescent current through the LED **118**.

Data Separator **411**

The data separator element **411**, preferably formed as a monolithic integrated circuit, such as type OMTI **20527** available from Scientific Microsystems, Inc., 339 N. Bernardo Avenue, Mountain View, Calif. 94043, or equivalent, is depicted in FIG. **11**. The data separator **411** performs three functions.

First, the data separator **411** determines head position relative to the data format. This task is accomplished by writing a special pattern onto the data surfaces **214***a*, **214***b*, commonly referred to as an address mark pattern, which can be identified when a read operation is initiated. The separator circuit **411** generates and writes the address mark pattern while formatting each data track, and it identifies the address mark when a read operation is begun.

Second, the data separator **411** defines bit cell boundaries on the disk data surface. This task is accomplished by a phase locked oscillator (PLO). The PLO constructs a data clock signal which precisely defines bit cell boundaries as they exist in the formatted data track. Essentially a flywheel oscillator with inertia to average out minute fluctuations in disk speed, the PLO constantly updates the phase and frequency of the data clock signal throughout each data read operation.

Third, the data separator encodes and decodes non return to zero (NRZ) data to a format more suitable for being recorded on the media as a series of magnetic flux transitions, due to constraints peculiar to magnetic recording phenomena. One suitable format is 2,7 code, and the data separator **411** handles the code conversion.

The monolithic data separator circuit **411** as shown in FIG. **11** includes a sync field qualifier circuit **551**. This circuit **551** inspects the frequency of incoming pulses from the read electronics **409**. The output of the circuit **551** is a logical one or zero, depending upon the frequency of the incoming pulses. For example, if the

pulses are separated by less than 204 nanoseconds or more than 602 nanoseconds, the output will be low. If the pulses are separated by greater than 300 nanoseconds and less than 492 nanoseconds, the output will be high, indicative that a sync field is validly present in the raw data stream. Only if the sync field is valid will the PLO be permitted to lock onto incoming data.

This circuit 551 is also used to reset a read sequence. A search for the address mark cannot be initiated until the sync field is valid for eight bytes of data. Only then may a read sequence progress if the sync field falls to zero. If it does before the consecutive eight bytes are received, the read sequence is automatically reset. This mechanism protects against write splices. For example, data having a dexadecimal value of 33 encodes to one pulse every 800 nanoseconds, which will force sync field low. A field of hex 33 is written on either side of a five byte field in the format where write splices may occur. This forces the read sequence to be reset upon entering the write splice and coming out of it. This is important, because over time, write splices could form into any pattern of data including hex FF data and an address mark. However, by making the correct sequence greater than five bytes and forcing a reset of the read sequence on either side of the write splice, a false address mark cannot be generated.

A read control circuit 553 povides a mechanism to discover where the data transducer head 320 is located relative to the data format of a track being read, and to lock the PLO to the disk data. The control circuit 553 includes a four bit asynchronous counter, three state holding flip flops and various decoding logic, A Lock to Data (LTD) signal forces the PLO to phase lock to the read raw (RD RAW) pulses coming from the read channel 409. A bit sync (BITSY) signal enables the decoder to block incoming encoded bits for correct decoding. A search for address mark (SAM) signal enables another state machine 555 to determine whether an address mark is present on the disk at the precise moment, or not. The appropriate action is then taken by the SAM circuit 555.

The phase lock oscillator 557 defines the bit cell boundaries as they exist on the formatted disk during a read operation. The PLO 557 comprises a phase comparator, a filter and a voltage controlled oscillator (VCO). The phase comparator compares the phase of the encoded data read from the data surface 214*a,b* with the VCO signal. It then supplies a current via an ISRCSNK pin whose duty cycle is proportional to the phase difference between the two signals. The filter requires external passive components to provide phase compensation to the phase lock loop, to attenuate the high frequency components of the ISRCSNK signal, and to convert the current into voltage. The VCO is a voltage to frequency converter which provides the decode machine with a bit rate clock of the same phase as raw data. The frequency is determined by the filtered ISRCSNK signal.

A decode machine 559 and a bit sync logic block 561, taken together, are the heart of the data separator. They take in encoded data, such as in 2,7 code format, or another suitable format, from the read channel 409, decode such data and put it out as NRZ data in phase lock with the read clock RD_CLK signal. There are two code bits for every one NRZ data bit, and the code bits must be blocked together correctly before they may be decoded. The bit sync logic block 561 determines correct blocking of encoded bits in response to a valid bit sync signal (BITSY) as generated by the read control circuit 553.

A write address mark state machine 563 generates the write address mark signal (WAM) at a specific time related to the address mark enable signal AM_ENABLE. The WAM signal is used to invert two adjacent code bits. This alters a correctly encoded byte of data into a unique pattern which is not generated by the encode logic because of the encoding rules of the particular code employed. This pattern serves as the address mark.

An encoder machine 565 converts NRZ data from the data sequencer 413 into encoded data in accordance with the selected encoding scheme, whether it be 2,7 code or some other satisfactory code. Encoding operations are carried out whenever the write gate line (WRT_GATE) is enabled. When the write address mark signal WAM is asserted, code bits are inverted. Code bits are synchronized to the reference clock signal REF_CLOCK provided from the data sequencer 413.

A clock generation and multiplexing circuit 567 contains the circuitry required to divide the reference clock signal by two in order to generate a write reference clock WREFCLK signal. This signal is required for the encoding operation of the machine 565. The multiplexer in the circuit 567 steers one of two inputs to a read reference clock output RD_REF_CLK which goes to the data sequencer 413. During a read operation, the read clock signal RD_{13} CLK (which is synchronous with the NRZ data put out by the bit sync logic block 561) is passed to the data sequencer 413 to synchronize it with the NRZ data stream.

A test logic block 569 enables special tests to be carried out on the data separator chip 411. Such tests include holding the LTD line high in order to measure loop parameters of the PLO 557. Also, data may be delayed from the disk with respect to the bit cell in order to perform window margin testing. Ant the time lag between two internal signals may be changed in order to optimize the setup time on the phase comparing flip-flop.

Disk Format

A format arrangement for the subsystem 31 is depicted in FIG. 12. Therein, eighteen identical sectors are provided following the index mark 399 and the post-index gap which contains the wedge servo bursts and a tolerance region for index drift. An ID preamble contains 12 bytes of hex FF data. Its purpose is to synchronize the PLO 557 before the data sequencer 413 reads the ID DATA FIELD. The hex FF pattern is used because it provides the highest frequency read pulses of any single byte repeating pattern. Its length allows for two bytes of PLO sync detection before locking the PLO, five bytes of PLO sync time, one byte of phase set time and four bytes for margin.

An ID SYNC BYTE is the single address mark byte for each sector. It is made unique by violating the encoding rules otherwise carried out by the encoding machine 565. The resultant unique pattern is known to, read and checked by the data sequencer 413 in order to validate the particular sector ID.

An ID MARKER BYTE is a byte of hex FE data, chosen only to be different from the DATA MARKER BYTE. The data sequencer 413 uses this byte to determine that a sector ID data field is about to be read.

An ID DATA FIELD includes four bytes holding the sector address in the form of cylinder high, cylinder low, head and sector.

An ID ECC field of two types of CRC information are used by the sequencer **413** to check the validity of the sector address.

A three byte field ID POSTAMBLE of hex **33** data is provided to guarantee a stable read clock from the PLO during the time that the last bits of the ID ECC field are read, decoded by the decoder **559** and passed to the sequencer **413**.

A DATA PREAMBLE field duplicates the ID Preamble field, and its purpose is to synchronize the PLO before reading the data field.

A DATA SYNC BYTE serves the same purpose for the data field as was served by the ID DATA SYNC BYTE for the ID data field.

DATA MARKER BYTE is a byte of hex **F8**, used by the data sequencer **413** to determine that a data field is about to be read.

DATA FIELD. This field is for storing a block of **512** bytes of user data.

DATA ECC is a six byte field for data error correction code.

DATA POSTAMBLE is a three byte field of hex **33** data and guarantees a stable read a clock from the PLO during the time that the last bits of ECC are being read, decoded and passed to the sequencer **413**.

INTERSECTOR GAP is a ten byte field of hex **33** data containing three functionally separate sections. A three byte write-update field allows for the data preamble and data field to move down the track by up to three bytes between a format operation and a write update operation. This shift is accounted for by the data format encode and decode delays, a one byte sequencer delay and a number of single bit resynchronization delays. A five byte speed tolerance gap allows for a plug and minus point four percent (**0.4%**) speed variation of the spindle motor **202** to be accommodated between track format operations and write update operations (a **0.8%** maximum difference). Finally, a two byte pad guarantees at least two bytes of hex **33** data before the ID Preamble of the next sector. This forces the PLO sync field detector to restart the address mark search sequence even if it has falsely detected some PLO sync data from write splices in the speed tolerance field.

PREINDEX GAP is a **43** byte field of hex **33** data at nominal spindle motor speed. Its purpose is to allow for motor speed variations during track formatting. An overspeed of up to 0.4% may be accommodated.

Control Software

The microcomputer **381** operates essentially in an interrupt driven mode. There are several inputs to the microcomputer **381** for setting its internal interrupt request flags. All interrupts are software maskable, except a nonmaskable interrupt line which may be operated by the host operating system (write to Port **1**), in order to reset the subsystem **31** should it become lost (hung up) during command execution. The host reset operation is flagged through the BAR NMI port, pin **25**. All other host commands are initiated by an interrupt which is flagged through bit position **3** of Port C, (BAR INT2, pin **20**), which may be software masked if some task having a higher priority is in a critical phase of execution.

There are three main phases of software execution: Initialization, Main Loop, and Command Execution. The initialization phase, at power on (or upon an NMI host RESET command) resets and/or preloads all of the control registers with initial or default values required for proper operation of the data sequencer **413**, the memory controller **417** and the head and disk assembly servo system. The operating parameter registers within the microcomputer **381** are also cleared and set with initial or default parameters. Once the subsystem **31** is set up, the microcomputer **381** seeks to track zero and enters the main loop.

The main loop is essentially an idle mode for maintaining the status quo. A track following servo value generated by the microcomputer **381** is latched into and converted to an analog voltage by the digital to analog converter **501** and is converted to a current which passes through the rotor coil **308** to keep the heads **320** centered on track. A phase byte selects which phase, whether **P1**, **P2**, BAR **P1**, or BAR **P2**, should be used for servoing on-track. (**P1** and **P2**, being in quadrature, logically define four adjacent track locations and boundaries). In the main loop, the microcomputer **381** creates a tight on-track servo loop about the selected phase signal. The selected phase is digitized and read, and the servo loop is updated, approximately every 90 microseconds. The analog to digital conversion process requires approximately 48 microseconds, and the digital processing and update requires the rest of the 90 microseconds, the time duration for main loop execution. This updating of the track following servo continues repeatedly until an interrupt occurs. It is expected that approximately 95 percent of the useful life of the subsystem **31** will be spent in executing the main loop.

There are three main interrupts which cause the microcomputer **381** to exit the main loop. The first interrupt is an Index Interrupt, which occurs once each revolution of the disk **214**. The prerecorded A and B bursts in the servo wedge **401** are read sequentially and peak amplitude sampled through the analog to digital converter within the microcomputer **381**. The two amplitude values are compared, and any difference value is used in a computation to provide an error correction value which is combined with the digitized selected phase value from the optical encoder to derive the correction value sent to the digital to analog converter **501**. At the completion of the servo routine at Index, the microcomputer **381** returns to the main loop.

Another interrupt is a RESET operation from the host which is generated by the host's operating system in the event that the subsystem **31** fails to respond to other host commands. The Reset operation creates a hardware interrupt in the subsystem **31** and forces it to reinitialize. In this manner, if the microcomputer **381** gets out of sequence in executing commands, error recovery, if possible, will be accomplished.

A third interrupt is a SELECT Interrupt which is generated by the host computer when it sends a Host Command to the subsystem **31**. Each command received by the microcomputer **381** is compared with a table of valid commands. When a matchup occurs, the table provides an address for a command execution routine in the program memory **383** which corresponds to the particular valid command received from the host. If no matchup occurs, the command is rejected as invalid. Ordinarily, when a command is received, the microcomputer **381** is interrupted, and jumps to, and begins executing the command routine for the particular command. At command completion, the microcomputer **381** returns to the main loop.

A Timer Interrupt occurs every **150** microseconds during seek operations which are carried out in response to a select interrupt which requires a seek operation.

There are a number of Host Commands which may be given to the subsystem **31**. The following Host Commands are representative of the types of commands likely to be sent by a host to the subsystem **31** in order to carry out useful data storage and retrieval operations.

TEST DRIVE READY which is a check to see if the subsystem **31** is ready to receive another command, or to see if it is e.g. seeking or otherwise unavailable. The subsystem **31** puts out an error message to the host in the event that it is not ready.

REQUEST SENSE STATUS which is invoked to send four bytes of a sense block which characterizes current status of the subsystem **31**. This command requires the subsystem **31** to be set up to transfer the four bytes; the bytes are placed in the buffer **421**, and then they are sent to the host via the interface **419**. The microcomputer **381** waits until the host signals receipt as a command completion. Any error conditions are sent to the host in response to this command.

READ ERROR LENGTH. This command sends the host a one byte burst length of the last ECC error. It requires a setup for a one byte transfer via the buffer.

INITIALIZE DRIVE CHARACTERISTICS. This command enables the host to initialize the characteristics of the subsystem **31**. The memory controller **417** is set up to transfer eight bytes of data from the host through the buffer **421** and into the internal RAM of the microcomputer **381**. This information includes the maximum number of cylinders (track locations) and heads. Also, the maximum ECC data burst length is stored.

FORMAT TRACK. This command enables the host to format a single track. The track address is checked to be sure it is legal; the sequencer **413** is set up for formatting; the format track command is sent to the sequencer; and a "bump detect" function is monitored throughout the formatting operation. (The Bump Detect Routine is used to detect whether any physical impulse has jarred the subsystem **31**, causing the head to move off of track centerline alignment. This routine calls for monitoring the selected servo phase put out by the optical encoder **86** is closely as possible (75 microsecond loop) during the format operation. If a bump is detected, the one track format operation is automatically repeated.)

FORMAT DRIVE. This command is invoked by the host in order to format all of the host-accessible storage capacity of the subsystem **31**. It includes carrying out the FORMAT TRACK command for all of the data tracks, beginning with the track specified in the command and continuing through track **611**.

READ DATA. This command enables the host to receive the data from one or more specified number of sectors. A legal starting address is checked. Then, the actuator is commanded to move the head transducer from its present track location to the target or destination track. After the seek, the memory controller **417** and the data sequencer **413** are set up for operations at the destination track, and a command byte is sent to the sequencer to start data transfer operations. The microcomputer **381** waits until the sequencer **413** finishes reading the proper sector at the destination tract. Errors are checked for, and the microcomputer **381** waits until the host memory channel is ready to receive the data commanded. The transfer process to the host is then initialized in the memory controller **417** and the transfer to the host is carried out.

If there are additional sectors to be transferred to the host, the next address is generated and loaded into the sequencer, and the sequencer is then restarted. This process goes on until all of the data is transferred to the host. If the operation requrires access to sectors in adjacent tracks, automatic single track stepping (and head switching) is commanded at the appropriate time by the microcomputer **381**. When all sectors have been transferred, the command is completed and the microcomputer signal command completion to the host.

WRITE DATA. This command follows the same progression of steps as are followed for the READ command, with the exception that data is received from the host over the interface **419** and via the buffer memory **421**. The microcomputer **381** moves the selected head to the correct track location. The first block of data is transferred from the host to the sector buffer **421**. The sequencer **413** begins reading sector headers. When the right sector is located, the sequencer transfers data from the buffer **421** through the write channel, so that it is recorded in proper time and position in the data area of the sector. This process is carried out for each sector, until the command is completed. During the writing process, the microcomputer **381** while waiting for a command completion signal constantly performs the bump detect routine, to be sure that writing is inhibited in the event that a bump is detected. If a bump is detected, the sector is rewritten after the head and disk assembly has stablized.

Other Commands. There are a number of utility commands (such as a SEEK which is not a part of a READ or WRITE command) which may be provided to carry out certain tests and operations desired by the host. These commands are a matter of design choice and are routinely understood in the art and are not essential for successful operation of the subsystem **31**. For this reason, they are not described herein.

Command Structure and Addressing

Every command which is sent to the subsystem **31** by the host is six bytes long. The first byte is a command code to identify the type of command, and the succeeding bytes provide the necessary parameters to carry out the command. Then, typically a block of sector data (512 bytes) is sent to or from the subsystem depending whether the command was a write or a read command. Other commands are the Initialize Drive Characteristics command which transfers eight bytes of data from the host to the subsystem **31**, the Request Sense Status command which transfers four status bytes from the subsystem **31** to the host, and the Read Error Length command which transfers one byte from the subsystems to the host.

After the subsystem **31** has completed each command, the microcomputer **381** sends out a one bye command completion signal to the host, of which only two bit positions are used. The first bit indicates drive number (whether drive number zero or one) and the other bit indicates whether or not an error was detected during command completion within the subsystem **31**.

All communication between the subsystem **31** and the host system is carried out across eight ports: four input ports and four output ports of the host system. The ports are paired together, so that for example port **0** which is at a single logical address is one port in its input mode and in its output mode is another port. All data

transfer is via port 0. All hardware status information is transferred from the subsystem 31 to the host system via port 1. The host reads the status port during data exchanges so that it may synchronize its operations with the state of the subsystem 31. For example, it looks at the request bit of port 1 before sending each command byte.

Port 1 has very different meanings in read and write modes. In the read mode port 1 enables the host to read the hardware status lines of the subsystem 31. The lower four status bits of port 1 are used to carry out a handshake control for each byte of data transferred between the host and the interface 419 of subsystem 31. The busy bit (3) is set by the subsystem 31 whenever it is in the process of executing a host command. For example, the busy bit is set by the subsystem 31 when the host selects it for an operation (a write to port 2) and remains set until the command completion byte is sent to the host via port 0 at the completion of execution of a host command, whereupon the busy bit of port 1 is cleared.

A control/data bit (2) indicates the status of the data bytes being transferred via port 0, whether control bytes or data bytes. An input/output bit (1) indicates whether the data at port 0 is output from the host or input to the host from the subsystem 31. (Output, if user data, corresponds to a Write command; Input, if user data, corresponds to a Read Command). A request bit (0) enables a byte by byte transfer handshake control. The setting and clearing of this bit coordinates the transfer of each byte between the host and the interface 419, during non-DMA data transfer operations as when command bytes are being sent.

A write operation to port 1 by the host generates a reset signal which results in a non-maskable interrupt of the microcomputer and a reinitialization of the subsystem 31 under host operating system control.

Port 2 is used by the host to read a drive type byte which may be used to indicate to the host which type of peripheral is attached to the host system. This byte may be polled, for example, by the host to determine storage capacity size, in the event that the storage capacity of the subsystem 31 is increased e.g. to 20 megabytes by the addition of another data storage disk 215.

A write to port 2 generates a controller select pulse which sets a flip-flop within the Input/Output Interface 419 which has an output line -BUSY. This line interrupts the micrcomputer 381 when a command from the host has been received at the interface 419. To start a command sequence, the host writes to port 2, causing the -BUSY line to become true. This event is detected by the microcomputer 381 and it leaves the main routine and begins a command execution routine. At the same time, the host monitors the subsystems hardware status port 1. As soon as the host sees the busy signal being asserted (true), the command/data (C/D) line being asserted (true), the input/output line not being asserted (not true), and the request line being asserted (true), it knows that the subsystem 31 is ready to receive the first command byte. The first byte is then written to port 0 by the host and is temporarily stored in the input data buffer 495 of the I/O interface 419. An ACK signal is then sent to the memory controller 417, telling it that the first command byte is in the buffer 495. The memory controller 417, drops the request signal, generates a Memory Enable signal, and the byte is then transferred to the buffer 421 and stored therein at an address commanded by the memory controller 417. The memory controller then raises the request signal again, thereby signalling the host to send the next command byte. This procedure is followed until all six command bytes are stored in the buffer 421. They then go to the microcomputer 381 for execution, and at the completion of execution a command completion byte is latched into the output data buffer 193 read by the host at port 0.

Port 3, the fourth port, is not used as a read port. It is used as a write port by the host to enable/disable DMA operations and interrupts sent to the host from the subsystem 31. Thus, the host may write to port 3 before every command so that it may specify to the subsystem 31 whether the host expects to be interrupted at the end of the command, and whether the command to be executed will use block transfers by DMA if it is e.g. a read or write command.

EXAMPLE 1

The subsystem 31 is in the main loop, servoing on track. The host operating system will write to port 2 which will create a signal -BUSY which is an interrupt to the microcomputer 381 and which causes it to exit the main loop. The microcomputer 381 enters an interrupt service subroutine which will cause the memory controller 417 to raise the Request bit in order to obtain the first command byte via port 0. When the host writes the command byte to port 0, an acknowledge signal is sent to the memory controller 417 causing it to lower the Request signal and temporarily store the byte in the buffer 421. The Request bit is again raised, and the next byte is received across the interface 419 in the same manner and stored in the buffer 421. The handshake via the Request bit of the status port 1 continues until all six bytes of the host command have been received and stored in the buffer memory. The memory controller 417 is preprogrammed so as to expect to handle a reception of the six command bytes. Completion of reception of the six command bytes is signalled to the microcomputer 381, whereupon it transfers the six bytes from the buffer 381 to its own registers via the data sequencer 413 as already explained and decodes the command by comparison with a list of valid commands in a look up table stored in the program memory 383. Once the command is decoded, the microcomputer 381 jumps to the routine necessary to carry out that command. In the event that the command received does not correspond to any of the valid commands listed in the lookup table, an invalid command error message is returned to the host. At the completion of execution of a command, a command completion acknowledge signal is returned to the host. The occurrence of any error known to the subsystem 31 occurring during command execution is also signalled to the host, and it can then test the status of the subsystem in an attempt to learn what type of error occurred.

EXAMPLE 2

One critical operating situation arises in the situation where the first host command received by the system is a Seek command, and the very next command received is a Test Drive Ready command. During the fastest portion of the seek, the microcomputer 381 has to receive, process and complete the command by returning a status byte to the host, while simultaneously monitoring track to track crossings of the head and actuator structure, all in such a manner that the actuator does not become lost. In order to carry out this worst case operating scenario, the processing task for processing the

incoming command from the host is divided up into several segments. The microcomputer **381** accomplishes the segments in the very little time available between the track boundary sensing and calculations which are required to maintain control over head position during the seek. The microcomputer **381** in effect begins to process the incoming command, and goes as far as it can with the process until it is time to leave it and to sense the track crossing and increment (decrement) the track counter. Then, the mirocomputer **381** returns to the task of processing the incoming command until the next time interval elapses for monitoring track crossing.

The seeking algorithm employed in the subsystem **31** is interrupt driven by a timer. It is a position algorithm, rather than a velocity or acceleration algorithm. Every **150** microseconds during track seeking, the microcomputer **381** is interrupted and carries out a Seek routine. It looks at the digital **P1-P2** phases to see how far the actuator has progressed in that fixed time intreval, i.e. how many tracks have been passed over by the head during that time; and, it updates the tracks traversed register and checks actual location of the transducer against a loop up table containing a power acceleration curve which contains expected position data. Finally, it adjusts the acceleration of the actuator **300** to bring head position into correspondence with expected head position stored in the look up table.

For example, if the head **320** has crossed **20** tracks by the end of the interval, and the look up table says the head should have crossed 25 tracks by that time, the acceleration (current through coil **308**) is increased to catch up. If the actuator **300** is four tracks off of the target track location stored in the look up table, the actuator **300** will receive a maximum torque value (maximum current will be passed through the coil **308**). At the completion of the Seek command, the actuator **300** will be permitted to settle at the target track.

Since the optical encoder **86** is capable of separately identifying each one of four tracks, the timer interval must be selected in relation to the maximum head actuator seek velocity, so that the head will not move more than three tracks during the time interval. If it were to move four tracks, a hopeless ambiguity would arise, making it impossible for the microprocessor **381** to update the track count register and to calculate the current correction value.

Here follows an object code listing of a control program which actually carries out the operations described hereinabove in a subsystem constructed in accordance with the presently preferred subsystem **31** as described. In this listing, in Tektronics format, each horizontal line represents a separate record. The slash mark is the beginning of each record. The first two hexadecimal bytes correspond to the address of the first byte of the record. The third byte corresponds to the hexadecimal count number of data bytes in the record. The fourth byte comprises an eight bit sum of four bit hexadecimal values for the six digits which make up the address and byte count. The last byte of the record in an eight bit check sum of the four bit hexadecimal digits comprising the program data bytes. All bytes between the fourth byte and the last byte of each record are program data bytes.

Having thus described an imbodiment of the invention, it will now be appreciated that the objects of the invention have been fully achieved in realizing a microprocessor controlled rigid disk file subsystem, and it will be understood by those skilled in the art that many changes and widely differing embodiments and applications of the invention will suggest themselves without departing from the spirit and scope of the invention. The disclosures and description herein are purely illustrative and are not intended to be in any sense limiting.

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We claim:

1. An improved control system for a disk file subsystem including a head and disk assembly for storing and retrieving user data, the subsystem having direct plug in connections to address, data, and control buses of a host computer, the control system comprising:

control means for mechanically controlling the position of a head of said assembly relative to a rotating data storage disk of said assembly to cause said head to move to a commanded track of a multiplicity of available concentric data tracks formed on a storage surface of said disk during track seeking operations and to cause said head to remain in substantial centerline alignment with said commanded track during track following operations;

controller/interface means for connecting said subsystem to a host computer including means for receiving commands and data to be stored from said host computer directly via the direct plug in connections to at least one of its said address, data and control buses, including means for controlling the storing and retrieving of data from said surface via said head, including means for reporting subsystem status and conditions to said host computer and including means for controlling the sending of retrieved data to said host computer via said interface and at least one of the said address, data and control buses of the host computer; and

a single programmed control microprocessor for operatively controlling user data disk storage and retrieval operations of said subsystem via said control means and host to disk data transfer operations of said controller/interface means in response to said commands received from said host computer via said controller/interface.

2. The improved control system set forth in claim 1 wherein said control means comprises at least one servo loop for sampling, holding and processing track centerline information sampled from the data storage surface which is closed through said microprocessor in order to cause said head to remain in substantial centerline alignment with said commanded track during track following operations.

3. The improved control system set forth in claim 1 wherein said control means comprises a plurality of servo loops, a main servo loop including polyphase position sensor means mechanically linked to said head for coarse servo control and for track boundary determination, and a fine servo loop including centerline offset information read by said head from said data surface at least once per revolution of said disk and wherein said microprocessor receives data from said main servo loop and data from said fine servo loop in order to maintain said head in substantial centerline alignment with said command track during track following operations of said head and disk assembly.

4. The improved control system set forth in claim 1 wherein said head and disk assembly includes an aerodynamically released shipping latch for latching said head in a safe region relative to said disk and further comprising an electronic return spring including sensing means for sensing loss or removal of power from said system and switching means for thereupon connecting voltage induced in a winding of a spindle motor rotating by virtue of kinetic energy stored in said disk ordinarily rotated by said motor, to an electromechanical head mover, so as to move said head to said safe region before said disk ceases to rotate sufficiently to maintain headflight.

5. The improved control system set forth in claim 2 further comprising bump detector means including said programmed digital microprocessor means and said servo loop for detecting the occurrence of mechanical shocks during writing operations on a data track and thereupon automatically inhibiting any writing to the disk surface in the event of detection of a mechanical shock which tends to move the head off of track centerline alignment.

6. The improved control system set forth in claim 1 wherein said controller/interface means includes a data sequencer for controlling the storing and retrieving of data from said surface via said head and an interface directly connected to the address, data and control buses of the host computer, said data sequencer including a plurality of internal control registers directly readable by said single programmed microprocessor, so that commands from said host computer may be recorded in said internal control registers of said sequencer from at least one of said address, data and control buses of said host computer via the interface, and so that the microprocessor may thereafter obtain the host commands to be executed by reading said internal control registers of said sequencer.

7. The control system set forth in claim 6 wherein said controller/interface means further comprises a buffer memory connected between said data sequencer and said interface for storing blocks of user data for transfer between said disk storage surface and said host computer, and a memory controller controlled by said microprocessor and connected to generate and put out addresses to said buffer memory for writing and reading said blocks of user data into and out of said buffer memory.

8. The improved control system set forth in claim 1 wherein said control system is comprised of electronics components mounted on a single substrate, said circuit substrate including subsystem to host connection means for mating with corresponding connection means of the host computer thereby providing the direct plug in connection to the address, data and control buses of the host computer; and, control system to head and disk assembly connection means for enabling connections to said head and disk assembly.

9. The control system set forth in claim 8 wherein said direct plug in connection between the subsystem and host computing system comprises an edge connector portion of said substrate, the edge connector adapted to mate with a receptable of the host computer leading to the address, data and control buses thereof.

10. The control system set forth in claim 8 wherein said control system to said head and disk assembly connection means comprises at least one plug and a mating jack.

11. The control system set forth in claim 1 wherein the data controller/interface means further includes data separator means connected to convert data words received from said host computer system into a serial bit stream for recording onto the disk surface during data write operations, and to convert serial bits in a stream bits received as a stream from the data surface into data words, in accordance with a predetermined data format arrangement.

12. The control system set forth in claim 11 wherein the data separator means encodes the predetermined

data format arrangement as 2,7 variable length, zero round length limited code format during data write operations and decodes the predetermined data format arrangement during data read operations.

13. An improved control system for a disk file subsystem including a head and disk assembly for storing and retrieving user data, the subsystem being directly connected to address, data, and control buses of a host computer, the control sytem comprising:

control means for electromechanically controlling the position of a head of said assembly relative to a rotating data storage disk of said assembly to cause said head to move to a commanded track of a multiplicity of available concentric data tracks formed on a storage surface of said disk during track seeking operations and to cause said head to remain in substantial centerline alignment with said commanded track during track following operations;

controller/interface means for connecting said subsystem to a host including means for receiving commands and data to be stored from said host computer directly via at least one of its said address, data and control buses, including means for controlling the storing and retrieving of data from said surface via said head, including means for reporting subsystem status and conditions to said host computer and including means for controlling the sending of retrieved data to said host via said interface means and at least one of the said address, data and control buses of the host computer and

a single programmed control microcprocessor for operatively controlling user data disk storage and retrieval operations of said subsystem via said control means and host to disk data transfer operations of said controller/interface means in response to said commands received from said host computer via said controller/interface,

said control means further including at least one servo loop which samples, holes and processes track centerline information from the storage surface and which is closed through said microprocessor to control head position correction to track centerline during track following operations, and

said microprocessor including program memory means for causing said microprocessor to remain in a main program loop in which said one servo loop is closed so that said head is maintained in substantial alignment with centerline of a said concentric data track and so that said microprocessor may exit said main program loop in order to execute a selected one of a plurality of available service routines which may be commanded by said host computer in order to carry out data read and write operations among the multiplicity of concentric data tracks.

14. The improved control system set forth in claim 13 wherein said control means comprises a plurality of servo loops, a main servo loop including polyphase position sensor means mechanically linked to said head for coarse servo control and for track boundary determination, and a fine servo loop including centerline offset information read by said head from said data surface at least once per revolution of said disk and wherein said microprocessor receives data from said main servo loop and data from said fine servo loop in order to maintain said head in substantial centerline alignment with said commanded track during track following operations of said head and disk assembly.

15. The improved control system set forth in claim 13 whrein said head and disk assembly includes an aerodynamically released shipping latch for latching said head in a safe region relative to said disk and further comprising an electronic return spring including sensing means for sensing loss or removal of power from said system and switching means for thereupon connecting voltage induced in a winding of a spindle motor rotating by virtue of kinetic energy stored in said disk ordinarily rotated by said motor, to an electromechanical head mover, so as to move said head to said safe region before said disk ceases to rotate sufficiently to maintain headflight.

16. The improved control system set forth in claim 13 further comprising bump detector means including said programmed digital microprocessor means and said servo loop for detecting the occurrence of mechanical shocks during writing operations on a data track and thereupon automatically inhibiting any writing to the disk surface in the event of detection of a mechanical shock which tends to move the head off of track centerline alignment.

17. The improved control system set forth in claim 13 wherein said control system is comprised of electronics components mounted on a single substrate, said circuit substrate including subsystem to host connection means for mating with corresponding connection means of the host computer thereby enabling direct plug in connection to the address, data and control buses of the host computer; and, control system to head and disk assembly connection emans for enabling connections to said head and disk assembly.

18. The control system set forth in claim 17 wherein said subsystem to host connection means comprises an edge connector portion of said substrate, the edge connector adapted to mate with a receptacle of the host computer leading to the address, data and control buses thereof.

19. The control system set forth in claim 17 wherein said control system to said head and disk assembly connection means comprises at least one plug and a mating jack.

20. The improved control system set forth in claim 13 wherein said controller/interface means includes a data sequencer for controlling the storing and retrieving of data from said surface via said head and an interface directly connected to the address, data and control buses of the host computer, said data sequencer including a plurality of internal control registers directly readable by said single programmed microprocessor, so that commands from said host computer may be recorded in said internal control registers of said sequencer from at least one of said address, data and control buses of said host computer via the interface, and so that the microprocessor may thereafter obtain the host commands to be executed by reading said internal control registers of said sequencer.

21. The control system set forth in claim 20 wherein said controller/interface means further comprises a buffer memory connected between said data sequencer and said interface for storing blocks of user data for transfer between said disk storage surface and said host computer, and a memory controller controlled by said microprocessor and connected to generate and put out addresses to said buffer memory for writing and reading said blocks of user data into and out of said buffer memory.

22. A method for controlling operation of a Winches-

ter fixed disk data storage subsystem including a head and disk assembly for storing and retrieving user data, a data controller/interface connecting directly to address, data, and control buses of a host computer system, a head position control electromechanical mechanism associated with the head and disk assembly and including at least one servo control loop for sampling and holding track centerline information from a data storage surface of a storage disk and for using the sampled and held centerline information for controlling track centerline position of a head of said assembly relative to a selected one of a multiplicity of concentric data tracks defined on the storage surface of the rotating data storage disk of said assembly, and a single programmed control microprocessor connected to control the data controller/interface and the head position controller, the method including the steps of:

receiving, decoding and executing host commands at the microprocessor via the controller/interface and the head position controller by:

causing the head to move to each selected data storage track of a multiplicity of available concentric data storage tracks formed on a surface of the disk during track seeking operations;

controlling the head position control electromechanical mechanism by correcting head position driver information to be in substantial centerline alignment with each commanded track during track following operations by reference to the sampled and held centerline information;

carrying out one of storing and retrieving of the user data from the commanded track via the head, and sending and receiving of the user data to and from the host computing system via the controller/interface, during the track following operations; and,

reporting subsystem status and conditions including command execution completion to the host computing system via the controller/interface.

23. The method set forth in claim **22** wherein the data controller/interface includes data sequencer having a plurality of storage registers directly associated therewith and directly readable by the single microprocessor and wherein the step of obtaining commands from the host computing system includes the steps of:

receiving each command from the host at a subsystem interface,

transferring the command from the subsystem interface to one of the storage registers of the data controller/interface; and,

reading the contents of the one register directly by the microprocessor to obtain the host command stored therein for execution.

24. The method set forth in claim **22** wherein the single programmed control microprocessor includes a look up program table including control routines for decoding and executing each host computing system command received via said data controller/interface and wherein the steps of decoding and executing the command include the step of executing one of the control routines from the look up program table pointed to by the command.

25. The method set forth in claim **22** wherein said controller/interface means further comprises a buffer memory and a buffer memory controller, and further includes the steps of:

supervising with the microprocessor the buffer memory controller to generate and put out user data storage addresses to the buffer memory,

storing and retrieving blocks of user data in accordance with the user data storage addresses so that the blocks may be transferred between the tracks and the host computing system directly, via the data controller/interface and the data bus of the host computing system.

26. The method set forth in claim **25** wherein the data controller/interface data sequencer having a plurality of storage registers associated therewith and directly readable by the single microprocessor and wherein the steps of maintaining commands from the host computing system includes the steps of:

receiving each command from the host at a subsystem interface and recording each command in the buffer memory,

transferring the command from the buffer memory to one of the storage registers of the data data sequencer, and

reading the contents of the one register directly by the microprocessor to obtain the host command for execution.

27. The method as set forth in claim **22** wherein the head position control electromechanical mechanism includes an electromagnetic voice coil actuator and a position sensor for positioning and stabilizing the head relative to track boundaries, the method further including the steps of:

repeatedly sampling at a predetermined sampling rate track position information from the position sensor which is indicative of present head location during a track seeking operation and sending each sample to the microprocessor,

looking up in a head position look up table with the microprocessor prestored position information on the desired position at which the transducer head should be located for each sample during the track seeking operation,

calculating desired head transducer position by comparing actual transducer head position at each signalled time elapse with the prestored position information, calculating a position correction value in the event of a discrepancy, and generating and applying a current related to the position correction value to the voice coil actuator to urge actual head transducer position into correspondence with desired head transducer position during an elapsed time interval between the present and next succeeding sample.

28. The method set forth in claim **27** wherein the position sensor comprises polyphase optical encoder means, and the head position control electromechanical mechanism further includes comparator means, and the position sampling step includes the step of generating polyphase position signals with the polyphase optical encoder means and comparing the analog polyphase position signals put out by the optical encoder means in the comparator means to provide digital track position information to the microprocessor during track seeking operations.

29. The method set forth in claim **27** comprising in the track following mode of operation the further step of monitoring with the microprocessor the position sensor during user data writing operations to detect any occurrence of mechanical shocks; and, upon detection of a shock, automatically inhibiting any writing to the disk surface in the event of a detected mechanical shock tending to move the head off of track centerline alignment.

30. The method set forth in claim **22** wherein the

steps of receiving, decoding and executing host commands at the microprocessor via the controller/interface and reporting subsystem status and conditions including command execution completion to the host computing system via the controller/interface are carried out via host input/output command and data port and status port addresses of the subsystem and wherein the host computing system accesses the subsystem status port in order to synchronize transfer of data between the host computing system and the subsystem command and data port.

31. The method set forth in claim 22 wherein the data controller/interface means further includes data separator means and the method comprises the further steps of:

converting with the data separator means data words received from said host computing system into a serial bit stream for recording onto the disk surface during data write operations, and

converting serial bits in a stream bits received as a stream from the data surface into data words, in accordance with a predetermined data format arrangement.

32. The method set forth in claim 31 wherein the data separator means carries out the further steps of encoding the predetermined data format arrangement as 2,7 variable length, zero run length limited code format during data write operations and decoding the 2,7 variable length, zero run length limited code format into the predetermined data format during data read operations.

33. An improved control system for a disk file subsystem including a head and disk assembly for storing and retrieving user data, the subsystem being operatively connected to logical address, data, and control bus lines of a host computer, the control system comprising:

control means for electromechanically controlling the position of a head of said assembly relative to a rotating data storage disk of said assembly to cause said head to move to a commanded track of a multiplicity of available concentric data tracks formed on a storage surface of said disk during track seeking operations and to cause said head to remain in substantial centerline alignment with said commanded track during track following operations;

controller/interface means including means for receiving commands and data to be stored from said host computer directly via the lines of at least one of its said address, data and control buses, including means for controlling the storing and retrieving of data from said surface via said head, including means for reporting subsystem status and conditions to said host computer and including means for controlling the sending of retrieved data to said host via said interface means and at least one of the said address, data and control buses of the host computer; and

a single programmed control microprocessor for operatively controlling user data disk storage and retrieval operations of said subsystem via said control means and host to disk data transfer operations of said controller/interface means in response to said commands received from said host computer via said controller/interface,

said control means further including at least one servo means for sampling, holding and processing track centerline information from the storage surface to control head position correction to track centerline during track following operations, and

said microprocessor including program memory means including a servo service routine for causing said microprocessor to participate with said control means to operate said servo means during track following operations in order to maintain said head in substantial alignment with centerline of a said concentric data track, the program memory means including a host command decode routine and a plurality of service routines executable by said microprocessor so that the microprocessor decodes a command received from host computer via said controller/interface and thereupon executes at least one of said service routines in response to the decoded command in order to carry out data read and write operations among the multiplicity of concentric data tracks.

34. The improved control system set forth in claim 33 wherein said control system is comprised of electronics components mounted on a single mounting and connection substrate, said substrate including subsystem to host connection means for mating with corresponding connection means of the host computer thereby enabling direct plug in connection to the address, data and control buses of the host computer; and, control system to head and disk assembly connection means for enabling connections to said head and disk assembly.

35. The control system set forth in claim 34 wherein said subsystem to host connection means comprises an edge connector portion of said substrate, the edge connector being adapted to mate with a receptacle of the host computer leading to the address, data and control buses thereof.

36. The control system set forth in claim 34 wherein said control system to said head and disk assembly connection means comprises at least one plug and a mating jack.

37. The control system set forth in claim 33 wherein said controller/interface means further comprises a buffer memory connected between said data sequencer and said interface for storing blocks of user data for transfer between said disk storage surface and said host computer, and a memory controller controlled by said microprocessor and connected to generate and put out addresses to said buffer memory for writing and reading said blocks of user data into and out of said buffer memory.

38. The control system set forth in claim 33 wherein said track centerline servo information is sampled only once per revolution of the disk and wherein servo means further includes a polyphase position sensor mechanically linked to said head to provide coarse track position control values during track following operations which are combined with said track centerline information sampled from the storage surface in order to control head position during track following operations.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,819,153

DATED : April 4, 1989

INVENTOR(S) : Randolph H. Graham

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page, Item [22], "Jun. 5, 1985" should read

-- Jun. 4, 1985 --.

Signed and Sealed this

Twenty-first Day of November, 1989

Attest:

JEFFREY M. SAMUELS

Attesting Officer *Acting Commissioner of Patents and Trademarks*