TRAINING MANUAL

November 1997


PHOENIX

PHOENIX

New Product Training
November 1997

Agenda Section

Training Day Agenda

Time (pst)		Day 1	
7:00-7:30am	4:00-4:30pm	Program Review	Brian Pirzadeh
7:30-8:30	4:30-5:30	Mechanical	Sam Ho
8:30-9:00	5:30-6:00	Heads & Media	Shu-Yu Sun
9:00-10:00	6:00-7:00	Read/Write	Jim Wiseman
10:00-11:00	7:00-8:00	Firmware	Mike Buckert

Time (pst)		Day 2	
7:00-8:00am	4:00-5:00pm	Servo	Jim Wiseman
8:00-9:00	5:00-6:00	Power Electronics, ASICs	Mehran Ataee
9:00-10:00	6:00-7:00	DVT/DMT Results	Debashish Nag
10:00-10:30	7:00-7:30	Test Process	Ted Caulfield


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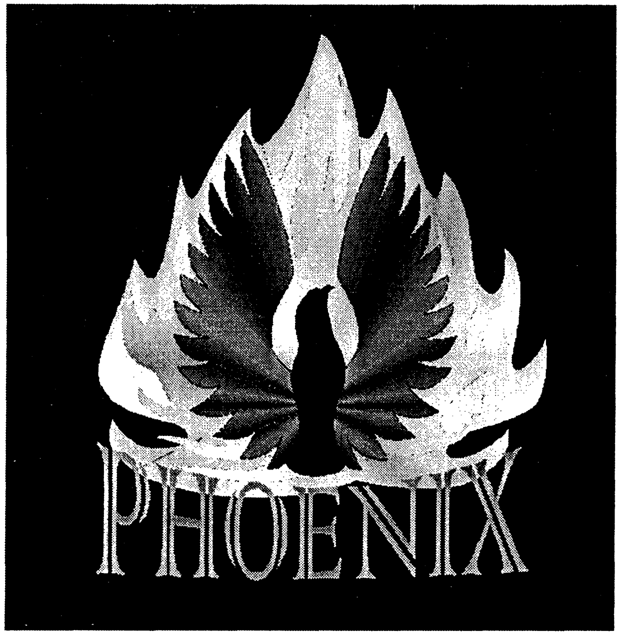
Overview Section



Technical Training

November 10-11, 1997

Engineering Program Overview

PHOENIX

- Specification Highlights
- Design Leverage and Enhancements
- Architecture Overview
- Reliability Enhancements
- Performance Enhancements over Viking
- Build Schedules
- P2 Build Update
- P2 to P3 Hardware Changes
- Key Components
- Head/Media Combinations
- Current Technical Issues
- Schedule Risks

Specification Highlights

- Capacity/Format/Channel
- Servomechanical Timing
- SCSI Interface
- Performance

Specification Highlights

Capacity/Format/Channel

Capacity	4.56GB / 9.1GB
Number of Disks	3 / 5
Number of Heads	5 / 10
Spindle Speed	7200 RPM
Servo Method	Embedded
Servo Samples per Track	90
Recording Code	16/17 PRML
Recording zones	16
Recording Format	ID-less Split Sector
ECC	224 bit RS with XCHK
Tracks per Inch	~ 8500
Flux Changes per Inch (Max)	166.5K
Bits per Inch (Max)	156.7K
Data Rate	98 - 169 Mb/s
Sectors per Track	150-258

Specification Highlights

Servomechanical Timing

	Typical	Maximum
Sequential Head Switch	1.0 msec	1.5 msec
Sequential Cylinder Switch	1.5 msec	2.0 msec
Random Average Seek (Read)	7.5 msec	
Random Average Seek (Write)	8.5 msec	
Average Rotational Latency	4.17 msec	
1/3 Stroke Seek (Read)	< 8 msec	
Full Stroke Seek	17 msec	
Power on to Drive Ready	15 sec	20 sec

Specification Highlights

SCSI Interface

- SCSI-2, SCSI-3, and SCSI-3 LVD supported
- Ultra-II transfer rates supported
- Highly automated SCSI protocol (including Auto Read/Write)
- Tagged command queuing with reordering (ORCA)
- S.M.A.R.T.
- SCAM level 2 supported
- Serpentine Head Switch
- Hot Pluggable
- Active negation drivers
- SCSI interface connector options (3 PCBs):
  - 50 pin Narrow
  - 68 pin Wide
  - 80 pin SCA
- Active SCSI-3 termination (except SCA)

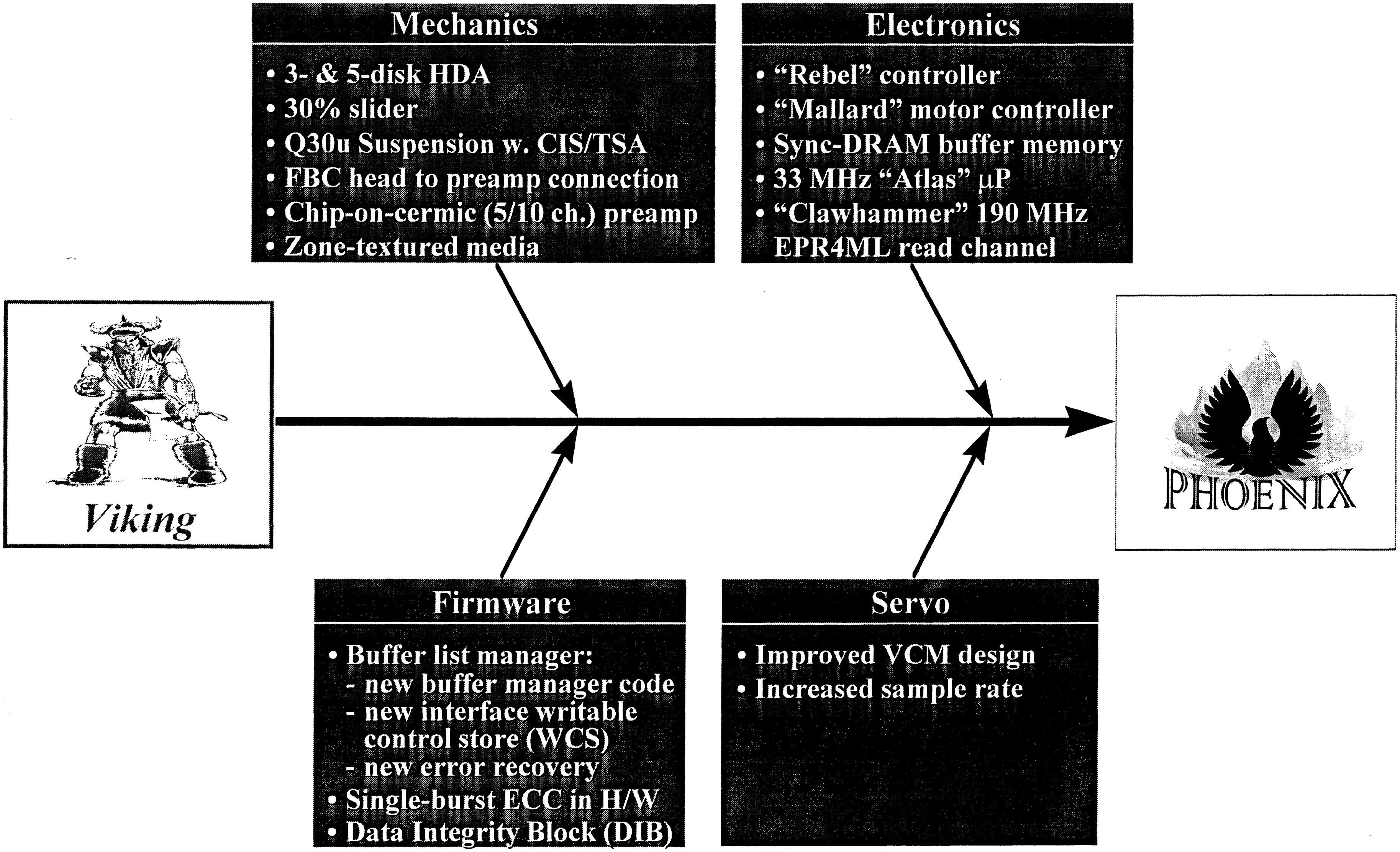
Specification Highlights

PHOENIX

Performance

• External Transfer Rate:	
– Burst	40 MB/s Narrow 80 MB/s Wide
– Sustained	>13 MB/s max (OD) >7.5 MB/s min (ID)
• Acoustics (Ideal)	<4.3 bels (4.5 GB) <4.5 bels (9.1 GB)
• Power Dissipation	<8.5 watts (4.5 GB) <9.5 watts (9.1 GB)

Design Leverage and Enhancements



Mechanics

- 3- & 5-disk HDA
- 30% slider
- Q30u Suspension w. CIS/TSA
- FBC head to preamp connection
- Chip-on-cermic (5/10 ch.) preamp
- Zone-textured media

Electronics

- "Rebel" controller
- "Mallard" motor controller
- Sync-DRAM buffer memory
- 33 MHz "Atlas" µP
- "Clawhammer" 190 MHz EPR4ML read channel

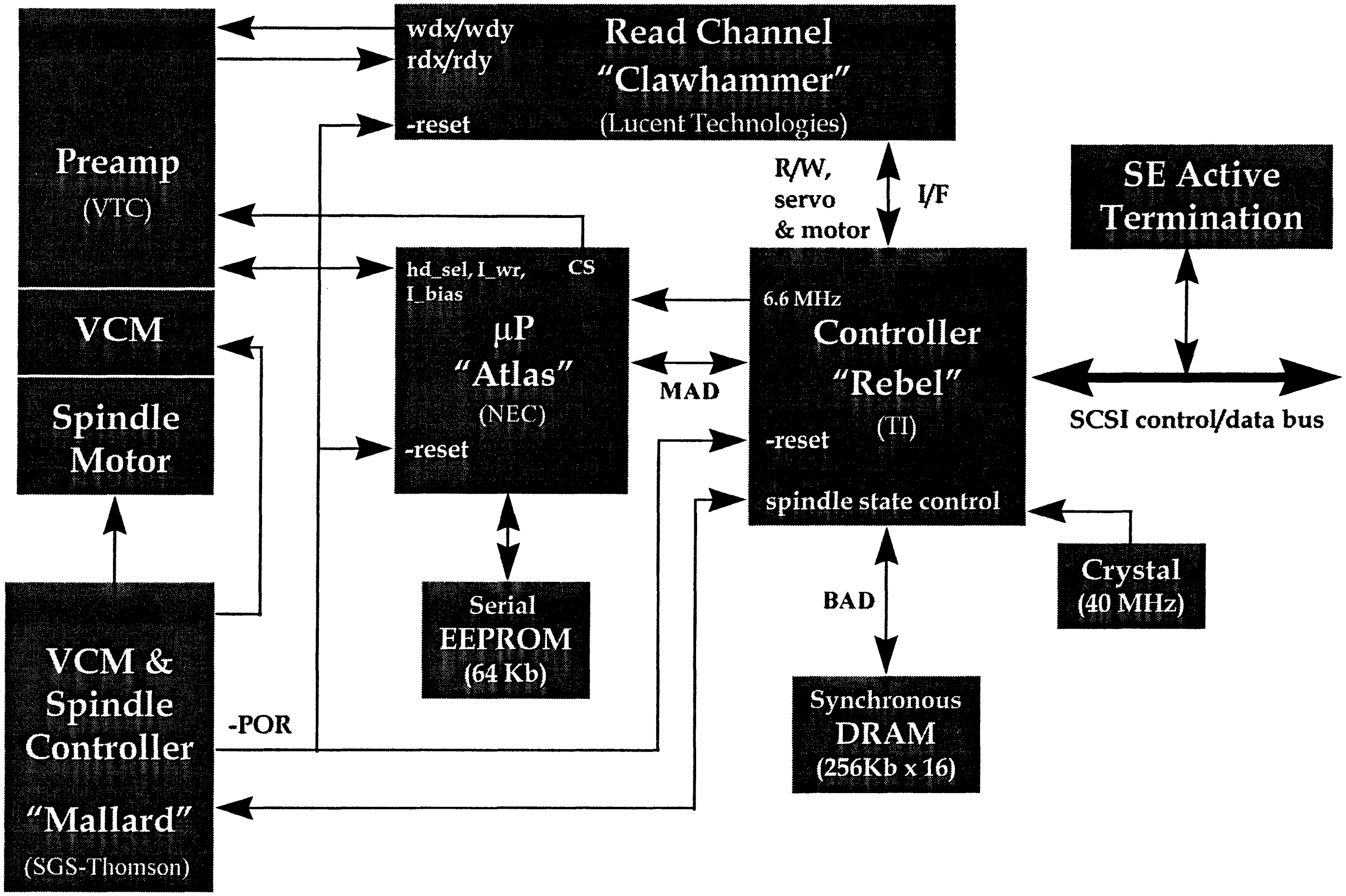
Firmware

- Buffer list manager:
  - new buffer manager code
  - new interface writable control store (WCS)
  - new error recovery
- Single-burst ECC in H/W
- Data Integrity Block (DIB)

Servo

- Improved VCM design
- Increased sample rate

Architecture Overview



Preamp
(VTC)

VCM

Spindle
Motor

VCM &
Spindle
Controller

"Mallard"
(SGS-Thomson)

-POR

wdx/wdy
rdx/rdy
-reset

Read Channel
"Clawhammer"
(Lucent Technologies)

R/W,
servo
& motor

I/F

hd_sel, I_wr,
I_bias

CS

µP
"Atlas"
(NEC)
-reset

MAD

Serial
EEPROM
(64 Kb)

6.6 MHz

Controller
"Rebel"
-reset
(TI)

spindle state control

BAD

Synchronous
DRAM
(256Kb x 16)

SE Active
Termination

SCSI control/data bus

Crystal
(40 MHz)

Reliability Enhancements

- FBC head wiring system
  - ⇨ Consistent automated head connection system
  - ⇨ No dragging service loop
- E-coat base plate
  - ⇨ To avoid any potential contamination from porous surface of casting.
- Shock Feet
  - ⇨ To minimize handling damage
- Shock Clip
  - ⇨ Improves operational and non-op shock performance after mounting.
- Breather Filter
  - ⇨ Provides a controlled clean path for airflow
- Longer Flash memory availability, later Mask ROM transition.
  - ⇨ To allow for a longer period for complete code upgradeability

Performance Enhancements Over Viking

- **Ultra-2 Interface.**
  - External Burst Transfer Rate: 40 MB/s Narrow and 80 MB/s Wide
- **BLM ASIC Architecture**
  - Fully hardware assisted "Zero Latency" implementation
  - Lower command overhead, less firmware intervention
  - Fewer SCSI bus disconnects
  - Similar buffer management architecture as the Atlas drive family
- **Sync DRAM Buffer Memory**
  - 2 x access time improvement (page mode) versus EDO memory access
- **Faster Microprocessor Speed**
  - 33 MHz CPU clock speed versus 25 MHz

Performance Enhancements Over Viking

- **Firmware Enhancements**
  - Auto-write implementation
  - Zero-Latency implementation
  - Lower command overhead with use of BLM
  - Improved SCSI bus utilization . Additional hardware assisted SCSI command handling

- **Increased Channel Rate**
  - 170 mbps at OD
  - External sustained transfer rate: >13.0 MB/s at OD
  - External sustained transfer rate: >7.5 MB/s at ID

Build Schedule

Build	Date	Quantity
E2	7/16/96	300
E2.5	12/3/96	100
P1	2/12/97	1200
P1.5	6/16/97	2160
P2	9/22/97	3500
Check Build	11/13/97	300-800
P3	12/1/97	3750
MP	12/16/97	Ramp

Phoenix P2 Build Update

- Over 3700 drives were built
- Servowriter yield greater than 95%
- Selfscan yield of approximately 70% using MP limits
- Disk load including disk clamp process was identical process as MP
- Head load process was automated but will use a different robot for MP
- Biggest issue was retuning servo parameters for the P2 system mode
- With proper servo notch filters seek performance exceeded spec.
- No component problem was identified.

P2 to P3 Hardware Changes

- Minor PCB layout changes to improve EMI margin
- Magnetic retrack as secondary/backup actuator locking mechanism

Source of Major HDA Components

	VENDOR-1	VENDOR-2	VENDOR-3
HEAD	TDK	Alps	Yamaha
MEDIA	MCC	AKCL	
MOTOR	OZU	TDK	
SUSPENSION	NHK (CIS)	HTI (TSA)	
FBC	Sumitomo	Nitto	
PREAMP	VTC		

Head / Media Combinations

	TDK	ALPS	Yamaha
MCC-M	✓	✓	?
AKCL	✓		

Current Technical Issues

- **Initiator ID selection is limited to <=7**
  - **Rebel-S5 fixes this problem, S5 will be phased in.**

- **SCSI bus parity**
  - **Configuration: Wide PCB, SE mode, and using on board termination**
  - **Options under evaluation:**
    - ➡ **Fix Rebel**
    - ➡ **Have two wide boards:**
      - –1) SE only with on board termination
      - –2) SE and LVD with no termination
    - ➡ **Use universal termination on board**

Schedule Risks

- Successful and on time DMT completion.

- Successful P2.5 "Check Build", new automation readiness

Phoenix Engineering Team

- Brian Pirzadeh
  Program Mgr
  - Julie Dianda
    Dept. Admin.
  - Mechanical Engrg
    Peter Hahn, Mgr
    - Rodica Florea - ME
    - Samuel Ho - ME
    - John Konings - ME
    - Arthur Lin - ME
    - Rod Ngai - ME
    - Shin John Choi - ME
    - Sue Hernandez - MT
    - Kelly Nobriga - MT
    - Adrienne Parcher (Consl)
  - Drive Engrg
    Mehran Ataee, Mgr
    - TBH - EE
    - Tim Howard - EE
    - Rudy Spajic - EE
    - Dayanand Prasad - EE
    - Walt Dobrzynski - TA
    - Kathleen Magazu - Cad
    - Devon Dyer - ET
    - Hal Stephens (Consl)
  - Analog Engrg
    Jim Wiseman, Mgr
    - ***Read/Write***
    - Max Roth - R/W GL
    - Steve Siegel - R/W
    - Emilio Lam - R/W
    - An Trinh - ET
    - ***Servo***
    - Fred Hansen - Servo GL
    - Ben Ryu - Servo
    - Ken Cheung - Servo
    - Anh Tran - Servo
    - ***Head/Media***
    - Shu-Yu Sun (OL)
  - Firmware Engrg
    Mike Buckert, Mgr
    - Alan Chen - FW
    - Linda Lin - FW
    - Hoa Luong - FW
    - Minh Luong - FW
    - Rick Matzkie - FW
    - Dale McNamara - FW
    - Kerry Mellor - FW
    - Steve Paul - FW
    - Mike Rogers - FW
    - Peter Whitney - FW
    - Xuan Phan - FT
  - Product Engrg
    Mike Perry, Mgr
    - Co Ha - Servo
    - Dat Le - R/W
    - James Luo - Mech
    - Ray Baltrenas - EE
    - Ed Shaules - EE
    - Lee Mauldin - FW
    - Hak Kim - FW
    - Diana Dominguez - MT
    - Hoang Nguyen - ET
  - NPI Engrg
    Ted Caulfield, Mgr
    - Cyrus Yamin
    - Dao Nguyen
    - Larry Sisneros
    - Ramon Del Rosario
    - Ken Tang
    - Kent Yang

Phoenix Product Team

Mike Wais	Sponsor
Larry Willson	Team Leader
Brian Pirzadeh	Development Engineering
Skip Shapiro	Marketing
Yvonne Mendoza	Materials
Shireesh Agharkar	Operations
Mike Perry	Product Engineering
Billy Pettit	Quality

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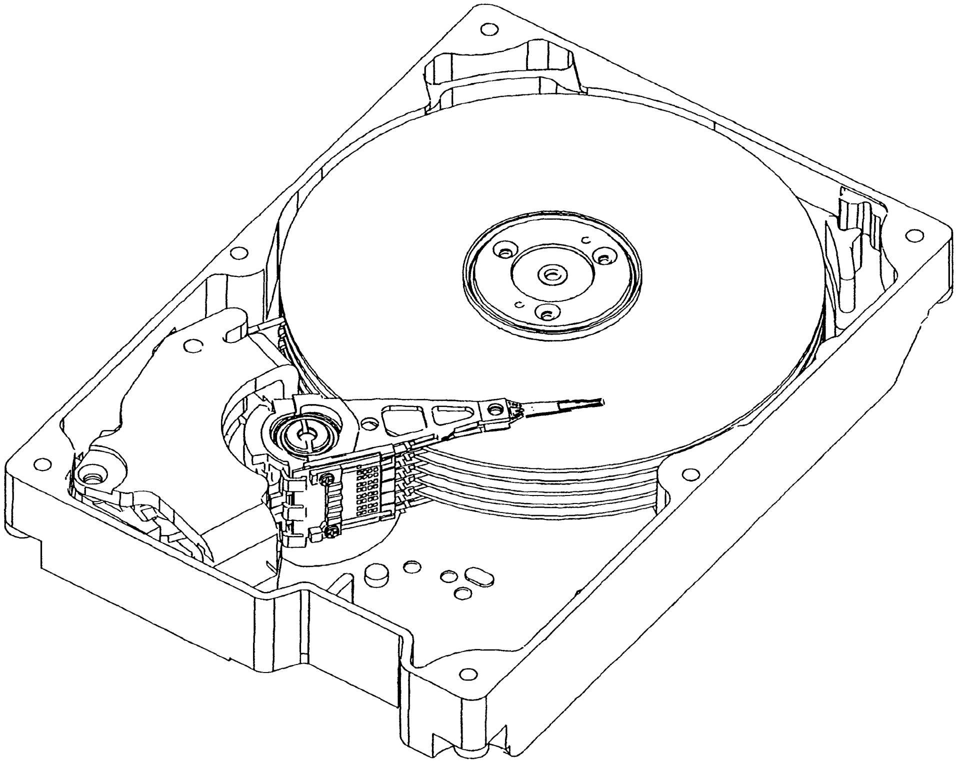
Mechanical Section

Drive Mechanics Consideration



Priority Considerations

- **Maximum design leverage off of Viking**
- **Five disks 9G in one inch form factor**
- **Reliable airlock**
- **Improve fragility performance**
- **Integrate FBC* and Q30 suspension into design for improved product reliability**
- **Achieve low acoustic noise**

- ***FBC - flexible bump circuit**

Similarity to Viking

- plan view
- pivot location
- coil encapsulation
- same style cover - stamped stainless steel laminated
- identical dynamic balancing scheme using same balancing clips (spec 50 mg-cm)
- same style servo-writer

Deviations from Viking

Deviations from Viking

Item	Reason
2 mm disk spacing	five disks - achieve required capacity
Airlock	improve reliability
30% slider /Q30u/ FBC	• reliable head wire connection • eliminate service loop drag possibility • improve manufacturability
Cartridge bearing	• thermal stability • reduce assembly process dependency
E-coated base	reduce contamination
6 screw disk clamp	improve disk slip shock limit with five disks

Acoustic

	9G (5d)	4.5G (3d)
Idle	3.7 bels	3.5 bels
Seek, 40%	4.5 bels	4.4 bels

- Data from P2
- Acoustic spec to be updated to reflect P2 improvement

Track MisRegistration (TMR)

	4.5 G	9G Ozu	9G TDK
w/r NRRO (goal:6.1%)	3.5% - 5.3% typical	4.2% - 5.6% typical	4.5% - 6.5% typical
CRTV (goal: 7.5%)	5.5% - 6.5% typical	5.9% - 7.5% typical	5.9% - 8.0% typical

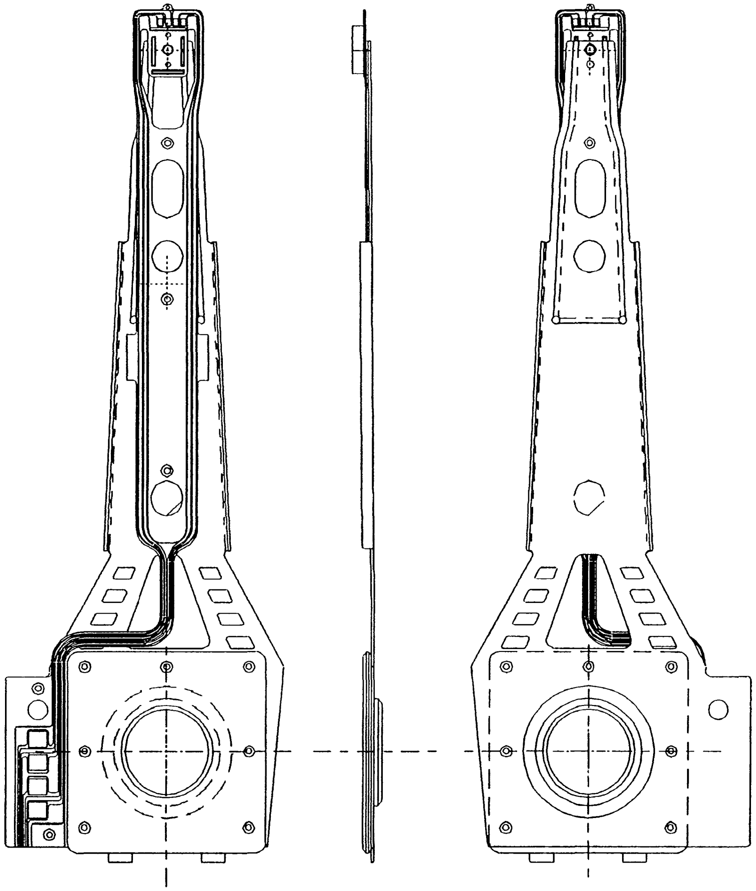
- Data from P1.5
- NRRO improvements implemented and proven during P2

Current Phoenix Features

- **30% MR, Q30 up rail suspension with 8mil thick Low Profile swage plate**
- **CIS/TSA with FBC interconnect (no tubing or wires)**
- **counterweight (extra swage plate) staked to outer arms to balance outer arms and help control resonance's**
- **actuator plan view similar to Viking with exception of airlock stop arm feature**
- **aluminum eblock, 1.00mm thick main arms, 0.66mm thick swage pads**
- **standard PPS encapsulation for coil**
- **cartridge bearing instead of discrete bearings**
- **new servowriter pushpin layout**

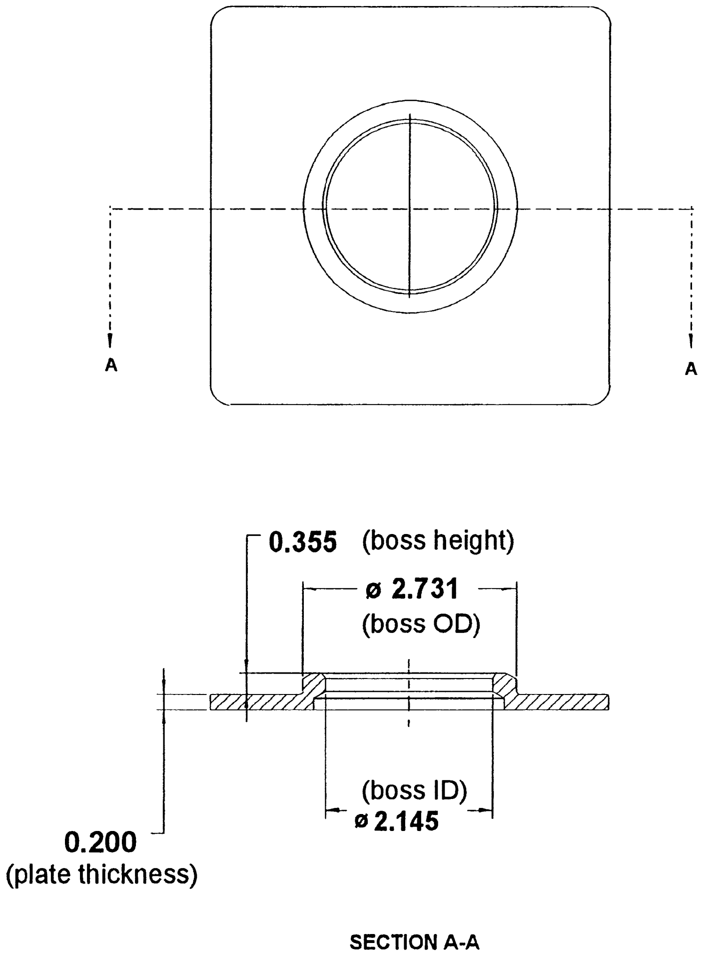
Heads/Suspension

- **30% MR sliders on Q30 up rail suspension**
- **FBC (flex bump circuit) to CIS (circuit integrated suspension, NHK) or TSA (trace suspension assembly, HTI)**
- **2.50 gm load**
- **HTI Low Profile 8mil swage plates**
- **allows for use of FBC**



Swage Plates

- non-Interlok
- Hutchinson “Low Profile”
- 0.20mm thick (8 mil) with boss height of 0.28mm above load beam
- expect ample swage retention torque



Gram Load/Retention Torque

P1 5 disk gram load (40 HSA's		
	average	stdev
up heads	2.48	0.25
down heads	2.26	0.24
all heads	2.37	0.27

P1 5 disk retention torque (20 heads)		
average	6.28	
stdev	0.41	

Disk Spacing

- 2.00mm -5 disks in 1" form factor
- generous margins for arm/disk clearance and headloading clearance (previously designed around 1.70mm spacing)

Phoenix Head/Disk touch Monte Carlo simulation results
(5 disk HDA, statistics of 10,000 sample runs)

clearance between disk and swage for 8 mil plate	0.3939

	3 sigma all	4 sigma all
minimum	0.0214	0.0138
maximum	0.2053	0.1618
mean shift	0.0741	0.0561
standard deviation	0.0292	0.0223
variance	0.0009	0.0005
skewness	0.8800	0.8761
kurtosis	3.7750	3.7303
# of interferences	0	0
sigma margin	**10.97**	**15.13**

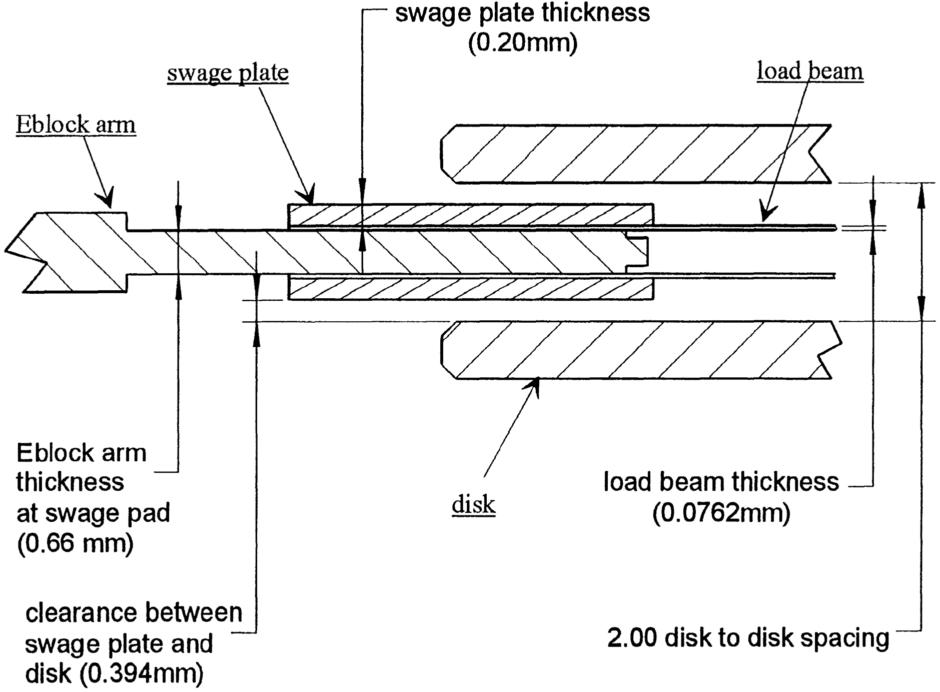
Phoenix Head Loading Monte Carlo simulation results
(5 disk HDA)
statistics of min clearance from all 10 heads of each HDA
Q30D suspension + 30% slider

nominal clearance between slider and disk =	0.5

	3 sigma all	4 sigma all
minimum	0.01157	0.01190
maximum	0.12874	0.12078
mean shift	0.05726	0.04301
standard deviation	0.01799	0.01385
variance	0.00032	0.00019
skewness	0.63548	0.72176
kurtosis	3.40408	3.59844
# of interferences (out of 10,000)	0	0
sigma margin	**24.61**	**33.00**

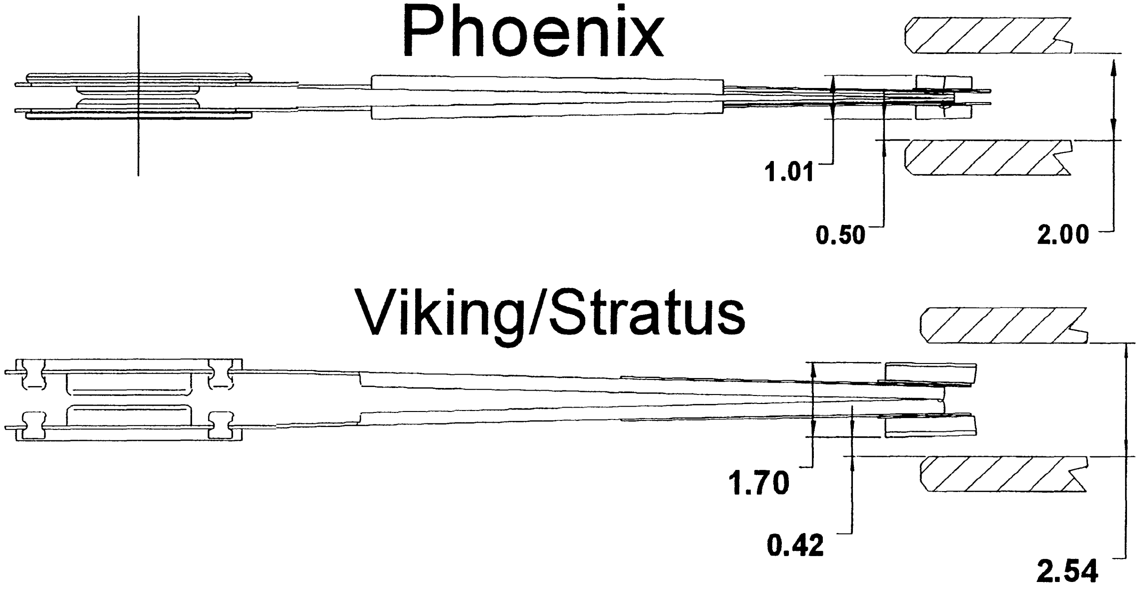
Swage Plate to Disk Clearance

- **clearance from swage plate to disk surface 0.39mm (compared to 0.31 for Viking/Stratus), provided by 8mil swage plates**
- **cartridge bearing provides better vertical tolerances**



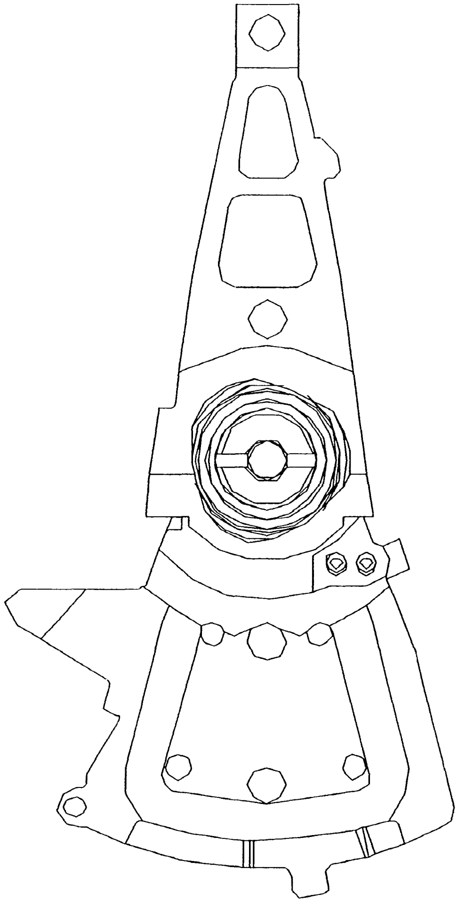
Headloading Clearance

- **clearance from disk to slider 0.50 mm (more than Viking/Stratus) -Monte Carlo tolerance analysis shows generous margin**
- **challenge in thin loading combs for 30%**

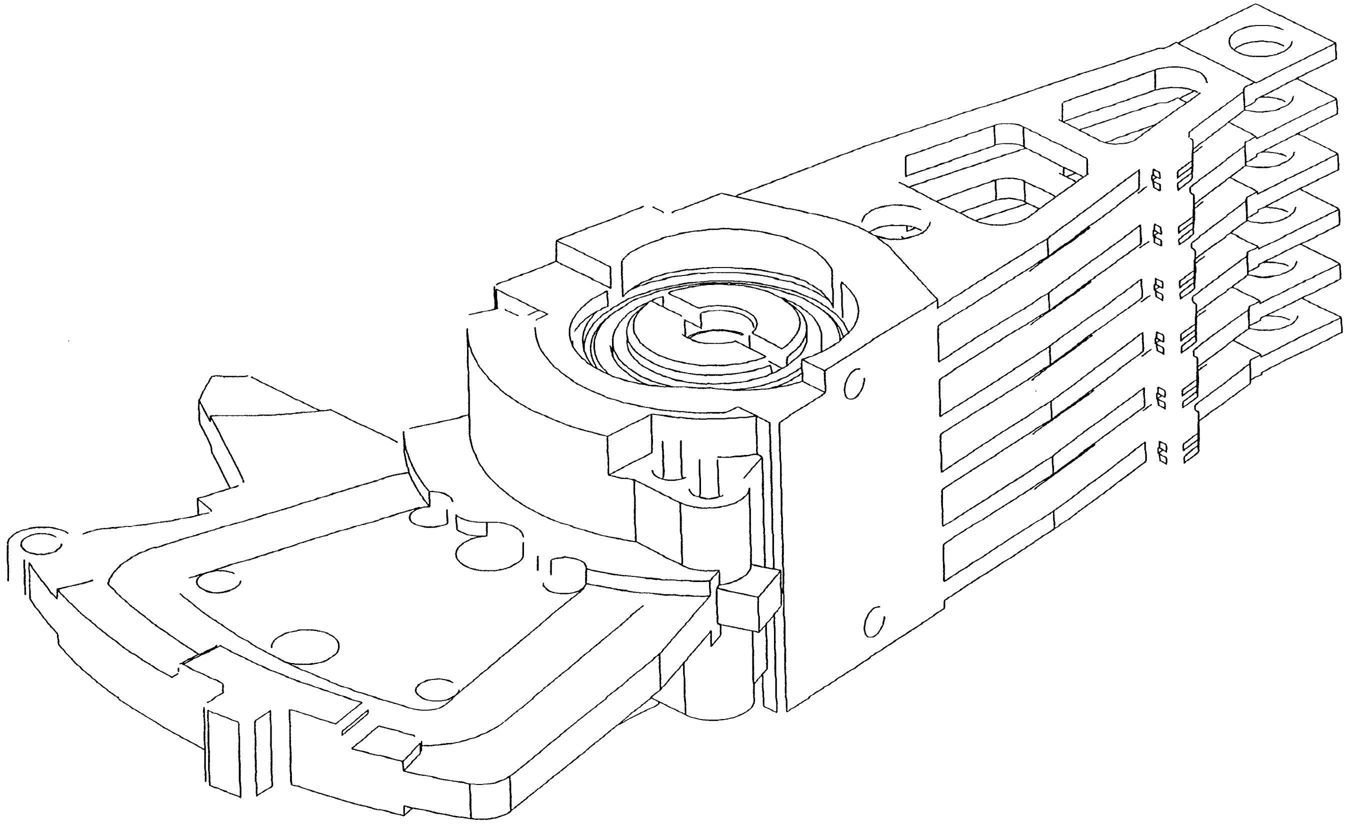


Eblock/Actuator

- extruded machined aluminum
- similar plan view to Viking
- single FBC support slit (second FBC slit on moving support)
- encapsulation, crash stop tang, coil pins
- no servowriter pushpin tang - pushpin uses same tang as crash stop
- new airlock stop arm and cutout

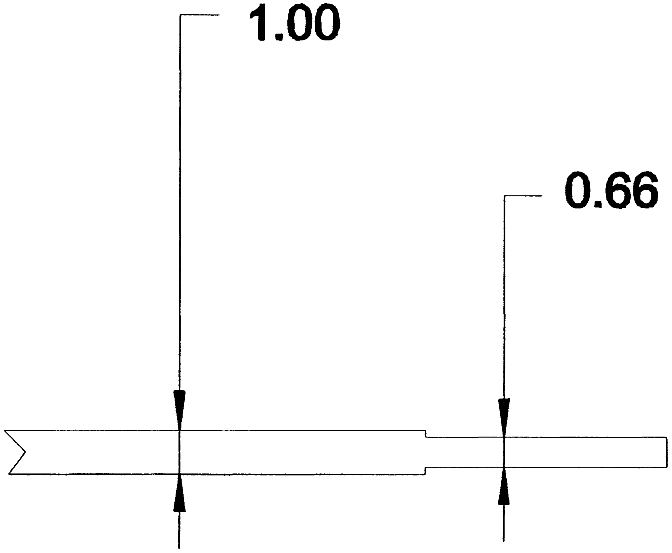


E Block



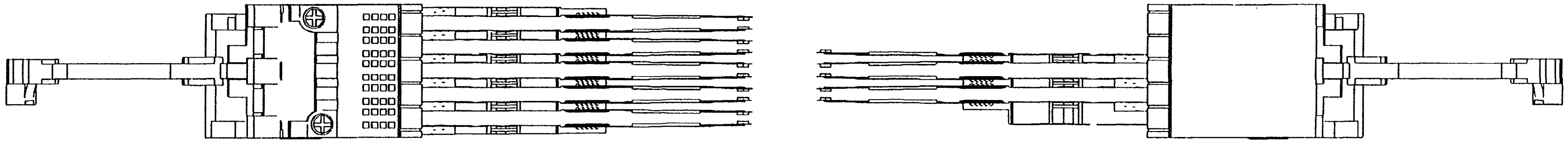
Eblock Arms

- **main arm thickness to be 1.00mm - extruded & machined**
- **swage pad thickness 0.66mm**



3 disk Actuator

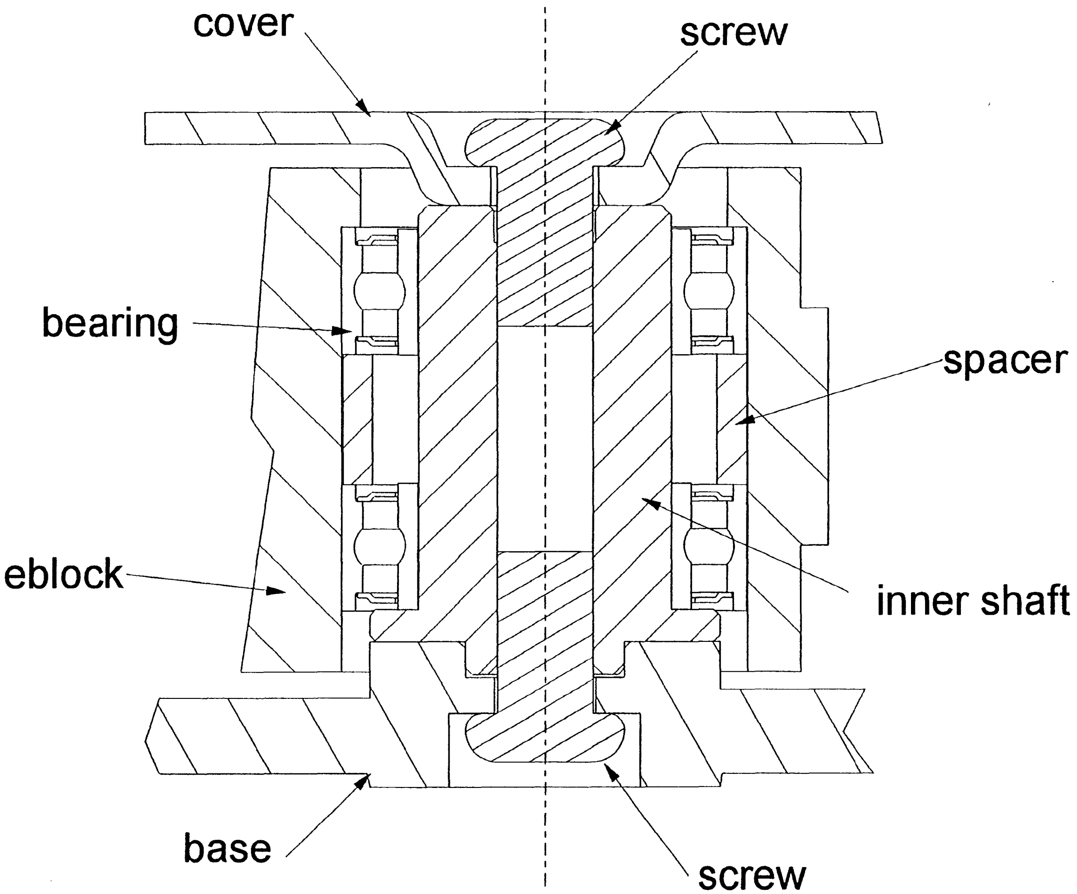
- missing top three arms and lower two arms (three disks in middle positions)
- no lightening holes in arms
- thick lower arm
- same encapsulation thickness, different coil (lighter) for balance



Cartridge Bearing

- “big” bearings (8516 - 1/2” OD) - higher system mode due to higher preload (2 pounds)
- better vertical tolerancing than discrete bearings
- more consistent preload and less thermal expansion sensitivity; therefore, theoretically, more stable system resonance mode
- double screw fastening (two cover screws) with one from the bottom of the base for minimal preload change

Cartridge Bearing Layout



VCM magnet assembly

- **46 MGOe grade magnets**
- **Identical magnet assembly for 3 and 5 disk**
- **Magplate electroless nickel plated**
- **FEM optimization recommends thickest magplates, thickest magnets, and smallest air gap possible**
  - **utilize full 16.3mm maximum z-height for magnet assembly**
  - **magplate thickness limited to 3.2mm by steel stamping process**

VCM Parameters

	5 disk	3 disk
gap to pivot radius (mm)	51.9	51.9
inertia (gm-mm^2)	4,552	3,894
imbalance (gm-mm)	<5	<5
coil resistance (ohms)	5.7	5.7
# turns	150	136
K_t (N-m/A)	0.0606	0.056
bang-bang (ms)	5.53	5.27

VCM magnet assembly

	5-disk	3-disk
magplate thickness (mm)	3.2	3.2
magnet thickness (mm)	3.6	3.6
gap width (mm)	2.7	2.7
max gap flux (gauss)	9200	9200
Kt max(N-m/A)	0.061	0.056
bang-bang access time (msec)	5.53	5.27

Track Layout

- laser zone textured media
- total data stroke = 0.9700”
- slider never flies over textured zone at ID data position
- slider outer corner always inside textured zone at outer landing zone
- allowable crash stop deflection =0.60mm ID&OD
- skews (CG of ABS) = -8.9 °(ID) to 16.3 °(OD)

E1 Track Layout

Phoenix E1 Track Layout
30% slider + Q30 suspension

AL 2/22/96

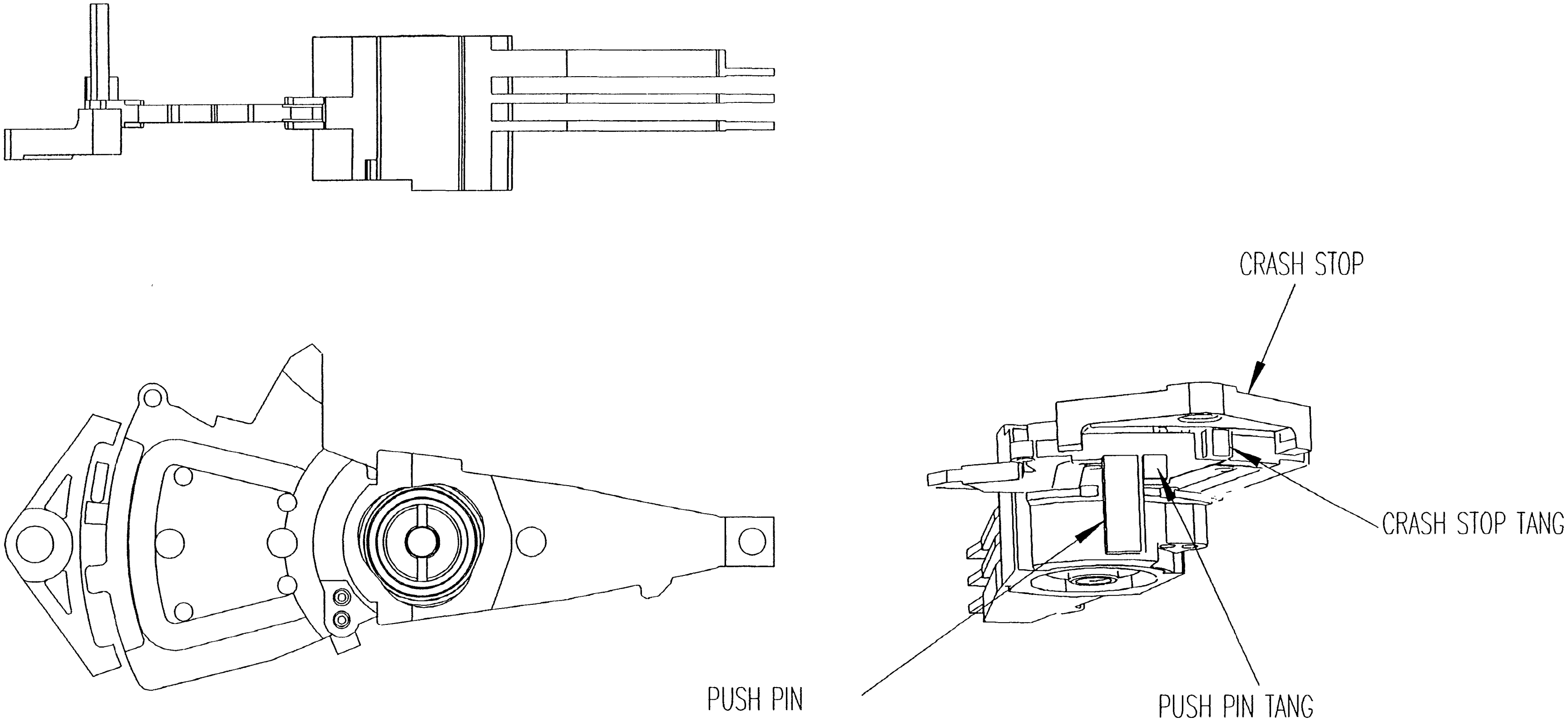
assumptions:
Viking-like plan view/skews
0.6mm crash stop deflection at both ID and OD (velocity limited)
laser textured media with 0.06m edge tolerance
slider NEVER flies over zone texture at ID data radius (inner rail is OUTSIDE of texture)
ENTIRE slider ALWAYS lands in textured zone (outer rail is INSIDE of texture OD)

	mm			inch		
	Min	Mean	Max	Min	Mean	Max
Disk Chamfer	47.0170	47.1960	47.3870	1.8511	1.8581	1.8656
Slider Outer Corner, compressed OD stop	46.3451	46.6357	46.9263	1.8246	1.8360	1.8475
Gap, compressed OD stop	46.2113	46.5019	46.7925	1.8193	1.8308	1.8422
Slider Outer Corner, uncompressed OD stop	45.7451	46.0357	46.3263	1.8010	1.8124	1.8239
Gap, uncompressed OD stop	45.6113	45.9019	46.1925	1.7957	1.8072	1.8186
OD System Track Radius		45.8003			1.8032	
OD Data Track Radius		**45.7156**			**1.7998**	
OD Certified		?				
ID Certified		?				
ID Data Track Radius	20.7836	**21.0769**	21.3702	0.8183	**0.8298**	0.8413
Total Data Stroke		**24.6387**			**0.9700**	
Slider Inner Corner at ID Data	19.9303	20.2236	20.5169	0.7847	0.7962	0.8078
Texture Zone OD (includes tolerances)		**19.7303**			**0.7768**	
Slider Outer Corner, outer landing zone	18.9577	19.1704	19.3831	0.7464	0.7547	0.7631
Gap, outer landing zone	18.5507	18.7634	18.9761	0.7303	0.7387	0.7471
Margin, Slider to ID Data	1.4005	1.9065	2.4125	0.0551	0.0751	0.0950
Air Lock Clearance		0.3413			0.0134	
Gap, uncompressed ID Stop	17.5308	17.9016	18.2724	0.6902	0.7048	0.7194
Slider inner corner, uncompressed ID Stop		17.0641				
Suspension, uncompressed ID Stop	16.2532	16.6240	16.9948	0.6399	0.6545	0.6691
Gap, compressed ID Stop	16.9308	17.3016	17.6724	0.6666	0.6812	0.6958
Suspension, compressed ID Stop	15.6532	16.0240	16.3948	0.6163	0.6309	0.6455
Spacer OD Radius	15.4750	15.5230	15.5820	0.6093	0.6111	0.6135

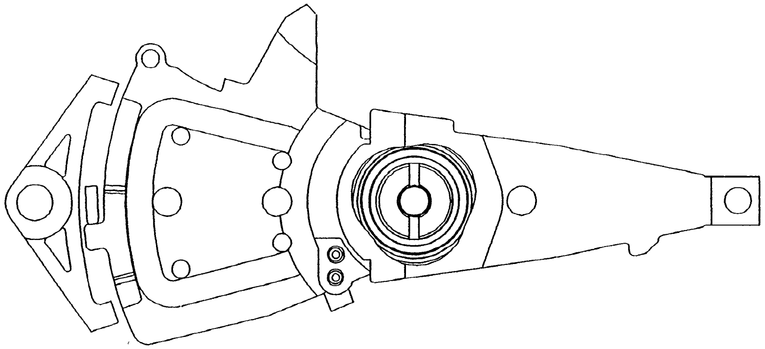
New Servowriter Pushpin Layout

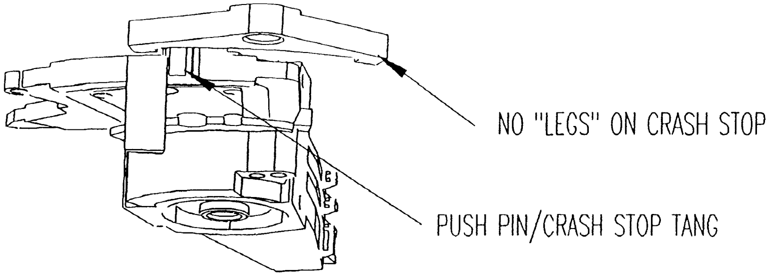
- noticeable 1.2kHz RRO spike on some Phoenix E2 drives - was ~3% problem on Viking
- Bode on servowriter pushing on crash stop tang shows 1.2kHz reduction
- eliminate push pin tang on eblock, push on current crash stop tang
- extend crash stop tang higher to impact crash stop above encapsulation
- cut “legs” off of crash stop
- shift banana slot in base
- new servowriter push pin/stroke
- all changes implemented for E2.5 and beyond

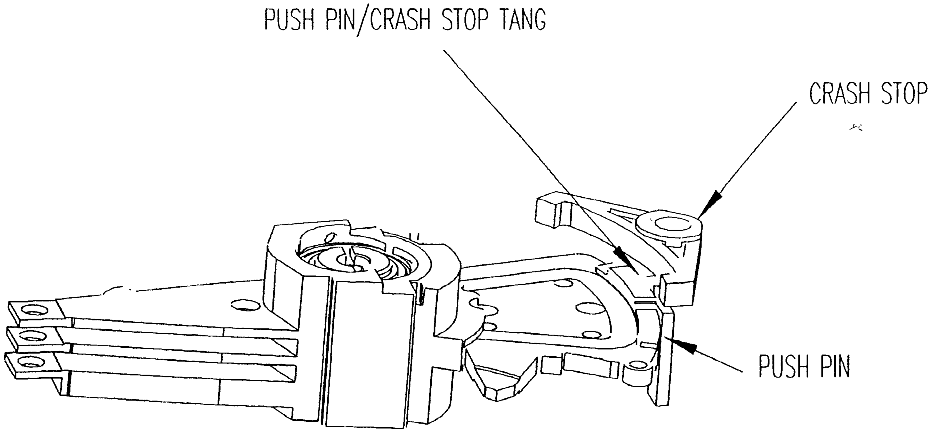
Old Pushpin Layout



New Pushpin Layout

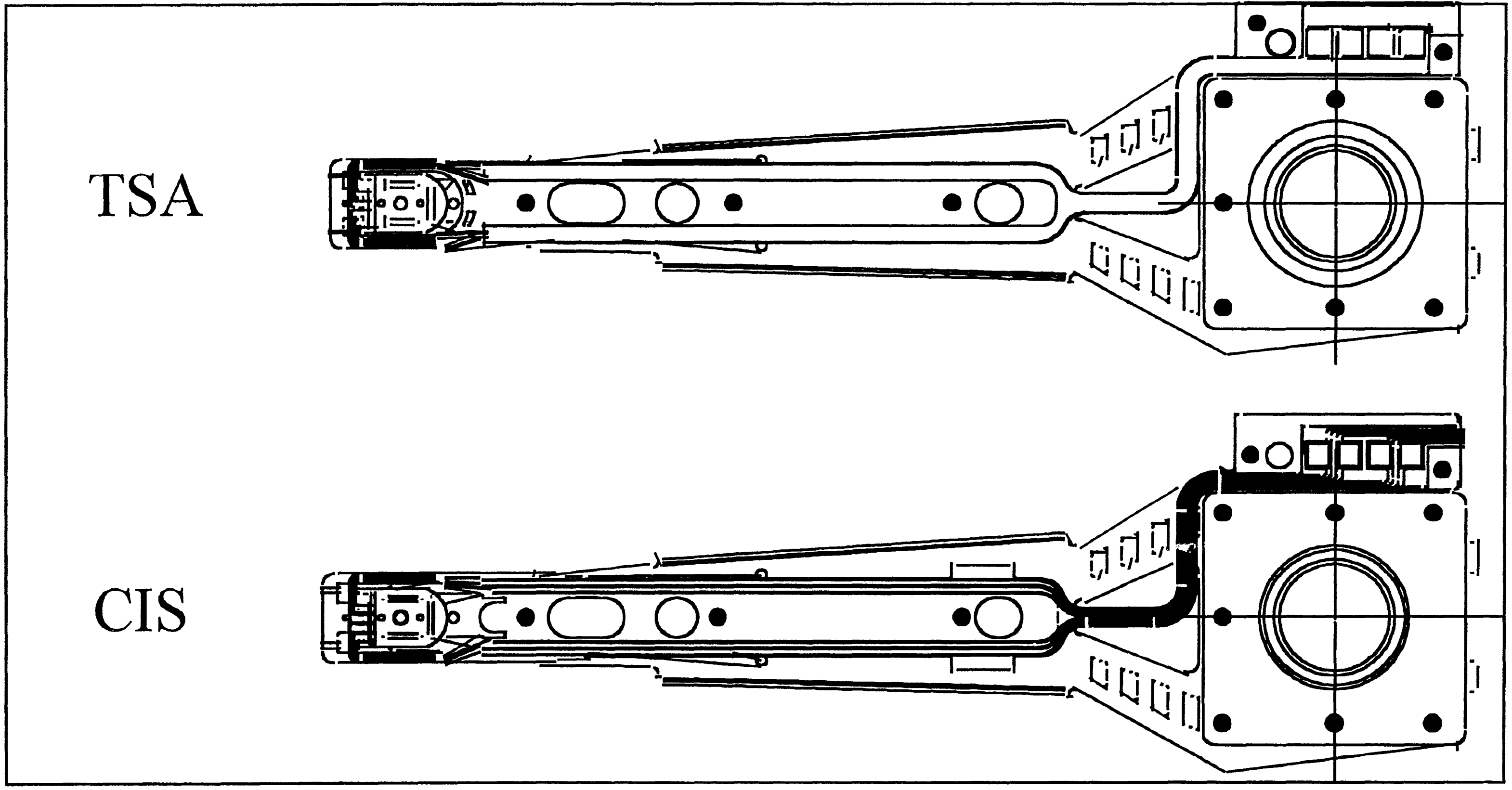






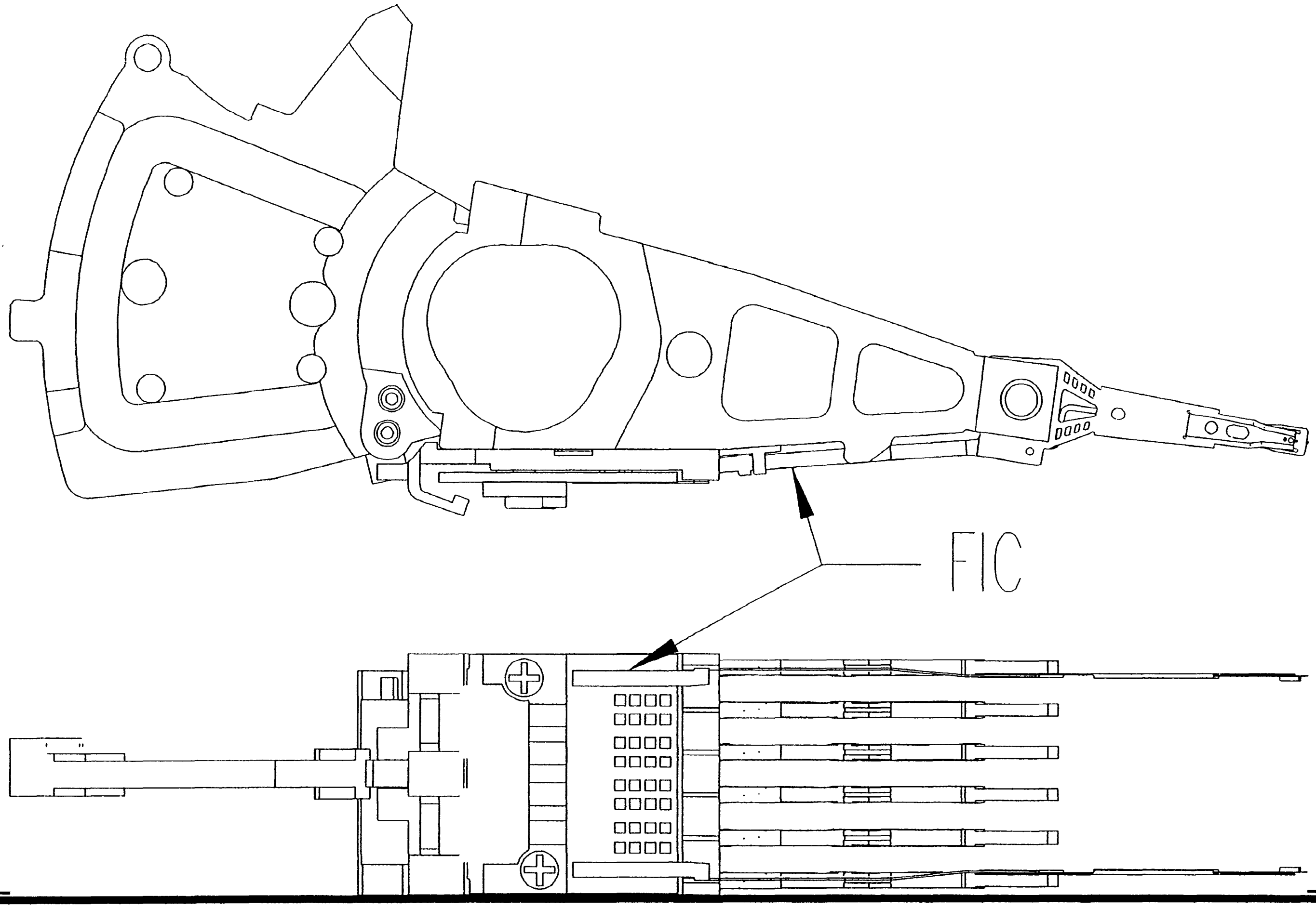
CIS/TSA

- Provides gimbling & replaces twisted wire pairs from heads to end of suspension



Flexible Bump Circuit (FBC)

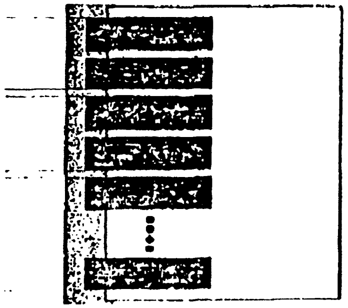
- **Replaces twisted wire pairs from end of suspension to flex**



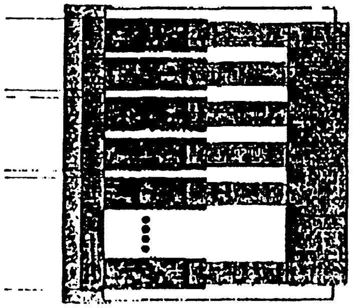
*Flexible Bump Circuit (FBC)**

- **Advantages:**
  - **can attach multiple head lead connections simultaneously through solder reflow (saves process time)**
  - **possible to automate FBC to flex attachment (cost reduction)**
  - **eliminates mis-wiring caused by multiple wires**
- **Challenges:**
  - **solder reflow attachment new process --- still needs maturing**
  - **electrical performance of CIS/TSA + FBC much different from twisted wire pairs**
- *** previously known as FIC (flexible interconnect circuit)**

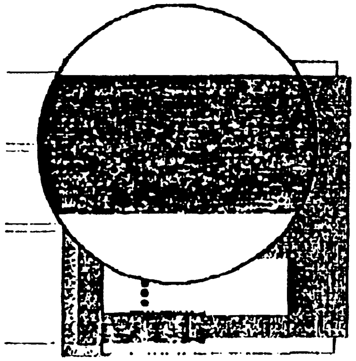
FBC Attachment Procedure



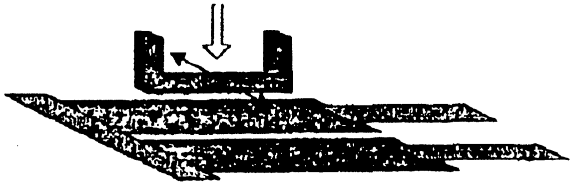
1.Fold FIC and set it on ceramic PCB



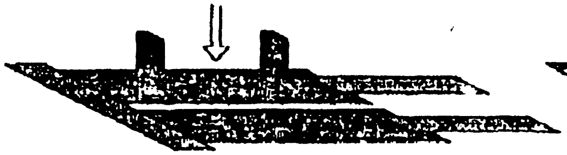
2.Position FIC and fix it one by one



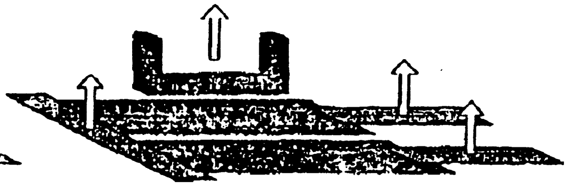
3.Verify by camera and adjust to the right position



4.Down heat tool and adjust the position



5.Press, pre-heat, main heat



6.Cool , up heat tool,and release

- average peel strength measured at 40 gmf per pad
- during P2, introduced single pass process which attaches all 10 FBC's at the same time

Preamp Die-on-Ceramic

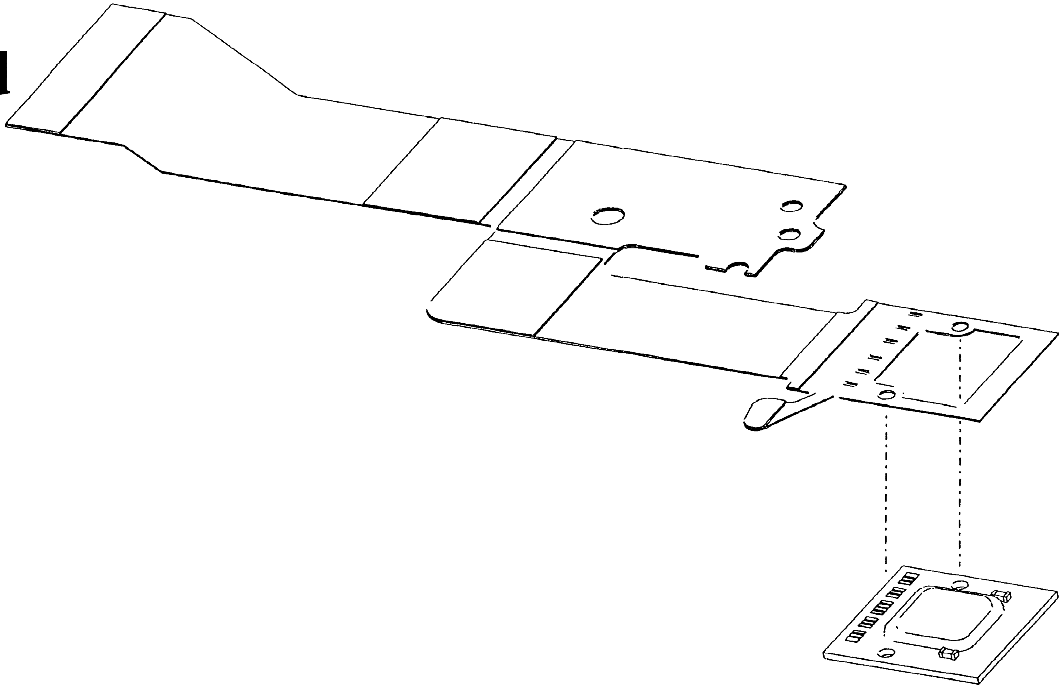
- Why ceramic?
  - 10 MR heads = 40 head pads
  - with increasing head count & I/O's, preamp packaging larger
  - FBC attachment tooling requires additional space around head pads
  - high trace count and density & limited space make flex design difficult and cost expensive
- use multi-layer ceramic for high density packaging
- employ very simple, low cost flex
- electrically and mechanically attach ceramic to flex
- overall cost and reliability better than other options

Preamp die-on-Ceramic

- **5 layers of ceramic**
- **6 layers of Ag/Pt ink conductors**
- **solder plating for head pads to improve FBC attachment**
- **Advantages:**
  - **multiple layers allow for optimized layout**
  - **able to place all components and die on 15.7mm X 15.7mm sq.**
- **Challenges:**
  - **ceramic brittle --- can crack after thermal cycling when screw applied: fastening/attachment spec has been developed carefully based on environmental data**
  - **satisfactory heat dissipation achieved by:**
    - **utilizing conductor-filled "thermal" vias to carry heat through ceramic layers**
    - **employing heat sinking bracket to absorb heat and transfer to air and actuator**

Ceramic to Flex Attachment

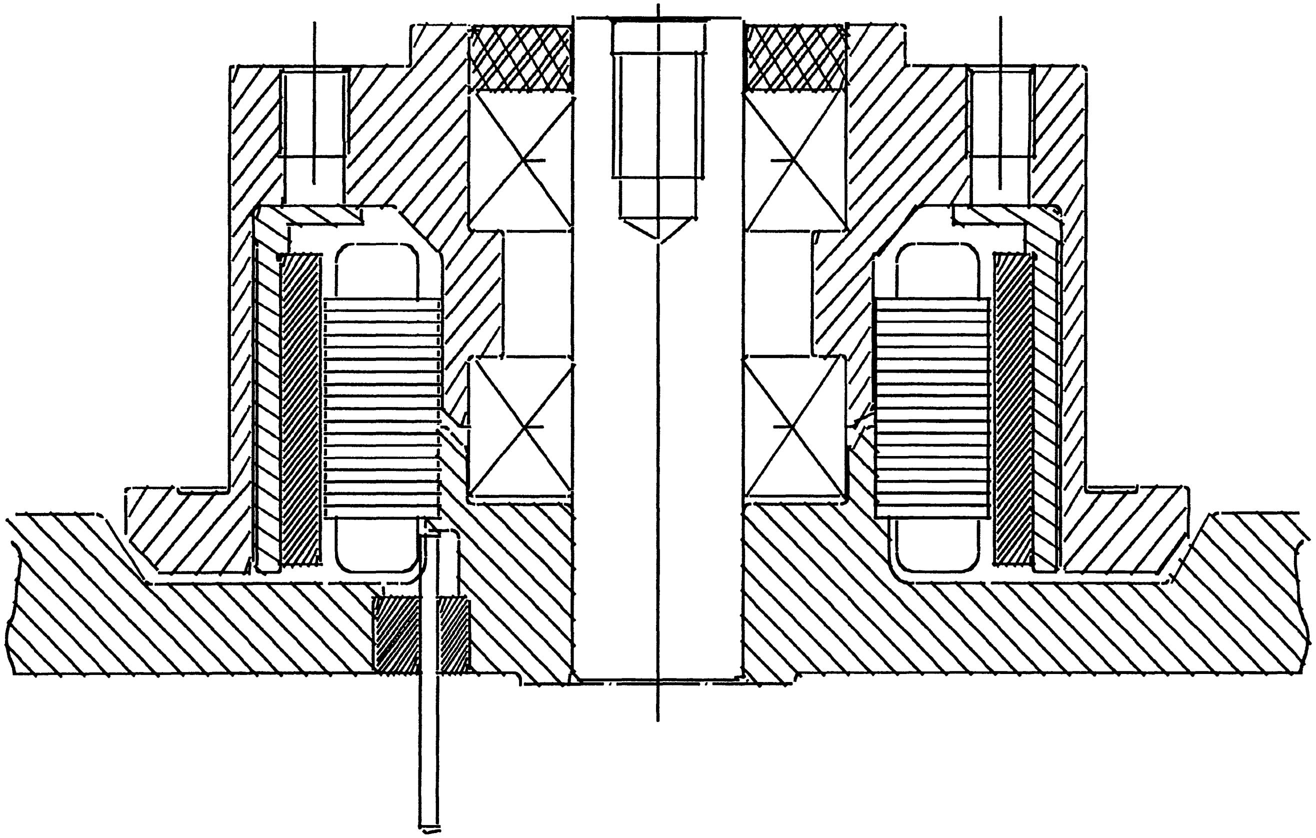
- Reflow solder attachment, similar to FIC process
- Peel strength measured at 200 gmf
- Good reliability under environmental test



Spindle Motor Assembly

- **Motor-in-hub design**
- **Fixed shaft, supported at both ends**
- **Size 1150 bearings**
- **Labyrinth seal**
- **Integral Connector Pins**
- **12 pole magnet, 9 slot stator, 3 phase coils**
- **7200 RPM**
- **Open stator design aids cooling**

5 Disk Spindle Motor

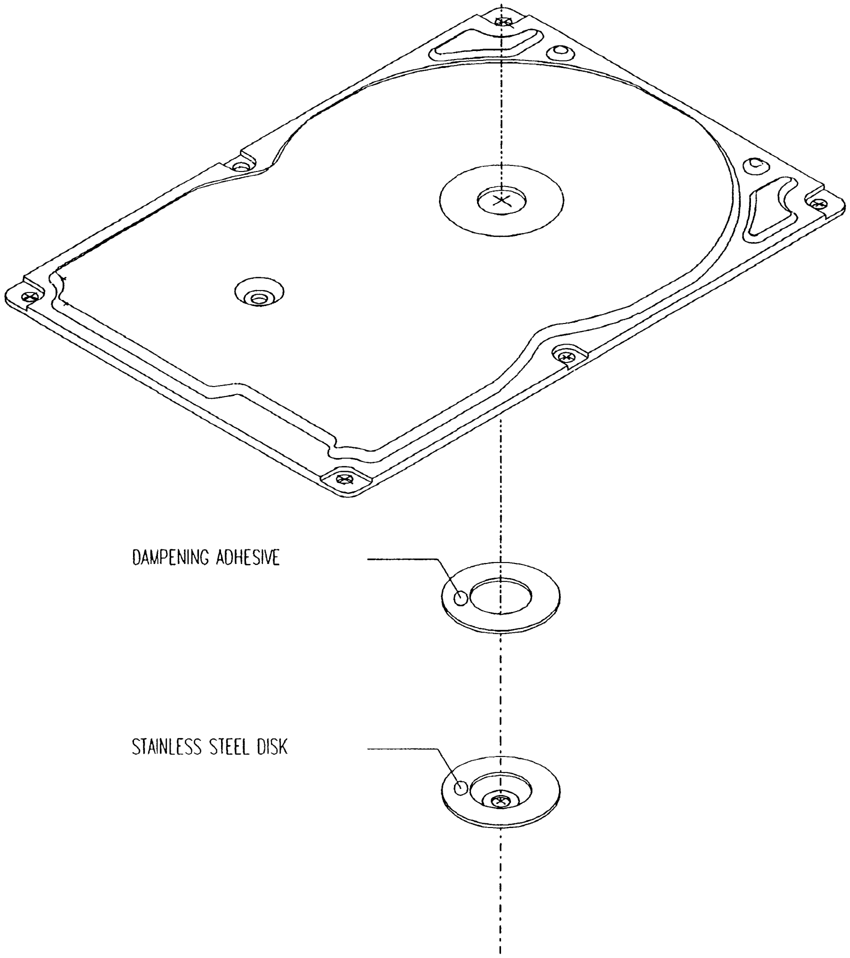


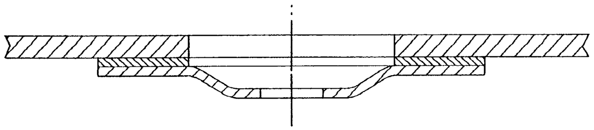
5 Disk Spindle Spec Summary

Parameter	Unit	Nom.	Max.	Min.
Winding Resistance, line-to-oine	ohm	-	2.3	1.9
Resistance Variation, line-to-line	%	-	+3	-3
BEMF, 0-Pk @ 7200	V	8.10	8.59	7.61
Run Current, No Load	A	-	0.170	-
Start Torque to Load @ 2.5A	gm-cm	-	-	171
Detent Torque @ < 5rpm, 0-pk	gm-cm	-	7	-
Leakage Flux	gauss	-	5	-
Bearing Preload	Kgf	1.2	1.4	1.0
Acoustic Noise, drive level sound power	bel	-	4.3	-
Commutation Angle Variation	degree	0	+0.5	-0.5
Bearing NRRO, 0-peak, axial and radial	u-in	see	#7.5	-
Balance	mg-cm	-	80	-
Bearing Axial Deflection @ 460 gmf	u-in	-	20	-
Particle Count, 0.1 micron or greater	total	-	50	-
, 0.3 micron or greater	total	-	15	-
, 0.5 micron or greater	total	-	10	-
Inductance @ 1kHz, phase to phase	uH	-	TBD	-
Rocking Frequency, Lower	Hz	-	TBD	TBD
Rocking Frequency, Upper	Hz	-	-	TBD

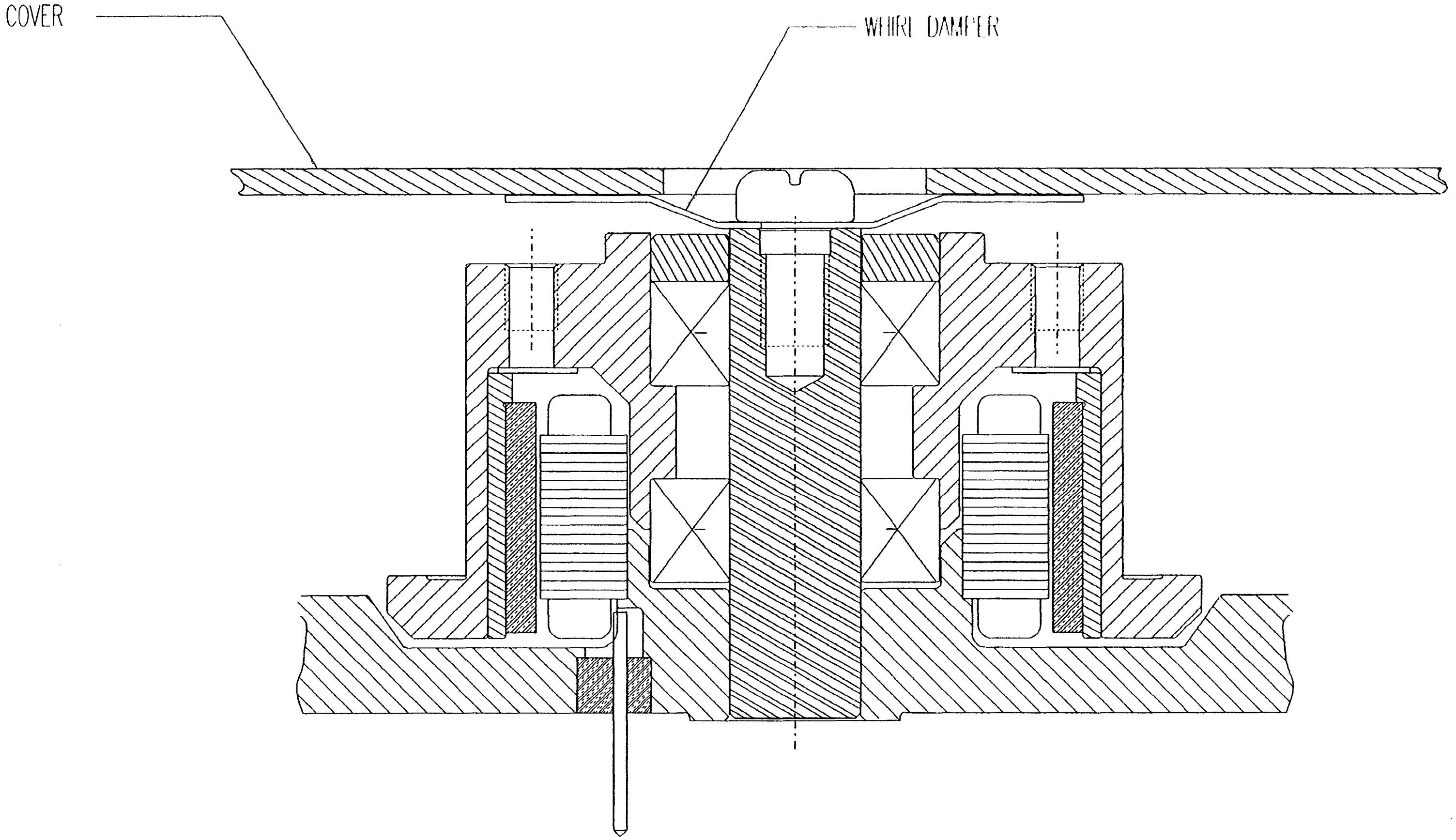
Whirl Damper

- **what is it?**
  - **thin dampening adhesive which isolates the spindle motor from the cover**
- **what does it do?**
  - **reduces amplitude of the rocking mode**

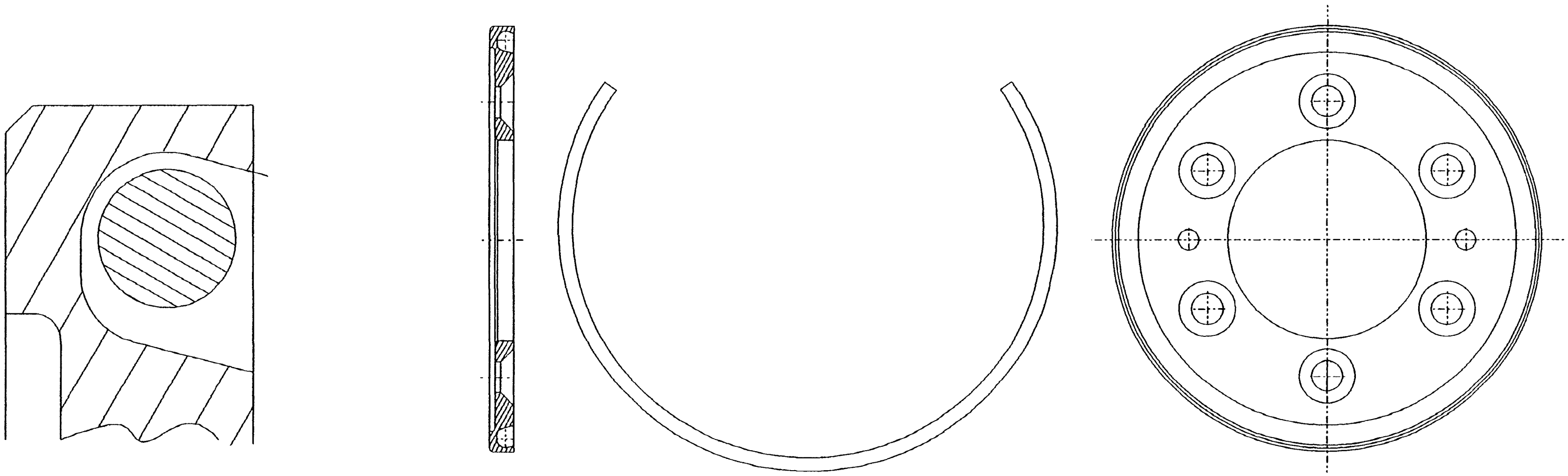




Whirl Dampe



Balance Metho



Airlock Design G

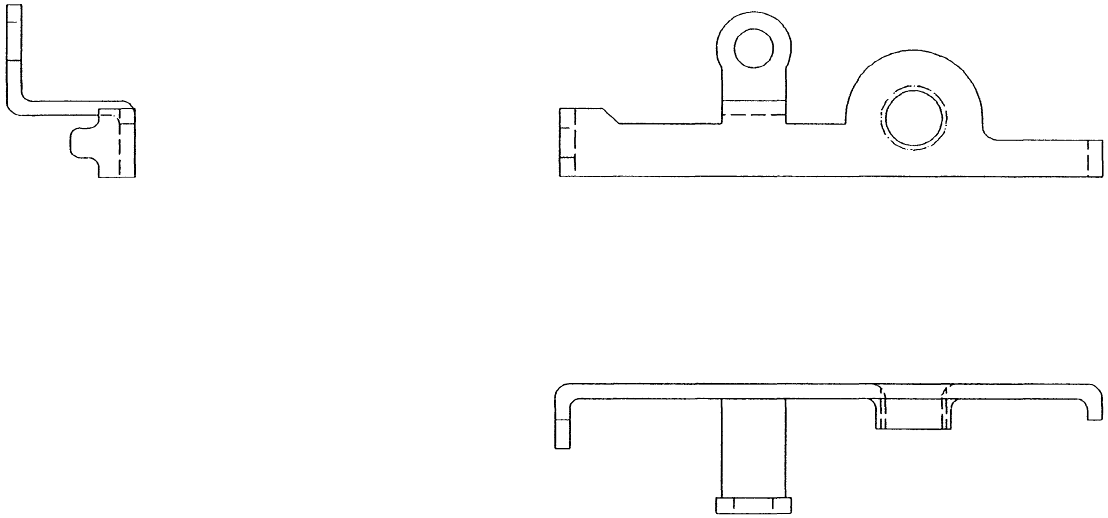
- Retain the Viking airlock shaft and ball
- Stubby design for enhanced shock performance
- Meet rotational shock spec. of 15k rad/sec^2, 2ms
- Meet linear shock spec. of 200g's, 2ms
- Max. open speed of 6500 RPM and min. closing speed of 3500 RPM.
- Small opening/closing rpm delta for better operating margin

Magnetic Return S

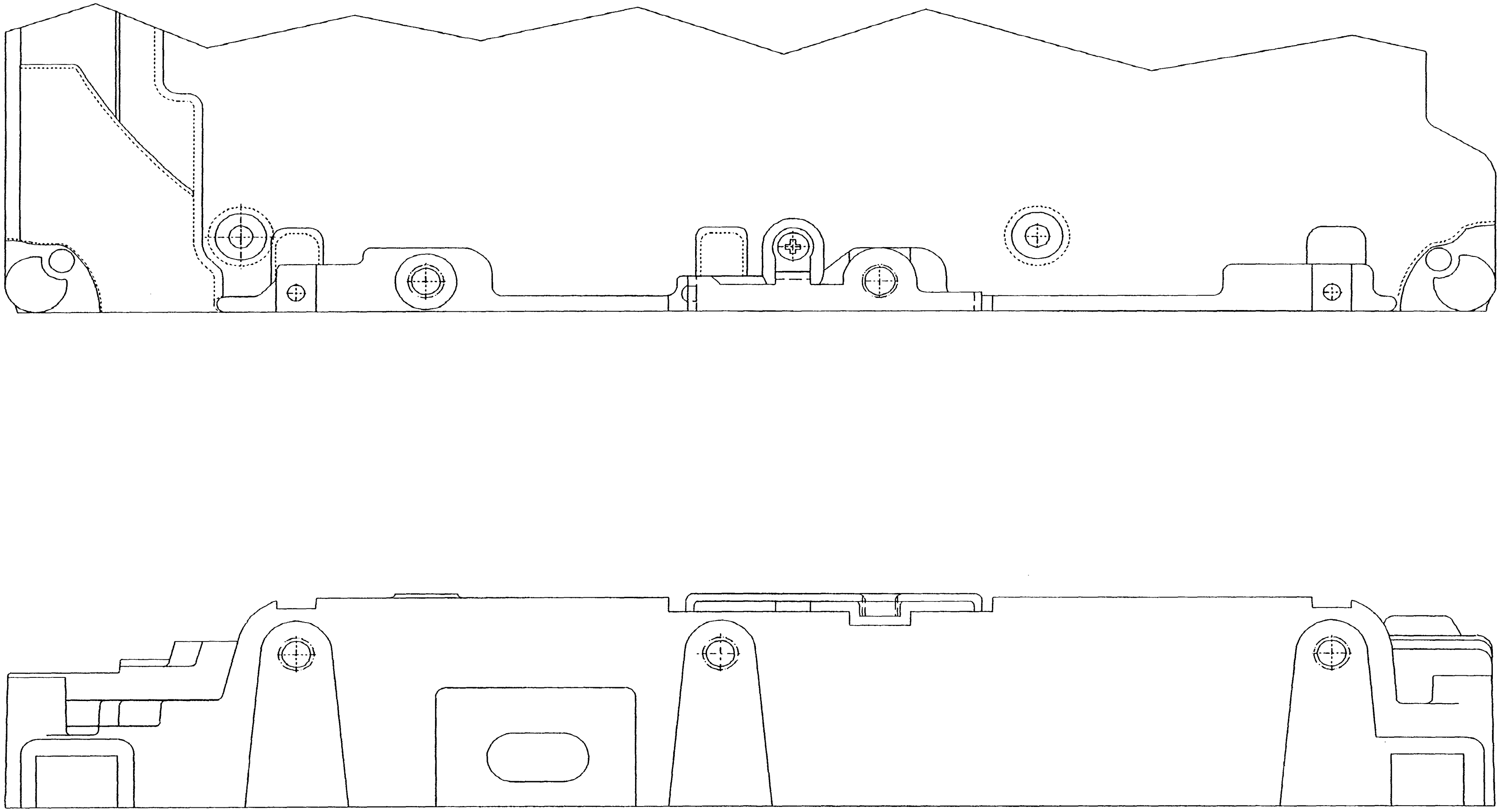
- Mechanical features which always biases actuator towards inner crashstop
- Ensures that actuator is in landing zone during spin down, even with low airlock closing RPM
  - Heads never land in data zones
- Redundant latch if airlock fails
- Designed to minimize impact on servo
- Will partially populations HDA's during P2.5 checkbuild ... if successful, will phase in for PMP and beyond

Shock Isolation Clip

- **Sheet metal spring clip replaces one of the four PCB side mounting points**
- **Creates "rigid" 3-point mounting condition while providing substantial protection for short duration shock**



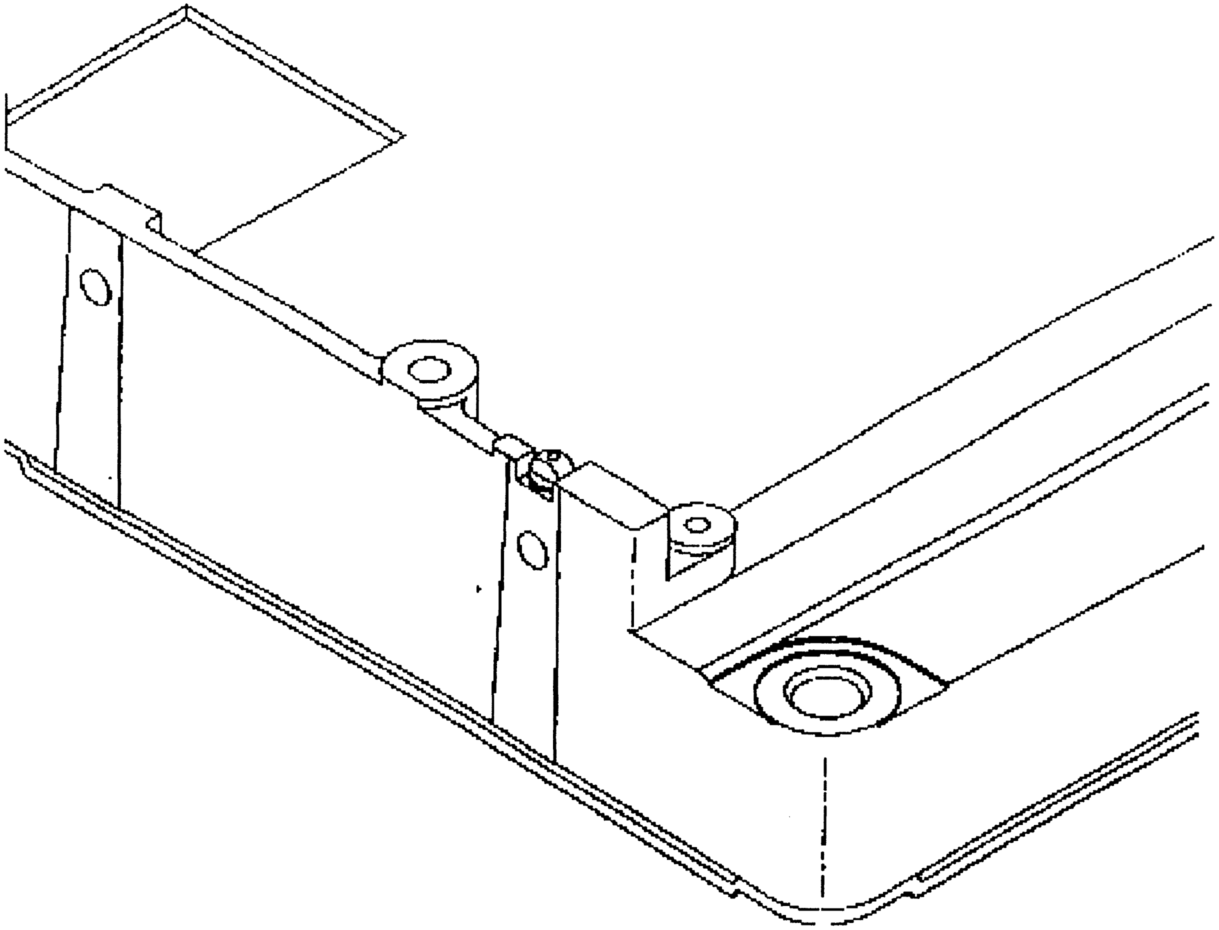
Shock Isolation Clip



Shock Feet

- Small, polypropylene feet that act as shock absorbers during bare handling
- Increases the pulse width and decreases amplitude of shocks induced to drive during handling
- Set of feet on both PCB and cover sides
- Feet protrude slightly from drive, and compress when installed

Shock Feet



Head Slap Fragility Test

- Iterative test to determine shock amplitude that induces head slap for various length half-sine shock pulses
- Use of an electrodynamic shaker as a shock machine
- Disks are divided into "zones" that are shocked in 10 g increments
- Media are inspected under microscope (60x) for signs of damage

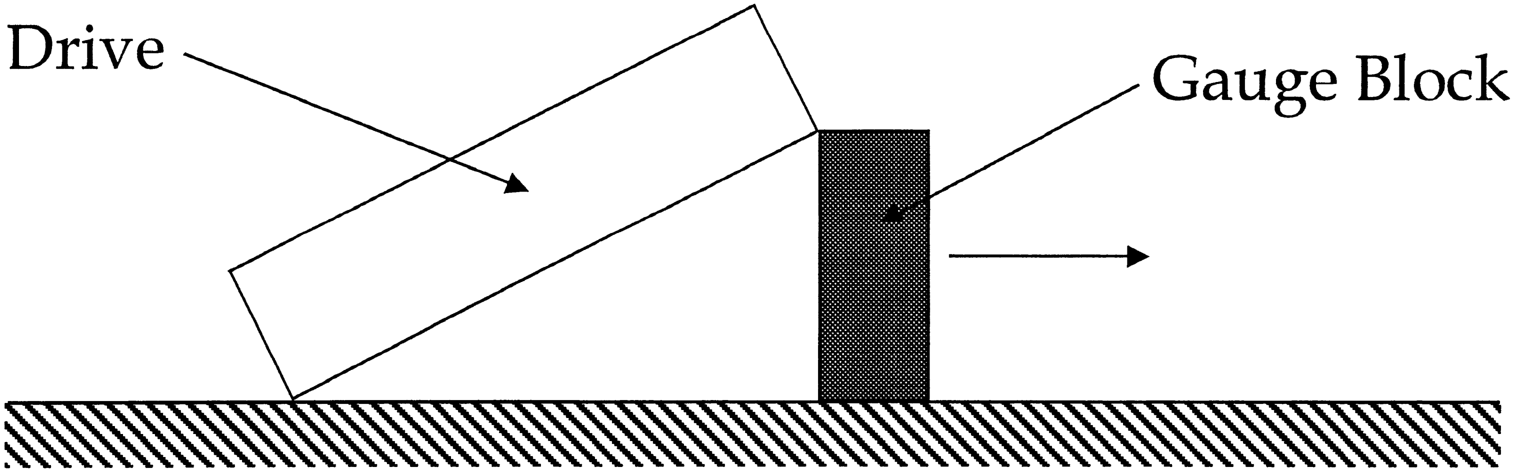
Head Slap Damage Threshold

	0.5 ms	1.0 ms	2.0 ms
Phoenix 4.5 GB (3 Disk)	100 g	120 g	>170 g
Phoenix 9.1 GB (5 Disk)	80 g	70 g	160 g

* Head Slap Threshold is defined as the amplitude at which head slap is first seen

Angle Drop Shock Test

- Simulates likely bare handling shock, and is used as one metric to measure drive handling fragility
- One end of the drive is lifted off a hard countertop (formica) and then dropped to shock the drive
- Survival of 2.5" drop is considered very robust



Angle Drop Test Results

	Angle Drop Test Height for Head Slap
Phoenix 4.5 GB (3 Disk)	> 3.5 “
Phoenix 9.1 GB (5 Disk)	> 3.5″

* Test conducted up to 3.5″ and no damage was seen in either model

PHOENIX TRAINING MANUAL

HEADS & MEDIA

November, 1997

PHOENIX

New Product Training
November 1997

Heads & Media Section

Phoenix Head/Media Design Review

- Specification Overview
- Fly Height Budget
- Electrical Performance
- CSS Performance
- Key Challenges to Date
- Supplier Statues

Specification Overview - Recording Performance

	Viking	Phoenix
RPM	7200	7200
Areal Density (Mbpsi)	900	1530
Track Density (TPI)	6432	8500
Linear Density, ID-OD (KFCI)	140-109	180-140
Frequency @ OD (MHz)	74 MHz	91 MHz

Specification Overview - Head Transducer

	Viking	Phoenix
MR Trans. Bias	SAL	SAL
MR Long. Bias	PM/AFM	PM/AFM
Write Width, Norminal(μm)	3.0	2.3
Write Gap Length (μm)	0.4	0.4
Read Width, Nominal (μm)	2.4	1.9
Read Gap Length (μm)	0.3	0.26
Top Pole Bsat (kG)	10 ($Ni_{80}Fe_{20}$)	16(~$Ni_{50}Fe_{50}$)

Specification Overview - Head Mechanical

	Viking	Phoenix
Slide Size	50%	30%
Air Bearing	NPAB	NPAB
Gram Load	3.5 g	2.5 g
Z - Height	26.4 mil	26.4 mil
Suspension	T850	Q30U
Connection	Wire/Tube	CIS or TSA/FIC
Fly Height, Nominal (u")	2.4	2.0
Fly Height, Min. (u")	1.9	1.4

Specification Overview - Media

	Viking	Phoenix
MrT(G-μm)	125	100
Coercivity (Oe)	2200	2300
Texture	Full Texture	Laser Zone Texture
GH, Data Zone (μ“)	1.2	1.0
GH, Landing Zone(μ“)	1.2	1.5

Fly Height Budget Analysis

- **A Mote-Carlo tool to monitor vendor's fly height and glide height distributions.**
  1. **Obtain mean & sigma of FH and GH distributions.**
  2. **Obtain gram load mean & sigma after stacking.**
  3. **Generate FH distribution and clearance at sea level after stacking.**
- **10K ft fly height and clearance estimation**
  1. **Obtain altitude sensitivity data from ABS design.**
  2. **Generate FH distribution and clearance at 10K ft after stacking.**

Phoenix HGA Fly Height Performance

Nominal Fly Height and Stdev

		ID			MD			OD	
Vendor	OT	GAP	STDEV	OT	GAP	STDEV	OT	GAP	STDEV
TDK	2.05	2.04	0.24	2.08	2.05	0.23	2.14	2.00	0.27
YAMAHA	2.88	2.61	0.15	2.84	2.40	0.13	2.95	2.36	0.16
ALPS	2.01	2.03	0.13	2.24	2.14	0.12	2.23	1.97	0.14

Gram Load and Altitude Sensitivities

Vendor		**Gram Load (u"/g)**	
	ID	MD	OD
TDK	-0.36	0.437	0.727

	Altitude (u"/10K ft)	
ID	MD	OD
-0.316	-0.356	-0.274

Electrical Performance Specification

Test Radius	**1.7392”**	**1.3148”**	**0.8298”**
Gap skew	15.76	6.74	-7.036
RPM	7200	7200	7200
Lv (ips)	1311.3	991.3	625.7
Test Frequency (Mhz)			
HF	91.79	74.35	56.31
MF(1/2 HF)	45.90	37.18	28.16
LF(1/6 MF)	7.65	6.20	4.69
NLTS(1/3 HF)	30.60	24.8	18.8
Performance Requirements			
TAA (MF)	350 uV min	350 uV min	350 uV min
TAA Asymmetry	-15 to +15%	-15 to +15%	-15 to +15%
PW50 (Positive and Negative)	400 nm max	400 nm max	400 nm max
PW50 Asymmetry	12% max	12% max	12% max
Overwrite (MF/LF)	- 30 dB	-30 dB	-30 dB
Amplitude COV	2.5% max	2.5% max	2.5% max
NLTS (HF over 1/3HF)	-12dB	-12 dB	-12 dB

Electrical Performance at P2 - Head Suppliers, Spin Stand Test

P1 Heads DET Data Using a MCC Disk (100 Gum, 2250 Oe) As Reference

Radius (in)	Vendors	PW50 (nm)	ASYM (%)	MFTAA (uV)	Res (%)	OW (dB)	NLTS_5 (dB) 5th Harm	COV (%)
0.8298	**Spec**	**<400nm**	**<15%**	**>350**	**NA**	**>30**	**<-12 dB**	**<2.5**
	TDK	333	7.3	510	70	35	-18	1.08
	Yamaha	314	-0.37	400	73	34	-16	0.98
	Alps	299	3.3	450	80	40	-23	0.88
1.3148	**Spec**	**<400nm**	**<15%**	**>300**	**NA**	**>32**	**<-12 dB**	**<2.5**
	TDK	329	9.0	620	86	37	-32	1.06
	Yamaha	321	0.1	460	84	33	-28	1.06
	Alps	306	4.2	500	92	40	-30	1.00
1.7392	**Spec**	**<400nm**	**<15%**	**>300**	**NA**	**>32**	**<-12 dB**	**<2.5**
	TDK	348	8.9	670	92	37	-25	1.17
	Yamaha	352	-0.03	440	91	32	-26	1.04
	Alps	332	3.8	480	95	38	-24	1.21

Note: Data taken from the average of 20 sets of heads from each group.

P2 Disk Suppliers, Spin Stand Test

Phoenix P1 Media Evaluation with TDK P1.5 Head

Radius (in)	Vendors	PW50 (nm)	MFTAA (uV)	Res (%)	OW (dB)	NLTS_5 (dB) 5th Harm
0.8298	**MCC**	314	560	76	33	-22
	AKCL	317	550	74	32	-14
1.3148	**MCC**	318	630	87	34	-27
	AKCL	324	640	85	32	-28
1.7392	**MCC**	344	610	93	34	-19
	AKCL	352	670	91	31	-23

Note: Data taken from the average of 20 pcs of disks from each group.

Phoenix Media Design Parameters

Vendor		**MCC**	**AKCL**
Substrate & Under-layer	**Material**	Al	Al
	Material	Cr	Cr
	Structure	Sub/Cr/Mag	Sub/Cr/Mag
Magnetic Layer	**Material**	CoCrTa	CoCrTaX
	Coercivity (Oe)	2300	2230
	MrT (G.um)	110	99
	S	> 0.8	0.78
	S*	0.75	0.86
Texture & Glide Height	**Type**	Laser Zone Texture	Laser Zone Texture
	Bump Height (A)	225	230
	Bump Density	10um x 4um	60um x 60um
	Data Zone Ra (A)	15	10
Lub	**Material**	Z-DOL	Z-DOL
	Thickness	18 A	40 A
	Bonded Ratio %	44	67
Overcoat	**Material**	Advance Carbon, Hydrogen &Nitrogen	Advance Carbon, Hydrogen &Nitrogen
	Thickness	150 A	100 A

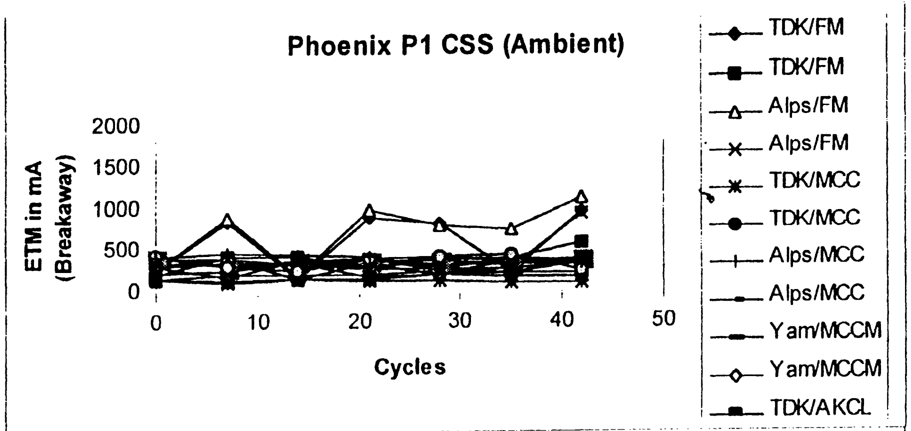
Drive Level CSS Performance:

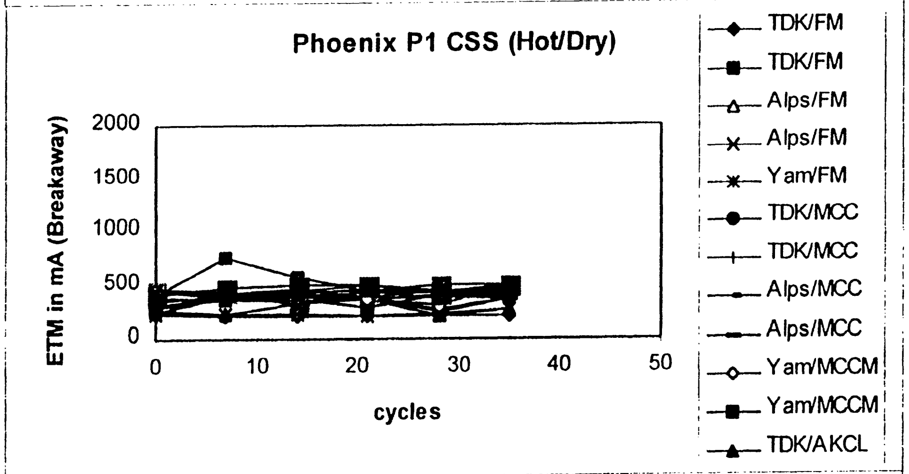
- Head Vendors: TDK, Yamaha, ALPS
- Media Vendors: MCC, AKCL

- Test Conditions/Quantity:

Ambient:	23+/-3 deg C, 50+/- 3 % RH
Hot Dry:	50+/3 deg C, 15+/-3 % RH
Warm/Wet:	32+/-3 deg C, 80+/-3% RH

Spec. is 20 K cycles, Test to 42 K cycles at all conditions.


Phoenix P1 CSS (Ambient)
ETM in mA (Breakaway)
2000
1500
1000
500
0
0
10
20
30
40
50
Cycles
TDK/FM
TDK/FM
Alps/FM
Alps/FM
TDK/MCC
TDK/MCC
Alps/MCC
Alps/MCC
Yam/MCCM
Yam/MCCM
TDK/AKCL


Phoenix P1 CSS (Hot/Dry)
ETM in mA (Breakaway)
2000
1500
1000
500
0
0
10
20
30
40
50
cycles
TDK/FM
TDK/FM
Alps/FM
Alps/FM
Yam/FM
TDK/MCC
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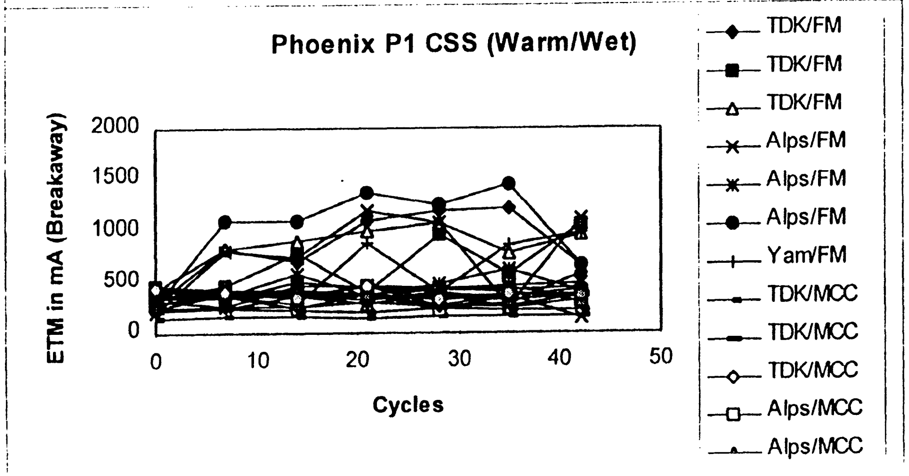
Alps/MCC
Yam/MCCM
Yam/MCCM
TDK/AKCL


Phoenix P1 CSS (Warm/Wet)
ETM in mA (Breakaway)
2000
1500
1000
500
0
0
10
20
30
40
50
Cycles
TDK/FM
TDK/FM
TDK/FM
Alps/FM
Alps/FM
Alps/FM
Yam/FM
TDK/MCC
TDK/MCC
TDK/MCC
Alps/MCC
Alps/MCC

Key Challenges to Date

- 1st Qntm Program With

  1. Pico Form Factor
  2. Quantum-designed Suspension (Q30U)
  3. Integrated Wire on Suspension (CIS/TSA)
  4. Flex Integrated Connector From Suspension to Preamplifier (FIC)

- 2nd Qntm Program With LZT Media (1st being Stratus)

Phoenix Head Vendor Status Overview

Head Vendor	Head Design	Comments
TDK	Option4 Pico, 2-layer coil HiBsat writer to improve NLTS.	1. Very good electrical performance. 2. Mature pico process. 3. Coming up to speed with Q30D/FIC assembly.
Yamaha	2-layer coil HiBsat writer design.	1. Mature pico process. 2. Coming up to speed with Q30D/FIC assembly. 3. Need improvements on TAA and NLTS performance.
Alps	HiBsat top pole writer design.	1. Mature MR process. 2. 1st pico program, good samples so far.

Phoenix Media Vendor Status Overview

Media Vendor	Media Design	Comments
MCC	LZT; 2300 Oe, 110 Gum	1. Mature LZT process. 2. Good magnetic performance. 3. Good CSS performance.
AKCL	LZT; 2230 Oe, 99 Gum	1. 1st LZT program. 2. Good CSS performance. 3. Need improvements on OW.

PHOENIX

PHOENIX

New Product Training
November 1997

Read / Write Section

Phoenix Read/Write Channel Overview

Key Features

- 1820 Mbytes/disk
- MR heads with 30% sliders (Q30 suspension), integrated wiring
- PRML channel with EPR4 detector

Capacity

- 5 disks/10 heads -- 9.1 Gbyte -- 17774666 user sectors
- 3 disks/5 heads -- 4.55 Gbyte -- 8887333 user sectors

Overview ... continued

Organization

- Id-less track format
- 90 wedges/track
- 16 recording zones -- 10 system cylinders
- 150 -- 259 physical sectors per track
- 8500 tracks per inch, 8338 total tracks
- Embedded servo with split data sectors
- Overlapping reads for improved format efficiency

Overview ... continued

Recording Specs

- 16/17 (0,12,12) PRML encoding with scrambler
- MR head, 2.3 um writer width, 1.9 um reader width
- Thin film 2300 Oe media
- Data rates from 98 to 169 Mbits/s
- Max FCI = 167,590 -- Max BPI = 157,730
- Max areal density = 1.34 Gbit/sq. in.
- Writer width to track pitch ratio: 76.7 +/- 10%

Jackhammer Read Channel Device Features

- Jackhammer is a 190 Mbit/s read channel ASIC implemented in 0.35 um CMOS.
- Based on the proven Hammer architecture used in other Quantum products.
- PRML channel features include:
  - ☐ Internal AC coupling with programmable corner frequency
  - ☐ 5 step, 12 dB range input attenuator
  - ☐ AGC digitally controlled in READ mode, analog or digital in SERVO
  - ☐ 4th order Butterworth continuous time data filter with programmable zeros
  - ☐ 10 tap discrete time adaptive FIR equalizer

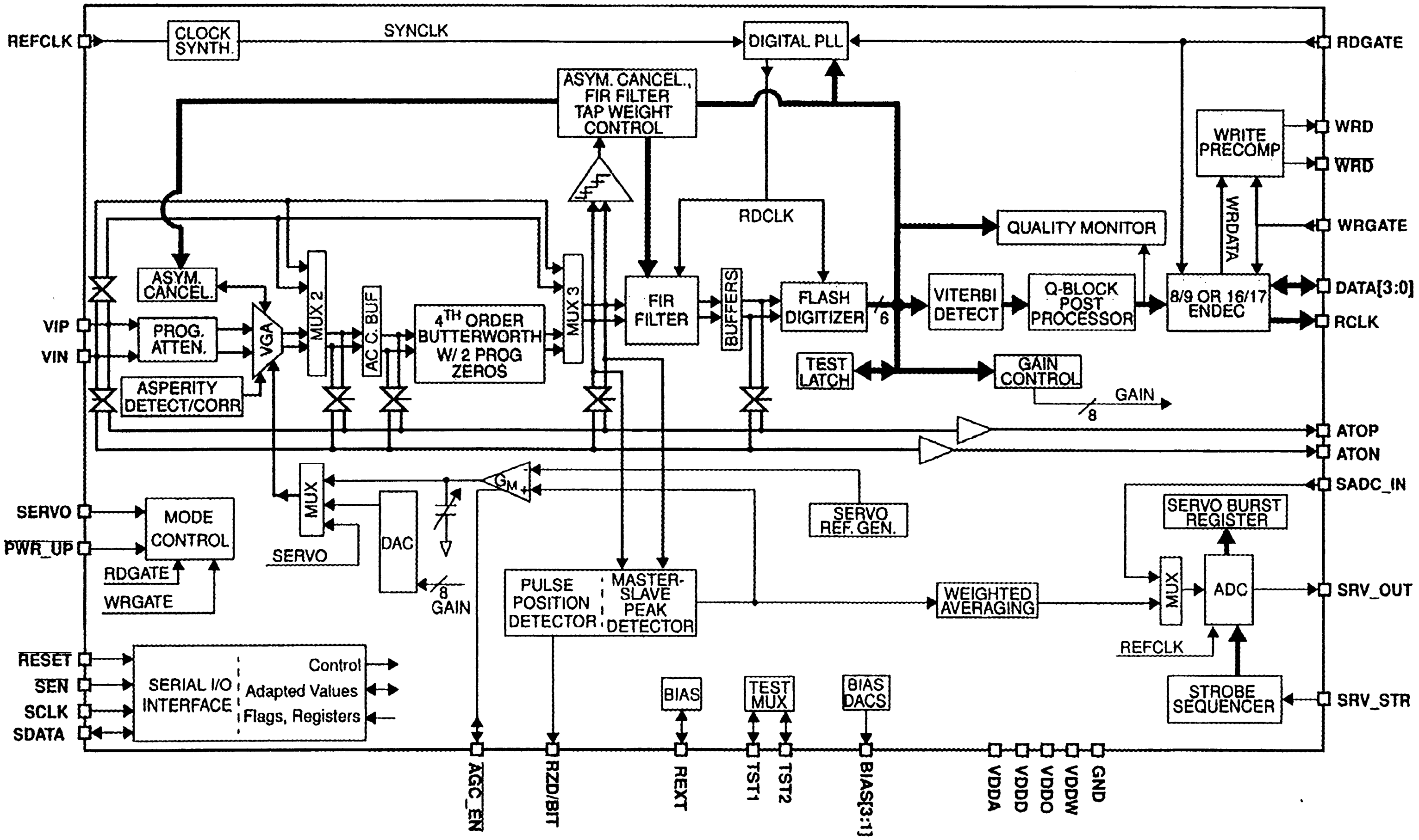
Jackhammer Channel Features ... continued

- ☐ 38 level flash quantizer (5.25 bits)
- ☐ Interleaved dicode Viterbi detectors
- ☐ Digital sample driven PLL
- ☐ Overlapped read support for reduced read-to-read latency
- ☐ Quality monitor (MSE)
- ☐ Thermal asperity detection and correction
- ☐ Nonlinear canceller to reduce MR head nonlinearity

Jackhammer Features continued ...

- Custom Quantum-designed block (Q-block post-processor)
  - ☐ EPR4 detector
  - ☐ Sequence Amplitude Margin for BER estimation
  - ☐ Harmonic sensor for parametric measurements
- Servo Interface
  - ☐ Servo demodulation via "weighted sum" averaging peak detection
  - ☐ Pulse position detector for reading gray code
  - ☐ Digital demodulator output using internal 8 or 9 bit A/D
- Thermally enhanced 100-pin TQFP package
- Low power consumption (1.2 watt read mode at 170 Mbit/s)

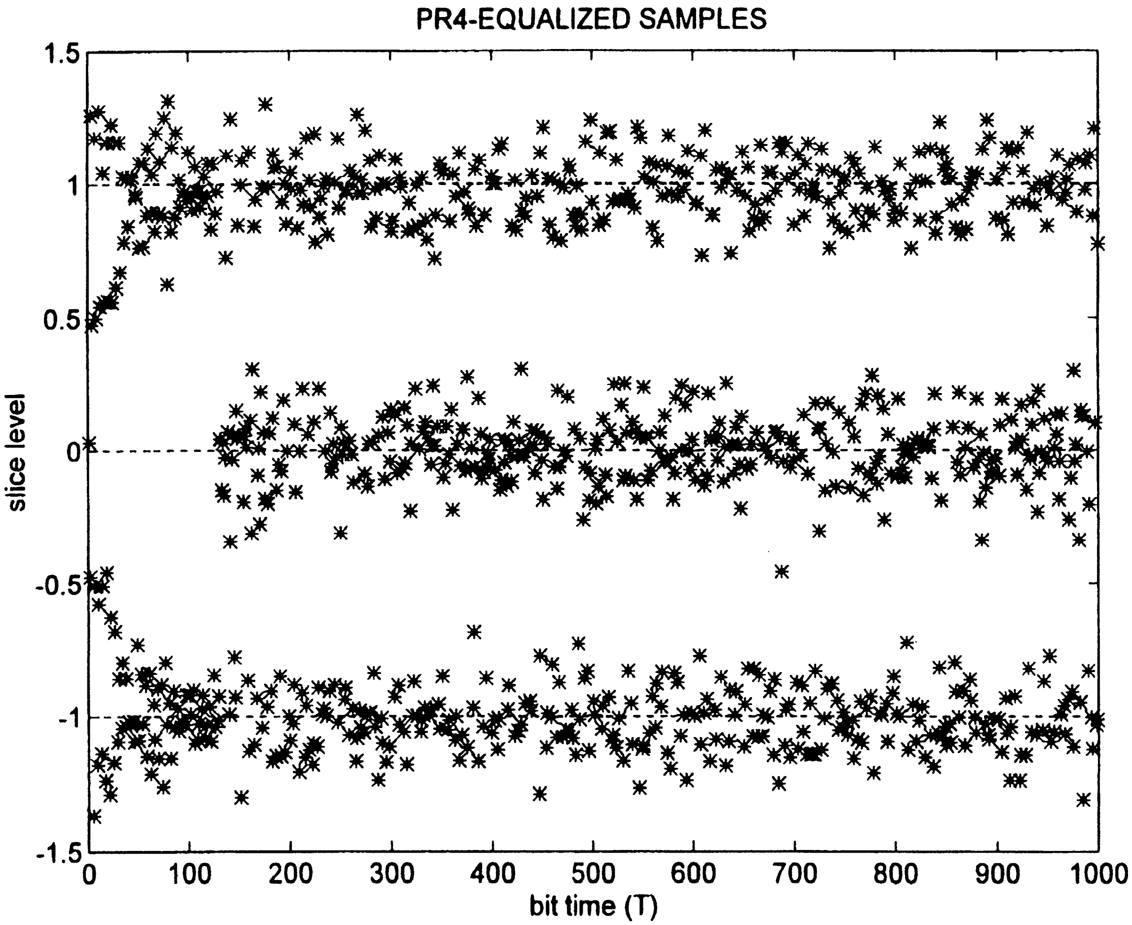
Jackhammer Block Diagram



Read Channel Optimization

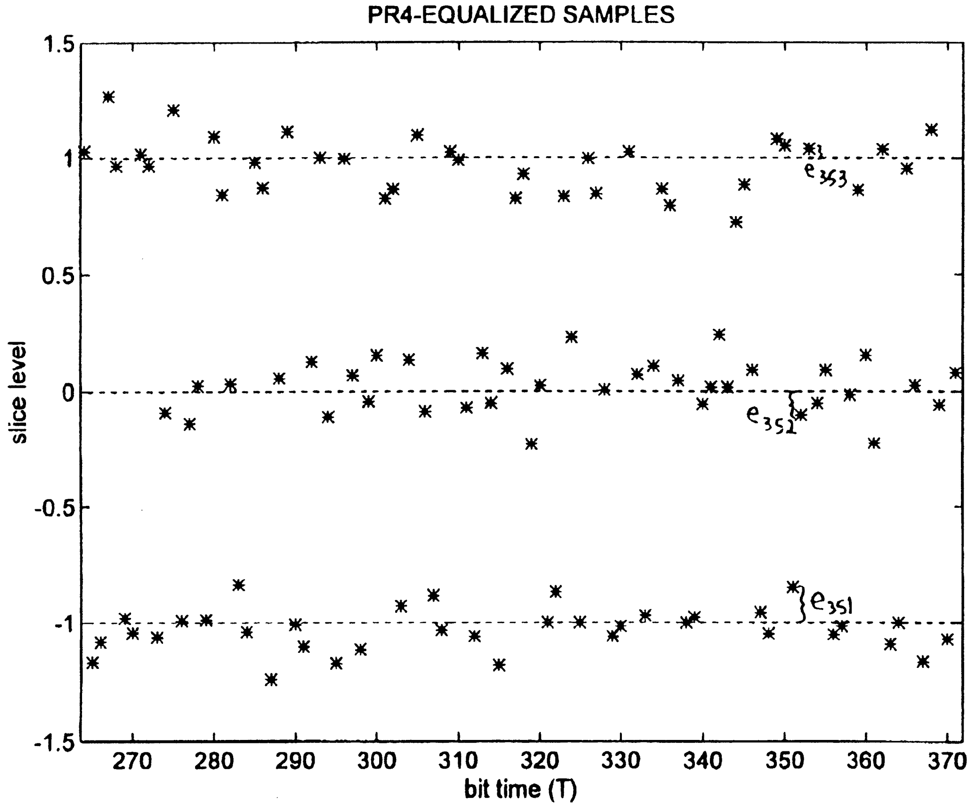
- Purpose: Optimize or "Train" various R/W channel parameters during the manufacturing process to obtain optimum BER performance with the head/media population encountered.
- Optimization is performed by minimizing the Mean Square Error (MSE) metric, which results in the best PRML channel performance for the given set of settings.
- R/W parameters that are trained include:
  - ☐ **MR bias**
  - ☐ **W/R element micropositioning (microjog)**
  - ☐ **Channel input attenuator**
  - ☐ **Write current**
  - ☐ **Write precompensation**
  - ☐ **Tap 4 of the FIR**
  - ☐ **Continuous time filter boost and cutoff**
  - ☐ **FIR taps**

An Example of PR4-Equalized Samples



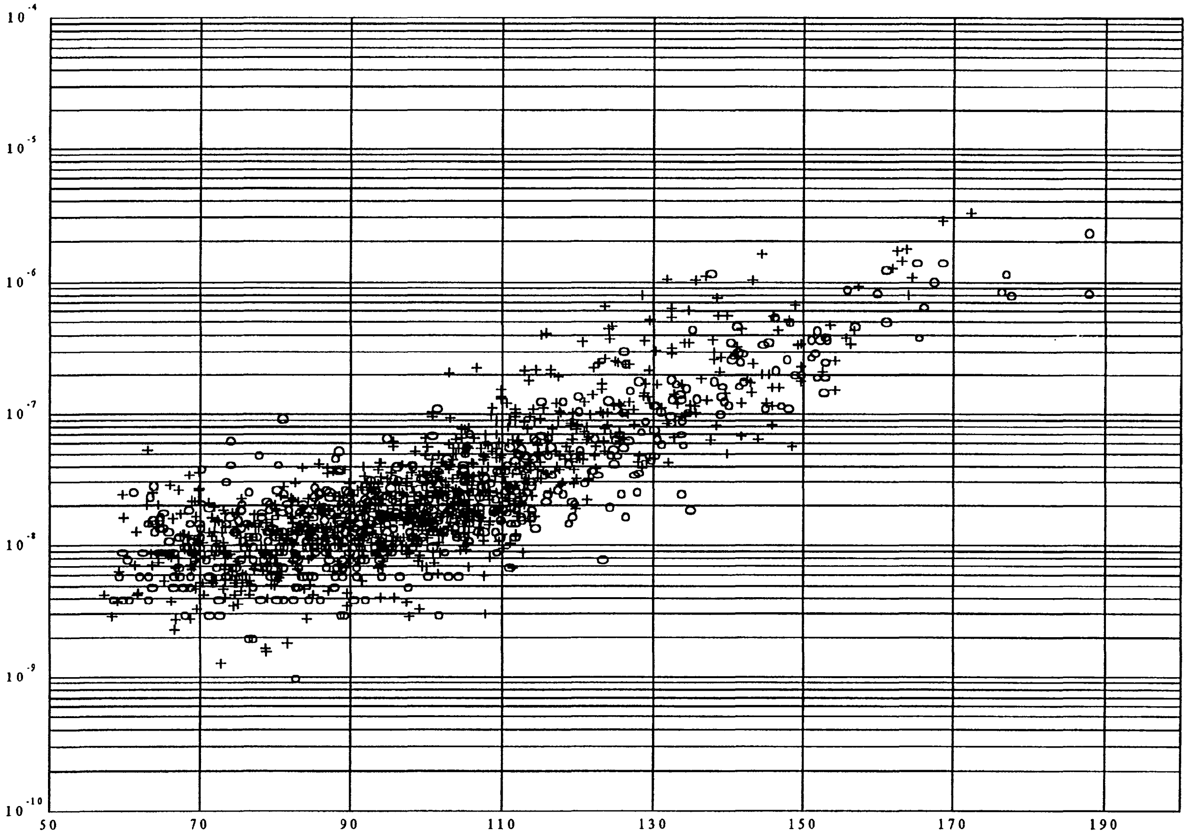
MSE Function Used in Jackhammer

MSE FUNCTION

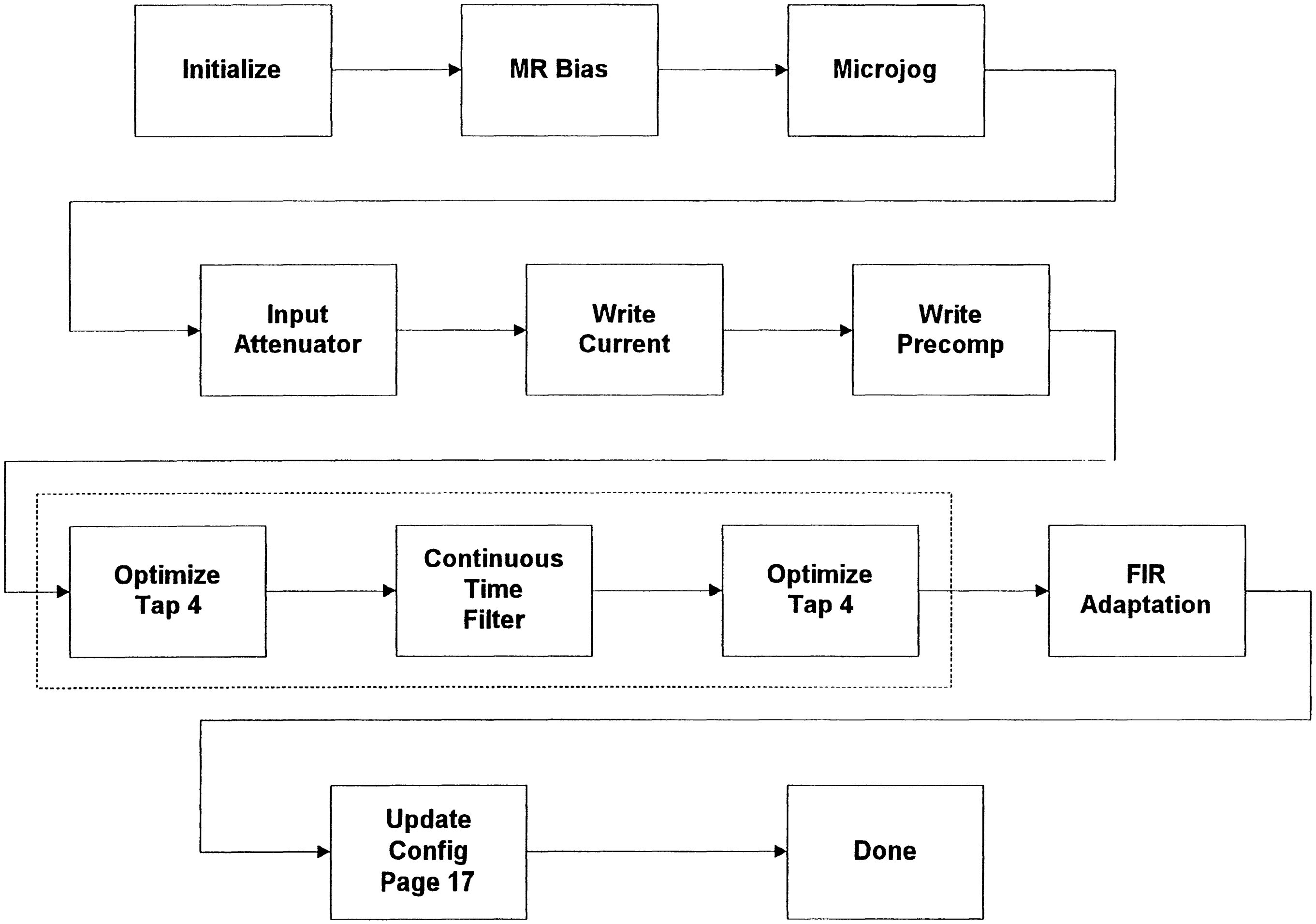


$$MSE = (0.444) * \frac{1}{32} * \sum_{n=1}^{Nbits} e_n^2$$

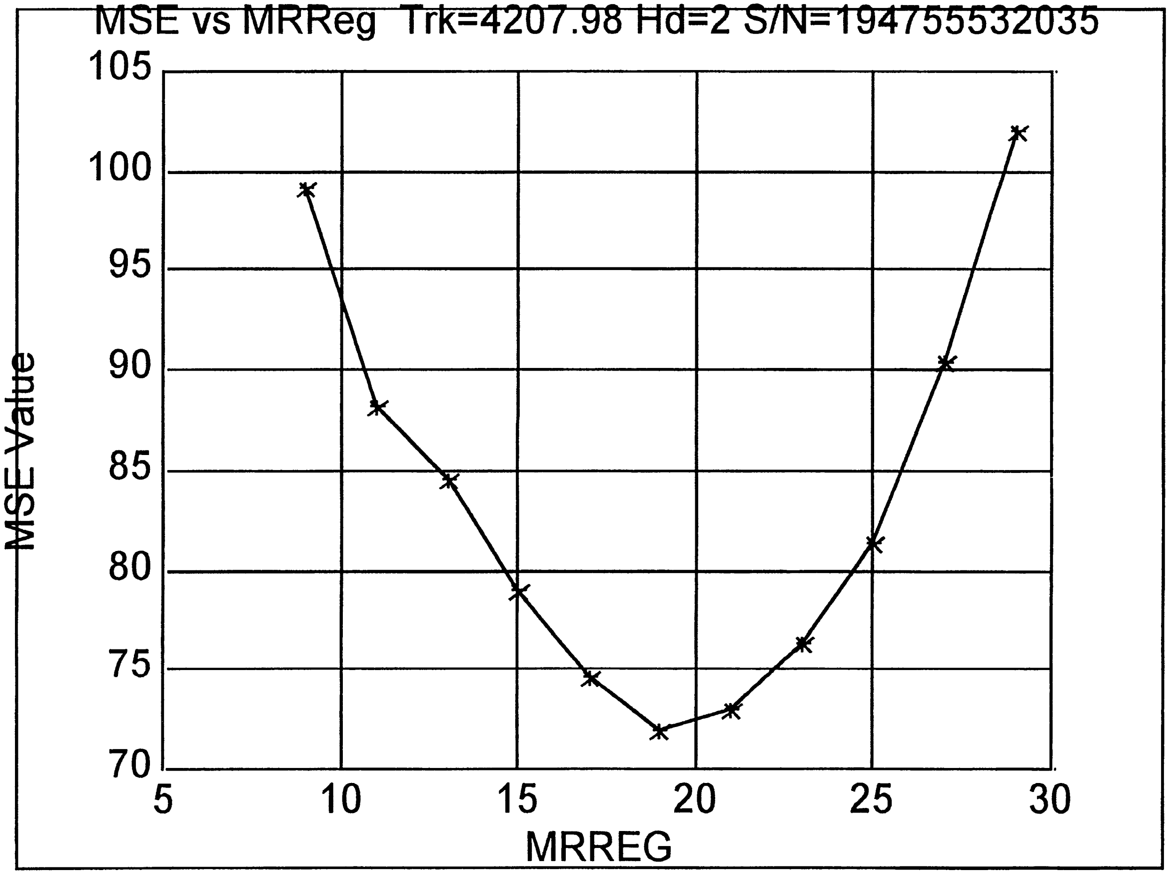
BER vs MSE



UPT/SelfScan Channel Optimization

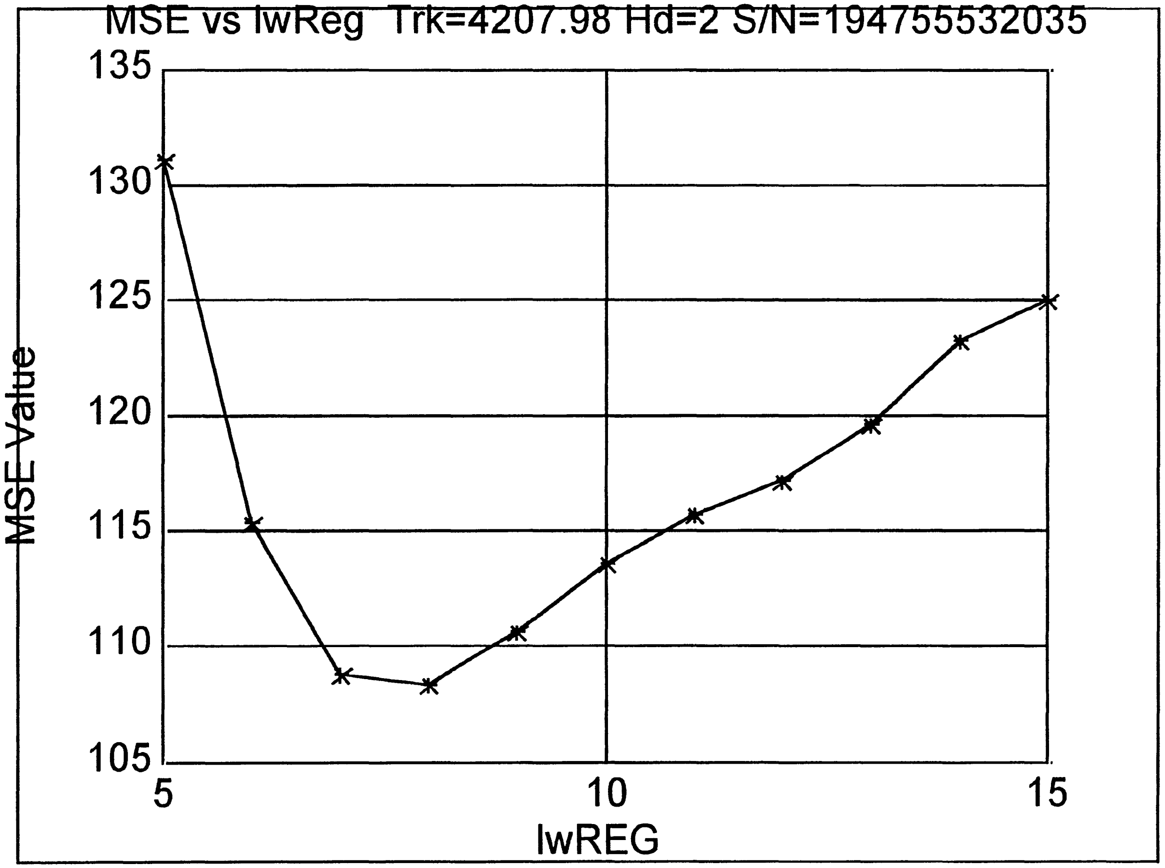


Channel Optimization:
Example of MR Bias Training



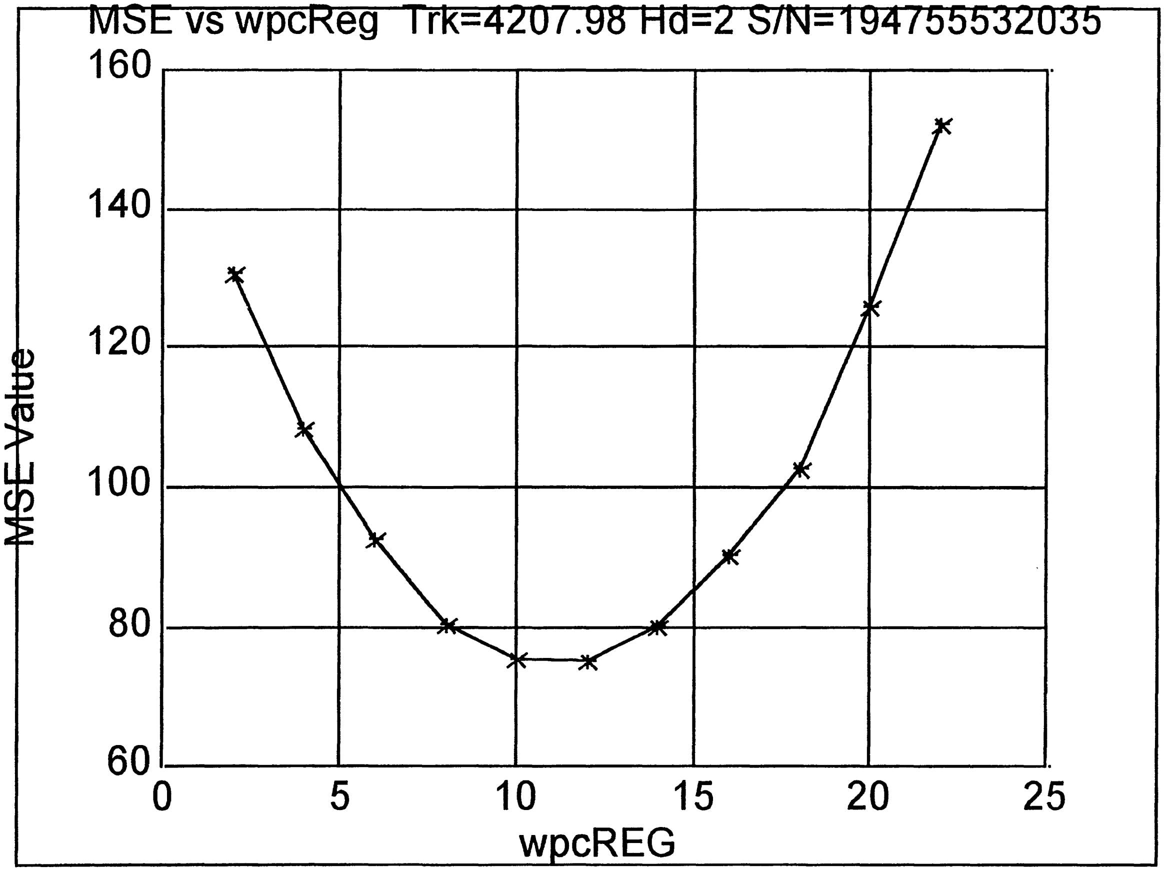
Channel Optimization:

Example of Write Current Training



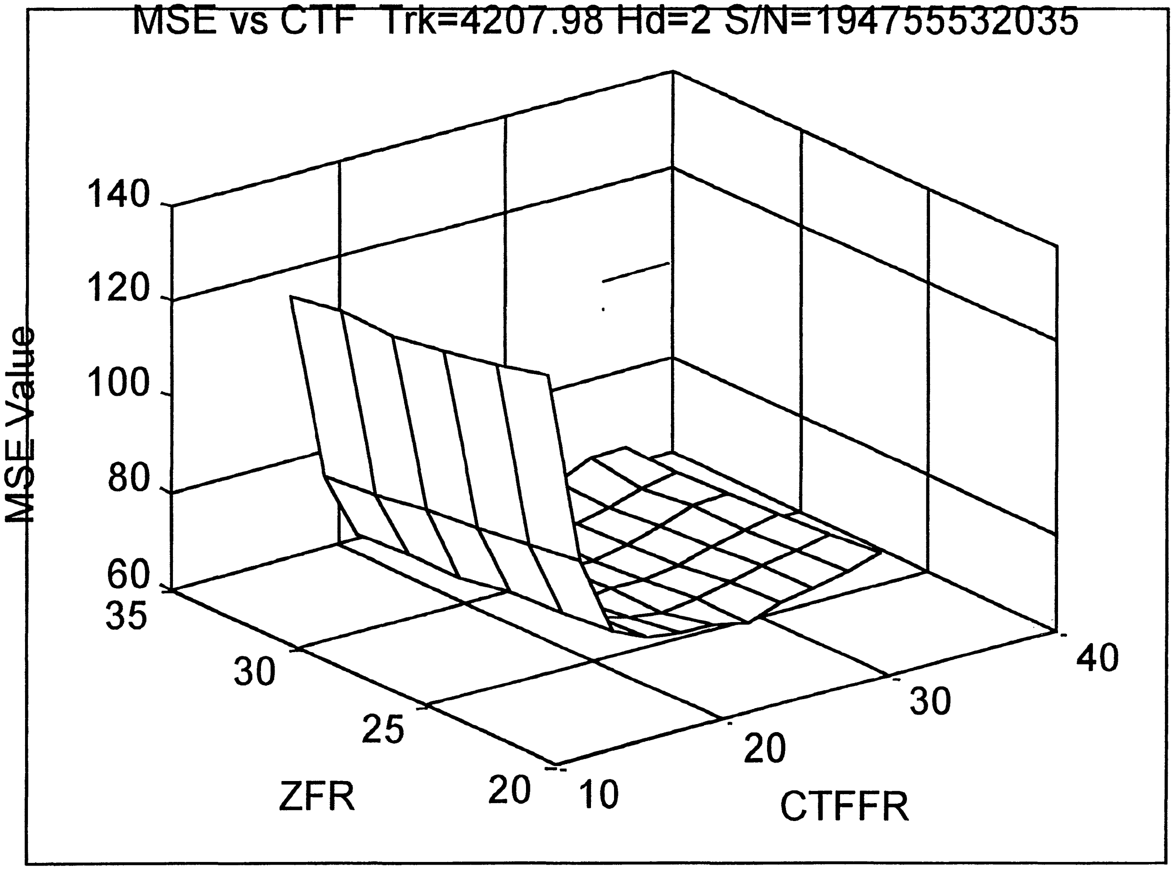
Channel Optimization:

Example of Write Precomp Training



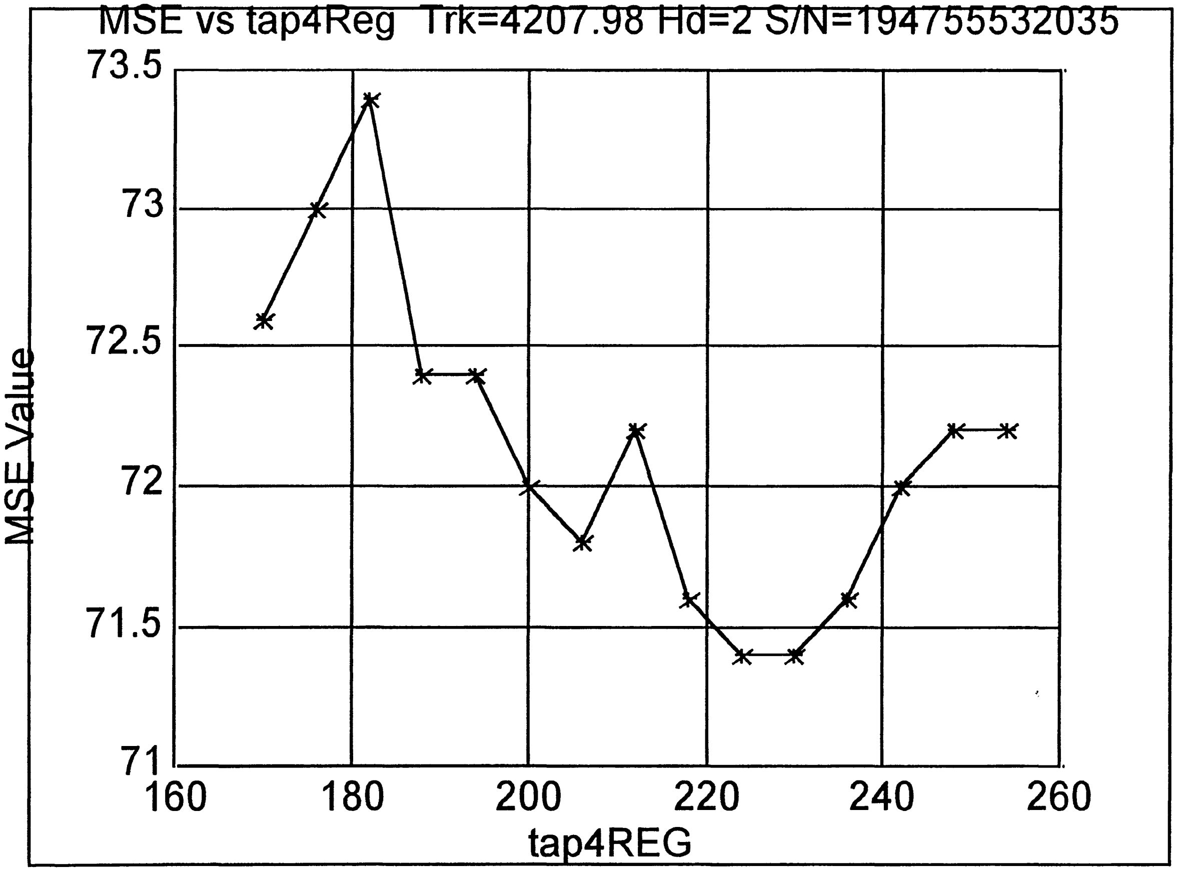
Channel Optimization:

Example of Continuous Time Filter Training

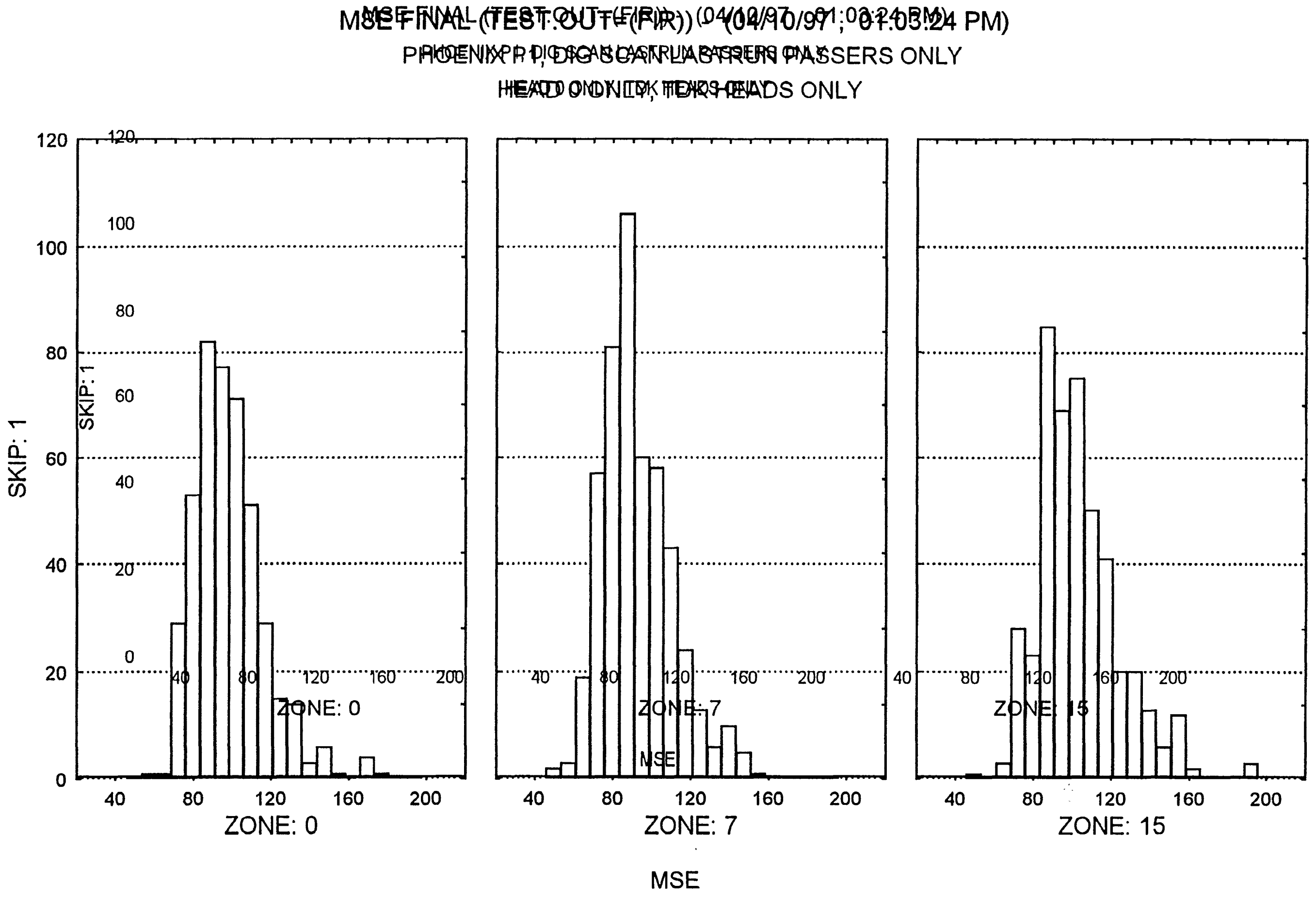


Channel Optimization:

Example of FIR Tap4 Training



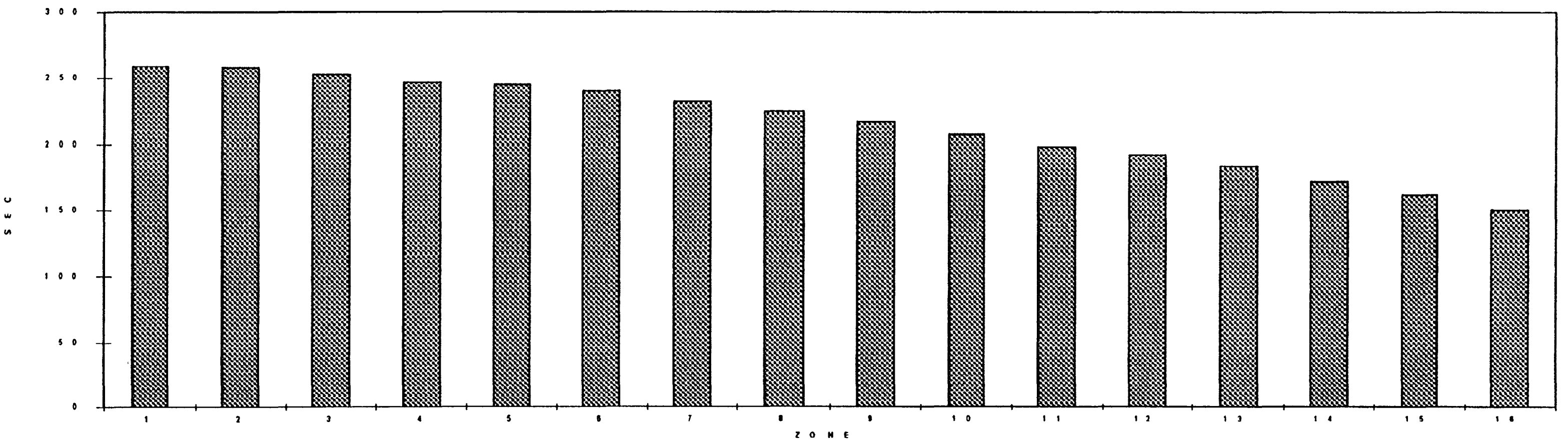
MSE After Channel Optimization in P1

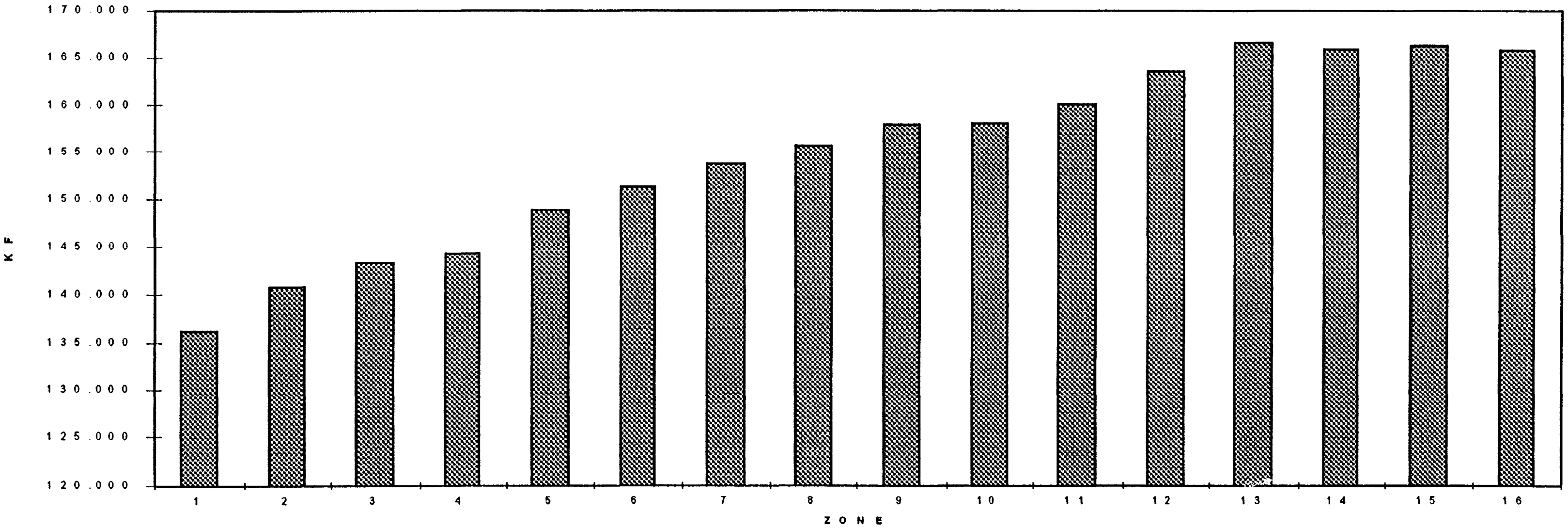


Track Layout

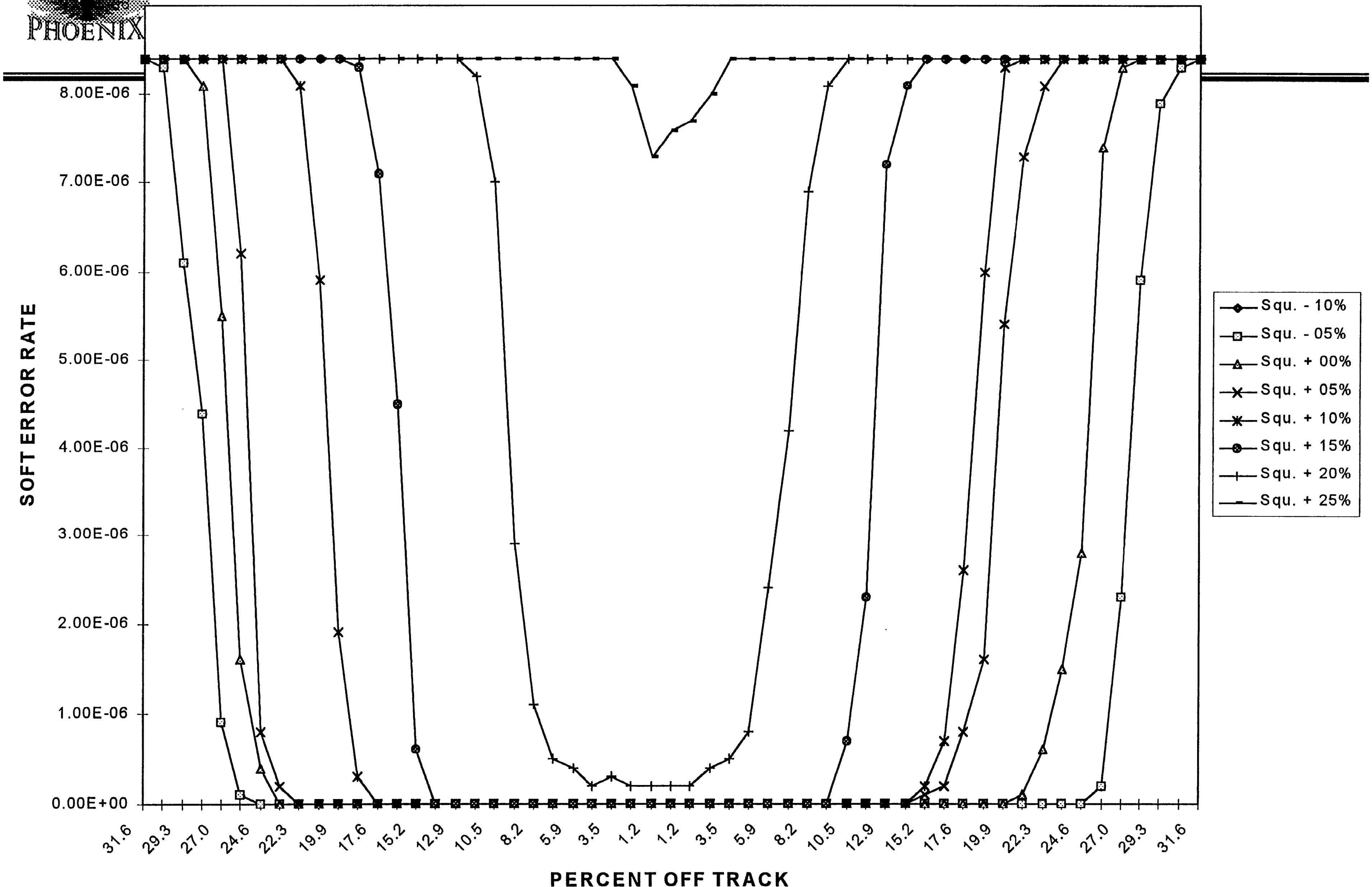
```
====================================================
Project:    C:\PHOENIX\ITF\P2_6\BCV_6C.csv    (Summary file)
Date:       8/30/97
Revision:    1
ITF version: 1.7
====================================================
```

	Zone	Innr		Max		Sec		TSTU	Slack	Track	% Eff	% Eff	Surface
Zone	Rad ID	Cyl#	Cyls	KFCI	ReadClk	Size	Spt	Byts	Byts	Capcy	NoWdg	w/Wdg	Capacity
0	1.7477	-1	536	135.99	179.2	512	258	40	8	132096	75.19	85.32	70803456
1	1.685	532	533	140.42	178.4	512	257	72	92	131584	75.23	85.37	70134272
2	1.6226	1062	530	142.73	174.6154	512	252	51	3	129024	75.37	85.52	68382720
3	1.5606	1589	527	144.47	170	512	246	50	10	125952	75.57	85.75	66376704
4	1.4989	2114	525	148.49	167.8049	512	243	32	4	124416	75.63	85.81	65318400
5	1.4373	2637	523	150.48	163.0769	512	236	0	166	120832	75.58	85.76	63195136
6	1.376	3158	521	153.15	158.8889	512	230	18	2	117760	75.6	85.78	61352960
7	1.315	3677	519	155.52	154.1935	512	225	0	0	115200	76.21	86.47	59788800
8	1.2542	4194	517	157.79	149.2063	512	216	68	4	110592	75.6	85.79	57176064
9	1.1934	4710	516	158.13	142.2951	512	205	24	414	104960	75.24	85.37	54159360
10	1.1329	5225	515	159.44	136.1905	512	196	0	233	100352	75.16	85.28	51681280
11	1.0724	5739	514	163.01	131.8033	512	190	0	0	97280	75.28	85.42	50001920
12	1.0119	6253	514	166.99	127.4074	512	183	0	211	93696	75.01	85.12	48159744
13	0.9513	6768	515	165.9	119	512	171	16	2	87552	75.04	85.15	45089280
14	0.8906	7284	516	166.93	112.0988	512	162	51	3	82944	75.47	85.64	42799104
15	0.8298	7801	517	165.6	103.6066	512	150	29	1	76800	75.61	85.79	39705600

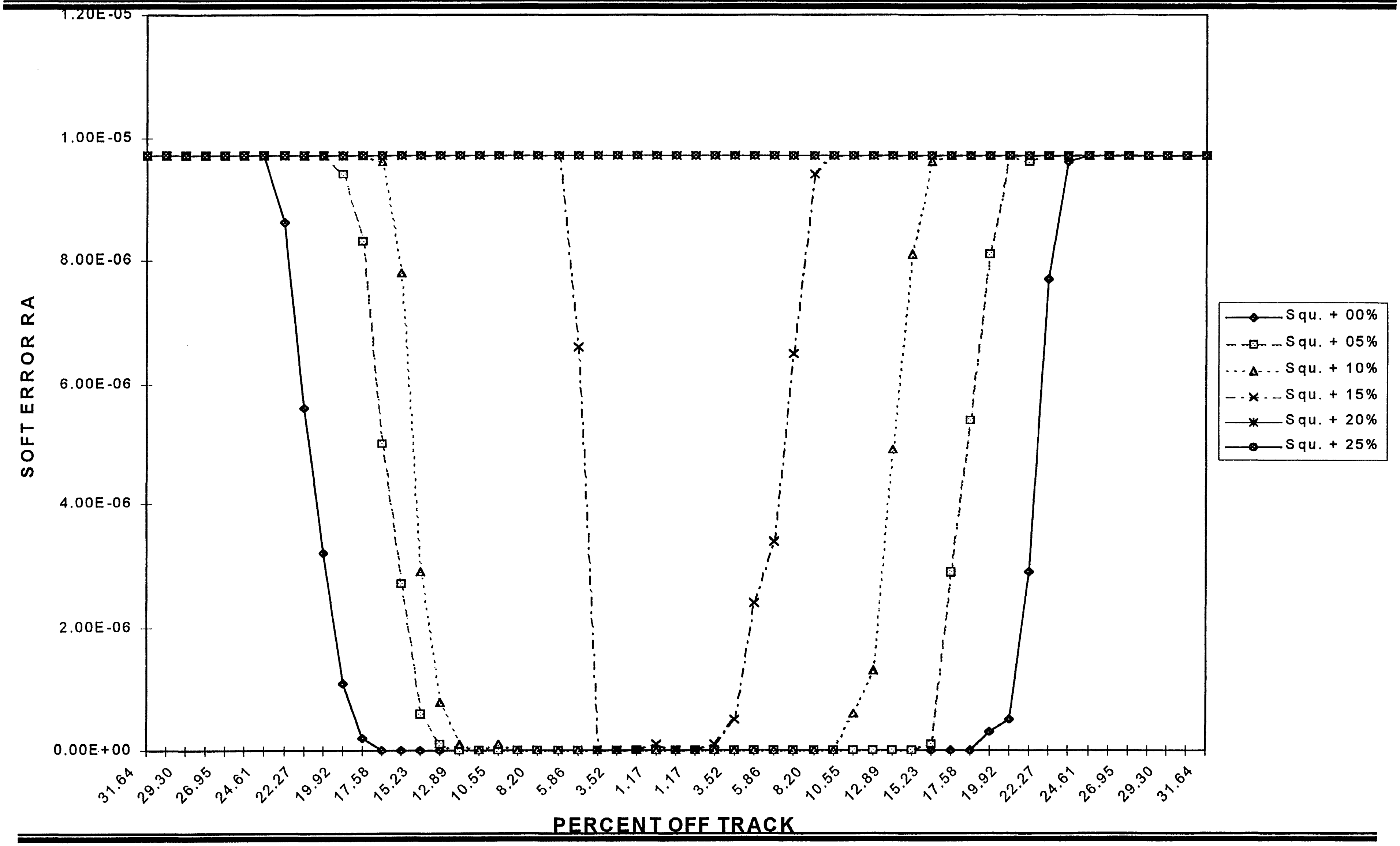

300
250
200
150
100
50
0
SEC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
ZONE


170.000
165.000
160.000
155.000
150.000
145.000
140.000
135.000
130.000
125.000
120.000
KF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
ZONE

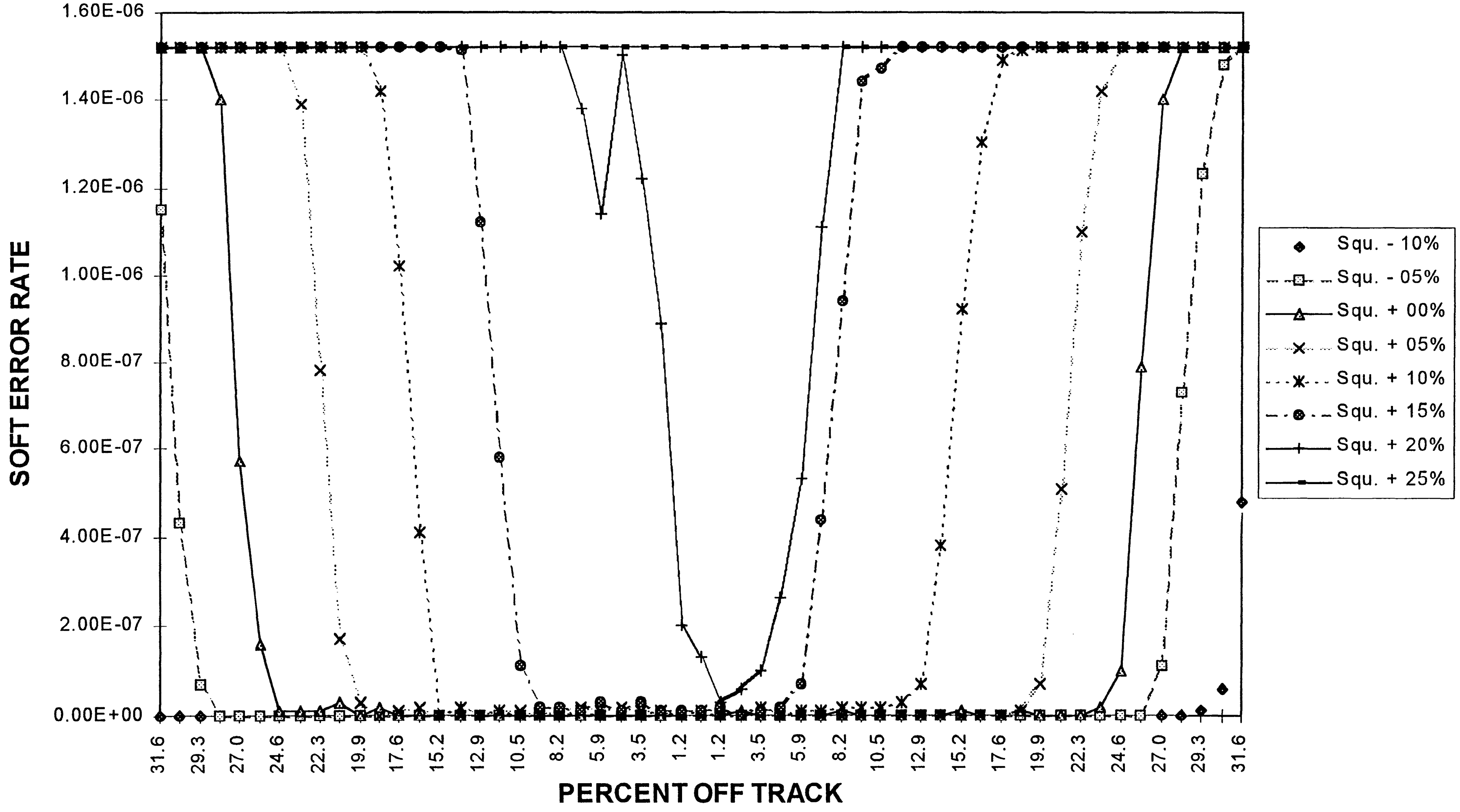
OTC AND SQUEEZE (ZONE 0)



OTC AND SQUEEZE (ZONE 7)

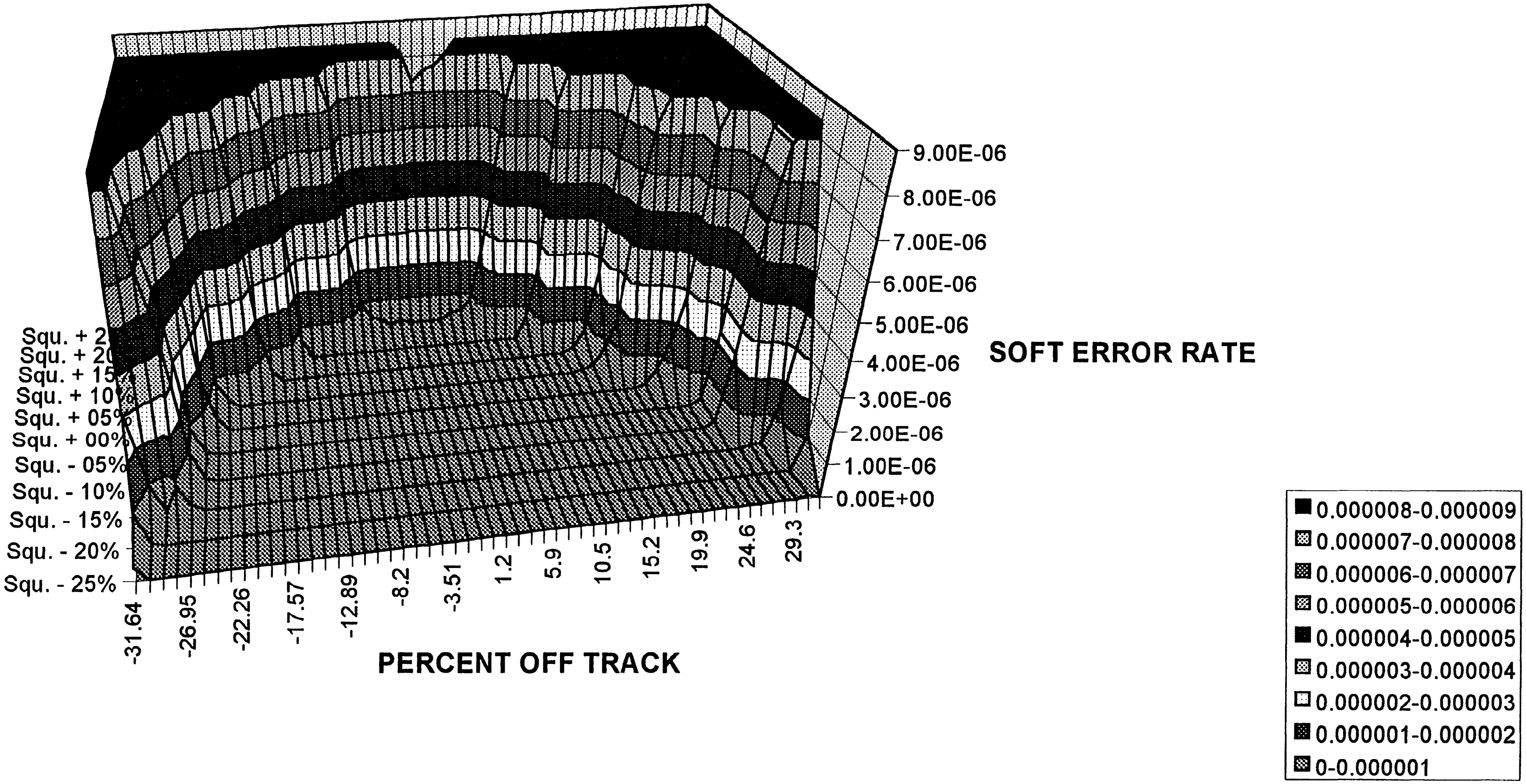


OTC AND SQUEEZE (ZONE 15)

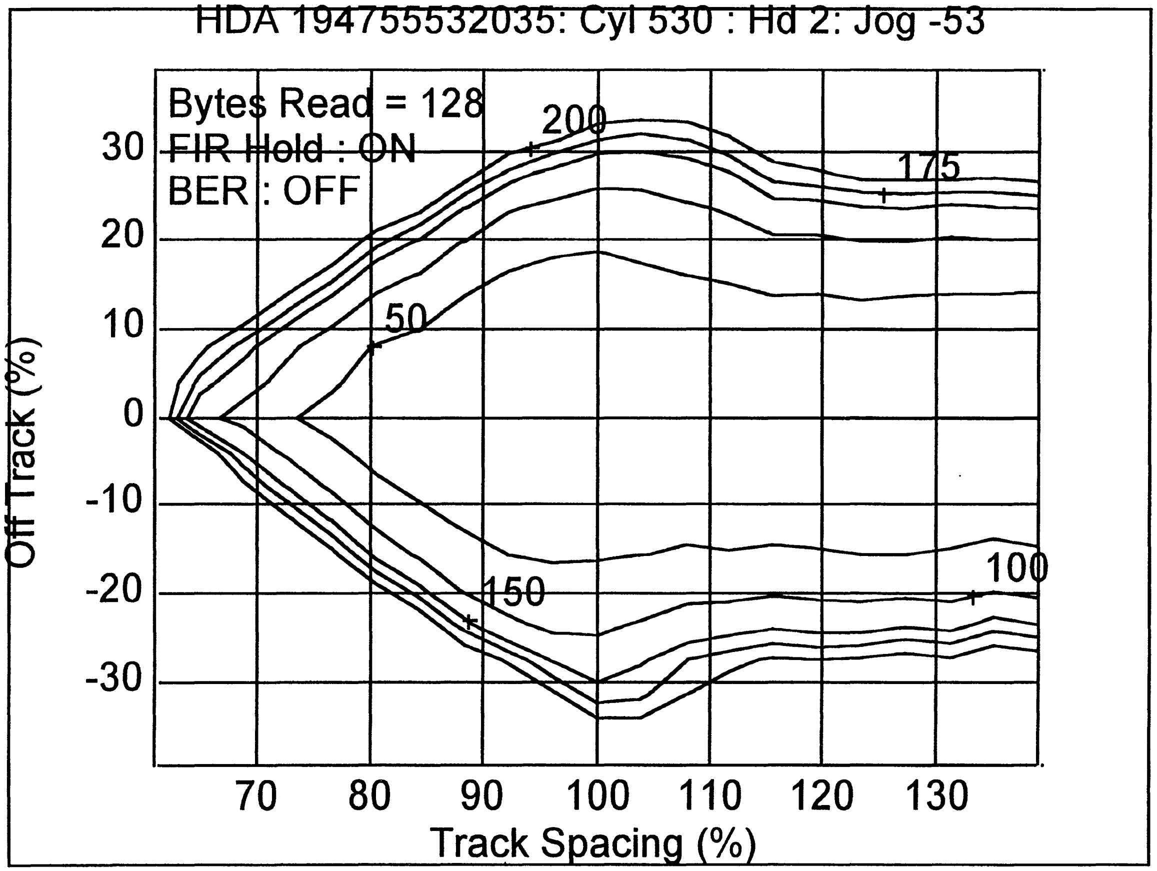


OTC AND SQUEEZE

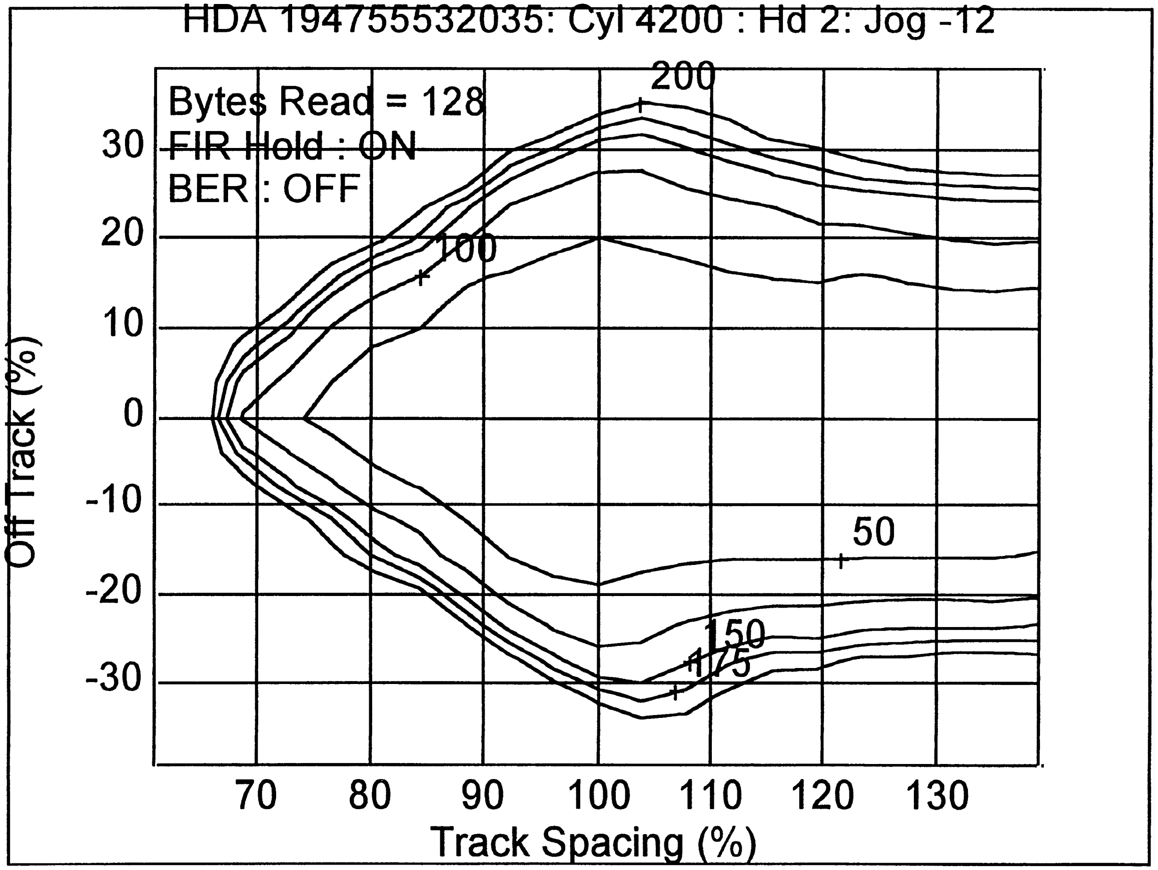
TDK, FUJI, ZONE 0



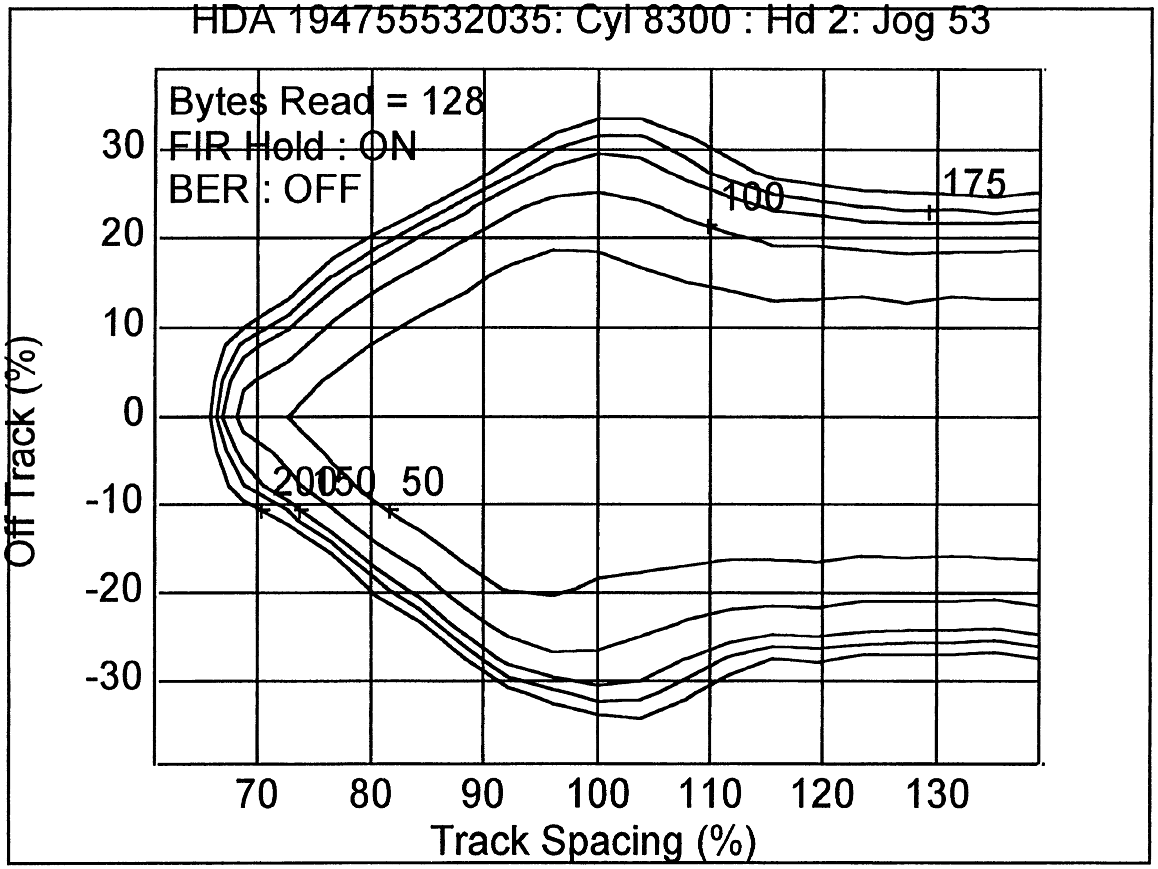
Channel Performance: 747 Plots, OD



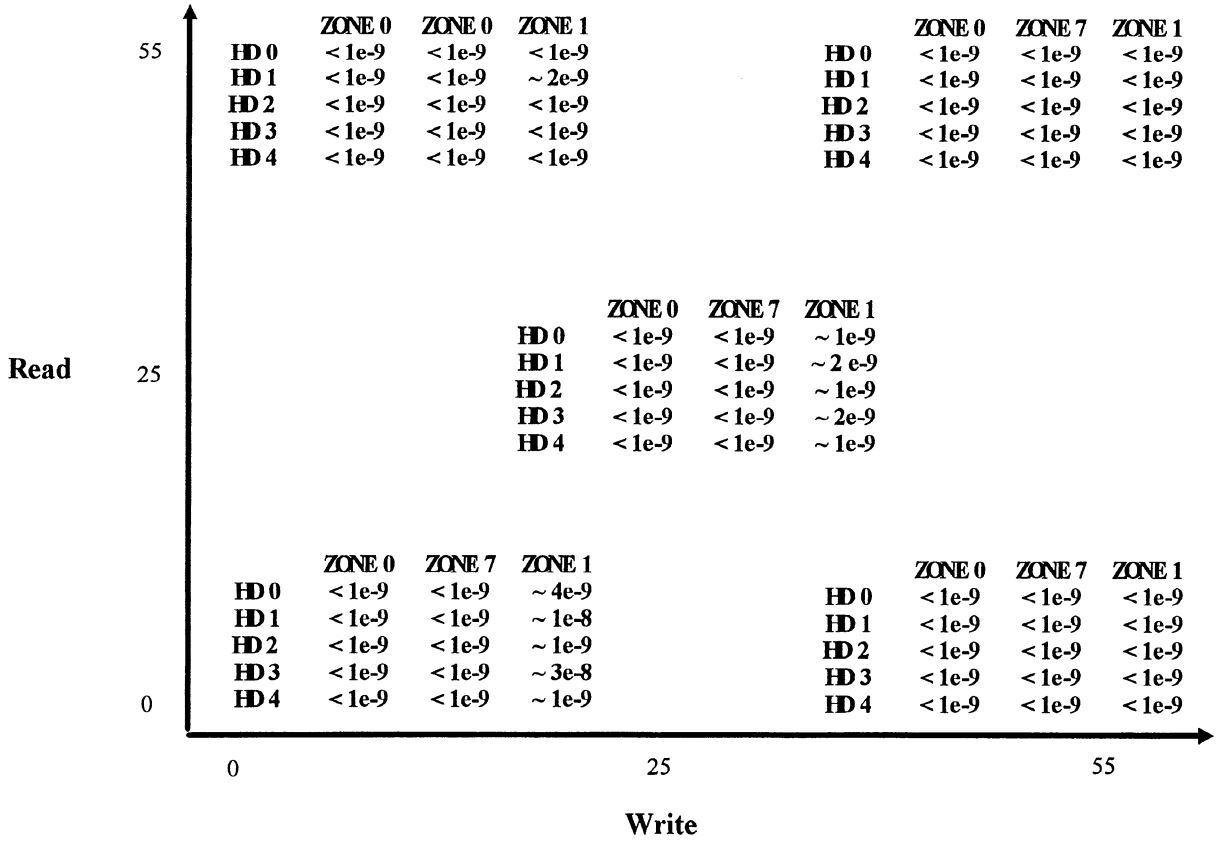
Channel Performance: 747 Plots MD



Channel Performance: 747 Plots ID



BER vs w/r Temperature



	ZONE 0	ZONE 0	ZONE 1
HD 0	< 1e-9	< 1e-9	< 1e-9
HD 1	< 1e-9	< 1e-9	~ 2e-9
HD 2	< 1e-9	< 1e-9	< 1e-9
HD 3	< 1e-9	< 1e-9	< 1e-9
HD 4	< 1e-9	< 1e-9	< 1e-9

	ZONE 0	ZONE 7	ZONE 1
HD 0	< 1e-9	< 1e-9	< 1e-9
HD 1	< 1e-9	< 1e-9	< 1e-9
HD 2	< 1e-9	< 1e-9	< 1e-9
HD 3	< 1e-9	< 1e-9	< 1e-9
HD 4	< 1e-9	< 1e-9	< 1e-9

	ZONE 0	ZONE 7	ZONE 1
HD 0	< 1e-9	< 1e-9	~ 1e-9
HD 1	< 1e-9	< 1e-9	~ 2 e-9
HD 2	< 1e-9	< 1e-9	~ 1e-9
HD 3	< 1e-9	< 1e-9	~ 2e-9
HD 4	< 1e-9	< 1e-9	~ 1e-9

	ZONE 0	ZONE 7	ZONE 1
HD 0	< 1e-9	< 1e-9	~ 4e-9
HD 1	< 1e-9	< 1e-9	~ 1e-8
HD 2	< 1e-9	< 1e-9	~ 1e-9
HD 3	< 1e-9	< 1e-9	~ 3e-8
HD 4	< 1e-9	< 1e-9	~ 1e-9

	ZONE 0	ZONE 7	ZONE 1
HD 0	< 1e-9	< 1e-9	< 1e-9
HD 1	< 1e-9	< 1e-9	< 1e-9
HD 2	< 1e-9	< 1e-9	< 1e-9
HD 3	< 1e-9	< 1e-9	< 1e-9
HD 4	< 1e-9	< 1e-9	< 1e-9

PHOENIX

New Product Training
November 1997

Firmware Section

Hardware Overview-Processor

- NEC High-performance 32 bit RISC (33 mhz) processor.
- 48K on-chip ROM: Flash, or masked.
- 2K on-chip RAM.
- 8K serial EEROM (NVR).

Hardware Overview-Asic

PHOENIX

- Highly Integrated control ASIC.
- SCSI block with automated WCS control.
- ID-LESS disk sequencer (formatter) with data integrity protection
- Buffer List manager block.
- Servo block.
- ECC block.
- Motor control block.

Firmware Features

- Full featured SCSI-2 implementation.
- Minimal firmware intervention for SCSI sequences.
- Diskware and flash ROM upgrades via SCSI write buffer command.
- Tagged command queuing with command reordering.
- Virtual Queue
- Serpentine Format*
- Auto Hot Sectors*
- Data Integrity Block*
- Zero Latency writes and reads *
- Write and read caching.
- SMART and SCAM support.
- Configurable table-driven error recovery procedures.
- Highly configurable for customer specific implementations.
- Code for manufacturing self-test separate from functional firmware.

* New feature on Phoenix

FIRMWARE ORGANIZATION

- 48K ROM CODE
- 8K SERIAL EEPROM
- 512K DRAM
- DISKWARE

48K ROM CODE

- Power on initialization
- Motor control and Servo firmware
- Basic SCSI protocol routines
  - SCAM
  - Selection, reselection, message and limited SCSI command set
  - Write buffer command allows diskware to be written to disk
  - Firmware to start drive and load diskware to DRAM
- Time critical code

8 K SERIAL EEPROM

◆ NON-VOLATILE STORAGE FOR DRIVE INFORMATION

- Serial Number
- Inquiry Data
- Mode Page Data
- Default Channel Parameters
- Default Id-less@ Parameters for system cylinders
- Drive Geometry Information
- SCAM code
- Motor control code
- etc.

512K DRAM

- SYSTEM INFORMATION
  - Processor Stack
  - Firmware variables
  - Virtual Queue tables
  - Real Queue tables
  - Buffer Manager List
  - Defect list
  - etc.
- DISKWARE
- DISK CACHE BUFFER

Phoenix / Viking firmware commonality

	% change from Viking
Kernel	5%
File system	5%
Command processing	5%
Read/Write control	70%
Servo	25%
Read/Write Callback	25%
Motor Control	100%
Tagged Command Queuing	10%
Defect management	30%
Write caching/coalescing	40%
Read caching	50%
ECC	10%
Diagnostic (super) command	10%
Self-scan (manufacturing/test)	30%

DISKWARE

- Diskware downloader: "throw-away" code used only during download.
- Resides in file system on system cylinders.
- Loaded during drive power up initialization and remains in DRAM while the drive is powered on.
- Contains remainder of drive firmware.
- Contains provisions to allow vectoring ROM routines to Diskware .

Major Firmware Blocks

- Kernel
- File system
- Command processing
- Read/Write control
- Servo
- Read/Write Callback
- Motor Control
- Tagged Command Queuing
- Defect management
- Buffer Management
- ECC
- Diagnostic (super) command
- Self-scan (manufacturing/test)
- BCM Control/Manage

Kernel and File System

- Kernel: Accepts messages and invokes tasks.

- File System: Manages system files on the disk and in the NVR.

Command Processing and Read/Write Control

- Command Dispatcher Task: Manages command dispatching and completion.
- Disk Request Handler: Invoked by software interrupt generated by Read/Write Callback. This code is the heart of the read/write control and interface data transfer control.
- Disk Monitor Task: Manages disk recovery processes and restart of disk in non-error cases.
- Queue Background Task: Queue management and reordering.
- Command processing routines: SCSI command processing.

Servo and Read/Write Callback

- Assembly (not C) code optimized for execution speed.

- Servo code operates at a non-maskable interrupt level.

- Read/write callback is "interface" between control code and servo code and is executed via subroutine call at the end of servo burst processing.

Buffer List Manager

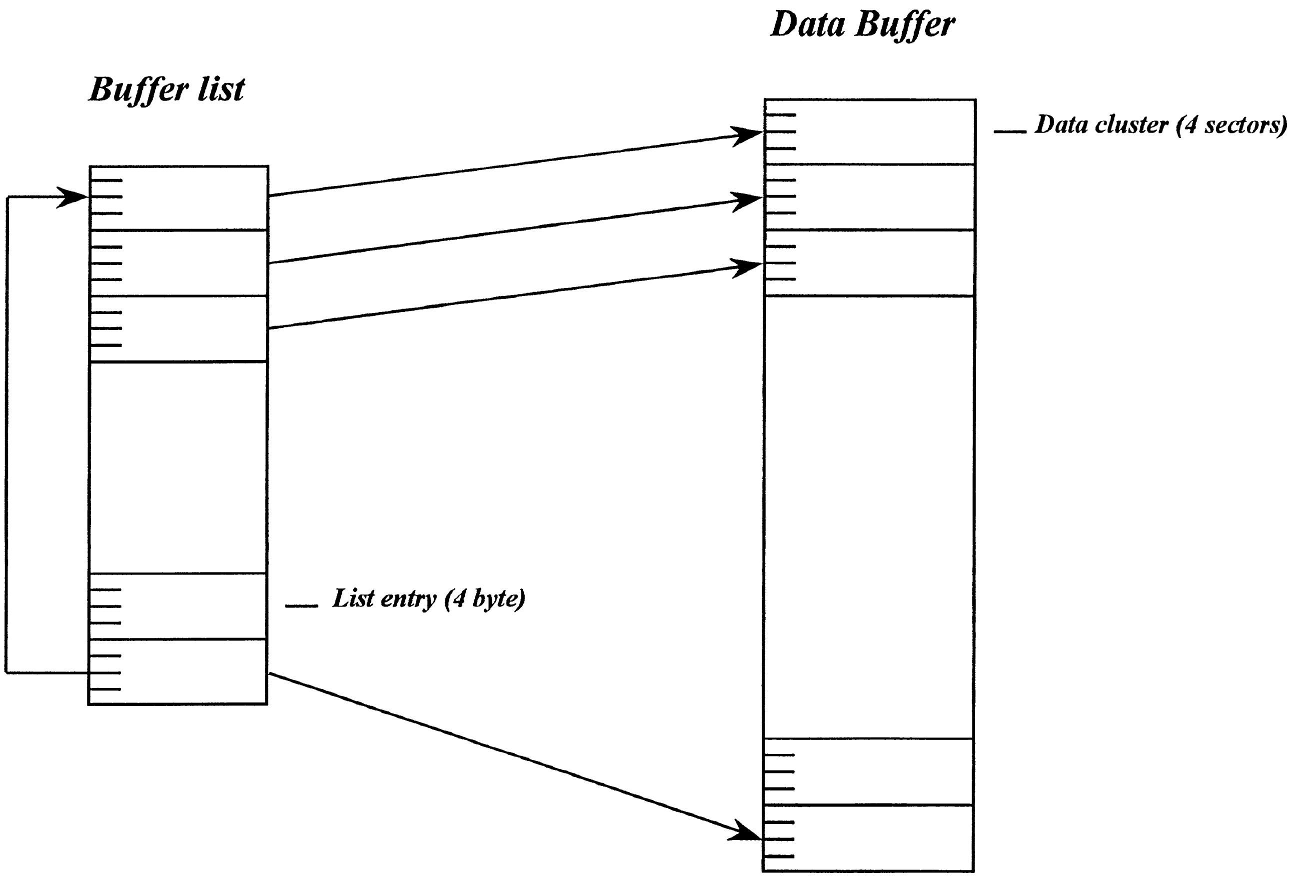
- ◆ Highly automated hardware that maximizes functionality of the Formatter with minimum firmware involvement
- ◆ Replaces lengthy Sector Descriptor table
- ◆ On the Host side, firmware does not involve during data transferring
- ◆ On the Disk side, firmware only involves on track switches
- ◆ Full features:
  - Auto Hot Sectors
  - Zero Rotational Latency
  - Scatter/Gather

The Buffer List Structure

- A circular link list that hardware uses to control data transfer within a segment buffer
- Each entry is associated to the control of a cluster of four sectors
- A list entry is a 4-byte entry that contains
  - Dual function Offset that calculates pointer to buffer in DRAM also pointer to next list entry
  - Status of transfer of each sector in the cluster (opcodes)
  - Interrupt, ECC error flags, etc.
- The length of list is programmable to cover multiple tracks

The Buffer List Data Structure

- The buffer list and data buffer



The Buffer List Data Structure

- The buffer list entry format

	BIT 7				*BIT 0*
0:	*u*	*ECC0*	*Opcode 0(1:0)*	*Offset (3:0)*	
1:	*u*	*ECC1*	*Opcode 1(1:0)*	*Offset (7:4)*	
2:	*u*	*ECC2*	*Opcode 2(1:0)*	*Offset (10:8)*	
3:	*INTR*	*ECC3*	*Opcode 3(1:0)*	*Sectors unused*	*Opcode Delta*

Buffer List Address = Buffer List Base Address + 4 x Offset
Buffer Address = (4 x Offset + Sector Offset).(Sector Size + DIB)

Auto Hot Sectors

- Automatically keeping track of both side of the transfer: the Host and the Disk
  - On a read, it notifies the Host block a sector is available for transfer to the Host. Also when a sector is transferred to the Host, that buffer space is available for the Disk
  - On a write, when a sector is put in the buffer by the Host, it notifies the disk block a sector is ready for writing. Also when a sector is written to the Disk, it notifies the Host block that buffer space is available
  - Old way (read example):
  - Firmware notices that a sector was read, it increments a counter on the Host side
  - Firmware latency would cause unecessary disconnects
- New way:
  - Hardware keeps track of transfer
  - Completion on the disk side are immediately posted to the Buffer List, and can be seen by the Host, and vice versa
  - Firmware is free during the transfer to reorder queue, command preprocess, house keeping, etc.

Zero Rotational Latency

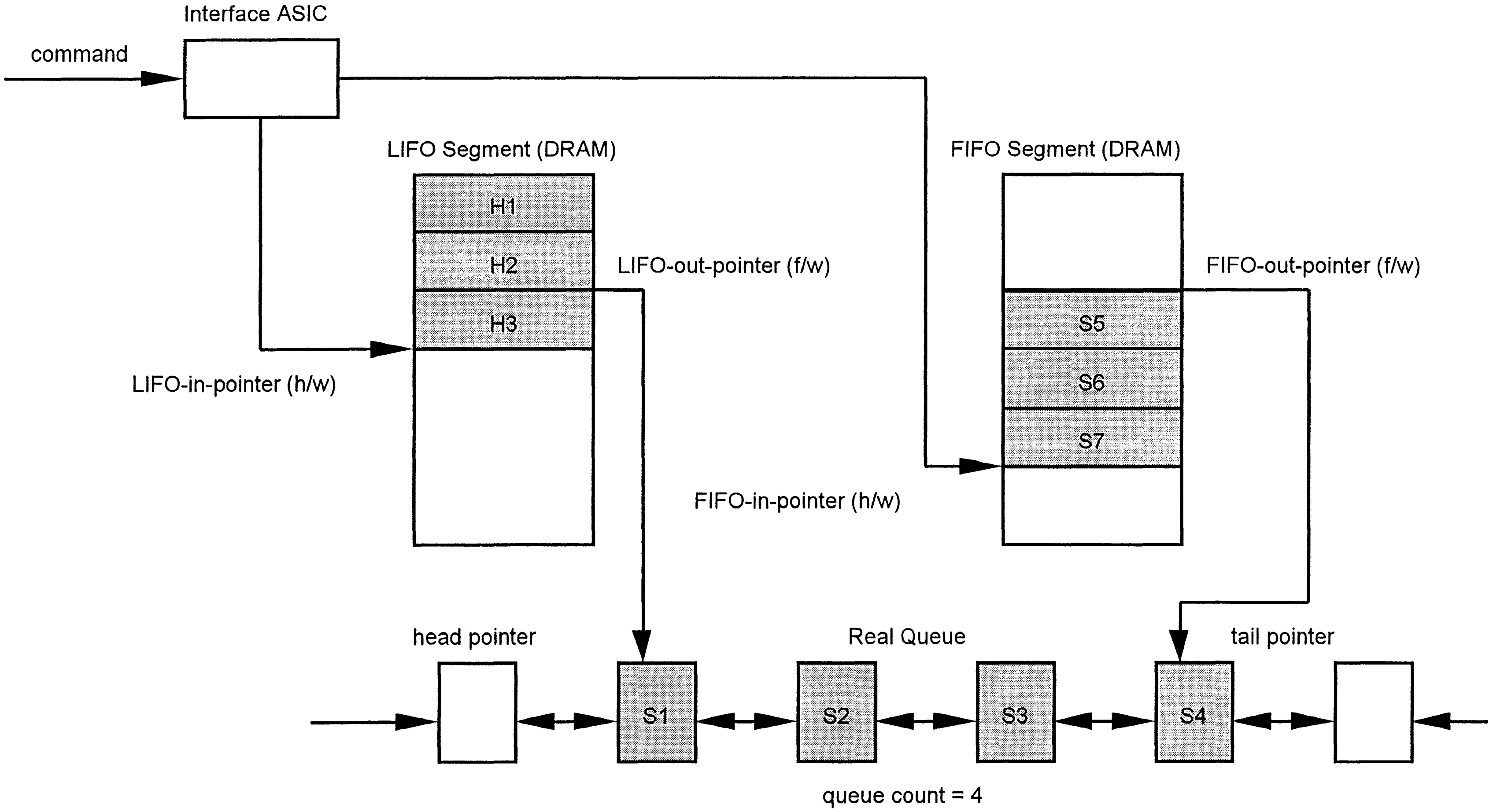
- When a head lands on track, the formatter starts the transfer on the next available sector immediately
- Old way:
  - Wait for first sector of transfer to be under the head
- New way:
  - Each sector is tracked individually, so the transfer may take place in any order
  - Apllied to both reads and writes
  - Firmware does not have to check head position, hardware automatically optimizes

Scatter/Gather

- Hardware is capable to detect and skip sectors that are not ready at any moment and then will pick up on next rev.
- Old way:
  - Formatter would loose a rev. for every skip
- New way:
  - Minimizes loosing rev.

Tagged Command Queuing

- Virtual queue structure



Benefits of the Virtual Queue

- **Unlimited Queue Depth**
  - The virtual queue keeps minimal information about the command and nexus in DRAM buffer. With the abundance of DRAM space in the drive, there is practically no limit on the number of commands we can queue in a drive. The command record arrangement and access method, which is based on pointer arithmetic, are also flexible enough that the maximum number of queued records is fully scaleable.
  - Zero Firmware Overhead
  - The interface ASIC captures all information pertaining to the command and the nexus during command reception, and stores it automatically into the command buffers. Queue record creation and insertion, which is done by firmware, is completely divorced from command reception, which is done by hardware. In this way, the bus transaction for command reception is all handled by hardware with zero firmware intervention. This results in minimal bus overhead time and highest bus performance. Queue insertion can be done at a later time after the bus transaction ends, at the firmware's convenience.

Benefits of the Virtual Queue

- SCSI Queuing Protocol Compliance
  - Dual command buffer design and hardware assists in the interface ASIC, together with the command processor firmware structure, allows head-of-queue commands to be handled semantically correctly according to SCSI specification without excessive firmware overhead.
  - Queue Related Performance Enhancements
  - By keeping a real queue in directly addressable DRAM, we are able to apply proven performance enhancing features such as background command preprocessing, rotational latency reordering, command dependency analysis, and data streaming. All these features require substantial additional information maintained on a per command basis. Queue reordering can only be efficiently done in a link list structure. By putting commands from the FIFO segment into a real queue, we apply these enhancements to a subset of commands in the drive. The size of the subset is adjustable to within reasonable limits of DRAM space and CPU processing time. The queue background process keeps the real queue as full as possible so that we can apply the enhancements to as large a subset of queued commands as possible to maximize performance.

Defect Management

- Both defective sectors and sectors associated with bad Wedges are mapped.
- Factor defects are inlined mapped across zone boundaries into an 11 cylinder sector pool at the drive i.d.
- One sector per cylinder is reserved for Grown defects.
- Grown defects are offlined mapped to nearest cylinder spare.
- Grown defects will be inlined mapped (if requested) during a SCSI format operation.

ERROR CORRECTION

- Read-Solomon Encoder/Decoder
    - 4 interleaves
    - 6 Redundancy bytes per interleave
    - 4 Cross-check bytes
    - 28 ECC bytes and 4 cross-check bytes for a total of 24 redundancy bytes per sector
- Correction capabilities
    - Hardware Single and Double burst correction 'on the fly'
    - Firmware Double/Triple burst correction 'on the fly'
    - Single burst error correction: 32 bits max (1 byte per interleave) guaranteed 25 bits
    - Double burst error correction: 64 bits max (2 bytes per interleave) guaranteed 57 bits
    - Triple burst error correction: 96 bits or (3 bytes per interleave) guaranteed 89 bit

Diagnostic and Self-Scan

- Diagnostic Super commands: Command processing code which is available in "super" mode. The super commands allow functions such as reading and writing file system and configuration files stored on the disk or in NVR, reading/writing control store memory, and executing diagnostic and drive test commands.

- Self-Scan: Code and scripts which allow the drive to perform manufacturing self test.

PHOENIX

New Product Training
November 1997

Servo Section

PHOENIX

Overview

- Specifications and Parameters
- Hardware and Software Block Diagrams
- Estimation / Control
- Seek State Transition Criteria
- Power on Calibration
- Passive Calibration
- Miscellaneous Features
- Wedge Format
- TMR
- Servo Error Handling
- Appendix

Specifications and Parameters

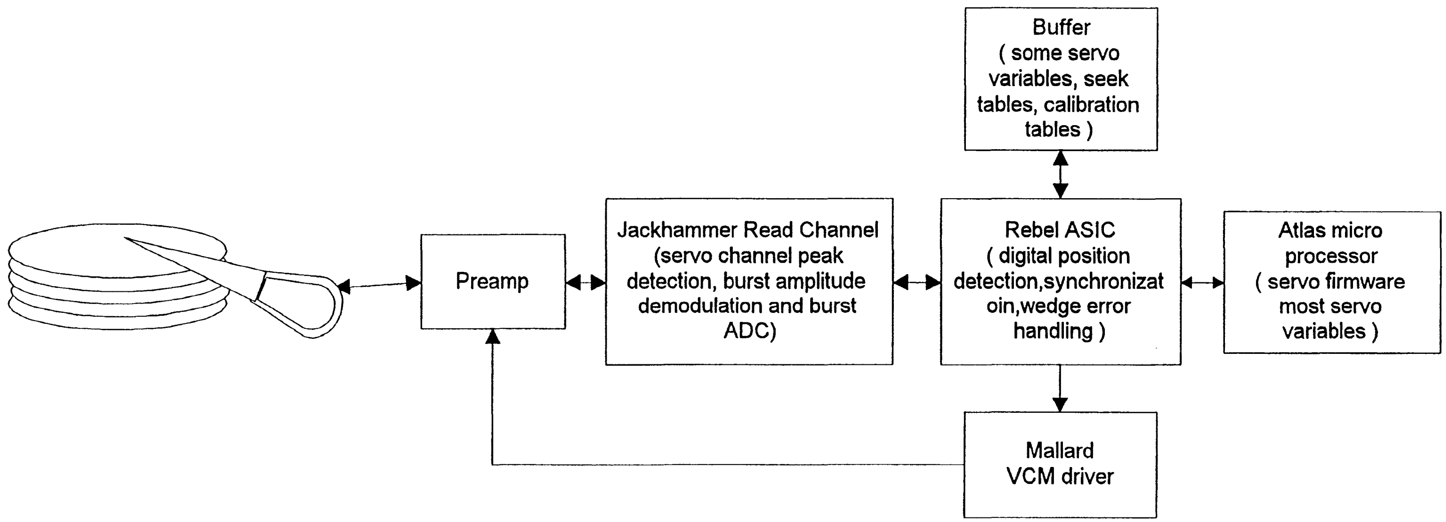
Performance Specifications:

Random read seek	<8 ms
Random write seek	<9 ms
Data delay at head switch	<1.5 ms
Data delay at cylinder switch	<2.0 ms
TPI	~8500
1/3 stroke bang-bang time	~6.0 ms

Servo Parameters:

control delay	12 usec
ISR Time	25 usec
Bandwidth	800 Hz
Phase margin	30 Degrees
Gain Margin	6 dB
Sample Rate	10800 Hz
number of wedges	90
max velocity	141 svoTk/CI (38 m/s)

Hardware Block Diagram



Buffer
(some servo variables, seek tables, calibration tables)

Preamp

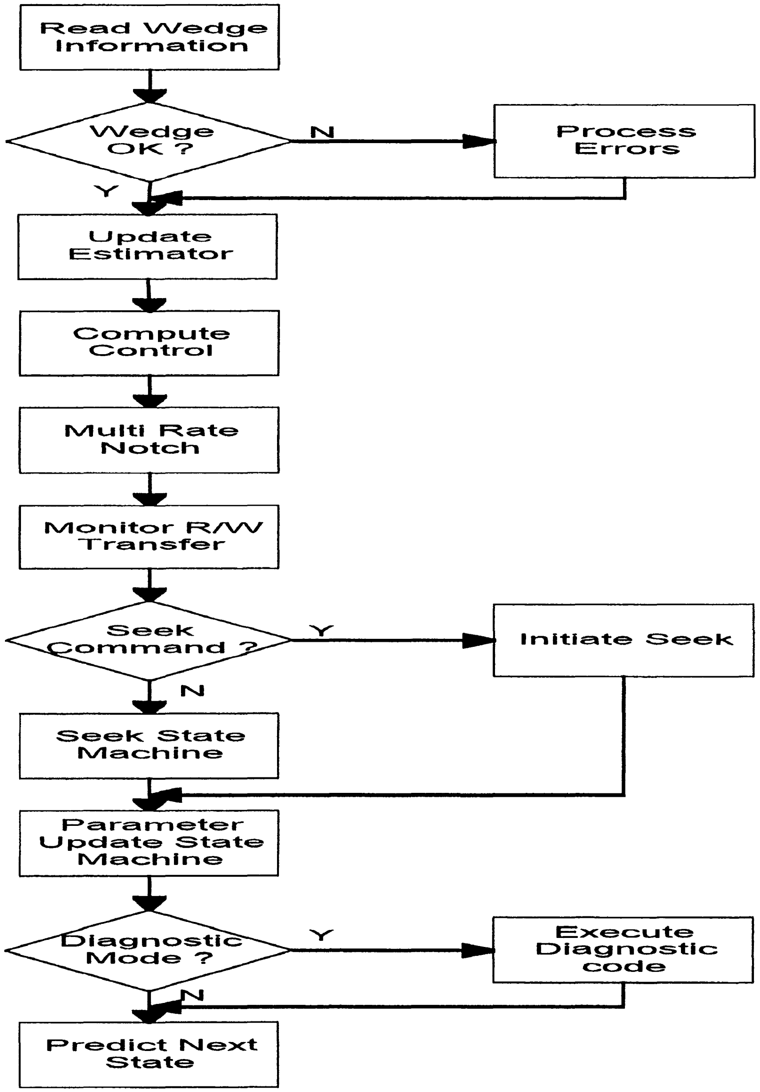
Jackhammer Read Channel
(servo channel peak detection, burst amplitude demodulation and burst ADC)

Rebel ASIC
(digital position detection,synchronizat oin,wedge error handling)

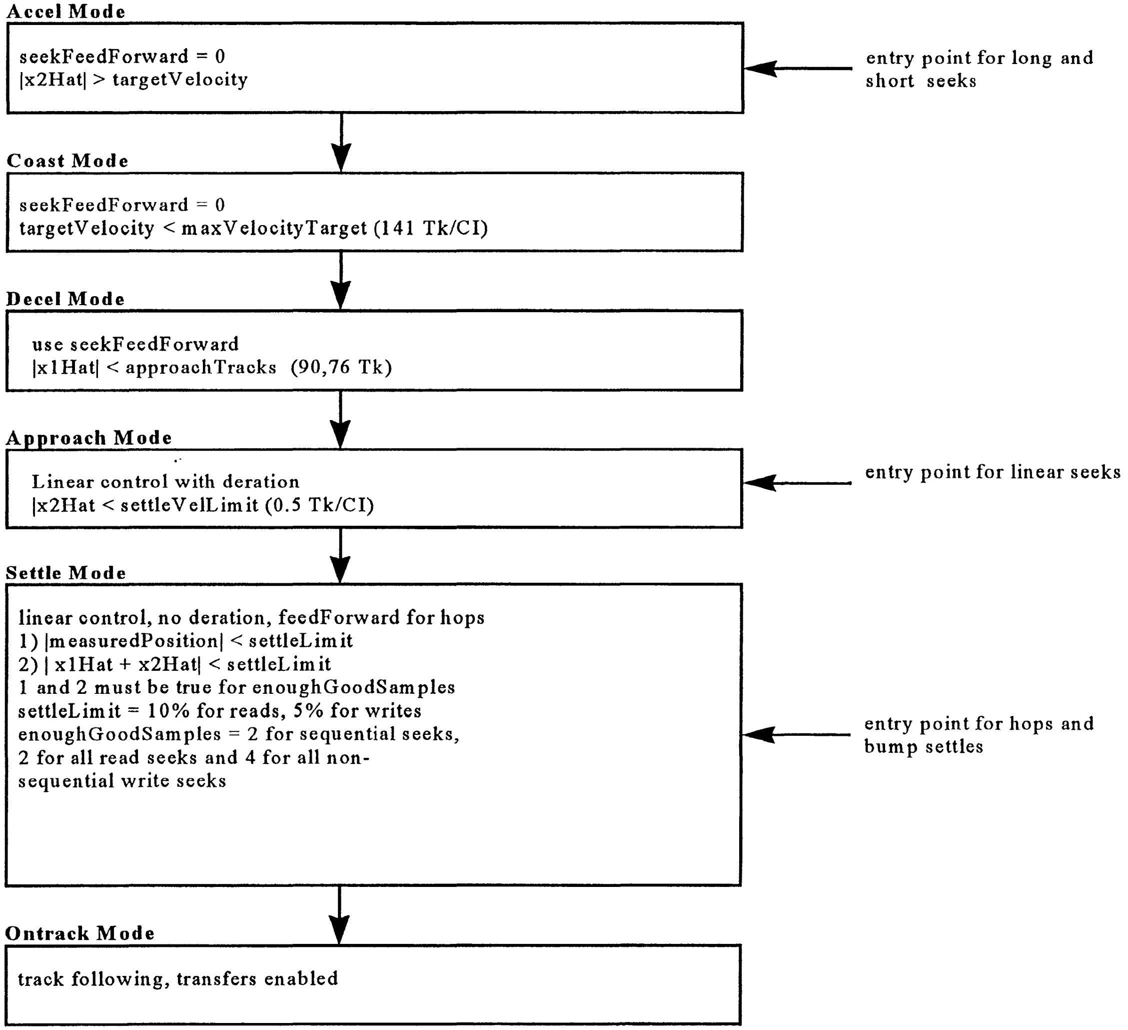
Atlas micro processor
(servo firmware most servo variables)

Mallard
VCM driver

Software Block Diagram



Seek State Transitions



Accel Mode

seekFeedForward = 0
|x2Hat| > targetVelocity

entry point for long and short seeks

Coast Mode

seekFeedForward = 0
targetVelocity < maxVelocityTarget (141 Tk/CI)

Decel Mode

use seekFeedForward
|x1Hat| < approachTracks (90,76 Tk)

Approach Mode

Linear control with deration
|x2Hat < settleVelLimit (0.5 Tk/CI)

entry point for linear seeks

Settle Mode

linear control, no deration, feedForward for hops
1) |measuredPosition| < settleLimit
2) | x1Hat + x2Hat| < settleLimit
1 and 2 must be true for enoughGoodSamples
settleLimit = 10% for reads, 5% for writes
enoughGoodSamples = 2 for sequential seeks, 2 for all read seeks and 4 for all non-sequential write seeks

entry point for hops and bump settles

Ontrack Mode

track following, transfers enabled

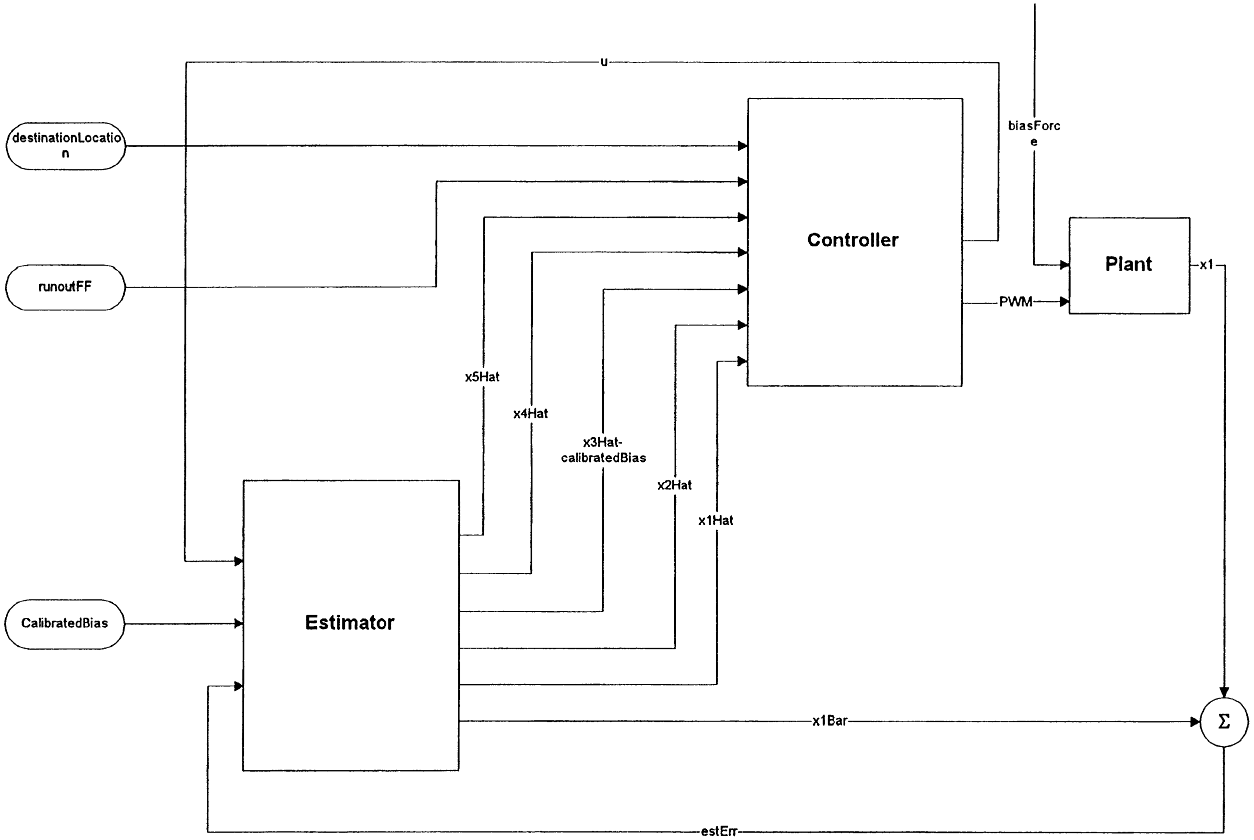
Control Features

- 6th order digital notch filter
- anticipate function for smooth switch from accel to decel
- derive feedforward from velocity table
- velocity table scale modification
- velocity gain is derated with velocity
- digital slew rate limiting
- compensation for bias hystereses
- seek feedforward for sequential seeks
- 1st, 2nd, and 3rd spindle harmonic RRO correction

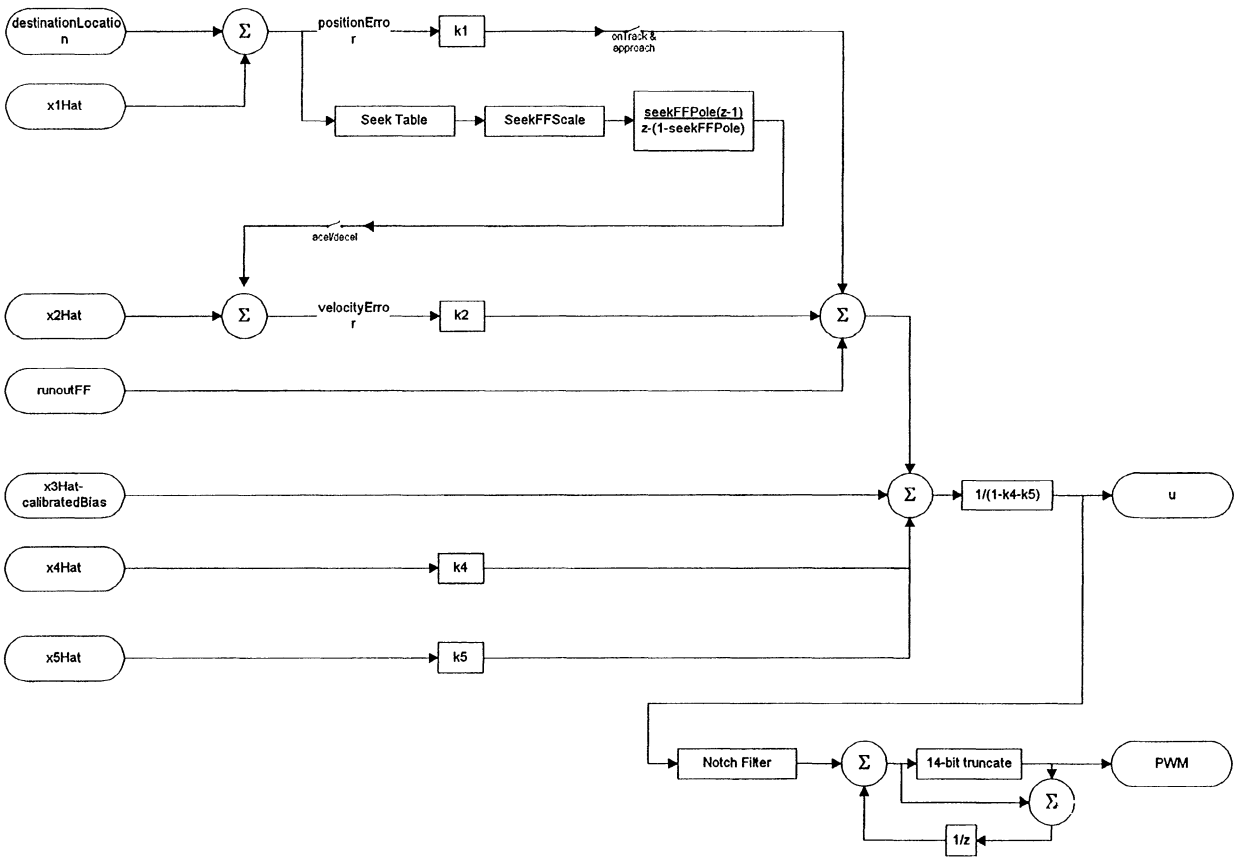
Estimation/Control

- **5 state current estimator**
  - **position**
  - **velocity**
  - **bias**
  - **current**
  - **last command**
- **4 control gains**
  - **position error (k1)**
  - **velocity error (k2)**
  - **current (k4)**
  - **last command (k5)**

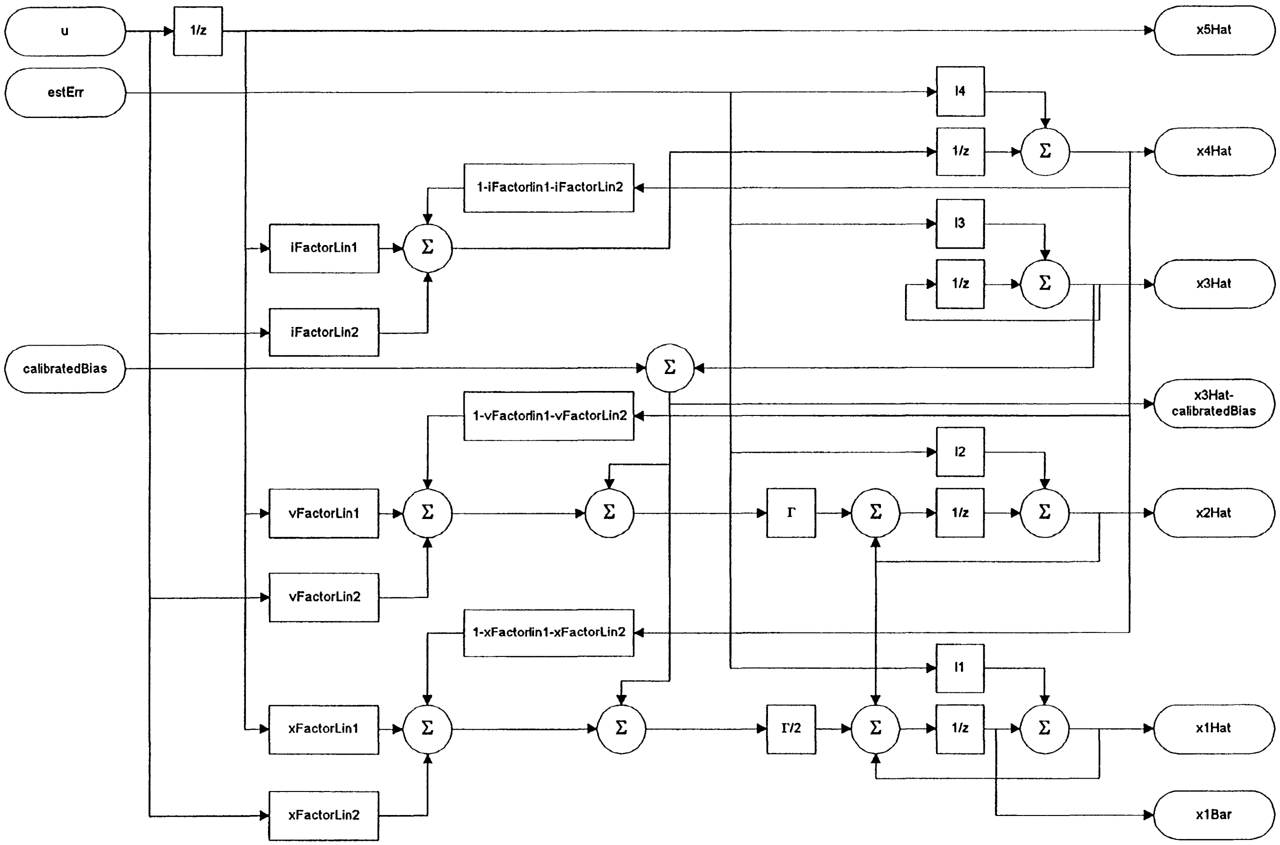
Estimation/Control



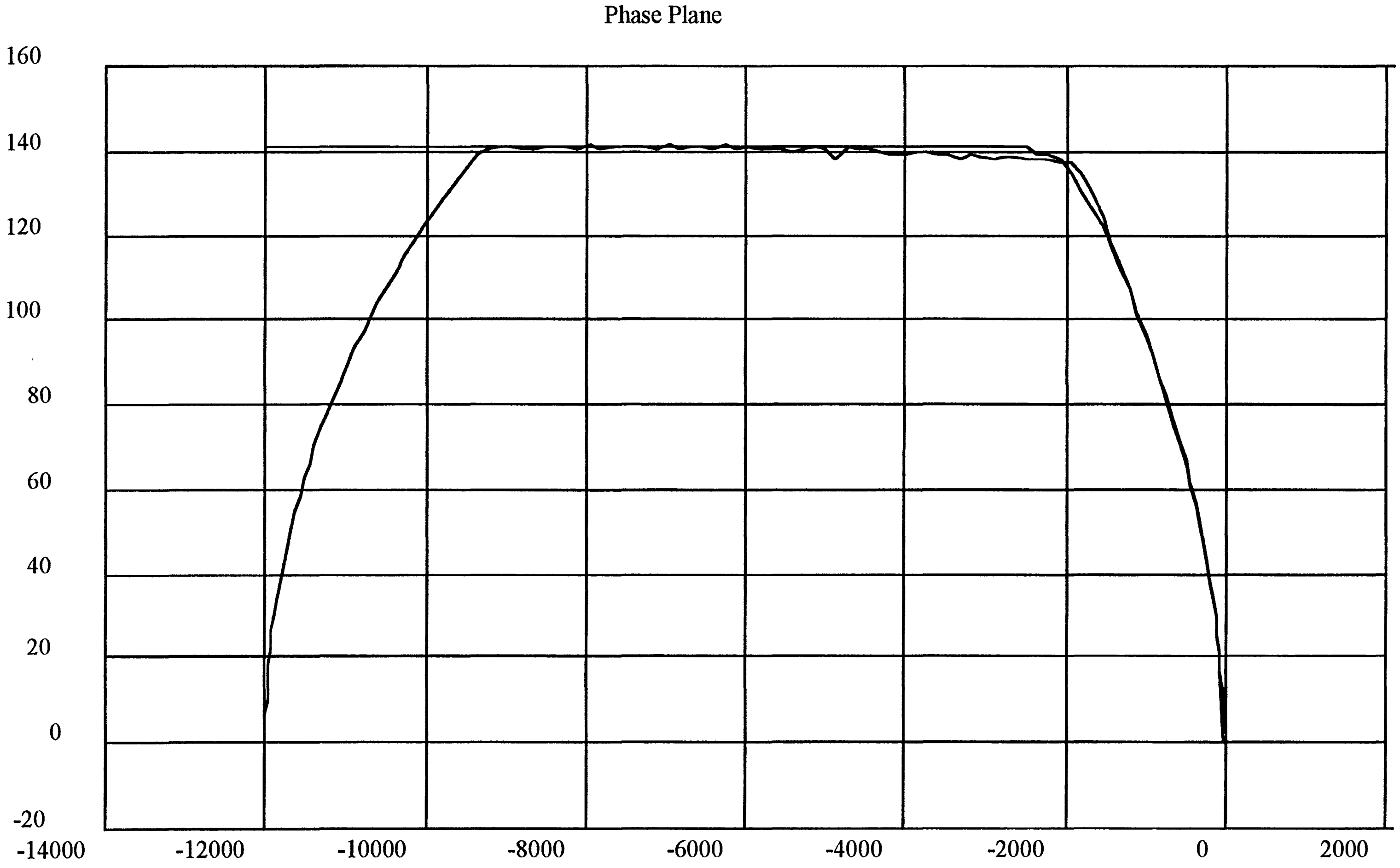
Controller


destinationLocation
x1Hat
Σ
positionError
k1
onTrack & approach
Seek Table
SeekFFScale
seekFFPole(z-1)
z-(1-seekFFPole)
acel/decel
x2Hat
Σ
velocityError
k2
Σ
runoutFF
x3Hat-calibratedBias
Σ
1/(1-k4-k5)
u
x4Hat
k4
x5Hat
k5
Notch Filter
Σ
14-bit truncate
PWM
Σ
1/z

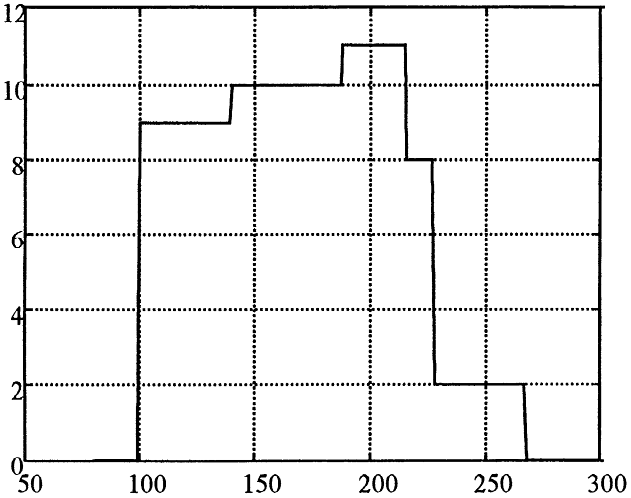
Estimator

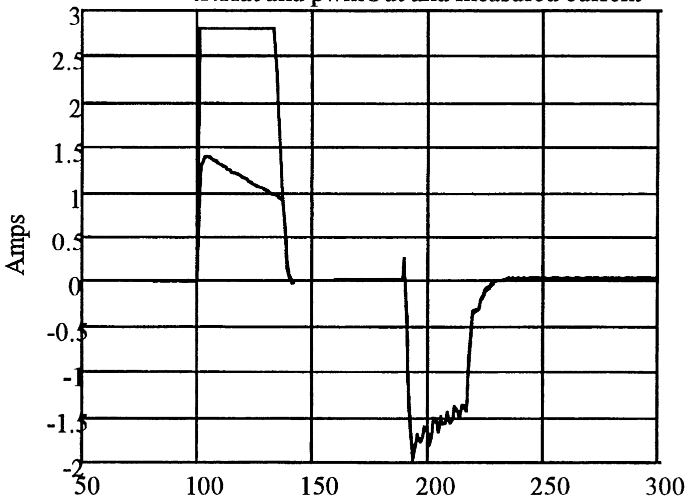

u
1/z
x5Hat
estErr
l4
1/z
Σ
x4Hat
1-iFactorlin1-iFactorLin2
l3
iFactorLin1
Σ
1/z
Σ
x3Hat
iFactorLin2
calibratedBias
Σ
x3Hat-calibratedBias
1-vFactorlin1-vFactorLin2
l2
vFactorLin1
Σ
Σ
Γ
Σ
1/z
Σ
x2Hat
vFactorLin2
1-xFactorlin1-xFactorLin2
l1
xFactorLin1
Σ
Σ
Γ/2
Σ
1/z
Σ
x1Hat
xFactorLin2
x1Bar

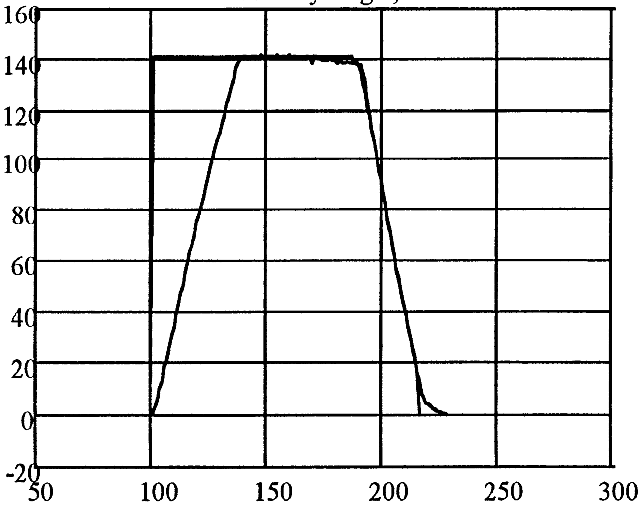
Full stroke seek

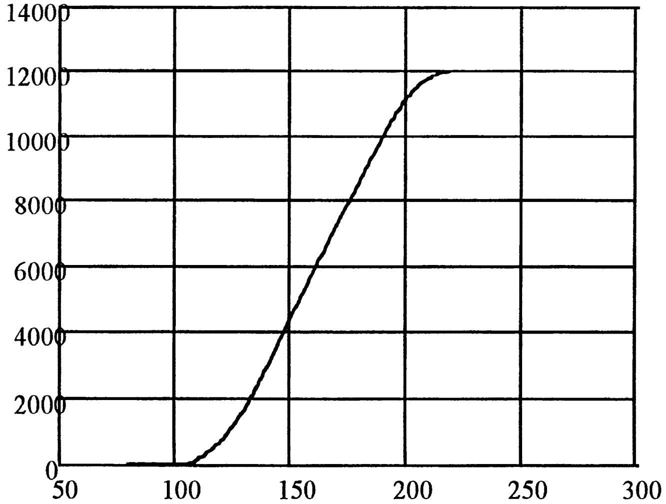


Full stroke seek


seekState


x4Hat and pwmOut and measured current

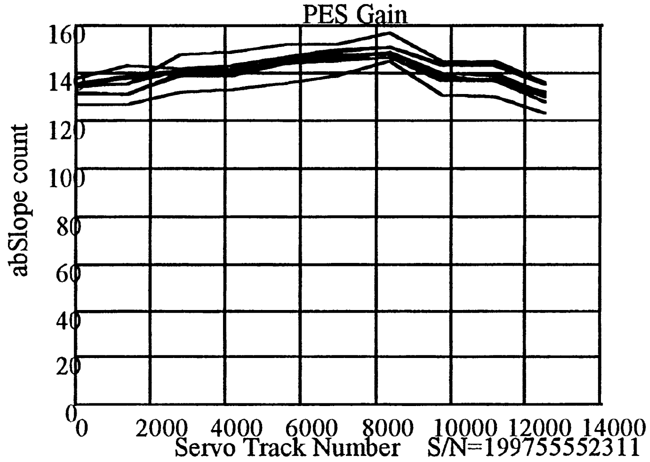

velocityTarget, x2Hat

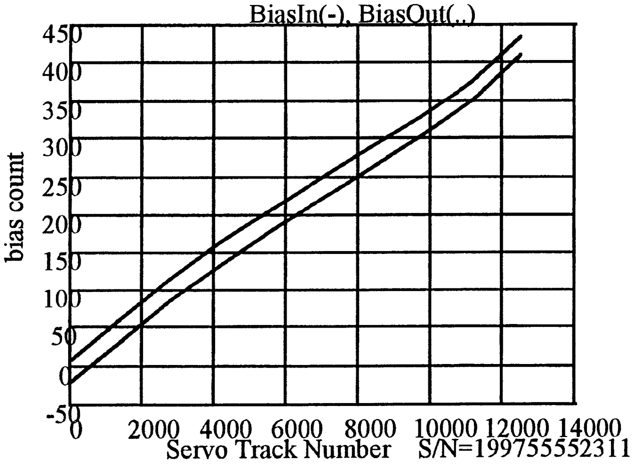

xMeas and x1Hat

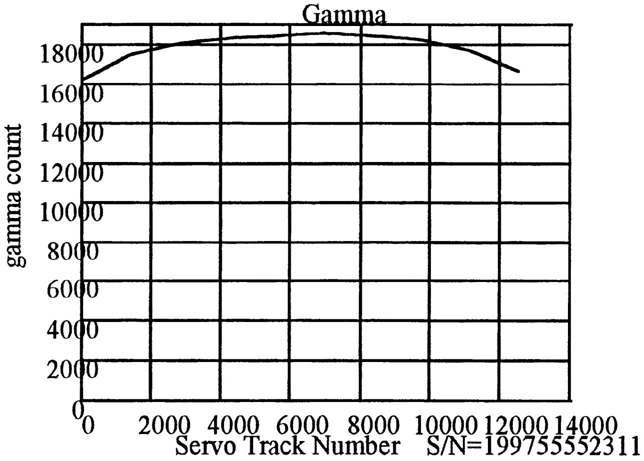
Power-on Calibration

- **Bias - Take an average of the current command. This is done for inward and outward going seeks in 10 zones.**
- **Pes gain - Servo at +/- 1/4 track offset and average burst values to derive PES gain. This is done on all heads in 10 zones.**
- **Kt/J - Inject digital sine wave disturbance and do a single point mechanical transfer function. This is done in 10 zones.**

Power-on Calibration



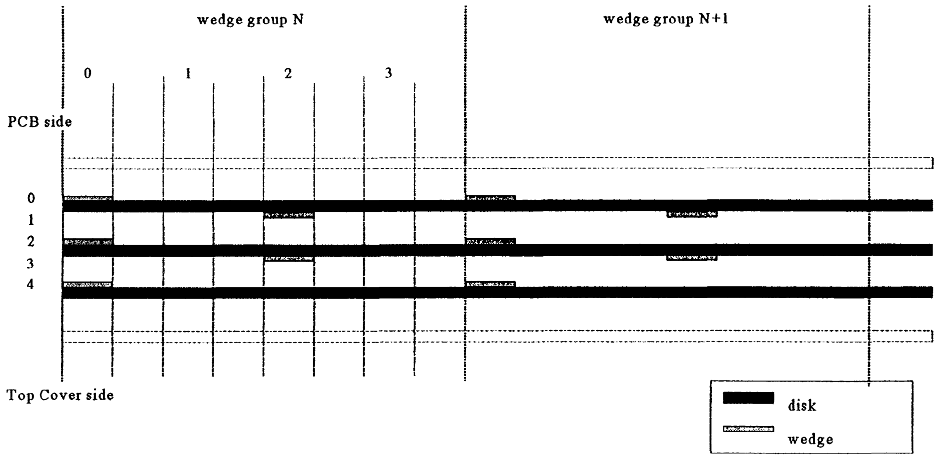




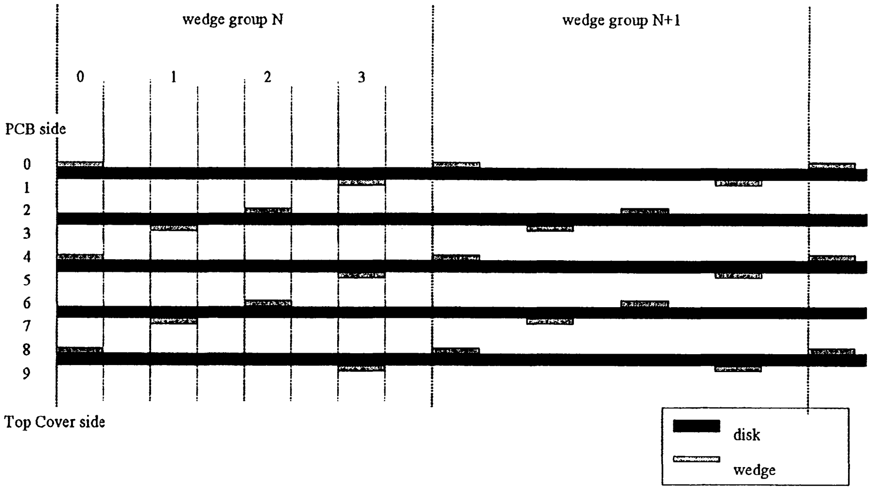
Passive Calibration

- **Repeatable runout - Find the 1st, 2ed, and 3rd harmonic components and cancel with feedforward.**
- **Feedforward scale - Integrate velocity error during decel and use result to scale feedforward.**
- **Maximum current - Derive maximum current from acceleration and use the result to scale the target velocity**

Wedge Stagger

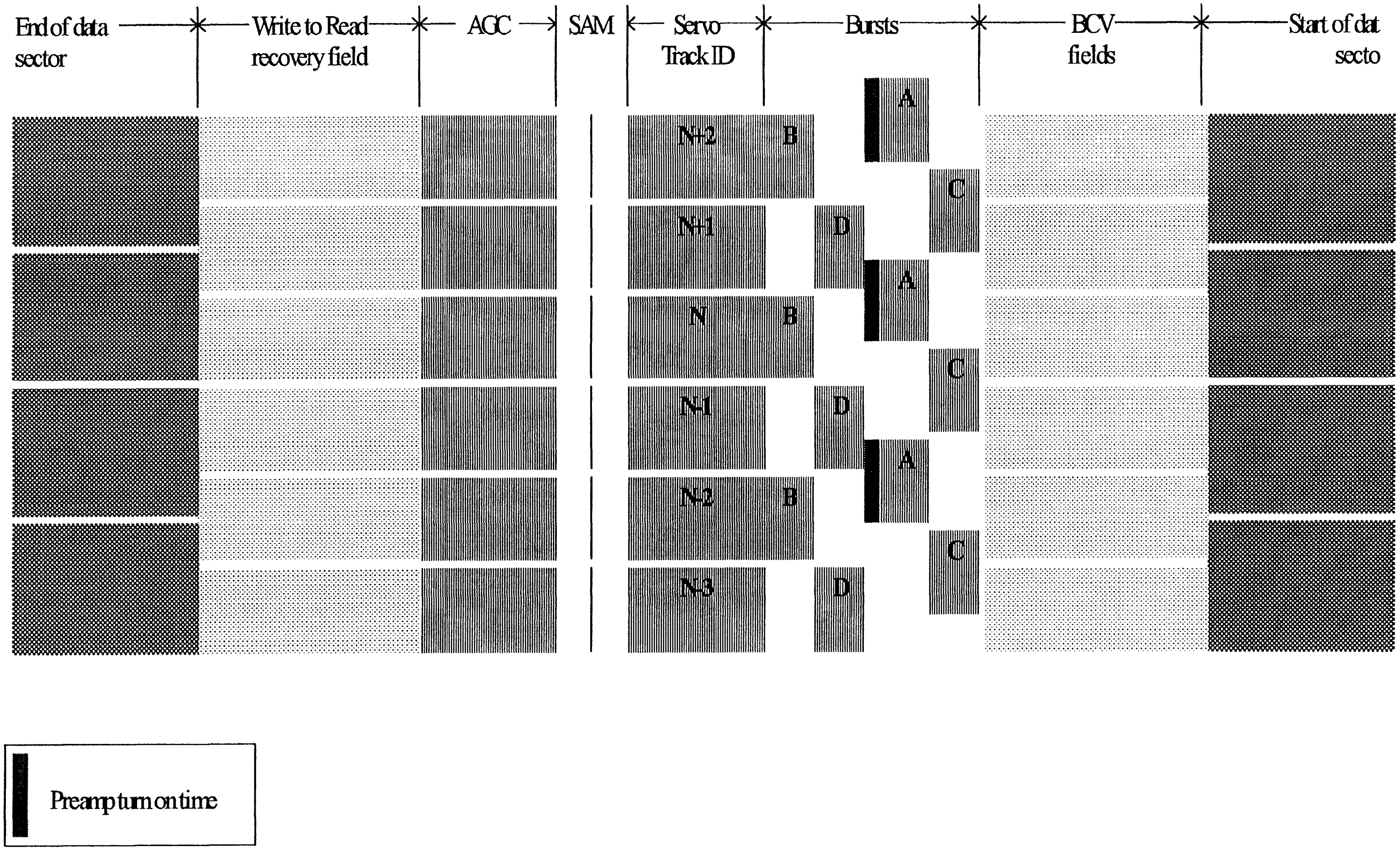


3-DISK ½ STAGGER

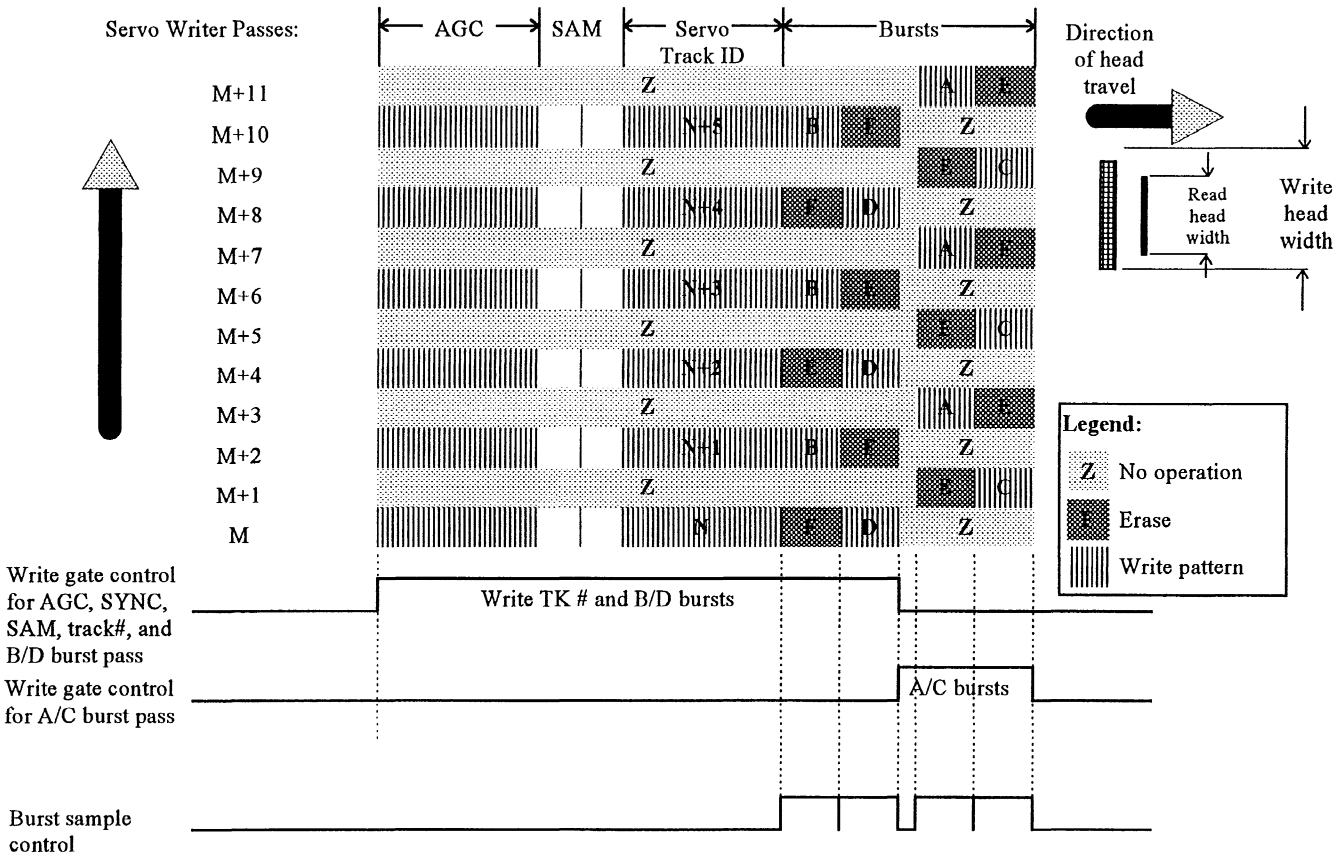


5-DISK ¾ STAGGER

Wedge Format



Write-gate Timing at Servowrite



PHOENIX

New Product Training
November 1997

Power Electronics Section

Refer to handouts

PHOENIX

Drive Electronics & PCB

November 10, 1997

Mehran Ataee

Quantum Confidential

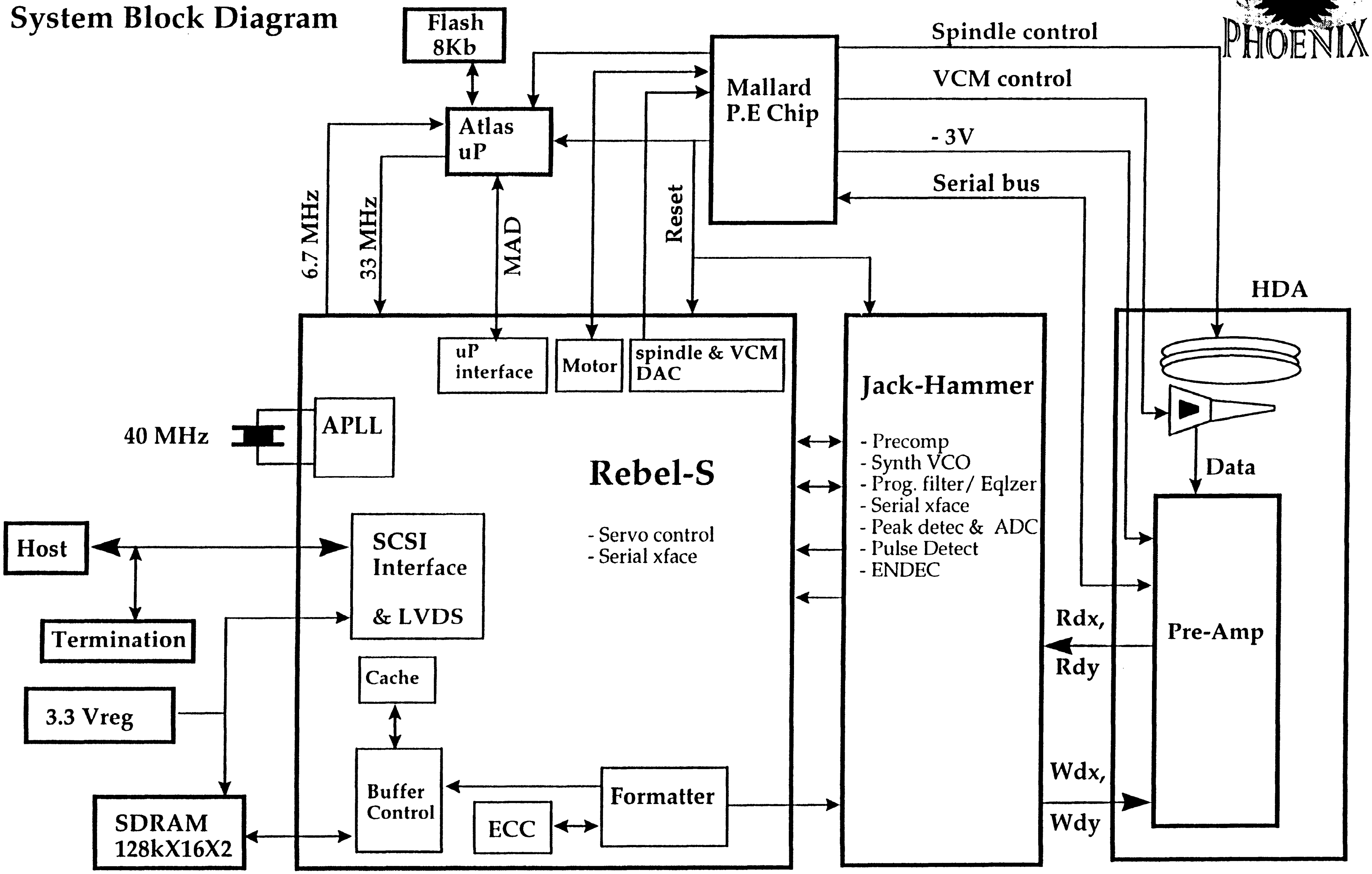
Phoenix Drive Electronics

Contents

- Block Diagram
- Pre-Amp
- Read/Write IC: *S-Hammer*
- Power Electronics IC: *Mallard*
- ASIC Control Chip: *Rebel-S*
- Micro-Processor: *Atlas*
- Memory
- SCSI Termination
- PCB
- Reference Material
  - Schematics & PCB Layout

Phoenix Drive Electronics

System Block Diagram



PHOENIX

Pre-Amp

- Designed for 4 terminal MR heads
- Serial port controls
    - Bias current
    - Write current
    - Head selection
    - Modes(i.e.: BHV, idle)
- Fast Mode for thermal Asperity recovery
- Multi head servo write
- Chip on ceramic packaging

PHOENIX

Read/Write IC

(Claw - Hammer)

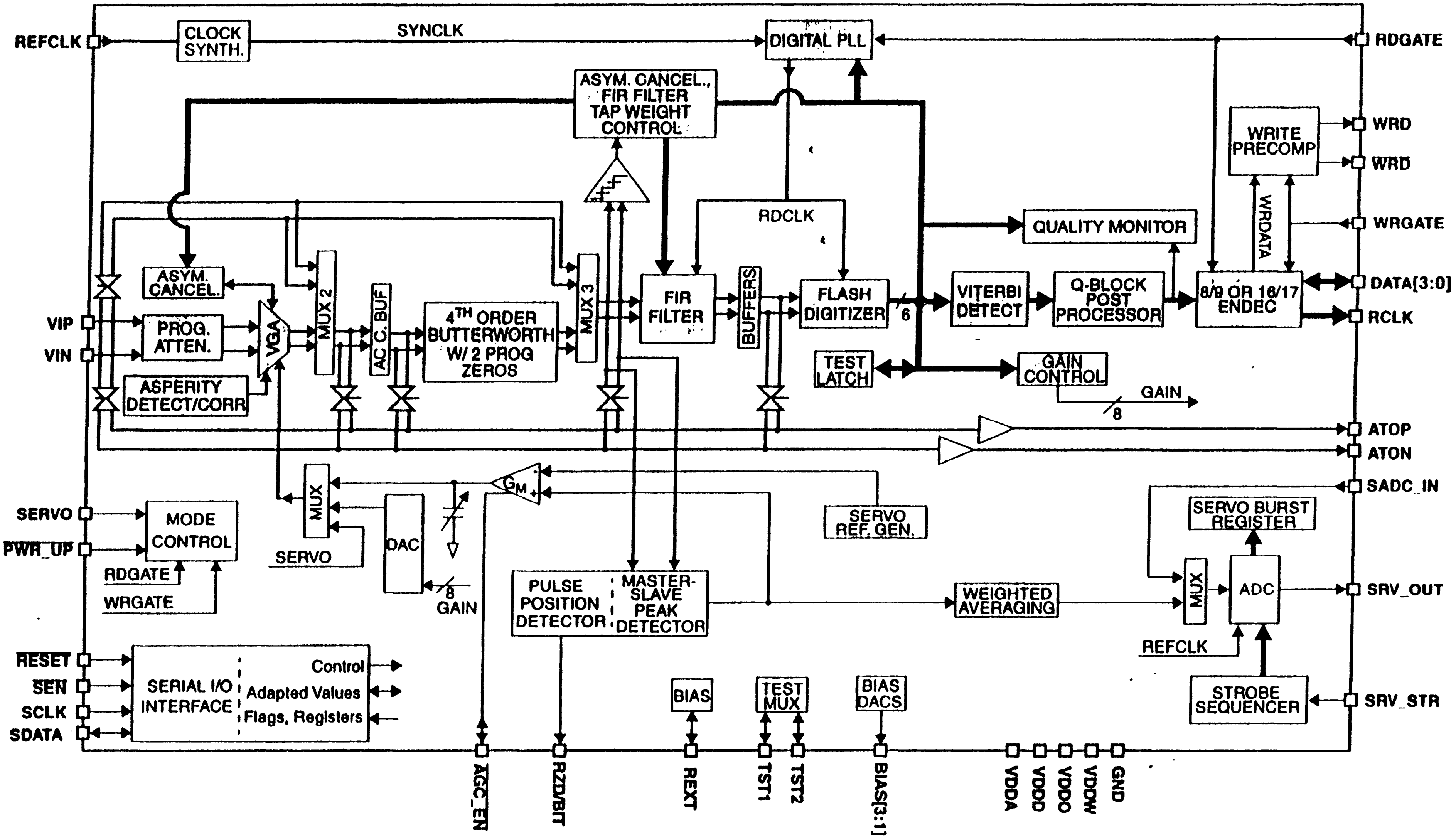
- 5V, 0.35 um CMOS process from Lucent Technologies Inc.
- 100 Pin single chip TQFP
- Functionality compatible with *Hammer (*Used in Viking drive)
- Higher performance than *Hammer*
- Pd: ~1.2 W (<5 mW in Power down mode)
- Data Rate: 190 Mbits/sec
- 5 step, 12 dB input attenuation range
- 4th order continuous time filter with 2 programmable zeros.
- 10 tap programmable discrete time adaptive FIR equalizer

Phoenix Drive Electronics

- Interleaved dicode *Viterbi* detectors
- Programmable Write data output: CMOS or differential pseudo-ECL
- Thermal Asperity detection & limited correction capability
- MR head non-linearity cancellation
- Encoder supports 8/9 & 16/17 density codes includes:
    - Preample generation
    - Sync mark
    - Fault tolerant sync mark recognition
    - Scrambling

Phoenix Drive Electronics

Claw- Hammer



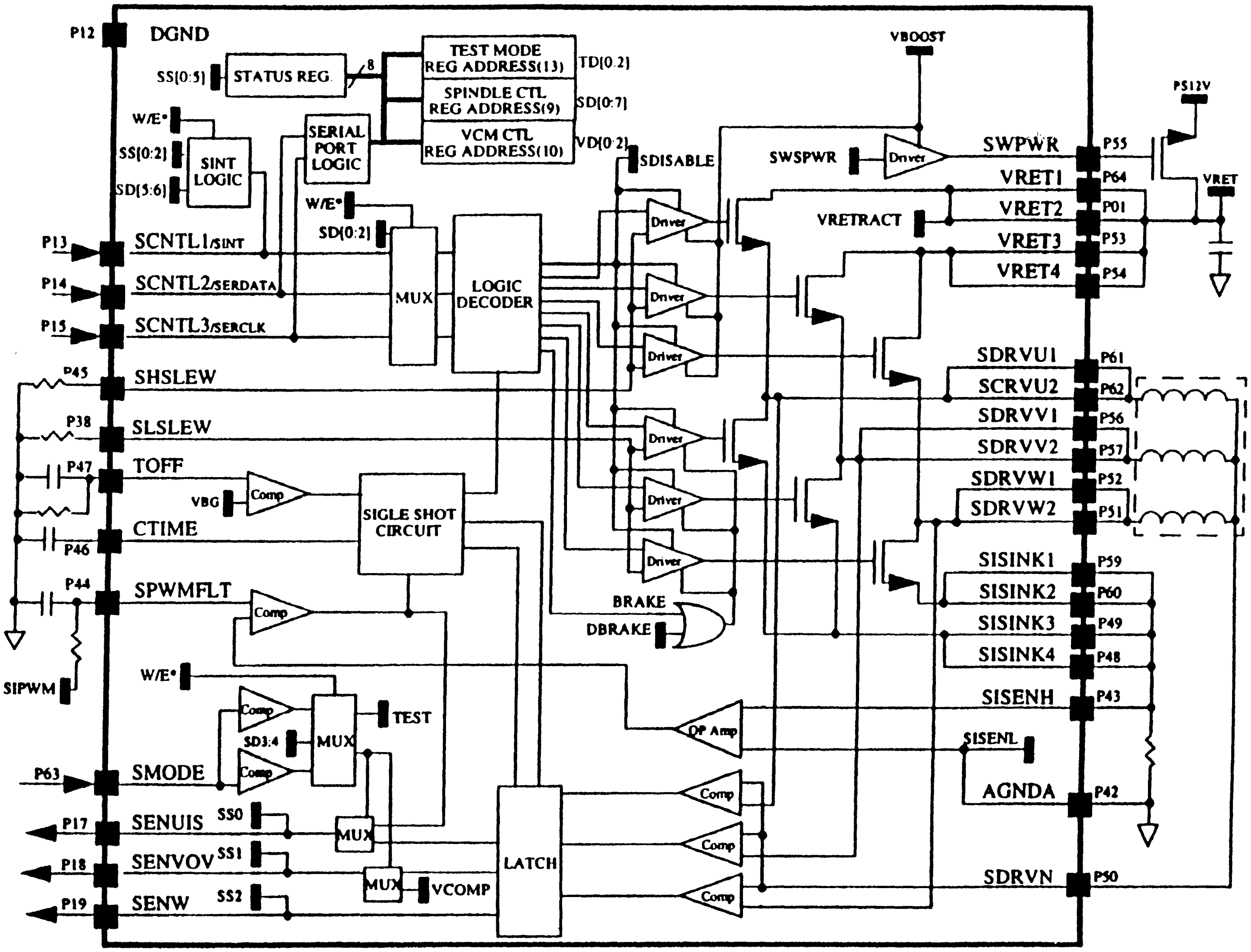
Power Electronic IC

(*Mallard*)

- **Single chip custom IC**
- **BICMOS / DMOS process**
- **TQFP 64 Pin with Slug**
- **Provides all Power, Analog, and thermal functions**
- **Provides -3V for pre-Amp**
- **Can handle over 4 Amp for spindle & 2.5 Amp for VCM.**
- **Digital Commutation/PLL with no drift over time & temperature**
- **Spindle Switchmode reduces Pd by X10**
- **Provides excellent rpm regulation**
  - Track Following: +/- 0.01%
  - Seek: +/- 0.04%

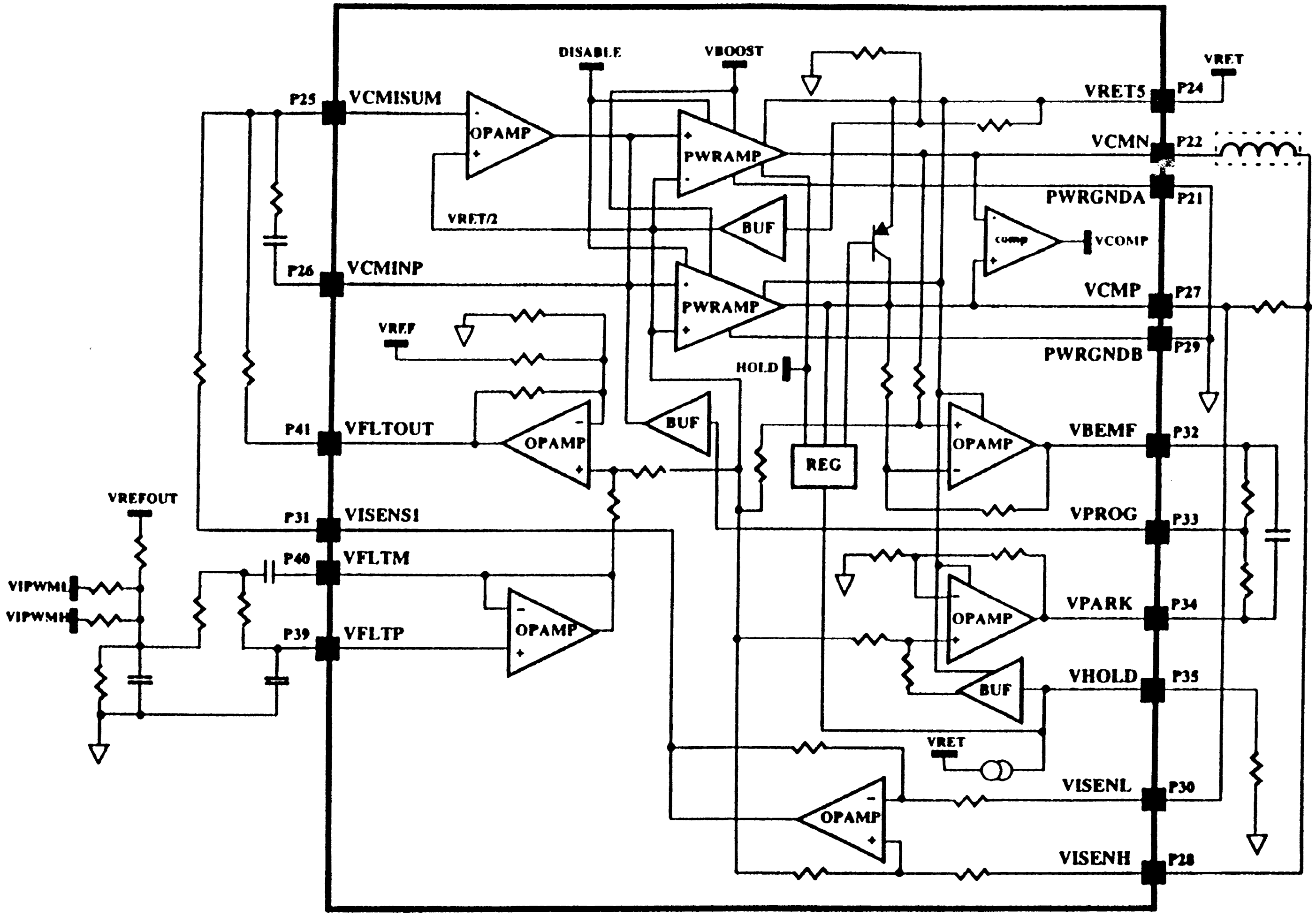
Phoenix Drive Electronics

Mallard:
Spindle



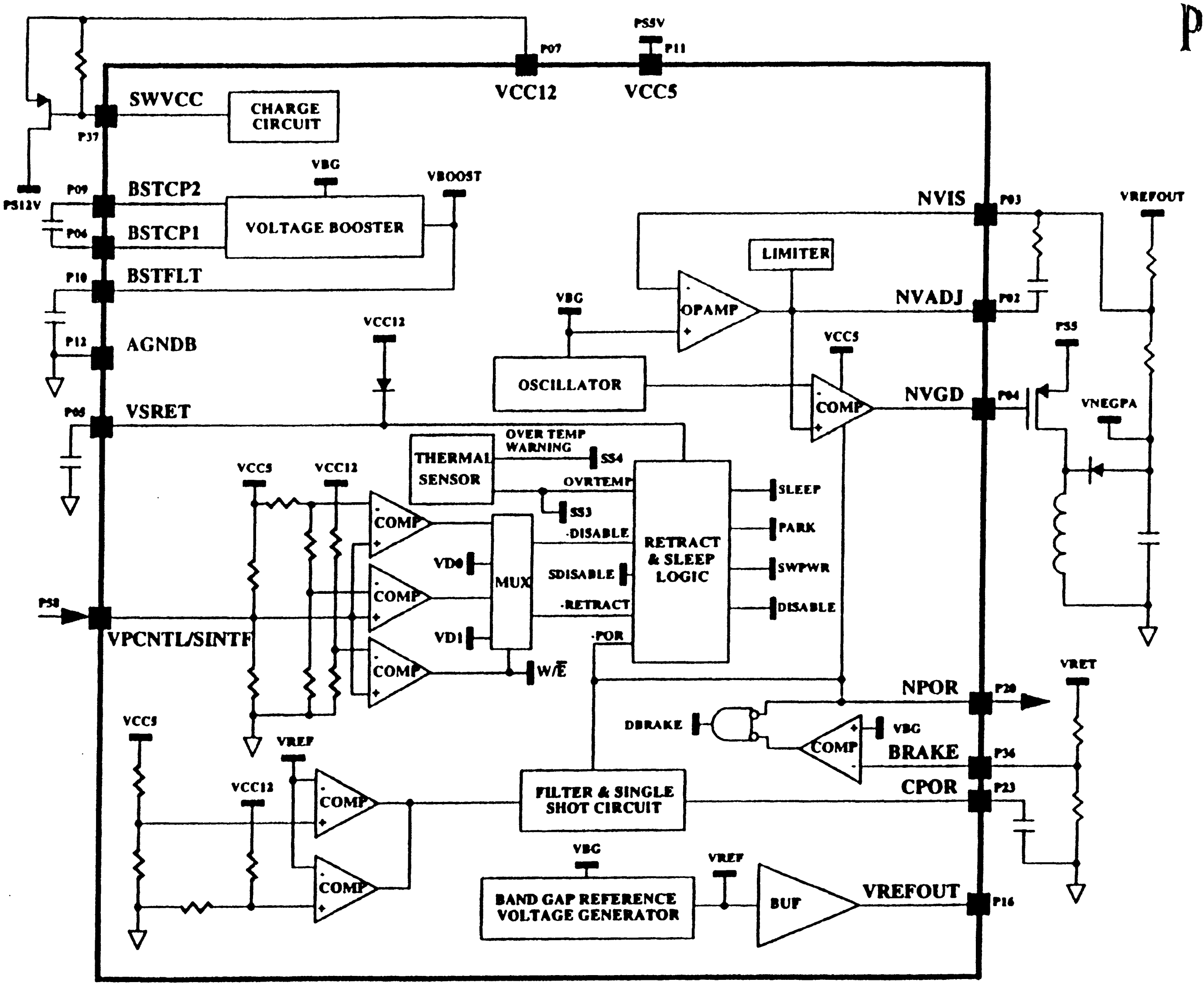
Phoenix Drive Electronics

Mallard:
VCM



Phoenix Drive Electronics

Mallard:
Other Blocks



PHOENIX

ASIC Control Chip

(*Rebel-S*)

- **Major block**
  - SCSI interface
  - Sequencer (formatter)
  - ECC
  - Buffer (can support either EDO or SDARM)
  - Servo
  - uP support
  - Serial interface
  - Motor
  - APLL
  - BLM

PHOENIX

SCSI Interface

- Asynchronous data transfer: 6 Mxfer/s
- Synchronous data transfer: 2.1 Mxfer/s - 10 Mxfer/s,
  20 Mxfer/s (Ultra 2 SCSI),
  40 Mxfer/s (in LVD)

- On-chip single ended 48 mA driver
- Write control store (WCS); 96 words x 24 bits
- Support data integrity code(i.e. CRC instead of parity) for buffer data
- Target mode only
- Selectable (single ended, or LVD) after power up
  - If the mode change stays on for more than 100 ms, uP re-initializes the SCSI mode.

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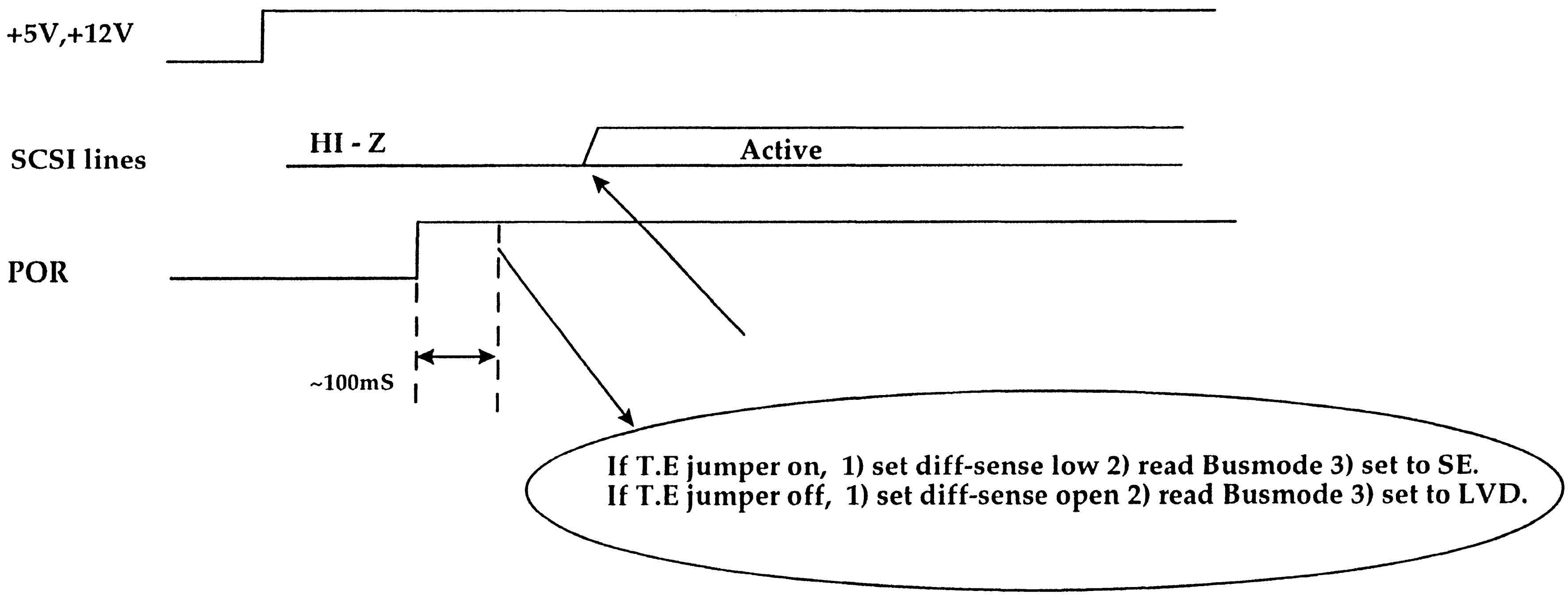
SCSI Interface *Continued,*

- **Power up SCSI mode select:**



If T.E jumper on, 1) set diff-sense low 2) read Busmode 3) set to SE.
If T.E jumper off, 1) set diff-sense open 2) read Busmode 3) set to LVD.

Low Voltage Differential

(*LVD*)

- New Technology Meets SPI-2 Specification
- Differential mode
    - Suedo ECL voltage swing generating less noise
        - > Single termination: 1.25V +/- 0.3V
    - Cable length: Greater than 10 Meter

Phoenix Drive Electronics

PHOENIX

Feature	Phoenix	Viking
Xfer rate	40 Mxfer/s	20 Mxfer/s
LVD	Yes	No
Switchable SCSI mode	Yes	N/A
WCS	96 wdX24 bit	76wdX24
CRC	Yes	No

Micro-Processor

(*Alas*)

- High performance RISC CPU
- 33 MHz clock
- General Registers: 32 bit X 32 bit
- 16 bit Data bus (MAD)
- Memory Space: 16 MB
- 14 Maskable interrupts
- Real time counters/timers
- On board Memory
  - ROM/PROM 48 KB
  - RAM 2K

Phoenix Drive Electronics

- **Instruction set:**
  - 74 instructions
  - 16 bit X 16 bit in 1-2 clocks
  - Saturated operation
  - 32 bit shift operation in 1 clock
  - Bit manipulation capability

PHOENIX

Memory

- Sych DRAM 128KX16X2 in 50 pin TSOP

- Serial EEPROM
  - 8 KB used for serial numbers, variation codes etc.
  - Can endure 1000,000 erase/write cycles
  - Data retention of 40 Years

PHOENIX

SCSI Termination IC

- Single monolithic bipolar IC
- Low capacitance output cell
- Termination Model:
    - 110 Ohm connected to 2.6V DC.
- User controlled termination enable/disable
- Thermal protection at 175C.

Phoenix Drive Electronics

- Termination Technique

  - Narrow:
    - > Single Ended termination
    - > Both Data & Data* are available at the connector
    - > Can also operate in LVD (no Termination)
    - > SCSI II voltage levels
  - Wide:
    - > Termination for Data* line
  - SCA:
    - > No termination(LVDs used)

Printed Circuit Board

- **4 Layer FR4 PCB**
- **Top-mount component**
- **Small form factor for maximum panel efficiency**
- **All Layers 1 Oz Cu:**
  - Layer 1 (top): Trace
  - Layer 2: Solid Ground
  - Layer 3: Power / trace
  - Layer 4: Trace / Ground

Phoenix Drive Electronics

PCB continued,

- ◆ **Designed for Excellent thermal performance**
- ◆ **Designed for minimum EMI**
- ◆ **Designed for minimum noise coupling**
- ◆ **Minimum conducted noise due to power electronics**
- ◆ **Designed for automated assembly, inspection & test**

Phoenix Drive Electronics

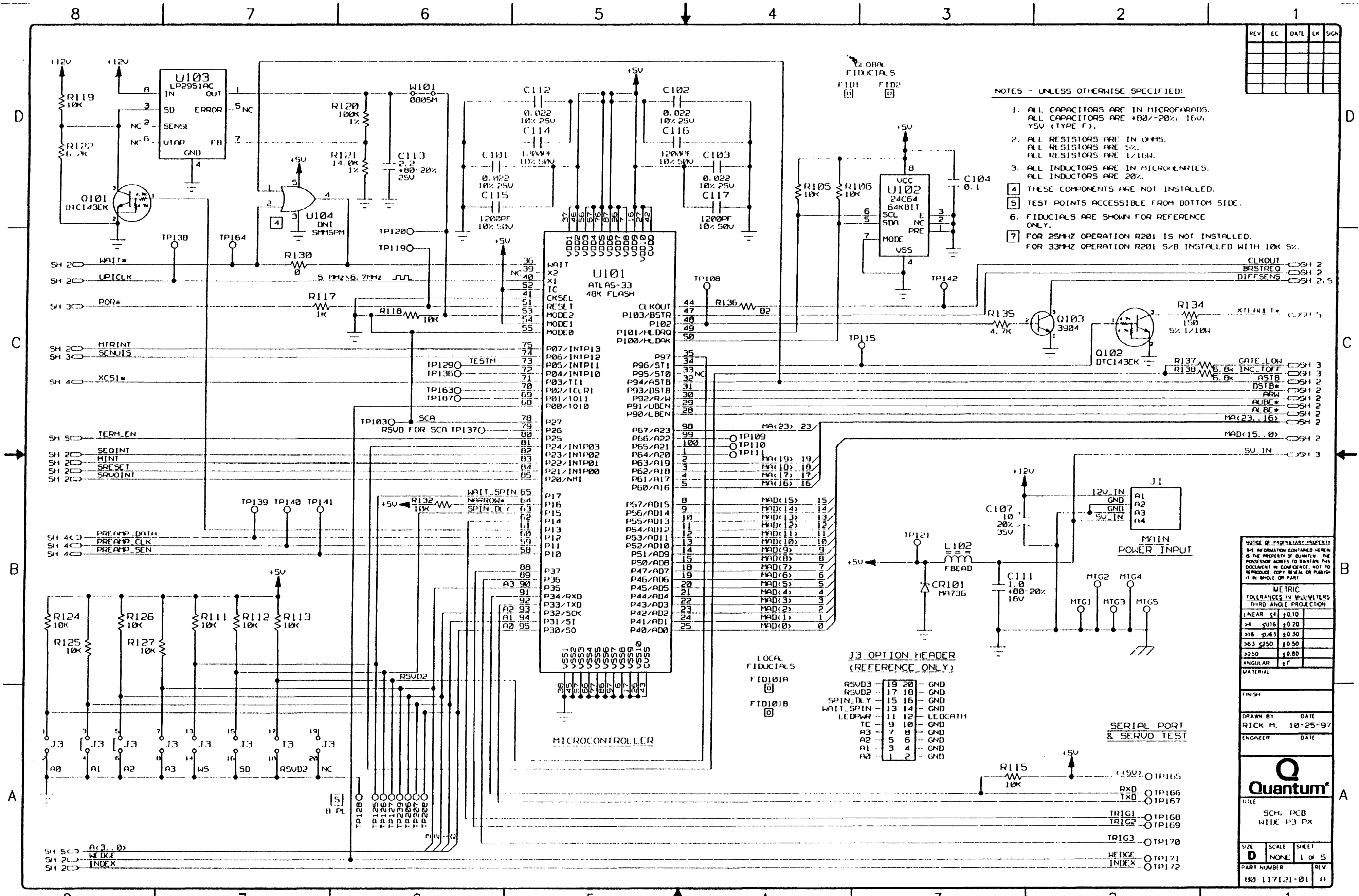
PCB Continued,

- **Maximum Component Height**

  >3.05 mm for SCSI connector & All Electronics

- **Providing LED for self test**

- **Providing Term-power fuse for protection**



NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL CAPACITORS ARE IN MICROFARADS.
   ALL CAPACITORS ARE +80/-20%, 16V,
   Y5V (TYPE F).
2. ALL RESISTORS ARE IN OHMS.
   ALL RESISTORS ARE 5%.
   ALL RESISTORS ARE 1/16W.
3. ALL INDUCTORS ARE IN MICROHENRIES.
   ALL INDUCTORS ARE 20%.

[4] THESE COMPONENTS ARE NOT INSTALLED.

[5] TEST POINTS ACCESSIBLE FROM BOTTOM SIDE.

6. FIDUCIALS ARE SHOWN FOR REFERENCE ONLY.

[7] FOR 25MHZ OPERATION R201 IS NOT INSTALLED.
FOR 33MHZ OPERATION R201 S/B INSTALLED WITH 10K 5%.

REV	EC	DATE	CK	SIGN

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METRIC
TOLERANCES IN MILLIMETERS
THIRD ANGLE PROJECTION

LINEAR ≤4	±0.10	
>4 ≤U16	±0.20	
>16 ≤U63	±0.30	
>63 ≤250	±0.50	
>250	±0.80	
ANGULAR	±1°	

MATERIAL

FINISH

DRAWN BY RICK M. DATE 10-25-97

ENGINEER DATE

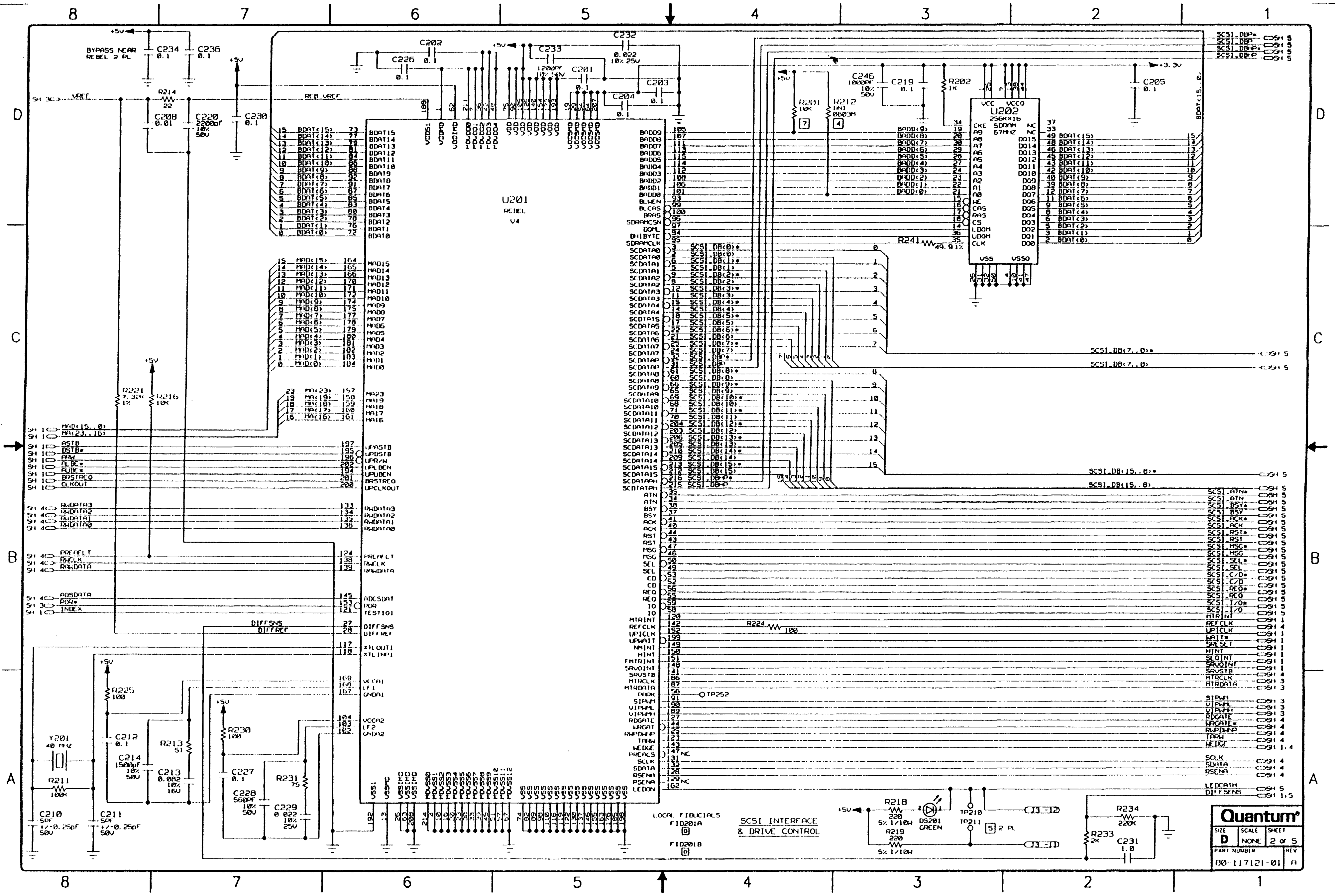
Quantum®

TITLE
SCH, PCB
WIDE P3 PX

SIZE D SCALE NONE SHEET 1 of 5

PART NUMBER 80-117121-01 REV A

DRAWING LAST_MODIFIED=Fri Nov 7 11:59:55 1997



Quantum®

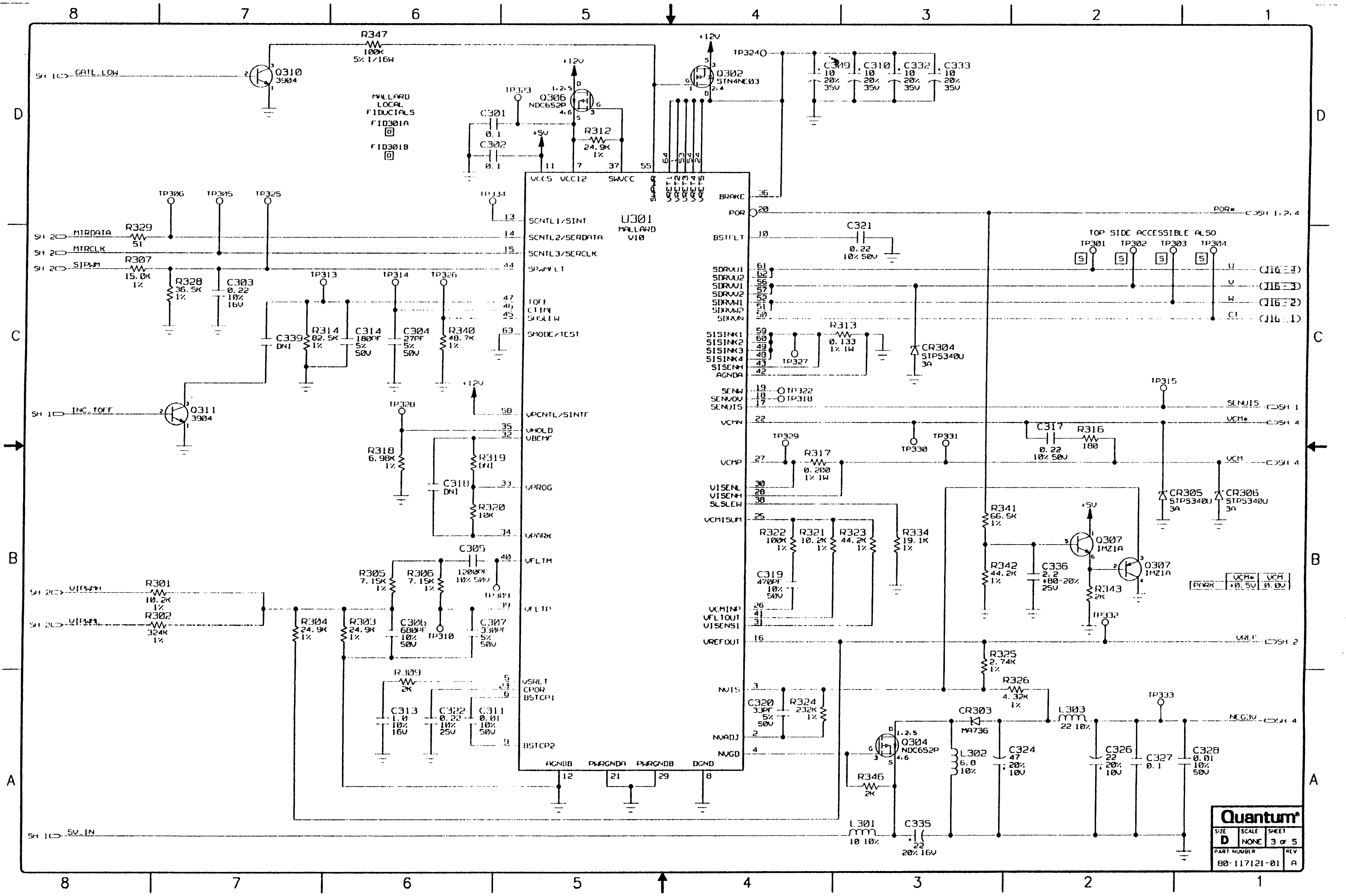
SIZE	SCALE	SHEET
D	NONE	2 of 5

PART NUMBER 80-117121-01 REV A

SCSI INTERFACE & DRIVE CONTROL

LAST_MODIFIED=Fri Nov 7 12:00:54 1997

DRAWINC



Quantum

SIZE	SCALE	SHEET
D	NONE	3 OF 5

PART NUMBER	REV
80-117121-01	A

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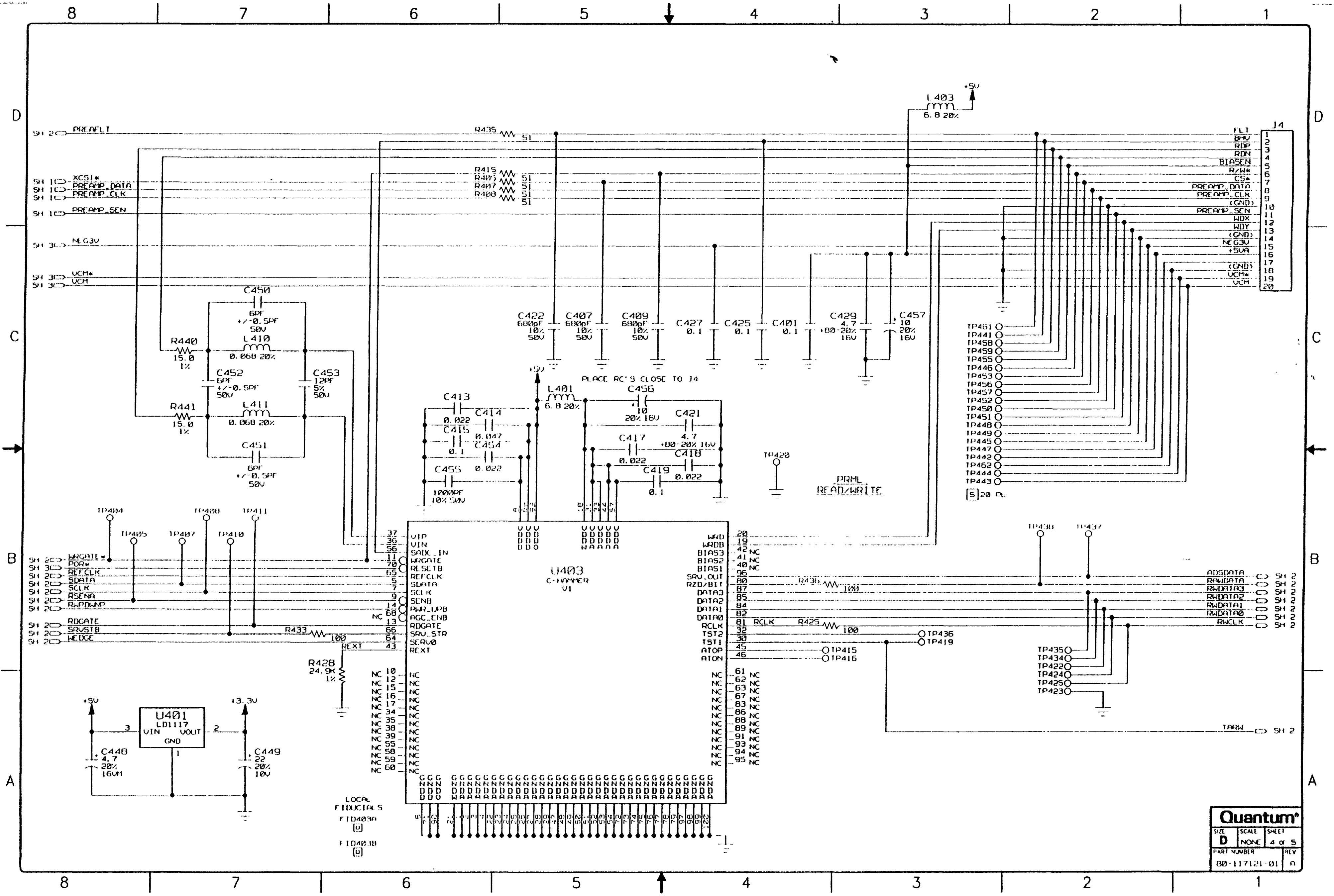

Quantum®

SIZE	SCALE	SHEET
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PART NUMBER	REV
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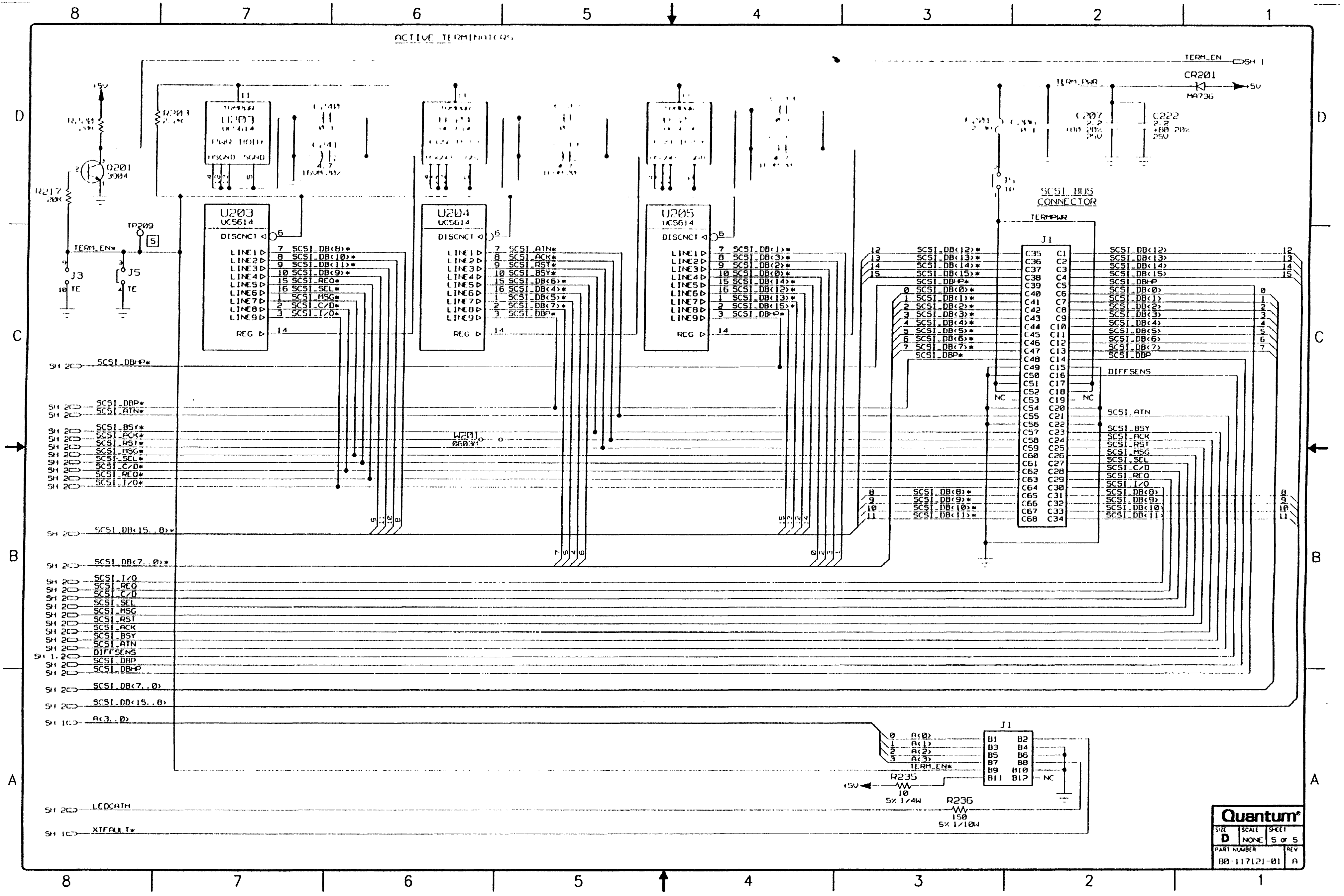


DRAWING LAST_MODIFIED=Fri Nov 7 12:02:17 1997

Phoenix Power Electronics

November 10, 1997

Mehran Ataee

Quantum Confidential

Phoenix Power Electronics

PHOENIX

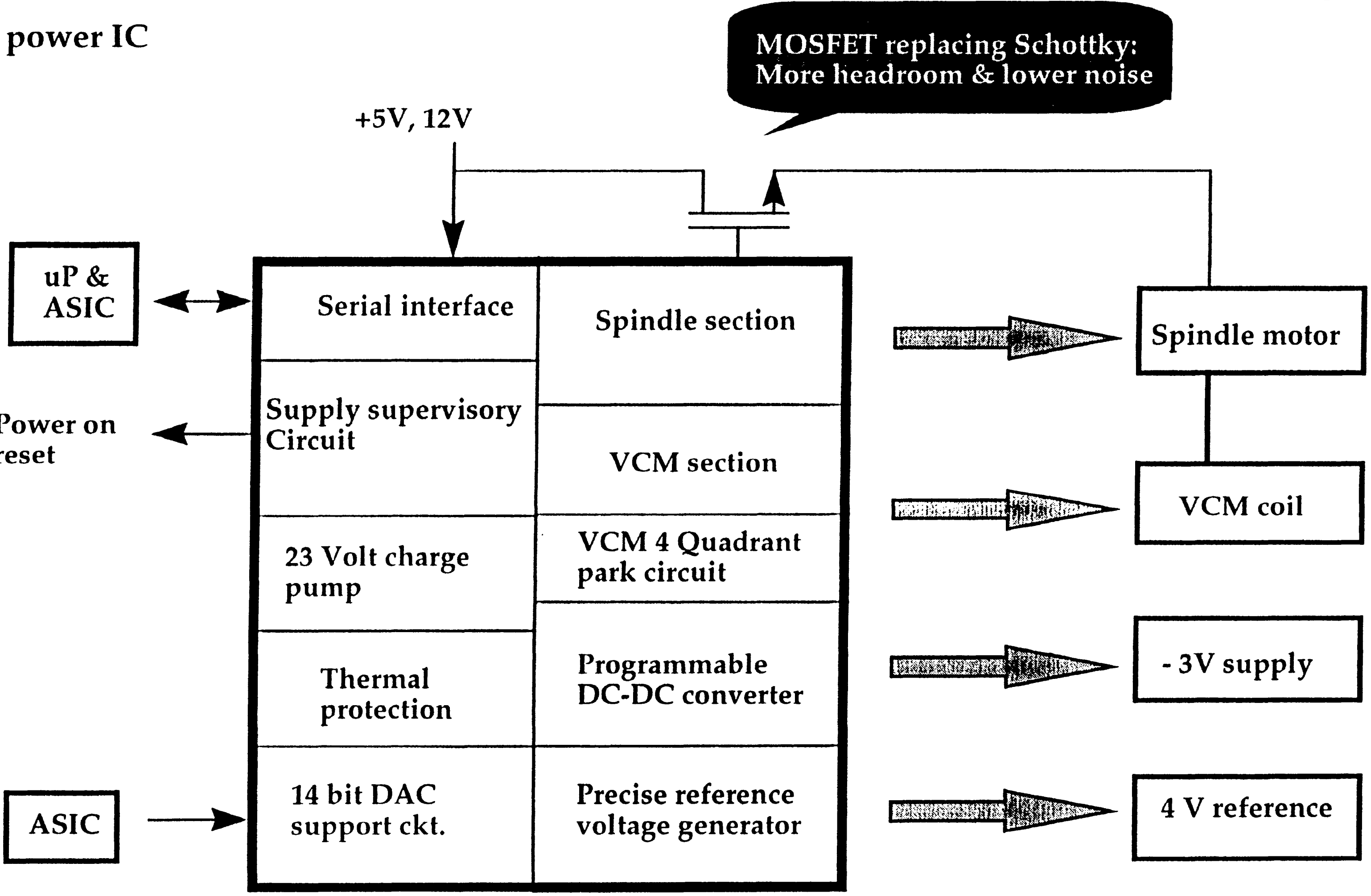
- Single Chip Custom IC (Mallard)
  - 1 chip provides all analog functions/power needs
  - Advanced BCD process: Low P_{stdby} & excellent speed
  - Monolithic performance
  - Drives Hall-less, Y- Connection Spindle motor
  - BEMF for spindle commutation

- Custom Package to Use PCB as Heat Sink ⇒ Excellent thermal path:
  - Lower Thermal Impedance
  - Higher Reliability

- Proper Circuit Partitioning ⇒ Best Silicon utilization

Mallard

Single chip power IC



MOSFET replacing Schottky:
More headroom & lower noise

+5V, 12V

uP & ASIC

Serial interface

Supply supervisory Circuit

Power on reset

23 Volt charge pump

Thermal protection

ASIC

14 bit DAC support ckt.

Spindle section

VCM section

VCM 4 Quadrant park circuit

Programmable DC-DC converter

Precise reference voltage generator

Spindle motor

VCM coil

- 3V supply

4 V reference

Phoenix Power Electronics

PHOENIX

- **VCM Driver**
  - **- Using 14 bit PWM DAC (simpler design than other DACs)**
  - **- Can Sink/source up to 2.5 Amps**
  - **- Programmable B.W (set to > 15 KHz)**
  - **- Programmable gain (set Gm ~1.4 A/V)**

- **Built-in thermal protection**
  - **- Provides thermal warning @ Tj = 125C prior to thermal shut down @ Tj = 150C**

Phoenix Power Electronics

- **Negative Voltage DC-DC Converter**
  - Uses 1 external transistor to meet current requirements (SOT 6)
  - Programmable voltage with 1 resistor
  - Output accuracy = < 2%

- **Supply Supervisory Circuit**
  - Monitors both 5V & 12V
  - Built-in de-glitcher & hysteresis
  - Programmable POR delay

- **14 bit VCM DAC Support**
  - Provides 3rd order Low Pass filter & summer

Phoenix Power Electronics

PHOENIX

Spindle Driver

- All Digital Commutation circuit
  - Reliable timings set by digital PLL
  - Stable operation over temperature and time

- Spindle switchmode operation
  - Reducing Pd by ~ 10X
  - Significant heat reduction, lower Tj rise than linear drive

- Spindle Control Loop
  - Reliable compensation via D.S.P.
  - No resistor/capacitor; no drift over time and temperature

Phoenix Power Electronics

Unique Spindle Startup Algorithm

- Always positive torque generation (no R.R)
- Achieves 0 - 7200 rpm in shortest time
- Extremely low "spin up retry" rate

◆ **Bipolar Start - Bipolar Run**

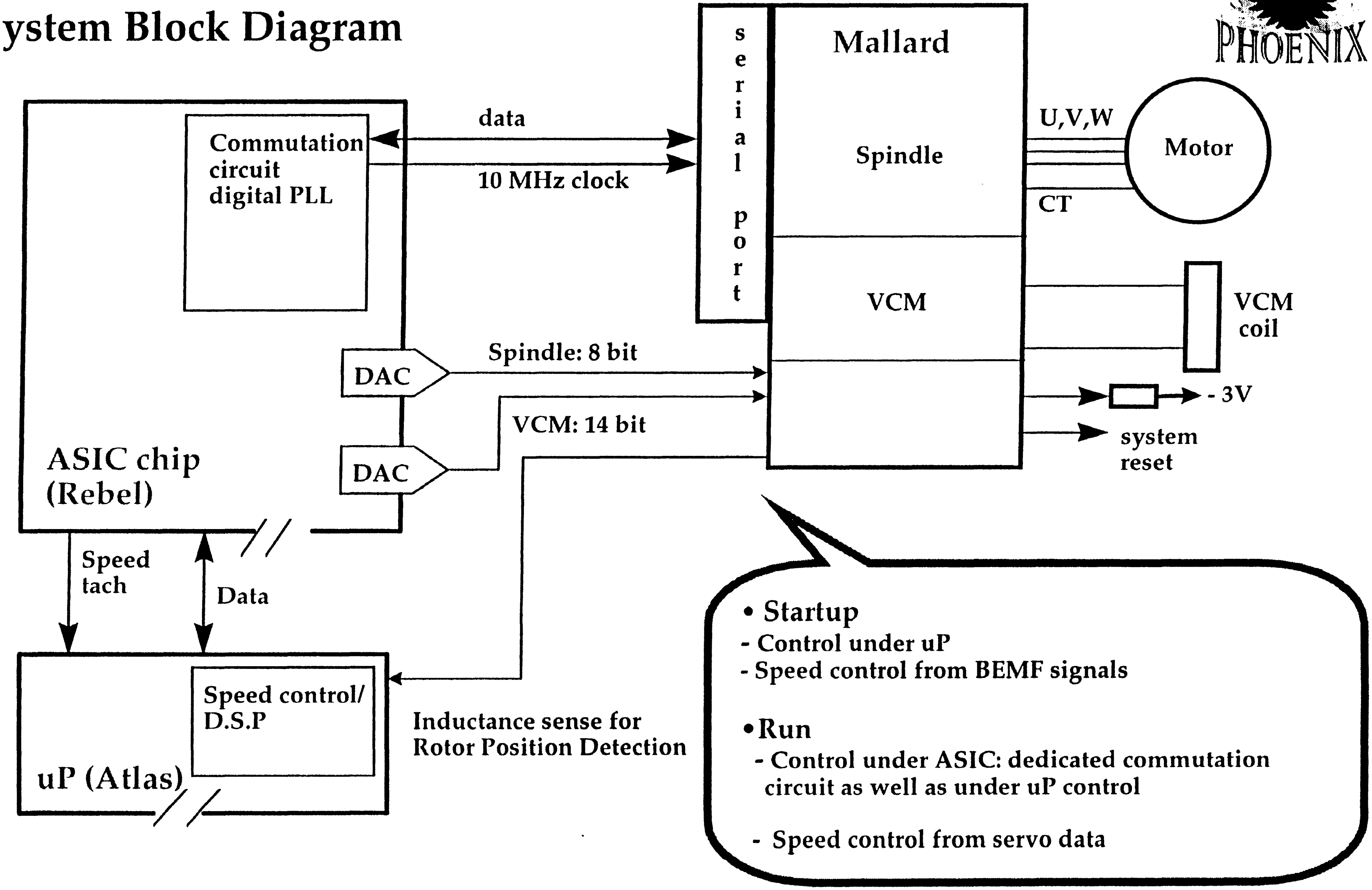
- Efficient operation during run

◆ **Excellent rpm regulation with improved control loop**

- Servo data used for speed regulation provides jitter-free period detection
- < 0.01% during "track following"
- < 0.04% step response(OD-ID-OD)

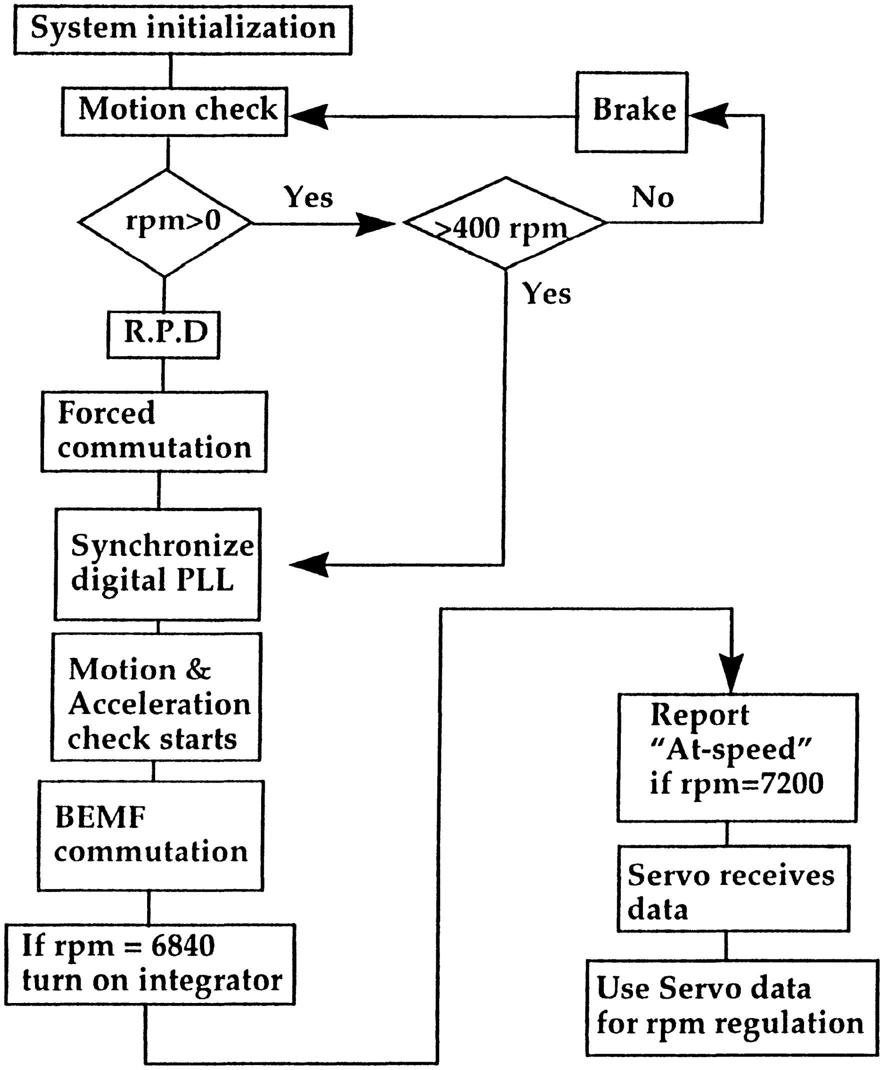
PHOENIX

System Block Diagram



- Startup
  - Control under uP
  - Speed control from BEMF signals
- Run
  - Control under ASIC: dedicated commutation circuit as well as under uP control
  - Speed control from servo data

Spin Up Algorithm



System initialization

Motion check

rpm>0

Yes

>400 rpm

No

Brake

Yes

R.P.D

Forced commutation

Synchronize digital PLL

Motion & Acceleration check starts

BEMF commutation

If rpm = 6840 turn on integrator

Report "At-speed" if rpm=7200

Servo receives data

Use Servo data for rpm regulation

1- Total of 5 spinup attempts allowed.

2- Braking at 6000 rpm and lower.

3- If Mallard Tj >125, the seek profile is adjusted to avoid thermal shut down >>> Lower seek performance at elevated temperature.

4- R.P.D: Rotor Position Detection using "Inductive sensing."

Phoenix Power Electronics

PHOENIX

Mallard Power IC (L6253)

Manufacturer:	**SGS-Thomson**
Design Center:	**San Jose**
Die Size:	**6.04 mm X 5.25 mm**
Package:	**64 pin TQFP with Slug**
Wafer Size:	**6 inches**

Phoenix Power Electronics

PHOENIX

- Process: BCD

NPN ft: 850 MHz & 180 MHz

PNP ft: 35 MHz

CMOS: tpd = 1.2 nS

22 Mask levels

3 Metal layers:

Metal 1= 0.7 um, Metal 2 = 1.0 um

Metal 3 = 3.0 um

Fab: Agrate & Castelletto (Italy)

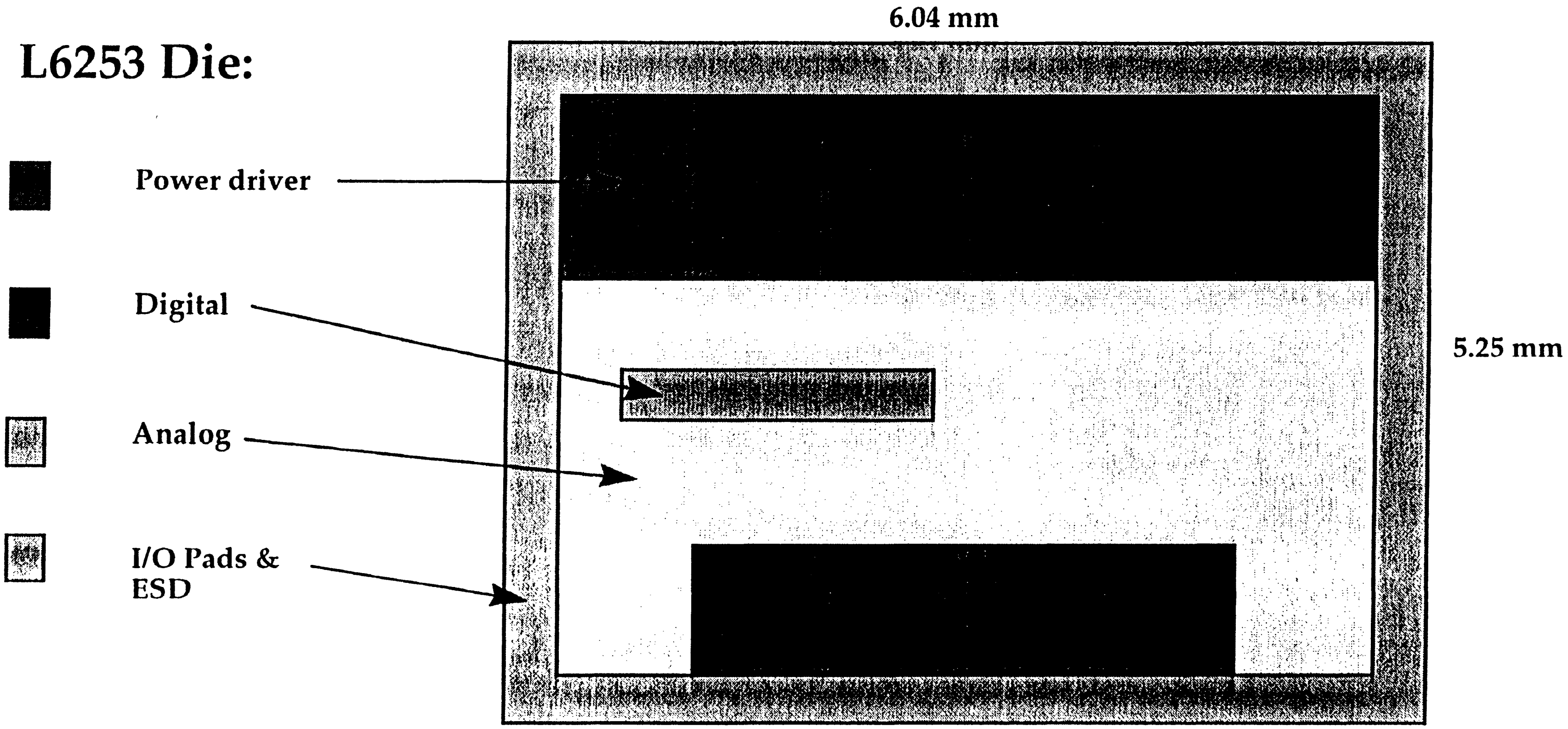
Assembly: Anam(Philippines)

Testing:

Final test: Topayo (Singapore)

Complete parametric and functionality at wafer level and packaged IC

L6253 Die:



■ Power driver

■ Digital

▨ Analog

▨ I/O Pads & ESD

PHOENIX

New Product Training
November 1997

Pre-Amp Section

READ CHANNEL: PREAMP, FLEX, CERAMIC, FIC

- PREAMP
  - KEY REQUIREMENTS FOR PHOENIX
  - FEATURES AND SPECIFICATIONS
  - MEASUREMENTS
- CERAMIC
  - CERAMIC DESCRIPTION
  - SCHEMATIC
  - DESIGN AND LAYOUT CONSIDERATIONS
- PREAMP TEMPERATURE MEASUREMENTS
  - TESTING METHODOLOGY
  - TEST RESULTS
- FIC/CIS
  - FIC CONFIGURATION
  - ELECTRICAL CHARACTERISTICS

KEY REQUIREMENTS FOR PHOENIX

- **FAST RISE AND FALL TIMES: < 2.0 NSEC(20% - 80%)**

- **METHOD OF CONTROLLING PREAMP WITHOUT THE NEED FOR SENSITIVE INPUTS TO BE BROUGHT TO PCB**

- **BUFFERED HEAD VOLTAGE MONITOR**
- **FAST WRITE TO READ RECOVERY**
- **READ AND WRITE FAULT DETECTION**

KEY SPECIFICATIONS

- **VTC 6160 PREAMP**
- **NOMINAL GAIN=220; INDEPENDENT OF MR RESISTANCE**
- **BANDWIDTH=130 MHZ**
- **EQUIVALENT INPUT NOISE=0.65 NV/RT HZ**
- **WRITE CURRENT RISE/FALL TIME: < 2.0 NS, SPECIFIED WITH 220NH, 15 OHM, 25 MA, 20-80%**
- **HEAD SWITCH TIME < 3 µSEC, IMR UNCHANGED**
- **WRITE TO READ RECOVERY TIME < 1.0 µSEC**
- **POWER SUPPLY REJECTION RATIO > 45 dB, UP TO 10 MHz**

KEY FEATURES

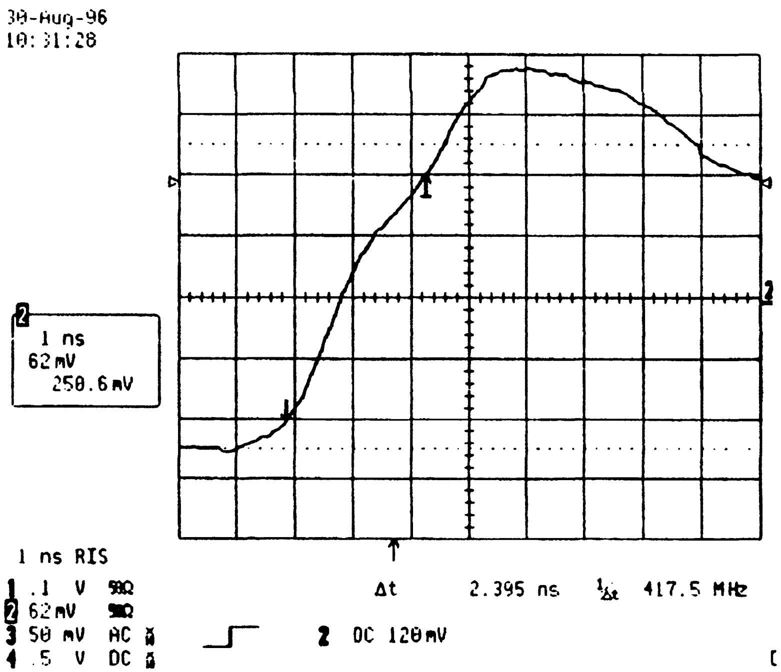
- DIFFERENTIAL PREAMPLIFIER
- I-BIAS/V-SENSE ARCHITECTURE
- SERIAL PORT PREAMP ELIMINATES NEED TO BRING SENSITIVE PREAMP INPUTS DOWN FLEX CABLE
- VERIFY MODE FOR SERIAL PORT REGISTERS
- DUAL SUPPLY PREAMP, +5V, -3V
- BUFFERED HEAD VOLTAGE MONITOR
- READ AND WRITE FAULT DETECTION

MR PREAMP/CERAMIC/FLEX

- **CHIP ON FLEX ON CERAMIC**
- **VTC DIFFERENTIAL PREAMPLIFIER**
  - **-VTC 6160 6-CHANNEL PREAMP FOR 3-DISK;**
    - **CERAMIC LAYOUT USES 5 CHANNELS**
  - **-VTC 6160 12-CHANNEL PREAMP FOR 5-DISK;**
    - **CERAMIC LAYOUT USES 10 CHANNELS**
- **HEAD PADS ON CERAMIC CONNECTED TO FIC**
- **SERIAL PORT COMMUNICATIONS FOR HEAD SELECT, BIAS CURRENT, WRITE CURRENT, AND SOME CONTROL FUNCTIONS.**

RISE AND FALL TIMES

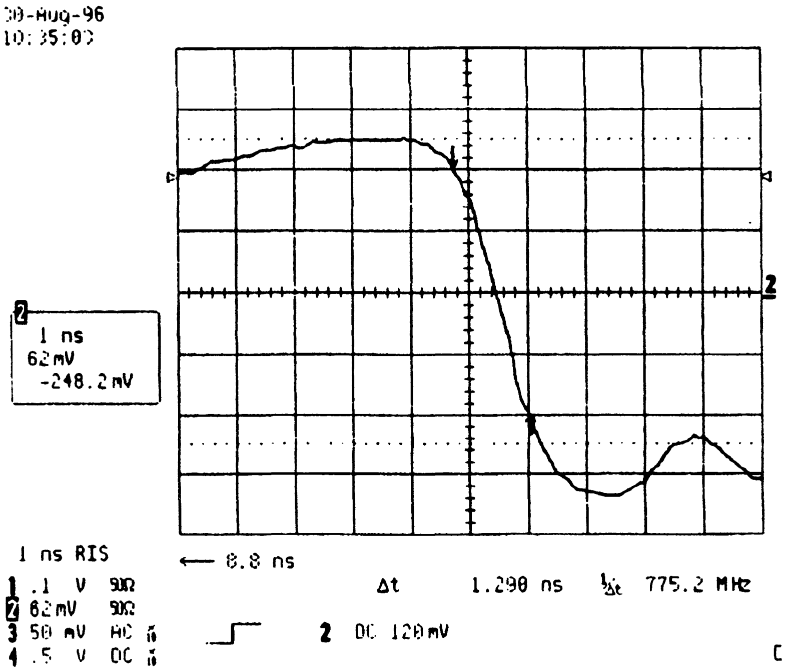
PREAMP RISE AND FALL TIMES ON SPIN STAND, 20%-80% < 2.0 nsec


30-Aug-96
10:31:28

2
1 ns
62mV
250.6mV

1 ns RIS
1 .1 V 50Ω
2 62mV 50Ω
3 50 mV AC
4 .5 V DC

Δt 2.395 ns 1/Δt 417.5 MHz
2 DC 120mV

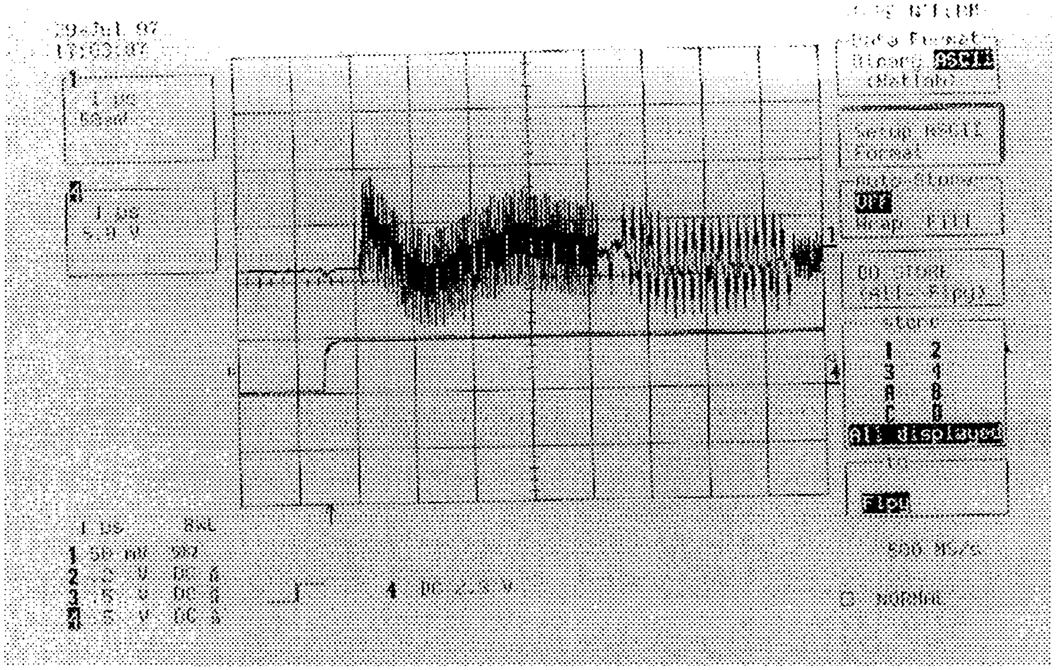

30-Aug-96
10:35:03

2
1 ns
62mV
-248.2mV

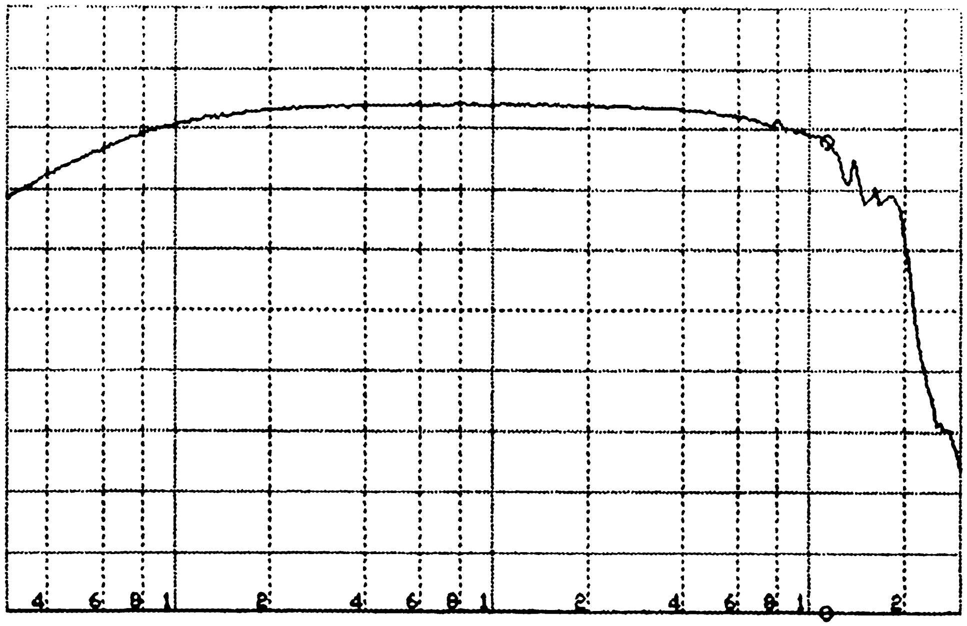
1 ns RIS
← 0.8 ns
1 .1 V 50Ω
2 62mV 50Ω
3 50 mV AC
4 .5 V DC

Δt 1.290 ns 1/Δt 775.2 MHz
2 DC 120mV

PREAMP WRITE TO READ RECOVERY



Preamp Bandwidth



```
 DIV       DIV      START       300 000.000 Hz
5.000     36.00      STOP 300 000 000.000 Hz
RBW:  1 KHz ST:12.8 sec RANGE:R=  0,T= 10dBm
```

PREAMP BANDWIDTH: LF = 700 khz, HF = 120Mhz

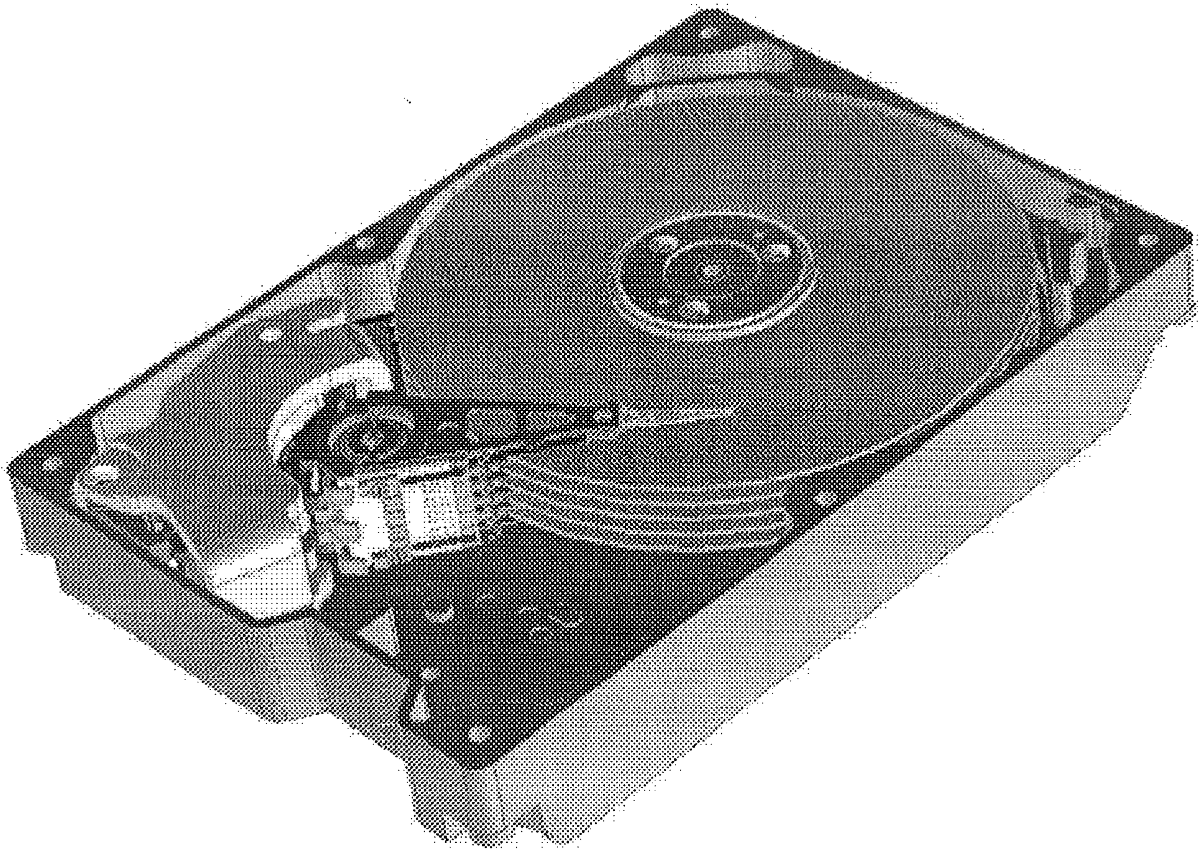
CERAMIC

- LOW TEMPERATURE CO-FIRED MULTILAYER CERAMIC
- SUBSTRATEPREAMP DIE IS MOUNTED ON CERAMIC, WIRE BONDED TO CERAMIC, AND ENCAPSULATED
- 6 LAYER CERAMIC ALLOWS ROOM FOR ROUTING OF HEAD TRACES AND FOR EXTERNAL COMPONENTS
- CERAMIC IS ATTACHED TO FLEX CABLE WITH A HOT BAR SOLDERING PROCESS
- CERAMIC PROVIDES AREA FOR CONNECTION OF FIC

CERAMIC LAYOUT CONSIDERATIONS

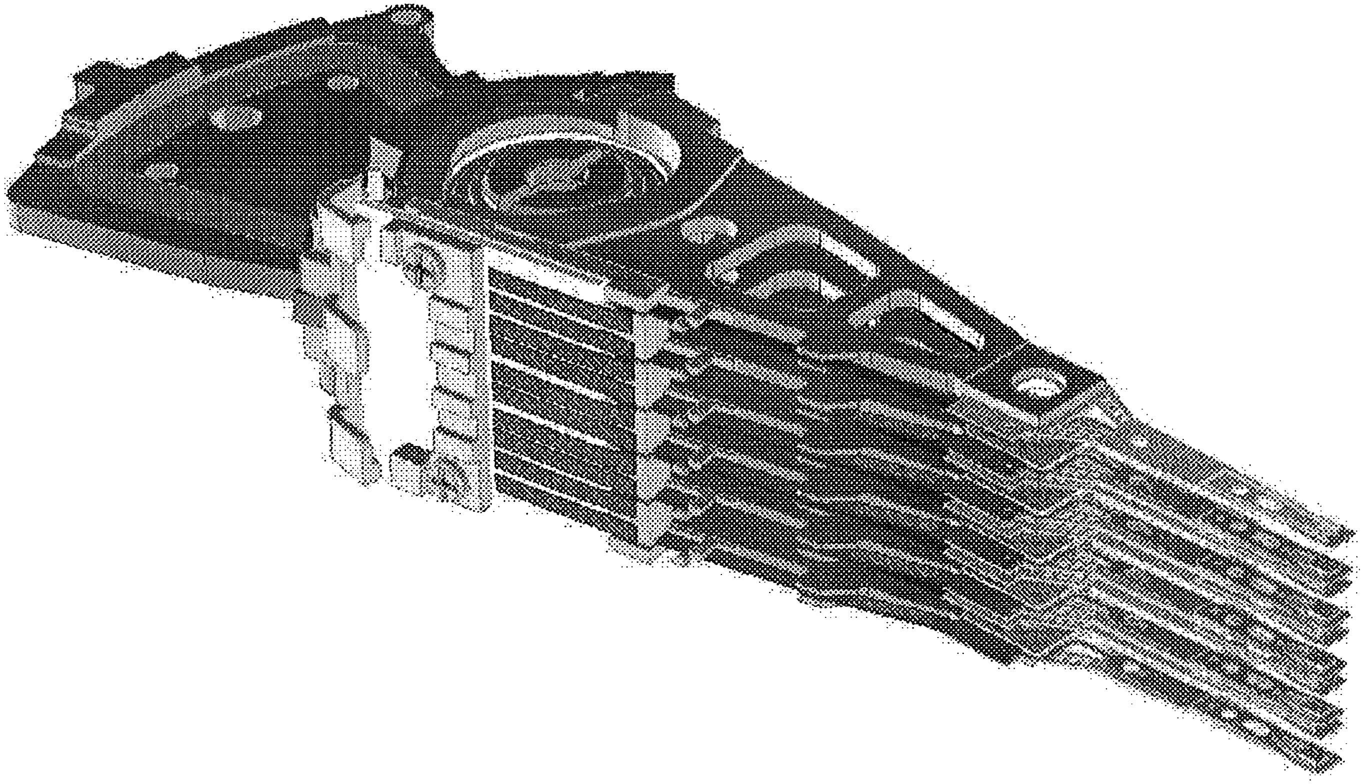
- ALL CAPACITORS SHOULD BE AS CLOSE AS POSSIBLE TO THE DIE
- CLOSEST LOCATION FOR CAPACITORS IN ON DIE SIDE. HOWEVER, NOT ENOUGH ROOM FOR ALL COMPONENTS ON DIE SIDE.
- PROBLEM IS TO MINIMIZE LENGTH TO COMPONENTS WHILE ROUTING LINES THROUGH 6 LAYERS.
- TO MINIMIZE TRACE LENGTHS, WOULD LIKE TO USE ALL 0402 SIZE COMPONENTS. HOWEVER, 0.1μF CAPACITORS ARE AVAILABLE ONLY IN 0602 SIZE.
- WOULD LIKE TO USE THERMAL VIAS FROM THE SUBSTRATE THROUGH ALL LAYERS OF CERAMIC FOR GOOD HEAT TRANSFER. HOWEVER, SUBSTRATE IS AT -3 VOLTS, SO THERMAL VIAS CAN NOT GO THROUGH ALL LAYERS. HEAT SINK ON TOP OF CERAMIC IS TIED TO GROUND

HDA



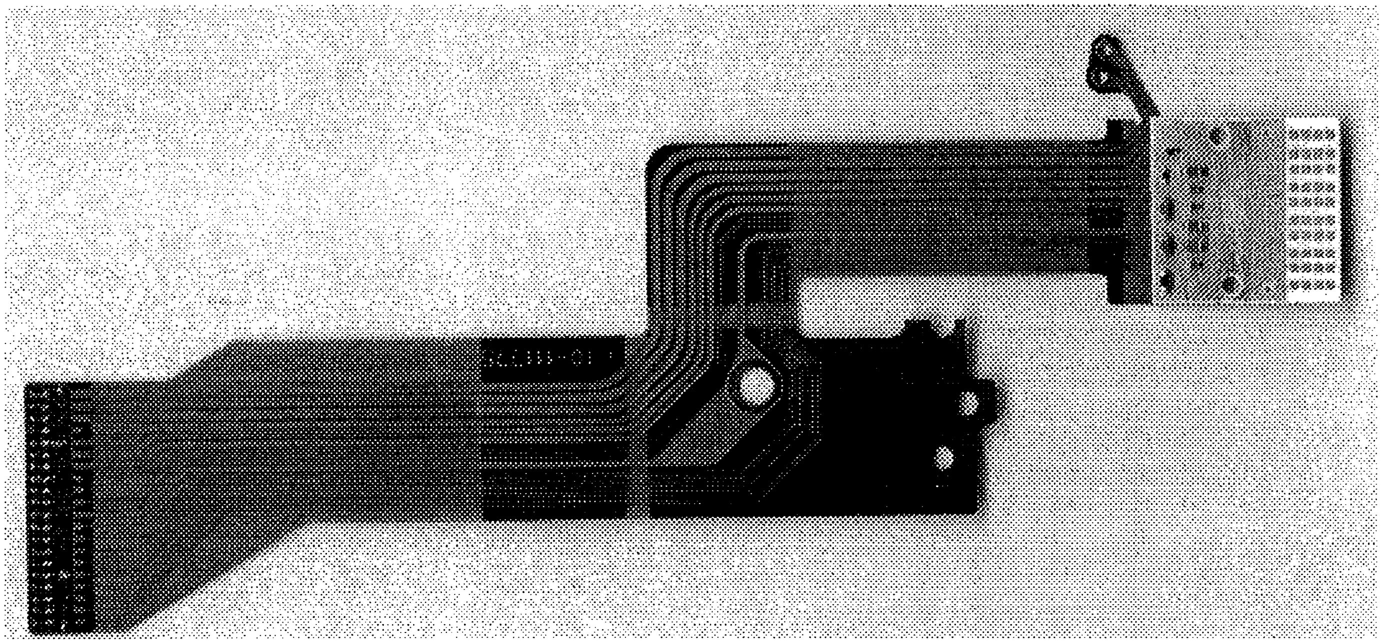
PICTURE OF HDA SHOWING E-BLOCK AND CERAMIC

Head Stack Assembly



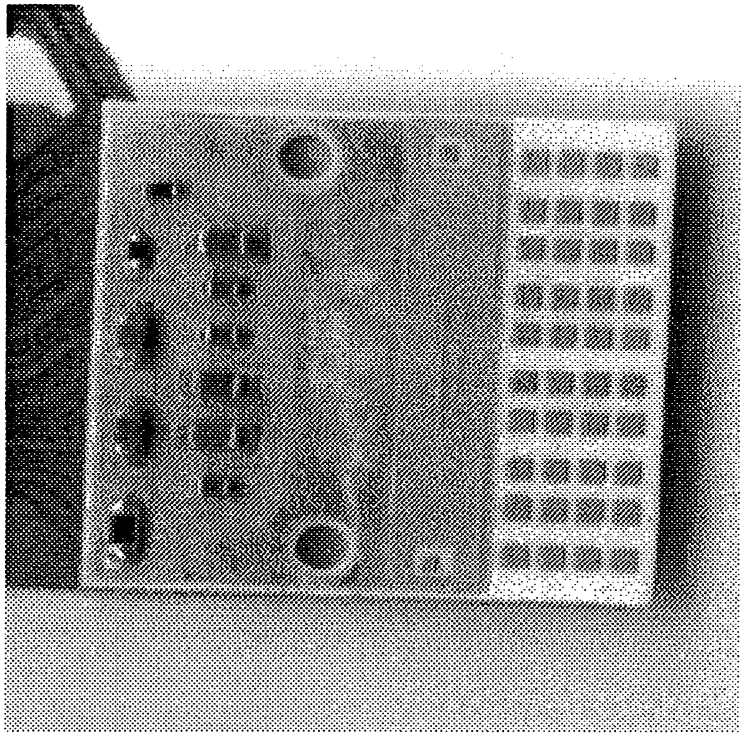
PICTURE OF HEAD STACK ASSEMBLY SHOWING CERAMIC AND FIC

Flex Cable



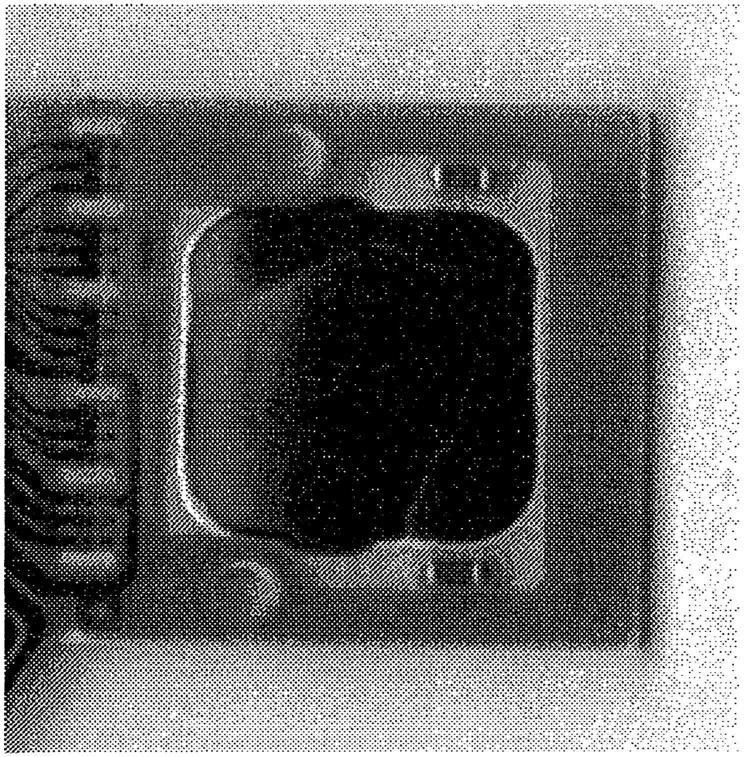
FLEX CABLE AND CERAMIC

10 Channel Ceramic



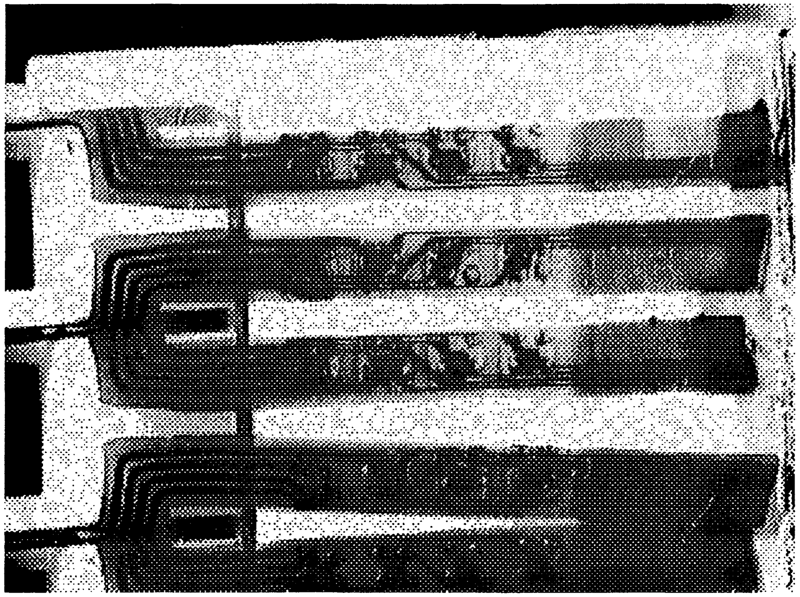
10 CHANNEL CERAMIC, TOP SIDE

10 Channel Ceramic



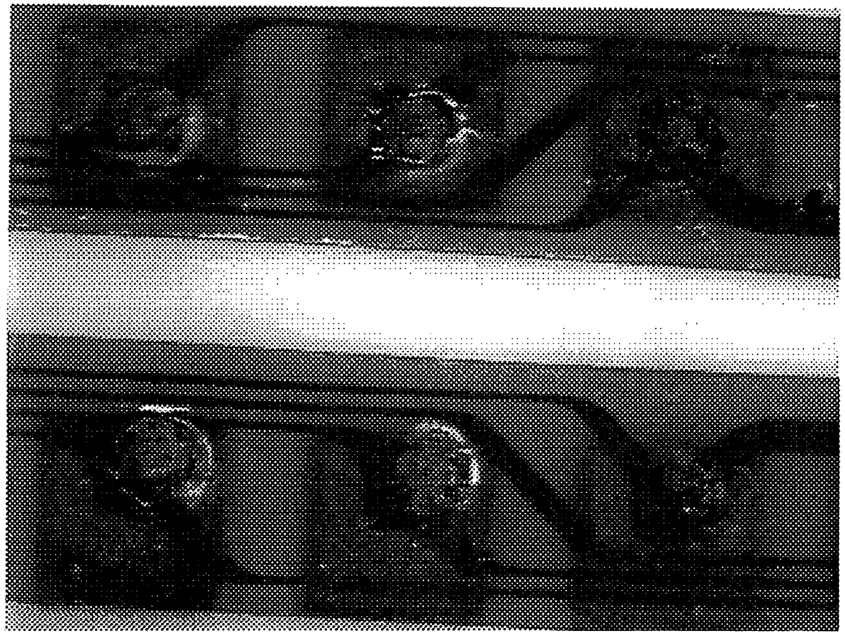
10 CHANNEL CERAMIC, BOTTOM SIDE

FIC Connection

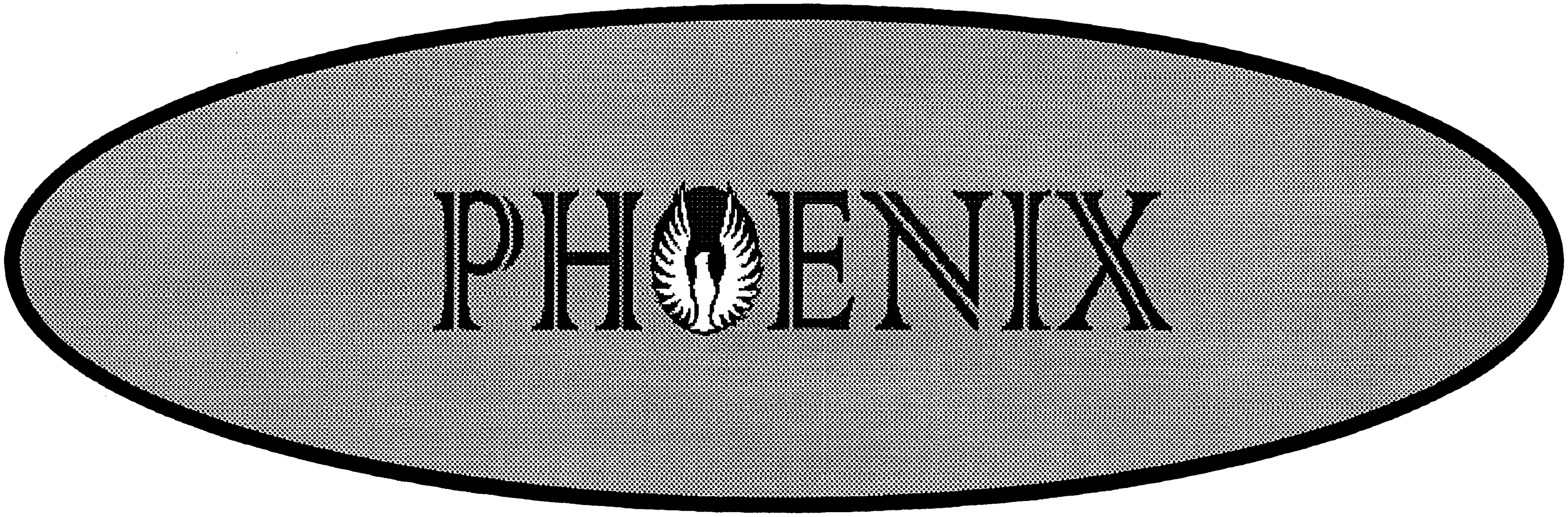


FIC CONNECTION TO CERAMIC

FIC Connection



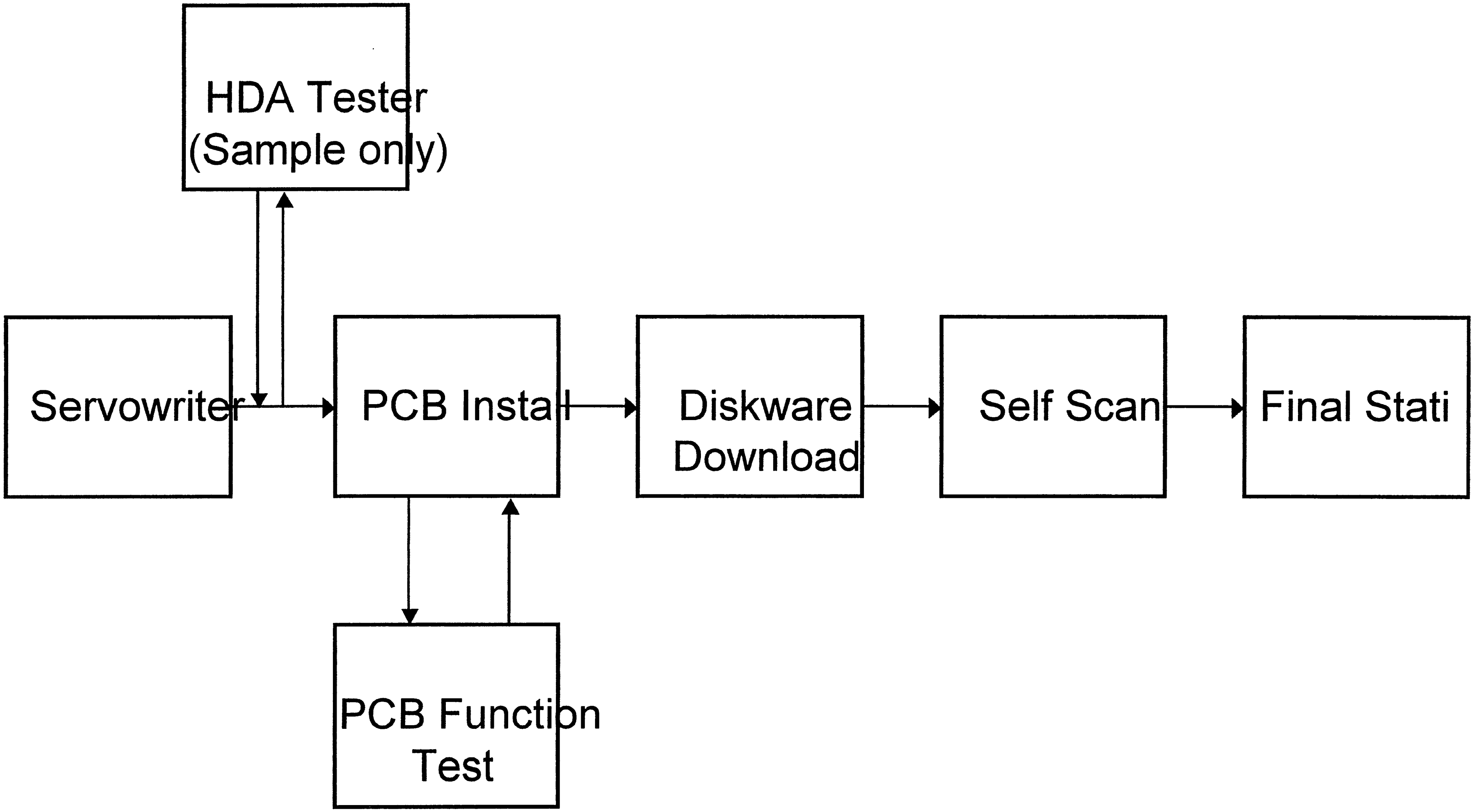
FIC CONNECTION TO HEAD PADS



New Product Training
November 1997

Manufacturing Test Process Section

Mass Pro Test Process Flow


HDA Tester
(Sample only)
Servowriter
PCB Install
Diskware
Download
Self Scan
Final Stati
PCB Function
Test

Servowrite Process

- **Purpose**
  - **Write servo wedges**
  - **Write Serial Number, Component Tracking Code & test info onto HDA**
- **Features**
  - **Laser system for Radial Positioning**
  - **Push pin - follower mirror arm**
  - **3 Head Bank Write, 3/4 (9 gig.) or 1/2 (4 gig.) stagger**
  - **3 pass servowrite (1.5 servo tracks/data track)**
  - **Bursts written with 2T pattern**

Servowrite Process (cont.)

- Test Sequence
  - Load HDA
  - Barcode
  - Initialize System
  - Motor Spinup/Speed
  - Load Clock Head (dynamically)
  - Find OD Crash Stop
  - Measure Stroke
  - Parametric Measurements
  - Write Clock Track - SAM To SAM Check
  - Write 4x Sample Wedges at OD
  - Write Servo Wedges
  - Write 4x Sample Wedges at ID
  - Write HDA S/N,CC, S/W Id, Date/Time
  - Verify Servo Wedges: Sample Cylinders at OD
  - Unload Clock Head
  - Spin Down
  - Unload HDA
  - Generate Test Results

HDA Test Process

- **Purpose**
  - **Obtain Head/Media Parametric Data for Analysis**

- **Features**
  - **Captive PCBA**
  - **LeCroy 7200A Digitizing Oscilloscope**
  - **Uniform Process Test (UPT) based test software**

HDA Test Process (cont.)

- **Test Sequence**
  - **MR Element Resistance Test**
  - **Microjog Cal**
  - **Amp Cal**
  - **HF TAA**
  - **LF TAA**
  - **Resolution**
  - **PW50**
  - **Modulation**
  - **Amplitude Variance Test.**
  - **Amplitude Asymmetry method**
  - **Non Linear Transition Shift (NLTS), instantaneous and average**
  - **Non Linear Transition Shift (NLTS), using 5th harmonic**
  - **Auto Correlation Signal to Noise Ratio (ACSN), instantaneous and average**
  - **Overwrite**
  - **Side Erasure**

PHOENIX

PCB Function Test Process

- **Purpose**
  - **Test functionality of PCBA**
- **Features**
  - **Test through SCSI Interface - Narrow, Wide, SCA, single ended and LDV mode**
  - **Symbios Fast-20 UltraSCSI Adapter**
  - **UPT based**
- **Test Sequence**
  - **Power Up/Detect/Time to Ready (Diskware loaded from the captive HDA)**
  - **buffer memory test**
  - **Fixed length seek test**
  - **FIR channel training test**
  - **2000 - block logical scan**
  - **Jumper / LED test**

Diskware Download Process

- **Purpose**
  - **Load Diskware, Self Scanware, Scripts to Drive**

- **Features**
  - **Uniform Process Test (UPT) based test software**

Diskware Download Process (cont.)

Test Sequence

- Power Up
- Load RAM Ware:
  - - Detect Drive Presence
  - - Load Ramware (Write Buffer)
  - - Initialize NVR
- Load Default Config Pages/Descriptor
- Interrogate Drive
- MR Resistance Check
- Read Super Cylinders (Servo writer Info)
- Prepare System Cylinders:
- Adaptive Equalization:
  - - Microjog Calibration
  - - Input Attenuation
  - - Write Precompensation
  - - Tap 4
  - - Continuous Time Filter
  - - Tap 4
  - - FIR Filter
- Defect Scanning of System Zone
- Initialize File System
- Write Diskware to Disk:
  - - Write Descriptor Table
  - - Write Config Pages
  - - Load Diskware to Disk
- Verify File System
- Load Self Scan Script

Self Scan Process

- **Purpose**
  - **Test Drive functionality, fit for use**
  - **Map out media defects**

- **Features**
  - **Firmware based, script is binary file**
  - **Requires 12V,5V power source only**

PHOENIX

Self Scan Process Sequence

- DRAM Test
- Estimator Error Test
- MR Bias Current Calibration
- Input Attenuation
- Microjog Calibration
- WPC Calibration
- TAP 4 Calibration
- CTF Calibration
- FIR Calibration
- Write BCV
- Servo Wedge Verify
- Scratch Wedge Fill
- Track TMR Test
- Head Stability Test
- Head Offset Test
- Headswitch Test
- Random Seek Test
- Full Stroke Test
- Third Stroke Test
- Wedge to Wedge Scan
- Scratch Fill
- Logical Sequential Scan
- Logical Random Scan
- Sequential Throughput Test
- Random Throughput Test
- Airlock Test

Final Station Process

- **Purpose**
  - **Collect Self Scan test results**
  - **Test Drive through the interface**
- **Features**
  - **UPT Based**

Final Station Process Sequence

- **Servowriter Report**
- **Self Scan Report**
- **Power Cycle Test**
- **Confidence Scan**
- **Full Compare**
- **Configuration**
- **Diskware Version Check**
- **Write Results**