7880

Z80A PROCESSOR CARD

PRELIMINARY

Document #.....

Eng.....Mkt.....

PRO-LOG
CORPORATION

NOTICE

FOREWORD

This manual explains how to use Pro-Log's 7880 Z80A Processor Card. It is structured to reflect the answers to basic questions you, the user, might ask yourself about the 7880. We welcome your suggestions on how we can improve our instructions.

The 7880 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and designed and built with second-sourced parts that are industry standards. They provide an industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports it's products with thorough and complete documentation. Also, we teach courses on how to design with, and use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: Microprocessor User's Guide, and the Series 7000 STD BUS Technical Manual. If you would like a copy of these documents, please write to us on your company letterhead.

Contents

Figures

The 7880 provides a buffered and fully expandable 4 MHz, Z80A Microprocessor with onboard memory (ROM and/or RAM) and a 10 ms. timer. It is designed for maximum cost effectiveness and reliability.

The memory consists of sockets for 2K RAM and 4K EPROM. The memory is suitable for small dedicated control programs, or to bootstrap microprocessor systems using mass storage devices.

The timer has a fixed duration of 10ms. It is suitable as a background timer, or a debouncer for mechanical switches, and other such devices.

The 7880 allows DMA control to other cards, and is compatible with all Z80 interrupt modes.

Main Features of the 7880 are:

- **Z80A Processor**
- **Crystal controlled 250 µs clock**
- **Socket for 2K byte wide RAM**
- **Socket for 4K EPROM**
- **10 ms. timer**
- **Compatible with all Z80 interrupt modes**
- **DMA capability to external memory**
- **Bootstrap capability**
- **MEMEX control**
- **Capable of addressing 128K bytes of memory**
- **Single +5V operation**

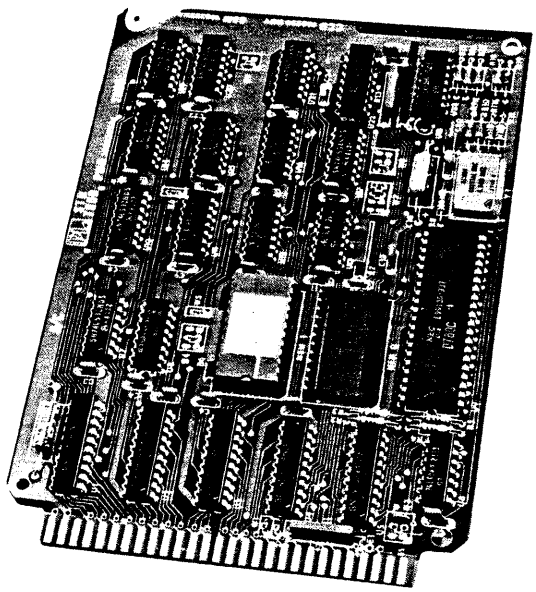


Figure 1-1. 7880 Z80A Processor Card.

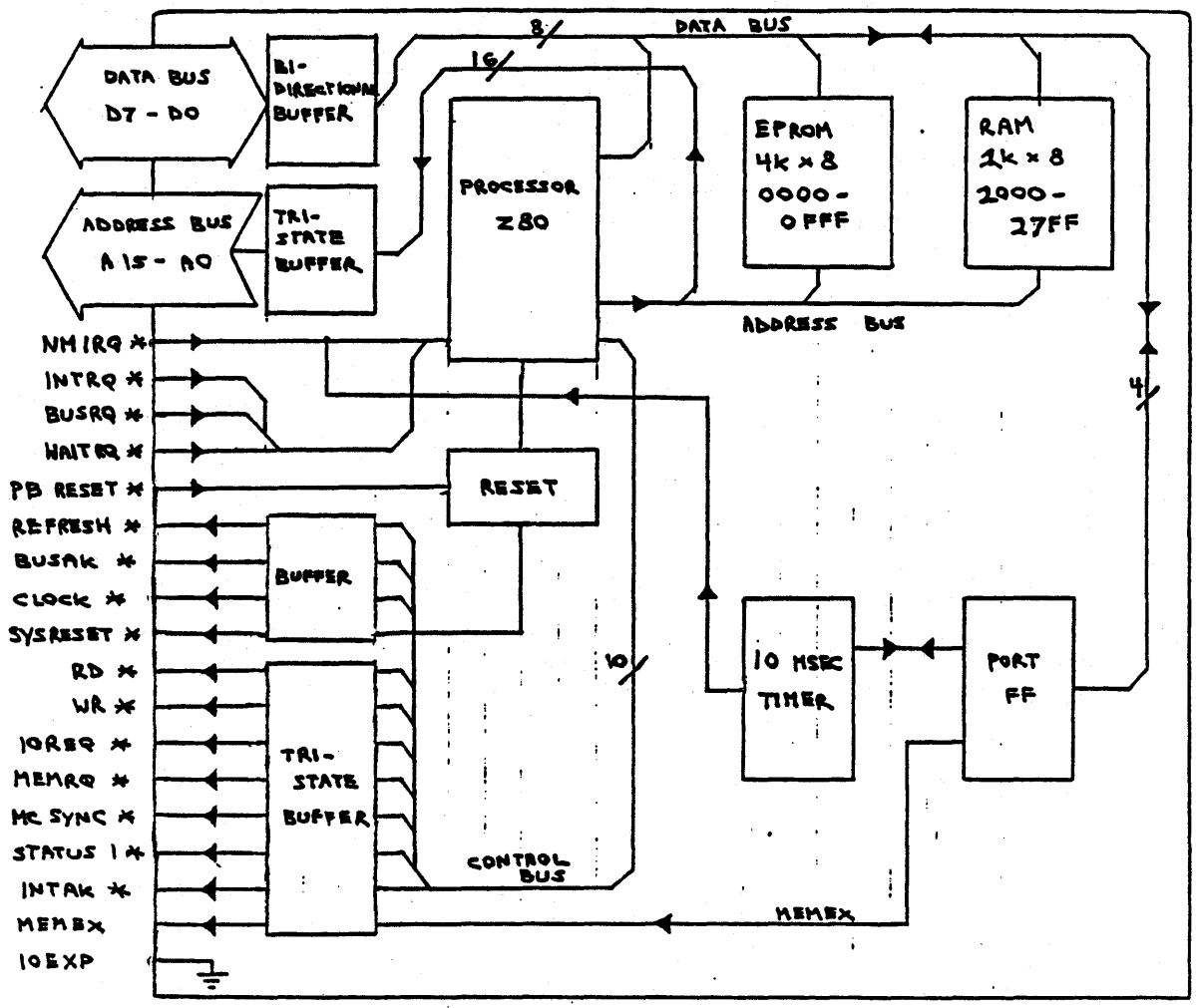


Figure 1-2. 7880 Block Diagram.

Introduction

The 7880 operates as part of an STD BUS system. You can plug it directly into the STD BUS backplane, See Fig. 2-1, or extend it from the motherboard with a 7901 card extender.

It can be plugged directly into any slot in the rack. If the extender card is used, plug the extender card in any slot and plug the 7880 into the connector on the card extender. This makes the 7880 accessible for testing.

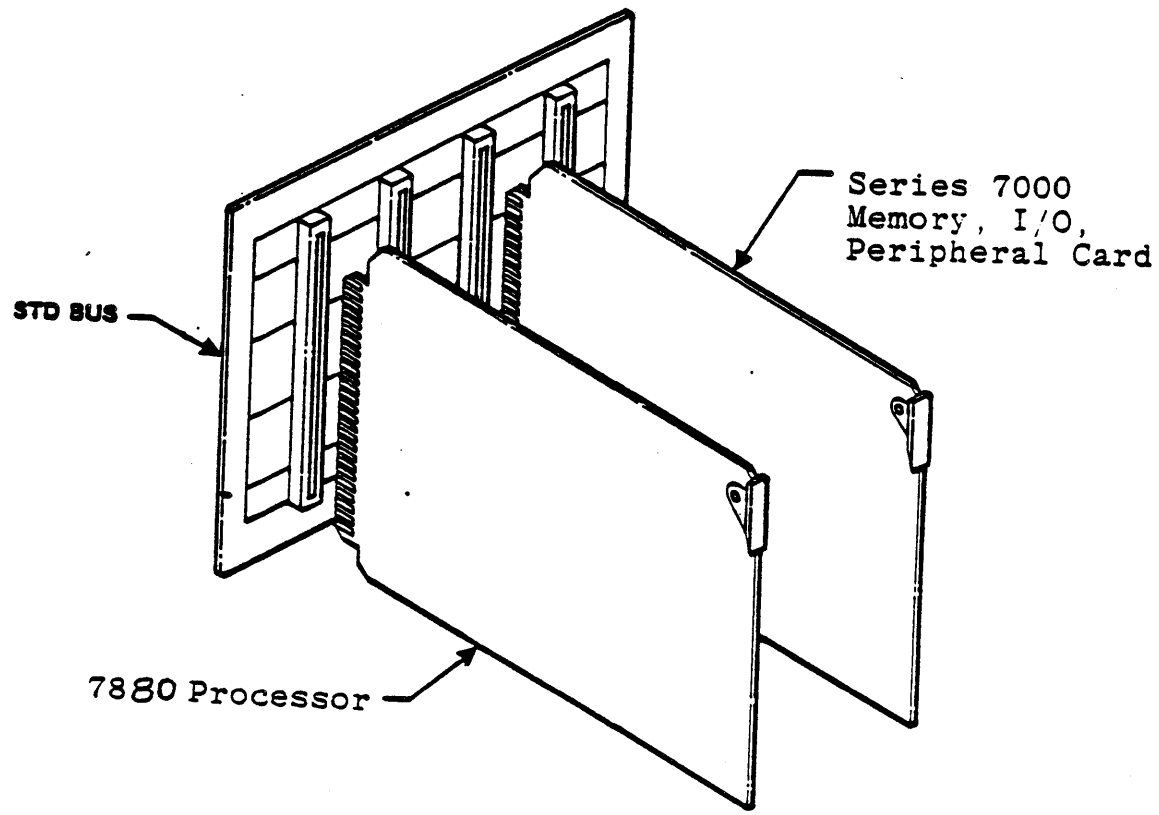


Figure 2-1. Installation of the 7880 Card in STD BUS Card Rack.

Wire Jumper Options

The 7880 has nine options which are selectable by wire jumpers. W1 determines whether the IOEXP line will be grounded or externally controlled. W2 determines whether the MEMEX line is internally or externally controlled. W3 determines whether the timer will control the maskable or non-maskable interrupt or if it will be disabled. W4 controls whether the onboard RAM will be disabled or at which address it will reside. W5 controls whether the onboard ROM will be enabled or disabled. W6 determines if the onboard port will be enable or disabled. W7 determines the address of the onboard port. W8 determines whether MEMEX will be high active or low active or permanently grounded for onboard memory. W9 determines whether onboard MEMEX control will be high or low after reset.

Note: See Fig. 2-4, Physical Location of Main Features of the 7880, for actual location of the above mentioned WX jumpers.

This section reviews the wire jumper options. Check to be sure the card is configured for your application before installing it in your system. When changing wire jumpers, first cut the jumper in half, then remove it one half at a time. This prevents damage to the solder pads. Remove any excess solder and install a new jumper where required.

If you anticipate changing the wire jumpers frequently, as for prototyping, the wire jumpers can be replaced with slip-on connectors. Permanent 0.025 in. square posts can be installed which accept the slip-on connectors. Two sources for the connectors and headers are shown in Fig. 2-2.

Part	Manufacturer Part Number	
	Elco Corp.	Berg Electronics
2 Pin Header	00 8261 02 32 00 852	65611-102
4 Pin Header	00 8261 04 32 00 852	65611-104
6 Pin Header	00 8261 06 32 00 852	65611-106
8 Pin Header	00 8261 08 32 00 852	65611-108
Connector	00 8261 02 42 00 870	

Figure 2-2. 7880 Wire Jumper Replacements for the 7880.

Memory Mapping

The 7880 comes with a socket for a 2K byte RAM and a socket for a 4K byte EPROM, see Fig. 2-4.

The type of EPROM to be used is a 2732A or equivalent. Be sure the memory part you use has an access time of 250 ns. or less. See Fig. 2-3 for recommended memory devices.

The EPROM socket, soocket 0, is mapped at addresses 0000-0FFF. It cannot be remapped to any other location. It can, however, be disabled. To do this, remove jumper W5. See Fig. 2-4

This will enable the 7880 to access memory on other cards in the system over the address range of the EPROM socket.

The RAM is mapped at addresses 2000-27FF. It can be remapped to addresses 1000-17FF or 3000-37FF. To do this, remove jumper W-4 from position 3-4, see Fig. 2-4, and install a jumper in position 1-2 or 5-6. A jumper at position 1-2 maps the RAM to addresses 1000-17FF. A jumper at position 5-6 maps the RAM to addresses 3000-37FF. Memory on other cards in the system can be mapped to any address not occupied by onboard memory.

As with the EPROM socket, the onboard RAM can be disabled. To do this, remove the jumper W4 altogether.

Memory Types

The 7880 can use two different kinds of memory, 2K RAMs and 4K EPROMs. Fig. 2-3 is a list of components which are recommended for use on the 7880 card. If you wish to use other memory components, compare their data sheets to the socket configurations. Also check their data sheets for any special requirements, and be sure they have an access time no greater than 250 ns.

Type	Part Number	Manufacturer
2K RAM	M48725P	Mitsubishi
2K RAM	MSM2128	OKI
2K RAM	TMM2016	Toshiba
2K RAM	µPD446	NEC
2K RAM	µPD447	NEC
2K RAM	21812	Intel
4K EPROM	2732A	Intel

Figure 2-3. Recommended Memory Devices for 7880.

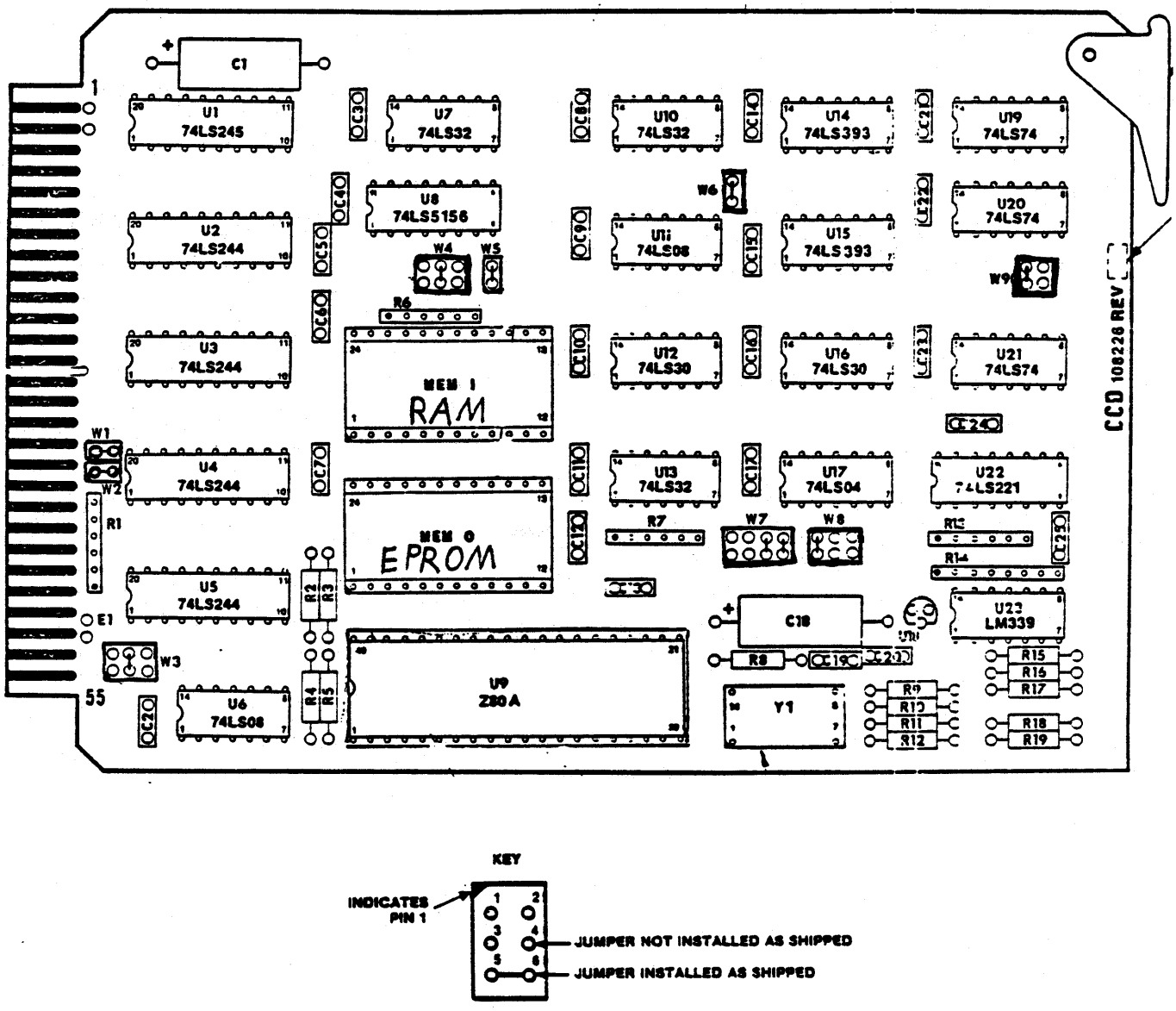


Figure 2-4. Physical Location of Main Features of the 7880.

MEMEX

The MEMEX line is a part of the STD BUS. It is used as a memory bank select line. It is possible to have two banks of memory, each with up to 64K bytes, in a system. One bank would be enabled when MEMEX is high, and the other when MEMEX is low. Pro-Log memory cards include the MEMEX line in their address decoding.

There are several wire jumper options affecting MEMEX. The first is MEMEX affecting onboard memory. Onboard memory can either be enabled when MEMEX is high or when it is low, or it can be permanently enabled regardless of MEMEX. Jumper W8, see Fig. 2-4, determines how MEMEX affects onboard memory. As shipped, the jumper is in position 1-2. In this position, onboard memory is enabled when MEMEX is low. If the jumper is replaced with one at position 3-4, onboard memory will be enabled when MEMEX is high. If the jumper is replaced by one at position 5-6, the onboard memory will be permanently enabled, regardless of the logic state of the MEMEX line.

Jumper W9 determines the state of the MEMEX line after reset. As shiped, the jumper is in position 1-2. This causes MEMEX to be in the low state after reset. Removing the jumper from position 1-2 and placing a jumper in position 3-4 will cause the MEMEX line to be high after reset. It also causes the output of the MEMEX control port to be inverting.

Removing jumper W2 will relinquish control of the MEMEX line from the 7880 to some other card in the system.

IOEXP

The IOEXP line is one of the STD BUS standard signals. It is typically used to select between different banks of input and output ports. The 7880 does not control the IOEXP line. IOEXP is tied to ground on the 7880 through jumper W1. If another card needs to control the IOEXP line, jumper W1 can be removed. This will leave the line floating and allow some other card in the system to control the IOEXP line.

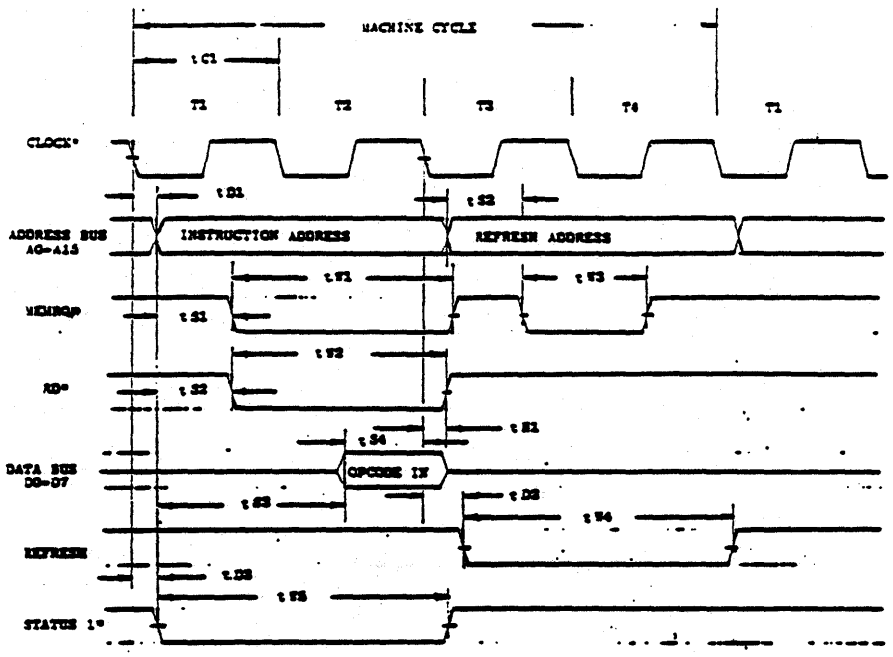
Interrupt and Counter Control Port

The onboard 10 ms. counter is capable of controlling either the maskable or non-maskable interrupt lines on the Z80A processor chip. The interrupt and counter control port is mapped at address FE. By removing jumpers 5-6 and 7-8 and adding jumpers 1-2 and 3-4 on W7, it is possible to change the address of the interrupt and counter control port to 7F. It is possible to disable the onboard interrupt and counter control port altogether by removing jumper W6.

It is possible to select which interrupt line, either the maskable or non-maskable. will be affected by the Interrupt and Counter Control Port. As shipped, the counter will strobe the processor's NMI* input. Removing jumper 3-4 and adding jumper 5-6 on W3 will relinquish control of the processor's NMI interrupt line to external sources outside of the 7880. If the counter is connected to the NMI* input of the processor, the input from the STD BUS NMIRQ* should not be used.

Timing Specifications

Figures 2-5 through 2-12 show the signal sequences and timing for various 7880 functions. They show the signals as they appear at the card edge connector of the 7880.

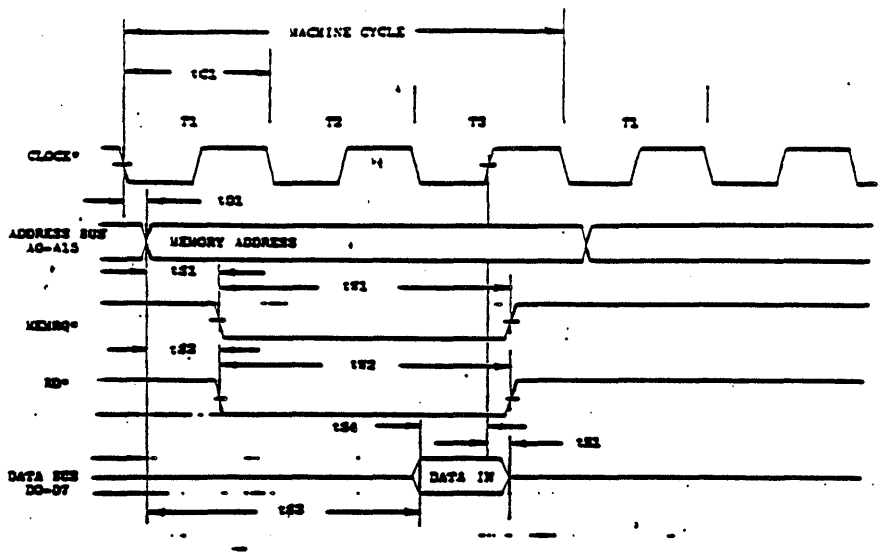


SYMBOL	PARAMETER	4 MHz MIN	MAX
tC1	Clock Cycle Time	250	
tD1	Address delay from T1 clock		110
tD2	REFRESH* delay from start of T3		130
tD3	STATUS 1* delay from T1 clock		100
tS1	Address setup before MEMRQ* active	65	
tS2	Address setup before RD* active	125	
tS3	Address setup before DATA valid	295	
tS4	Data Bus setup before T2 clock ends	70	
tH1	Data Bus hold time after T2	0	
tW1	MEMRQ* pulse width (OPCODE FETCH)	290	
tW2	RD* pulse width	280	
tW3	MEMRQ* pulse width (REFRESH)	220	
tW4	REFRESH* pulse width	370	
tW5	STATUS 1* pulse width	400	

All times given in nanoseconds

OPCODE FETCH TIMING, REFRESH TIMING

Figure 2-5. Opcode Fetch Timing, Refresh Timing for 7880.



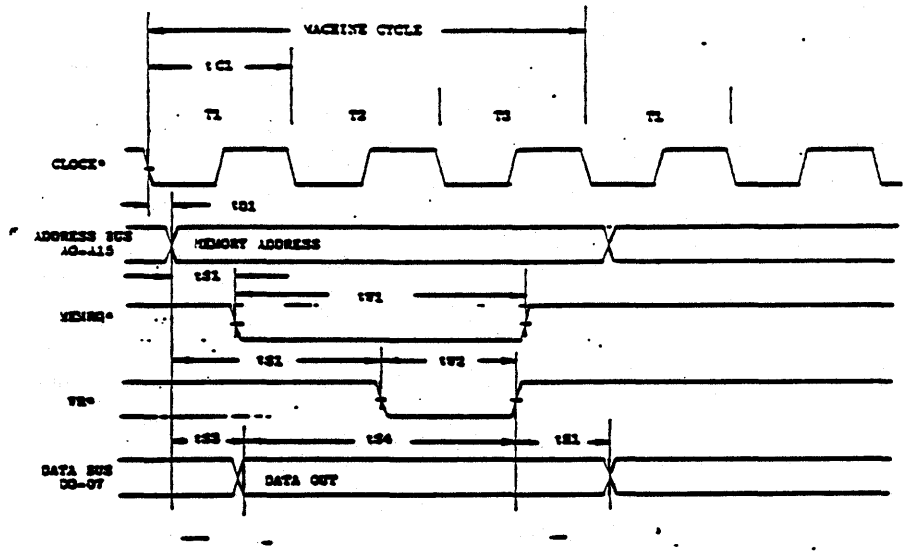
4.0 MHz

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock Cycle Time	250	
tD1	Address delay from T1 clock		110
tH1	Data hold time after clock high	0	
tS1	Address setup before MEMRQ* active	75	
tS2	Address setup before RD* active	110	
tS3	Address setup before DATA valid	430	
tS4	Data setup time before clock high	90	
tW1	MEMRQ* pulse width	415	
tW2	RD* pulse width	405	

All times given in nanoseconds

MEMORY READ TIMING OTHER THAN OPCODE FETCH

Figure 2-6. 7880 Memory Read Timing Other than Opcode Fetch.



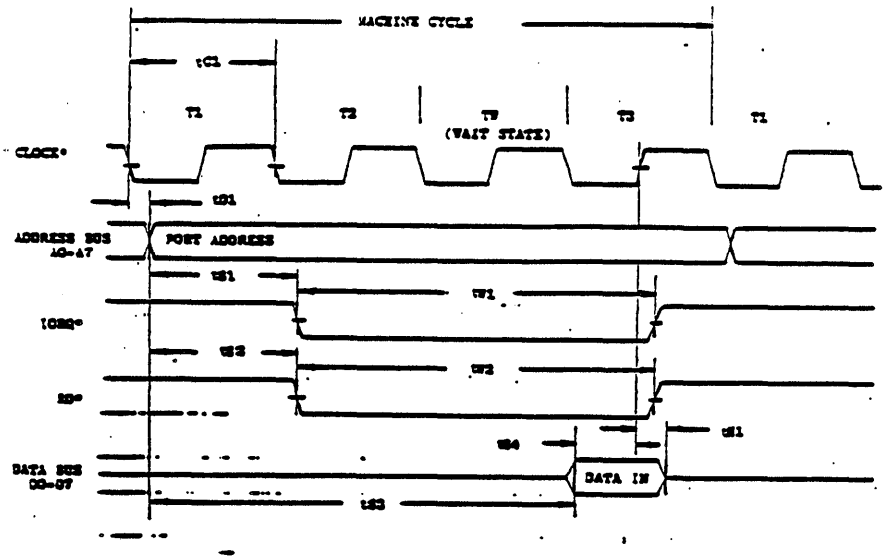
4.0 MHz

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock cycle time	250	
tD1	Address delay from T1 clock		110
tH1	Data hold time after WR* ends	60	
tS1	Address setup before MEMRQ* active	65	
tS2	Address setup before WR* active	240	
tS3	Address setup before data valid	175	
tS4	Data setup time before WR* ends	300	
tW1	MEMRQ* pulse width	415	
tW2	WR* pulse width	220	

All times given in nanoseconds

WRITE TIMING

Figure 2-7. 7880 Write Timing.



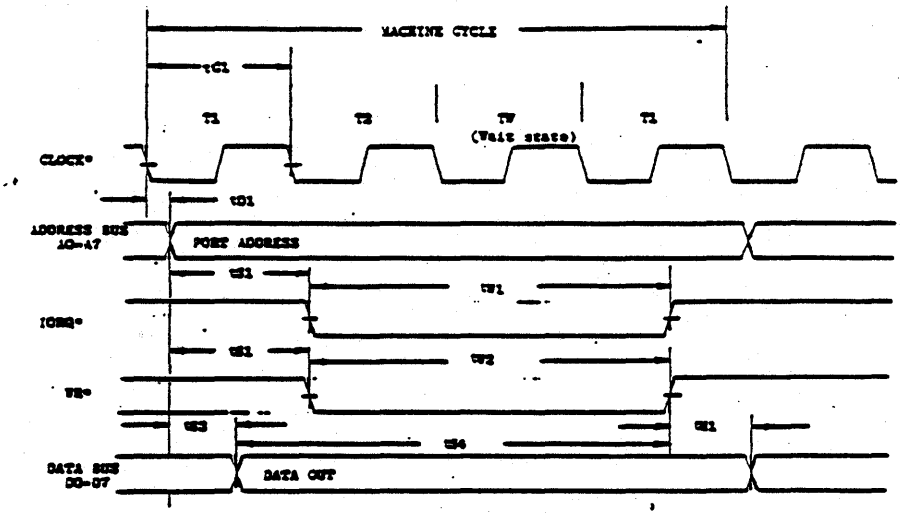
4.0 MHZ

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock Cycle Time	250	
tD1	Address delay from T1		110
tH1	DATA hold time after clock	0	
tS1	Address setup before IORQ* active	180	
tS2	Address setup before RD* active	190	
tS3	Address setup before DATA valid	600	
tS4	Data setup time before clock high	70	
tW1	IORQ* pulse width	540	
tW2	RD* pulse width	540	

All times given in nanoseconds

INPUT TIMING

Figure 2-8. 7880 Input Timing.



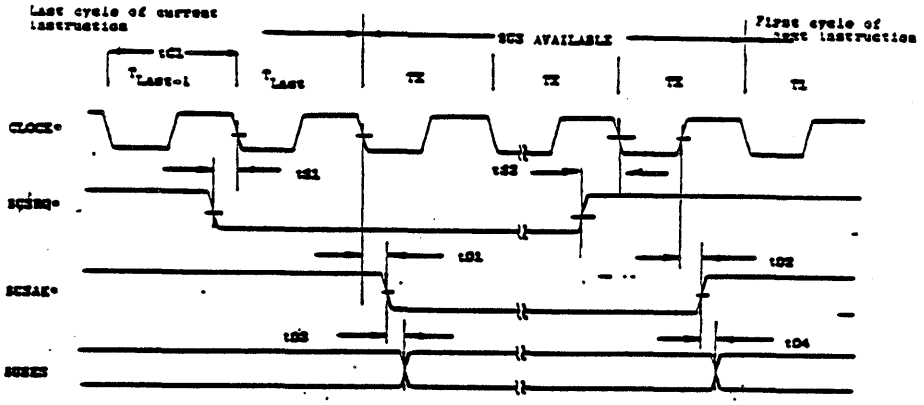
4.0 MHz

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock Cycle time	250	
tD1	Address delay from T1 clock		110
tH1	Data hold time after WR* ends	0	
tS1	Address setup before IORQ* active	180	
tS2	Address setup before WR* active	205	
tS3	Address setup before DATA valid	700	
tS4	Data setup time before WR* ends	735	
tW1	IORQ* pulse width	540	
tW2	WR* pulse width	545	

All times given in nanoseconds

OUTPUT TIMING

Figure 2-9. 7880 Output Timing.



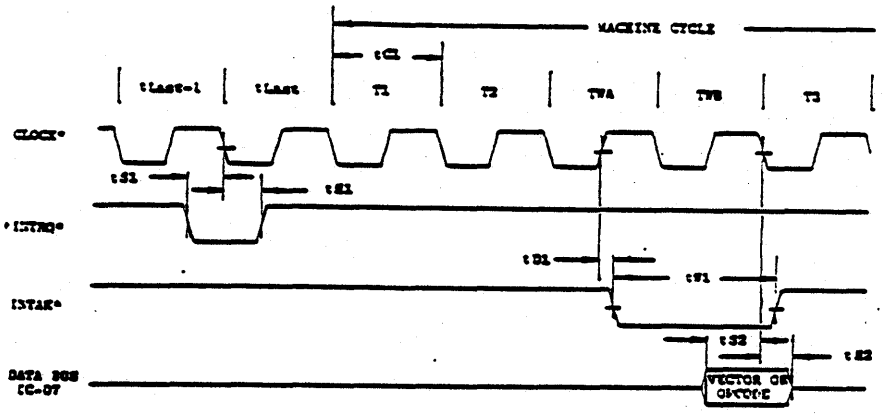
4.0 MHz

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock Cycle Time	250	
tD1	BUSAK* delay after start of first DMA cycle		120
tD2	BUSAK* delay after last DMA cycle		120
tD3	Buses delay after BUSAK* active		20
tD4	Buses delay after BUSAK* inactive		20
tS1	BUSRQ* setup prior to last time state	70	
tS2	BUSRQ* release prior to sample	70	

All times given in nanoseconds

BUS REQUEST TIMING

Figure 2-10. 7880 Bus Request Timing.



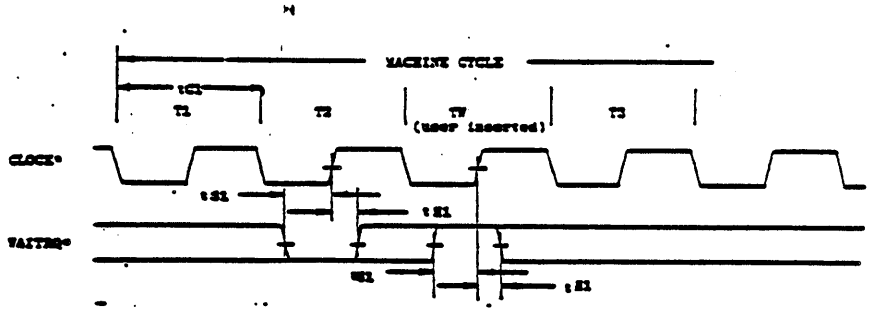
4.0 MHz

SYMBOL	PARAMETER	MIN	MAX
tC1	Clock Cycle Time	250	
tH1	INTRQ* hold time after clock low	0	
tH2	DATA BUS hold after clock low	0	
tS1	INTRQ* setup prior to last time state	100	
tS2	Data Bus setup before clock low	75	
tD1	INTAK* delay after clock high		105
tW1	INTAK* pulse width	290	

All times given in nanoseconds

INTERRUPT REQUEST TIMING

Figure 2-11. 7880 Interrupt Request Timing.



SYMBOL	PARAMETER	4.0 MHz MIN	MAX
tC1	Clock Cycle Time	250	
tH1	WAITRQ* hold after clock high	0	
tS1	WAITRQ* setup before clock high	90	

All times given in nanoseconds

WAIT STATE TIMING

Figure 2-12. 7880 Wait State Timing.

Specifications

Figure 2-13 shows the electrical specifications for the 7880. Environmental and power specifications are shown in Figures 2-14 and 2-15. Figure 2-16 gives the pinout and electrical characteristics of the connection between 7880 and the STD BUS.

MNEM.	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
V_{CC}	Supply Voltage	4.75	5.00	5.25	0	5.50	Volts

Figure 2-13. 7880 Electrical Specifications.

		Recommended Operating Limits			Absolute Non-Operating Limits		
MNEM.	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
-	Free Air Temp.	0	+25	+55	-40	+75	°C
-	Humidity	5	95[1]*	5	95[1]*	%RM	

1* Non-condensing

Figure 2-14. Environmental Specifications.

MNEM.	PARAMETER	MIN	TYP	MAX	UNITS
I_{CC}	V_{CC} Supply Current		500	850	milliAmps

Figure 2-15. Electrical Specifications Over Operating Range.

Mechanical Specifications

The 7880 card conforms to all STD BUS mechanical standards.

PIN NUMBER	OUTPUT LSTTL DRIVE	INPUT (LSTTL LOADS)	MNEMONIC		PIN NUMBER	OUTPUT LSTTL DRIVE	INPUT (LSTTL LOADS)	MNEMONIC
2		IN	+5 VOLTS		1		IN	+5 VOLTS
4		IN	GROUND		3		IN	GROUND
6			-5 VOLTS		5			-5 VOLTS
8	50	1	D7		7	50	1	D3
10	50	1	D6		9	50	1	D2
12	50	1	D5		11	50	1	D1
14	50	1	D4		13	50	1	D0
16	50		A15		15	50		A7
18	50		A14		17	50		A6
20	50		A13		19	50		A5
22	50		A12		21	50		A4
24	50		A11		23	50		A3
26	50		A10		25	50		A2
28	50		A9		27	50		A1
30	50		A8		29	50		A0
32	50		RD*		31	50		WR*
34	50		MEMRQ*		33	50		IORQ*
36	50		MEMEX		35	GND		IOEXP
38	50		MCSYNC*		37	50		REFRESH*
40			STATUS 0*		39	50		STATUS 1*
42		5[1]	BUSRQ*		41	50		BUSAK*
44		5[1]	INTRQ*		43	50		INTAK*
46		5[1]	NMIRQ*		45		5[1]	WAITRQ*
48		[2]	PBRESET*		47	50		SYSRESET*
50			CNTRL*		49	50		CLOCK*
52		IN	PCI		51	OUT		PCO
54			AUX GND		53			AUX GND
56			AUX -V		55			AUX +V

[1] DRIVE WITH OPEN COLLECTOR
[2] DRIVE WITH PUSHBUTTON

Figure 2-16. STD/7780 Edge Connector Pin List.

This section explains the operation and programmable functions of the 7880 card. These programmable functions are controlled by the onboard I/O port.

Bootstrap

The onboard memory can be used to bootstrap up systems using disc or other mass storage devices. The MEMEX line is used to facilitate this.

Fig. 3-1 shows a system with 70K of memory. In this figure, the onboard memory of the 7880 consists of 4K of ROM and 2K of RAM. The additional 64K is RAM, and is on four Pro-Log 7704 memory cards. The memory on the 7880 is enabled when MEMEX is low. The RAM on the 7704 card addressed at 0000-3FFF is enabled when MEMEX is high. The memory on the other 7704 cards is permanently enabled. When the system is first powered-up, the MEMEX port output is low and the processor reads the program in ROM on the 7880. The program would direct the processor to read in a control program off a disc or other storage device. The control program would be loaded into RAM in the upper addresses. It would reside, for instance, in the upper address range of the 7704 card addressed at 0000-FFFF. Now the processor jumps to the control program in RAM. The control program directs the processor to set the MEMEX control port high. This disables the memory on the 7880, and enables the 7704 card mapped at 0000-3FFF. The processor is now working with 64K of RAM.

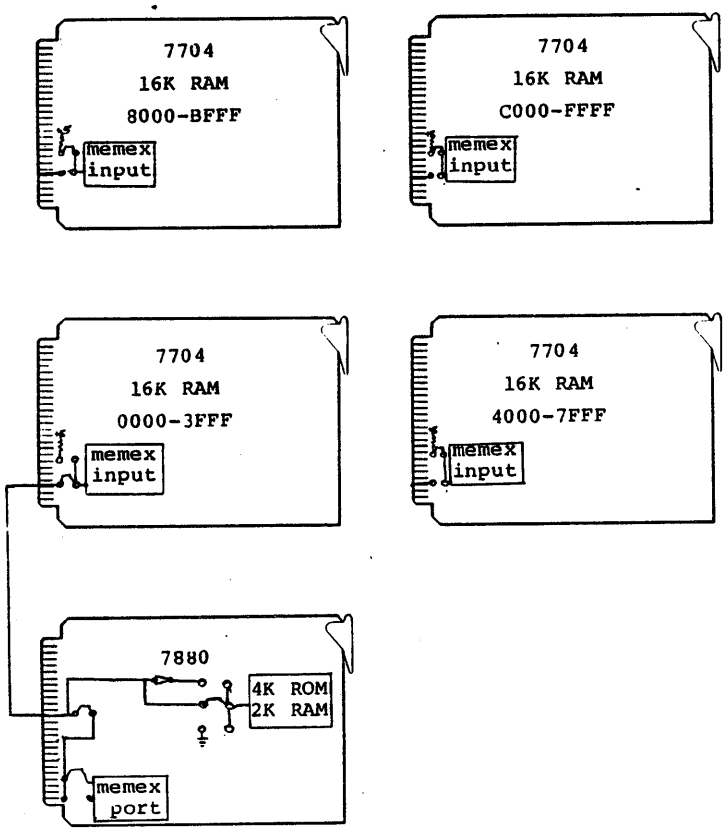


Figure 3-1. Bootstrap Example.

Direct Memory Access

Direct memory access, or DMA, is a function whereby another controller in the system can request that the processor release the address, data, and control busses, and allow the external controller direct access to memory. The 7880 features this option, however, access to onboard memory is not possible.

To perform a DMA the external device must generate the STD BUS signal BUSRQ*. Fig. 2-10 shows the timing of the signals involved in the DMA operation. The Z80A samples the BUSRQ* line at the start of the last time state of any machine cycle. It will respond by generating the signal BUSAK* and releasing the bus at the start of the next time state. BUSAK* is also an STD BUS signal and can be sampled by the external controller to determine when the bus is available.

The processor stays inactive until BUSRQ* goes high and the bus will return to normal during the first time state that BUSRQ* is found high. The processor resumes where it left off during the next time state.

During DMA operations, no interrupts can be acknowledged, and will only be serviced when the processor returns to normal operation.

Controlling the Interrupt and Counter Control Port

The interrupt and counter control port is addressed at FE. (See Section 2 for instructions on changing port FE address to 7F). Only the least significant nibble is relevant to the controls affecting the 7880. The most significant nibble is not used.

Bit 0 of the interrupt and counter control port controls the MEMEX line. Bit 1 pertains to the interrupt latch. This latch is set by the output of the counter and is controlled by bit 1. A latch is necessary to drive INT* because the counter output is active for 250 ns., which is too fast to be read by the processor, or the processor may be too busy to respond to the interrupt immediately. This latch can be reset by writing a 0 to that bit location and should be reset programmatically after the processor has determined the source of an interrupt.

Bit 2 controls the mask gate. When set, either the interrupt latch is enabled to drive the processor's interrupt request, or the output of the counter is enabled to drive the processor's NMI* input, depending on the position of jumper W3. This jumper option is explained in Section 2. The mask must be disabled by the program after power-on or reset, or the timer will not be able to generate an interrupt. Bit 3 restarts the counter any time through software.

The status port is an input port addressed at FE (see Section 2 for instructions on changing port address to 7F). It is used to monitor the status of the output port latches. Bit 0 is used to read the state of the MEMEX line. Bit 1 is used to read the status of the interrupt latch after an interrupt request, to see if the interrupt was caused by the timer or by an external INTRQ*, when the timer is jumpered to INT* on the processor. Bit 2 is used to read the state of the mask gate.

When setting up the timer, special care should be taken to follow the correct sequence of events. If the timer is connected to the NMI* pin, as it is when it si shipped, the timer should be restarted and then as a second step the interrupt mask should be removed. If the timer is connected to the INTRQ* pin, the timer should be restarted, the interrupt latch cleared, and the interrupt mask removed all at once. This can be accomplished by writing an OE to the onboard interrupt and timer control port.

The 10 ms. Duration Timer

The 10ms duration timer is driven by the same 4 MHz clock that drives the Z80A processor. The 4 MHz clock has an accuracy of +0.00% - 0.02%. At power-on, the counter starts counting from zero and counts up to some terminal count 10 ms. later. Every 10 ms a 250 ns pulse is generated which resets the counter and sets the interrupt latch. On the next clock cycle, the counter starts counting from zero again.

The counter can be halted and restarted by writing out bit 3 to the Interrupt and Counter Control Port FE.

Some of the uses of the timer might as a means of time interval measurement. It can be used as a very precise timed interrupt or a one-shot simulator with software triggering.

The timer consists of four cascaded binary counters constituting the 16 bit counter. The outputs of the counter are gated through to a flip-flop U21 along with the system clock. The Q side of the flip-flop is the 250 ns pulse output. The pulse is latched by the interrupt latch in the Interrupt and Counter Control Port. The condition of the latch can then be read back by the Status Port U5.

Power-On and Push-Button Reset

Power-on reset holds the SYSRESET* line low and releases it a maximum of 40 ms after Vcc reaches 4.75V. The PBRESET* is debounced approximately 20 ms, and produces a maximum 40 ¢s SYSRESET* pulse. The push-button reset is triggered off the Z80A processor chip's M1* output. This is done to avoid disturbing refresh cycle timing to dynamic RAM. Should M1* fail to occur, the one-shot U22 will time out and produce the RST* signal about 300 ¢s later.

SECTION 4
Operating Software

This section contains hardware level subroutine module examples that will work with the 7880. The software in this section can be used without license from Pro-Log. Although believed to be correct, this software is not represented to be free from errors or copyright infringement, or appropriate for any particular application.

The subroutines are in STD instruction mnemonics. The coding forms are grouped at the end of this section, following the flowchart.

Software Example

The 7880 timer can be used as an interrupt timer. The following software example, Fig. 4-1 and 4-2, demonstrate how the 7880 can perform such a function. It is intended only as an example. The exits in the example indicate that the processor can jump to some other location enabling it to continue performing other functions. It is beyond the scope of this manual to develop a program so involved. However, the example is intended to spark the creativity of the user. It consists of 2 subroutines, one is a preliminary timer set-up, the other consists of instructions for when the processor receives an interrupt.

The program begins setting up the timer by loading Register C with a predetermined delay count. Then the timer is restarted by loading an 08 to the accumulator and outputting it to port FE. Next, the interrupt mask is removed by loading the accumulator with an 04 and sending it to port FE. At that point, the first subroutine exits and the processor is free to go back to program memory and continue doing whatever it was doing before. The second subroutine is a time check. It is initiated when the processor receives a non-maskable interrupt. It starts out by decrementing Register C where the delay count is stored. It then checks if the count is zero, if not, the subroutine exits and the processor is again free to perform another function. If the count is equal to zero, the processor services the interrupt and then the time is reloaded again. At this point, the second subroutine exits.

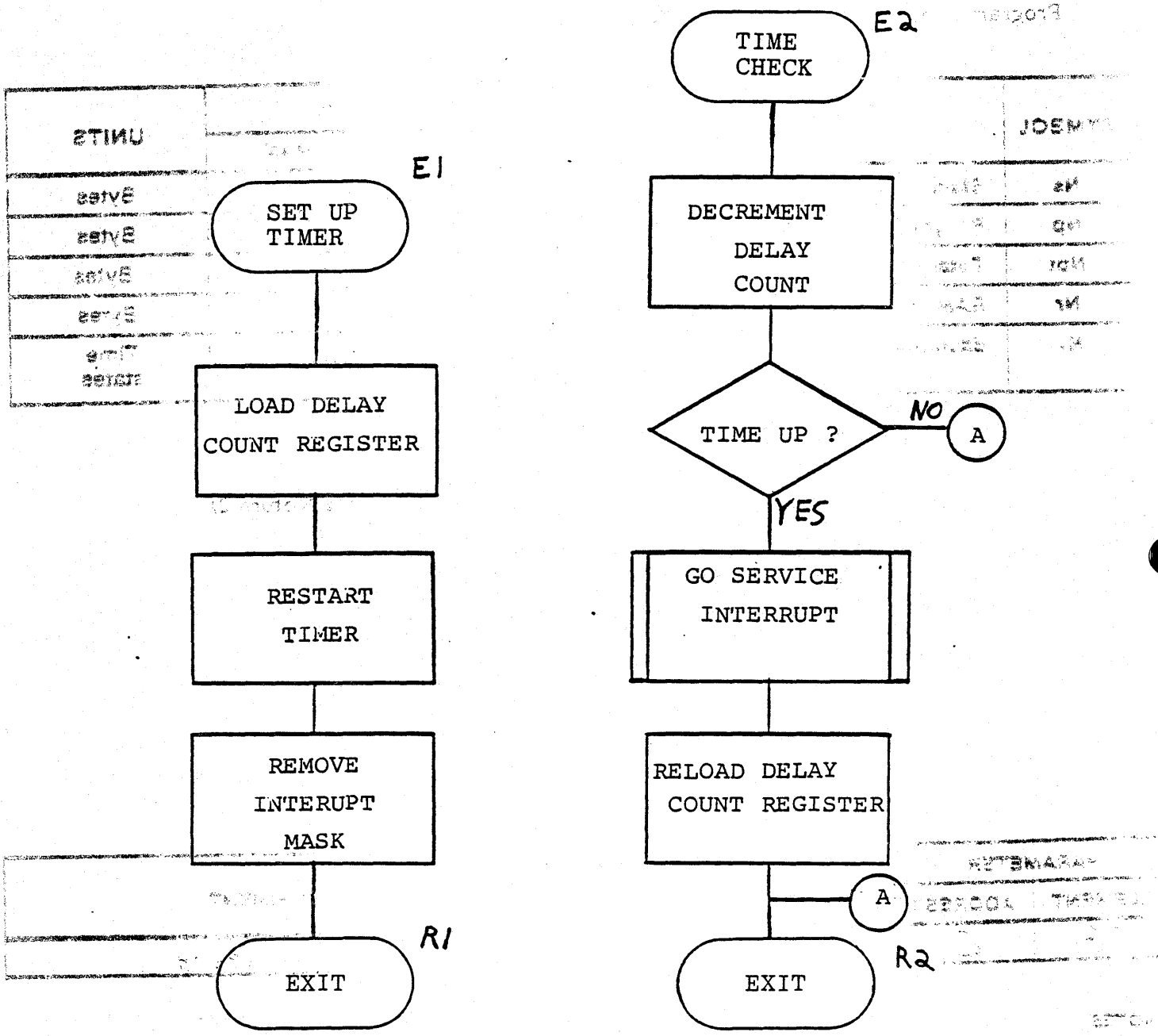


Figure 4-1. 7880 Software Example.

SYMBOL	SUBROUTINE PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
Ns	Stack memory			7	Bytes
Np	Program memory			10	Bytes
Npt	Total program memory				Bytes
Nr	RAM memory				Bytes
N_t	Execution time	8085		43	Time states
		Z80		49	

Figure 4-2. 7880 Subroutine Characteristics (Entry 2 Return 2)

PARAMETER ELEMENT	PARAMETER ADDRESS	ENTRY REQUIREMENT	EXIT CONDITION	COMMENT
REG	C	COUNT LEFT FROM LAST PASS	DECREMENTED	USED TO COUNT # OF PASSES TH

NOTES
1. For registers not shown, entry contents are not used or remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-3. 7880 Subroutine Register and Memory Allocation (Entry 2 Return 2)

SYMBOL	SUBROUTINE PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
Ns	Stack memory		4		Bytes
Np	Program memory		11		Bytes
Npt	Total program memory				Bytes
Nr	RAM memory				Bytes
N_t	Execution time	8085	43		Time states
		Z80	43		

Figure 4-4. 7880 Subroutine Characteristics (Entry 1 Return 1).

PARAMETER ELEMENT	PARAMETER ADDRESS	ENTRY REQUIREMENT	EXIT CONDITION	COMMENT
REG.	A	XX	??	
REG.	C	XX	??	

NOTES
1. For registers not shown, entry contents are not used or remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.
3. ?? means contents are unknown or meaningless.

Figure 4-5. 7880 Subroutine Register and Memory Allocation (Entry 1 Return 1).

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADDR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	TITLE / COMMENTS
	6	0D	(TIME CHECK)	DCC		CHECK DELAY COUNT + GO EXIT IF
	7	C2		JP	ZO	TIME NOT UP
	8	6F		—		
	9	00		—	EXIT	
	A	CD		JS	UN	GO SERVICE INTERRUPT
	B	XX		—		
	C	XX		—	(SERVICE INT.)	
	D	0E		LDCI		RELOAD C WITH DELAY COUNT
	E	XX		—		
	F	C9	EXIT	RTS		EXIT
	0					
	1					
	2					
	3					
	4					
	5	0E	(SET UPTIMER)	LDCI		LOAD C WITH DELAY COUNT
	6	XX		—		
	7	3E		LDAI		RESTART TIMER
	8	08		—		
	9	D3		OPA		
	A	FE		—		
	B	3E		LDAI		REMOVE INTERRUPT MASK
	C	04		—		
	D	D3		OPA		
	E	FE		—		
	F	C9		RTS		EXIT

Figure 4-6. 7880 Software Example.

Reference Drawings

The schematic (Fig. 5-2) and assembly drawing (Fig. 5-3) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user received from Pro-Log.

The schematic and assembly drawing shipped by Pro-log with the card are those from which the card was manufactured.

Card Layout

Figure 5-1 shows the physical location of the 7880's main components and jumpers. The functions of the various components are identified. Note the position of pin 1 on the IC's. When replacing chips, be careful to insert them only with pin 1 positioned as shown in the figure. Also, make sure that no pins are bent beneath the body of the chip.

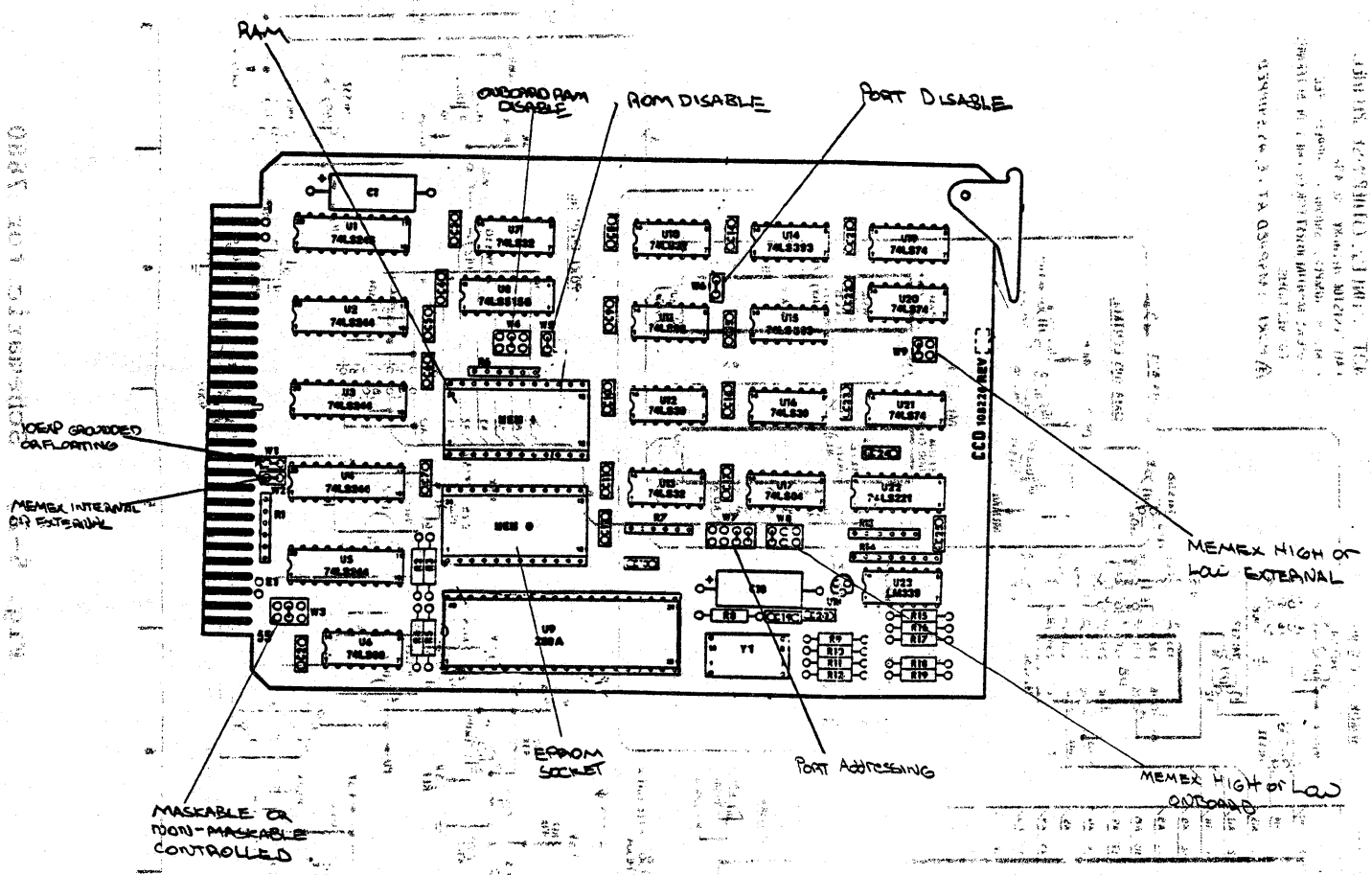


Figure 5-1. Location and Function of Main Components.

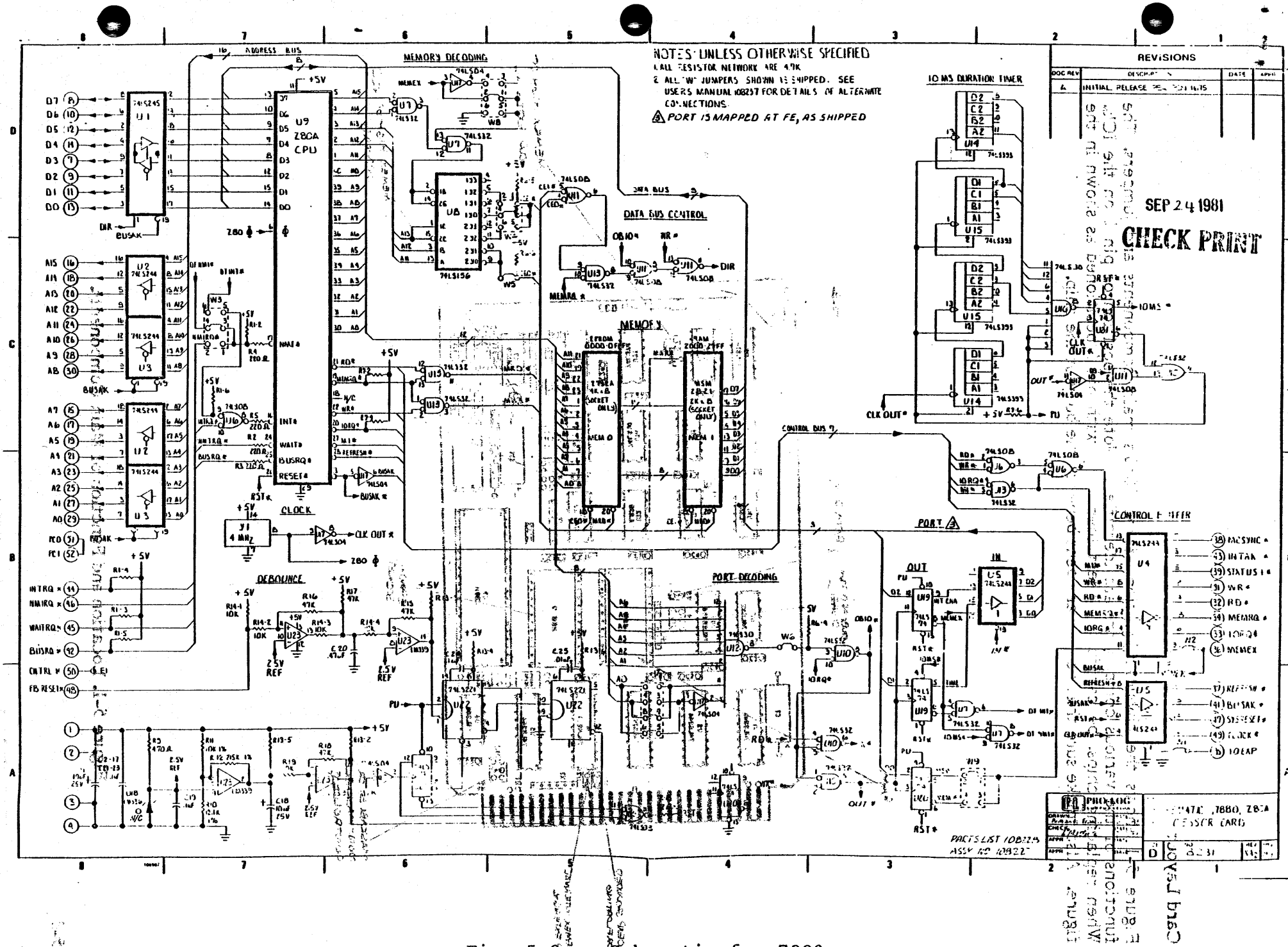


Fig. 5-2, Schematic for 7880
(Reference Only)

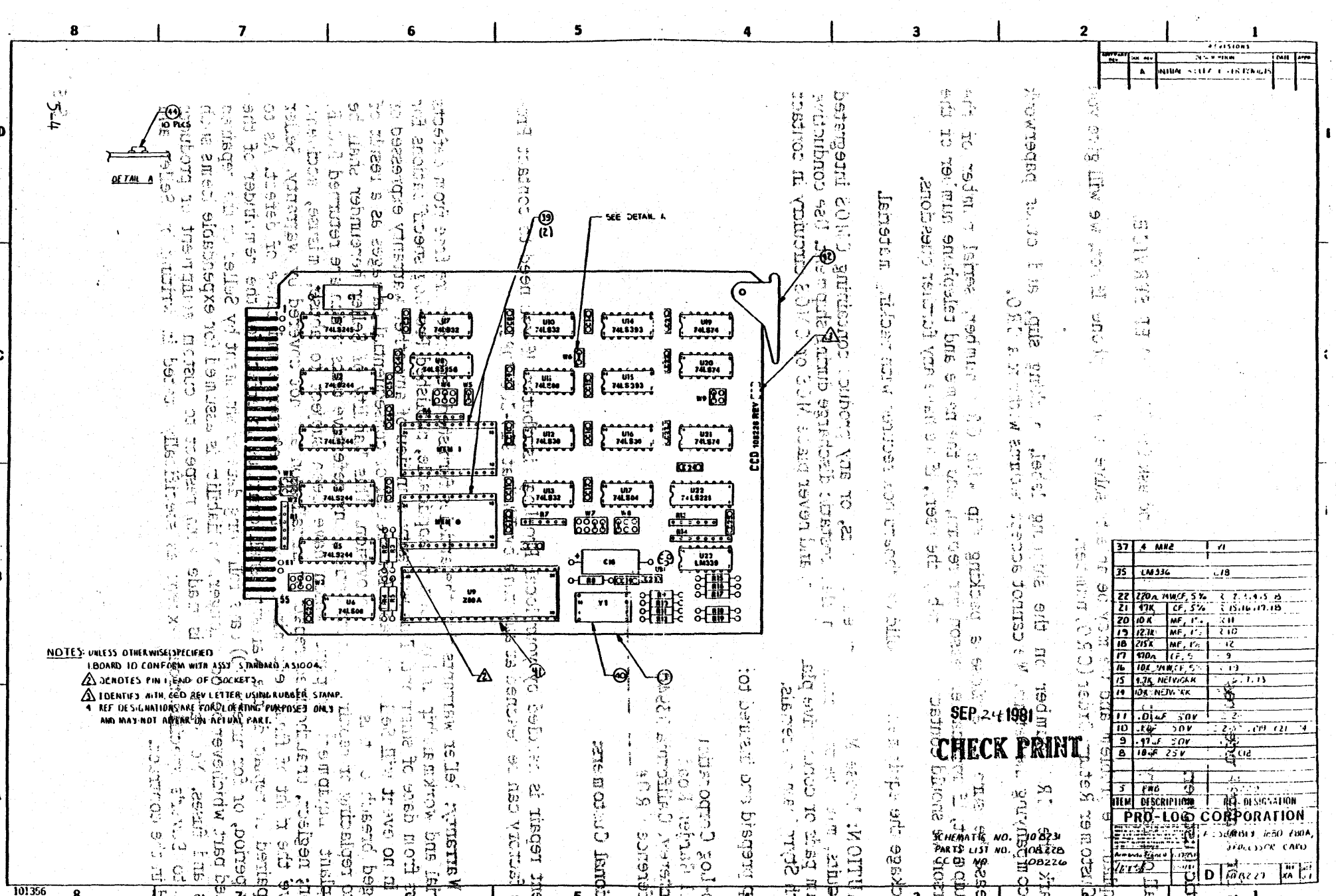


Fig. 5-3, Assembly for 7880 (reference Only)

Return for Repair Procedures

Domestic Customer:

1. Call our factory direct at (408)372-4593, and ask for CUSTOMER SERVICE.

2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.

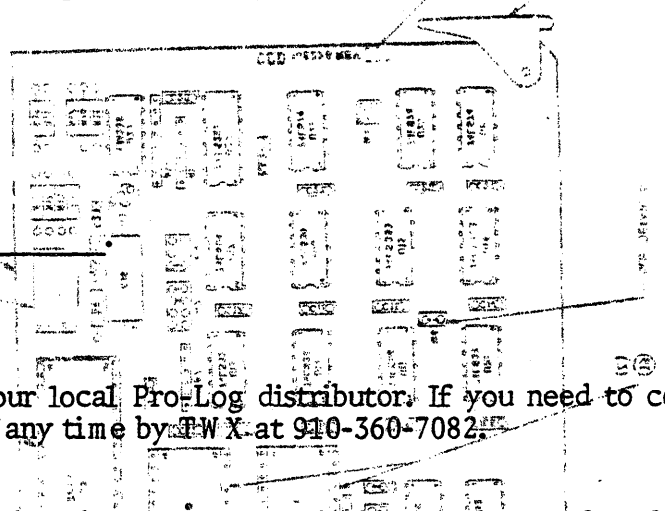
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, reason for return, and the name and telephone number of the person we should contact (preferably the user), if we have any further questions.

4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940
   Reference CRO# _____



International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. This liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

PRO-LOG
CORPORATION 2411 Garden Road Monterey, California 93940 Telephone (408) 372-4593
108237A 12/81
TWX: 910-360-7082