LATEST and GREATEST

ADD-ON I/O PORTS

00) Same as Bally Arcade

1F)

28 Number Cruncher Data Port (Read/Write)

29 Number Cruncher Command/Status Port (Read/Write)

Notes:

1. See AMD 9511 Data Sheet for details.
2. If bit 7 of command port is set, number cruncher will initiate a service request interrupt upon completion of current task. This service request will clear upon number cruncher read.
3. The following operations will put the Z-80 into a wait condition:
   - A. Device is busy and command entry is attempted. Wait will be assertive until previous operation is finished.
   - B. Device is busy and stack access is attempted. Wait will be assertive until previous operation is finished.
   - C. Device is not busy and data removal attempted. Wait pulled low until data is put into interface latch.
   - D. Device is not busy and data write is attempted. Wait will be assertive until the interface latch is available.
   - E. Wait is assertive for the length of time necessary to put device status information into the interface latch. Device status can be read at any time.
   - *** F. Items A. and B. above are potentially disastrous to RAM data. Therefore, either a service request interrupt or a status register busy bit poll should be used to determine completion of number cruncher tasks.

2A UART Data Port (Read/Write)

2B UART Command/Status Port (Read/Write)

Notes:

1. See AMD 9551 Data Sheet for details.
2. Do Not use synchronous mode.
3. See Port 23 description for clock modes.

25)
26) Not Used.
27)

2C or 2D Keyboard Port (Read/Write)

The keyboard is configured in an 8 x 8 matrix.

The keyboard can be accessed by writing a pattern to either port number. (The hardware responds to either address). This pattern has a Ø in the selected bit. All other bits are 1's. A "0" will pull down the input resistor of any row where a switch is closed. Column Ø is on bit Ø,Column 1on bit 1, etc.

When reading, a closed crosspoint will come back as a Ø in a field of ones. Row Ø comes back in bit Ø, row 1 on bit 1, etc. Read at either port, also. In addition, if ØØ is written to the port, it can be determined if any key is closed. Any key closed will return a pattern ≠ FF. For crosspoint definitions, see attached sheet.

20 NORML. (Write Only)

When the game is either reset or the panic button is pushed, the top two bits (A14 and A15) are forced high, and HVGSYS is disabled, this forces the processor to fetch from the OPSYS ROMs, starting at address CØØØ upon reset. When the Panic Button is pushed, an NMI occurs and hardware then forces the processor to fetch from OPSYS starting at address CØ66. If any bit pattern is written to port 29, the 1's are removed from address lines 14 and 15, and HVGSYS is then enabled, at it's normal address. Further writes to port 29 will have no effect until either reset or NMI occur.

21 VCTR (Write Only)

This port controls add-on interrupts. There are two sources of interrupt in the add-on. They are: UART Receive Character Available (Highest Priority), and number cruncher service request.

Bits 7 through 3 get returned as a vector when the ADD-ON responds to an interrupt acknowledge. Bit 2 when written to a '1' enables add-on interrupts. Bits 1 and 0 are not used.

Turn on reset will disable add-on interrupts and force the Bit 3-7 vector to 00.

With interrupts enabled, the ADD-ON will return the following vectors:

	B7	B6	B5	B4	B3	B2	B1	B0
UART Reve Data	B7	B6	B5	B4	B3	1	0	0
Number Cruncher Service Request	B7	B6	B5	B4	B3	0	1	0

If the Add-On and Bally Arcade generate interrupts simultaneously, the Add-On Vector will be the one that actually gets back to the CPU.

22 BSAUD. (Write Only)

The I/O Chip audio output can be output to a stereo system by using this port.

Bits Ø-2 control left channel volume,

Bits 3-5 control right channel volume,

Bits 6-7 are not used.

A zero in the bit pattern defines no volume, 7 in the bit pattern defines full volume.

By rapid switching of this port, a stereo image can be made out of I/O chip audio, and moved around the room.

23 BAUDSEL (Write Only)

This port provides for miscellaneous UART control.

Bit Ø 1 = Read from cassette 1, Write to Cassette 2.
Ø = Read from Cassette 2, Write to Cassette 1.

Bit 1 1 = Cassette # 1 motor on (Only if Bit 4 = Ø)
Ø = Off

Bit 2 1 = Cassette # 2 motor on (Only if Bit 4 = Ø)
Ø = Off

Bit 3 1 = RS232 Enabled
Ø = Cassette Enabled

Bits 4, 5, 6 defines baud rate.

Bit 6 5 4	Baud Rate	X Clock for UART
0 0 0	19.2K Baud	16
0 0 1	9600 Baud	16
0 1 0	4800 Baud	16
0 1 1	2400 Baud	16

Bit	Baud Rate	X Clock for UART
1 0 0	1200 Baud	16
1 0 1	600 Baud	16
1 1 0	300 Baud	16
1 1 1	2400 Baud	1 (See Note)

Note: Use only this baud rate for cassette interfacing.

24 LEDS (Write Only)

A Ø on an individual bit will turn on the associated LED; a 1 turns it off.

Initialization Note:

OPSYS 1 ROM should contain the following initialization procedure:

C000	NOP
C001	JMP
C002	04
C003	C0
C004	XRA
C005	OUT
C006	2ØH