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IM88-0415-90
HARDWARE INSTRUCTION MANUAL
ND560 ADC ANALOG TO DIGITAL CONVERTER

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SECTION I
INTRODUCTION

1-1. GENERAL DESCRIPTION

1-2. This manual contains instructions necessary to operate and maintain the ND560 ADC Analog to Digital Converter Module, part number 88-0415, manufactured by Nuclear Data, Inc. The ND560 ADC (figure 1-1), is a highly versatile analog to digital converter designed for processing amplitude modulated signals such as encountered when measuring fast, random phenomenon. It may also be used to sample dc or slowly varying voltages. The ADC is a NIM compatible 2-wide module which may be used singly or in combinations providing an analyzer with capability for single or multiparameter analysis. Since it is only a 2-wide module, its use is enhanced where conservation of bin space is a requirement.

1-3. Data acquisition efficiency is enhanced by a 50 MHz digitizing rate. The digitizing oscillator is crystal controlled to ensure long term stability. In addition, all critical circuitry is temperature compensated to ensure drift-free operation.

1-4. Conversion gain is selectable in binary increments from 128 to 4096 channels full scale. Front panel selection of group size in binary increments from 64 to 4096 allows resolution of up to 4096 in a memory group of only 64 channel capacity.

1-5. Digital zero shift selection is provided by five toggle switches representing 128, 256, 512, 1024 and 2048 channels. By placing these switches in the appropriate position, the selected channel can be digitally moved to zero, automatically suppressing all previous channels. Any combination of switches may be used, providing a maximum zero shift of 3968 channels. Analog zero is adjustable from 0 to over 50% of full scale by front panel coarse and fine zero controls.

1-6. Both upper and lower level discriminators are variable from 0 to 110% by front panel ten-turn potentiometers. Upon acceptance of an event, the lower level discriminator is locked out of operation until completion of an ADC cycle. If at the time it is re-enabled, the input level is higher than the discriminator threshold (indicating an event at the linear gate), the ADC does not accept the event for analysis. The operation of the upper level discriminator provides a fast dump feature which rapidly discharges the stretcher and clears the ADC either automatically or upon command from an external analyzer. These features provide a significant reduction in system dead time.

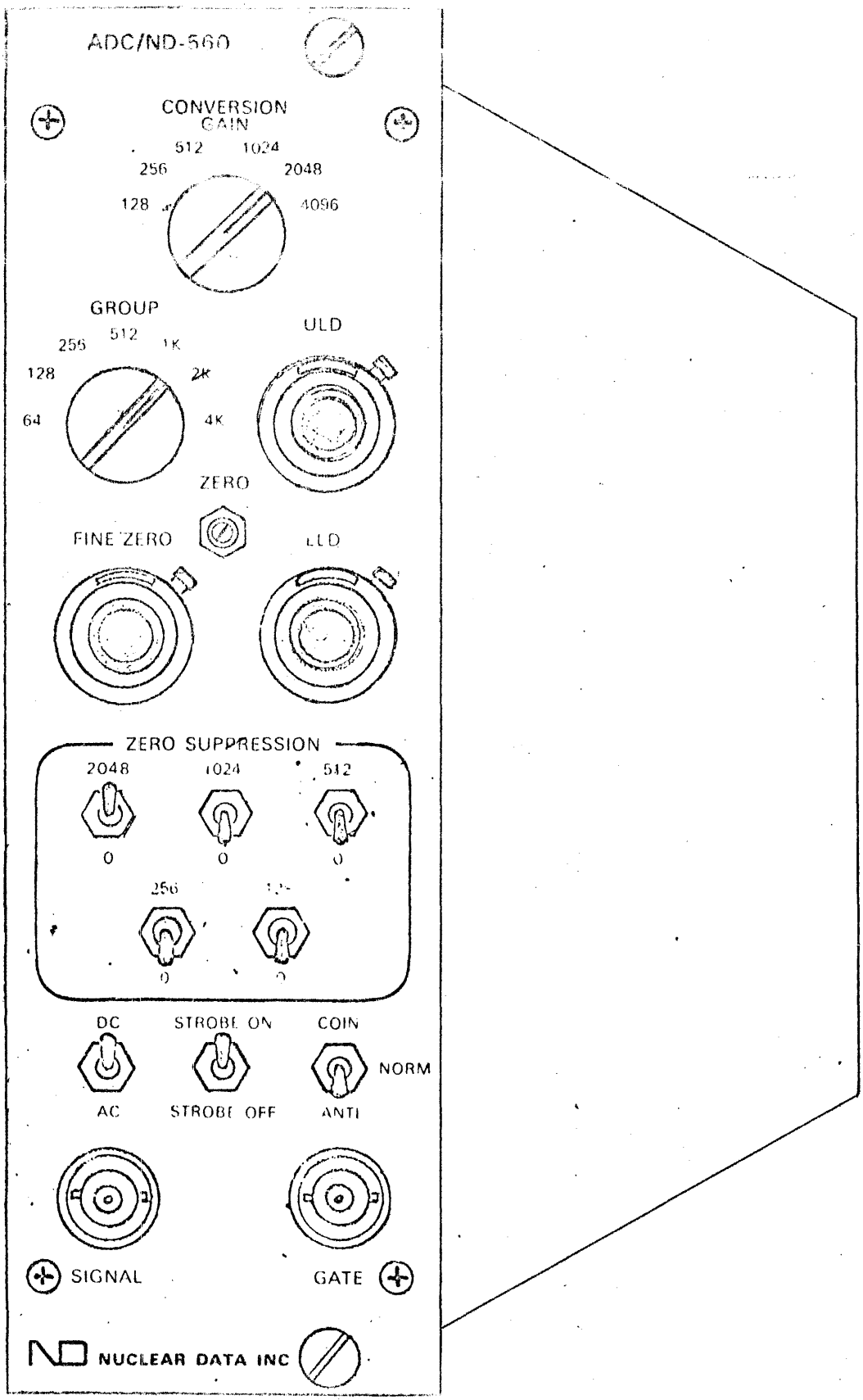


Figure 1-1. ND560 ADC Analog to Digital Converter Module

1-7. SPECIFICATIONS

1-8. Technical specifications applicable to the ND560 ADC are listed in table 1-1.

Table 1-1. ND560 ADC Technical Specifications

Characteristic	Specification
Conversion Gain	128, 256, 512, 1024, 2048 or 4096 channels full scale
Digitizing Rate	50 MHz on all conversion ranges
ADC Conversion Time	6 + 0.02N μSec on all conversion ranges where n is equal to the number of address advances for a given input event. The fixed dead time (6 μSec) includes initialization, pedestal rundown, delay line propagation, bad data flag (ALT*) check, etc.
Signal Input	
Coupling	ac or dc, switch selectable
Amplitude	0 to +8V, nominal
Polarity	Positive monopolar or initially positive bipolar.
Rise Time	0.2 to 70 μSec
Duration	1 μSec, minimum
Internal Delay	1 μSec
Input Impedence	1000 ohms
Baseline Restoration	
Type	Robinson
Input	Positive monopolar, operative in ac mode only
Baseline Shift	Less than 0.1% for a full scale pulse at random couting rates up to 25 kHz
Coincidence or Anticoincidence Input	
Selection	Coincidence, anticoincidence or normal operation
Amplitude	3 to 10V, ac or dc coupled
Polarity	Positive from 0V reference
Duration	1 μSec, minimum
Timing	Determined by interval adjustment which allows coincidence or anticoincidence pulse to occur before or after the input event. Nominally set at 2 μSec. Overlap of the input event is not necessary in either coincidence or anticoincidence.
Input Impedence	1000 ohms
Strobe	Front panel switch selectable for use in measuring slowly varying dc signals or rapidly determining the zero energy intercept
Auto Position	Opens the linear gate for a pre-determined time, as selected by the LGT control.

Table 1-1. ND560 ADC Technical Specifications (Cont'd)

Characteristic	Specification
	Rate is nominally 8,000 samples per second. An external 3 to 10V positive strobe pulse, 1 to 10 μSec in duration, may be entered via rear panel BNC to open the linear gate for the pre-determined time. Pulse rate not to exceed 8,000 samples/Sec.
Normal Position	Disables internal and external auto strobe.
Zero Suppression	Five front panel switches allow binary selection of zero suppression from 128 to 3968 channels. When not in acquire, the digital circuitry is live, providing valid data commencing with the initial input event.
Upper and Lower Level Discriminator	Adjustable from 0 to 110% of full scale by front panel ten-turn potentiometers. Both upper and lower level discrimination is provided in all modes by dc coupling.
Coarse Zero	Adjustable from 0 to over 50% of full scale by front panel fifteen-turn trim potentiometer.
Fine Zero	Adjustable from 0 to 0.5% of full scale by front panel ten-turn potentiometer.
Group Selection	Group size is switch selectable in binary increment from 64 to 4096. Allows resolution of up to 4096 in a memory group of only 64 channel capacity.
Linearity	
Integral	Better than 0.075% over 99% of full scale.
Differential	Less than 1.0% deviation from mean channel width over 99% of full scale.
Stability	
Time	Less than 0.5 channels per day at stable ambient temperature.
Temperature	Less than + 0.01% zero shift and less than + 0.01% gain shift per 1°C from 15 to 40°C.
Live Time/Clock Time Switch	Provides selection of live or clock time when the ADC is used in the ND2200 or ND4400 Analyzer System.

Table 1-1. ND560 ADC Technical Specifications (Cont'd)

Characteristic	Specification
AUT ALT CLR Switch	
OFF Position	Disables Auto ALT CLR Function. When this function is disabled, the ADC provides a bad data flag (ALT*) for an invalid event which ic cleared upon issuance of an external clear ADC signal (CLRADC*). Data transferred for an invalid event will be all zeroes.
AC1 Position	Enables Auto ALT CLR function when the ADC is used in the ND4400 or ND50/50 Analyzer System. When this function is enabled, the ADC will automatically clear all invalid data and will not issue a data ready flag thus eliminating additional dead time due to processing of invalid event.
AC2 Position	Enables Auto ALT CLR function when the ADC is used in the ND2200 or ND2400 Analyzer System.
LGT Control	Continously variable from 7 to 70 µSec. Must be set such that the linear gate time (LGT) exceeds the rise time of the input event.
BUSY BNC J1	Provides a signal which resides at +5V when the ADC is not busy and at 0V when the ADC is busy processing data.
SCA BNC J2	Provides a nominal +5 to 0V output pulse, 5 µSec in duration, for every event that falls within the limits set by the upper and lower level discriminators.
BLOCK BNC J3	Requires a 0V signal during the time the ADC is not busy but the lower level discriminator is triggered to set the bad data flag and reject the data. Normally used with the ND521 M/R Mixer/Rejector.
DC STROBE BNC J4	Accepts a positive 3 to 10V pulse, 1 to 10 µSec in duration to open the linear gate for the pre-determined time as selected by the LGT control. Maximum rate not to exceed 10 kHz. Input is only accepted when the Strobe switch is in the Normal position.

Table 1-1. ND560 ADC Technical Specifications (Cont'd)

Characteristic	Specification
EXT ZERO BNC J5	Provides connection to the ND Digital Stabilizer (normally equipped with a shorting BNC).
EXT GAIN BNC J6	Provides connection to the ND Digital Stabilizer (normally equipped with a shorting BNC.
Power Requirements	+24 Vdc @ 115 mA - 24 Vdc @ 115 mA +12 Vdc @ 840 mA - 12 Vdc @ 15 mA When a +6 Vdc supply is available, 800 mA is automatically switched from +12 Vdc to +6 Vdc.
Dimensions	8.71"h X 2.68"w x 9.7"d (NIM compatible two width module)
Part Number	88-0415

SECTION II
EQUIPMENT PREPARATION

2-1. GENERAL

2-2. This section contains instructions for preparation for use, installation and interconnections and preliminary check-out.

2-3. PREPARATION FOR USE

2-4. UNPACKING AND INSPECTION

2-5. When unpacking the equipment save the shipping cartons for possible reshipment. Visually inspect the equipment for damaged panels, controls, indicators, or connectors. If damage is apparent, notify the nearest Nuclear Data representative immediately.

2-6. INSTALLATION AND INTERCONNECTIONS

2-7. The ND560 ADC module is designed to be mounted in a Nuclear Data NIM Bin equipped with a Bin Power Supply or any compatible NIM Bin. The following is a step-by-step installation and interconnection procedure for the ND560 ADC.

a. Insert the ND560 ADC Module into a compatible NIM bin in such a manner as to mate the power connector on the rear of the module with a bin power connector.

NOTE

Ascertain that the bin power supply powering the ND560 ADC meets the power requirements outlined in table 1-1.

b. Connect the ND560 ADC Module to the external Analyzer System with a suitable interconnecting cable ascertaining that the signal terminations coincide with those outlined in table 4-1.

2-8. CABLE FABRICATION

2-9. To interconnect the ND560 ADC with an external analyzer system not manufactured by Nuclear Data, it may be necessary to fabricate an interconnecting cable to mate with the rear panel 50-pin female connector. The mating connector is an AMP 200276-4 connector equipped with AMP 201354-1 male pin. The logic input/output signals, the associated pin locations and a brief functional description is listed in table 4-1.

2-10. If a standard NIM bin and power supply are unavailable, it may be necessary to fabricate an interconnecting cable to mate with the 42-pin male power connector on the rear panel of the ND560 ADC Module. The mating connector is an AMP 202516-3 connector equipped with AMP 202508-1 female pins. The voltages, associated pin location and power requirements are listed in table 4-2.

2-11. PRELIMINARY CHECK-OUT

2-12. The following procedures provide step-by-step instructions to ensure the module is ready for normal operation. These procedures should be performed as a matter of routine before operating the ND560 ADC.

a. Set front panel switches and controls as follows:

Switch/Control	Initial Position
CONVERSION GAIN Switch	Equivalent to memory group size selected at external analyzer.
GROUP Switch	Equivalent to memory group size selected at external analyzer.
ULD Control	Fully clockwise (10.0)
LLD Control	Fully counter clockwise (0.0)
ZERO Trim Potentiometer	Fully counter clockwise
FINE ZERO Control	Fully counter clockwise (0.0)
ZERO SUPPRESSION Switches	All zero (0)
STROBE On/STROBE OFF Switch	STROBE ON
DC/AC Switch	AC
COIN/NORM/ANTI Switch	NORM

b. Set rear panel switches and controls as follows:

Switch/Control	Initial Position
AUT ALT CLR Switch	As desired
LGT Control	Set at a time greater than the rise time of the input event.
LIVE TIME/CLOCK TIME	As desired

c. Set the bin POWER switch to ON. POWER indicator lamp shall light.

d. Adjust FINE ZERO control until storage is observed in channel zero.

e. Set STROBE ON/STROBE OFF switch to STROBE OFF.

f. Apply an appropriate signal to the front panel SIGNAL INPUT BNC.

g. Adjust the LLD control clockwise until storage of a spectrum is observed. The ADC is now operational and properly zeroed.

SECTION III
OPERATING INSTRUCTIONS

3-1. GENERAL

3-2. This section contains instructions for operating the ND560 ADC. Included are control and connector functions and general operational considerations for obtaining results in various experimental applications.

3-3. CONTROL AND CONNECTOR FUNCTIONS

3-4. Front panel controls and connectors for the ND560 ADC module are illustrated in Figure 3-1. Table 3-1 lists the front panel controls and connectors, and describes their function. Rear panel controls and connectors for the ND560 ADC module are illustrated in Figure 3-2. Table 3-2 lists the rear panel controls and connectors, and describes their function.

Table 3-1. ND560 ADC Front Panel Control and Connector Functions

Control/Connector	Description	Function
CONVERSION GAIN	6-position Rotary Switch	Position 128, 256, 512, 1024, 2048 or 4096 selects the number of channel advance pulses produced for a full scale input signal.
GROUP	7-position Rotary Switch	Position 64, 128, 256, 512, 1K, 2K, or 4K selects the memory group size for data storage.
ZERO	15-turn Trim Potentiometer	Permits coarse adjustment of the zero energy intercept from 0 to over 50% of full scale.

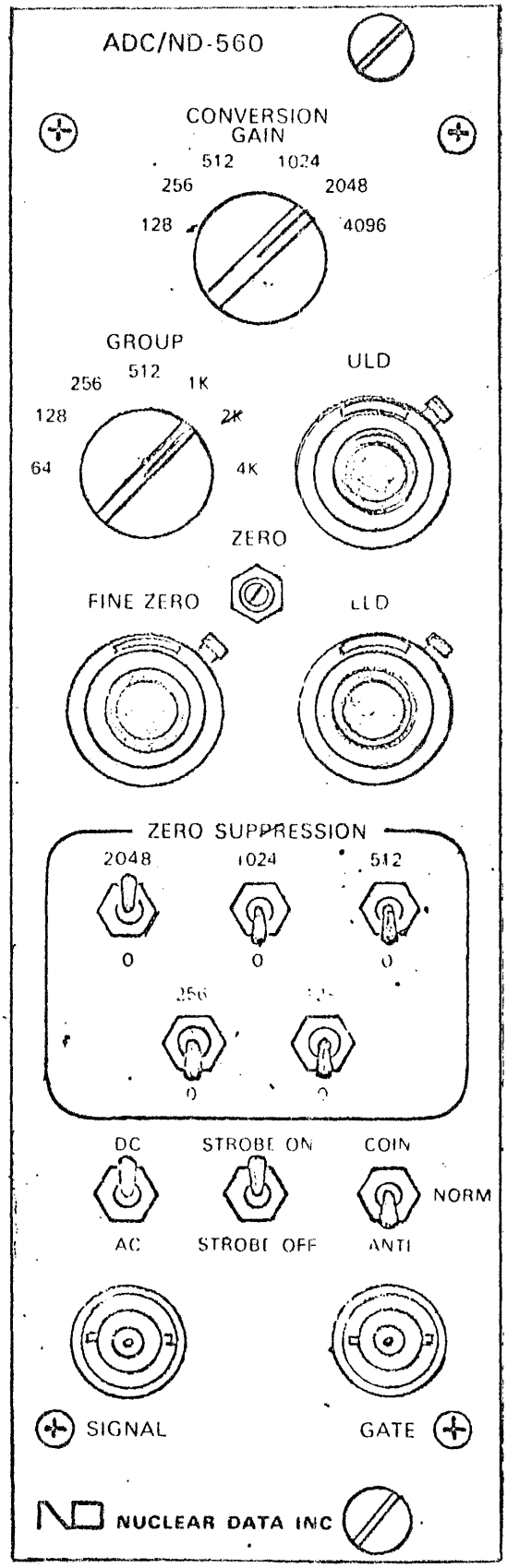


Figure 3-1. ND560 ADC Front Panel Controls and Connectors

Table 3-1. ND560 ADC Front Panel Control and Connector Functions (Cont'd)

Control/Connector	Description	Function
FINE ZERO	10-turn Potentiometer	Permits fine adjustment of the zero energy intercept from 0 to 0.5% of full scale.
ULD	10-turn Potentiometer	Determines the maximum amplitude level of an input signal which will be accepted by the ADC. Adjustable from 0 to 110% of full scale.
LLD	10-turn Potentiometer	Determines the minimum amplitude level of an input signal which will be accepted by the ADC. Adjustable from 0 to 110% of full scale.
ZERO SUPPRESSION	Five 2-position Toggle Switches	Appropriate positioning of these switches permit the selected channel (128, 256, 512, 1024 or 2048) to be digitally moved to zero, automatically, suppressing all previous channels. Any combination of switches may be used, providing a maximum zero shift of 3968 channels.
AC/DC	2-position Toggle Switch	Selects ac or dc coupling of input signals applied to the front panel SIGNAL INPUT BNC.
STROBE ON/STROBE OFF	2-position Toggle Switch	STROBE ON: Opens the linear gate for a pre-determined time as selected by the LGT control. Also permits entry of an external 3 to 10V strobe pulse via the rear panel, DC STROBE BNC J4, 1 to 10 μSec in duration, to open the linear gate for the pre-determined time. STROBE OFF: Disables internal and external auto strobe function.

Table 3-1. ND560 ADC Front Panel Control and Connector Functions (Cont'd)

Control/Connector	Description	Function
COIN/NORM/ANTI	3-position Toggle Switch	COIN: Selects coincidence mode of operation using signal applied to front panel GATE BNC. NORM: Selects normal ADC operation ANTI: Selects anticoincidence mode of operation using signal applied to front panel GATE BNC.
SIGNAL INPUT	BNC	Ac or dc coupled input to ADC, switch selectable. Requires positive monopolar or initially positive bipolar 0 to 8V pulses with rise time between 0.2 and 70 μSec. Minimum duration is 1 μSec. Internal delay is 1 μSec. Input impedance is 1000 ohms.
GATE	BNC	Coincidence/anticoincidence input to ADC, switch selectable. Requires ac or dc coupled, 0 to 10V pulses, positive from 0V reference, with a minimum duration of 1 μSec. Timing is determined by an internal adjusment which allows the coincidence or anticoincidence pulse to occur before or after the input event (nominally set at 2 μSec). Overlap of the input event is not necessary in either the coincidence or anticoincidence mode.

Table 3-2. ND560 ADC Rear Panel Control and Connector Functions

Control/Connector	Description	Function
AUT ALT CLR	3-position Toggle Switch	OFF: Disables Auto ALT Clear function. When this function is disabled, the ADC provides a bad data flag (ALT*) for an invalid event which is cleared upon issuance of an external clear ADC signal (CLRADC*). Data transfered for an invalid event will be all zeroes. AC1: Enables Auto ALT Clear function when the ADC is used in the ND4400 or ND50/50 Analyzer System. When this function is enabled, the ADC will automatically clear all invalid data and will not issue a data ready flag thus eliminating additional dead time due to processing of invalid events. AC2: Enables Auto ALT Clear function when the ADC is used in the ND2200 or ND2400 Analyzer System.
LGT	3/4-turn Trim Potentiometer	Adjust linear gate time (LGT) from 7 to 70 μSec. Must be set such that the linear gate time is greater than the rise time of the input event.
LIVE TIME/CLOCK TIME	2-position Toggle Switch	Selects either live or clock time gating when the ADC is used in the ND2200 or ND4400 Analyzer System.
J1 BUSY	BNC	Provide a signal which resides at +5V when the ADC is not busy and at 0V when the ADC is busy processing data.

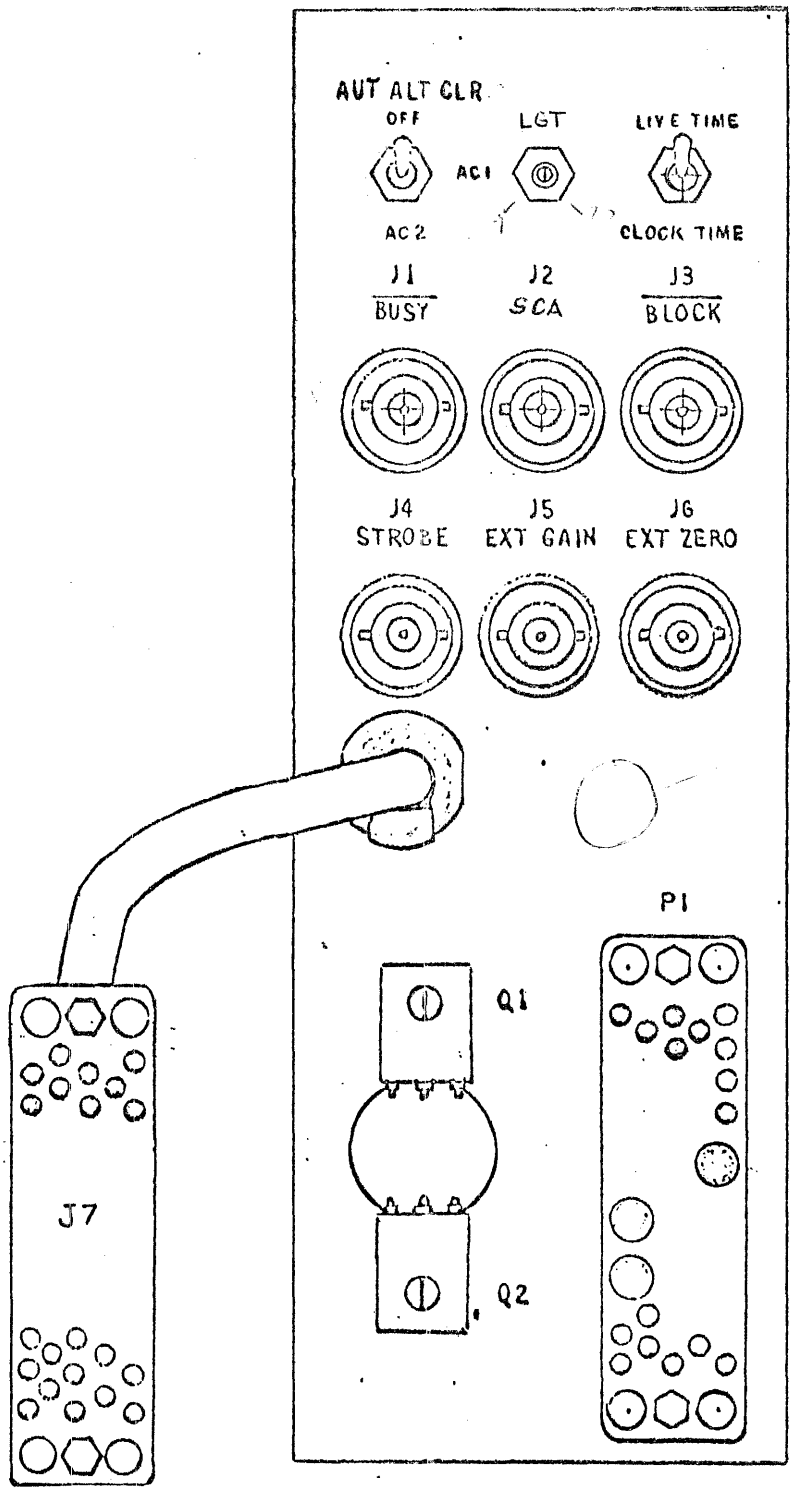


Figure 3-2. ND560 ADC Rear Panel Controls and Connectors

Table 3-2. ND560 ADC Rear Panel Control and Connector Functions (Cont'd)

Control/Connector	Description	Function
J2 SCA	BNC	Provides a nominal +5 to 0V output pulse, 5 µSec in duration, for every event that falls within the limits set by the upper and lower level discriminators.
J3 BLOCK	BNC	Requires a 0V signal during the time the ADC is not busy but the lower level discriminator is triggered, to set the bad data flag (ALT*) and reject the data. Normally used with the ND521 M/R Mixer/Rejector.
J4 DC STROBE	BNC	Accepts a positive 3 to 10V pulse, 1 to 10 µSec in duration to open the linear gate for the predetermined time as selected by the LGT control. Maximum rate not to exceed 10 kHz. Input is only accepted when the STROBE ON/STROBE OFF switch is in the STROBE ON position.
J5 EXT ZERO	BNC	Provides connection for the ND Digital Stabilizer (normally equipped with a starting BNC).
J6 EXT GAIN	BNC	Provides connection for the ND Digital Stabilizer (normally equipped with a starting BNC).
50F	50-pin Female Connector	Provides connection to the input/output signals of an external analyzer. Refer to Table 4-1 for individual signal terminations.
Power	42-pin Male Connector	Provides connection for input power from the bin power supply. Refer to Table 4-2 for individual signal terminations.

3-5. GENERAL OPERATIONAL CONSIDERATIONS

3-6. CONVERSION GAIN SELECTION

3-7. One factor to consider in the selection of the proper conversion gain is storage capacity of the analyzer memory being used. Since the number of address advance pulses for a full scale (8 volt) input signal corresponds to the CONVERSION GAIN Switch positions of 128, 256, 512, 1024, 2048, and 4096, it may seem feasible to select the switch position corresponding to the memory size, i.e., for a 1024 channel memory, set the switch at 1024, for a 2048 channel memory, set the switch at 2048, etc. This is true in some experiments but not necessarily in others. For example, if the energy of interest does not exceed four volts, it would be better to select a conversion gain of 2048 with a 1024 channel memory size since the spectrum peaks would be spread out over the full memory rather than half as would be the case of a conversion gain of 1024 were chosen.

3-8. Another factor to consider is resolution. With the CONVERSION GAIN Switch set at 1024, each channel represents 8 millivolts for a full scale 8 volt input. This means the voltage levels can be resolved within 8 millivolts of each other, hence the term resolution. As the conversion gain is lowered (voltage per channel increased), the resolution decreases accordingly. Therefore, if the experiment being performed requires high resolution to obtain the desired accuracy, it may be advantageous to use a higher conversion gain setting.

3-9. Still another factor to consider is speed. Since the analysis time for a full scale input pulse with the CONVERSION GAIN Switch set at 1024 is twice as long as it is with the switch set at 512, it may be feasible to use a lower conversion gain setting when speed rather than resolution is desired. However, since the average analysis time rather than the maximum is usually used in evaluating the selection of the proper conversion gain, the percentage of increase in speed is considerably less and the loss in resolution may be enough to make the increase in speed meaningless. Therefore, first consider how these factors will affect the experiment being performed and then select the conversion gain which is most applicable.

3-10. LOWER LEVEL DISCRIMINATOR ADJUSTMENT

3-11. In some experiments, intense noise or low energy radiation may be present. To reduce the effect of dead time, which is a result of noise analysis. the LLD control must be adjusted above the level of the noise. The LLD control biases a transistor circuit such that signals below the bias level imposed by this control are not presented to the ADC for analysis. For those signals which exceed the bias level, the bias is removed to permit the passage of the entire signal. Therefore, a large signal would be analyzed into exactly the same counting channel, independent of the bias, but small signals would not be analyzed.

3-12. When the analyzer is preoccupied with the useless analysis of noise, most of the noise will fall at channel zero. But, since channel zero is reserved for storing of clock pulses, it is not always evident that the ADC is preoccupied with noise analysis.

3-13. A percent dead time meter, which is incorporated in the ND565 DTM Module is a useful tool in determining whether or not the ADC is preoccupied with the useless analysis of noise. This allows the user to determine whether or not the setting of LLD control affects the indicated percent dead time.

3-14. When this is no appreciable noise mixed with the input signal, a minimum LLD control setting of 0.3 is usually appropriate. For highest linearity in the lower energy regions, the LLD Control should be set at the minimum value. However, if there is an apparent increase in noise which may be caused by increasing the amplifier gain, the minimum setting should be increased accordingly.

3-15. UPPER LEVEL DISCRIMINATOR ADJUSTMENT

3-16. The setting of this control selects the triggering level of the upper level discriminator circuit. Input pulses which exceed the bias setting imposed by this control will cause the linear gate of the ADC to close, prohibiting the analysis of the input pulse. For most experiments, this control is set at maximum (10.0), but can be set as desired depending upon experiment requirements.

3-17. ZERO LEVEL ADJUSTMENT

3-18. When the ZERO SUPPRESSION Switches are not used, the FINE ZERO Control is used primarily for precise adjustment of energy zero to correspond to the lower boundary of channel zero. It will be found that alteration of the CONVERSION GAIN Switch changes the energy zero position. It is therefore recommended that the proper setting of the FINE ZERO Control to locate the zero energy intercept correctly be determined for each of the six conversion gains, in order to facilitate later experimental set-up operations. It is likely that a calibration performance check once a month will be adequate for most applications, but this must be determined by experience.

SECTION IV
FUNCTIONAL DESCRIPTION

4-1. GENERAL

4-2. This section contains theory of operation for the ND560 ADC Module. Theory of operation is presented as a general functional description and a detailed functional description.

4-3. INPUT/OUTPUT SIGNAL DESCRIPTION

4-4. Table 4-1 lists the signal name, the associated pin locations, and a brief functional description of the input/output signals for the "pigtail" cable and 50-pin female connector on the rear panel of the ND560 ADC Module. Table 4-2 lists the voltages, associated pin locations and power requirements of the input power signals for the 42-pin male connector on the rear panel of the ND560 ADC Module.

Table 4-1. "Pigtail" Cable and 50-pin Female Connector I/O Signal Description

Signal	Pin	Description
ADCØ*	C	Buffer Scaler Outputs
ADC1*	H	
ADC2*	M	The steady state condition of the buffer scaler outputs
ADC3*	S	is +5V. A true condition ("1" state) of a scaler bit is
ADC4*	W	indicated by its buffered output being at 0V during
ADC5*	a	transfer time.
ADC6*	e	
ADC7*	k	Address bits: +5V = 0
ADC8*	r	0V = 1
ADC9*	v	Output impedance: 6 kohm ("0" state), to +5V
ADC10*	z	Output current: 5 mA, maximum ("1" state)
ADC11*	DD	
ATR*	Y	ADC Transfer Input

Table 4-1. "Pigtail" Cable and 50-pin Female Connector I/O Signal Description (Cont'd)

Signal	Pin	Description
		The steady state condition of signal ATR* should be +5V. A transfer will occur when signal ATR* goes from +5 to 0V any time after a conversion is completed. A minimum pulse duration of 2 μSec is required. Signal ATR* can be replaced by output signals BCB* and BF* if BF* is inverted and then combined with BCB* in a NAND gate.
CLRADC*	c	Clear ADC Input The steady state condition of signal CLRADC* should be +5V. The ADC will reset when signal CLRADC* goes from +5 to 0V any time after an address has been transferred. A minimum pulse duration of 1 μSec is required. CLRADC* causes signal BF* to return to +5V.
SS*	d	Single Sample Input Signal SS* is normally open. When operating in the coincidence mode, bringing signal SS* to ground (0V) disables the coincidence circuits causing operation in a straight singles mode.
ADCB*	h	ADC Busy Output Signal ADCB* represents the time the ADC cannot validly accept input pulses. Signal ADCB* is at +5V when the ADC is not busy and at 0V when it is busy and cannot validly accept input pulses. Signal ADCB* can be used for live time control.
REJ*	j	Reject Input Signal REJ* is normally open. When signal REJ* is brought to ground (0V) the remaining events are rendered invalid and rejected.
READY*	n, EE	Ready Output The steady state condition of signal READY* is +5V. Upon completion of a conversion, signal READY* goes to 0V to signal the external computer to supply signal ATR*.

Table 4-1. "Pigtail" Cable and 50-pin Female Connector I/O Signal Description (Cont'd)

Signal	Pin	Description
CT*	E	Clock Time Output Signal CT* is open except when rear panel LIVE TIME/ CLOCK TIME Switch is in the CLOCK TIME position, then signal CT* is held at ground (0V).
MS*	F	Multiscale Input Signal MS* is normally open. When using the ADC as a single channel analyzer in multichannel scaling experiment, signal MS* should be brought to ground (0V). Signal MS* at 0V provides signal CLRADC* after each processed event.
BALT	K,L ?	Buffer Alter Output Signal BALT is at +5V when information is acceptable and at 0V when information is to be rejected.
ELG*	P 5.17V	Enable Linear Gate Input Signal ELG* should be +5V or open to enable the linear gate or 0V to disable the linear gate.
BF*	R	Buffer Free Output The steady state condition of signal BF* is +5V. Upon starting a conversion, signal BCB* and then signal BF* go to 0V. At completion of a conversion, signal BCB* goes back to +5V and BF* remains at 0V until signal CLR ADC* causes BF* to return to +5V. Signal BCB* at +5V and signal BF* at 0V indicates a conversion is complete.
A*	U 1.9V	Analyze Input Signal A* should be at 0V to enable to ADC or at +5V to disable the ADC.
BCB*	t,V 0	Buffer Converter Busy Output The steady state condition of signal BCB* is +5V. Signal BCD* is at +5V when the converter is not busy and at +0V when it is busy.

Table 4-1. "Pigtail" Cable and 50-pin Female Connector I/O Signal Description (Cont'd)

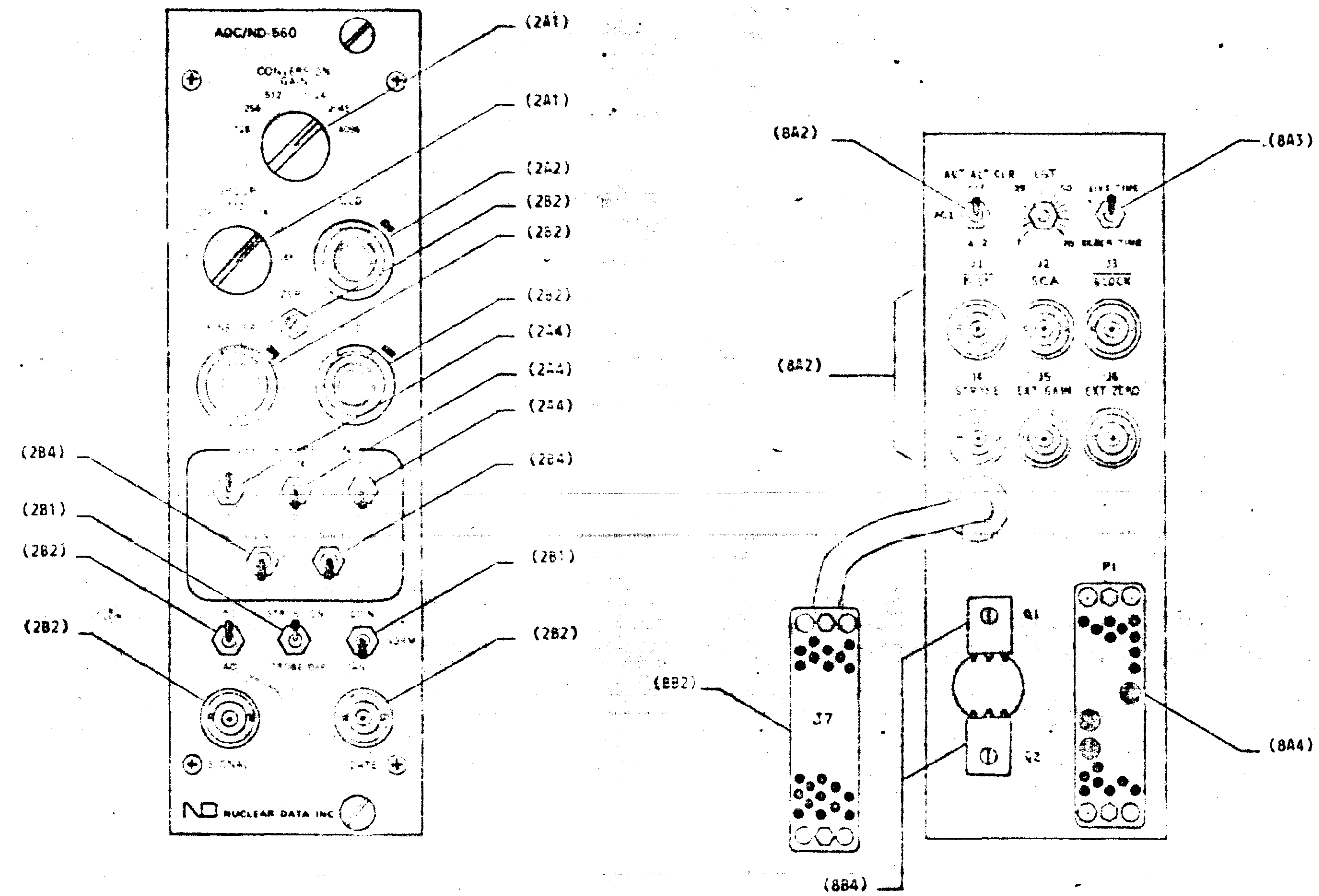
Signal	Pin	Description
DC COM	S, BB, FF	Logic Signal Common.
LLD	AA	Lower Level Discrminator Output The steady state condition of signal LLD is +5V. When the lower level discriminator is triggered by an input pulse, signal LLD goes to 0V.
ACLRON	HH	Auto Clear On Output Signal ACLRON is open when the rear panel AUT ALT CLR switch is in the AC1 or AC2 position and at 0V when the switch is in the OFF position.

Table 4-2. 42-pin Male Power Connector Signal Description

Signal	Pin	Description
+6V	10	+6 Vdc @ 800 mA (see note below)
+12V	16	+12 Vdc @ 840 mA (see note below)
-12V	17	-12 Vdc @ 15 mA
+24V	28	+24 Vdc @ 115 mA
-24V	29	-24 Vdc @ 115 mA
DC COM	34	Power return ground.
DC COM	42	High quality ground.

NOTE

If a +6 Vdc supply is available, 800 mA is automatically switched from the +12 Vdc supply to the +6 Vdc supply.

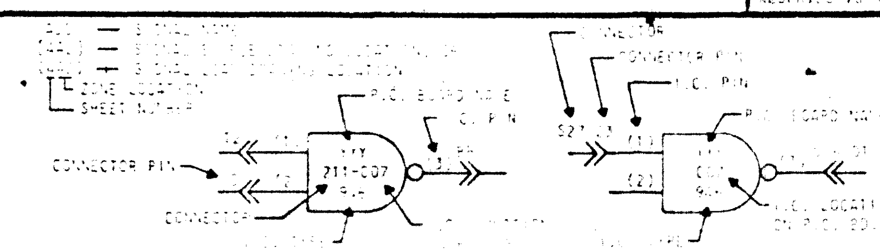


NOTES:

1 - [illegible] ARE [illegible] EXCEPT AS NOTED.
2 - ALL RESISTORS ARE 1/4W, ±5%, EXCEPT AS NOTED.
3 - ALL CAPACITORS [illegible] EXCEPT AS NOTED.
4 - [illegible] VOLTAGES, EXCEPT AS NOTED:
14 PIN [illegible] PIN (7) [illegible] PIN (14) +5V
16 PIN [illegible] PIN (8) [illegible] PIN (16) +5V

5 - THE FOLLOWING SYMBOLS/NOTATIONS ARE USED ON THE DIAGRAM AND/OR PRINTED CIRCUIT ASSEMBLY:

IC - INTEGRATED CIRCUIT
Q - TRANSISTOR
( ) - IC PIN DESIGNATION
CONNECTOR DESIGNATION
NC - NO CONNECTION
SAT - SELECT AT TEST
(P1) - PRECISION RESISTORS 100PPM 1/8W, ±1% METAL FILM
DC COMMON
FB - FERRITE BEAD
[illegible] DIODE
SILICON DIODE
ZENER DIODE
TUNNEL DIODE
SELENIUM DIODE

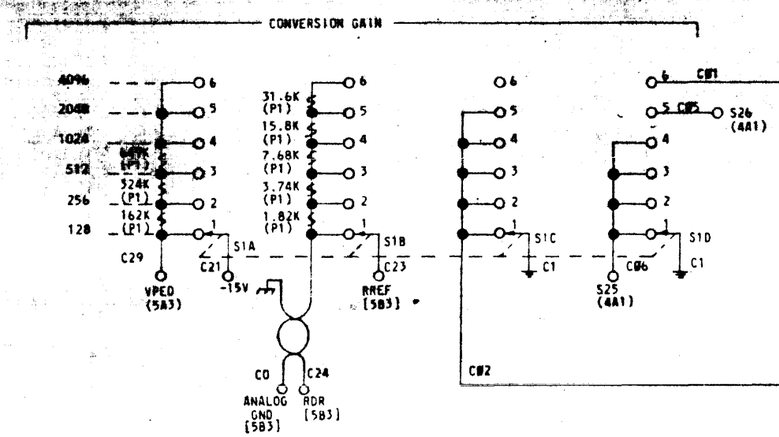


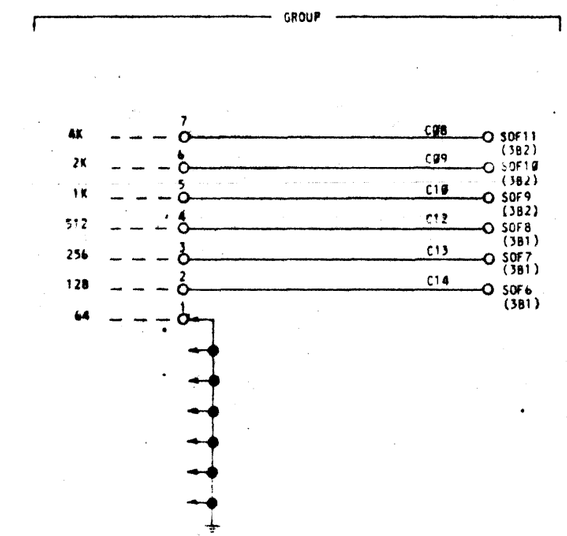
NUCLEAR DATA INC

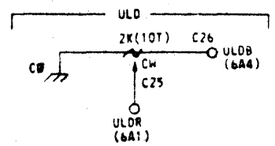
SYSTEM DIAGRAM
ADC/ND-560

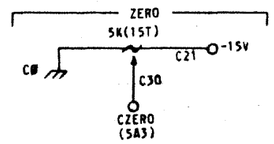
(FRONT & REAR PANEL)

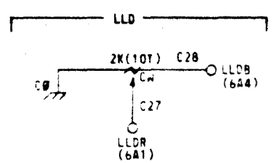
R.K.
9/15/71
L88-0415 01

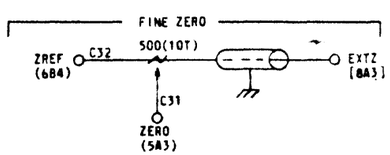


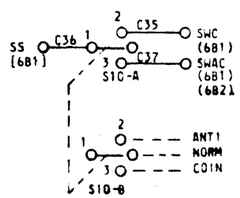


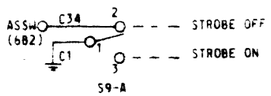


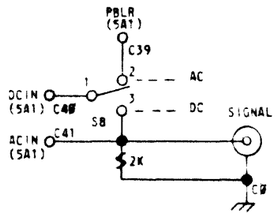


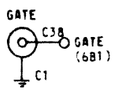


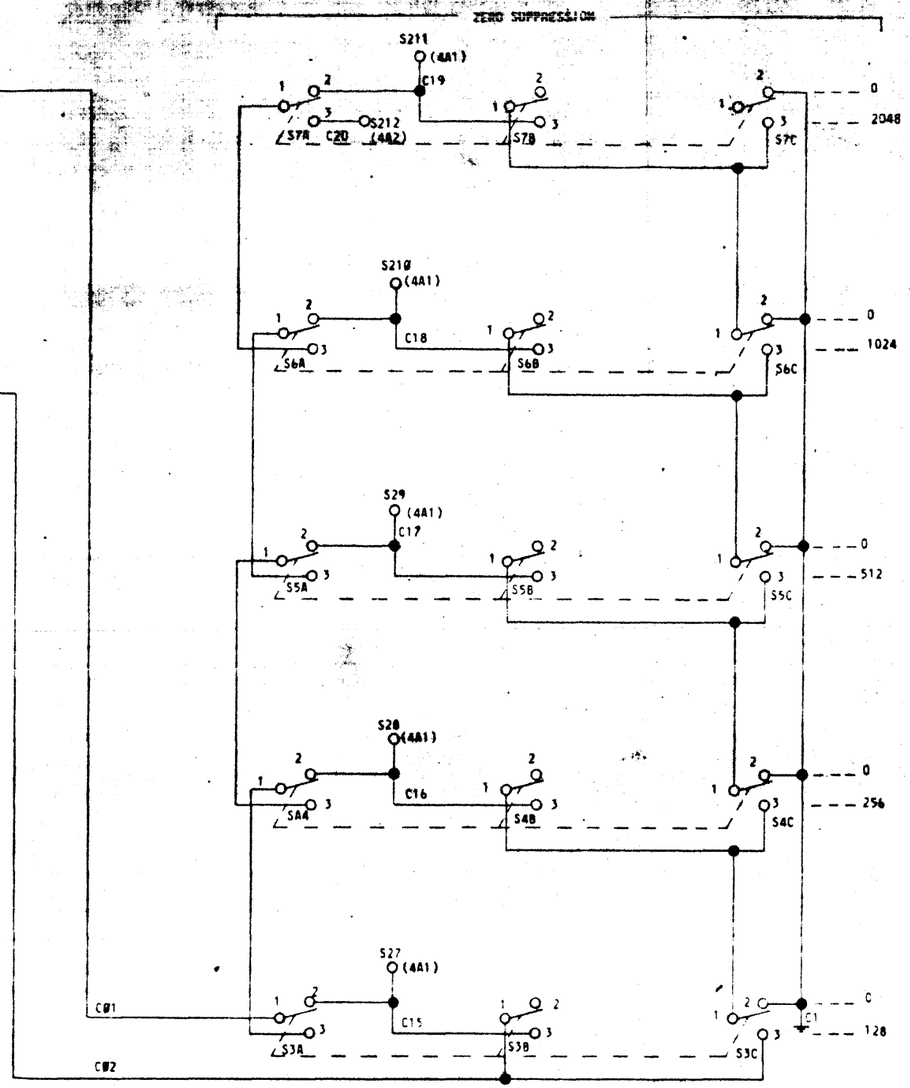












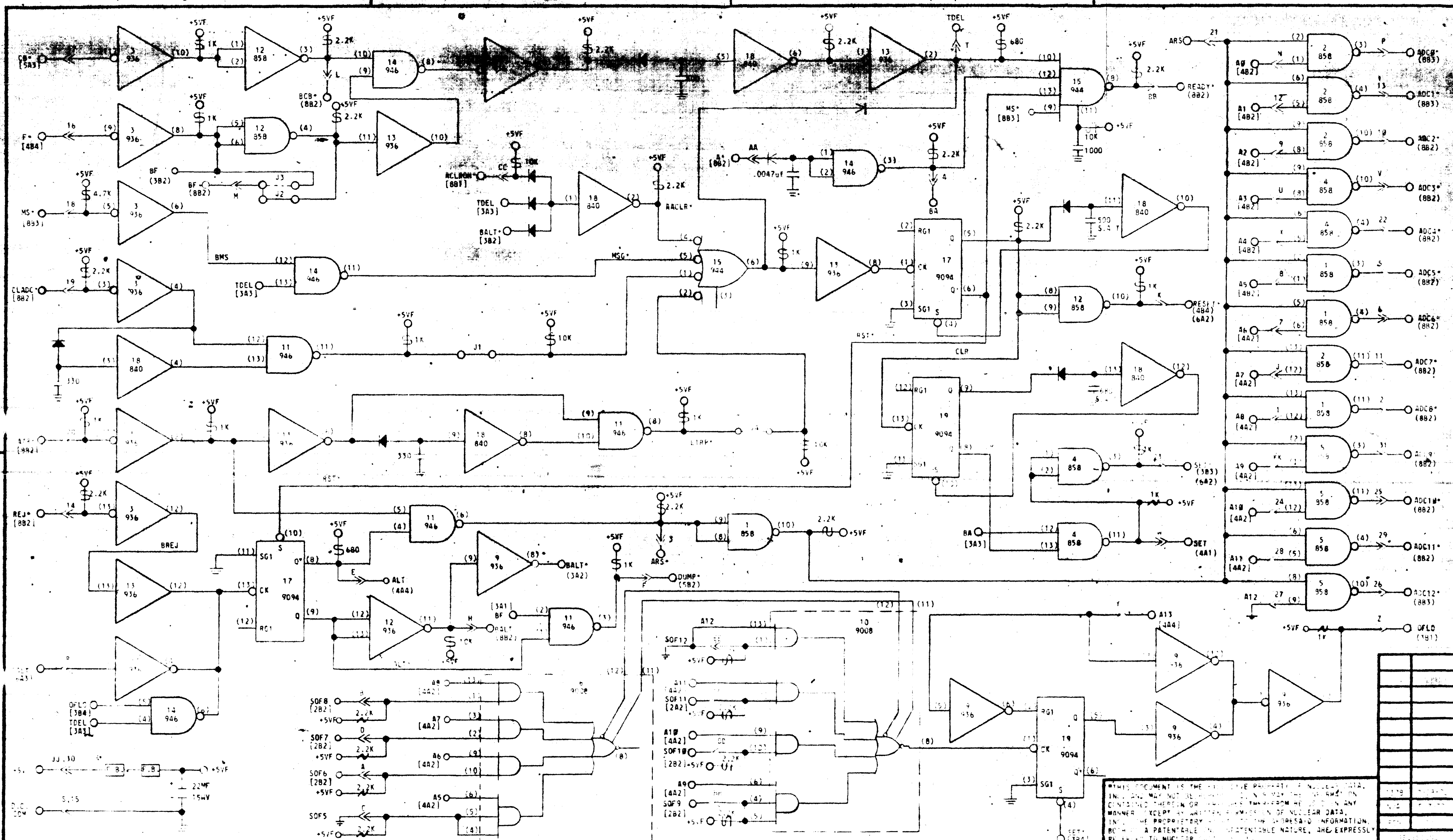
1378	7-28-72
N/A	5-8-72
ECN	DATE
REVISIONS	

NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

SYSTEM DIAGRAM
ADC ND-560
(FRONT PANEL COMPONENTS)

DRAWN BY: R.M.G.	CHECKED BY: P.L.	SHEET 2 OF 11
DATE DRN: 5-8-72	APPROVED BY:	388-1415-02

REVISING ECN



NOTES:

1 - ALL DIODES ARE D964 OR EQUIVALENT, EXCEPT AS NOTED.

2 - ALL RESISTORS ARE 1/4W, ±5%, EXCEPT AS NOTED.

3 - ALL CAPACITORS ARE pF, EXCEPT AS NOTED.

4 - I.C. VOLTAGES, EXCEPT AS NOTED:

14 PIN DIP, PIN (7) GND; PIN (14) +5V

16 PIN DIP, PIN (8) GND; PIN (16) +5V,

24 PIN DIP, PIN (12) GND; PIN (24) +5V

5 - THE FOLLOWING SYMBOLS/NOTATIONS ARE USED ON THE DIAGRAM AND/OR PRINTED CIRCUIT BOARD ASSEMBLY:

IC - INTEGRATED CIRCUIT

Q - TRANSISTOR

( ) - IC PIN DESIGNATION

CONNECTOR DESIGNATION

NC - NO CONNECTION

SAT - SELECT AT TEST

(P) OR (P1) - PRECISION RESISTORS 100PPM 1/8W, ±1% METAL FILM

DC COMMON

FB - FERRITE BEAD

GERMANIUM DIODE

SILICON DIODE

ZENER DIODE

TUNNEL DIODE

SELENIUM DIODE

RST — SIGNAL NAME

[4A2] — SIGNAL SOURCE DRAWING LOCATION, OR

[4A2] — SIGNAL LOAD DRAWING LOCATION

ZONE LOCATION

SHEET NUMBER

P.C. BOARD NAME

P.C. PIN

CONNECTOR PIN

CONNECTOR

CONNECTOR PIN

P.C. PIN

P.C. BOARD NAME

NUCLEAR DATA INC

POST OFFICE BOX 451 PALATINE, ILLINOIS 60067

SYSTEM DIAGRAM

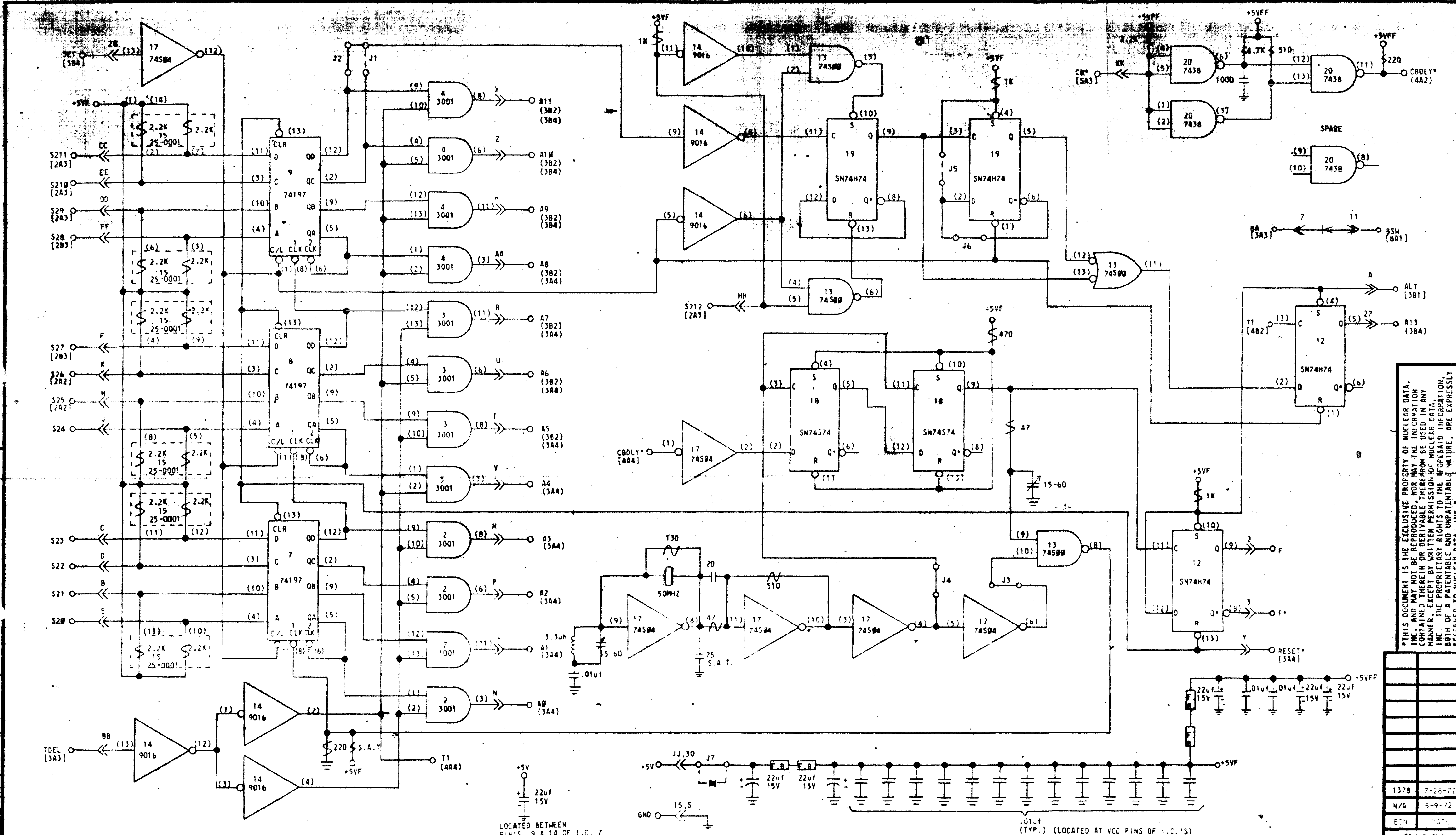
ADC/ND-560

(ND-ADL-A, 70-1616)

BOARD LOCATION 101

SHEET 3 OF 11

188-0415-02



1378	7-28-72
N/A	5-9-72
ECN	DATE

REVISIONS

NOTES:

1 - ALL DIODES ARE G964 OR EQUIVALENT, EXCEPT AS NOTED.

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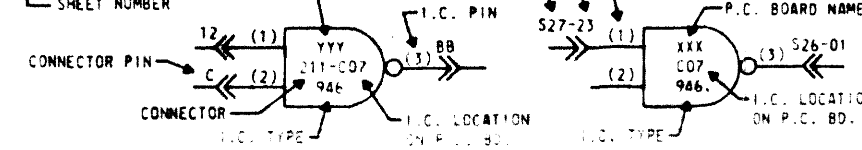
4 - I.C. VOLTAGES, EXCEPT AS NOTED:
- 14 PIN DIP, PIN (7) GND: PIN (14) +5V
- 16 PIN DIP, PIN (8) GND: PIN (16) +5V
- 24 PIN DIP, PIN (12) GND: PIN (24) +5V

5 - THE FOLLOWING SYMBOLS/NOTATIONS ARE USED ON THE DIAGRAM AND/OR PRINTED CIRCUIT BOARD ASSEMBLY

- IC - INTEGRATED CIRCUIT
- Q - TRANSISTOR
- ( ) - IC PIN DESIGNATION
- - CONNECTOR DESIGNATION
- NC - NO CONNECTION
- SAT - SELECT AT TEST
- (P1) - PRECISION RESISTORS 100PPM 1/8W, ±1% METAL FILM
- - DC COMMON
- FB - FERRITE BEAD
- - GERMANIUM DIODE
- - SILICON DIODE
- - ZENER DIODE
- - TUNNEL DIODE
- - SELENIUM DIODE

ADC* — SIGNAL NAME
[4A2] — SIGNAL SOURCE DRAWING LOCATION, OR
(4A2) — SIGNAL LOAD DRAWING LOCATION
ZONE LOCATION
SHEET NUMBER



NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

SYSTEM DIAGRAM
ADC ND-560

(ND-AHV-A 70-1639)

BOARD LOCATION 102

DRAWN BY: R.K.	CHECKED BY:	SHEET 4 OF 11
DATE DRAWN: 3-22-	APPROVED BY:	498-0415-02

PENDING ECN

1 - SOURCE
2 - GATE
3 - DRAIN
4 - SUBSTRATE

BOTTOM VIEWS

3N170

2N5046

TO701
(FLAT SIDE P.N.P.
TRANSISTOR)

2N4416

UC734

2N5555

1452	11-13-72
1439	11-13-72
1379	[illegible]
N/A	9-8-72
ECN	DATE
REVISIONS	

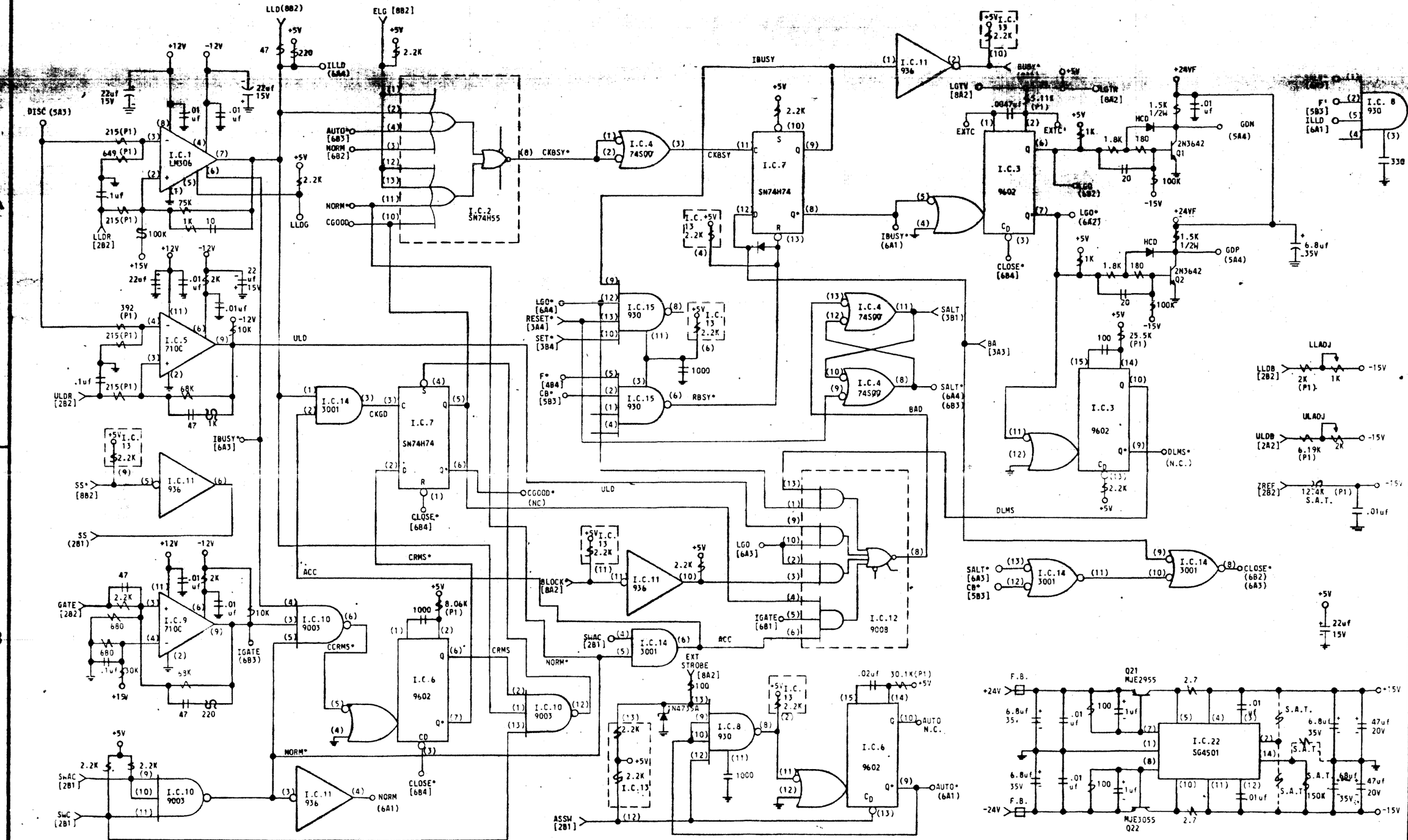
NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

SYSTEM DIAGRAM
ADC/ND-560

(ND-AHT-A 70-1849)

DRAWN BY: S.V.W.	CHECKED BY:	SHEET 5 OF 11
DATE DRAWN: 7/15/71	APPROVED BY:	L88-0415-04

THIS ECN



NOTES:

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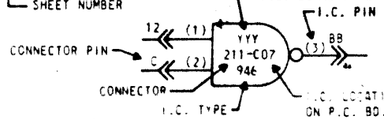
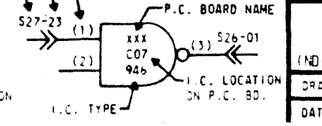
( ) - IC PIN DESIGNATION
- CONNECTOR DESIGNATION
NC - NO CONNECTION
SAT - SELECT AT TEST
(P1) - PRECISION RESISTORS 100PPM 1/8W, ±1% METAL FILM
- DC COMMON
FB - FERRITE BEAD
- GERMANIUM DIODE
- SILICON DIODE
- ZENER DIODE
- TUNNEL DIODE
- SELENIUM DIODE

ADC* — SIGNAL NAME
(4A2) — SIGNAL SOURCE DRAWING LOCATION, OR
(4A2) — SIGNAL LOAD DRAWING LOCATION
ZONE LOCATION
SHEET NUMBER





1452	11-13-72
1378	7-28-72
N/A	5-8-72
ECN	DATE

REVISIONS

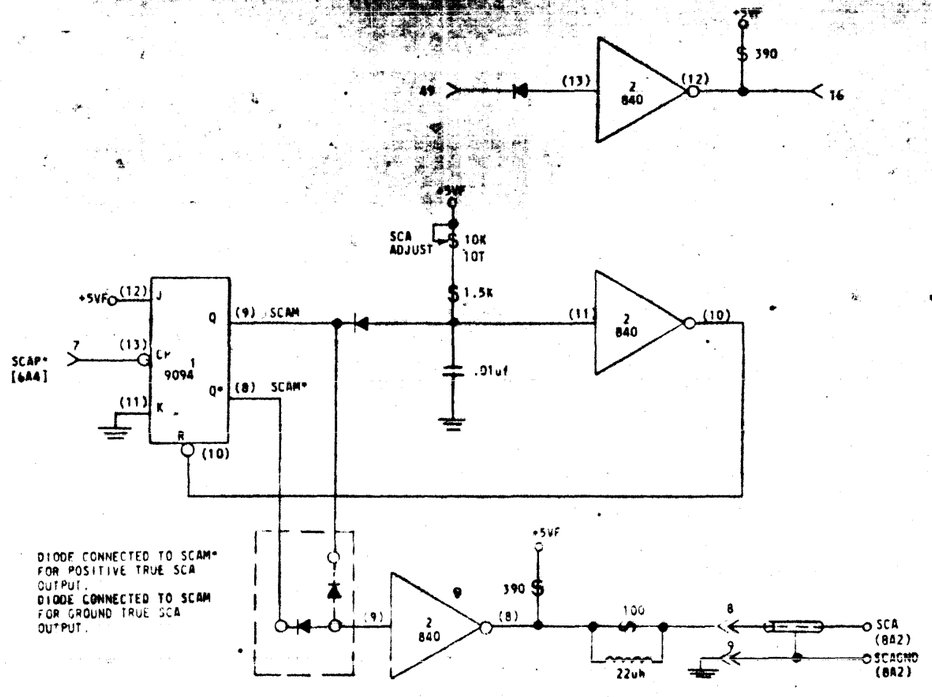
NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

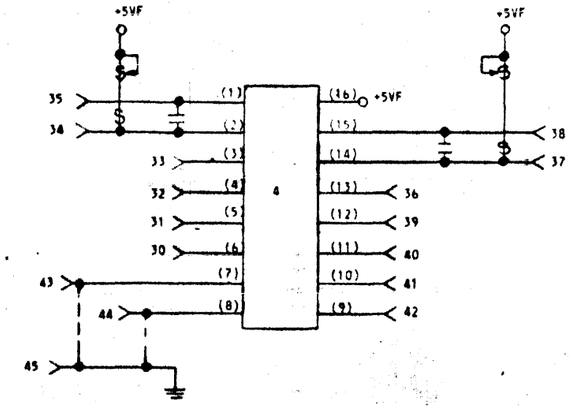
SYSTEM DIAGRAM
ADC/ND-560

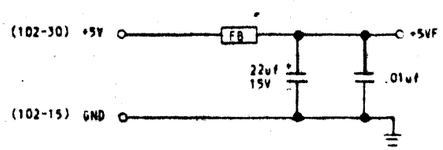
(ND-AHT-A 70-1849)

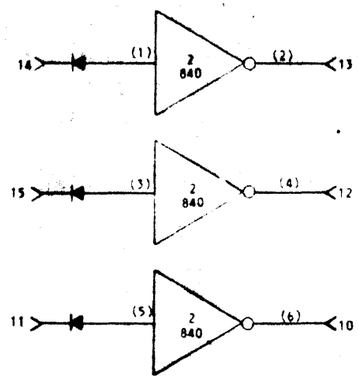
DRAWN BY: S.V.W.	CHECKED BY: - -	SHEET 6 OF 11
DATE DRAWN: 7/14/71	APPROVED BY:	L88-0415-03

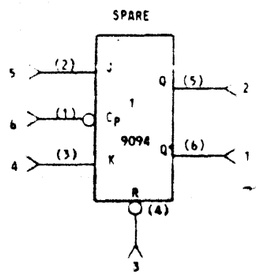
TRADING ETN

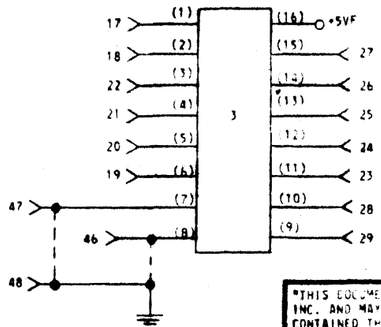












1378	7-28-72
N/A	7-28-72
[illegible]	[illegible]
[illegible]	[illegible]

NOTES:

1 - ALL DIODES ARE 1N9140R EQUIVALENT, EXCEPT AS NOTED.
2 - ALL RESISTORS ARE 1/4W, ±5%, EXCEPT AS NOTED.
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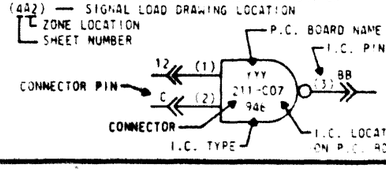
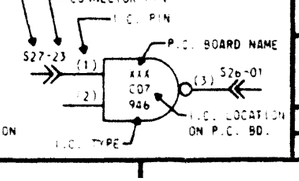
FB - FERRITE BEAD
- GERMANIUM DIODE
- SILICON DIODE
- ZENER DIODE
- TUNNEL DIODE
- SELENIUM DIODE

ADC* — SIGNAL NAME
(4A2) — SIGNAL SOURCE DRAWING LOCATION, OR
(4A2) — SIGNAL LOAD DRAWING LOCATION
ZONE LOCATION
SHEET NUMBER



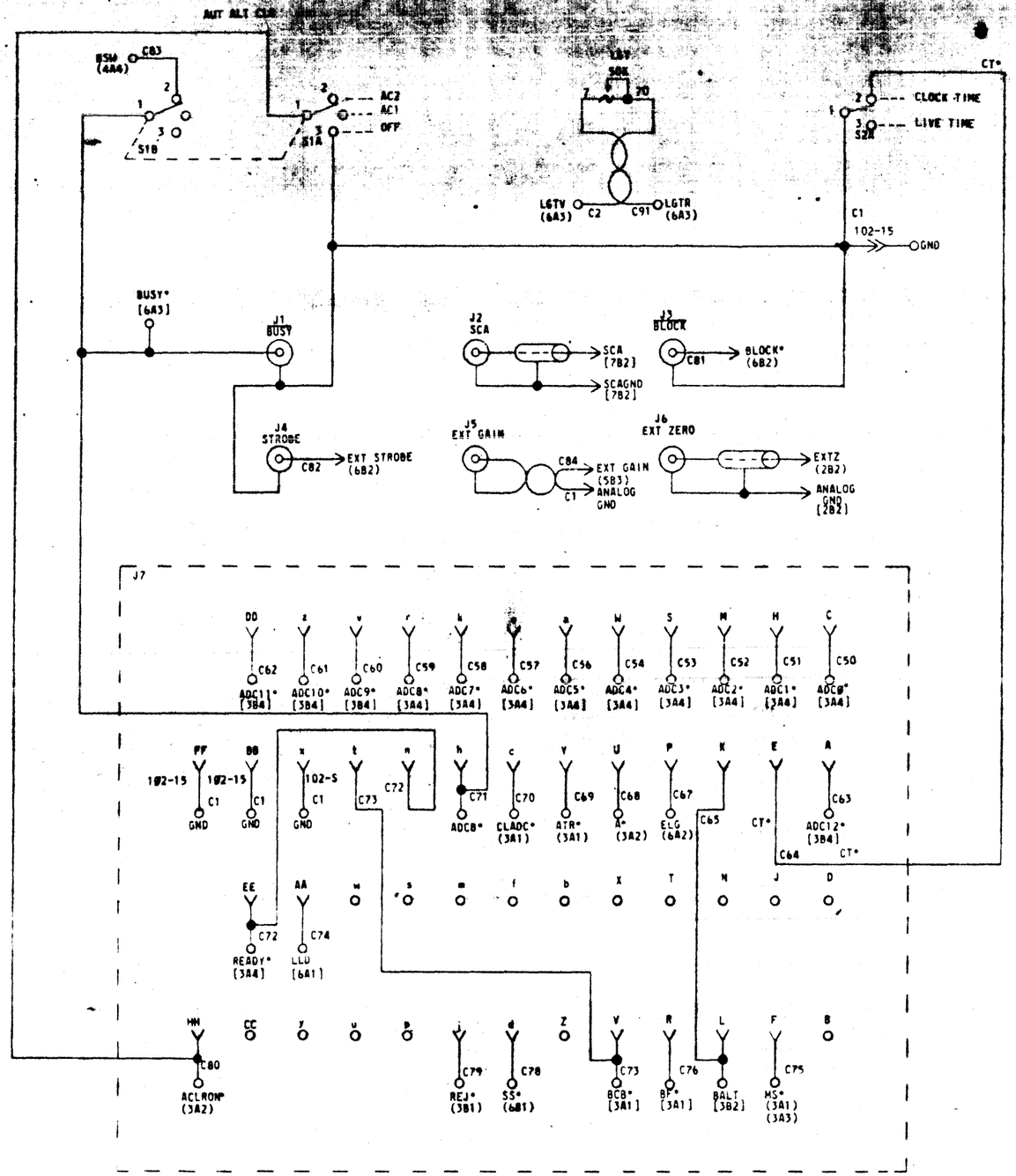


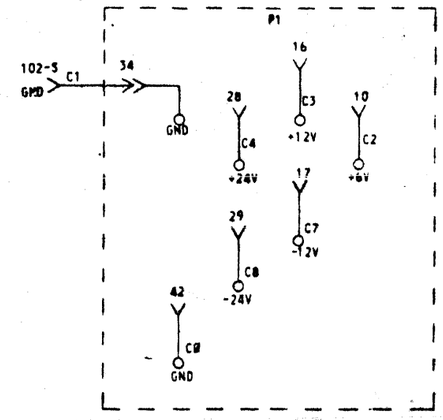
NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

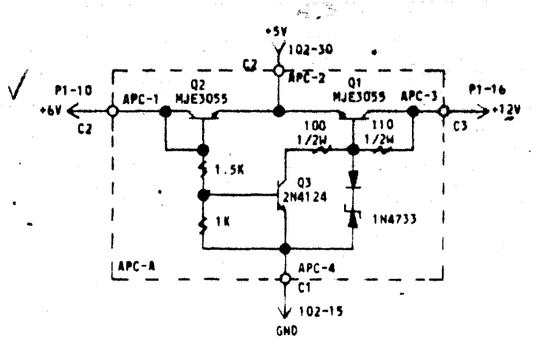
SYSTEM DIAGRAM
ADC/ND-560

DRAWN BY G.J.V	[illegible]	SHEET 7 OF 11
DATE PRINT 7-7-72	[illegible]	DRAWING 02

PENDING ECN







1378	7-28-72
ECN	DATE

REVISIONS

NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS 60067

SYSTEM DIAGRAM
ADC, ND-560
(REAR PANEL COMPONENTS)

DRAWN BY: R M G	CHECKED BY:	SHEET 8 OF 11
DATE: 5-9-72	APPROVED BY:	199 0415 01

PENDING ECN

CONNECTOR 101			
PIN	SIGNAL	PIN	SIGNAL
1	A6[3A4]	A	SOF6[3B1]
2	ADC8*[3A4]	B	SOF8[3B1]
3	ARS*[3B2]	C	SOF5[3B1]
4	BA[3A3]	D	SOF7[3B1]
5	ADC5*[3A4]	E	ALT[3B1]
6	ADC6*[3A4]	F	DUMP*[3B2]
7	A6[3A4]	H	BALT[3B2]
8	A5[3A4]	J	A7[3A4]
9	A2[3A4]	K	RESET*[3A4]
10	ADC2*[3A4]	L	BCB*[3A1]
11	ADC7*[3A4]	M	BF*[3A1]
12	A1[3A4]	N	AØ[3A4]
13	ADC1*[3A4]	P	ADCØ*[3A4]
14	REJ*[3B1]	R	SALT[3B1]
15	GND[3B1]	S	GND[3B1]
16	F*[3A1]	T	TDEL[3A3]
17	CB*[3A1]	U	A3[3A4]
18	SS*[3A1]	V	ADC3*[3A4]
19	CLADC*[3A1]	W	SET[3B4]
20	ATR*[3A1]	X	A4[3A4]
21	ARS[3A4]	Y	A13[3B4]
22	ADC4*[3A4]	Z	OFLO[3B4]
23	SET*[3B4]	AA	A*[3A2]
24	A10[3B4]	BB	READY*[3A4]
25	[illegible]	CC	ACLRON*[3A2]
26	ADC12*[3B4]	DD	SOF1Ø[3B2]
27	A12[3B4]	EE	SOF12[3B2]
28	A11[3B4]	FF	SOF11[3B2]
29	ADC11*[3B4]	HH	SOF9[3B2]
30	+5V[3B1]	JJ	+5V[3B1]
31	ADC9*[3B4]	KK	A9[3B4]

CONNECTOR 102			
PIN	SIGNAL	PIN	SIGNAL
1		A	ALT[4A4]
2	F[4B4]	B	S21[4B1]
3	F*[4B4]	C	S23[4B1]
4		D	S22[4B1]
5		E	S2Ø[4B1]
6		F	S27[4A1]
7	BA[4A4]	H	S25[4A1]
8		J	S24[4A1]
9		K	S26[4A1]
10		L	A1[4B2]
11	BSW[4A4]	M	A3[4B2]
12		N	AØ[4B2]
13		P	A2[4B2]
14		R	A7[4A2]
15	GND[4B2]	S	GND[4B2]
16		T	A5[4A2]
17		U	A6[4A2]
18		V	A4[4B2]
19		W	A9[4A2]
20		X	A11[4A2]
21		Y	RESET*[4A4]
22		Z	A12[4A2]
23		AA	A8[4A2]
24		BB	TDEL[4B1]
25		CC	S211[4A1]
26		DD	S29[4A1]
27	A13[4A4]	EE	S21Ø[4A1]
28	SET[4A1]	FF	S28[4A1]
29		HH	S212[4A2]
30	+5V[4B2]	JJ	+5V[4B2]
31		KK	CB*[4A4]

AMT BOARD			
SIGNAL	LOCATION	SIGNAL	LOCATION
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	CB*	[illegible]
[illegible]	[5B3]	[illegible]	[illegible]
F*	[5B3]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	ELG	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	EXT STROB	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

CONNECTOR ALB BOARD			
PIN	SIGNAL	PIN	SIGNAL
1	[7B3]	2	[7B3]
3	[7B3]	4	[7B3]
5	[7B3]	6	[7B3]
7	SCAP*[7A1]	8	SCA[7B2]
9	SCAGND[7B2]	10	[7B2]
11	[7B2]	12	[7B2]
13	[7B2]	14	[7B2]
15	[7B2]	16	[7A2]
17	[7B3]	18	[7B3]
19	[7B3]	20	[7B3]
21	[7B3]	22	[7B3]
23	[7B4]	24	[7B4]
25	[7B4]	26	[7B4]
27	[7B4]	28	[7B4]
29	[7B4]	30	[7B3]
31	[7B3]	32	[7A3]
33	[7A3]	34	[7A3]
35	[7A3]	36	[7A4]
37	[7A4]	38	[7A4]
39	[7B4]	40	[7B4]
41	[7B4]	42	[7B4]
43	[7B3]	44	[7B3]
45	[7B3]	46	[7B3]
47	[7B3]	48	[7B3]
49	[7A2]		

CONNECTOR J7			
PIN	SIGNAL	PIN	SIGNAL
A	ADC12*[8B3]	B	
C	ADCØ*[8B3]	D	
E	CT*[8B3]	F	MS*[8B3]
H	ADC1*[8B3]	J	
K	BALT[8B2]	L	BALT[8B2]
M	ADC2*[8B2]	N	
P	ELG[8B2]	R	BF*[8B2]
S	ADC3*[8B2]	T	
U	A*[8B2]	V	BCB*[8B2]
W	ADC4*[8B2]	X	
Y	ATR*[8B2]	Z	
a	ADC5*[8B2]	b	
c	CLADC*[8B2]	d	SS*[8B2]
e	ADC6*[8B2]	f	
h	ADC8*[8B2]	j	REJ*[8B2]
k	ADC7*[8B2]	m	
n	READY*[8B2]	p	
r	ADC8*[8B2]	s	
t	BCB*[8B2]	u	
v	ADC9*[8B2]	w	
x	GND[8B1]	y	
z	ADC10*[8B2]	AA	LLD[8B2]
BB	GND[8B2]	CC	
DD	ADC11*[8B2]	EE	READY*[8B2]
FF	GND[8B1]	HH	[illegible]

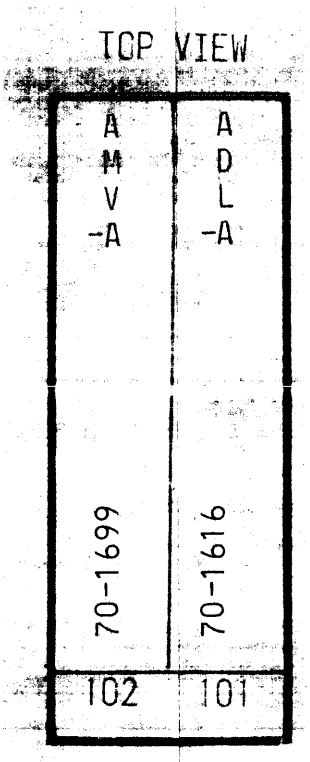
[illegible] P11			
PIN	SIGNAL	PIN	SIGNAL
			+6V[8A4]
			+12V[8A4]
	-12V[8A4]		
			+24V[8A4]
	-24V[8A4]		
		34	GND[8A4]
		38	
		42	GND[8A4]

INTERNAL SIGNALS	
SIGNAL	LOCATION
BA	(3A3)(3B3)(4A4)(6A3)
CB*	(5A3)(3A1)(4A4)(6A2)
F*	[4B4](3A1)(5B3)(6A2)
[illegible]	([illegible]B3)(3A2)(3A1)(3B1)(4B1)
+5V	(8B4)(3B1)(4B2)(7B1)
+6V	[8A4]
+12V	[8A4]
+24V	[8A4](6B3)
-12V	[8A4]
-24V	[8A4](6B3)

NUCLEAR DATA INC
POST OFFICE BOX 451 PALATINE ILLINOIS [illegible]

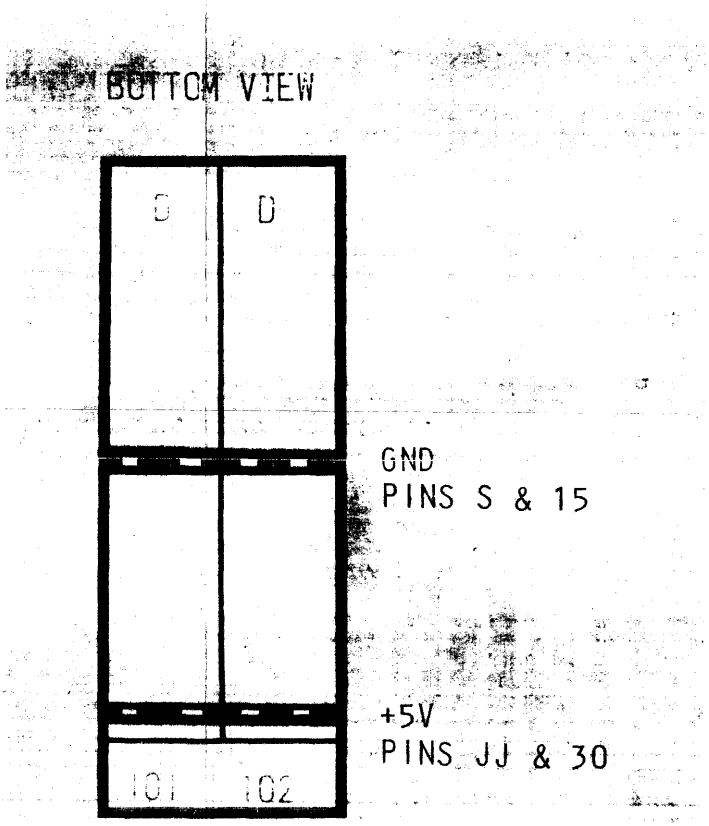
SYSTEM DIAGRAM
ADC ND-560
(CONNECTOR & REFERENCE TABLES)

DRAWN BY: R M G	CHECKED BY: [illegible]	SHEET [illegible]
DATE DRAWN: 5-10-72	APPROVED BY:	188-0915 [illegible]



ADC/ND560
LOADING DIAGRAM
SHEET 10 OF 11

L88-0415-00



ADC/ND560

BUSSING DIAGRAM

SHEET 11 OF 11

L88-0415-00