Microdata

Micro 820 Computer

GENERAL DESCRIPTION

The MICRO 820 is a high-speed microprogrammed general-purpose computer that provides a comprehensive instruction repertoire and a powerful input/output facility. System architecture is byte oriented. This allows variable precision operations and character manipulation to be highly efficient in both speed and memory utilization.

Use of high-speed read-only memories for macro control greatly reduces the number of CPU circuits which otherwise would be required to provide the powerful instructions of the MICRO 820. The superior price/performance ratio of the MICRO 820 is brought about by efficient core utilization and ease of programming.

The MICRO 820 system is designed to accommodate additional standard and special firmware inexpensively, thereby permitting the user to specify augmented capabilities such as multiply/divide instructions, BCD arithmetic, floating point arithmetic, trigonometric and transcendental functions, and fully buffered communication multiplexers.

Standard Features

Variable precision operations

Character/string manipulation

Stack processing

Memory addressing to 32,768 bytes
- 4096 and 8192 byte plug-in memory modules
- 32,768 bytes of memory in basic enclosure
- 1.1 microsecond memory cycle time

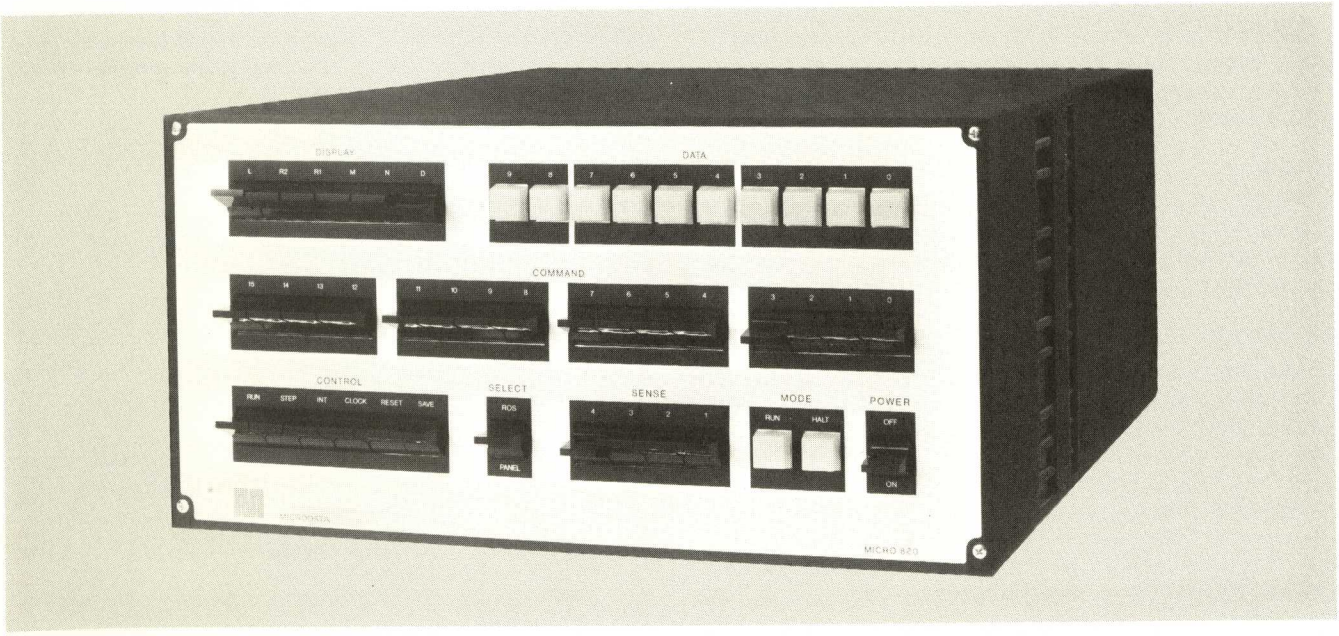
Six operational registers
- Accumulator (A) 16 bits
- Auxiliary accumulator (B) 16 bits
- Index register (X) 16 bits
- Program counter (P) 15 bits
- Overflow (O) 1 bit
- Word length control (W) 2 bits

Comprehensive instruction set including 102 basic operations
- Control (16)
- Multi-bit arithmetic and logical shifts (12)
- Conditional jumps (17)
- Input/Ouput (6)
- Inter-register (19)
- Stack control (8)
- Character/string manipulation (4)
- Memory reference including jump, compare and variable word length operations (20)

Eight operand addressing modes
- Direct to page 0 (first 256 bytes)
- Direct relative to P (±128 bytes)
- Indirect to page 0 (first 256 bytes)
- Indirect relative to P (±128 bytes)
- Indexed (to 32,768 bytes)
- Indexed with bias (to 32,768 bytes)
- Extended address (to 32,768 bytes)
- Literal

Multi-precision 1, 2, 3 or 4 byte load, store and arithmetic operations

Flexible I/O facilities
- Programmed transfers to/from A register, B register and memory
- Concurrent buffered I/O
- Direct memory access



Expandable priority interrupt system

Processor options
- Real-time clock
- Power-fail detect and automatic restart
- Memory parity detect and interrupt

Built-in bootstrap loader in non-volatile read-only memory

Standard supplied software
- Loaders
- Teletype debug and operating system
- Two-pass assembler
- Text editor
- Diagnostics

Optional Software Available
- "Basic" programming language
- Executive program
- File management program
- Data management program

TTL integrated circuitry
Power: 115/230 vac, 47-63 cycle, 380 watts
Environment: 0-50°C
Dimensions: 8¾ inches high, 19 inches wide, 23 inches deep

ORGANIZATION

Basic elements of the MICRO 820 include the operational registers, core memory, interrupt system, input/output system, and control section.

Registers

The MICRO 820 contains six operational registers which are accessible to the programmer. These operational registers occupy nine of the sixteen file registers of the basic MICRO 800 hardware; the remaining seven file registers are used for internal operations and buffering but are not directly accessible.

Core Memory

The magnetic core memory is organized into pluggable modules of 1024, 4096 or 8192 bytes each. It is byte addressable, each byte containing eight information bits. And it may be expanded to four 8192 byte modules, a total of 32,768 bytes within the basic 8¾ inch cabinet. A direct memory access (DMA) selector channel option allows interfacing peripheral devices directly with memory providing transfer rates of up to 909,000 bytes per second.

Interrupts

The MICRO 820 priority interrupt system provides for internal processor interrupts on power failure and real time clock and external interrupts on the byte I/O bus, each with its own unique interrupt memory address and priority assignment.

Control Section

The control section and associated read only memory provide the operational architecture and basic instruction repertoire through a series of microprogrammed sequences which operate at 220 nanoseconds per command. The basic MICRO 820 system employs three pages of 256 word (16 bit) high-speed read-only memories. The system read only memory is expandable to eight pages of 256 words, a total of 2048 words permitting significant architectural expansion in instruction repertoire and in application oriented input/output systems.

INSTRUCTION REPERTOIRE

Control

The control-group instructions are single byte instructions which provide specific control functions.

Code	Mnemonic	Description
00	HLT	HALT
01	TRP	TRAP
02	ESW	ENTER SENSE SWITCHES
04	DIN	DISABLE INTERRUPT SYSTEM
05	EIN	ENABLE INTERRUPT SYSTEM
06	DRT	DISABLE REAL TIME CLOCK
07	ERT	ENABLE REAL TIME CLOCK
08	RO1	RESET OVERFLOW AND SET WORD LENGTH TO 1
09	RO2	RESET OVERFLOW AND SET WORD LENGTH TO 2
OA	RO3	RESET OVERFLOW AND SET WORD LENGTH TO 3
OB	RO4	RESET OVERFLOW AND SET WORD LENGTH TO 4
OC	SO1	SET OVERFLOW AND SET WORD LENGTH TO 1
OD	SO2	SET OVERFLOW AND SET WORD LENGTH TO 2
OE	SO3	SET OVERFLOW AND SET WORD LENGTH TO 3
OF	SO4	SET OVERFLOW AND SET WORD LENGTH TO 4
34	NOP	NO OPERATION

Conditional Jumps

The conditional jump instructions are a two byte format. The first byte provides the operation code which includes the condition being tested and whether the jump will be made on the condition being true or false. The second byte contains an 8-bit signed value which specifies a jump location relative to the program counter which holds the address of the next instruction to be executed.

Code	Mnemonic	Description
10	JOV	JUMP IF OVERFLOW SET
11	JAZ	JUMP IF A EQUAL TO ZERO
12	JBZ	JUMP IF B EQUAL TO ZERO
13	JXZ	JUMP IF X EQUAL TO ZERO
14	JAN	JUMP IF A NEGATIVE
15	JXN	JUMP IF X NEGATIVE
16	JAB	JUMP IF A EQUALS B
17	JAX	JUMP IF A EQUALS X
18	NOV	JUMP IF OVERFLOW NOT SET
19	NAZ	JUMP IF A NOT EQUAL TO ZERO
1A	NBZ	JUMP IF B NOT EQUAL TO ZERO
1B	NXZ	JUMP IF X NOT EQUAL TO ZERO
1C	NAN	JUMP IF A NOT NEGATIVE
1D	NXN	JUMP IF X NOT NEGATIVE
1E	NAB	JUMP IF A NOT EQUAL TO B
1F	NAX	JUMP IF A NOT EQUAL TO X
5A	JEP	JUMP IF EVEN PARITY

Shifts

The shift group of instructions provides both arithmetic and logic shifts of A register, B register and A and B registers together. A signed shift count is specified in the second byte of the instructions.

Code	Mnemonic	Description
20	LLA	LOGICAL LEFT A
21	LLB	LOGICAL LEFT B
22	LLL	LOGICAL LEFT LONG
24	LRA	LOGICAL RIGHT A
25	LRB	LOGICAL RIGHT B
26	LRL	LOGICAL RIGHT LONG
28	ALA	ARITHMETIC LEFT A
29	ALB	ARITHMETIC LEFT B
2A	ALL	ARITHMETIC LEFT LONG
2C	ARA	ARITHMETIC RIGHT A
2D	ARB	ARITHMETIC RIGHT B
2E	ARL	ARITHMETIC RIGHT LONG

Register Operate

The register operate group of single byte instructions provides for special arithmetic and logical operations on individual registers and between registers.

Code	Mnemonic	Description
40	ORA	OR B WITH A
41	XRA	EXCLUSIVE-OR B WITH A

Code	Mnemonic	Description
42	ORB	OR A WITH B
43	XRB	EXCLUSIVE-OR A WITH B
48	INA	INCREMENT A
49	INB	INCREMENT B
4A	OCA	ONE'S COMPLEMENT A
4B	OCB	ONE'S COMPLEMENT B
44	INX	INCREMENT X
45	DCX	DECREMENT X
46	AWX	ADD WORD LENGTH TO X
47	SWX	SUBTRACT WORD LENGTH FROM X
4C	TAX	TRANSFER A TO X
4D	TBX	TRANSFER B TO X
4E	TXA	TRANSFER X TO A
4F	TXB	TRANSFER X TO B
58	MST	MULTIPLY STEP
59	ADX	ADD TO X
5B	EBX	EXCHANGE B AND X

Stack Control

The stack control group of instructions provides for CPU context switching of all active registers to and from a designated stack. The stacking capability of the MICRO 820 is efficient in processing multiple external interrupts and in employing reentrant coding techniques.

Code	Mnemonic	Description
50	RTN	RETURN
51	CAL	CALL
52	PLX	PULL X
53	PSX	PUSH X
54	PLA	PULL A
55	PSA	PUSH A
56	PLB	PULL B
57	PSB	PUSH B

Character/String Manipulation

The character/string manipulation group of instructions provides the capability to process both individual characters and strings of characters in a manner compatible to common Input-Output operations and communications processing.

Code	Mnemonic	Description
5C	MOV	MOVE
5D	GCC	GENERATE CYCLIC CODE
5E	SCH	SEARCH
5E	SCH	SEARCH NOT
5F	GAP	GENERATE ASCII PARITY

Memory Reference

The 20 instructions of the memory reference group obtain their operands from memory. The operand memory location is addressed by one of eight modes. The number of bytes required for the instruction depends on the addressing mode and the length of the operand.

Code	Mnemonic	Description
60	JMP	JUMP
68	RTJ	RETURN JUMP
70	IWM	INCREMENT WORD IN MEMORY
78	DWM	DECREMENT WORD IN MEMORY
80	LDX	LOAD X
88	STX	STORE X
90	LDB	LOAD B
98	STB	STORE B
A0	ADA	ADD TO A
A8	ADV	ADD VARIABLE
B0	SBA	SUBTRACT FROM A
B8	SBV	SUBTRACT VARIABLE
C0	CPA	COMPARE A (LESS THAN, EQUAL TO, GREATER THAN)
C8	CPV	COMPARE VARIABLE (LESS THAN, EQUAL TO, GREATER THAN)
D0	ANA	AND
D8	ANV	AND VARIABLE
E0	LDA	LOAD A
E8	LDV	LOAD VARIABLE
F0	STA	STORE A
F8	STV	STORE VARIABLE

INPUT/OUTPUT OPERATIONS

Three types of Input/Output are available: Program-controlled transfer of data bytes via the Byte Input/Output Bus. Buffered concurrent transfer of data bytes via the Byte Input/Output Bus. Direct transfer to memory via the direct memory access (DMA) channel.

The Standard Byte I/O Bus provides a path for transfer of data, control, and status between the processor and external peripheral devices. The direct memory access (DMA) channel option communicates directly with memory.

Byte Input/Output Instructions

Byte programmed Input/Output operations provide transfer of data, control and status over the Byte I/O channel. This channel permits intermixed program and concurrent I/O transfers. Up to 32 devices on the bus may be operating in the Byte I/O or concurrent block transfer mode at the same time.

Code	Mnemonic	Description
31	IBA	INPUT BYTE TO A
32	IBB	INPUT BYTE TO B
33	IBM	INPUT BYTE TO MEMORY
39	OBA	OUTPUT BYTE FROM A
3A	OBB	OUTPUT BYTE FROM B
3B	OBM	OUTPUT BYTE FROM MEMORY

Concurrent Input/Output

The concurrent I/O allows for block transfers between the external device on the Byte I/O bus and memory, at an asynchronous rate up to 20,000 bytes per second. The transfers are fully automatic, and once started, proceed without program intervention. Concurrent I/O takes priority over instruction execution.

External Interrupts

External interrupts originate with device controllers or interrupt modules on the Byte I/O bus. An interrupt module provides control of eight external interrupt signals. Device controllers may also generate interrupts to signify individual data transfers, end of operation, or error conditions.

The external interrupt system contains a single interrupt line, a priority line, and a select line. A device may initiate an interrupt request only if priority has been received from higher level interrupts on the priority chain. Devices not requiring interrupt service will propagate priority to the next device in line.

OPERATOR CONTROLS

Two control consoles are available: system console and basic console. These consoles differ in their number of displays and controls. This range of consoles permits the user to tailor the cost to meet the control and display capability required for a particular application.

STANDARD SYSTEM EXPANSION ELEMENTS AND OPTIONS

Magnetic Core Memory

Item	Description
8218	1,024 Byte (8 bit) core memory module. (P/N10001040)
8248	4,096 Byte (8 bit) core memory module. (P/N1000926)
8288	8,192 Byte (8 bit) core memory module. (P/N1000925)

Central Processor Options

Item	Description
8406	Power Fail/Auto-Restart, and Real Time Clock (P/N0594004)
8421	Communications Multiplexer (firmware) Power Fail/Auto-Restart, Real Time Clock, and Communications Rate Generators. (P/N10001038)

General Purpose and Utility Interfaces

Item	Description
8701	Teletype Controller and Interface, employs serial/parallel conversion and buffering, transfers are programmed control. (P/N0549002)
8722	General Purpose Wire-Wrap Board including 64 each 16-pin sockets and 6 each 24-pin sockets, occupies one Input/Output slot. (P/N1000755)
8703	Priority Interrupt Board, provides eight levels of priority interrupt expansion with individual arm/disarm and request storage. (P/N1000781)
8704	Direct Memory Access (DMA)—Selector Channel, block or multiple buffer modes, includes end of transfer interrupt, will accommodate up to four devices. (P/N1000482)
8705	General Purpose I/O Interface—provides 32 input and 32 output lines under program control: can be used for interfacing incremental tape drives, MUX-ADC's, DAC's and other low speed peripheral devices. (P/N0637001)
8710	General Purpose Byte I/O System, provides independent Input/Output controllers each with 8-bit data transfers in the programmed, concurrent I/O or interrupt modes. Is used as interface for paper tape reader and punch, buffered line printer, and character oriented devices. (P/N10001033)

Communications Interfaces

Item	Description
8800	Full Duplex Synchronous Modem Interface, provides dual independent control for the transmission and receiving elements of synchronous modems operating up to 9600 baud. Each control element includes programmed, concurrent I/O, and interrupt data transfer modes. The unit will accommodate programmed sync patterns 5, 6, 7, or 8-bit character size, and standard baud rates to 9600. Interface signals are EIA Standard RS-232-C. (P/N1000825)
8801-1	Synchronous Modem Interface with Auto-Call/Answer unit provides full duplex operation in the programmed transfer mode or half full duplex operating in the concurrent I/O mode with 201 Series modems or other synchronous modems up to 9600 baud with EIA Standard RS-232-C levels. (P/N1000858)
8803-1	Eight Channel Low Speed Modem Interface—provides eight full duplex RS-232-B interfaces. (P/N0437001)
8803-2	Sixteen Channel Low-Speed Modem Interface—provides sixteen full duplex RS-232-B interfaces. (P/N0437002)
8803-3	Eight Channel Low-Speed Modem Interface—provides eight full duplex RS-232-B interfaces and modem control interfaces. (P/N0437003)
8804-1	Eight channel teletype control—provides eight full duplex 20ma teletype interfaces. (P/N0496001)
8804-2	Sixteen channel teletype control—provides sixteen full duplex 20ma teletype interfaces. (P/N0496002)
8805	Four Channel Communications Interface and character buffered Controller, provides simultaneous operation of four full duplex asynchronous lines with four independent controllers. Each controller is programmable for eight combinations of baud rate from 75 to 2400 and character lengths from 7.5 to 10 bits. EIA Standard RS-232-C or teletype 20ma current loop can be selected. (P/N1000991)
8806	Eight Channel Communications Interface and character buffered Controller provides simultaneous operation of 8 full duplex asynchronous lines. Eight combinations of baud rate from 75 to 2400 and character lengths from 7.5 to 10 bits can be selected, will apply to all 8 lines. EIA Standard RS-232-C or Teletype 20ma current loop can be selected. (P/N1000994)
8807	Automatic Call Unit Interface and Controller, provides control functions for either four Bell Model 801 Automatic Call Units or one 16-channel single port unit with EIA Standard RS-232-C Interface Levels. (P/N1000829)

Peripheral Device Interfaces

Item	Description
8901-1	Magnetic Tape Transport Controller and Interface, will handle 1 to 4 of 7 or 9 track transports, data transfer through concurrent I/O channel. (P/N1000987)
8902	Rotating Memory System Controller and Interface, for Disc Drive Units, data transfer through DMA selector channel, cables and connectors are included. (P/N10001041)
8917	Card Reader Controller and Interface.

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