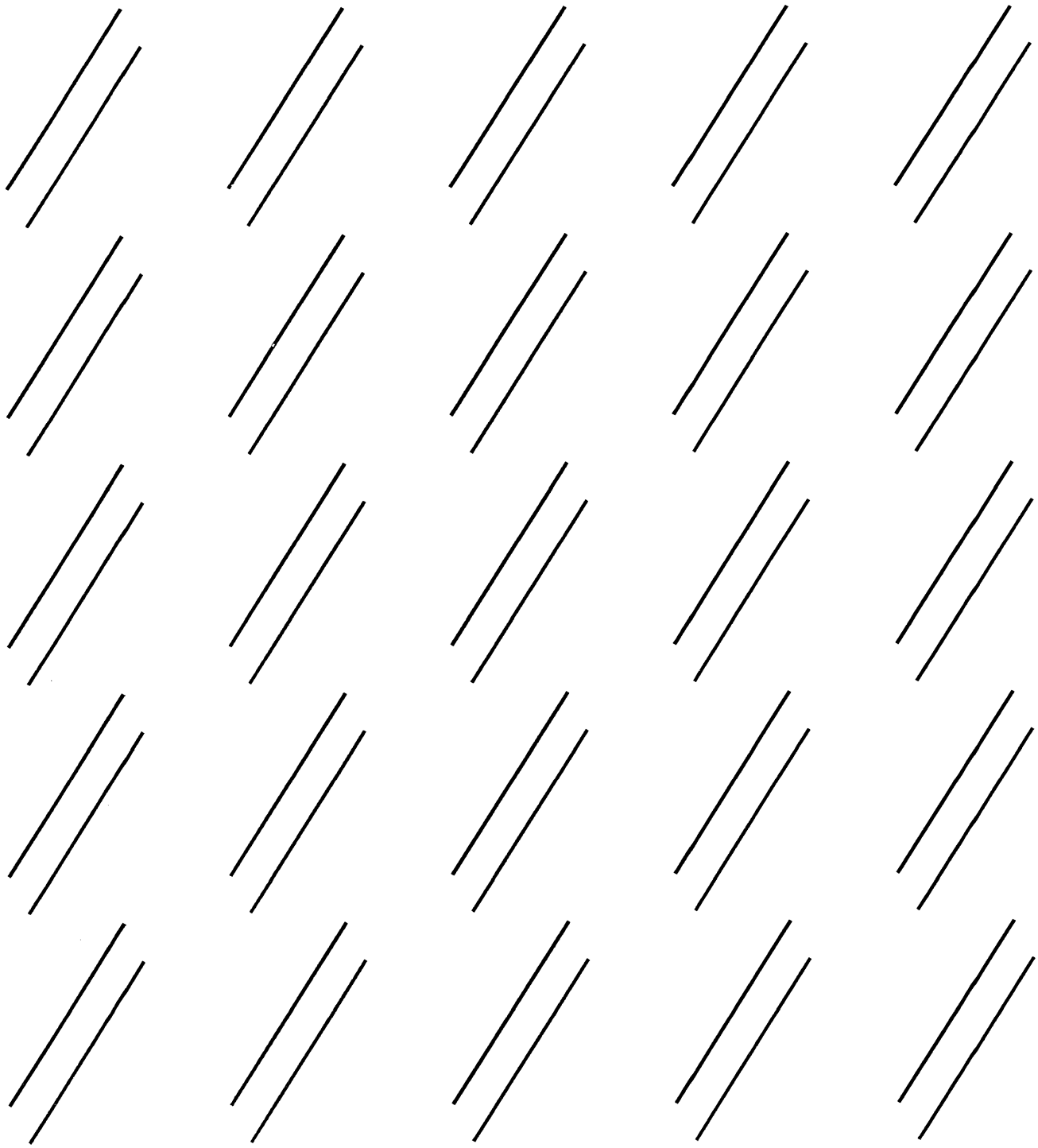
XT-8000E/EH

Product Specification and OEM Technical Manual

Revision F/April 1991



Maxtor®

XT-8000E/EH

Product Specification
and OEM Technical Manual

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Revision F
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WARRANTY

Maxtor warrants the XT-8000E/EH Family of disk drives against defects in materials and workmanship for a period of two years, for the original purchaser. This warranty can be extended an additional three years for a nominal fee. Direct any questions regarding the warranty to your Maxtor Sales Representative. Maxtor maintains Customer Service Centers for the repair/reconditioning of all Maxtor products. Direct all requests for repair to the Maxtor Service Center in your area. This assures you of the fastest possible service.

REGULATORY APPROVALS

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PREFACE

Maxtor reserves the right to make changes and/or improvements to its products without incurring any obligation to incorporate such changes or improvements in units previously sold or shipped.

Maxtor publishes descriptive brochures and data sheets, and an OEM technical manual for each product line. In addition, important changes to a product are conveyed in technical bulletins sent to all product customers of record. Changes that affect the content of any manual are covered by publishing addenda or revisions to the affected manual.

REFERENCE NUMBERS

For information concerning drive set-up and operation, contact Maxtor Technical Support at (800) 356-5333 or call the 24 hour Tech. Support hotline at (408) 432-3730.

To receive Maxtor product literature via facsimile machine, call the MaxFax hotline at (303) 678-2618. For various information on distributors, drive parameters, installation tips, and application notes as well as Maxtor product literature, the Maxtor Bulletin Board may be accessed via modem at (303) 678-2222.

For information regarding PC AT/XT™, PS-2™, and Macintosh® applications, contact Storage Dimensions Inc. (SDI) Technical Support at (408) 879-0300.

PRECAUTION FOR DRIVE HANDLING

Caution: *Condensation can cause damage to the disk drive. To avoid condensation damage to the drive, let the drive acclimate to room temperature before removing it from its protective bag, as specified in the chart below.*

Acclimation Time	Storage Temperature Below Current Room Temperature by:
24 Hours	Greater than 10° C (18° F)
16 Hours	6 -10° C (10 - 17° F)
5 Hours	3 - 5° C (5 -9° F)
0 Hours	0 - 2°C (0 - 4° F)

Acclimation Time Table

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1.0 INTRODUCTION

The XT-8000E™ Family disk drives are low cost, high capacity, high performance random access storage devices using from five to eight nonremovable 5.25-inch disks as storage media. Each disk surface employs one moveable head to access 1,632 data tracks. The total unformatted capacity of the disk drives ranges from 410.09 to 768.92 megabytes.

The disk incorporates the Enhanced Small Device Interface (ESDI) high performance 5.25-inch standard. Among the resultant benefits are a 15 megabit per second transfer rate, status and configuration reporting across the interface, and nonreturn to zero (NRZ) data transfer.

Low cost and high performance are achieved through the use of a rotary voice coil actuator and a closed loop servo system using a dedicated servo surface. The innovative MAXTORQ™ rotary voice coil actuator provides maximum average access times of 16 or 18 milliseconds and a track-to-track access time of 3 milliseconds for the standard products and maximum average access times of 15.0 or 15.5 milliseconds and a track to track access time of 2.5 milliseconds for the XT-8000EH high performance products. This level of performance is usually achieved only with larger, higher powered linear actuators. The closed loop servo system and dedicated servo surface combine to allow state-of-the-art recording densities with 1,376 tracks per inch (tpi) and 31,596 flux changes per inch (fci)) in a 5.25-inch package.

High capacity is achieved by a balanced combination of high areal recording density, run-length limited (RLL) data encoding techniques, and high density packaging techniques. Maxtor's advanced MAXPAK™ electronic packaging techniques use miniature surface mount devices to allow all electronic circuitry to fit on one printed circuit board (PCB). Advanced head flexures, and thin film sliders, allow closer spacing of disks, and therefore allow a higher number of disks in a 5.25-inch package. Maxtor's unique integrated drive motor/spindle design allows a deeper head disk assembly (HDA) casting than conventional designs, thus permitting more disks to be used.

The electrical interface is compatible with the industry standards established by the ESDI committee. The drive size and mounting are also identical to the industry standard 5.25-inch floppy and Winchester disk drives, and the disk uses the same direct current (DC) voltages and connectors. No alternating current (AC) power is required.

Key features of the drive include:

- Storage capacity of 410.09 to 768.92 megabytes nominal unformatted.
- Same physical size and mounting as standard floppy disk drives.

- Same control and data cabling as ST-506/412 interface drives.
- Same DC voltages as standard floppy disk drives.
- No AC voltage required.
- Rotary voice coil actuator and closed loop servo system for fast, accurate head positioning.
- Microprocessor-controlled servo for fast access times, high reliability, and high density functional packaging.
- 15.0 megabit per second transfer rate.
- ESDI interface.
- Track capacity of 31,410 bytes minimum, unformatted.
- Single PCB for improved reliability.
- Automatic actuator lock.
- Brushless DC spindle motor inside disk hub.
- Microprocessor-controlled spindle motor for precision speed control (±0.1%) under all load conditions.
- Dynamic braking during power down cycle.
- User selectable hard or soft sectors.
- Synchronization of spindle motors for parallel data transfer of multiple drives.

2.0 PRODUCT SPECIFICATIONS

2.1 PHYSICAL SPECIFICATIONS

	EQUIPMENT OPERATING	EQUIPMENT NON-OPERATING
AMBIENT TEMPERATURE	50° F to 122° F (10° C to 50° C)	-40° F to 149° F (-40° C to 65° C)
MAXIMUM TEMPERATURE GRADIENT	18° F/hr (10° C/hr), Below Condensation	18° F/hr (10° C/hr), Below Condensation
RELATIVE HUMIDITY	8 to 80% Non-Condensing with Maximum Slew Rate of 10% Per hour	8 to 80% Non-Condensing with Maximum Slew Rate of 10% per hour
MAXIMUM WET BULB	26.7° C	26.7° C
MAXIMUM ELEVATION	10,000 ft Maximum	-1,000 ft to 40,000 ft
VIBRATION (Inputs To Frame Of Drive)	All Axes, 5-40 Hz, 0.006 in. P-P 40-500 Hz, 0.5 G Peak Acceleration	All Axes, 5-31 Hz, 0.02 in. P-P 31-500 Hz, 1.0 G Peak Acceleration
SHOCK (Inputs To Frame Of Drive)	5 G with 11 msec Pulse Width, Half Sine Wave (All Axes)	25 G with 11 msec Pulse Width, Half Sine Wave (All Axes)

Table 2-1
Environmental Limits

HEIGHT	= 3.25 in. (82.55 mm)
WIDTH	= 5.75 in. (146.05 mm)
DEPTH	= 8.20 in. (208.28 mm)
WEIGHT	= 7.1 lb (3.2 kg)
SHIPPING WEIGHT	= 9.3 lb (4.2 kg)
HEAT DISSIPATION	= 27 W Typical, 35 W Max.

Table 2-2
Mechanical Dimensions

NOTE: Forced air cooling of approximately 500 linear feet per minute across the PCB is recommended.

2.2 PERFORMANCE SPECIFICATIONS

	XT-8380E	XT-8760E	XT-8610E	XT-8380EH	XT-8760EH
CAPACITY, UNFORMATTED					
PER DRIVE (Mbytes)	410.09	768.92	615.13	410.09	768.92
PER SURFACE (Mbytes)	51.26	51.26	51.26	51.26	51.26
PER TRACK (Bytes) MINIMUM	31,410	31,410	31,410	31,410	31,410
CAPACITY, FORMATTED (512 Bytes/Sector)					
PER DRIVE (Mbytes)	360.97	676.82	541.45	360.97	676.82
PER SURFACE (Mbytes)	45.12	45.12	45.12	45.12	45.12
PER TRACK (Bytes)	27,648	27,648	27,648	27,648	27,648
SECTOR/TRACK **	54	54	54	54	54
TRANSFER RATE, MBITS/SEC	15.080	15.080	15.080	15.080	15.080
MAX ACCESS TIME, MSEC*					
AVERAGE	16	18	18	15	15.5
TRACK-TO-TRACK	3	3	3	2.5	2.5
FULL STROKE	35	35	35	30	30
TYPICAL ACCESS TIME, MSEC*					
AVERAGE	14.5	16.5	15.5	13.5	14.0
TRACK-TO-TRACK	2.5	2.5	2.5	2.0	2.0
FULL STROKE	32	33	33	28	28

*Includes Settling
** Hard or Soft Sector, with One Byte Granularity Supported
Track format to support 54 sectors/track
controller dependent

Table 2-3
Performance Specifications

2.3 FUNCTIONAL SPECIFICATIONS

	XT-8380E/EH	XT-8760E/EH	XT-8610E
ROTATIONAL SPEED (rpm) *	3,600	3,600	3,600
AVERAGE LATENCY (msec)	8.33	8.33	8.33
RECORDING DENSITY (bpi)	31,596 **	31,596 **	32,320 **
FLUX DENSITY (fci)	21,064	21,064	24,300
TRACK DENSITY (tpi)	1,376	1,376	1,376
CYLINDERS	1,632	1,632	1,632
TRACKS	13,056	24,480	19,584
SECTORS (54 Sectors/Track)	705,024	1,321,920	1,057,536
DATA HEADS	8	15	12
SERVO HEADS	1	1	1
DISKS	5	8	7

*Accurate to ±0.1% ** 1,7 RLL Encoding

Table 2-4
Functional Specifications

2.4 RELIABILITY SPECIFICATIONS

MTBF	≥150,000 Hours, POH, Typical Usage
PM	Not Required
MTTR	30 Minutes
COMPONENT DESIGN LIFE	5 Years

Table 2-5
Reliability Specifications

2.5 ERROR RATES

SOFT READ ERRORS	10 per 10^{11} Bits Read
HARD READ ERRORS*	10 per 10^{13} Bits Read
SEEK ERRORS	10 per 10^{7} Seeks

*Not Recoverable within 16 Retries

Table 2-6
Error Rates

VOLTAGE (NOMINAL)	+12 V DC	+5 V DC
REGULATION	±5%	±5%
CURRENT (Typical)	1.5 A	1.7 A
CURRENT (Maximum)	4.5 A *	1.9 A
RIPPLE (Maximum, P-P)	120 mV	50 mV

* Potential current surge greater than 4.5A during rise time, to charge capacitors at power on, is possible for power supplies with fast rise times (less than 15 msec). However, the capacitors are eliminated on the XT-8000EH products.

Table 2-7
DC Power Requirements

2.6 STANDARDS AND REGULATIONS

It is intended that the Maxtor XT-8000E Family of disk drives satisfy the following standards and regulations.

UNDERWRITERS LABORATORIES (UL) is United States safety; UL 478, Standard for Safety, Electronic Processing Units and Systems.

CANADIAN STANDARDS ASSOCIATION (CSA) is Canadian safety; CSA C22.2 No. 220, 1986, Information Processing and Business Equipment (Consumer and Commercial Products).

VERBAND DEUTSCHER ELECTROTECHNIKER (VDE) is German safety; VDE 0806/8.81, Safety of Office Appliances and Business Equipment.

3.0 FUNCTIONAL CHARACTERISTICS

3.1 GENERAL THEORY OF OPERATION

The drive consists of read/write and control electronics, read/write heads, a servo head, a head positioning actuator, media, and an air filtration system. The components perform the following functions:

- Interpret and generate control signals
- Position the heads over the desired track
- Read and write data
- Provide a contamination-free environment

3.2 READ/WRITE AND CONTROL ELECTRONICS

Drive electronics are packaged on a single PCB. This board, which includes two microprocessors, performs the following functions:

- Reading and writing of data
- Index detection
- Head positioning
- Head selection
- Drive selection
- Fault detection
- Voice coil actuator drive circuitry
- Track zero detection
- Recalibration to track zero on power up
- Track position counter
- Power and speed control for spindle drive motor
- Braking for the spindle drive motor
- Drive up-to-speed indication circuit
- Monitoring for write fault conditions
- Control of all internal timing
- Generation of seek complete signals
- RLL encoding/decoding
- Data separation
- Address mark detection (soft sector)
- Sector detection (hard sector)
- Spindle synchronization

3.3 DRIVE MECHANISM

A brushless DC drive motor, contained within the spindle hub, rotates the spindle at 3,600 revolutions per minute. The motor and spindle are designed to ensure a low vibration level. Dynamic braking is used to quickly stop the spindle motor when power is removed. The HDA is shock mounted to minimize transmission of vibration through the chassis or frame.

3.4 AIR FILTRATION SYSTEM

The disks and read/write heads are assembled in an ultra clean-air environment, and then sealed within the HDA. The HDA contains an internal absolute filter, mounted inside the casting, to provide constant internal air filtration. A second filter, located on the bottom of the base casting, permits pressure equalization between internal and ambient air. See Figure 3•1, Air Filtration System.

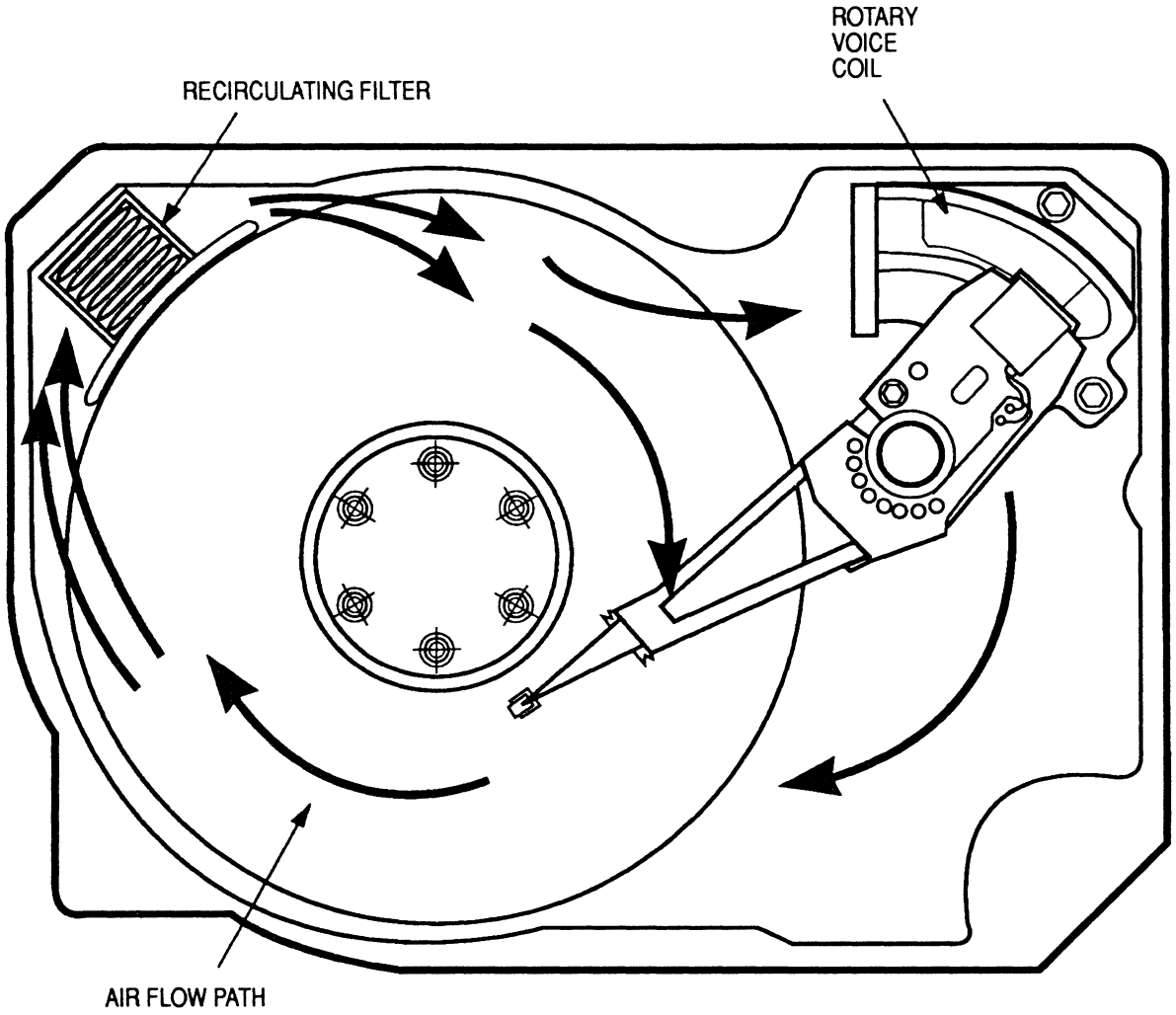


Figure 3•1
Air Filtration System

3.5 POSITIONING MECHANISM

The read/write heads are mounted on a head/arm assembly, which is then mounted on a ball bearing supported shaft. See Figure 3•2, Head Positioning System. The voice coil, an integral part of the head/arm assembly, lies inside the magnet housing when installed in the drive. Current from the power amplifier, controlled by the servo system, causes a magnetic field in the voice coil, which either aids or opposes the field around the permanent magnets. This reaction causes the voice coil to move within the magnetic field. Since the head/arm assemblies are mounted on the voice coil, the voice coil movement is

transferred, through the pivot point, directly to the heads, and positions the heads over the desired cylinder.

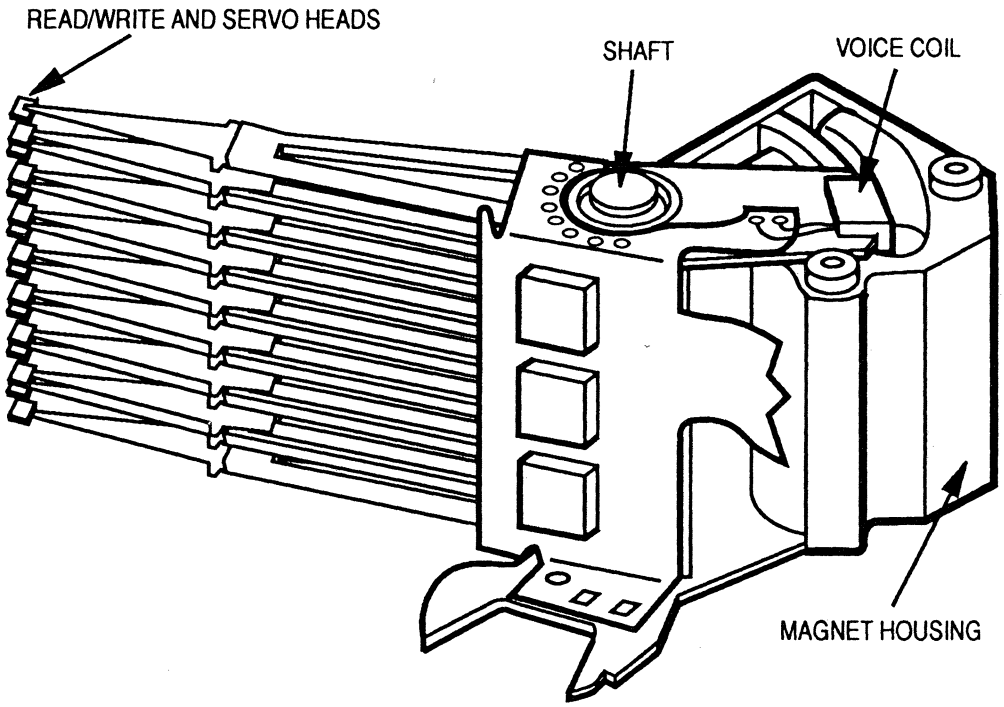


Figure 3-2
Head Positioning System

Actuator movement is controlled by the servo feedback signal from the servo head. The servo information is prewritten at the factory. This servo information is used as a control signal for the actuator to provide track-crossing signals during a seek operation, track-following signals during on cylinder operation, and timing information, such as index, sector pulses (hard sector) and servo clock.

3.6 READ/WRITE HEADS AND DISKS

The medium uses thin metallic film deposited on 130 millimeter diameter aluminum substrates. The coating formulation, together with the low load force/low mass Whitney-type heads, permit highly reliable contact start/stop operation. The metallic recording film yields high amplitude signals, and very high resolution performance, compared to conventional oxide coated medium. The metallic medium also provides a highly abrasion-resistant surface, decreasing the potential for damage caused by shipping shock and vibration.

Data on each of the data surfaces is read by one of 8 or 15 read/write heads, each of which accesses 1,632 tracks. There is one surface dedicated to servo information in each drive.

4.0 FUNCTIONAL OPERATION

4.1 POWER UP SEQUENCE

DC power (+5 volts and +12 volts) may be supplied to the drive in any order, but +12 volts DC are required to start the spindle motor. See Figure 4.1, Power Up Sequence (Jumper JP6 Open). The motor power up is controlled by the status of jumper JP6 on the drive electronics PCB assembly. (The location and function of all PCB jumpers are shown in Figures 8•1 through 8•6, Drive Jumper Options, and in Tables 8•6 through 8•11, Jumper Selections.)

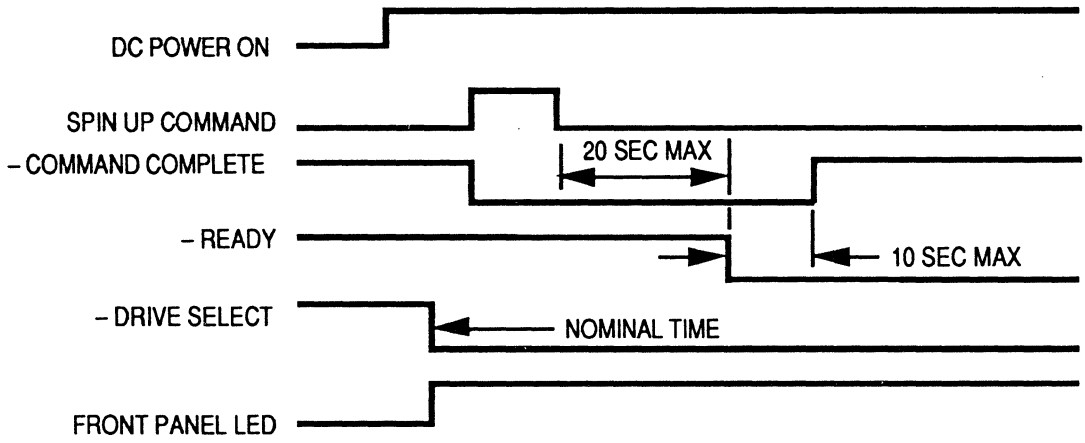


Figure 4•1
Power Up Sequence (Jumper JP6 Open)

If jumper JP6 is open, the spindle power up sequencing is initiated by the issuance of the START MOTOR CONTROL command.

When the spindle reaches full speed, the actuator lock automatically disengages and the heads then recalibrate to track zero. Upon successfully recalibrating, READY and COMMAND COMPLETE status signals are true. The unit does not perform any read, write, or seek functions until READY is true. (If after starting, 1,000 revolutions per minute is not reached in 7 seconds, an automatic shut down procedure is initiated; power to the spindle motor is shut off and the drive does not become READY.)

If jumper JP6 is shorted, the spindle power up sequencing is initiated by the application of DC power. (When shipped, the JP6 jumper is shorted.)

4.2 DRIVE SELECTION

Drive selection occurs when the controller places the address of the drive to be selected on the three drive select lines. See Figure 4•2, Drive Select Circuit, and Table 4•1, Drive Selection Matrix. Only the selected drive responds to the input signals, and only that drive's output signals are then gated to the controller. The details of setting the drive selection jumper are covered in section 8.1, Drive Address Selection Jumper.

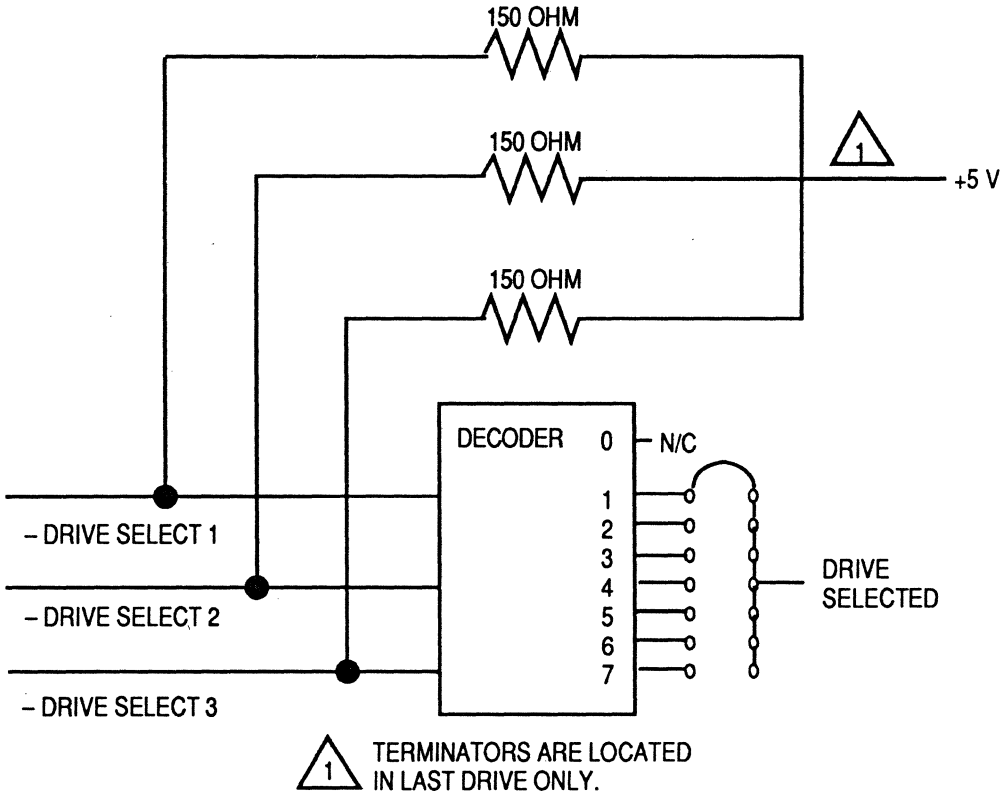


Figure 4•2
Drive Select Circuit

DRIVE SELECTED	DRIVE SELECT 3	DRIVE SELECT 2	DRIVE SELECT 1
None	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table 4•1
Drive Selection Matrix

4.3 DRIVE TERMINATION

If more than one Maxtor drive is used in a system, the terminator packs (RN13 and RN14) must be removed in all but the last drive in the string. Figures 8•1, 8•2, 8•3, 8•4, 8•5, and 8•6, Drive Jumper Options, show the location of RN13 and RN14.

5.0 ELECTRICAL INTERFACE

The interface to the drive can be divided into four separate categories, each of which is physically separated.

- Control signals
- Data signals
- DC power
- Auxiliary signals

All control lines are digital (open collector transistor-transistor logic (TTL)), and either provide signals to the drive (input) or signals to the host (output), via interface connection J1/P1. The data transfer signals are differential, and provide data either to (write) or from (read) the drive, via J2/P2.

Figure 5•1, Control Cable J1/P1 Signals, Table 5•1, Control Cable J1/P1 Pin Assignments, Figure 5•2, Data Cable J2/P2 Signals, and Table 5•2, Data Cable J2/P2 Pin Assignments, show connector pin assignments and interconnection of cabling between the host controller and drives.

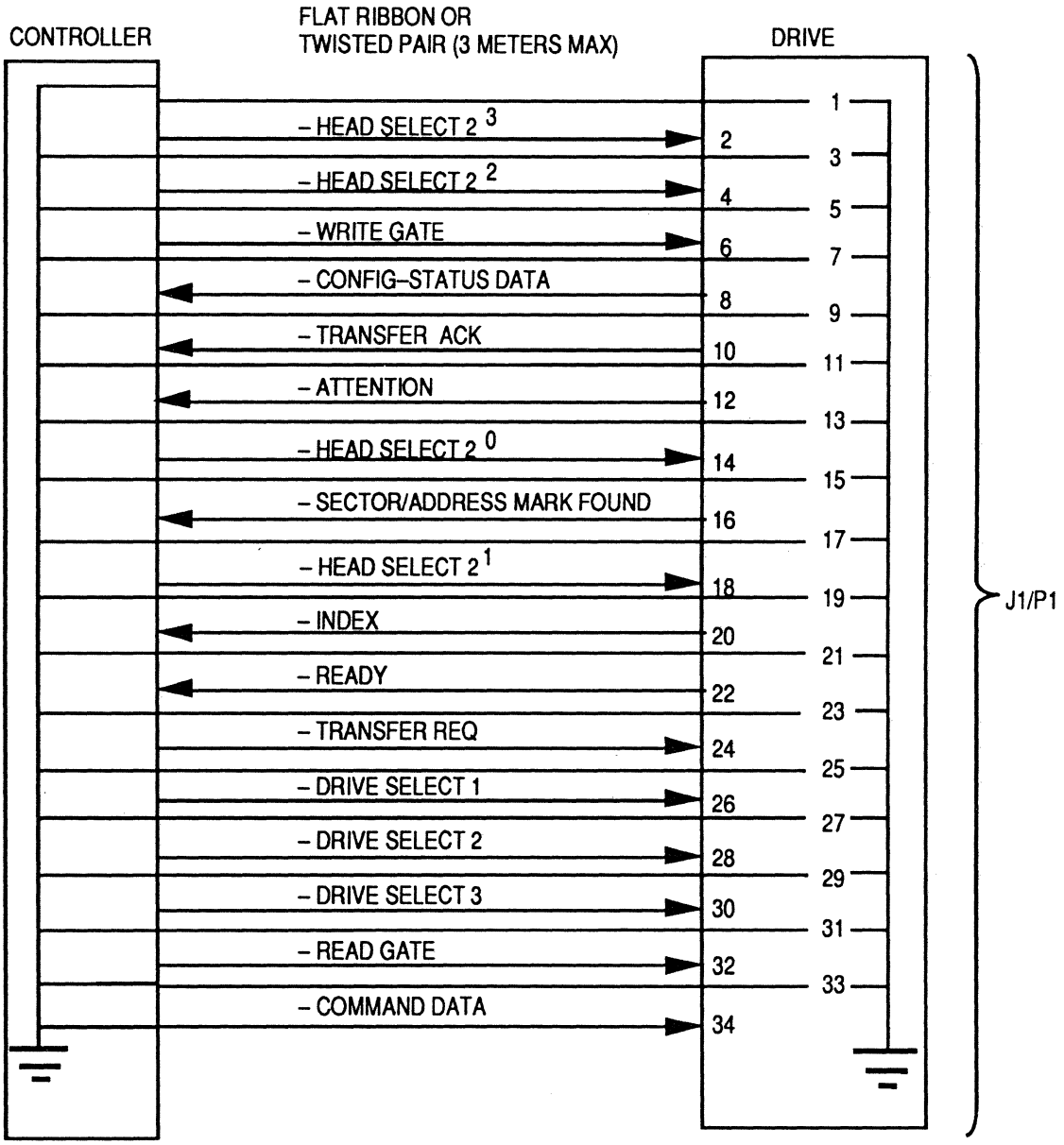


Figure 5-1
Control Cable J1/P1 Signals

SIGNAL NAME	SIGNAL PIN	GROUND PIN
– HEAD SELECT 2 ^{3}	2	1
– HEAD SELECT 2 ^{2}	4	3
– WRITE GATE	6	5
– CONFIG–STATUS DATA	8	7
– TRANSFER ACK	10	9
– ATTENTION	12	11
– HEAD SELECT 2 ^{0}	14	13
– SECTOR/ADDRESS MARK FOUND	16	15
– HEAD SELECT 2 ^{1}	18	17
– INDEX	20	19
– READY	22	21
– TRANSFER REQ	24	23
– DRIVE SELECT 1	26	25
– DRIVE SELECT 2	28	27
– DRIVE SELECT 3	30	29
– READ GATE	32	31
– COMMAND DATA	34	33

Table 5•1
Control Cable J1/P1 Pin Assignments

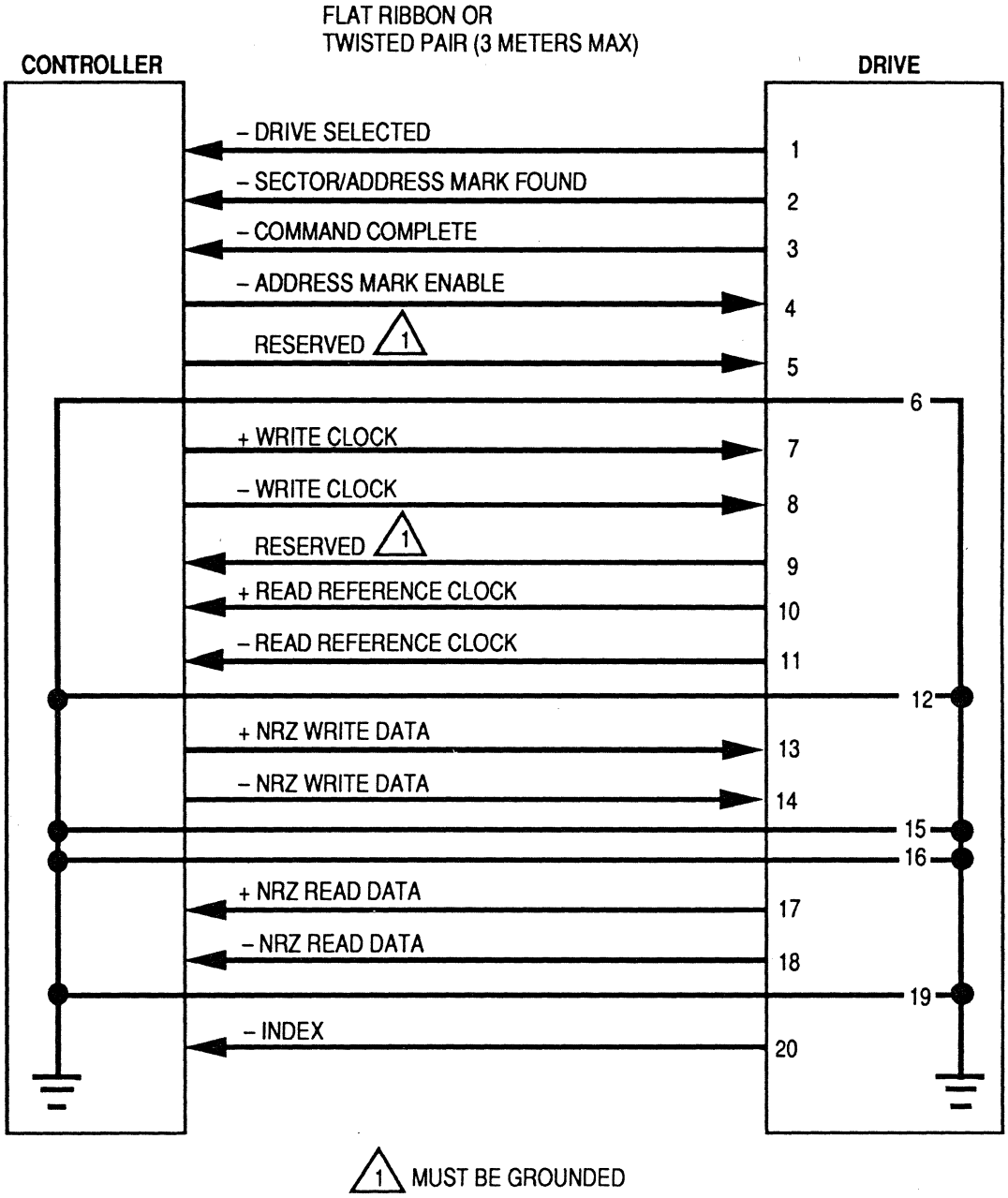
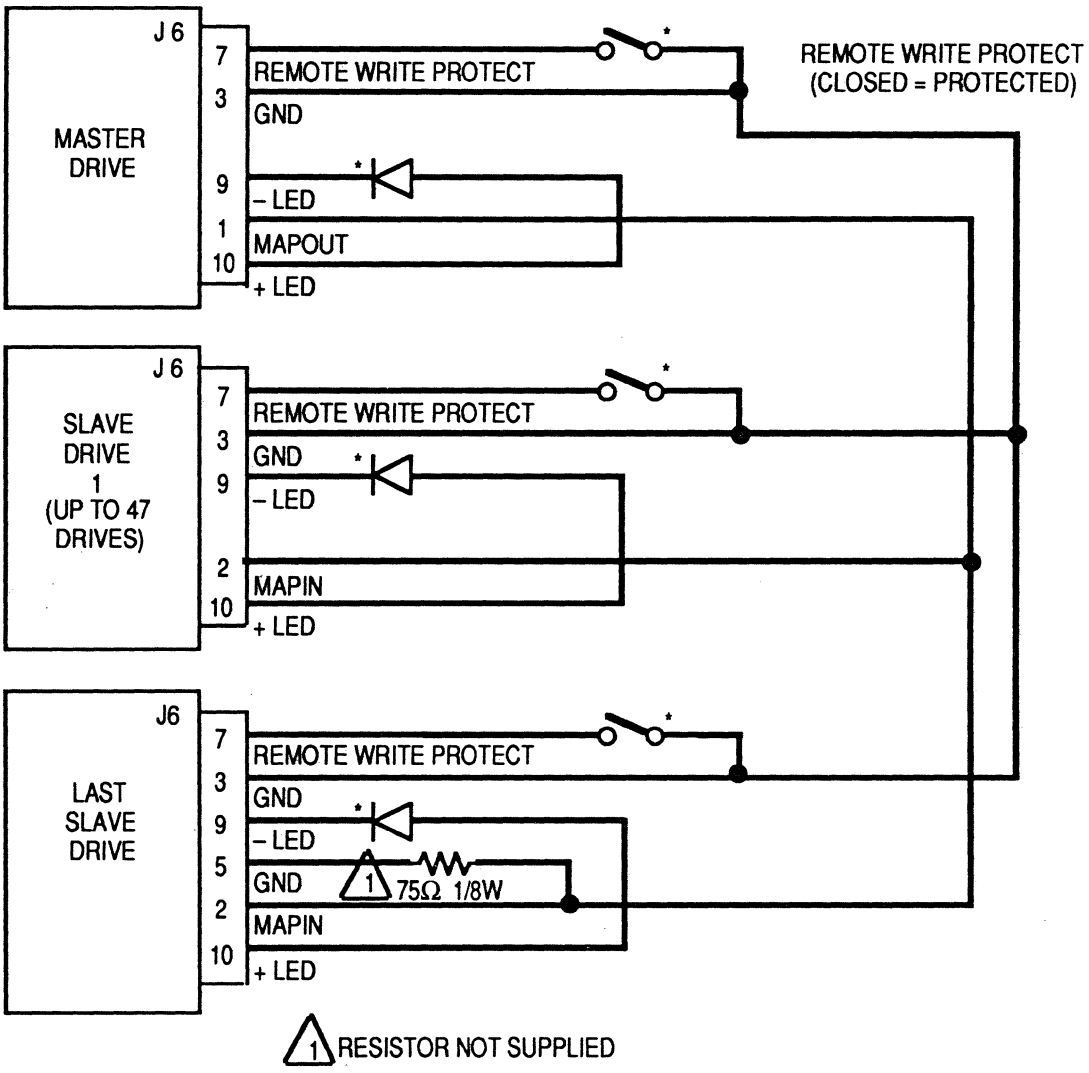


Figure 5-2
Data Cable J2/P2 Signals

SIGNAL NAME	SIGNAL PIN	GROUND PIN
– DRIVE SELECTED	1	
– SECTOR/ADDRESS MARK FOUND (not gated with DRIVE SELECTED)	2	
– COMMAND COMPLETE	3	
– ADDRESS MARK ENABLE (not gated with DRIVE SELECTED)	4	
Reserved	5	6
+/– WRITE CLOCK	7/8	
Reserved	9	
+/– READ/REF CLOCK	10/11	12
+/– NRZ WRITE DATA	13/14	15/16
+/– NRZ READ DATA	17/18	19
– INDEX (not gated with DRIVE SELECTED)	20	

Table 5•2
Data Cable J2/P2 Pin Assignments

Figure 5•3, Typical Auxiliary Cable, and Spindle Synchronization Connection, and Table 5•3, Auxiliary Cable (J6) Pin Assignments, show connector pin assignments and interconnection of cabling between drives for the auxiliary signals.



NOTE: *UP TO 48 SLAVE DRIVES ARE ALLOWED.*
THE MAXIMUM LED CURRENT IS 40 mA.
THE TERMINATOR IS APPLIED AT THE DRIVE CONNECTOR FARTHEST FROM THE MASTER DRIVE.
CONNECTION SHOWN FOR RIBBON CABLE.

Figure 5-3
Typical Auxiliary Cable, and Spindle Synchronization Connection

SIGNAL NAME	PIN
MAPOUT	1
MAPIN	2
GND	3
MAPIN	4
GND	5
KEY (N.C.)	6
REMOTE WRITE PROTECT	7
	8
- LED	9
+ LED	10

Table 5-3
Auxiliary Cable (J6) Pin Assignments

5.1 CONTROL INPUT LINES

The control input signals are of two types: those to be multiplexed in a multidrive system, and those intended to do the multiplexing. The signals to be multiplexed are WRITE GATE, TRANSFER REQ, and COMMAND DATA. The signals to do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.

The input lines have the following electrical specifications. Refer to Figure 5-4, Control Signals, Driver/Receiver Combination, for the recommended circuit.

TRUE: 0.0 V DC to 0.4 V DC = 1 @ -48 mA (max)
FALSE: 2.5 V DC to 5.25 V DC = 0 @ +250 µA (open collector)

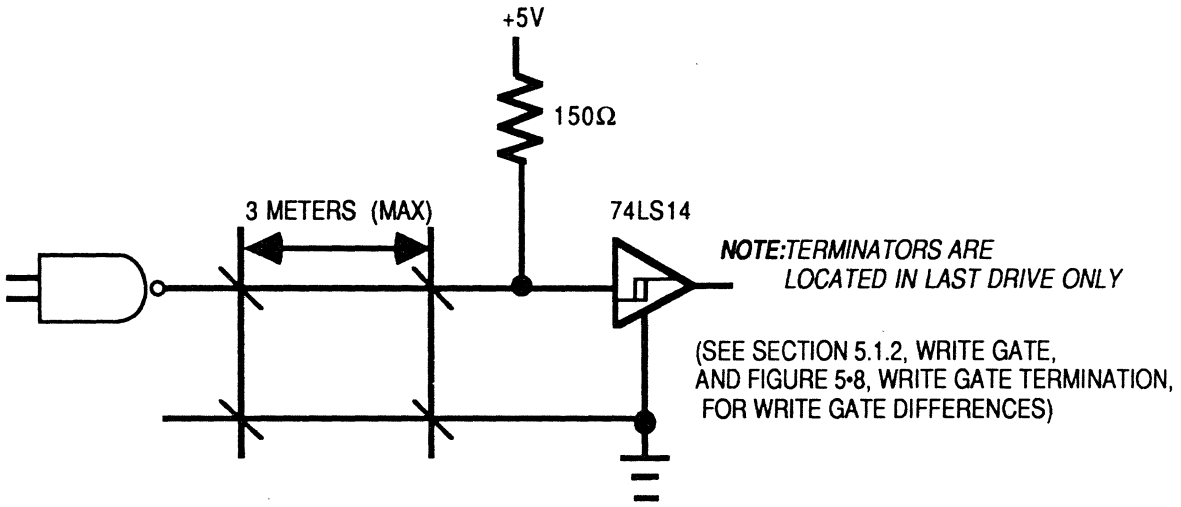


Figure 5•4
Control Signals, Driver/Receiver Combination

5.1.1 HEAD SELECT 2^0, 2^1, 2^2, 2^3

The four HEAD SELECT lines allow selection of each individual read/ write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Data heads are numbered and addressed continuously from zero through the maximum head number. When all HEAD SELECT lines are high (inactive), head zero is selected.

Addressing more heads than contained in the drive (eight heads for the XT-8380E, fifteen for the XT-8760E) results in a write fault when attempting to perform a write operation.

A 150 ohm resistor pack allows for line termination.

5.1.2 WRITE GATE

The active state of this signal, or low level, enables write data to be written on the disk.

The HI to LO transition of this signal creates a write splice, and initiates the writing of the data phase-locked oscillator (PLO) synchronization field by the drive, see Figure 5•5, Soft Sector Address Mark, WRITE GATE, PLO Synchronization Format Timing, and Figure 5•6, Hard Sector WRITE GATE, PLO Synchronization Format Timing. When formatting, WRITE GATE should be deactivated for 2 bit times, minimum, between the address area and the data area, to identify to the drive the beginning of the data PLO synchronization field.

***NOTE**: The controller must send zeros during the writing of a PLO synchronization field.*

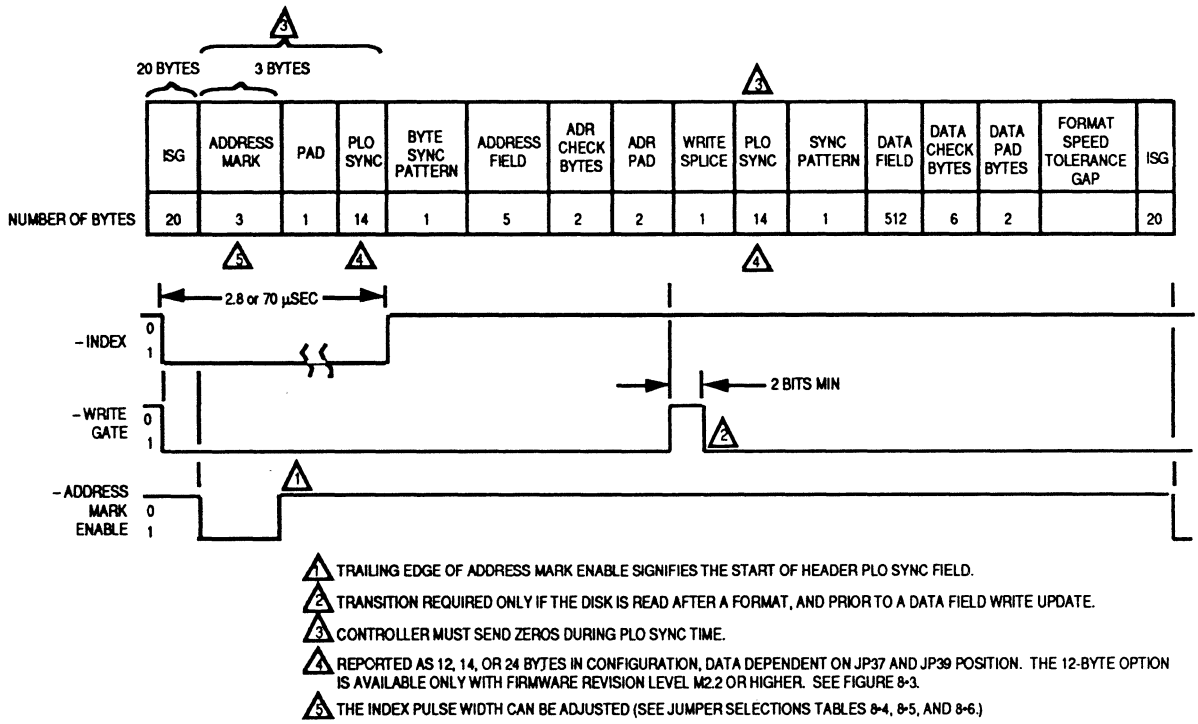


Figure 5-5
Soft Sector Address Mark, WRITE GATE, PLO Synchronization Format Timing

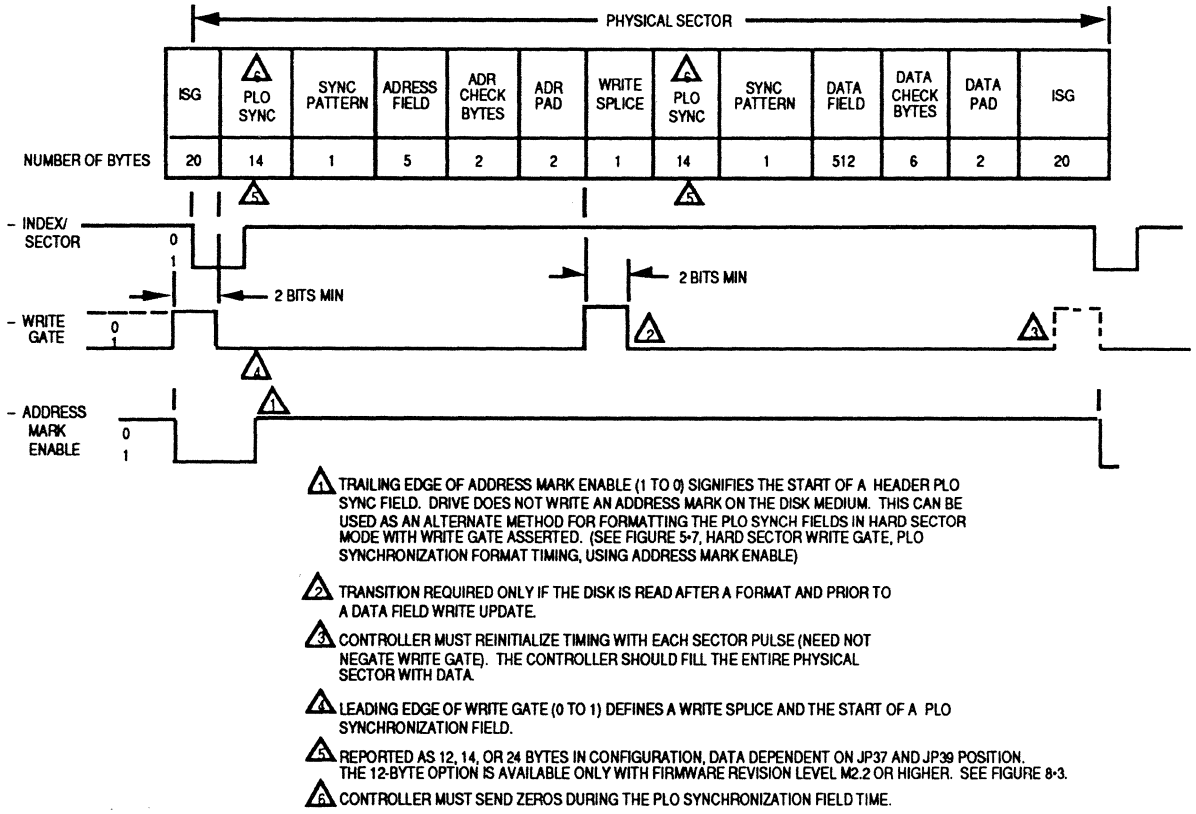
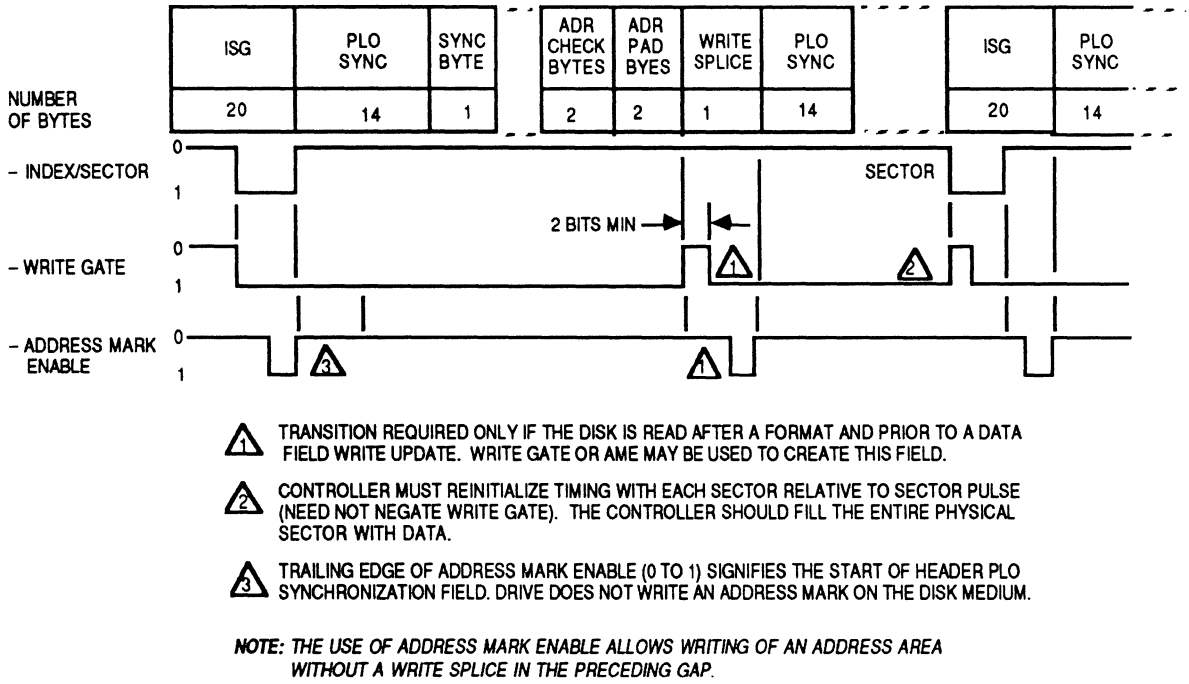


Figure 5-6
Hard Sector WRITE GATE, PLO Synchronization Format Timing

An alternate format timing in hard sector mode, using the ADDRESS MARK ENABLE signal, is shown in Figure 5-7, Hard Sector WRITE GATE, PLO Synchronization Format Timing, Using ADDRESS MARK ENABLE.



1. TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE. WRITE GATE OR AME MAY BE USED TO CREATE THIS FIELD.

2. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR RELATIVE TO SECTOR PULSE (NEED NOT NEGATE WRITE GATE). THE CONTROLLER SHOULD FILL THE ENTIRE PHYSICAL SECTOR WITH DATA.

3. TRAILING EDGE OF ADDRESS MARK ENABLE (0 TO 1) SIGNIFIES THE START OF HEADER PLO SYNCHRONIZATION FIELD. DRIVE DOES NOT WRITE AN ADDRESS MARK ON THE DISK MEDIUM.

NOTE: THE USE OF ADDRESS MARK ENABLE ALLOWS WRITING OF AN ADDRESS AREA WITHOUT A WRITE SPLICE IN THE PRECEDING GAP.

Figure 5•7
Hard Sector WRITE GATE, PLO Synchronization Format Timing, Using ADDRESS MARK ENABLE

This line is protected from terminator power loss by implementation of the circuit shown in Figure 5•8, WRITE GATE Termination.

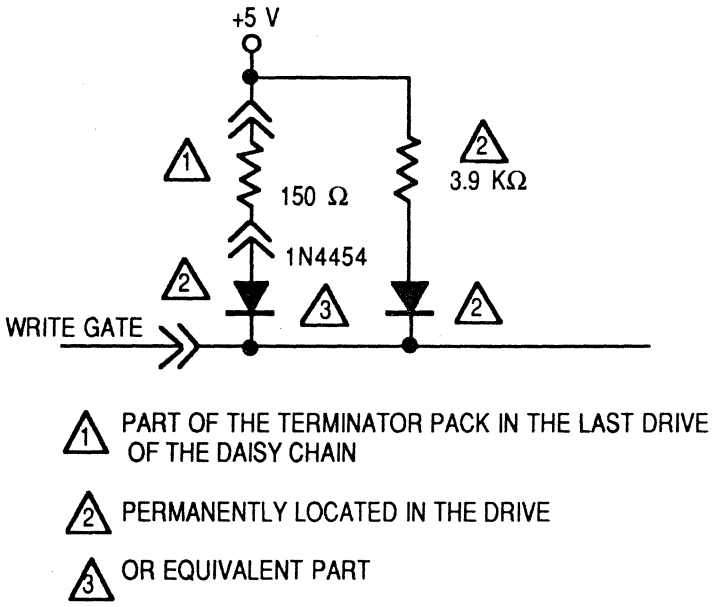


Figure 5•8
WRITE GATE Termination

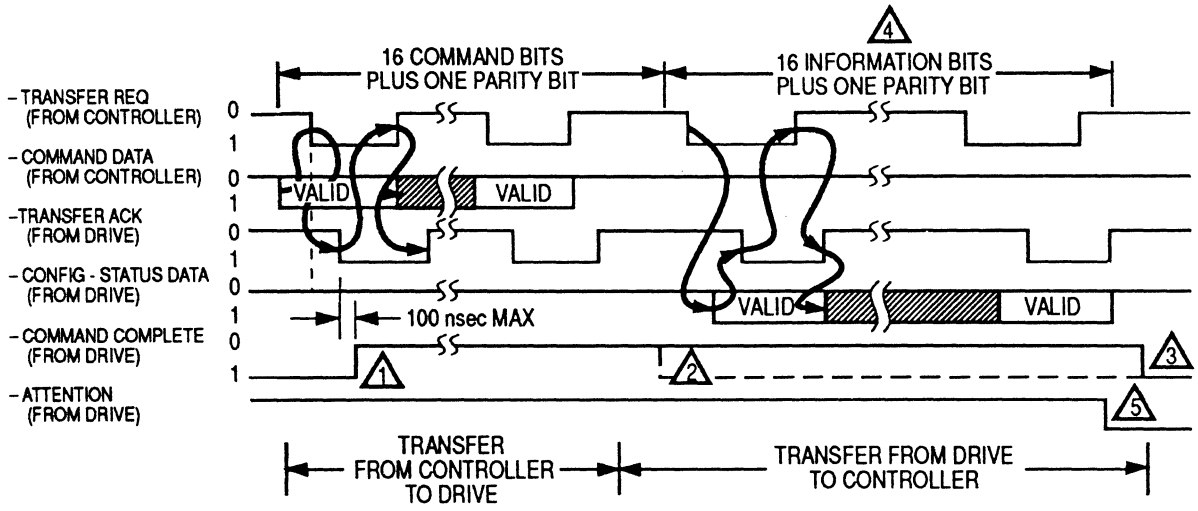
5.1.3 READ GATE

The active state of this signal, or low level, enables data to be read from the disk. This signal should be activated only during a PLO synchronization field. The PLO synchronization field length is indicated by the response to the REQUEST PLO SYNC FIELD LENGTH command. READ GATE must be deactivated when passing over a write splice area.

A 150 ohm resistor pack allows for line termination.

5.1.4 COMMAND DATA

When presenting a command, sixteen information bits of serial data, plus parity, are presented on this line. This data is to be controlled by the handshake protocol with signals TRANSFER REQ and TRANSFER ACK. See Figure 5•9, Typical Serial Operation(s). Upon receipt of this serial data, the drive performs the required function, as specified by the bit configuration. Data is transmitted most significant byte first. See Table 5•4, COMMAND DATA Definition, for the meaning of the various bit combinations, and Figure 5•10, COMMAND DATA Word Structure. See also Figure 5•11, One Bit Transfer Timing—To Drive. Odd parity must be maintained. (The number of bits set to one in a command, including parity, must be odd.)



1. COMMAND COMPLETE IS DEACTIVATED FOR ALL COMMANDS TO THE DRIVE
2. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF EXECUTION OF A COMMAND. APPLICABLE FOR ALL COMMANDS.
3. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF THE REQUESTED CONFIGURATION/STATUS TRANSFER.
4. APPLICABLE FOR ALL REQUEST STATUS AND CONFIGURATION COMMANDS.
5. IF AN ERROR IS ENCOUNTERED DURING THE CURRENT COMMAND, ATTENTION IS ACTIVATED AT LEAST 100 nsec BEFORE COMMAND COMPLETE IS ACTIVATED.

Figure 5-9
Typical Serial Operation(s)

CMD FUNCTION BIT 15	14	13	12	CMD FUNCTION DEFINITION	CMD MODIFIER APPLICABLE (BITS 11-8)	CMD PARAMETER APPLICABLE (BITS 11-0)	STATUS CONFIGURATION DATA RETURNED TO CONTROLLER
0	0	0	0	Seek	No	Yes	No
0	0	0	1	Recalibrate	No	No	No
0	0	1	0	Request Status	Yes	No	Yes
0	0	1	1	Request Configuration	Yes	No	Yes
0	1	0	0	Reserved	–	–	–
0	1	0	1	Control	Yes	No	No
0	1	1	0	Reserved	–	–	–
0	1	1	1	Track Offset	Yes	No	No
1	0	0	0	Initiate Diagnostics	No	No	No
1	0	0	1	Set Bytes per Sector	No	Yes	No
1	0	1	0	Set High Order Value	Yes	Yes	No
1	0	1	1	Reserved	–	–	–
1	1	0	0	Reserved	–	–	–
1	1	0	1	Reserved	–	–	–
1	1	1	0	Set Configuration	Yes	No	No
1	1	1	1	Reserved	–	–	–

NOTES: *1. All unused or not applicable lower order bits must be zero.*
2. Any reserved or command functions received are treated as invalid commands.

Table 5•4
COMMAND DATA Definition

No communications may be attempted unless the COMMAND COMPLETE line is true.

Reading and writing are inhibited during the execution of commands.

NOTE: *The COMMAND DATA line must be at a logic zero when not in use.*

A 150 ohm resistor pack allows for line termination.

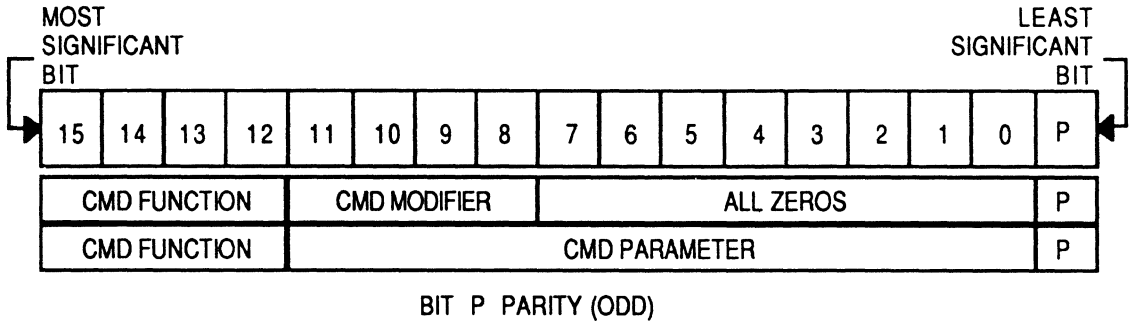


Figure 5•10
COMMAND DATA Word Structure

SEEK (0000): This command causes the drive to seek to the cylinder indicated in bits eleven through zero. A SEEK command restores track offsets to zero.

RECALIBRATE (0001): This command causes the actuator to return to cylinder 0000. A RECALIBRATE command restores track offsets to zero.

REQUEST STATUS (0010): This command causes the drive to send 16 bits of standard status information to the controller, as determined by the command modifier bits. See Table 5•9, Standard Status Response Bits

When the command modifier bits (eleven through eight) of the REQUEST STATUS command are 0000, the drive responds with 16 bits of standard status. See Table 5•5, REQUEST STATUS MODIFIER BITS. Bits fifteen through twelve of this status are defined as state bits, which do not cause ATTENTION to be asserted. Bits eleven through zero of this status are fault, or change of status, bits, which cause ATTENTION to be asserted each time one is set.

REQUEST STATUS MODIFIER BITS: When the command modifier bits (eleven through eight) of the REQUEST STATUS command are 0001 through 0111, the drive responds with the vendor unique status. See Table 5•5, REQUEST STATUS MODIFIER BITS. The number of vendor unique status words is specified by the configuration data.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Request Standard Status
0	X	X	X	Request Vendor Unique Status
1	X	X	X	Reserved

Table 5•5
REQUEST STATUS MODIFIER BITS

REQUEST CONFIGURATION (0011): This command causes the drive to send 16 bits of configuration data to the controller. The specific configuration requested is specified by bits eleven through eight of the command, as shown in Table 5•6, REQUEST CONFIGURATION Modifier Bits. Furthermore, the drive responds to the subscripted command, REQUEST FOR CONFIGURATION, as shown in Table 5•7, Configuration Subscripted.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	General Configuration of Drive and Format
0	0	0	1	Number of Cylinders
0	0	1	0	Reserved
0	0	1	1	Number of Heads
0	1	0	0	Minimum Unformatted Bytes per Track
0	1	0	1	Number of Unformatted Bytes per Sector (Hard Sector)
0	1	1	0	Number of Sectors per Track (Hard Sector)
0	1	1	1	Minimum Bytes in ISG Field
1	0	0	0	Minimum Bytes in PLO Synchronization Field
1	0	0	1	Number of Vendor Unique Status Words Available
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Seek Overhead Skew; Bits 15-8 = Cylinder Switch Skew Bits 7-0 = Head Switch Skew
1	1	1	1	Vendor ID

Table 5•6
REQUEST CONFIGURATION Modifier Bits

CMD FUNCTION	CMD MODIFIER	SUBSCRIPT	CONFIGURATION RESPONSE
Bits 15 - 12	Bits 11- 8	Bits 7- 0	
0 0 1 1	0 0 0 0	1	If Map-in is present, 8000h. If Map-in is not present, 000h.
0 0 1 1	0 0 0 0	8	Transfer Rate Rounded Off in KHz

NOTE: *All other configurations subscript commands are not supported*

Table 5•7
Configuration Subscripted

CONTROL (0101): This command causes the control operations specified by bits eleven through eight to be performed as described in Table 5•8, CONTROL Modifier Bits.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Reset Interface Attention and Standard Status
0	0	0	1	Reserved
0	0	1	0	Stop Motor (when jumper JP6 is open)
0	0	1	1	Start Motor (when jumper JP6 is open)
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	X	X	X	Reserved

Table 5•8
CONTROL Modifier Bits

TRACK OFFSET (0111): This command causes the drive to perform a track offset in the direction and amount specified by bits eleven through eight, as outlined in Table 5•9, TRACK OFFSET Modifier Bits. Each offset value is 36 microinches. SEEK and RECALIBRATE commands restore track offsets to zero.

NOTE: *Whenever there is any track offset, writing is not allowed.*

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	Restore Offset to Zero
0	0	0	1	Restore Offset to Zero
0	0	1	0	Positive Offset One
0	0	1	1	Negative Offset One
0	1	0	0	Positive Offset Two
0	1	0	1	Negative Offset Two
0	1	1	0	Positive Offset Three
0	1	1	1	Negative Offset Three
1	X	X	X	Reserved

Table 5•9
TRACK OFFSET Modifier Bits

INITIATE DIAGNOSTICS (1000): This command causes the drive to perform 10,000 random seeks as a diagnostic aid. Successful completion of the diagnostics is indicated by COMMAND COMPLETE with no ATTENTION.

SET UNFORMATTED BYTES PER SECTOR (1001): This command causes the drive to set the number of unformatted bytes per sector indicated in bits eleven through zero. This command is valid only if the drive is configured to be in the drive hard sectored mode, JP31 removed, and jumper JP30 is installed. (Jumper 16 through 29 settings are ignored.) For less than 4,095 bytes per sector, command A40Xh is used.

SET HIGH ORDER VALUE (1010): A40Xh, where X defines the upper four bits of the number of unformatted bytes per hard sector.

SET CONFIGURATION (1110): E101h sets the drive to soft sector mode. E102h sets the drive to hard sector mode. The number of bytes per sector defaults to 258.

5.1.5 TRANSFER REQ

This line functions as a handshake signal, in conjunction with TRANSFER ACK, during command and configuration/status transfers. See Figure 5•11, One Bit Transfer Timing—To Drive, and Figure 5•12, One Bit Transfer Timing—From Drive, for timing. The transfer speed (one complete handshake) takes typically 11.76 microseconds per bit. Longer times may be experienced, depending on the overhead experienced at the controller.

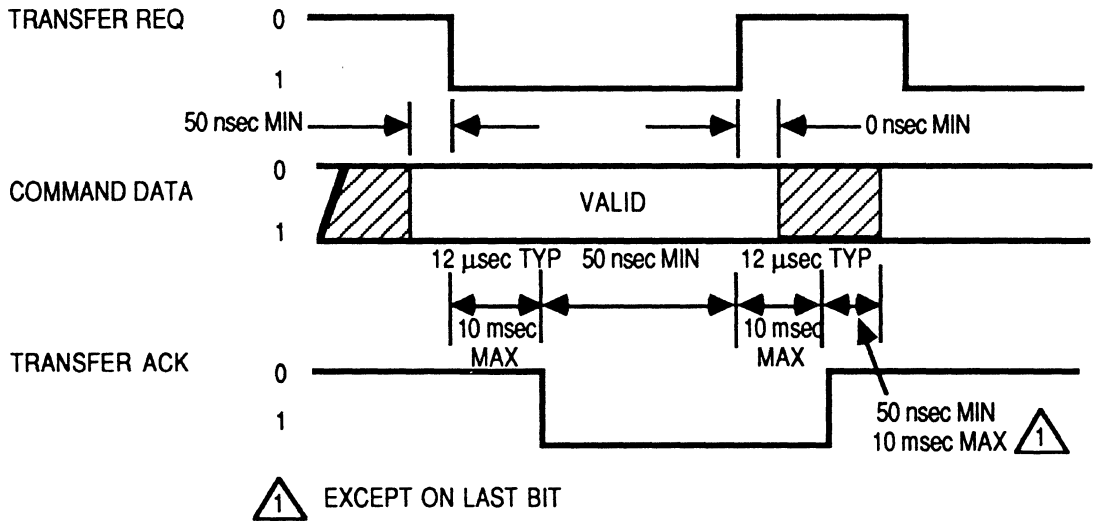


Figure 5•11
One Bit Transfer Timing—To Drive

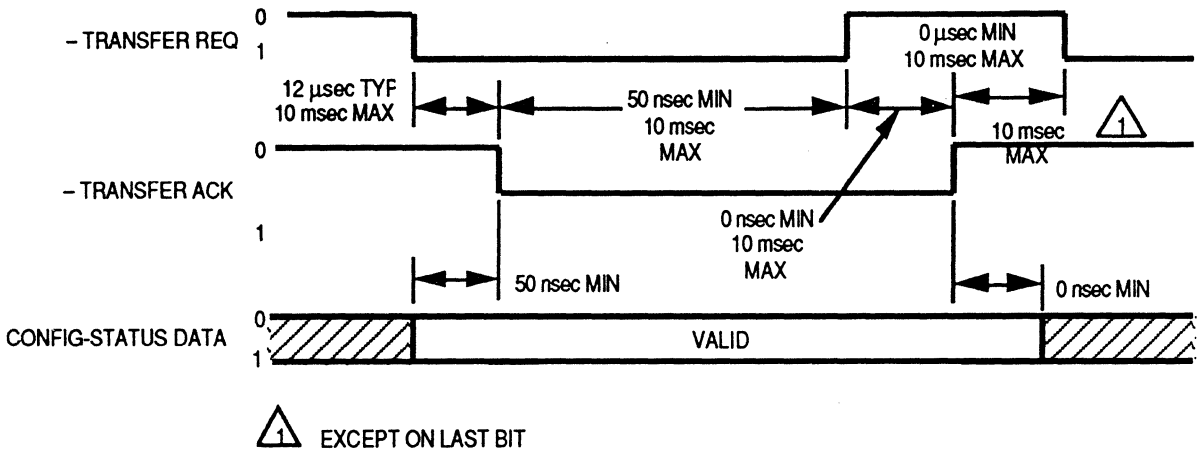


Figure 5•12
One Bit Transfer Timing—From Drive

5.1.6 ADDRESS MARK ENABLE

5.1.6.1 SOFT SECTOR MODE

This signal, when active with WRITE GATE, causes an address mark to be written. ADDRESS MARK ENABLE is active for 24 bit times. See Figure 5•13, Write Address Mark Timing, for timing.

ADDRESS MARK ENABLE, when active without WRITE GATE or READ GATE, causes a search for address marks.

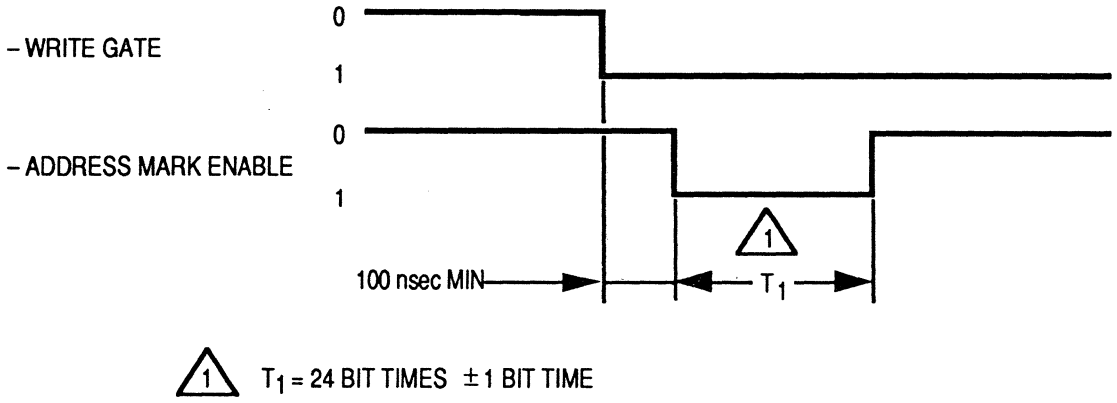


Figure 5•13
Write Address Mark Timing

5.1.6.2 HARD AND SOFT SECTOR MODES

If WRITE GATE is true, the LO to HI transition, or deassertion of ADDRESS MARK ENABLE, causes the drive to begin writing the ID PLO synchronization field. The drive does not write an address mark in this mode (see Figure 5•5, Soft Sector Address Mark, WRITE GATE, PLO Synchronization Format Timing, and Figure 5•7, Hard Sector WRITE GATE, PLO Synchronization Format Timing, Using ADDRESS MARK ENABLE). The controller must send zeros when writing the PLO synchronization field.

A 150 ohm transistor pack allows for line termination.

5.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector output stage, capable of sinking a maximum of 48 milliamps at low level, or true state, with a maximum voltage of 0.4 volts, measured at the driver. When the line driver is in the high level, or false state, the driver transistor is off and collector leakage current is a maximum of 250 microamps.

All J1 output lines are enabled by their respective DRIVE SELECT decodes.

Figure 5•4, Control Signals, Driver/Receiver Combination, shows the recommended circuit.

5.2.1 DRIVE SELECTED

DRIVE SELECTED is a status line, provided at the J2/P2 connector, to inform the host system of the selection status of the drive. The DRIVE SELECTED line is driven by a TTL open collector driver, as shown in Figure 5•4, Control Signals, Driver/Receiver Combination. This signal becomes active only when the drive is selected, as defined in section 4.2, Drive Selection. The DRIVE SELECT lines at J1/P1 are activated by the host system.

5.2.2 READY

This signal indicates that the spindle is up to speed. This interface signal, when true, together with COMMAND COMPLETE, indicates that the drive is ready to read, write, or seek. When the line is false, all writing and seeking is inhibited.

5.2.3 CONFIG-STATUS DATA

The drive presents serial data on this line upon request from the controller. See Figure 5•9, Typical Serial Operation(s), for typical operation. This CONFIG-STATUS serial data is presented to the interface, and transferred using the handshake protocol, with signals TRANSFER REQ and TRANSFER ACK. See Figure 5•11, One Bit Transfer Timing—To Drive. Once initiated, 16 bits, plus parity, are transmitted most significant bit first. Odd parity is maintained. See Figure 5•14, CONFIG-STATUS DATA Word Structure.

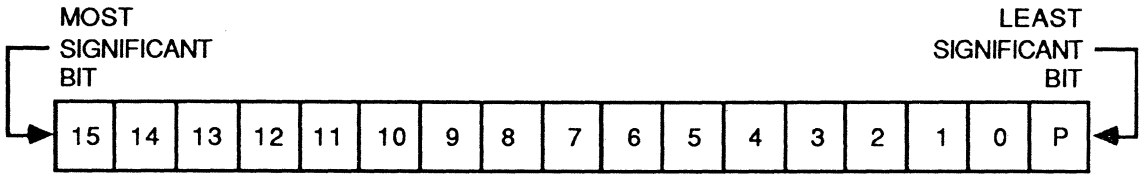


Figure 5•14
CONFIG-STATUS DATA Word Structure

5.2.3.1 STATUS RESPONSE FLAGS

In response to the REQUEST STATUS command 16 bits of status information are returned to the controller. See section 5.1.4, COMMAND DATA. Odd parity is maintained.

If the command modifier bits (eleven through eight) are 0000, the standard status information is returned. See Table 5•10, Standard Status Response Bits.

BIT POSITION	BIT VALUE	FUNCTION
15	0	Reserved
14	0	Reserved
13	0	Reserved
12	C	Write Protected, Fixed Medium
11	0	Spindle Synchronized
10	0	Reserved
9	C	Spindle Motor Stopped
8	C	Power On Reset Conditions Exist
7	C	Command Data Parity Fault
6	C	Interface Fault
5	C	Invalid or Unimplemented Command Fault
4	C	Seek Fault
3	C	Write Gate with Track Offset Fault
2	C	Vendor Unique Status Available
1	C	Write Fault
0	0	Reserved

C = Condition Dependent

Table 5•10
Standard Status Response Bits

Bits fifteen through twelve of the status are defined as state bits, which do not cause ATTENTION to be asserted. Bits eleven through zero are fault, or change of status, bits which cause ATTENTION to be asserted.

Conditions that can cause a write fault are:

- Having no write current with WRITE GATE active and the drive selected.
- Writing before COMMAND COMPLETE.
- Having multiple heads selected, no head selected, or improperly selecting a head with WRITE GATE active.
- Writing while the head is off track.
- Having DC voltages grossly out of tolerance.
- Having WRITE GATE active to a write protected drive.
- Sending nonzero data during a PLO synchronization field write.
- Simultaneously activating READ GATE and WRITE GATE.

5.2.3.2 VENDOR UNIQUE STATUS RESPONSE BITS

If the command modifier bits (eleven through eight) are used, the vendor unique status information shown in Table 5•11, Vendor Unique Status Response Bits, is returned.

BIT POSITION	BIT VALUE	FUNCTION
15	C	Motor Status (see Table 5•11, Motor Status)
14	C	
13	C	
12	C	
11	C	Motor Synchronization
10	C	Unable to Read Configuration Data
9	C	SEEK Calibration Failure
8	C	Head Offset out of Tolerance
7	C	Multiple Preamplifiers Selected
6	C	WRITE GATE without COMMAND COMPLETE
5	C	WRITE GATE while Offtrack
4	C	Write to Protected Drive
3	C	Preamplifier Write Unsafe
2	C	READ GATE Before AMF
1	C	Nonzero Data During PLO Write
0	C	Simultaneous READ and WRITE GATE

C = Condition Dependent

Word 1

BIT POSITION	BIT VALUE	FUNCTION
15	1	XT-8000E
14	0	Reserved
13	C	SEEK Calibration Error Code (See Table 5•12, SEEK Calibration Error Codes)
12	C	SEEK Calibration Error Code
11	C	Number of Heads
10	C	
9	C	
8	C	
7	C	Servo Writer Version
6	C	
5	C	
4	C	
3	C	
2	C	
1	C	
0	C	

C = Condition Dependent

Word 2

Table 5•11
Vendor Unique Status Response Bits

The motor status portion of word one of the vendor unique response is translated as in Table 5•12, Motor Status.

BIT POSITION				FUNCTION
15	14	13	12	
BIT VALUES				
0	0	0	0	Normal Run Mode
0	0	0	1	Bad Spindle Position Sensor
0	0	1	0	Reserved
0	0	1	1	Excessive Time to 1,000 rpm
0	1	0	0	Excessive Time to 3,000 rpm
0	1	0	1	Cannot Lock to Speed
0	1	1	0	Abnormal Accel/Decel Condition at Start
0	1	1	1	Motor Running at Wrong Speed
1	0	0	0	Normal Run Mode With Locked Spindle Synchronized Feature Active
1	0	0	1	Locked Spindle Feature Active, Spindle Not Synchronized
1	0	1	0	Locked Spindle Synchronization Lost
1	0	1	1	Spindle Stuck
1	1	0	0	Reserved
1	1	0	1	Locked Spindle Sync Up Mode Active
1	1	1	0	Locked Spindle Feature Active, but No MAPIN Pulse Provided for Synchronization
1	1	1	1	Reserved

Table 5•12
Motor Status

The SEEK calibration error portion of word two is only valid with bit nine of word one set. With this bit set, the error code is interpreted as in Table 5•13, SEEK Calibration Error Codes.

BIT POSITION		FUNCTION
13	12	
BIT VALUES		
0	0	SEEK Error During Calibration
0	1	SEEK Calibration Time Excessive
1	0	Torque Profile Error
1	1	Head Calibration Error

Table 5•13
SEEK Calibration Error Codes

5.2.3.3 CONFIGURATION RESPONSE FLAG BITS

In response to the REQUEST CONFIGURATION command 16 bits of configuration information are returned to the controller. See section 5.1.4, COMMAND DATA. Odd parity is maintained.

If the command modifier bits (eleven through eight) are 0000, the general configuration status information shown in Table 5•14, General Configuration Response Bits, is returned.

BIT POSITION	BIT VALUE	FUNCTION
15	0	Magnetic Disk Drive
14	0	Format Speed Tolerance Gap Not Required
13	1	Track Offset Option Available
12	0	Reserved
11	0	Reserved
10	1	Transfer Rate > 10 MHz
9	0	Reserved
8	0	Reserved
7	0	Reserved
6	1	Fixed Drive
5	P	Spindle Motor Control Option Implemented
4	0	Reserved
3	1	RLL encoded (not MFM)
2	P	Soft Sectored (address mark)
1	P	Hard Sectored (sector mark)
0	1	Spindle Synchronization Subscripted Configuration Supported

P = Programmable

Table 5•14
General Configuration Response Bits

If other command modifier bits are used, the specific configuration information shown in Table 5•15, Specific Configuration Response Bits, is returned.

COMMAND MODIFIER BITS				CONFIGURATION RESPONSE	VALUE
11	10	9	8		
0	0	0	1	Number of Cylinders, Fixed	1,632
0	0	1	0	Number of Cylinders, Removable	0
0	0	1	1	Number of Heads, Bits 7-0	8 or 15
0	1	0	0	Minimum Unformatted Bytes per Track	31,410
0	1	0	1	Number of Unformatted Bytes per Sector (Hard Sector)	P
0	1	1	0	Number of Sectors per Track (Hard Sector)	P
0	1	1	1	Minimum Bytes in ISG Field	
				(Not Including Intersector Speed Tolerance)	-
				Bits 15-8: ISG Bytes After Index	20
				Bits 7-0: Bytes per ISG Field	20
1	0	0	0	Minimum Bytes per PLO Synchronization Field	
				Bits 7-0: Bytes per PLO Synchronization Field *	12, 14, or 24
1	0	0	1	Number of Vendor Unique Status Words Available	2
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	Reserved	
1	1	1	1	Vendor Identification	8

P = Programmable

* Dependent on position of JP37 and JP1 for PCB assembly 1023051 and position of JP37 and JP39 for all other PCB assemblies.

Table 5•15
Specific Configuration Response Bits

One subscripted status response command is supported, SPINDLE SYNCHRONIZATION STATUS (0011 0000 0000 0001). The response is 1000 0000 0000 0000 if spindle synchronization is active, or 0000 0000 0000 0000 if it is not active.

5.2.4 TRANSFER ACK

This signal functions as a handshake signal, along with TRANSFER REQ, during COMMAND data and CONFIG-STATUS transfers. See Figure 5•11, One Bit Transfer Timing—To Drive, and Figure 5•12, One Bit Transfer Timing—From Drive.

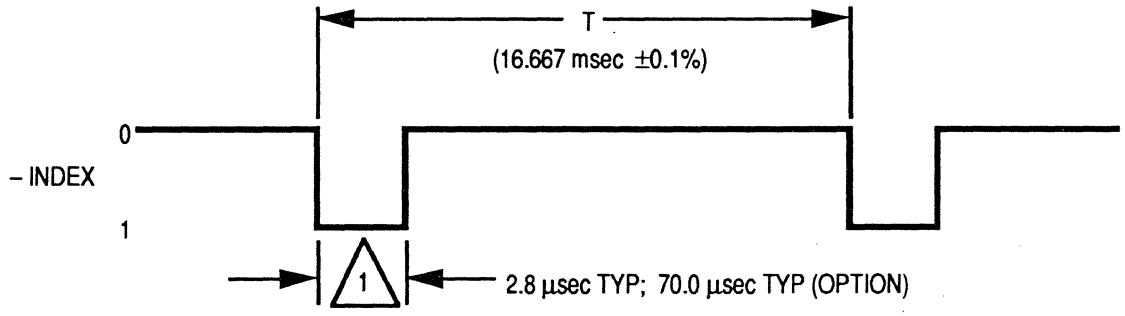
5.2.5 ATTENTION

This output is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status. Writing is inhibited

when ATTENTION is asserted. ATTENTION is deactivated by the RESET INTERFACE ATTENTION command (section 5.1.4, COMMAND DATA).

5.2.6 INDEX

This pulse is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is high and makes the transition to low to indicate INDEX. Only the transition at the leading edge of the pulse is accurately controlled. The period (T) of this signal is reciprocal of the rotational speed. See Figure 5•15, INDEX Timing. This signal is available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated). Jumpers R220 and R221, or JP9 depending on PCB level, allow a pulse width selection of 2.8 microseconds or 70 microseconds. Default factory selection is a pulse width of 2.8 microseconds.



1 THE INDEX PULSE WIDTH IS SET AT THE FACTORY TO 2.8 µsec.

Figure 5•15
INDEX Timing

5.2.7 ADDRESS MARK FOUND (Soft Sector)

This signal indicates the detection of the end of an address mark. See Figure 5•16, Read Address Mark (Soft Sector), for timing.

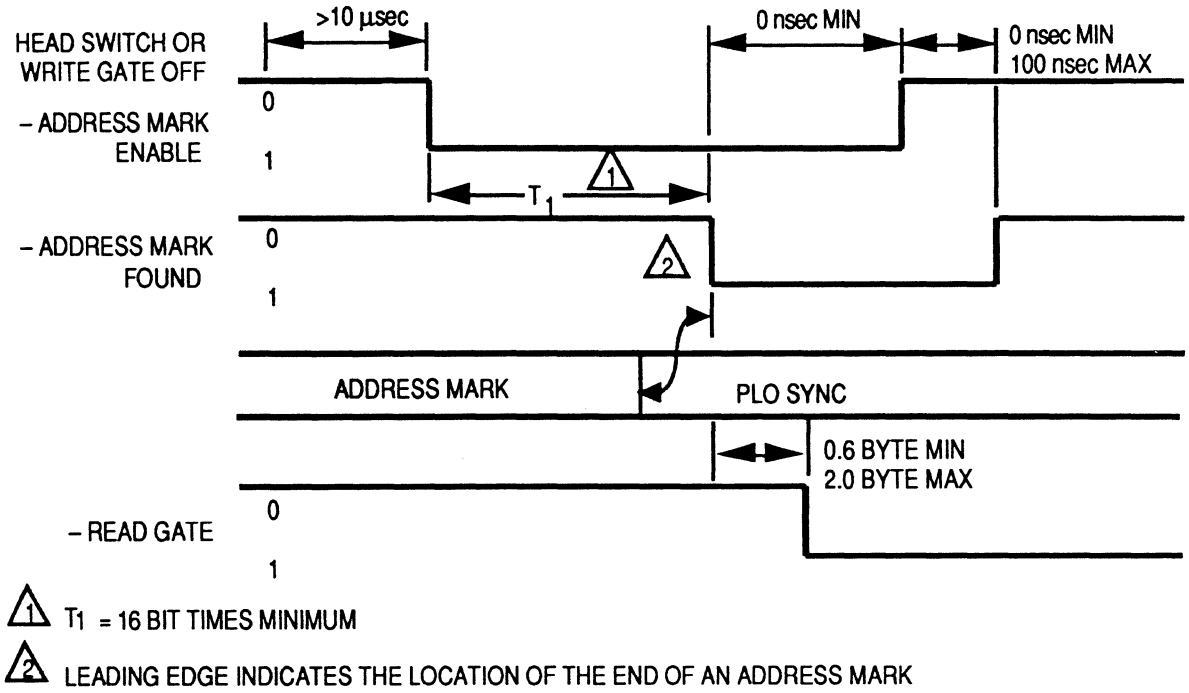


Figure 5•16
Read Address Mark Timing (Soft Sector)

5.2.8 SECTOR MARK (Hard Sector)

This optional interface signal indicates the start of a sector. No short sectors are allowed. The leading edge of the asserted sector pulse is the only edge that is accurately controlled. The INDEX pulse indicates sector zero. See Figure 5•17, Sector Pulse Timing (Hard Sector).

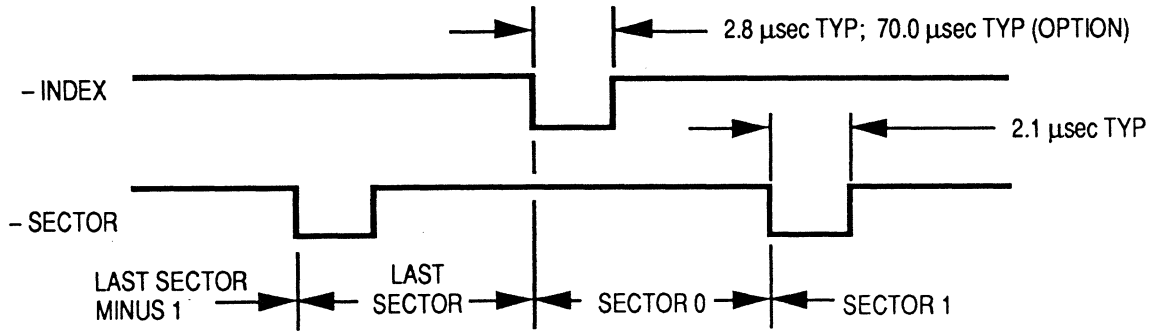


Figure 5•17
Sector Pulse Timing (Hard Sector)

5.2.9 COMMAND COMPLETE

This signal is a status line provided at the J2/P2 connector. This is an ungated output from the drive, which allows the host to monitor the drive's COMMAND COMPLETE status during overlapped commands, without selecting the drive. This signal line becomes false in the following cases:

- When a recalibration sequence is initiated (by drive logic) at power on, if the read/write heads are not over track zero.
- Upon receipt of the first COMMAND DATA bit. COMMAND COMPLETE stays false during the entire command sequence.

This signal is driven by an open collector driver, as shown in Figure 5•4, Control Signals, Driver/Receiver Combination.

5.3 SPINDLE SYNCHRONIZATION CONTROL OPTION

This feature allows up to 48 drives to synchronize the angular position of their spindles such that their INDEX signals line up to within ±20 microseconds of each other. All drives synchronize their spindles to the MAPIN signal of J6 such that their INDEX signal leads MAPIN by 40 ±10 microseconds. In the absence of a MAPIN signal, the drive synchronizes to its internal clock.

The MAPIN is a TTL signal at 60.0 Hz, with a pulse width of 20 microseconds. It is derived from either an external source, or from the MAPOUT signal available on J6 from one drive defined as the master drive.

In the event synchronization is lost after the drive has reported it achieved synchronization, ATTENTION is set.

5.4 ADDITIONAL SIGNALS ON J6

The light-emitting diode (LED) output on J6 is an optional drive-selected signal that is available for use in systems that cannot use the LED on the faceplate.

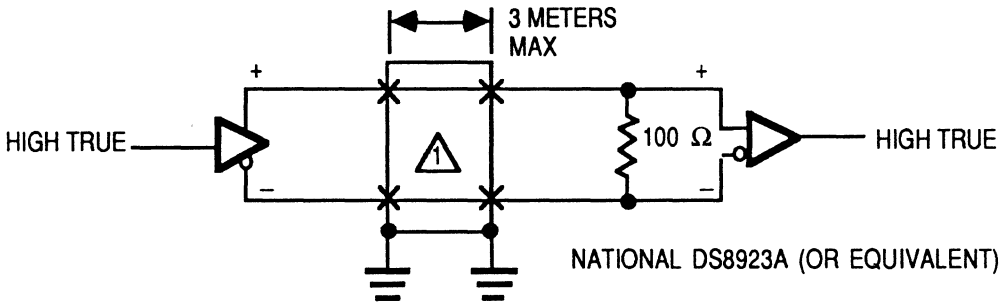
The REMOTE WRITE PROTECT input allows the drive to be write protected via the J6 connector. The active state of this signal, or low level, prohibits data from being written to the drive.

See Figure 5•3, Typical Auxiliary Cable, and Spindle Synchronization Connection, for a typical configuration.

5.5 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential and are not multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Four pairs of balanced signals are used for the transfer of data and clock: NRZ WRITE DATA , NRZ READ DATA, WRITE CLOCK, and READ/REFERENCE CLOCK. Figure 5•18, Data Line Driver/Receiver Combination, illustrates the recommended driver/receiver circuit.



Z = 105Ω FLAT RIBBON OR TWISTED PAIR.
ANY DRIVER AND RECEIVER WHICH COMPLIES
WITH EIA STANDARDS RS-422 MEETS
THESE REQUIREMENTS

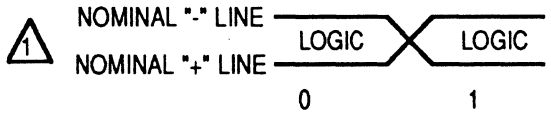
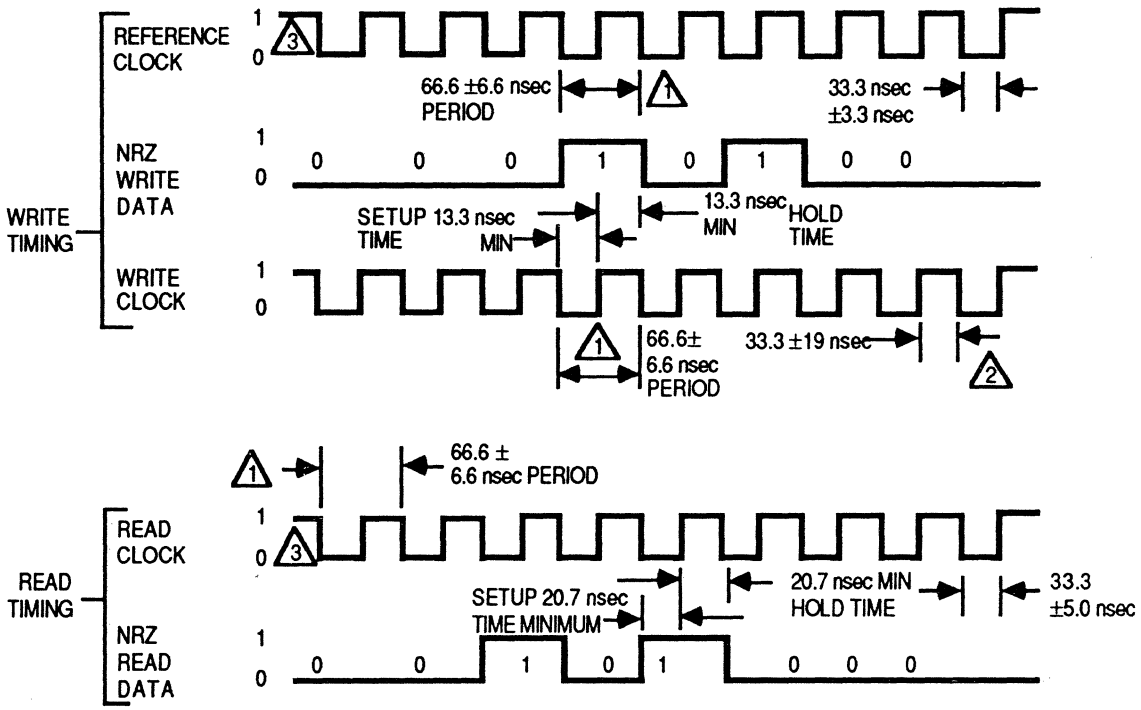


Figure 5•18
Data Line Driver/Receiver Combination

5.5.1 NRZ READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of NRZ READ DATA lines. This data is clocked by the READ CLOCK signal. See Figure 5•19, NRZ READ/WRITE DATA Timings, for timing. These lines are held at a zero level until PLO synchronization has been obtained and data is valid.



1. SIMILAR PERIOD SYMMETRY IS IN ±4 nsec BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
2. SETUP AND HOLD TIME MINIMUMS MUST NOT BE VIOLATED BY ALLOWED DUTY CYCLE TOLERANCE
3. REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLO SYNCHRONIZATION HAS BEEN ESTABLISHED.

NOTE: *ALL TIMES IN nsec MEASURED AT I/O CONNECTOR OF THE DRIVE. SEE FIGURE 5•17, SECTOR PULSE TIMING (HARD SECTOR), FOR DEFINITION OF ZERO AND ONE ON THESE DIFFERENT SIGNAL LINES.*

Figure 5•19
NRZ READ/WRITE DATA Timings

5.5.2 NRZ WRITE DATA

This is a differential pair that defines the data to be written on the track. This data is clocked by the WRITE CLOCK signal. See Figure 5•19, NRZ READ/WRITE DATA Timings, for timing. These lines must be held at a zero level during the writing of PLO synchronization.

5.5.3 READ/REFERENCE CLOCK

The timing diagram, as shown in Figure 5•19, NRZ READ/WRITE DATA Timings, depicts the necessary timing restrictions for proper read/write operation of the drive. The REFERENCE CLOCK signal from the drive determines the data transfer rate. The transition from REFERENCE CLOCK to READ CLOCK is performed without glitches. Two missing clock cycles are permissible.

The REFERENCE CLOCK rate is 15.080 megahertz, typical.

The READ CLOCK rate is 15.080 megahertz, typical.

5.5.4 WRITE CLOCK

WRITE CLOCK is provided by the controller and must be at the bit data transfer rate. This clock frequency is dictated by the READ/REFERENCE CLOCK during the write operation. See Figure 5•19, NRZ READ/WRITE Timings, for timing.

WRITE CLOCK need not be continuously supplied to the drive. WRITE CLOCK is supplied before beginning a write operation and must last for the duration of the write operation.

6.0 PHYSICAL INTERFACE

The electrical interface between the drive and the host controller is via four connectors:

- J1 - Control signals (multiplexed)
- J2 - Read/write signals (radial)
- J3 - DC power input
- J4 - Frame ground

J6 is the spindle synchronization connector and is connected to the drives using this option.

Refer to Figure 6•1, Interface Connector Physical Locations, for connector locations.

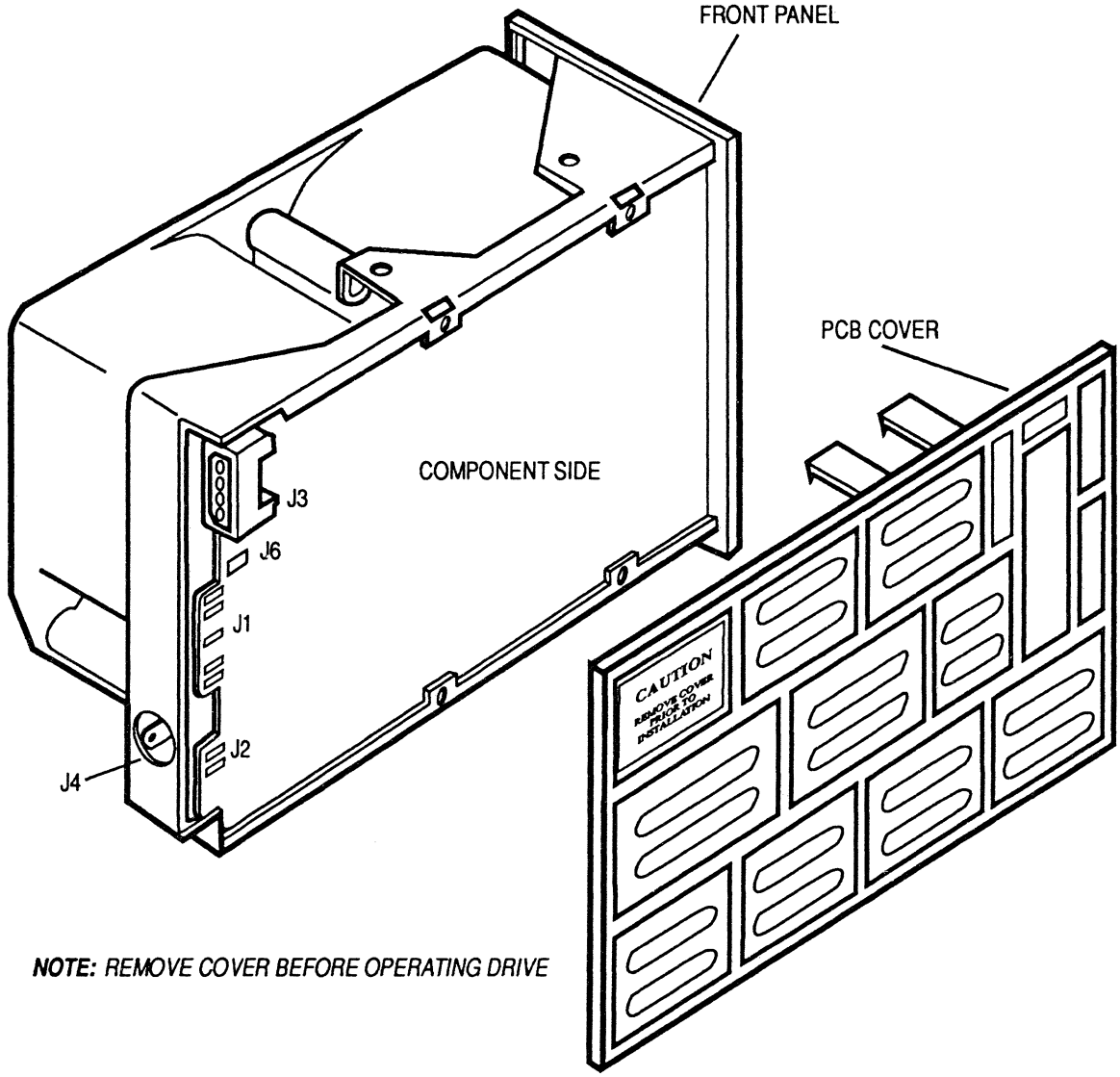


Figure 6•1
Interface Connector Physical Locations

6.1 J1/P1 CONNECTOR

Connection to J1 is via a thirty-four-pin PCB edge connector. The dimensions for this connector are shown in Figure 6•2, J1 Connector Dimensions. The pins are numbered one through thirty-four, with the even pins located on the component side of the PCB. Pin two is located on the end of the PCB connector closest to the DC power connector J3/P3. A key slot is provided between pins four and six. The recommended mating connector for P1 is AMP ribbon connector, part number 88373-3, or equivalent.

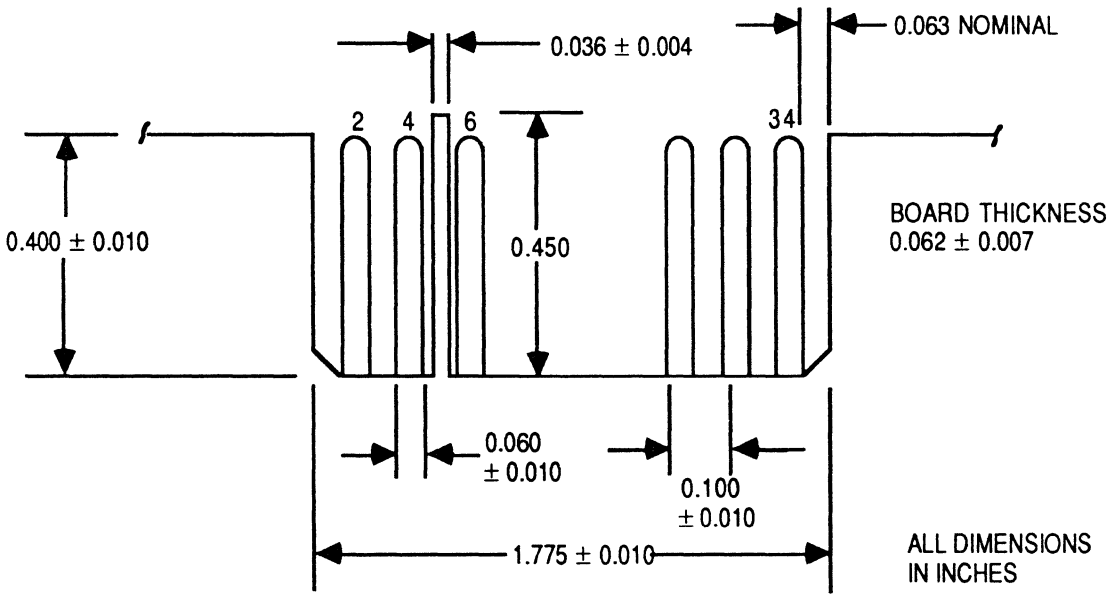


Figure 6-2
J1 Connector Dimension

6.2 J2/P2 CONNECTOR

Connection of J2 is via a twenty-pin PCB edge connector. The dimensions for the connector are shown in Figure 6-3, J2 Connector Dimensions. The pins are numbered one through twenty, with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector, part number 88373-6. A key slot is provided between pins four and six.

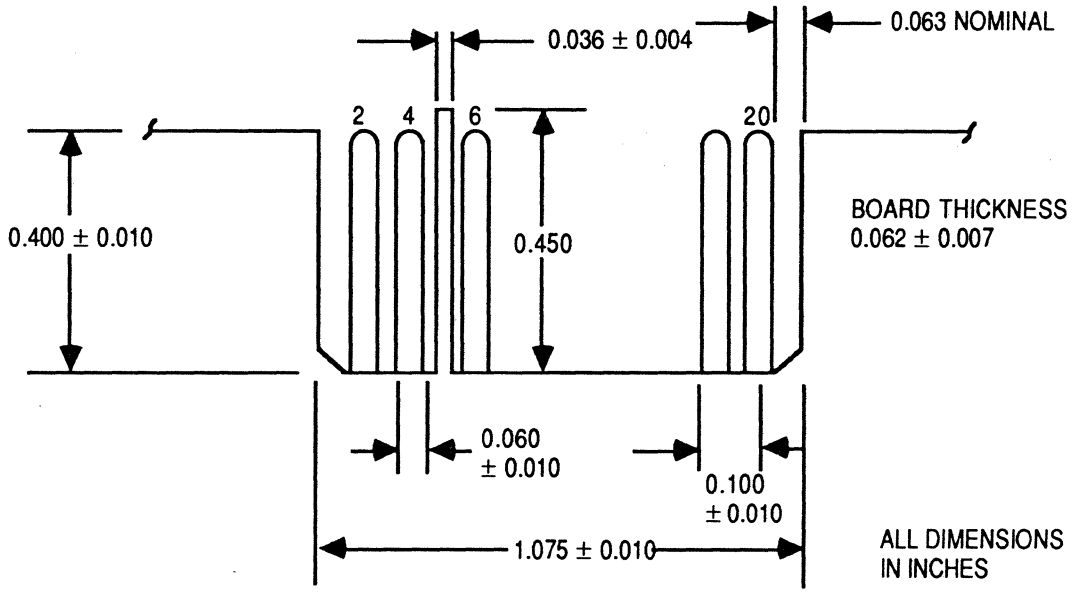


Figure 6•3
J2 Connector Dimensions

6.3 J3/P3 CONNECTOR

The four-pin DC power connector, J3 (shown in Figure 6•4) is similar to AMP's MATE-N-LOCK connector, part number 350543-1. J3 however, is surface mounted to the PCB rather than free-hanging as the AMP part is. The recommended socket housing that is compatible with connector J3 is AMP part number 1-480424-0. The recommended female sockets that are compatible with connector J3 are AMP socket part numbers 350078-4 (strip) or 61173-4 (loose piece). J3 pins are numbered and assigned as shown in Figure 6•4. Figure 6•1, Interface Connector Physical Locations, shows the location of J3 on the disk drive.

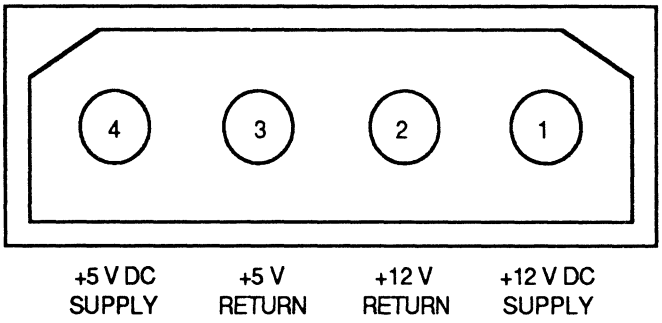
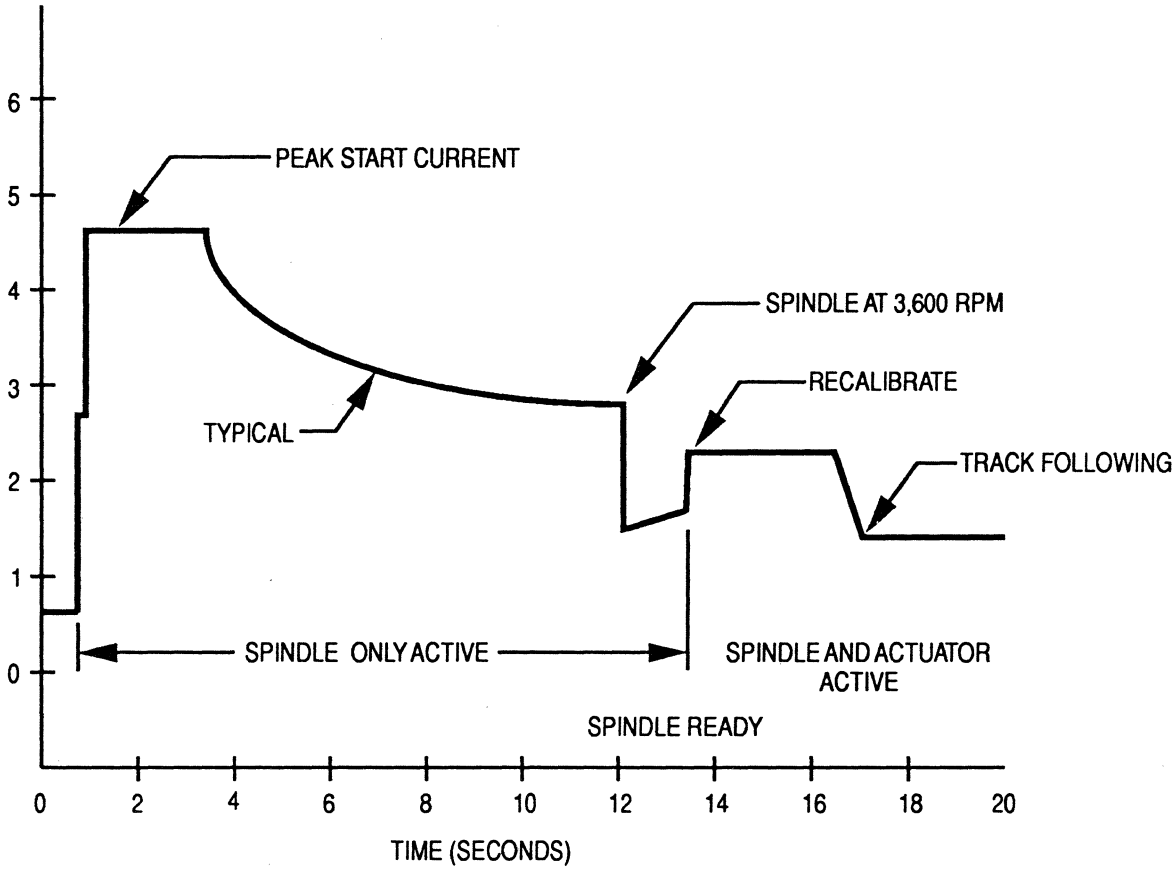


Figure 6•4
J3 Connector (Drive PCB, Solder Side)

The required voltages and current levels on connector J3/P3 are shown in Figure 6•5, Typical Motor Start Current Requirements, and Table 6•1, DC Power Requirements.

NOTE: *A short duration in-rush current exceeding the maximum specification on both the 5 volt and 12 volt supplies may be observed at power on. This is dependent on the power supply used, and is due to charging of bypass and storage capacitors. See Table 6•1.*



NOTE: *WHEN A FULL-LENGTH SEEK IS DONE, ONE ADDITIONAL AMP IS REQUIRED FOR A DURATION OF 15 MILLISECONDS*

Figure 6•5
Typical Motor Start Current Requirements

VOLTAGE (NOMINAL)	+12 V DC	+5 V DC
REGULATION	±5%	±5%
CURRENT (Typical)	1.5 A	1.7 A
CURRENT (Maximum)	4.5 A *	1.9 A
RIPPLE (Maximum, P-P)	120 mV	50 mV

* Potential current surge greater than 4.5A during rise time, to charge capacitors at power on, is possible for power supplies with fast rise times (less than 15 msec). However, the capacitors are eliminated on the XT-8000EH products.

Table 6•1
DC Power Requirements

6.4 J4/P4 Frame Ground Connector

The frame ground connection is a Faston-type connection, AMP part number 61761-2. The recommended mating connector is AMP 62187-1. If wire is used, the hole in J4 accommodates a maximum wire size of 18 AWG. Normally, this connection should not be used.

6.5 J6/P6 Auxiliary Connector

The auxiliary connector is a Berg 68451-121, ten-pin connector. The mating connector is a 3M 3473-6010. See Table 6•2, J6 Auxiliary Signal Cable Pin Assignments, for pin assignments.

SIGNAL NAME	PIN
MAPOUT	1
MAPIN	2
GND	3
MAPIN	4
GND	5
KEY (not connected)	6
- REMOTE WRITE PROTECT	7
	8
- LED	9
+ LED	10

Table 6-2
J6 Auxiliary Signal Cable Pin Assignments

7.0 PHYSICAL SPECIFICATIONS

This section describes the mechanical and mounting recommendations for the drive.

7.1 MOUNTING ORIENTATION

The drive may be mounted in any orientation. In any final mounting configuration, insure that the operation of the three shock mounts, which isolate the base casting from the frame, is not restricted. Certain switching power supplies may emanate electrical noise which degrades the specified read error rate. For best results, orient the drive so that the PCB assembly is not adjacent to these noise sources.

7.2 INSTALLATION REQUIREMENTS

The XT-8000E must operate in a temperature range between 50° F and 122° F (10° C and 50° C). The drive should be installed in applications where temperature extremes outside of this range are avoided.

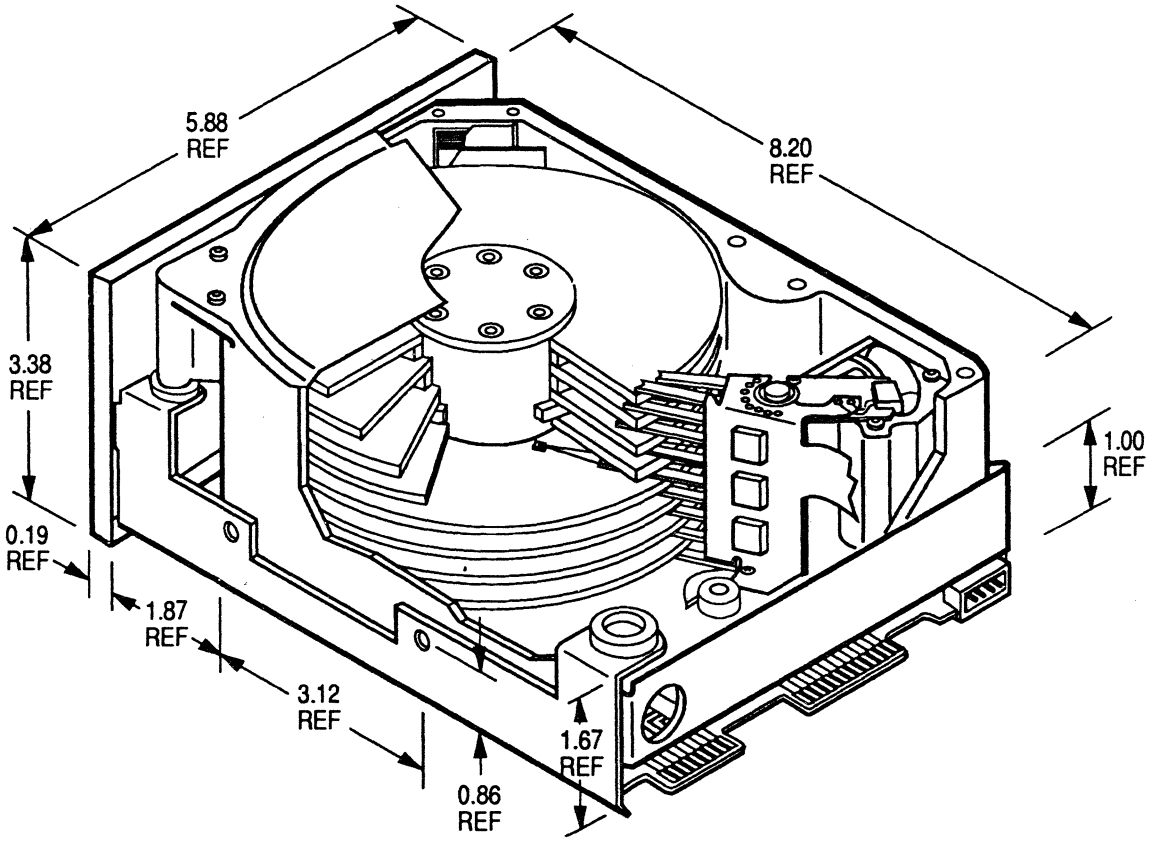
To maintain proper operating temperature, the XT-8000E must be mounted in such a way as to ensure adequate airflow.

CAUTION: *These requirements must be met to ensure proper functioning of the drive. If they are not met, data loss and/or permanent damage to the drive will result.*

7.3 MOUNTING HOLES

Eight mounting holes, four on the bottom and two on each side, are provided for mounting the drive into an enclosure. The size and location of these holes, shown in Figure 7•1, Mechanical Outline and Mounting Hole Locations, are identical to industry standard floppy drives.

CAUTION: *The casting is very close to the frame mounting holes in some locations. Mounting screw lengths must be chosen such that no more than 0.125 inches of the screw is available to enter the frame mounting hole. The torque applied to the mounting screws should be between 9 and 12 inch-pounds.*



REF = REFERENCE. FOR EXACT MEASURMENTS, SEE FIGURE 7•2, MECHANICAL OUTLINE, BOTTOM AND SIDE VIEWS.

Figure 7•1
Mechanical Outline and Mounting Hole Locations

7.4 PHYSICAL DIMENSIONS

Overall height, width, and depth, along with other key dimensions, are shown in Figure 7•1, Mechanical Outline and Mounting Hole Locations, and Figure 7•2, Mechanical Outline, Bottom and Side Views.

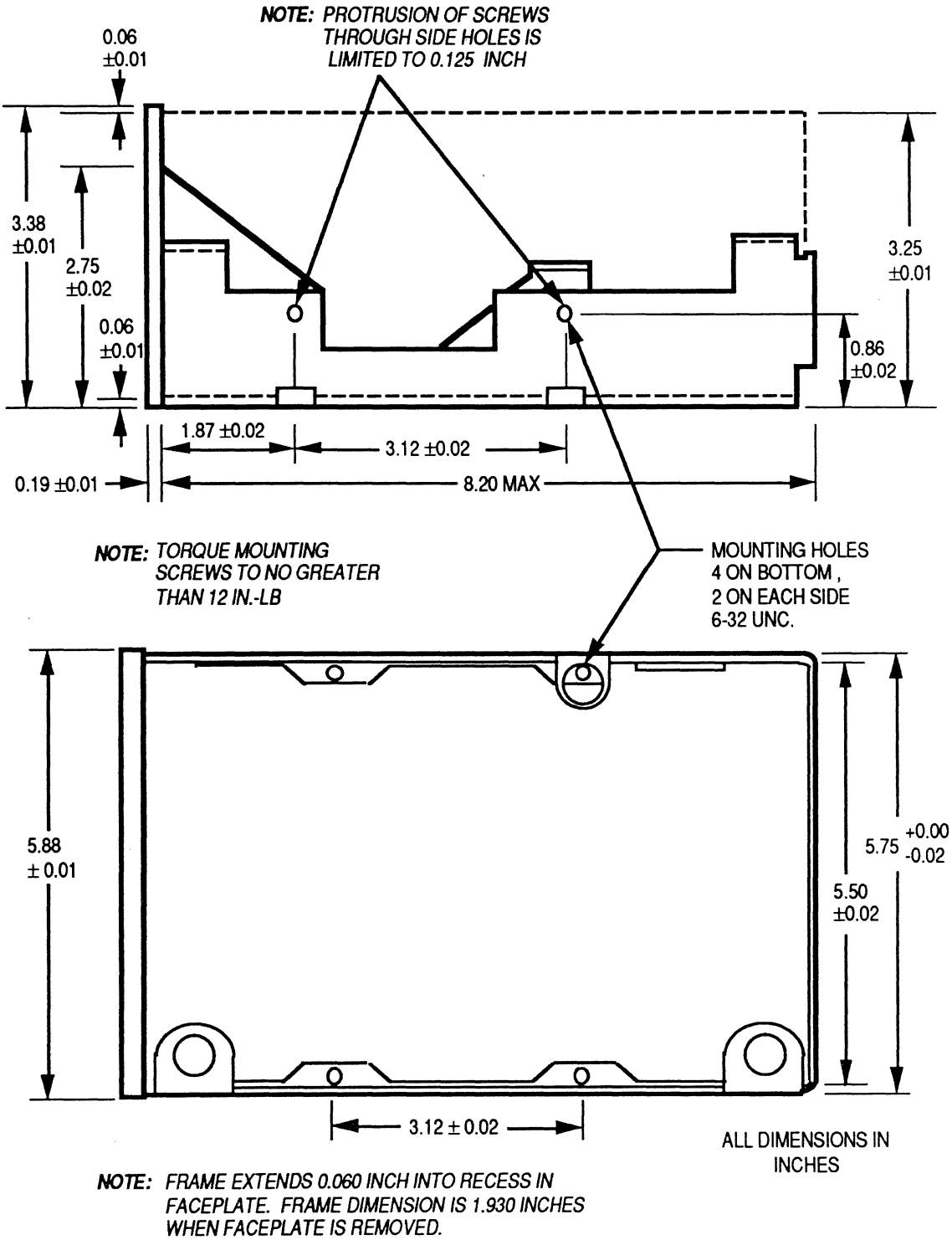


Figure 7-2
Mechanical Outline, Bottom and Side Views

7.5 SHIPPING REQUIREMENTS

At power down, the heads are automatically positioned over the nondata, dedicated landing zone on each disk surface. The automatic shipping lock solenoid is also engaged at this time.

7.6 REMOVABLE FACEPLATE

The faceplate may be removed in installations that require it. Remove the two E-clips and unplug the LED cable from the PCB. See Figure 7•3, Removable Faceplate.

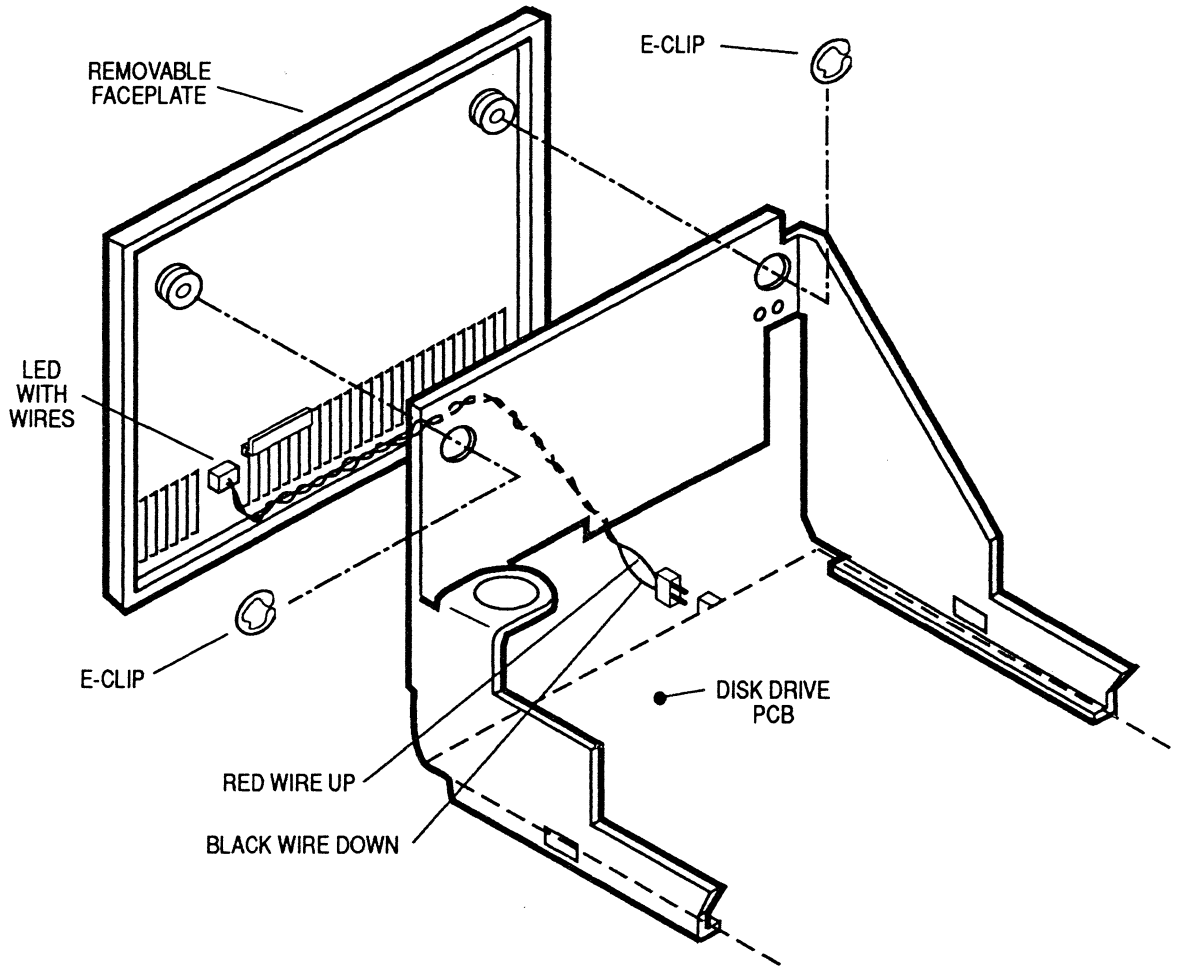


Figure 7•3
Removable Faceplate

8.0 PCB JUMPER OPTIONS

8.1 DRIVE ADDRESS SELECTION JUMPER

In multidrive configurations, it is necessary to configure each drive with a unique address. A maximum of seven drives is permitted per host controller. The address for the drive is determined by installing the jumper plug in the appropriate jumper location. Table 8•1, Drive Select Jumpers, shows the drive selection jumpers. As shipped from the factory, the DS1 jumper is installed. Removing the jumper entirely is equivalent to a "no select." See Figures 8•1 through 8•6, Drive Jumper Options, and Tables 8•6 through 8•11, Jumper Selections.

DRIVE SELECT NUMBER	JUMPER INSTALLED
1	DS1
2	DS2
3	DS3
4	DS4
5	DS5
6	DS6
7	DS7

Table 8•1
Drive Select Jumpers

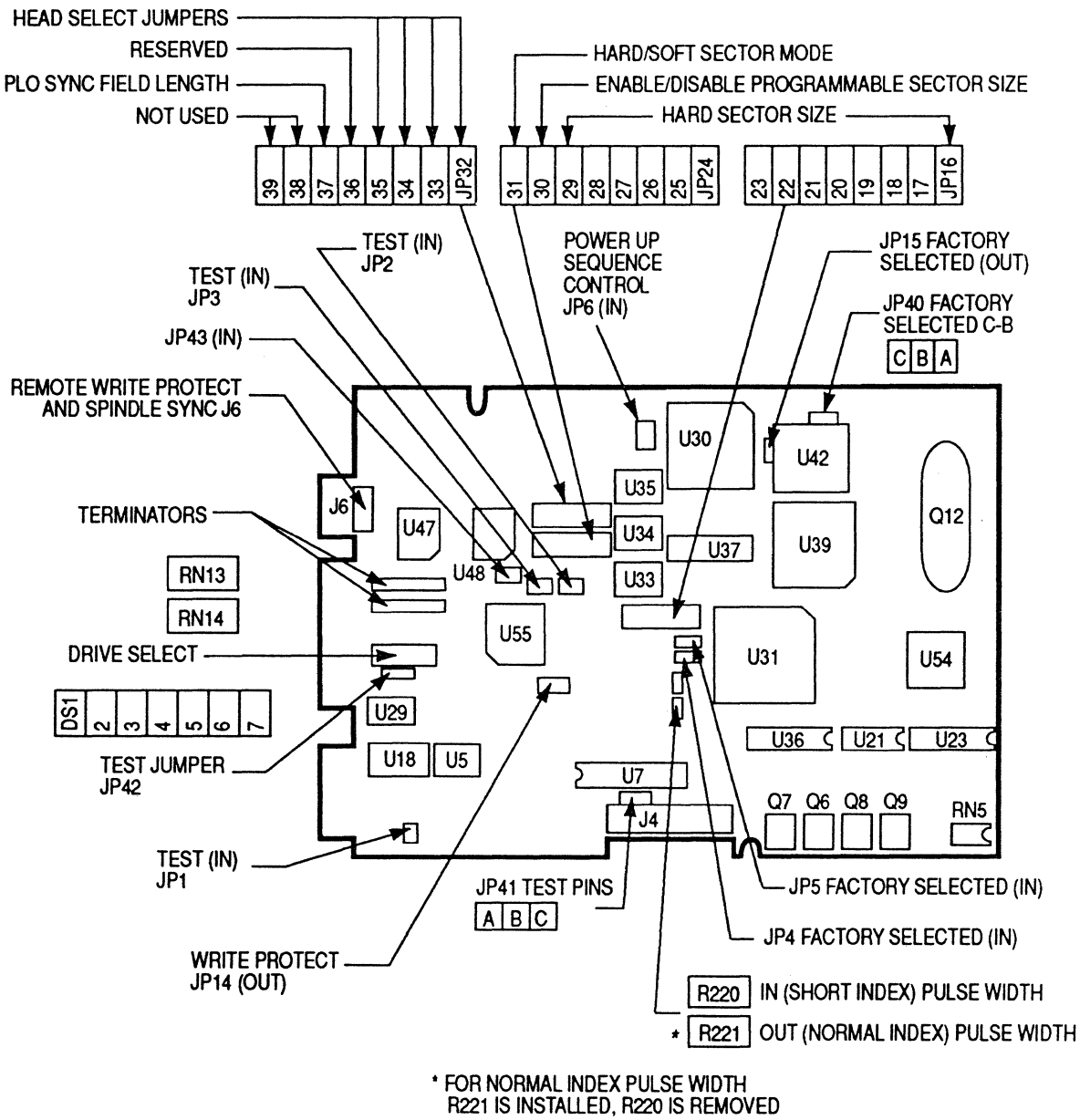


Figure 8-1
Drive Jumper Options (PCB Part Number 1014150)

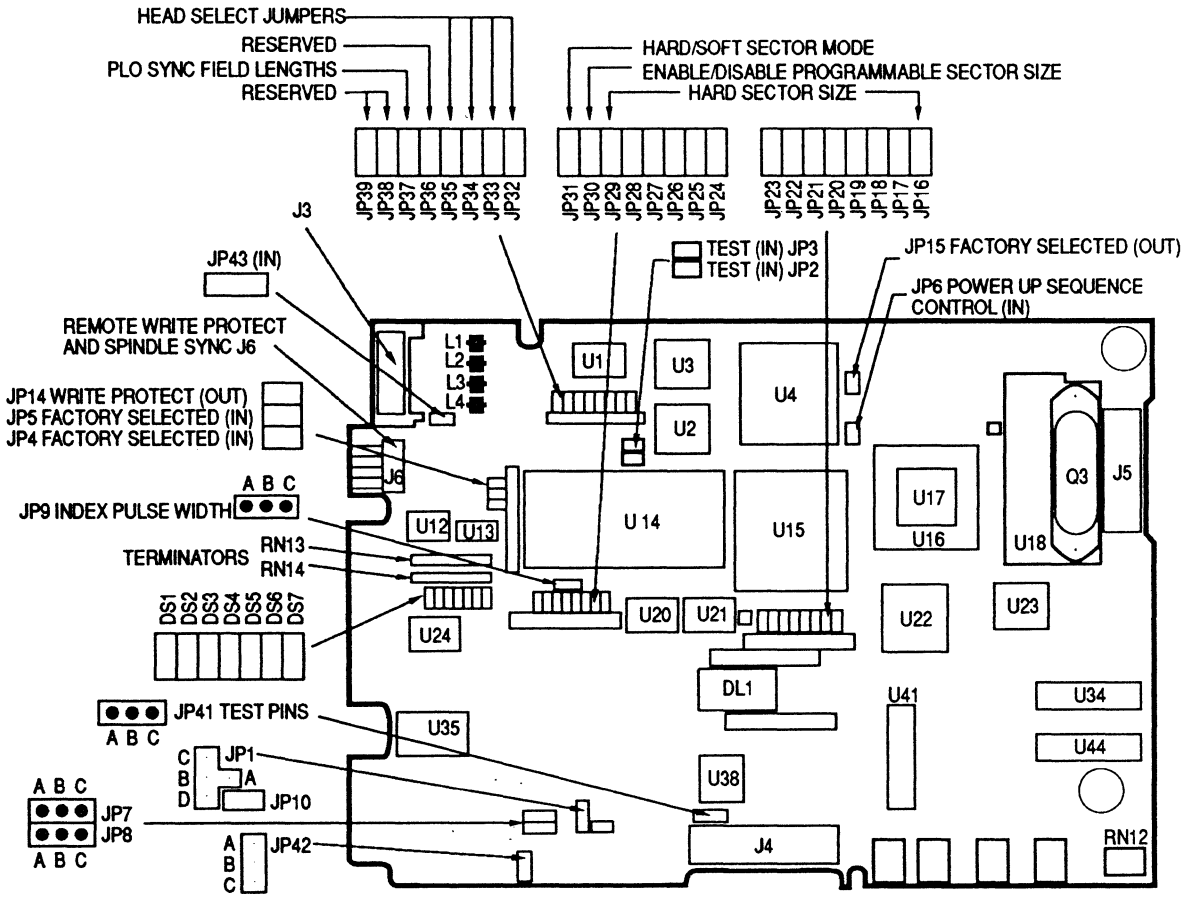
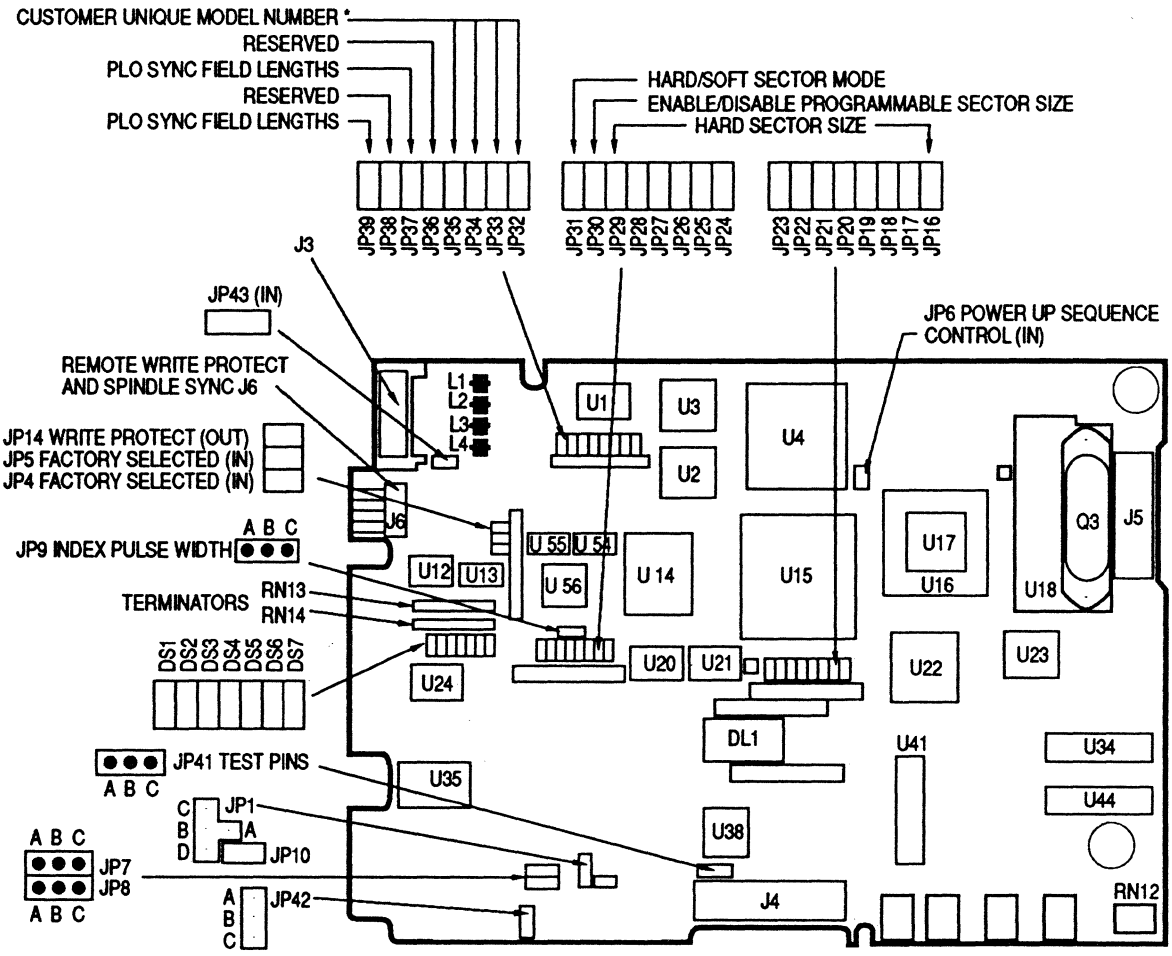
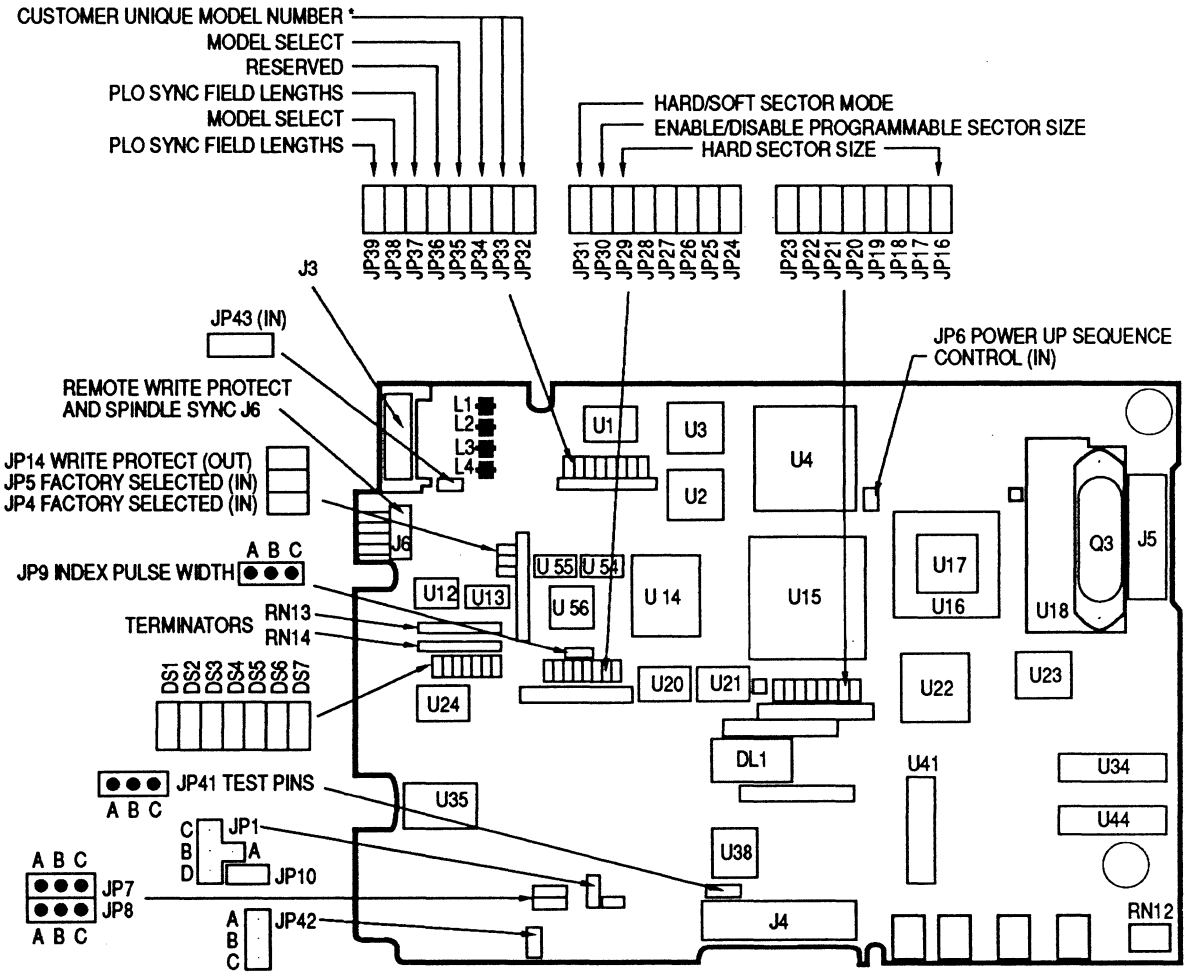


Figure 8-2
Drive Jumper Options (PCB Part Number 1015468)



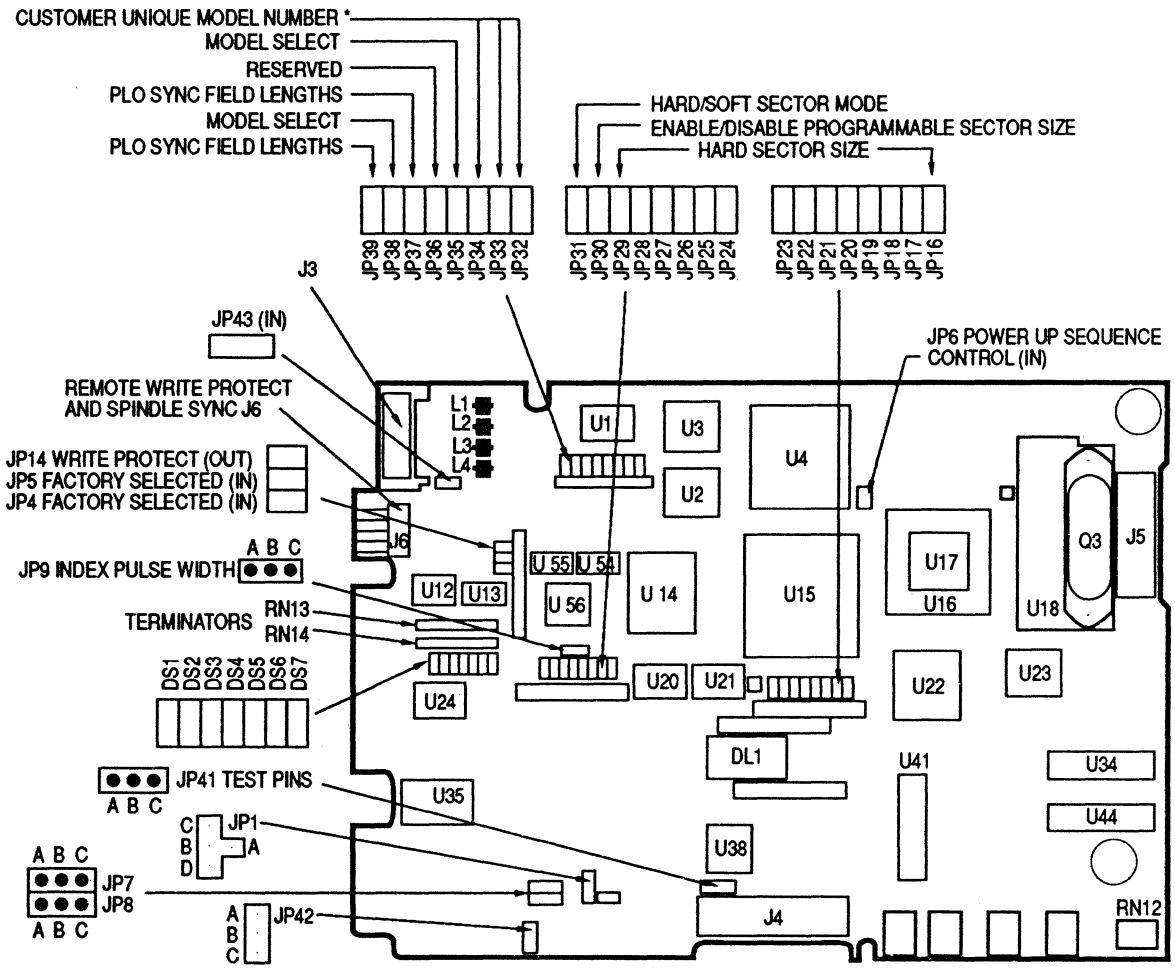
NOTE: CUSTOMER UNIQUE MODEL NUMBER SELECTION IS AVAILABLE ONLY WITH FIRMWARE REVISION LEVEL M2.2 OR HIGHER. SEE U3 AND U2 FOR REVISION LEVEL. IF FIRMWARE REVISION LEVEL IS BELOW M2.2, SEE FIGURE 8-2.

Figure 8-3
Drive Jumper Options (PCB Part Number 1014520)



**NOTE: CUSTOMER UNIQUE MODEL NUMBER SELECTION IS AVAILABLE ONLY WITH FIRMWARE REVISION LEVEL M2.2 OR HIGHER. SEE U3 AND U2 FOR REVISION LEVEL. IF FIRMWARE REVISION LEVEL IS BELOW M2.2, SEE FIGURE 8-2.*

Figure 8-4
Drive Jumper Options (PCB Part Number 1023821)



NOTE: CUSTOMER UNIQUE MODEL NUMBER SELECTION IS AVAILABLE ONLY WITH FIRMWARE REVISION LEVEL M2.2 OR HIGHER. SEE U3 AND U2 FOR REVISION LEVEL. IF FIRMWARE REVISION LEVEL IS BELOW M2.2, SEE FIGURE 8-2.

Figure 8-5
Drive Jumper Options (PCB Part Number 1023856)

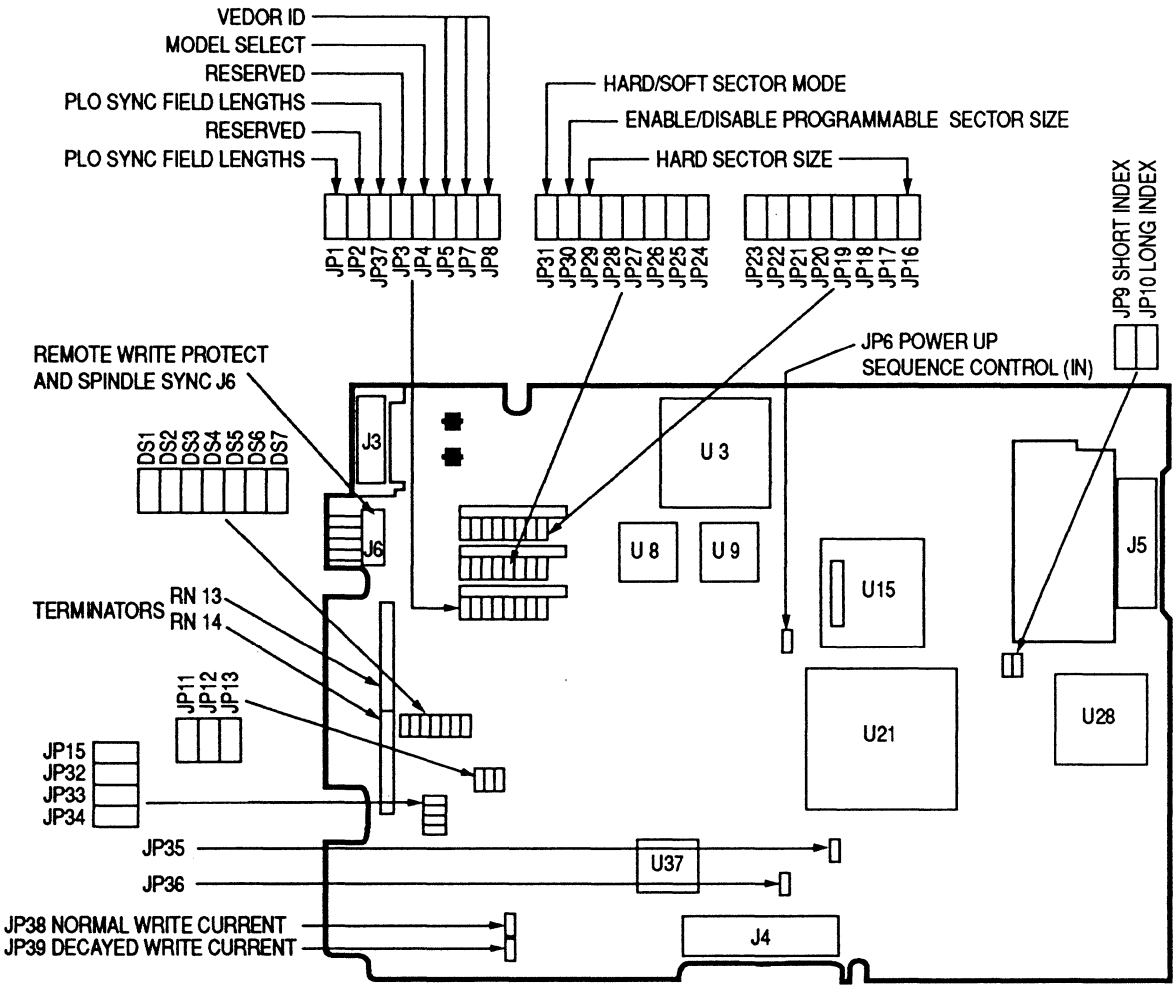


Figure 8-6
Drive Jumper Options (PCB Part Number 1023051)

JUMPER				REQUEST CONFIGURATION, VENDOR ID (3F00h)			
				BEFORE THE FIRST START SPINDLE COMMAND IS EXECUTED (5300h) *	AFTER DRIVE IS READY		
JP35	JP34	JP33	JP32		8380E	8760E	8610E
In	In	In	In	0801h	0802h	0801h	0806h
In	In	In	Out	0821h	0822h	0821h	0826h
In	In	Out	In	0841h	0842h	0841h	0846h
In	In	Out	Out	0861h	0862h	0861h	0866h
In	Out	In	In	0881h	0882h	0881h	0886h
In	Out	In	Out	08A1h	08A2h	08A1h	08A6h
In	Out	Out	In	08C1h	08C2h	08C1h	08C6h
In	Out	Out	Out	08E1h	08E2h	08E1h	08E6h
Out	In	In	In	0802h	0802h	0801h	0806h
Out	In	In	Out	0822h	0822h	0821h	0826h
Out	In	Out	In	0842h	0842h	0841h	0846h
Out	In	Out	Out	0862h	0862h	0861h	0866h
Out	Out	In	In	0882h	0882h	0881h	0886h
Out	Out	In	Out	08A2h	08A2h	08A1h	08A6h
Out	Out	Out	In	08C2h	08C2h	08C1h	08C6h
Out	Out	Out	Out	08E2h	08E2h	08E1h	08E6h

* ***NOTES:*** *1) The information in this table assumes that JP6 is out; drive is in the remote spin mode. If JP6 is in, ignore this column.*
2) This table applies only to drives with firmware revision level M2.2 and higher. See Figure 8•3

Table 8•2
Drive Vendor ID Selection Jumpers

JUMPER				REQUEST CONFIGURATION, VENDOR ID (3F00h)		
				BEFORE THE FIRST START SPINDLE COMMAND IS EXECUTED (5300h) *	AFTER DRIVE IS READY	
JP8	JP7	JP5	JP4		8380EH	8760EH
In	In	In	In	0801h	0802h	0801h
Out	In	In	In	0821h	0822h	0821h
In	Out	In	In	0841h	0842h	0841h
Out	Out	In	In	0861h	0862h	0861h
In	In	Out	In	0881h	0882h	0881h
Out	In	Out	In	08A1h	08A2h	08A1h
In	Out	Out	In	08C1h	08C2h	08C1h
Out	Out	Out	In	08E1h	08E2h	08E1h
In	In	In	Out	0802h	0802h	0801h
Out	In	In	Out	0822h	0822h	0821h
In	Out	In	Out	0842h	0842h	0841h
Out	Out	In	Out	0862h	0862h	0861h
In	In	Out	Out	0882h	0882h	0881h
Out	In	Out	Out	08A2h	08A2h	08A1h
In	Out	Out	Out	08C2h	08C2h	08C1h
Out	Out	Out	Out	08E2h	08E2h	08E1h

* ***NOTES:*** *1) The information in this table assumes that JP6 is out; drive is in the remote spin mode. If JP6 is in, ignore this column.*
2) This table applies only to drives with firmware revision level M2.2 and higher. See Figure 8•3

Table 8•3
Drive Vendor ID Selection Jumpers for PCB 1023051

JP39	JP37	BYTES PER PLO SYNC FIELD
Out	Out	14
Out	In	24
In	Out	14
In	In	*12

*NOTE: *This value applies only to drives with firmware revision level M2.2 or higher, otherwise this value is undefined. See Figure 8-3.*

Table 8-4
JP37 and JP39 Jumper Selections

JP37	JP1	BYTES PER PLO SYNC FIELD
Out	Out	14
In	Out	24
Out	In	14
In	In	*12

*NOTE: *This value applies only to drives with firmware revision level M2.2 or higher, otherwise this value is undefined. See Figure 8-3.*

Table 8-5
JP37 and JP1 Jumper Selections (PCB 1023051)

JUMPER	TYPE *	DESCRIPTION
JP1 (In)	F	Encoded Write Data, TTL
JP2 (In)	F	Need for Phase Margin Testing: ECL Level Clock Output = Pin 18. Input = Pin 19.
JP3 (In)	F	Used for Phase Margin Testing: ECL Level Data Output = Pin 20. Input = Pin 21.
JP4 (In)	F	In = 2, 7 Encoding
JP5 (In)	F	In = 15 Mbit/sec Transfer Rate
JP6 (In)	C	In = Motor Remote Spinup Option Disabled Out = Motor Spinup Option Enabled
DS1-DS7	C	Drive Select
JP14 (Out)	C	In = Write Protect
JP15 (Out)	F	Not Used
JP16-JP29	C	Hard Sector Size
JP30	C	Out = Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In = Enable ESDI Programmable Sector Size (Hard Sector Mode Only)
JP31	C	In = Soft Sector Mode; Out = Hard Sector Mode
JP32-JP35	F	Head Configuration
JP36	F	Reserved
JP37	C	In for 24-Byte PLO Sync Field, Out for 14-Byte PLO Synchronization Field
JP38	F	Reserved
JP39	F	Reserved
JP40	F	Test Jumper
JP41	F	Test Pins (Differential Data Read Signals)
JP42 (In)	F	Test (WRITE GATE to Flex Circuit)
JP43 (In)	F	Test Out Disables Onboard RAM
R220 (In)	F	Short INDEX Pulse Width (2.8 µsec)
R221 (Out)**	F	Normal INDEX Pulse Width (70 µsec)

* C = Customer Configurable
F = Factory Select
** For normal INDEX pulse width, R221 is installed, R220 is removed.

Table 8-6
Jumper Selections (PCB Part Number 1014150)

JUMPER	TYPE *	DESCRIPTION
JP1 (B-C)	F	Encoded Write Data, TTL
JP2 (In)	F	Need for Phase Margin Testing: ECL Level Clock Output = Pin 18. Input = Pin 19.
JP3 (In)	F	Used for Phase Margin Testing: ECL Level Data Output = Pin 20. Input = Pin 21.
JP4 (In)	F	In = 2, 7 Encoding
JP5 (In)	F	In = 15 Mbit/sec Transfer Rate (Hard Wired)
JP6 (In)	C	In = Motor Remote Spinup Option Disabled Out = Motor Spinup Option Enabled
JP7 (B-C)	C	Read Gate Delay Option
JP8 (Out)	C	Read Gate Delay Option
JP9 (A-B)	C	INDEX Width Selection, AB = 2.8 µsec. BC = 70 µsec.
JP10 (Out)	F	Write Current Selection
DS1-DS7	C	Drive Select
JP14 (Out)	C	In = Write Protect
JP15 (Out)	F	Not Used
JP16-JP29	C	Hard Sector Size
JP30 (In)	C	Out = Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In = Enable ESDI Programmable Sector Size (Hard Sector Mode Only)
JP31 (Out)	C	In = Soft Sector Mode. Out = Hard Sector Mode.
JP32-JP35	F	Head Configuration
JP36 (Out)	F	Reserved
JP37 (Out)	C	In for 24-Byte PLO Sync Field, Out for 14-Byte PLO Synchronization Field
JP38 (Out)	F	Reserved
JP39 (Out)	F	Reserved
JP41	F	Test Pins (Differential Data Read Signals)
JP42 (In, A-B)	F	Test (WRITE GATE to Flex Circuit)
JP43 (In)	F	Test Out Disables Onboard RAM

* C = Customer Configurable
F = Factory Select

Table 8-7
Jumper Selections (PCB Part Number 1015468)

JUMPER	TYPE *	DESCRIPTION
JP1 (B-C)	F	Encoded Write Data
JP4 (out)	F	Out = 1,7 Encoding
JP5 (In)	F	In = 15 Mbit/sec Transfer Rate (Hard Wire)
JP6 (In)	C	In = Motor Remote Spinup Option Disabled Out = Motor Spinup Option Enabled
DS1-DS7	C	Drive Select
JP7 (B-C)	C	Read Gate Delay Option
JP8 (Out)	C	Read Gate Delay Option
JP9 (A-B)	C	INDEX Width Selection. A-B = 2.8µsec. B-C = 70µsec.
JP10 (In)	F	Write Current Select
JP14 (Out)	C	In = Write Protect
JP16-JP29	C	Hard Sector Size
JP30 (In)	C	Out = Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In = Enable ESDI Programmable Sector Size (Hard Sector Mode Only)
JP31 (Out)	C	In = Soft Sector Mode. Out = Hard Sector Mode.
JP32-JP35	F	Drive Model Selection. See Table 8•2.
JP36 (Out)	F	Reserved
JP37	F	Bytes per PLO Sync Field. See Table 8•3.
JP38 (Out)	F	Reserved
JP39	F	Bytes per PLO Sync Field. See Table 8•3.
JP41 (Out)	F	Test Pins (Differential Data Read Signals)
JP42 (B-C)	F	Write Enable Select
JP43 (In)	F	Test Out Disables Onboard ROM

* C = Customer Configurable
F = Factory Select

Table 8•8
Jumper Selections (PCB Part Number 1014520)

JUMPER	TYPE *	DESCRIPTION
JP1 (B-C)	F	Encoded Write Data
JP4 (Out)	F	Out = 1,7 Encoding
JP5 (In)	F	In = 15 Mbit/sec Transfer Rate (Hard Wired)
JP6 (In)	C	In = Motor Remote Spinup Option Disabled Out = Motor Spinup Option Enabled
DS1-DS7	C	Drive Select
JP7 (B-C)	C	Read Gate Delay Option
JP8 (Out)	C	Read Gate Delay Option
JP9 (A-B)	C	INDEX Width Selection. A-B = 2.8µsec. B-C = 70µsec.
JP10 (In)	F	Write Current Select (Hard Wired)
JP14 (Out)	C	In = Write Protect
JP16-JP29	C	Hard Sector Size
JP30 (In)	C	Out = Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In = Enable ESDI Programmable Sector Size (Hard Sector Mode Only)
JP31 (Out)	C	In = Soft Sector Mode. Out = Hard Sector Mode.
JP32-JP34	F	Drive Model Selection. See Table 8•2.
JP36 (Out)	F	Reserved
JP37 (In)	F	Bytes per PLO Sync Field. See Table 8•3.
JP38	F	Model Select 1
JP39 (In)	F	Bytes per PLO Sync Field. See Table 8•3.
JP41 (Out)	F	Test Pins (Differential Data Read Signals)
JP42 (B-C)	F	Write Enable Select
JP43 (In)	F	Test Out Disables Onboard ROM
JP 35	F	Model Select 0

* C = Customer Configurable
F = Factory Select

Table 8•9
Jumper Selections (PCB Part Number 1023821)

JUMPER	TYPE *	DESCRIPTION
JP1 (A-B)	F	Encoded Write Data
JP4 (Out)	F	Out = 1,7 Encoding
JP5 (In)	F	In = 15 Mbit/sec Transfer Rate (Hard Wired)
JP6 (In)	C	In = Motor Remote Spinup Option Disabled Out = Motor Spinup Option Enabled
DS1-DS7	C	Drive Select
JP7 (B-C)	C	Read Gate Delay Option
JP8 (Out)	C	Read Gate Delay Option
JP9 (A-B)	C	INDEX Width Selection. A-B = 2.8µsec. B-C = 70µsec.
JP10 (In)	F	Write Current Select (Hard Wired)
JP14 (Out)	C	In = Write Protect
JP16-JP29	C	Hard Sector Size
JP30 (In)	C	Out = Disable ESDI Programmable Sector Size (Hard Sector Mode Only) In = Enable ESDI Programmable Sector Size (Hard Sector Mode Only)
JP31 (Out)	C	In = Soft Sector Mode. Out = Hard Sector Mode.
JP32-JP34	F	Drive Model Selection. See Table 8•2.
JP36 (Out)	F	Reserved
JP37 (In)	F	Bytes per PLO Sync Field. See Table 8•3.
JP38	F	Model Select 1
JP39 (In)	F	Bytes per PLO Sync Field. See Table 8•3.
JP41 (Out)	F	Test Pins (Differential Data Read Signals)
JP42 (B-C)	F	Write Enable Select
JP43 (In)	F	Test Out Disables Onboard ROM
JP 35	F	Model Select 0

* C = Customer Configurable
F = Factory Select

Table 8•10
Jumper Selections (PCB Part Number 1023856)

JUMPER	TYPE*	DESCRIPTION
JP1 (In)	F	Bytes per PLO Sync Field
JP2 (Out)	F	Reserved
JP3 (Out)	F	Reserved
JP4 (In)	F	In for 8760 Out for 8380
JP5 (In)	F	Vendor ID
JP6 (In)	C	In = Motor Spinup Option Disabled Out = Motor Spinup Option Enabled
JP7 (In)	F	Vendor ID
JP8 (In)	F	Vendor ID
JP9 (In)	C	Short Index
JP10 (Out)	C	Long Index
JP11 (Out)	F	Decayed Write Current
JP12 (In)	F	Normal Write Current
JP13 (Out)	F	Hardware DC Erase
JP14 (Out)	C	In = Write Protect
JP15 (In)	F	Read Gate Nominal Delay
JP16-JP29	C	Hard Sector Size
JP30 (In)	C	In = Enable ESDI Programmable Sector Size Out = Disable ESDI Programmable Sector Size
JP31 (Out)	C	In = Soft Sector Mode Out = Hard Sector Mode
JP32 (In)	F	Read Gate Nominal Delay
JP33 (Out)	F	Read Gate Nominal Delay
JP34 (Out)	F	Read Gate Nominal Delay
JP35 (In)	F	In = Normal Write Current Out = Decay Write Current
JP36 (Out)	F	In = Write Unsafe Disable Out = Write Unsafe Enable
JP37 (In)	F	Bytes per PLO Sync Field
JP38 (In)	F	Normal Write Current
JP39 (Out)	F	Decayed Write Current

* C = Customer Configurable
F = Factory Select

Table 8•11
Jumper Selections (PCB Part Number 1023051)

8.2 READ GATE DELAY JUMPERS

Jumpers JP15, JP32, JP33 and JP34 on PCB number 1023051 and jumpers JP7 and JP8 on all other PCBs have been provided to allow a specified delay to be set on the read gate received by the controller. As shipped by the factory the jumpers for PCB number 1023051 are configured for a delay of 533 nsec. All other PCBs are configured for zero delay. See Tables 8•12 and 8•13 below for reference.

NOMINAL DELAY nsec	O = OPEN		S = SHORT	
	JP8		JP7	
	A - B	B - C	A - B	B - C
0	O	O	O	S
423	S	O	S	O
533	O	S	S	O
633	S	O	O	O
933	O	S	O	O
1233	O	O	S	O

Table 8-12
Read Gate Delay Jumper Settings

NOMINAL DELAY nsec	O = OPEN		S = SHORT	
	JP32	JP33	JP34	JP15
45	O	S	O	O
423	S	O	S	O
533	S	O	O	S
633	O	O	S	O
933	O	O	O	S
1233	S	O	O	O

Table 8-13
Read Gate Delay Jumper Settings (PCB 1023051)

8.3 WRITE PROTECT SELECTION JUMPER (JP14)

Jumper JP14 is the write project jumper. When the jumper is present (installed), the drive is write protected and can only be read; no writing can take place. As shipped from the factory, jumper JP14 is removed.

8.4 SEQUENTIAL SPINDLE MOTOR SPINUP JUMPER (JP6)

The spindle motor spinup jumper (JP6) allows a string of drives to be started sequentially by the controller. When the jumper is present (installed), the drive automatically spins up as soon as power is applied. If JP6 is removed, the drive is started by issuing the appropriate command from the controller. As shipped from the factory, jumper JP6 is installed.

8.5 TEST JUMPERS (JP1-JP3)

These jumpers provide access to certain test signals. The specific signals and the normal factory settings are shown below in Table 8•14, Test Pin Jumpers.

JUMPER	FACTORY SETTING	NOTES ON FUNCTION
JP 1	In	Encoded Write Data; TTL
JP2	In	Used for Phase Margin Testing; ECL Level Clock. Output = Pin 18. Input = Pin 19
JP 3	In	Used for Phase Margin Testing; ECL Level Data. Output = Pin 20. Input = Pin 21.

Note: *These jumper settings and functions do not apply to those on PCB number 1023051.*

Table 8•14
Test Pin Jumpers

8.6 HARD SECTOR CONFIGURATION JUMPERS (JP16-JP29)

Jumper JP31 selects the mode of operation. Jumper JP31 installed configures the drive as a soft sector drive; removed, it configures the drive as a hard sectored drive.

Jumpers JP16 through JP29 allow the user to configure the drive's hard sector size. The sector size can range from a minimum of 123 to a maximum of 31,410 unformatted bytes per sector, with 1 byte granularity.

The hard sector configuration jumpers are encoded in a binary fashion, with JP16 being the least significant byte and JP29 being the most significant byte. An installed jumper selects the binary value. See Table 8•15, Customer Selectable Jumpers.

Jumper JP30, if installed, enables setting the hard sector size over the ESDI. The drive must be in hard sector mode, that is, JP31 removed.

JUMPER	BINARY VALUE FOR EACH JUMPER*
JP16	1
JP17	2
JP18	4
JP19	8
JP20	16
JP21	32
JP22	64
JP23	128
JP24	256
JP25	512
JP26	1,024
JP27	2,048
JP28	4,096
JP29	8,192

** Used to Determine the Number of Unformatted Bytes/Sector*

Example: 54 Sectors Desired

1. $\frac{31,410}{54}$ = *581 Unformatted Bytes/Sector*

2. *Install Jumpers J25, +J22, J18, +J16*
   # Bytes/Sector 512 + 64 + 4 + 1 = 581

Table 8•15
Customer Selectable Jumpers

9.0 MEDIUM DEFECTS AND ERRORS

Defects on the medium surface are identified on both a paper defect map and a defect map written on the drive according to the ESDI format rules. These defect maps indicate the head number, track number, and number of bytes from index, for each defect.

The maximum number of encoded (NRZ) defects per drive is 200 for the XT-8380E/EH, and 300 for the XT-8760E/EH. The maximum number of defects per surface cannot exceed 100. See Table 9•1, Maximum Number of Defects. Cylinder zero is certified to be defect-free.

DRIVE MODEL	NO. OF DISKS	NO. OF DATA SURFACES	MAXIMUM NO. OF DEFECTS
XT-8380E/EH	5	8	200
XT-8760E/EH	8	15	300

Table 9•1
Maximum Number of Defects

As shipped, the drive contains three copies of the defect map, written in different locations on the disks.

One complete defect list resides on sector zero of cylinder 1,631. Identical copies are located on sector zero of cylinder 1,623 and sector zero of cylinder 1,632. This allows for redundancy should an error occur on cylinder 1,631. Sector zero of any surface contains the defects for that surface. The format for the data field portion of this sector is 512 bytes, with 2 bytes of cyclic redundancy check (CRC) ($x^{16} + x^{12} + x^5 + 1$). See Figure 9•1, Defect List Format.

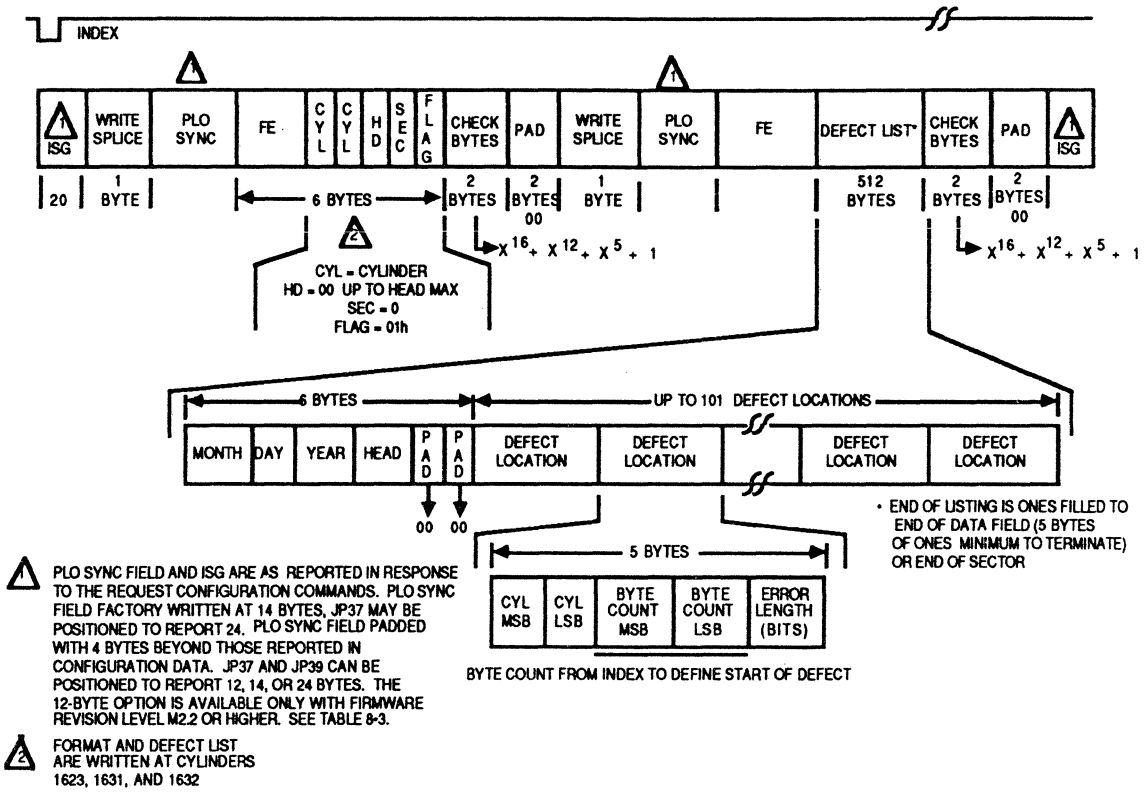


Figure 9-1
Defect List Format

Defect locations are identified by fields 5 bytes long. Other byte definitions are shown in Figure 9-1. Byte count is the number of bytes from INDEX.

The location of the start of the actual defect may vary from the location specified on the defect list by up to ±10 bytes.

The end of the defect list for each surface is indicated by 5 bytes of ones in the defect location field, or the end of the sector.

The CRC check bytes should be used, if that capability exists, but may be ignored if multiple reads are a more desirable approach.

READ GATE can be asserted between bytes five and twenty-five, from INDEX, to read the header for drives reporting 14-byte PLO synchronization fields. Likewise, for drives reporting 24-byte PLO fields, READ GATE can be asserted between bytes five and twenty. For the data field it is not necessary to toggle READ GATE to reacquire the clock. If it is, however, READ GATE can be asserted between bytes zero and seven, after receiving the CRC bytes on NRZ READ DATA, for drives reporting 14-byte PLO synchro-

nization fields. Likewise, for drives reporting 24-byte PLO synchronization fields, READ GATE may be asserted between bytes zero and two from the CRC bytes.

APPENDIX: UNITS OF MEASURE

Abbreviation	Meaning
A/m	amps per meter
AWG	average wire gauge
bpi	bits per inch
fci	flux changes per inch
g	gram
Gbyte	gigabyte
Hz	hertz
mA	milliamp
µA	microamp
Mbit	megabit
Mbyte	megabyte
µm	micrometer
msec	millisecond
µsec	microsecond
nsec	nanosecond
Oe	oersted
RH	relative humidity
rpm	revolutions per minute
tpi	tracks per inch
xxB	binary values
xxh	hexadecimal values

GLOSSARY

3rdPty. Third party

ack. Acknowledge

ADR. Address

ANSC. American National Standards Committee

ANSI. American National Standards Institute

arbitration winner. The arbitrating SCSI device which has the highest SCSI address.

assert. A signal driven to the true state.

async. Asynchronous

BCV. Buffer control valid

bit. Binary digit

byte. Eight consecutive binary digits

C/C. Continuous/composite (format)

CCS. Common Command Set

CDB. Command descriptor block, the structure used to communicate requests from an initiator to a target.

cmd. Command

connect. The function that occurs when an initiator selects a target to start an operation.

CRC. Cyclic redundancy check

CSA. Canadian Standards Association

dBA. Decibel, audible

DC. Direct current

DCR. Disabled correction (signal)

disconnect. The function that occurs when a target releases control of the SCSI bus allowing it to go to the BUS FREE phase.

DMA. Direct memory access

DTE. Disable transfer on error

EBP. Erase bypass

ECC. Error correction code

ECL. Emitter-coupled logic

EDAC. Error detection and correction

EEC. Enable early connection

EH. ESDI High Performance

EIA. Electrical Industry Association

ENDEC. Encoder/decoder

ERA. Erase all

ESDI. Enhanced Small Device Interface

FCC. Federal Communication Commission

firmware. Computer programs encoded permanently into a ROM

FW. Firmware

G. Constant of gravitation

gnd. Ground

HDA. Head disk assembly

HW. Hardware

I/O. Input and/or output

initiator. A SCSI device, usually a host system, that requests that an operation be performed by another SCSI device.

intermediate status. A status code sent from a target to an initiator upon completion of each command in a set of linked commands, except for the last command in the set.

ISG. Inter-sector gap

ISO. International Standardization Organization

LBA. Logical block address

LED. Light-emitting diode

logical thread. The logical path which exists between an initiator's memory and a bus device LUN, even though the physical path may be disconnected.

logical unit. A physical or virtual device addressable through a target.

LSB. Least significant byte

LUN. Logical unit number, an encoded 3-bit identifier for the logical unit.

MFM. Modified frequency modulation (encoding)

MO. Magneto optics

MSB. Most significant byte

MTBF. Mean time between failures

MTTR. Mean time to repair

MZCAV. Maxtor Zoned Constant Angular Velocity (format)

N.C. No connection

negate. A signal driven to the false state

nom. Nominal

OEM. Original equipment manufacturer

one. True signal value

P-P. Peak to peak

P/N. Part number

parity. A method of checking the accuracy of binary numbers

PC. Polycarbonate

PCB. Printed circuit board

PCF. Page control field

peripheral device. A peripheral that can be attached to a SCSI device

PLL. Phase-locked loop

PLO. Phase-locked oscillator

PM. Preventive maintenance

PMI. Partial medium indicator

POH. Power On hours

PTRN. Pattern

R/W. Read and/or write

RAM. Random-access memory

reconnect. The function that occurs when a target selects an initiator to continue an operation after disconnect.

req. Request

reserved. Bits, bytes, fields and code values that are set aside for future standardization.

RLL. Run-length limited

ROM. Read-only memory

SCSI. Small Computer Systems Interface

status. One byte of information sent from a target to an initiator upon completion of each command.

STD. Standard

SW. Software

sync. Synchronization, synchronous

Tahiti Family disk drive. Family of magneto optical disk drive

target. A SCSI device that performs an operation requested by an initiator.

tbd. To be determined. Values which are not defined as of the date this manual is published.

TLA. Top level assembly

TTL. Transistor-transistor logic

typ. Typical

UL. Underwriter's Laboratories, Inc.

UNC. United Core Thread, "C" Category

VDE. Verband Deutscher Electrotechniker

vendor unique. The bits, fields, or code values that are vendor specific.

WORM. Write once read multiple

zero. False signal code

µC. Microcomputer