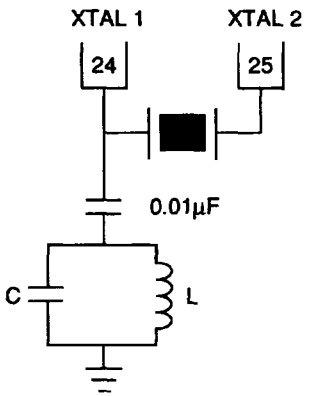
REFERENCE OSCILLATOR

An internal reference oscillator generates the standby reference for the PLL. For the 32D5321/5322 and the 32D535/5351, a series resonant crystal of twice the data rate should be used between XTAL1 and XTAL2. For the 32D5362, the series resonant crystal should be selected at three times the data rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

If it is desired to operate a crystal at a non-fundamental or harmonic frequency, then the following network is suggested:



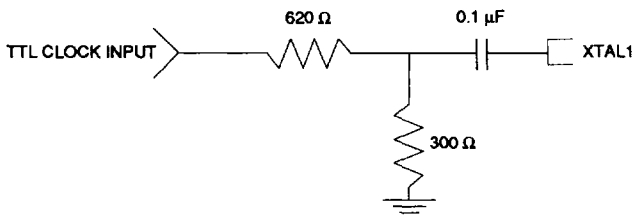
$$\omega_o = 2\Pi F_o = \frac{1}{\sqrt{LC}}$$

$$Q_o = \omega_o C R_{in}$$

The typical input impedance looking into XTAL1 is approximately Rin = 250Ω. It is recommended to design the value of Q_o at approximately 10 to 15. Therefore, a resonant frequency of F_o = 20 MHz would result in L ≅ 0.16 μH and C ≅ 380 pF.

ATTENUATOR CIRCUIT

If a crystal oscillator is not desired, then an external TTL Compatiable reference may be applied to XTAL1 leaving XTAL2 open. It is required, however that the TTL signal be attenuated then A.C. coupled into XTAL1 using the following network:



The signal amplitude into XTAL1 should be attenuated to approximately 1.0 to 2.0 Vp-p; this will insure that the transients associated with TTL switching characteristics won't couple into the data synchronizer and degrade performance.

LOOP FILTER

The performance of the data synchronizer is directly related to the selection of the loop filter. The loop filter characteristics should be optimized for:

(A) Fast Acquisition

The ability of the loop to quickly obtain lock when the input signal to the Phase Detector is switched between the reference oscillator (crystal) and the Read Data ($\overline{RD}$). Fast acquisition implies a large loop bandwidth so that it can quickly respond to changes at the input.

(B) Data Margin

The ability of the loop to ignore bit shifts (jitter) and maintain a well centered window about the data pulse train. In general, it is not desirable to allow the loop to respond to a single shifted bit as this would cause the subsequent bit to be poorly centered within its window and possibly cause an error. This requirement implies a small loop bandwidth reducing the sensitivity to high frequency jitter.

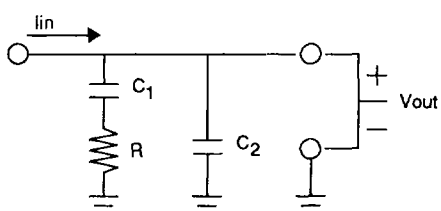
(C) Data Tracking

The ability to respond to instantaneous changes in phase and frequency of the data. This can be a result of such phenomena as disk rotational speed variations which cause changes in the characteristics of the incoming data stream. In general, this requirement is consistent with that of fast acquisition, however, this depends upon the application.

Although the loop performance characteristics place conflicting requirements on the loop bandwidth, the architecture of the Silicon Systems chip family significantly simplifies the design by minimizing the "step in phase" and "step in frequency" encountered when switching the Phase Detector input reference signal. A zero phase restart technique is employed to minimize the initial phase error while the standby reference oscillator keeps the VCO at the center frequency during non-read modes.

One approach in determining the initial loop filter selection is to consider the requirements imposed during acquisition. This includes both acquiring lock to the crystal reference in non-read modes, as well as locking to the preamble field prior to decoding data. The format of the sector will dictate which of these two criteria imposes the tightest restriction on acquisition.

The requirements for acquiring lock to the crystal oscillator are application specific and usually depend upon the length of the Write Splice gap. Therefore, the design approach employed in this analysis will be based upon the requirements during acquisition to the preamble field. The length (in time) of the preamble field is set by the data synchronizer's locking sequence. Knowing this length in time, and that our initial phase error is less than 0.5 radians, we can determine an acceptable loop bandwidth (ωn) and damping factor (ζ).
One possible loop filter configuration is as follows:



The role of C1 is as an integrating element. The larger this capacitance, the longer the acquisition time; the smaller the capacitance, the greater the ability to track high frequency jitter. The resistor R reduces the phase shift induced by C1. The capacitor C2 will suppress high frequency transients and will have minimal effect on the loop response if it is small relative to C1 (typically C2 = C1/10)

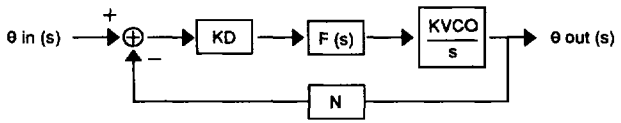
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + C_2/C_1\right)}$$

If C2 << C1, then:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The overall block diagram for the phaselock loop can be described as:



Where:

KD = Phase Detector gain [A/rad]

F(s) = Loop filter impedance [V/A]

KVCO/s = VCO control gain [rad/s V]

N = The ratio of the reference input frequency to the VCO output frequency

The closed loop transfer function is:

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + GH(s)} = \frac{KD \cdot KVCO[(1 + sRC_1)/C_1]}{s^2 + s[N \cdot KD \cdot KVCO \cdot R] + \frac{N \cdot KD \cdot KVCO}{C_1}}$$

by putting the characteristic equation (denominator) in the form of:

$$s^2 + 2s\zeta\omega n + \omega n^2$$

we can solve for ωn and ζ to get:

$$\omega n^2 = \frac{N \cdot KD \cdot KVCO}{C1} \qquad \zeta = \frac{N \cdot KD \cdot KVCO \cdot R}{2\omega n}$$

Now we can solve for R, C1 and C2:

$$C1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} \qquad R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} \qquad C_2 = \frac{C_1}{10}$$

where: ωn = loop bandwidth and, ζ = loop damping factor

Because of the nature of Run Length Limited (RLL) codes, the Phase Detector will only be enabled during a data pulse. This technique allows the VCO to run at a center frequency with period, TVCO, equal to one encoded data bit cell time.

Figure 1 represents the relationship between the VCO output when locked to various Phase Detector input signals.

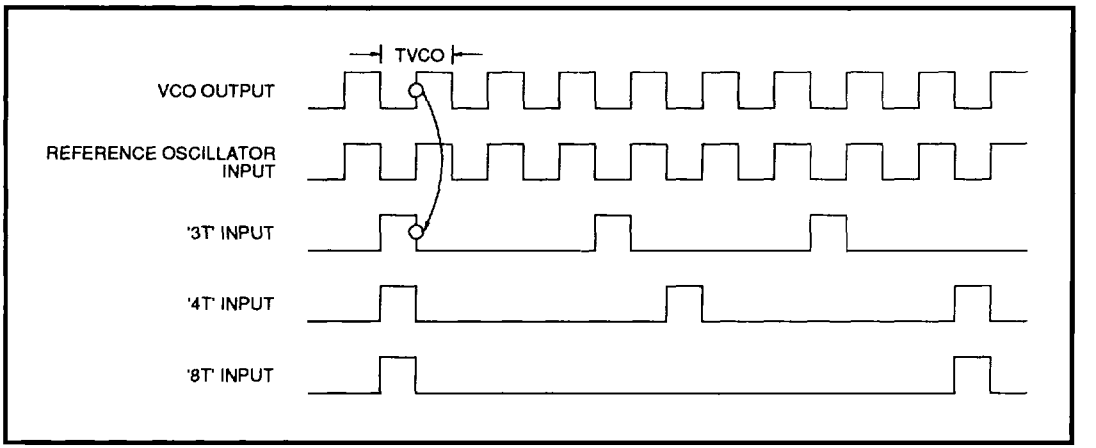


FIGURE 1: Relationship of VCO Output to Phase Detector Input

The average amplitude of the Phase Detector gain depends upon the Phase Detector input signal. When the PLL is locked to the reference oscillator, the Phase Detector is continuously enabled and the gain is at its maximum. When the PLL is tracking data and the input is an "8T" pattern, then the Phase Detector gain is at its minimum. The following indicates the value of "N" for various input conditions:

N = 1.0	for θin = reference oscillator
N = 0.33	for θin = 3T (100) preamble field (maximum data frequency)
N = 0.25	for θin = 4T (1000) preamble field
N = 0.125	for θin = 8T (minimum data frequency)

Throughout this analysis the PLL has been considered as a continuous time system. In actuality the characteristics of the Phase Detector result in a sampled data system. By utilizing an integrating loop filter to average and smooth the Phase Detector charge pump output pulses, this analogy should be reasonable.

Determining an acceptable amount of phase error after locking to the preamble field depends upon the system requirements. In addition, it may be necessary to consider the effects of frequency steps in applications where motor speed control tolerances are significant. Generally, an acceptable amount of error is defined to be that amount which when added to all other timing error contributors, results in the data being within its timing window by the required margin.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth.

Figure 2 represents the phase error's response in time to a transient step in phase as a function of the loop bandwidth and damping factor. Figure 3 indicates the response of the VCO control voltage to compensate for this step in phase.

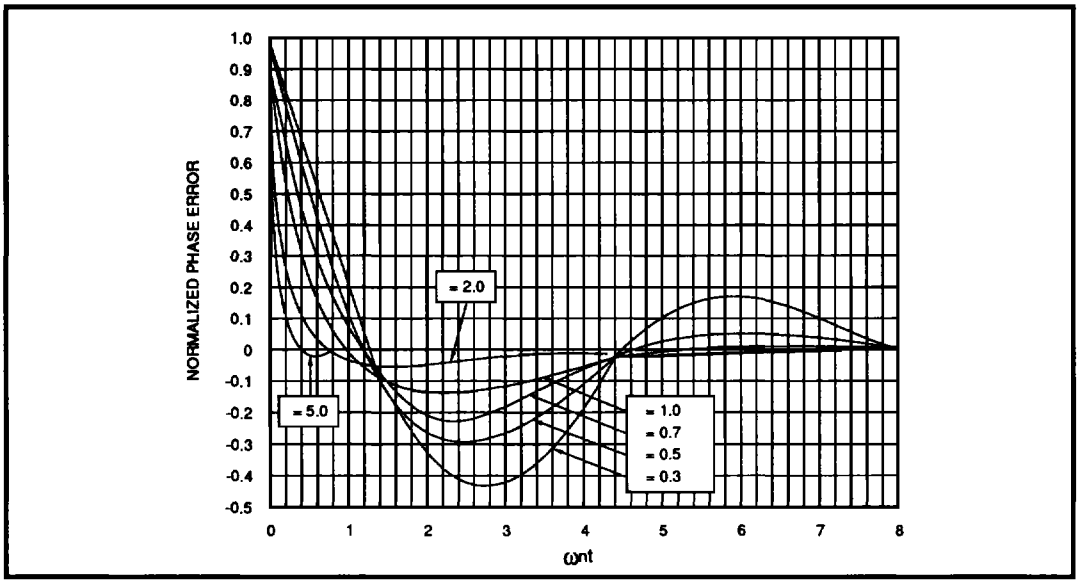


FIGURE 2: Transient Phase Error θe(t) Due To a Step In Phase Δθ

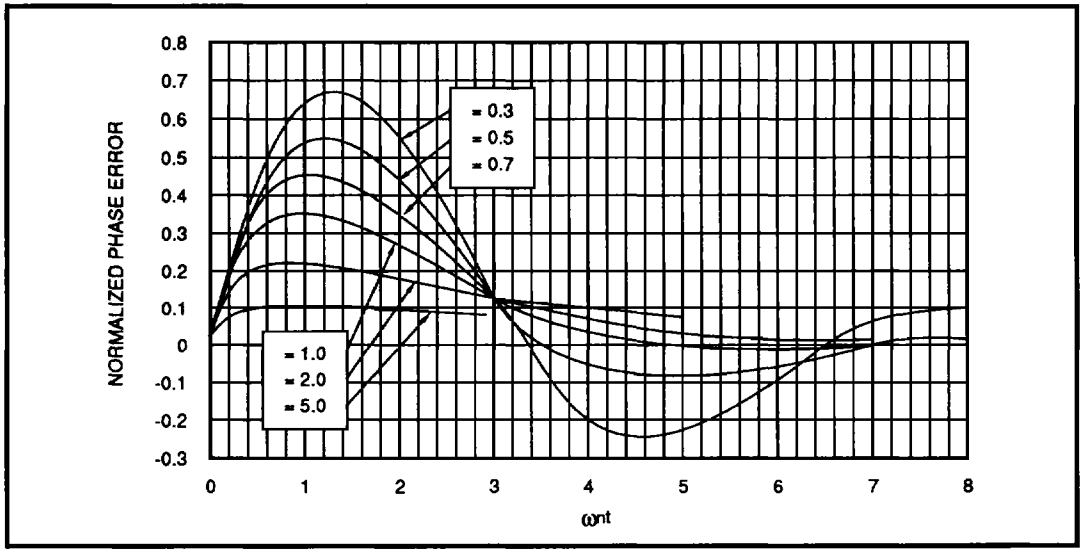


FIGURE 3: Transient Phase Error θe(t) Due to a Step In Frequency Δω

APPLICATION OF THE SSI 32D5321/5322

10 Mbit/s Soft Sector Example

For a data rate of 10 Mbit/s the SSI 32D5321/5322 requires a series resonant crystal of twice the data rate or 20 MHz. In the Soft Sector mode the PLL locking sequence allows the VCO to be within a determined amount of error after 38 x '3T' (100) bit groups. At 10Mbit/s each data bit cell time, TVCO, is equal to 50 ns. This results in:

$$t_{max} = (38)\ (3)\ (50\ ns) = 5.7\ \mu s$$

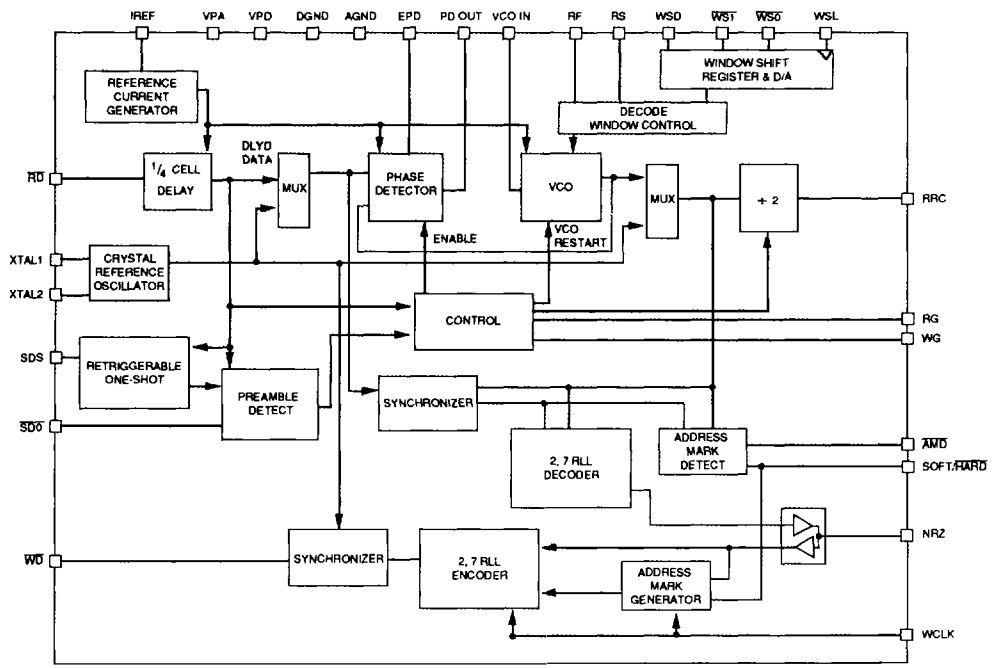
Therefore, the PLL has 5.7 µs to settle to within an acceptable amount of error before tracking and decoding data. Because the SSI 32D5321/22 employs a zero phase restart technique, the initial phase error is less than 8% TORC (0.5rad) or:

$$\theta e < (0.08)(100\ ns)$$

$$\theta e < 8\ ns$$

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth. For this example we will let $\zeta = 0.7$.

SSI 32D5321/5322 BLOCK DIAGRAM



As shown in Figure 2, with $\zeta = 0.7$, our initial transient phase error will be at most 22% of its original value at $\omega nt = 2.3$, 7.5% at $\omega nt = 4.0$, etc. For this example we want the final phase error to be less than 1% of its original level. This results in a ωnt between 5 and 6. To simplify the results, let $\omega nt = 5.7$.

Now, $\omega nt = 5.7$
and $t_{max} = 5.7\ \mu s$
$\therefore \omega n = 1.0 \cdot 10^6$ rad/s
with $\zeta = 0.7$

Since we are evaluating the loop response during acquisition to the '3T' preamble, N = 0.33.

4

Now we have all the information required to calculate the loop filter component values.

For the SSI 32D5321:

$$RR = \frac{40.67}{10\ Mbs} - 0.5 = 3.567\ k\Omega$$

$\omega n = 1.0 \cdot 10^6$ rad/s

$\zeta = 0.7$

$KD(typ) = 0.309/(RR+500) = 7.6 \cdot 10^{-5}$ A/rad

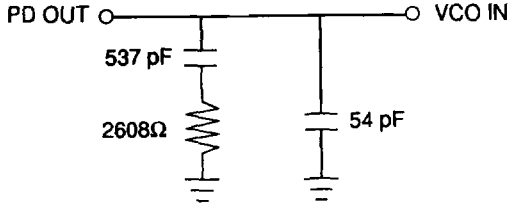
$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/To = 2.14 \cdot 10^7$ rad/s V

$N = 0.33$

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} = 2608\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 537\ pF$$

$$C_2 = \frac{C_1}{10} = 54\ pF$$



For the SSI 32D5322:

$$RR = \frac{43.86}{10\ Mbs} - 1.2 = 3.186\ k\Omega$$

$\omega n = 1.0 \cdot 10^6$ rad/s

$\zeta = 0.7$

$KD(typ) = 0.309/(RR+500) = 8.38 \cdot 10^{-5}$ A/rad

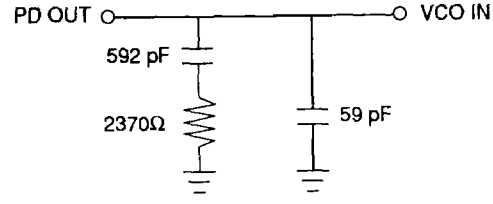
$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/To = 2.14 \cdot 10^7$ rad/s V

$N = 0.33$

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} = 2.37\ k\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 592\ pF$$

$$C_2 = \frac{C_1}{10} = 59\ pF$$



This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

Data Synchronizer Family Application Notes

SSI 32D5321/5322
SSI 32D535/5351
SSI 32D5362

32D5321

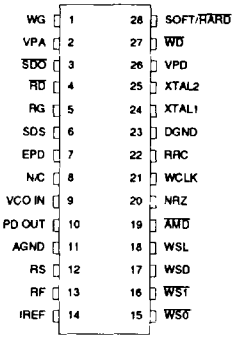
DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	ωnt	BANDWIDTH $\omega n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(KΩ)	Cd(pF)	Rd(KΩ)	R(KΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.1	680	68
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51

32D5322

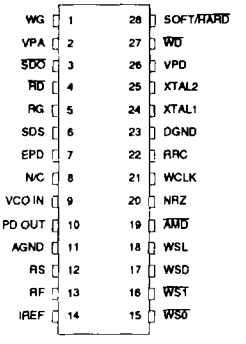
DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME t_{max} (μs)	ωnt	BANDWIDTH $\omega n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(KΩ)	Cd(pF)	Rd(KΩ)	R(KΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.64	100	13.0	2.94	710	71
10.0	0.7	5.7	5.7	1.0×10^6	3.19	100	10.0	2.37	590	59
15.0	0.7	3.8	5.7	1.5×10^6	1.72	100	6.49	1.43	654	65

LAYOUT CONSIDERATIONS

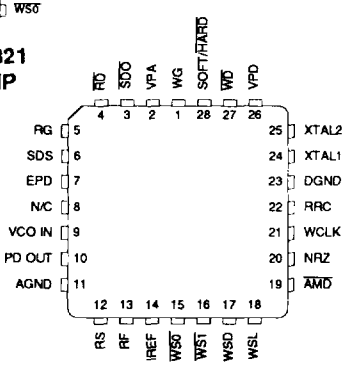
As with other high frequency analog devices the SSI 32D5321/22 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D5321/22, and associated circuitry, from other circuits on the PCB.



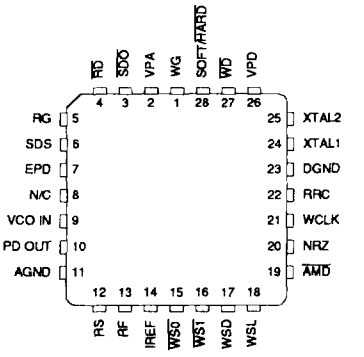
SSI 32D5321
28-Pin DIP



SSI 32D5322
28-Pin DIP



SSI 32D5321
28-Pin PLCC



SSI 32D5322
28-Pin PLCC

APPLICATION OF THE SSI 32D535/5351

10 Mbit/s Soft Sector Example:

For a data rate of 10 Mbit/s the SSI 32D535/5351 requires a series resonant crystal of twice the data rate or, 20 MHz. In the Soft Sector mode the PLL locking sequence allows the VCO to be within a determined amount of error after 38 x '3T' (100) bit groups. At 10 Mbit/s each data bit cell time, TVCO, is equal to 50 ns. This results in:

$$t_{max} = (38)(3)(50\ ns) = 5.7\ \mu s$$

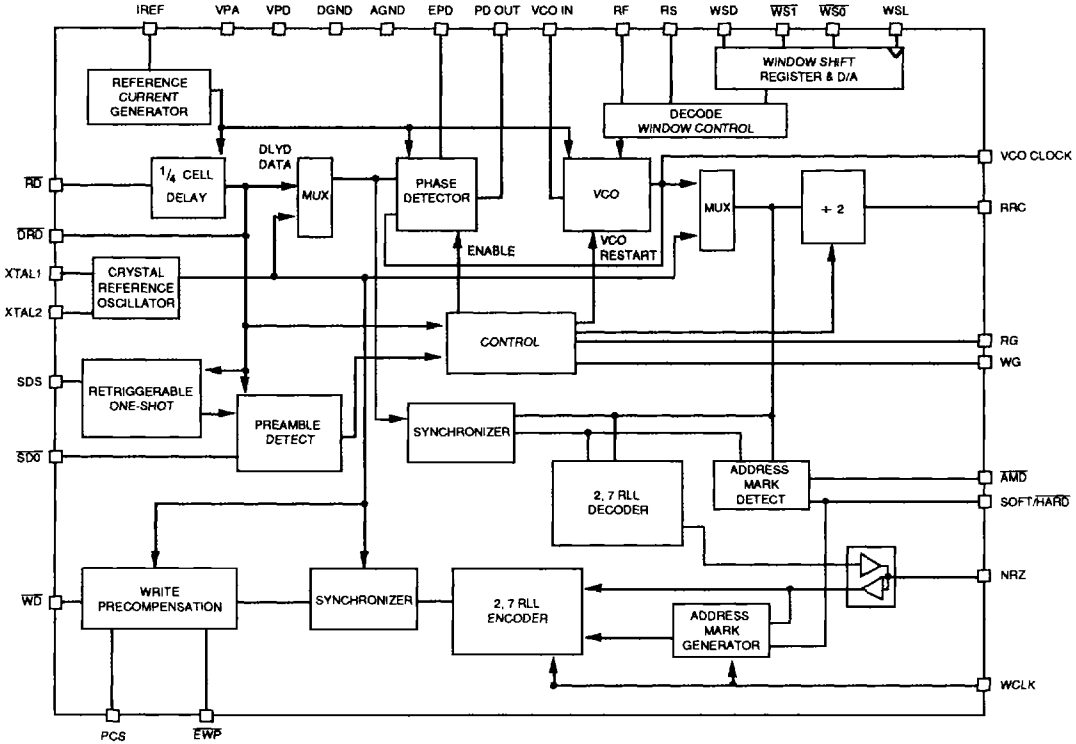
Therefore, the PLL has 5.7 µs to settle to within an acceptable amount of error before tracking and decoding data. Because the SSI 32D535 employs a zero phase restart technique, the initial phase error is less than 8% TORC (0.5rad) or:

$$\theta e < (0.08)(100\ ns)$$

$$\theta e < 8\ ns$$

4

SSI 32D535/5351 BLOCK DIAGRAM



In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth. For this example we will let $\zeta = 0.7$.

As shown in Figure 2, with $\zeta = 0.7$, our initial transient phase error will be at most 22% of its original value at $\omega nt = 2.3$, 7.5% at $\omega nt = 4.0$, etc. For this example we want the final phase error to be less than 1% of its original level. This results in a ωnt between 5 and 6. To simplify the results, let $\omega nt = 5.7$.

This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

Now,

$\omega nt = 5.7$

and $t_{max} = 5.7\ \mu s$

$\therefore\ \omega n = 1.0 \cdot 10^6$ rad/s

with $\zeta = 0.7$

Since we are evaluating the loop response during acquisition to the '3T' preamble, N = 0.33.

Now we have all the information required to calculate the loop filter component values.

For the SSI 32D535:

$$RR = \frac{40.67}{10MB} - 0.5 = 3.567\ k\Omega$$

$\omega n = 1.0 \cdot 10^6$ rad/s

$\zeta = 0.7$

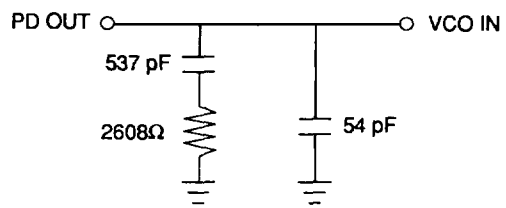
$KD(typ) = 0.309/(RR+500) = 7.6 \cdot 10^{-5}$ A/rad

$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/T0 = 2.14 \cdot 10^7$ rad/s V

$N = 0.33$

$$R = \frac{2\zeta\omega_n}{N \cdot KD \cdot KVCO} = 2608\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 537\,pF \qquad C_2 = \frac{C_1}{10} = 54\ pF$$



For the SSI 32D5351:

$$RR = \frac{76}{DR} - 1.75 = 5.85\ k\Omega$$

$\omega n = 1.0 \cdot 10^6$ rad/s

$\zeta = 0.7$

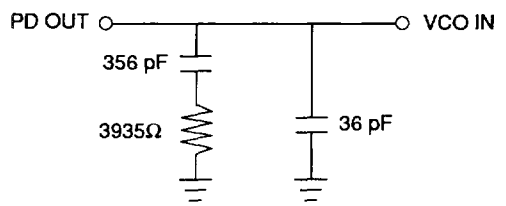
$KD(typ) = (0.34/RR+900) = 5.04 \cdot 10^{-5}$ A/rad

$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/T0 = 2.14 \cdot 10^7$ rad/s V

$N = 0.33$

$$R = \frac{2\zeta\omega_n}{N \cdot KD \cdot KVCO} = 3935\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} 356\,pF \qquad C_2 = \frac{C_1}{10} = 36\,pF$$



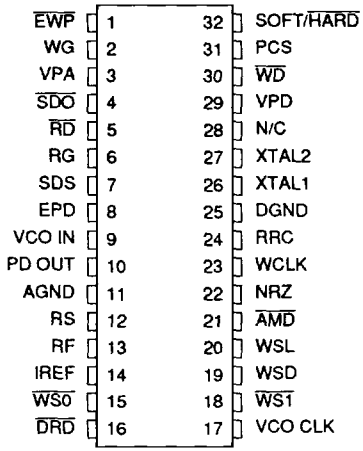
This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

32D535

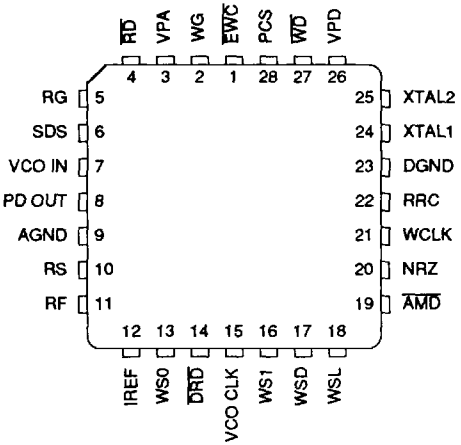
DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME tmax (μs)	ωnt	BANDWIDTH ωn (rad/sec)	EXTERNAL COMPONENT VALUES					
					RR(KΩ)	Cd(pF)	Rd(KΩ)	R(KΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.0	687	69
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51

32D5351

DATA RATE (Mbit/s)	DAMPING FACTOR,ζ	LOCK TIME tmax (μs)	ωnt	BANDWIDTH ωn (rad/sec)	EXTERNAL COMPONENT VALUES					
					RR(KΩ)	Cd(pF)	Rd(KΩ)	R(KΩ)	C_1 (pF)	C_2 (pF)
10.0	0.7	5.7	5.7	1.0×10^6	5.85	100	10.0	3.94	356	36
15.0	0.7	3.8	5.7	1.5×10^6	3.32	100	6.49	2.46	379	38



32 LEAD SOW, DIP

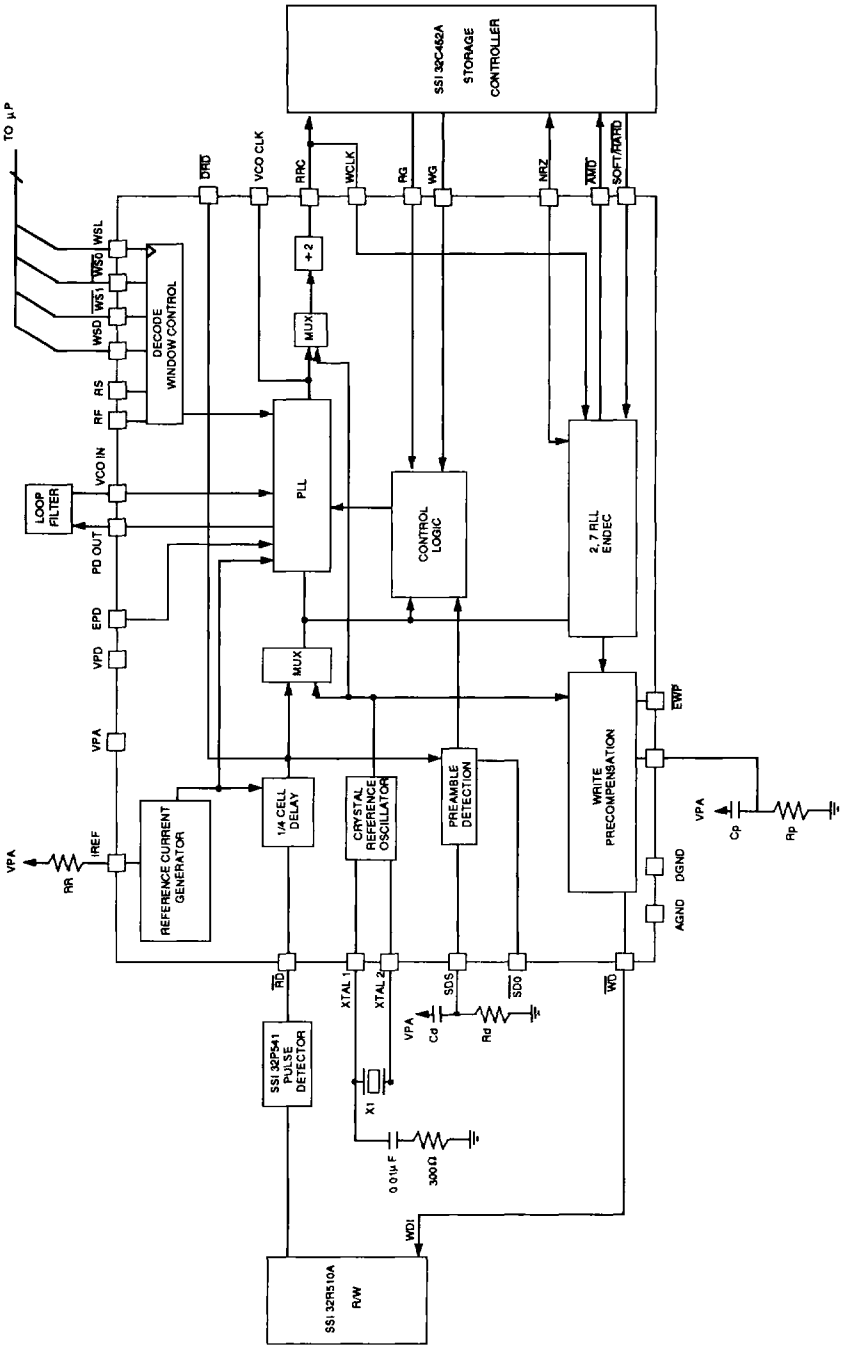


28 Pin PLCC

NOTE: Does not include the following pins which are available on the 32-Pin packages

- SDO
- EPD
- SOFT/HARD (internally pulled up high)

So must be used in soft sector applications only.



TYPICAL SSI 32D535/5351 APPLICATION

APPLICATION OF THE SSI 32D5362

15 Mbit/s Soft Sector Example

For a data rate of 15 Mbit/s the SSI 32D5362 requires a serial resonant crystal of three times the data rate or 45 MHz. In the Soft Sector mode the PLL locking sequence allows the VCO to be within a determined amount of error after 16 x '3T' (100) bit groups. At 15Mbit/s each data bit cell time, TVCO, is equal to 44.4 ns. This results in:

$$t_{max} = (16)\ (3)\ (44.4\ ns) = 2.1\ \mu s$$

Therefore, the PLL has 2.1 µs to settle to within an acceptable amount of error before tracking and decoding data. Because the SSI 32D536 employs a zero phase restart technique, the initial phase error is less than 16% TORC (1.0rad) or:

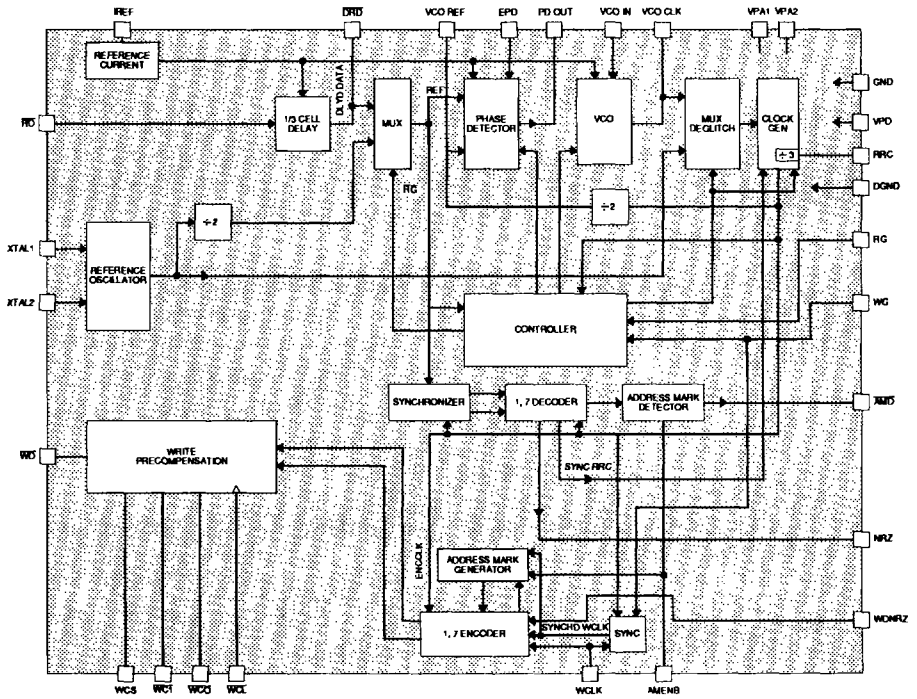
$$\Delta\theta e < (0.16)(66.7\ ns)$$

$$\Delta\theta e < 10.7\ ns$$

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth. For this example we will let $\zeta = 0.7$.

4

SSI 32D5362 BLOCK DIAGRAM



As shown in Figure 2, with $\zeta = 0.7$, our initial transient phase error will be at most 22% of its original value at $\omega nt = 2.3$, 7.5% at $\omega nt = 4.0$, etc. For this example we want the final phase error to be less than 15% of its original level. This results in a ωnt between 3 and 4. To simplify the results, let $\omega nt = 3.2$. This results in a maximum final phase error of 1.6 ns.

Now,

$\omega nt = 3.2$

and $tmax = 2.1\ \mu s$

$\therefore \omega n = 1.5 \cdot 10^6$ rad/s

with $\zeta = 0.7$

Since we are evaluating the loop response during acquisition to the '3T' preamble, N = 0.33.

Now we have all the information to calculate the loop filter component values.

$RR = 3873\Omega$

$\omega n = 1.5 \cdot 10^6$ rad/s

$\zeta = 0.7$

$KD(typ) = 0.57/(RR+530) = 1.3 \cdot 10^{-4}$ A/rad

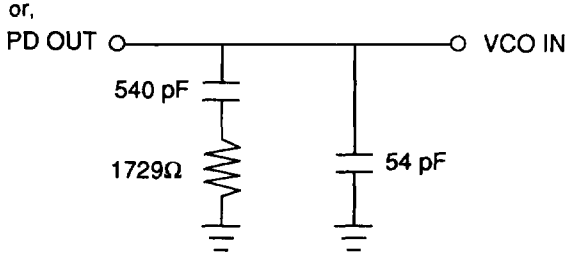
$$KVCO(typ) = \frac{0.20(2\pi)}{2To} = 2.83x10^7$$

$N = 0.33$

which results in:

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} = 1729\Omega \qquad C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 540pF \qquad C_2 = \frac{C_1}{10} = 54pF$$

or,



This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends on the system requirements and can certainly be optimized for a specific application. In the following table we have listed some suggested external component values for two common data rates:

DATA RATE (Mbit/s)	DAMPING FACTOR, ζ	LOCK TIME tmax (μs)	ωnt	BANDWIDTH $\omega n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES			
					RR(kΩ)	R(Ω)	C_1(pF)	C_2(pF)
10	0.7	3.2	3.2	1.0×10^6	6.96	2957	470	47
15	0.7	2.1	3.2	1.5×10^6	3.87	1729	540	54

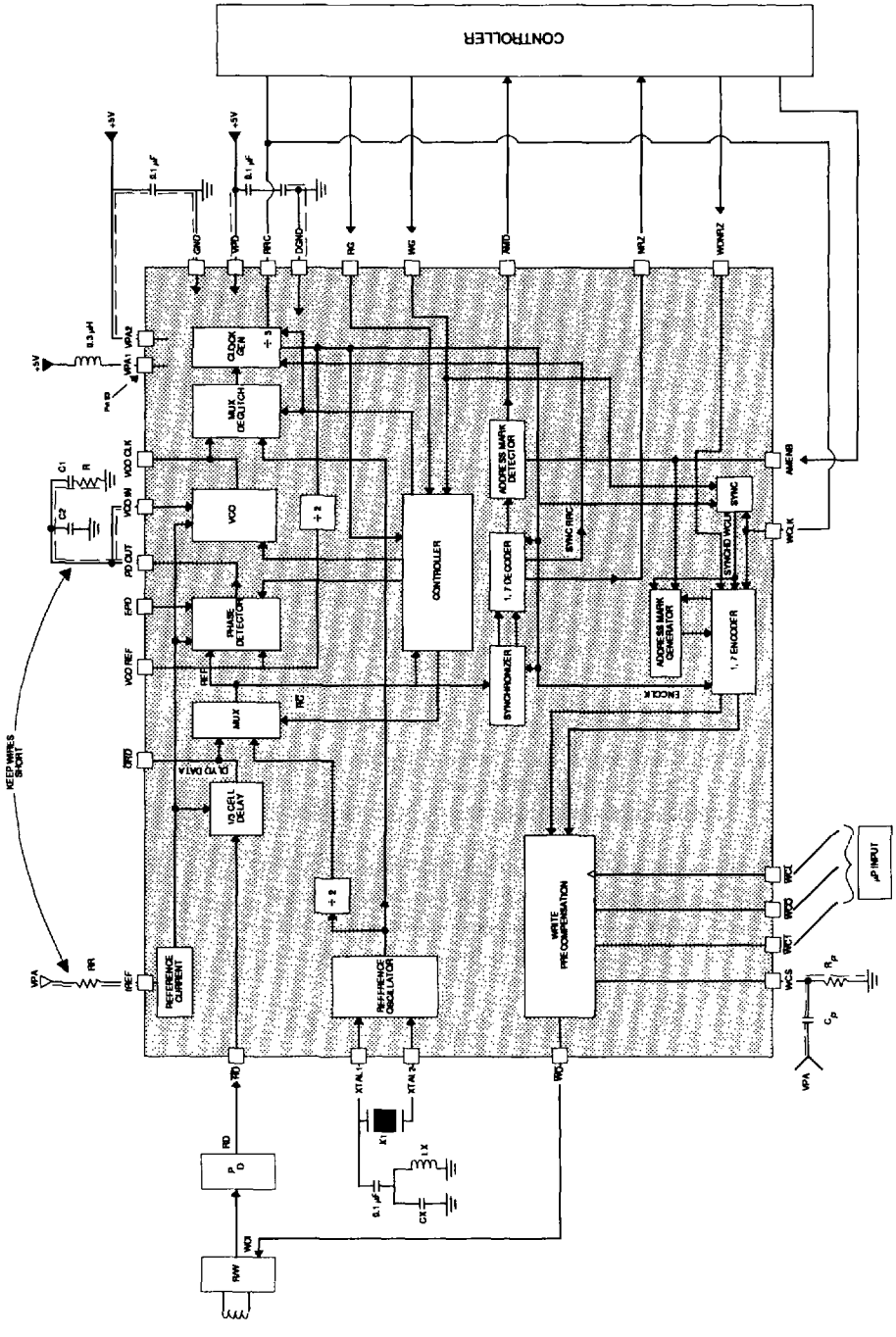
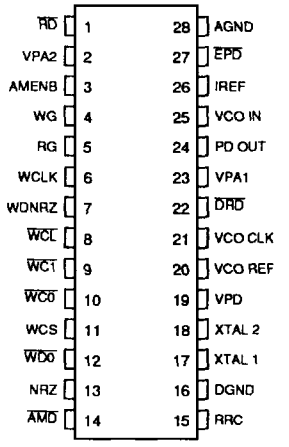
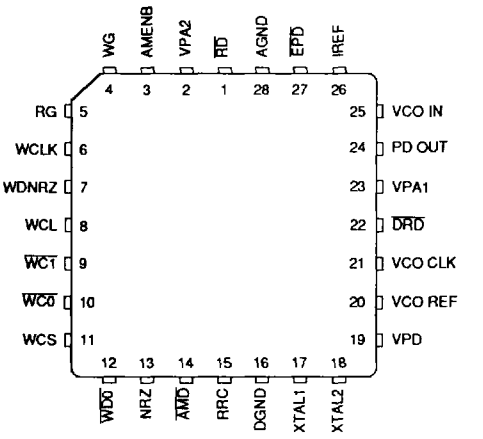


FIGURE 5: Typical Application



28-Pin DIP



28-Pin PLCC

LAYOUT CONSIDERATIONS

As with other high frequency devices the SSI 32D5362 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D5362 and associated circuitry, from other circuits on the PCB. It is also recommended that an inductor (0.3 µH) be placed in series with the analog supply which supports the VCO circuitry (VPA1, Pin 23). This additional filtering has been shown effective in eliminating VCO jitter, which can degrade window margin performance.

TEST POINTS

The SSI 32D5362 provides three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position
(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder
(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

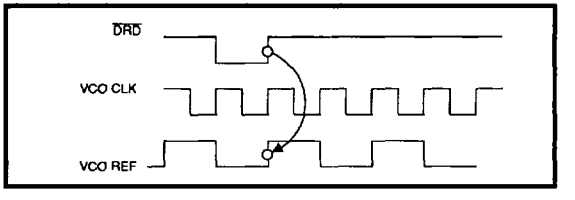


FIGURE 6: Test Point Relationships

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