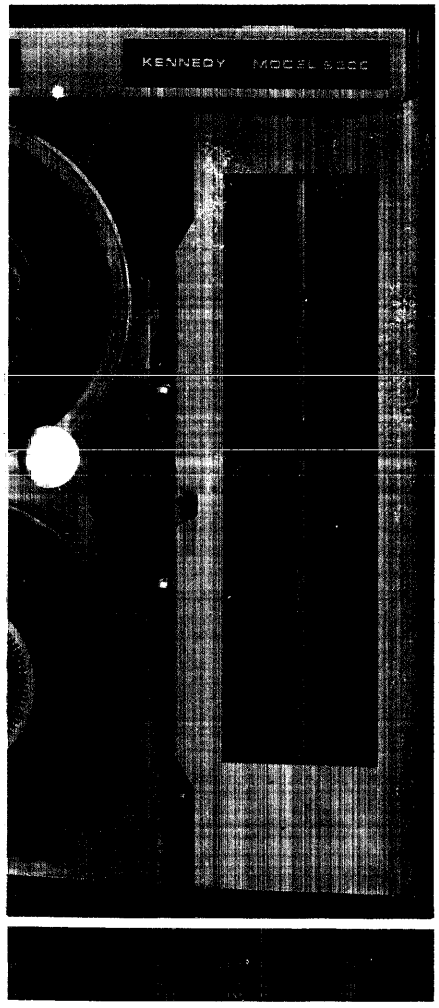
Operation and Maintenance Manual

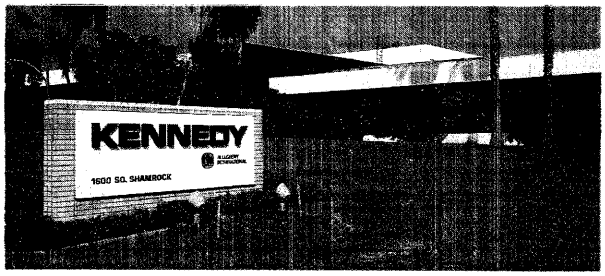
KENNEDY

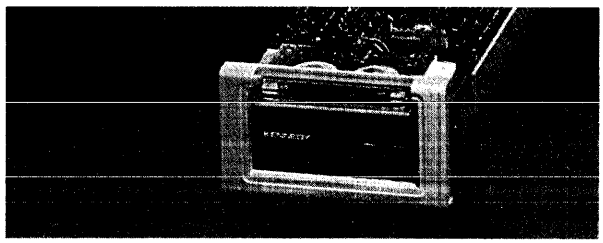
ALLEGHENY INTERNATIONAL

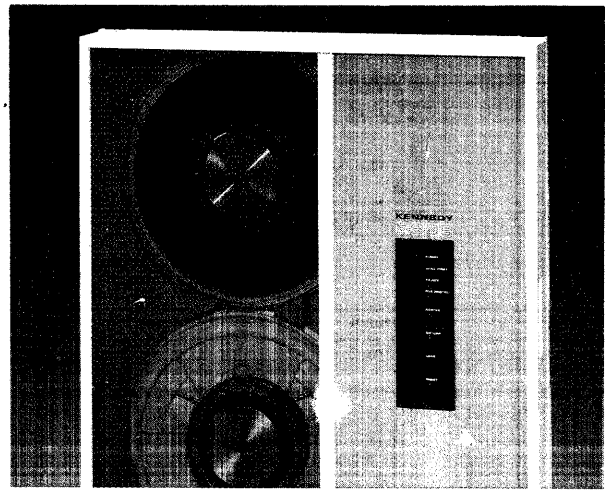
Model 9220

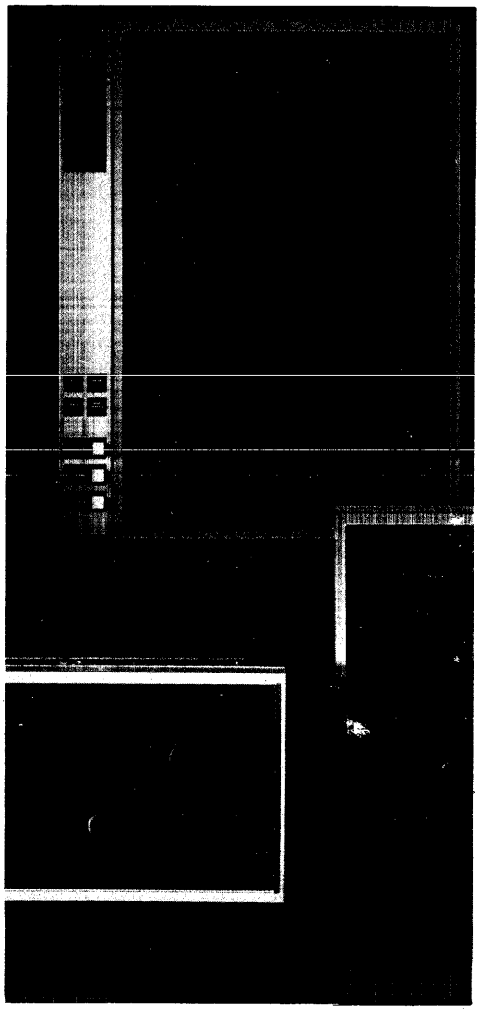
Embedded Formatter

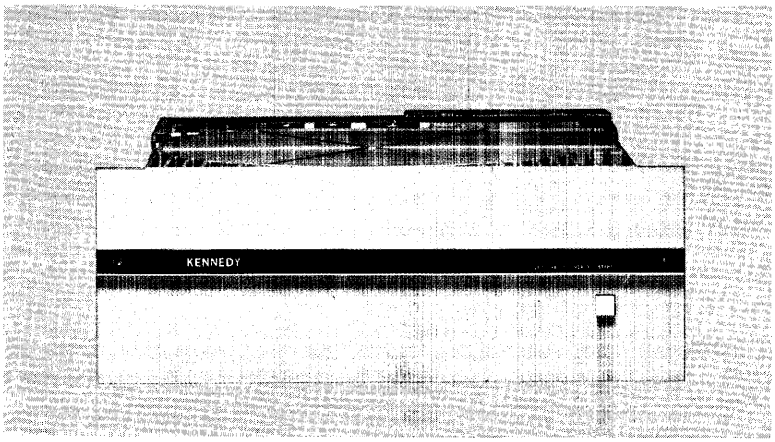


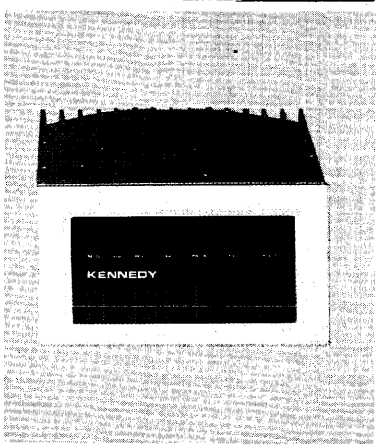












FCC CERTIFIED COMPUTER EQUIPMENT

Warning: This equipment generates and uses radio frequency energy and if not installed and used in accordance with the instruction manual may cause harmful interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

1.0 INTRODUCTION

These application notes are provided for the user or system designer and contain information necessary to interface and install the Kennedy 9X00F tape subsystems. Figures 1-1 through 1-5 illustrate the outline and installation drawings of the 9000 Series with the mounted 9220 formatter.

1.1 GENERAL DESCRIPTION

There are five models in the Kennedy tape subsystem line: Models 9000F, 9800F, 9700F, 9100F and 9300F. Seven tape speeds are available from 12.5 ips to 125 ips. Refer to the configuration table and operational specifications given in section 2 for reel size and tape speeds available for each model.

The Kennedy 9X00F consists of a digital synchronous tape transport and embedded formatting control electronics. The control electronics meet all requirements for reading and writing ANSI/IBM compatible 800 cpi NRZI and 1600 cpi PE formats.

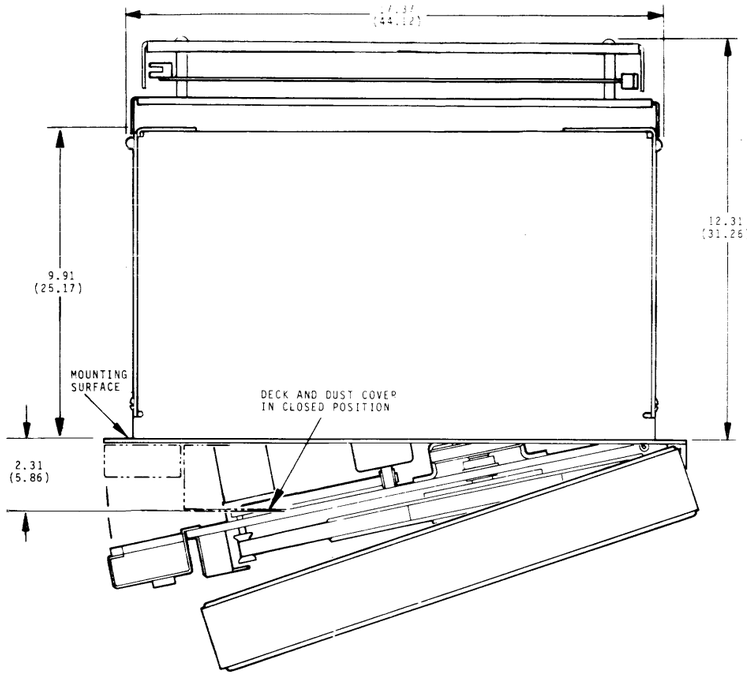
1.2 STANDARD FEATURES

1. Industry compatible formatter interface
2. Signature analysis formatter design
3. Offline customer engineering test panel
4. Marginal skew check
5. Read-after-write shortened skew gate
6. Crystal controlled timing
7. LED indicators
8. Switch selectable addressing
9. Quick release hubs
10. Modular transport design
11. Simplified tape loading
12. Variable capacitance tape location detector (Models 9100F/9300F only)

1.3 RELATED DOCUMENTS

1. ANSI X3.22 Recorded Magnetic Tape for information interchange (800 cpi, NRZI)
2. ANSI X3.39 Recorded Magnetic Tape for information interchange (1600 cpi, PE)
3. ANSI X3.40 Unrecorded Magnetic Tape for information interchange (800 cpi, NRZI and 1600 cpi, PE)
4. Embedded Formatter Product Specification PN 102-0022-001
5. Model 9X00F Operation and Maintenance Manual
6. Model 9000 Product Specification PN 102-0025-001
7. Model 9000 Operation and Maintenance Manual PN 193-9000-000
8. Model 9700 Product Specification PN 102-0026-001
9. Model 9700 Operation and Maintenance Manual PN 193-9701-000
10. Model 9800 Product Specification PN 102-0027-001
11. Model 9800 Operation and Maintenance Manual PN 193-9801-000
12. Model 9100 Product Specification PN 102-0019-001
13. Model 9100 Operation and Maintenance Manual PN 193-9100-000
14. Model 9300 Product Specification PN 102-0020-001
15. Model 9300 Operation and Maintenance Manual PN 193-9300-000

106-9000-001A



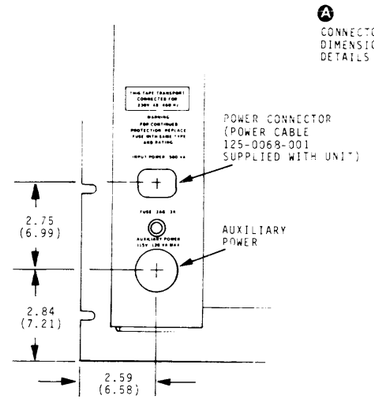
DUST COVER OPENS TO APPROX 120° FOR ACCESS TO TAPE REELS

WARNING

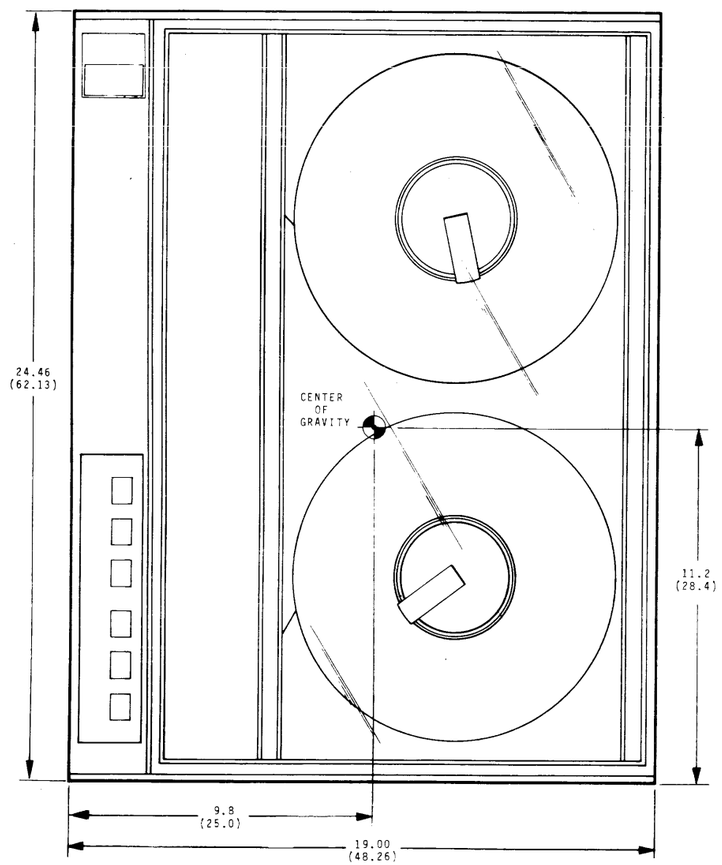
DUST COVER MUST BE FULLY OPENED BEFORE OPENING DECK ASSEMBLY

DECK ASSEMBLY OPENS TO APPROX 90° FOR ACCESS TO TRANSPORT & ELECTRONICS

Ⓐ CONNECTOR LOCATION DIMENSIONS (TYPICAL) DETAILS FOR 230V OPERATION

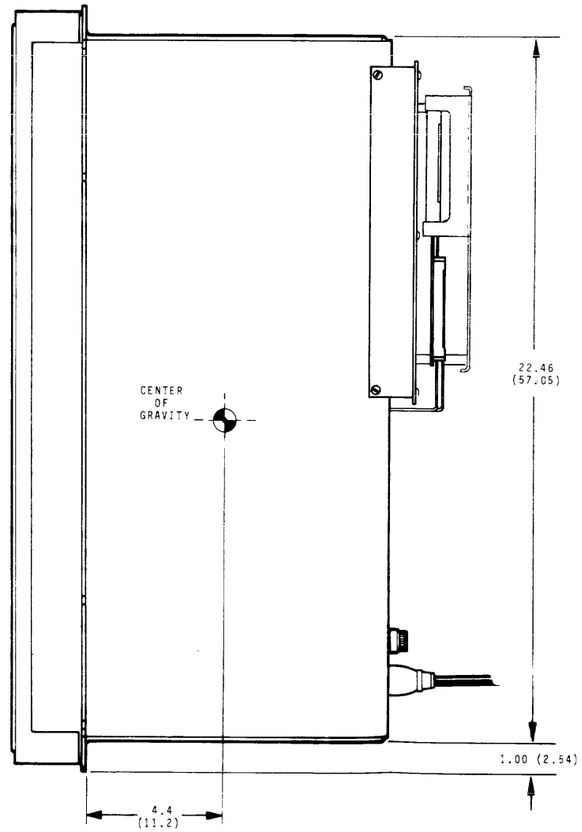


FIRST DIMENSIONS SHOWN ARE IN INCHES.
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS
UNLESS OTHERWISE SPECIFIED
DIMENSIONS SHOWN ARE NOMINAL.

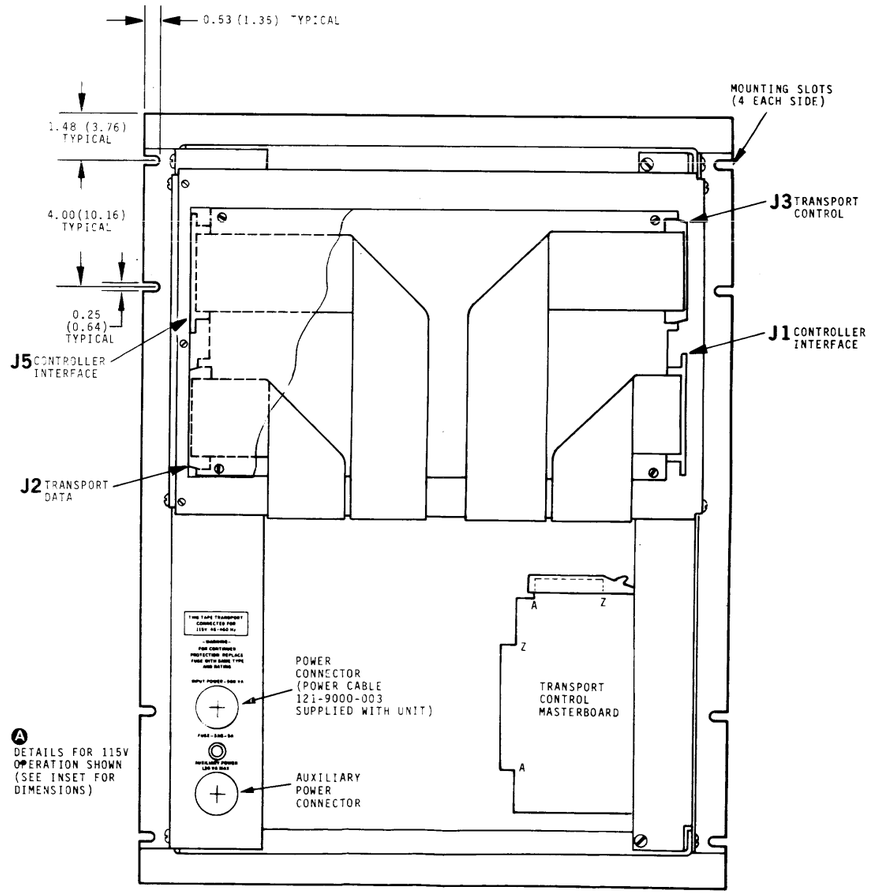


410-4042

Front View



Side View

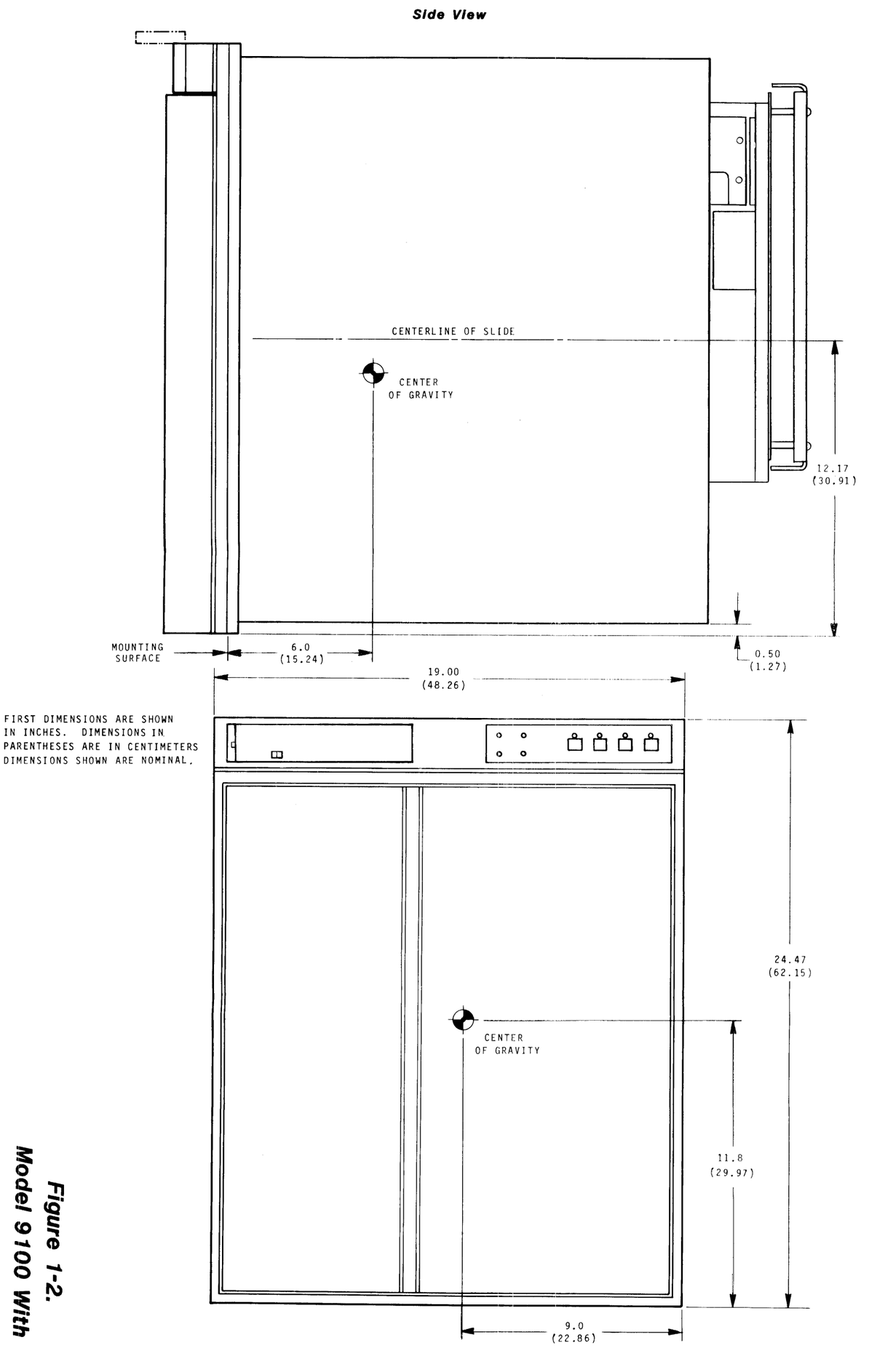


Ⓐ DETAILS FOR 115V OPERATION SHOWN (SEE INSET FOR DIMENSIONS)

Rear View

Figure 1-1. Model 9000 With Mounted 9220 Formatter

310-3040



106-9100-001A

Figure 1-2. Model 9100 With Mounted 9220 Formatter

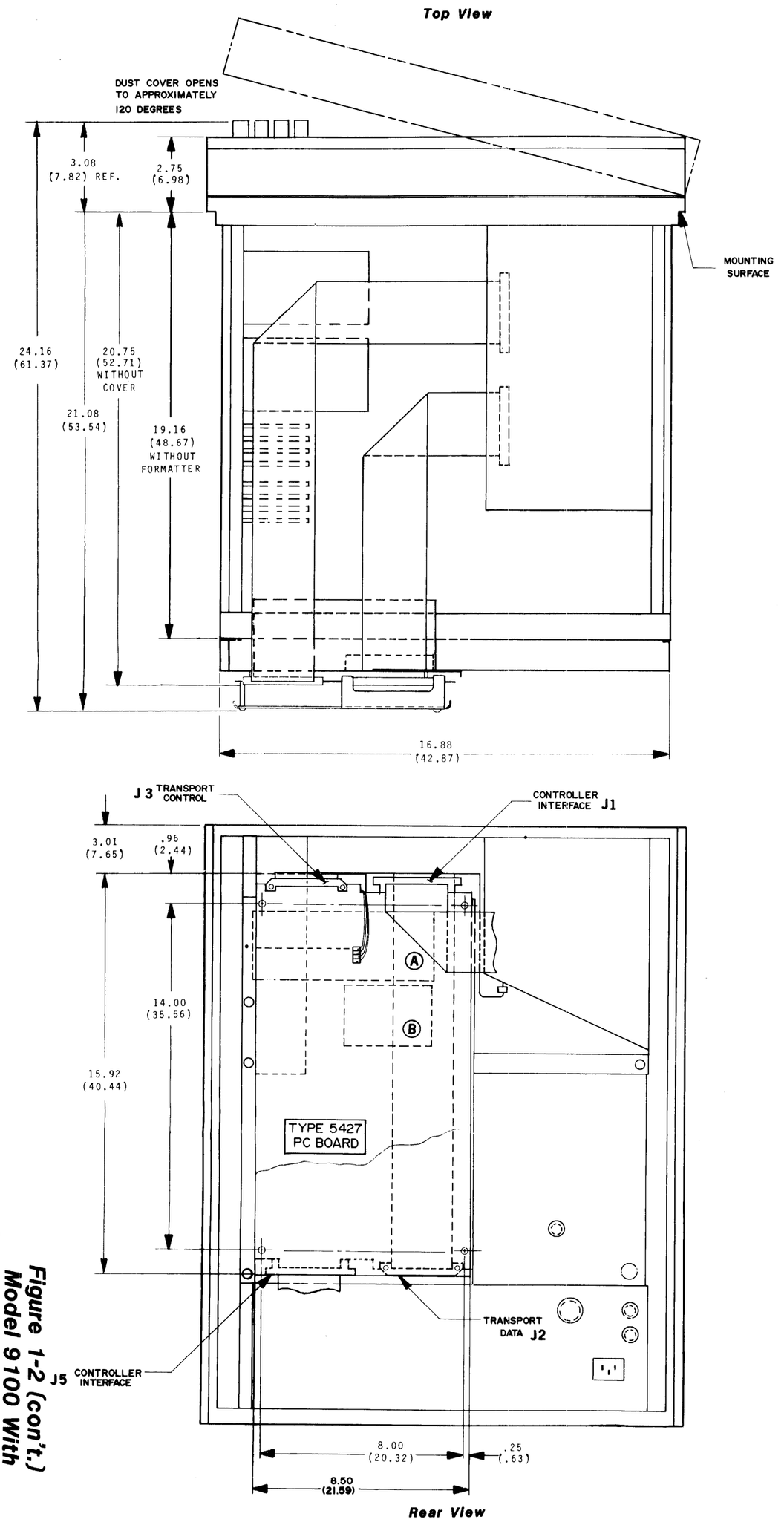


Figure 1-2 (con't.)
Model 9100 With
Mounted 9220 Formatter

106-9100-002A

310-3041

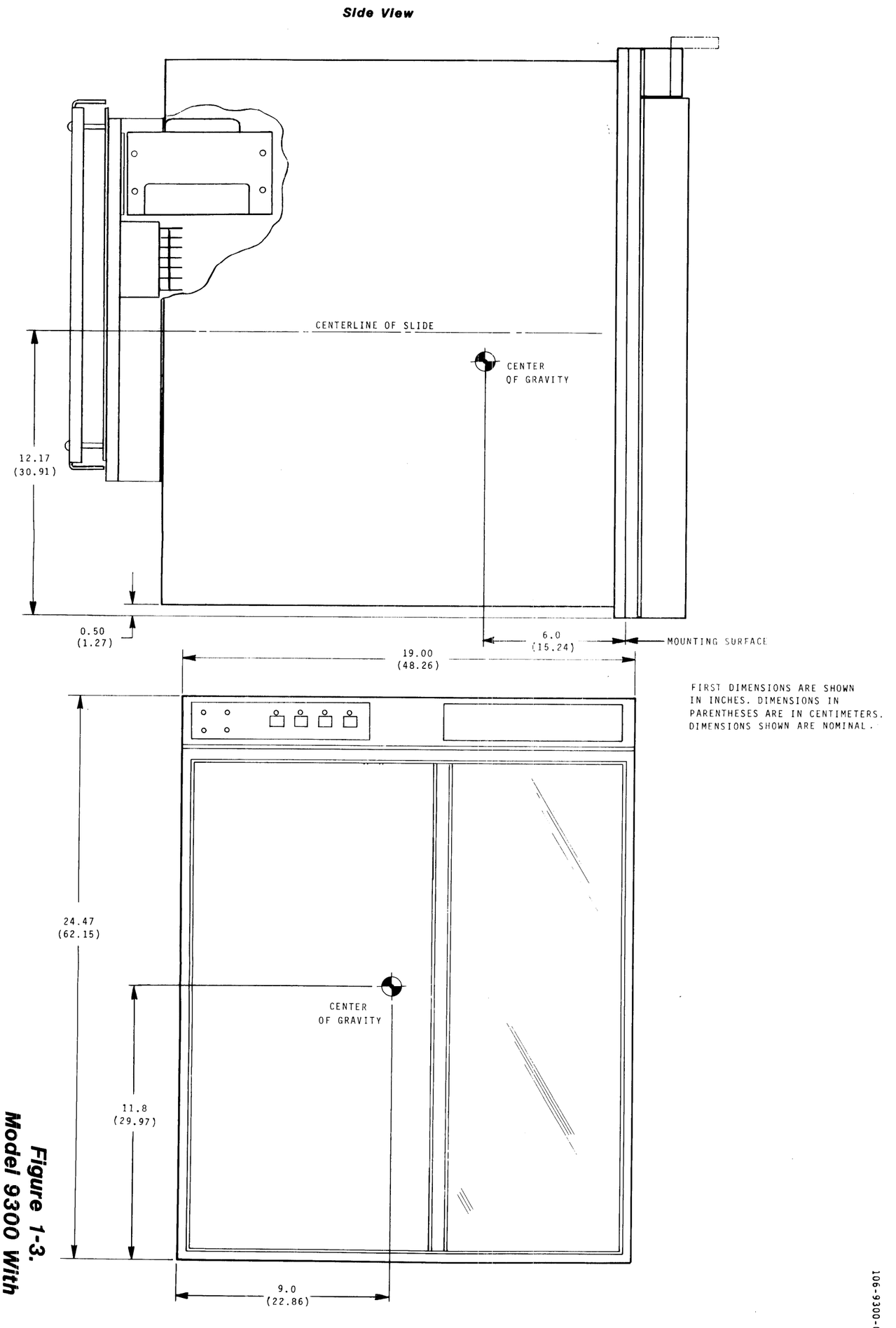


Figure 1-3. Model 9300 With Mounted 9220 Formatter

Figure 1-2. Model 9300 with Mounted 9220 Formatter

106-9300-001A

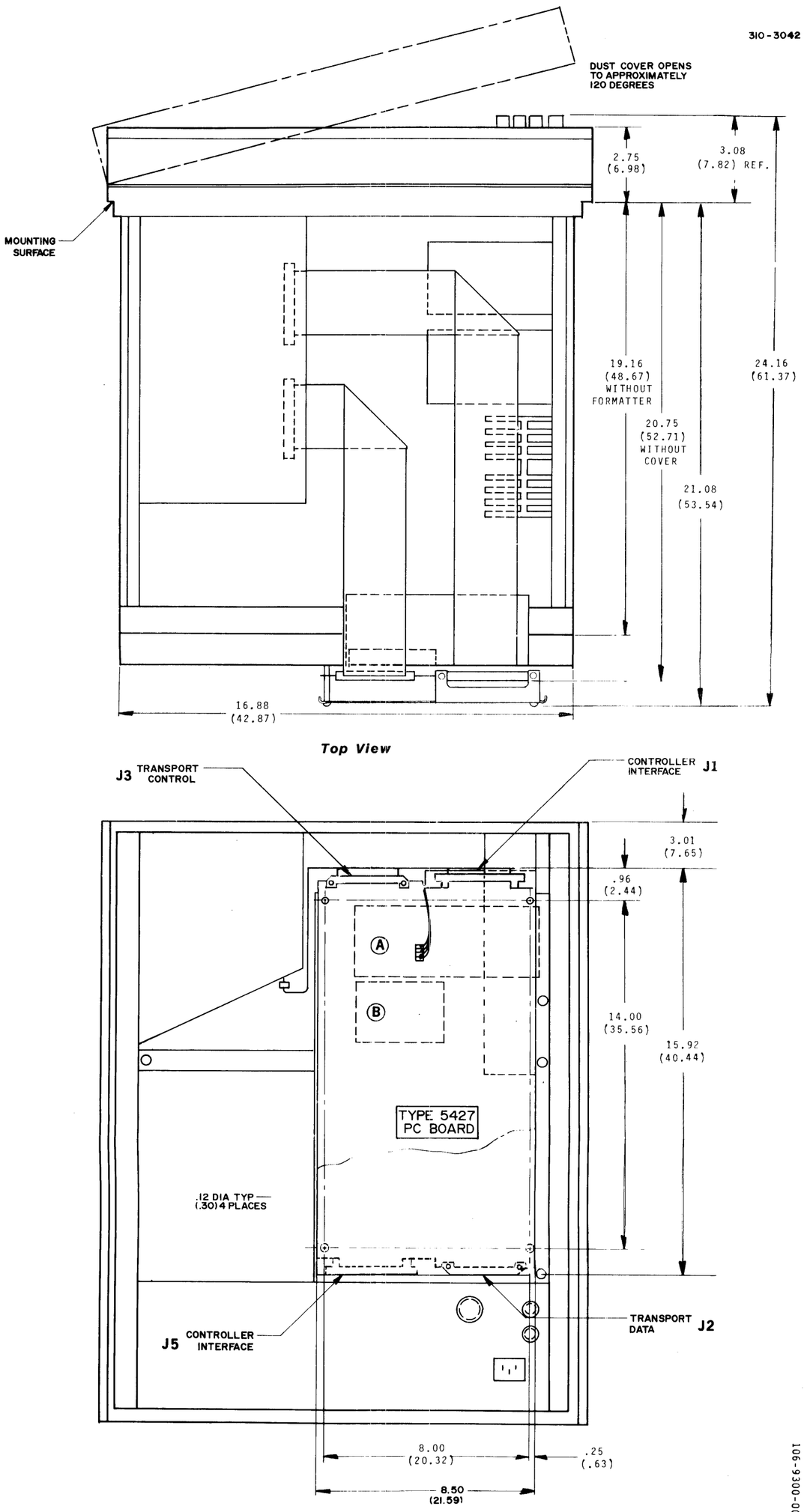


Figure 1-3 (con't.)
Model 9300 With
Mounted 9220 Formatter

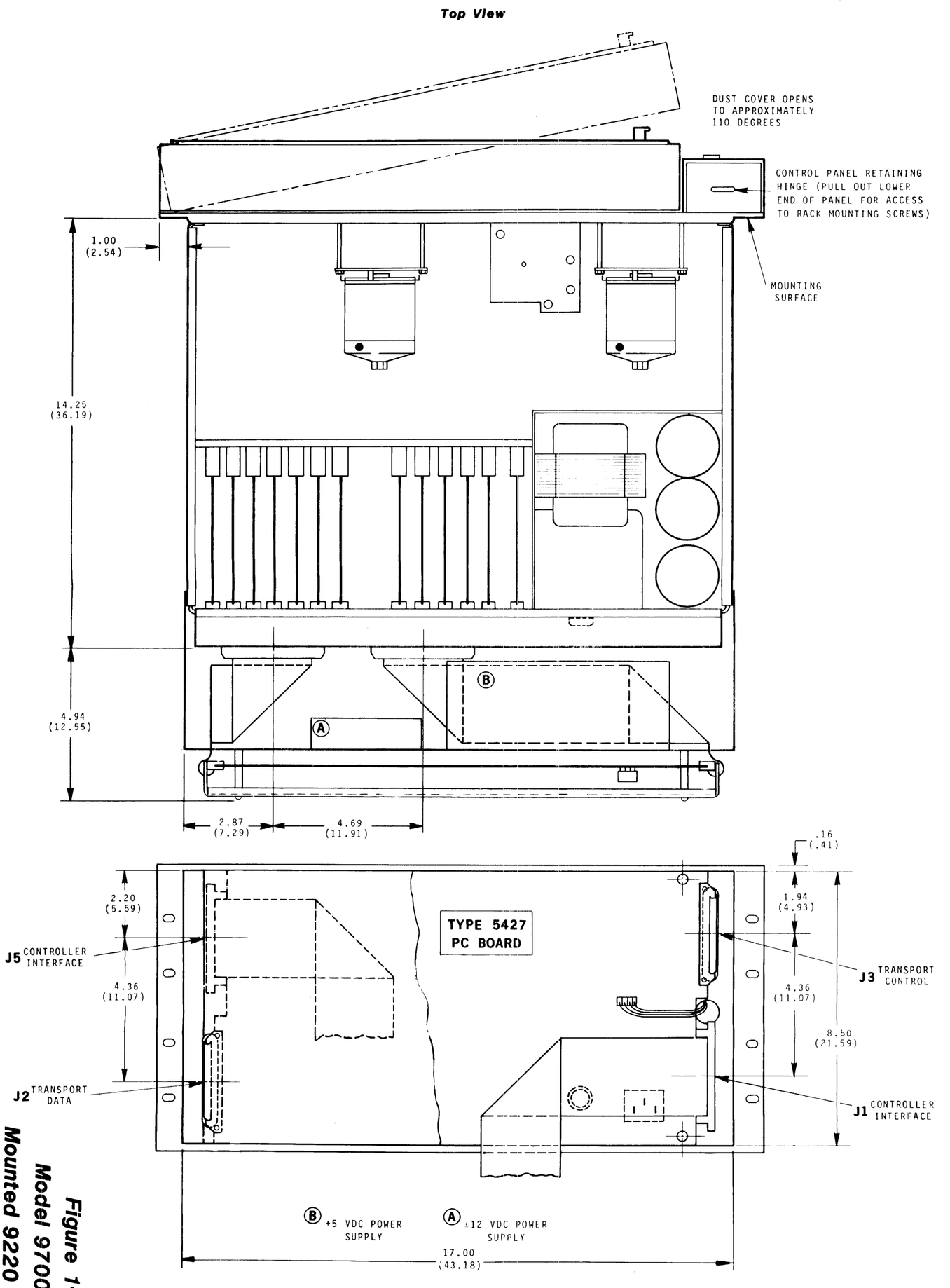


Figure 1-4.
Model 9700 With Mounted 9220 Formatter

106-9700-001A

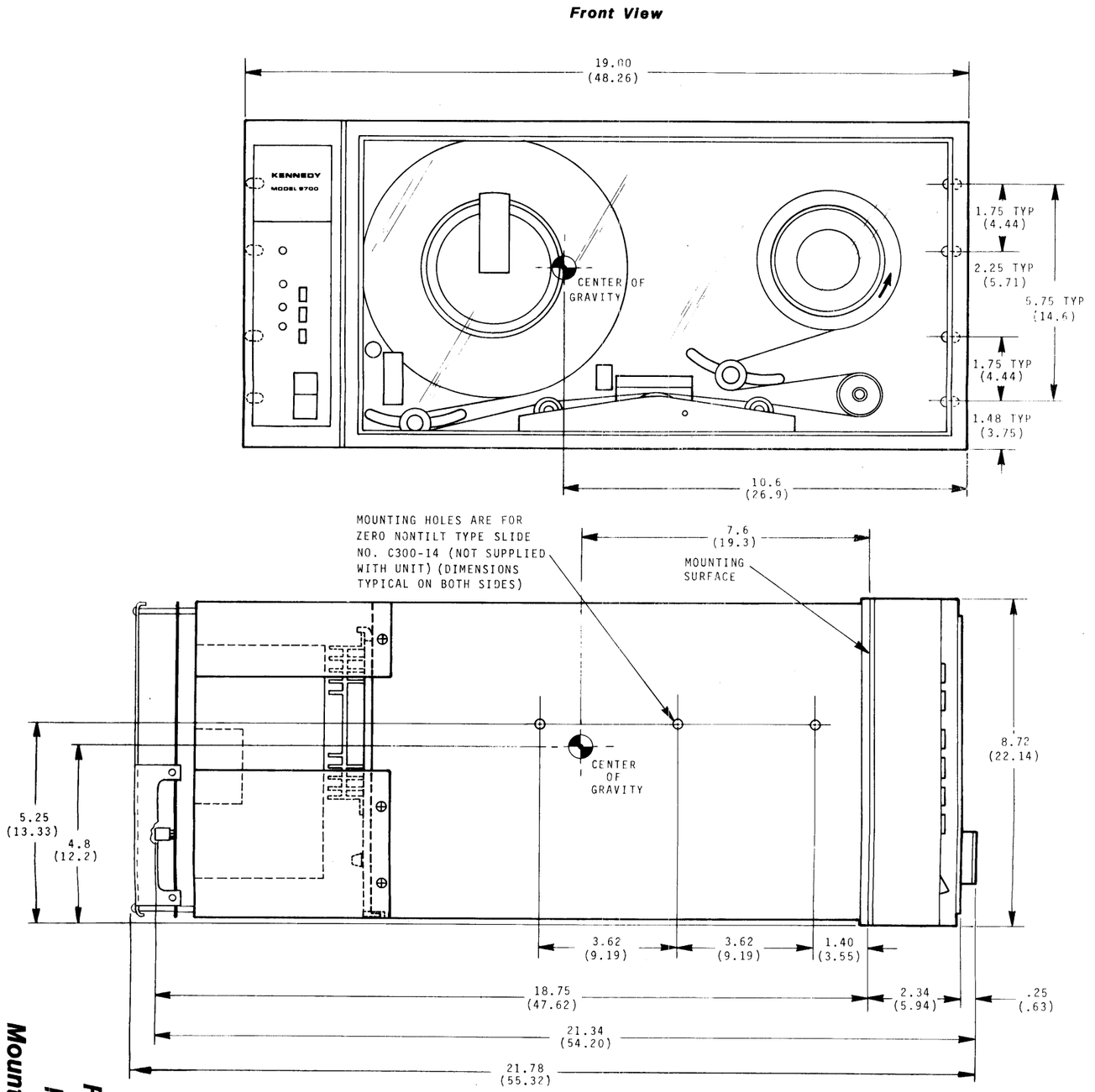


Figure 1-4 (con't.)
Model 9700 With
Mounted 9220 Formatter

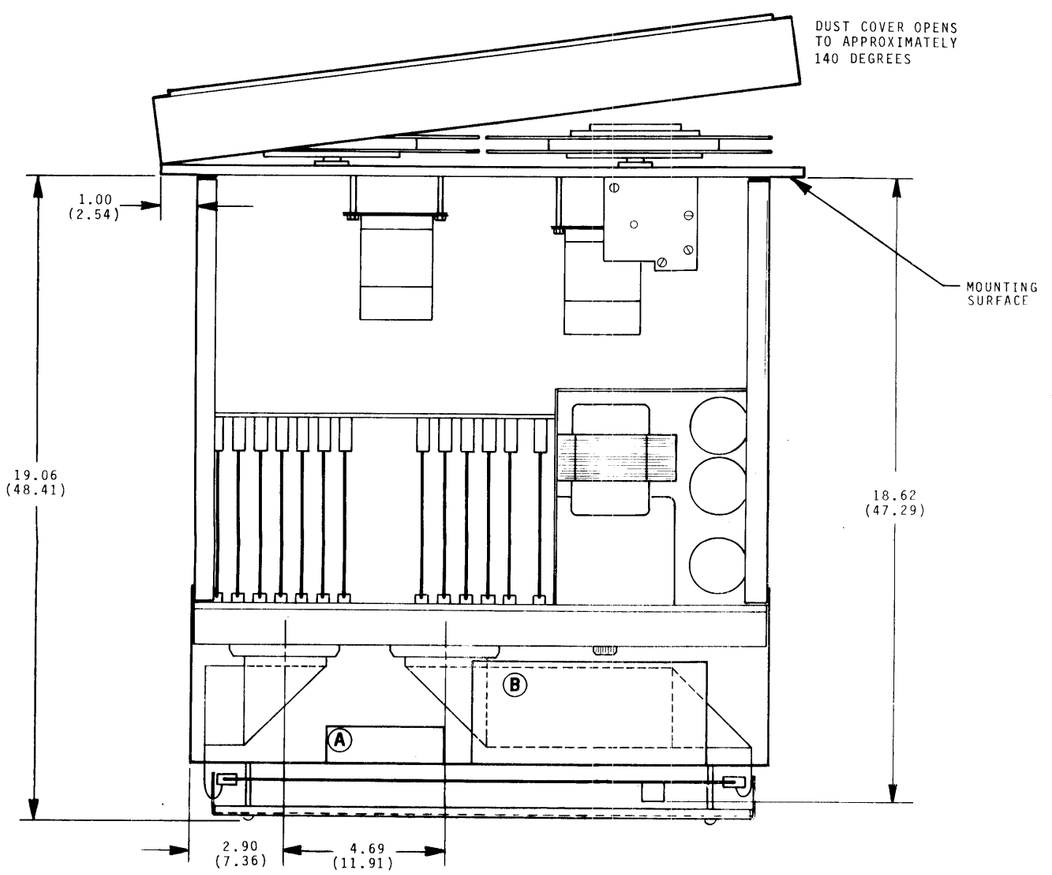
310-3060

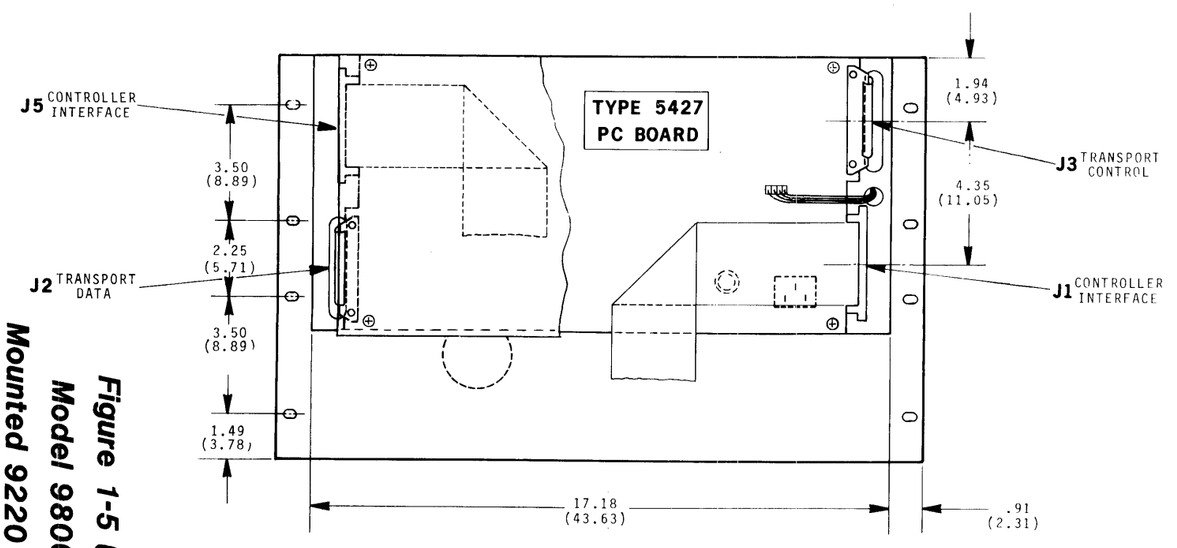
106-9700-002A

106-9800-001A

Figure 1-5.
Model 9800 With
Mounted 9220 Formatter

Top View





Rear View

Ⓑ +5 VDC POWER SUPPLY

Ⓐ ±12 VDC POWER SUPPLY

310-3061

106-9800-002A

Figure 1-5 (con't.)
Model 9800 With
Mounted 9220 Formatter

2.0 SPECIFICATIONS

Although all Kennedy tape subsystems feature a common electrical interface, the various models are uniquely packaged. This section provides mechanical and electrical information to interface 9X00F series Kennedy subsystems with any computer system.

2.1 MECHANICAL SPECIFICATION

Tables 2-1 and 2-2 are summaries of operational specifications for Kennedy tape subsystems. When integrating into a system, it should be noted that the units utilize convection cooling as the sole means of heat dissipation (except Model 9300) and that heat sinks are oriented for vertical transport mounting. A fan is provided in Model 9300 for heat dissipation. The operating range of the units is consistent with normal environments; however, care must be taken when enclosing the units to provide adequate air flow to assure that operating temperature limits will not be exceeded.

In the case of horizontally mounted units, it is suggested that forced air cooling be utilized.

All necessary mounting and interfacing hardware are provided as an installation kit with each unit. Figures 2-1 through 2-5 provide details for rack mounting and installing the various units.

2.2 OPERATIONAL SPECIFICATION (MODELS 9100F/9300F)

Model	9100	9300
Data Density	9 track 800 cpi, 1600 cpi, 800/1600 cpi	Same
Number of Tracks	9 Read-after-Write	Same
Format	NRZI/PE IBM Compatible	Same
Tape Velocity	75 ips	125 ips
Instantaneous Speed Variation	+/-3%	Same
Long Term Speed Variation	+/-1%	Same
Interchannel Displacement Error	150m inches max 800 cpi 200m inches max 556 cpi	Same
Start/Stop Time	5 ms +/-0.5 ms at 75 ips Inversely proportional to tape speed	3 ms +/-0.3 ms at 125 ips
Start/Stop Displacement	0.1875 +/-0.0125 inch	Same
Gaps	Internally Timed	Same
Parity (VRC) CRC/LRC	Internally or Externally Generated Internally Generated	Same
Tape Tension	8.0 oz	Same
Reel Size	10.5 inch 2400 feet, 1.5 mil 0.5 inch wide tape	Same
Drive System	Single Capstan 180^{o} wrap	Same
Tape Buffer Tape Detection	Vacuum Column Capacitive	Same
Rewind Speed	200 ips nominal	300 ips nominal
Electronics	TTL	Same

Model	**9100**	**9300**
Subsystem Interface	TTL Industry Compatible low true	Same
Physical Dimensions	**9100**	**9300**
Mounting	Standard EIA rack	Same
Weight	155 lb	170 lb
Power	115 vac +/-10% 48-60 Hz 750 watts maximum	Same
Operating Temperature	$+2^{\circ}$ to $50^{\circ}C$	Same
Altitude	0 to 4000 feet	Same
Humidity	15 to 95% noncondensing	Same
Options Available	High altitude kit, special paint, 230 vac	Same

Table 2-1
Operational Specification, Models 9100F/9300F

2.3 OPERATIONAL SPECIFICATION (MODELS 9000F/9800F/9700F)

Model	9000	9800	9700
Data Density	9 track, 800 cpi, 1600 cpi, 800/1600 cpi	9 track, 800 cpi, 1600 cpi, 800/1600 cpi	9 track 800 cpi, 1600 cpi, 800/1600 cpi
Number of Tracks	9 Read-after-Write	9 Read-after-Write	9 Read-after-Write
Format	NRZI/PE IBM Compatible	NRZI/PE IBM Compatible	NRZI/PE IBM Compatible
Tape Velocity	10-45 ips	10-37.5 ips	10-37.5 ips
Instantaneous Speed Variation	+/-3%	+/-3%	+/-3%
Long Term Speed Variation	+/-1%	+/-1%	+/-1%
Interchannel Displacement Error	150m in., max 800 cpi 200m in., max 556 cpi	150m in., max 800 cpi 200m in., max 556 cpi	150m in, max 800 cpi 200m in., max 556 cpi
Read Data	NRZI 9 output levels with Read Strobe PE 9 output levels with Read Strobe	NRZI 9 output levels with Read Strobe PE 9 output levels with Read Strobe	NRZI 9 output levels with Read Strobe PE 9 output levels with Read Strobe
Start/Stop Time	15 ms +/-1 ms at 125 ips inversely proportional to tape speed	15 ms +/-1 ms at 125 ips inversely proportional to tape speed	15 ms +/-1 ms at 125 ips inversely proportional to tape speed
Start/Stop Displacement	0.1875 +/-0.0125"	0.1875 +/-0.0125"	0.1875 +/-0.0125"
Gaps	Internally timed	Internally timed	Internally timed
Parity (VRC) CRC/LRC	Internally or externally generated Internally generated	Internally or externally generated Internally generated	Internally or externally generated Internally generated
Tape Tension	8.0 (+/-0.5) oz	8.0 (+/-0.5) oz	8.0 (+/-0.5) oz
Reel Size	10.5", 2400 ft 1.5 mil 0.5" wide tape	8.5 ", 1200 ft 1.5 mil 0.5" wide tape	7", 600 ft 1.5 mil 0.5" wide tape

Model	9000	9800	9700
Drive System	Single Capstan 180 wrap	Single Capstan 180 wrap	Single Capstan 180 wrap
Servo Buffer Arm Positioning	Electromagnetic	Electromagnetic	Electromagnetic
Rewind Speed	150 ips nominal	120 ips nominal	120 ips nominal
Electronics	TTL	TTL	TTL
Subsystem Interface	TTL Industry Compatible low true	TTL Industry Compatible low true	TTL Industry Compatible low true
Physical Dimensions	**9000**	**9800**	**9700**
Mounting	Standard EIA rack	Standard EIA rack	Standard EIA rack
Weight	90 lb	45 lb	35 lb
Power	115 vac +/-10% 48-400 Hz UL approved	115/230 vac +/-10% 48-500 Hz	115/230 vac +/-10% 48-500 Hz
Operating Temperature	+2° to 50°C	+2° to 50°C	+2° to 50°C
Altitude	0 to 30,000 feet	0 to 30,000 feet	0 to 30,000 feet
Humidity	15 to 95% noncondensing	15 to 95% noncondensing	15 to 95% noncondensing
Options	37.5, 45 ips switch selectable addressing special paint, 230 vac	25, 37.5 ips special paint	25, 37.5 ips special paint

Table 2-2
Operational Specification, Models 9000F/9800F/9700F

3.1 CONTROLS AND INDICATORS

An illustration of controls and indicators on the series 9X00 transports is shown in figure 3-1. These local controls and indicators are utilized to prepare the transports for operation and to monitor key functions. They are described only to provide greater familiarization with the units.

3.1.1 POWER

On Models 9100 and 9300, there is a momentary pushbutton switch/indicator which connects line voltage to the power transformer. Models 9000, 9700 and 9800 utilize a power switch only. When power is on: all power supplies are established; all motors are open-circuited (low value resistors are connected across the reel motors), and a reset signal is applied to key control flip-flops.

3.1.2 LOAD

The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. Tape runs forward at normal speed to the reflective foil load point marker, then stops. The indicator is illuminated when the reel servos are activated and tape is tensioned.

3.1.3 ONLINE

A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an online condition; when the tape unit is online it can be remotely selected and will be ready if tape is loaded to or past the load point tape marker. When activated again it takes the tape unit offline. The indicator is illuminated in the online condition.

3.1.4 REWIND

This momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is offline. The indicator is illuminated during either a local or remote rewind operation.

Enabling this control causes tape to rewind at the specified speed. On reaching the load point marker, the rewind operation ceases and the load sequence is automatically entered, positioning the tape approximately 0.19 inch beyond the load point marker.

If the REWIND control is depressed and released when tape is at load point (LOAD indicator illuminated), tape rewinds off the takeup reel and tension is lost.

LOAD and REWIND pushbuttons are disabled when the tape unit is online.

3.1.5 READ

Illuminates when tape unit is online, selected and read selected. (This indicator is not available on Model 9700.)

3.1.6 WRITE

Illuminates when tape unit is online, selected and write status selected. Write enable signal must also be true, indicating a tape with a write enable ring mounted on the transport.

3.1.7 SELECT

Illuminates when tape unit is online and selected.

3.1.8 WRITE ENABLE

Write enable is an indicator which is illuminated whenever power is ON and a reel of tape with a write enable ring installed is mounted on the transport.

3.1.9 UNIT SELECT SWITCH

This rotary selector switch is utilized in applications requiring addressing one of several transports. Activating the SLT line corresponding to the address (0-3 or 1-4) selected causes the transport to be selected. This feature is optional on Models 9000, 9700 and 9800, but is standard on Models 9100/9300.

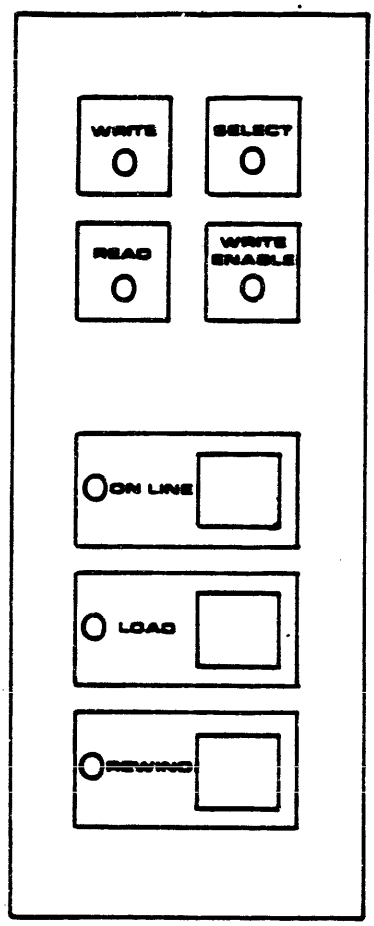
3.2 TEST PANEL

Models 9000, 9100 and 9300 contain test panels which provide a means of exercising, testing and adjusting the tape transport while it is offline, eliminating the need for a separate test fixture or for the use of valuable computer time. (Test panels are optional in models 9700 and 9800.) The test panel can initiate forward and reverse tape motions at either normal or high tape speeds. It can also initiate a write test, generating a crystal controlled all-1s test pattern on tape. The test panel also provides indicators for load point, end of tape and data available. An additional indicator monitors excessive skew and is used to align the read/write head in conjunction with an 800 cpi skewmaster tape. When the head is properly aligned and the data is written on tape properly the SKEW indicator is extinguished.

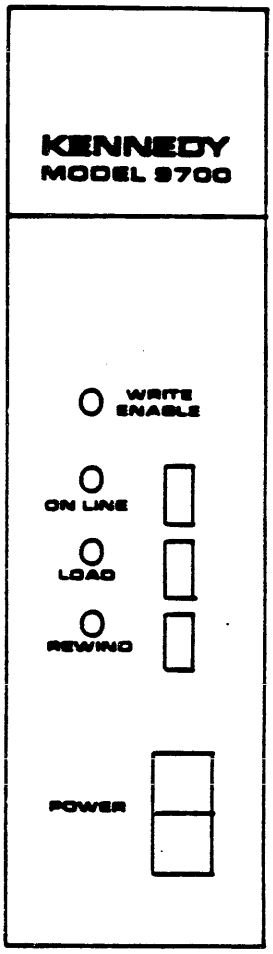
The controls and interlocks for the test panel are located on the Pushbutton Control card. The skew detect network is located on the Delay Timing module in the read logic section of the transport. The test panel becomes operational only when the transport is offline with the test panel STOP pushbutton depressed. If these conditions are satisfied the test panel pushbuttons are enabled when the TEST MODE pushbutton is pressed.

Figure 3-2 illustrates the test panel of various transports.

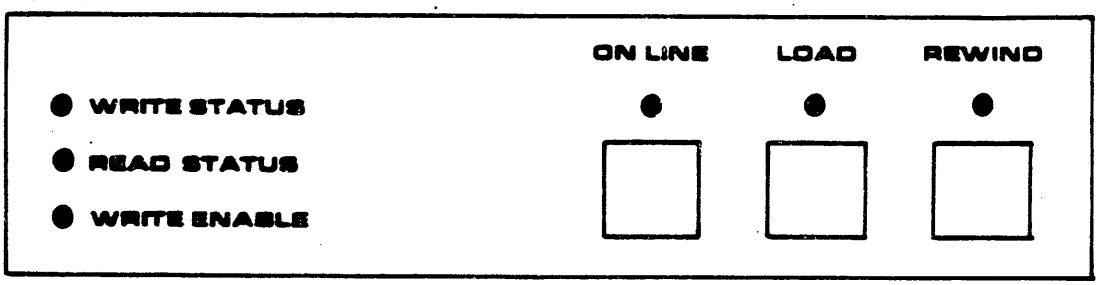
Model 9000



Model 9700



Model 9800



Models 9100; 9300

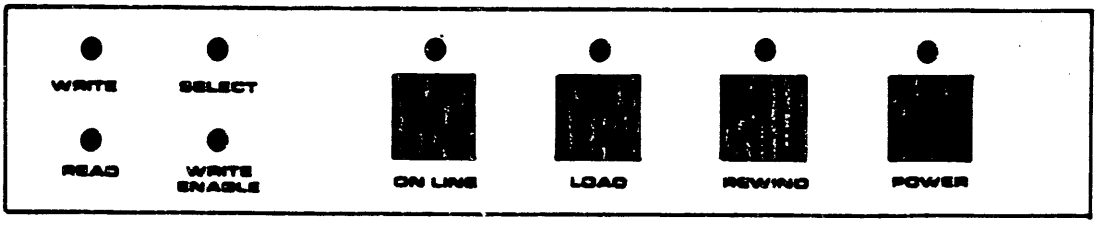


Figure 3-1. Control Panel Controls and Indicators

3.2.1 TEST POINT AND SKEW INDICATOR

Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope test point is available for monitoring skew gate timing.

3.2.2 HDS

Indicates that high density mode has been selected. Replaces data LED used with single density units.

3.2.3 EOT

Indicates that tape has reached or passed the reflective end of tape marker.

3.2.4 LOAD POINT

Indicates that tape is at load point.

3.2.5 CYCLE (9100/9300 TRANSPORTS ONLY)

An interlocked pushbutton which runs tape in alternating forward and reverse modes. Useful for making ramp or vacuum sensor adjustments. Depressing STOP pushbutton terminates this operation.

3.2.6 FAST FORWARD

An interlocked pushbutton switch that allows tape unit to run forward at fast speed. Depressing STOP pushbutton or advancing tape to EOT marker terminates this operation.

3.2.7 REVERSE RUN

An interlocked pushbutton switch that allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or rewinding tape to load point marker terminates this operation.

3.2.8 FORWARD RUN

An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or advancing tape to EOT marker terminates this operation.

3.2.9 STOP

An interlocked pushbutton switch that terminates tape motion.

3.2.10 WRITE TEST

A momentary pushbutton which programs 1s to be written on all channels to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator remains illuminated while unit is in this mode.

3.2.11 TEST MODE

This momentary pushbutton selects test mode and activates test panel. When indicator is illuminated, test panel is active. (Tape unit must be offline and STOP pushbutton depressed before test panel will function.)

3.2.12 FAST REVERSE (9700/9800/9000 ONLY)

An interlocked pushbutton switch that allows tape unit to run in reverse at specified speed. Depressing STOP pushbutton or rewinding tape to BOT marker will terminate this operation.

3.2.13 DATA

Indicates when data is being processed by read/write electronics.

3.3 OPTIONS

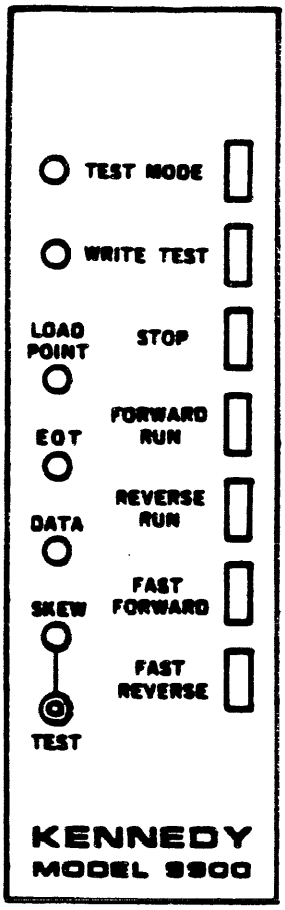
When incorporated in series 9X00 tape transports the type 4843 pushbutton control module allows use of several factory installed optional features. These functions are determined by optional straps and use of components.

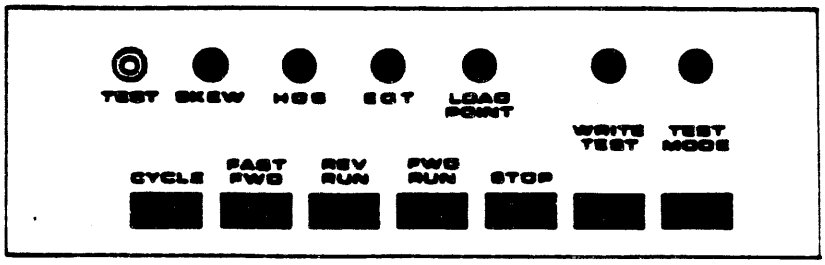
3.3.1 AUTO POWER RESTART

With the standard APR option, this circuitry continually monitors the line voltage and whether the tape unit is online or offline. If the external voltage falls below the minimum value required by the tape unit, this option will force the unit into an offline state and issue a BROKEN TAPE command. When the input power level returns to an acceptable value, the APR circuitry will do one of two things, depending on whether the deck was online before the power failure: (1) nothing, if the unit was in an offline state, or (2) load, advance tape several inches and place the unit online if it was previously in an online state.

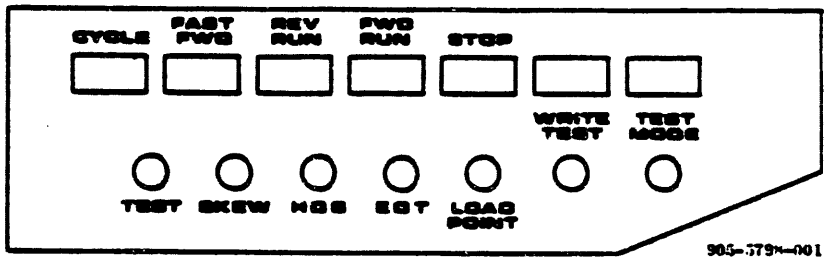
3.3.2 ON TAPE (OT)

With this option the tape unit cannot be placed online until a reel of tape is loaded and positioned at or past the BOT tab.





Model 9100



Model 9300

Model 9000; Model 9900 Test Box

Figure 3-2
Test Panel Controls and Indicators

4.0 INTERFACE DESCRIPTION

4.1 INTERFACE SIGNAL CHARACTERISTICS

Signals from the controller to the 9X00F must conform to the following specifications:

Levels: Low = True = 0V
High = False = +3V (approx.)

Pulses: Low = True = 0V
High = False = +3V (approx.)

Minimum Pulse Width: 1.0 microsecond

Total edge transmission delay to be no greater than 200 nanoseconds over 20 foot cable

All output signals from the Model 9X00F are driven by open collector type line drivers capable of sinking up to 36 ma (25 standard unit loads) in the low true state. Open lines will result in false signal levels.

Configuration switches are provided for speed selection. Two speeds may be selected in multidrive phase encoded formatter systems A or B. Any four of seven available NRZI speeds may be selected. Switch settings are given in table 4-5. Component values for the VCO filter are given in table 4-6.

Typical line driver and receiver circuits are shown below in figure 4-1. Twisted pair or ribbon cables with alternate wire ground are required for all inputs and outputs. The maximum recommended length for controller to formatter cables is 20 feet (Pertec compatible). Connector pin assignments and cross reference to 100 pin edge connector are provided in tables 4-1 and 4-3.

Typical write and read interface timing diagrams are shown in figures 5-1 and 5-2. Commands for Model 9X00F are shown in table 4-2.

4.2 INTERFACE INPUT SIGNALS (CONTROLLER TO FORMATTER)

The following paragraphs describe the specifications and functions for each input signal required from the controller to the formatter interface inputs of Model 9X00F. Under the signal name are listed the connector and active pin designation for the input signal line, and the mnemonic designation of the line. An I/O signal list is provided in table 4-1.

FORMATTER ADDRESS
FAD Level B48

A level which selects one of two formatters. FAD false selects formatter address 0; FAD true selects formatter address 1. The formatter addresses are determined by an address switch on the formatter PCBA. Normally, the formatter must be selected in order to perform any formatter operations. FAD is not latched on go pulse.

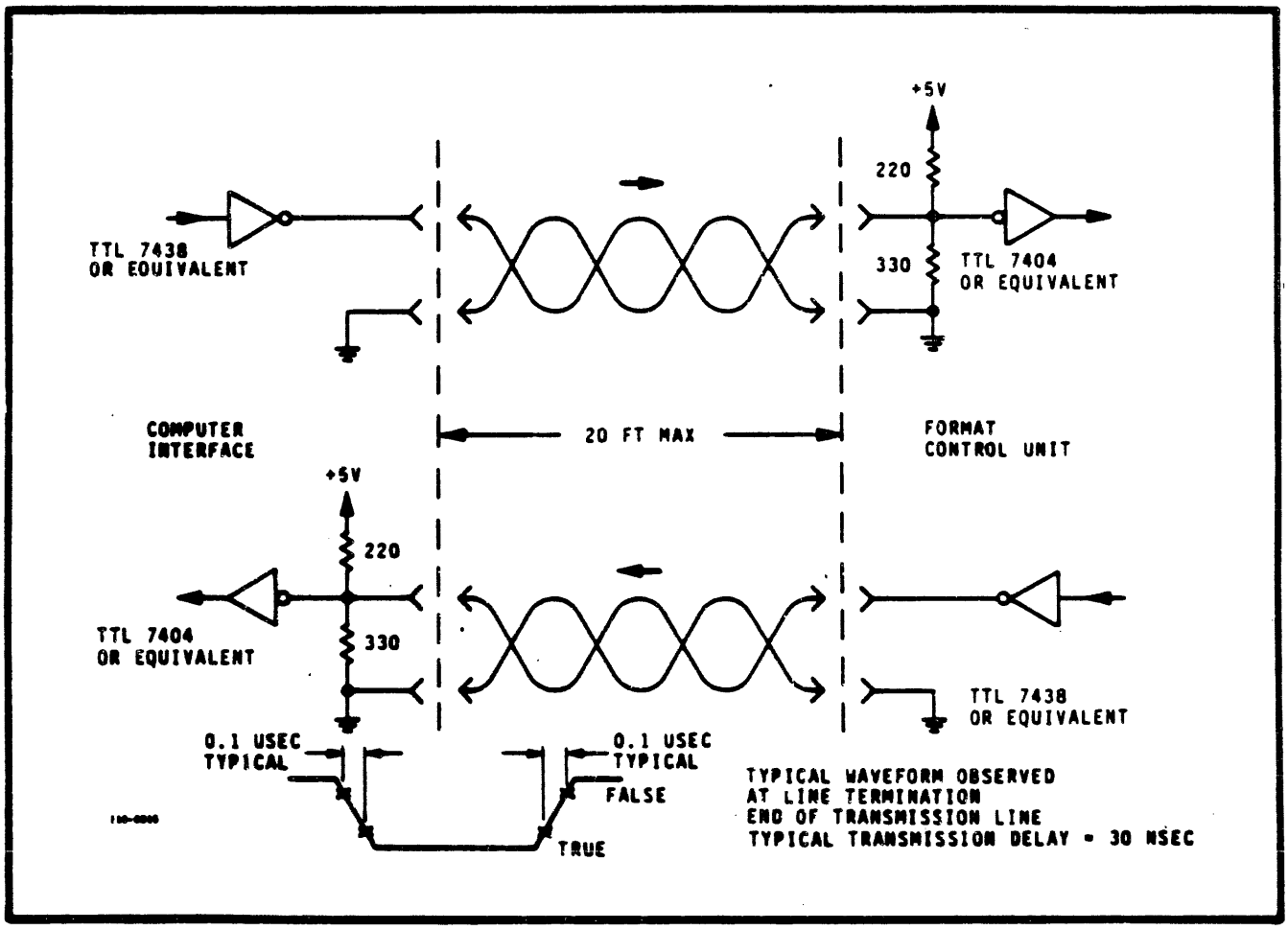


Figure 4-1
Typical Interface Configuration

Signal	Mnemonic	Level or Pulse
Interface Inputs		
(Controller to Formatter)		
Formatter Address	FAD	L
Transport Address	TAD0, TAD1	L
Initiate Command	GO	P
Reverse/Forward	REV	L
Write/Read	WRT	L
Write File Mark	WFM	L
Edit	EDIT	L
Erase	ERASE	L
Rewind	REW	P
Density Select	DEN	L
Offline Command	OFL	P
Last Word	LWD	L
Formatter Enable	FEN	L
Write Data Lines	WP, W0-W7	L
Interface Outputs		
(Formatter to Controller)		
Formatter Busy	FBY	L
Data Busy	DBY	L
Hard Error	HER	P
Check Character Gate	CCG	L
Identification	IDENT	L
Corrected Error	CER	P
File Mark	FMK	P
Write Strobe	WSTR	P
Read Strobe	RSTR	P
Read Data Lines	RP, R0-R7	L
Ready	RDY	L
Rewinding	RWD	L
Load Point	LDP	L
Online	ONL	L
File Protect	FPT	L
End of Tape	EOT	L
NRZI/PE	NRZI/PE	L

Table 4-1
Input/Output Signal List

TRANSPORT ADDRESS
TAD0, TAD1 Levels J5-46; J1-46

The status of these lines determines which of up to four transports are selected by the formatter. The following lists define the tape transport addresses produced as a result of the various TAD0, TAD1.

TAD0	TAD1	ADDRESS
0	0	SLT0
0	1	SLT1
1	0	SLT2
1	1	SLT3

Transport addresses are latched by the formatter on go pulse.

INITIATE COMMAND
GO Pulse J5-8

A pulse which initiates any command specified by the command lines described in the following paragraphs. Information on the command lines is copied in the formatter on the trailing edge of the GO pulse. FBY is set true when the GO pulse is given with the formatter and the selected transport ready.

NOTE: Command lines must be stable 0.5 microsecond before and after.

(X = Asserted)	Rev/Fwd	WRT/Rd	WFM	Edit	Erase
Read Forward					
Read Reverse	X				
Read Reverse (Edit)	X			X	
Write		X			
Write (Edit)		X		X	
Write File Mark		X	X		
Erase (Variable)		X			X
Erase (Fixed)		X	X		X
Space Fwd Block					X
Space Rev Block	X				X
Space Fwd File			X		X
Space Fwd File (w/STB)			X		
Space Rev File	X		X		X
Space Rev File (w/STB)	X		X		

Table 4-2
Command Table

COMMAND LINES

The levels on these lines issue a command to the formatter on the trailing edge of the GO pulse. The REV, WRT, WFM, EDIT, ERASE and DEN levels must be held steady from 0.5 microsecond prior to the edge to 0.5 microsecond following the trailing edge of the GO pulse.

REVERSE
REV Level J5-18

A level which initiates reverse tape motion when true. When false, this level specifies forward tape motion.

WRITE
WRT Level J5-34

Write mode is specified when this level is true; read mode is specified when this level is false.

WRITE FILE MARK
WFM Level J5-42

When this level and WRT are true, the formatter will write a file mark on the tape.

EDIT
EDIT Level J5-38

EDIT true and REV true modify the read reverse stop delay to optimize head positioning for a subsequent edit operation. When the EDIT level is true and WRT is true, the OVW (overwrite) line is activated and the selected transport operates in the edit mode.

ERASE
ERASE Level J5-40

ERASE true and WRT true cause the formatter to execute a dummy write command. The formatter will issue a normal write command but no data will be recorded. A length of tape, as defined by LWD, will be erased. When ERASE, WRT/READ and the WFM command lines are true approximately 3.75 inches (9.52 cm) of tape will be erased.

DENSITY SELECT
DEN Level J1-50

When true, this optional level selects the lower of two possible data transfer packing densities. When this level is false, the higher packing density is selected. This line is not latched by formatter on GO pulse. Also, to be used only with transport in remote density select. Formatter density will be slaved off transport status.

REWIND
REW Pulse J5-20

A pulse which causes the transport to rewind to load point. This pulse is directly routed to the transport and does not cause the formatter to go busy.

OFFLINE COMMAND
OFL Pulse J1-24

This pulse causes the transport to go offline without causing the formatter to go busy.

LAST WORD
LWD Level J5-4

When this level is true during a write or erase command, it indicates that the next character to be strobed into the formatter is the last character of the record. LWD goes true when the last data character is placed on the interface lines.

FORMATTER ENABLE
FEN Level J1-18

When false, this level causes all formatters in the system to revert to the quiescent state. This line may be used to disable the formatters if controller power is lost or to clear formatter logic when illegal commands or unusual conditions occur.

WRITE DATA PARITY AND WRITE DATA LINES
WP, W0-W7 Levels (refer to pin list)

These lines are present in both NRZI and PE formatters and will be defined for each application.

(1) NRZI Formatter

These 9 lines transmit write data from the controller to the formatter. Lines WP, W0-W7 are utilized for 9-channel operation.

For 9-channel operation the 8 data bits appearing on W0-W7 are written onto the corresponding channels on tape; W7 corresponds to the least significant bit of the character.

Line WP is optional and is utilized only if it is required to write the parity bit specified by the customer. When this option is not employed the formatter generates odd parity internally on the basis of data contained on W0-W7.

The first character of a record should be available on these lines within one character period after DBY goes true and remain until the trailing edge of the first WSTR is issued by the formatter.

The next character of information must then be placed on these lines within one-half of a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

(2) PE Formatter

The 8 write data lines (9 in the case of external parity option) are utilized to transmit write data from the controller to the formatter. W0 corresponds to the most significant bit and W7 to the least significant bit of each character.

The first character of a record should be available on these lines less than 40 character periods after DBY goes true and remain until the trailing edge of the first WSTR is issued by the formatter. The next character of information must then be placed on these lines within one-half of a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

4.3 INTERFACE OUTPUTS (FORMATTER TO CONTROLLER)

Pins J1-16 - J1-15 output the CHECK CHARACTER GATE for NRZI mode and the IDENTIFICATION for PE mode. The controller must allow for this signal when combination NRZI/PE formatting is used. All pulse widths are 1 microsecond wide (minimum).

FORMATTER BUSY
FBY — Level — J5-2

The level goes true on the trailing edge of GO when a command is issued by the controller. FBY will remain true until tape motion ceases.

DATA BUSY
DBY — Level — J1-38

This level goes true when the tape is up to speed, has traversed the IBG, and the formatter is about to write data or look for a read signal on the tape. DBY remains true until data transfer is completed and the appropriate post record delay is completed. DBY goes false when the capstan starts to decelerate the tape. New commands may be issued 0.5 microsecond after DBY goes false.

HARD ERROR
HER (NRZI Mode) — Pulse — J1-12

When true, this pulse indicates a read error. This line will be true during read operations when one or more of the following occurs:

(1) Longitudinal parity error
(2) Improper record format
(3) CRCC parity error
(4) Vertical parity error on a data character

In all cases except a vertical parity error, HER will be pulsed after the complete record has been read. In the case of a vertical parity error, the HER line will be pulsed when a read strobe (RSTR) pulse is issued for the character in error. DBY goes false after all error information has been transferred to the controller.

CORRECTED ERROR
CER — Pulse — J1-42
(PE Mode only)

When true, this pulse indicates that a single track dropout has been detected and the formatter is performing an error correction.

HARD ERROR
HER — Pulse — J1-12
(PE Mode)

When true, this pulse indicates that an uncorrectable read error has occurred and that the record should either be reread or rewritten. Here is a table illustrating the possible HER/CER signal combinations, together with their meaning:

Signal States			
HER	CER		
0	0	=	No Error Detected
0	1	=	Single Channel Error
1	0	=	Postamble, VRC ERROR or: Multiple Channel Errors
1	1	=	Excessive Skew or: Single Channel Failure w/Postamble VRC Error

HER/CER valid during RDS.

CHECK CHARACTER GATE
CCG — Level — J1-16
(NRZI Mode only)

This level is set true by the NRZI formatter when the read information being transmitted to the controller is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). When data characters are transmitted, CCG goes false. Data and check information can be distinguished by gating READ STROBE (RSTR) with CCG or its inverse. After leaving load point, J1-16 should be used only when $\overline{\text{NRZ}}$/PE status indicates NRZI mode.

IDENTIFICATION
IDENT — Level — J1-16
(PE Mode)

When true, this level identifies PE tapes. PE tapes are detectable in the read forward mode from load point by the presence of an identification burst on the parity channel. Use with NRZ line.

FILE MARK
FMK Pulse J1-14

File mark is pulsed when a file mark is detected on the tape during a read operation or during a write file mark operation in a read-after-write transport. The FMK line will be pulsed after a complete file mark record has been read. Error conditions should be ignored when a file mark is detected.

TRANSPORT STATUS AND CONFIGURATION LINES

These lines indicate the status and configuration of the selected transport to the controller after being gated with the formatter address signal, FAD. The low true transport status lines are: READY (RDY), ONLINE (ONL), REWINDING (RWD), FILE PROTECT (FPT), LOAD POINT (LP) and END OF TAPE (EOT).

Transport configuration lines are $\overline{\text{NRZ}}$/PE, $\overline{\text{7TK}}$/9TK and LOW/HIGH. Refer to pin list for location.

WRITE STROBE
WSTR Pulse J1-36

This line pulses each time a data character is written onto tape. WSTR samples the write data lines WP, W0-W7 from the controller and copies this information character by character into the formatter write logic. The first character should be available prior to the first write strobe pulse and succeeding characters should be set up within half a character period after the trailing edge of each write strobe pulse. The write strobe is also active during variable length erase commands; however, the data being copied into the formatter will have no meaning.

READ STROBE
RSTR Pulse J1-34

This line consists of a pulse for each character of read information to be transmitted to the controller. These signals should be used to sample the read data lines RDP, RD0-RD7.

In NRZI formatters, the transmission of CRC and LRC data characters will be flagged by the check character gate (CCG) signal as described under HARD ERROR (HER).

READ DATA LINES
RP, R0-R7 Levels (see pin list)

In the NRZI formatter, RP and R0-R7 are utilized for 9-channel operation; in PE formatters the 9 PE channels are assigned to RP, R0-R7.

Each character read from tape is made available by parallel sampling the read lines with READ STROBE. Since the data remains on the read data lines for a full character period, the corresponding RSTR pulses are timed to occur after approximately the center of the character period.

EMBEDDED FORMATTER INTERFACE PIN LIST AND CROSS REFERENCE TO 100 PIN CONNECTOR (J101)

J5 (A Connector) Sig	Gnd	Signal Name	Mnemonic	In/Out	9219 J101 Sig Gnd
2	1	Formatter Busy	FBY	Out	B22/B23
4	3	Last Word	LWD	In	B13/B14
6	5	Write Data 4	W4	In	B19/B20
8	7	Initiate Command	GO	In	A3/A2
10	9	Write Data 0	W0	In	B16/B17
12	11	Write Data 1	W1	In	A16/A17
14	13	Single	SGL	Out	A33/A32
16	15	+5v	+5V	Out	A48, 49, 50
18	17	Reverse/Forward	REV	In	B4/B5
20	19	Rewind	REW	In	B12/B11
22	21	Write Data Parity	WP	In	A15/A14
24	23	Write Data 7	W7	In	A21/A20
26	25	Write Data 3	W3	In	A18/A17
28	27	Write Data 6	W6	In	B21/B20
30	29	Write Data 2	W2	In	B18/B17
32	31	Write Data 5	W5	In	A19/A20
34	33	Write/Read	WRT	In	A4/A5
36	35	Read Threshold Level 2 (not used)	THR2	In	B9/B8
38	37	Edit	EDIT	In	A6/A5
40	39	Erase	ERASE	In	B7/B8
42	41	Write File Mark	WFM	In	B6/B5
44	43	Read Threshold Level 1 (not used)	THR1	In	A7/A8
46	45	Transport Address 0	TAD0	In	A1/A2
48	47	Read Data 2	R2	Out	B39/B38
50	49	Read Data 3	R3	Out	A39/A38

J1 (B Connector) Sig	Gnd	Signal Name	Mnemonic	In/Out	9219 J101 Sig Gnd
1	5	Read Data Parity	RP	Out	A36/A35
2	5	Read Data 0	R0	Out	B37/B38
3	5	Read Data 1	R1	Out	A37/A38
4	5	Load Point	LDP	Out	B30/B29
6	5	Read Data 4	R4	Out	B40/B41
8	7	Read Data 7	R7	Out	A42/A41
10	9	Read Data 6	R6	Out	B42/B41
12	11	Hard Error	HER	Out	A24/A23
14	13	File Mark	FMK	Out	A25/A26
16	15	Check Character Gate/Identification	CCG/IDENT	Out	B24/B23
18	17	Formatter Enable	FEN	In	A13/A14
20	19	Read Data 5	R5	Out	A40/A41
22	21	End of Tape	EOT	Out	A30/A29
24	23	Off Line Command	OFL	In	A12/A11
26	25	NRZI	NRZ	Out	A31/A32
28	27	Ready	RDY	Out	B27/B26
30	29	Rewinding	RWD	Out	B28/B29
32	31	File Protect	FPT	Out	A28/A29
34	33	Read Strobe	RSTR	Out	B36/B35
36	35	Write Strobe	WSTR	Out	A34/A35
38	37	Data Busy	DBY	Out	A22/A23
40	39	Speed	SPEED	Out	B34/B35
42	41	Corrected Error	CER	Out	B25/B26
44	43	Online	ONL	Out	A27/A26
46	45	Transport Address 1	TAD1	In	B3/B2
48	47	Formatter Address	FAD	In	B1/B2
50	49	Density Select	DEN	In	A9/A8

Table 4-3

100 PIN EDGE CONNECTOR TO EMBEDDED FORMATTER I/O CONNECTION CORRELATION CHART

9219 J101 Sig	Gnd	Signal Name	Mnemonic	In Out	Embedded Formatter Sig	Gnd
A1/A2		Transport Address 0	TAD0	In	A46/A45	
A3/A2		Initiate Command	GO	In	A8/A7	
A4/A5		Write/Read	WRT	In	A34/A33	
A6/A5		Edit	EDIT	In	A38/A37	
A7/A8		Read Threshold Level 1 (not used)			A44/A43	
A9/A8		Density Selection (see notes)	DEN	In	B50/B49	
A10		No Connection				
A12/A11		Offline Command	OFL	In	B24/B23	
A13/A14		Formatter Enable	FEN	In	B18/B17	
A15/A14		Write Data Parity	WP	In	A22/A21	
A16/A17		Write Data 1	W1	In	A12/A11	
A18/A17		Write Data 3	W3	In	A26/A25	
A19/A20		Write Data 5	W5	In	A32/A31	
A21/A20		Write Data 7	W7	In	A24/A23	
A22/A23		Data Busy	DBY	Out	B38/B37	
A24/A23		Hard Error	HER	Out	B12/B11	
A25/A26		File Mark	FMK	Out	B14/B13	
A27/A26		Online	ONL	Out	B44/B43	
A28/A29		File Protect	FPT	Out	B32/B31	
A30/A29		End of Tape	EOT	Out	B22/B21	
A31/A32		NRZI/PE	NRZI/PE	Out	B26/B25	
A33/A32		Single (not used)	SGL	Out	A14/A13	
A34/A35		Write Strobe	WRST	Out	B36/B35	
A36/A35		Read Data Channel P	RP	Out	B1/B5	
A37/A38		Read Data Channel 1	R1	Out	B3/B5	
A39/A38		Read Data Channel 3	R3	Out	A50/A49	
A40/A41		Read Data Channel 5	R5	Out	B20/B19	
A42/A41		Read Data Channel 7	R7	Out	B8/B7	
A43/A47		No Connection				
A48, 49, 50		+5 vdc	+5	Out	A16	
B1/B2		Formatter Address	FAD	In	B48/B47	
B3/B2		Transport Address 1	TAD1	In	B46/B45	
B4/B5		Reverse/Forward	REV	In	A18/A17	
B6/B5		Write File Mark	WFM	In	A42/A41	
B7/B8		Erase	ERASE	In	A40/A39	
B9/B8		Read Threshold Level 2 (not used)	THR2	In	A36/A35	
B10/B11		Parity Select (see notes)	PAR	In	(not used)	
B12/B11		Rewind	REW	In	A20/A19	
B13/B14		Last Word	LWD	In	A4/A3	
B16/B17		Write Data 0	W0	In	A10/A9	
B18/B17		Write Data 2	W2	In	A30/A29	
B19/B20		Write Data 4	W4	In	A6/A5	
B21/B20		Write Data 6	W6	In	A28/A27	
B22/B23		Formatter Busy	FBY	Out	A2/A1	
B24/B23		Check Character Gate (see notes)	CCG	Out	B16/B15	
B24/B23		Identification (see notes)	IDENT	Out	B16/B15	
B25/B26		Corrected Error	CER	Out	B42/B41	
B27/B26		Ready	RDY	Out	B28/B27	
B28/B29		Rewinding	RWD	Out	B30/B29	
B30/B29		Load Point	LDP	Out	B4/B5	
B33/B32		7 Track/9 Track	7TRK/9TRK	Out	(not used)	
B34/B35		Low/Hi Tape Speed (not used)	SPEED	Out	B40/B39	
B36/B35		Read Strobe	RSTR	Out	B34/B33	
B37/B38		Read Data 0	R0	Out	B2/B5	
B39/B38		Read Data 2	R2	Out	A48/A47	
B40/B41		Read Data 4	R4	Out	B6/B5	
B42/B41		Read Data 6	R6	Out	B10/B9	
B43/B47		No Connection				
B48, 49, 50		Ground				

Table 4-4

Notes

Density Selection (DEN) used in 9219 NRZI configuration only.
Parity Selection (PAR) used in 9219 NRZI configuration only.
Check Character Gate (CCG) is used in NRZI mode only. Identification (IDENT) is used in PE mode only.

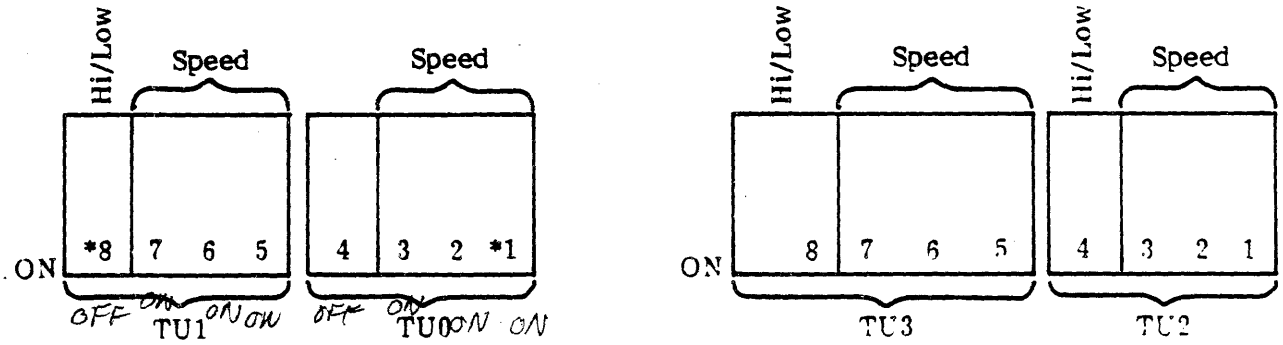
4.4 SPEED SELECTION

The formatter may be used with tape transports operating at seven different speeds, ranging from 12.5 to 125 ips. In NRZI operation each of the four addressable transports can operate at a different speed, while in PE operation only two different speeds may be used. Two DIP switches, K14 and N14, are used to match the formatter write clock frequency to the speed of each of the four addressable transports. Additionally PE operation requires switch settings to distinguish between the high and the low speeds and insertion of a header that includes the PLO components required for the different speeds. The two speed selection switches are shown in table 4-5, while the speed selection header configuration is shown in table 4-6.

Each of the two switch packages, shown in table 4-5 is divided into 2 groups of 4 switches each — 1 through 4 and 5 through 8. Each group of four switches is assigned to one of the four addressable transports, as shown in the table. The three lower order switches of each group (1 through 3 and 4 through 7) are used to select the actual speed using assigned binary values, as shown in the table. Switches 4 and 8 of each package are used in PE only to indicate whether the speed selected by the other three switches of the group is the high of the low PE speed, with the ON position indicating HIGH speed, and the OFF position indicating LOW speed. For example, in a system that includes two tape transports with tape unit 0 operating at 125 ips and tape unit 1 operating at 25 ips, the switch settings on K14, as derived from table 4-5, would be as follows:

	Speed			H/L	Speed			H/L
K14 Switch Number	1	2	3	4	5	6	7	8
Tape Unit 0 (125 ips)	ON	ON	ON	ON	X	X	X	X
Tape Unit 1 (25 ips)	X	X	X	X	OFF	ON	ON	OFF

As mentioned above, the component values of the PE speed selection header must match the speed of the system transport(s). The header is installed in the factory with single speed or dual speed components that are determined by the unit dash number, as tabulated in table 4-6.



K-14 N-14

035

OFF ON ON ON OFF ON ON ON
8 7 6 5 4 3 2 1

Speed ips	K14/N14 Switch Settings					
	SW1 (1)**	SW2 (2)	SW3 (4)	SW5 (4)	SW6 (2)	SW7 (1)
12.5 (1**)	ON	OFF	OFF	OFF	OFF	ON
18.75 (2)	OFF	ON	OFF	OFF	ON	OFF
25 (3)	ON	ON	OFF	OFF	ON	ON
37.5 (4)	OFF	OFF	ON	ON	OFF	OFF
45 (5)	ON	OFF	ON	ON	OFF	ON
75 (6)	OFF	ON	ON	ON	ON	OFF
125 (7)	ON	ON	ON	ON	ON	ON

Table 4-5
Speed Selection Switches

*Note that when looking at a mounted formatter the switch numbers appear upside down.

**Numbers in parentheses are binary values.

Single Speed Versions
(Low Speed Only: C3, C5 and R9 Not Used)

Dash No.	011	033	044	055	066	077	088
Speed (ips)	12.5	18.75	25	37.5	45	75	125
C4 (MFD)	.47	.33	.33	.33	.15	.068	.047
C6 (PF)	1500	820	680	430	390	220	150
R10 (OHMS)	270	150	150	150	270	560	820

Dual Speed Versions

		HIGH SPEEDS					
Speed (ips)		18.75	25	37.5	45	75	125
C3/C4 (MFD) C5/C6 (PF) R9/R10 (OHMS)		C3=.33 C5=820 R9=150	C3=.33 C5=680 R9=150	C3=.33 C5=430 R9=150	C3=.15 C5=390 R9=270	C3=.068 C5=220 R9=560	C3=.047 C5=150 R9=820
LOW SPEEDS 12.5	C4=.47 C6=1500 R10=270	-031	-041	-051	-061	-071	-081
18.75	C4=.33 C6=820 R10=150	see -033 single speed	-043	-053	-063	-073	-083
25	C4=.33 C6-680 R10=150	not used	see -044 single speed	-054	-064	-074	-084
37.5	C4=.33 C6=430 R10=150	not used	not used	see -055 single speed	-065	-075	-085
45	C4=.15 C6=390 R10=270	not used	not used	not used	see -066 single speed	-076	-086
75	C4=.068 C6=220 R10=560	not used	not used	not used	not used	see -077 single speed	-087

C3/C4 = 115-5040-xxx plastic capacitor
C5/C6 = 115-0016-xxx mica capacitor
(12.5 ips, 1500 pf is 115-0017-152
R9/R10 = 147-0002-xxx 1/4w resistor

Speed Selection Header

121-0153-001 → 14 pin dip component Header

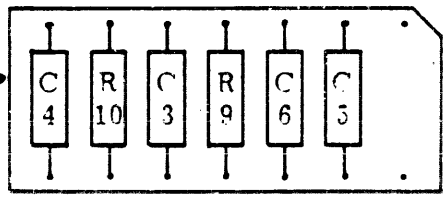


Table 4-6

4.5 INTERFACE CABLING REQUIREMENTS

The 9X00F formatter board is designed to accept two 50 conductor 3M type ribbon cables. An adapter board type 5304 is available to utilize 100 pin edge connectors cable configuration. If 100 pin twisted pair cable is utilized, all wires should be 24 AWG minimum with insulation thickness not less than 0.1 inch. Twist should not be less than one per inch and cable length should not exceed 20 feet. If ribbon cable is utilized, each cable should not exceed 20 feet in length.

Edge connectors are Kennedy PN 121-0162-002 for fifty conductor ribbon. Connector is Kennedy PN 121-0159-002 for 100 pin edge.

4.6 DAISYCHAINING

Up to three additional transports may be daisychained to the formatter in the 9X00F master. Daisychaining is accomplished utilizing ribbon cables and appropriate adapters for the transports.

Model 9000 transports will require a cable set PN 190-4999-001, one 190-4778-001 control adapter, and one 190-4779-001 data adapter. The 3860 data terminator and 3841 control terminator PCBAs should be removed from all but the physical last transport.

Models 9700, 9800, 9100 or 9300 may be daisychained by utilizing one 190-4747-001 adapter for each unit and two 190-4999-NLL cables (N = number of transports, LL = total length).

If one Model 9000 is mixed with 9100, 9300, 9700 or 9800 transports, it must be the physical last transport. Data and control terminators must be removed from all but the physical last transport. Maximum total cable length must not exceed 20 feet for any daisychaining configuration. Transport address may be assigned by switches (in the transport control masterboard for Model 9000, or at switches on the 4747 adapter board for other than Model 9000, or by thumbwheel address switch if ordered in the transport).

5.0 MODES OF OPERATION

5.1 READ OPERATIONS

5.1.1 READ ONE BLOCK

Select formatter and transport by setting appropriate FAD, TAD0, TAD1 with FEN true. During read operations HER should be monitored as well as status lines. In read from load point CCG/IDENT should be monitored. If IDENT is true from load point, this indicates tape is recorded in PE mode. IDENT should be compared with NRZ to ensure transport is set at appropriate density. And, if operation is in NRZI mode, CHG true indicates check characters and not data are being transferred with RDS.

The following sequence of commands to and responses from the formatter are used in a read operation:

a. With transport selected and online at LP set all command lines false (read one block).

b. Initiate command: issue go pulse.

c. FBY will go true.

d. After prerecord delay, DBY will go true.

e. Check status and configuration (ONLINE, RDY, NRZ and IDENT).

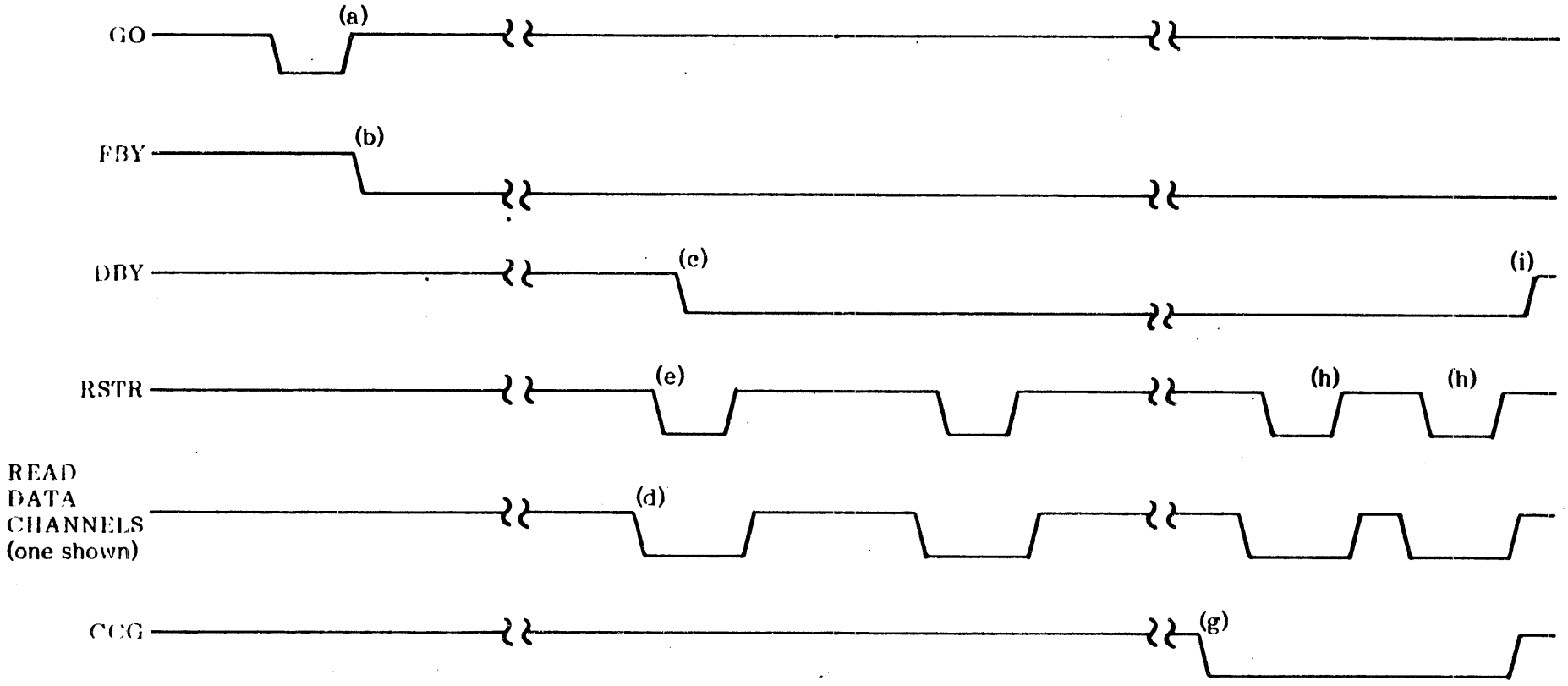
f. If status OK, then read data with RDS.

g. At end of record, DBY will go false.

h. A new command may be issued at drop of DBY. If no new command is issued, transport will stop and

i. FBY will go false.

Refer to figure 5-1 for read operation timing.



a. Read one block command accepted
b. FBY set true
c. DBY set true after prerecord delay
d. Read data true
e. Read data clocked on RDS
g. At end of data CHG true
h. CRC and LRC bytes with RDS
i. DBY false

NOTE: For PE operation omit g and h as there is no CRCC or LRCC in PE format.

Figure 5-1
Read Sequence Timing

5.1.2 READ ERROR RECOVERY

If HER was indicated during read operation, then error recovery should be attempted. This may be done at drop of DBY or FBY. Use the following sequence to reread a record in error:

a. Set Rev/Fwd True

b. Initiate command: issue GO pulse

c. FBY will go true

d. DBY will go true after delay

e. When DBY goes false read one block command may be reissued. It will not be executed until FBY would have dropped.

f. Follow sequence for read one block above

NOTE: After three retrys, all of the automatic clipping levels available have been tried. More attempts may be made or the record may be flagged as a nonrecoverable error.

5.1.3 READ FILE MARK

File marks detected in read one block operations are flagged by FMK. If FMK is true at end of record, error status should be ignored.

5.1.4 FILE SEARCH OPERATION

There are two forward and two reverse file search modes available (refer to command table 4-2 in previous section). The following sequence should be followed for file search operations:

a. Set desired search command

b. Initiate: issue GO pulse

c. FBY true

d. DBY true after delay

e. File Mark flag (FMK) true

f. Ignore errors for FMK record if any occur

g. DBY false

h. New command may be issued at drop DBY

i. If no command issued, FBY false

NOTE: If file search w/strobe was used RSTR will be active for all records read.

5.1.5 PE READ REVERSE

This command, when executed in PE, allows reverse read of a record. Execute in same manner as a read command with reverse set true.

5.2 WRITE OPERATIONS

5.2.1 WRITE ONE BLOCK OPERATION

Refer to figure 5-2 for basic signal sequencer information. Use the sequence listed below. Sequence assumes proper FAD, FEN, TAD0, TAD1, ONLINE and READY monitor status. If initiated from load point, BOT GAP and if PE, IDENT burst must be written first and is performed automatically. Sequence is for NRZI. For PE operation, see note after sequence.

a. Set WRT true

b. Initiate command: issue go pulse

c. FBY true

d. After prerecord delay, DBY true

e. One character period after DBY true WSTR will issue — first byte must be on data lines within one half character time of DBY true

f. Data may be changed on trailing edge of WSTR — must be changed at least one half character time before WSTR

g. Set last word (LWD) true coincident with last byte to be written

h. Formatter automatically writes proper CRCC and LRCC

j. Complete RAW ERROR checking

k. Record terminated — DBY false

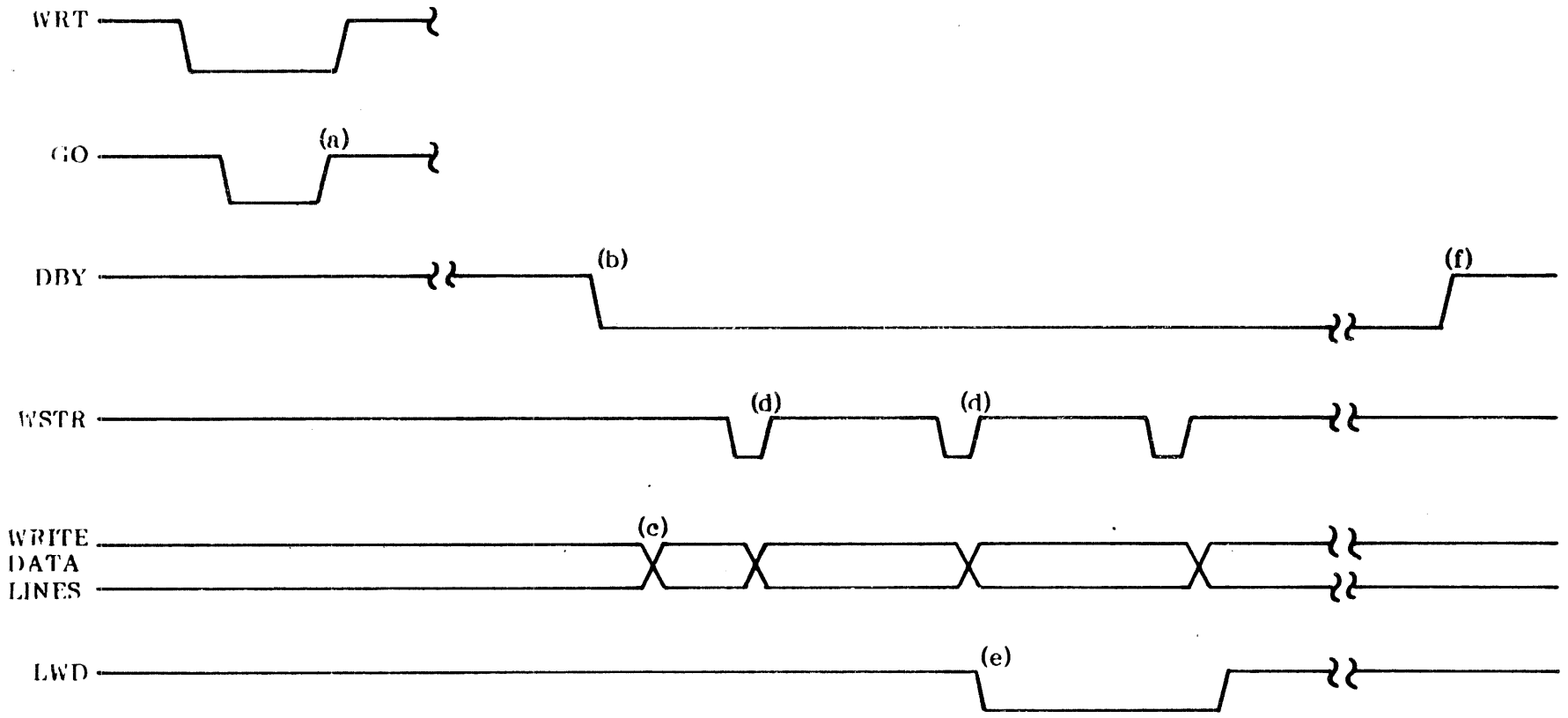
l. New command may be issued on drop of DBY

m. If no new command, transport stops, FBY false

NOTE: In PE operation, WSTR is delayed 40 character times after DBY. IDENT will go true on start from LP. HER and CER should be monitored throughout record. Refer to HER, PE mode in section 4 for HER/CER meanings.

5.2.2 WRITE FILE MARK OPERATION

Follow same sequence as above (5.2.1) with the addition of set WFM true along with WRT. A file mark will automatically be written. No WSTR will be issued. File mark flag will go true on read-after-write of file mark.



a. Command set on trailing edge of GO
b. After prerecord delay DBY true
c. Write data set true at least one half character time before WSTR (b to d = d to d_1)
d. Write strobe (WSTR) writes data
e. Last word (LWD) set true coincident with last byte terminates record
f. After post record delay DBY false

Figure 5-2
Write Sequence Timing

5.2.3 WRITE ERROR RECOVERY

When a write error occurs, it is desirable to either rewrite the record or ensure its erasure. Since write errors may be caused by dust on the head it is recommended that attempts to rewrite the record be made. If write error is repeated, then bad tape may be the problem, in which case the record should be erased and written again on an area "down tape."

The recommended method for handling write errors is to follow the command chain listed below:

a. On detection of a write error — at drop of FBY, set space rev. block command

b. Issue GO pulse — space rev. block CMD will be executed FBY will go true

c. At drop of FBY, set WRT command

d. Continue as in sequence for write one block in paragraph 4.1.1

If the error continues to occur, then assume bad tape and erase the area on tape where attempts had been made and write record again. This is accomplished with the following procedure:

a. On detection of a write error — at drop of FBY, set space rev. block command

b. Issue GO to initiate command

c. FBY will go true

d. At drop of FBY, set erase variable command

e. Initiate GO pulse

f. Set LWD at a number of bytes in excess of the length of the record to be erased

g. Sequence from setting of LWD is the same as for write one block in paragraph 4.1.1

Alternatively, if record length is less than 4 Kbytes, an erase fixed length command may be issued. In this case, approximately 3.75 inches of tape will be erased and it is not necessary to use LWD in the sequence above. New command may be issued with GO pulse at drop of DBY.

5.2.4 WRITE EDIT OPERATION

When it is desired to update a record on an existing tape, the following write edit operation may be used:

a. Read tape until desired record is found

b. Read forward one additional record

c. Read reverse

d. Read reverse edit

e. Write edit

Updated record must be the same length as original record. Also, it is not recommended to edit the same record more than three times.

5.3 ON THE FLY OPERATION

The timings noted in previous paragraphs are for on the fly operation. Issuing the commands for on the fly operation is done at drop of DBY. For full start/stop mode operation, wait for drop of FBY before issuing new command. Reverse motion commands are accepted on the fly and executed at the same time they would be if FBY were dropped and command were issued on drop of FBY.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

The formatter performs all the functions required for reading and writing tapes in phase encoded or NRZI formats that conform to ANSI specifications and are compatible with IBM standards. This formatter may be used with Kennedy Models 9000, 9100, 9300, 9700 and 9800 tape transports at selectable speeds of 12.5, 18.75, 25, 37.5, 45, 75 and 125 inches per second.

The formatter accepts commands and write data in the form of logic levels from the computer controller, converts the data to the selected density and format and translates the controller commands to transport motion commands, satisfying all timing and interlock requirements. The formatter also accepts read data, either in PE or NRZI codes, from the tape transport, converts the data to logic levels, performs error checks (and correction in PE) and supplies the required clocks to the controller. The formatter consists of the following functional blocks:

a. A microsequencer network, which controls all aspects of formatter operation, including tape motion, read recovery and data generation

b. A data recovery section that converts the coded data supplied from the transport to the logic level data supplied to the controller and performs error checking and clock generation functions for both PE and NRZI formats

c. A data generation section which converts logic level data supplied by the controller interface to the selected format and supplies it to the transport

d. A crystal oscillator and timing network that generates the microsequencer clock and the write clocks

e. An interface section that accepts and supplies commands and status to and from the controller and tape transport

Figure 3-1 is a general block diagram of the functional units of the formatter. The following paragraphs offer a complete description of the various functions.

3.2 MICROSEQUENCER NETWORK

THE CONCEPT

The microsequencer is at the heart of the formatter design. As the name implies, this network controls the sequence of events that takes place in reading and writing formatted tapes. Note that a thorough understanding of the microsequencer is not essential for troubleshooting purposes. The signature analysis (SA) method of troubleshooting was implemented in the formatter design, allowing for a straightforward method of troubleshooting which does not require delving into the complexities of the network. A detailed explanation of SA is offered in the maintenance section of the manual.

The main components of the microsequencer network are: a program controller, an arithmetic logic unit (ALU), an input section, an output section, and the program memory. The central component of the network is Microprogram Controller type 2910, an address sequencer that controls the sequence of execution of the microinstructions stored in the program memory. This

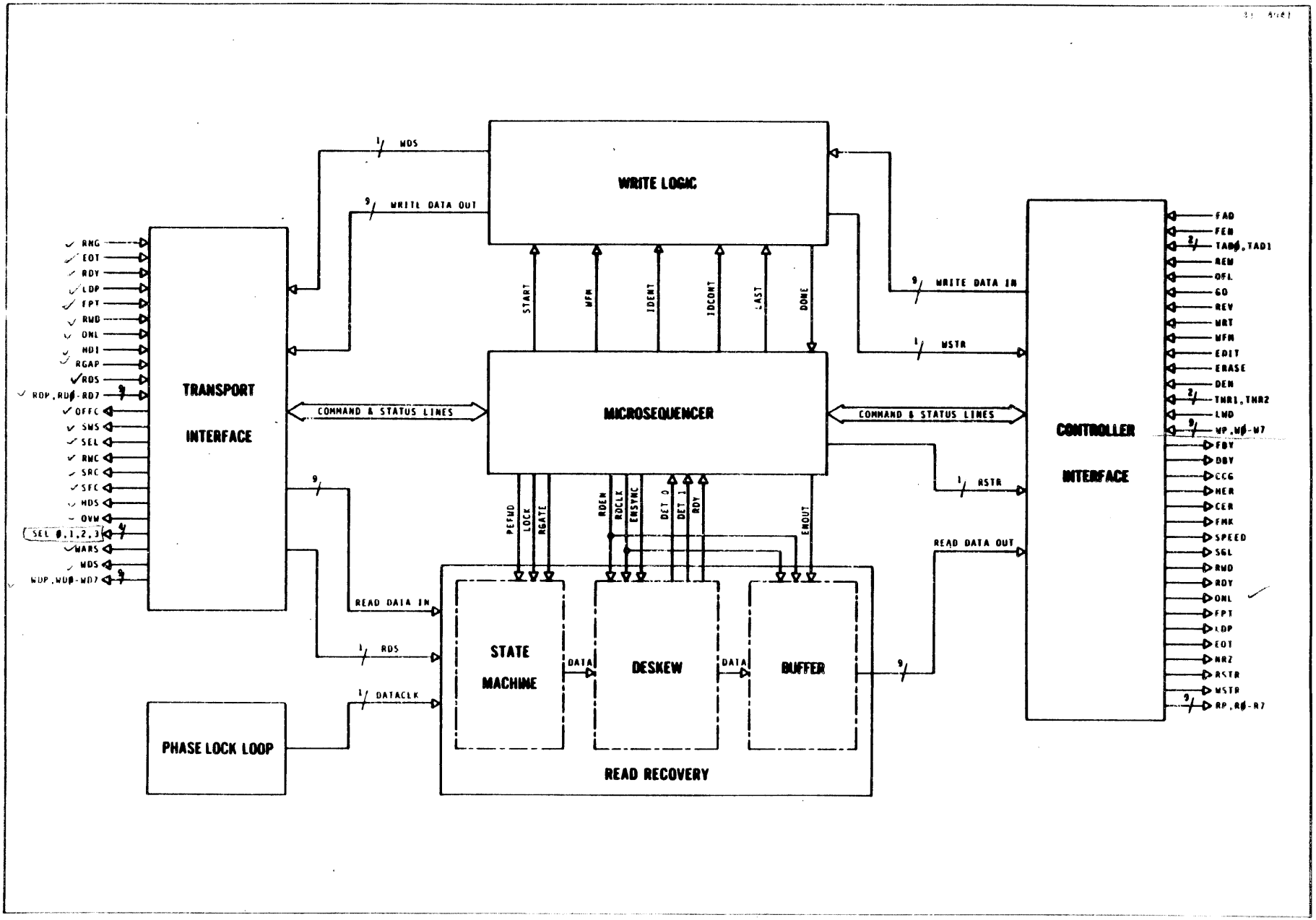


Figure 3-1. Overall Block Diagram

device has sequential addressing and branching and looping capabilities in response to a set of 18 instructions. A single bit ALU network provides the program controller with the condition code necessary during conditional branching instructions. The ALU is also used to set or reset particular bits in the output section of the microsequencer. The microsequencer input section supplies the status of various lines from both the tape transport and the formatter, and controller commands supplied from the command latch to the input of the ALU network. The microsequencer output section supplies the motion commands to the transport, formatting instructions and intermediate flags used during the reading and writing of data. The program store is addressed by the program controller and provides the actual microinstruction words, each 23 bits wide. The microinstruction words include ALU instruction fields for manipulating the data, program control instructions for deriving the next address, and specific bits that control certain microsequencer functions. The following paragraphs offer a detailed explanation of each component in the microsequencer network.

THE DETAILS

Program Controller

(Schematic sheet 7 of 12)

Microprogram Controller type 2910 (IC N10) is a device that selects one output address from four possible address sources, in accordance with microprogram instructions. The 2910 device consists of a 12 bit program counter, a 5 word by 12 bit push/pop stack, at 12 bit register/counter, an instruction decoder and a 4 to 1 multiplexer. The four address sources selectable by the program controller are:

a. The internal program counter, which provides sequential addressing when no branches or jumps are called for by the program. The program counter is incremented by Sequence Clock SEQCLK, and presents the present address plus one following each sequence cycle.

b. The internal stack, a five word, twelve bit stack which stores the present program counter contents plus one during branch to subroutines instructions, thus providing the program controller with a return address when subroutine execution is completed. The stack provides for five levels of subroutine nesting.

c. Direct inputs. Two three-state sources are tied to the direct input bus of the Program Controller. One source is the mapping ROM (K11), selected by MAP/ true, which provides the general reference within the main program. The second direct input source, selected by PL/ true, is the address field of the microinstruction word (NA0-NA9), supplied from the main control store through pipeline register N9, P9. During branching instructions this address field supplies the subroutine address or the branch address of the next microinstruction.

d. The internal 12 bit counter/register. This counter/register is provided with the same parallel direct inputs described in step c. It can be loaded with direct inputs for later branching, or it can be used as a decrementing counter. In its second mode of operation the counter/register is loaded with a count from the direct inputs and is then decremented and its output is tested for a zero internally for branching purposes. In this mode the counter is particularly useful for implementing time dependent functions, such as timing out prerecord gaps, fixed erase gaps, etc.

The program controller is clocked by SEQCLK, a 3.6 MHz frequency supplied from the crystal oscillator. The source of the next instruction is determined by the program controller instruction field INST0-3 of the microinstruction word. These four instruction lines encode the sixteen possible controller instructions, as listed in Table 3-1. Conditional branches are determined by the state of the ALU result register, supplied as RESULT to the program controller Condition Code (CC/) input at N10-14. During unconditional branches Condition Code Enable CCEN/ false, supplied by the microinstruction word, forces the branch regardless of the outcome of the ALU test.

Code (INST0-3)	Mnemonic	Instruction
0	JZ	Unconditional jump to map address
1	CJS	Conditional jump to subroutine address
1 (CCEN=1)	JSB	Unconditional jump to specified subroutine address
2	JMAP	Unconditional jump to specified map address
3	CJP	Conditional jump to specified branch address
3 (CCEN=1)	JMP	Unconditional jump to specified branch address
4	PUSH	Push the PC contents onto stack and load counter with specified count if CC=0
7	JRP	Conditional jump to address in register
8	RFCT	Loop, via the stack address, until counter=0, then proceed to next sequential address
10	CRTN	Conditional return from subroutine
10 (CCEN=1)	RTN	Unconditional return from subroutine
11	CJPP	Conditional jump to specified branch address and POP the stack
11 (CCEN=1)	POP	Unconditional jump to branch address and POP stack
12	LDCT	Load internal counter with specified count
13	LOOP	Proceed to next sequential address if CC=1, loop, via stack address, if CC=0
14	CONT	Proceed to the next sequential address
15	TWB	Jump to the stack address until the counter equals zero, then jump to the specified branch address.

Table 3-1. Program Controller Instruction Set

Control Store

(Schematic sheet 9 of 12)

The control store consists of three 512 word by 8 bit PROMs (P13, N13, R13) whose parallel configuration yields a 512 word by 24 bit (only 23 bits are utilized) program memory. The 10 bit address presented at the output of Program Controller is supplied to the address inputs of the control store as RA0-RA8, and to the Chip Enable input of the PROMs as PAGE0/. During each microsequencer cycle a different microinstruction word is addressed by the program controller and is then presented at the PROMs' outputs as RD0-RD22. The RD4-RD22 bits of the microinstruction word are clocked into a set of three octal flip-flop devices N9, P9 and R10 (see schematic page 7 of 12) by Sequence Clock SEQCLK. The RD0-RD3 outputs of the PROMs are first supplied to a quad 2 to 1 multiplexer (R9). During the Signature Analysis K9 substitutes preset levels for the PROM outputs, forcing the Program Controller into the Continue state, in which it continually loops through its address range. The microinstruction word is divided into 9 fields, each used to control a different aspect of microsequencer operation. The microsequencer fields are listed in Table 3-2.

PROM Outputs	Latch Outputs	Functional Description
RD0-3	INST0-3	Program controller instructions
RD4-7	INST4-7	ALU instructions
RD8-12	NA0-4	Input/output sections address lines
RD8-17	NA0-9	Program controller direct address inputs
RD18	RSTR	Read strobe
RD19	CCEN/	Condition code enable
RD20	TCLR	External timer clear
RD21	TMEN	External timer enable
RD22	INIT/	Initialize

Table 3-2. Microinstruction Word Fields

The Input Section

(Schematic sheet 8 of 12)

The microsequencer Input Section consists of four 8 to 1 multiplexers (K10, K11, K12, K13) whose three-state outputs are wire OR'ed. The Input Section accepts controller commands from the command latch (such as ERASE), transport status indications (such as Load Point LDP), status indications from other formatter sections (Envelope ENV, for example), the outputs of external timers (TMOUT1, for example), and temporary register outputs (TEMPA). During certain microsequencer operation the program calls for loading a particular signal from the Input Section into the ALU input latch, to be tested during conditional branching instructions. In that

case the address of the particular signal to be tested is carried by bits NA0-NA4 of the microinstruction. Bits NA3, NA4 are supplied to the address inputs of dual 2 to 4 demultiplexer K9, selecting one of the Input Section multiplexers by setting its Enable input low. Bits NA0-NA2 of the microinstruction select a particular input of the enabled multiplexer, and that input is gated through to the ALU input latch at L13-12.

ALU Network

(Schematic sheet 8 of 12)

A single bit ALU network is utilized by the microsequencer to test the status of bits in the Input Section, and set and reset bits of the Output Section, as well as generate the Read Clock RCLK. The ALU instruction set is listed in Table 3-3.

The main ALU network components are:

a. Input latch L13-12, used to store bits supplied from the Input Section to be tested by the ALU.

b. ALU ROM M9, used to decode the ALU instructions and perform the logic operations required.

c. Result register L13-2, used to store intermediate results which may be output to the Output Section or supplied to the Program Controller to determine the outcome of conditional branching instructions.

As an example of ALU operation we will use a fictitious microinstruction which calls for ANDing TEMPA with the present contents of the result register and storing the complement of the result in the Output Section TEMPA register. On the falling edge of SEQCLK TEMPA, addressed by bits NA0-4 of the microinstruction, is loaded into the ALU input latch L13-12 from the Input Section. The input latch presents the state of TEMPA to the M9-5 address input of the ALU ROM, while the state of the result register is presented to the ROM address input at M9-6. The ALU instructions, carried on bits INST4-7 of the microinstruction, are supplied to four address inputs of the ALU ROM. The ROM decodes the instruction and, in this particular case, performs the AND operation on the contents of the result register and the input latch. The outcome of the operation is then supplied to the result register L13-2 on the rising edge of SEQCLK. To store the complement of the outcome of the operation in TEMPA of the Output Section, the ROM sets its output enable line high at M9-12. The output enable line opens NAND gate M3-9, gating the next SEQCLK through to the enable input of demultiplexer K9-15. The NA3-4 bits of the microinstruction enable selectable octal latch L12 through K9, while bits NA0-2, applied to the select lines of L12, cause TEMPA to be selected. The result register output is then inverted by exclusive-OR gate L8-3 and is loaded into TEMPA at L12-3, completing the execution of the instruction. The output of the result register L13-5 is applied directly (as RESULT) to the Condition Code input of the Program Controller, where it determines the outcome of conditional branching instructions.

Code (INST4-7)	Mnemonic	Instruction
0	NOP	No operation, does not affect result register
1	LD	Loads selected status from Input Section into result register
2	LDC	Loads complement of the selected input into results register
3	LAND	Loads result of (result register contents AND selected input) into result register
4	NAND	Loads complement of (3) into result register
5	LSET	Sets selected bit of Output Section to one
6	NULL	Forces result register to one
7	LOR	Loads result of (result register contents OR selected input) into result register
8	RST	Sets selected bit of Output Section to zero
9	NOR	Loads complement of (7) into result register
A	CRCLK	Conditionally generates RCLK pulse
B	LXOR	Loads result of (result register contents XOR selected input) into result register
C	XNOR	Loads complement of (B) into result register
D	STO	Loads the selected output with the content of the result register
E	STOC	Loads the selected output with the complement of the result register content
F	RCLK	Unconditionally generates RCLK pulse

Table 3-3. ALU Instruction Set

ion

e outputs supplied from the microsequencer network to the other ape transport and to the controller interface. The Output Section ble octal flip-flop devices, ICs L9, L10, L11 and L12. The output of nnected to the D input of all four devices through exclusive-OR gate the microinstruction word enable a particular output device through s NA0-2 select a single flip-flop on the enabled device. At the eration the four devices are cleared by the Initialize INIT/ line re register (schematic page 7 of 12).

the microsequencer network with a single data cell time reference time reference TMOUT2. The timer consists of dual eight-bit shift e shift register is enabled by Timer Enable TMEN, supplied from the ked by 1/8C, a clock frequency at eight times the PE data rate ork. After eight 1/8C pulses TMOUT1 goes high, indicating that one e second portion of the timer is enabled by PEOUT and is clocked by y clock generated by the microsequencer. After eight data cell T2 goes high. Timer Clear TCLR clears both halves of the timer. supplied to the Input Section of the microsequencer network, to be nt subroutines.

R AND

ling network are used to generate the master frequency that clocks , as well as the write clocks used to generate both PE and NRZI data. he timing network are a crystal controlled, 7.2 MHz oscillator, a an associated ROM that generates write clock frequencies in ed transport speed and data density, a register used to determine itional flip-flops and gates.

ency is supplied by an oscillator network utilizing a 7.2 MHz crystal two inverter sections of P5. The resultant 7.2 MHz square wave is p N6-9, supplying SEQCLK, a 3.6 MHz frequency used to clock the ciated functions. The 7.2 MHz oscillator output is also supplied to counters R6, R8 connected as a divide-by-256 counter. The parallel reset by the outputs of timing ROM R7. The ROM address inputs

include the transport speed selection lines SPD0-2, density select line PE/NRZ/, and IDENT/, the ID burst mode output by the microsequencer. The counter is preset in accordance with the selected transport speed and data density and counts up to full count. At full count the carry output of R8-15 goes high, gating the subsequent oscillator transition through P8-3 to preload the counter and repeat the sequence. Note that in the NRZI mode the counter clock is halved by SEQCLK/, gated through J5-6 to the enable input of R6. In addition the counter frequency is halved during the PE identification burst, to generate the frequency required to write the ID burst on channel P. The carry output of R8-15 is supplied to the J-K inputs of flip-flop N6-1, to produce WCLK, a square wave at twice the data rate for PE, and at the data rate during NRZI operation. In the PE mode WCLK is divided by 2 by flip-flop P6-11 to generate TOGGLE, a PE data rate square wave used to invert data polarity in PE data generation. TOGGLE is inhibited during NRZI operation by NRZI/ low at the direct clear of P6-13.

WCLK is also supplied to a pulse shaping network consisting of D flip-flop P6-3 and 8-bit shift register P7. The rising edge of WCLK clocks P6-5 to the set state, supplying a high input to the shift register. The register is clocked by the 7.2 MHz output of the crystal oscillator. Following one clock count the QA output of the register goes high, generating Out Clock OCLK, used to clock the write data out of the formatter outputs. Five 7.2 MHz clock counts later the QE output of shift register P7 goes high to generate Write Data Strobe WDS. WDS, gated with Write Data Strobe Enable WDSEN, is the write strobe that is supplied to the transport write amplifiers to clock the data in. Three 7.2 MHz clock counts later the QH output of P7 goes high to reset flip-flop P6-1, which in turn supplies a low input to the shift register to terminate the clock pulses. The output of flip-flop P6-5 is supplied to NAND gate P8-6. During PE operation TOGGLE halves the clock frequency of P6-5, generating the data rate internal write strobe WSTB. Note that during NRZI operation the output rate of P6-5 is already at the data rate, consequently TOGGLE is inhibited. WSTB is gated with MARK and SYNC/, which inhibit the clock during the file mark, enabling it only during actual data, and is output as the external Write Strobe WSTR/ to the controller interface at connector J1.

3.4 PHASE ENCODED DATA GENERATION

3.4.1 INTRODUCTION

Write data in the form of logic levels, supplied from the controller interface, is converted to phase encoded data by the PE write circuits. The write clocks required, shown in timing diagram Figure 3-2, are supplied from the crystal controlled oscillator and dividing network. The PE formatting circuits generate the writing of the preamble and postamble, and supply the control signals to the write circuits. The PE write program of the microsequencer oversees the entire operation, supplying the required motion commands to the transport. These functions are explained in the following paragraphs.

3.4.2 PHASE ENCODED DATA FORMATTING

THE CONCEPT

The formatting of phase encoded data includes the generation of an identification burst of alternate 1s and 0s on channel P at loadpoint, the writing of a preamble consisting of 40 all-0 characters followed by a single all-1 character prior to each block, and writing a postamble consisting of a single all-1 character followed by 40 all-0 characters following each data block. The main component in formatting the data is a formatting counter that is enabled by the START pulse supplied by the microsequencer when the tape is up to speed and the prerecord gap has been timed out. The formatting counter counts out the 40 preamble 0s then the all-1 character while the network supplies Write Data Strobe Enable WDSEN and Output Enable OUTEN true, enabling the writing of the preamble. During the data portion of the block the formatting counter is locked on the 41st count until the last word indication is received from the controller, at which point the counter is enabled again and counts the single all-1 character and the 40 0s of the postamble.

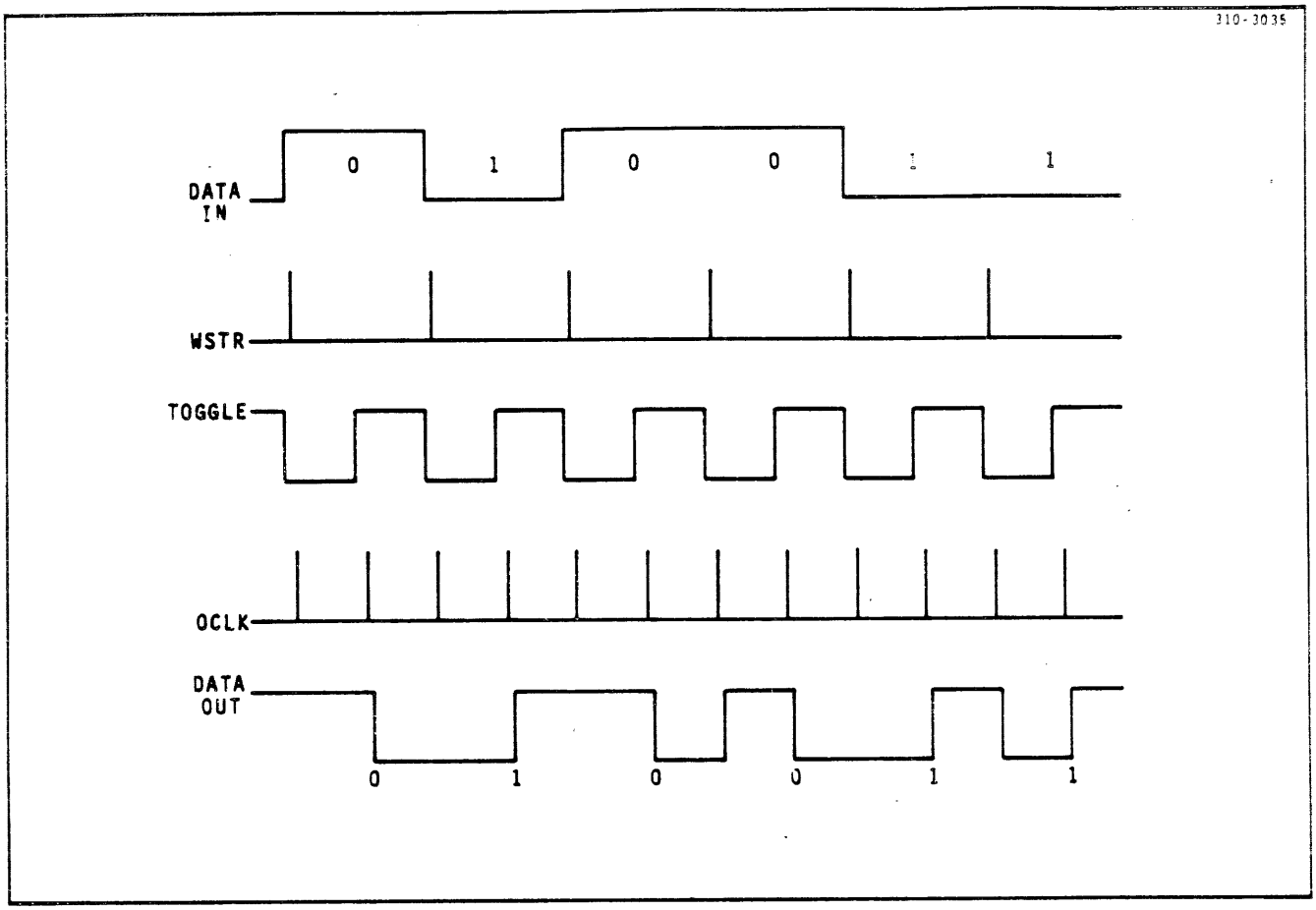


Figure 3-2. PE Write Timing

THE DETAILS

(Schematic sheet 11 of 12)

Once a write command is issued by the controller, provided that all the relevant interlocks are satisfied, the microsequencer supplies a Synchronous Forward Command SFC, and times out the prerecord gap. When the transport is up to speed and the prerecord gap has been timed out, the microsequencer issues a START pulse, about 280 nsec in duration. This pulse sets flip-flop N7-13, whose high output enables the formatting counter to start counting. The counter consists of a decade counter and a 4-bit binary counter in tandem, and is clocked by TOGGLE atthe PE data rate. Additionally the Q output of flip-flop N7-13 DONE/ high is stored by flip-flop M6-12. The Q output of the latter flip-flop generates Write Data Strobe Enable WDSEN true through OR gate ICL7-6 and its Q/ output generates Output Enable OUTEN true through NAND gate K8-6. These signals enable the write gating and initiate the writing of the 40 preamble 0s. The formatting counter counts up to 40, its QC output then goes high to reset flip-flop N7-4. The next TOGGLE transition, equivalent to the 41st character count of the preamble, clears flip-flop M6-5, the Q output of the flip-flop going low to disable the formatting counter, which remains locked at count 41. At this point the Q/ output of flip-flop M6-6 is high, and the Q/ output of the next flip-flop, M5-6, is low; these two outputs then activate exclusive-OR gate L8-6 to generate Write Zero WRTZ true. This signal is used to invert the polarity of write data for a single character frame in order to write the all-1 character at the end of the preamble. The following TOGGLE transition clears flip-flop M5-6 and sets WRTZ false again. Once flip-flop M5-6 is cleared, the Q/ outputs of both M5, M6 flip-flops are high and activate AND gate L5-3, generating SYNC/ high. SYNC/ high indicates the beginning of the actual data, enabling the write data buffer to accept data from the controller. SYNC/ remains high until the first character of the postamble, when it goes low again to disable the write buffer. When the last word indication is supplied, either from the controller as Last Word LWD, or is internally derived during self-terminating sequences as LAST from the microsequencer network, NOR gate N8-13 is activated to set flip-flop N7-9. The Q output of the flip-flop goes high, is inverted and sets flip-flop N7-3. The N7-4 output sets flip-flop M6-5 on the next TOGGLE transition. M6-5 high enables the formatting counter once again to initiate the writing of the postamble. Note that the Q/ output of M6 is high during the first postamble count, the Q/ output of M5 is still low, so the inputs to exclusive-OR gate L8 are opposite in polarity and the gate generates WRTZ high for a single character period to write the postamble all-1 character. On the next TOGGLE transition flip-flop M5 is cleared to set WRTZ low. When the formatting counter reaches the count of 80, its QD output at M8-11 goes high, activating NOR gate N8-10 and resetting flip-flop N7-13 to generate DONE/ true. DONE/ low disables the formatting counter and causes flip-flop M6 to be cleared on the next TOGGLE transition. The Q output of the flip-flop goes low to set Write Data Strobe Enable WDSENB false, and its Q/ output goes high to activate K8-6, supplying Output Enable OUTEN false, inhibiting the data outputs to the transport.

3.4.3 PHASE ENCODED WRITE CIRCUITS

THE CONCEPT

Write data in the form of logic levels is supplied from the controller interface and clocked into a write buffer by Write Strobe WSTR. The outputs of the write buffer are gated through a set of exclusive-OR gates with TOGGLE, a square wave at the data frequency that generates polarity reversals in mid-cell, thus phase encoding the data, as shown in timing diagram Figure 3-2. The outputs of the exclusive-OR gates are clocked through a set of multiplexers by Out Clock OCLK at the 3200 fri rate, and through a set of open collector drivers to be supplied to the transport write amplifiers, provided that Output Enable OUTEN, supplied from the formatting circuits, is true. The parity channel may be supplied from the controller or it may be derived internally by a parity tree, at the user's discretion.

During a Write File Mark command only channels 2, 6 and 7 gate TOGGLE through, while the remaining channels are held quiescent, thus writing a burst of 0s only on the required channels. During the writing of the PE Identification Burst at load point all channels with the exception of channel P are held quiescent, while channel P is toggled at the 1600 fri rate to write alternate 1s and 0s as required.

THE DETAILS

(Schematic sheet 10 of 12)

The nine Write Data channels, WDP, WD0-WD7, are supplied from the controller interface through connector J5, are inverted and applied to the D inputs of write buffer flip-flops N2, R2. The data is clocked into the buffer by Write Strobe WSTR, provided that SYNC/, supplied from the PE formatting section, is high. Note that SYNC/ is high only during actual data and is kept low during the preamble and postamble, keeping the write buffer cleared. Once the data is presented at the output of the write buffer it is applied to the data inputs of parity tree P2, and to one input of each of the exclusive-OR gates J3, H3. Either the external parity channel or the output of the parity tree P2 may be used to supply channel P to the transport, according to the placement of the jumper at H5-5.

TOGGLE, a square wave at 1600 cpi (3200 fri) frequency, supplied from the crystal oscillator dividing network, is gated with Write Zero WRTZ (supplied from the formatting section) through exclusive-OR gate J7-3, and through both OR gates R3-3 and R3-8 to the inputs of exclusive OR gates J3, R3. TOGGLE is used to reverse the data polarity in mid-cell, thus converting the data from logic level to phase encoded (as shown in timing diagram Figure 3-2). TOGGLE is also applied to multiplexer J4-14 where it phase encodes channel P data. The phase encoded data of the eight channel is then clocked through multiplexers H2 and J2 by Out Clock OCLK, and through open collector drivers H1, J1, provided that the formatting section supplies Output Enable true. The output drivers supply the data through connector J2 to the transport write amplifiers.

Note that when the preamble is written SYNC/ low keeps the write buffer cleared while TOGGLE generates the 3200 fri frequency on all channels to write the 40 preamble all-0 characters. When the preamble all-1 character is to be written, the formatting section supplies WRTZ high, inverting the phase of TOGGLE for a single character, thus generating the required polarity for the all-1 character. Similarly, WRTZ is kept high for a single character period right after the end of the data to write the all-1 character at the beginning of the postamble, and is then returned to a low state for writing the postamble all-0 characters.

File Mark Generation

When the file mark is to be written the microsequencer supplies Write File Mark WFM/ true. WFM/ low keeps the outputs of OR gates R3-6 and R3-8 low and flip-flop J8-1 cleared. This inhibits TOGGLE to all channels with the exception of channel 2, 6 and 7. TOGGLE, gated through OR gates R3-3 and P3-11, generates 3200 fri frequency on channel 2, 6 and 7 to write the burst of all-0 characters on these channels, as required for file mark generation.

Identity Burst Generation

When a write operation is initiated at BOT the microsequencer supplies IDENT/ true, setting OR gates R3-3 and R3-8 low, thus inhibiting the TOGGLE to eight of the nine channels. TOGGLE is gated through J7-6 to multiplexer J4-14, where it generates the Identification Burst on channel P. Note that during the ID burst mode the frequency of TOGGLE is halved by the crystal oscillator dividing network to generate the 1600 frpi frequency required for writing alternate 1s and 0s.

3.4.4 PHASE ENCODED WRITE PROGRAM

The PE write program controls the motion control of the transport, gap timing and command decoding for writing phase encoded data. The sequence of steps used in performing these functions is described in the following paragraphs. The microsequencer initially checks the status of the Load Point (LDP) line, initiating the writing of the ID burst if LDP is true and times out the Beginning of Tape (BOT) gap. If the transport is not at load point, a normal write routine is initiated. The microsequencer then sets PE Write Enable (PWEN) true, enabling the data and write strobe outputs; the program also sets Set Write Status SWS true and supplies Synchronous Forward Command SFC to the transport. The prerecord gap is timed out and once the transport is up to speed the START pulse is issued to the formatting circuits, initiating the writing of the preamble.

The write program also monitors the states of the Erase, Edit and Write File Mark lines, taking the required steps in each case: during the Erase mode PWEN is reset, disabling the write outputs; during Edit Overwrite OVW is set true; during Write File Mark the file mark gap is timed out and the file mark written by issuing WFM/ true.

Following the initiation of the write sequence the microsequencer program branches to the read subroutine in order to perform read-after-write. The read subroutine also controls the ramp-down and command termination sequence.

3.5 NRZI DATA GENERATION

3.5.1 INTRODUCTION

The NRZI write circuitry accepts data in the form of logic levels from the controller interface, generates the vertical parity and cyclic redundancy check character and passes the data to the transport. The NRZI formatting circuitry controls the write circuits and times out the check characters. The microsequencer supervises the entire operation, controlling the starting and ending of the data flow, and issues the necessary motion commands to the transport while satisfying all required interlocks.

3.5.2 NRZI FORMATTING

THE CONCEPT

Once the tape transport has advanced through the prerecord gap the microsequencer supplies a START pulse, indicating the beginning of the data block. START is supplied to the formatting circuits where it initiates Write Data Strobe Enable WDSEN, SYNC/ and Output Enable OUTEN all high, to enable the writing of the data on tape. The Last Word Indication, supplied from the controller or internally generated during self-terminating sequences, terminates the writing of the data and enables a check character timing register. The timing register supplies the timing for the writing of the CRC and the LRC characters.

THE DETAILS

(Schematic sheet 11 of 12)

Once the prerecord gap has been timed out under microsequencer control and the tape is up to speed, the microsequencer issues a START pulse one SEQCLK period wide. START is inverted by N5-12 and sets flip-flop N7-13, generating DONE/ false (high). The next Write Data Strobe WDS is gated noninverted through exclusive-OR gate J7-6 (since QA output of L6 is low at this time) and clocks flip-flop K7-5 to the set state. The Q/ output of the flip-flop activates NAND gate

N8-1 and the high output of the gate activates OR gate L7-11 to generate SYNC/ high, indicating the beginning of actual data. OR gates L7-11 and L7-6 are also activated to generate Write Data Strobe Enable WDSEN to NAND gate H4-10, gating WDS through to the transport at connector pin J2-29. SYNC/ is supplied to the write circuitry (schematic sheet 10 of 12) where it enables the input write buffer. The Q/ output of flip-flop K7-6 low also disables OR gate L7-8 (NODAT is high only during an erase command), L7-8 going low to disable NAND gate K8-6, generating Output Enable OUTEN high. OUTEN enables the write circuitry output drivers, allowing write data transmission to the tape transport. SYNC/, WDSEN and OUTEN remain in their high states during the data portion of the block, allowing write data to be accepted by the formatter and to be transferred to the tape transport. When the controller supplies Last Word LWD indication, signifying that the coincident data character is the last of the block, LWD high activates NOR gate N8-13 to set flip-flop N7-9. Alternately, during self terminating sequences, such as a fixed erase command, the microsequencer supplies LAST true at the end of the sequence to flip-flop M5-12, and the flip-flop is set on the following Write Strobe WSTB, its Q output also activating N8-13. In either case, when N8-13 goes low, it sets flip-flop N7-9, the Q output of the flip-flop going high to remove the direct clear from the check character timing register L6-9. Note that the Data A input of the register is set high at this time by the high output of flip-flop K7-5. Register L6 is clocked by WCLK/, a crystal generated clock at the NRZI data frequency. Following one data period the QA output of the register goes high, disabling NAND gate N8-1, thus terminating WDSEN and setting SYNC/ low. This inhibits the write strobes to the transport, and disables the reception of any more write data from the controller. After the next WCLK transition the QB output of the register goes high, is inverted by N5-8 to disable AND gate L5-8, inhibiting ERRCLK. ERRCLK is the Write Data Strobe WDS supplied to the CRC generator (see reference sheet 10 of 12) during the block to accumulate the CRC character. Following the block the CRC generator is shifted an extra time with all inputs equal to zero and is then locked when ERRCLK is disabled. On the fourth WCLK count following the end of data the QD output of register L6 goes high. For a single WCLK count the QD and QE outputs of the reister are going to be in opposite states, activating exclusive-OR gate L8-8. The high output of gate L8-8 activates NAND gate J6-12 for a single character period, generating Write Enable WEN/ true, and after being inverted by N5-10 and activating OR gates L7-11, L7-6, supplying WDSEN true for a single character period. WEN/ and WDSEN enable the writing of the CRC character on tape. On the eighth WCLK count the QH output of register L6 goes high, resetting flip-flop N7-14 through NOR gate N8-10. The output of flip-flop at N7-13 goes low to generate DONE/true, indicating the completion of the writing of the data block.

DONE/ low causes flip-flop K7-8 to clear, its Q/ output going high to activate OR gate L7-8 and NAND gate K8-6, generating Output Enable OUTEN low. OUTEN low is inverted twice (see reference sheet 10 of 12) and is then supplied as Write Amplifier Reset WARS/ to the transport write amplifiers for the writing of the LRC character on tape, eight character periods following the last data byte of the block.

3.3.5 NRZI WRITE CIRCUITRY

THE CONCEPT

Write data from the controller interface is inverted and clocked into a write buffer by Write Strobe WSTR provided that the formatting network supplies SYNC/ high. The outputs of the write buffer are supplied to a vertical parity generator, a Cyclic Redundancy Check Character (CRCC) generator, and to a set of 2-to-1 multiplexers clocked by Out Clock OCLK. During the data block write data is passed through the multiplexers and through a set of drivers enabled by Output Enable OUTEN to the transport write amplifiers. During the CRC period, four character counts following the last data byte of the block, the output of the CRCC generator is passed through the multiplexers to be written on tape. The Write File Mark WFM/ signal is used to write the tape mark on channels 3, 6 and 7.

THE DETAILS

(Schematic sheet 10 of 12)

Write Data Channel W0-W7 and WP are input at connector J5 from the controller interface to the inputs of D-type flip-flops N2, R2 on the leading edge of Write Strobe WSTR. The flip-flops are enabled only when SYNC/ (supplied from the formatting network) is high, indicating the presence of actual data. The data at the output of the write buffer flip-flops is supplied to vertical parity generator P2, to CRCC generator K2, and to one input of exclusive-OR gates J2, H2. Note that the derivation of the parity channel may be either internal or external, according to customer requirements, and is determined by the insertion/removal of the strap connected to pin 6 of P2. During the data portion of the block CRCC generator K2 is clocked by Error Clock ERRCLK, accumulating the CRC.

At this time Write Enable WEN/, supplied from the formatting network, is high. WEN/ high is supplied to the select lines of the multiplexers, gating the write data from the exclusive-OR gates through to open collector drivers H1, J1, which are enabled by Output Enable OUTEN. The data is output through connector J2 to the transport write amplifiers.

Following the end of the data block, the CRCC generator is shifted an additional time by ERRCLK with the data inputs to the generator held low by SYNC/ low. On the fourth character period following the last data byte of the block WEN/ is set low for a single character period by the formatting network. WEN/ low enables the outputs of the CRCC generator and switches the multiplexers, routing the outputs of the CRCC generator through to the output drivers, to write the CRCC on tape. Four character periods later the Output Enable line is set low by the formatting section, generating Write Amplifiers Reset WARS high to the transport, to write the LRC character on tape.

When a Write File Mark command is issued by the controller, the microsequencer controls the timing of the file mark gap, then issues Write File Mark WFM/true. WFM/ low and NRZI/ low activate NAND gate K5-1, which in turn activates OR gates P3-8, P3-11. The high outputs of these OR gates are gated through the exclusive-OR gates of channels 3, 6 and 7, writing a single 1 on these channels, as required for the NRZI file mark.

3.5.4 NRZI WRITE PROGRAM

During a write sequence, such as a write one block command, the microsequencer program performs the following steps: it loads the internal counter with the initial write gap count, sets Set Write Status SWS true, issues a Synchronous Forward Command SFC and times out the prerecord gap until the counter is decremented to zero. The microsequencer then issues Data Busy DBY true, indicating that data manipulation is under way. Next the microsequencer issues a START pulse to the write formatting circuit, indicating that data transmission from the controller to the formatter is about to begin. Finally the microsequencer issues NRZOUT true to enable the data outputs to the transport, and calls for the read subroutine in order to perform read-after-write. The read subroutine, described in paragraph 3.6.4, includes the instructions for timing out the ramp-down and the command termaination sequence.

The write program also includes steps to sample the BOT status, initiating the long BOT gap if tape is at load point. The Erase, Edit, Write File Mark command lines are also sampled. During an Erase command the microsequencer issues NODAT true, inhibiting the data outputs during erase operations. During Edit the microsequencer issues Overwrite OVW true. During Write File Mark the microsequencer issues WFM/ true and times out the long file mark gap.

3.6 NRZI DATA RECOVERY

3.6.1 INTRODUCTION

The NRZI data recovery operation is performed under microsequencer program control using hardware elements including nine read channels, a NRZI read timing network, a data accumulation network, and an LRC error detection network. The various circuits involved in data recovery will be described first, followed by a description of the control program that oversees their functioning.

3.6.2 NRZI READ TIMING NETWORK

THE CONCEPT

The NRZI timing network performs the following functions:

a. Generates the NRZI LOCK pulse coincidentally with the leading edge of each Read Data Strobe supplied from the transport. In the NRZI read mode the LOCK pulse is used to generate the shift-in pulse, transferring the data from the input latch of each read channel to the respective FIFO. LOCK is also used in accumulating the LRC count for each data channel.

b. Keeps track of whether the number of characters in the block is odd or even, generating CERR high if the number is odd, CERR low if the number is even. CERR, in conjunction with the CRCC parity, is sampled by the microsequencer to check for an error condition.

c. Generates Mark Clock MRKCLK, a delayed RDS pulse used to clock the file mark flip-flop when a tape mark is detected.

d. Times the NRZI gap, providing TOUT1 and TOUT2 timing outputs to the microsequencer to enable CRC character identification four character periods following the last data character of the block.

THE DETAILS

(Schematic sheet 1 of 12)

NRZI LOCK

Read Data Strobe RDS is a negative going pulse inversely proportional to tape speed that is supplied from the tape transport coincident with each read data byte. After being terminated and inverted RDS is clocked into the first of three flip-flops by DATACLK (a crystal derived 7.2 MHz frequency) provided that the microsequencer has enabled the read chain by supplying Read Gate RGATE high. For one DATACLK period (140 nsec) the output of the first flip-flop is high while the output of the second flip-flop of the chain (D-15) is low, setting both inputs to NOR gate L5-11 high. The output of the gate goes low for a single DATACLK period, until the next DATACLK transition sets the output of the second flip-flop high NOR gate F5-3 then outputs a low going pulse on the leading edge of each RDS. This pulse is gated through AND gate L5-11 by LOCKIN (always high during NRZI), and is supplied as LOCK to each of the nine read channels, where it is used to accumulate the LRC count for each track and generate the shift pulse, causing data to be shifted from the input latch into the FIFO.

Data Count CERR

The pulse formed on the leading edge of each Read Data Strobe RDS is inverted by E1-6 and gated through exclusive-OR gate F1-3 to CERR flip-flop B2-14. Initially the flip-flop is cleared, its output setting one input of the exclusive-OR gate low. The first positive going pulse is gated uninverted through the exclusive-OR gate and sets the flip-flop. The output of the flip-flop then goes high and stays high until the following RDS generated pulse this time inverted by the exclusive-OR gate, resets the flip-flop. The next RDS generated pulse sets the flip-flop once again, repeating the sequence. In short, the flip-flop will generate CERR high following an odd number of RDS pulses, and CERR low after an even number of RDS pulses. CERR is supplied to the micro-sequencer network where it is sampled in conjunction with the parity of the Cyclic Redundancy Check Character (CRCC). Following a block with an odd number of bytes, the CRCC parity should be even, and following a block with an even number of bytes the CRCC parity should be odd. If these conditions aren't met, the microsequencer flags an error condition.

Mark Clock MRCLK

RDS, after being clocked through all three flip-flops by DATACLK, is supplied as Mark Clock MRKCLK. MRKCLK clocks the file mark detect flip-flop (schematic sheet 6 of 12) to the set state whenever a file mark is detected.

NRZI Gap Timer

The NRZI gap timer consists of shift register F9, clocked by crystal derived frequency 2 x WCLK at twice the 800 cpi data rate. Read Data Strobe RDS, delayed by two DATACLK periods, output by inverter E1-12, is supplied to the data input of the shift register. During the block each negative going RDS pulse resets the shift register. Following the last data character of the block the shift register is not reset, and the high input is shifted into the register. After four 2 x WCLK pulse, or 2 character periods, the QD output of the shift register goes high to supply TOUT1 true. Two character periods later TOUT2 goes high. TOUT2 high is inverted by H5-8 to disable the serial input to the register. Two character periods after that TOUT1 is terminated, and two character periods later TOUT2 is terminated, as shown in timing diagram Figure 3-3. TOUT1 and TOUT2 are supplied to the microsequencing network where they are sampled during NRZI read operations in order to detect the end of data and to identify the NRZI check characters.

3.6.3 NRZI READ CHANNEL

THE CONCEPT

While the NRZI read channel utilizes a portion of the PE read channel, the functioning of the read channel in NRZI is considerably different, and simpler. The NRZI read uses the input latch, the ROM, the FIFO, and the delay shift register. Read Data from the transport is clocked by DATACLK into an input flip-flop, which presents it to one ROM address. LOCK, a pulse formed on the leading edge of each Read Data Strobe RDS supplied from the transport, is supplied to another ROM address. Each time LOCK is applied the ROM supplies a shift in SI pulse that clocks the data from the input flip-flop to the FIFO. The NRZI read timing is shown in Figure 3-4. When a data byte is present at the output of the nine FIFOs, the microsequencer samples RDY true and supplies nine RDCLK pulses, to clock the data from the output of the FIFO through the delay register to the controller interface.

Additionally the NRZI read channel uses the Error In Channel EIN line to accumulate the LRC error. Recall that the LRC check accumulates the number of 1s for each track, and that following the reading of the LRC character at the end of each block, the number of 1s for each

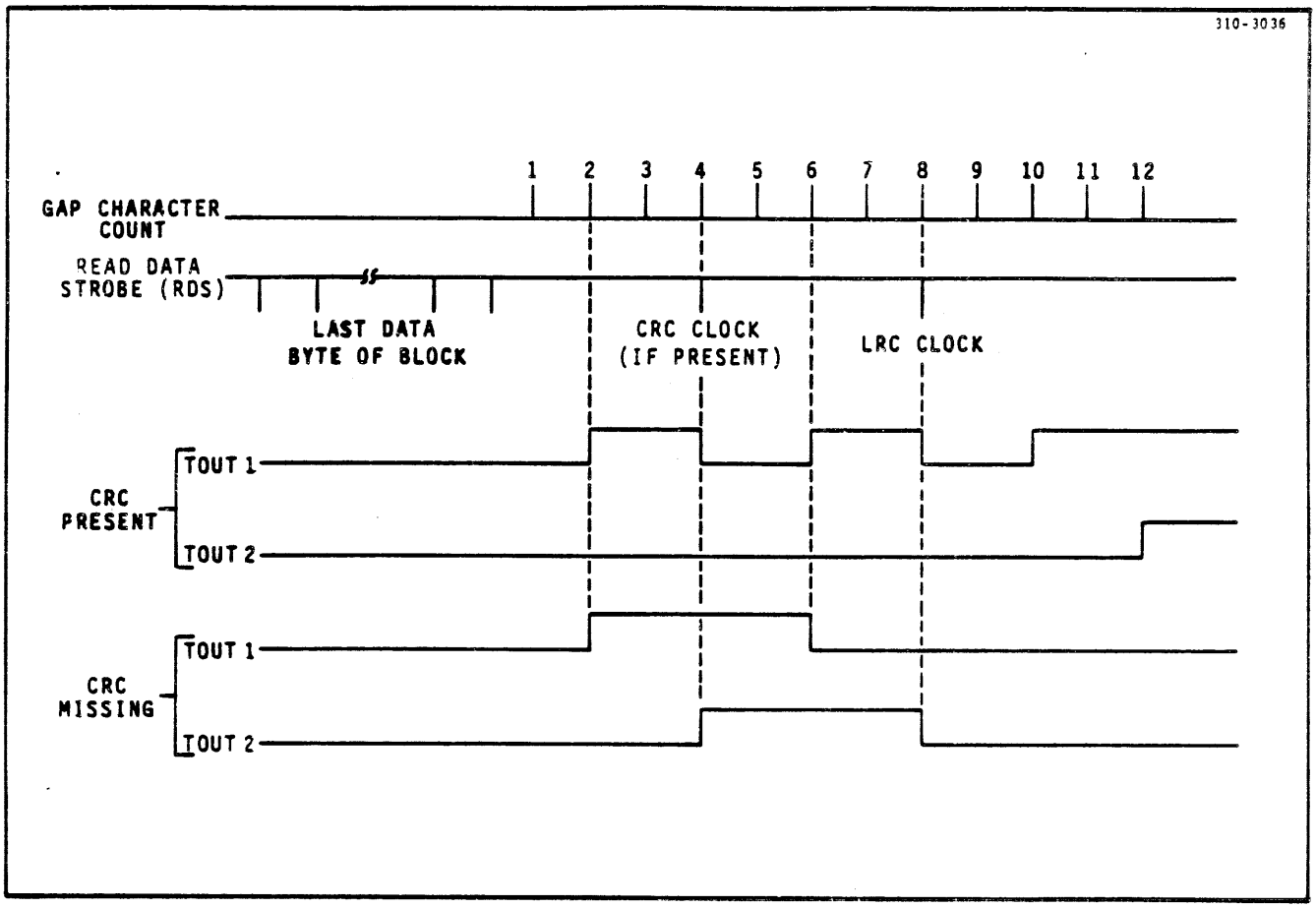


Figure 3-3. NRZ1 Read Gap Timing

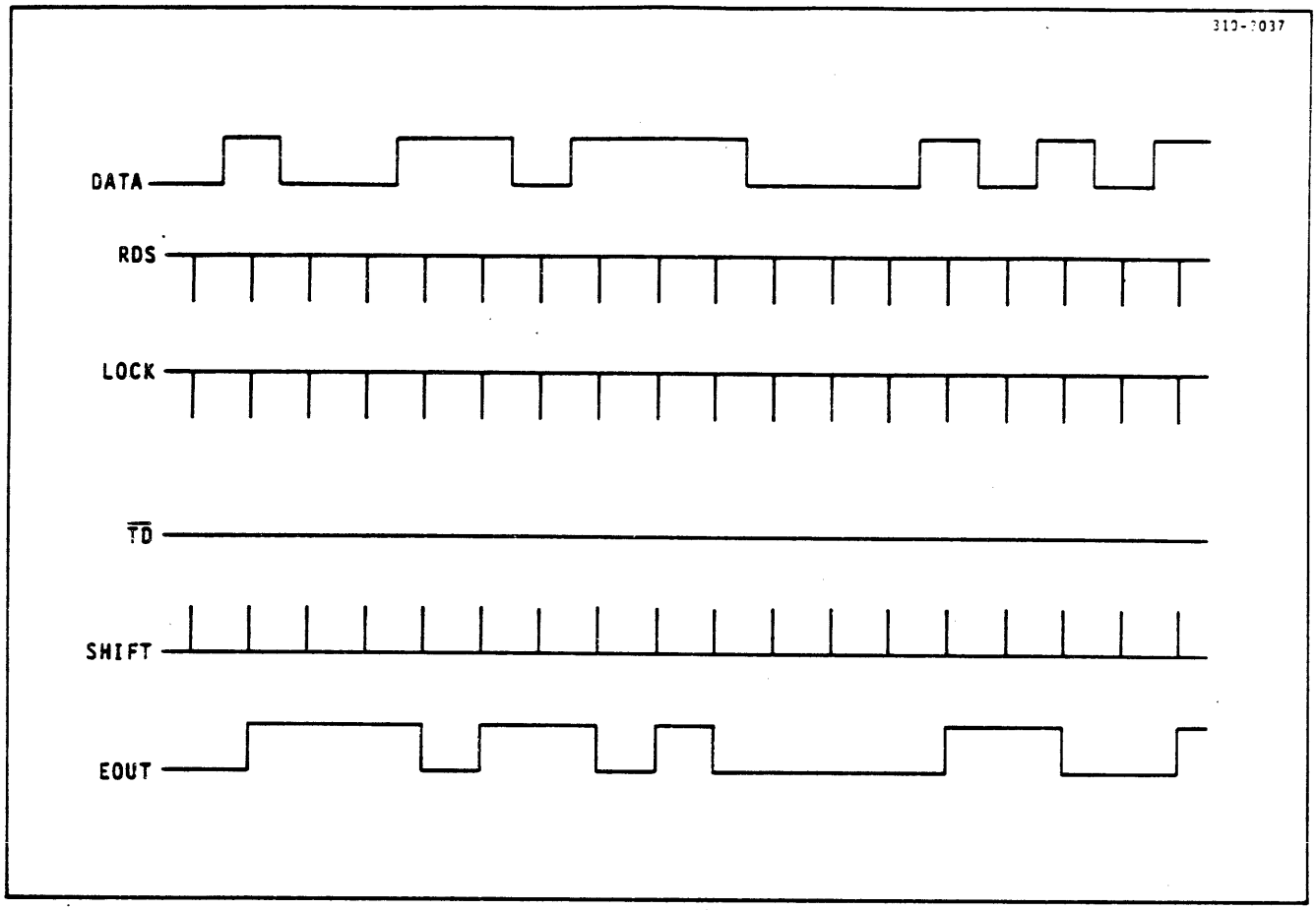


Figure 3-4. NRZ1 Read Timing

track should be even. Each time a 1 is detected in the channel, the EIN line reverses polarity and each time a 0 is detected EIN is unaffected. Following the reading of the LRC character the EIN lines of all channels should all be low, having reversed polarity an even number of times. If the EIN line of any channel is high following the block an LRC error indication is issued.

THE DETAILS

(Schematic sheet 2 of 12)

Since the nine read channels are practically identical, specific references will be made to channel 0 only (schematic sheet 2 of 12). It is up to the reader to translate IC numbers to the particular channel he is examining.

Channel 0 data is supplied from the transport read electronics at connector pin J2-5. The data is inverted once by E1-10 and is gated through exclusive gate D1-6 uninverted, since PEFWD is always low during NRZI operation. The data is then clocked into D type flip-flop D10-4 by DATACLK, a crystal generated 7.2 MHz frequency. The output of the flip-flop supplies the data to the input of First In First Out register D14. The data is also supplied to an address input of ROM D11. LOCK is supplied to another ROM address at D11-1. During NRZI operation LOCK is a pulse 1 DATACLK wide formed on the leading edge of Read Data Strobe supplied from the transport. Whenever LOCK is generated the ROM O3 output goes high and is clocked into flip-flop D10-11, which in turn supplies a Shift In input to FIFO D14-3. The data bit present at the output of flip-flop D10-5 is then shifted into the FIFO and bubbles to the output. When a data bit is present at the FIFO output, its Output Ready OR signal goes high at D14-14, and is buffered by D8-2 to supply Ready RDY true. The RDY lines of all nine channels are wire-OR'ed, consequently when RDY goes true it is an indication that all nine channels have bits ready to be output. The RDY line is supplied to the microsequencer where it is sampled regularly during the NRZI recovery routine. When RDY is high the microsequencer generates a series of nine Read Clocks RDCLK. The first RDCLK pulse clocks flip-flop D15-3 to the set state, supplying a high Shift Out input to the FIFO, shifting out the data character present at the FIFO outputs of all nine channels. On channel 0 the data is shifted into flip-flop D15-12. Once the data is shifted out of the FIFO, the Output Ready OR line goes low, resetting shift control flip-flop D15-1. OR remains low until the next bit becomes available at the FIFO output.

The output of data flip-flop D15-12 presents the data to the input of delay shift register D9-5. The next series of eight RDCLK pulses supplied by the microsequencer shifts the data through the delay register to the output. The data is gated through NAND gate C16 provided that the microsequencer supplies Enable Output ENOUT true, and is output to the controller interface at connector pin J1-2.

In addition to handling the data, the read channel also accumulates the LRC count for each track. Each time a LOCK pulse is applied to the ROM and the data input to the ROM is high, indicating a 1 bit is present, the ROM reverses the polarity of its O4 output at D11-13. The state of O4 is clocked into flip-flop D10-6 and is supplied as EIN0 to a plurality network (see schematic sheet 6 of 12). After the entire block has been read, including the LRC character, the state of EINP, EIN0-7 should be low, since each track should contain an even number of 1s. If any EIN line is high, an LRC error indication is issued.

3.6.4 NRZI READ PROGRAM

When the NRZI, Forward and Read, status lines are all true the mapping ROM directs the program controller to the NRZI forward routine. This routine enables the read chain outputs by issuing NRZOUT true, and samples the transport Load Point status. If the tape is found to be at load point a beginning of tape read routine is entered, in which a data search is conducted on channel P. If data is found an ID burst indication is supplied to the controller, signifying that the

; then up to the controller to select the correct data density, t. The internal counter of the program controller is then loaded Synchronous Forward Command is issued and the prerecord gap is . counter is decremented to zero Data Busy DBY is set true, to speed and data recovery is underway. The read chain is then Gate RGATE and Read Enable RDEN lines and the program enters tine. During NRZI data recovery the LOCK pulse, generated by ifts the input read data into each read channel FIFO. The tate of RDY, the wire-OR'ed output of the nine FIFOs. If a t of all FIFOs the data extraction subroutine is entered, in which he FIFO and through the delay register, the byte vertical parity is generated for the character. This subroutine is repeated as long hen the NRZI gap timer supplies TOUT1 high, indicating that two without encountering a Read Data Strobe, the NRZI read program CCG true and searches for the CRC character by sampling the the gap timer (see Figure 3-3). If a CRC character is not found ie File Mark status line. If a file mark is recognized no Read is generated for a file mark. If the file mark status is false then a Read Strobe is generated by the microsequencer. The parity of onjunction with the accumulated data count of the block (CERR) ut if the required conditions are not met (odd CRCC parity for vice versa). The next subroutine samples the state of LRCERR cation if an LRC error was detected. The file mark status line is ndication is supplied to the interface if a file mark was detected.

very the post record gap count is loaded into the internal counter d. In this routine the Check Character Gate CCG line is reset, ed to clear the BUSY flip-flop and Data Busy DBY is reset to next command. While the program samples the BUSY signal t command, the actual ramp down is being counted as the internal new command is issued, the ramp down is completed and the to the all-0 wait state. If a new command is received before rogram verifies the validity of the new command by checking the of motion of the new command to be consistent with those of the mand is found valid the program controller jumps to the mapping the new command. If the new command is invalid, ramp down is returned to the all-0 state.

ECOVERY

ng a single phase locking oscillator, nine parallel read channels, a k and the PE recovery program of the microsequencer. The phase f the data channels and provides the nine read channels with the decoding. The read channels, in addition to decoding the data, track errors and perform single track error correction. The data number of valid channels, inhibiting data recovery unless eight of data. Overall control of the read recovery is implemented by the the required motion commands to the transport, checks the les the required timing for the read recovery sequence. These ollowing paragraphs.

3.7.2 PHASE LOCKING OSCILLATOR

THE CONCEPT

The Phase Locking Oscillator (PLO) generates DATACLK, a frequency at 32 times the input data rate, used to synchronize the data recovery functions. This frequency is derived using a voltage controlled oscillator (VCO) whose center frequency is 32 times the data rate. The VCO output is divided by 32 and its phase is compared with the phase of a reference read channel (either channel 2 or channel P) during the data, and a crystal derived reference frequency WSTB/ during the gaps. The output of the phase comparator is supplied to an integrating operational amplifier whose output current is translated to the corrective voltage supplied to the VCO. If the reference channel and the VCO output are in phase, no change in the VCO corrective voltage will occur. If the VCO phase lags the phase of the reference channel, the op amp will provide increased output current which will increase the corrective voltage to the VCO until the phase lag is corrected. Similarly, if the VCO phase leads that of the input data, the operational amplifier will cause a reduced corrective voltage to be supplied to the VCO until the oscillator slows down enough to match the input reference phase.

THE DETAILS

Voltage Controlled Oscillator

(reference sheet 6 of 12)

The main component of the tracking oscillator is voltage controlled multivibrator F12. The multivibrator center frequency is determined by the state of the HI-LO/ line (note that during PE operation only two transport speeds can be selected). During high speed operation HI-LO/ is high, selecting timing capacitor C5, resistor R9, and potentiometer R12 through CMOS switch H12. During low speed operaiton HI-LO/ is low, selecting capacitor C6, resistor R10 and potentiometer R11. With the summing comparator input disconnected (jumper removed between the op amp H11 and resistor R13) the center frequency of the oscillator, determined by measuring Reference Clock REFCLK at R4-11, is adjusted using potentiometer R12 for high speed operation and R11 for low speed oepration. The potentiometers control the emitter current of transistor Q1, thus the voltage across R14, which converts the current to an error voltage supplied to the VCO at F12-2. The center frequency is adjusted for optimal data rate at the factory and the jumper is reaplaced. The resulting oscillator output, DATACLK, is a frequency at 32 times the data rate.

DATACLK is supplied to a dividing network consisting of D type flip-flop H6 and four bit counter R4 in tandem. The frequency is divided by 4 to supply 1/8C, at 8 times the data rate, and divided by 32 to supply the data rate frequency REFCLK as one input to the phase comparator.

Reference Frequency Selection

The reference input of the phase comparator accepts one of three frequencies, WSTB/, DETP/, or DET2/, depending on the status of Write Select WSEL/, and on the status of the dropout flip-flop F2. During the interrecord gap the microsequencer supplies WSEL/ true to 4-to-1 multiplexer H7, routing the crystal derived data rate frequency WSTB/ through to the phase locking oscillator, to maintain the oscillation at the reference data frequency. Once the transport is up to speed and data has been detected, the microsequencer sets WSEL/ high, switching the reference input from WSTB/ to either DET2/ or DETP/, in accordance with the status of dropout flip-flop F2. If a dropout has been detected on channel P, DROPP high would set F2-1 low and would select DET2/ as the reference frequency; DROP2 high would similarly select DETP/ as the reference frequency. When neither channel has a dropout the first of the two channels to detect data is selected as the reference frequency.

The Phase Comparator

The phase comparator consists of 2 D flip-flops on H8, and associated gating. The reference frequency is supplied to the clock input of the upper H7 flip-flop. The output of the VCO is divided by 32 and supplied to the clock input of the lower H7 flip-flop. If the VCO output frequency and the reference channel are in phase, both flip-flops are toggled to the set state simultaneously and are immediately reset following a propogation delay by NAND gate H9-6.

When both flip-flops are reset, the Q output of the upper flip-flop sets the output of NAND gate H9-3 high, the Q output of the lower flip-flop sets the output of H9-8 low. Consequently the voltage divider network including resistors R5, R6, R4 and R7 provides about 6 volts at the summing point of the operational amplifier H11. The noninverting input is supplied with 6.2 volts. In this case the output of the op amp supplies minimum current to summing transistor Q1 and no correction voltage change occurs across load resistor R14.

When the phase of the VCO output leads that of the reference channel, the lower H8 flip-flop is set first, causing the output of NAND gate H9-8 to swing high for the duratio of the phase dealy and supplying 12 volts across the resistors at the inverting input of the op amp. This increases the positive feedback current of the op amp and reduces the output current to summing transistor Q1. As a result, the corrective voltage of the VCO is reduced until the output frequency slows down sufficiently for the phases to match. When the VCO output lags the reference channel, the upper D flip-flop will be set first and the output of NAND gates H9-3, H9-8 will be grounded for the duration of the phase delay. This will produce a negative feedback current, increasing the positive output current to summing transistor Q1. As a result the corrective voltage to the VCO will be increased until the VCO frequency speeds up sufficiently for the phases to match.

3.7.3 DROPOUT RESYNCHRONIZATION

THE CONCEPT

Either channel P or channel 2 are used as the reference channels for the tracking oscillator. Should a dropout occur in the reference channel, tracking is automatically switched to the alternate channel. Since a phase difference may exist between the tracking channel and its alternate due to skew, there may be a gap during the switching which could be interpreted by the phase comparator as a drastic slow down or speed up of data, and synchronization could be lost during the attempted correction. This condition is averted by a dropout detection network that preloads the VCO dividing network during the switchover, thus maintaining synchronization of tracking.

THE DETAILS

(reference sheet 6 of 12)

DROPP and DROP2 are connected to a flip-flop consisting of two segments of F2. Normally, when both channels are read properly, the flip-flop output at F2-1 would be low, causing DET2/ to be selected by multiplexer H7. When a dropout occurs on channel 2, DROP2 high clears flip-flop F2-1, and the high output of the flip-flop causes multiplexer H7 to switch the reference input from DET2/ to DETP/. For one DATACLK period the inputs to exclusive OR gate J7-11 would be opposite in polarity, generating a positive pulse. This pulse, indicating a switch over in tracking channels, clocks J-K flip-flop K7 to set state. The Q/ output of the flip-flop preloads the tracking oscillator dividing network (R4, H6) to maximum count minus one. The switchover pulse output by exclusive OR J7-11 is also inverted by NOR gate K5-4 and is supplied as Correct CORR to NAND gate F10-6. The gate is enabled only when LOCK/ is high, indicating that phase locking has been achieved. The output of F10-6 goes low and direct clears both phase

comparator flip-flops H8, preventing excessive correction voltage from drastically altering the tracking oscillator frequency during the switchover in tracking channels.

3.7.4 DATA DECODING, DESKEWING AND SINGLE TRACK ERROR DETECTION

THE CONCEPT

Read data from the transport read amplifiers is supplied to nine parallel decoding channels, each consisting of a latch, a ROM, and a state counter. Using the counter outputs and the LOCK signal, the ROM distinguishes between data transitions and interphase transitions, and determines whether the data transitions occur within the required time frame. The ROM supplies three latched outputs: Shift In (SI), Error In Channel (EIN), and Transition Detect (TDET). SI is used to shift the data and EIN from the latch output into the deskew FIFO register. EIN is generated each time a data transition does not meet the required timing criteria. TDET, issued each time a data transition is detected, resets the state counter. The PE read timing relationships are shown in Figure 3-5. Since channels 2 and P are used as reference inputs to the phase locking oscillator, the two channels are also equipped with early dropout detection networks to allow for immediate switching in reference channels.

The deskew register of each channel consists of a First In First Out (FIFO) register and associated logic. Data from the decoding latch and Error In Channel EIN are entered into parallel inputs of the deskew register each time the ROM supplies SI true. SI is generated only for actual data transitions, not for interphase transitions. When a data bit is shifted into the input of the deskew register, it bubbles to the register output. Data is kept at the output of each deskew register until all channels have bit at the respective FIFO output, at which point the wire-OR'ed Output Ready OR signals of all nine deskew register generate Ready RDY true. RDY is supplied to the microsequencer network which returns Read Clock RDCLK that shifts the data from the deskew FIFOs to a set of eight bit delay registers. The actual data alignment is accomplished using the all-1 character at the end of the preamble. When a particular channel detects a 1 bit during the preamble, that bit is stored at the output of the channel deskew FIFO until all channels contain a 1 bit at their respective FIFO outputs. At this point the microsequencer supplies a RDCLK pulse that generates a Shift Out signal to all the FIFOs simultaneously, shifting the deskewed data from the FIFOs to the output delay registers. The delay registers are eight bit shift registers, also clocked by RDCLK, that provide sufficient data storage to allow for postamble recognition. After eight RDCLK periods the data output by the FIFOs is presented at the delay registers outputs to the controller interface, accompanied by the Read data Strobe supplied by the microsequencer.

THE DETAILS

(Schematic sheet 1 of 12)

Early Dropout Detection

As mentioned previously, only channels 2 and P are equipped with the early dropout detection networks, since these channels are used as references for the phase lock loop. Since the dropout detection networks are identical for the two channels, only channel P will be described in detail and it is up to the reader to translate IC numbers if he is working on channel 2.

Channel P read data is supplied from the transport read amplifiers at connector pin J2-3. The data is inverted twice in the forward mode (only once in the reverse mode, since PEFWD is low) and is supplied to the early dropout detection network consisting of eight bit shift register F3, multiplexer F4, exclusive OR gate F1-6 and NAND gate F2-4. The incoming data is shifted through F3 by DATACLK at 32 times the data rate, providing a quarter of a character delay.

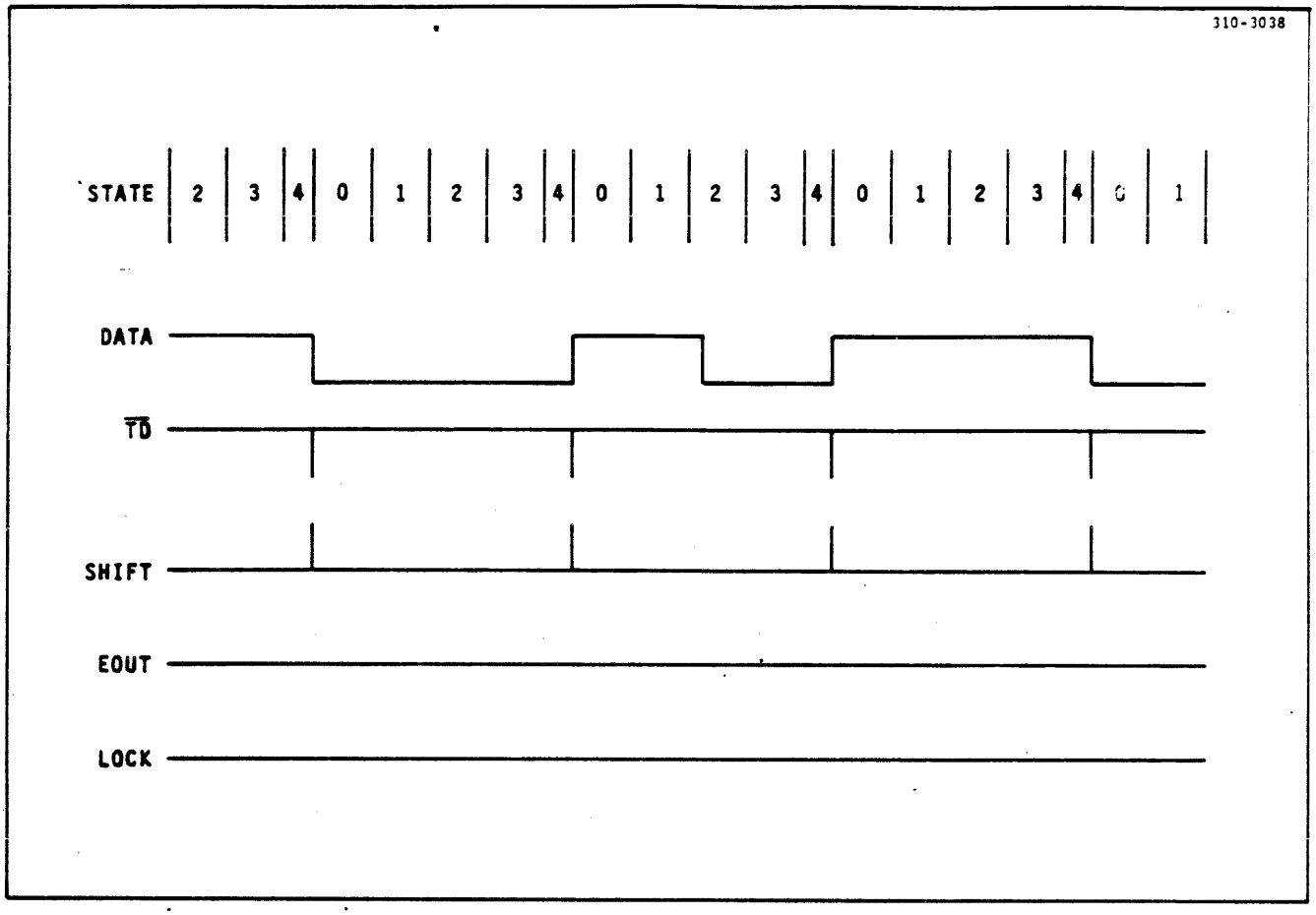


Figure 3-5. PE Read Timing

The delayed data is then passed through multiplexer F4 to latch E2-4. One DATACLK period later the data is clocked into a second latch output at E2-2, and is supplied to one input of exclusive-OR gate F1. The incoming data is presented to the second input of gate F1. As long as the incoming and delayed data are in the same state the output of F1-6 stays low, enabling one input of NAND gate F2-6. The gate is activated by state counter output E4-2 if one and a quarter character periods elapse without change in the state of the incoming data. In this case NAND gate F2-4 output goes high to generate DROP high, supplied to the phase locking oscillator (see schematic sheet 6 of 12) where it is used to switch tracking from channel P to channel 2. Note that in all channels except P and 2 the incoming data from the transport is supplied directly to the latch after being inverted and gated through the exclusive-OR gate.

Read Decoding and Error Detection

(Schematic sheet 1 of 12)

Since the read decoding networks of the nine channels are nearly identical, only channel P will be described in detail, and it is up to the reader to translate specific IC numbers to the particular channel under examination. The Channel P decoding network consists of a hex D flip-flop latch (E2), a ROM (E3), and a six bit state counter (E4, E5). As mentioned above, the channel P data is supplied to one latch input at E2-4. One DATACLK pulse later the read data is supplied to a ROM address input (at E3-5) and to another latch input (E2-3). The second latch supplies the data to another ROM address input (at E3-6) following a 1 DATACLK delay. The two latch outputs are in the same state when no transition has occurred, and are in the opposite states for 1 DATACLK period following each transition. The counter, also clocked by DATACLK, supplies the ROM with the count reference necessary to identify the time of occurrence of each data transition. This is accomplished by dividing each character frame into six states. Five of the states are a quarter of a character frame wide, and the sixth is one DATACLK period wide. When a transition occurs, the ROM identifies the transition as either valid data, an interphase transition, or an error transition, according to the time of its occurrence. Interphase transitions occur in states 2 and 3, between 25% and 75% of the character frame. Error transitions are defined as transitions occurring too early (during state one, or within 25% of a character frame since the last data transition), or too late (when no transition is detected within 125% of a character frame since the last data transition). Valid data transitions occur in states 4 and 5, between 75% and 125% of a character frame since the last data transition. The state counter supplies three of the address inputs to the ROM, at E3-3, 4 and 7. LOCK is another ROM input. During PE operation LOCK is set high at the beginning of each read operation by the microsequencer. During LOCK high the ROM identifies only zeros (negative going transitions) as data, and positive going transitions are identified as interphase transitions. Thus the ROM locks unto the data during LOCK high, distinguishing data transitions from interphase transitions. During LOCK high no data is shifted into the deskew shift registers.

The ROM provides three latched outputs:

a. Transition Detected TDET, output at E2-11 and latched at E2-12. This output is used to reset the counter following each data transition.

b. Error In Channel EIN, generated when an error is detected in the transition timing.

c. Shift In SI, generated when a data character and a possible error indication are to be shifted into the deskew shift register.

Note that the Transition Detected signal is used only to reset the counter after data transition and not after interphase transitions. The latched EIN channel is supplied to the deskew register as well as to a plurality network used to develop the data envelope (see schematic sheet 6 of 12).

The Deskew Register, Delay Register and Single Track Error Correction

(Schematic sheet 1 of 12)

The deskew register of channel P consists of FIFO E6 and related logic. When the decoding ROM generates a Shift In SI input at E6-3, read data from the decoding latch (E2-5) and the latched error indication EINP (E2-7) are shifted in parallel into the first register location. Once a bit is input into the register it bubbles to the output of the register and remains there until it is shifted out by Shift Out SO signal from the deskew control flip-flop E7-5. The Shift Out SO signal is generated as follows. When a data bit is present at the FIFO output, the Output Ready status of the FIFO goes true (E6-14). Output Ready buffered by E8-12 becomes the Ready (RDY) signal. The RDY outputs of all nine channels are wire-ANDed, and consequently will not become true until all nine channels present RDY true, indicating that all have bits at the outputs of their FIFOs. The RDY signal is supplied to the microsequencer network, where it is sampled during the PE read recovery subroutine. When the microsequencer senses RDY true it generates a Read Clock (RDCLK). RDCLK will toggle the deskew control flip-flop of all nine channels simultaneously, shifting the data byte out of the deskew FIFO. The data bit of channel P, in particular, is shifted from the FIFO output into data flip-flop E7-12. If the decoded bit is a one, the Q output of the flip-flop will go high, generating DET1 true. Conversely the Q/ output will go high if the decoded bit is a zero, generating DET0 true. Note that the DET1 lines of all nine channels are wire-ANDed, as are the DET0 lines of all channels. Consequently DET1 will go true only during an all-1 byte and DET0 will go true only during an all-0 byte.

The actual alignment (deskewing) of data is accomplished by using the all-1 character at the end of the preamble. When channel P, for instance, detects its first 1 bit, the output of flip-flop E7-9 will go high, enabling NAND gate F6-4. Assuming no error is detected, the error output of the FIFO (E6-13) will be low, setting NAND gate F5-11 high, consequently enabling F6-5.

The Enable Synchronization (ENSYNC) line, supplied from the microsequencer, is set high during the beginning of the preamble. NAND gate F6-6 is then activated, and its low output prevents flip-flop E7 from being toggled. Thus E7-5 does not generate a Shift Out pulse and the 1 bit is retained at the output of the FIFO. When all channels contain a 1 bit at their outputs DET1 goes high, is sampled by the microsequencer which in turn sets ENSYNC low. The output of F6-6 goes high and the next Read Clock RDCLK pulse will toggle E7-3. The flip-flop then generates a Shift Out pulse and the first deskewed data byte is shifted from the outputs of all nine FIFOs.

Data from the Q2 output of the FIFO is passed through flip-flop E7-9 to the D1 input of eight-bit delay register E9. The delay register is also clocked by RDCLK, supplied from the microsequencer network each time a byte is ready to be shifted out. The eight character delay provided by the register ensures valid postamble recognition, requiring an all-1 character to be followed by eight all-0 characters before the postamble is recognized.

As mentioned above, both a data bit and an error indication are shifted through the FIFO. In the case of a mistimed data transition, Error In Channel P EINP goes high and is shifted along with the data to the FIFO output. The Q0 (E6-13) output of the FIFO goes high, activating NAND gate F5-11. The output of the gate goes low and sets both outputs of data flip-flop E7 high. This prevents a single track error from disrupting the data recovery sequence. In addition, the Select input of the delay shift register is set low (at E9-13) and causes Parity Correct PARCOR, the parity derived from the other eight channels, to be substituted for the erroneous data and shifted through the delay register to the output. The data output by the delay register is gated through F10-8, provided that the microsequencer supplies Enable Output ENOUT high and is supplied to the interface at connector J1.

3.7.5 DATA ENVELOPE DETECTION

THE CONCEPT

The Error In Channel indications EINP-EIN7, output by the read stage ROMs, are supplied to a plurality network that determines, in case of an error, whether it is a single track error or a multiple track error. If a single track error is detected, the plurality network supplies a Single Error SER true to the microsequencer, which in turns supplies a Correctable Error CER indication to the interface. If a multiple track eror is detected the microsequencer supplies a Hard Error HER status to the interface, indicating that the error cannot be corrected.

The output of the plurality network is also used to reset the LOCK signal, used by the nine read channels to lock unto data transitions during the beginning of the preamble. The LOCK signal is reset after eight valid preamble characters are encountered. Additionally, the plurality network is used to recognize the PE file mark. When the Error In Channel signals of channels 2, 6 and 7 are false while those of the remaining channels are true, the plurality network supplies a file mark indication to the microsequencer.

THE DETAILS

(Schematic sheet 6 of 12)

The error indications output by the nine read channels are supplied to a plurality network consisting of ROM F7 and associated gating. EIN0, EIN1 and EIN3 through 7 are supplied to the ROM address inputs, while EINP and EIN2 are supplied to a gating network which complements the ROM functions. If a maximum of one error is detected, the output of NOR gate F5-6 goes high, generating Envelope ENV true. ENV true indicates that at least eight of the nine channels contain valid data, enabling data recovery. ENV is supplied to the microsequencer network where it is sampled continuously during the data recovery sequence. Whenever ENV goes low, indicating that two or more channels are in error, the microsequencer enters an error subroutine and issues a Hard Error HER indication to the controlelr interface. Another source of HER is the output of parity tree F8. When even parity is detected for a particular byte F8-5 goes high, supplying a high input to shift register E9. Eight data periods later (the delay is provided to match the data delay) the output of E9 goes high, activating OR gate J5-3 and supplying Hard Error HER true. Note that the output of the parity tree is also supplied, after being inverted by E12-11, as Parity Correct PARCOR to each of the nine read channels. PARCOR is used to replace the data of an erroneous channel during a single track error.

When the plurality network including F7 detects a single track error OR gate J5-11 is activated, supplying Single Error SER true to the microsequencer. The microsequencer then issues a Correctable Error CER indication to the controller, signifying a single channel error. The erroneous channel, in the meantime, replaces its data with Parity Correct PARCOR.

LOCK Generation

At the beginning of the PE data recovery sequence the microprocessor sets Lock Enable LOCKEN high. LOCKEN high clears the flip-flop consisting of two K5 NOR gates, generating LOCKIN high, LOCK/ low. LOCKIN becomes the LOCK signal during PE operation (see schematic sheet 1 of 12) and is supplied to the nine read channel stages. During LOCK high only zero data transitions are recognized by the read stage ROMs, allowing the read circuits to lock unto the data transitions while ignoring the interphase transitions. At the beginning of the read recovery sequence the microsequencer supplies WSEL/ high to the data input of shift register K6. When the plurality network supplies ENV high, indicating that valid preamble characters are being read, ENV high removes the direct clear from shift register K6 and K6 starts shifting the high input level through. The QH output of the register goes high after eight consecutive valid

preamble characters are read, setting K5-12 high and supplying LOCKIN low. LOCKIN low removes the LOCK signal from the read channel inputs, allowing all data transitions to be processed.

File Mark Detection

ROM F7 is programmed to recognize the PE file mark when channels 2, 6 and 7 are valid while the remaining channels are quiescent. When a byte meets these criteria F7-11 goes high, generating FMKDET true. FMKDET true is supplied to the microsequencer, which in turn supplies the file mark indication to the controller interface.

3.7.6 PE READ PROGRAM

The PE read program oversees the motion control, gap timing, read decoding, error detection and read strobe generation for recovering phase encoded read data. Initially the program sets the PEOUT and FEFWD status lines, enabling the PE read section and the read data outputs. Next the read chain is initialized by setting then resetting Read Enable RDEN/, and Read Gate RGATE. In addition WSEL/ is reset to route WCLK to the PLO network. The microsequencer then samples the load point status line supplied from the tape transport. If the tape is at load point, a beginning of tape subroutine is entered in which channel P is checked for the Identification Burst. If the ID burst is found, it is so indicated on the CCG line, and the PE read routine is continued. If no ID burst is found, it is up to the controller to select the proper density. Assuming a PE read operation, a Synchrounous Forward Command SFC is issued and the microsequencer starts searching for data. The search for data consists of sampling the Data Detect lines of channels 2 and P. If data is detected on either channel for four consecutive character periods it is assumed that a valid data block has been found and a read recovery subroutine is entered. If less than four valid data characters are found the search for data is continued.

The read recovery subroutine begins by setting LOCK high. LOCK is supplied to the ROM of each read channel, instructing the ROM to recognize only zeros as data transitions and to ignore the interphase transitions. It is during LOCK high that the read channels lock on data transitions as opposed to interphase transitions. Next the program sets WSEL/ high, routing Data Detect 2 (or P) to the reference input of the phase locking oscillator, replacing the crystal derived WSTB/. The program then calls for the data read routine which samples the Ready RDY line of the FIFOs. When a data character is present at the output of all channel (or at least eight out of nine) the microsequencer generates Read Clock RCLK, clocking the byte from the deskew FIFOs outputs to the delay buffers. DET0, the wire-ORed Detect 0 outputs of all nine channels is sampled; if it is false a formatting error is flagged, and if it is true, as should be the case during the preamble, the read recovery is continued. After a sufficient number of all-0 characters has been detected to confirm the presence of the preamble, the microsequencer begins the search for the all-1 character that signifies the end of the preamble. At this time the microsequencer issues Enable Sync ENSYNC high. ENSYNC high retains any one bits present at the outputs of the FIFOs until all channels have a one bit present at their respective outputs. When this happens DET1 goes high and ENSYNC is reset to allow the data character to be shifted from the FIFO outputs to the delay buffers of the nine read channels. This aligns the data, compensating for any delays between the tracks due to head scatter or any other factors. Each time a byte is shifted from the FIFOs the microsequencer generates a read strobe RSTR of the required duration, to be supplied to the interface. The data is continually processed, with a continuous check for errors, until the DET1 signal goes high again, at which point the microsequencer samples the DET0 line in search of the postamble. If the DET0 line stays true for 16 consecutive characters, a postamble is recognized. If a non zero character is then detected the microsequencer flags a formatting error. Once the postamble detection is complete the microsequencer enters the gap detect subroutine. In this routine WSEL/ is set low to route WSTB/ as the PLO reference and Data Detect lines DDETP and DDET1 are sampled alternately.

If no data is detected on both channels for four consecutive character periods a gap is assumed and the internal counter is loaded with the ramp down count and the command completion subroutine is entered. In this subroutine the post-record gap is timed out as the BUSY/ line is sampled in search of a new command. The original motion commands are reset and the ramp down begins. If a new command is received during this period, the microsequencer checks whether the direction and read/write status of the new command are consistent with those of the previous command. If they are consistent, the new command is accepted on the fly, without the tape having to stop. If the new command is not consistent with the previously issued command, the ramp down is completed and the tape has to come to a complete stop with the microsequencer entering the zero wait state prior to the acceptance of a new command.

3.8 INTERFACE SECTION

THE CONCEPT

This section includes the input command latch that stores controller commands supplied to the formatter, and the output drivers that return formatter status lines to the controller interface. This section also includes the output drivers that supply formatter commands to the tape transport and the status lines returned from the transport to the formatter. Also included in this section are the formatter address circuit and the speed selection circuits that match the formatter clocks with the tape speed of each of the selected transports. The Power On Reset POR is also described in this section.

THE DETAILS

(Schematic sheet 12 of 12)

Controller Command Latch

Interface commands are supplied through connector J5 to the D inputs of octal D-latch device M2, with the exception of the Rewind REW and Off Line comamnds, which are routed directly through output drivers to the transport. A command is latched when BUSY/ goes true following a GO pulse. GO, supplied from the interface at J5-8, is gated through J6-6, provided that two interlocks are satisfied:

a. No Reverse command is issued at load point.

b. No write command is issued when the transport supplies File Protect (FPT) true, indicating that the write enable ring is missing from the reel of tape presently mounted.

If these conditions are satisfied GO is gated through J6-6 and sets flip-flops N3-3 and N3-11, generating BUSY true and Formatter Busy FBSY true. BUSY/ low is supplied to latch M2 to lock the command at the output of M2 until BUSY/ goes false again. FBSY is inverted and returned to the controller to indicate that the formatter has accepted a command, and that no new command should be issued until the present operation has been completed. At the completion of the operation the microsequencer clears the BUSY flip-flop by issuing Command Clear CCLR/, enabling the acceptance of the next command on the fly, provided that the new command is consistent in direction and write status with the previous command. If no new comamnd is received the microsequencer issues END/ true, clearing the Formatter Busy line.

Formatter and Transport Addressing, Speed Selection

Two formatter addresses are available, depending on the status of the Formatter Address line FADS, supplied by the controller. The address of the particular formatter is determined by the insertion/removal of the jumper between the input of exclusive-OR gate L8-13 and ground. With the jumper in the formatter is addressed when the FADS line is high; with the jumper out the formatter is addressed when the FADS line is low.

high = 3V · FAD false = 0
low = 0V FAD true = 1.

The transport address is determined by the status of the TAD0, TAD1 lines supplied from the controller. These lines are supplied to demultiplexer K3 and select one of four transports, provided that the formatter is addressed. Transport speeds are selectable by switches K14, N14 (see Table 2-5). In NRZI operation each of the selected transports may be assigned a different speed, selected by lines SPD0-SPD2. In PE operation only two speeds may be used, as assigned by the HI/LO/ line.

Power On Reset

When power is initially supplied to the formatter, the input to inverter M1-13 stays low until capacitor C12 charges up sufficiently. During this period the inverter output is high and activates NAND gate L3-3, setting the input to L3-11 low and generating Power On Reset POR high. POR high initializes the microsequencer network by forcing the program controller to program step 0 (schematic sheet 7 of 12). POR is kept true until the controller addresses the particular formatter, supplying FADS/ true, the formatter is enabled by Formatter Enable FEN/ ture, and the selected tape transport is ready, supplying Unit Ready URDY true. When these conditions are satisfied the Y3 output of 2 to 4 demultiplexer K3-3 is set low, setting the output of NAND gate L3-8 high and POR low.

POR true is also generated when a Synchronous Reverse Command SRC is issued while the tape is at load point, calling for the unloading of the reel of tape. In this case LDP and SRC true activate NAND gate L3-6, grounding the input to L3-12 and issuing POR true.

Interface Drivers

Most of the formatter status lines returned to the controller are simply inverted and output by a set of open collector drivers through connector J1. The exceptions are the Hard Error HER line, which is gated with Correctable Error CER/, and Read Strobe and Correctable Error, which in PE are gated with the TMOUT2 output of the external timer. TMOUT2 provides the eight character delay required to match the data delay during PE operation. The controller outputs to the transports are gated with Formatter Address FADS before they are supplied to the transports through connector J3. The formatter initiated commands to the transports including SFC, SWS, SRC, are simply inverted before being output through connector J3.

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 INTRODUCTION

Since the 9X00 Formatter consists of a single PC board, there are no mechanical adjustments or maintenance to be performed. The only electrical adjustment provided is the adjustment of the Phase Locking Oscillator (PLO) center frequencies for PE read. The PLO adjustment procedure is described below. This section also includes the description of the Signature Analysis procedure to be performed when troubleshooting the microsequencer network. Conventional troubleshooting schemes, using the information provided in the theory of operation section of the manual, may be used when troubleshooting the other components of the formatter..

4.2 PLO CENTER FREQUENCY ADJUSTMENT

The PLO center frequency is adjusted in the factory and normally does not require readjustment. If the replacement of components, or other conditions, necessitates the readjustment of the PLO frequency, follow the procedure outlined below.

Required equipment:

Frequency counter
Hewlett Packard Model 5300 (or equivalent)

a. Remove jumper, marked PLL, at output of operational amplifier H11-6.

b. Connect frequency counter probe to pin 11 of four bit counter K4.

c. Select HIGH speed PE read operation.

d. Adjust potentiometer R12 to the frequency matching the HIGH transport speed, as shown in Table 4-1.

e. Select LOW speed PE read operation.

f. Adjustment potentiometer R11 to the frequency matching the LOW transport speed, as shown in Table 4-1.

Transport Speed (ips)	Reference Frequency (kc)
12.5	20
18.75	30
25	40
37.5	60
45	72
75	120
125	200

Table 4-1. PLO Reference Frequencies

4.3 SIGNATURE ANALYSIS OF THE MICROSEQUENCER

Since the microsequencer network is bus based and since its nonsequential programming generates varying data patterns at its various nodes, normal troubleshooting procedures would be quite cumbersome when applied to this network. To alleviate this difficulty Signature Analysis (SA) was incorporated into the design of the microsequencer. Signature Analysis consists of introducing a predetermined stimulus into a network and observing the network response. The stimulus is identical in all cases, consequently so should be the response of all properly functioning networks. Since the network nodes generate long strings of binary data, a method was devised for compressing the data strings into easily identifiable "signatures." This method is implemented using a Signature Analyzer (HP Model 5004A). The Signature Analyzer presents a four digit alphanumeric display in response to a series of binary data inputs. The display is unique and repeatable for any binary data stream. Using a properly functioning formatter, a signature table was constructed which delineates the signatures at the nodes of the microsequencer network. When troubleshooting another formatter the signatures at the prescribed nodes are read and compared with those given in the signature table. Note that for each configuration of PROMs a completely different set of signatures is generated; consequently it is necessary to match the revision letter of the PROMs (the revision letter is marked on the PROMs) to the revision letter of the particular signature table. The signatures in the table are arranged in a series of sets, each set representing the outputs of a particular component of the microsequencer. It is recommended that the signatures be read in the order presented in the table, following the actual generation of the signals. When a faulty signature is recognized, it would nearly always be caused by the failure of the component generating that signature. To perform the signature analysis follow the procedure outlined below.

Microsequencer Signature Analysis Procedure

Required equipment:

SA Analyzer
HP Model 5004A

a. Disconnect the 9X00 formatter cables from the controller and transport, leaving only the power supply connected.

b. Ground the Formatter Enable (J1-18) and Ready (J3-13) lines.

c. The Formatter Address line should be grounded if the Address Select strap (between R25 and ground) is out, or should remain floating if the Address Select strap is in.

d. Move the SA plug from its normal position to the adjacent, or SA, position.

e. Connect the Signature Analyzer to the 2910 Program Controller, IC N10, as follows:

CLOCK to N10-31
GROUND to N10-30
START to N10-28
STOP to N10-24

f. Place the Signature Analyzer pushbuttons in the following positions:

START in the IN position,
triggering on the trailing edge
STOP in the OUT position,
triggering on the leading edge
CLOCK in the OUT position,
triggering on the leading edge

g. Using the Signature Analyzer probe, read the signatures at the nodes listed in the signature table, comparing signatures.

NOTE

Make sure that the dash number of the PROMs installed in the microsequencer network matches that of the signature table.

Set 1
Instructions

- Pin	Signature
- 19	0000
- 16	4596
- 15	4596
- 12	4596

Set 2
er Outputs

- Pin	Signature
- 33	3F8H
- 35	PC84
- 37	627P
- 39	CHU8
- 1	8C36
- 3	FA11
- 18	41F7
- 20	HFP7
- 22	CC34
- 24	0000

Set 3
ol Store

- Pin	Signature
- 2	A59P
- 5	APU6
- 11	AC73
- 14	9PP8
- 8	2225
- 7	5HFH
- 3	6UH8
- 4	3149
- 18	9543
- 17	P56P
- 13	1337
- 14	6A1P
- 3	3P8A
- 8	P5FF
- 7	3A70
- 4	968U
- 18	147F
- 17	288F
- 14	IC53
- 13	9P05
- 4	8UCP
- 3	7840
- 7	22F8

Set 4
e Register

- Pin	Signature
- 9	2A96
- 6	7639
- 5	2082
- 2	HC7H
- 9	764U
- 6	F9CC
- 5	7UU9
- 2	50C1
- 12	PPF6
- 15	H252
- 16	15PA
- 19	2HUF
- 12	A85U
- 15	PAU4
- 16	U31C
- 19	PH63
- 5	2F1A
- 6	7A65
- 9	95CC
- 2	U818

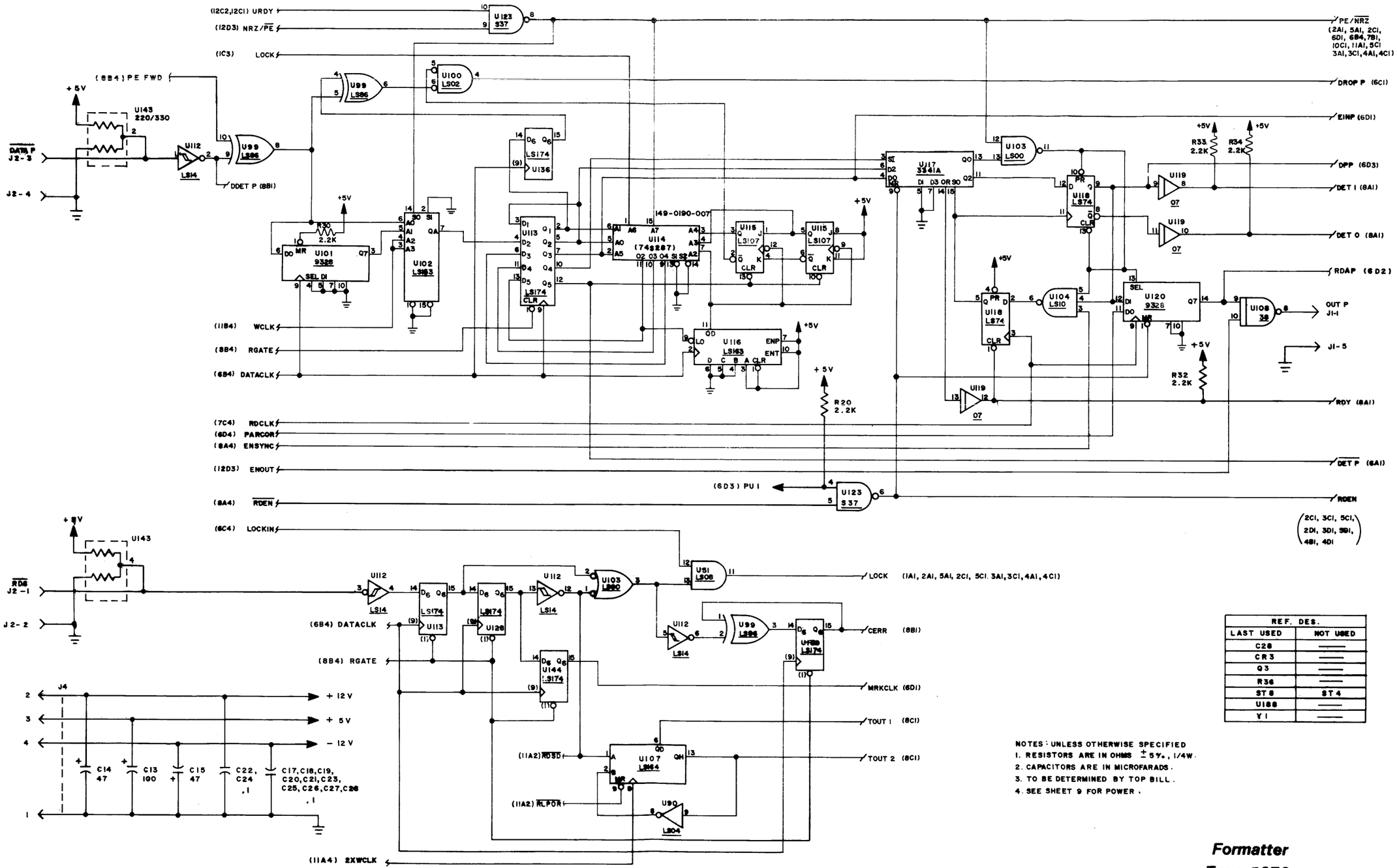
Set 5
ALU

Mnemonics	IC - Pin	Signature
RSLT1	M9 - 9	A460
RSLT2	M9 - 10	PC7C
RCLK	M9 - 11	9C97
I/O	M9 - 12	7774
IN0	K9 - 4	C3C4
IN1	K9 - 5	1C41
IN2	K9 - 6	HA38
IN3	K9 - 7	375C
OT3	K9 - 9	F755
OT2	K9 - 10	0183
OT1	K9 - 11	0031
OT0	K9 - 12	C193
RESULT	L13 - 5	H230
XDO	L7 - 3	394C

Set 6
Output Section

Mnemonics	IC - Pin	Signature
SFC	L12 - 4	3C25
SRC	L12 - 5	3UU4
OVW	L12 - 6	U244
SWS	L12 - 7	HH9C
DBY	L11 - 5	AHFC
CCLR/	L9 - 6	7CPA
END/	L9 - 12	88C3
RDEN/	L10 - 5	HA3A
LOCKEN	L10 - 6	1AP0
ENSYNC	L10 - 7	156U
WSEL/	L10 - 9	93AF
PEFWD	L10 - 11	4223
RGATE	L9 - 4	U6PU
TEMPA	L12 - 10	F104
TEMPB	L12 - 11	P55H
TEMPC	L12 - 12	A667
FMK	L11 - 4	4795
CCG	L11 - 6	H20P
NRZOUT	L11 - 7	2720
HER	L11 - 9	FHHU
PEOUT	L11 - 10	8444
CER	L11 - 11	H6PA
CER/	F14 - 10	937F
LAST	L10 - 12	3514
PWEN	L9 - 5	8PF0
IDCONT	L9 - 7	1665
WFM/	L9 - 9	258H
IDENT/	L9 - 10	F535
START	L9 - 11	1P60
NODAT	L11 - 12	9AP6

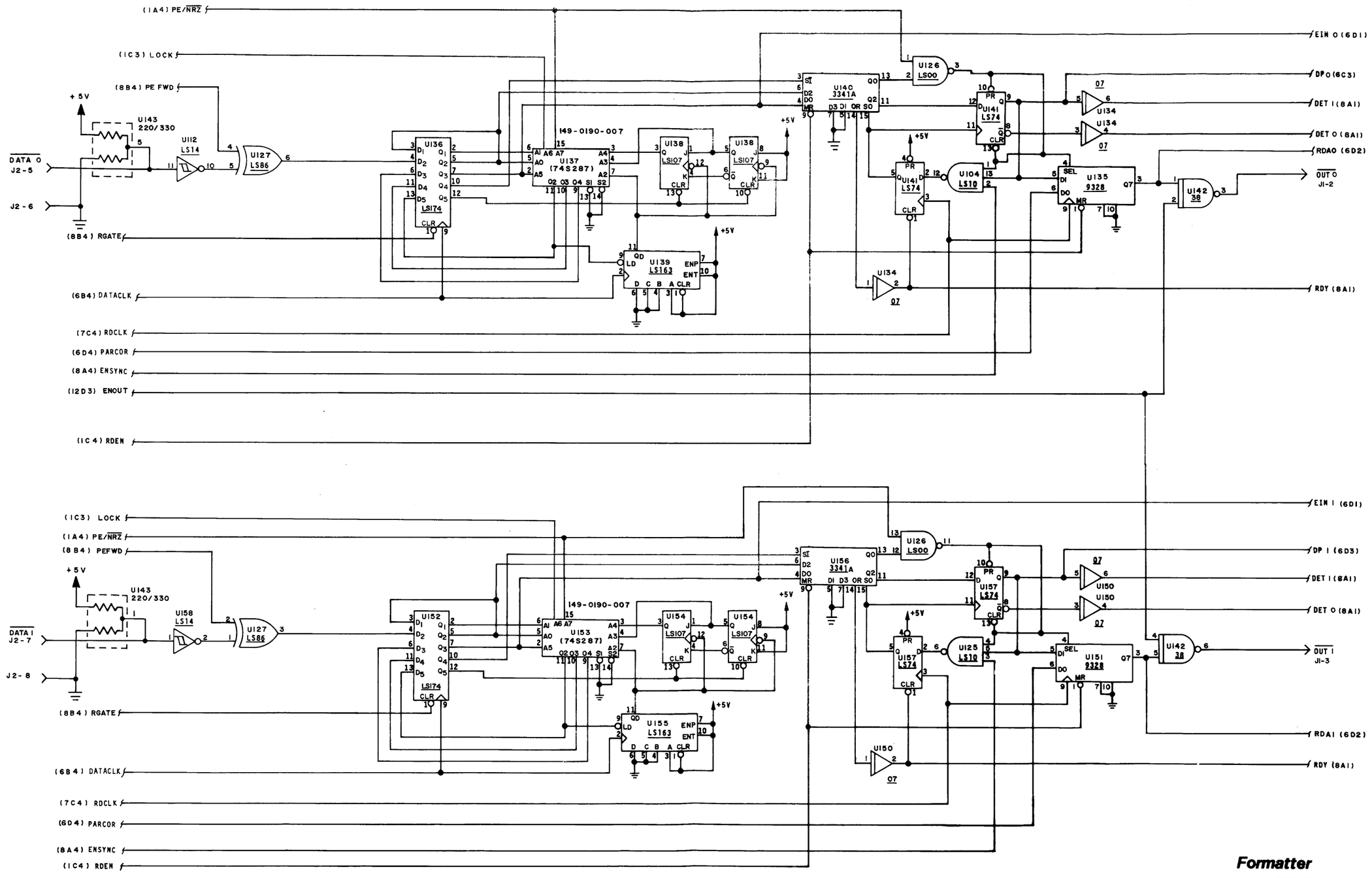
Signature Table for Dash Numbers 4, 5 and 6 PROMs



REF. DES.	
LAST USED	NOT USED
C28	—
CR3	—
Q3	—
R36	—
ST8	ST4
U188	—
Y1	—

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS ±5%, 1/4W.
2. CAPACITORS ARE IN MICROFARADS.
3. TO BE DETERMINED BY TOP BILL.
4. SEE SHEET 9 FOR POWER.

Formatter
Type 6679
Schematic Diagram



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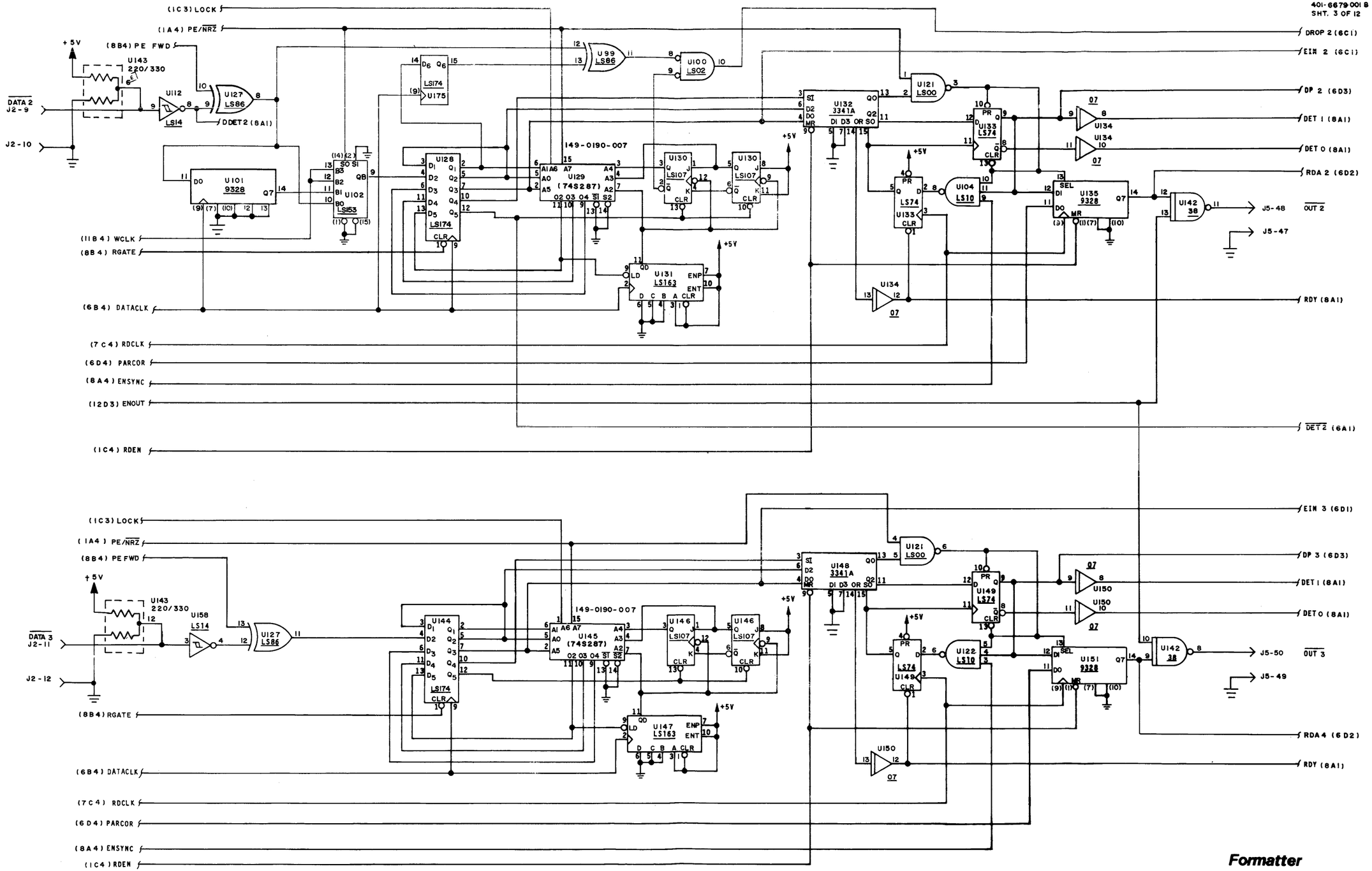

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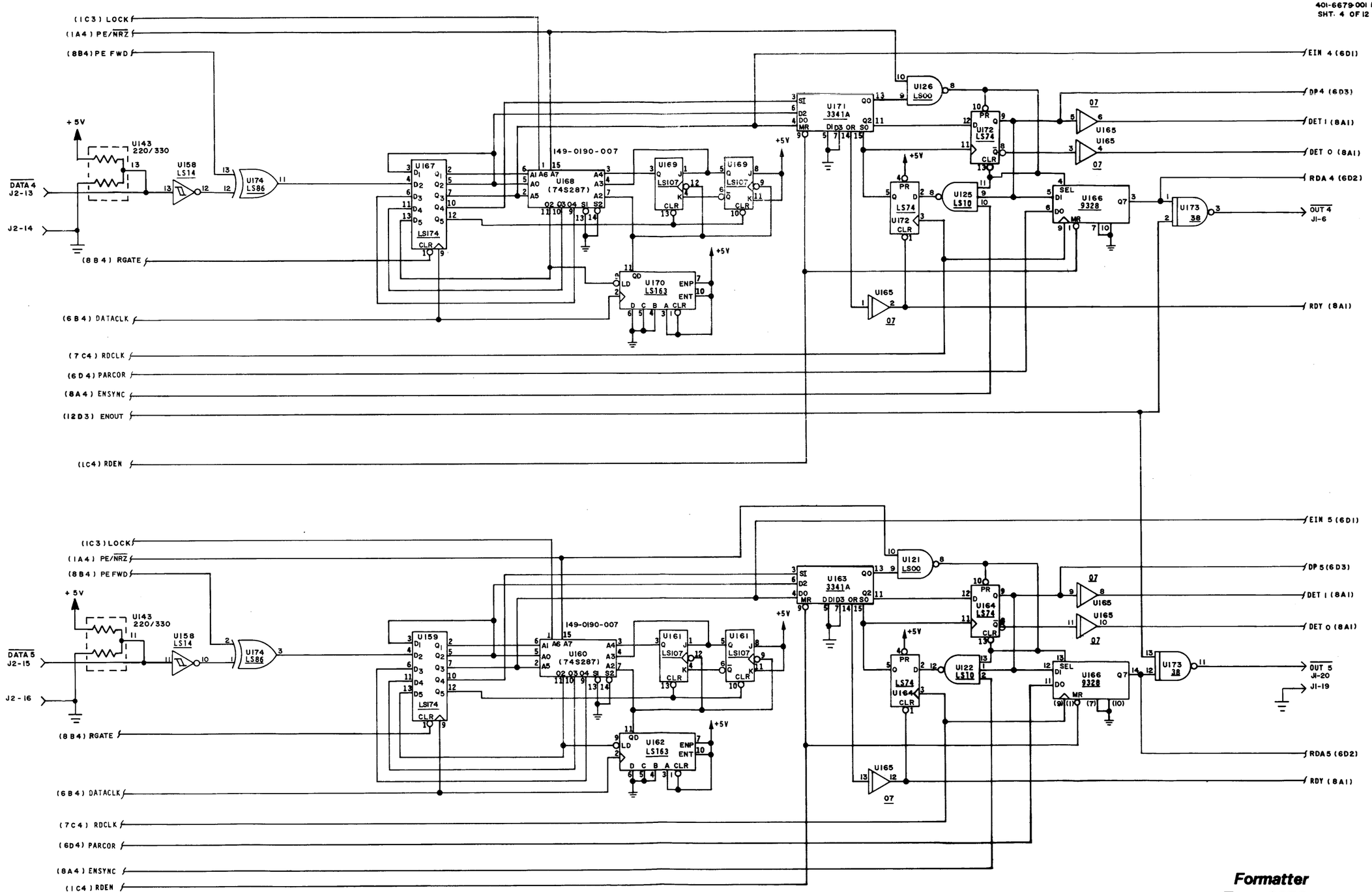

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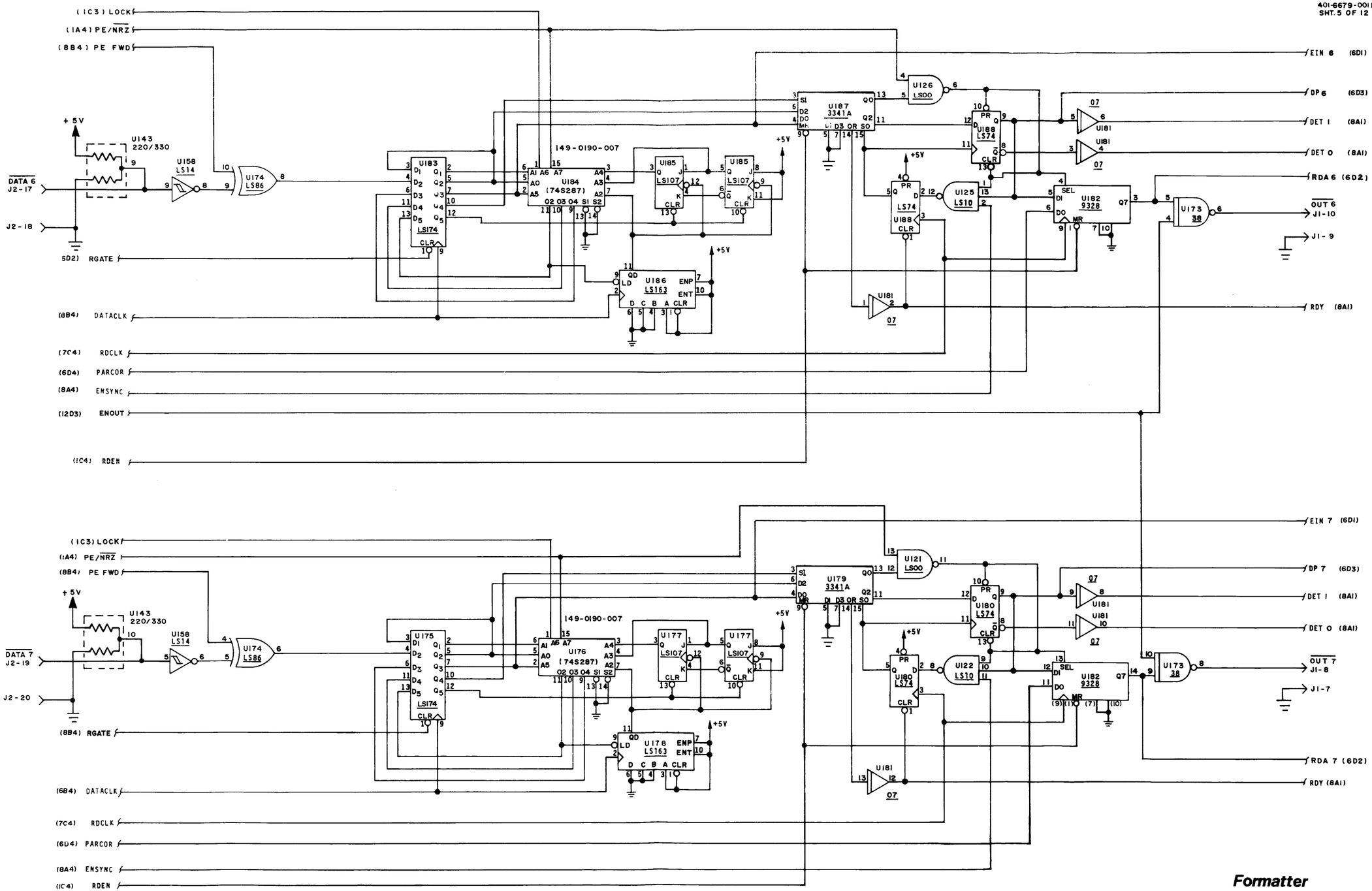
Schematic Diagram



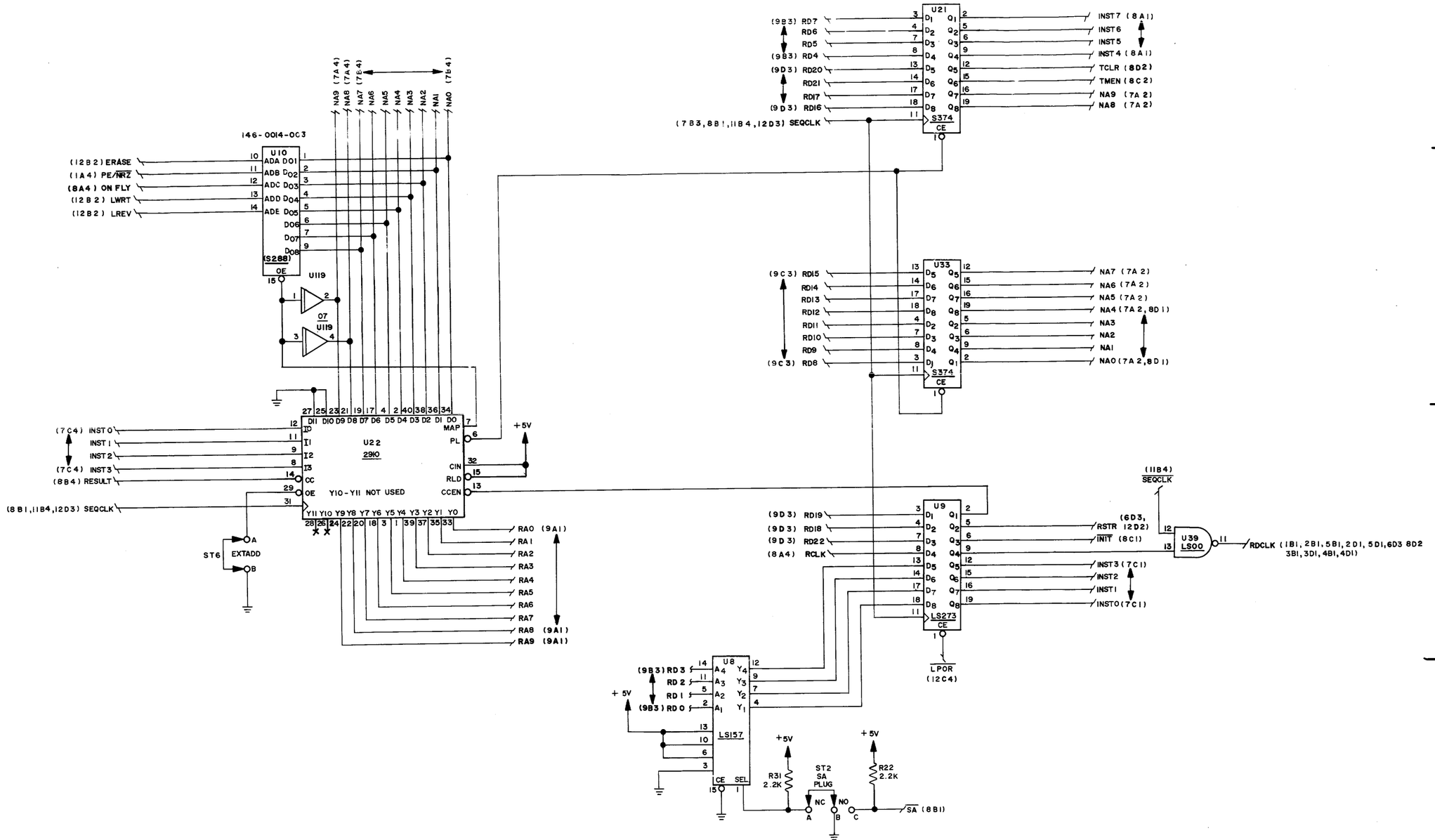
Formatter
Type 6679

Schematic Diagram

1 2 3 4

A B C D

Formatter Type 6679 Schematic Diagram



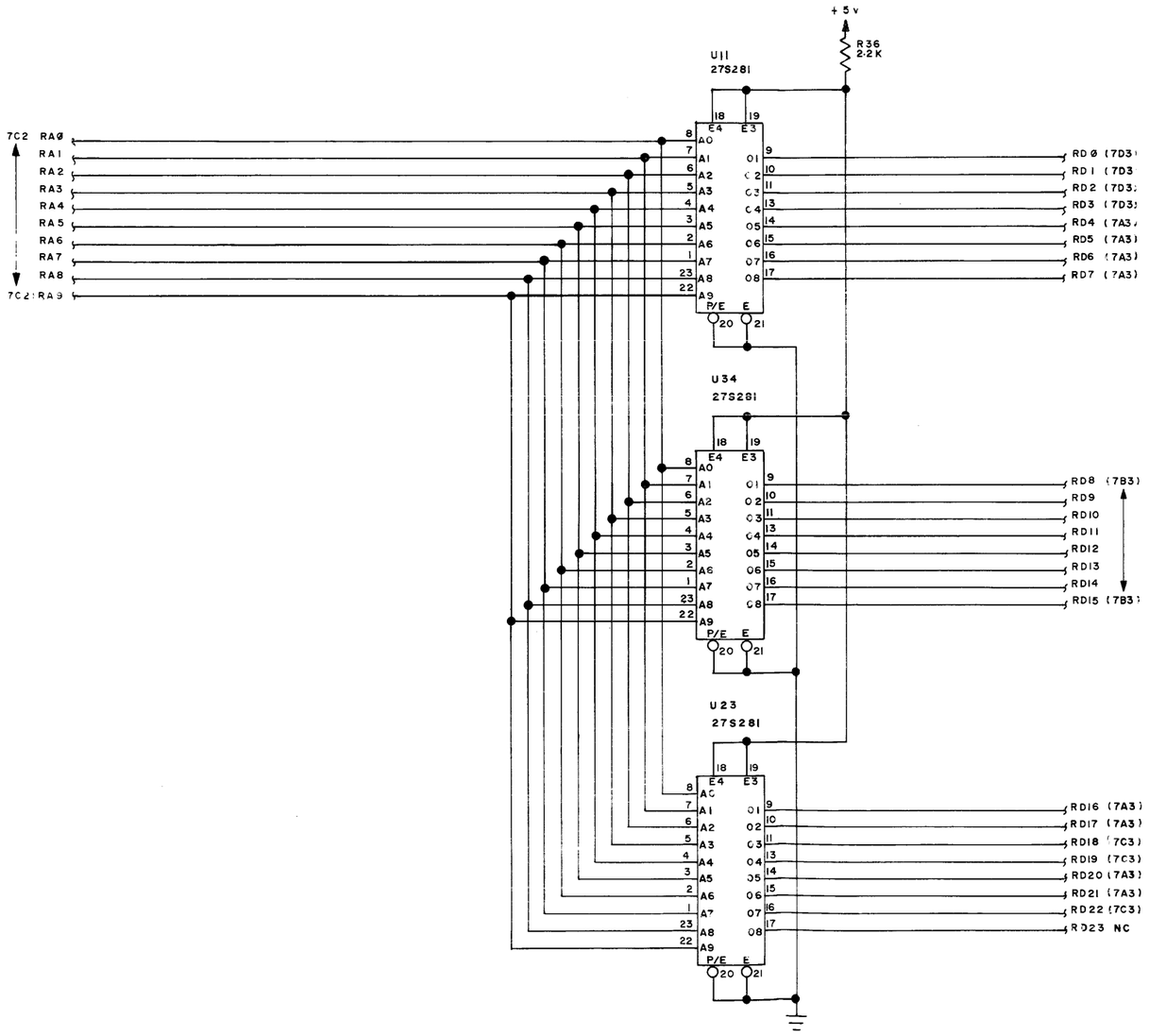
Formatter
Type 6679
Schematic Diagram

1 2 3 4

A B C D

(7A4) INST7
(7A4) INST6
(7B4) INST5
(7B4) INST4
(11B2) 7.2MHZ
(8A4) ON FLY
(2A4,2C4,1B4,4A4,4C4,3A4,5A4,3C4,5C4) DET 0
(1B4,4A4,4C4,3A4,5A4,3C4,5C4) DET 1
(3B4,3D4,4B4,4D4,1B4,2B4,5B4,2D4,5D4) RDY
(2A4,2C4)
(6C4) ENV
(6D2) LRCERR
(6D2) FMKDET
(3A1) DDET 2
U70 S251
(7C1,7B3,11B4,12D3) SEQCLK
(7D3) $\overline{SA}$
(11B4) $\overline{SEQCLK}$
(1B1) DDET P
(12C2) BUSY
(6D2) NFMK
(1C3) CERR
(6C4) PARITY
(12C2) LDP
(12C2) EOT
(12B2) EDIT
U71 S251
149-0177-004
U44 (S287)
U54 LS86
U59 S74
U3 LS08
U39 LS00
+5V
RCLK (7C3)
RESULT (7C1)
U56 LS259
(0) ON FLY (7A1, 8B1)
(1) $\overline{RDEN}$ (1C1)
(2) LOCKEN (6C3)
(3) ENSYNC (1C1,2B1,5B1,2D1,5D1,3B1,3D1,4B1,4D1
(4) $\overline{WSEL}$ (6B1, 6C3)
(5) WARSEN (10D4)
(6) PEFWD (1A1,2A1,5A1,2C1,5C1,3A1,3C1,4A1,4C1
(7) LAST (11C1)
U55 LS259
(8) RGATE (1B1, 4B1, 1D1, 4D1, 2B1, 3B1, 5B1, 2D1, 3D1, 5D1, 6D1)
(9) PWEN (11D1)
(A) $\overline{CCLR}$ (12C2)
(B) IDCONT (11B1)
(C) $\overline{WFM}$ (10C1, 11D1)
(D) $\overline{IDENT}$ (10C1, 11A1)
(E) START (11C1)
(F) $\overline{END}$ (12C2)
U69 S139
(8D3) TMOUT1
(8D3) TMOUT2
(1D3) TOUT1
(1D3) TOUT2
(6D2) SER
(8C4) TEMPA
(8C4) TEMPB
(8C4) TEMPC
U72 S251
U58 LS259
(10) SFC (12D1)
(11) SRC (12C1,12D1)
(12) OVW (12D1)
(13) SWS (12D1)
(14) SEL (12D1)
(15) TEMPA (8C1)
(16) TEMPB (8C1)
(17) TEMPC (8C1)
(7C3) $\overline{INIT}$
(7B4,7A2) NA0
NA1
NA2
NA3
(7B4,7A2) NA4
(12B2) LWRT
(12B2) LREV
(12B2) LWFMK
(8C4) FMK
(11C2) $\overline{DONE}$
(12B2) ERASE
(11B4) WCLK
(6D2) NOENV
U73 S251
U57 LS259
(18) FMK (8D1,12B2)
(19) DBY (12A2)
(1A) CCG (12A2,6D5)
(1B) NRZOUT (12D2)
(1C) HDER (6D4)
(1D) PEOUT (8D2)
(1E) CER (12B2)
(1F) NODAT (11D1)
(7B4) TMEN
(6B4) I/BC
(7C4) RDCLK
(7B4) TCLR
(8D4) PEOUT
U84 9328
TMOUT1 (8C1)
TMOUT2 (8C1,12B2,12D2)

Formatter
Type 6679
Schematic Diagram



IC POWER AND GROUND BUS

REF. DES.	TYPE	+5V	+12V	-12V	GND.
U1,26,37,62,85, 110,112,158	74LS14	14			7
U2,27,113,128, 136,144,152,159, 167,175,183	74LS174	16			8
U3,51	74LS08	14			7
U4,5,7,116,131, 139,147,155,162, 170,178,186	74LS163	16			8
U6,10	(74S288)	16			8
U8	74LS157	16			8
U9	74LS273	20			10
U11,23,34	(27S181)	24			12
U12,16,53,80	74LS32	14			7
U13,25,36,48, 50,75,76,86,89, 98,108,111,142, 173	7438	14			7
U14,61,49,143	220/330	14			7
U15,46,106	74LS280	14			7
U17,24,29,90	74LS04				
U18,28,40,41,45, 83,91,118,133, 141,149,157,164, 172,180,188	74LS74	14			7
U19,52,66,107	74LS164	14			7
U20,39,103,121, 126	74LS00	14			7
U21,33	74S374	20			10
U22	2910	10			30
U30,67,115,130, 138,146,154,161, 169,177,185	74LS107	14			7
U31,	74LS279	16			8
U32,65,100	74LS02	14			7
U38	74LS373	20			10
U42	74LS162	16			8
U43	74LS161	16			8
U44,105,114,129 137,145,153,160, 168,176,184	(74S287)	16			8
U47,60	74LS240	20			10
U54,78,82,88, 99,127,174	74LS86	14			7
U55,56,57,58	74LS259	16			8
U59,93	74S74	14			7
U63	MC8500	24			12
U64	74LS139	16			8
U68,U123	74S37	14			7
U69	74S139	16			8
U70,71,72,73	74S251	16			8
U77,87	74LS298	16			8
U79,102,92	74LS153	16			8
U81,104,122, 125	74LS10	14			7

CONT

REF. DES.	TYPE	+5V	+12V	-12V	GND.
U84,101,120,135, 151,166,182	9328	16			8
U94,	74LS26	14			7
U95	2517		7	4	
U96	4053		16		8
U109	MC1658	1,5			8
U117,132,140,148, 156,163,171,179, 187	3341A	16		1	8
U119,134,150, 165,181,	7407	14			7
U124	74S132	14			7

Formatter
Type 6679

Schematic Diagram

1 2 3 4

A B C D

(11B4) WSTR

+5V

U14 220/330

J5

$\overline{WO}$ 10
$\overline{W1}$ 12
$\overline{W2}$ 30
$\overline{W3}$ 26
$\overline{W4}$ 6
$\overline{W5}$ 32
$\overline{W6}$ 28
$\overline{W7}$ 24
$\overline{WP}$ 22
$\overline{LWD}$ 4

LSI4 U1 U26

U27 LS174 CLR

U2 LS174 CLR

(11C4) $\overline{SYNC}$

(8B4) $\overline{WFM}$
(8B4) $\overline{IDENT}$
U3 LS08

(1A4) PE/$\overline{NRZ}$
U65 LS02

(11C4) $\overline{WEN}$
(11D4) ERRCLK
(11B4) WRTZ
(11B4) TOGGLE
U82 LS86

(11A4) OCLK
(11C4) OUTEN

U15 LS280

INPUT

ST3 EXT
INT

MCB500
U63

U16 LS32

U90 LS04

SSI U79 LSI53

U78 LS86

U88 LS86

U77 U87 LS298 SEL

U83 LS74 PR CLR

U62 LS14

U90 LS04

U76 38

U86 38

U89 38

J2

35 $\overline{WD0}$
36
37 $\overline{WD1}$
38
39 $\overline{WD2}$
40
41 $\overline{WD3}$
42
43 $\overline{WD4}$
44
45 $\overline{WD5}$
46
47 $\overline{WD6}$
48
49 $\overline{WD7}$
50
33 $\overline{WDP}$
34
(8A4) WARSEN
31 $\overline{WARS}$
32

LWD (11D1)

$\overline{MARK}$ (11C1, 11D1)

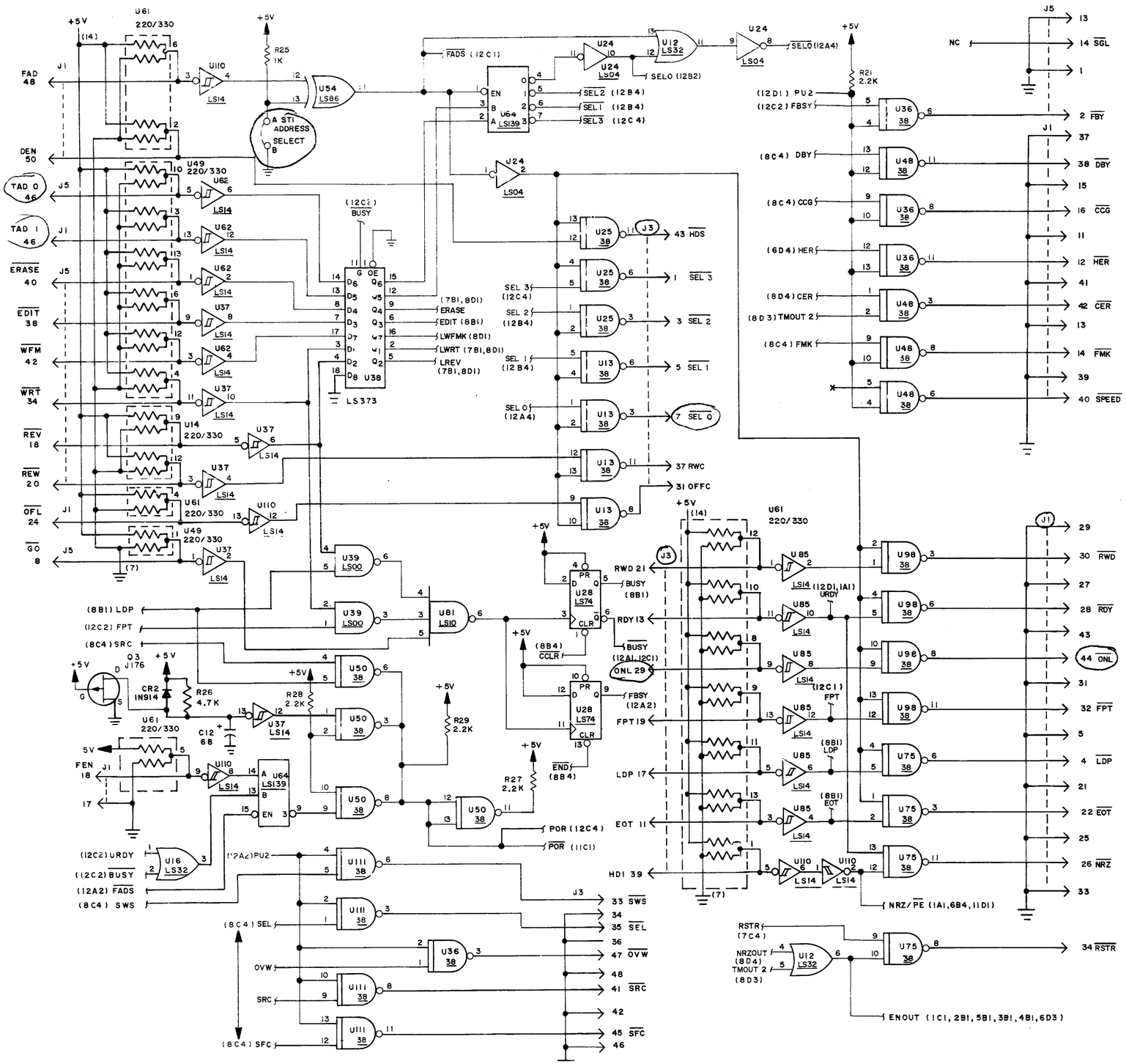
Formatter
Type 6679
Schematic Diagram

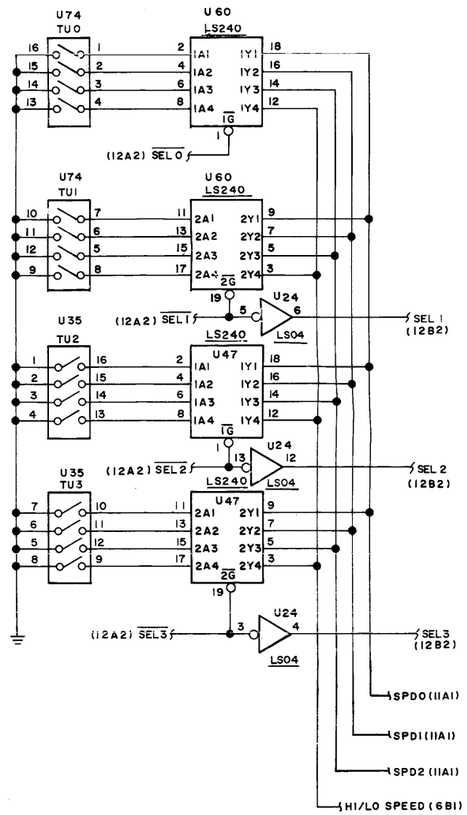
1 2 3 4

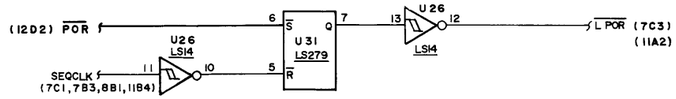
A B C D

(11B4) WCLK
146-0015-001 U6 (74S288)
(1A4) PE/NRZ
(8B4) IDENT
(12C4) SPD 2
(12C4) SPD 1
(12C4) SPD 0
(11B4) SEQCLK
U80 LS32
U17 LS04
C10 270PF
R23 1K
R24 1K
Y1 7.2MHZ
C9 10 PF
C11 10PF
ST 5 SEQ. CLK
U5 LS163
U7 LS163
U68 S37
(12C4) LPDR
(1D2) RDSD
(12,13)
RLPOR (1D2)
U20 LS00
2XWCLK (1D1)
7.2MHZ (8A1)
+5V
U18 LS74
U19 LSI64
U30 LSI07
U54 LS86
U32 LS02
U89 38
U51 LS08
U53 LS32
U68 S37
U81 LSI0
U29 LS04
U16 LS32
U31 LS279
U40 LS74
U41 LS74
U42 LSI62
U43 LSI61
U67 LSI07
U82 LS86
U52 LSI64
U54 LS86
WSTB (6A1)
WSTB (11C1)
7.2MHZ (6B4)
OCLK (10D1)
WDS (11D1)
29 WDS
30
36 WSTR
35
WSTR (10A1)
TOGGLE (10C1)
WCLK (1B1, 3B1, 8D1, 11A1)
SEQCLK (7C4, 8B1, 11A1)
SEQCLK (7C1, 7B3, 8B1, 12D3)
WCLK (11D1)
WRTZ (10C1)
SYNC (10B1, 11C1, 11B4)
WDSEN (11A4)
OUTEN (10D1)
WEN (10C1)
ERRCLK (10C1)
(8B4) IDCONT
(10C4) MARK
(8B4) START
12C2) POR
(8B4) LAST
(11A4) WSTB
(11C4) SYNC
(1084) LWD
(12D3) NRZ/PE
(8B4) PWEN
(8B4) WCLK
(8B4) WFM
(11A4) WDS
(8D4) NODAT
DONE (8D1)

Formatter
Type 6679
Schematic Diagram







Formatter
Type 6679
Schematic Diagram

KENNEDY

ALLEGHENY INTERNATIONAL

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