

JADE COMPUTER PRODUCTS

**THE
BIG-Z**

REV-A

Z-80 MICRO PROCESSOR BOARD

4901 WEST ROSECRANS BLVD., HAWTHORNE, CALIFORNIA, 90250

THE BIG-Z

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1. FEATURES

On board 2704/2708/2716/2532 EPROM can be addressed on any 1K, 2K, or 4K ■ Power-on jump directly to on-board EPROM. ■ Optional wait state for on-board EPROM. ■ On-board EPROM may be used in shadow mode (access only after power-on or reset). Allows full 64K RAM memory to be used.

Automatic MEM WRITE generation if front panel is not used. Disabled if front panel is connected. ■ DMA Capability ■ 2 or 4 MHz operation ■ Latched data output bus provides additional data hold time for reliable operation with all device types. ■ Straight-through address and data paths provide improved read access times for I/O and memory devices. ■ On-board USART for synchronous or asynchronous RS232 operation.

Baud rate generator provides all standard baud rates. ■ USART can be assigned to any group of four I/O addresses (only two are used) ■ Reverse channel capability on USART allows use with buffered peripherals or devices with "not-ready" indication. ■

II. Board Assembly

- 1) Install chip sockets at U4, U5, U6, U7, U8, U10, U14, U15, U17, U18, U20, U21, U22, U25, U16, U26, U27, U28, U29, U30, U32, U35, U36, U37, U38, U39, U40, and U41.
- 2) Install 1.5 uf capacitor at C16. ✓
- 3) Install .1 uf capacitors at C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, and C11 = 6.8 μ F ✓
- 4) Install 7805/LM340T5 Regulator at VR4. ✓
- 5) Install 100 uf capacitor at C22. ✓
- 6) Install 100 pf capacitor at C24. ✓
- 7) Install 10 pf capacitor at C23. ✓
- 8) Install 330 resistor at R5. ✓
- 9) Install 1K resistor at R4. ✓
- 10) Install 2.7K resistor at R2. ✓
- 11) Install 4.7K resistors at R1, R7, R8, R9, and R3. ✓
- 12) Install crystal at Y1 (18 MHz or 30 MHz). ✓
- 13) Install IC's and resistor modules in locations shown in parts list.

III. Options

A. 2 MHz operation

Install:

- 1) 18 MHz crystal at Y1
- 2) Jumper from U to S.

B. 4 MHz operation

Install:

- ~~1) 36 MHz crystal at Y1~~
- ~~2) 1 uh coil at L1~~
- ~~20 pf cap at C25~~
- ~~.1 uf cap at C26~~
- 3) Jumper from U to T.

C. On board EPROM:

Install:

- 8 position switch module
at U33.
24 pin chip socket at U13.
16 pin chip socket at U34
8131 IC at U34.
2704/2708/2716/2516/

2704/2708 EPROM

- 1) Install 7905 regulator at VR1.
Install 7812 regulator at VR3 (used for USART also).
- 2) Install 1.5 uf capacitors at C19, C18, and C17.
Install .1 uf capacitors at C13, C15, and C12.
- 3) Set switch 7 on U33 to off.
Set switch 8 on U33 to on.
- 4) Select EPROM address from table III-1 and set switches on U33 as shown.
- 5) Install jumper from B to C

TMS 2716 EPROM

- 1) Install 7905 regulator at VR1.
Install 7812 regulator at VR3, (used for USART also)
- 2) Install 1.5 uf capacitors at C19, C18, and C17.
Install .1 uf capacitors at C13, C15, and C12.

3) Install jumpers:

A to C

D to B

4) Set switch 1 and 7 on U33 to on. Set switch 8 on U33 to off.

5) Select EPROM Address from table III-2 and set switches on U33 as shown.

INTEL 2716/TMS 2516 EPROM

1) Cut etch L to E.

Cut etch F to M.

2) Install jumper from D to M.

Install jumper from C to B.

Install jumper from I to A.

3) Set Switch 1 and 7 on U33 to on.

Set switch 8 on U33 to off.

4) Select EPROM address from table III-2 and set switches on U33 as shown.

Install jumper from +5 to E.

INTEL 2732/TMS 2532 EPROM

1) Cut etch L to E.

Cut etch F to M.

Cut etch G to H.

2) Install jumper from D to M.

Install jumper from C to B.

Install jumper from G to E.

Install jumper from H to I.

3) Set switch 5, 6, and 7 on U33 to on.

Set Switch 8 on U33 to off.

4) Select EPROM address from table III-3 and set switches on U33 as shown.

Install jumper from A to I.

5) MI wait state: set switch 7 on U23 to off. Install jumper from R to P, and change USART option to H.

D. No EPROM and no power-on jump:

Set switch 7 and 8 on U23 to off.

E. Power-on jump:

Note: An EPROM must be on the board to use the power-on jump option.

Set switch 8 on U23 (if installed) to on.

Jumper U23 pin 8 to 9 if switch not installed.

F. EPROM wait state:

Note: An EPROM must be on the board to use this option.

Set switch 7 on U23 (if installed) to on.

~~NO~~ Jumper U23 pin 7 to 10 if switch not installed.

G. USART option:

1) Install:

28 pin socket at U3

24 pin socket at U2

16 pin socket at U24

14 pin sockets at U9 and U12

8 position dip switch at U1 and U23

8251A IC at U3

MC14411 IC at U2

8131 IC at U24

1489 IC at U9

1488 IC at U12

1.8432 MHz crystal at Y2

22 Meg resistor at R6

7912 regulator at VR2

7812 regulator at VR3, (used for EPROM also)

1.5 uf capacitors at C20, C21, and C17

.1 uf capacitors at C14, C15, and C13.

2) Set one switch on U1 to desired baud rate, (silk screened next to U1 switches) and set all other switches on U1 to off.

3) Select desired I/O port address from table III-4 and set switches on U23 as shown.

IV. Circuit Description

The Z-80 address bus is driven to the S100 bus by U35, U36 and a portion U25. The ADDSB signal on pin 22 will tri-state the address bus for DMA or maintenance functions when driven low.

The S100 DI (data in) bus is provided to the Z-80 during read memory or I/O input cycles by U38 and a portion of U29. The DI bus receivers are disabled when a write memory or I/O output cycle is performed. They are also disabled by the following conditions:

1) SSWDSB low at pin 53.

2) RUN and SS low at pins 71 and 21.

3) EPROM selected during memory read operation.

4) USART selected during I/O operation.

5) Power-on jump enabled and Power-on latch (2 sections of U10) is set.

The Z-80 data bus is provided to the S100 data out (DO) bus for memory write or I/O output cycles by U37 and part of U25. The DODSB signal on pin 23 will tri-state the data out bus for DMA or maintenance functions when driven low.

The Z-80 clock and reset signals are generated by U21. The crystal and tank circuit used allow operation at 2 or 4 MHz. When the RESET signal on pin 75 is driven low, U21 provides a reset signal to the Z-80 and the power-on jump latch if used. This signal is provided to the S100 bus as POC at pin 99. Pin 75 is held low momentarily during power-up due to the time it takes to charge C22. 01 and 02 signals are provided to the S100 bus on pins 24 and 25. The S100 bus 2 MHz CLOCK signal on pin 49 is derived from 02 directly for 2 MHz operation and is divided down by U21 for 4 MHz operation.

The Z-80 WAIT signal is activated by the following conditions:

- 1) XRDY on pin 3 going low.
- 2) PRDY on pin 72 going low.
- 3) First 02 clock cycle after EPROM is selected when EPROM wait state is enabled, (U20).

EPROM wait state is enabled, (U20). PWAIT on pin 27 will go high to indicate when the Z-80 wait signal is enabled.

The following S100 signals are derived from the Z-80 RD, WR, IORQ, MRQ, M1, and RFSH signals:

- 1) SOUT + WR and IORQ (output to I/O port).
- 2) SINP + RD and IORQ (input from I/O port).
- 3) SMEMR + RD and MRQ (read memory).
- 4) MWRT + WR and MRQ (write memory).
- 5) PWR + WR and MRQ (processor is outputting data).
- 6) INTA + M1 and IORQ (interrupt acknowledge).
- 7) PDBIN + RD or INTA (processor inputting data).
- 8) RFSH + RFSH (refresh access request).
- 9) MRQ + MRQ (memory access request).
- 10) SM1 + M1 (processor fetching instruction op code).
- 11) SWO + RD and INTA (processor not inputting data). This signal is used as an early indication that a write operation will take place.
- 12) PSYNC + IORQ or MRQ and RFSH (valid memory or I/O access). The PSYNC signal is only high during the first part of a memory or I/O cycle due to multi U5. This signal is provided for S100 bus devices that look at status information during the first portion of a cycle as per 8080 device conventions. SINP, SMEMR, and SWO are latched by PSYNC on U40 before being placed on the S100 bus to make look like 8080 status signals.

The STADSB signal on pin 18 will tri-state the SOUT, SINP, SMEMR, SWO, and SM1 signals when it is driven low. The CCDSB signal on pin 19 will tri-state the PDBIN, INTA, PSYNC, and PWR signals when it is driven low. When a front panel is not used, the RUN signal from the processor board. When a front panel makes RUN low, the MWQRT signal is tri-stated to allow the front panel circuitry to perform writes to memory with its own MWRT signal.

The Z-80 BUSRQ signal is activated when the PHOLD signal on pin 74 is driven low. The Z-80 tri-states its data and address busses and generates BUSAK low in response to BUSRQ. BUSAK is provided to the S100 bus as HLDA on pin 26 to acknowledge that the processor is in a "hold" condition. HLTA is provided as HLTA on pin 48 whenever the Z-80 is executing a halt instruction.

The INT signal on pin 73 will cause the Z-80 maskable interrupt request to become active when driven low.

The EPROM (U13) is selected by the power-on jump latch (2 sections of U10) after it is set by the reset signal. The address bus is compared to switch settings of U33 by comparator U34. When the selected address range is detected the power-on latch is reset by the comparator output. The comparator output will also select the EPROM when the shadow EPROM option is not installed. The EPROM is accessed only when memory is requested.

The lower portion of the address bus is compared to the switch settings of U23 by comparator U24. When the selected address range is detected during an I/O operation, the USART (U3) is enabled. The USART derives its transmit and receive clock from the baud rate generator U2. The desired clock rate is selected by switch module U1. All the clocks are 16 times the baud rate indicated. The USART should be programmed for 16X clocks. Refer to vendor data for detailed programming information on the 8251. Appendix A is enclosed for your reference. The transmit data (TXD), receive data (RXD), and reverse channel (RVC) signals are provided at connector socket U19.

JADE Z-80 KIT

PACK #1

- 1 Z-80 CPU
- 1 8224
- 1 18 MHz Crystal

PACK #2

- 1 Z80A CPU
- 1 8224-4
- 1 36MHz Crystal
- 1 20pf Disc Cap
- 1 1Uh Coil

PACK #3

- 2 7400
- 1 7402
- 3 7404
- 2 7408
- 1 7410
- 1 7432
- 1 7474
- 3 7475
- 1 74121
- 9 74367/8097/8T97
- 2 DM8131
- 1 8251
- 1 MC14411
- 1 1488
- 1 1489
- 1 LM320T-5/7905
- 1 LM320T-12/7912
- 1 LM340T-5/7805
- 1 LM340T-12/7812
- 3 8 Position Dip Switch

PACK #4

- 1 330 ohm ¼W 5%
- 1 1K
- 1 2.7K
- 5 4.7K
- 1 22meg./20meg.
- 2 4.7K 16 pin 15 res. Resistor Pack
- 16 .1mf Disc
- 6 1.5/1.8mf Disc
- 1 10pf Disc
- 1 100pf Disc
- 1 100mf 25V Axial Electrolytic

PACK #5

- 17 14 pin Lo Pro Sockets
- 12 16 pin Lo Pro Sockets
- 2 24 pin Lo Pro Sockets
- 1 40 Pin Lo Pro Sockets

PACK #6

- 1 373 Heatsink
- 4 6-32 Hex Nut
- 4 6-32 x ⅜" Screw
- 4 6-32 Lockwasher

Table III-1 2704/2708 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11	SW6 A10
0000-03FF	X	X	X	X	X	X
0400-07FF	X	X	X	X	X	
0800-0BFF	X	X	X	X		X
0C00-0FFF	X	X	X	X		
1000-13FF	X	X	X		X	X
1400-17FF	X	X	X		X	
1800-1BFF	X	X	X			X
1C00-1FFF	X	X	X			
2000-23FF	X	X		X	X	X
2400-27FF	X	X		X	X	
2800-2BFF	X	X		X		X
2C00-2FFF	X	X		X		
3000-33FF	X	X			X	X
3400-37FF	X	X			X	
3800-3BFF	X	X				X
3C00-3FFF	X	X				
4000-43FF	X		X	X	X	X
4400-47FF	X		X	X	X	
4800-4BFF	X		X	X		X
4C00-4FFF	X		X	X		
5000-53FF	X		X		X	X
5400-57FF	X		X		X	
5800-5BFF	X		X			X
5C00-5FFF	X		X			
6000-63FF	X			X	X	X
6400-67FF	X			X	X	
6800-6BFF	X			X		X
6C00-6FFF	X			X		
7000-73FF	X				X	X
7400-77FF	X				X	
7800-7BFF	X					X
7C00-7FFF	X					

X = switch on

Table III-1 (continued)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11	SW6 A10
8000-83FF		X	X	X	X	X
8400-87FF		X	X	X	X	
8800-8BFF		X	X	X		X
8C00-8FFF		X	X	X		
9000-93FF		X	X		X	X
9400-97FF		X	X		X	
9800-9BFF		X	X			X
9C00-9FFF		X	X			
A000-A3FF		X		X	X	X
A400-A7FF		X		X	X	
A800-ABFF		X		X		X
AC00-AFFF		X		X		
B000-B3FF		X			X	X
B400-B7FF		X			X	
B800-BBFF		X				X
BC00-BFFF		X				
C000-C3FF			X	X	X	X
C400-C7FF			X	X	X	
C800-CBFF			X	X		X
CC00-CFFF			X	X		
D000-D3FF			X		X	X
D400-D7FF			X		X	
D800-DBFF			X			X
DC00-DFFF			X			
E000-E3FF				X	X	X
E400-E7FF				X	X	
E800-EBFF				X		X
EC00-EFFF				X		
F000-F3FF					X	X
F400-F7FF					X	
F800-FBFF						X
FC00-FFFF						

X = switch on

Table III-2 2716/2516 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11
0000-07FF	X	X	X	X	X
0800-0FFF	X	X	X	X	
1000-07FF	X	X	X		X
1800-1FFF	X	X	X		
2000-27FF	X	X		X	X
2800-2FFF	X	X		X	
3000-37FF	X	X			X
3800-3FFF	X	X			
4000-47FF	X		X	X	X
4800-4FFF	X		X	X	
5000-57FF	X		X		X
5800-5FFF	X		X		
6000-67FF	X			X	X
6800-6FFF	X			X	
7000-77FF	X				X
7800-7FFF	X				
8000-87FF		X	X	X	X
8800-8FFF		X	X	X	
9000-97FF		X	X		X
9800-9FFF		X	X		
A000-A7FF		X		X	X
A800-AFFF		X		X	
B000-B7FF		X			X
B800-BFFF		X			
C000-C7FF			X	X	X
C800-CFFF			X	X	
D000-D7FF			X		X
D800-DFFF			X		
E000-E7FF				X	X
E800-EFFF				X	
F000-F7FF					X
F800-FFFF					

X = switch on

Table III-3 2732 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12
0000-0FFF	X	X	X	X
1000-1FFF	X	X	X	
2000-2FFF	X	X		X
3000-3FFF	X	X		
4000-4FFF	X		X	X
5000-5FFF	X		X	
6000-6FFF	X			X
7000-7FFF	X			
8000-8FFF		X	X	X
9000-9FFF		X	X	
A000-AFFF		X		X
B000-BFFF		X		
C000-CFFF			X	X
D000-DFFF			X	
E000-EFFF				X
F000-FFFF				

X = switch on

Table III-4 USART Address Select (U23)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A2
00-01	X	X	X	X	X	X
04-05	X	X	X	X	X	
08-09	X	X	X	X		X
0C-0D	X	X	X	X		
10-11	X	X	X		X	X
14-15	X	X	X		X	
18-19	X	X	X			X
1C-1D	X	X	X			
20-21	X	X		X	X	X
24-25	X	X		X	X	
28-29	X	X		X		X
2C-2D	X	X		X		
30-31	X	X			X	X
34-35	X	X			X	
38-39	X	X				X
3C-3D	X	X				
40-41	X		X	X	X	X
44-45	X		X	X	X	
48-49	X		X	X		X
4C-4D	X		X	X		
50-51	X		X		X	X
54-55	X		X		X	
58-59	X		X			X
5C-5D	X		X			
60-61	X			X	X	X
64-65	X			X	X	
68-69	X			X		X
6C-6D	X			X		
70-71	X				X	X
74-75	X				X	
78-79	X					X
7C-7D	X					

X = switch on

Table III-4 (continued)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A2
80-81		X	X	X	X	X
84-85		X	X	X	X	
88-89		X	X	X		X
8C-8D		X	X	X		
90-91		X	X		X	X
94-95		X	X		X	
98-99		X	X			X
9C-9D		X	X			
A0-A1		X		X	X	X
A4-A5		X		X	X	
A8-A9		X		X		X
AC-AD		X		X		
B0-B1		X			X	X
B4-B5		X			X	
B8-B9		X				X
BC-BD		X				
C0-C1			X	X	X	X
C4-C5			X	X	X	
C8-C9			X	X		X
CC-CD			X	X		
D0-D1			X		X	X
D4-D5			X		X	
D8-D9			X			X
DC-DD			X			
E0-E1				X	X	X
E4-E5				X	X	
E8-E9				X		X
EC-ED				X		
F0-F1					X	X
F4-F5					X	
F8-F9						X
FC-FD						

X - switch on

APPENDIX A

8251A USART

The 8251A USART must be programmed by outputting, first a mode, then a command, to the control port.

The 8251A always wants to set the mode instruction after an internal or external reset. The next command is the command instruction. Bit 6 of the command instruction is an internal reset and sets the USART back to the mode instruction, otherwise the USART is always looking for another command instruction.

The following programs are examples of the steps necessary to use a 8251A.

```
INIT:                .      INITIALIZATION
MVI A, 4E H  ..... Sets Mode
OUT 1
MVI A, 37 H ..... Sets Receive and Transmit
OUT 1
```

INPUT

Checks status and inputs a Byte to Accumulator

```
START:
IN 1 ..... Read Status

ANI 2, ..... Check Bit 1
JZ START ..... Loop until true
IN 0 ..... Read Data
```

OUT

Checks status and outputs a Byte from Register B, destroys Accumulator

```
BEGIN:
IN 1 ..... Read Status

ANI 1 ..... Check Bit 0
JZ BEGIN ..... Loop until true
MOV A, B
OUT 0 ..... Output Data
```

This program echos characters. A reset must be performed before this program can be run.

```
20 OUT 1, 206 Sets Mode
30 OUT 1, 39 Sets Receive and Transmit
35 WAIT 1,2 Wait for character from USART
40 A = INP(0) Get character from USART
50 WAIT 1,1
70 OUT O, A Send character to USART
80 Go to 30
```

THE BIG Z

PARTS LIST

() = Acceptable Substitution [] = 4 MHz Parts

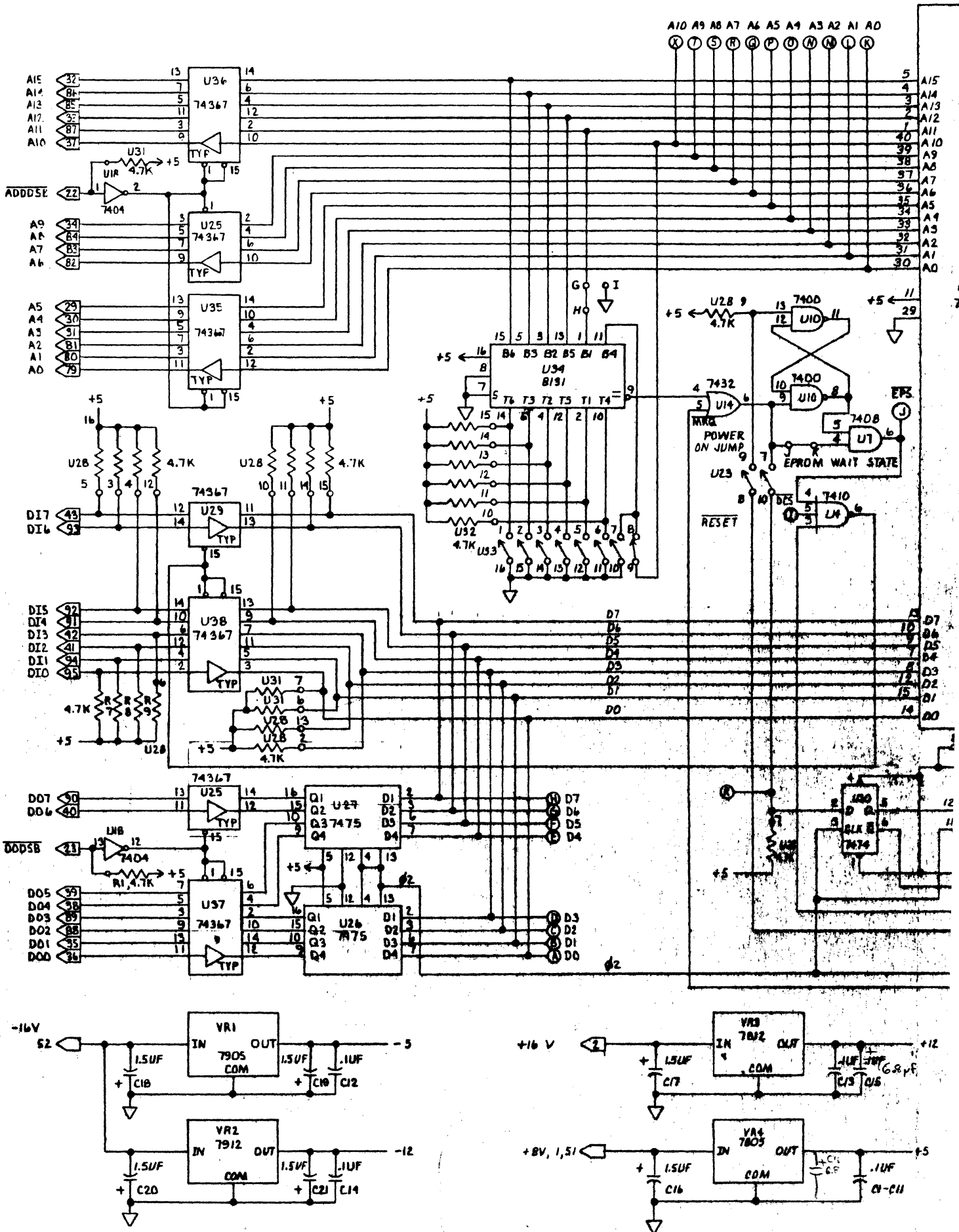
Reference Designator	Part Number	Quantity Part Description	Per Assembly
U1	Z80	IC, Processor	1
[U1]	[Z80A]	[IC, Processor, 4MHz]	[1]
U6, U17, U25, U29, U35-39	74367, (8097), (8T97)	IC, Hex TS Buffer	9
U24 , U34	8131	IC, Comparator, 6 bit	2
U40, U26, U27	7475 (74LS75)	IC, Latch, Quad	3
U3	8251	IC, USART	1
U2	MC14411	IC, Baud Rate Generator	1
U13	2708 (2704), (2716), (2516), (2532)	IC, EPROM	1
20	7474 (74LS74)	IC, Flip-flop, Dual D	1
U21	8224	IC, Clock Generator	1
[U21]	[8224-4]	[IC, Clock Gen., 4MHz]	[1]
U5	74121	IC, One Shot	1
U14	7432 (74LS32)	IC, OR, Quad 2 Input	1
U22, U10	7400 (74LS00)	IC, NAND, Quad 2 Input	2
U7, U41	7408 (74LS08)	IC, AND, Quad 2 Input	2
U4	7410, (74LS10)	IC, NAND, Triple 3 Input	1
U8	7402, (74LS02)	IC, NOR, Quad 2 Input	1
U15, U18, U30	7404, (74LS04)	IC, Hex Inverter	3
U12	1488	RS232 Driver	1
U9	1489	RS232 Receiver	1
VR4	7805 (LM340T5)	Regulator, +5 volts	1
VR3	7812 (LM340T12)	Regulator, +12 volts	1
VR1	7905 (LM320T5)	Regulator, -5 volts	1
VR2	7912 (LM320T12)	Regulator, -12 volts	1
Y2		Crystal, 1.8432 MHz	1
Y1		Crystal, 1.8000 MHz,	1
[Y1]		[Crystal 36.000 MHz]	[1]
		Socket, IC, 40 Pin	1
		Socket, IC, 28 Pin	1
		Socket, IC, 24 Pin	2
		Socket, IC, 16 Pin	19
		Socket, IC, 14 Pin	15
U33, U23 , U1		Switch, DIP, 8 Pos.	3
U28, U31, U32		15 Resistor, 4.7K, Resistor Network	3
R8, R9, R1, R3, R7		Resistor, 1/4 Watt, 4.7K	5
R5		Resistor, 1/4 Watt, 330	1
R4		Resistor, 1/4 Watt, 1K	1
R2		Resistor, 1/4 Watt, 2.7K	1
[R2]		[Resistor, 1/4 Watt, 1.2K]	
R6		Resistor, 1/4 Watt, 22 Meg	1
C26 C1-C15		Capacitor, Ceramic, .1uf	16
C25		Capacitor, Ceramic, 56pf,	1
[C25]		[Capacitor, Ceramic, 20pf]	[1]
C22		Capacitor, Elec, 100uf, 25V	1
C23		Capacitor, Ceramic, 10pf	1
C24		Capacitor, Ceramic, 100pf	1
C16-C21		Capacitor, Tant, 1.5uf	6
[L1]		[Coil .1uh]	[1]
		Heat Sink (TO220)	1
		Screws, 6-32 x 1/2	4
		Nuts, Hex, # 6-32	4
		Washers, Lock. #6	4

D

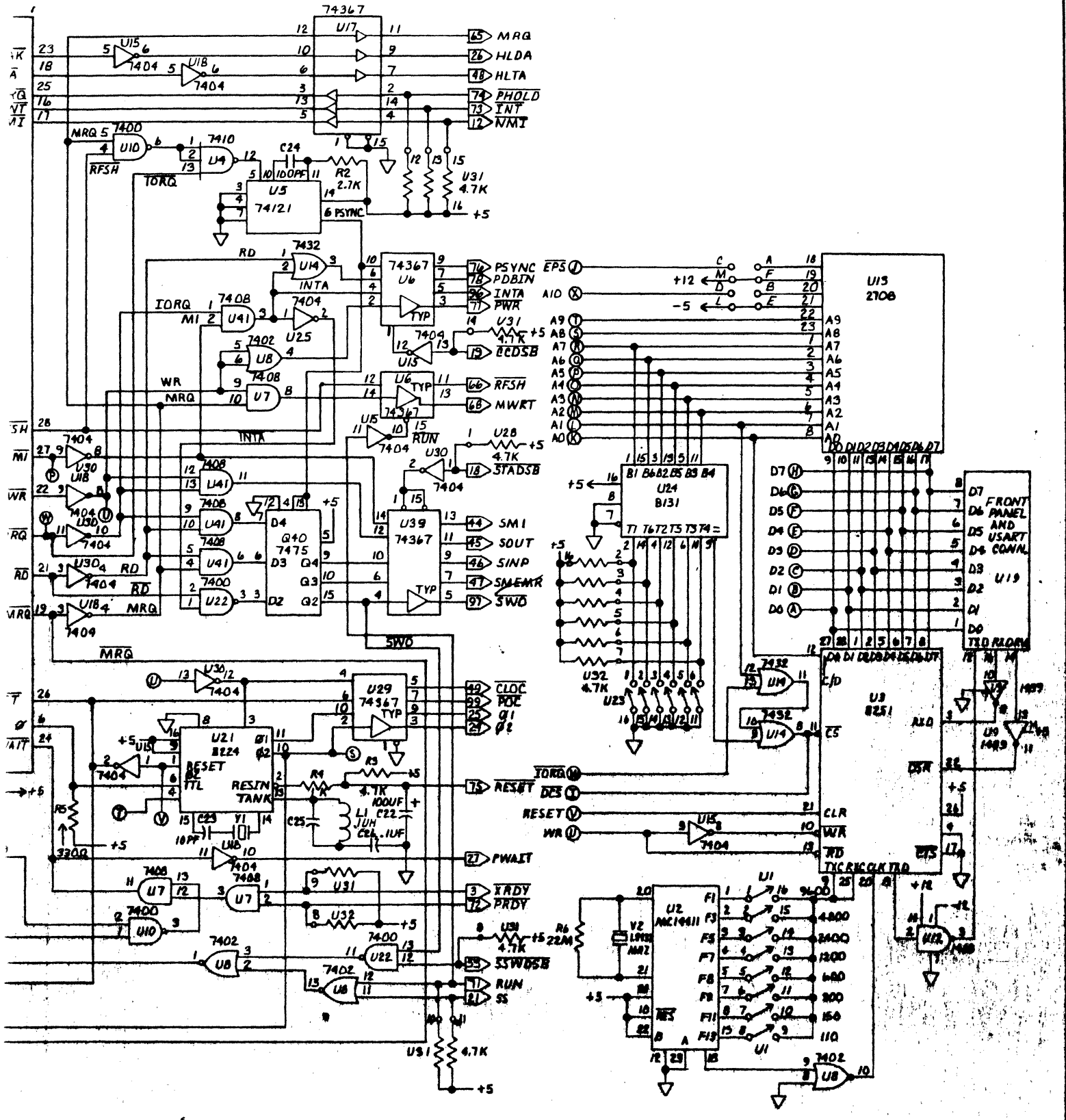
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REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



QTY		PART OR IDENTIFYING NO.		NOMINATING		REVISION	
REQD	REQD			DESCRIPTION			
PARTS LIST							
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES = = =				CONTRACT NO.		JADE Computer Systems	
MATERIAL		APPROVALS		DATE			
FINISH		DRAWN		6-22-79		BIG "Z" BOARD	
NEXT ASSY		CHECKED		ISSUED			
USED ON		SCALE		SIZE		DWG. NO.	
APPLICATION		DO NOT SCALE DRAWING		D		001 007	
						REV.	
						SHEET 1 OF 1	