VME-SCSI Host Adapter
Hardware Reference Manual

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PREFACE

This manual describes Integrated Solutions' VME-SCSI host adapter board and is divided into the following sections:

- Section 1 provides a product overview.
- Section 2 describes specifications.
- Section 3 describes how to configure and install the VME-SCSI board.
- Section 4 describes the software interface between the VME-SCSI and Host CPU.
- Appendix A provides disk parameters, (number of heads, number of cylinders, and formatting constants) for selected drives.

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SECTION 1: INTRODUCTION

1.1 Features

Integrated Solutions' VME-SCSI Host Adapter board is a 5¼-inch Winchester disk controller/formatter. The single VME double wide board adapts up to four Small Computer System Interface (SCSI) compatible Winchester disk drives to VME bus-based host processors. The VME-SCSI complies with all VME bus electrical specifications.

The VME-SCSI channels and controls the flow of information between the host memory and attached I/O devices. Thus, the VME-SCSI relieves the host CPU of direct communications with I/O devices and permits data processing to proceed concurrently with I/O operations. It accepts data from the host processor and converts it into information blocks and control signals that conform to the SCSI standard (ANSI X3T9.2). Full electrical and logical compatibility with this standard is provided, except for command chaining, disconnection, and reconnection.

1.2 Architecture

The VME-SCSI internal organization, shown in Figure 1-1, consists of a 16-bit control microprocessor, a host interface section, EPROM, RAM, and a SCSI Protocol Controller (SPC) that is implemented on a VLSI chip to handle the SCSI interface. These internal elements are attached to an address and data bus controlled by the microprocessor. Internal communication, as well as direct memory access (DMA), is under microprocessor program control. There is no specific DMA controller.

1.2.1 Control Microprocessor

The high-speed 16-bit microprocessor directly controls all communications across the VME host interface and sets up and monitors all operations to the SCSI interface, which is handled by the SCSI Protocol Controller (SPC). Use of a 16-bit microprocessor gives the VME-SCSI a higher level of functionality, independent of host processor intervention, than is possible with less intelligent controllers. Such functions as media formatting and defect analysis are performed completely in the VME-SCSI.

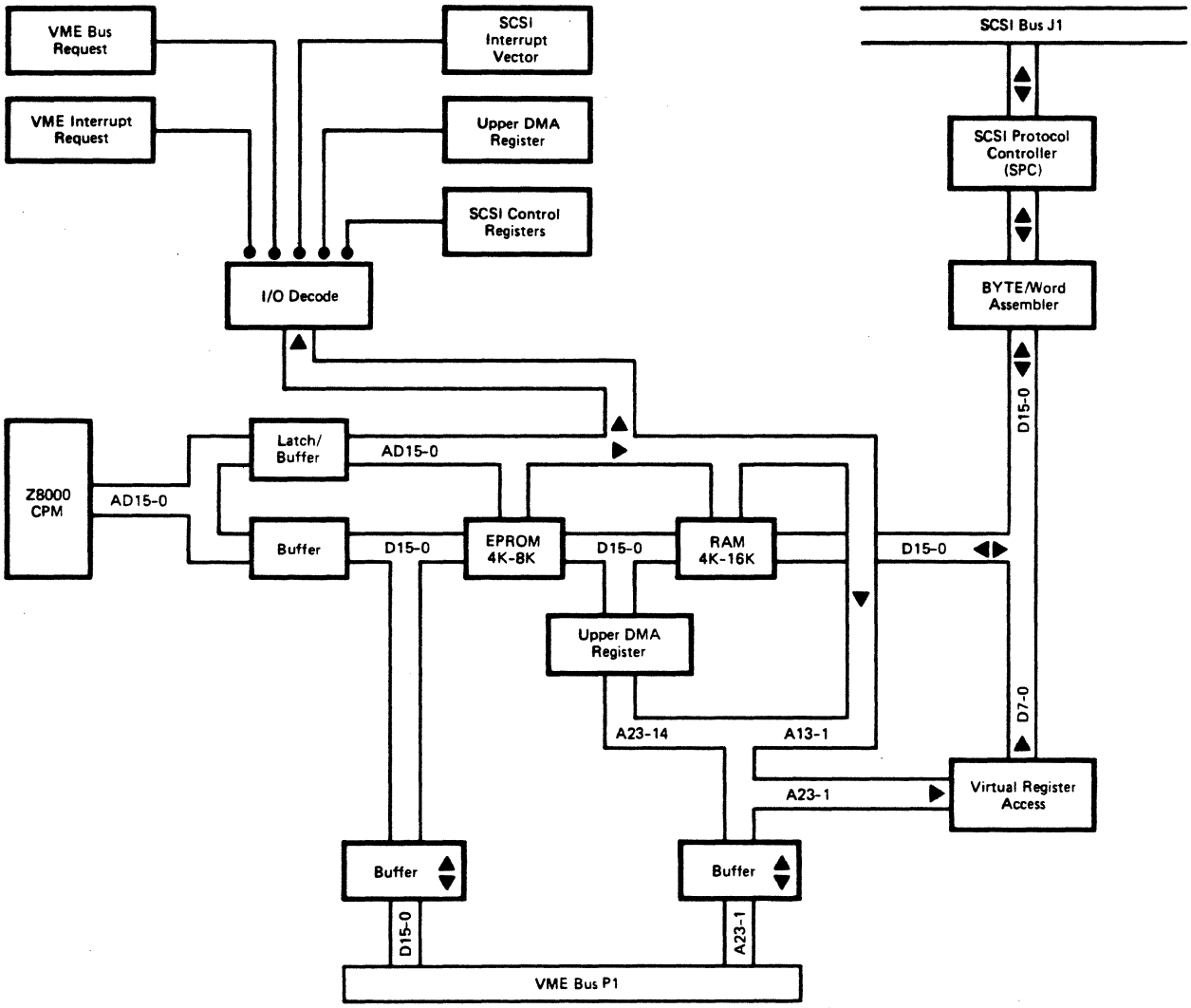

Figure 1-1. VME-SCSI Block Diagram

1.2.1.1 Control Microprocessor Memory Address Map

Memory address space mapping of the control microprocessor is represented in Table 1-1.

1.2.1.2 Control Microprocessor I/O Address Map

I/O ports and their respective port addresses referenced by the control microprocessor are defined in Table 1-2.

Table 1-1. Control Microprocessor Memory Address Map

Address Range	Access	Function
C000-FFFE	Host Memory	All memory references by control microprocessor occur within this range. Map to memory on the VME bus.
A000-BFFE	Rdport	Data read from device via SPC/SCSI.
8000-9FFE	Wrport	Data written to device via SPC/SCSI.
7000-7FFE	Accport	Address referenced by microprocessor when it is in a scan loop to sense if the host processor is accessing a register.
6000-6FFE	Regport	Address referenced by the microprocessor to determine which register was accessed and the type of access.
2000-5FFE	RAM Buffer	Assigned to internal buffer.
0000-1FFE	EPROM	Reserved for program op code operand reference.

Table 1-2. Control Microprocessor I/O Port Addresses

Address(H)	Port	Function
002E	ZBREQ	A reference to this port causes a Bus Request signal to be set on the VME bus.
002C	SACKRES	A reference to this port causes the Bus Busy signal to the VME bus to be reset. This would occur following a block move to host memory.
002A	SETIRQ	A reference to this port causes an Interrupt Request signal to the VME bus to be set.
0024	SUPRDMA	A reference to this port causes the internal data bus to be loaded into a register for subsequent gating onto the VME address bus Bits 23-14, during DMA transfers into VME memory.
0029	WRVECT	A reference to this port causes eight bits of the internal data bus to be loaded into a register for subsequent use as a vector number source for SPC interrupts.
0020	BRDRES	A reference to this port causes the reset to an enable control latch in the byte/word assembler/ disassembler logic. The latch is set by the first reference to either Wrport or Rdport.

1.2.2 Buffer RAM

All information is transferred between the peripheral devices and the VME bus memory through an on-board buffer memory implemented in either 2K x 8 or 8K x 8 static RAMs. This prevents data late (overrun) problems, which can occur with non-buffered controllers and adapters that are unable to acquire the host memory bus fast enough to prevent the loss of data due to a FIFO overflow.

There are two selectable buffer size options. The standard buffer is capable of buffering up to seven logical blocks (512 bytes/block). The high-capacity buffer is capable of storing up to thirty-one logical blocks.

Most available target controllers also contain single or double block buffers. Taking the target controller's buffers into consideration along with the VME-SCSIs, and assuming an ST506 5¼-inch disk drive, the standard buffer can store one-half track of data. The high-capacity buffer can store more than an entire track of data independent of additional mechanical latency beyond that of the initial access.

1.2.3 SCSI Protocol Controller

The SCSI Protocol Controller (SPC) is an interface sequencer chip designed to accommodate the Small Computer Systems Interface. The SPC is attached to the control microprocessor as a peripheral device. The SPC is accessed by reading and writing several internal registers, which are mapped into the control microprocessors I/O space. Table 1-3 lists the address and register ports inside the SPC. For more detailed information on the ports refer to the specifications for the SPC.

Table 1-3. SPC Addresses/Ports

Address (H)	Port
0001	SDATAREG
0003	SCMDREG
0005	SCNTLREG
0007	SDESTREG
0009	SAUXSTAT
000B	SIDREG
000D	SINTRREG
000F	SSRCREG
0013	SDIAGREG
0019	STRCREG2
001B	STRCREG1
001D	STRCREG0

The SPC is controlled directly by the VME-SCSI firmware. Command sequences are started when the firmware issues a Select Target command to the SPC. From that point on, the SCSI interface sequencing is performed by the SPC, independent of the microprocessor. Further communication between the control microprocessor and the SPC occurs by means of interrupts from the SPC, which occur whenever the SPC detects a bus condition that requires servicing beyond its internal capability.

DMA mode is also supported. The DMA interface signals from the SPC are interlocked with the firmware by means of the microprocessor wait signal.

1.2.4 EPROM

All VME-SCSI operations are controlled and monitored by the Adaptec firmware which resides in two EPROMs. Provision has been made for the selection of one or the other of two EPROM types: 2716 or 2732. This makes available either 2K or 4K words of PROM space.

The firmware is organized into two functional modules: a host interpreter and a SCSI command dispatcher. The VME-SCSI EPROMs that support the Adaptec ACB-4000/4070 consist of one high level EPROM (noted by H) and one low level EPROM (noted by L). The part numbers are 750022 (H) and 750023 (L).

1.2.4.1 Host Command Interpreter

The Host Command Interpreter controls all VME host interface sequences. It also processes the received commands and initiates the assembling of the required SCSI command and data structures. Upon completion of each SCSI command, the interpreter evaluates the status returned by the target controller and either advances to another SCSI command or assembles staus information to be returned to the host processor.

1.2.4.2 SCSI Command Dispatcher

The SCSI Command Dispatcher initiates the issuing of the command to the Target controller by initially setting up the SPC to execute a target selection. The dispatcher than controls the transfer of command and data blocks on a demand basis by means of interrupts from the SPC. Upon completion of command execution, the dispatcher assembles a status byte from the target controller into a word whose other byte reflects the VME-SCSI completion status. At that point, control is returned to the interpreter.

1.3 External Attachment Characteristics

The VME-SCSI board attaches to the VME bus via connector P1 and to the SCSI bus through connector J1 (see Section 2 for connector pin assignments). The following paragraphs discuss the VME host interface and the SCSI I/O device interface.

1.3.1 VME Host Interface

The host interface section provides interfacing capability consistent with the VME specification for the following VME-defined functional modules:

1. Data Transfer Bus Requester — This is the bus acquisition interface based on a Bus Request/Bus Grant protocol. There are actually four separate sets (0-3) of these lines defined by VME. Each set supports a *daisy chain propagation* priority scheme among multiple requesters within the set. Prioritization also exists between sets, with highest priority going to Request 3. All four sets are supported by the VME-SCSI.
2. Data Transfer Bus Master — This is the ability to initiate data transfer cycles across the Data Transfer Bus. Once acquisition of the bus has been granted, the VME-SCSI may directly access the host memory independent of the CPU.
3. Interrupter — The Interrupter performs three tasks. It asserts the interrupt request line, supplies a status/ID (vector) byte to the data bus when its request has been acknowledged, and propagates the interrupt acknowledge daisy chain signal if it is not requesting that level of interrupt. There are seven levels (1-7) of interrupt request priority supported by VME, with level 7 being the highest. The VME-SCSI can select one level from Levels 3-6; Levels 0-2 and 7 are not selectable.
4. Slave — This is the ability to respond to an access attempt by a master. Determination of an attempt to access is based on recognition of a certain address, set of addresses, or address range. The VME-SCSI responds to one of four sets of addresses, each set containing eight unique addresses.

The interface sequences for Requester, Master, and Slave read cycles are each tightly interlocked with the VME-SCSI firmware through assertion of the microprocessor wait signal until the proper interface signal has occurred. The Slave Read and Write cycles are each interlocked with the firmware by holding off the VME DTACK signal until the proper internal signal sequence has occurred.

The Interrupter cycles are initiated by firmware through the execution of an Out instruction which is latched up. Completion of the cycle beyond this point is a hardware function.

For more detailed information on the host interface, refer to VMEbus Specification, Rev. B.

1.3.2 SCSI I/O Device Interface

Communication between the VME-SCSI and attached peripheral devices occurs across the SCSI bus interface. Featured characteristics supported by this interface are

- Single or multiple host system.
- Multiple peripheral devices and device types.
- Prioritized arbitration resolution of bus contention.
- Asynchronous data transfer at up to 1.5 Mbytes/second.
- Host-to-host communication.

There are three SCSI-defined functions not supported by the present VME-SCSI implementation:

1. Command chaining
2. Disconnection
3. Reconnection

There are two communication roles defined for users of the interface: initiator and target. The VME-SCSI is an initiator.

Actual cycling of the interface itself is accomplished by the SCSI Protocol Controller (SPC) chip.

The SCSI data bus is eight bits wide, as is the SPC data bus to the VME-SCSI internal data bus. A byte/word assemble/disassemble hardware assist feature has been implemented between those two buses. This allows the DMA transfer cycles to the internal RAM buffer to occur 16 bits at a time rather than only eight.

For further details on this interface, refer to the SCSI specification.

1.4 Host I/O Registers

The host processor and any other attached bus masters access the VME-SCSI through eight 16-bit memory mapped I/O registers:

- Control and Status Register
- Disk Address Register
- Bus Address Register
- Word Count Register
- Address Extension Register
- Sense Word Registers (3)

1.5 Commands

The VME-SCSI supports several commands:

- Format
- Size
- Seek
- Read
- Write

1.6 Subsystem Configurations

The VME-SCSI, which is currently available in a factory-set configuration (Firmware set 4000), can support up to two target controllers each with two disk drives. Firmware set 4000 supports:

- Adaptec ACB-4000 - ST506 target
- Adaptec ACB-4070 - ST506 target with run length limit (RLL) encoding

With the Adaptec ACB-4070, the RLL encoding scheme is used to obtain an increased formatted drive capacity.

1.7 Formatting/Sector Mapping

The VME-SCSI automatically spares up to 128 bad blocks on each drive. At the completion of formatting, the drive appears error-free to the host.

1.8 Local Interrupts (Z8000)

Three interrupt types are supported, nonmaskable, nonvectored, and vectored. A nonmaskable interrupt occurs in the event of an attempt by the VME-SCSI to reference a non-existent location in host memory. A non-vectored interrupt occurs in the event of a Bus Clear signal on the host interface and is processed in the firmware by releasing and re-requesting the bus. The vectored interrupts are used by the SCSI controller chip to signal phase and state changes on the SCSI interface.

SECTION 2: SPECIFICATIONS

This section provides performance specifications, operating requirements, and options for the VME-SCSI.

2.1 Compatability

The VME-SCSI plugs into a VME bus based system and attaches to the Small Computer System Interface (SCSI) to support 5¼-inch disks.

2.1.1 System Bus

The VME-SCSI interfaces with the VME bus as defined in the *VMEbus Specification Manual*, Motorola part number MVMEBS/D1. Table 2-1 provides the pin assignments and signal mnemonics for the VME-SCSI VME bus connector, P1. (The P1 connector pin layout is given in Section 3, Figure 3-1.)

2.1.2 Small Computer System Interface (SCSI)

The VME-SCSI attaches to the SCSI standard as defined in ANSI X3T9.2 for 5¼-inch disk drives. The interface connection is via SCSI I/O port connector J1. Table 2-2 provides the J1 connector pin assignments. The J1 connector pin layout is shown in Section 3, Figure 3-1.

2.2 I/O Register Addresses

The host processor, and any other attached bus masters, access the VME-SCSI through eight jumper selectable memory mapped I/O registers. The factory default address for each I/O register is given in Table 2-3.

2.3 Target Controllers

Adaptec's ACB-4000 or ACB-4070 hard disk controller board interfaces ST506-type Winchester disk drives to the VME-SCSI host adapter as defined in Adaptec's *ACB-4000 Series User's Manual*. The ACB-4000, which controls two ST-506/412 or equivalent Winchester drives, supports standard SCSI features as well as extensions and uses MFM encoding. The ACB-4070 interfaces to ST506/412 or equivalent Winchester drives, but uses 2,7 run length limited (RLL) encoding.

Table 2-1. VME Bus Connector P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	VMED0	BBUSY*	VMED8
2	VMED1	BCLR*	VMED9
3	VMED2	ACFAIL*	VMED10
4	VMED3	BG0IN*‡	VMED11
5	VMED4	BG0OUT*‡	VMED12
6	VMED5	BG1IN*‡	VMED13
7	VMED6	BG1OUT*‡	VMED14
8	VMED7	BG2IN*‡	VMED15
9	GND	BG2OUT*‡	GND
10	SYSCLK†	BG3IN*‡	SYSFAIL*†
11	GND	BG3OUT*‡	VMEBERR*
12	VMEDS1*	BR0*†	SYSRESET*
13	VMEDS0*	BR1*†	LWRD*
14	VMEWR*	BR2*†	VMEAM5†
15	GND	BR3*†	VADD23
16	VMEDTACK*	VMEAM0†	VADD22
17	GND	VMEAM1	VADD21
18	VMEAS*	VMEAM2†	VADD20
19	GND	VMEAM3†	VADD19
20	VMEIACK*	GND	VADD18
21	IACKIN*‡	SERCLK†	VADD17
22	IACKOUT*‡	SERDAT†	VADD16
23	VMEAM4†	GND	VADD15
24	VADD7	IRQ7*†	VADD14
25	VADD6	IRQ6*	VADD13
26	VADD5	IRQ5*	VADD12
27	VADD4	IRQ4*	VADD11
28	VADD3	IRQ3*	VADD10
29	VADD2	IRQ2*†	VADD9
30	VADD1	IRQ1*†	VADD8
31	-12V†	+5V STDBY†	+12V†
32	+5V	+5V	+5V

NOTE:
In all tables in this manual, an asterisk (*)
following a signal name indicates a true low signal.

† VME bus signals, but no connection on VME-SCSI board.

‡ These signals are daisy-chained through the board, but no other connections are made.

Table 2-2. I/O Port Connector J1 Pin Assignments

Pin Number	Signal Mnemonic	Signal Name
2	DB0	Data Bus 0
4	DB1	Data Bus 1
6	DB2	Data Bus 2
8	DB3	Data Bus 3
10	DB4	Data Bus 4
12	DB5	Data Bus 5
14	DB6	Data Bus 6
16	DB7	Data Bus 7
18	DBP	Data Bus Parity
20	GND	Ground
22	GND	Ground
24	GND	Ground
26	TERMPWR	Terminator Power
28	GND	Ground
30	GND	Ground
32	ATN	Attention
34	GND	Ground
36	BSY	Busy
38	ACK	Acknowledge
40	RST	Reset
42	MSG	Message
44	SEL	Select
46	C/D	Control/Data
48	REQ	Request
50	I/O	Input/Output

Table 2-3. I/O Registers Default Addresses

Register	Default Address
Control/Status Register	FFFFE0
Disk Address Register	$FFFFE2_{16}$
Bus Address Register	$FFFFE4_{16}$
Word Count Register	$FFFFE6_{16}$
Address Extension Register	$FFFFE8_{16}$
Sense Word Register 0	$FFFFEA_{16}$
Sense Word Register 1	$FFFFEC_{16}$
Sense Word Register 2	$FFFFEE_{16}$

2.4 Interrupt Vector

The interrupt vector is jumper-selectable from one of the following:

60_{16}
64_{16}
68_{16}
$6C_{16}$
70_{16}
74_{16}
78_{16} (factory default)
$7C_{16}$

2.5 Transfer Rate

The transfer rates with the 5.6 MHz clock are

- 1.2 MBytes/Second burst from SCSI Adapter to SCSI Controller.
- 1.33 MBytes/Second burst from SCSI Controller to VME bus.

2.6 Diagnostic Indicator

An LED located on the VME-SCSI board provides diagnostic assistance.

2.7 Power Requirements

The VME-SCSI power requirements are +5V @ 3.1 amps.

2.8 Environmental

The suggested temperatures are

- 0 degrees centegrade to 50 degrees centegrade (operating).
- -40 degrees centegrade to 65 degrees centegrade (non-operating).

The suggested humidity is from 10 percent to 95 percent (noncondensing).

2.9 Form Factor

The form factor is a standard double-sized VME (160mm x 233.33mm).

SECTION 3: CONFIGURATION

This section describes how to configure and install the VME-SCSI board. Figure 3-1 is a layout of the VME-SCSI board that shows the jumper and switch locations.

3.1 Jumper Configuration

Jumpers are used for setting the desired configuration options for both the VME and SCSI interfaces. The jumpers are two position Berg type and are plugged on to pins mounted on the board spaced on one-hundredth inch centers.

3.2 VME Interface Jumpers

Jumpers E15 and E17 are set at the factory. E17 should always be installed. E15 should be installed with the Adaptec ACB-4000. With the Adaptec ACB-4070, E15 should be removed. The user-configurable jumpers for the VME interface are

- Host Control Registers
- Bus Request/Grant
- Interrupt Vector
- Interrupt Request Grant

3.2.1 Host Control Registers

The Host Control Registers can be mapped to one of four alternate sets of addresses within the VME memory address map based on jumper settings E18 through E21 (see Table 3-1). The jumpers allow the decoding of one or the other phases of VME address Bits 4 and 5. The factory default is jumpers at E18 and E21.

Table 3-1. Host Control Register Jumpers

Address Set	VMEA 5	VMEA 4	E18	E19	E20	E21
FFFFC0-FFFFCE	0	0	jmpr	open	jmpr	open
FFFFD0-FFFFDE	0	1	jmpr	open	open	jmpr
FFFFE0-FFFFEE	1	0	open	jmpr	jmpr	open
FFFFF0-FFFFFE	1	1	open	jmpr	open	jmpr

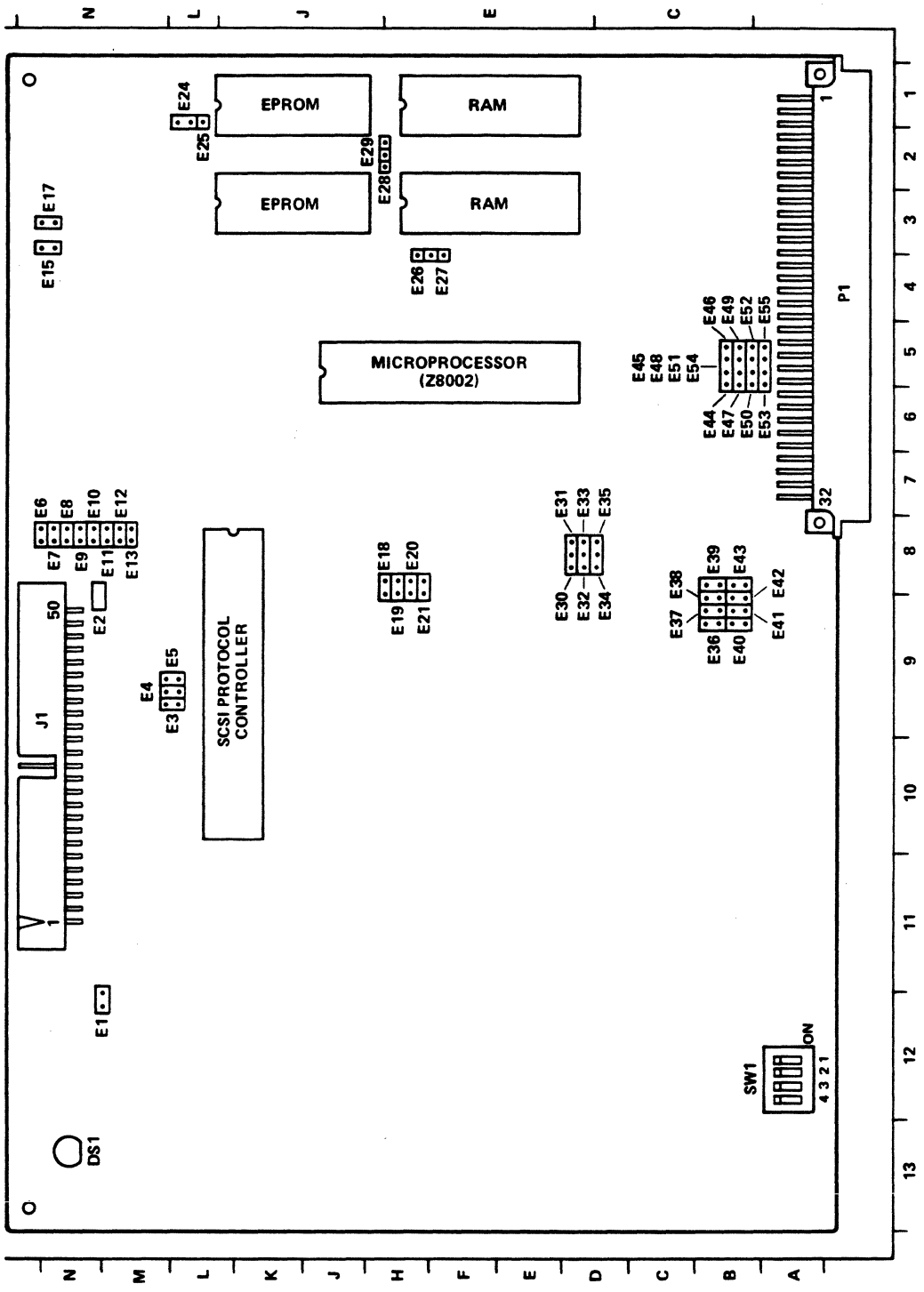

Figure 3-1. VME-SCSI Board Layout

3.2.2 Bus Request/Grant

There are four sets of Bus Request/Grant lines from which one set must be selected. Figure 3-2 represents the Bus Request selection jumpers as they appear on the board. One jumper is installed. The factory default is Bus Request 3 (BRQ3).

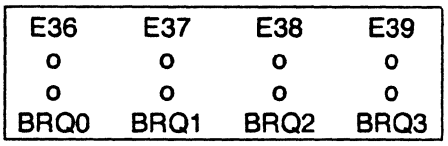

Figure 3-2. Bus Request Jumpers on the VME-SCSI Board

The jumpers which must be installed for the Bus Grant signals are represented in Figure 3-3. Refer to Table 3-2 for the correct jumper configuration based on the specific Grant being selected.

The Bus Request and Bus Grant levels selected must be the same.

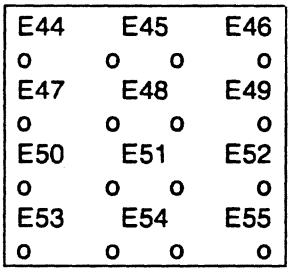

Figure 3-3. Bus Request Jumpers to be Installed

Table 3-2. Bus Grant Jumper Configurations

Bus Grant 0			Bus Grant 1		
E44 jmpr	E45 open	E46 jmpr	E44 open	E45 jmpr	E46 open
E47 open	E48 jmpr	E49 open	E47 jmpr	E48 open	E49 jmpr
E50 open	E51 jmpr	E52 open	E50 open	E51 jmpr	E52 open
E53 open	E54 jmpr	E55 open	E53 open	E54 jmpr	E55 open
Bus Grant 2			**Bus Grant 3**		
E44 open	E45 jmpr	E46 open	E44 open	E45 jmpr	E46 open
E47 open	E48 jmpr	E49 open	E47 open	E48 jmpr	E49 open
E50 jmpr	E51 open	E52 jmpr	E50 open	E51 jmpr	E52 open
E53 open	E54 jmpr	E55 open	E53 jmpr	E54 open	E55 jmpr

3.2.3 Interrupt Vector

The interrupt vector is specified by setting jumpers E30 through E35 as shown in Figure 3-4. Table 3-3 shows the correct jumper configuration for each possible vector number.

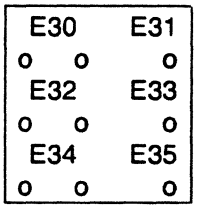

Figure 3-4. Interrupt Vector Jumpers

Table 3-3. Interrupt Vector Jumper Configurations

Vector #(h)	E30	E31	E32	E33	E34	E35
60	open	jmpr	open	jmpr	open	jmpr
64	open	jmpr	open	jmpr	jmpr	open
68	open	jmpr	jmpr	open	open	jmpr
6C	open	jmpr	jmpr	open	jmpr	open
70	jmpr	open	open	jmpr	open	jmpr
74	jmpr	open	open	jmpr	jmpr	open
78	jmpr	open	jmpr	open	open	jmpr
7C	jmpr	open	jmpr	open	jmpr	open

The factory default is vector 78.

3.2.3.1 Interrupt Request/Grant

There are four Interrupt Request lines from which one must be selected. Figure 3-5 represents the Interrupt Request (IRQ) selection jumpers. One jumper is installed. The factory default is level IRQ6.

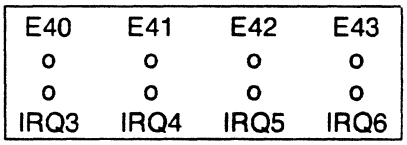

Figure 3-5. Interrupt Request Jumpers

3.3 SCSI Interface Jumpers

The SCSI interface jumpers are

- SPC ID
- SCSI Arbitration Level
- SCSI Termination
- RAM

3.3.1 SPC ID0*-ID2*

Three low true input signals to the SPC chip are used to encode the SCSI bus ID assigned to the VME-SCSI. Figure 3-6 represents the SPC ID jumpers on the VME-SCSI board. Table 3-4 specifies the correct jumper configuration for each bus ID. The factory default is Bus ID 7.

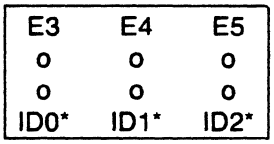

Figure 3-6. SPC Jumpers

Table 3-4. SPC Jumper Configurations

Bus ID	E5	E4	E3
0	open	open	open
1	open	open	jmpr
2	open	jmpr	open
3	open	jmpr	jmpr
4	jmpr	open	open
5	jmpr	open	jmpr
6	jmpr	jmpr	open
7	jmpr	jmpr	jmpr

3.3.2 SCSI Arbitration Level

Each SCSI bus user has a unique arbitration level for gaining access to the bus. This level is established by jumpering the buffered arbitration output signal from the SPC to one of the eight data bus lines. Figure 3-7 represents the jumper pins as they appear on the VME-SCSI board. Install one jumper as appropriate for the required arbitration level. The factory default is level 7.

Jumper Position	Arbitration Level
o E06 o	0
o E07 o	1
o E08 o	2
o E09 o	3
o E10 o	4
o E11 o	5
o E12 o	6
o E13 o	7

Figure 3-7. Arbitration Level Jumper Configurations

3.3.3 SCSI Termination

If the VME-SCSI board is positioned at one or the other of the ends of the SCSI bus, it must provide terminators for the bus signals. In that case, jumpers must be installed on E1 and E2.

3.3.4 Hi/Lo* RAM

Two internal RAM buffer sizes are available on the VME-SCSI board, 2K x 8 or 8K x 8 static RAMs. Jumpers E26, E27, E28, and E29 must be configured in accordance with the information provided in Table 3-5.

Table 3-5. Hi/Lo RAM Jumper Configurations

Jumper Number	2K x 8	8K x 8
E26	jmpr	open
E27	open	jmpr
E28	jmpr	open
E29	open	jmpr

If the VME-SCSI board is being configured for the 2K buffer option, a jumper is also required at E17.

3.4 Dipswitch (SW1)

SW1 is a four-position switch that implements two functions on the VME-SCSI board. These functions include

- Interrupt Acknowledge
- Disk Format Enable

3.4.1 Interrupt Acknowledge

The interrupt acknowledge code is configured based on the selected Interrupt Request line. Bits 1-3 on SW1 are used to set this code.

Table 3-6 indicates the correct switch settings for each Interrupt Request line selection.

Table 3-6. Interrupt Request Switch Settings

Interrupt Request Line	Bit 1	Bit 2	Bit 3
3	open	open	closed
4	closed	closed	open
5	open	closed	open
6	closed	open	open

The factory default is 6.

3.4.2 Format Enable

To disable disk formatting, set Bit 4 of SW1 off.

3.5 LED

A diagnostic LED is located at position 3N on the VME-SCSI board. This LED is available as a diagnostic aid. The LED blinks codes of long and short duration. At initial power-up, the LED blinks 16 times (approximately 30 seconds) allowing all disks to come up to speed. After the power-up sequence, the LED is used to describe subsystem errors. The LED error codes are described in Table 3-7.

Table 3-7. LED Error Codes

LED Indicator				Description
short	short	short	long	Could not home the drive
short	short	long	short	Drive not ready
short	short	long	long	Seek never completed
short	long	short	short	Cannot find drive 0 on power-up
short	long	short	long	Write fault
short	long	long	short	Drive not connected
short	long	long	long	SPC phase change or self test error
long	short	short	short	SCSI target selection failed
long	short	short	long	Target controller error

SECTION 4: SOFTWARE INTERFACE

4.1 Introduction

This section describes the software interface between the VME-SCSI and Host CPU.

4.2 Host Interface Protocol

The VME-SCSI/Host CPU interface protocol is based on the exchange of control and status information through eight addressable 16-bit registers. These registers can be accessed by the host CPU like any location in host memory, providing the VME-SCSI is *ready*. If it is *busy* (not *ready*) data cannot be transferred to or from the registers, although a mechanism is provided to complete the access cycle. A unique host memory address is assigned to each register as shown in Table 4-1.

NOTE

Byte access to these registers is not supported.

Table 4-1. Register Addresses

VME Bus Address	Register Name
FFFFx0h	Control/Status Register
FFFFx2h	Disk Address Register
FFFFx4h	Bus Address Register
FFFFx6h	Word Count Register
FFFFx8h	Address Extension Register
FFFFxAh	Sense Word Register 0
FFFFxCh	Sense Word Register 1
FFFFxEh	Sense Word Register 2

NOTE

x is jumper-selectable as *C*, *D*, *E* (factory default), or *F*.

This high-level host interface protocol permits a simple sequence of operation for software drivers:

1. The Disk Address Register and Address Extension Register are written with the starting logical block number to be read or written.
2. The Bus Address Register and Address Extension Register are written with the beginning host address to be read or written.
3. A positive word count is written into the Word Count Register indicating the number of words to be transferred.

These operations can be completed in any order. The final operation is to write the Control/Status Register with the command to be executed. The command consists of the command code, the drive number (in the device select bits), controller busy bit (bit is set), and optional interrupt enable bit. If the interrupt enable bit is set, the controller will interrupt when the operation completes successfully, or terminates due to an error. If the interrupt enable bit is not set, the host can poll the CSR for command completion.

4.3 Interrupt Vectors

The VME-SCSI initiates communication with the host by issuing a host interrupt request to one of eight jumper-selectable interrupt vector addresses: 60h, 64h, 68h, 6Ch, 70h, 74h, 78h (factory default), or 7Ch. Instructions for setting the interrupt vector are given in Section 3.

4.4 Registers

As discussed in Section 4.2, VME-SCSI/Host CPU exchange control and status information via eight addressable registers. These registers are

- Control Status Register
- Disk Address Register
- Bus Address Register
- Word Count Register
- Address Extension Register
- Sense Word Registers (3)

Each register is discussed in more detail in the paragraphs that follow.

4.4.1 Control Status Register (CSR)

The Control Status Register (CSR) is a 16-bit word addressable register. Bits 1 through 9 can be read or written; the other bits can only be read. Figure 4-1 shows the CSR format. The meaning of the individual fields and bits are provided in Tables 4-2 and 4-3.

When the controller is initialized, Bits 1-6 and 8-13 are cleared and Bit 7 is set. Bit 0 is set whenever the selected device is in the ready condition; otherwise the bit is cleared. Bit 14 is set whenever the selected device is busy, such as when a seek is in progress; it is cleared when the busy condition has cleared. Bit 15 is set whenever a VME-SCSI, target controller or device error has occurred. Further definition of the error is indicated in Bits 13-10.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE OR MR P	DB ES VY	Error Field				DS EE VL 0	DS EE VL 1	CB TS LY R	IE NN TB L	Not Used		CMD Field			Not Used

Figure 4-1. Control Status Register Format

Table 4-2. CSR Bit Definitions (Bits 0-9)

Bit(s)	Function	Description
Bit 0		Not used.
Bits 3-1	Command Field	The specific command to be executed by the target device is indicated in this field, set by the host software. See Table 4-4.
Bits 5-4		Not used.
Bit 6	Interrupt Enable	This bit, set by the host software, allows the VME-SCSI to interrupt the host processor upon normal or error command termination.
Bit 7	Controller Busy	When cleared by the controller, this bit indicates to the host software that the controller is ready to accept a command. When set by the host software, this bit indicates to the controller that a command to be executed has been set in Bits 3-1.
Bits 9-8	Drive Select (DS0,DS1)	This field of two encoded bits is set by the host software to indicate for which of up to four target devices the command is intended.

Table 4-3. CSR Bit Definitions (Bits 10-15)

Bit(s)	Function	Description
Bits 13-10	Error Field	The bits within this field are each individually significant, i.e., an error indicated in this field is not represented by an encoding of the four bits but rather, may be any combination, with the on or off state of one bit having no effect on the meaning of another bit.
Bit 10	Operation Incomplete	The command has terminated prior to completion of the operation to be performed as specified by the command.
Bit 11	SCSI Target Check	An error has been detected by the target controller. Specific details relating to that error are available in Sense Words 0-2.
Bit 12	Host Adapter Check	An error has been detected by the VME-SCSI. The SCSI command that was active at the time of failure and the corresponding error code is available in Sense Word 0.
Bit 13	Non-Existent Memory	The VME-SCSI has attempted to reference a location in host memory from which there has been no response.
Bit 14	Device Busy	This bit is set by the host adapter whenever the host CPU attempts to select a target device that is busy, e.g., a disk with a seek in progress.
Bit 15	Composite Error	This bit is set by the VME-SCSI to indicate one or more of the bits in the error field (Bits 13-10) has been set. If the Interrupt Enable bit (Bit 6) has been set, and an error occurs (which also sets Bit 7), an interrupt will be initiated.

Table 4-4. Command Codes

Bit 3	Bit 2	Bit 1	Definition
0	0	0	Format
0	0	1	N/A *
0	1	0	Size
0	1	1	Seek
1	0	0	N/A
1	0	1	Write Data
1	1	0	Read Data
1	1	1	N/A

* Not assigned

4.4.2 Disk Address Register (DAR)

The Disk Address Register (DAR) is a 16-bit word addressable register. All 16 bits can be read or written by the host processor. The DAR is cleared by either initializing the device or by loading the register with zeros. It can have one of two meanings depending upon whether a Data Transfer (Read or Write) or Format command is being executed. The meaning and format of the DAR fields are shown and described in the Read/Write and Format Command descriptions (see Sections 4.5.4.1 and 4.5.5).

4.4.3 Bus Address Register (BAR)

The Bus Address Register (BAR) is a 16-bit register (see Figure 4-2). All 16 bits of this register can be read or written by the host processor. It is used as a pointer during data transfer operations to specify the two low-order address bytes of the first location in VME host memory to/from which data is to be transferred. The high-order byte is specified in the Address Extension Register (AER).

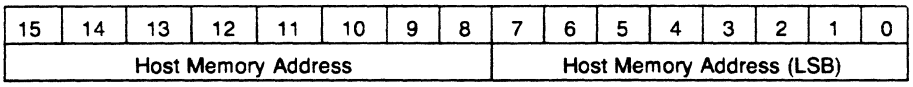

Figure 4-2. Bus Address Register Format

4.4.4 Word Count Register (WCR)

The Word Count Register (WCR) is a 16-bit register (see Figure 4-3). All 16 bits of this register can be read or written by the host processor. The WCR is used during data transfer operations to specify the total number of words to be transferred to/from VME host memory.

If a data transfer operation does not proceed to completion, this register contains a residual count indicating the number of words that failed to transfer to/from VME host memory.

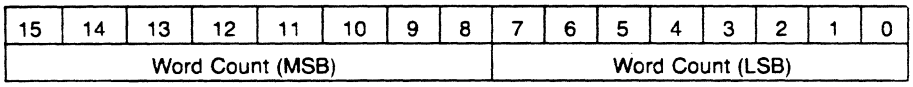

Figure 4-3. Word Count Register Format

4.4.5 Address Extension Register (AER)

The Address Extension Register (AER) is a 16-bit register (see Figure 4-4). All 16-bits of this register can be read or written by the host processor. The AER is used as a pointer during data transfer operations to specify the high-order address byte of the first location in VME host memory to/from which data is to be transferred and the high-order byte of the first logical block address on the I/O device to/from which data is to be transferred. The low-order bytes for each of these source/destination addresses are specified in the Disk Address Register (DAR) and the Bus Address Register (BAR).

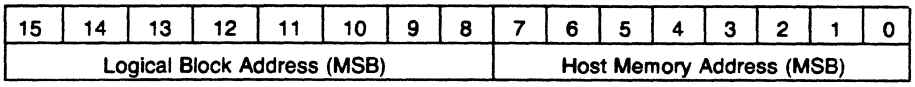

Figure 4-4. Address Extension Register Format

4.4.6 Sense Word Registers (SWR0, SWR1, SWR2)

The Sense Word Registers hold information about commands that terminate due to an error.

4.4.6.1 Sense Word Register 0

The VME-SCSI loads Sense Word Register 0 (SWR0) in the event of either of two abnormal occurrences:

1. A sequence control error (CSR Bit 12) within the VME-SCSI is detected.
2. An error is detected by the target controller. The occurrence of this type of error is signalled to the VME-SCSI by means of a premature SCSI status phase accompanied by the *check* bit set in the completion status returned by the target controller. This event is initially indicated to the host processor by the setting of CSR Bit 11.

Table 4-5 gives the bit definitions for SWR0.

Table 4-5. Sense Word 0 Register Bit Definitions

Bit(s)	Function	Description
Bits 15-8	SCSI Command Op Code	This field indicates the op code for the SCSI command being executed at the time of the error. Specific op codes and their meanings are defined in Table 4-6.
Bits 7-0	VME-SCSI Completion Code	This field contains errors detected by the VME-SCSI, the result of which was the setting of CSR Bit 12 and premature termination of the operation in progress as defined in the SCSI command op code field of this sense word. See Table 4-7.

Table 4-6. SCSI Command Op Codes

Op Code	Command	Op Code	Command
00	Test Unit Ready	0F	Translate
01	Rezero Unit	13	Write Buffer
03	Request Sense	14	Read Buffer
04	Format Unit	15	Mode Select
08	Read	1A	Mode Sense
0A	Write	1B	Start/Stop Unit
0B	Seek	1D	Send Diagnostic
25	Read Capacity	2E	Write and Verify
28	Read (Extended)	2F	Verify
2A	Write (Extended)	31	Search Data Equal

NOTE

These codes are not required by the SCSI spec, but they are, in general, the codes used by most disk target controller vendors.

Table 4-7. VME-SCSI Completion Codes

Code	Error
00	No Errors
01	Interrupt Error (SPC)
02	Adapter Control Check
04	Phase Change Error
08	Selection Error
10	Self Test Error (SPC)
20	Bad Media (Too Many Defects)

4.4.6.2 Sense Word Register 1

The VME-SCSI loads Sense Word Registers 1 and 2 when an error is detected by the target controller. Figure 4-5 shows the SWR1 format. Table 4-8 gives this register's bit definitions.

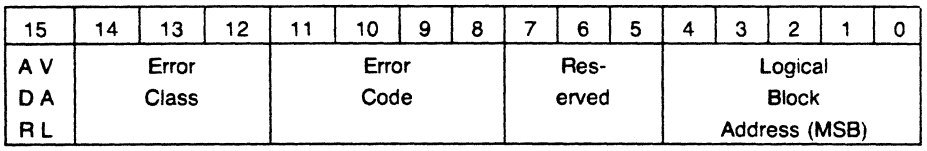

Figure 4-5. Sense Word Register 1 Format

Table 4-8. SWR1 Bit Definitions

Bit	Function	Description
Bit 15	Address Valid	This bit indicates that the logical block address field contains valid information.
Bits 14-12	Error Class	The two following fields indicate the failure in terms of an error class and an error code. This field expresses the error in terms of one of three possible classes. 1. Class 0: Drive Errors 2. Class 1: Target Controller Errors 3. Class 2: System Related Errors
Bits 11-8	Error Code	This field indicates a code which defines the specific failure. Refer to Tables 4-9, 4-10, and 4-11 for Class 0, 1, and 2 error codes.
Bits 7-5		Reserved
Bits 4-0	Logical Block Address	Most significant byte

Table 4-9. Class 0 Error Codes

Code	Error
00	No Sense
01	No Index Signal
02	No Seek Complete
03	Write Fault
04	Drive Not Ready
06	No Track 00

Table 4-10. Class 1 Error Codes

Code	Error
10	ID CRC Error
11	Uncorrectable Data Error
12	ID Address Mark Not Found
13	Data Address Mark Not Found
14	Record Not Found
15	Seek Error
16-17	Not Assigned
18	Data Check In No Retry Mode
19	ECC Error During Verify
1A	Interleave Error
1B	Not Assigned
1C	Unformatted Or Bad Format On Drive
1D	Self Test Failed
1E	Too Many Bad Blocks
1F	Not Assigned

Table 4-11. Class 2 Error Codes

Code	Error
20	Invalid Command
21	Illegal Block Address
22	Not Assigned
23	Volume Overflow
24	Bad Argument
25	Invalid Logical Unit (Device) Number
26-2F	Not Assigned

4.4.6.3 Sense Word Register 2

Sense Word Register 2 contains the remaining two bytes of the target device logical block address. Figure 4-6 illustrates the SWR2 format.

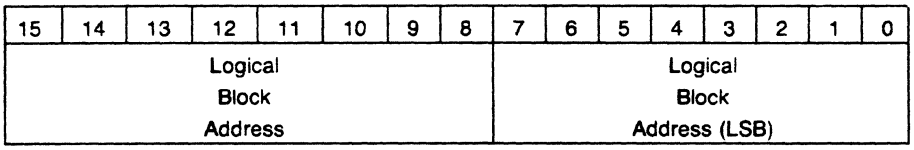

Figure 4-6. Sense Word Register 2 Format

4.5 Command Descriptions

The following paragraphs describe the commands supported by the VME-SCSI, specify the associated parameters and describe command completion results that can be expected following command execution.

4.5.1 Seek Command

The seek command (CSR Bits 3-1, Op Code 100) is used to position the addressed drive to the logical block specified. (The logical block address must also be specified for reads and writes following a seek.) Upon initiation of the seek, controller ready and drive ready status bits are set, and providing the interrupt enable bit was set in the CSR by the host, a host interrupt request is activated.

4.5.2 Size Command

The size command (CSR Bits 3-1, Op Code 010) returns the formatted geometry of the specified disk drive in the following registers:

1. DAR provides the number of heads
2. BAR provides the block size
3. WCR provides the number of sectors per track
4. AER provides the number of formatted cylinders

Upon successful completion of the size command, controller ready and drive ready status bits are set, and providing the interrupt enable bit was set in the CSR by the host, a host interrupt request is activated.

4.5.3 Write Data Command

The Write Data command (CSR Bits 3-1, Op Code 101) transfers information from host memory to the addressed device. Certain parameters related to the transfer must be specified in the addressable registers prior to writing the command to the CSR.

1. Logical Block Address - The address of the logical block on the device to which data is to be written must be specified in the DAR and the most significant byte of the AER.
2. Host Memory Address - The first memory address in host memory from which the transferred data is to be fetched must be specified in the BAR and the least significant byte of the AER.
3. Word Count - The total number of words to be transferred is specified in the WCR.

Upon successful completion of the transfer, controller ready and drive ready status bits are set, and providing the interrupt enable bit was set in the CSR by the host, a host interrupt request is activated.

If the transfer failed to complete successfully, additional status bits are set as required and, if appropriate, information relating to the failure is stored in the SCSI sense word registers.

4.5.4 Read Data Command

The Read Data command (CSR Bits 3-1, Op Code 110) transfers information from the addressed device to host memory. Certain parameters related to the transfer must be specified in the addressable registers prior to writing the command to the CSR.

1. Logical Block Address - The address of the logical block on the device from which data is to be read must be specified in the DAR and the most significant byte of the AER.
2. Host Memory Address - The first memory address in host memory to which the transferred data is to be stored must be specified in the BAR and the least significant byte of the AER.
3. Word Count - The total number of words to be transferred is specified in the WCR.

Upon successful completion of the transfer, controller ready and drive ready status bits are set, and providing the Interrupt Enable bit was set in the CSR by the host, a host interrupt request is activated.

If the transfer failed to complete successfully, additional status bits are set as required and, if appropriate, information relating to the failure is stored in the SCSI sense word registers.

4.5.4.1 DAR During Read/Write/Seek Command

For a read or write command, the DAR is loaded with the two low-order bytes of the address of the first logical block to be transferred (see Figure 4-7). This register is not updated with successive block transfers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Logical Block Address								Logical Block Address (LSB)							

Figure 4-7. DAR During Read/Write Command

4.5.5 Format Command

For a Format command (CSR Bits 3-1, Op Code 000), the DAR contains three separate information fields as shown in Figure 4-8. Table 4-12 gives the DAR bit definitions during a format command. Bit 15 represents the command modifier field and specifies the performance

of one of two different functions. The remaining two fields each specify parameters related to the execution of the Format Disk command modifier.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cmd. Mdfr	Maximum Head				Maximum Cylinder										

Figure 4-8. DAR During Format Command

Table 4-12. DAR Bit Definitions During Format Command

Bit(s)	Function	Description
Bit 15	Command Modifier Field	Action by the VME-SCSI upon receipt of a Format command varies depending upon the decode of these bits. See Table 4-13.
Bits 14-11	Maximum Head	This field, used only for the Format Disk command modifier, specifies the number of data surfaces on the drive, minus one.
Bits 10-0	Maximum Cylinder	This field, used only for the Format Disk command modifier, specifies the number of cylinders on the drive, minus one.

Table 4-13. Format Command Modifier Field in the DAR

Bit 15	Meaning
0	Format Disk
1	Read Parameter Defect List

4.5.5.1 Format Disk

A drive is formatted in one operation. This is accomplished by placing the format parameters for the addressed drive in the remaining fields of the DAR prior to writing the command to the CSR. A successful format should have a value of 0 in the CSR on completion. After a successful format, the system should be reset to allow correct power-up recognition of the drive.

4.5.5.2 Read Parameter and Defect Lists

This command performs two functions, it reads the parameter list and the defect list.

The command reads from the disk the parameter list provided to the SCSI target controller at the time the disk was formatted. The list contains four sections, the first three of which conform precisely to the SCSI specified format for Mode Select Parameter, Extent Descriptor, and Drive Parameter lists respectively. The fourth section specifies the total number of data blocks available to the host.

The list is placed in host memory starting at location 1000H and is 26 bytes in length. Specific byte format in terms of host memory addresses is shown in Table 4-14.

The command also reads the defect list for the addressed drive. It is then appended in host memory to the last parameter list word. The list conforms to the SCSI specified format. The

length of the defect list is variable as a function of the number of defects found on the disk. Length = 8n+4 where n (number of defects)</=128.

Byte format in terms of host memory addresses is shown in Table 4-15.

Table 4-14. Parameter List Format

Address(H)	Function	Code(H)	F/V (Fixed/Variable)
1000-1002	Reserved	00 00 00	F
1003	Extent Descriptor Length	08	F
1004	Density Code	00	F
1005-1008	Reserved	00 00 00 00	F
1009-100B	Block Size	00 20 00	V (512 bytes)
100C	List Format Code	01	F
100D-100E	Cylinder Count	01 32	V (306 cyl.'s)
100F	Head Count	04	V (4 heads)
1010-1011	Reduce Write Current Cyl.	01 00	V (Cyl. 256)
1012-1013	Write Pre-Compensation Cyl.	01 00	V (Cyl. 256)
1014	Landing Zone Position	08	V
1015	Step Pulse Rate	01	V
1016-1017	Number of Blocks	51 46	V (21830)

Table 4-15. Parameter and Defect List Format

Address(H)	Field Definition	Code(H)	F/V (Fixed/Variable)
101A-101B	Reserved	00 00	F
101C-101D	Defect List Length	xx xx	V (8n+4)
101E-1020	Cylinder Number	xx xx xx	V (Definition 1)
1021	Head Number	xx	V (Definition 1)
1022-1025	Byte Offset *	xx xx xx xx	V (Definition 1)

* From index

Format from 101F to 1025 is repeated "n" times.

APPENDIX A: DISK PARAMETERS FOR SELECTED DRIVES

This appendix contains formatting constants for a selected group of disk drives supported by the VME-SCSI controller. Table A-1 provides information for the VME-SCSI board; the table is not complete nor is it an endorsement of any drive or drive manufacturer.

Table A-1. Disk Drives and Formatting Constants

Manfacturer	Model	Heads	Cyl	Format Constant
AMPEX	PYXIS 13	4	322	1941
AMPEX	PYXIS 20	6	322	2941
AMPEX	PYXIS 27	8	322	3941
CDC	WREN 9415-3	3	697	12B8
CDC	WREN 9415-5	5	697	22B8
CDC	WREN-II	9	918	4395
FUJITSU	M2241	4	754	1AF1
FUJITSU	M2242	7	754	32F1
FUJITSU	M2243	11	754	52F1
IMI	5006H	2	322	0941
IMI	5012H	4	322	1941
IMI	5018	6	322	2941
MAXTOR	1065	7	918	3395
MAXTOR	1085	8	1024	5395
MAXTOR	1105	11	918	5395
MAXTOR	1140	15	918	7395
MICROPOLIS	1302	3	830	133D
MICROPOLIS	1303	5	830	233D
MICROPOLIS	1304	6	830	2B3D
QUANTUM	520	4	512	19FF
QUANTUM	530	6	512	29FF
QUANTUM	540	8	512	39FF
RHODIME	202	4	322	1941
RHODIME	202	6	322	2941
RHODIME	202	8	322	3941
VERTEX	V130	3	987	1BDA
VERTEX	V150	5	987	23DA
VERTEX	V170	7	987	33DA
VERTEX	V185	7	1166	348D