MODEL 3203 SYSTEM

Service Manual

47-087 R18

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PREFACE

The information in this manual is provided to permit authorized technicians to install, operate, and service Model 3203 Systems manufactured by the Concurrent Computer Corporation. This installation and service manual is divided into five chapters, an index and a drawing set.

Chapter 1 contains a general description of the Model 3203 System hardware and options. This chapter also includes the system block diagram and an analysis of the bus structure of the system.

Chapter 2 describes system power requirements and the physical configuration of the cabinet.

Chapter 3 provides installation information such as strapping, cabling, and initial setup/startup procedures. The startup procedure includes information describing the autoload sequence.

Chapter 4 gives a detailed circuit analysis of the power supply board. All other components of the system, including the central processor unit (CPU)/memory board, are described at a higher functional level. This approach was taken because detailed descriptions of these products are provided in separate manuals.

Chapter 5 provides a list of available diagnostics and a general troubleshooting guide.

The manual contains reference drawings that may be required to install and service the Model 3203 System. Drawings for components of the system that are provided in other manuals are not repeated herein.

Revision R18 contains revisions R02 through 18. This manual has been significantly revised to incorporate the new Model 3203 System (01-339) configurations with the embedded controller SCSI disk and tape drive units. For the convenience of previous users, all pertinent information for the earlier system (01-277) has been retained in this manual. In addition, and as applicable, all outstanding ECNs since the release of revision R01 have been incorporated in the manual. These included the addition of a new tape controller (35-999) for use in 01-277 systems. All detailed analysis in Chapter 4 concerning the CPU/memory board has been deleted. This information now resides in the 35-864 Central Processing Unit (CPU)/Memory Board Theory of Operation Manual.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 3203 System is a compact 32b computing system ideally suited for use in an office environment. The basic Model 3203 System (Figure 1-1) consists of a slender vertical desk-high cabinet. The basic cabinet contains a control panel, a central processing unit (CPU)/memory board, an intelligent peripheral controller (IPC) board, and a modular power supply board. The cabinet also contains a 5.25" Winchester-type disk drive and a streaming tape drive along with their respective controllers. These controllers (disk and tape) can be external to the drive units; or they may be an integral part of the units, depending upon the type of system purchased. The differences between the two types of systems are specified in Section 1.2.

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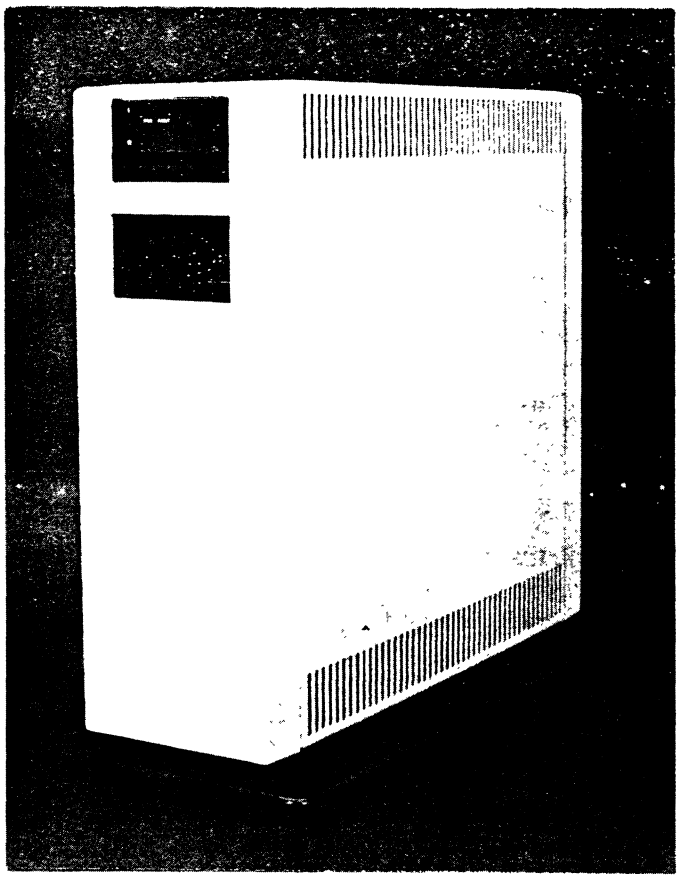

Figure 1-1 Model 3203 System

Options for the Model 3203 System include a second 5.25" disk, memory expansion on the CPU/memory board up to 4MB, a second MPC board, an Ethernet data link controller (EDLC) and a universal logic interface (ULI) board. Two spare input/output (I/O) slots are provided in the chassis to accommodate any two of these three boards. A Model 6100 or 6312 video display unit (VDU) is required as the system console.

This manual provides authorized technicians and customer service engineers with the information necessary to install and service a Model 3203 System. This chapter defines the equipment complement of the Model 3203 Systems; briefly describes each major assembly; and provides an overview of the internal architecture and bus stucture of the system.

1.2 SYSTEM LAYOUT AND EQUIPMENT COMPLEMENT

This section illustrates the physical layout and defines the equipment complement of basic 3203 systems. The layout of the basic system cabinet is illustrated in Figure 1-2. As previously mentioned, there are two types of systems. The first system is hereby identified as type 01-277. This system incorporates mass storage units (disk/tape devices) which require controllers that are external to the device. The mass storage units for the second system (identified as type 01-339) are self-contained devices which have their own embedded controllers. Regardless of type, both systems are functionally identical. The only difference is in the equipment complement of each system, as defined in Table 1-1.

1.3 UNIT DESCRIPTIONS

The following sections (1.3.1 through 1.3.9) provide a brief functional description of each major unit of the type 01-277 and 01-339 Model 3203 Systems. Inactive units, such as the I/O connector panel and the various system cables are described elsewhere in this manual as defined in Table 1-1.

1.3.1 Control Panel

The system control panel is used to power the system on and off. The control panel contains an ON/OFF (1/0) switch and two red LED indicators (power and fault). The power indicator is lit when power to the system is on. The fault indicator is lit on power-up and remains lit until successful completion of the basic confidence and memory tests. The fault indicator is also lit when an invalid condition called a BOMB is detected by the CPU/memory board. Additional information on system BOMBs is provided in the 35-864 Central Processing Unit CPU/Memory Board Theory of Operation Manual.

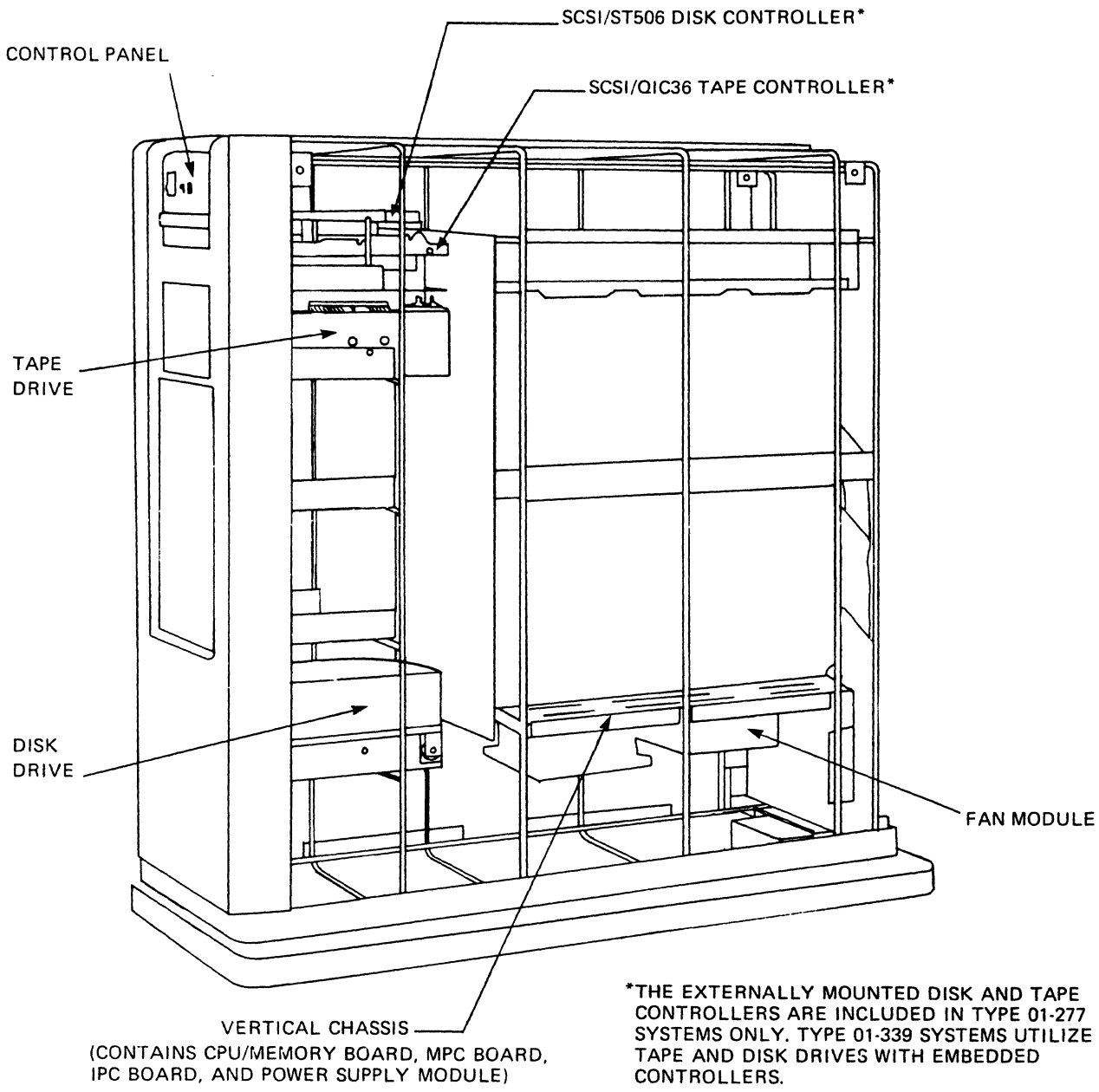

Figure 1-2 General Layout of Basic Cabinet

TABLE 1-1 EQUIPMENT COMPLEMENT FOR MODEL 3203 SYSTEMS

Item No. (For Ref. Only)	Unit Complement Per System Type — Part Numbers: 01-277 SYSTEMS (Which Contain Tape/Disk Units W/External Controllers)	Unit Complement Per System Type — Part Numbers: 01-339 SYSTEMS (Which Contain Tape/Disk Units W/Embedded Controllers)	Description	Definitions and Functions
1	09-169	Same as 01-277 System	System Control Panel	The control panel includes a power on/off switch and two LEDs to monitor power on and fault conditions. See Sections 1.3.1 and 4.2 for more information.
2	09-170	Same as 01-277 System	Fan Module	Ensures proper air circulation to maintain the enclosure at ambient room temperature as described in Section 2.8.
3	09-172	09-219	Basic 3203 System Enclosure	Both types of enclosure house the various system components and peripheral mass storage devices. The 09-172 enclosure accommodates two 51MB or 85MB disk drives and a 0.25" streaming tape drive for disk backup. The 09-219 enclosure accommodates two 182MB disks and a streaming tape drive.
4	17-726 M00	17-726 M01	QIC36 Interface Cable	Items 4 through 16 are all a part of the 3203 System cabling which is fully defined in Sections 3.4 and 3.5, as applicable.
5	17-727	N/A	ST506 Daisy Chain Cable	
6	17-728	N/A	ST506 Radial Data Cable	
7	17-732	Same as 01-277 System	Internal AC Cable	
8	17-733 or 17-756	Same as 01-277 System	AC Power Cable (115V, Domestic) or AC Power Cable (250V, International)	

9	17-734	Same as 01-277 System	12 Volt Power Cable	
10	17-737	17-927	50 Conductor IPC Cable	
11 12 13 14	17-738 F00 17-738 F01 17-738 F02 17-738 F03	Same as 01-277 System	Communication Multiplexer (Comm Mux) Cables (4)	
15	17-747	Same as 01-277 System	Ground Strap Cable	
16	17-758	Same as 01-277 System	12V Peripheral Power Cable	
17	27-159		1/4" Streaming Tape Drive (for Disk Backup)	The 27-159 tape drive uses an external controller. The 27-192 tape drive (in the 01-339 system) has an embedded controller. Refer to Sections 1.3.7 and 1.3.8 for more information.
18	27-160 or 27-161	27-189 F01	5.25" Disk Drive	The disk drives for the 01-277 system have an external controller and are described in Section 1.3.5.1. The 27-189 disk drive (in the 01-339 system) has an embedded controller as described in Section 1.3.5.2.
19	34-045	Same as 01-277 System	Power Supply Assembly (P575A / P1212A)	The system power supply assembly provides +5VDC and +12VDC system operating voltages. These voltages are generated on the 35-903 power board which is described in Sections 1.3.9 and 4.10.
20	35-864 M00 or 35-864 M01	35-864 M01	Central Processing Unit (CPU)/Memory Board	There are two manufacturing variations of the CPU/Memory board, multiwire and multilayer; both are functionally identical. The multi-wire version (M00) was provided in earlier 3203 systems. The M01 multilayer version is currently provided in all systems. See Sections 1.4.1 and 4.3 for more information.

TABLE 1-1 EQUIPMENT COMPLEMENT FOR MODEL 3203 SYSTEMS (Continued)

Item No. (For Ref. Only)	Unit Complement Per System Type — Part Numbers: 01-277 SYSTEMS (Which Contain Tape/Disk Units W/External Controllers)	Unit Complement Per System Type — Part Numbers: 01-339 SYSTEMS (Which Contain Tape/Disk Units W/Embedded Controllers)	Description	Definitions and Functions
21	35-905 or 35-999	N/A	SCSI/QIC 36 Tape Drive Controller	This unit serves as an adapter between the IPC/SCSI and the 27-159 tape drive unit QIC36 interface as defined in Sections 1.4.5 and 4.8.
22	35-906	N/A	SCSI/ST506 Disk Controller	This unit serves as an adapter between SCSI signals from the IPC to the ST506 signals recognized by the 27-160 and 27-161 disk drives. Refer to Sections 1.3.6 and 4.7 for more information.
23	35-907	Same as 01-277 System	I/O Panel Interconnection Board	This board provides the interconnection path between the internal and external I/O cable connectors. See Section 2.9.
24	35-915	N/A	Connector Transition Board	This board transposes the QIC36 interface 50 pin cable connection from the tape controller to the 50 50 pin orientation required by the tape drive.
25	35-910 F01	Same as 01-277 System	Multiperipheral Controller (MPC) with 3203 Initial Program Loader (IPL).	The MPC board provides interface for eight RS232C user devices or terminals. The MPC also includes a precision internal clock, a line frequency clock, a loader storage unit and a parallel line printer interface. A second MPC is optional. See Sections 1.3.3 and 4.4 for details.
26	35-918	Same as 01-277 System	Intelligent Peripheral Controller (IPC)	The IPC board provides data management for the peripherals. It interfaces the CPU via the PMUX bus and the peripherals via the SCSI bus. See Sections 1.3.4 and 4.5 for details.

1.3.2 Central Processor Unit (CPU)/Memory Board (35-864)

All processing and arithmetic logic unit (ALU) functions are contained on a single 38.1cm X 43.2cm (15" X 17") printed circuit (PC) board with built-in single and double precision floating point registers. The CPU/memory board monitors the majority of the system activity, provides user and memory interface and manages all system I/O. The CPU/memory board has on-board memory which provides 0.5MB or 1MB with 64kb random access memory (RAM) in 256kb single in-line packages (SIPs) or 2MB to 4MB using 256kb RAMS in 1MB SIPs. The memory system provides an error check and correction (ECC) function that detects and corrects all single bit errors, and detects all double and some multiple bit errors.

Currently, the basic system is provided with 2MB of memory and with 4MB as the option. Formerly, the basic system was available with 0.5MB of memory and options of 1,2,3 and 4MB. For continuity purposes, information concerning these smaller increments of memory expansion is retained in this manual even though they are no longer offered.

1.3.3 Multiperipheral Controller (MPC) Board (35-910)

The MPC is a single 38.1cm x 38.1cm (15" x 15") PC board which provides the means of interfacing user devices or terminals to the system over eight programmable, full-duplex data communication channels. These communication channels may be assigned to a combination of asynchronous and synchronous devices. The Model 3203 System can support a maximum of four synchronous channels, the remainder may be asynchronous. A second MPC can be configured into the system providing a total capability of 16 channels.

Permissable combinations of synchronous and asynchronous channels are defined in Table 1-2.

TABLE 1-2 MPC CHANNEL CONFIGURATION

ONE MPC		TWO MPCs	
ASYNC	SYNC	ASYNC	SYNC
8	0	16	0
7	1	15	1
6	2	14	2
5	3	13	3
4	4	12	4

The MPC also contains the precision interval clock/line frequency clock (PIC/LFC), a loader storage unit (LSU) and a parallel line printer interface.

1.3.4 Intelligent Peripheral Controller (IPC) Board (35-918)

The IPC board is designed to provide a major portion of data management required by peripherals while minimizing processor intervention in I/O operations. The IPC interfaces to the processor via the PMUX bus. When not transferring data, it releases the PMUX bus to other controllers. The IPC interfaces to the peripherals over the small computer systems interface (SCSI) bus at a transfer rate of 1.5MB per second. The IPC supports two 5.25" disks and a 0.25" streaming tape located in the system cabinet. When used in a type 01-339 system or in a type 01-277 system that has a 35-999 tape drive controller, the IPC must be at revision level R11 or higher.

1.3.5 5.25" Disk Drives

The following sections describe the various disk drive units used in each type of the Model 3203 System.

1.3.5.1 Disk Drives For Type 01-277 Systems

The type 01-277 Model 3203 System is configured with a 51.4MB or 85MB Winchester-type disk drive. Both units have a transfer rate of 625kB/second, an average access time of 30ms, an average rotational latency of 8.3ms and use modified frequency modulation (MFM). These disk drives interface to the disk drive controller via the ST506 interface.

The 51.4MB disk drive (27-160) is a random access storage device using three nonremovable 5.25" disks. Each disk surface employs one movable head to access up to 987 tracks, which provides up to 40.4MB (32 sectors X 256 bytes) of formatted capacity and a total unformatted capacity of 51.4MB.

The 85MB disk drive (27-161) uses four nonremovable 5.25" disks as storage media. Each disk surface employs one movable head to access up to 1166 tracks, which provides up to 66.9MB of formatted capacity and a total unformatted capacity of 85MB.

1.3.5.2 Disk Drive For Type 01-339 Systems

The type 01-339 Model 3203 System is configured with a 182MB Winchester-type disk drive (27-189). The 182MB disk drive is a random access storage device using five nonremovable 5.25" disks. Each disk surface employs one movable head to access up to 967 tracks per surface, which provides up to 142.5MB of formatted capacity and a total unformatted capacity of 182MB. This unit has a transfer rate of 1.25MB/second, an average seek time of 19ms, and an average rotational latency of 8.33ms.

Note that the 182MB disk drive has an embedded SCSI device controller and is available with or without internal terminating resistors as follows:

1. Type 27-189 F01 terminated disk provided for basic system.

2. 27-189 F02 unterminated second disk option.

The first (basic) disk is always the terminated functional variation F01. When provided, the second disc is always the unterminated F02 variation.

1.3.6 5.25" Disk Controller (35-906)

The 5.25" disk controller is a single board adapter providing two standard interfaces which enable the two Winchester-type disks to communicate with the IPC. The disk controller interfaces to the IPC over the SCSI bus and to the disk drives via the ST506 interface. The disk controller formats both disk drives at 512B per sector. The disk controller also features 11b error detection and correction capabilities, a 1kB on-board data buffer with parity, and internal diagnostics.

1.3.7 0.25" Streaming Tape Drive (27-159 and 27-192)

There are two types of tape drives available for use in Model 3203 Systems. Functionally, both drives are identical and have the same main characteristics. The main differences between the tape drives are as follows:

1. The type 27-159 tape drive is used in type 01-277 Model 3203 Systems and requires the tape controller (35-905 or 35-999) as described in Section 1.3.8.

2. The type 27-192 tape drive is configured in type 01-339 Model 3203 Systems. This tape drive unit is SCSI compatible and has its own embedded controller.

Both units are 0.25" streaming tape drives specifically designed for back-up of Winchester-type disks at a transfer rate of 86.7kB/s. The 0.25" streaming tape drive is capable of supporting 60MB of formatted data on a 600' tape contained in a 4" X 6" data recording cartridge. The tape drive functions in a streaming mode with a data density of 8kb per inch (bpi).

1.3.8 0.25" Tape Controller (35-905 and 35-999)

The 0.25" tape controller is a single board streaming tape controller providing two standard interfaces which enable the tape drive to communicate with the IPC. The controller interfaces to the IPC via the SCSI bus and to the tape drive via the QIC36 interface. The tape controller is responsible for data encoding/decoding, tape position control and tape formatting. The tape controller formats the streaming tape using a QIC24 media format which has a block size of 512B. The tape controller also provides 16b cyclic redundancy check (CRC) error detection coding, an 8k on-board data buffer, internal diagnostics and the capability of disconnecting from the SCSI bus during large tasks to allow multitasking operation. Two tape controllers (35-905 and 35-999) currently exist. While their strapping options and appearances are slightly different, they are functionally equivalent. To determine which tape controller has been installed in your system, refer to the part number stamp located near the edge of the controller board. For strapping and switch settings, see Figures 3-12 and 3-13. Note that when the 35-999 tape controller is used, the associated IPC must be at revision level R11 or higher. Furthermore, if the 35-999 controller is used in a system having the XELOS™ operating system, ensure that the revision level of XELOS is at R02 or higher.

1.3.9 Power Supply Board (35-903)

The 35-903 power supply is a nonexpandable power supply contained on a single PC board which connects directly into the system backpanel. The power supply provides two DC output voltages (P5 and P12) to power the CPU/memory board, MPC board, IPC board, peripherals and fans. For domestic use, an AC cable and plug are provided for connection to a 120VAC, 15A power outlet. For international use, an AC cable is provided for connection to a 230VAC, 6A power outlet. A plug at the outlet end has been excluded to permit the user to select one that complies with local codes.

1.4 INTERNAL ARCHITECTURE

Architectural block diagrams of both types of Model 3203 Systems are illustrated in Figure 1-3. Part a (Figure 1-3a) represents the type 01-277 system which has controllers that are external to the tape and disk drive units. The type 01-339 system (which has disk and tape units with embedded controllers) is represented in Figure 1-3b. Figure 1-3 is provided to support the following descriptions of the internal and external buses and the system structure.

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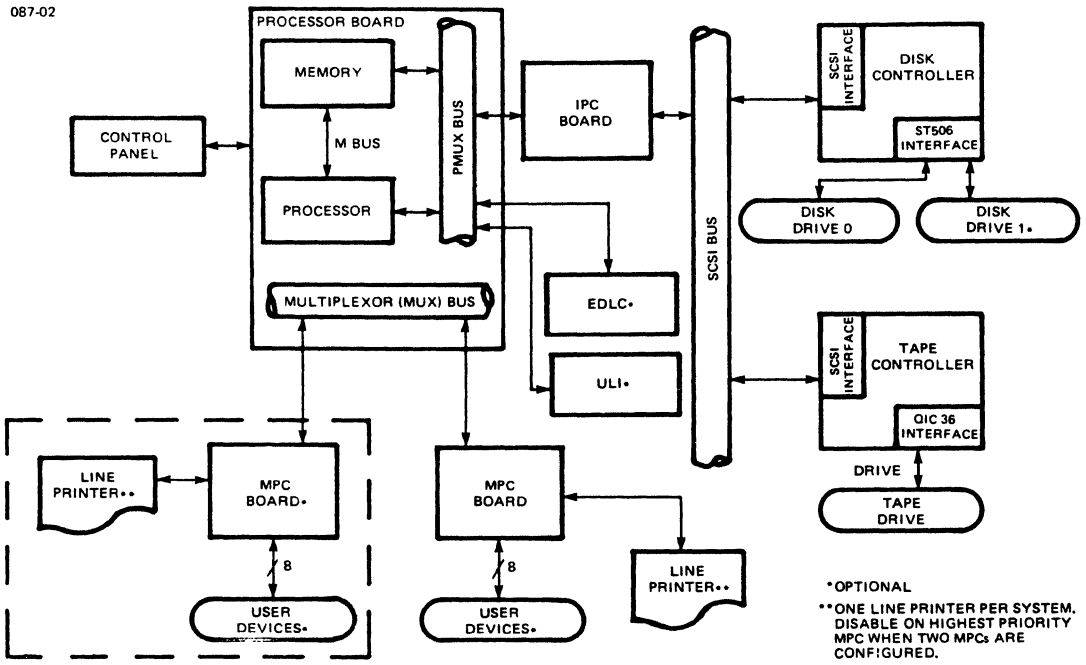
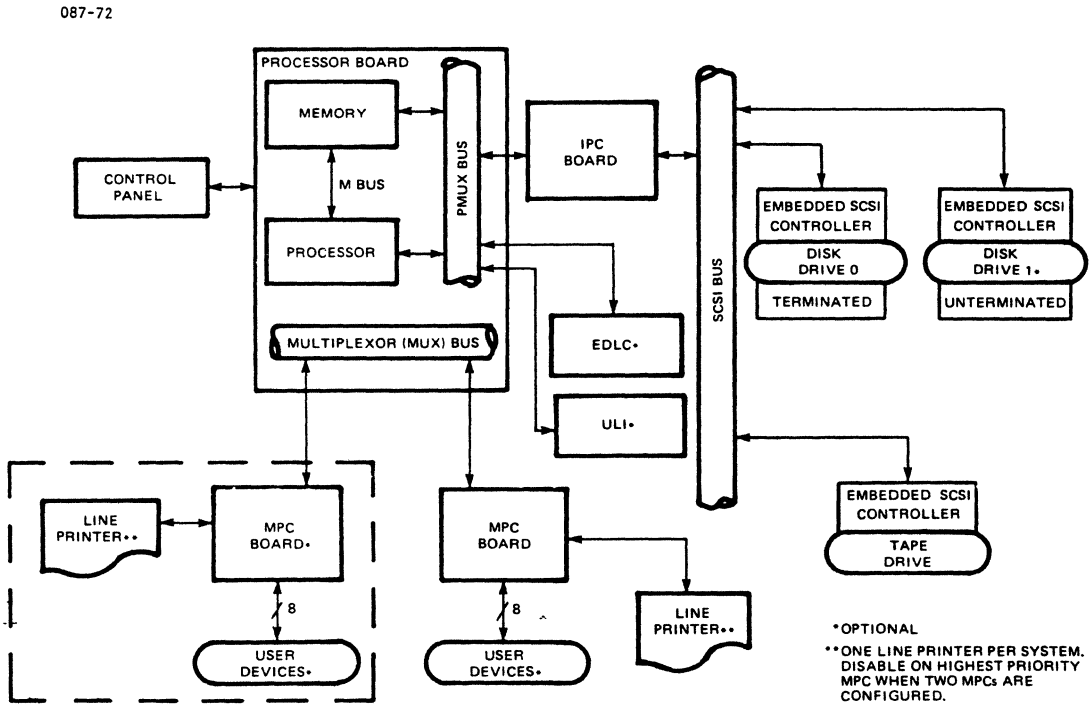


a. Type 01-277 System With Controllers External to Tape/Disk Drives



b. Type 01-339 System With Embedded Tape/Disk Controllers

Figure 1-3 Model 3203 System Block Diagram

1.4.1 Central Processing Unit (CPU)/Memory and Input/Output (I/O) Buses

The following sections provide a general description of the I/O buses, the CPU/memory buses and their functions in the system. As applicable, refer to the 35-864 Central Processing Unit CPU/Memory Board Theory of Operation Manual for more detailed bus descriptions.

1.4.1.1 Multiplexor (MUX) I/O Bus

The MUX bus is the primary data/control channel between the CPU/memory board and system devices. The CPU/memory board initiates, monitors and responds to all system devices via MUX operation sequences. The MUX bus is a byte-oriented or halfword-oriented I/O system that can address a maximum of 1,024 peripheral devices.

The MUX bus consists of 27 signal lines, shown in Table 1-3, on connector 0 (CONN0) of every backpanel slot.

TABLE 1-3 MUX BUS SIGNAL LINES

TYPE	MNEMONIC	DIRECTION PROCESSOR <-> DEVICE	NUMBER
Data lines	D000:150	<---------->	16 lines
Control lines	ADRS0	---------->	1 line
	SR0	---------->	1 line
	DR0	---------->	1 line
	DA0	---------->	1 line
	CMD0	---------->	1 line
	RACK0/		
	TACK0	-----(daisy-chain)-->	1 line
	CLO70	---------->	1 line
Test lines	SYN0	<----------	1 line
	ATN0	<----------	1 line
	HW0	<----------	1 line
Initialize line	SCLR0	---------->	1 line

1.4.1.2 Private Multiplexor (PMUX) Input/Output (I/O) Bus

The PMUX bus interfaces high-speed secondary storage devices such as disks and magnetic tapes to the integrated selector channel (ISELCH). In Model 3203 Systems, the ISELCH is operated in the high-speed handshake protocol mode for higher throughput rates than are achievable with the standard handshake protocol. Refer to the 35-864 Central Processing Unit CPU/Memory Board Theory of Operation Manual for more information concerning the ISELCH.

Once the PMUX bus has been activated and interfaced to the ISELCH for a direct memory access (DMA) transfer, it functions in a completely autonomous fashion with one controller or device at any one time. When the PMUX bus is not interfaced to the ISELCH, it is placed in the idle mode and functions as an extension of the MUX bus. The PMUX is disconnected from the MUX bus during an ISELCH initialize operation.

The PMUX bus consists of 30 signal lines, shown in Table 1-4, on CONN1 of every backpanel slot.

TABLE 1-4 PMUX BUS SIGNAL LINES

TYPE	MNEMONIC	DIRECTION PROCESSOR <-> DEVICE	NUMBER
Data lines	PD000:150	<---------->	16 lines
Control lines	PADRS0	---------->	1 line
	PSR0	---------->	1 line
	PDR0	---------->	1 line
	PDA0	---------->	1 line
	PCMD0	---------->	1 line
	PRACK0/		
	PTACK0	-----(daisy-chain)-->	1 line
	PCLO70	---------->	1 line
	SBUSY0	---------->	1 line
Test lines	PSYN0	<----------	1 line
	PATN0	<----------	1 line
	PHW0	<----------	1 line
	SENS0	<----------	1 line
	SCHK0	<----------	1 line
Initialize line	SCLR0	---------->	1 line

1.4.1.3 Processor Internal Buses

The X, Y and S buses interconnect major units on the CPU/memory board.

- The X bus is the destination bus containing the results of the operation.
- The Y bus is the first operand bus.
- The S bus (sequencer bus) is used for inputting address data for branching, user instruction decode and loading the repeat counter (RPCT) in the microaddress sequencer.

1.4.1.4 Processor/Memory Buses

There are two processor/memory buses as follows:

- The C bus is a 24b unidirectional bus which passes addresses to the virtual address register.
- The M bus is a 16b bidirectional bus which passes data between the processor and memory.

1.4.1.5 Internal Memory Buses

There are three internal buses as defined in the following:

- The E bus is a 16b bidirectional bus which passes data to or from the memory data register, ECC and the memory RAMs.
- The MA bus is a 9b unidirectional bus which passes addresses from the real address bus to local memory RAMs.
- The memory MUX bus which passes addresses from the real address bus to the expansion memory RAMs.

1.4.2 Multiperipheral Controller (MPC) Buses

The following sections provide a general description of the MPC buses and their interfaces to the CPU/memory and to users.

1.4.2.1 Multiplexor (MUX) Bus Interface

The MUX bus interface enables the MPC to interact with the processor in the form of request/response signals. The MPC MUX bus interface consists of 26 signal lines, 16 bidirectional data lines, six control lines, three test lines and an initialize line. These signal lines are the same as those listed in Table 1-3. Details on the MUX bus interface are provided in the Multiperipheral Controller (Multi-layer MPC) Installation, Theory of Operation and Programming Manual.

1.4.2.2 8-Channel Data Communications Multiplexor (COMM MUX)

The 8-channel data COMM MUX is contained in four serial communications controllers on the MPC board. Each controller contains two full-duplex (FDX) RS-232C channels that provide an 8-channel COMM MUX to the data sets or terminals via front-edge connectors 2 through 5 (CONN2:5). Any one of the eight channels can be asynchronous, synchronous data logic control (SDLC), bisynchronous (BISYNC) or monosynchronous. Any mixture of protocols are allowed to exist in the 8-channel COMM MUX. The Model 3203 will support asynchronous and synchronous combinations as described in Section 1.3.3.

1.4.2.3 Parallel Line Printer Interface

The parallel line printer interface provides the necessary logic for interfacing the MUX bus to a line printer. The MPC communicates with the line printer over eight parallel data lines, one strobe line, one acknowledgement line, one busy-line and three status lines (paper empty, fault and selected). The line printer interface accepts the standard 7b ASCII code and has the capability of converting lower- and upper-case characters to all upper-case if required.

1.4.3 Intelligent Peripheral Controller (IPC) Buses

The following sections provide a general description of the buses the IPC uses to interface to the CPU/memory board and to data storage devices.

1.4.3.1 Small Computer System Interface (SCSI) Bus

The SCSI bus is an asychronous bus which interfaces the IPC to several peripheral devices. On the Model 3203 System, two Winchester-type disks and one 0.25" streaming tape are interfaced to the IPC board via the SCSI bus. The SCSI bus is comprised of 18 signal lines, nine control lines, eight data lines and one parity line. These signals are transmitted over an open collector, 50-conductor cable. Data transfers and handshaking occur at a rate of 1.2MB per second. The signals that define the SCSI bus are shown in Figure 1-4.

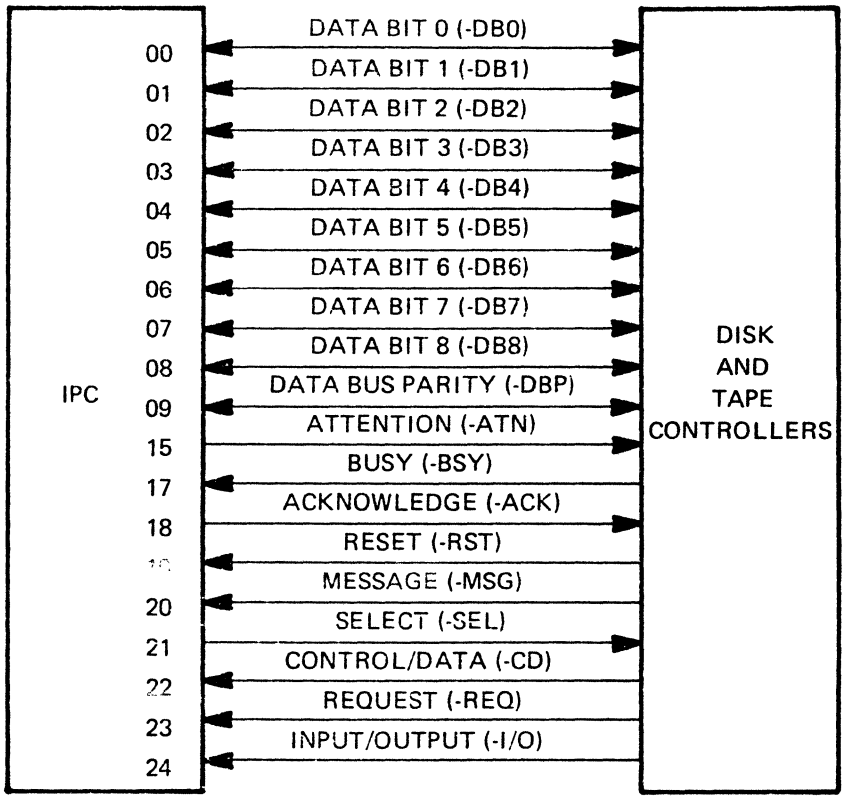


Figure 1-4 SCSI Signal Interface

1.4.3.2 Private Multiplexor (PMUX) Bus Interface

The PMUX bus interface provides the IPC with the means to interact with the processor via request/response signals. See Table 1-5 for a list of the IPC PMUX bus signal lines.

TABLE 1-5 IPC PMUX BUS INTERFACE SIGNAL LINES

TYPE	MNEMONIC	DIRECTION ---> PROCESSOR IPC <---	NUMBER
Data lines	D15-:00-	<---------->	16 lines
Control lines	ADRS-	---------->	1 line
	CMD-	---------->	1 line
	DA-	---------->	1 line
	DR-	---------->	1 line
	RACK-/TACK-	-(daisy-chain)->	1 line
	SBSY-	---------->	1 line
	SR-	---------->	1 line
Test lines	ATN-	<----------	1 line
	HW-	<----------	1 line
	SCHK-	<----------	1 line
	SNS-	<----------	1 line
	SYN-	<----------	1 line
	BUSSW-	<----------	1 line
Initialize line	SCLR-	---------->	1 line

1.4.4 Intelligent Peripheral Controller (IPC)/Disk and Tape Interfaces

The external tape and disk controllers interface the 27-159 tape drive and the 27-160 or 27-161 disk drive units to the IPC via the SCSI bus. Since the 27-192 tape and 27-189 disk drives utilize embedded SCSI controllers, they interface directly to the IPC over the SCSI bus. The SCSI bus consists of nine control signals, eight data signals and one parity signal line. These signal lines are defined in Section 1.4.3.1.

1.4.5 Tape Controller/Tape Drive Interface (35-905 and 35-999)

The QIC36 interface of the 0.25" tape drive uses 22 signal lines to interface the streaming tape drive to the controller; 15 signal lines originate at the controller. The remaining seven signal lines originate at the streaming tape drive. These signal lines, shown in Table 1-6, are defined in the SCSI Tape Controller Manual.

TABLE 1-6 QIC36 INTERFACE SIGNAL LINES *

NAME	MNEMONIC	DIRECTION ---> CONTROLLER/DRIVE <---	NUMBER
Select	DS0-	---------->	1 line
Reset	RST-	---------->	1 line
Go	GO-	---------->	1 line
Reverse	REV-	---------->	1 line
Threshold	THD-	---------->	1 line
Track 0-3	TR0-:TR3-	---------->	4 lines
Write Data+	WDA+	---------->	1 line
Write Data-	WDA-	---------->	1 line
High Current	HC--	---------->	1 line
Erase Enable	EEN-	---------->	1 line
Write Enable	WEN-	---------->	1 line
High Speed	HSD-	---------->	1 line
Read Data Pulses	RDP-	<----------	1 line
Upper Tape Hole	UTH-	<----------	1 line
Lower Tape Hole	LTH-	<----------	1 line
Drive Selected	SLD-	<----------	1 line
Cartridge In	CIN-	<----------	1 line
Unsafe	USF-	<----------	1 line
Tachometer Pulses	TCH-	<----------	1 line

* Table 1-6 is only applicable to the 27-159 tape drive.

1.4.6 Disk Controller/Disk Drive Interface (35-906)

The ST506 interface for the 27-160 and 27-161 disk drive units uses 13 control signal lines and five data signal lines to interface the disk drive to the controller. The signal names, direction and mnemonics are provided in Table 1-7. For details of these signal lines see the SCSI Disk Controller Manual.

TABLE 1-7 ST506 INTERFACE SIGNAL LINES *

NAME	MNEMONIC	DIRECTION ---> CONTROLLER/DRIVE <---	NUMBER
CONTROL LINES			
Drive 1 Select	SEL1-	---------->	1 line
Drive 2 Select	SEL2-	---------->	1 line
Head Select 0-2	HD0-:HD2-	---------->	3 lines
Write Gate	WG-	---------->	1 line
Seek Complete	SKCPT-	<----------	1 line
Track 0	TR0-	<----------	1 line
Write Fault	WFLT-	<----------	1 line
Index	INDEX-	<----------	1 line
Ready	RDY-	<----------	1 line
Step Pulse	STEP-	---------->	1 line
Direction	DIR-	---------->	1 line
DATA SIGNALS			
Drive Selected	SLCTD-	<----------	1 line
MFM Read Data+	RD+	<----------	1 line
MFM Read Data-	RD-	<----------	1 line
MFM Write Data+	WD+	---------->	1 line
MFM Write Data-	WD-	---------->	1 line

* Table 1-7 is only applicable for the 27-160 and 27-161 disk drives.

CHAPTER 2
MECHANICAL CONFIGURATION

2.1 INTRODUCTION

This chapter contains a description of the AC and DC power requirements. Also described are the mechanical components of the cabinet, electrostatic discharge (ESD) care and prevention, grounding, cooling requirements and the input/output (I/O) connector panel.

2.2 AC POWER REQUIREMENTS

Table 2-1 provides the AC power requirements for the Model 3203 System.

TABLE 2-1 AC POWER REQUIREMENTS

	DOMESTIC (120V)	INTERNATIONAL (230V)
AC Voltage	90-132VRMS	180-264VRMS
Frequency	47-63Hz	47-63Hz
Phase	Single 3-Wire	Single 3-Wire
Input AC Current	12A	6A
Circuit Breaker Rating	15A	15A
Power Cord Length	3.05m (10')	3.05m (10')
Power Cord Plug NEMA Type/ Rating	Hubbell # 5266* 5-15 125VAC 15A	** 6-15 250VAC 15A

* Or equivalent
** Connector which complies with local codes to be furnished by user.

2.3 DC POWER REQUIREMENTS

The following sections describe the P5 and P12 power requirements. The 35-903 power supply provides the following DC outputs to power the processor, memory and peripherals.

- o P5 = 80A @ +5V
- o P12 = 14.5A (startup) @ +12V
- o P12 = 10.5A (nominal) @ +12V

2.3.1 P5 Requirements

Table 2-2 provides the P5 power requirements for the type 01-277 and 01-339 Model 3203 Systems.

TABLE 2-2 P5 POWER REQUIREMENTS

LOAD	P5 AMPERES TYPE OF SYSTEM	
	01-277	01-339
Processor/Memory Board	25	25
Multiperipheral Controller (MPC) Board	11	11
Intelligent Peripheral Controller (IPC) Board	14	14
Spare I/O Slot	10*	12.5*
Spare I/O Slot	9*	12.5*
0.25" Tape Drive with Controller	4	2.2
5.25" Disk Drive with Controller	5	1.4
Second 5.25" Disk Drive	2	1.4

* Any combination for these two slots providing total current is less than or equal to 19A for the pair in 01-277 systems, or is less than 25A in 01-339 systems.

2.3.2 P12 Requirements

Table 2-3 provides the P12 power requirements for the type 01-277 Model 3203 System. The P12 power requirements for the type 01-339 system are given in Table 2-4.

TABLE 2-3 P12 POWER REQUIREMENTS FOR TYPE 01-277 SYSTEMS

LOAD	P12 (AMPS)	
	NOMINAL	START-UP
0.25" Tape Drive with External Controller	2.5	1.0 (300ms)*
5.25" Disk Drive with External Controller	3.5	5.0 (10-30s)
Second 5.25" Disk Drive	3.5	5.0 (10-30s)
Fan Assembly	1.0	3.5

* Less than 1.0A while disks are at 5.0A peak (the tape drive starts up after the disks have dropped to 3.5A)

TABLE 2-4 P12 POWER REQUIREMENTS FOR TYPE 01-339 SYSTEMS

LOAD	P12 (AMPS)	
	NOMINAL	START-UP
0.25" Tape Drive with Embedded Controller	2.6	1.0 (300ms)*
5.25" Disk Drive with Embedded Controller	2.4	4.5
Second 5.25" Disk Drive with Embedded Controller	2.4	4.5
Fan Assembly	1.0	3.5

* Less than 1.0A while disks are at 4.5A peak (the tape drive starts up after the disks have dropped to 2.4A)

2.4 GROUNDING

AC ground is connected to chassis ground on the cabinet by connecting a 17-747 ground strap between the line filter and the chassis as shown in Figure 2-1.

AC ground is connected between the power supply and chassis ground through the cover plate mounting hardware at the upper and lower guide trays. AC grounding for the transformer frame and shield is maintained through the hardware which mounts the power supply printed circuit (PC) board to the chassis.

DC ground is isolated from AC ground throughout the system except at a single point where the backpanel is mounted to the chassis. This unipoint ground location is shown in Figure 2-1 and Information Drawings 01-277 D12 and 01-339 D12.

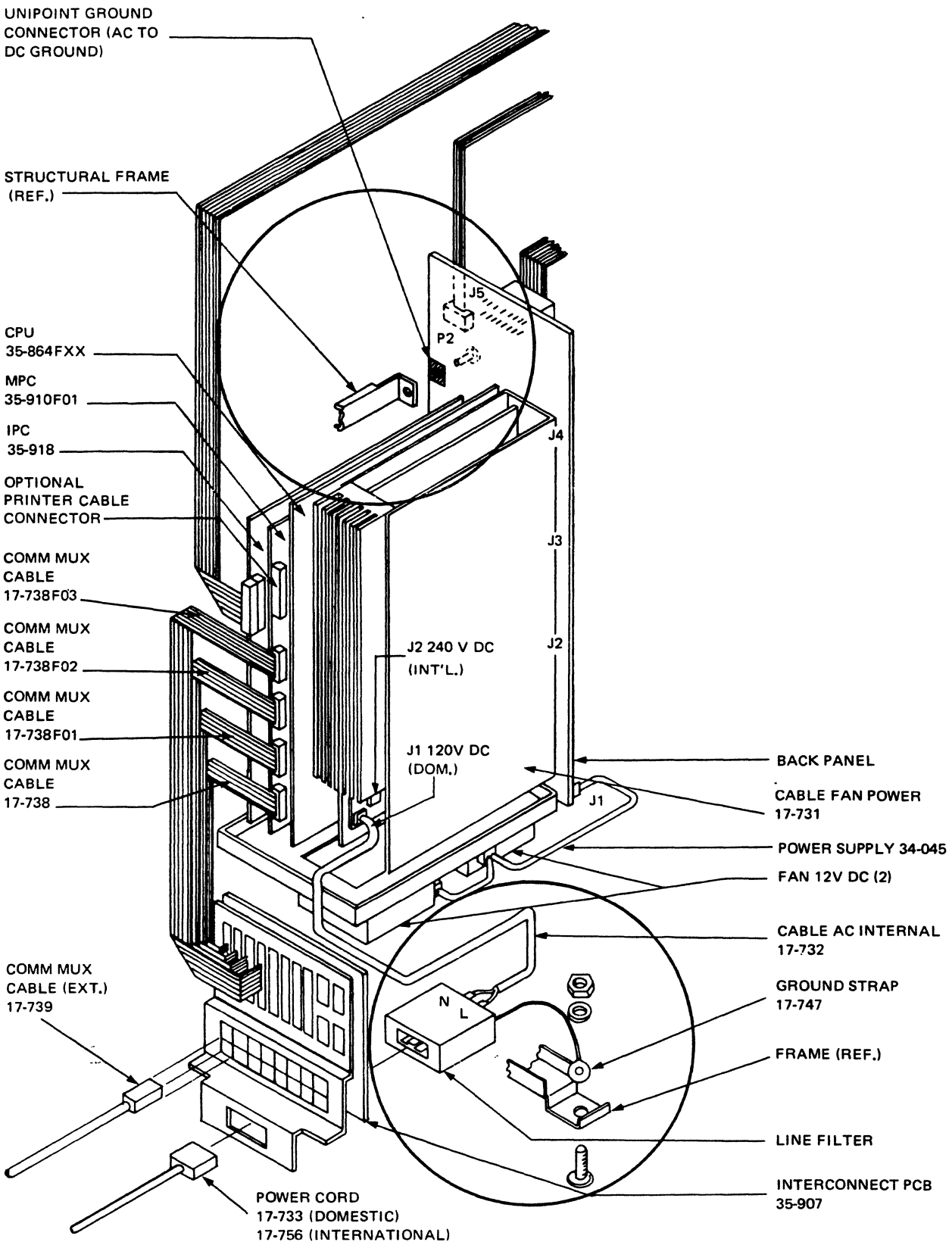


Figure 2-1 System Grounding

2.5 ELECTROSTATIC DISCHARGE (ESD) PROCEDURES

The discharge of electrical charges can damage many of the components in electronic equipment. To prevent any damage from ESD, the following static control procedures are recommended using field service kit 45-111 F24. This kit consists of a 24" X 24" conductive work surface, a 10' grounded cable with a 1-megohm resistor, a 6' extended coil cord with a 1-megohm resistor and two sizes of elastic wrist straps. The ESD field service kit is shown in Figure 2-2.

087-6

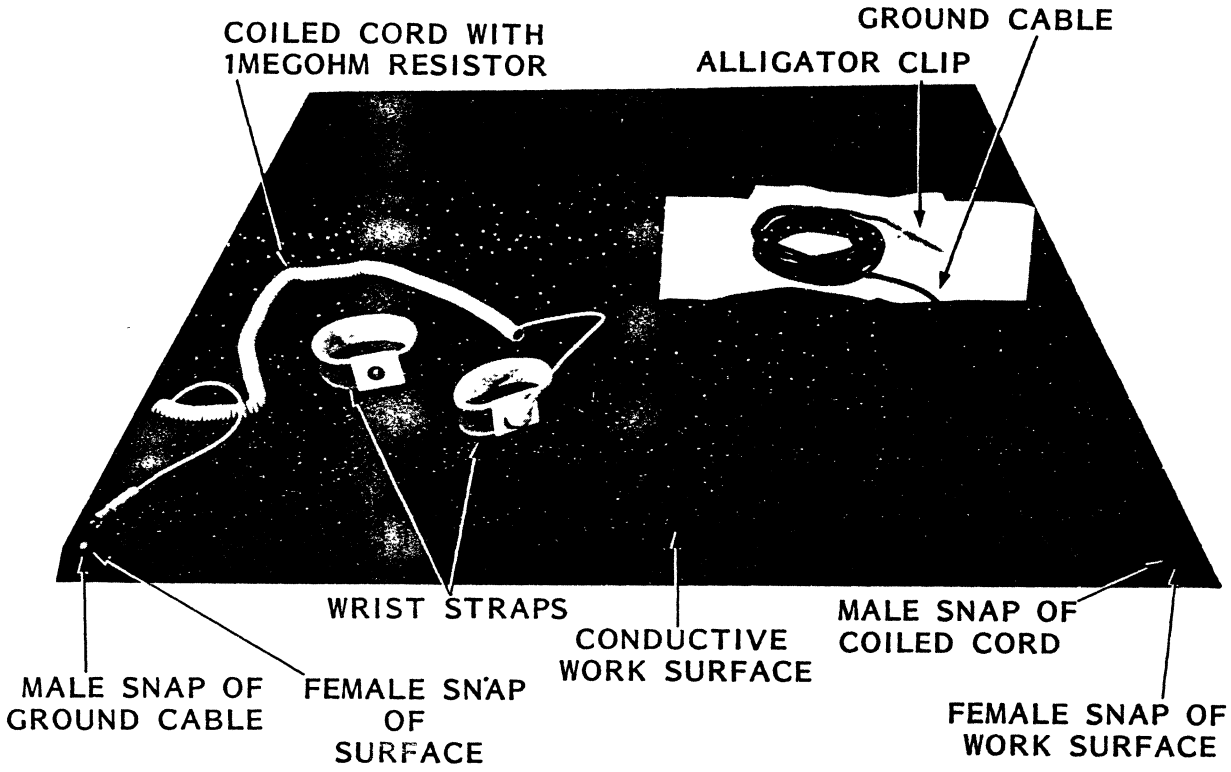


Figure 2-2 ESD Field Service Kit

1. Before performing any work on the Model 3203 System, open the field service kit and lay out the conductive work surface in a location where it is convenient to work.

2. Attach the male snap of the ground cable to one of the female snaps on the conductive work surface. Attach the alligator clip of the ground cord to a grounded surface, preferably the unipoint ground connection on the system backpanel.

3. Fasten the coiled cord to the work surface. Slip on the elastic wrist band that fits snugly on your wrist and fasten the band to the coiled cord via the snap. Make certain that the wrist strap is on exposed skin since contact between the interwoven metallic strands on the inside of the band and your wrist is crucial to dissipation of static electricity.

4. You are now safely grounded and can begin work. Note that any boards to be installed should be stored in approved antistatic or conductive bags. Open these bags at the immediate site of the field service kit only. Placing the bag on the work surface or holding it, when properly grounded through the wrist strap, eliminates any external charges. You should also wrap the replaced board in a conductive bag. If a suitable bag is not available, wrap the board in the conductive surface provided with the kit. This will suffice until a suitable bag is obtained.

5. Please keep in mind that the board is only static safe if the following conditions are adhered to:

   - the board is in an approved antistatic or conductive bag,
   - the board is properly installed in the unit,
   - the board is on the grounded work surface, and
   - the board is being held by properly grounded personnel.

2.6 ENVIRONMENTAL GUIDELINES

This section provides the recommended temperature and humidity ranges required around the equipment for trouble-free operation. Clearance for equipment access is not critical if the Model 3203 cabinet can be moved from its location for maintenance and equipment repair.

- Temperature:
  - 15°C to 30°C (59°F to 86°F)

- Temperature rate of change: - 2.5° C per hour (5° F per hour)
- Relative humidity:
  - 20% to 80% noncondensing
- Humidity rate of change:
  - 5% per hour
- Heat dissipation:
  - 2458 BTU/hr (2592 kilo-Joules per hour)
- Equipment area clearance:

  Sufficient clearance area is required behind the cabinet to allow for the cables connected into the rear of the cabinet.

2.7 MECHANICAL COMPONENTS

This section describes the basic system cabinet for the Model 3203 System. Figure 2-3 shows the frame substructure with placement of support rails and chassis guide trays. Figures 2-4 and 2-5 show the basic system cabinet structure consisting of frame substructure, base, front cover, rear cover and side panels. Figures 2-6 and 2-7 show front and rear views of the basic cabinet.

The front and rear covers are secured to the bracket cover mounts with one #8-32 Phillips head screw, preinstalled on each side of the cabinet. To install the front and rear covers, hook the lower tabs of the panels into the base and pivot the cover forward until the tabs slide onto the mounting screws. Tighten the mounting screws. The front and rear covers should be installed prior to the installation of side panels to provide access to the mounting screws. Figure 2-4 shows the installation of front and rear covers.

The side panels are secured to the base with two #8-32 screws for each side, which may be installed in the side panel prior to mounting. To install the side panels, hook the two screws onto the base and pivot forward to seat the upper tabs into the slots provided in the frame and tighten the screws as shown in Figure 2-5.

NOTE

Ensure that the grounding clips contact front, side and back panels when side panels are mounted.

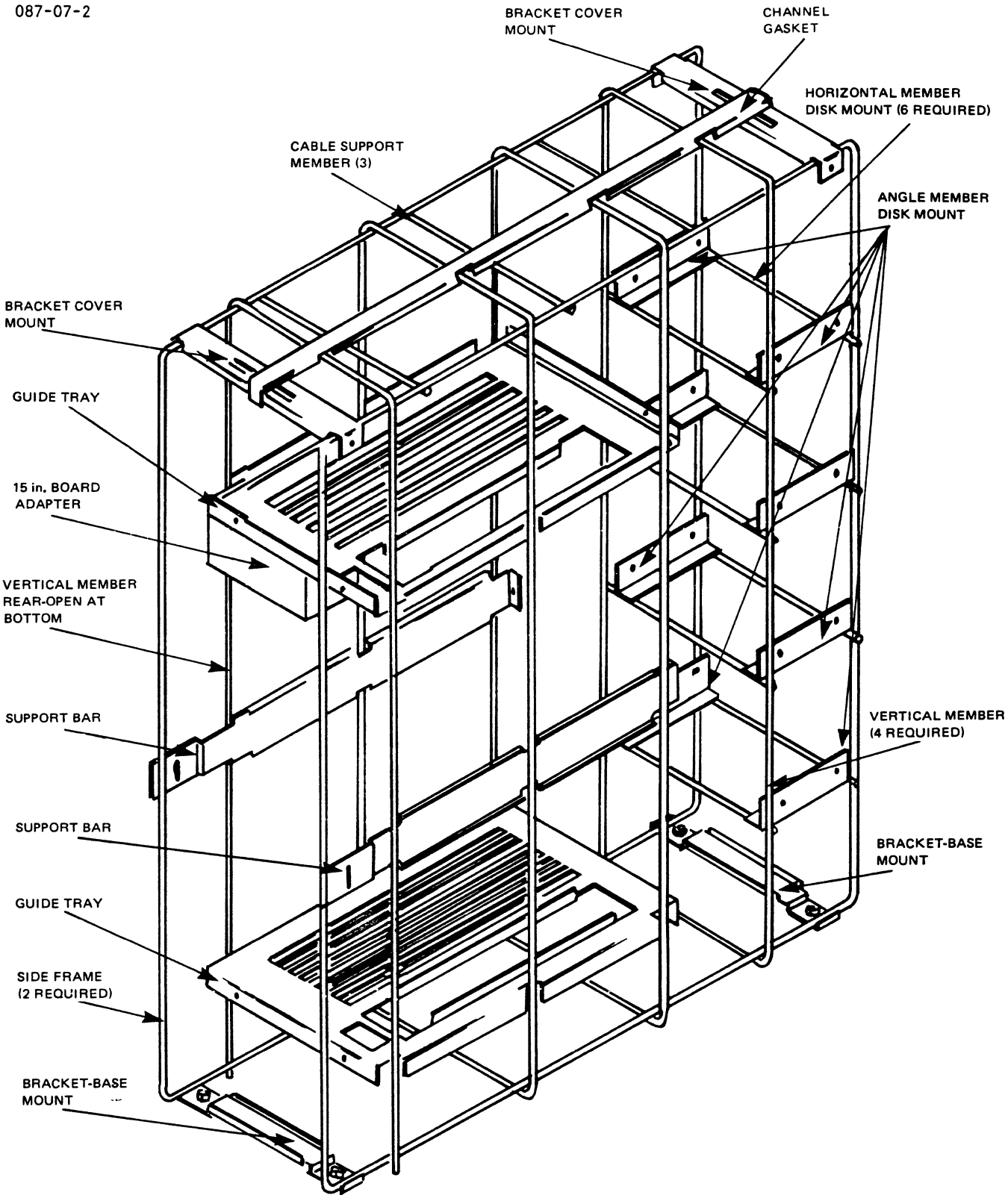


Figure 2-3 Model 3203 Frame Substructure

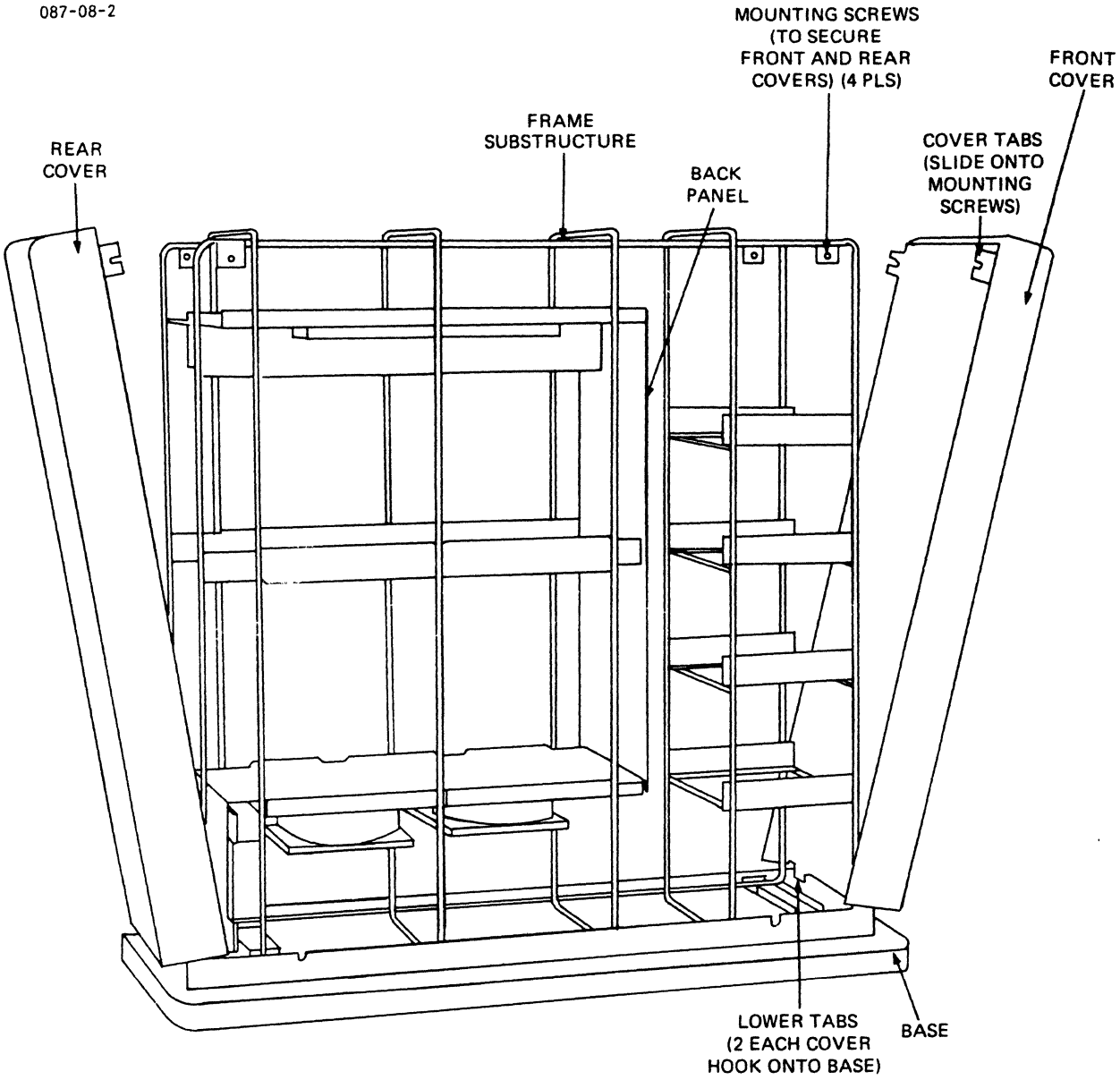


Figure 2-4 Front and Rear Cover Installation

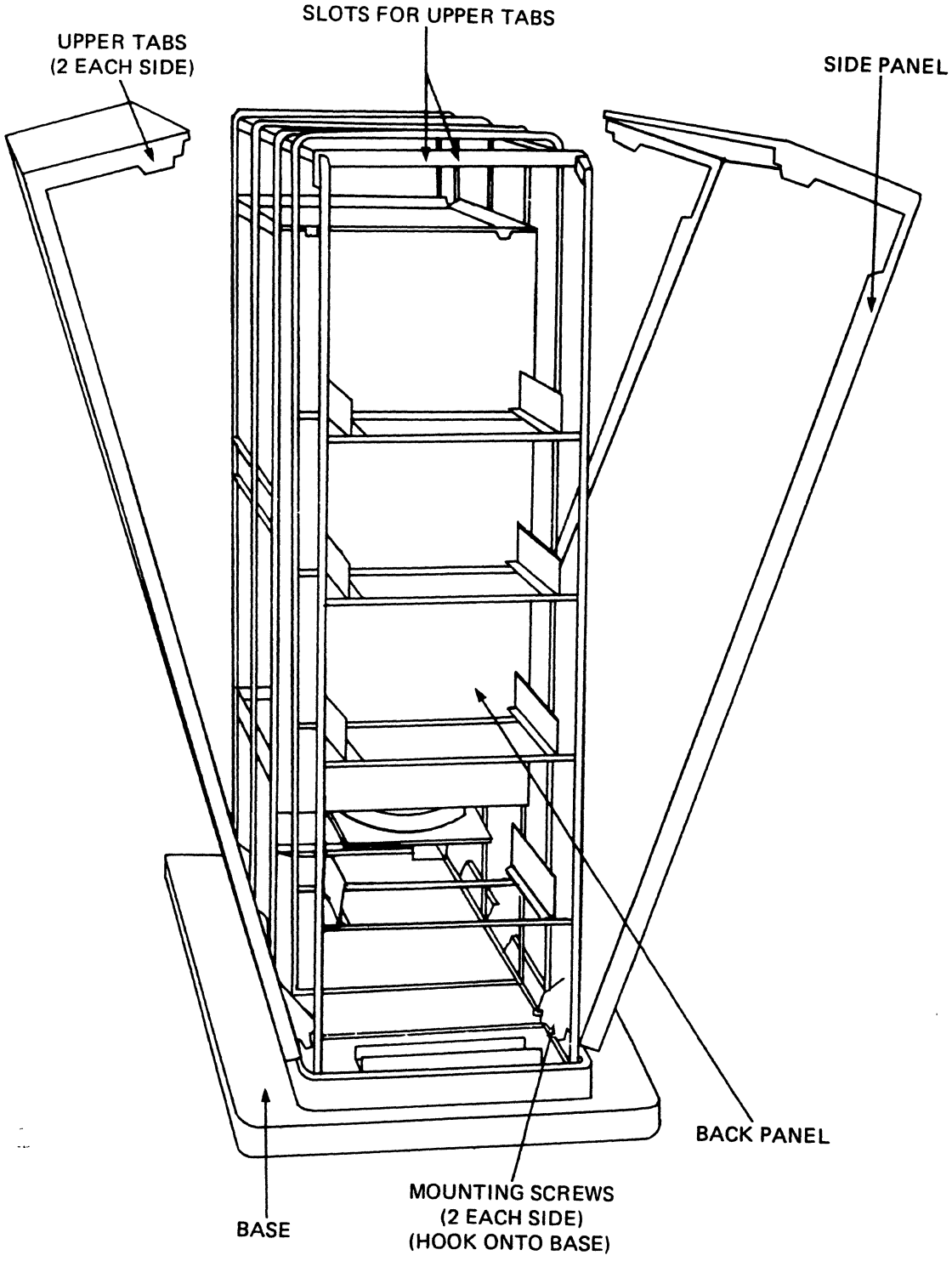


Figure 2-5 Side Panel Installation

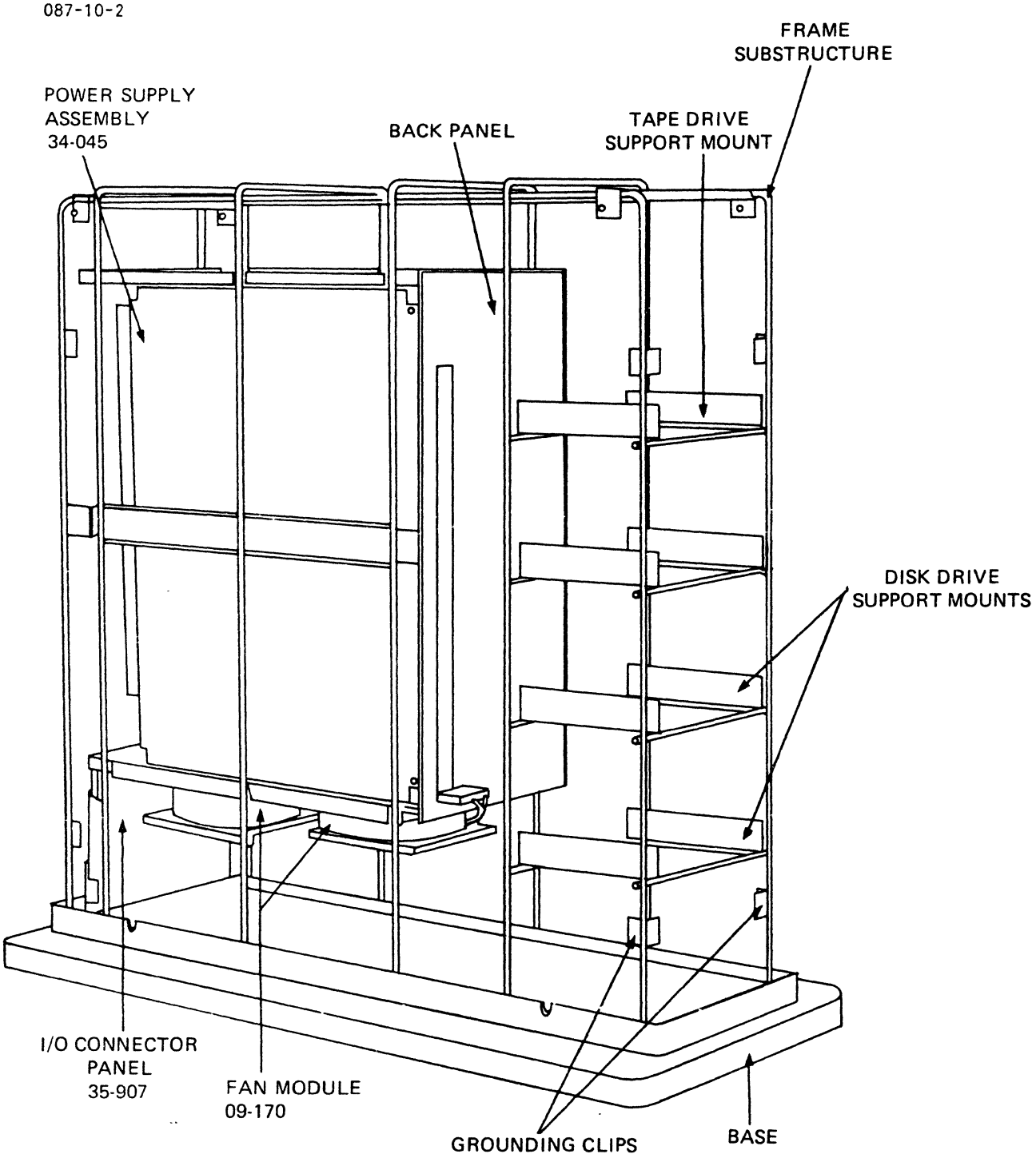


Figure 2-6 Basic System Cabinet (Front View)

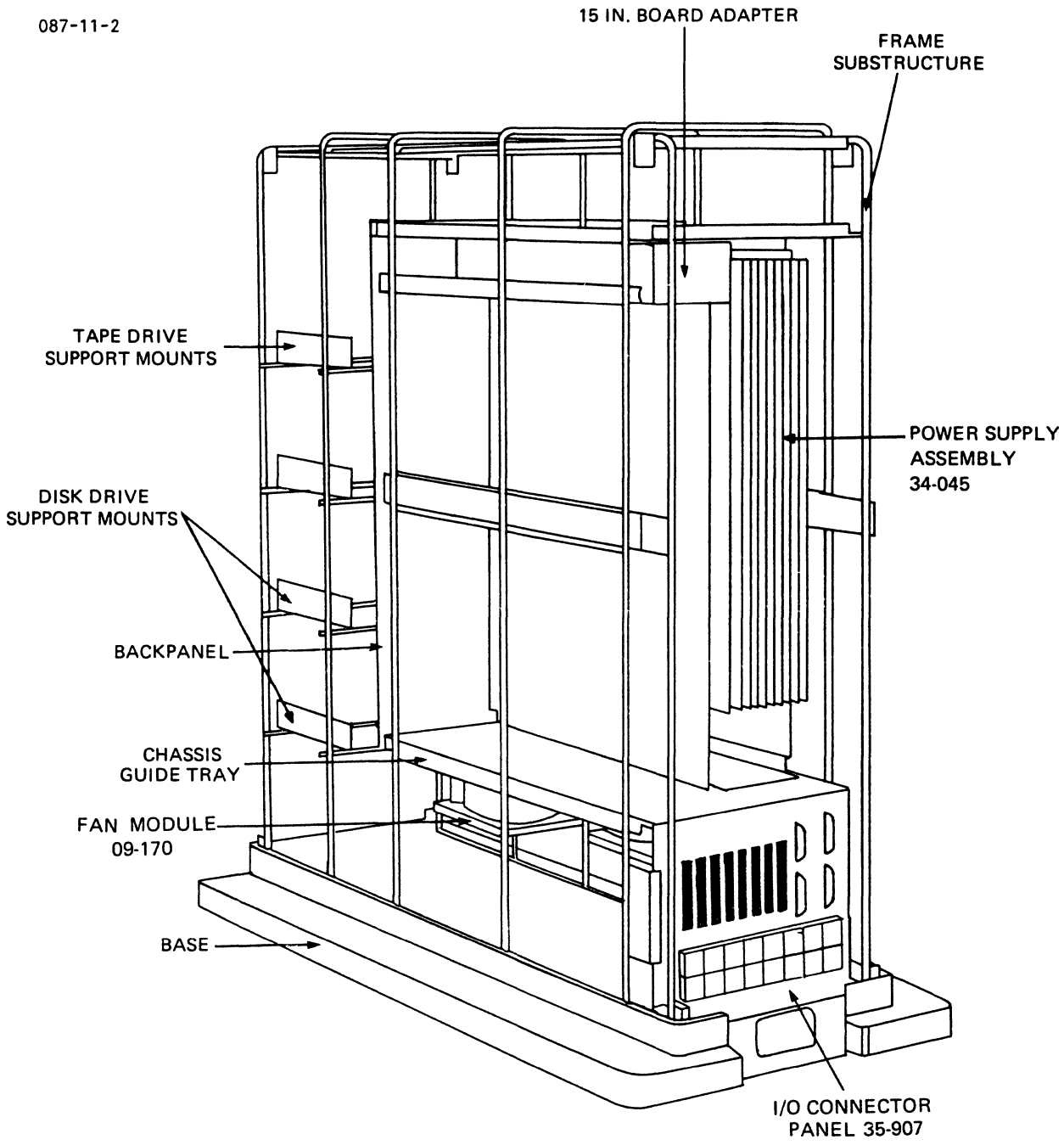


Figure 2-7 Basic System Cabinet (Rear View)

2.8 COOLING

The cabinet is designed to allow cooling and ventilation, using room ambient air for heat generating components.

The 09-170 modular fan assembly consists of two 11.7cm x 11.7cm (4.6" x 4.6"), 94 CFM, 12VDC fans. The fan assembly is mounted to the guide tray, with four #4-40 hex-head self-tapping screws, directly below the chassis. Air is pulled into the cabinet through the perforations at the bottom of the side panels, forced upward through the cabinet and exits at the perforations at the top of the side panels. The base of the cabinet extends 1.5" on either side providing sufficient clearance area for air circulation.

NOTE

The fans should be checked periodically for proper operation as they are not monitored electronically.

2.9 INPUT/OUTPUT (I/O) CONNECTOR PANEL

An I/O connector panel is mounted at the rear of the cabinet to provide a convenient interface between internal and external cables. A 35-907 interconnect PC board, connects (in copper) internal connectors J1 through J8 with external asynchronous jacks J1A/B through J8A/B. Internal connectors J7 and J8 are also connected to the four 15-pin external connectors J7C/D and J8C/D (asynchronous or synchronous). For details on the 35-907 interconnect board, see Functional Schematic 35-907 D08.

The base of the cabinet and the rear cover provide cutouts for external cables to exit the cabinet. The I/O connector panel is shown in Figure 2-8.

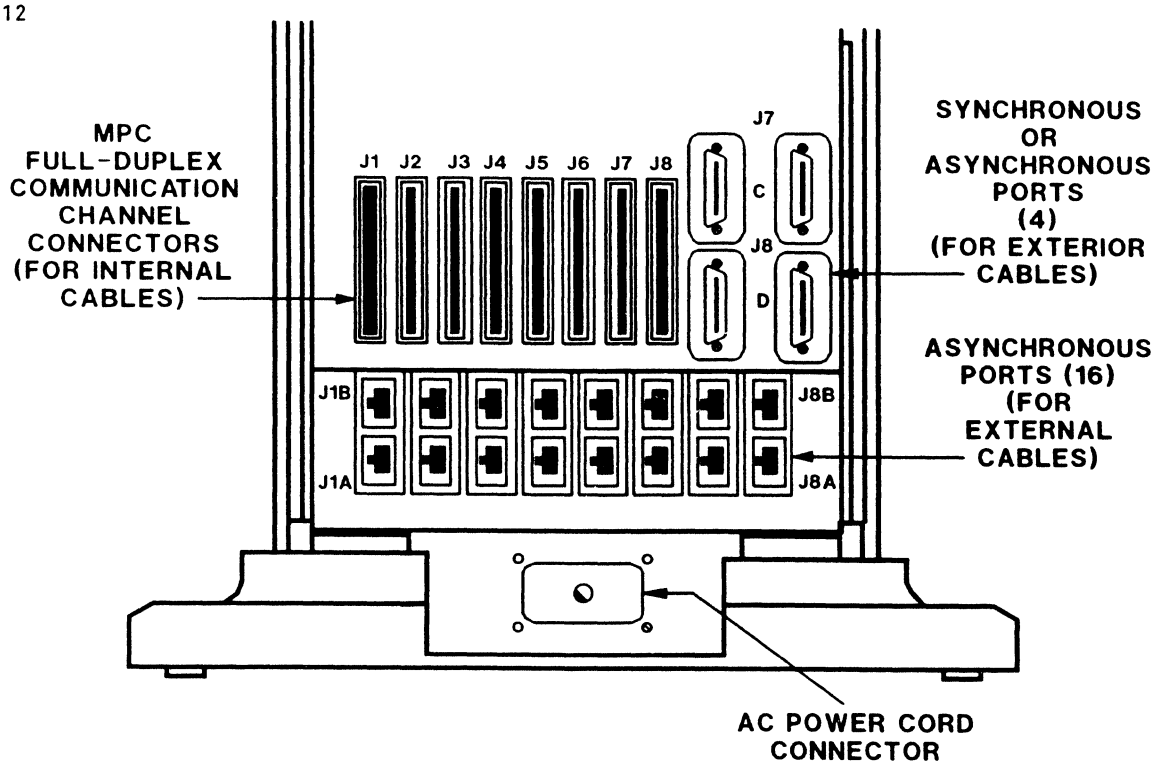


Figure 2-8 I/O Connector Panel (35-907)

CHAPTER 3
INSTALLATION AND SYSTEM CONFIGURATION

3.1 INTRODUCTION

This chapter provides system installation information including: recommended cabinet location, cabling, strapping, and initial setup/startup procedures. Basic information for the various system options is also provided and the interrupt priority arrangement is described.

Note that this chapter covers installation of type 01-277 and 01-339 Model 3203 Systems, which are defined in Section 1.2 and Table 1-1. Some of the information in this chapter is common to both types of systems. However, the cabling and strapping information has some significant differences. Therefore, to avoid confusion, cabling and strapping is covered in separate sections for each type of system.

See Section 3.4 for information on cabling for an 01-277 system and Section 3.5 for an 01-339 system. Strapping is detailed in Section 3.6 for an 01-277 system and Section 3.7 for an 01-339 system.

Cabling and strapping information for the type 01-339 system that is the same as the 01-277 system is not repeated in Sections 3.5 and 3.7. Instead, simple references are made to Sections 3.4 and 3.6 as appropriate.

3.2 SYSTEM LOCATION

The Model 3203 System cabinet is designed to be located anywhere in an office environment but it is recommended that the cabinet be out of the mainstream of traffic. The base of the cabinet provides 1.5" on either side of the cabinet for necessary air flow. It is recommended that additional space be allocated around one side of the cabinet to provide access to the side panel screws. Environmental recommendations are provided in Section 2.6.

3.3 BOARD CONFIGURATION

Figure 3-1 shows the system backpanel of the Model 3203 System cabinet and the location of the boards in the cabinet. Slot 5 is dedicated to the power supply board; slot 4 is dedicated to the central processing unit (CPU)/memory board; slot 3 is dedicated to the multiperipheral controller (MPC) board; and slot 2 is dedicated to the intelligent peripheral controller (IPC) board. Slots 1 and 0 are reserved for optional boards.

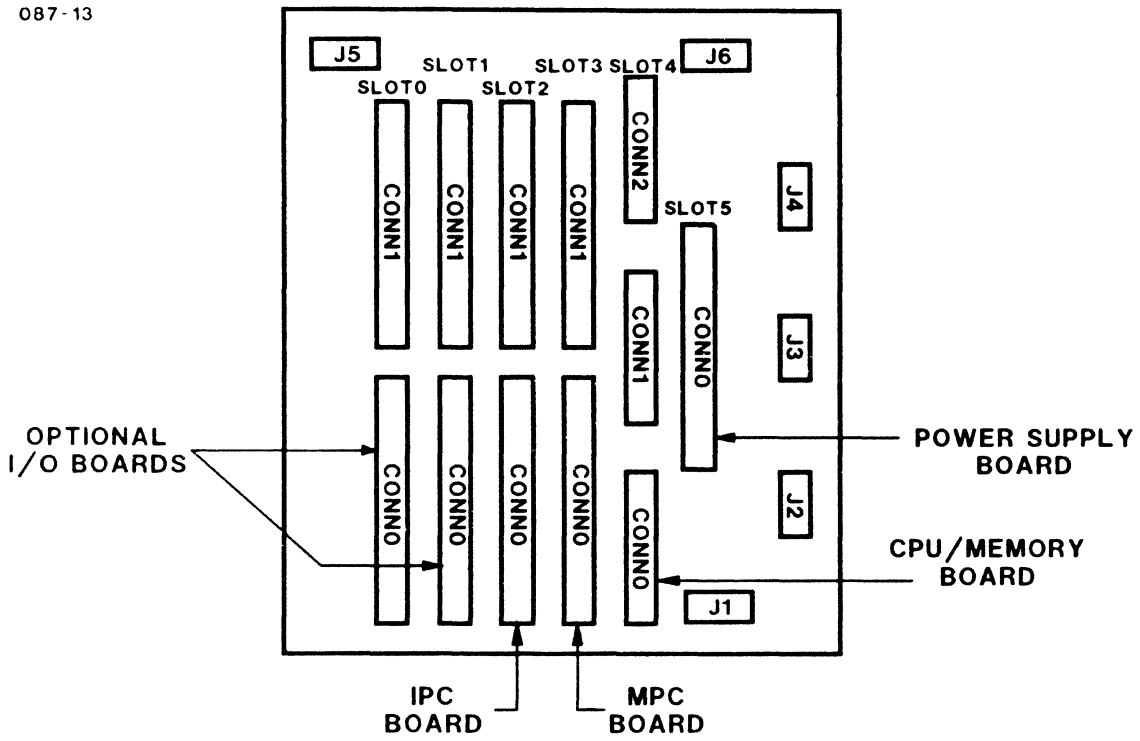


Figure 3-1 Model 3203 Backpanel Layout
(As Viewed From Back Of Cabinet)

3.4 CABLING FOR TYPE 01-277 SYSTEMS

The following sections (3.4.1 through 3.4.6) provide cabling information for the type 01-277 Model 3203 System. See Figure 3-2 and Information Drawing 01-277 D12 for diagrams of the system cabling.

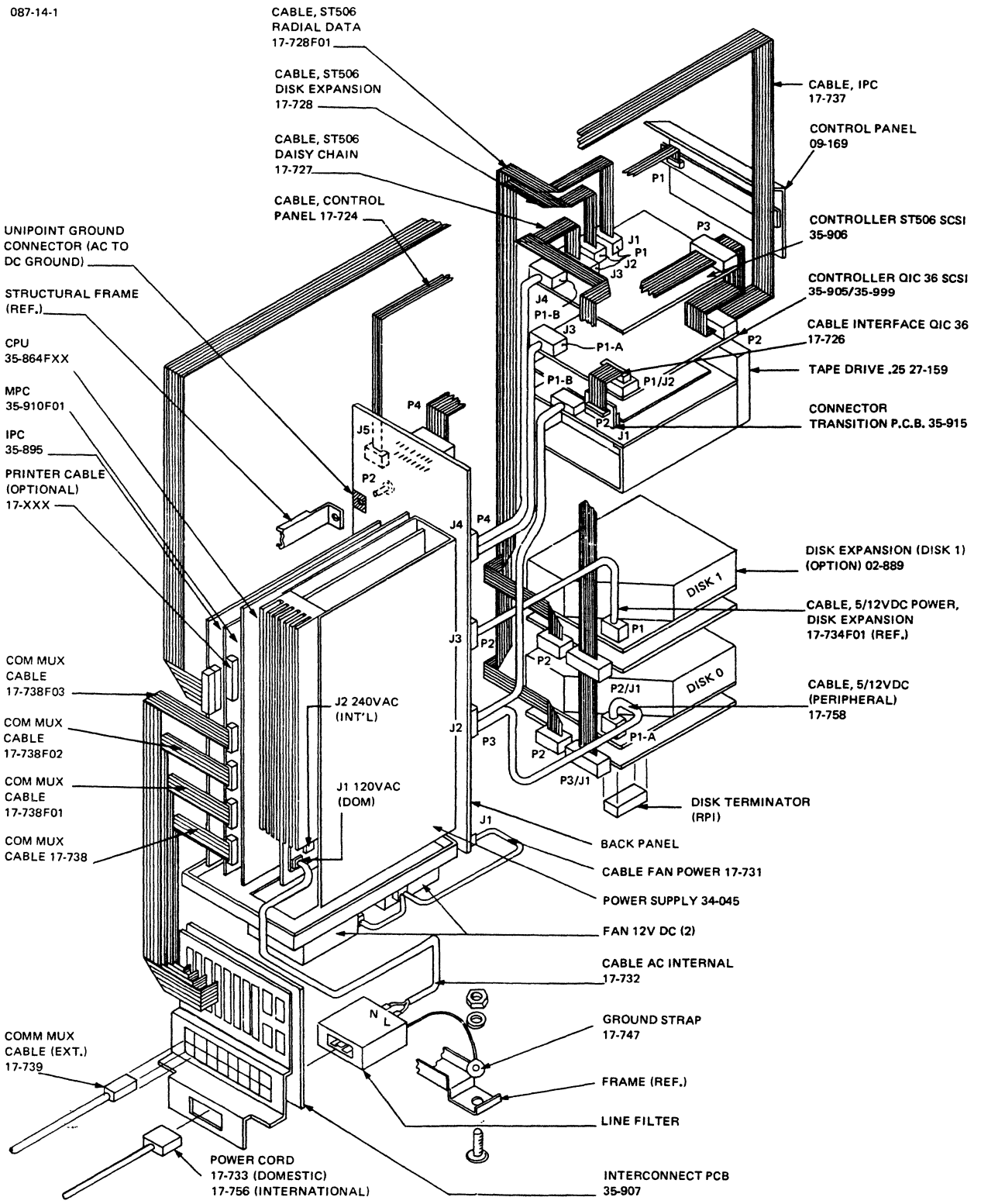


Figure 3-2 01-277 System Cabling Diagram

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3.4.1 Intelligent Peripheral Controller (IPC) Cabling

The following small computer system interface (SCSI) bus signal cable is required to connect the IPC board to the disk and tape controllers.

- 17-737 127cm (50") ribbon cable. Connector P1 plugs into connector 2 (CONN2) on the front of the IPC board, plug P2 connects to J1 of the SCSI/QIC36 tape controller (35-905), connector P3 plugs into J7 on the SCSI/ST506 disk controller (35-906) and plug P4 terminates at system backpanel connector J6.

3.4.2 Disk Controller/Disk Drive Cabling

The following cables are required to connect the SCSI/ST506 disk controller (35-906) to the disk drive.

- 17-727 67.3cm (26.5") ST506 daisy-chain ribbon cable. Plug P1 connects to J3 on the disk controller and plug P3 connects to J1 on disk 0. P2 is not connected for a single disk configuration. When a second disk drive is configured into the cabinet, plug P2 is connected to J1 on disk 1 at the time of that configuration.
- 17-728 F01 67.3cm (26.5") ST506 radial-data ribbon cable. Connector P1 plugs into J1 on the disk controller and connector P2 mates with J2 on disk 0.
- 17-728 F00 52.5cm (21") ST506 expansion-disk signal cable. This cable is used when a second disk drive is configured into the cabinet. Plug P1 connects into J2 on the disk controller (35-906) and connector P2 mates with J2 on disk 1.

3.4.3 Tape Controller/Tape Drive Cabling

The following cable is required to connect the SCSI/QIC36 tape controller (35-905) to the tape drive.

- 17-726 5.08cm (2") QIC36 tape interface cable. Connector P1 Plugs into J2 on the tape controller and plug P2 connects to J1 on the 35-915 transition printed circuit (PC) board mounted to the tape drive. For details of the 35-915 transition board, see Functional Schematic 35-915 C08.

3.4.4 Multiperipheral Controller (MPC) Board Cabling

The user peripheral controllers or terminals are connected to the MPC via the 34-pin, front-edge CONN2:5. Each connector services two full-duplex (FDX) channels:

CONN2 = channels 0 and 1

CONN3 = channels 2 and 3

CONN4 = channels 4 and 5

CONN5 = channels 6 and 7

The line printer interfaces to the MPC via the 34-pin front-edge CONN6.

The following internal cables are required to connect the MPC board to the input/output (I/O) connector panel.

- 17-738 F00 17.8cm (7") communication multiplexor (COMM MUX) cable. This cable is connected between front-edge CONN2 on the MPC board and connector J1 on the I/O connector panel.
- 17-738 F01 27.9cm (11") COMM MUX cable. This cable is connected between front-edge CONN3 on the MPC board and connector J2 on the I/O connector panel.
- 17-738 F02 35.6cm (14") COMM MUX cable. This cable is connected between front-edge CONN4 on the MPC board and connector J3 on the I/O connector panel.
- 17-738 F03 40.6cm (16") COMM MUX cable. This cable is connected between front-edge CONN5 on the MPC board and connector J4 on the I/O connector panel.

This configuration allows for asynchronous operation only since internal connectors J1 through J6 on the I/O connector panel are connected only to asynchronous external connectors J1A/B through J6A/B. For synchronous operation or to run remote diagnostics, one of these cables must be connected from MPC front-edge connectors 2 through 5 (CONN2:5) to internal connector J7 or J8 on the I/O connector panel. The 17-738 Fxx cable supports both synchronous and asynchronous operation. Cabling for the second MPC board is described in Section 3.9.3.

3.4.5 AC Power Cables

This section describes the power cables which distribute AC power through the system. Figure 3-3 shows the power cabling for type 01-277 systems.

- 17-733 289.6cm (114") 13A, 125VAC domestic power cable. This cable has a 3-wire female plug that connects to the 15A line filter and a 3-wire 15A, 125VAC connector (NEMA reference 5-15) which connects into an appropriate wall receptacle.

- 17-756 289.6cm (114") 6A, 250VAC international power cable. This cable has a 3-wire female plug that connects to the 15A line filter. No connector is provided at the other end of this cable to allow the user to provide a connector which complies with local codes.

- 17-732 40.6cm (16") internal power cord. For domestic (120VAC) use, this cable connects from the 15A, 250VAC line filter to J1 (AC IN) located on the 35-903 power supply board. For international use (230VAC), this cable connects from the line filter to J2 (AC IN) located on the 35-903 power supply board. Figure 3-3 shows the location of these connectors on the power supply board.

NOTE

The Model 3203 System should have a separate AC circuit. Other electrical devices on the same circuit can cause power surges.

3.4.6 DC Power Cables

The following DC power distribution cables are required to carry DC power between the power supply and the system major assemblies. Also included is a description of the control panel cable. Figure 3-3 shows this cabling.

- 17-731 fan power cable. This cable connects both fans to connector J1 on the system backpanel.

- 17-724 50.8cm (20") control panel cable. This cable is connected between the control panel and the system backpanel. Plug P1 is connected to the control panel and plug P2 is connected to J5 on the system backpanel.

- 17-734 F00 5/12VDC controller power cable. This cable connects the system backpanel to both the disk and tape controllers. Plug P4 is connected to J4 on the system backpanel. Plug P1-A is connected to J3 on the tape controller (35-905) and plug P1-B is connected to J4 on the disk controller (35-906).

- 17-758 5/12VDC power cable. This cable connects the system backpanel to both the disk and tape drives. Connector P3 is connected to J2 on the system backpanel. Connector P1-A is connected to J3 on disk 0 and connector P1-B is connected to J3 on the tape drive.

- 17-734 F01 5/12VDC expansion disk power cable. This cable is used if the system is configured with a second disk drive. Plug P2 is connected to J3 on the system backpanel and plug P1 is connected to J3 on disk 1.

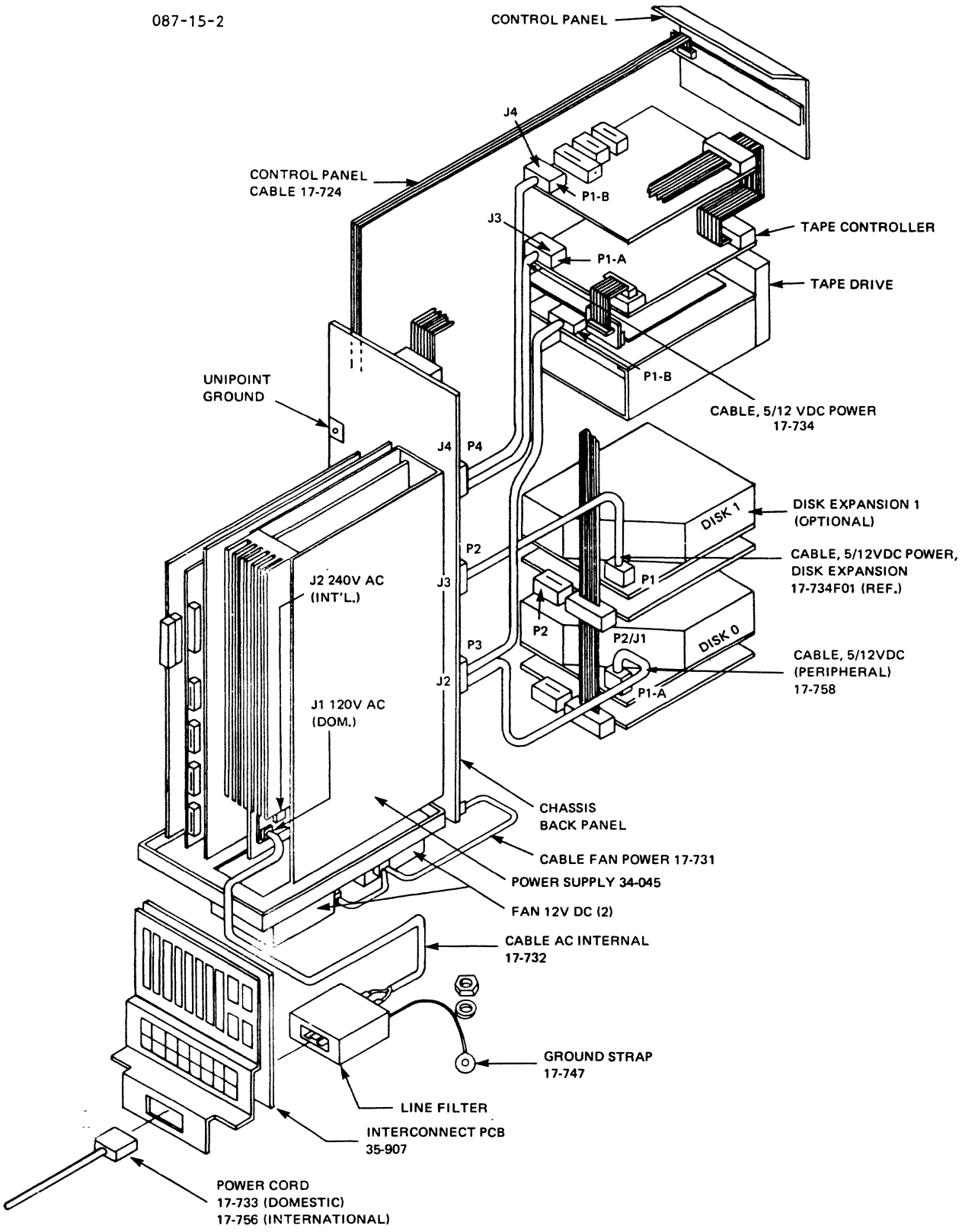


Figure 3-3 01-277 System Power Supply Cabling

3.5 CABLING FOR TYPE 01-339 SYSTEMS

The following sections (3.5.1 through 3.5.4) provide cabling information for the type 01-339 Model 3203 System. Refer to Figure 3-4 and Information Drawing 01-339 D12 for diagrams of the cabling for this system.

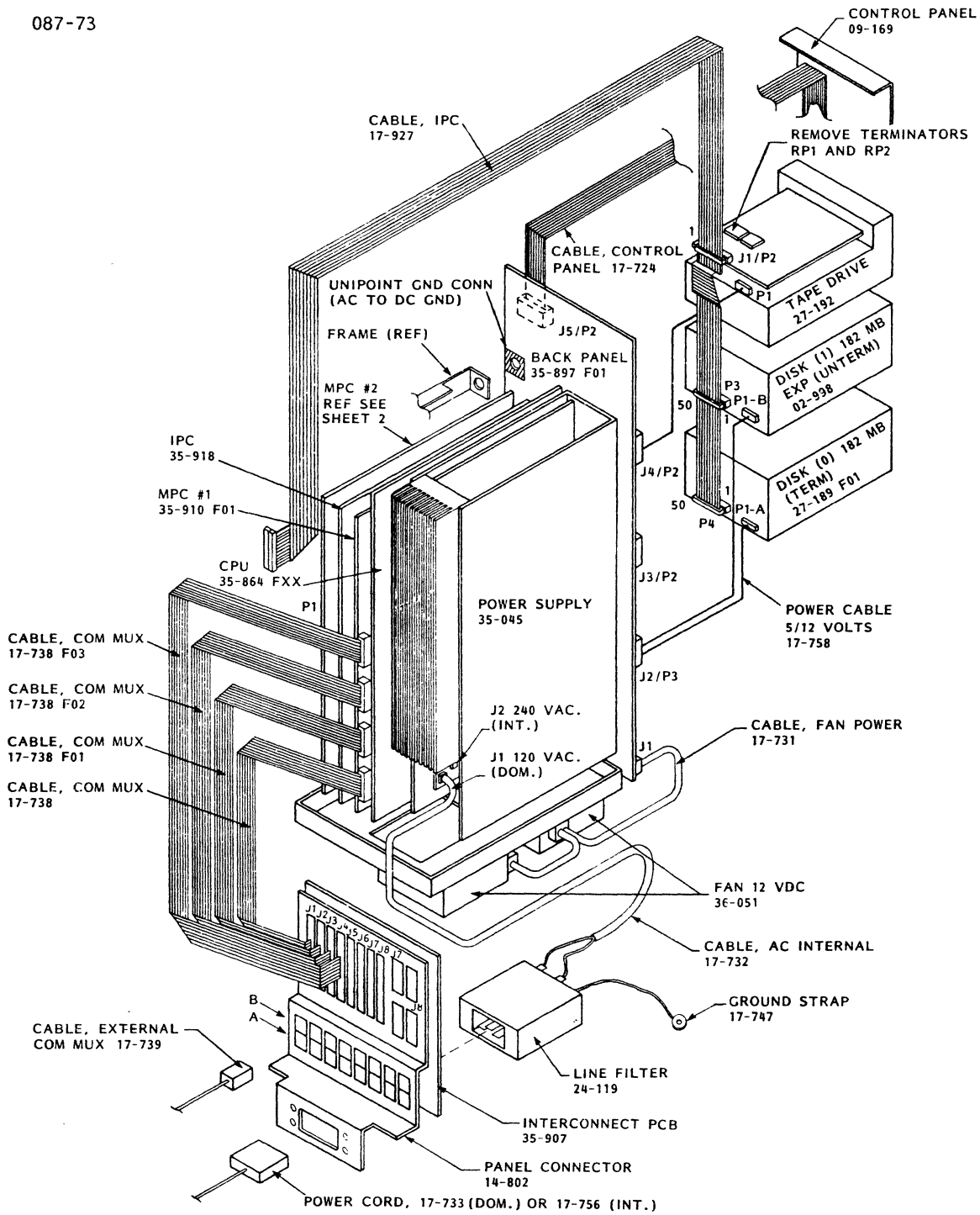


Figure 3-4 01-339 System Cabling Diagram

3.5.1 IPC/Disk and Tape Drive Cabling

In type 01-339 systems, a single daisy chain cable with four connectors provides the required link between the intelligent peripheral controller (IPC) and the tape and disk drive units. This link represents the SCSI signal bus.

The IPC cable (17-927) is a 50 conductor ribbon cable and is about 105cm (41.3") in length. Connector P1 plugs into connector 2 (CONN2) at the front of the IPC board; plug P2 connects to J1 on the tape drive unit; plug P3 mates with the connector at the back of the second disk drive (disk 1), when provided, and; plug P4 mates with the 50 pin connector at the rear of disk drive 0.

3.5.2 Multiperipheral Controller (MPC) Board Cabling

All cabling and cable routing for the MPC in the type 01-339 system is identical to the cabling described for the 01-277 type system. Refer to Section 3.4.4 and Figure 3-2 for this information.

3.5.3 AC Power Cables

The AC power cables and cable routing for the type 01-339 system is the same as that described for in Section 3.4.5 for the 01-277 type system. Refer to Figure 3-5 for details.

3.5.4 DC Power Cables

The DC power cables and cabling is functionally the same as that described in Section 3.4.6 for the 01-277 type system. The main difference is that the DC cables for the type 01-339 system connect directly to the disk and tape drive units which have embedded controllers as illustrated in Figure 3-5.

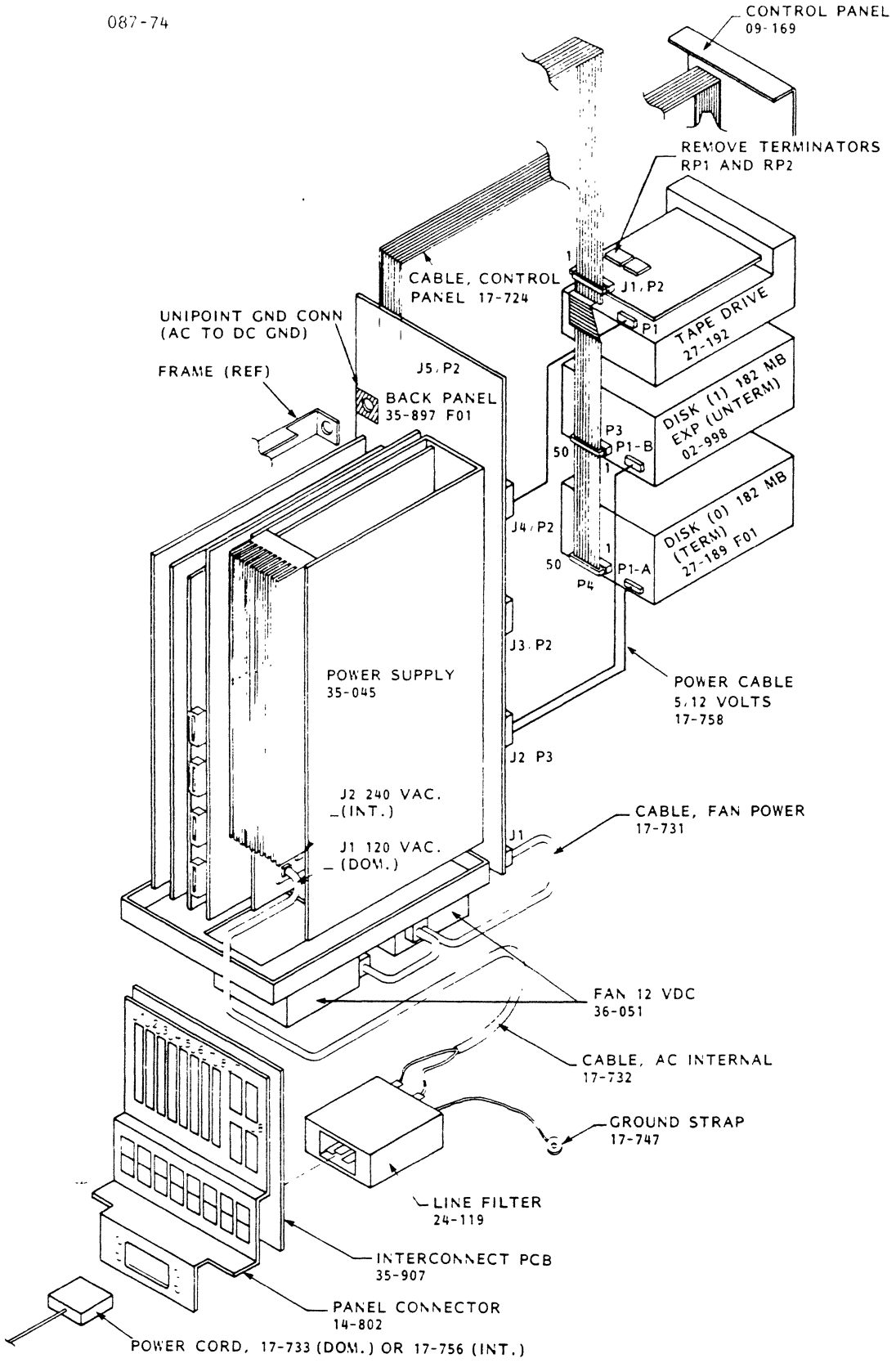


Figure 3-5 01-339 System Power Supply Cabling

3.6 STRAPPING FOR TYPE 01-277 SYSTEMS

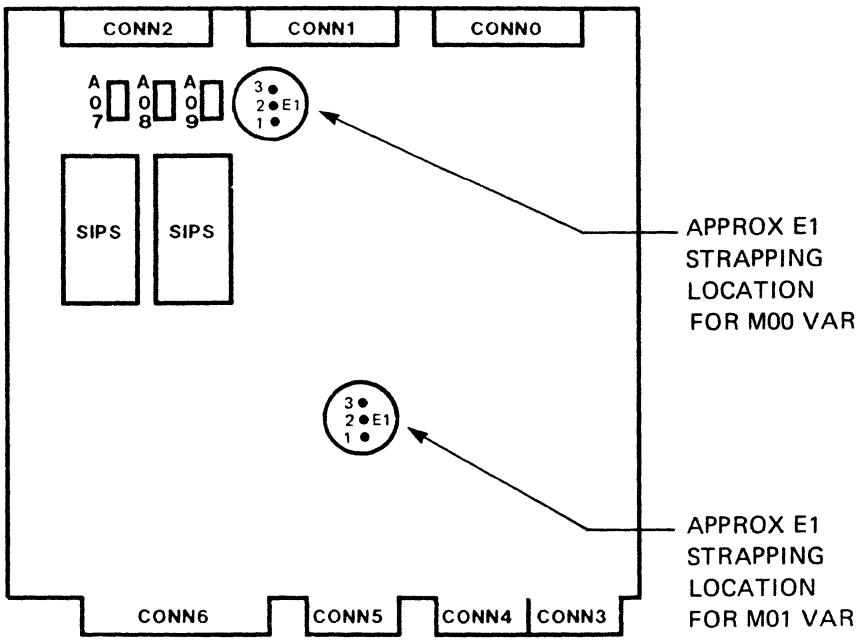
The strapping and switch setting requirements for the various units of the type 01-277 Model 3203 System are described and illustrated in Figures 3-6 through 3-14. Some of these figures are common to the type 01-339 system while others are unique to the type 01-277 system. Figures 3-6 through 3-9 pertain (respectively) to the following units that are common to both types of systems; the CPU/memory, the MPC, the IPC and the power supply boards. Figures 3-10 through 3-14 pertain to units that are unique to the type 01-277 system. These include strapping for the SCSI/ST506 disk controller, the 27-160 and 27-161 drives, the SCSI/QIC36 tape controller, and the 27-159 tape drive. Refer to Section 3.7 for information that is specific to the type 01-339 system.

3.7 STRAPPING FOR TYPE 01-339 SYSTEMS

The strapping and switch setting requirements for the units of the type 01-339 Model 3203 System are defined and illustated in several figures ,some of which are common to the type 01-277 system. These are defined in the following:

- Figures 3-6 through 3-9 pertain to units that are common to both systems as described in Section 3.6.
- Figures 3-15 and 3-16 pertain to the strapping for the type 27-189 disk drive and the 27-192 tape drive which are unique to the 01-339 type system.

087-16-1



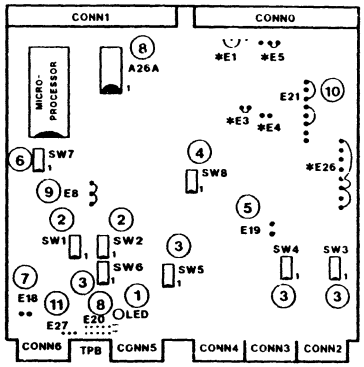
SIZE OF MEMORY (IN MB)	CPU BOARD FUNCTIONAL VARIATION	PAL FUNCTIONAL VARIATION REQUIRED AT LOCATION: A07	A08	A09	STRAP LOCATION E1 M00	M01	MEMORY SIP P/N REQUIRED
0.5	35-864F00	19-339F06	19-339F07	19-339F01	1-2	1-3	19-326
1	35-864F01	19-339F06	19-339F07	19-339F02	1-2	1-3	19-326
2	35-864F05	19-339F09	19-339F10	19-339F03	1-3	1-2	19-517
4	35-864F06	19-339F09	19-339F10	19-339F05	1-3	1-2	19-517

NOTE

The CPU board is configured at time of shipment. This table is to be used as a guide to verify factory configuration.

Figure 3-6 CPU/Memory Board (35-864) Strapping

087 17



*FACTORY SET

1. LED

   Status: ON - Failed power up diagnostics
   OFF - No board clocks.
   Flash - Normal operations.

2. Baud Rate (SW1 & SW2)

   There are four possible 'groups' of baud rates for the COMM MUX ports, selectable by these switches.

BAUD RATE GROUP SELECTION

GROUP	SW2 CLKD	SW1 CLKC	DATA 8 CLKB	DATA 9 CLKA	RATE
0	ON	ON	0	0	50
	ON	ON	0	1	110
	ON	ON	1	0	300
	ON	ON	1	1	1,200
1	ON	OFF	0	0	75
	ON	OFF	0	1	134.5
	ON	OFF	1	0	2,000
	ON	OFF	1	1	3,600
2	OFF	ON	0	0	150
	OFF	ON	0	1	600
	OFF	ON	1	0	4,800
	OFF	ON	1	1	9,600
3	OFF	OFF	0	0	1,800
	OFF	OFF	0	1	2,400
	OFF	OFF	1	0	7,200
	OFF	OFF	1	1	19,200

ON=0
OFF=1

NOTE

Dipswitch positions 1 through 8 correspond directly to the COMM MUX ports 0 through 7.

3. COMM MUX Data Set Status (SW 3 through SW 6)

   a. Switch 3 controls COMM MUX ports 0 and 1, switch 4 controls ports 2 and 3, switch 5 controls ports 4 and 5 and switch 6 controls ports 6 and 7.

   b. For normal operation, switch positions 1, 2, 3 and 5,6,7 on SW3 through SW6 should be OFF and switch positions 4 and 8 should be ON.

4. 8-Channel Data COMM MUX Address Switch (SW 8)

   a. Normal Position: Set rotary switch for hex '1' (Base Address=Hex 10)

5. Line Printer Enable/Disable (E19)

   a. Normal Operation: No strap installed. (Enable printer).

   b. If two MPC's are used (preferrably one populated and one unpopulated version), this strap should be installed on the MPC in the highest priority slot and NOT on the MPC in the lowest priority slot. Line printer should then be connected to lowest priority MPC.

6. Printer Addressing (SW7)

   a. Preferred address; '62'.

   'Dip' switch positions should be:

1	2	3	4	5	6	7	8
ON	OFF	OFF	ON	ON	ON	OFF	ON

7. Line Printer Upper-Case /Lower-Case (E18)

   a. Normal: No strap installed. (Allows lower-case and upper-case letters to be printed. Strapping forces to upper-case letters.)

8. LSU Enable/Disable (E20)

   a. Normal Operation: No strap between pins 100 and 200 (enable). Strap between 100-7 and 200-7 disables LSU.

   b. There are two different versions of copper, R00 and R01, for the MPC board in the Model 3203.

   Strapping for the R00 copper version:

   - To activate the external LSU (A26A), remove the strap between 203-7 and 100-7.
   - To activate the internal LSU, install a strap between 203-7 and 100-7.

   Strapping for the R01 copper version:

   - To activate the external LSU (A26A), remove the strap between 200-7 and 201-7.
   - To activate the internal LSU, install a strap between 200-7 and 201-7.

9. Hardware Communication Assist. (E8).

   a. Normal: Wire wrap 1 to 2 and 3 to 2 (disabled).

10. Precision Interval/Line Frequency Clocks (E21)

    a. Normal Operation: Default to clock addresses 06C and 06D. (Wire wrap pins 3 and 5, also pins 6 and 8.)

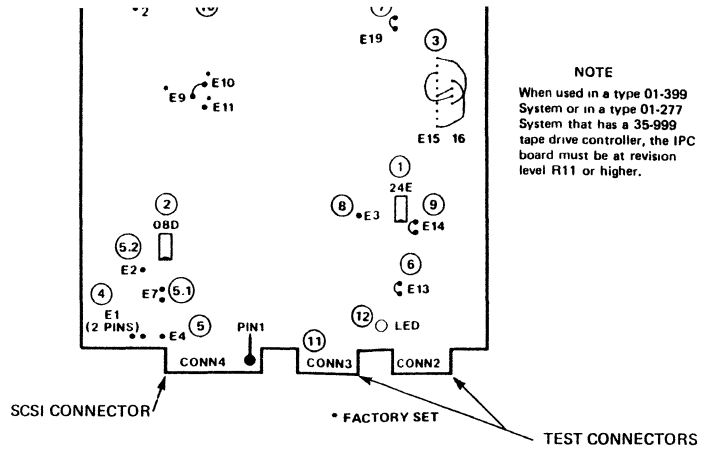
    b. To deactivate PIC/LFC: Wire wrap pins 1 and 2.

11. External Service Aides (E27)

    a. Two service functions are provided by these pins:

       1. External clear (resets SPC) - Momentarily connect pins 2 and 3 together.

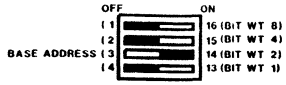
       2. Enable internal sync clocks - Wire wrap pins 1 and 2 together. (Testing only).



NOTE

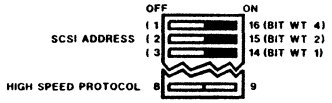
When used in a type 01-399 System or in a type 01-277 System that has a 35-999 tape drive controller, the IPC board must be at revision level R11 or higher.

1. IPC Base Address (Loc. 24E)



a. Normal Settings: Base Address - Switch for 'D' (Hex).

2. SCSI Address/High-Speed Protocol (Loc. 08D)



a. Normal Position: SCSI Address - Switch for '7' (Hex).

High-Speed Protocol - Switch 'ON' enable

3. DRAM Timing (Loc. E15/16)

a. Normal Position: DRAM timing is strapped at factory. (Factory use only)

a. Normal Position: Shorting the pins at E1 will execute a 'test clear'.

5. Bus Clear (Loc. E4)

a. Normal position: Shorting the pins at E4 will execute a 'SCSI' Bus Reset (factory use only).

5.1 SCSI Bus 'Reset' Inhibit (Loc. E7) (factory use only).

5.2 SCSI Bus 'Reset' Test Point (Loc. E2)

a. Normal Operation: Test point carries the SCSI Bus 'reset' signal.

6. IPC Clock (Loc. E13)

a. Normal position: Strapped. (Clock enable).

7. Refresh Clock (Loc. E19)

a. Normal position: Strapped. (Clock enable).

8. Test Points (Loc. E3)

a. E3 is a test point on the microprocessor's address strobe.

9. Dynamic Random Access Memory (DRAM) Parity Strapping (Loc. E14)

a. DRAM parity is normally strapped at pins 1 and 2.

10. High-Speed Protocol Strapping.

a. When the IPC is operating through a I/O switch, E17-1 should be strapped to E18-2. When not transferring through a I/O switch, E17-1 should be strapped to E18-1.

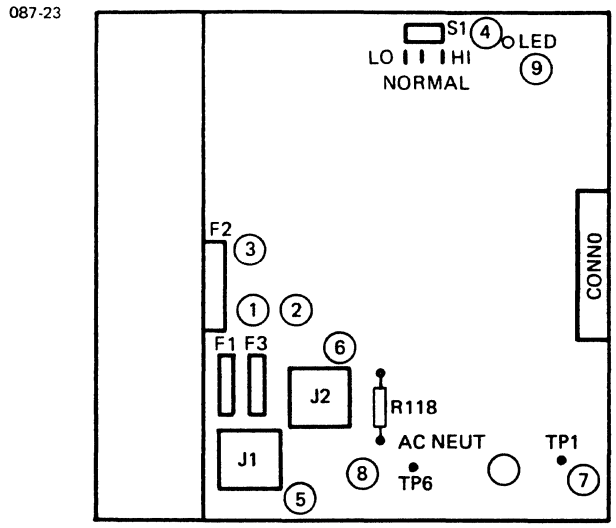
11. Hex Display Port/(CONN3)

a. The Hex Display Port is a 4-digit hex display that provides error codes for the IPC (optional test aid required).

12. LED (Located near CONN3)

a. This LED is an indicator of a potentially bad IPC. During initial power up/self test of the IPC, it remains lit for approximately 5 seconds. There after, it will 'blink' at a speed relative to the activity on the IPC. If after the self test period the LED again remains lit, it indicates a probable IPC 'hard' failure. (Bad board).

Figure 3-8 IPC Board (35-918) Strapping



1. Line Voltage - High (F1)

   a. Incoming voltage - high side. 15A fuse.

2. Line Voltage - Low (F3)

   a. Incoming Voltage-Neutral can be monitored at R118.

3. Bridge Diode Output (F2)

   a. Output of bridge rectifier, D101. 10A fuse.

4. P5 Margining Switch (S1)

   a. Used to 'bias' P5 either plus (+) or minus (-) for testing purposes.

5. Incoming Voltage - Domestic (J1)

   a. Plug output of line filter here for 120VAC use.

6. Incoming Voltage - International (J2)

   a. Plug output of line filter here for 240VAC use.

7. Consolette Power On/Off Signal (TP1)

   a. Test point for scoping power on/off signal from consolette.

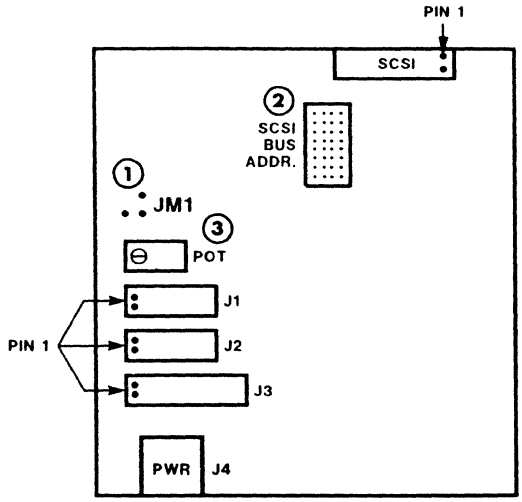
8. Signal Ground (TP6)

   a. Test point for power supply signal ground.

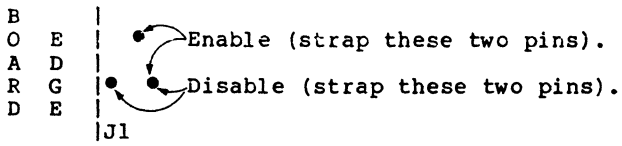
9. LED (P12)

   a. P12 drives the DC fans.

Figure 3-9 Power Supply Board (35-903) Strapping

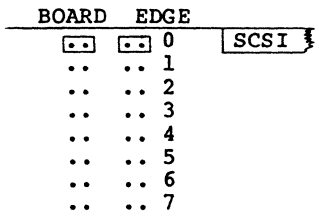


1. Parity Checking Strap (JM1)



Normal Postion: Enable. (May have PC in enable position.)

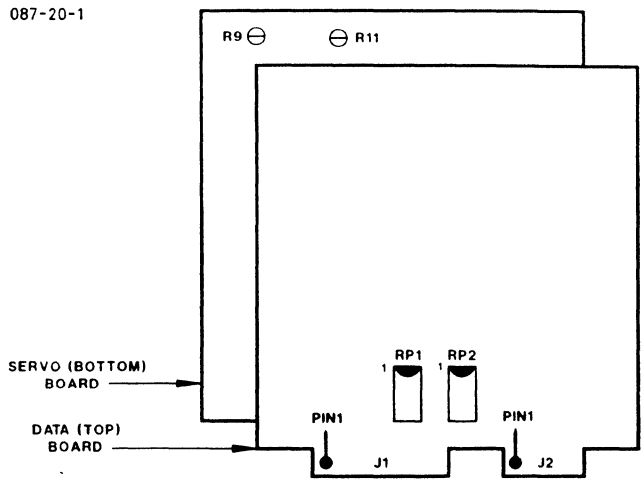
2. SCSI Bus Address Selection.



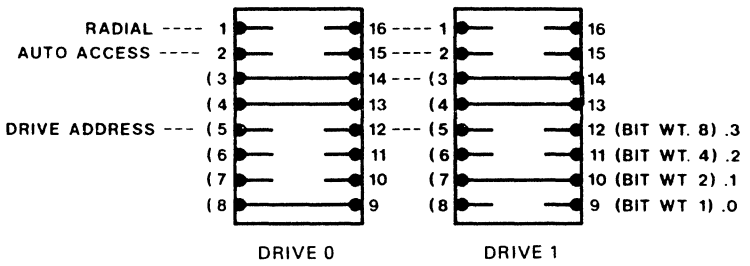
Normal Position: Strap both address '0' positions using straps provided with board, or use wire wrap.

3. Pot factory set. Do not touch.

Figure 3-10 SCSI/ST506 Disk Controller (35-906) Strapping



1. Option Shunt Block. RP2 (P/N 45-134 F02)



NOTE

Shunt block has 'wire' bridges. Left uncut enables the function. Cutting the bridge disables the function.

a. Normal Positions: Radial - Always inactive, cut bridge between 1 + 16.

Auto Access -Is a factory function and is normally cut. With the bridge uncut between 2 and 15 the drive will run a series of random seeks.

Capacity I.D.- Leave factory set

Drive Address- Address plugged for '0' cut the following:
7 to 10
6 to 11
5 to 12

2. Terminator (RP1)

a. Normal Position: Always installed in drive 0. Drive 1 (when present) is not to be terminated in any case.

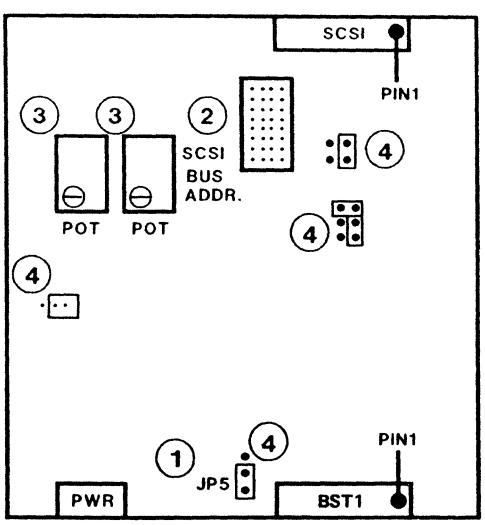
3. Offset Adjustment (R9)

a. Normal Position: Preset at factory for servo system null.

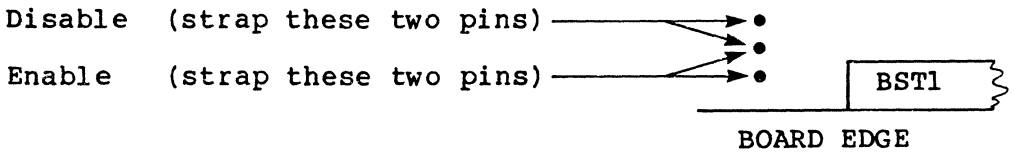
4. Servo Gain Adjustment (R11).

a. Normal Position: Leave factory set.

Figure 3-11 Disk Drive (27-160 and 27-161) Strapping

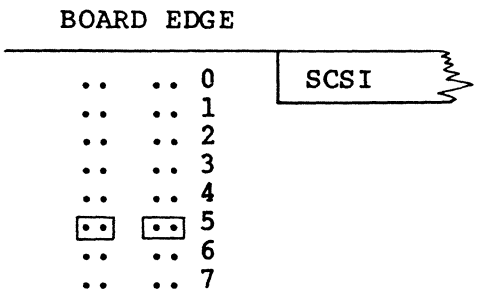


1. Parity Checking strap (JP5).



Normal Position; Enable. (May have PC in enable position.)

2. SCSI Bus Address Selection



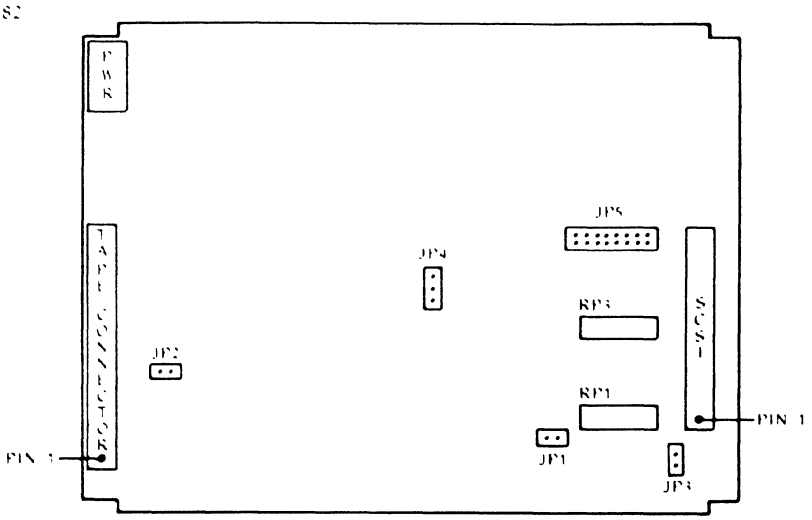
Normal Position: Strap both address '5' positions using straps provided with board, or use wire wrap.

3. Pot factory set. Do not touch.

4. Straps

   a. Other straps are factory preset.

Figure 3-12 SCSI/QIC36 Tape Controller (35-905) Strapping



NOTE

Do not install or use the 35 999 tape controller un less the associated IPC is at Revision Level R11 or higher. Additionally, if the 35 999 controller is installed in a system using the XELOS operating sys tem, ensure that the re vision level of XELOS is at R02 or higher.

1. Reset option (JP1)

strap in place

2. Margin select (JP2)

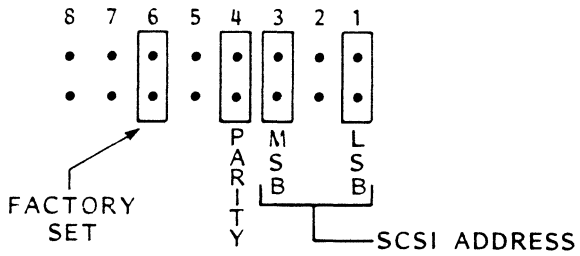
no strap

3. Terminator power (JP3)

4. Prom size (JP4)

strap 2 to 3

5. SCSI bus address and parity selection (JP5)

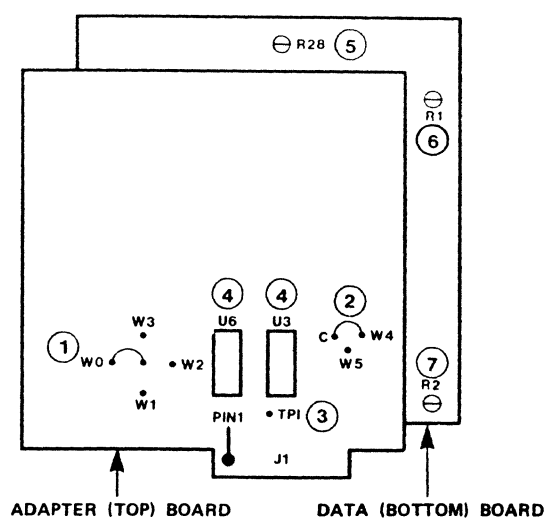


The normal address for this device is '5'. Strap pins 1 and 3 (binary) using the jumpers provided with the board or using wire wrap.

Parity is normally enabled. Strap pins 4.

6. Resistor packs (RP1 and RP3) - Must not be installed.

Figure 3-13 SCSI/QIC36 Tape Controller (35-999) Strapping



1. Drive Addressing (Pins W0 through W3 and C)

   a. Allows drive addressing from '0' to '3'.

   b. Normal Position: Strap W0 to C using vendor supplied straps or wire wrap. (Address '0')

2. LED Operation (Pins W4 through W5 and C)

   a. Enables or disables LED on front of drive to illuminate when drive is selected.

   b. Normal Position: Strap W4 to C using vendor supplied straps or wire wrap. (Illuminates LED when selected.)

3. Test Point 1 (TP1)

   a. Normal Operation: Can use test point to scope drive read data, if desired.

4. Terminators (U3 & U6)

a. Normal Position: Terminators should be installed in both positions.

5. Read Amplifier Gain (R28)

   a. Normal Position: Preset at factory.

6. Read Amplifier Null (R1)

   a. Normal Position: Preset at factory.

7. Drive Motor Tach Gain (R2)

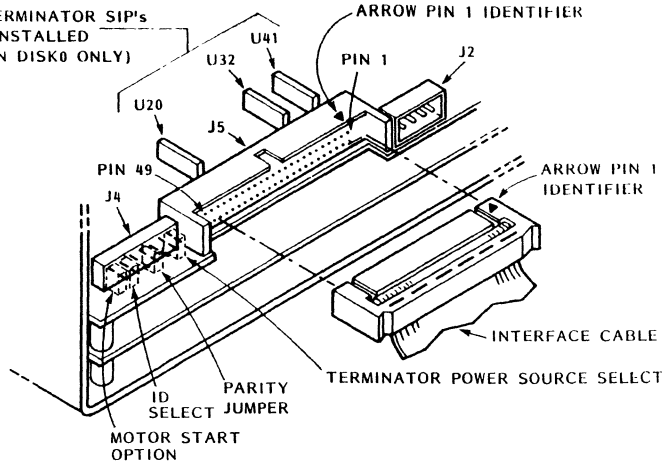
   a. Normal Position: Preset at factory.

NOTE

R1, R2 and R28 should NOT be adjusted by the Field. They are preset by Vendor and are presented for reference only.

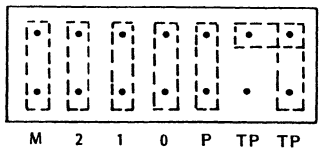
Figure 3-14 Tape Drive (27-159) Strapping

087-75



a. Jumper, Terminator and I/O Cable Location/Identification

087-76



M = Motor Start Option:- Motor starts on command when M is jumpered, otherwise, the disk motor starts on power up. The start on command option is not used in Model 3203 Systems.

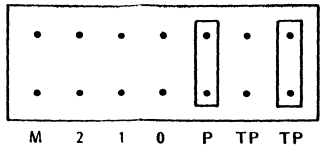
2-0 = Drive Select Positions:- Permits jumper selection of one of eight drive numbers (0-7). Uses binary code (4,2,1) with MS bit at left. Positions 2 (binary 4) and 1 (binary 2) are never used in Model 3203 Systems, which have a maximum complement of two disk drive units.

P = Parity Check:- Parity check for the disk drive is enabled when the P jumper is installed. This is the normal configuration for Model 3203 Systems.

TP = Terminator Power Source Select:- When jumpered at vertical TP position, receives +5V terminator power from source connected to J2 (the system P5 supply). The horizontal TP jumper position is shown for reference only, and is never used in Model 3203 Sytems.

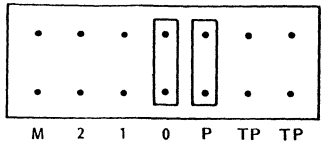
b. Drive ID/Option Select Header (J4) Configuration

087-77



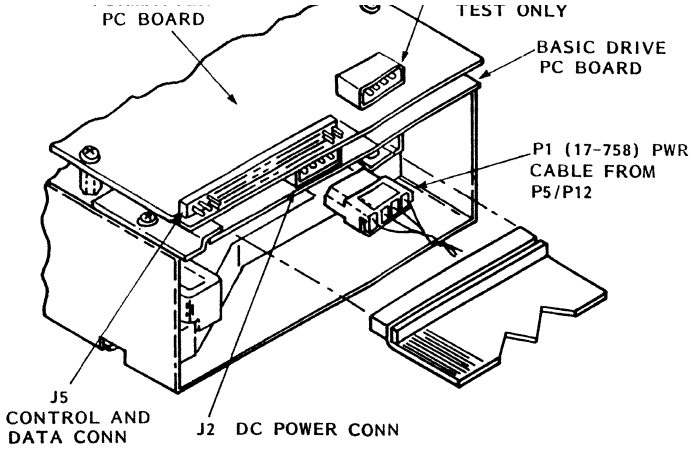
c. Jumper Configuration for Disk 0 (Terminated)

087-78

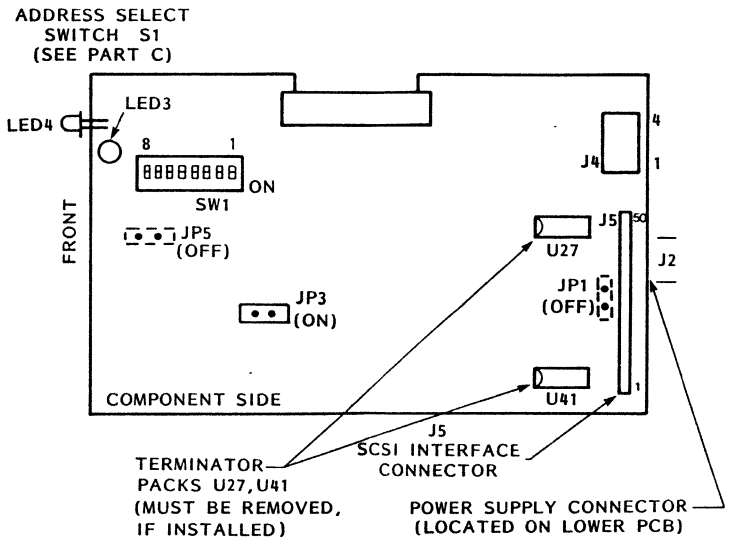


d. Jumper Configuration for Disk 1 (Unterminated)

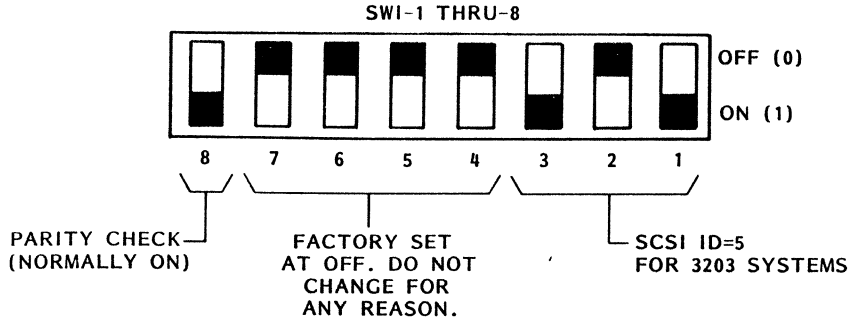
Figure 3-15 SCSI 182MB Disk Drive (27-189) Strapping



. PC Board and Interface Connector Location and Identification



. Formatter PC Board General Layout



c. Address and Option Switch Setup

Jumper JP1 = Removed (Off):- Bus Termination Power Option. Not applicable in Model 3203 Systems. Only the last device on the daisy chain requires terminating resistors. The tape drive is the first device and is always accompanied by the first disk (0) which is configured as the last device on the daisy chain.

Jumper JP3 = Installed (On):- OEM Setup, Undefined. DO NOT REMOVE FOR ANY REASON.

Jumper JP5 = Removed (Off):- Hard/Soft Reset Option. When installed, causes the tape drive to perform a hard power up type reset when the reset signal on the SCSI bus is asserted. The Soft Reset Option (JP5 removed) enables the drive to remove itself from the bus and perform an orderly halt (soft reset) to any operation it is executing.

d. Jumper Configurations/Descriptions

Figure 3-16 SCSI Tape Drive (27-192) Setup and Strapping

3.8 INITIAL SETUP/STARTUP PROCEDURE

The Model 3203 System has an automatic loading feature which provides the user with the means of loading the operating system without operator intervention. The operating systems available with the Model 3203 System are OS/32 and XELOS. OS/32 is Concurrent Computer Corporation's proprietory operating system and XELOS is based on a UNIX® operating system.

The automatic loading procedure is as follows:

1. If the operating system exists on the tape cartridge and not on DISK1 or DISK2, insert the streaming tape cartridge into the tape drive.

2. Switch on DC power by placing the ON/OFF switch on the control panel to the ON (1) position. When the power is on, the bootstrap loads the initial program load (IPL). The IPL provides automatic loading operation with progress messages displayed on the local console. The preferred load devices are selected from those devices that exist under the IPC. These load devices are:

   SCSI DISK 1
   SCSI DISK 2
   SCSI TAPE

3. The IPL runs a basic confidence test and an initial configuration check on the IPC. If there is a hard IPC failure, a default menu is displayed which provides a list of devices from which an operating system could be loaded. If no errors occur, the following message is displayed and the IPL attempts to load the operating system named DEFAULT.OS from the first disk in the system. This name is valid for both the OS/32 and XELOS operating systems.

```
CONCURRENT COMPUTER CORPORATION                IPL06-298F01RXX
      All Rights Reserved                       Copyright 1986

BASIC CONFIDENCE TEST COMPLETE

IPC INITIAL CONFIGURATION CHECK OK
DEV=SCSI DISK 1
```

UNIX is a registered trademark of A.T. & T.

4. At this point, a ten second delay loop is provided for operator intervention if desired. If the operator depresses the asterisk (*) key or the carriage return (RETURN) key, the timeout is aborted and the program proceeds with the current selection. If the operator depresses the BREAK key on the console, the automatic loading procedure is overridden and the standard menu is output. If there is no operator input after ten seconds, the IPL proceeds with the current selection and the following message is output:

```
VOLUME=XXXX
FILE NAME = DEFAULT.OS
```

A ten second delay loop is again provided to allow for operator intervention. As previously stated, if either the asterisk (*) key or return (RETURN) key is depressed, or there is no operator intervention for ten seconds, the IPL attempts to load the operating system. If the operating system is found, it is loaded and the following message is displayed on the console:

```
LOAD COMPLETE
```

and control is transferred to the operating system. If the operating system is not found, the IPL proceeds to search the second disk as indicated by the following message displayed on the console.

```
FILE NOT FOUND
DEV=SCSI DISK 2
VOLUME = XXXX
FILE NAME=DEFAULT.OS
```

5. If no second disk is configured in the system, the IPL prints the following message and proceeds to search the tape.

```
UNRECOVERABLE ERROR ON DEVICE XXX, STATUS = YY
DEV=SCSI TAPE
FILEMARKS=
```

If the system is configured with two disks, the IPL now searches the second disk for DEFAULT.OS. Again the IPL provides two 10 second delay loops for operator intervention. If the operating system is found, the message LOAD COMPLETE is displayed and control is transferred to it. If the operating system is not found the IPL proceeds to search the tape for the operating system as indicated by the following message displayed on the console.

```
FILE NOT FOUND
DEV=SCSI TAPE
FILE MARKS=
```

6. When loading from the tape, no particular operating system name is sought. After the FILEMARKS = prompt is displayed, a ten second delay loop is provided to enable the operator to specify a decimal number indicating at what filemark the IPL is to begin loading. For example, if the operator enters a 2 after the FILEMARKS = prompt, the operating system is loaded from the record following the second filemark. If no decimal number is specified, the IPL loads from the first file on the streaming tape. As soon as the operating system has been loaded, control is transferred to it. Subsequent screen activity depends on the operating system.

   If no operating system has been found, a default menu is displayed which provides a list of devices from which you could load an operating system.

3.9 SYSTEM OPTIONS

The following sections provide information on memory expansion, the second disk, the second MPC, the Ethernet data link controller (EDLC) and universal logic interface (ULI) boards.

3.9.1 Memory Expansion

The memory capacity of the 01-277 Model 3203 System ranges from 512kB to 4MB of directly addressable MOS memory. The 01-339 system has a minimum capacity of 2MB and is expandable to 4MB. When using the 256kb x 1 single in-line packages (SIPs) (19-326) the CPU/memory board can be configured with either 512kB or 1MB of memory. When using the 1024kb x 1 SIPs (19-517), the CPU/memory board can be configured with either 2MB or 4MB of memory.

There are two rows provided on the CPU/memory board for memory. When using the 256kb SIPs (19-326), each row contains 0.5MB of memory. When using the 1024kb SIPs (19-517), each row contains 2MB of memory. A summary of the memory configurations with necessary strapping and programmable array logic (PAL) changes are shown in Figure 3-6.

Note that current Model 3203 Systems are provided with 2MB or 4MB of memory using the 1024kb SIPS. The smaller increments of memory, using the 256kb SIPS, are no longer offered. The information concerning the 256kb SIP configurations is retained in this manual to satisfy the requirements of earlier users.

3.9.2 Second Disk Drive

When a second disk drive is configured into the system, mount it in the cabinet directly above the first disk drive. Secure the drive to the disk mounts with four #6-32 x .25in phillips head screws and lock washers. Then, install and/or connect the necessary cables, as applicable.

Signal cabling for the expansion disk drive is described in Section 3.4.2 for type 01-277 systems and Section 3.5.1 for type 01-339 systems.

DC power cabling for the expansion disk drive is described in Section 3.4.6 for type 01-277 systems and Section 3.5.4 for type 01-339 systems.

3.9.3 Second Multiperipheral Controller (MPC) Board

The second MPC board can be installed in the first available I/O slot (slot 1 or slot 0) and connects into the MUX bus on the CONN0 side of the backpanel. When two MPCs are configured in the system, the line printer interface is enabled only on the second MPC board in the system.

To facilitate cabling for the second MPC board, relocate the cables for the first MPC board at the I/O connector panel as follows:

- Move P1 connectors at J1, J2, J3 and J4 to J5, J6, J7 and J8.
- Change the Communication Multiplexor cable (17-739) from position 1A to position 5A.

After relocating the cabling for the first MPC board, install the cables provided with the second MPC board as outlined in Table 3-1. In all cases, cable connector P1 mates with the specified connector (CONNn) on the MPC board, and P2 mmates with the specified connector (Jn) on the I/O Panel.

TABLE 3-1 SECOND MPC BOARD CABLING

COMM MUX CABLE	LENGTH	INTERCONNECTIONS	
		MPC BOARD	I/O PANEL
17-738 F00	17.8cm (7")	CONN2	J1
17-738 F01	27.9cm (11")	CONN3	J2
17-738 F02	35.6cm (14")	CONN4	J3
17-738 F03	40.6cm (16")	CONN5	J4

3.9.4 Ethernet Data Link Controller (EDLC)

The Ethernet controller (32-217) is built on a 38.1cm x 38.1cm (15in x 15in) PC board with the Ethernet protocol module (EPM) mounted on it. The EDLC can be installed in the first available I/O slot (slot 1 or slot 0) and connected to the private multiplexor (PMUX) bus on the CONN1 side of the backpanel.

Refer to the Series 3200 Ethernet Controller Installation and Theory of Operation Manual for instructions to connect cable 17-785 and for strapping details of the EDLC board.

3.9.5 Universal Logic Interface (ULI) Board

The ULI (35-860) is configured on one 37.5cm (15in) board that is divided into two halfboard sections. One section contains general-purpose interface logic components that allow users with compatible device controllers to interface directly to the system. The other section provides a halfboard wire-wrap field which allows the user to construct a compatible device controller to interface user peripheral equipment to the system.

The ULI can be installed in either available I/O slot (slot 1 or slot 0) and connects to the PMUX bus on the CONN1 side of the backpanel.

For details of the ULI board, see the Universal Logic Interface (ULI) Installation, Theory of Operation and Programming Manual.

3.9.6 Model 6100 or Model 6312 Video Display Unit (VDU)

External signal cable 17-739 FXX connects the Model 6100 or Model 6312 VDU to the Model 3203 System. The designation FXX represents a functional variation (F) of the part number that is unique to cable length requirements. Where XX can be a number from 00 through 99. The 17-739 FXX cable is equipped with a standard 25-pin RS232 connector which plugs into the modem connector at the rear of the VDU monitor and a keyed modular connector which plugs into one of the asynchronous connectors J1-A/B through J8-A/B on the I/O connector panel. The VDU being used as the system console should be connected to connector J1-A on the I/O connector panel as shown in Figure 3-17.

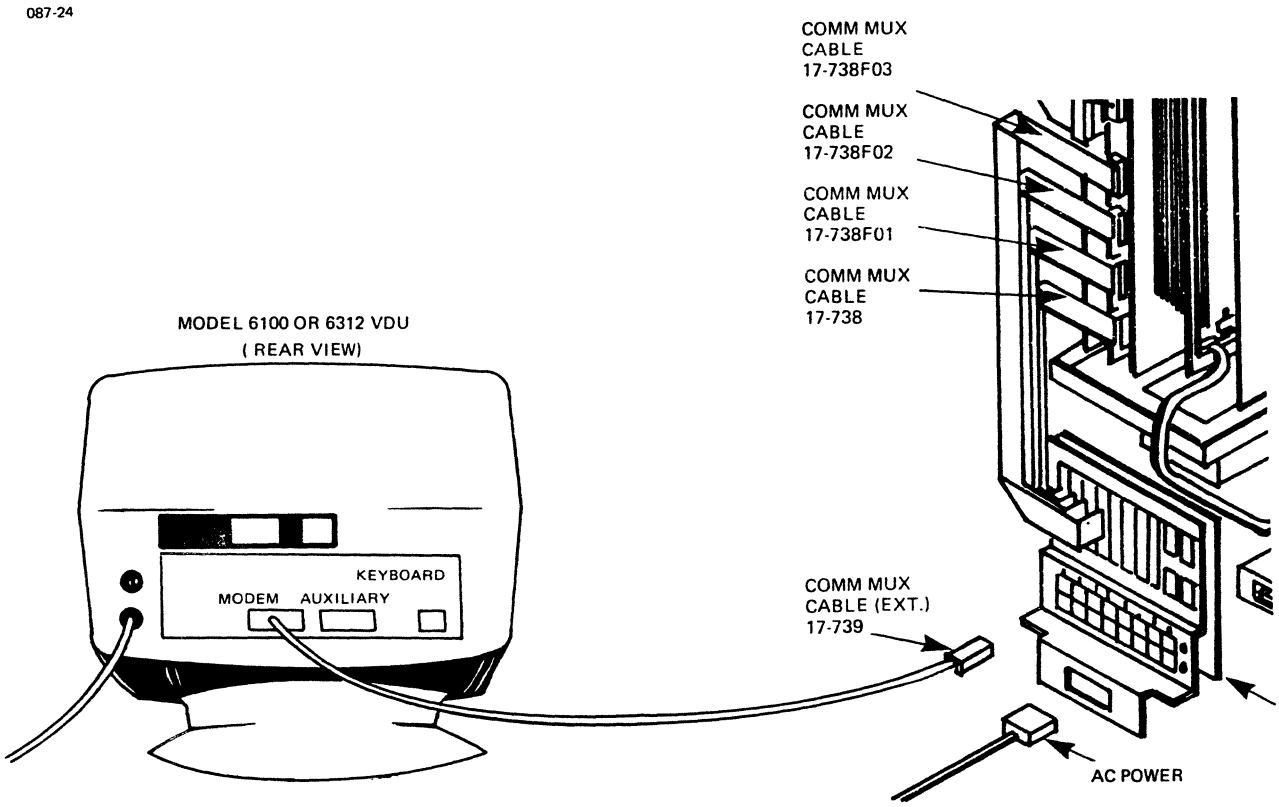


Figure 3-17 VDU Cabling

3.10 INTERRUPT PRIORITY

The acknowledge (ACK) control line, from the CPU/memory board in the vertical chassis, carries the interrupt ACK signal. This line breaks into a series of short lines at each device controller in the chassis slot to form the daisy-chained priority. The ACK signal must pass through every controller equipped with interrupt control circuits in a serial fashion.

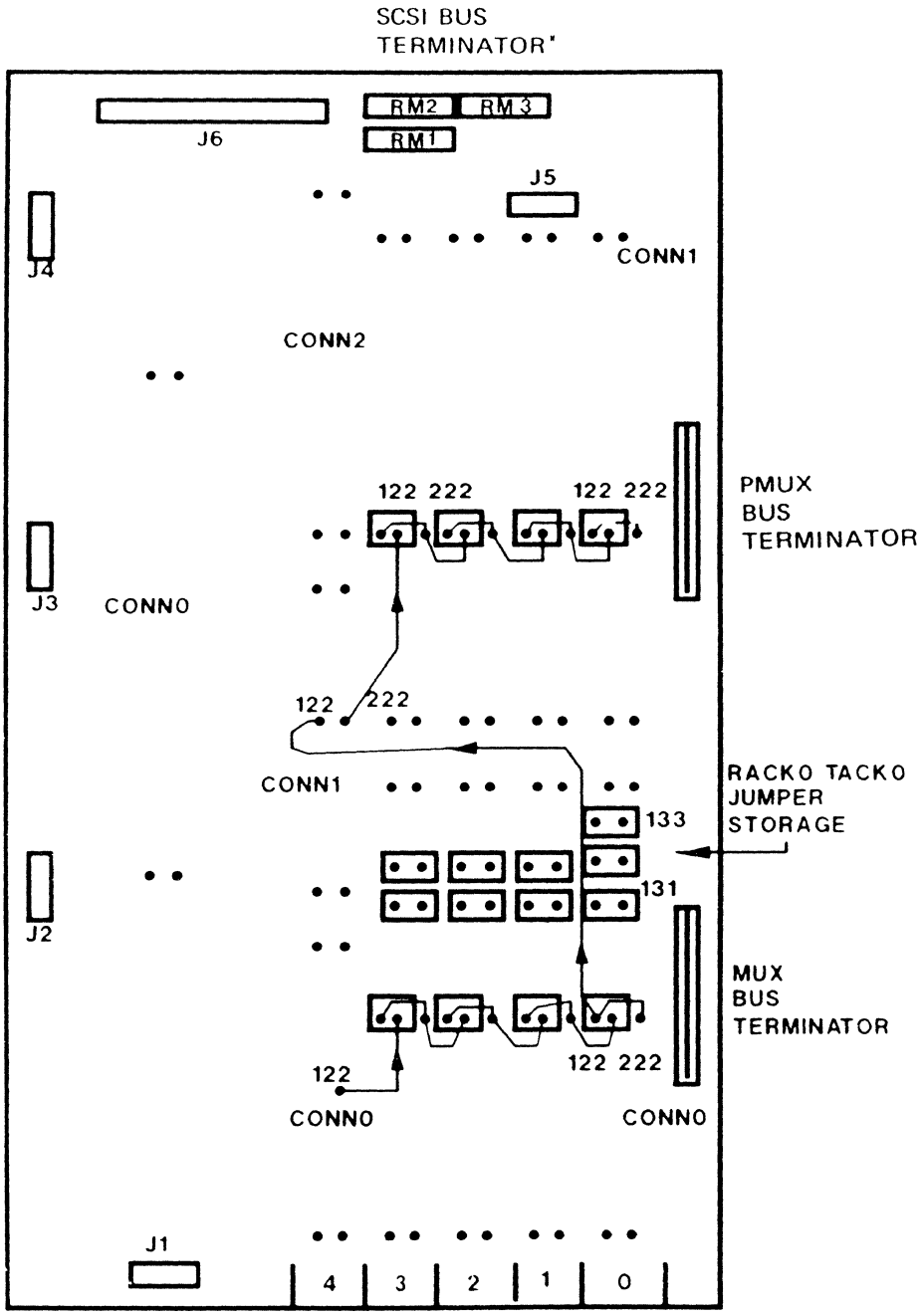
Backpanel wiring for interrupt control at a given position is as follows. The received ACK (RACK0) is input at pins 122-0 and 122-1 and the transmitted ACK (TACK0) is output at pins 222-0 and 222-1. The daisy-chain bus is formed by a series of line segments that connect TACK0 at pins 222-1 and 222-0 of a given slot to RACK0 at pins 122-1 and 122-0, respectively, of the next slot (lower priority). Slots unequipped with controllers are bypassed by Berg-type jumpers that short pin 122-1 and pin 122-0 to pin 222-1 and pin 222-0, respectively. Backpanels are wired with Berg-type jumpers on all slots. Therefore, whenever a chassis slot is equipped with a controller that requires interrupt capability, the Berg-type jumper between pin 122-1 and pin 222-1 and/or the Berg-type jumper between pin 122-0 and pin 222-0 must be removed at that slot according to installation instructions for that controller.

NOTE

Do not discard these jumpers. The Berg-type jumpers removed from active slots should be stored on pins 131 or 132 of the same slot. See Figure 3-18 for jumper the storage area.

When the PMUX bus, which is wired down the CONN1 side of the chassis, is idle, it serves as an extension of the MUX bus. During PMUX operation, MUX bus RACK0/TACK0 operates on the CONN0 side of the backpanel and the PMUX bus RACK0/TACK0 operates independently on the CONN1 side of the system backpanel.

Figure 3-18 shows an example of the interrupt priority wiring; the arrows indicate the direction of priorities. Slot 3 on the CONN0 side of the backpanel has the highest priority. Slot 0 on the CONN1 side of the backpanel has the lowest priority. When PRACK0 is generated by the CPU for the PMUX bus, slot 3 on the CONN1 side has the highest priority and slot 0 on the CONN1 side has the lowest priority. The last slot of the MUX bus must have TACK0 wired back to slot 4, pin 122 on the CONN1 side of the backpanel.



* SCSI BUS TERMINATOR COMPONENTS (J6 AND RM1–RM3) ARE NOT INCLUDED ON THE TYPE 01-339 MODEL 3203 SYSTEMS

Figure 3-18 Interrupt Priority Backpanel Wiring (As Viewed From The Front Of The Cabinet)

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

This chapter provides a detailed description of the major assemblies and the overall system theory of operation. Also included is a description of the system options.

4.2 CONTROL PANEL

The control panel for the Model 3203 System contains an ON/OFF switch, a red LED power indicator and a red LED fault indicator. Control panel details are shown on Functional Schematic 35-902 B08.

- ON/OFF (1/0) SWITCH

  DC Power is applied to the system when this switch is in the ON (1) position. AC power is present whenever the AC power cable is plugged into an AC wall receptacle.

- POWER INDICATOR

  This LED lights when the ON/OFF switch is in the ON position and the 5VDC power is present.

- FAULT INDICATOR

  This LED lights when the power is turned on and remains lit while the basic confidence and memory tests are running. The LED goes out on successful completion of the self-tests. If the processor self-test fails, the LED remains lit. The fault indicator also lights when an invalid condition, referred to as a system BOMB, occurs. System BOMBS are associated with the microinterrupt logic as described in the 35-864 Central Processing Unit CPU/Memory Board Theory of Operation Manual.

4.3 CENTRAL PROCESSING UNIT (CPU)/MEMORY BOARD

The 35-864 central processing unit (CPU)/memory board is a single-board processing unit with an on-board memory. It has a built-in single and double precision floating point, provides user and memory interface and manages all system input/output (I/O).

The CPU board is comprised of six functional units: control, execution, memory, power up/down, consolette interface and I/O.

These six units are synchronized by a 5MHz clock (200ns cycle). This cycle is divided into four 50ns states (0 to 3) with most microinstruction execution being completed within one cycle. These four states are used to divide the operation into two or more tasks.

The following sections (4.3.1 through 4.3.6) provide a brief overview of the functional units identified above. Refer to the 35-864 Central Processing Unit CPU/Memory Board Theory of Operation Manual for detailed functional descriptions and circuit analysis.

4.3.1 Control Unit

The control unit contains the control store (CS), control register (CR), microaddress sequencer, N register (NR), condition code multiplexor (CCMUX), instruction registers, macrointerrupt and microinterrupt circuitry.

4.3.2 Execution Unit

The execution unit contains an arithmetic logic unit (ALU), a parallel multiplier, a variety of registers and a constant progammable read only memory (PROM).

4.3.3 Memory

The CPU/memory board supports up to 4MB of directly addressable main memory by using 256kb random access memory (RAM) technology. When using 64kb RAMs, on-board memory is limited to 1MB.

The memory unit contains the address registers, memory address translator (MAT), error check and correction (ECC), error logger, direct memory access (DMA) word counter and memory refresh.

4.3.4 Input/Output (I/O) Interface

The CPU/memory board incorporates two communications buses. The man/machine multiplexor (MUX) bus and the machine/machine private multiplexor (PMUX) bus.

- MUX bus

  The MUX bus can address up to 1,023 medium-speed devices such as printers, consoles, card readers, etc.

- PMUX bus

The PMUX bus interfaces high-speed secondary storage devices such as disks and magnetic tapes to the integrated selector channel (ISELCH). The PMUX bus supports five device controllers. Once the PMUX bus has been activated and interfaced to the ISELCH for a DMA transfer, it functions in a completely autonomous fashion, with one controller or device at any one time. When the PMUX bus is not interfaced to the ISELCH, it is placed in the idle mode and functions as an extension of the MUX bus.

The ISELCH interfaces with the PMUX and provides for DMA transfers.

4.3.5 Consolette Interface

The consolette logic section of the CPU/memory board interfaces a consolette to the processor. The interface circuitry generates three macrointerrupts and a single instruction mode signal.

4.3.6 Power Up/Down

The power up/down section of the CPU/memory board monitors both the P5 and P5U voltage levels and generates power fail signals, which are sent to the consolette interface logic. These signals are gated with other signals to generate power fail interrupts.

4.4 MULTIPERIPHERAL CONTROLLER (MPC)

In the Model 3203 System, the MPC board provides eight FDX RS232C interfaces for eight user devices or terminals. The first MPC (35-910-F01) provides the precision interval clock/line frequency clock (PIC/LFC), an LSU with a watchdog timer and a parallel line printer interface. When two MPC boards are configured in a system, the line printer interface is activated only on the second MPC board (35-910 F02).

The following sections describe the major functions of the MPC in further detail.

4.4.1 Data Communications Multiplexor (COMM MUX)

The 8-channel data COMM MUX consists of four serial communication controllers. Each controller contains two independent full-duplex channels and provides the following features:

- A crystal oscillator
- A first-in/first-out (FIFO) buffer with quad receive/dual transmit capabilities

- Channel operation can be asynchronous, synchronous or monosynchronous

Refer to Sections 1.3.3 and 1.4.2.2 for more information concerning COMM MUX features and permissable combinations of synchronous and asynchronous channels.

4.4.2 Loader Storage Unit (LSU)

The primary function of the LSU is to automatically load into the computer's memory, upon initialization, a bootloader program stored on nonvolatile EPROM. The IPL bootloader program automatically loads the operating system from the disk or tape. For details of the automatic loading procedure, see Section 3.8.

The watchdog timer feature is included in the LSU which, when enabled by the program, has the capability of initializing the processor. Under normal operating conditions, the timer is reset by a software generated output command prior to the preset time-out delay. If the program fails, time-out occurs and the restart sequence is initiated. The watchdog timer may also be used to restart the user program upon restoration of the power after a power failure.

4.4.3 Precision Interval Clock/Line Frequency Clock (PIC/LFC)

The MPC clock timer is a versatile timer consisting of two independent clock devices, the PIC and the LFC. Both clocks provide timer controlled processor interrupts but have different timing mechanisms. The LFC is derived directly from the AC power line and has a fixed clock rate equal to twice the line frequency. The user has no control over the LFC other than to disable, enable or disarm interrupts. The PIC, although derived from an 8MHz crystal oscillator, is dynamically variable through program control.

4.4.4 Line Printer Interface

The MPC line printer interface is designed to operate any line printer with a Centronics-compatible I/O scheme. The line printer interface supports both upper- and lower- case characters. If the system is configured with multiple MPC boards, only the line printer interface on the lowest priority MPC board is activated.

For details on the MPC board, see the Multiperipheral Controller (Multilayer MPC) Installation, Theory of Operation and Programming Manual.

4.5 INTELLIGENT PERIPHERAL CONTROLLER (IPC)

The IPC board (35-918) is designed to provide a major portion of the data management required by the peripherals by minimizing processor intervention in I/O operations. The IPC interfaces with the PMUX bus at the maximum allowable speed, then releases the bus to other controllers when not transferring data. The IPC interfaces to the disks and tapes over the small computer system interface (SCSI) bus.

The IPC is divided into two sections. The first section, called the local IPC processor (LIP), is responsible for management of the two buses and overall I/O operation control. The second section, called the data transfer engine (DTE), consists of two DMA engines, buffer array control, PMUX bus interface and SCSI bus signal generation. The DTE is responsible for all data transfers between the two buses.

For details on the IPC board see the Intelligent Peripheral Controller (IPC) Installation, Theory of Operation and Programming Manual.

4.6 5.25" DISK DRIVE UNITS

There are three 5.25" disk drive units available for use in Model 3203 Systems as described in Section 1.3.5. The first two (27-160 and 27-161) are operated in conjunction with the 35-906 external controller described in Section 4.7. For information concerning the characteristics of the 27-160 and 27-161 disk drives, refer to Section 1.3.5.1.

The third disk drive unit (27-189) has an embedded SCSI controller and interfaces directly with the IPC. Refer to Section 1.3.5.2 for all pertinent characteristics of this device.

The following description of the electrical interface applies to the 27-160 and the 27-161 disk drives (51.4MB and 85MB units, respectively). Similar information for the 182MB disk drive unit (27-189) is covered in the vendor documentation for that device and in the 47-136 SCSI Installation, Operation and Programming Manual.

The electrical interface to the disk drive is divided into three categories: control signals, data signals and DC power. All of the control lines are digital in nature (open collector) transistor-transistor logic (TTL), and either input signals to the drive or output signals to the controller via interface connector J1/P1. The data transfer signals are differential in nature and provide data to either write to, or read from the drive via J2/P2. Figures 4-1 and 4-2 provide handshaking between the disk drive and the disk controller. Details of the 27-160 and 27-161 disk drive units are given in the vendor manual provided for those devices.

4.7 DISK CONTROLLER (35-906)

The 35-906 disk controller is a single board controller which provides standard SCSI and ST506 interfaces for the 27-160 and/or 27-161 Winchester-type disk drives. This controller is external to the 27-160 and 27-161 disk drives and is not used in conjunction with the 27-189 disk drive which has an embedded SCSI controller.

The IPC communicates with the disk controller via the SCSI interface while the 27-160 and 27-161 drive units require an ST506 interface. The disk controller serves as an adapter which converts the SCSI signals from the IPC to the ST506 signals recognized by the associated drive unit. This controller is capable of operating two disk drive units simultaneously and formats them to a 512B per sector format. For details of the 35-906 disk controller, see the SCSI Disk Controller Manual.

4.7.1 Small Computer System Interface (SCSI)

The SCSI interface provides the means of interfacing the disk controller to the IPC board via the SCSI bus.

4.7.2 Disk Drive Interface (ST506)

The ST506 interface consists of two connectors, data and control. The data connector establishes the serial data link between the controller and the disk drive. The control connector establishes the required signals for changing cylinders, selecting different heads and returning disk drive status signals.

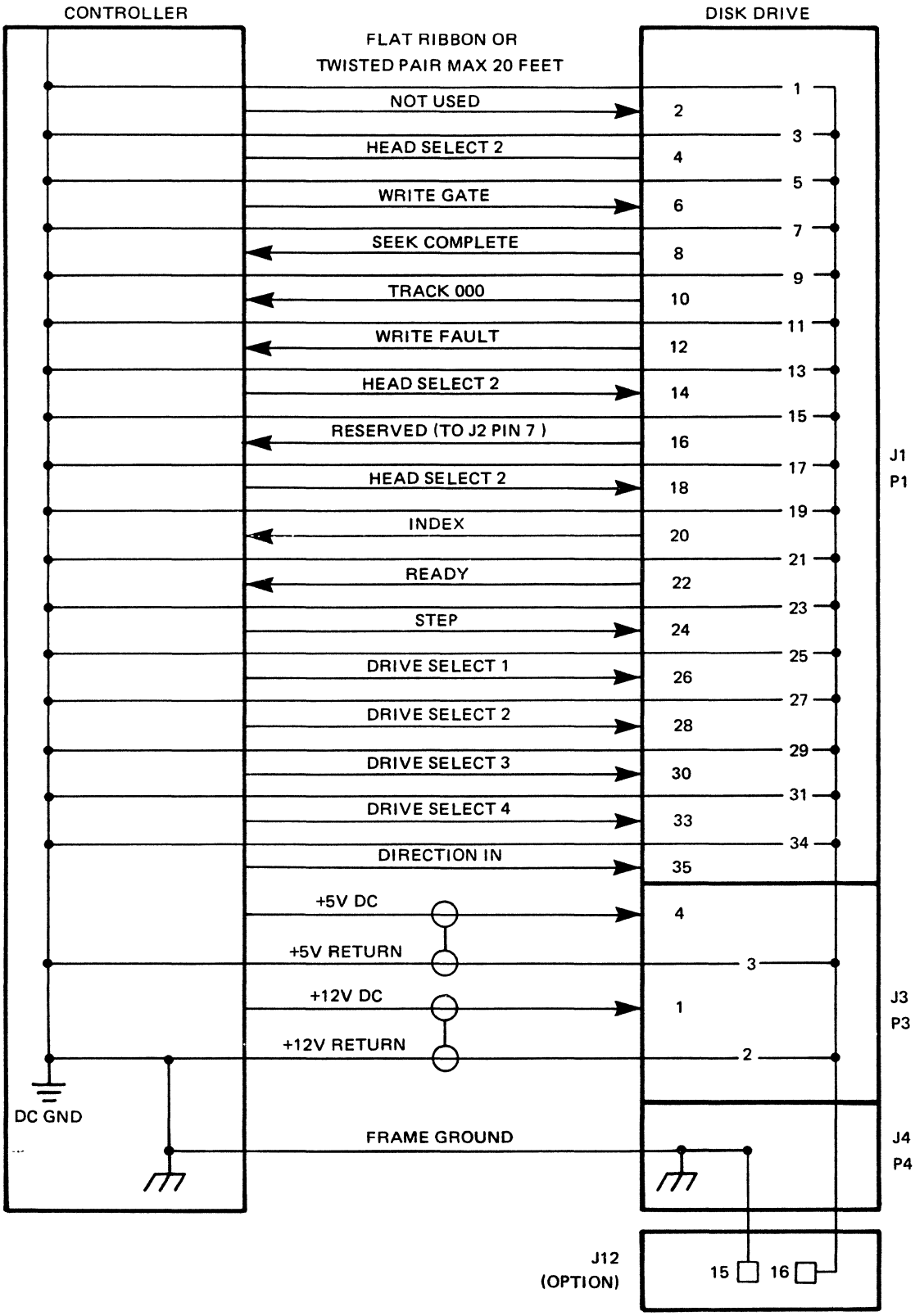


Figure 4-1 27-160 and 27-161 Disk Drive Control Signals

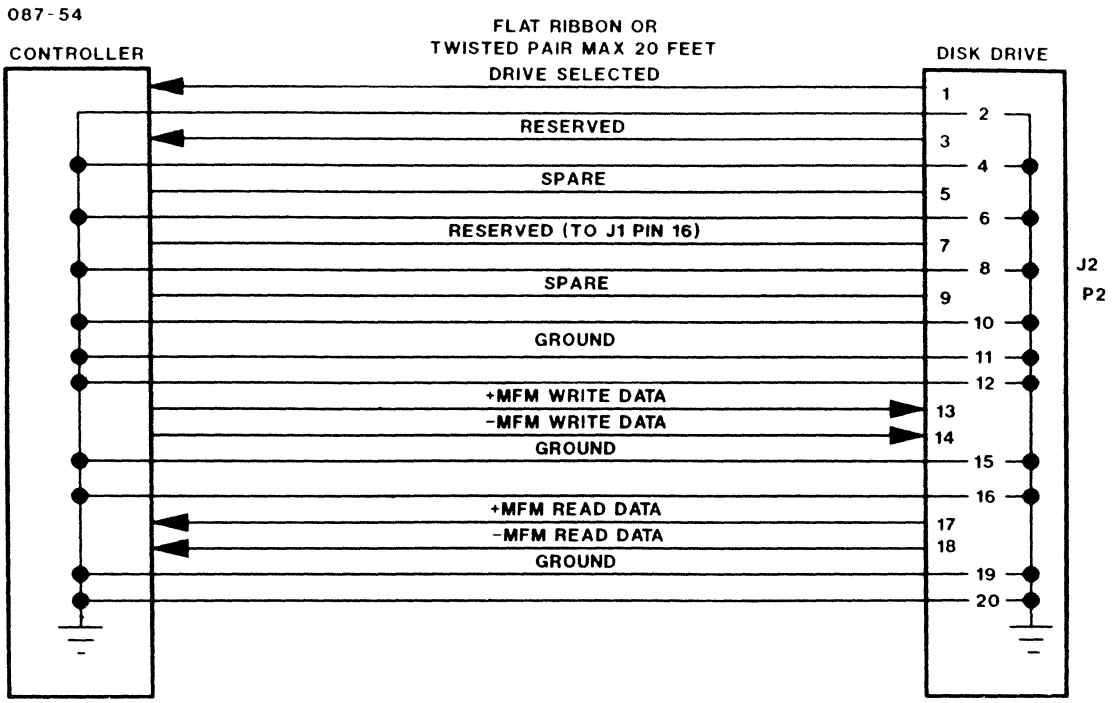


Figure 4-2 27-160 and 27-161 Disk Drive Data Signals

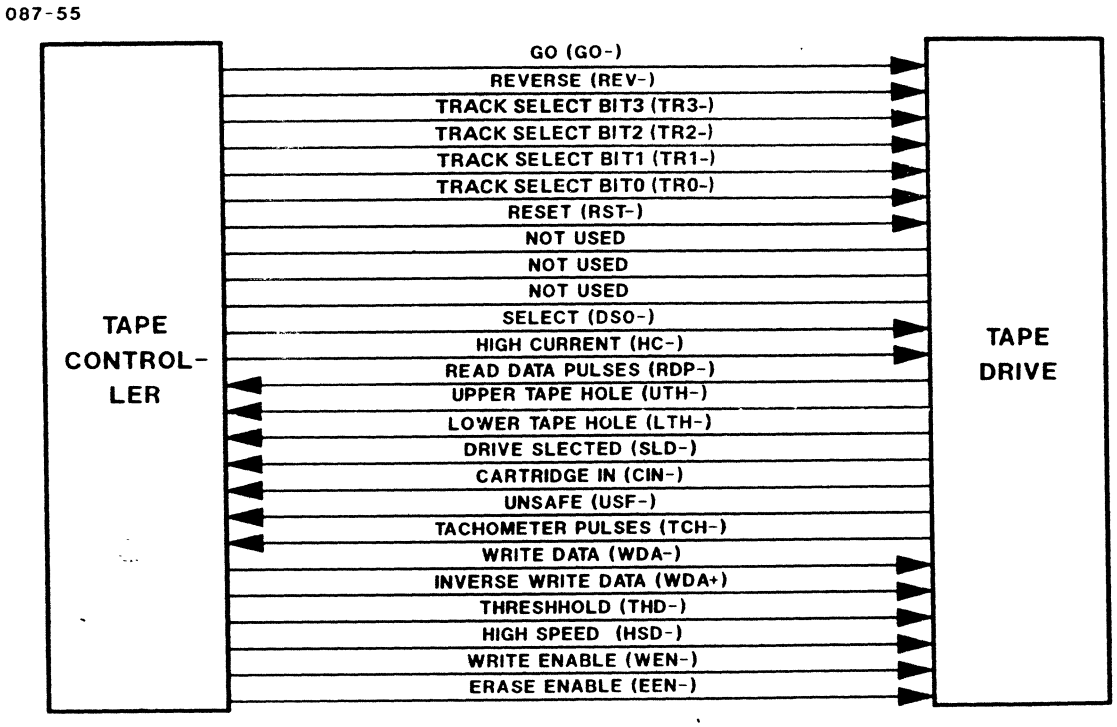


Figure 4-3 Tape Controller/Drive Handshaking Signals

4.8 0.25" TAPE DRIVE UNITS

There are two types of tape drives available for use in Model 3203 Systems as defined in Table 1-1 and Section 1.3.8. Functionally, both units are the same. The 27-159 tape drive is provided in type 01-277 Model 3203 Systems which use a SCSI/QIC36 tape drive controller to satisfy the interface requirements of the drive unit. The 27-192 tape drive is self-contained, having its own embedded device controller. Therefore, it is used in a type 01-339 system which is configured without the SCSI/QIC36 controller.

The 0.25" tape drive is a high-performance streaming tape drive which can store up to 60MB of formatted data on a 600' cartridge. The drive operates on +5VDC (P5) and +12VDC (P12).

The tape drive functions in a streaming mode with a data density of 8,000 bits per inch (bpi). Recording is done in a serial recording format which provides constant tape motion and very short interblock gaps with minimal format overhead. Handshaking signals between the 35-905 tape controller and the 27-159 tape drive are illustrated in Figure 4-3. Since the 27-192 SCSI tape drive controller is embedded, controller to drive handshaking for that unit is not defined herein.

Information on tape handling and care is provided in the Model 3203 System Owners Manual. Detailed information for the 27-159 tape drive can be found in the vendor 0.25" Streaming Tape Drive Manual. For details of the 27-192 tape drive, refer to the SCSI Tape Drive Installation and Operation Manual.

4.9 TAPE CONTROLLER (35-905 and 35-999)

The streaming tape controller (either 35-905 or 35-999) provides standard SCSI and QIC36 interfaces for the 27-159 tape drive unit and is not used in conjunction with the 27-192 tape drive which has an embedded SCSI controller. See Section 1.3.8 for further unit identification.

The IPC communicates with the tape controller via the SCSI interface while the streaming tape drive (27-159) requires a QIC36 interface to communicate with the tape controller. This controller serves as an adapter between the IPC SCSI interface and the tape drive QIC36 interface.

All information on the tape is accessed in sequential blocks. The 0.25" tape drive uses a QIC24 media format which has a block size of 512B. The read and write format (QIC24) is selected at the beginning of the tape and must be adhered to for the entire tape.

For more information concerning the tape controller, refer to the appropriate SCSI Tape Controller Manual.

4.10 POWER SUPPLY

The Model 3203 System power supply, shown in Figure 4-4, consists of one 35-903 printed circuit board which provides +5V at 80A and +12V (P12) at 10.5A. The power supply board is contained in a metal enclosure and connects into CONN0, slot five of the backpanel.

Table 4-1 provides the general specifications for the Model 3203 System power supply board.

087-56-2

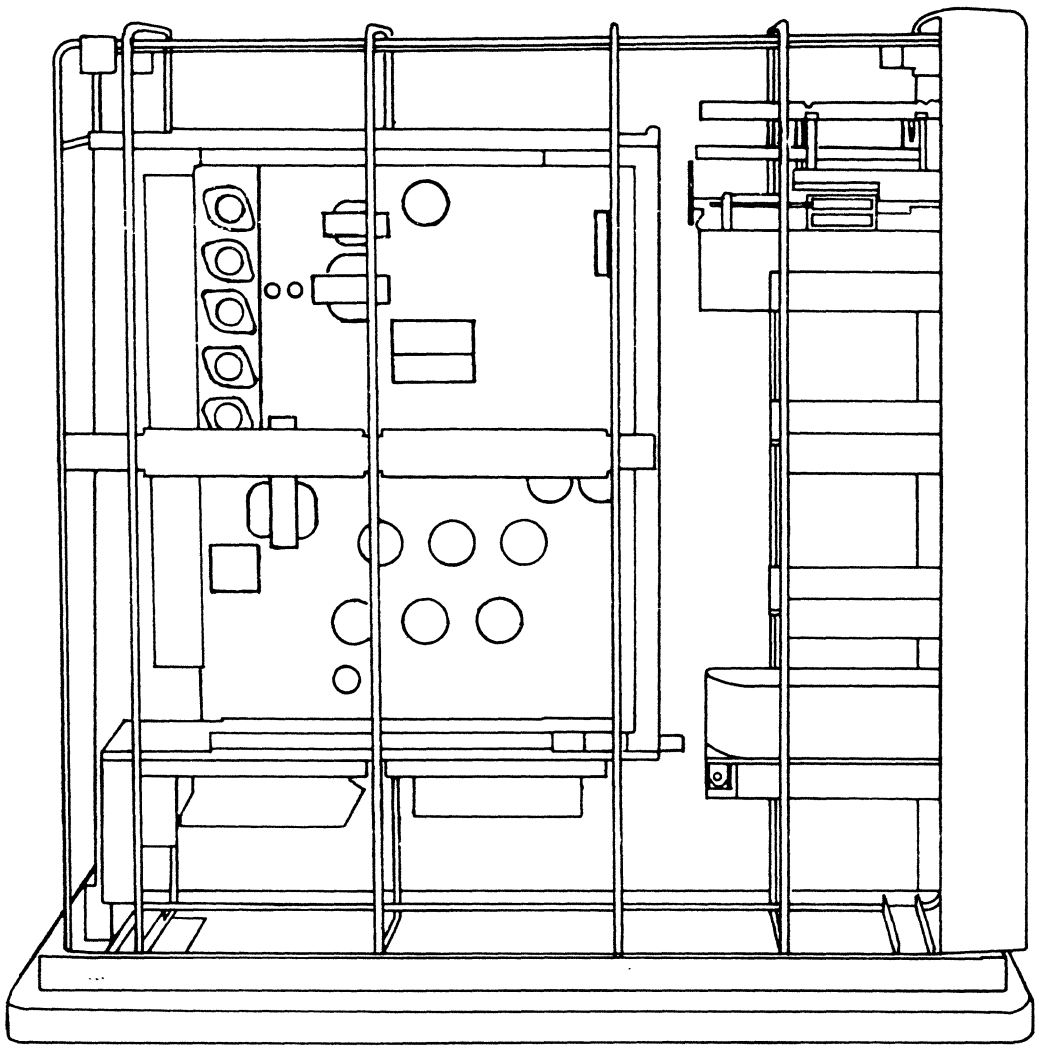


Figure 4-4 Model 3203 System Power Supply Board

TABLE 4-1 MODEL 3203 SYSTEM POWER SUPPLY SPECIFICATIONS

INPUT	AC Line Voltage: 90-132VAC or 180-264VAC (RMS) AC Line Frequency: 47-63Hz							
OUTPUT	Margin Switch Position	Output Current Rating 0-50 C Ambient Min	Output Current Rating 0-50 C Ambient Max	Output Current Rating 0-30 C Ambient Min	Output Current Rating 0-30 C Ambient Max	Output Voltage Min	Output Voltage Max	
P5	Normal	8 A	80 A	-	-	5.01	5.09	
	High	8 A	80 A	0	90 A	5.19	5.25	
	Low	8 A	80 A	0	90 A	4.79	4.85	
P12	Normal	0	12 A	0	12 A	11.50	12.50	
OVERCURRENT PROTECTION	Mnemonic	Converter shut-down point						
	P5	105 amps min/120 amps max						
	P12	15.5 amps min/19.5 amps max						
OVER VOLTAGE LIMITING (at sense points)	Mnemonic	Maximum output voltage						
	P5	6.0 V +/- 0.2 V						
	P12	14 V +/- 0.2 V						
OUTPUT SIGNALS TO THE BACK-PANEL	Mnemonic	Description						
	PFDT0	Output power fail detect Logic levels: 1...Open circuit with pull-up to P5 through a resistor on the processor board 0...1 VDC maximum						
	2XLF1	Twice LFC signal output Logic levels: 1...Approximately 1 millisecond (ms) wide 5VDC pulse every 8.3 ms. 0...1 VDC maximum Maximum loading: No more than two MPCs controllers MPCs connected to the backpanel.						
INPUT SIGNALS FROM THE BACKPANEL	Mnemonic	Description						
	KSON0	Keyswitch on Logic levels: 1...Open circuit when ON/OFF switch on control panel is in the OFF position. 0...Ground when ON/OFF switch on the control panel is in the ON position.						

NOTE

P12 drives the DC fans. In case of P12 failure, the control logic shuts off the P5 to prevent circuit damage.

4.10.1 Line Filter

For the domestic version, a 15A, 120V plug and power cord supply power to the line filter. For international use, a 6A, 250V plug and power cord supply power to the line filter. The line filter is connected in series with the AC line to reduce any conducted line interference. The filtered 120VAC or 230VAC is supplied to input fuses as described in the following section.

4.10.2 Input Fuses

For domestic use, a 15A fuse F1 (1A1) is provided for overcurrent protection. In the international version, two 15A fuses, F1 and F3 (1A1) are provided for overcurrent protection.

4.10.3 Input Rectifiers

D101 (1B1) is a full-wave bridge rectifier in the 230V configuration (or a full-wave voltage doubler in the 120V configuration) which converts the AC input voltage to corresponding DC voltage levels. The output of the rectifier is fused by F2, an 10A fuse. This DC voltage is the high voltage DC bus whose amplitude depends upon the value of the AC input voltage and the power supply loading. The high voltage DC bus varies from 227VDC at low line, full load to 365VDC at high line, no load. The power supply is normally started by an input from the control panel. When the keyswitch-on (KSON0) signal arrives at the power supply, it initiates the turn-on of the P12 pulse-width modulator.

4.10.4 Inrush Current Limiters

The inrush current through the AC input lines at AC power turn-on is limited by resistors R1 (1C1) and R2 (1C2). The inrush current is due to the charging of input filter capacitors across the high voltage DC bus.

4.10.5 Input Filter Capacitor

The input filter capacitor is designed to minimize the peak-to-peak ripple voltage and consists of C15 (1C1) and C16 (1C2).

Resistors R118 (1D1) and R119 (1D2) discharge these capacitors within three minutes after the input power cord is removed.

4.10.6 47/63Hz Transformer

The 47/63Hz step down transformer T1 (1B3) provides the bias power for the logic circuits and pulse-width modulators (PWMs). The output of T1 is rectified by bridge rectifier D4 (1B3). The output of D4 is input to a three terminal regulator Q1 (1C3) which provides 15V bias used throughout the board. The 15V is also used by Q2 (1C2), a 3-terminal precision reference which produces 10V for use as a reference voltage to the PWMs. This 10V is divided by resistor networks A35 (2B3) for P5 PWM A21 and A36 (2B6) for PWM A20. Use of a precision reference and a precision voltage divider network allow setting of the output voltage without the need for a potentiometer. These resistor networks provide 3.33V to the noninverting input of A21 (pin 2) for the P5 output, and into the noninverting input of A20 (pin 2) for the P12 output. This reference voltage is compared to the output of P5 or P12 coming back to the inverting input of the respective PWM.

4.10.7 Pulse-Width Modulators (PWMs)

The power supply board consists of two half-bridge PWMs (A20 and A21) producing a P5 and P12 output. The PWM for the P5 output is A21 (2C1). The half-bridge circuit consists of transistors Q3 and Q4 (2H1 and 2H2) with capacitors C38 and C37 (2J1 and 2J2). The P12 PWM is A20 (2C5); the half-bridge circuit consists of transistors Q5 and Q6 (2H4 and 2H5) with capacitors C39 and C40 (2J4 and 2J5).

The frequency of the P5 PWM A21 is set by resistor R72 (2B1) and capacitor C63 (2B2). The oscillator output from A21 pin 4 synchronizes the A20 regulator whose frequency determining components are R70 and C27 (1B5). R70 and C27 are set with a time constant which is about 15% longer than the frequency determining components of A21. The PWM operates at approximately 23KHz.

4.10.8 High Voltage Logic

There is a section of high voltage logic that is operated directly from the high voltage DC bus. R27 and R28 (1D2) are dropping resistors which in conjunction with zener diode D1 (1D3) provide 15V for the high voltage logic. The 15 volts provided by D1 also power A13 (1E3), which is a 1.235V reference. This reference is input to pins 9, 6 and 4, three sections of quad-comparator A11 (1E2). The other input to the three sections of A11 on pins 8, 7 and 5 consists of the high voltage bus itself divided down by resistors R14 through R20 (1E2 and 1E3).

The three input voltages from the bus are sensed by comparator A11, latched by two RS flip-flops (1G2 and 1G3) and coupled out of the high voltage section by two opto-couplers (1H2 and 1H3).

When power is initially applied, the first voltage of interest is the 229 VDC level on the high voltage bus which initiates the enable signal (1H3). If the level of the high voltage bus is 229V or higher, the enable signal is high. The enable signal drives A7 whose LED (1H3) is in the high voltage logic section and whose opto-transistor (1G5) is in the low voltage logic section.

In the event of a power failure, as the voltage on the high voltage bus decays below 165V, the enable signal is terminated and the power supply is shut down.

In addition to the enable signal, another signal is generated within the high voltage logic section. This is the power fail detect signal (PFDT) (1H2). The power fail detect signal is high whenever the high voltage bus drops below 200V. On initial power-up, the PFDT signal is held off until after the high voltage DC bus has risen above the 229V level, which is also used by the enable signal. The PFDT signal is coupled out of the high voltage logic section by opto-coupler A6, whose LED (1H2) is in the high voltage section and whose opto-transistor (1H5) is in the low voltage section.

4.10.9 Low Voltage Logic

In the low voltage logic section comparator A1 monitors the bias supply. When the bias supply is above approximately 10V, the BUP1 signal is high and input to A5 pin 12 (1D6) where it is ANDed with the enable signal input at A5 pin 13. The output of A5 pin 11 (1D6) is inverted and goes to A5 pin 9 (1E6) where it is ANDed with the keyswitch on (KSON1) signal input to A5 pin 8. The output on A5 pin 10 provides a turn-on signal A20ON0 (1F6) for the P12 modulator A20. The A20ON0 signal is input to A15 pin 11 (2F6) and ORed with the overvoltage protection (OVP) and overcurrent protection (OCP) signals input to A15 pins 12 and 13, respectively. The output of A15 pin 10 is inverted by A9 (2B5) which also reduces it to a 5V level required by the PWM. If this input is high, the PWM is shut down. If this signal is low at the shut-down pin when the keyswitch is turned on, the P12 pulse-width modulator A20 starts. The start-up of A20 is controlled by the soft-start capacitor C26 (2C5). When the P12 output reaches approximately 10.7V another section of A1 which monitors P12 provides a P12UP signal (1E7).

The P12UP1 signal at A5 pin 5 (1E7) is ANDed together with the A20ON1 signal input to A5 pin 6 and produces A21ON0 (1F7). A21ON0 is input to pin 8 of 3-input OR gate A15 (2F3) and provides the 5V signal (5FL0) required for shut-down pin 10 of the P5 PWM A21. The start-up of A21 is controlled by soft-start capacitor C62 (2C2).

The P5 PWM is started only after the P12 output has reached 10V or more, since the P12 drives the two DC fans. If the P12 fails the P12UP1 signal goes low and the P5 PWM is shut down.

4.10.10 Overcurrent and Overvoltage Protection

Both PWMs have overvoltage and overcurrent protection circuits which are identical. The P5 overcurrent protection circuit receives its input from current transformer T5 (2F2) which monitors the primary current of T2 (2G2) and provides 1V out for each amp in the T2 primary.

This voltage is divided by R126 (2C3) and R33 (2B3) and is applied to one section of quad comparator A16 (2C3). The quad comparator receives 3.3V reference (at pin 5) from the divider that provides voltage to A20 pin 2. This limits the output of P5 to approximately 100A. The output of the overcurrent protection comparator A16 pin 2 (2C3) is applied to RS flip-flop 2D3 which latches the data and shuts down P5 PWM via the shut-down pin.

To restart the supply, the RS flip-flop must be reset. Reset can occur in one of two ways. The most common method is with the ON/OFF switch on the control panel. When the ON/OFF switch is off, the RS flip-flops for overvoltage and overcurrent protection are held reset. The other method of resetting these flip-flops is via the bias up. In case of a power line fault such as a brownout or blackout, the power supply may shut down with an overvoltage or overcurrent condition. When the bias supply is low, these flip-flops are held reset. When the power line fault clears and the voltages come back up, the PWM starts up again.

One section of NAND gate A5 (1C7) is used as a negative input OR gate to OR the BUP1 and KSON1 signals together. The output of A5 pin 3 (1D7) is inverted by A4 and becomes the RESET for the four RS flip-flops.

Overvoltage protection is provided by another section of quad comparator A16 (2E3). The voltage produced by P5 is sensed through R115 and R125 (1E3 and 1D3). A16 shuts down the P5 modulator if the voltage exceeds 6V.

4.10.11 Output Signals

There are two output logic signals from the power supply board to the backpanel, power fail detect (PFDT) and twice line frequency clock (2XLF).

The PFDT logic signal monitors the high voltage DC bus and provides a PFDT when the bus is decaying. R3 and C3 delay PFDT by 800 to 1000ms when power is reapplied after a brownout or blackout. This allows time for the P12 and P5 voltages to reach normal levels. A9 (1G7) is a logic level shifter which provides 5V to the output IC A10 (1H7), which is a low power Schottky TTL open collector device.

The 2XLF logic signal is initiated by the bias transformer T1 (1B3). When the secondary goes through zero, a trigger is generated from one section of quad comparator A1 (1C5). This trigger drives a 555 timer A8 (1E4), which produces a 1ms pulse. The level of the 1ms pulse is shifted by logic level shifter A9 (1G7) and leaves the board via A10 (1H7), the open collector device with a 2 kilohm pull-up resistor on pin 6.

4.10.12 Power Supply Mnemonics

This section provides a list of the 35-903 power supply board mnemonics, a brief definition of each mnemonic and the source location of the mnemonic on Functional Schematic 35-903 E08.

MNEMONIC	DEFINITION	LOCATION
A20ON0	Turn on signal for A20 PWM	1F6
A21ON0	Turn on signal for A21 PWM	1F7
BUP1	Bias Up	1G5
EN	Enable (Sufficient high voltage)	1H3
H.V. HIGH	High voltage + rail	1H1
H.V. LOW	High voltage - rail	1H1
KSON0	Keyswitch on	1A7
PF	Power fail (AC input below normal)	1H2
PFDT0	Power fail detect (PFDT)	1J7
P5SGND	P5 sense ground	2K3
P5SNSE	P5 sense	2K3
P12SNSE	P12 sense	2H6
P12UP	P12 level greater than 10V	1E7
RESET	Clear signal for OVP and OCP latches	1A8
SGND	Signal ground	2K3
2XLF1	Twice Line Frequency	1J7
5FL0	5V fault	2G3
12FL0	12V fault	2F7

4.11 OPTIONS

The following sections provide a brief description of the options available for the Model 3203 System. Details on these options are provided in their respective manuals.

4.11.1 Model 6100 Video Display Unit (VDU)

The Model 6100 VDU, which can be used as a system console or user terminal, consists of a green or amber phosphorous monitor and an adjustable low profile keyboard. The alphanumeric screen format of the monitor is 24 lines by 80 characters each, with a 25th line for status display. The keyboard comes equipped with a detachable 6' coiled cable for operator flexibility and mobility. The Model 6100 VDU provides a printer port, four programmable function keys shiftable to eight, a numeric keypad and a full 128 ASCII character set.

For details on the Model 6100 VDU, see the Model 6100 Video Display Unit (VDU) Installation and Programming Manual.

4.11.2 Model 6312 Video Display Unit (VDU)

The Model 6312 VDU is a complete stand-alone terminal which may also be used as a system console or user terminal. The Model 6312 VDU consists of a green or amber phosphorous monitor and an adjustable low-profile keyboard. The Model 6312 monitor provides two independent, 24 line X 80 character displays and provides a 25th status line. The keyboard provides a numeric keypad, 16 programmable function keys (shiftable to 32) and six edit keys (shiftable to 12). The keyboard comes equipped with a detachable 6' coiled cable for operator flexibility.

For details on the Model 6312 VDU, see the Model 6312 Video Display Unit (VDU) User Guide.

4.11.3 Ethernet Data Link Controller (EDLC)

The Ethernet controller consists primarily of two boards, the Ethernet PMUX bus interface (35-861) and the Ethernet protocol module (EPM) (35-863). The EPM implements the data link layer of the Ethernet specification. The Ethernet PMUX bus interface provides a private SELCH MUX bus interface that controls the operation of the EPM from the I/O bus SELCH.

For details on the Ethernet Data Link Controller, see the Series 3200 Ethernet Controller Installation and Theory of Operation Manual.

4.11.4 Universal Logic Interface (ULI) Board

The ULI (35-860) is configured on one 37.5cm (15") board that is divided into two halfboard sections. Each section provides two ways to interface user device controllers to the ULI. One section contains general-purpose interface logic components that operate under request/response I/O control for data transfer in the byte or halfword (two bytes) mode. This enables users having device controllers compatible with the ULI I/O request/response signals to interface directly to the system. This section also contains a small wire-wrap field that allows the user to construct a device controller and connect it between an on-board connector, containing the ULI I/O request/response signals and an off-board connector on the component side or the wire-wrap side, as required. The remaining section contains a halfboard wire-wrap field for the construction of device controllers that are too large to be constructed in the wire-wrap field located on the component side. The device controllers built on this section are also connected between the on-board connector and an off-board connector on the component side or the wire-wrap side, as required. The on-board connector can be directly strapped to the off-board connector on the wire-wrap side to make the 35-860 ULI board compatible with an M48-013 ULI board. All sections are connected in parallel to form the data link between the user's peripheral equipment and a Concurrent Computer Corporation System.

For details on the ULI board, see the Universal Logic Interface (ULI) Installation, Theory of Operation and Programming Manual.

4.11.5 Additional Multiperipheral Controller (MPC) Board

The Model 3203 System has the capability of supporting two MPC boards. The second MPC board (35-910 F02) provides eight additional FDX data communication channels to interface user devices or terminals. The second board also provides a line printer port. When the second MPC board is configured in the system, the line printer port must be deactivated on the highest priority MPC board in the system. See Section 3.5 for MPC board strapping information.

4.11.6 Additional 5.25" Disk Drive

The Model 3203 System can support up to two 5.25" disk drives. This second disk drive is identical to the first disk drive in the system and provides an additional storage capacity of 51.4MB, 85MB or 182MB of unformatted data depending, upon the exact expansion disk installed.

CHAPTER 5
TROUBLESHOOTING PROCEDURE

5.1 INTRODUCTION

This chapter provides a list of the diagnostics available and a troubleshooting guide for the Model 3203 System.

5.2 DIAGNOSTIC SUPPORT

The following diagnostics are provided for the Model 3203 System. For details on these diagnostics, see the appropriate test description.

06-145 F01	Diagnostic Executive
06-228	Concurrent Computer Corporation Series 3200 System Processor Test Part 1
06-229	Concurrent Computer Corporation Series 3200 System Processor Test Part 2
06-231	Concurrent Computer Corporation Series 3200 Floating Point Test
06-238	Commercial Instruction Set Test
06-280 F01	Memory Address Translator (MAT) Test
06-280 F02	Memory Address Translator (MAT) Test
06-289 F01	Model 3205 System Memory Test
06-289 F02	Model 3205 System Memory Test
06-291	Multiperipheral Controller (MPC) Test
06-295	Model 6312 Video Display Unit (VDU) Test
06-297	Intelligent Peripheral Controller (IPC) Test

5.3 TROUBLESHOOTING SEQUENCE

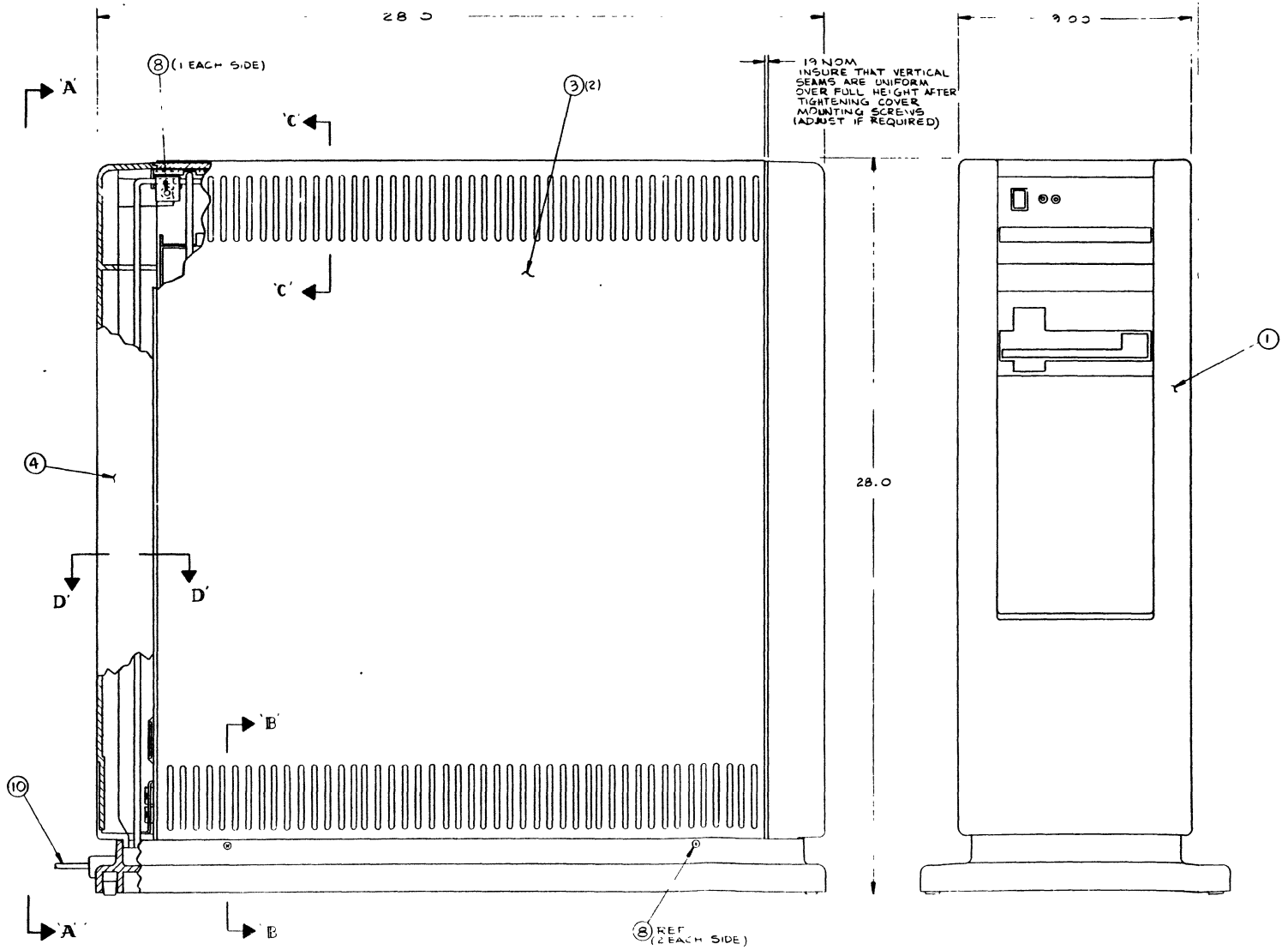
Table 5-1 contains a troubleshooting guide for the operation of the Model 3203 System.

TABLE 5-1 TROUBLESHOOTING GUIDE

APPARENT PROBLEM	PROBABLE CAUSE	SOLUTION
When the ON/OFF switch is placed to the ON position, the POWER indicator does not light. (This is true for both the system and video display units (VDUs)).	No power to the system or VDU.	1. Check the connection of the power cord to both the wall receptacle and the plug on the rear of the cabinet or VDU. 2. Check the circuit breaker or fuse for the wall receptacle to ensure it is on. 3. Check the power supply fuses (F1, F2 and F3). See Figure 3-5 for description and location of fuses.
No response from the VDU.	The cable connected to the primary modem port is not properly connected.	Disconnect the cable connected to the primary modem port, remove any dust or lint and reconnect the cable.
	The cable between the monitor and keyboard is not properly connected.	Disconnect and then reconnect this cable to ensure a proper connection.
	Either the cable connecting the VDU and the system or the keyboard and the monitor is faulty.	Replace the cable between the monitor and keyboard. If there is no response, replace the cable between the VDU and the system.
	The VDU is not online.	Check the configuration of the VDU.

TABLE 5-1 TROUBLESHOOTING GUIDE (Continued)

APPARENT PROBLEM	PROBABLE CAUSE	SOLUTION
FAULT light lit.	Fault during diagnostic testing when the system is first turned on.	The system can be shut down and turned on again to restart the diagnostics.
	During the automatic load, the operating system is not found.	Remove and reinsert the tape cartridge and restart the software load procedure.
	During system operation one of various faults occurs.	Try for a response from the system by inputting via the terminal.



REVISIONS

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	PROD	

AREA NS MANUAL WAS 47 082 IN ERROR. AREA H9 ADDED REV LEVEL BLOCK

MF		5921	D	4-18-85	R01 X

REVISED FUNCTIONAL VARIATION TABLE IN AREA K3-M9 REVISED SHTS 1&2

DB		6021	R	7-15-85	R02 X

REVISED SHT 2

MF		6370	R	3-21-86	R03 X

USED IN MANUAL 47-087

UNLESS OTHERWISE SPECIFIED

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DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

NAME	TITLE	DATE
MANFIELD	DES/DFT	10-19-84
R CERO	SUPV	
	CHK	
D FOGGIA	ENG	
P.ABITANTE	MGR	
R.A. BARKER	QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE PACKAGED SYSTEM
CORSAIR II
MODEL 3203

TASK 03354 SHT 1 - 2

DWG 01-277 R03. D03

NOTES

SHT NO	1	2
REV LEVEL	03	02

PART NO	DESCRIPTION
01-277 F01,03,05,07,09,11,13,15	INT 230V AS SHOWN LESS DET A
01-277 F00,02,04,06,08,10,12,14	DOMESTIC 120V AS SHOWN LESS DET B

FUNCTIONAL VARIATION

REVISIONS					
(AREA No.-N7) COMPLETE REVISIONS TO DETAIL "A" & DETAIL "B"					
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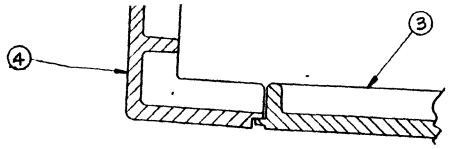
MF	DM	6370	R	3 21 86	R02



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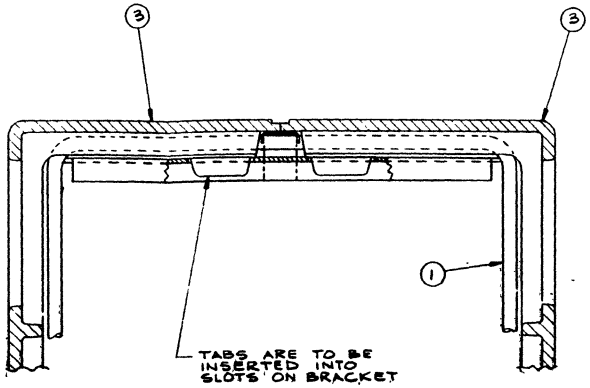
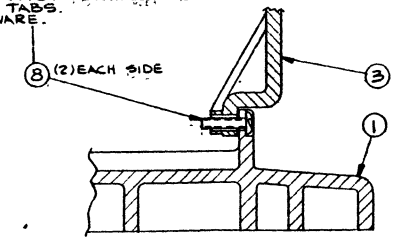


SECTION 'C'-'C'
SCALE 1/1

HARDWARE MAY BE INSTALLED PRIOR TO MOUNTING SIDE PANELS. HOOK PANELS ONTO BASE (2) PLACES AT BOTTOM AND PIVOT FORWARD TO SEAT ON UPPER TABS. TIGHTEN HARDWARE.



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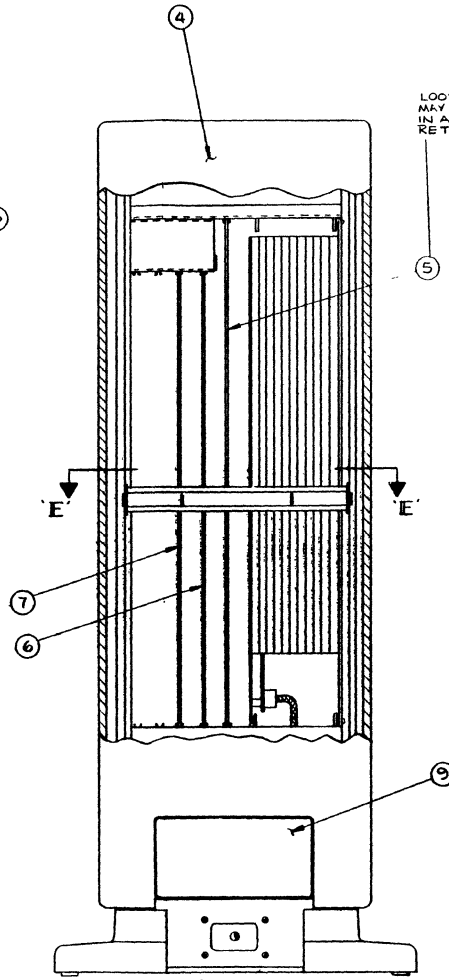
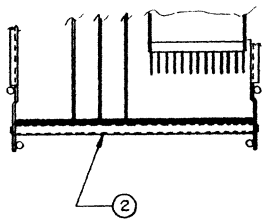
SCALE 1/1



VIEW 'A'-'A'
REAR VIEW

LOOSENING OF BACK PANEL MOUNTING SCREWS MAY BE NECESSARY TO ESTABLISH INITIAL 'PLUG-IN ALIGNMENT OF CPU BOARD. RETIGHTEN SCREWS AND INSTALL REMAINING BOARDS



SECTION 'E'-'E'

DETAIL 'B'
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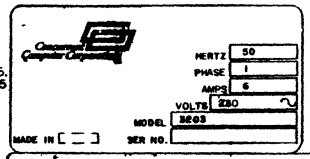
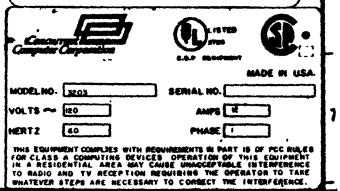


DETAIL 'A'
DOMESTIC
LABEL USE WITH
01-277 F00, F02 F04, F06, F08, F10 F12 & F14



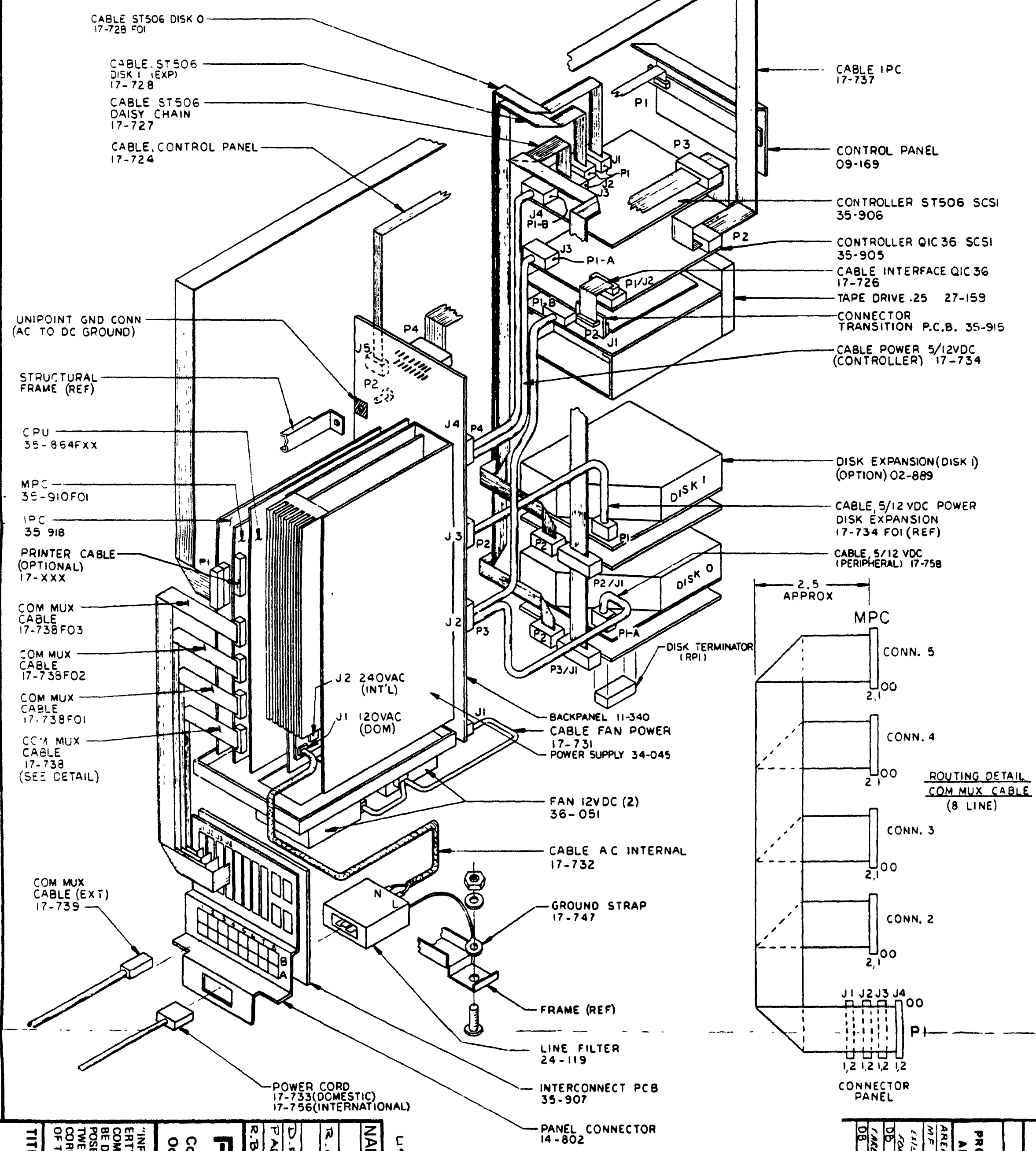
NOTES

DRAFTER	MANFIELD
DATE	10-19-84

TITLE
PACKAGED SYSTEM
CORSAIR II
MODEL 3203

TASK 03354	SHT 2 - 2
DWG 01-277 R02	D03

NOTES



USED IN MANUAL 47-087

NAME	TITLE	DATE
MANFIELD	DES/DFT	10-14-84
R. CERO	SUPV	
D. FOGGIA	CHK	
FABITANTE	ENG	
R. BARKER	MGR	
	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CABLING DIAGRAM
CORSAIR II
MODEL 3203

TASK 03354
DWG 01-277 R03 D12 SHT 1-1

REVISIONS

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PRE PRODUCTION APPROVAL	DEV / PROD		
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AREA H9 THE IPC WAS "35-895" / DB 6057	M	7-24-85	R03

FUNC.VAR.	DESCRIPTION
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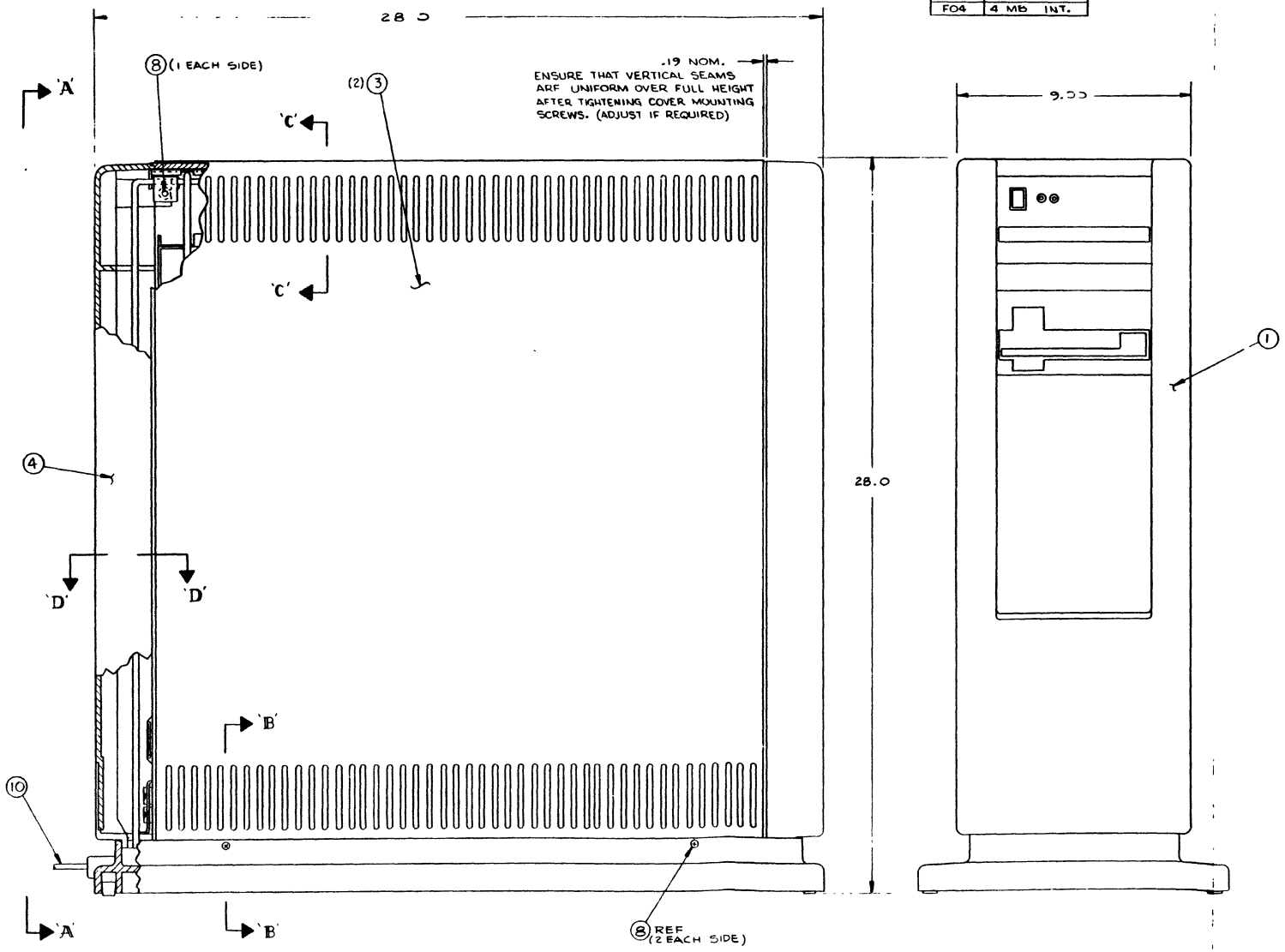
F02	2 MB INT.
F03	4 MB DOM.
F04	4 MB INT.



REVISIONS		
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PRE PRODUCTION APPROVAL	DEV	
	PROD	

USED IN MANUAL 58-031

UNLESS OTHERWISE SPECIFIED		
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DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
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V. GORDI MANFIELD	DES/DFT	12/22/86
R. CERO	SUPV	
	CHK	
D. FOGGIA	ENG	
PABITANTE	MGR	
R A. BARKER	QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE: PACKAGED SYSTEM MODEL 3203

TASK 03039/03214 | SHT 1-2

DWG 01-339 003

NOTES
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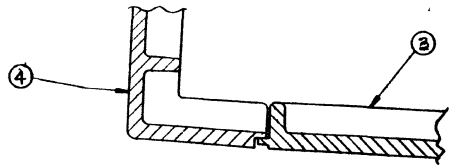
REV LEVEL			



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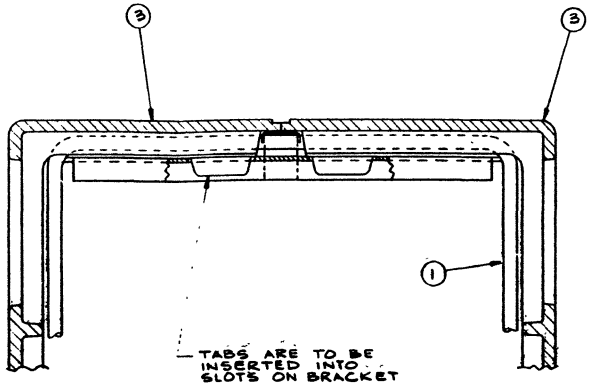
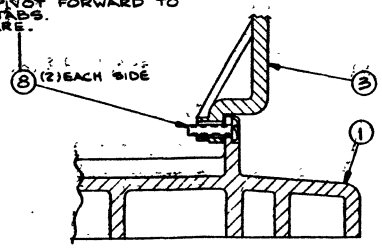


TABS ARE TO BE INSERTED INTO SLOTS ON BRACKET

SECTION 'C'-'C'
SCALE 1/1

HARDWARE MAY BE INSTALLED PRIOR TO MOUNTING SIDE PANELS. HOOK PANELS ONTO BASE (2) PLACES AT BOTTOM AND PIVOT FORWARD TO SEAT ON UPPER TABS. TIGHTEN HARDWARE.



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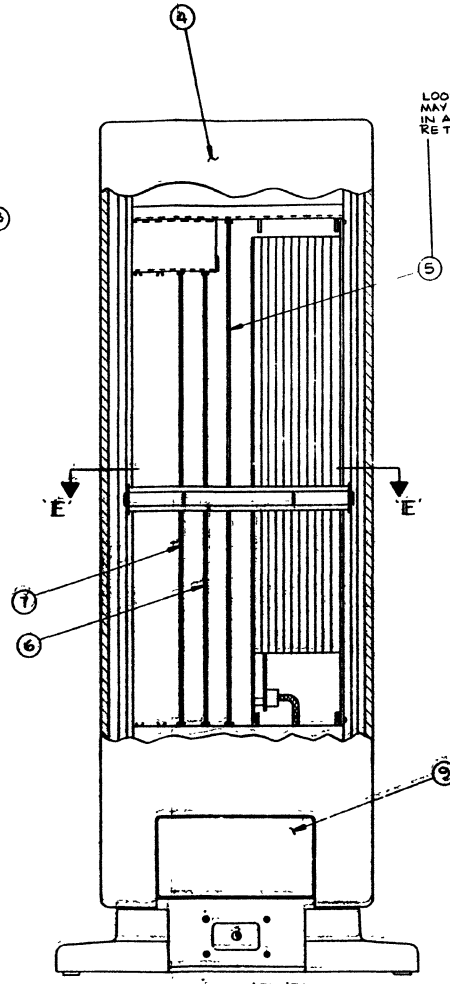
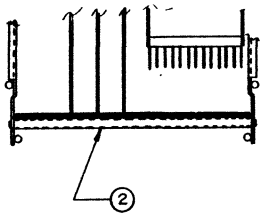
SCALE 1/1



APPLY ADHESIVE-BACKED LABEL EVENLY IN RECESSED AREA OF REAR COVER SEE DETAIL A/B FOR APPROPRIATE INFORMATION

VIEW 'A'-'A'
REAR VIEW

LOOSENING OF BACK PANEL MOUNTING SCREWS MAY BE NECESSARY TO ESTABLISH INITIAL PLUG-IN ALIGNMENT OF CPU BOARD. RETIGHTEN SCREWS AND INSTALL REMAINING BOARDS.



SECTION 'E'-'E'

DETAIL 'B'
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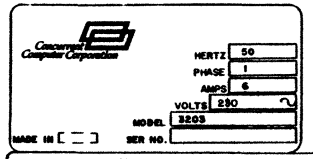
LABEL USE WITH
01-339 F01 & F03



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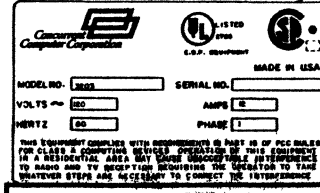
LABEL USE WITH
01-339 F02 & F04



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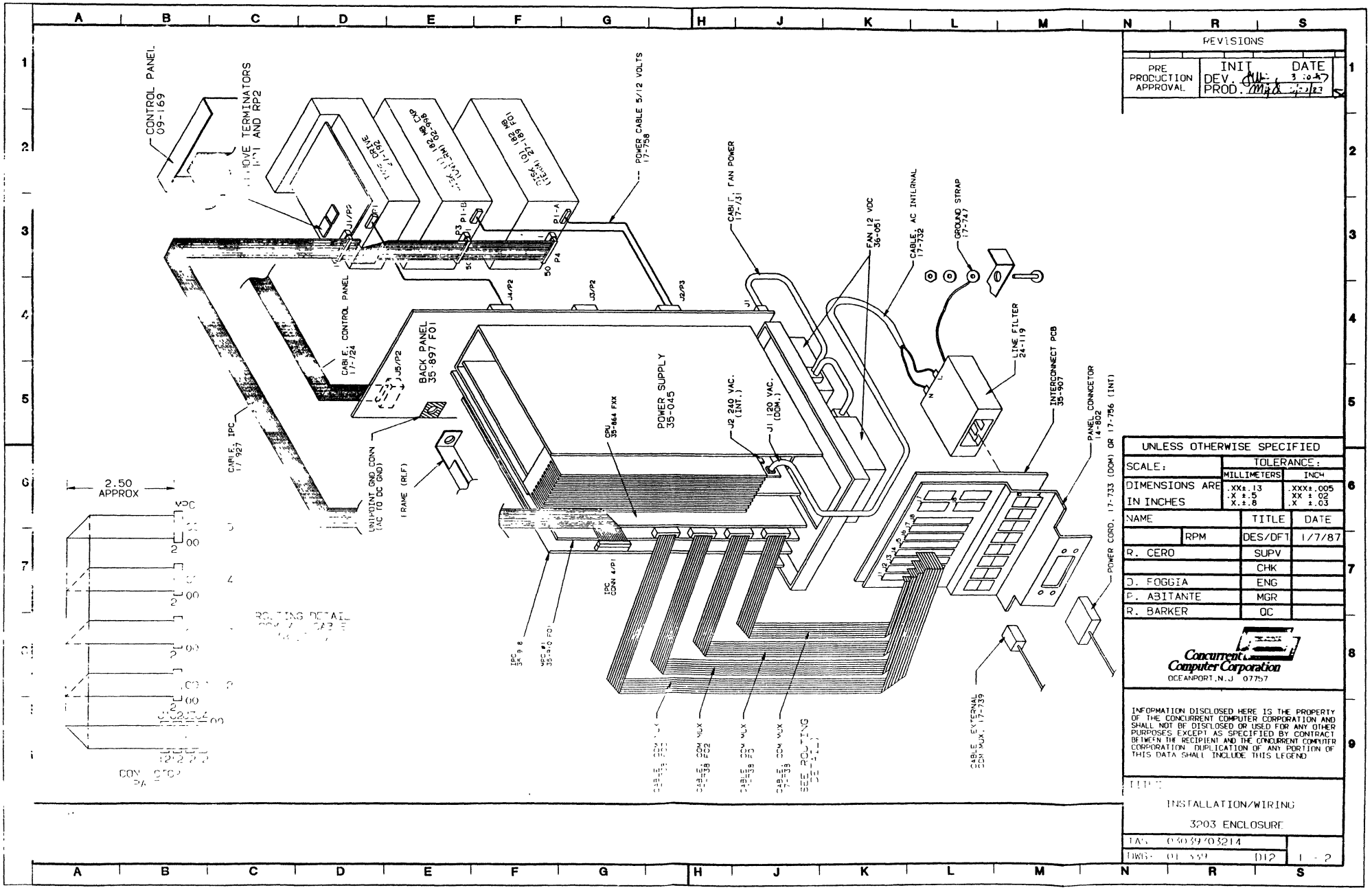
REVISIONS

NOTES

DRAFTEN	VILLARD / MAYFIELD
DATE	12/22/86
TITLE	PACKAGED SYSTEM MODEL 3203
TASK	03039 / 03214
DWG	01-339 D03
SHT	2 - 2



REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV.	3-10-87
	PROD.	3-10-87

UNLESS OTHERWISE SPECIFIED		
SCALE:	TOLERANCE:	
	MILLIMETERS	INCH
DIMENSIONS ARE IN INCHES	.XX±.13 .X ±.5 X.±.8	.XXX±.005 XX ± .02 .X ±.03

NAME		TITLE	DATE
	RPM	DES/DFT	1/7/87
R. CERO		SUPV	
J. FOGGIA		ENG	
P. ABITANTE		MGR	
R. BARKER		QC	

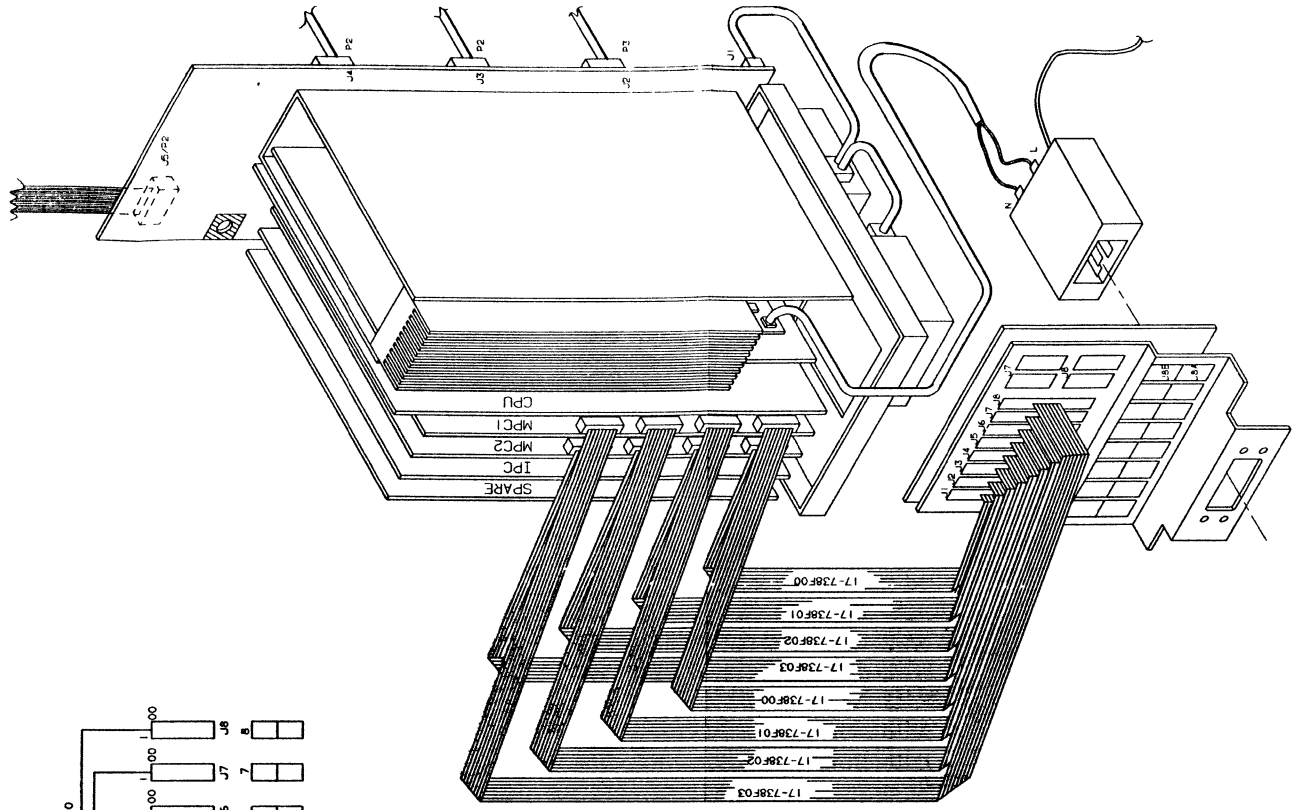
Concurrent Computer Corporation
OCEANPORT, N.J. 07757

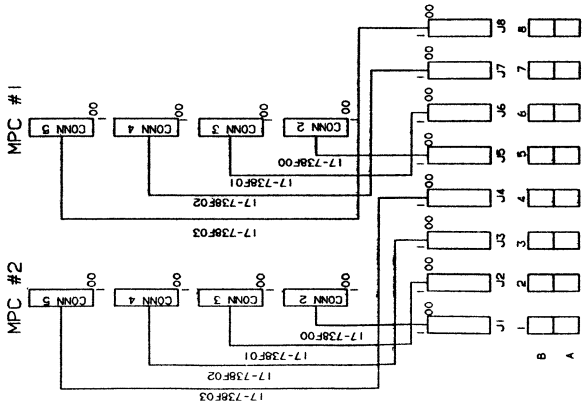
TITLE:
INSTALLATION/WIRING
3203 ENCLOSURE

TAS 0303203214

DWG: 01 559 012 1 - 2

REVISIONS





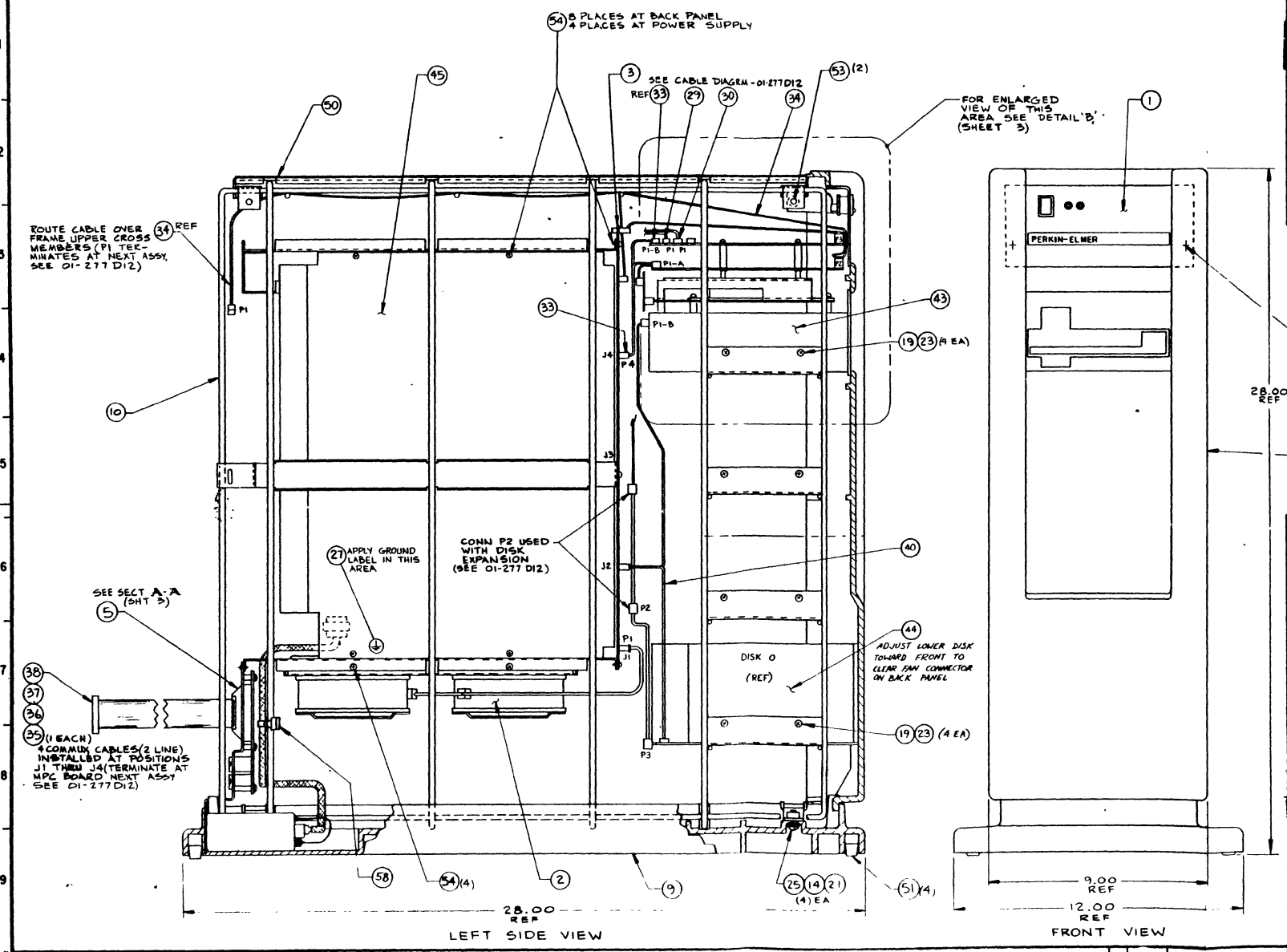
NOTES:

DRAFTER	
RPM	
DATE	TASK: 03039/03214
12-22-8(	DWG: 01-339 D12

2 - 2

Concurrent Computer Corporation
OCEANPORT, N.J. 07757

TITLE:
INSTALLATION DRAWING
3203 ENCLOSURE



USED IN MANUAL 47-087

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV	11-5-84			
	PROD				
AREA G4, J4 WAS 'P2', J3 WAS 'P2', AREA M9 ADDED SHT/REV BOX. REVISED SHTS 1 & 3.					
MF	VNC	5875	M	3-8-85	R01
AREA M9, REVISED SHTS 1, 2 & 3.					
MF	VNC	5884	R	6-3-85	R02
EXTENSIVE CHANGES, SEE ROO MICROFILM FOR PREVIOUS REV CHANGES. REV'D SHTS 1 & 2.					
DB	VNC	6027	M	6-11-85	R03 X
AREA M9, REVISED SHEETS 1 & 2.					
JB	VNC	6096	MS	8-15-85	R04 X
AREA 8 ADDED ITEM 58. REVISED SHTS 1 & 2					
JB	VT	6603	MS	8-20-86	R05 X

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX±.005 .XX±.03 .X±.02 ANGLES±1°	
NAME		TITLE	DATE
	MANFIELD	DES/DFT	10-19-84
R. CERO		SUPV	
		CHK	
D. FOGGIA		ENG	
PABITANTE		MGR	
R. BARKER		QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

NOTES

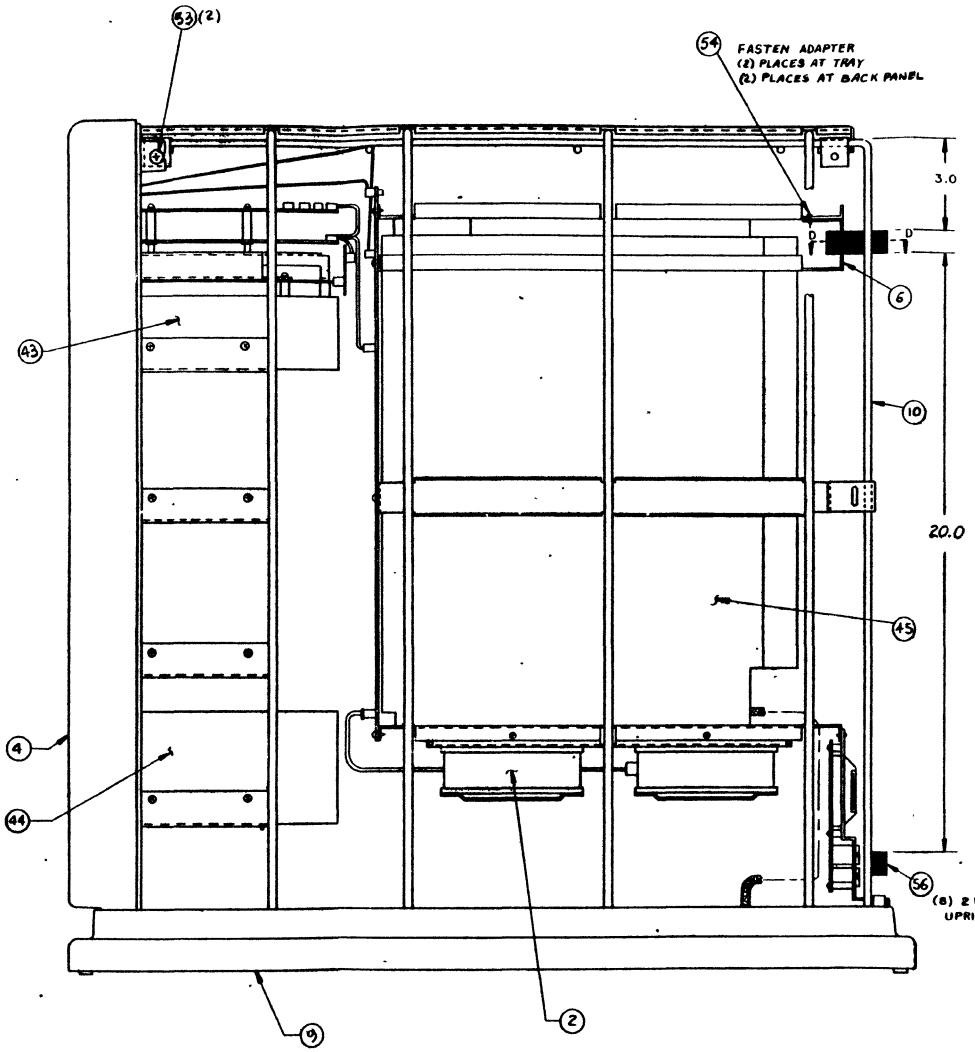
3	SHEET NUMBER
2	REVISION LEVEL

TITLE
BASIC ENCLOSURE
CORSAIR II

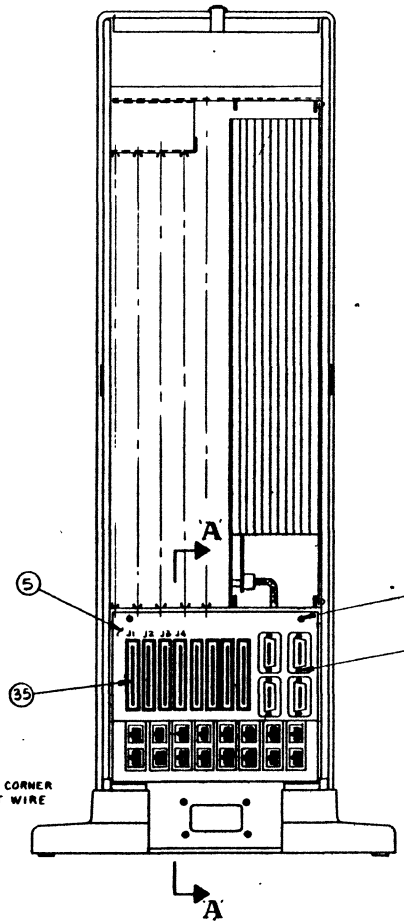
TASK 03354 | SHT 1-3

DWG 09-172 R05 D03

ADDED DIMENSIONS. AREA H3, ADDED SECTION 'D-D'					
MF	DRD	5884	R	6-5-85	R01
EXTENSIVE CHANGES, SEE R00 MICROFILM FOR PREVIOUS REV CHANGES.					
DB	DRD	6027	M	6-11-85	R02 X
AREA M7, ADDED ITEM 57 & NOTE					
JB	DRD	6096	MS	8-15-85	R03 X
AREA H3 THRU H8 CHANGED MEASUREMENTS. 9.5 NOM TWICE TO SINGLE 20.0. DELETED CENTER CLIPS AREA H5 ITEM 56					
JB	VT	6409	MS	8-20-86	R04 X



RIGHT SIDE VIEW
(LESS CABLES)



REAR VIEW

Concurrent Computer Corporation

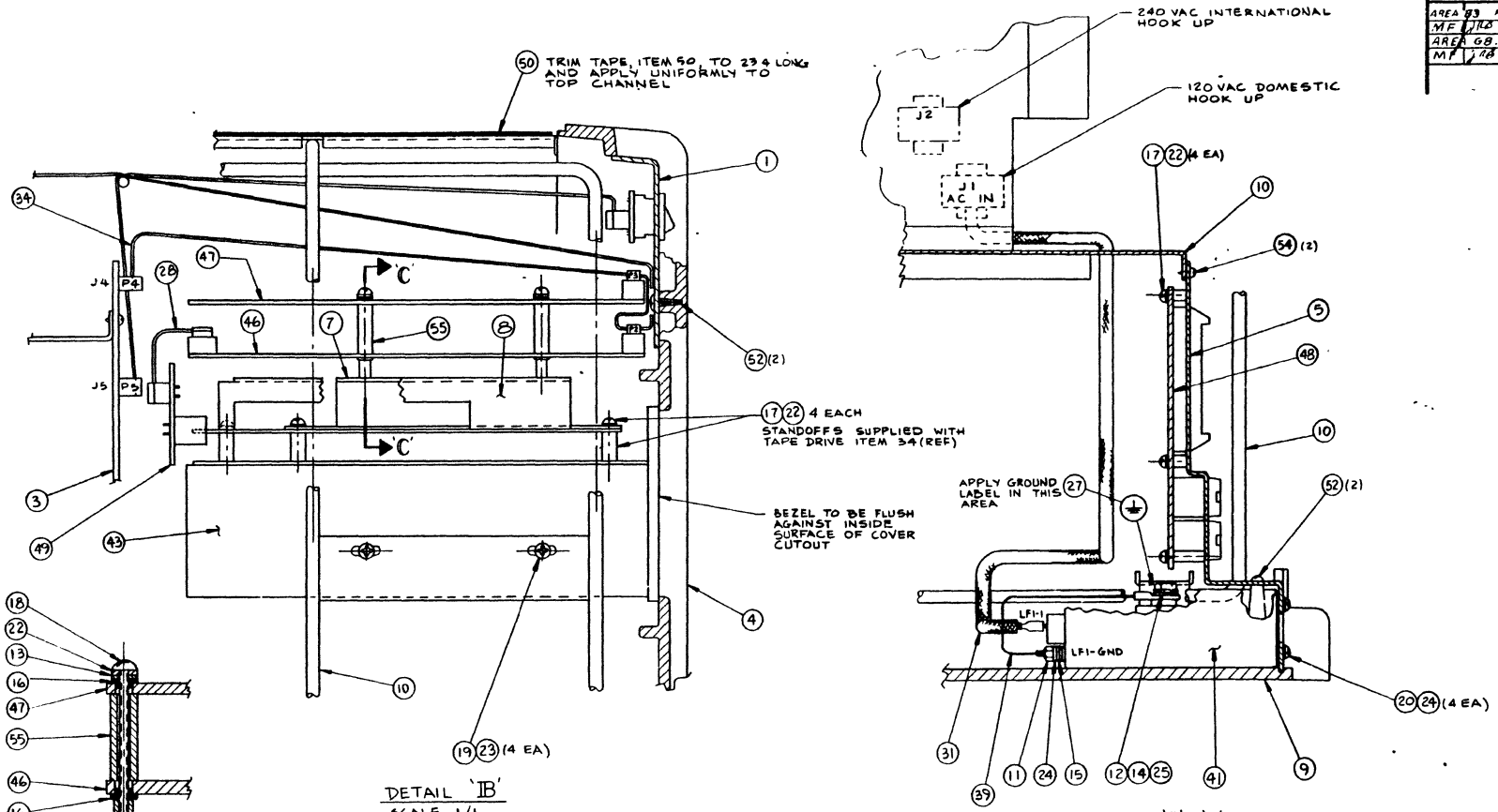
NOTES

DRAFTER	MANFIELD
DATE	8-27-84

TITLE
BASIC ENCLOSURE
7 CORSAIR II

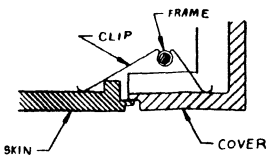
TASK 03354	SHT 2-3
DWG 09-172 R04 D03	

REVISIONS					
AREA 03 P.S. WAS P.S.					
MF	JRB	5875	M	3-8-85	R01
AREA 08. ADDED SECTION L-D.					
MF	JRB	5884	R	6-5-5	R02 X



DETAIL 'B'
SCALE 1/1

SECTION 'C'-'C'
CONTROLLER MOUNTING DETAIL TYPICAL 2 PLACES BOTH SIDES
(SCALE 2/1)



SECTION 'D'-'D'

SECTION 'A'-'A'
SCALE 1/1

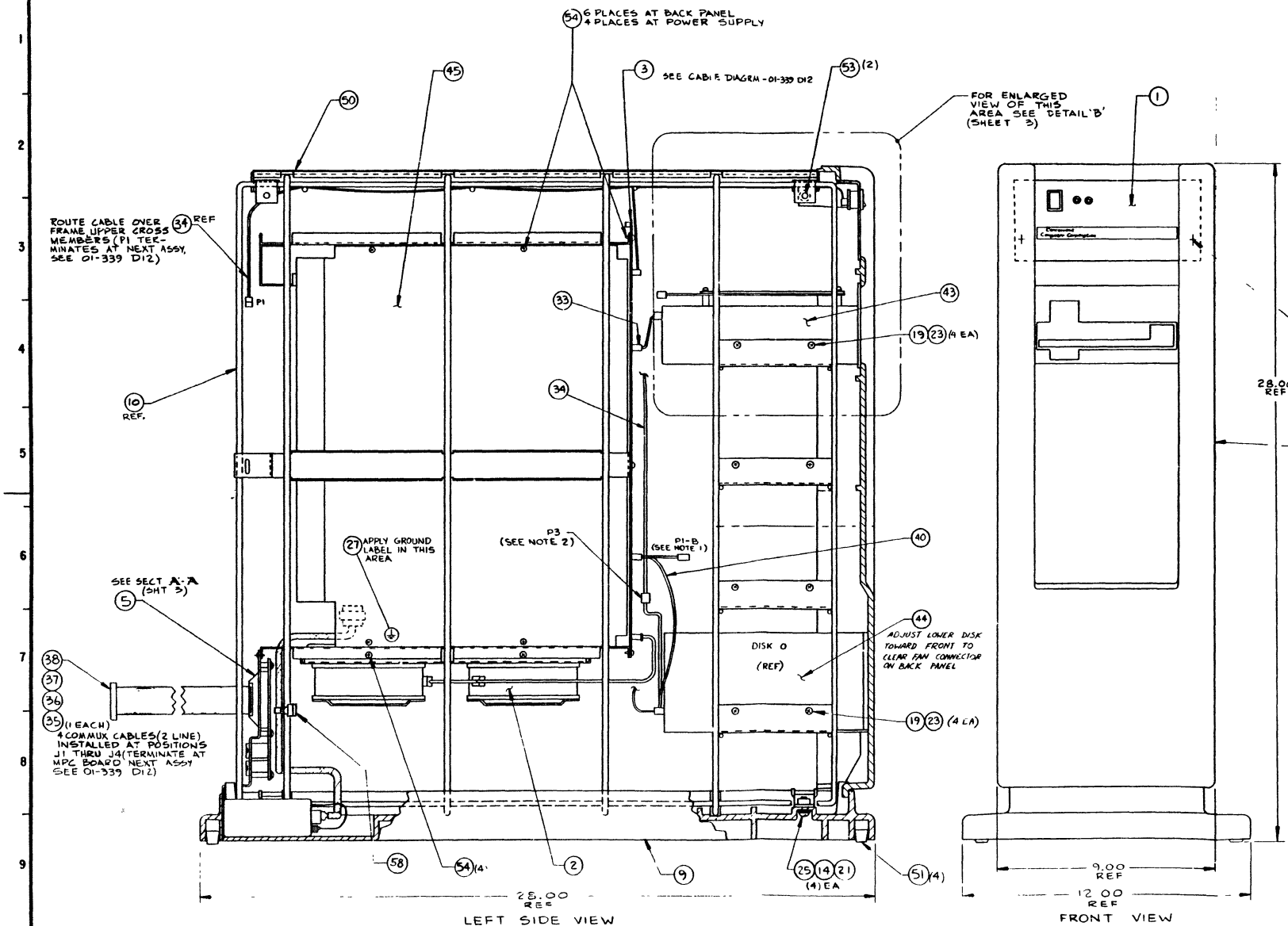
NOTES

DRAFTER	
MAYFIELD	
DATE	
8-27-84	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE
BASIC ENCLOSURE
CORSAIR II

TASK 03354	SHT
DWG 09-172 R02 D03	3-3



REVISIONS		
	INIT	DATE
PRE PRODUCTION APPROVAL	DEV	
	PROD	

UNLESS OTHERWISE SPECIFIED			
SCALE: 1/2		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX±.005 .XX±.03 .XX±.02 ANGLES ±1°	
NAME		TITLE	DATE
VILARDI	MANFIELD	DES/DFT	12/22/86
R CERO		SUPV	
		CHK	
D. FOGGIA		ENG	
PABITANTE		MGR	
R. BARKER		QC	

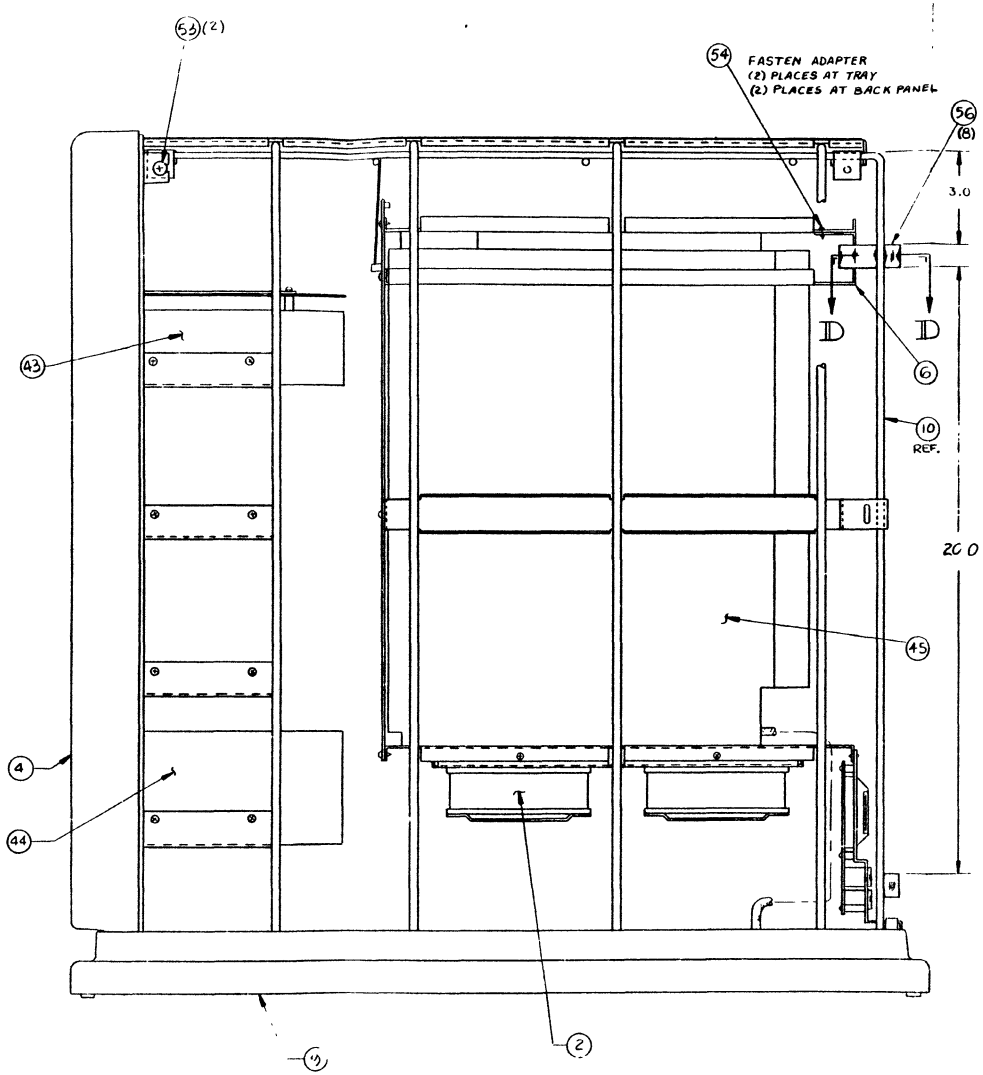
Concurrent Computer Corporation
Oceanport, N.J. 07757

NOTES:
1. CONN. P1-B (5/12 V POWER CABLE) FOR DISK EXP. SECURE WITH CABLE TIE WHEN NOT IN USE.
2. CONN. P3 (IPC CABLE) FOR DISK EXP. 01-339 D12.

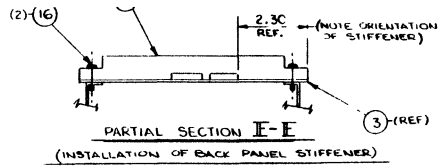
SHEET NUMBER	3	6
REVISION LEVEL	-	-

TITLE
BASIC ENCLOSURE
MODEL 3203

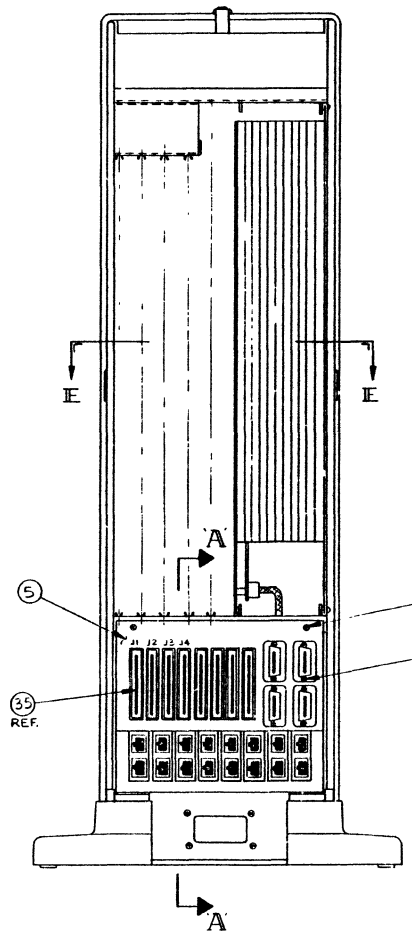
TASK 03039/03214	SHT
DWG 09-219 D03	1-3



RIGHT SIDE VIEW
(LESS CABLES)



PARTIAL SECTION E-E
(INSTALLATION OF BACK PANEL STIFFENER)



REAR VIEW

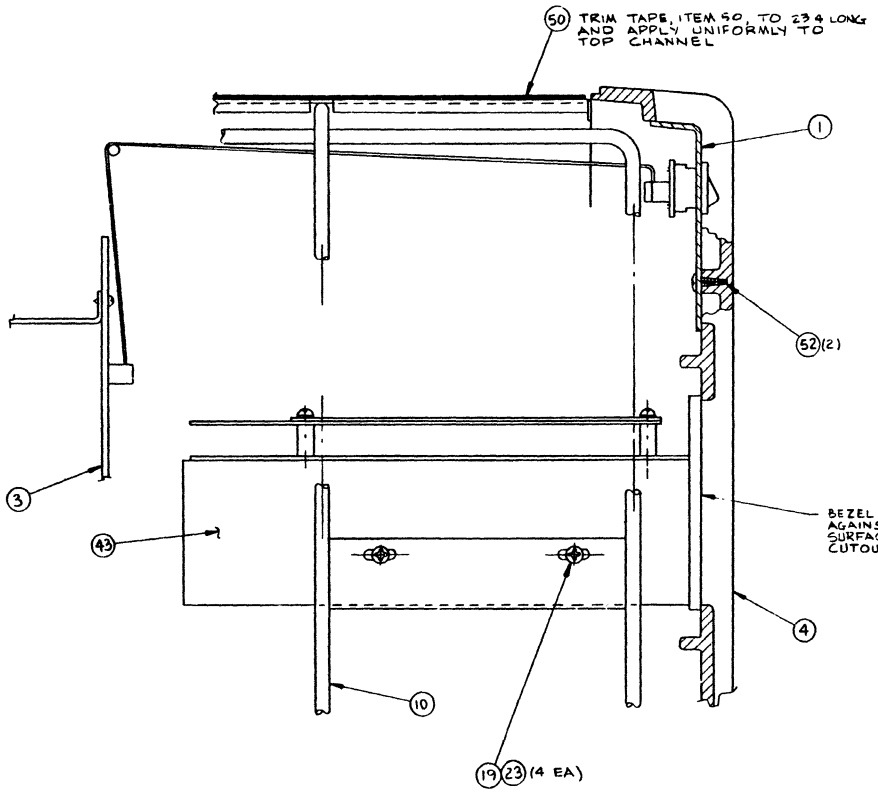
NOTES

DRAFTER	
DATE	12/22/86

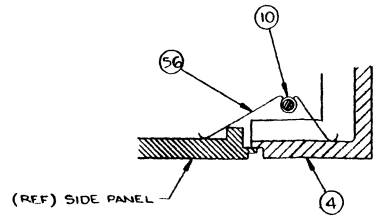
Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE
BASIC ENCLOSURE
MODEL 3203

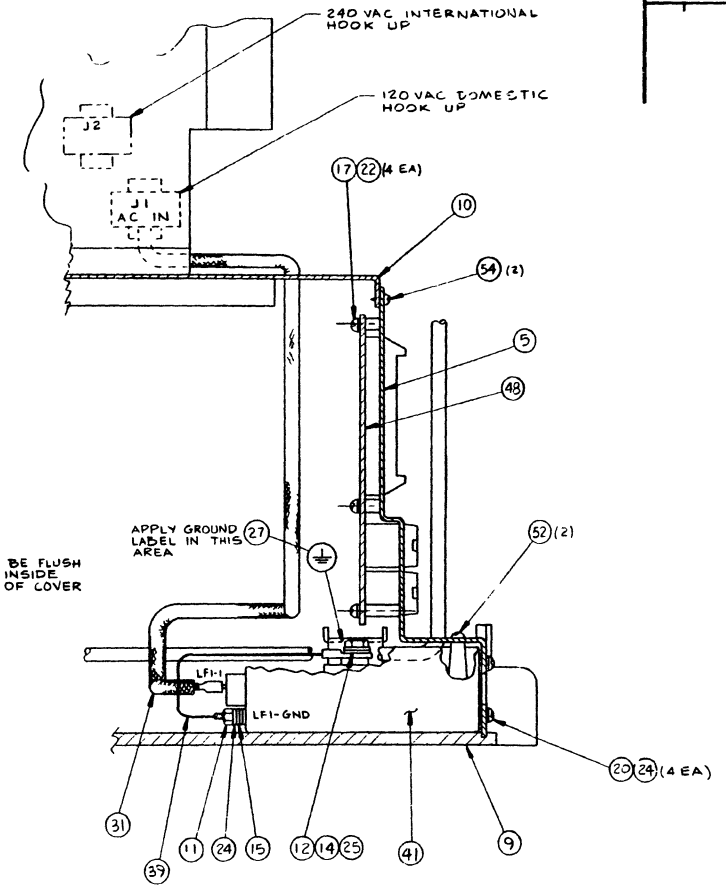
TASK 0309/03214		SHT
DWG 09-219	D03	2-?



DETAIL 'B'
SCALE 1/1



SECTION 'D-D'
DETAIL TYP.
(2 CLIPS PER CORNER UPRIGHT)



SECTION 'A-A'
SCALE 1/1

NOTES

REVISIONS

TITLE
BASIC ENCLOSURE
MODEL 3703

DRAFTER
[illegible]

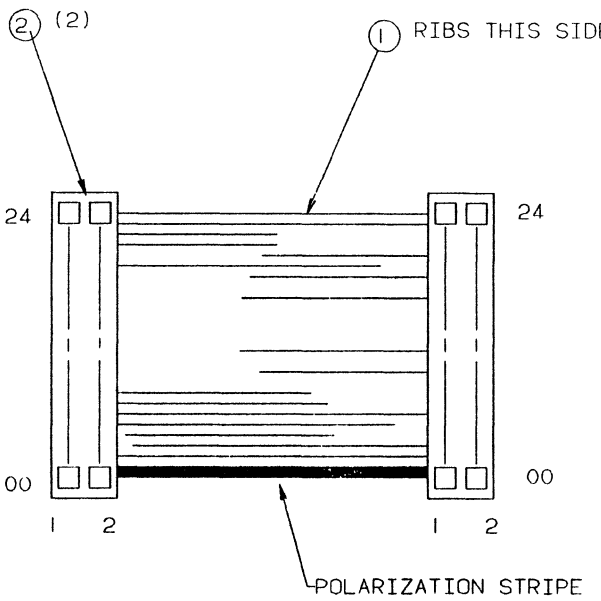
DATE
12/[illegible]

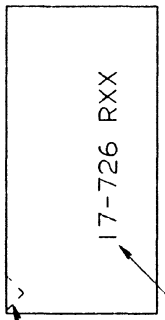
TASK [illegible]0309/03214

DWG 09-219 D03

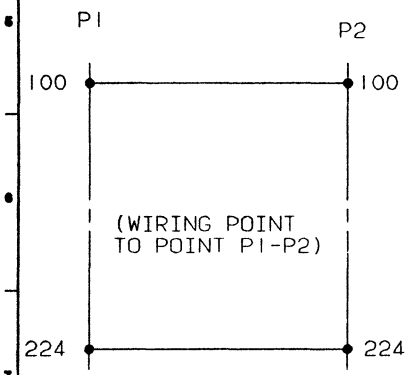
SHT 3-[illegible]

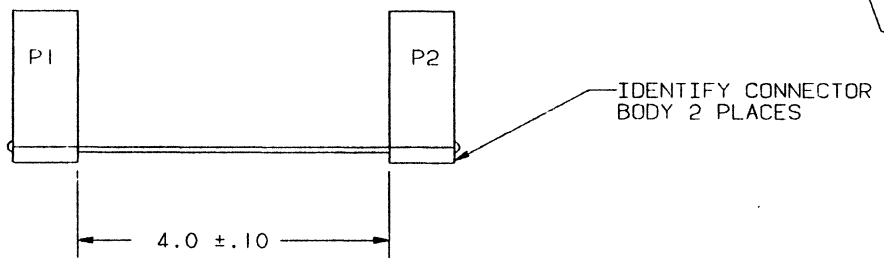
REVISIONS				
PRE PRODUCTION APPROVAL	INIT	DATE		
	DEV DF	11-8-84		
	PROD MJO	11-2-84		
AREA J,6 ADDED MANUAL NOTE				
SM	JRB	5921	D	5-3-85	R01
AREA D6, DIM. WAS 1.8 ±.10				
VT		6604	MS	8-31-86	R02





WIRING SCHEMATIC





USED IN MANUAL 47-087

NOTES:

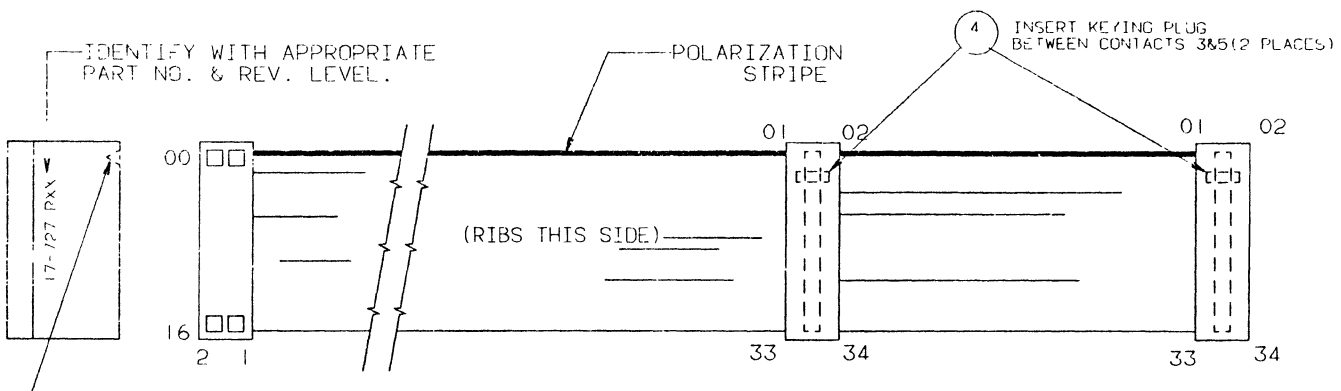
UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ±.005	.X ±.03	ANGLES ±1°
	.XX ±.02		
NAME	TITLE	DATE	
MAYFIELD	DES/DFT	9-13-84	
R CERO	SUPV		
	CHK		
D FOGGIA	ENG		
P ABITANTE	MGR		
R BARKER	QC		

Concurrent Computer Corporation
OCEANPORT, N J 07757

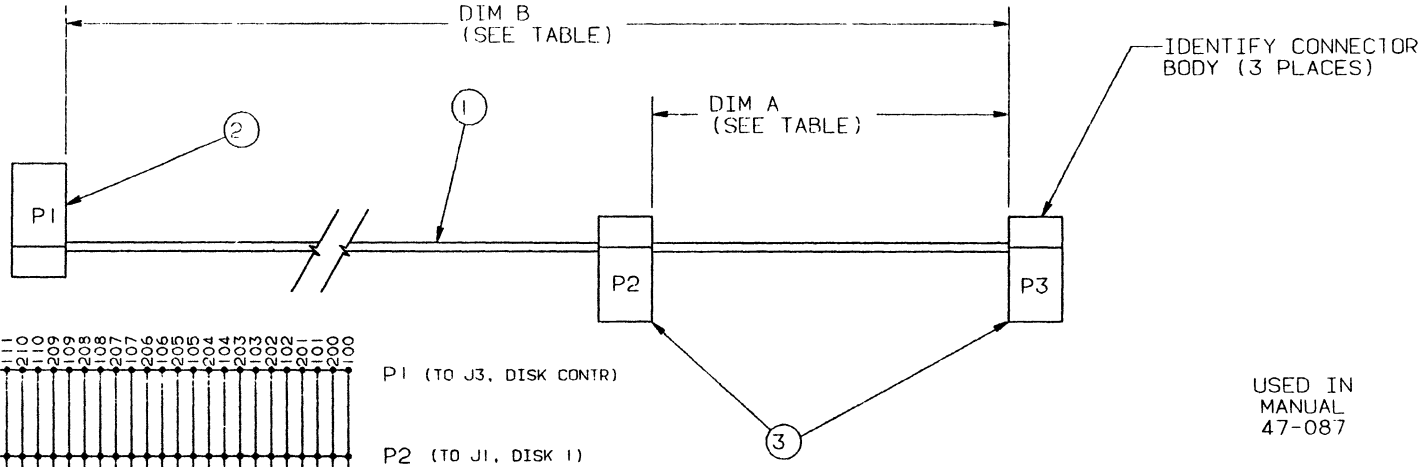
TITLE:
CABLE
INTERFACE OIC 36
CORSAIR II

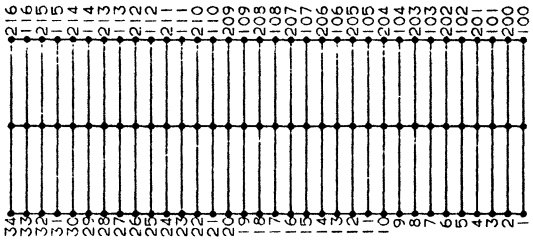
TASK 03354

DWG: 17-726R02 C03 1 - 1



TRIANGLE AT POS 100 (FARSIDE)





P1 (TO J3, DISK CONTR)

P2 (TO J1, DISK 1)

P3 (TO J1, DISK 2)

WIRING SCHEMATIC

USED IN MANUAL 47-087

17-727 F01	10.0	18.0
17-727 F00	4.8	26 5
FUNCTIONAL VARIATION	DIM A ±.25	DIM B ±.25

NOTES,

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV SF	10-24-84
	PROD MJV	10-24-84

AREA J.5 ADDED MANUAL NOTE					
SM	JRB	5921	D	5-3-85	R01
AREA G,1 ADDED ITEM 4. ADDED VARIATION TABLE					
SM	JRB	5961	P	6-10-85	R02
ADDED DIMENSION 10 00. WAS 18.0 ± 05					
SM	JRB	6027	R	6-10-85	R03
CORRECTED PIN NO'S. ON P2 & P3					
JT	JRB	6183	D	10/1/85	R04

UNLESS OTHERWISE SPECIFIED

SCALE.

DIMENSIONS ARE IN INCHES

TOLERANCE: XXX ± 005 .X ± 03 .XX ±.02 ANGLES ±1°

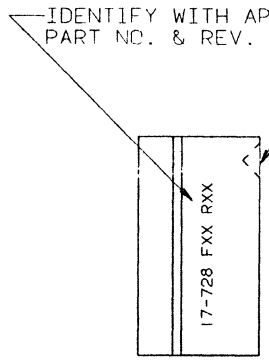
NAME	TITLE	DATE
MAYFIELD	DES/DFT	9-14-84
R CERO	SUPV	
	CHK	
D FOGGIA	ENG	
P ABITANTE	MGR	
R BARKER	QC	

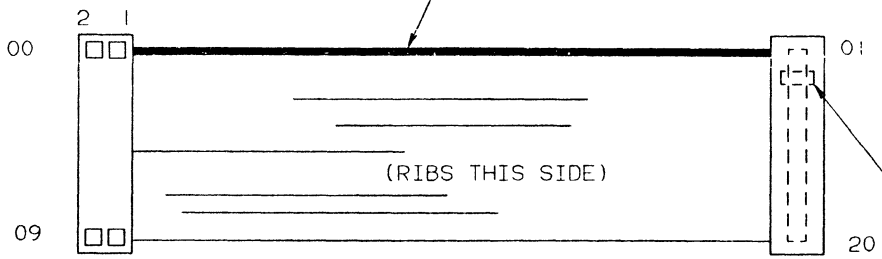
PERKIN-ELMER
Oceanport, N J 07757

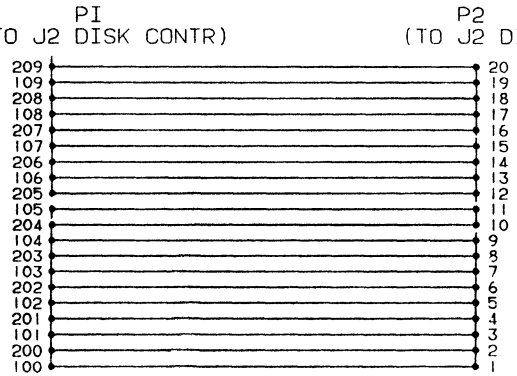
TITLE
CABLE, DISK
ST506 DAISY CHAIN
CORSAIR II

TASK 03354

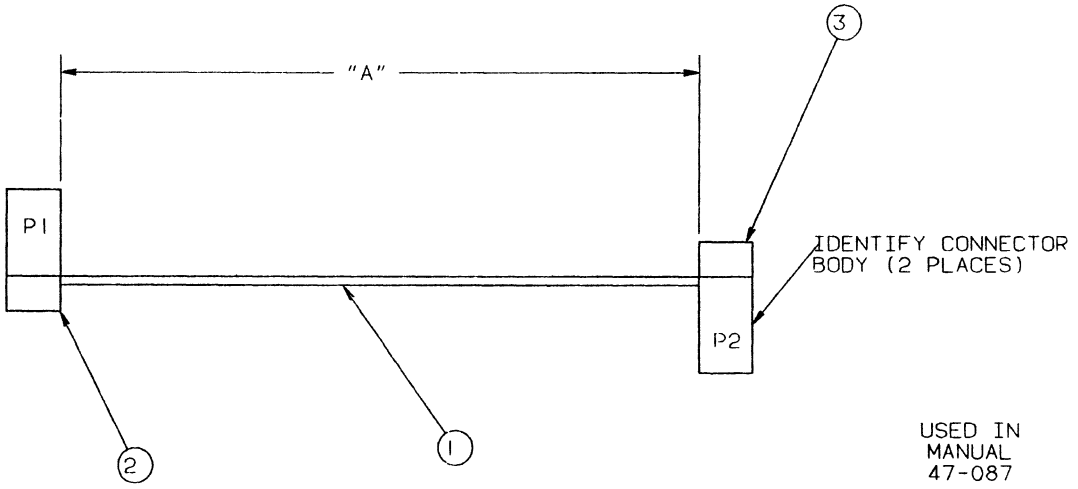
DWG 17-727P04 C03 1 - 1







WIRING SCHEMATIC



USED IN
MANUAL
47-087

17-728F02	6.0
17-728F01	26.5
17-728F00	21.0
PART NO.	DIM. "A"

REVISIONS

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV QE	10-24-84
	PROD MFG	10-24-84

AREA K,6 ADDED MANUAL NOTE					
SM	JRB	5921	D	5-3-85	R01
AREA H,2 ADDED ITEM 4 AREA B,6 ADDED F02 TO VAR. TABLE					
SM	JRB	5961	R	6-10-85	R02
IN VARIATION TABLE 21.0 WAS 13 26.5 WAS 17.5					
SM	JRB	6027	R	6-16-85	R03 X

NOTES.

UNLESS OTHERWISE SPECIFIED

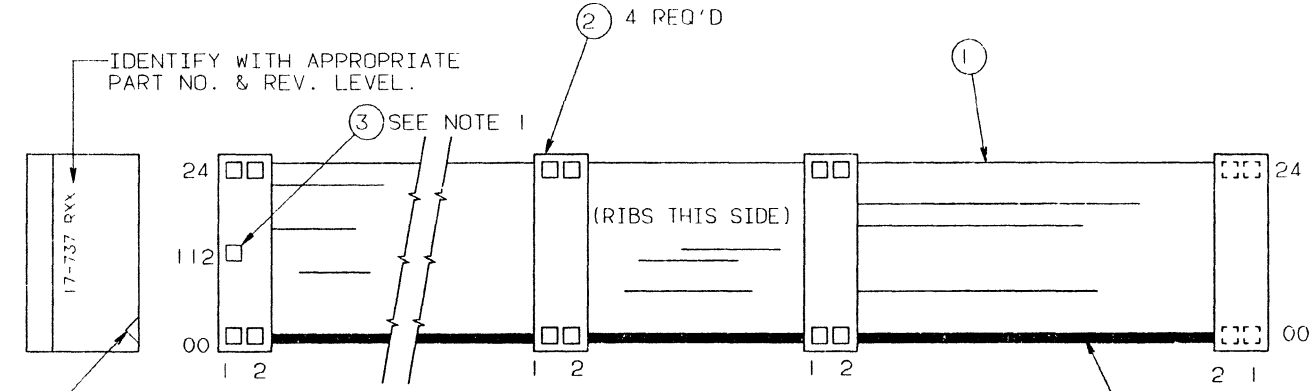
SCALE:	TOLERANCE.
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

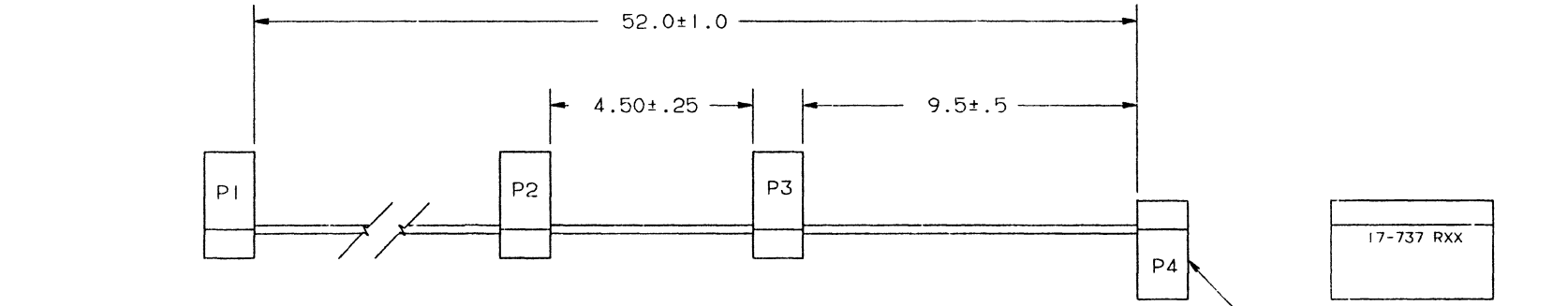
NAME		TITLE	DATE
	MAYFIELD	DES/DFT	9-14-84
R CERO		SUPV	
		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

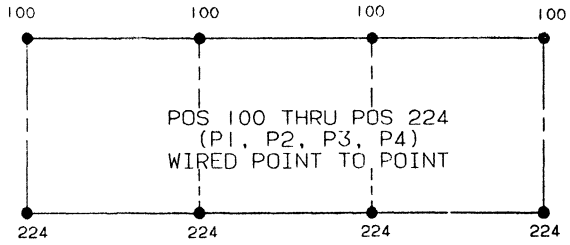
PERKIN-ELMER
Oceanport, N J 07757

TITLE
CABLE, DISK
ST 506 RADIAL DATA
CORSAIR II

TASK: 03354
DWG: 17-728R03 C03
1 - 1







P1 (TO CONN 2 IPC PCB) P2 (TO J M.T. CONTROLLER) P3 (TO J7, DISK CONTROLLER) P4 (TO JC, BACK PANEL)

WIRING SCHEMATIC

USED IN MANUAL 47-087

REVISIONS							
PRE PRODUCTION APPROVAL		INIT	DATE				
		DEV DF	11-2-84				
		PROD MJD	11-2-84				
ADDED ITEM 3, AND NOTE 1							
SM	JRB	5883	M	3-23-85	R01		
AREA K,6 ADDED MANUAL NOTE							
SM	JRB	5921	D	5-3-85	R02		
AREA E,4 DIM. WAS 48.0±1.0							
SM	JRB	6013	R	6-16-85	R03	X	
AREA E4, DIM WAS 2.5 ±.25							
VT	VT	6507	MS	9-13-86	R04	X	

NOTES:

1. ITEM NO. 3 (KEY PLUG) USED IN CONNECTOR P1 ONLY.

UNLESS OTHERWISE SPECIFIED			
SCALE	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± 005	.X ±.03	ANGLES ±1°
NAME		TITLE	DATE
	MAYFIELD	DES/DFT	9-14-84
R CERO		SUPV	
		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

Concurrent Computer Corporation
OCEANPORT, N J 07757

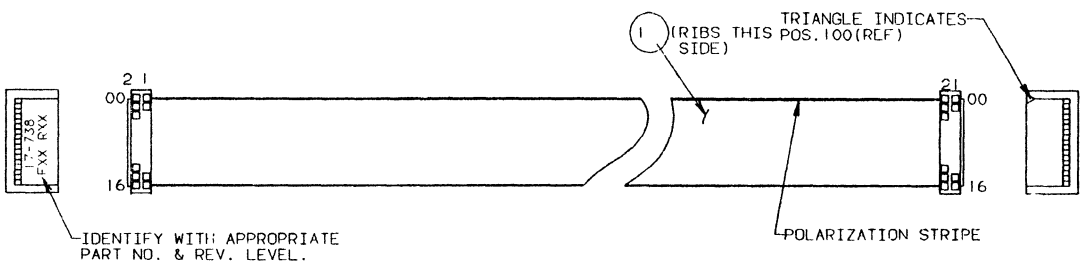
TITLE
CABLE, IPC
CORSAIR II

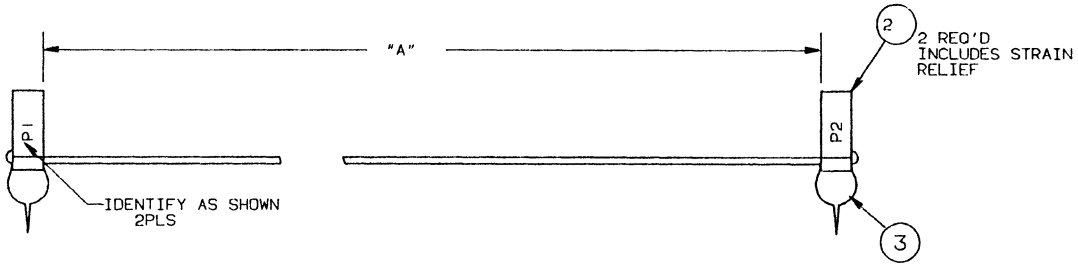
TASK. 03354

DWG 17-737 R04 C03

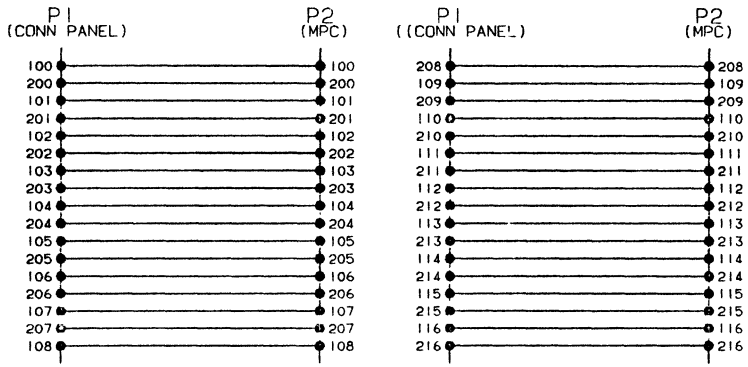
1 - 1

REVISIONS			
PRE PRODUCTION APPROVAL	INIT	DATE	
	DEV DF	10-24-84	
	PROD MJO	10-24-84	
AREA G6 9 0 WAS 11.0 11.0 WAS 14.0,14.0 WAS 16.0			
SM JRB 5883 M 3-23-85 R01			
AREA K,6 ADDED MANUAL NOTE			
SM JRB 5921 D 5-3-85 R02 X			
AREA A2 THRU G4 REV'D CABLE, ADDED ITEM 3 AREA G6 ADDED P/N TO FUNC VARI VARI CHG TITLE FROM 'CORSAIR II'			
MCF JRB 6725 MS 2/27/87 R03 X			





WIRING DIAGRAM



17-738F03	14.0
17-738F02	11.0
17-738F01	9.0
17-738F00	7.0
PART NO.	DIM A
FUNCTIONAL VARIATION CHART	

USED IN
MANUAL
47-087

Concurrent Computer Corporation
OCEANPORT, N J. 07757

UNLESS OTHERWISE SPECIFIED			
SCALE: 1.5:1	TOLERANCE		
DIMENSIONS ARE IN INCHES	.XXX ±.005	.X ± 03	
	.XX ±.02	ANGLES ±1°	

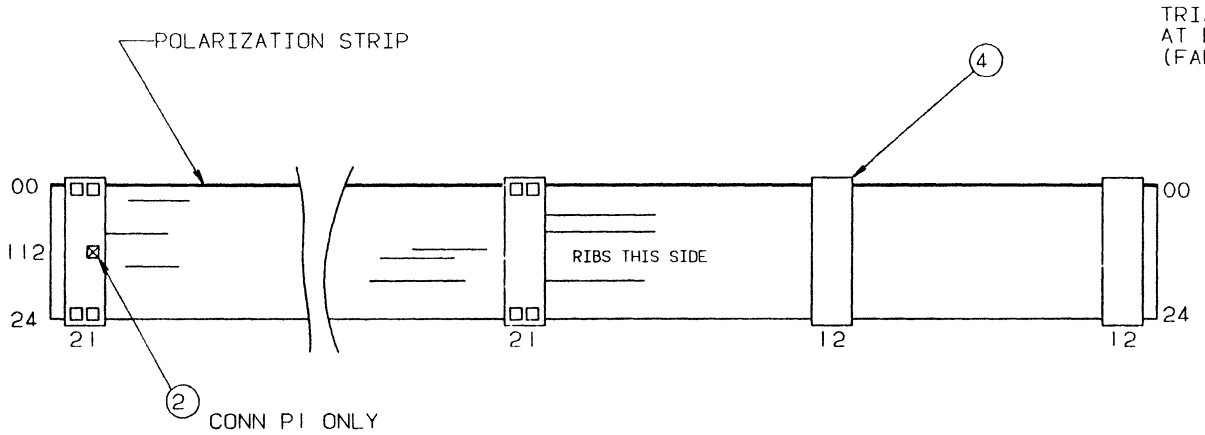
NAME		TITLE	DATE
D STINE	D STINE	DES/DFT	4-30-84
R CERO		SUPV	
		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

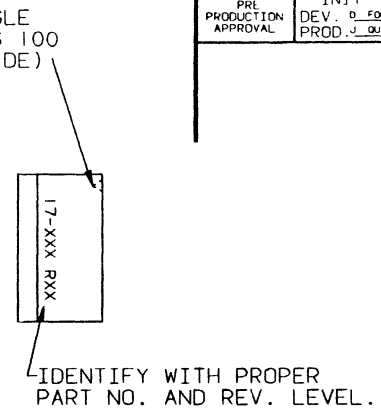
NOTES.

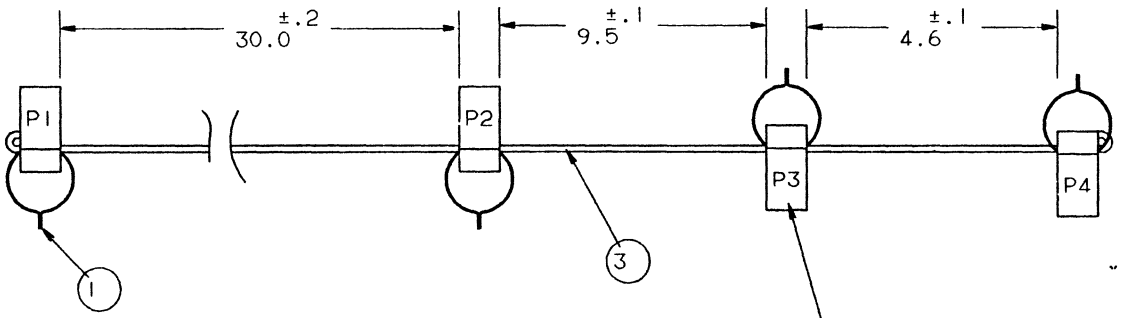
TITLE:
CABLE
COM MUX (INTERNAL)
3203

TASK 03069

DWG 17-738 R03 C03 1 - 1







IDENTIFY AS SHOWN
TYP 4 PLCS

REVISIONS		
	INIT	DATE
PRE PRODUCTION APPROVAL	DEV. D FOGGIA 3/20/87	
	PROD. J QUINN 3/20/87	

NOTES:

UNLESS OTHERWISE SPECIFIED

SCALE: ---	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°

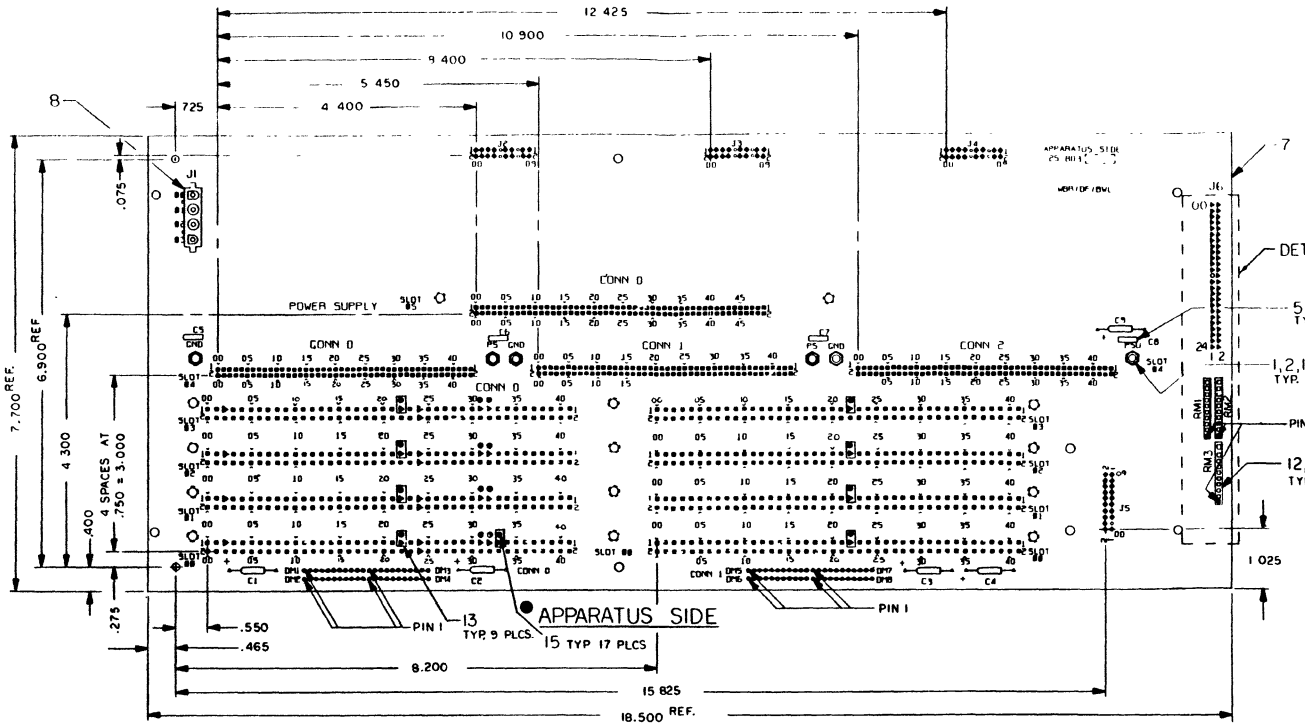
NAME		TITLE	DATE
	RPM	DES/DFT	11-6-86
R CERO		SUPV	
		CHK	
D FOGGIA		ENG	
P ABITANTE		MGR	
R BARKER		QC	

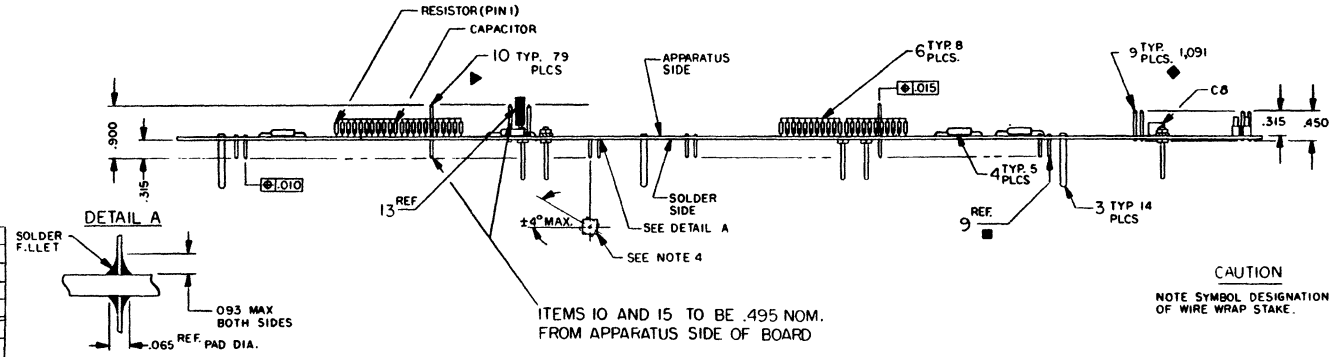
Concurrent Computer Corporation
OCEANPORT, N J 07757

TITLE:
CABLE, IPC 50COND
3203

TASK 03039/03214

DWG: 17-927 C03 1-1





SYMBOL	DESCRIPTION
○	NOT EQUIPPED
●	ITEM 15 (APP SIDE)
▶	ITEM 10 STAKE
◆	ITEM 9 (APP SIDE)
■	ITEM 9 (SOLDER SIDE)

STAKE SYMBOL TABLE

CAUTION

NOTE SYMBOL DESIGNATION OF WIRE WRAP STAKE.

NOTES
1. AFTER STAKING PINS (ITEMS 9 & 10) TO P.C. BOARD, SOLDER INTO PLACE
2. BOARD MUST PASS INSPECTION PROCEDURE QI 10-001 "PRINTED BACKPANEL ASSEMBLY."
3. FOR BOARD IDENTIFICATION SEE SSP 002-0D.
4. MAX VARIATION FOR PIN ORIENTATION SHALL NOT EXCEED ± 4°, (NTS)

PART NO.	DESCRIPTION
35-897F01	AS SHOWN LESS COMPONENTS IN DETAIL A
35-897F00	AS SHOWN WITH COMPONENTS IN DETAIL A

FUNCTIONAL VARIATION TABLE

EXT CHG'S				
EC	—	—	10-3-84	R01

PRE PRODUCTION APPROVAL	INIT	DATE
DEV		
PROD		

EXTENSIVE CHANGE, FOR PREVIOUS REV SEE R01
MICROFILM COPY AREA IN MANUAL WAS 47 082

M.F.	3881	M	3-28-85	R02

ADDED FUNCTIONAL VALIDATION TABLE AREA
(3 ADDED DETAILS)

KP	6760	K	7 28 87	E03

USED IN MANUAL : 47-087

UNLESS OTHERWISE SPECIFIED		
SCALE: 1:1	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME	TITLE	DATE
B. LUSK E. JOHNSON	DES/DFT	4-28-84
R. CERO	SUPV	10-18-84
	CHK	
D FOGGIA	ENG	
P. ABITANTE	MGR	
R. A. BARKER	QC	

Concurrent Computer Corporation
Oceanport, N.J. 07757

TITLE ASSEMBLY DRAWING
BACKPANEL
5 BRD. VERT.

TASK 03354	SHT
DWG 35-897R03 D03	1-1

J1	
PIN	FUNCTION
00	P12
01	P12
02	-P12
03	-P12

J2			
ROW 1		ROW 2	
PIN	FUNCTION	PIN	FUNCTION
09	P12	09	P12
08	P12	08	P12
07		07	
06	-P12	06	-P12
05	-P12	05	-P12
04		04	
03	P5	03	P5
02	P5	02	P5
01	GND	01	GND
00	GND	00	GND

J3			
ROW 1		ROW 2	
PIN	FUNCTION	PIN	FUNCTION
09	P12	09	P12
08	P12	08	P12
07		07	
06	-P12	06	-P12
05	-P12	05	-P12
04		04	
03	P5	03	P5
02	P5	02	P5
01	GND	01	GND
00	GND	00	GND

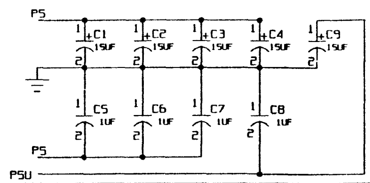
J4			
ROW 1		ROW 2	
PIN	FUNCTION	PIN	FUNCTION
09	P12	09	P12
08	P12	08	P12
07		07	
06	-P12	06	-P12
05	-P12	05	-P12
04		04	
03	P5	03	P5
02	P5	02	P5
01	GND	01	GND
00	GND	00	GND

J5			
ROW 1		ROW 2	
PIN	FUNCTION	PIN	FUNCTION
09	GND	09	GND
08	P5	08	
07	C4	07	
06	WAIT0	06	POFF0
05	SNGL0	05	FAULT0
04		04	PFDT0
03		03	RCATN0
02		02	SCATN0
01	KEYED	01	LSU1
00	GND	00	GND

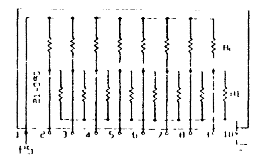
SLOT 5

ROW 1				ROW 2			
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
24	P5	49	P12	24	P5	49	P12
23	GNDSNSE	48	P12	23	P5SNSE	48	P12
22	GND	47	P12	22	GND	47	-P12
21	GND	46	-P12	21	GND	46	-P12
20	GND	45	-P12	20	GND	45	-P12
19	GND	44	P5U	19	GND	44	P5U
18	GND	43	P5USNSE	18	GND	43	P5U
17	GND	42		17	GND	42	
16	GND	41	P5	16	GND	41	P5
15	GND	40	P5	15	GND	40	P5
14	GND	39	P5	14	GND	39	P5
13	GND	38	P5	13	GND	38	P5
12	GND	37	P5	12	GND	37	P5
11	GND	36	P5	11	GND	36	P5
10	GND	35	P5	10	GND	35	P5
09	GND	34	P5	09	GND	34	P5
08	GND	33	P5	08	GND	33	P5
07	GND	32	P5	07	GND	32	P5
06	GND	31	P5	06	GND	31	P5
05	GND	30	P5	05	GND	30	P5
04	GND	29	P5	04	GND	29	P5
03	C4	28	P5	03		28	P5
02	2XLF	27	P5	02	PFDT0	27	P5
01		26	P5	01		26	P5
00		25	P5	00		25	P5

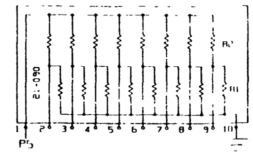
J6			
ROW 1		ROW 2	
PIN	FUNCTION	PIN	FUNCTION
24	GND	24	RM2-9
23	GND	23	RM1-9
22	GND	22	RM2-8
21	GND	21	RM1-8
20	GND	20	RM2-7
19	GND	19	RM1-7
18	GND	18	RM2-6
17	GND	17	RM1-6
16	GND	16	RM2-5
15	GND	15	RM1-5
14	GND	14	RM2-4
13	GND	13	RM1-4
12		12	
11	GND	11	RM2-3
10	GND	10	RM1-3
09	GND	09	RM2-2
08	GND	08	RM1-2
07	GND	07	RM3-9
06	GND	06	RM3-8
05	GND	05	RM3-7
04	GND	04	RM3-6
03	GND	03	RM3-5
02	GND	02	RM3-4
01	GND	01	RM3-3
00	GND	00	RM3-2



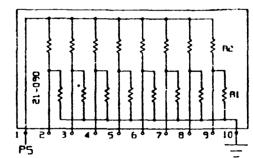
RM1



RM2



RM3



REVISED SHEETS 1 AND 3 ADDED [illegible]
BWI | BWI | | - | 10/16/84 | R01 | Y

PRE PRODUCTION APPROVAL	INT	DATE
	DEV WBR	10/23/84
	PROD	

ADDED RCATN0 TO CONN J5-PIN 203 ADDED KEYED TO CONN J5-PIN 101, DELETED MEMPWR FROM CONN 5 PIN 208, DELETED MEMPWR1 FROM SLOT 5-PIN 203, ADDED CLRCNT0 TO CONN 2 PINS 122 AND 123, AREA M9, MANUAL WA[illegible]-082
BWI | [illegible] | 5881 | M | 03/23/85 | R02

SLOT 04

CONN 0

PIN	ROW 1	FUNCTION	LOCATION	PIN	ROW 2	FUNCTION	LOCATION
43	GND			43	GND		
42	GND			42	GND		
41				41			
40	GND			40			
39	GND			39			
38	KEYED			38			
37	GND			37	C4	R	
36	GND			36	POFF0	R	
35	GND			35	WAIT0	S	
34	GND			34	FAULT0	S	
33	GND			33			
32	GND			32	SNGL0	R	
31	GND			31	PFDT0	S	
30	GND			30	RCATN0	R	
29	GND			29	SCATN0	R	
28	GND			28	LSU1	R	
27				27			
26	SCLR0	S		26	HW0	R	
25				25			
24				24			
23	SYN0	R		23	ATN0	R	
22				22	TACK0	S	
21	CL070	S		21	DA0	S	
20	DR0	S		20	CMD0	S	
19	SR0	S		19	ADRS0	S	
18	D140	S/R		18	D150	S/R	
17	D120	S/R		17	D130	S/R	
16	D100	S/R		16	D110	S/R	
15	D080	S/R		15	D090	S/R	
14	D060	S/R		14	D070	S/R	
13	D040	S/R		13	D050	S/R	
12	D020	S/R		12	D030	S/R	
11	D000	S/R		11	D010	S/R	
10				10			
09				09			
08				08	GND		
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	GND			00	GND		

CONN 1

PIN	ROW 1	FUNCTION	LOCATION	PIN	ROW 2	FUNCTION	LOCATION
43	GND			43	GND		
42	GND			42	GND		
41	SC01	S		41	SC11	S	
40	SC21	S		40	SC31	S	
39	SC41	S		39	SC51	S	
38				38	CB01	R	
37				37			
36	GND			36	GND		
35	CB11	R		35	CB21	R	
34	CB31	R		34	CB41	R	
33	CB51	R		33			
32	GND			32			
31	E000	S/R		31	E010	S/R	
30	E020	S/R		30	E030	S/R	
29	E040	S/R		29	E050	S/R	
28	E060	S/R		28	E070	S/R	
27	GND			27	GND		
26	SCLR0	S		26	PHW0	R	
25				25	SCHK0	R	
24	SENS0	R		24	SBUSY0	S	
23	PSYN0	R		23	PATN0	R	
22	PRACK0	R	NOTE 2	22	PTACK0	S	NOTE 2
21	PCL070	S		21	PDA0	S	
20	PDR0	S		20	PCMD0	S	
19	PSR0	S		19	PADRS0	S	
18	PD140	S/R		18	PD150	S/R	
17	PD120	S/R		17	PD130	S/R	
16	PD100	S/R		16	PD110	S/R	
15	PD080	S/R		15	PD090	S/R	
14	PD060	S/R		14	PD070	S/R	
13	PD040	S/R		13	PD050	S/R	
12	PD020	S/R		12	PD030	S/R	
11	PD000	S/R		11	PD010	S/R	
10	GND			10	GND		
09	E080	S/R		09	E090	S/R	
08	E101	S/R		08	E111	S/R	
07	E121			07	E131	S/R	
06	E141	S/R		06	E151	S/R	
05	GND			05	GND		
04	D0E	S		04	MEMCLK0	S	
03	GND			03	GND		
02				02	WECLK	S	
01	GND			01	GND		
00	GND			00	GND		

CONN 2

PIN	ROW 1	FUNCTION	LOCATION	PIN	ROW 2	FUNCTION	LOCAT
43				43			
42				42			
41				41			
40				40			
39				39			
38				38			
37				37			
36				36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29				29			
28				28			
27				27			
26				26			
25				25			
24				24			
23	CLRCNT0			23			
22	CLRCNT0			22			
21				21			
20				20			
19	GND			19	GND		
18	WE60	S		18	WE70	S	
17	WE40	S		17	WE50	S	
16	WE20	S		16	WE30	S	
15	GND			15	GND		
14	CAS60	S		14	CAS70	S	
13	CAS40	S		13	CAS50	S	
12	CAS20	S		12	CAS30	S	
11	GND			11	GND		
10	RAS20	S		10	RAS30	S	
09	RAS00	S		09	RAS10	S	
08	GND			08	GND		
07	MX80	S		07	GND		
06	GND			06	GND		
05	MX60	S		05	MX70	S	
04	MX40	S		04	MX50	S	
03	GND			03	GND		
02	MX20	S		02	MX30	S	
01	MX00	S		01	MX10	S	
00	GND			00	GND		

NOTES - 1 S - SENDER
R - RECEIVER
S/R - SENDER RECEIVER

2. USE JUMPER BLOCK PROVIDED WHEN SLOT IS NOT EQUIPPED

REV	R02	R00	R01
SHT	1	2	3

THE REVISION LEVEL OF THIS SHEET IS THE REVISION LEVEL OF THE DOCUMENT

BOARDS AGREEING WITH THIS SCHEMATIC SHOULD BE AT THE FOLLOWING REVISION LEVEL

PART NO	REVISION
35-897	R02

USED IN MANUAL 47-08[illegible]

DISKETTE - SCH01222

UNLESS OTHERWISE SPECIFIED

SCALE 2/1

DIMENSIONS ARE IN MILLIMETERS

TOLERANCE
XXX - .13
XX - .5
X - 8
ANG - 1°

NAME		TITLE	DATE
BLUSK	BLUSK	DES/DFT	04/84
R. CERO		SUPV	09/84
		CHK	
RICE/FOGGIA		ENG	
RICE/FOGGIA		MGR	
R. BARKER		QC	

PERKIN-ELMER

OCEANPORT, NEW JERSEY 07757

TITLE BACKPANEL MAP

CORSAIR II BACKPANEL

TASK 03017

DWG 35-897 R02 D08

SHT 1 - 3

I/O

SLOTS 0 AND 1

CONNECTOR 1

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37	GND		
36				36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29				29			
28				28			
27	GND			27			
26	SCLR0	A	NOTE 2	26	HW0	S	NOTE 2
25				25	SCHK0	S	NOTE 2
24	SENS0	S	NOTE 2	24	SBUSY0	A	NOTE 2
23	SYN0	S	NOTE 2	23	ATN0	S	NOTE 2
22	RACK0	A	NOTE 3	22	TACK0	S	NOTE 4
21	CL070	A	NOTE 2	21	DA0	A	NOTE 2
20	DA0	A	NOTE 2	20	CM00	A	NOTE 2
19	SA0	A	NOTE 2	19	ADRS0	A	NOTE 2
18	D140	S/A	NOTE 2	18	D150	S/A	NOTE 2
17	D120	S/A	NOTE 2	17	D130	S/A	NOTE 2
16	D100	S/A	NOTE 2	16	D110	S/A	NOTE 2
15	D080	S/A	NOTE 2	15	D090	S/A	NOTE 2
14	D060	S/A	NOTE 2	14	D070	S/A	NOTE 2
13	D040	S/A	NOTE 2	13	D050	S/A	NOTE 2
12	D020	S/A	NOTE 2	12	D030	S/A	NOTE 2
11	D000	S/A	NOTE 2	11	D010	S/A	NOTE 2
10				10			
09				09			
08				08	GND		
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	P5			00	GND		

CONNECTOR 0

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37			
36	GND			36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29	GND			29			
28				28			
27				27			
26	SCLR0	A		26	HW0	S	
25				25			
24	LSU1		NOTE 3	24	PFDT0		NOTE 3
23	SYN0	S		23	ATN0	S	
22	RACK0	A	NOTE 4	22	TACK0	S	NOTE 4
21	CL070	A		21	DA0	A	
20	DA0	A		20	CM00	A	
19	SA0	A		19	ADRS0	A	
18	D140	S/A		18	D150	S/A	
17	D120	S/A		17	D130	S/A	
16	D100	S/A		16	D110	S/A	
15	D080	S/A		15	D090	S/A	
14	D060	S/A		14	D070	S/A	
13	D040	S/A		13	D050	S/A	
12	D020	S/A		12	D030	S/A	
11	D000	S/A		11	D010	S/A	
10				10			
09				09			
08				08			
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	P5			00	GND		

IPC

SLOT 2

CONNECTOR 1

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37	GND		
36				36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29				29			
28				28			
27	GND			27			
26	SCLR0	A		26	PHW0	S	
25				25	SCHK0	S	
24	SENS0	A		24	SBUSY0	A	
23	PSYN0	S		23	PATN0	S	
22	PRACK0	A	NOTE 4	22	PTACK0	S	NOTE 4
21	PCL070	A		21	PDA0	A	
20	PDA0	A		20	PCM00	A	
19	PSA0	A		19	PADRS0	A	
18	PD140	S/A		18	PD150	S/A	
17	PD120	S/A		17	PD130	S/A	
16	PD100	S/A		16	PD110	S/A	
15	PD080	S/A		15	PD090	S/A	
14	PD060	S/A		14	PD070	S/A	
13	PD040	S/A		13	PD050	S/A	
12	PD020	S/A		12	PD030	S/A	
11	PD000	S/A		11	PD010	S/A	
10				10			
09				09			
08				08	GND		
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	P5			00	GND		

CONNECTOR 0

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37			
36	GND			36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29	GND			29			
28				28			
27				27			
26	SCLR0	A		26	HW0	S	
25				25			
24	LSU1		NOTE 3	24	PFDT0		NOTE 3
23	SYN0	S		23	ATN0	S	
22	RACK0	A	NOTE 4	22	TACK0	S	NOTE 4
21	CL070	A		21	DA0	A	
20	DA0	A		20	CM00	A	
19	SA0	A		19	ADRS0	A	
18	D140	S/A		18	D150	S/A	
17	D120	S/A		17	D130	S/A	
16	D100	S/A		16	D110	S/A	
15	D080	S/A		15	D090	S/A	
14	D060	S/A		14	D070	S/A	
13	D040	S/A		13	D050	S/A	
12	D020	S/A		12	D030	S/A	
11	D000	S/A		11	D010	S/A	
10				10			
09				09			
08				08			
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	P5			00	GND		

MPC

SLOT 3

CONNECTOR 1

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37	GND		
36				36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29				29			
28				28			
27	GND			27			
26	SCLR0	A		26	PHW0	S	
25				25	SCHK0	S	
24	SENS0	S		24	SBUSY0	A	
23	PSYN0	S		23	PATN0	S	
22	PRACK0	A	NOTE 4	22	PTACK0	S	NOTE 4
21	PCL070	A		21	PDA0	A	
20	PDA0	A		20	PCM00	A	
19	PSA0	A		19	PADRS0	A	
18	PD140	S/A		18	PD150	S/A	
17	PD120	S/A		17	PD130	S/A	
16	PD100	S/A		16	PD110	S/A	
15	PD080	S/A		15	PD090	S/A	
14	PD060	S/A		14	PD070	S/A	
13	PD040	S/A		13	PD050	S/A	
12	PD020	S/A		12	PD030	S/A	
11	PD000	S/A		11	PD010	S/A	
10				10			
09				09			
08				08	GND		
07				07			
06				06			
05				05			
04				04			
03				03			
02				02			
01	GND			01	GND		
00	P5			00	GND		

CONNECTOR 0

PIN	ROW 1	FUNCTION	LOC	PIN	ROW 2	FUNCTION	LOC
41	P5			41	GND		
40	GND			40	GND		
39				39			
38				38			
37				37			
36	GND			36			
35				35			
34				34			
33				33			
32				32			
31				31			
30				30			
29	GND			29			
28				28			
27				27			
26	SCLR0	A		26	HW0	S	
25				25			
24	LSU1	A	NOTE 3	24	PFDT0	A	
23	SYN0	S		23	ATN0	S	
22	RACK0	A	NOTE 4	22	TACK0	S	
21	CL070	A		21	DA0	A	
20	DA0	A		20	CM00	A	
19	SA0	A		19	ADRS0	A	
18	D140	S/A		18	D150	S/A	
17	D120	S/A		17	D130	S/A	
16	D100	S/A		16	D110	S/A	
15	D080	S/A		15	D090	S/A	
14	D060	S/A		14	D070	S/A	
13	D040	S/A		13	D050	S/A	
12	D020	S/A		12	D030	S/A	
11	D000	S/A		11	D010	S/A	
10				10			
09				09			
08				08			
07				07			
06				06			
05				05			
04				04			
03				03			
02	2XLF	A		02			
01	GND			01	GND		
00	P5			00	GND		

NOTES 1. S - SENDER
A - RECEIVER
S/A - SENDER RECEIVER

2. SIGNALS TO BE WIRE WRAPPED - SLOTS 0 THRU 1

3. SIGNALS TO BE WIRE WRAPPED - SLOTS 0 THRU 3

4. USE JUMPER BLOCK PROVIDED WHEN JUMPER BLOCK IS NOT PROVIDED

REVISIONS

DFT/DES	
BLUSK	
DATE	
03/31/84	

DISKETTE - SCH01221

PERKIN-ELMER

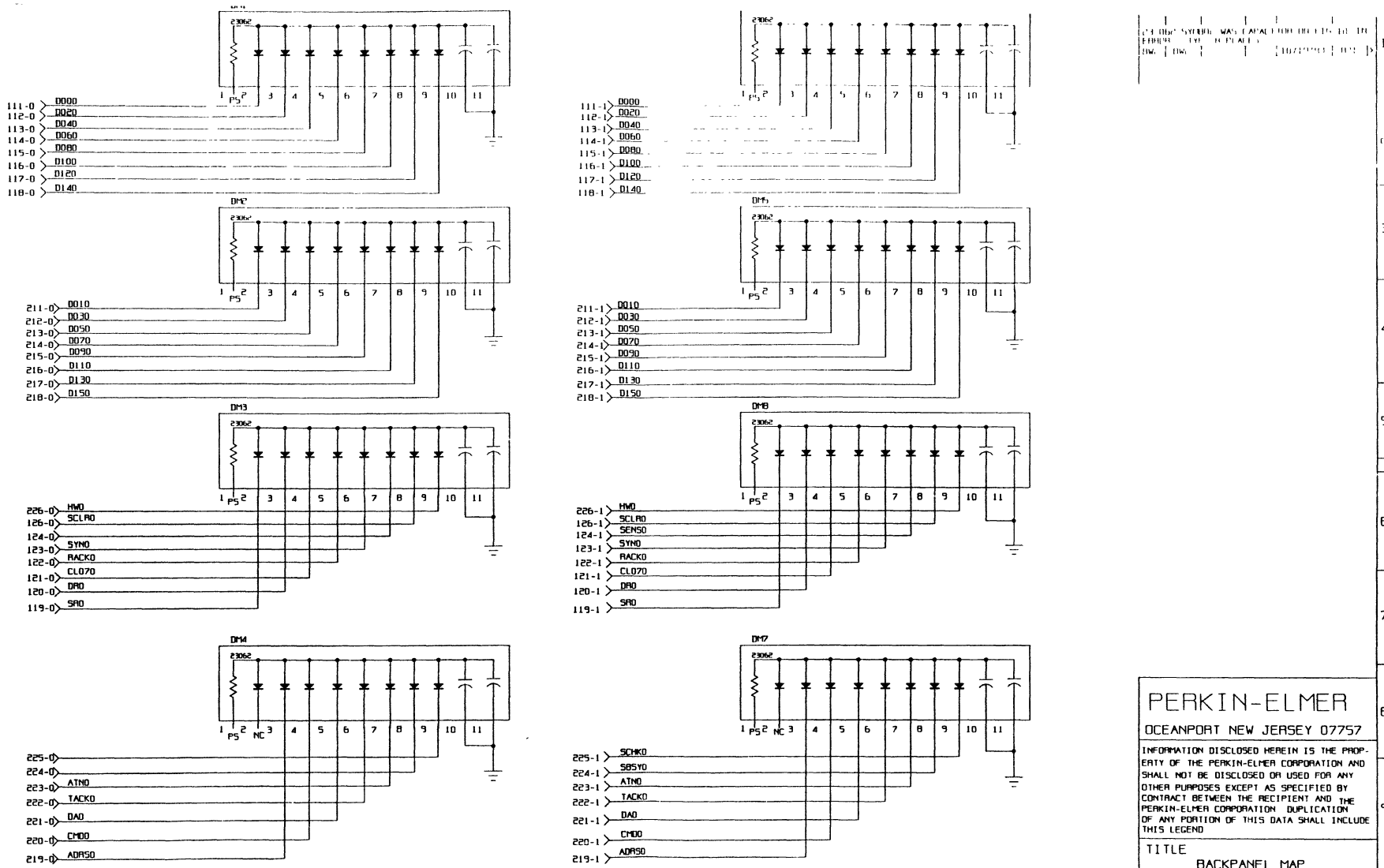
OCEANPORT NEW JERSEY 07757

TITLE

BACKPANEL MAP

CORSAIR II BACKPANEL

TASK	03017	SHT
DWG	35-897 D08	2 - 3



PERKIN-ELMER

OCEANPORT NEW JERSEY 07757

TITLE

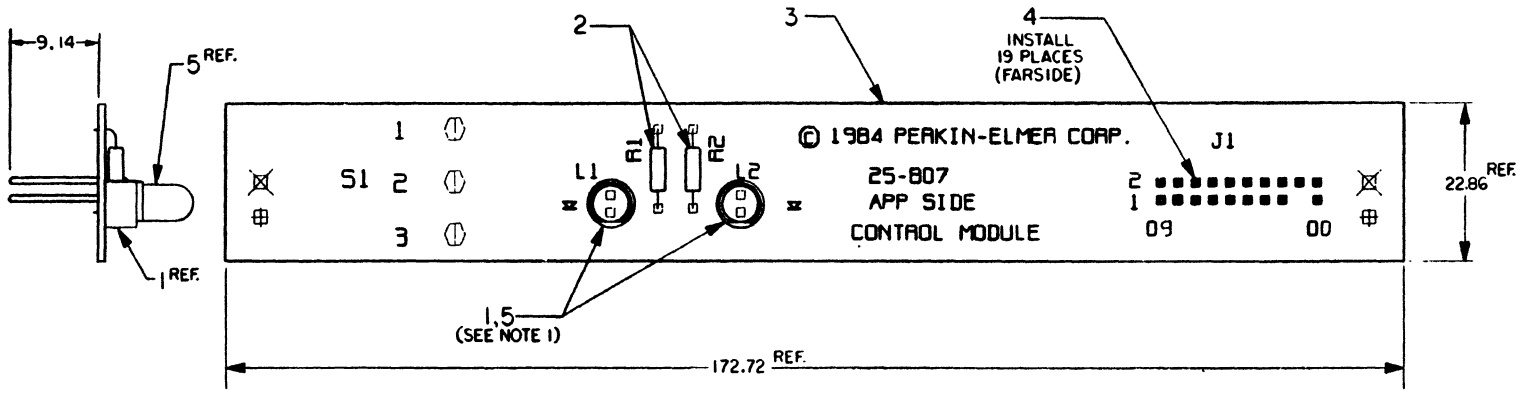
BACKPANEL MAP

CORSAIR II BACKPANEL

DFT/DES	
BLUSK	
DATE	
03/30/84	

TASK 03017	SHT
DWG 35-897 A01 D08	3 - 3

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
DEV		10-2-84			
PROD					
AREA H4 J1 PIN 09 WAS PIN 00 / PIN 00 WAS PIN 09. AREA A4 DIM. "9.14" WAS "7.87" AREA A7 "9.14" WAS "7.87" / ".360" WAS ".310".					
MF	JRB	5850	M	3-1-85	R01
AREA K6, MANUAL WAS "47-082" IN ERROR.					
MF	JRC	5921	D	6-4-85	R02



METRIC

USED IN MANUAL: 47-087

MILLIMETERS	INCHES
172.72	6.80
22.86	.900
9.14	.360

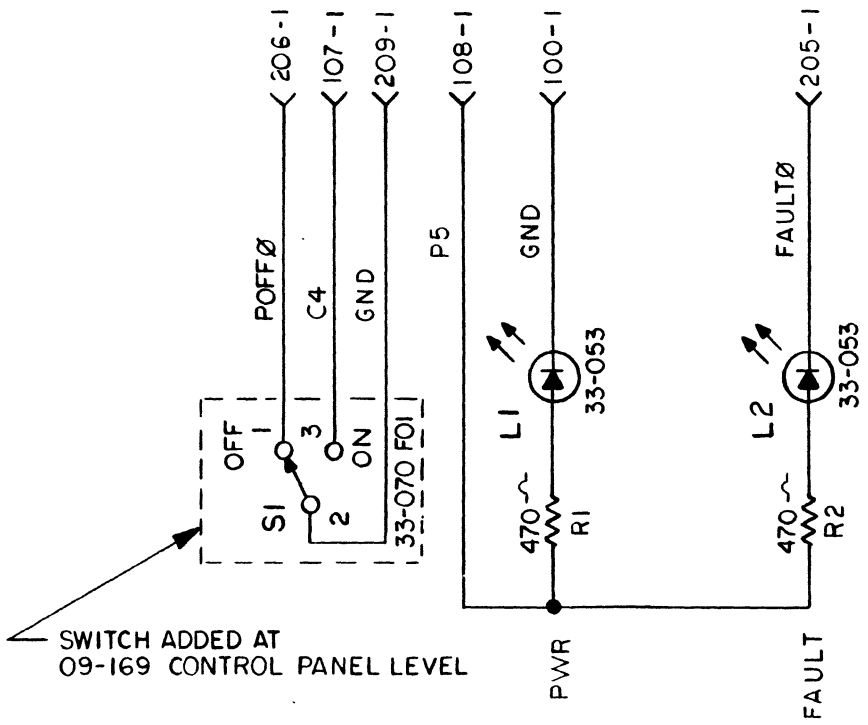
NOTES
1. FLAT SIDE & LONG LEAD INDICATES CATHODE END
2. FOR BOARD IDENTIFICATION SEE SSP 002-0D.

UNLESS OTHERWISE SPECIFIED			
SCALE: 2:1	TOLERANCE: MILLIMETERS	INCHES	
DIMENSIONS ARE IN INCHES/MILLIMETERS	X = ±.8 .X = ±.5 .XX = ±.13	.XXX = ±.005 .XX = ±.02 .X = ±.03	
NAME		TITLE	DATE
M. CAPRIO / WM. KITZ		DES / DFT	7-21-84
R. CERO		SUPV	8[illegible]-84
		CHK	
W. RICE / D. FOGGIA		ENG	
W. RICE		MGR	
R.A. BARKER		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
CONTROL MODULE
(CORSAIR II)

TASK	SHT
03356/03017	1-1
DWG 35-902 R02 C03	



USED IN MANUAL: 47-087

REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
	DEV				
	PROD				
AREA G8, BOARD 35-902 WAS R00.					
MF	JCC	5850	M	2-19-85	R01
AREA L8, MANUAL WAS "47-082" IN ERROR.					
MF	JCC	5921	D	6-4-85	R02

35-902	R01
BOARD	REV LEVEL
BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE REV LEVEL ABOVE	

UNLESS OTHERWISE SPECIFIED	
SCALE: ~	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°

NAME	TITLE	DATE
B.GRAY	DES / DFT	5-1-84
R.CERO	SUPV	
E.GREENSTEIN	TEST	
W.R'CHARD BOGGI	ENG	
W.RICE	MGR	
R.A.BARKER	QC	

NOTES

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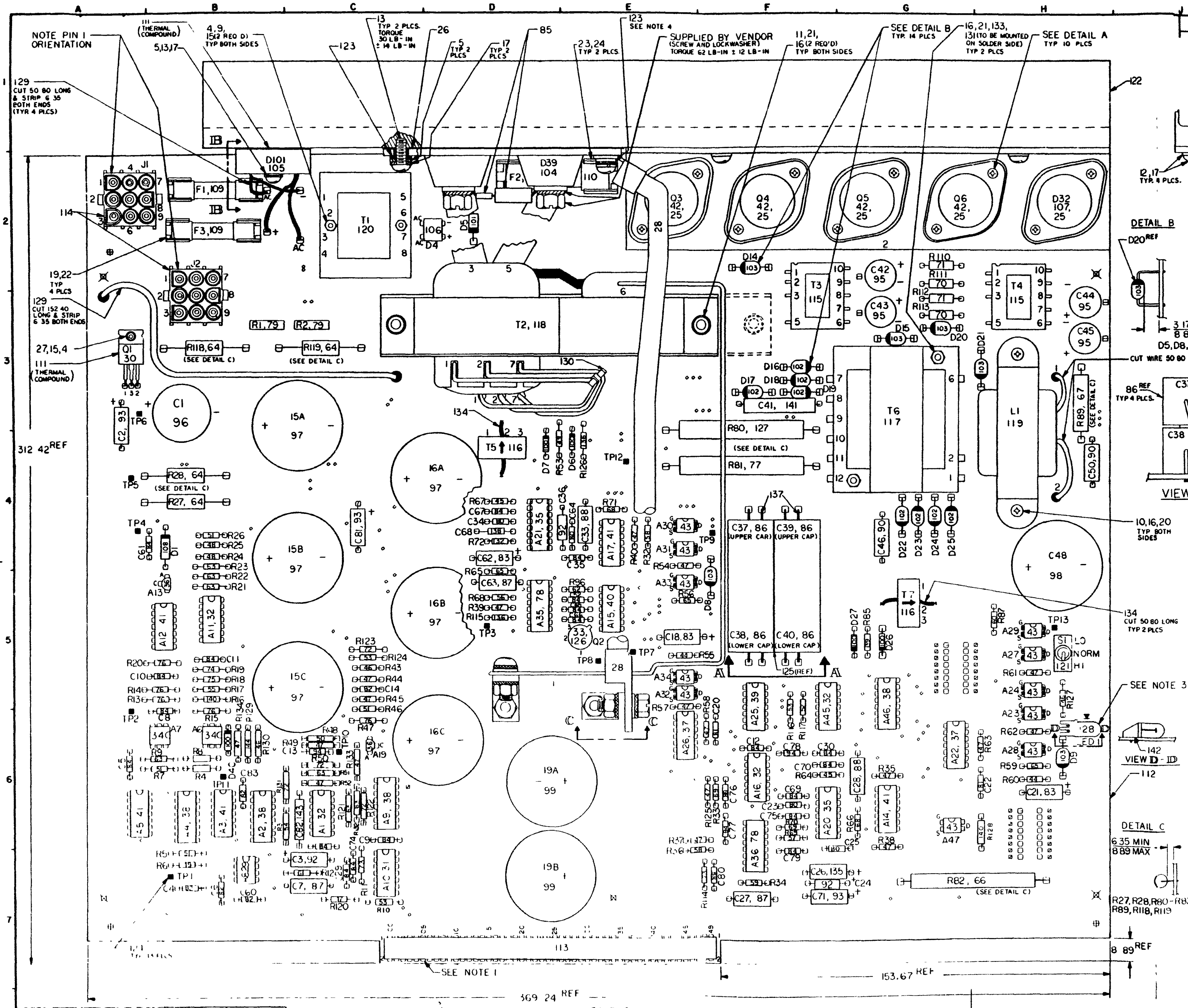
TITLE SCHEMATIC
CORSAIR II
CONTROL MODULE

TASK 03354/03017	SHT
DWG 35-902 R02 B08	1 - 1



USED IN MANUAL . 47-087

COMPONENT	REF. DESIGNATION
L.E.D	LED1
SWITCH	S1
TEST POINT	TP1-TP13
TRANSFORMER	T1-T7
RESISTOR	R110-R134, A35, A36 R80-R82, R85-R87, R89, R1-R28, R32-R40, R43-R72
TRANSISTOR	Q1-Q6, A23, A24, A27-A34, A47
INDUCTOR	L1
CONNECTOR	J1, J2
FUSE	F1-F3
DIODE	D1, D4-D9, D14-D27, D32, D39, D40, D101
CAPACITOR	C52, C60-C71, C74-C83, C1-C30 C33-C46, C48, C50,
INT CIRCUITS	A46 A1-A17 A19-A22, A25, A26, A45.

REFERENCE DESIGNATION CHART

NOTES:
1. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING
2. FOR BOARD IDENTIFICATION SEE SSP 002-OD

UNLESS OTHERWISE SPECIFIED

SCALE 2/1

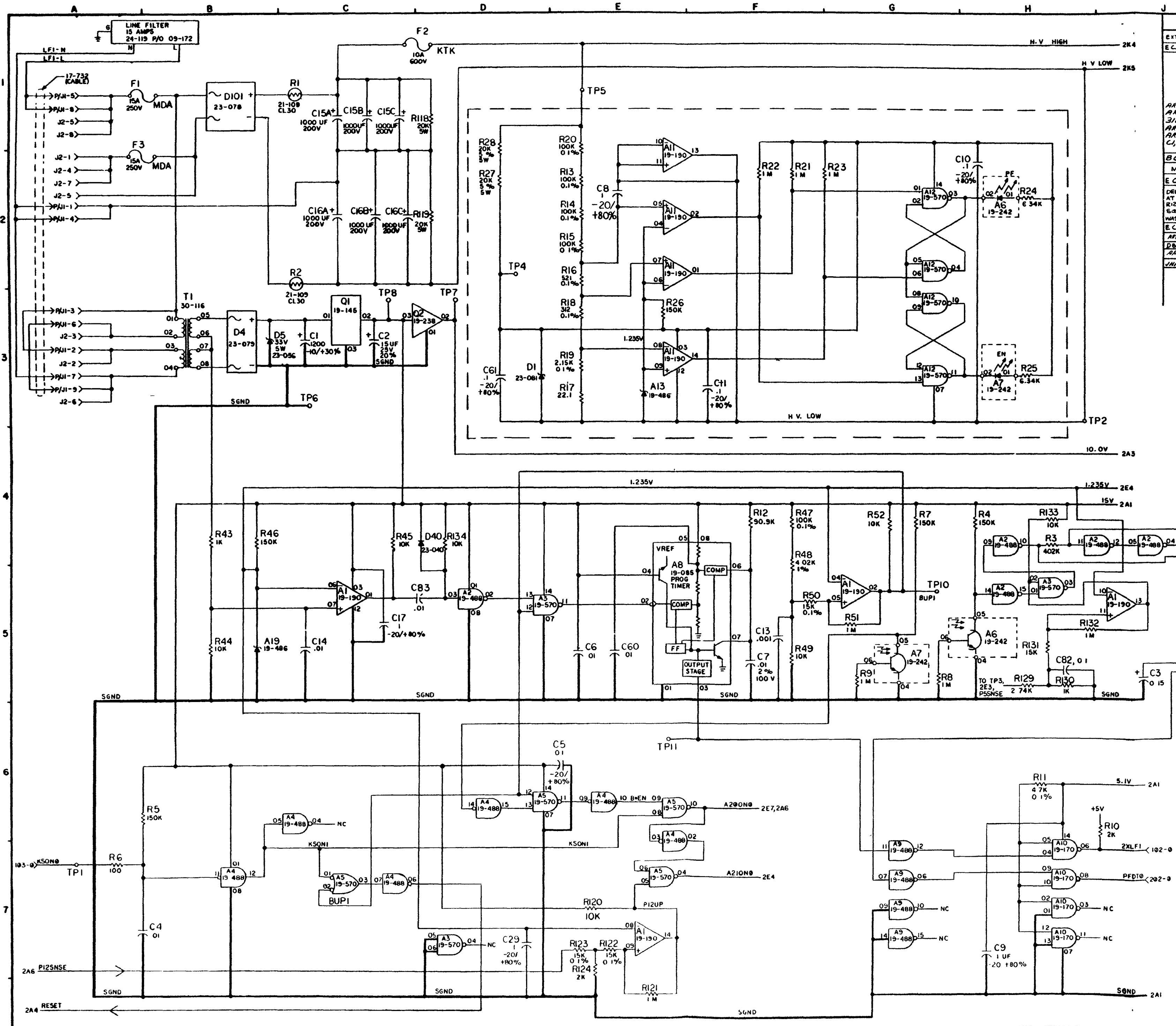
DIMENSIONS ARE IN INCHES

TOLERANCE	
MILLIMETERS	INCHES
XX ± 13 X ± 5 X ± 8	XXX ± 005 XX ± 02 X ± 03
ANGLES ± 1°	

NAME	TITLE	DATE
B LUSK / E JOHNSON	DES/DFT	10-24-84
R CERO	SUPV	11-13-84
H BRION	ENG	
E CENTOFANTI	MGR	
R A BARKER	QC	

Concurrent Computer Corporation
Oceanport, N.J 07757

TITLE ASSEMBLY DRAWING
3203
POWER BOARD



8 NOTES

REVISIONS

EXT CHG'S - DELETED PSU CIRCUITRY. REVISED SHT 2.

E.C.J.	[signature]	—	—	10-1-84	R01

PRE PRODUCTION APPROVAL	DEV	INIT H.B.A.	DATE 11/15/84

AREA D8, ADDED C29; AREA F5, ADDED C13; AREA H4, R3 WAS 200K; AREA E3, R16 WAS 312 OHMS; AREA H6 R10 WAS NOT SPECIFI... AREA F6, ADDED X-REF "2A6" TO "A2ØONØ"... AREA A1 & B1, ADDED "250V" TO F1 & F3; AR... C1, ADDED "600V" TO F2; REVISED SHEET...

BG	JRO	5839	M	3-19-85	R0.

MANUAL NO AT K5 47-082. SHT. LEV AT H6 WA...

E.C.J.	JRO	5921	D	3-29-85	R0

DELETED GATE A3-03 AT D7. DELETED GATE A1-13 AT A5... AT H5, ADDED GATES A3-03, A1-13, A2-15, R133, R132, R... R129, R130, C82 & REVISED CIRCUITRY. A2-14 WAS CONN... SGND. A2-09 WAS CONN TO A6-05. AT H8, REV. LEVEL OF... WAS R03, SHT 2 WAS R02.

E.C.J.	JRO	5971	M	4-1-85	R0

AREA H8, 35-303 WAS R05. REVISED SHTS 1 & 2

DB	JRO	6118	MS	8-23-85	R0

AREA D4 ADDED D40, C83 & R134. R45 WAS 150K

JHN	JRO	6654	M	11-21-86	R0

USED IN MANUAL: 47-087

UNLESS OTHERWISE SPECIFIED

SCALE NONE	TOLERANCE
DIMENSIONS ARE IN INCHES	XXX ±.005 .X ±.03 XX ±.02 ANGLE

NAME		TITLE	DA
B. LUSK	E. JOHNSON	DES/DFT	8-18
R. CERO		SUPV	10-2
E. GREENSTEIN		TEST	
H. BRION		ENG	
E. CENTOFANTI		MGR	
R. A. BARKER		QC	

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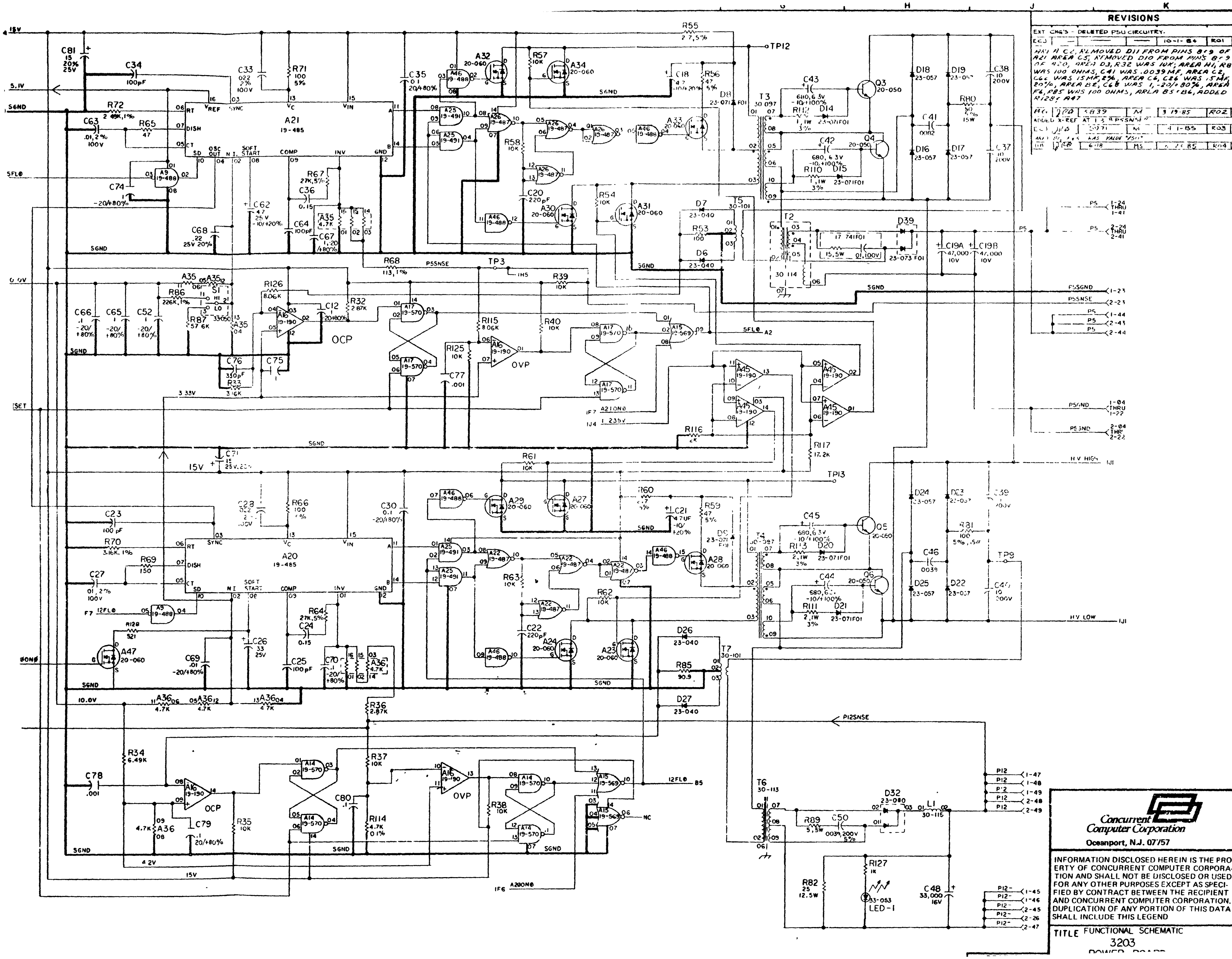
Oceanport, N.J 07757

TITLE FUNCTIONAL SCHEMATIC 3203 POWER BOARD

REVISION LEVEL		BOARDS AGREEING WITH SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL	
SHT 1	R06	BOARD	REVISION LEVEL



REVISIONS

EXT CHG'S - DELETED PSU CIRCUITRY.

ECJ	—	——	——	10-1-84	R01

AREA A C2, REMOVED D11 FROM PINS 8 & 9 OF A21 AREA C5, REMOVED D10 FROM PINS 8 & 9 OF A20, AREA D3, R32 WAS 10K; AREA H1, R80 WAS 100 OHMS, C41 WAS .0039 MF, AREA C2, C66 WAS 15MF, 2%, AREA C6, C26 WAS 15MF, 20%, AREA B2, C68 WAS 1, -20/+80%, AREA F6, R85 WAS 100 OHMS, AREA B5 & B6, ADDED R128 & A47

BG	JPA	5839	M	3-19-85	R02

ADDED X-REF AT F3 "P5SNSE"

ECJ	JPA	5971	M	4-1-85	R03

AREA B1, R75 WAS VALUE "150"

DB	JPA	6118	MS	6-28-85	R04

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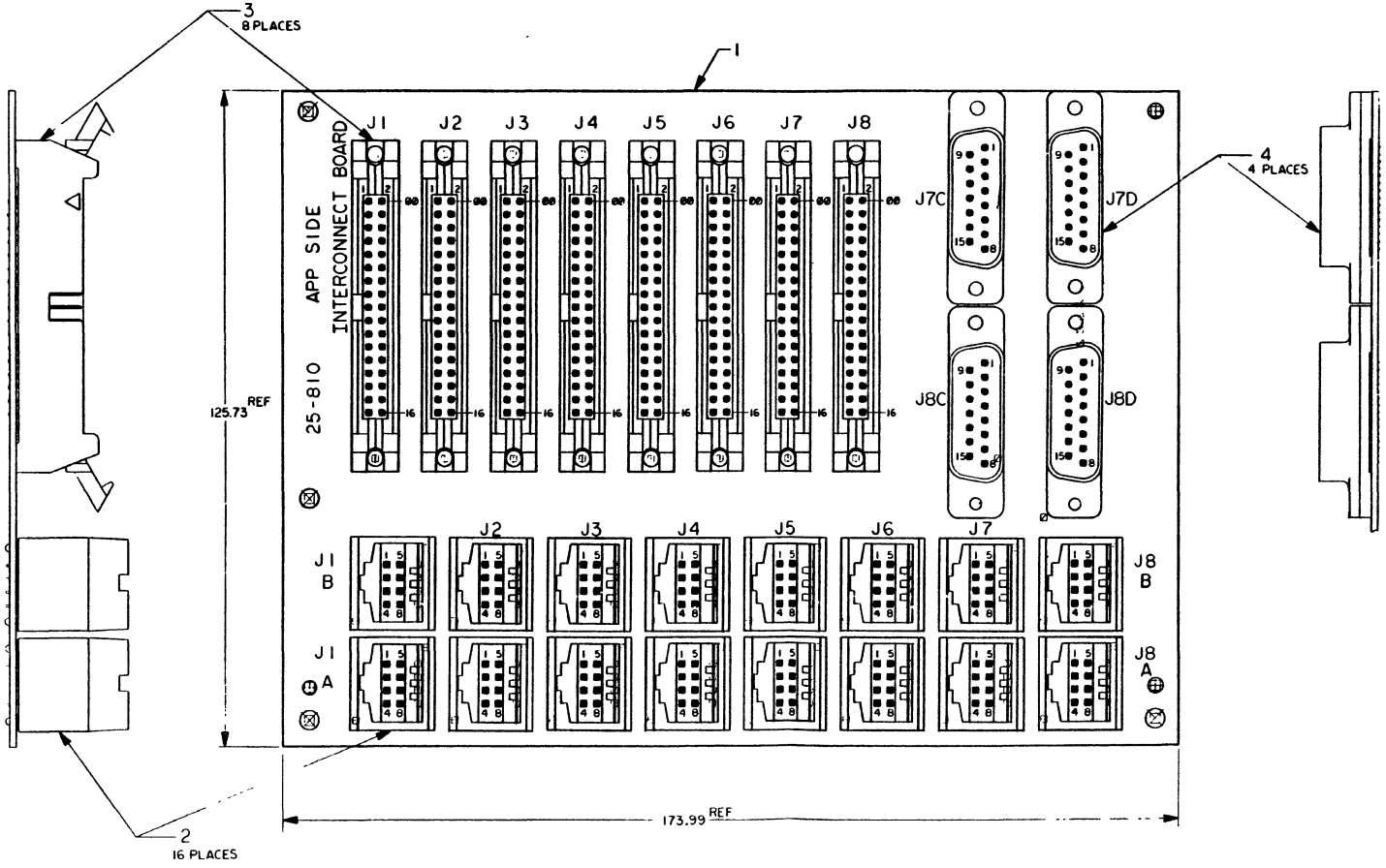
TITLE FUNCTIONAL SCHEMATIC
3203
POWER BOARD



MILLIMETERS	INCHES	COMPONENT	REF. DISIGNATIONS
173 99	6.850	JACKS	J1-J8, J7C, J7D, J8C, J8D,
125 73	4 950		J1A-J8A, J1B-J8B

NOTES 1 FOR BOARD INDENTIFICATION SEE SPP 002-00

REVISIONS

PRE PRODUCTION APPROVAL	INI
	DEV
	PROD

AREA NO. MANUAL NO WAS 47
MF | JTC | 5921 | D

METRIC

USED IN MANUAL: 47

UNLESS OTHERWISE

SCALE: 2:1	TOLE
DIMENSIONS ARE IN INCHES/MILLIMETERS	METR X ±.8 .X ±.5 .XX ±.13 ANGLES

NAME		T
M. CAPRIO	WM. KITZ	DES
R. CERO		S
D. FOGGIA		
W. RICE		
R.A. BARKER		

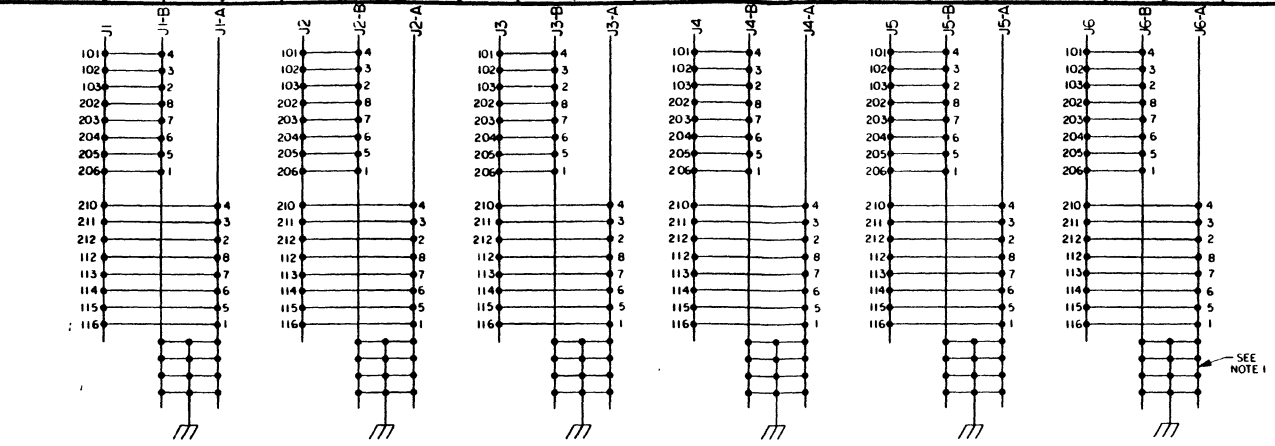
PERKIN-E

Computer Systems Divi
Oceanport, N.J. 07757

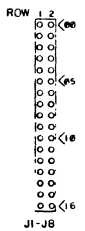
TITLE

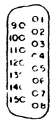
INTERCONNECT E
CORSAIR II

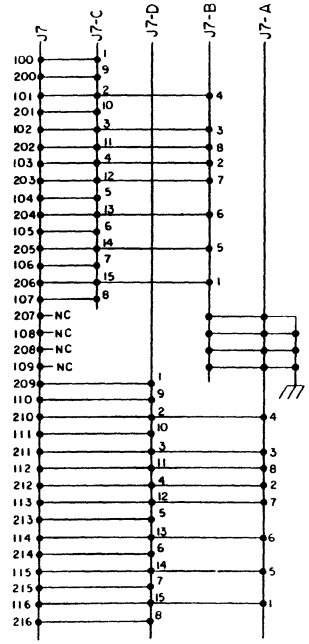
TASK 03354/03018

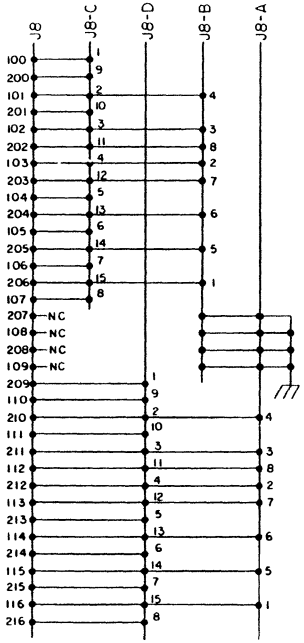


CONNECTORS
VIEWED FROM PCB APPARATUS SIDE









REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	

AREA NO MANUAL NO WAS 47-08L IN ERROR
MF | | 3241 | D | 4.17.85 | R01

USED IN MANUAL: 47-087

UNLESS OTHERWISE SPECIFIED	
SCALE: NONE	TOLERANCE:
DIMENSIONS ARE IN INCHES	.XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°

NAME		TITLE	DATE
M.CAPRIO	K.REED	DES/DFT	7-30-84
R.CERO		SUPV	
		CHK	
W.RICE / D.FOGGIA		ENG	
W.RICE		MGR	
R.BARKER		QC	

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Computer Systems Division
Oceanport, N.J. 07757

TITLE
INTERCONNECT BOARD
CORSAIR II

TASK 03354/03018	SHT
DWG 35-907 R01 D08	1-1

NOTES
1. FOUR PINS ARE CONNECTED TO FRAME OF CONNECTORS J1A/B THRU J8A/B

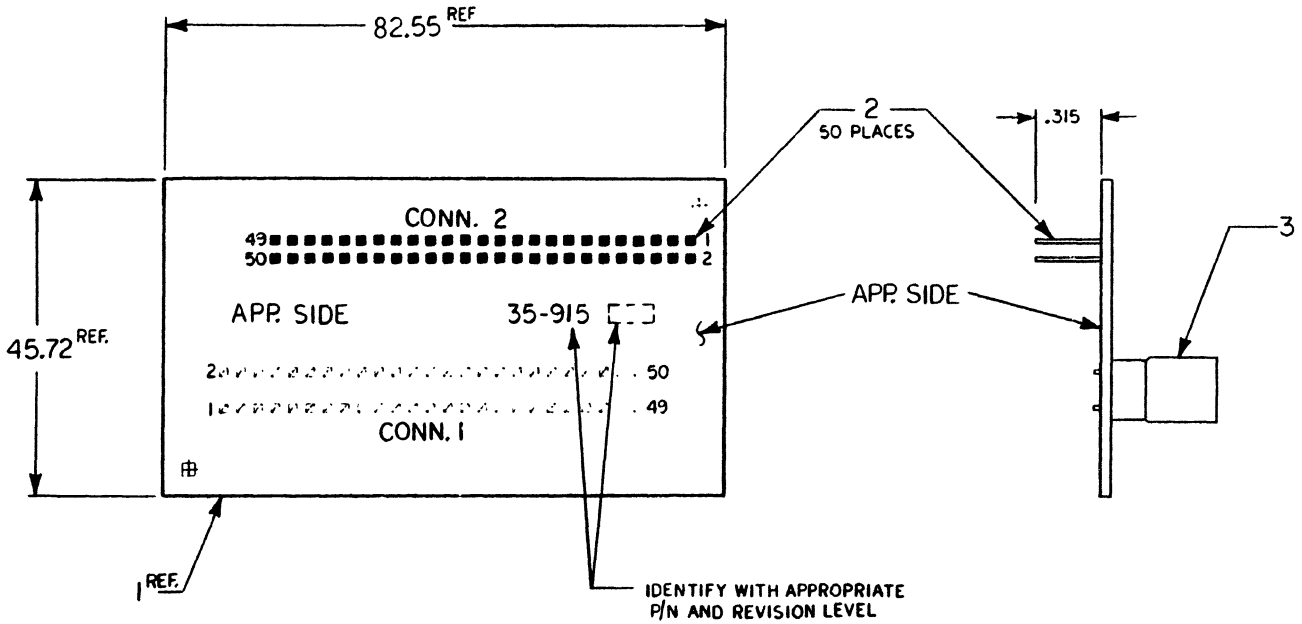
35-907	R00
BOARD	REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	11-5-84
	PROD	

AREA K6, MANUAL NO. WAS 47-082 IN ERROR.

MF	JMP	5921	D	4-17-85	R01



USED IN MANUAL 47-087

45.72	1.800
82.55	3.250
MILLIMETERS	INCHES

NOTES

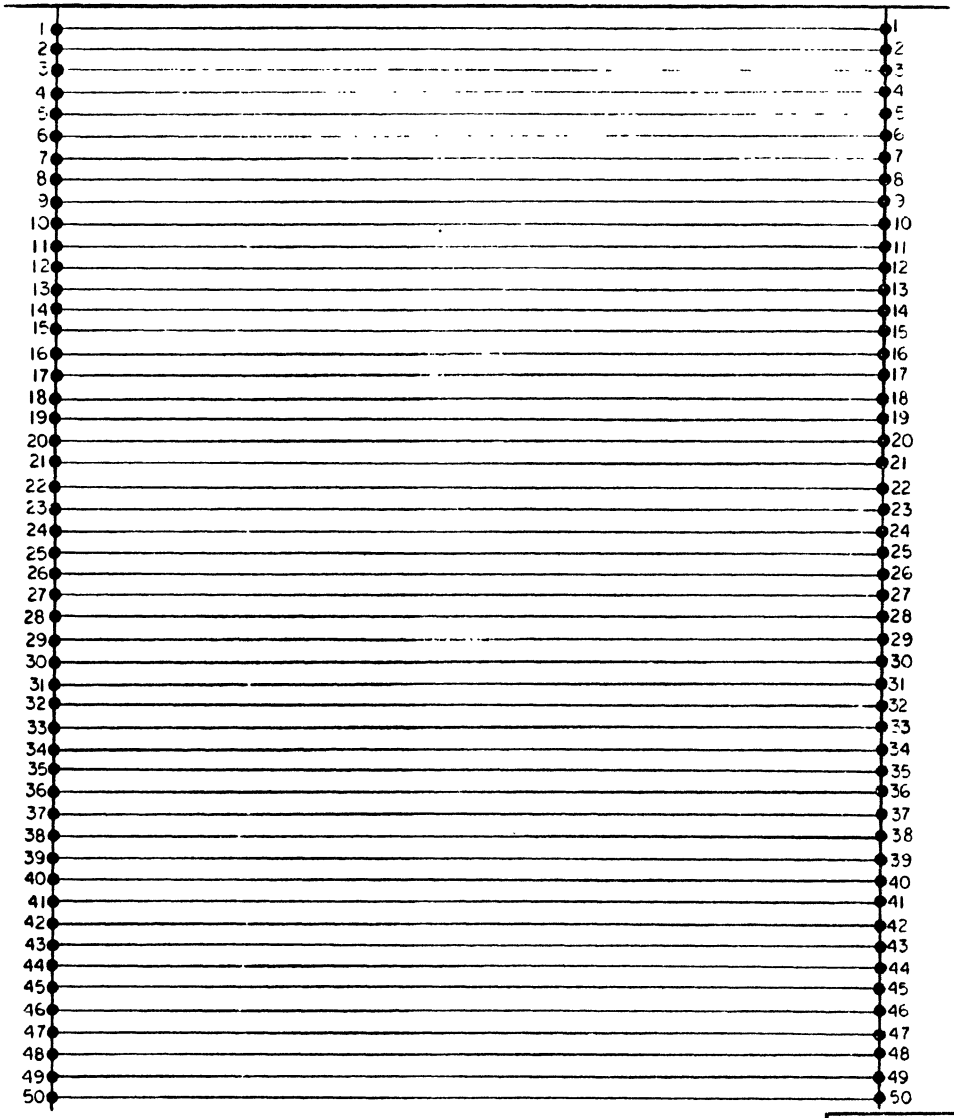
UNLESS OTHERWISE SPECIFIED			
SCALE: 2:1	TOLERANCE: .XXX ± .005 .X ± .03 .XX ± .02 ANGLES ± 1°		
DIMENSIONS ARE IN INCHES			
NAME		TITLE	DATE
V. PERRI		DES / DFT	10-17-84
R. CERO		SUPV	
		CHK	
D. FOGGIA		ENG	
P. ABITANTE		MGR	
R.A. BARKER		QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE PRINTED CKT. ASSY.
CONN. TRANSITION BOARD
CORSAIR II

TASK 03018 SHT

DWG 35-915 R01 C03 1 - 1



REVISIONS					
PRE PRODUCTION APPROVAL	INIT	DATE			
DEV		11-8-84			
PROD					
AREA K6, MANUAL WAS 47-082 IN ERROR					
MF	5921	D	4 17 85	R01	

USED IN MANUAL 47-087

35-915	R00
BOARD	REV LEVEL

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

NOTES

UNLESS OTHERWISE SPECIFIED		
SCALE: ~	TOLERANCE:	
DIMENSIONS ARE IN INCHES	.XXX ± 005 .XX ± .02	.X ± .03 ANGLES ± 1°

NAME	TITLE	DATE
V. PERRI	DES / DFT	10-17-84
R. CERO	SUPV	
	CHK	
D. FOGGIA	ENG	
P. ABITANTE	MGR	
R. A. BARKER	QC	

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE FUNCTIONAL SCHEMATIC
CONN. TRANSITION BOARD
CORSAIR II

TASK 03018 SHT 1 - 1
DWG 35-915 R01 C08