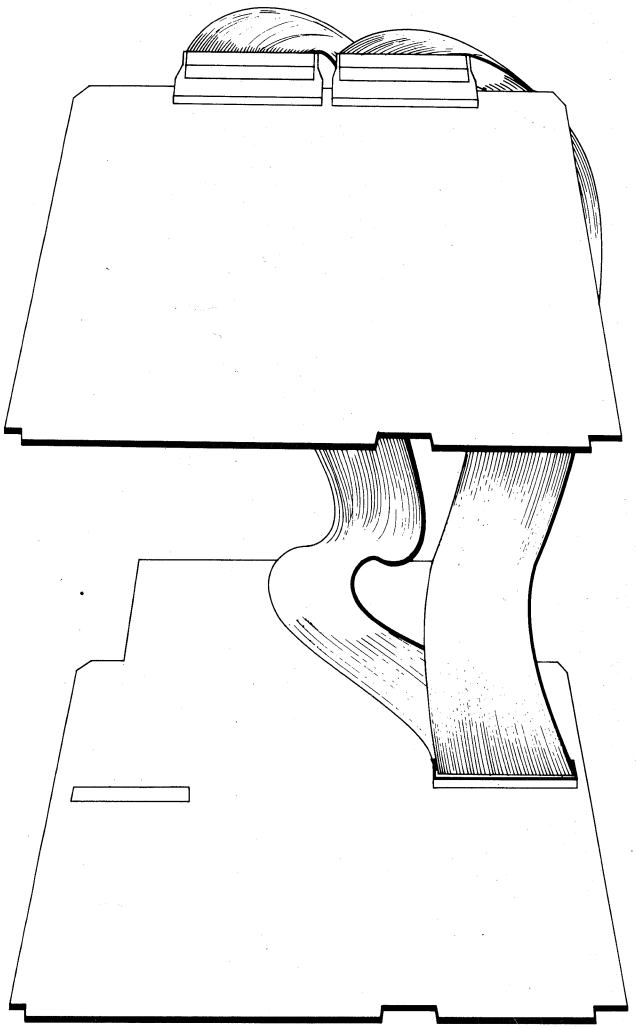
iSBC® 386/20P SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 148550-001

iSBC® 386/20P
SINGLE BOARD COMPUTER
HARDWARE REFERENCE MANUAL

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CAUTION

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A Computing Device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

PREFACE

AUDIENCE AND PURPOSE

This manual is written for hardware and software engineers who will install, configure, or troubleshoot the iSBC® 386/20 board. Knowledge of the 80386 microprocessor and its family of support chips, as well as the MULTIBUS® architecture, will help in understanding the board's operation.

RELATED PUBLICATIONS

This manual references information contained in these publications:

- iSBC 386/20 Starter Kit Overview and Installation Manual, Order Number: 148549.
- iAPX 386 Data Sheet, Order Number: 231630.
- iAPX 286 Operating Systems Writer's Guide, Order Number: 121960.
- Intel Microsystem Components Handbook, Order Number: 230843.
- Intel Memory Components Handbook, Order Number: 210830.
- Intel MULTIBUS Specification, Order Number: 980683.
- Intel iSBX™ Bus Specification, Order Number: 142686.
- EIA Standard for RS-232C Interfacing, EIA-RS-232C.

You may also find these Intel publications helpful:

- iAPX 386 Product Briefs Handbook, Order Number: 231635.
- Guide to Configuring MULTIBUS-Based Systems, Order Number: 144788.
- OEM Systems Handbook, Order Number: 210941.
- Solutions Magazine, Order Number: 231135.

These and other Intel publications are listed in Intel's Literature Guide, Order Number: 210621. See page ii for the ordering address.

NOTATIONAL CONVENTIONS

This manual uses two special characters, the asterisk (*) and the section symbol (§):

- * Used after a signal mnemonic to indicate that the signal is active-low. Signal mnemonics without a trailing asterisk are active-high. The asterisk replaces the slash (/) used previously to indicate the active state of a signal.

- § Used after a jumper connection to indicate a factory-installed jumper (default configuration).

You will encounter **NOTES**, **CAUTIONS**, and **WARNINGS** throughout this manual. Notes emphasize information for special consideration. Cautions indicate possible errors that could result in software or hardware damage. Most importantly, warnings indicate a possibility of personal injury.

ORGANIZATION OF THIS MANUAL

This section provides a short abstract of each chapter and appendix.

CHAPTER 1. GENERAL INFORMATION

This chapter provides a brief overview of the features of the 80386 CPU and the iSBC 386/20P Single Board Computer. The chapter also summarizes the board's specifications.

CHAPTER 2. BOARD OPERATION

This chapter provides a brief description of the board's operation based on its block diagram.

CHAPTER 3. BOARD PREPARATION AND INSTALLATION

This chapter supplies information to help you prepare the board for installation. It provides a list of user-supplied components and equipment you may need.

CHAPTER 4. CONFIGURATION

This chapter contains jumper and programming information for each configurable or programmable feature of the board.

CHAPTER 5. SERVICE INFORMATION

This chapter provides service and repair assistance instructions for the board.

APPENDIX A. JUMPER AND DEFAULT INFORMATION

This appendix consolidates all the jumper information so you can use it for quick reference. It shows the jumper locations, explains jumper functions, and provides a jumper index for the iSBC 386/20P board's schematic.

APPENDIX B. MEMORY BOARD INFORMATION

This appendix provides the default jumper configurations for the iSBC 402P and 404P memory boards. The jumpers are factory set and are not user-configurable.

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CONTENTS

CONTENTS

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC® 386/20P Single Board Computer (Figure 1-1) is the first 80386-based board product in the MULTIBUS® product line. The "P" designates it as an early release version of the iSBC 386/20 board. The iSBC 386/20P board, the 80287 Math Module, and an iSBC 402P (2M-byte) or 404P (4M-byte) memory board all combine to form a "virtual single board computer," meaning that numeric calculations and memory accesses are as fast as if they were on-board. These products plus monitor software are included in the iSBC 386/20 Starter Kit (more information about the kit is supplied in the iSBC 386/20 STARTER KIT OVERVIEW AND INSTALLATION MANUAL).

This manual provides or references the information necessary to configure and use the iSBC 386/20P board, 80287 Math Module, and iSBC 402P or 404P memory board. This chapter provides a brief overview of the 386/20P board's features and specifications.

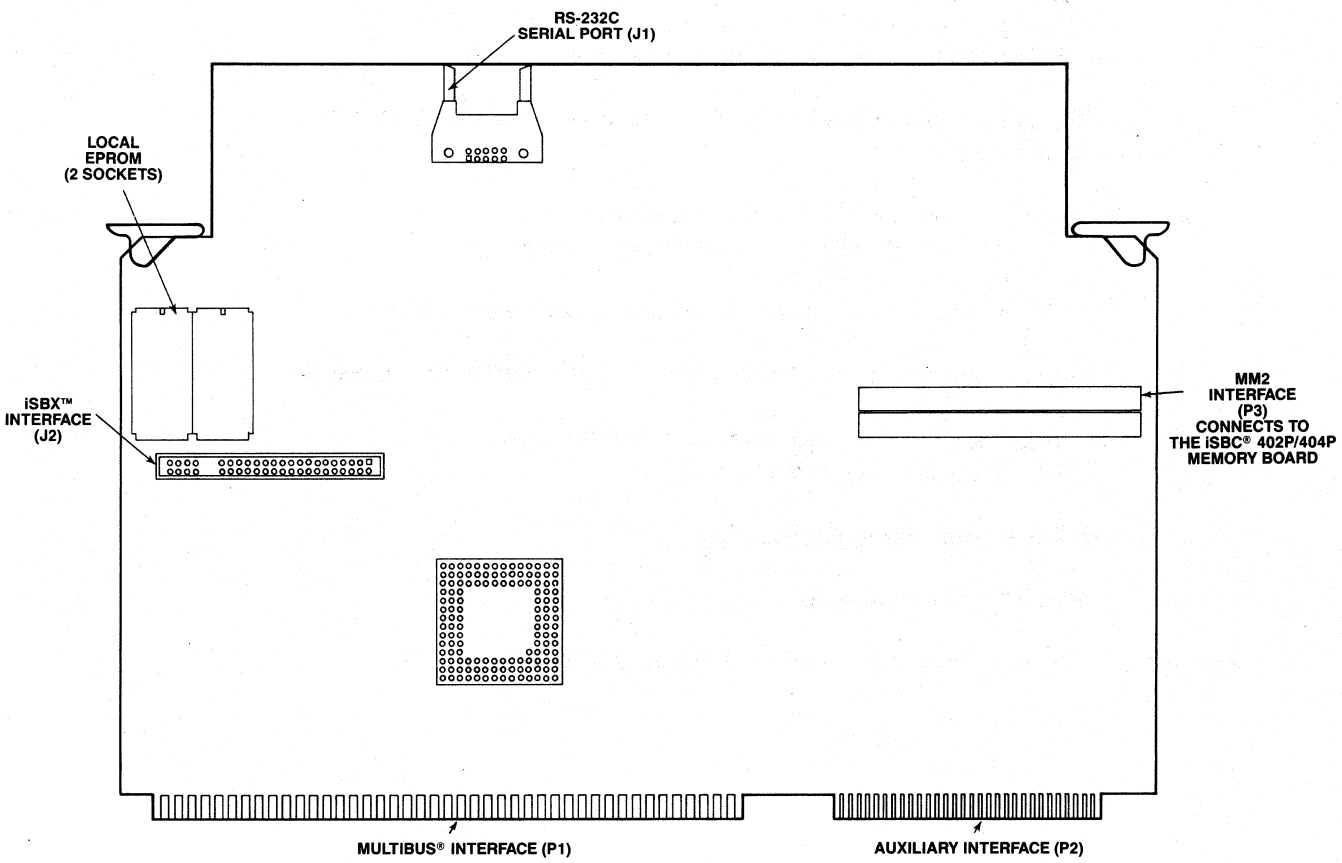


Figure 1-1. iSBC® 386/20P Single Board Computer 2326

The board uses the iSBX™ and MULTIBUS interface standards with their wide product support while it decouples the 80386 from those buses to take advantage of its higher performance.

The 386/20P board can boost performance in applications originally designed for Intel's other 16-bit single board computers (e.g., the iSBC 286/10A and iSBC 286/12 boards, refer to Section 2.3). With this compatibility, performance can be improved without requiring major hardware or software changes.

1.2 80386 CPU FEATURES

The 80386 is Intel's first true 32-bit microprocessor (32 address lines and 32 data lines). Here are the chip's major features:

- High performance
  - -- 12 MHz and 16 MHz clock speeds
  - -- 2 times the performance (at 16 MHz) of an 8 MHz 80286 CPU
  - -- Pipelined instruction execution
  - -- 8-, 16-, and 32-bit data
  - -- Multiple on-chip caches
  - -- Integrated multitasking capability
  - -- On-chip virtual memory capability
- Software compatibility with the 8086/88/186/188/286 microprocessors
- Complete support for 32-bit addressing
  - -- 2^{32} bytes of physical address space
  - -- 2^{32} bytes per segment
  - -- 2^{46} bytes of virtual address space per task
- Numeric coprocessor extension (80387 NPX) interface
- On-chip memory management and protection
  - -- Fully compatible with 80286
- Optional on-chip paging
- CHMOS III technology

For detailed information, refer to the 80386 data sheet.

1.3 iSBC® 386/20P BOARD FEATURES

In addition to the CPU's features, the iSBC 386/20P board has these features:

- Complete memory support
  - -- Two EPROM sites supporting up to 128K bytes
  - -- 2M bytes (with the iSBC 402P board) or 4M bytes (with the iSBC 404P board) of local DRAM, which can be dual-ported between the 386/20P board and other MULTIBUS masters
  - -- 16K bytes of cache memory
  - -- DRAM byte parity generation and checking

- High-performance DRAM reads and writes
  - -- 0 wait-state read hit from cache
  - -- 2 wait-state read miss or write with address pipelining
  - -- 3 wait-state read miss or write without address pipelining

- Industry-standard interfaces
  - -- MULTIBUS interface using the full memory and I/O address space
  - -- iSBX interface supporting 8- or 16-bit I/O
  - -- A 10-pin connector utilizing the 9-pin IBM PC standard RS-232C DTE asynchronous interface

- Peripheral support
  - -- Two programmable timers for generating interrupts
  - -- A programmable timer for generating the serial port's baud rate
  - -- One programmable RS-232C serial port
  - -- Numeric coprocessing with the 80287 NPX math module

- Hardware support
  - -- On-board control registers for signaling errors, configuring the board, and reporting board status
  - -- Two programmable interrupt controllers providing a total of 15 interrupts, 13 of which are jumper configurable

1.4 COMPATIBLE EQUIPMENT

The iSBC 386/20P board is designed to operate as either a master or an intelligent slave with other single board computers on the MULTIBUS interface. It also interfaces with any 8- or 16-bit iSBX MULTIMODULE™ board. Refer to the MULTIBUS SPECIFICATION for more information specific to the MULTIBUS system architecture.

The 386/20P board provides an asynchronous RS-232C DTE serial port. It can be directly connected to a DCE interface, or it can be modified by cabling to connect to a DTE interface. Its pinout supports the IBM PC standard when using a 10-pin to 9-pin DCE ribbon cable assembly (user-supplied). The starter kit supplies a 10-pin to 25-pin DTE ribbon cable assembly for interfacing the 386/20P board to a host terminal.

The 386/20P board has two 28-pin JEDEC sockets that accept 32Kx8 or 64Kx8 components. The sockets can be configured for three to six wait-states (allowing EPROMs with access times from 130 nsec to 320 nsec).

The 386/20P board requires an iSBC 402P or 404P memory board for providing local and dual-port DRAM. The 386/20P board connects to the 402P and 404P memory board through the MM2 interface cables. The starter kit supplies the memory board and connecting cables.

1.5 BOARD SPECIFICATIONS

Table 1-1 summarizes the specifications for the board.

Table 1-1. Specifications

CPU	80386 32-bit microprocessor
WORD SIZE	
Data:	8-, 16-, and 32-bit
Physical Addressing:	2^{32} bytes
Virtual Addressing:	2^{46} bytes per task
PERFORMANCE	
Clock Speed:	12 MHz or 16 MHz
Instruction Execution Time at 16 (12) MHz:	250 (333) nsec 125 (167) nsec, instruction in queue

(continued)

Table 1-1. Specifications (continued)

MEMORY	
Local EPROM:	Two 28-pin JEDEC sockets (holds 64K or 128K bytes)
Local and dual-port DRAM:	iSBC 402P board (2M bytes) or iSBC 404P board (4M bytes)
PHYSICAL CHARACTERISTICS	
Width (left to right):	30.5 cm (12.00 in)
Length (front to back):	22.2 cm (8.7 in)
Depth (top to bottom):	3.6 cm (1.4 in) with the MM2 bus cable attached
Weight:	216 gm (6 oz)
ENVIRONMENTAL REQUIREMENTS	
Operating Temperature:	0°C to 55°C with airflow at 200 linear feet/minute
Relative Humidity:	Up to 90%, noncondensing
INTERFACE COMPLIANCE LEVELS	
MULTIBUS Compliance:	MASTER D16 M24 I16 V023 L
iSBX Bus Compliance:	D16/16 I
I/O CAPABILITY	
Serial:	One 10-pin RS-232C DTE serial port (supports nine leads: GND, RI, DTR, CTS, TD, RTS, RD, DSR, CD)
I/O Expansion:	One iSBX interface for local bus expansion Supports an 8- or 16-bit iSBX MULTIMODULE board
SERIAL COMMUNICATIONS CHARACTERISTICS	Supports the following modes of the 8251A PCI:
Asynchronous:	5- to 8-bit characters; break character generation; 1, 1-1/2, or 2 stop bits; false start-bit detection, even or odd parity
Baud Rate:	From 75 Hz to 38.4 KHz

(continued)

Table 1-1. Specifications (continued)

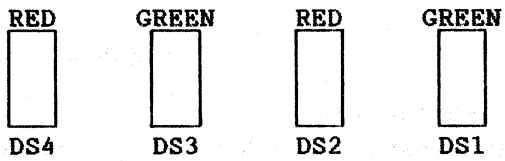
ELECTRICAL CHARACTERISTICS

DC Power Requirements:

Voltage Maximum	Amperage 80% WCCP/Maximum	Wattage*	BTU*	Gram-Calories*
+ 5.25	13.5/16.8	70.6	4.1	1005
+ 12.6	0.8/1.1	8.9	0.5	126
- 12.6	0.8/1.1	8.9	0.5	126

VISUAL INDICATORS

LED Layout



Red LED (DS4) — Parity Error LED. Turned on by a DRAM parity error; turned off by writing any value to the register (I/O address 00E8H). See Section 4.3.5 for details.

Green LED (DS3) — Programmed Status Latch LED. Controlled by your software. Odd data (written to I/O address 00E4H) will turn it on; even data will turn it off. See Section 4.3.5 for details.

Red LED (DS2) — Time-out LED. Turned on by a MULTIBUS or iSBX time-out; turned off by writing any value to the register (I/O address 00E2H). See Section 4.3.5 for details.

Green LED (DS1) — Run LED. Stays on during 80386 CPU bus cycles; goes off if a HALT occurs.

* At 80% worst case calculated power (WCCP) current levels.

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CHAPTER 2
BOARD OPERATION

2.1 INTRODUCTION

This chapter provides an overview of the board's operation. Each functional area of the board is shown in the block diagram and then briefly explained. Refer to Chapter 4 for configuration information.

2.2 BLOCK DIAGRAM EXPLANATION

A block diagram of the iSBC 386/20P board is shown in Figure 2-1. The following sections describe each of the functional units of the block diagram, in this order:

- Processor Section
- Memory Section
- Controller Section
- I/O Section
- Interface Section

2.2.1 PROCESSOR SECTION

This section consists of the Central Processor Unit (80386 CPU), 80287 math module, clock circuits, and buffers.

2.2.1.1 80386 CPU

The 80386 CPU extends the features of the 80286 CPU. It is enhanced to provide 4 gigabytes of physical address space and a 32-bit data path. The 386/20P board comes with either a 12 MHz or 16 MHz CPU. The 12 MHz CPU uses a 24 MHz clock, and the 16 MHz CPU uses a 32 MHz clock.

The 80386 processor operates in one of two modes: Real Address mode or Protected Virtual Address Mode (PVAM). PVAM can run in either paged or nonpaged mode. The CPU automatically operates in Real Address mode after power-up or reset; you can then switch to PVAM by performing a mode switch (Section 4.3.5.1 explains how). The differences between the two modes are quite significant. For more information, refer to the 80386 DATA SHEET.

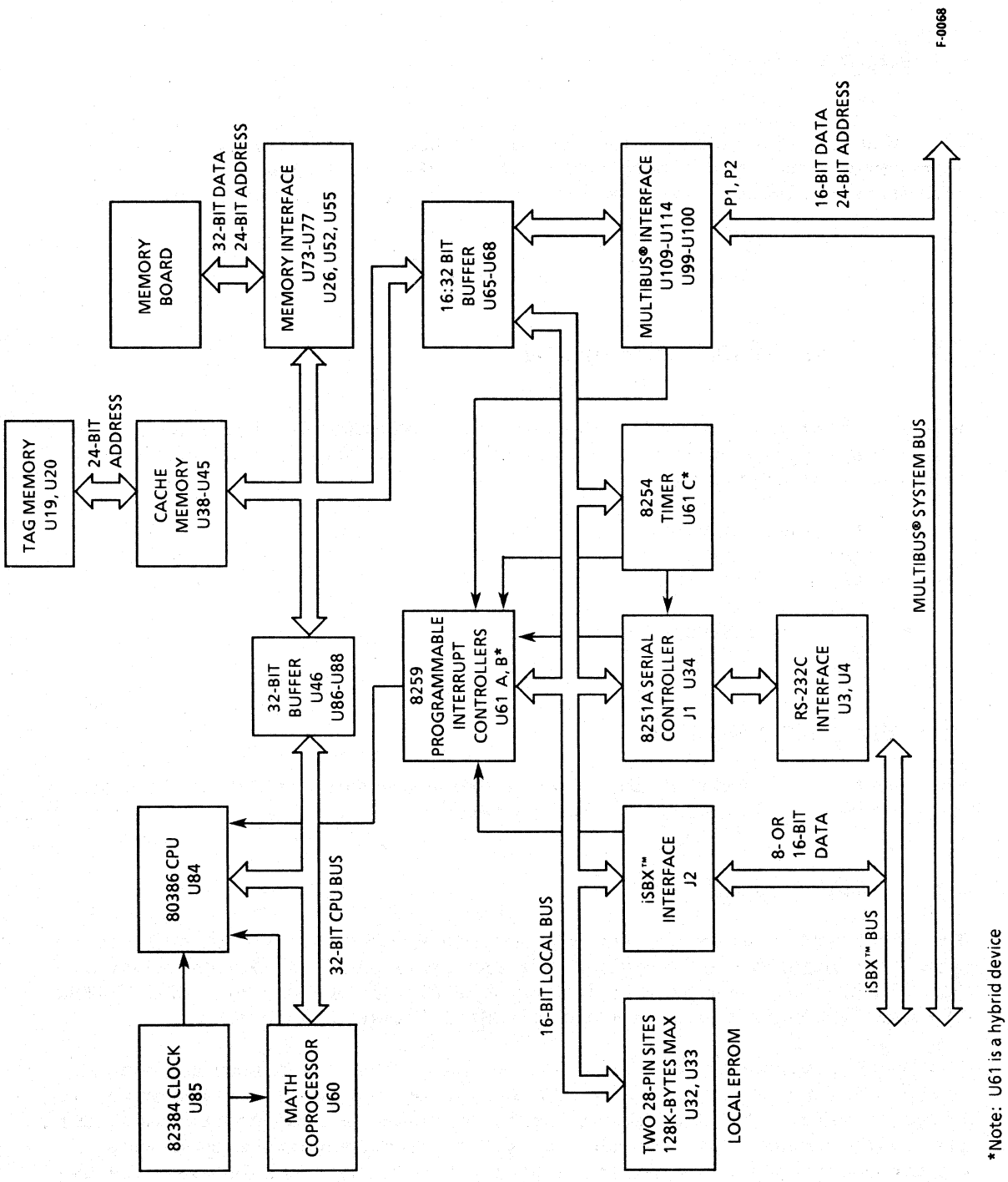


Figure 2-1. iSBC® 386/20P Board Block Diagram

The board contains the circuitry to allow the CPU to enter the self-test mode on a reset. The results of the self-test are stored in the EAX and EDX registers and can be read by instructions after a reset. A successful completion of the self test results in a value of 0 read from the registers. The self-test requires about 33 msec to complete, which is then followed by a normal CPU reset sequence.

The CPU supports slower memory and I/O devices by using wait-states. Only the local EPROM sockets are user-configurable for device-dependent wait-states.

The CPU supports address pipelining: it can drive the address for the next cycle onto the bus before the previous cycle has completed. Whenever the CPU has been in the non-pipelined mode, it cannot enter the pipelining mode until it has incurred at least one clock cycle between the time the address becomes valid and the time the data becomes valid at the processor (one wait-state). The CPU is placed into pipelined mode on a cache miss. The CPU, if in pipelined mode, will be forced to non-pipelined mode if an idle state occurs or an access to a dual-port memory location has been initiated or any type of non-DRAM bus cycle occurs.

The 80386 allows space for up to 256 interrupt vectors. Interrupt vectors 0 through 31 are used by internally generated interrupts and are reserved. The 8259 interrupt controllers map the 15 levels of hardware interrupts into vectors 32 through 256. All are available through software interrupts.

2.2.1.2 80287 Math Module

The board has a 68-pin PGA socket at U60 for a math module with the 80287 Numeric Processor Extension (NPX). The NPX provides high-speed math processing that supports the specifications in the IEEE Microcomputer Floating Point Standard P754. This module contains the 80287 NPX and the necessary logic for interfacing the CPU's 32-bit data bus to the NPX's 16-bit data bus. The math module informs the CPU that it is the math coprocessor by driving the ERROR* line low during the high-to-low transition of reset.

The 80287 NPX's execution unit runs asynchronously to (independent of) the CPU. The asynchronous mode requires that the NPX and CPU have their own clock circuits.

Programming the 80287 NPX is done exactly as for the 8087 NPX, by inserting escape sequences into the instruction execution sequence. When the CPU executes an escape sequence, it starts program execution in the 80287. At that point, the CPU and NPX devices execute instructions in parallel until the CPU executes a WAIT instruction to wait for completion of the NPX operation.

2.2.1.3 Clock Circuits

The board contains three clock sources: an 82384 component for generating the CPU clock, a 20 MHz oscillator, and a 9.8304 MHz oscillator. The 82384 generates the 32 MHz clock (for a 16 MHz CPU) or the 24 MHz clock (for a 12 MHz) for the CPU as well as the system clock, which is in phase with the divide-by-two clock internal to the CPU. The clock generator is also used for reset synchronization for the CPU, the NPX, and other support components. A 24 MHz oscillator on the math module provides the NPX clock. The 9.8304 MHz oscillator is used for the MULTIBUS BCLK and CCLK signals, the master clock for the iSBX interface, and the clock input to the programmable interval timers.

2.2.1.4 Address and Data Buffers

The buffers provide the CPU's address and data buffering. The address buffering includes the latches necessary for pipelined operation. Many of the standard system addresses are generated from these pipelined addresses. The data buffering provides the system data buffering to the CPU, so the NPX is the only other component that resides directly on the CPU's data bus.

2.2.2 MEMORY SECTION

This section explains the local EPROM, local DRAM, dual-port DRAM, and cache memory resources.

2.2.2.1 Local EPROM

Two 28-pin EPROM sites (U32 and U33) support 27256 (32Kx8) or 27512 (64Kx8) EPROMs, which usually hold the start-up instructions. When the CPU is in Real mode, the EPROM sites occupy the upper portion of memory in the processor's 1M-byte memory space. When the CPU is in PVAM, the EPROM sites occupy the upper portion of memory in the processor's 4-gigabyte memory space. You can configure the EPROMs for three to six wait-states. The default configuration accepts 27256 (32Kx8) memory components with six wait-states. Note that the 386/20P board does not support the iSBC 341 memory expansion MULTIMODULE board.

2.2.2.2 Local DRAM

The 386/20P's DRAM resource is the iSBC 402P (2M-byte) or 404P (4M-byte) memory board. The size select lines on the memory boards tell the 386/20P board how much memory it holds. The memory boards contain no user-configurable jumpers; the 386/20P board configures the DRAM resource. The local DRAM starting address is always zero, but its ending address is configurable.

Although the memory is physically located on another board, it is seen by the CPU as an on-board resource. The DRAM interface logic accesses memory through Connector P3 (proprietary MM2 interface) and supports parity generation and checking.

2.2.2.3 Dual-Port DRAM

All or a portion of local DRAM can be configured for dual-port DRAM. Dual-porting allows access to memory from either the 386/20P board or from other MULTIBUS masters using the MULTIBUS interface on the 386/20P board, but only the on-board CPU can transfer 32-bit data streams to memory. Both the starting and ending addresses for dual-port DRAM are configurable.

The dual-port memory appears to other bus masters to be an independent memory resource on the MULTIBUS interface. If the on-board CPU has to arbitrate for the memory resource with another MULTIBUS master, then the on-board CPU cycle will be held off until the other MULTIBUS master has completed its memory access.

NOTE

The 386/20P board cannot access the dual-port memory from its own MULTIBUS interface.

2.2.2.4 Cache Memory

The cache memory improves performance by allowing zero wait-state read accesses to memory when the requested data by the CPU already resides in the cache memory. The cache is transparent to you except for an increase in system performance. The MULTIBUS interface cannot access data directly from the cache. However, the cache will be updated if a MULTIBUS agent is writing information into a dual-ported memory location and if the previous information from that same location resides within the cache memory. This maintains data coherency between the cache and dual-port memory.

The 16K-byte cache has 4K entries. Each entry consist of a 32-bit data field (four bytes) and an 8-bit tag field. The cache entry corresponding to a memory address on the board is determined by address bits 2-15. Each byte in memory maps to one and only one entry in the cache memory. All memory locations on the board for which address bits 2-15 are the same map to the same cache entry.

The tag field is used to determine if, on a 80386 read or a MULTIBUS write cycle into dual-port memory, the desired entry currently resides in cache memory. During either of these two cycles, bits 2-15 of the address provided by the requesting agent are used to access the cache entry and the contents of the tag.

The tag field is compared to bits 16-23 of the address provided by the requestor. If there is a "match," indicating that the two fields are equal, the access is a "hit," meaning that the data requested currently resides in the cache. The data field of the cache entry is read, and the cycle is completed for a CPU access or the cache entry is updated with the new data being written into DRAM by the MULTIBUS agent. If the two fields do not match, the access is a miss.

A miss has different connotations, depending on whether it is a CPU miss or a MULTIBUS master miss. The CPU miss indicates that the current read data does not reside in the cache or that the data transfer is a write operation. When a CPU miss occurs, a DRAM cycle begins. If a CPU hit occurs, no DRAM cycle starts. A MULTIBUS agent miss indicates that the DRAM cycle begun does not affect the cache. The MULTIBUS agent hit, which may occur only on a write cycle, updates the cache if the cache currently holds the old data of the DRAM location being written.

To ensure data coherency between the DRAM and the corresponding cache entries, a write-through strategy is implemented. On any CPU write cycle, the transferred data is written to both the data field of the appropriate cache entry and to the DRAM array. Writes of less than 32 bits cause part of the cache data field to be filled from the DRAM array. CPU read operations that are not hits cause the data field of the cache entry to be filled from the DRAM array. All 32 bits of the data field are always filled. In addition, whenever a cache entry is filled from a CPU access, bits 16-23 update the tag field. MULTIBUS master hits do not update the tag field. The cache is not updated on CPU accesses to or from the MULTIBUS interface.

2.2.3 CONTROLLER SECTION

The controller provides control logic to perform memory and I/O cycles for the local CPU and the MULTIBUS agent (a MULTIBUS agent is another system board on the MULTIBUS interface). It also performs on-board tasks, such as memory refresh, and it contains the necessary circuitry to generate the processor ready signal. The following sections explain bus arbitration, data buffer control, memory access control, and decode control.

2.2.3.1 Bus Arbitration

The controller provides arbitration for the dual-port memory among MULTIBUS masters, the on-board CPU, and the refresh logic. During a transfer cycle, the master from which the request came controls the memory resource of the board. This control cannot change during a transfer cycle; once a DRAM transfer cycle has been started by an agent on one of the buses, the memory cannot reply to a request from the other agent.

The dual-port arbiter determines who will control the dual-port memory. It is based on this algorithm:

a) The MULTIBUS agent will be granted the request if the on-board CPU is not currently executing a cycle and it has not locked the dual-port memory.

b) The MULTIBUS agent will be granted the request if the CPU is currently executing an operation and if the CPU wants to use the MULTIBUS interface or if the CPU is doing a math operation.

   The 80287 math module resides on the CPU bus, which does not use the dual-port circuitry.

c) The CPU will retain control of dual-port memory until conditions validate either (a) or (b).

The dual-port logic will try to force condition (a) above by inhibiting address pipelining when a dual-port request occurs. This creates a time window to ensure that dual-port requests will be honored. The dual-port logic will return to local control if neither the MULTIBUS agent nor the on-board CPU have a request pending.

2.2.3.2 Data Buffer Control

The data buffer control directs the output enable and direction of all the data buffers on the board. It ensures that the data gets to the right place at the right time, without bus contention.

Also, because of the timing disparity between the MULTIBUS interface and the on-board CPU, the data buffer control system is responsible for latching data and addresses from the CPU to meet MULTIBUS hold timing specifications.

2.2.3.3 Memory Access Control

The controller generates the control and timing signals that control access to the memory elements. It also generates the refresh cycles to maintain data integrity.

These signals are generated for the memory interface:

- RAS - Row Address Strobe
- CAS - Column Address Strobe
- MUX - Interchanges the row addresses and column addresses
- RAEN - Refresh Address Enable for refresh cycles
- REFREQ - A pulse that initiates a refresh request

The DRAM state machine completes a transfer cycle in 5 clock cycles in the non-pipelined mode (three wait-states for the CPU). In the address pipelining mode, the number of wait-states is reduced to two (four clock cycles).

2.2.3.4 Decode Control

The decode section decodes CPU addresses and requests the proper cycles to perform an access.

To select Real mode or PVAM, the processor must programmatically set the PROT register located at I/O address 00E0H. When the iSBC 386/20P board powers up, it is configured for Real mode (PROT = 0). Thus, the top of the DRAM can be as high as 1M byte less the amount of EPROM that is present (128K bytes maximum).

In PVAM (PROT = 1), the top of DRAM can be as high as 16M bytes. If there is not 16M bytes of DRAM, any access between the top of DRAM and the 16M byte boundary is a MULTIBUS access.

For accesses to I/O, the decode circuitry determines if the access is for an on-board resource. If so, then the proper chip selects are generated. If not, then a MULTIBUS I/O access is initiated.

2.2.4 I/O SECTION

This section describes the on-board I/O devices: programmable interval timers, programmable interrupt controllers, and the on-board control registers.

NOTE

The 8254 Programmable Interval Timer and the 8259A master and slave Programmable Interrupt Controllers are packaged together in one IC (8259H). Their programming is the same as if they were in separate ICs.

2.2.4.1 Programmable Interval Timers

An 8254 programmable interval timer provides three 16-bit interval timers, which all have dedicated functions (no jumper options for the timer outputs):

- Counter 0 is connected to IR0 on the master PIC. You can program this timer to generate real-time interrupts.
- Counter 1 is connected to IR5 on the slave PIC. You can also program this timer to generate real-time interrupts or to time operations.
- Counter 2 is connected to the transmit and receive clocks on the 8251A serial controller. You can program this timer to generate bauds rates from 75 Hz to 38.4 KHz.

The timers have the same 1.23 MHz clock input.

2.2.4.2 Programmable Interrupt Controllers

Two 8259As are used for processing interrupts: one is the master and the other is the slave. Together they can process 15 interrupts. Three of the interrupts have dedicated purposes, leaving 12 interrupts that you can configure (not counting NMI on the CPU).

The board can receive the eight MULTIBUS interrupt signals (MBINT0* through MBINT7*). Eight inverters are supplied at the interrupt matrix to invert the signals to an active-high level (required by the PICs). The board can also generate two MULTIBUS interrupts (parity error and MULTIBUS interrupt), which can be connected to any of the unused MULTIBUS interrupt lines.

2.2.4.3 On-Board Control Registers

The 386/20P board has six I/O control registers to control the status of the system:

1. PROT Register -- This register enables the 386/20P board to work with Real mode or PVAM addressing (20-bit addressing or 32-bit addressing).

2. Time-Out Register -- This register resets the time-out interrupt signal and the red LED (DS2).

3. Processor Status Latch -- You can write to this register to turn the green LED (DS3) on or off.

4. MULTIBUS Interrupt Register -- You can use this register to set or reset a MULTIBUS interrupt.

5. On-Board Parity Error Latch -- You can write to this register to reset the parity error interrupt and the red LED (DS4).

6. NMI Mask Latch -- You can use this register to enable or disable parity checking.

2.2.5 INTERFACE SECTION

This section describes the iSBX, serial, MULTIBUS, and auxiliary interfaces.

2.2.5.1 iSBX™ Interface -- Connector J2

Connector J2 provides iSBX I/O expansion. A jumper indicates whether the module is an 8-bit (default) or a 16-bit iSBX MULTIMODULE board. You can configure the two option lines and the two iSBX interrupt lines.

The iSBC 386/20P board assigns I/O port addresses 0080H through 009FH to the iSBX bus connector for iSBX MULTIMODULE boards, whether they are installed or not.

2.2.5.2 RS-232C Serial Interface -- Connector J1

The 386/20P board provides one asynchronous RS-232C serial port using an 8251 serial controller. No jumper configurations are supported for the serial port.

The port is a 10-pin connector that uses the 9-pin IBM PC serial standard. Because of this format, the interface provides minimum modem support. The ringing indicator (RI) is implemented as an interrupt input in the interrupt jumper matrix. The carrier gain and loss interrupts are not supported, but carrier detect is supported.

The DTE interface mass terminates to modem equipment. However, the signal lines can be rerouted for connection with terminal equipment.

2.2.5.3 MULTIBUS® Interface -- Connector P1

The CPU can access the full address space on the MULTIBUS interface. The on-board CPU can transfer a maximum of 16 bits of data at one time (a MULTIBUS limitation). For compatibility with 8-bit MULTIBUS boards, 16-bit to 8-bit swapping logic is incorporated. The 386/20P board uses the 8288 bus controller and 8289 bus arbiter to provide complete MULTIBUS compatibility.

NOTE

Double-word transfers to the MULTIBUS interface are done by two 16-bit word transfers. These two transfers may be interleaved by other MULTIBUS transfers from other masters on the bus.

2.2.5.4 Auxiliary Interface -- Connector P2

Connector P2 is used as an auxiliary interface. Note that other MULTIBUS boards might use Connector P2 as an iLBX interface, which is not compatible with this auxiliary interface. This interface accesses system features not found on the other standard interfaces. Only a few lines from this connector are used:

- The upper four MULTIBUS address lines (ADR20-23*)
- Power fail interrupt input (PFINT*)
- Address Latch Enable (ALE) from the 80386 CPU for a front panel run indicator
- Console lock input (CONSLCK*) for disabling the 8251A serial controller chip
- Auxiliary reset input (AUXRES*) from the MULTIBUS system (resets the 80386 CPU)

See Section 4.4.3 for more information on these signals.

2.3 SOFTWARE DIFFERENCES BETWEEN THE iSBC® 386/20P AND 286/12 BOARDS

Since the 80386's instruction set is fully compatible with the instruction set of the 8086/186/286, you can run 8086/186/286 code on the 386/20P board with little modification. If you want to modify code written for the iSBC 286/12 board to run on the 386/20P board, the similarities and differences between the 286/12 and 386/20P boards are as follows:

Similarities:

- An iSBX port resides at I/O address range 0080H-009FH.
- The master and slave PICs share the same I/O addresses.
- The programmable timers share the same I/O addresses.
- The parity port addresses are identical.
- Neither board translates addresses for dual-port memory. (MULTIBUS agents and the on-board CPU both access dual-port memory with the same address; address aliasing is not supported.)

Differences:

- The 386/20P board's I/O register for switching CPU modes resides at I/O address 00E0H, and it can be set or reset by the 80386 CPU. The 286/12 board's I/O address resides at 00CAH, and it can only be set by the 80286 CPU. It is reset by a software reset. The 386/20P board does not support software resets.
- The 386/20P uses an 8251A serial controller instead of the 8274 multiple serial controller. The 386/20P board supports only the serial DTE interface. The 286/12 board supports only DCE on Channel B. Channel A is configurable for DCE or DTE.
- The 386/20P board does not support parallel I/O.

***

CHAPTER 3
BOARD PREPARATION AND INSTALLATION

3.1 INTRODUCTION

This chapter presents the equipment and components that you may need for your application. It includes information on preparing the board's environmental conditions and lists the equipment and components that you must supply. Programming and configuration information is located in Chapter 4.

3.2 UNPACKING AND INSPECTING THE BOARD

Inspect the shipping carton immediately on receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection. Refer to Chapter 5 for repair and service information.

3.3 PREPARING THE BOARD ENVIRONMENT

The iSBC 386/20P board has requirements for power, cooling, physical space, and weight, which are explained in the following sections and summarized in Table 1-1.

3.3.1 POWER REQUIREMENTS

The MULTIBUS interface provides power for the iSBC 386/20P board. At most, the board requires three voltage levels and ground:

- +5 volts power source for all configurations
- ±12 volts power source for system configurations using either the RS-232C interface or an iSBX MULTIMODULE board
- Ground for all configurations

3.3.2 COOLING REQUIREMENTS

You must provide adequate air circulation to prevent the air around the board from rising above 55°C. A minimum air flow of 200 linear feet per minute across the board provides enough air circulation. Table 1-1 summarizes the board's temperature and humidity specifications.

3.3.3 SIZE AND WEIGHT SPECIFICATIONS

The iSBC 386/20P board has non-standard MULTIBUS form factor dimensions, which may require additional mounting space. Refer to Table 1-1 for the size and weight specifications.

3.4 COMPONENTS REQUIRED

You need to ensure your system is configured with the necessary components for operation, namely the memory resource and correct MULTIBUS termination. Figure 3-1 shows the location and connectors for any user-supplied parts you might use.

3.4.1 MEMORY

You need to install your own local EPROM, local DRAM, and dual-port DRAM. The two EPROM sockets (U32 and U33) are configurable for 27256 (32Kx8) or 27512 (64Kx8) components and from three to six wait-states. You must install the same size component in both sockets. Any electrically and mechanically equivalent components may be substituted. Local and dual-port DRAM must be supplied by either the iSBC 402P (2M-byte) or 404P (4M-byte) memory board. The 386/20P board connects to the 402P or 404P memory board via the MM2 interface (Connector P3). The starter kit includes these memory resources.

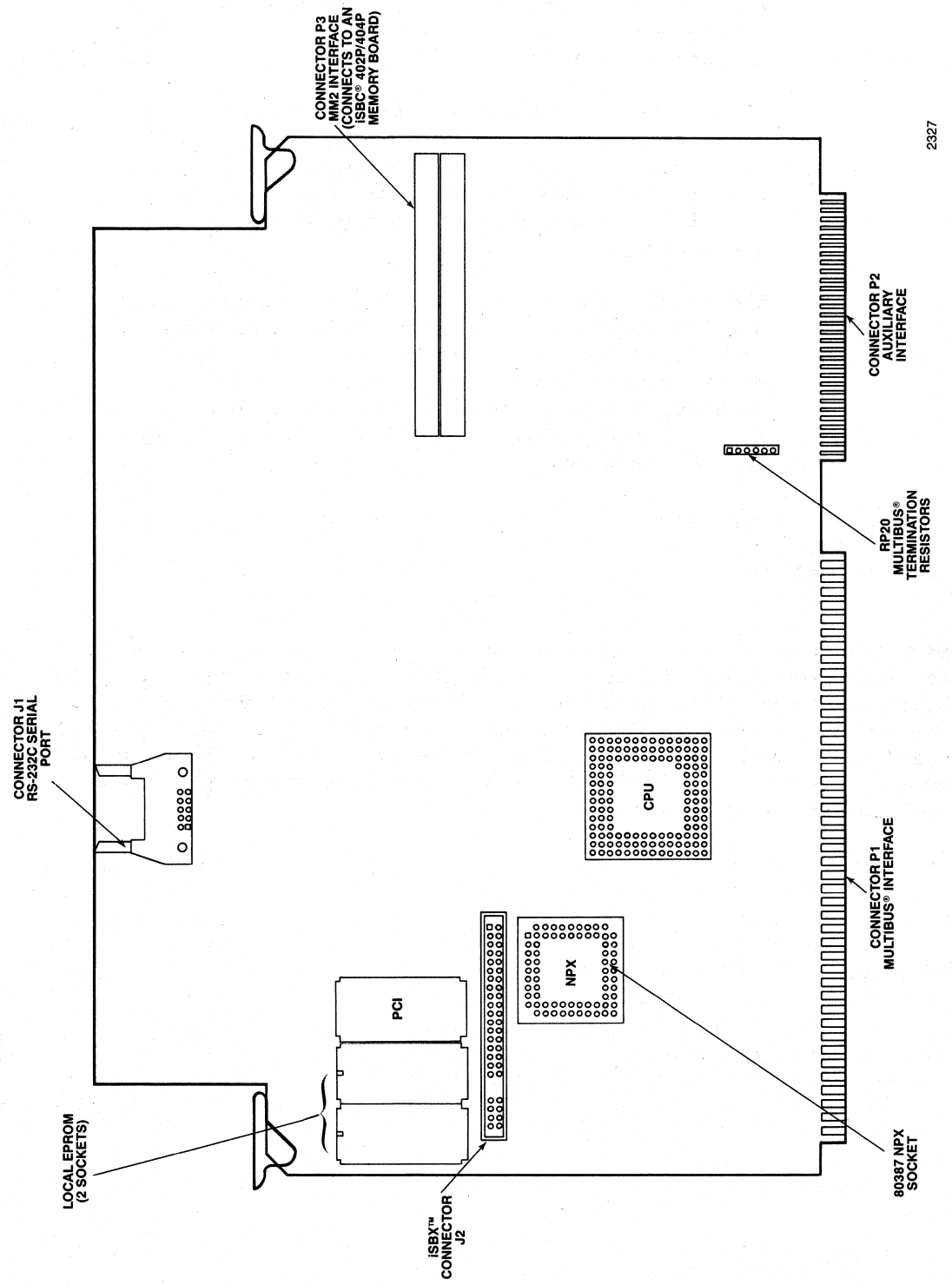


Figure 3-1. Parts Location Diagram

CAUTION

Never insert components into a board when power is applied. Doing so could damage the components and/or the board.

When installing the integrated circuit packages into the sockets, ensure that pin 1 of the chip is inserted into pin 1 of the chip socket. This orientation places pin 1 of the chip closest to the silk-screened dot (which indicates pin 1 of the socket).

MOS EPROMs are highly susceptible to damage from static electricity. Use extreme caution when installing MOS components in a low-humidity environment. Always ground yourself before handling MOS components; this ensures that a static charge build-up is not dissipated through the MOS devices.

3.4.2 Resistor Pack

The iSBC 386/20P board contains one user-configurable resistor pack (RP20) to terminate the upper four MULTIBUS address lines. Only one board in the MULTIBUS system should terminate these MULTIBUS lines. If the resistor pack is left installed, ensure that the other MULTIBUS boards have their termination R-packs removed. If the resistor pack is removed from the iSBC 386/20P board, ensure one and only one other MULTIBUS board terminates the lines.

3.5 CONNECTOR AND CABLE PARTS

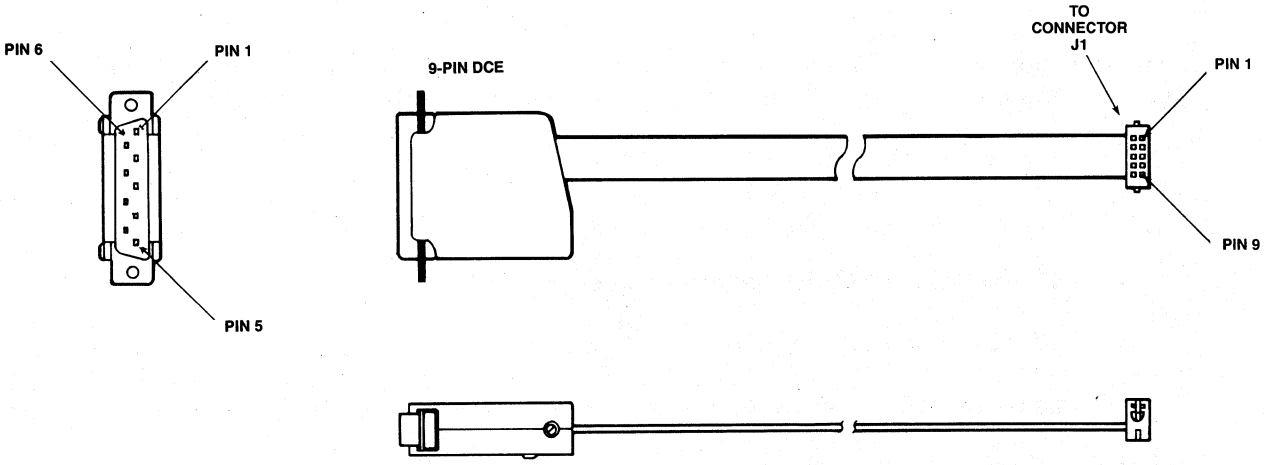
Depending on your application, you may need to supply connector and cable parts. Figure 3-1 shows the location of the five connector types:

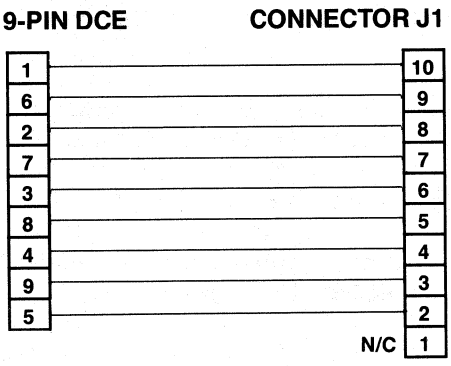
- 9-pin IBM standard RS-232C DTE interface (J1)
- 36- or 44-pin iSBX interface connector (J2)
- 86-pin MULTIBUS interface connector (P1)
- 60-pin auxiliary connector (P2)
- 100-pin MM2 interface memory board connector (P3A and P3B)

The serial and MM2 interface cables are included in the starter kit. Figure 3-2 shows the cable assembly for connecting J1 to a 9-pin DCE connector. Figure 3-3 shows the cable assembly for connecting J1 to a 25-pin DCE connector. Figure 3-4 shows the cable assembly for connecting J1 to a 25-pin DTE connector (this assembly is provided with the starter kit).

Table 3-1 provides a list of connector parts that interface to the board connectors. The table also provides the manufacturers' names and part numbers so you can order the connectors. Any electrically and mechanically equivalent parts may be substituted.

Table 3-2 provides information on cables compatible with the connector parts in Table 3-1 for the serial I/O interface.





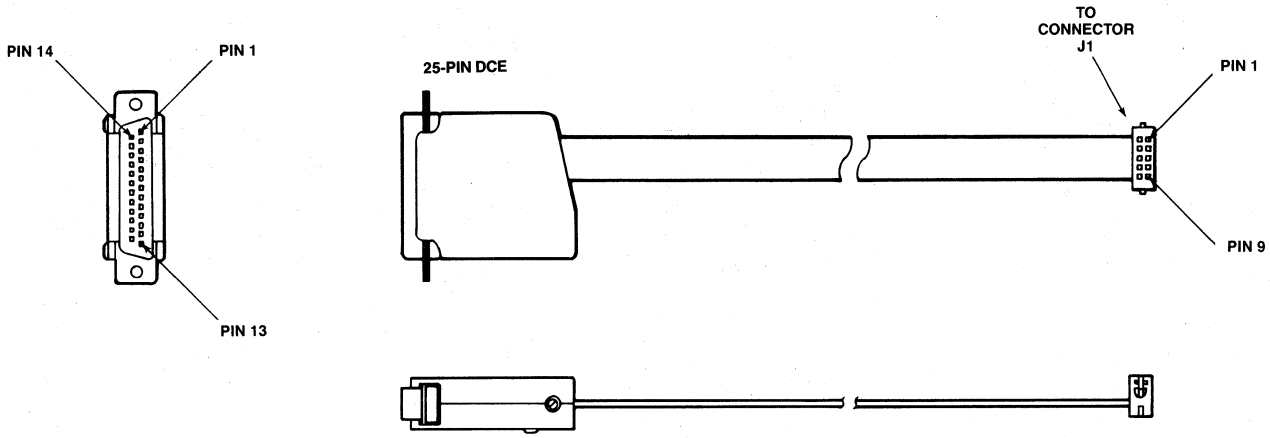
WIRING DIAGRAM

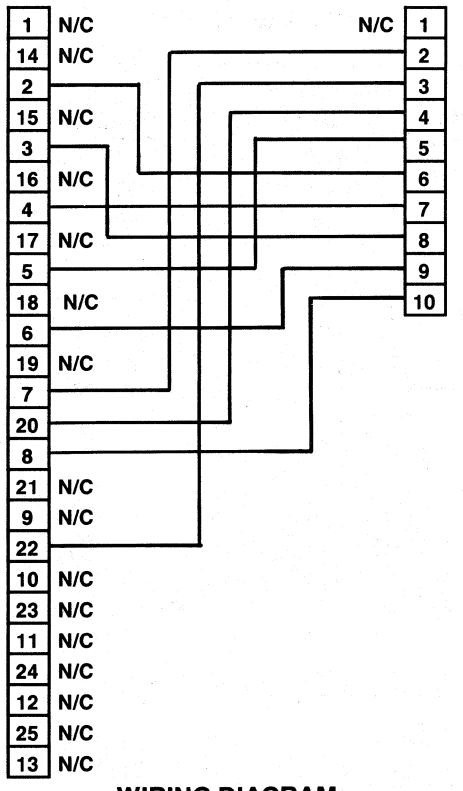
PIN ASSIGNMENT

Connector			
9-Pin DCE	Signal	J1	Signal
5	SGND	2	SGND
9	RI	3	RI
4	DTR	4	DTR
8	CTS	5	CTS
3	TD	6	TD
7	RTS	7	RTS
2	RD	8	RD
6	DSR	9	DSR
1	CD	10	CD

2328

Figure 3-2. Connector J1 to 9-Pin DCE Cable Assembly





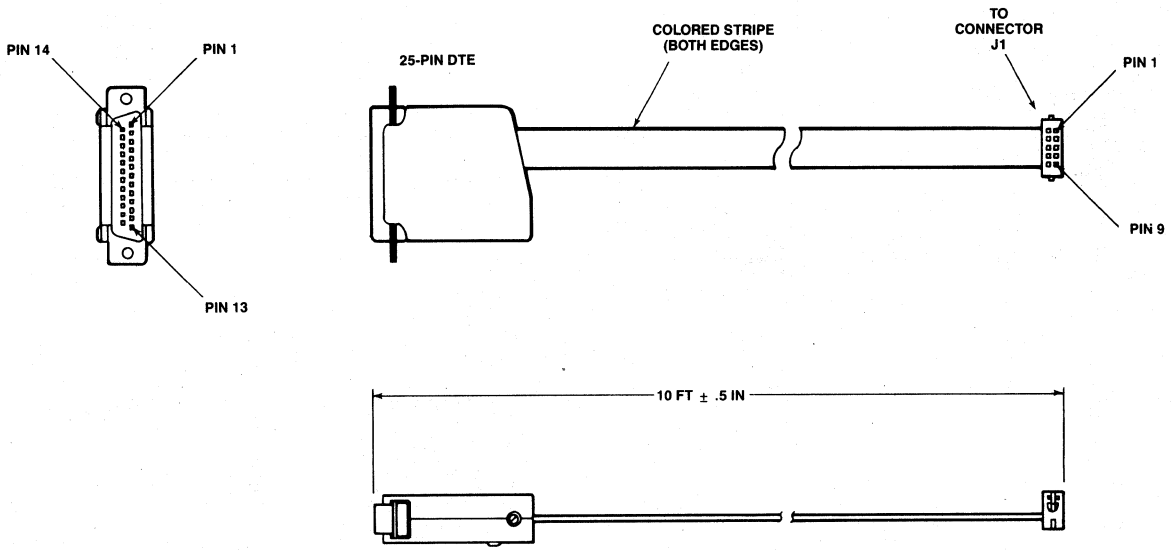
WIRING DIAGRAM

PIN ASSIGNMENT

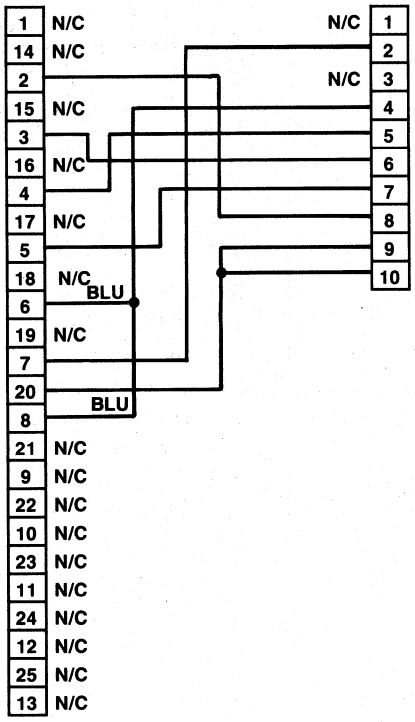
Connector			
25-Pin DCE	Signal	J1	Signal
7	SGND	2	SGND
22	RI	3	RI
20	DTR	4	DTR
5	CTS	5	CTS
2	TD	6	TD
4	RTS	7	RTS
3	RD	8	RD
6	DSR	9	DSR
8	CD	10	CD

2329

Figure 3-3. Connector J1 to 25-Pin DCE Cable Assembly



STARTER KIT CONFIGURATION



WIRING DIAGRAM

PIN ASSIGNMENT

Connector			
25-Pin DTE	**Signal**	**J1**	**Signal**
7	SGND	2	SGND
6,8	DSR,CD	4	DTR
4	RTS	5	CTS
3	RD	6	TD
5	CTS	7	RTS
2	TD	8	RD
20	DTR	9,10	DSR,CD

2330

Figure 3-4. Connector J1 to 25-Pin DTE Cable Assembly (Starter Kit Configuration)

Table 3-1. User-Supplied Connector Parts

Function	# of Pins	Centers (inches)	Connector Type	Vendor	Vendor Part Number
MULTIBUS connector (P1)	86	0.156	Soldered[1] PC board mount	Viking ELFAB	2KH43/9AMK12 BS1562D43PBB
			Wirewrap Without ears	EDAC ELFAB	337086540201 BW1562D43PBB
			Wirewrap (.128 dia.) Mounting holes	EDAC ELFAB	337086540202 BW1562A43PBB
Auxiliary interface connector (P2)	60	0.1	Soldered Soldered Soldered	KELAM KELAM T&B Ansley	RF30-2803-5 110-10-001-37 A3020
		0.1	Soldered	ELFAB EDAC	97169001 345060500202
			Wirewrap Without ears	ELFAB EDAC	BW1020D30PBB 345060540201
			Wirewrap	ELFAB EDAC	BS1020A30PBB 345060524202
			Wirewrap (.128 dia.)	TI Viking	H421121-30 3KH30/9JNK
iSBX bus connector 8-bit (J2)	36	0.1	Soldered	Viking Viking	000292-0001 male 000291-0001 female

(continued)

Table 3-1. User-Supplied Connector Parts (continued)

Function	# of Pins	Centers (inches)	Connector Type	Vendor	Vendor Part Number
iSBX bus connector 16-bit (J2)	44	0.1	Soldered	Viking	000293-0001 male
				Viking	000294-0001 female
Serial I/O connector (J1)	10		Strain-relief	T&B Ansley	609-1000M connector
			female		609-1031 strain-relief
	25		"D" type male	T&B Ansley	609-25PM
Note: [1] Connector heights are not guaranteed to conform to Intel packaging equipment.					

Table 3-2. Ribbon Cable

Interface Type	# of Pins	Vendor	Part Number
Serial I/O connector (J1)	10	T&B Ansley	171-10

3.6 iSBC® 386/20P BOARD AND iSBC® 402P OR 404P MEMORY BOARD TARGET SYSTEM INSTALLATION

Complete instructions for installing the 386/20P and memory boards into a target system are in the iSBC 386/20 STARTER KIT OVERVIEW AND INSTALLATION MANUAL.

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CHAPTER 4
CONFIGURATION

4.1 INTRODUCTION

This chapter describes the configurable functions on the board and includes jumper, addressing, interface, and programming information, in the following sections:

4.2 Memory Configuration
- Local EPROM
- Local DRAM
- Dual-Port DRAM
- MULTIBUS Memory
- Configuration Example

4.3 I/O Configuration
- Numeric Processor Extension (NPX -- 80287 Math Module)
- Programmable Interrupt Controllers (PICs -- 8259A)
- Programmable Interval Timer (PIT -- 8254)
- Serial Interface Programming (PCI -- 8251A)
- I/O Registers

4.4 Interface Configuration
- Serial I/O Interface
- MULTIBUS Interface
- Auxiliary Interface
- iSBX Interface

See Figure 2-1 for a block diagram of the 386/20P board and Appendix A for a jumper location diagram, jumper description list, and schematic jumper index list. The following sections describe the configurations available for each function.

4.2 MEMORY CONFIGURATION OVERVIEW AND DEFAULT MEMORY MAP

The 386/20P board supports four types of memory: local EPROM, local DRAM, dual-port DRAM, and MULTIBUS memory. Local EPROM is read-only memory accessed only from the CPU and not from other MULTIBUS masters. EPROM holds the start-up instructions for the CPU. Local DRAM is read/write memory accessible only from the CPU. Dual-port DRAM is a portion of the local DRAM accessible from both the CPU and other MULTIBUS masters. MULTIBUS memory allows the 386/20P board to access memory or buffers located on other MULTIBUS boards (such as an iSBC 214 disk controller).

Each type of memory has different configuration options. The local EPROM starting address and address space is defined by the type of EPROMs installed (27256 or 27512 devices). The local DRAM always starts at 0H (the bottom of memory), but its ending address is configurable. Dual-port DRAM has configurable starting and ending addresses.

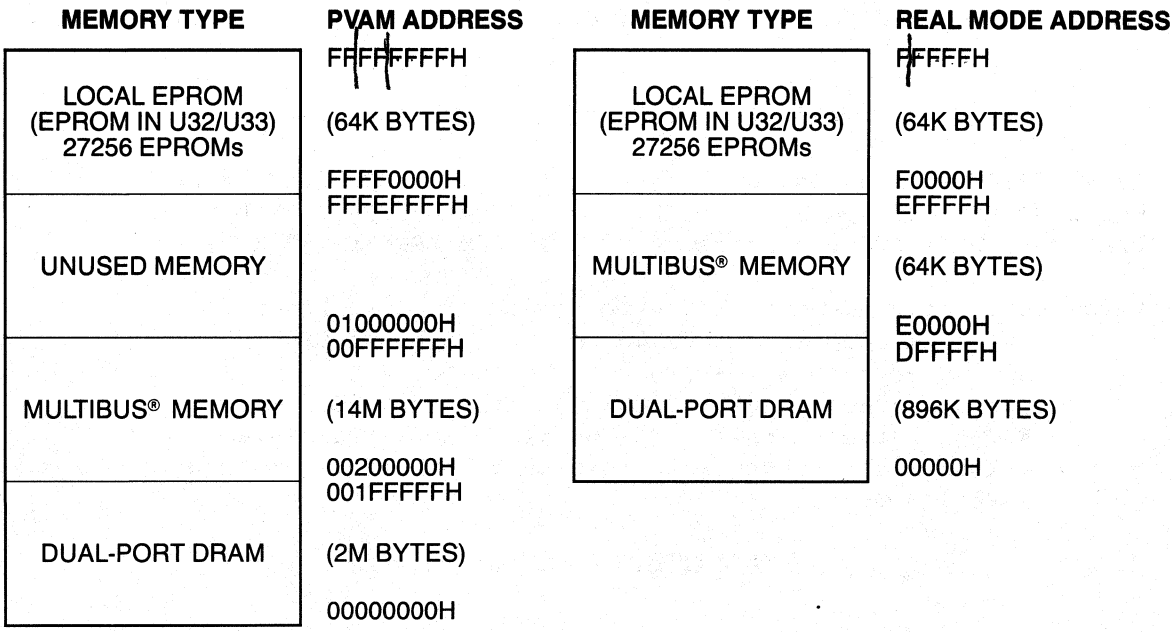
Figure 4-1 shows the default memory map ("H" designates hexadecimal notation). If the default configuration is not suitable for your application, you can reconfigure memory using these four steps:

1. Configure your local EPROM space.
2. Configure your local DRAM space.
3. Configure your dual-port DRAM space.
4. All undefined memory space is then assigned as MULTIBUS memory.

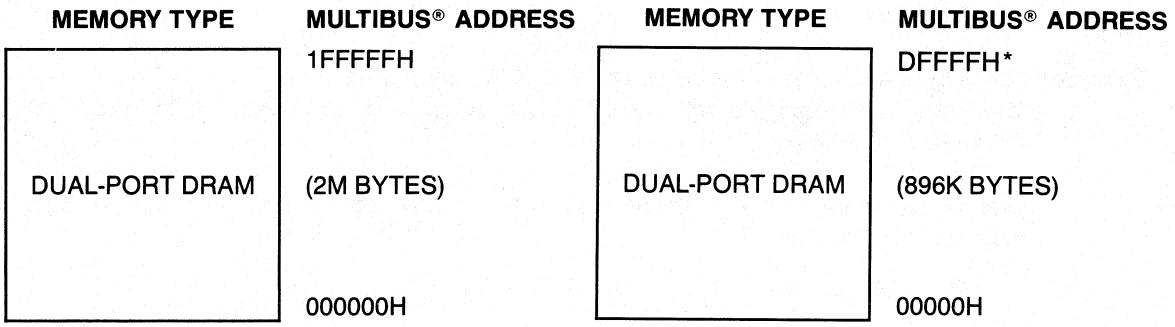
The following sections give details for configuring memory:

NOTE

The default memory configuration is for PVAM. If you intend to use Real mode, reconfigure the ending address of dual-port DRAM to DFFFFH. Otherwise, MULTIBUS masters will access dual-port DRAM from 000000H-1FFFFFH and the on-board CPU will access dual-port DRAM from 00000H-DFFFFH, creating a MULTIBUS memory resource from 0E0000H-1FFFFFH not accessible to the on-board CPU.



Memory as seen from the on-board 80386



Memory as seen from the MULTIBUS® Interface

* The default memory configuration is for PVAM. If you want to use Real mode, you need to reconfigure the dual-port DRAM ending address to DFFFF, as shown.

2331

Figure 4-1. Default Memory Map of the iSBC® 386/20P Board

NOTE

Other MULTIBUS masters access dual-port DRAM with the same addresses as the CPU, regardless of the board CPU mode (Real Mode or PVAM); therefore, address aliasing is not supported.

DEFAULT PARAMETERS

Local and dual-port DRAM are supplied by the 402P (2M-byte) memory board. EPROM is supplied by two 27256 (32Kx8) components with six wait-states.

REAL MODE DEFAULT MEMORY MAP

Local EPROM Address Space:	F0000H-FFFFFH (64K bytes)
MULTIBUS Address Space:	E0000H-EFFFFH (64K bytes)
Dual-Port DRAM Address Space:	00000H-DFFFFH (896K bytes)

Parameters for Dual-Port DRAM with the CPU in Real Mode:

Starting address at 00000H for the on-board CPU
Ending address at DFFFFH for the on-board CPU
Starting address at 000000H for other MULTIBUS masters
Ending address at 1FFFFFH for other MULTIBUS masters
(You should reconfigure this to DFFFFH if you intend to use only Real mode)

PVAM DEFAULT MEMORY MAP

Local EPROM Address Space:	FFFF0000H-FFFFFFFFH (64K bytes)
Unused Address Space:	01000000H-FFFEFFFFH
MULTIBUS Address Space:	00200000H-00FFFFFFH (14M bytes)
Dual-Port DRAM Address Space	00000000H-001FFFFFH (2M bytes)

Parameters for Dual-Port DRAM with the CPU in PVAM:

Starting address at 00000000H for both the on-board CPU and other MULTIBUS masters

Ending address at 001FFFFFH for both the on-board CPU and other MULTIBUS masters

4.2.1 LOCAL EPROM CONFIGURATION

You must install two EPROM components (containing initialization code) for local memory before you can use the board.

Figure 4-1 shows the default memory map, which depends on which mode the CPU is in (PVAM or Real Address mode). The board is default configured for two 27256 (32Kx8) EPROMs at six wait-states.

The 386/20P board is configurable for two types of EPROM and for four different wait-states. It accepts either 27256 (32Kx8) or 27512 (64Kx8) EPROMs. Therefore, using two 27512 EPROMs, the board can hold up to 128K bytes of local EPROM. You can choose from three to six wait-states. Wait-states ensure that the CPU waits long enough for a response from a slower type of memory device.

You can logically step through the entire local EPROM configuration sequence by performing these five steps:

1. Select a device type
2. Find the socket configuration from Table 4-1
   Install and remove the necessary jumpers
3. Determine the number of wait-states needed
   (wait-state timing is shown in Table 4-2)
4. Find the wait-state configuration from Table 4-2
   Install and remove the necessary jumpers
5. Record your local EPROM address space from Table 4-1

EXAMPLE

1. 27512 (250 nsec access speed)
2. E1-E3 IN, E8-E9 IN, E11-E12 IN, E8-E10 OUT, E11-E13 OUT
3. 5 wait-states using a 386/20P board with a 12 MHz CPU
4. E108-E109 IN, E106-E107 OUT
5. Real Mode: FFFFFH-E0000H
   PVAM: FFFFFFFFH-FFFE0000H

NOTE

You cannot mix types within the socket pair. For example, if you install a 32Kx8 EPROM device at U32, then you must install a 32Kx8 EPROM device at U33.

Table 4-1. EPROM Jumper Selection

Device Type	E1-E3	U32 E8-E9	U32 E8-E10	U33 E11-E12	U33 E11-E13	Address Range
27256 § (32Kx8)	OUT	OUT	IN	OUT	IN	Real Mode: F0000H-FFFFFH PVAM: FFFF0000H-FFFFFFFFH
27512 (64Kx8)	IN	IN	OUT	IN	OUT	Real Mode: E0000H-FFFFFH PVAM: FFFE0000H-FFFFFFFFH

§ identifies the default configuration.

Notes: Local EPROM is always top-justified (ending at the highest address).
U32 and U33 accept only EPROM devices.

Table 4-2. Local Memory Wait-State Jumpers

Local Pair U32/U33 Wait-states	EPROM access speed (max.) 16 MHz (12MHz)	Jumper E106-E107	Jumper E108-E109
3	130 (less than 200) nsec	IN	IN
4	200 (less than 250) nsec	IN	OUT
5	250 (less than 350) nsec	OUT	IN
6 §	320 (less than 450) nsec	OUT	OUT

§ Identifies the default configuration.

4.2.2 LOCAL DRAM CONFIGURATION

The iSBC 386/20P board uses Connector P3 for interfacing to an iSBC 402P or 404P (2M-byte or 4M-byte) memory board. The memory board supplies the local and dual-port DRAM for the 386/20P board.

Local DRAM always starts at the bottom of memory (0H), but you can configure its ending address by changing jumpers E14 through E37. You must configure two ending addresses: one for each operating mode of the CPU (Real Mode or PVAM). You configure the ending address on 1M-byte and 64K-byte boundaries. The 386/20P board has local DRAM default configured for the first 896K bytes in Real Mode and the first 2M bytes in PVAM.

The 386/20P board's logic enables local DRAM only if the configured address is greater than the requested address. Therefore, you must configure your ending address at one greater than the actual ending address. You can configure the local DRAM address in four steps:

1. Choose your actual ending address

2. Add 1 to get your configured ending address

3. Configure the megabyte boundary from Table 4-3
   Install or remove the necessary jumpers

4. Configure the 64K-byte boundary from Table 4-4
   Install or remove the necessary jumpers

EXAMPLE

	PVAM	Real Mode
1.	1FFFFFH	0DFFFFH
2.	200000H	0E0000H
3.	2xxxxxH E15-E18 IN, E21-E24 IN, E27-E30 OUT, E33-E36 IN	na
4.	x00000H E14-E17 IN, E20-E23 IN, E26-E29 IN, E32-E35 IN	xE0000H E16-E19 OUT, E22-E25 OUT, E28-E31 OUT, E34-E37 IN

There are two exceptions to this procedure:

1. If the configured address is 000000H, local DRAM is disabled. This is because the configured address would never be greater than the requested address.

2. The highest possible ending address is FEFFFFH (PVAM) or EFFFFH (Real Mode) using the configured address of FF0000H. This configuration does not allow you to access the upper 64K bytes, which contain EPROM when in Real Mode.

NOTE

Remember that the local EPROM starting address was previously defined. Any memory space configured for both local EPROM and local DRAM will default to local EPROM.

Any portion of local DRAM not further configured as dual-port DRAM is accessible only by the local CPU.

Table 4-3. Local DRAM Ending Address -- Megabyte Page Configuration

Jumpers Installed (PVAM only)				Megabyte Addresses
E15-E18 ADR23	E21-E24 ADR22	E27-E30 ADR21	E33-E36 ADR20	
OUT	OUT	OUT	OUT	FxxxxxH
OUT	OUT	OUT	IN	ExxxxxH
OUT	OUT	IN	OUT	DxxxxxH
OUT	OUT	IN	IN	CxxxxxH
OUT	IN	OUT	OUT	BxxxxxH
OUT	IN	OUT	IN	AxxxxxH
OUT	IN	IN	OUT	9xxxxxH
OUT	IN	IN	IN	8xxxxxH
IN	OUT	OUT	OUT	7xxxxxH
IN	OUT	OUT	IN	6xxxxxH
IN	OUT	IN	OUT	5xxxxxH
IN	OUT	IN	IN	4xxxxxH
IN	IN	OUT	OUT	3xxxxxH
IN	IN	OUT	IN	2xxxxxH §P
IN	IN	IN	OUT	1xxxxxH
IN	IN	IN	IN	0xxxxxH §R

§P Identifies the PVAM default configuration.
§R Identifies the Real Mode configuration (nonconfigurable).
ADR Identifies the decimal address line number (ADR0 is LSB).
Notes: This address is only selectable for PVAM. For Real Mode, these upper four address lines are automatically set to "0".
The starting address is always 0H.

Table 4-4. Local DRAM Ending Address -- 64K-byte Page Configuration

Jumpers Installed				64K-byte Addresses
PVAM				
E14-E17 CA19	E20-E23 CA18	E26-E29 CA17	E32-E35 CA16	
Real Mode				
E16-E19 CA19	E22-E25 CA18	E28-E31 CA17	E34-E37 CA16	
OUT	OUT	OUT	OUT	xF0000H
OUT	OUT	OUT	IN	xE0000H §R
OUT	OUT	IN	OUT	xD0000H
OUT	OUT	IN	IN	xC0000H
OUT	IN	OUT	OUT	xB0000H
OUT	IN	OUT	IN	xA0000H
OUT	IN	IN	OUT	x90000H
OUT	IN	IN	IN	x80000H
IN	OUT	OUT	OUT	x70000H
IN	OUT	OUT	IN	x60000H
IN	OUT	IN	OUT	x50000H
IN	OUT	IN	IN	x40000H
IN	IN	OUT	OUT	x30000H
IN	IN	OUT	IN	x20000H
IN	IN	IN	OUT	x10000H
IN	IN	IN	IN	x00000H §P

§P This identifies the PVAM default configuration.
§R This identifies the Real Mode default configuration.
Note: The starting address is always 0H.

4.2.3 DUAL-PORT DRAM CONFIGURATION

You now configure all or a portion of your local DRAM to be dual-port DRAM, which is accessible from the on-board CPU and other MULTIBUS masters. The 386/20P board is default configured for the full range of local DRAM to be dual-port DRAM.

You must configure both the starting and ending addresses of dual-port DRAM. The addresses are configured on 1M-byte and 256K-byte boundaries.

The 386/20P board's logic enables dual-port DRAM only if the requested address is greater than or equal to the configured starting address and less than or equal to the configured ending address. You can configure the local DRAM starting and ending addresses in six steps:

1. Choose your starting address

2. Configure the megabyte boundary from Table 4-5
   Install or remove the necessary jumpers

3. Configure the 256K-byte boundary from Table 4-6
   Install or remove the necessary jumpers

4. Choose your ending address

5. Configure the megabyte boundary from Table 4-7
   Install or remove the necessary jumpers

6. Configure the 256K-byte boundary from Table 4-8
   Install or remove the necessary jumpers

EXAMPLE

1. 1C0000H
2. 1xxxxxH E156-E157 OUT, E154-E155 OUT, E152-E153 OUT, E150-E151 IN
3. xC0000H E165-E166 IN, E163-E164 IN
4. 2BFFFFH
5. 2xxxxxH E161-E162 OUT, E159-E160 OUT, E174-E175 IN, E172-E173 OUT
6. xBFFFFH E170-E171 IN, E168-E169 OUT

There is an exception to this procedure:

1. Remember that the dual-port DRAM configuration is the same for PVAM or Real Mode. If the dual-port DRAM is configured in EPROM space, the space defaults to EPROM.

NOTE

Dual-port DRAM has the same address configuration for Real Mode and PVAM.

If a portion of the available DRAM is not configured in the local DRAM space but is configured in the dual-port DRAM space, you will create a memory resource available only to other MULTIBUS masters. You can avoid this by either configuring all available DRAM to be local DRAM or ensuring your dual-port DRAM configuration is located within your DRAM configuration.

By configuring the dual-port DRAM's ending address to be smaller than its starting address, you effectively disable dual-port memory, yet you still enable local DRAM accesses.

Table 4-5. Dual-Port DRAM Starting Address -- Megabyte Page Configuration

Jumpers Installed				Megabyte Addresses
E156-E157 ADR23	E154-E155 ADR22	E152-E153 ADR21	E150-E151 ADR20	
OUT	OUT	OUT	OUT	0xxxxxH §
OUT	OUT	OUT	IN	1xxxxxH
OUT	OUT	IN	OUT	2xxxxxH
OUT	OUT	IN	IN	3xxxxxH
OUT	IN	OUT	OUT	4xxxxxH
OUT	IN	OUT	IN	5xxxxxH
OUT	IN	IN	OUT	6xxxxxH
OUT	IN	IN	IN	7xxxxxH
IN	OUT	OUT	OUT	8xxxxxH
IN	OUT	OUT	IN	9xxxxxH
IN	OUT	IN	OUT	Axxxxxh
IN	OUT	IN	IN	Bxxxxxh
IN	IN	OUT	OUT	Cxxxxxh
IN	IN	OUT	IN	Dxxxxxh
IN	IN	IN	OUT	Exxxxxh
IN	IN	IN	IN	Fxxxxxh

§ Identifies the default configuration.
ADR This identifies the decimal address line number (ADR0 is LSB).
Note: This configures the starting address for Real Mode and PVAM.

Table 4-6. Dual-Port DRAM Starting Address -- 256K-byte Page Configuration

Jumpers Installed		256K-byte Addresses
E165-E166 ADR19	E163-E164 ADR18	
OUT	OUT	x00000H §
OUT	IN	x40000H
IN	OUT	x80000H
IN	IN	xC0000H

§ Identifies the default configuration.
ADR This identifies the decimal address line number (ADR0 is LSB).
Note: This configures the starting address for Real Mode and PVAM.

Table 4-7. Dual-Port DRAM Ending Address -- Megabyte Page Configuration

Jumpers Installed				Megabyte Addresses
E161-E162 ADR23	E159-E160 ADR22	E174-E175 ADR21	E172-E173 ADR20	
OUT	OUT	OUT	OUT	0xxxxxH
OUT	OUT	OUT	IN	1xxxxxH §
OUT	OUT	IN	OUT	2xxxxxH
OUT	OUT	IN	IN	3xxxxxH
OUT	IN	OUT	OUT	4xxxxxH
OUT	IN	OUT	IN	5xxxxxH
OUT	IN	IN	OUT	6xxxxxH
OUT	IN	IN	IN	7xxxxxH
IN	OUT	OUT	OUT	8xxxxxH
IN	OUT	OUT	IN	9xxxxxH
IN	OUT	IN	OUT	Axxxxxh
IN	OUT	IN	IN	Bxxxxxh
IN	IN	OUT	OUT	Cxxxxxh
IN	IN	OUT	IN	Dxxxxxh
IN	IN	IN	OUT	Exxxxxh
IN	IN	IN	IN	Fxxxxxh

§ Identifies the default configuration.
ADR This identifies the decimal address line number (ADR0 is LSB).
Note: This configures the ending address for Real Mode and PVAM.

Table 4-8. Dual-Port Ending Address -- 256K-byte Page Configuration

Jumpers Installed		256K-byte Addresses
E170-E171 ADR19	E168-E169 ADR18	
OUT	OUT	x3FFFFH
OUT	IN	x7FFFFH
IN	OUT	xBFFFFH
IN	IN	xFFFFFH §

§ Identifies the default configuration.
ADR This identifies the decimal address line number (ADR0 is LSB).
Note: This configures the ending address for Real Mode and PVAM.

4.2.4 MULTIBUS® MEMORY CONFIGURATION

The MULTIBUS memory space is memory available to the iSBC 386/20P board via the MULTIBUS interface. It is indirectly configured by the local EPROM and local DRAM configuration; the address range for the MULTIBUS interface is memory not configured as local EPROM or local DRAM.

The only exception is when the iSBC 386/20P board runs in PVAM. In this case, all addresses past 16M bytes (FFFFFFH) are unused, except the portion of memory used by local EPROM. This is because the MULTIBUS system can access only up to 16M bytes (24 address lines).

After you determine the MULTIBUS memory space, the iSBC 386/20P board's memory map is complete.

4.2.5 MEMORY CONFIGURATION EXAMPLE

Figure 4-2 is an example of how to configure memory for the iSBC 386/20P board. The example supports either addressing mode of the CPU. It also shows a memory map and lists all of the jumper connections required for configuring memory.

Parameters:

Local EPROM:	Two 27512 (64Kx8) EPROM components with 5 wait-states
DRAM Resource:	iSBC 402P (2M byte) memory board
Dual-Port DRAM:	100000H - 1FFFFFH in PVAM (1M byte)
MULTIBUS Memory:	64K-bytes in Real mode
CPU Mode:	Real mode or PVAM

Step 1. Determine your memory map.

Real Mode:	EPROM	128K bytes	E0000H-FFFFFH
	MULTIBUS Memory	64K bytes	D0000H-DFFFFH
	Local DRAM	832K bytes	00000H-CFFFFH
	Dual-port DRAM	none	
PVAM:	EPROM	128K bytes	FFFE0000H-FFFFFFFFH
	Unused Memory		01000000H-FFFDFFFFH
	MULTIBUS Memory	14M bytes	00200000H-00FFFFFFH
	Dual-port DRAM	1M byte	00100000H-001FFFFFH
	Local DRAM	1M byte	00000000H-000FFFFFH

(See the memory map at the end of this example.)

Step 2. Determine your local EPROM configuration.
Refer to Section 4.2.1.

2.1 EPROM Type Select -- 64Kx8 EPROM

E1-E3	In
E8-E9	In
E11-E12	In
E8-E10	Out
E11-E13	Out

2.2 EPROM Wait-State Select -- 5 wait-states

E106-E107	Out
E108-E109	In

2.3 EPROM Address Space

Real Mode:	E0000H-FFFFFH
PVAM:	FFFE0000H-FFFFFFFFH

Figure 4-2. Total Memory Configuration Example (continued)

Step 3. Determine your local DRAM ending address.
Refer to Section 4.2.2.

```
Local DRAM Ending Address
Real mode configuration --     832K bytes (00000H-CFFFFH)
PVAM configuration      --     full 2M bytes (00000000H-001FFFFFH)
                               of the 402P memory board

3.1   Real mode configuration -- Ending address = CFFFFH
                               -- Configuration address = D0000H
      E16-E19  OUT
      E22-E25  OUT   Select configuration address xD0000H
      E28-E31  IN    (From Table 4-4)
      E34-E37  OUT

3.2   PVAM configuration -- Ending address = 001FFFFFH
                         -- Configuration address = 00200000H
      E15-E18  IN
      E21-E24  IN    Select configuration address 2xxxxxH
      E27-E30  OUT   (From Table 4-3)
      E33-E36  IN

      E14-E17  IN
      E20-E23  IN    Select configuration address x00000H
      E26-E29  IN    (From Table 4-4)
      E32-E35  IN
```

Figure 4-2. Total Memory Configuration Example (continued)

Step 4. Determine your dual-port DRAM starting and ending addresses.
Refer to Section 4.2.3

Dual-port DRAM starting address for Real mode and PVAM:
Starting Address: 100000H
Ending Address: 1FFFFFH

NOTE

Since the starting and ending addresses are not part of local DRAM when the CPU is in Real Mode, the CPU cannot access any of the dual-port memory while it is in Real Mode.

4.1 Dual-port DRAM starting address = 100000H

E156-E157	OUT	
E154-E155	OUT	Select configuration address 1xxxxxH
E152-E153	OUT	(From Table 4-5)
E150-E151	IN	
E165-E166	OUT	Select configuration address x00000H
E163-E164	OUT	(From Table 4-6)

4.2 Dual-port DRAM ending address = 1FFFFFH

E161-E162	OUT	
E159-E160	OUT	Select configuration address 1xxxxxH
E174-E175	OUT	(From Table 4-7)
E172-E173	IN	
E170-E171	IN	Select configuration address xFFFFFH
E168-E169	IN	(From Table 4-8)

Step 5. Determine your MULTIBUS memory range and your unused memory range.
Refer to Section 4.2.4

Real Mode: MULTIBUS memory is all leftover, unconfigured memory.

PVAM: MULTIBUS memory is all leftover, unconfigured memory up to address FFFFFFH. Your unused memory is 1000000H to the beginning of EPROM space (FFFE0000H).

Figure 4-2. Total Memory Configuration Example (continued)

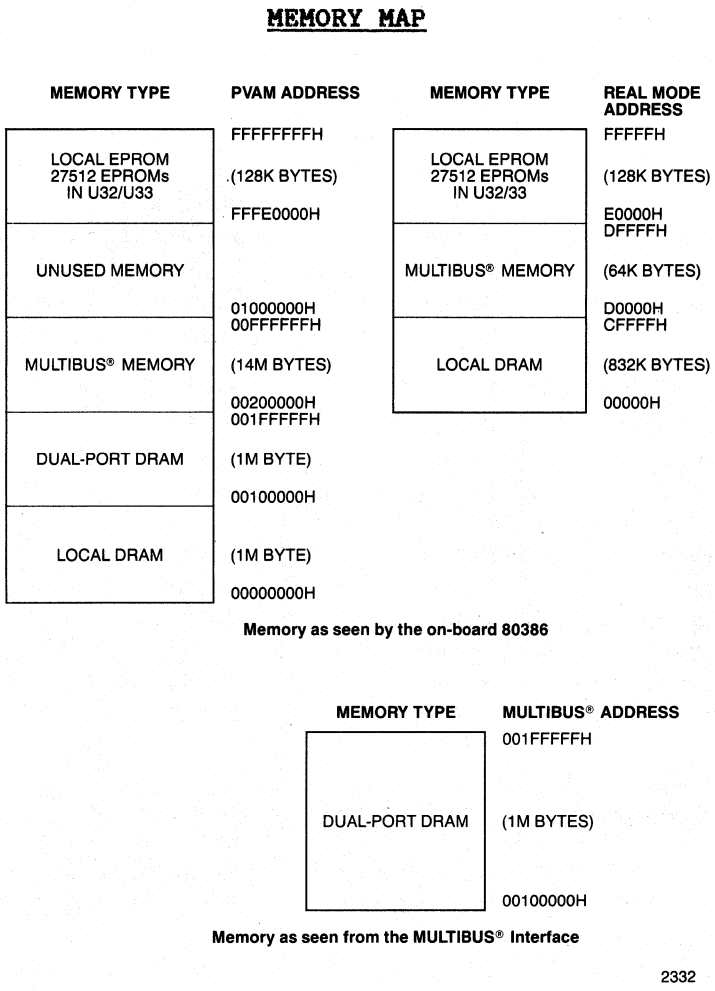


Figure 4-2. Total Memory Configuration Example (continued)

4.3 I/O CONFIGURATION

This section provides programming and configuration information for the on-board programmable devices and I/O registers, in the following order:

- Numeric Processor Extension (NPX -- 80287 Module)
- Programmable Interrupt Controllers (PICs -- 8259A)
- Programmable Interval Timer (PIT -- 8254)
- Serial Interface Programming (PCI -- 8251A)
- I/O Registers

Table 4-9 summarizes the I/O port addresses for the 386/20P board.

Table 4-9. iSBC® 386/20P I/O Port Addresses

I/O Port	Device	Size	Function
0080-8E Even	iSBX	Byte: Word:	8 or 16-bit iSBX, MCS0-Active 16-bit iSBX, MCS0 Active and MCS1 Active
0081-8F Odd	iSBX	Byte: Word:	16-bit iSBX, MCS1 Active None
0090-9E Even	iSBX	Byte:	8-bit iSBX, MCS1 Active
00C0	Master PIC	Byte:	Status, ICW1
00C2	Master PIC	Byte:	Mask
00C4	Slave PIC	Byte:	Status, ICW1
00C6	Slave PIC	Byte:	Mask
00D0	Timer	Byte:	Counter 0
00D2	Timer	Byte:	Counter 1
00D4	Timer	Byte:	Counter 2
00D6	Timer	Byte:	Control
00D8	Serial I/O	Byte:	8251A Data
00DA	Serial I/O	Byte:	8251A Control
00E0	PROT Control Register	Byte Write: Byte Read:	BD0 = 0 Set for Real Mode BD0 = 1 Set for PVAM Read PROT Status
00E2	Time Out	Byte Write:	BD0 = X Reset Time Out Latch
00E4	Processor Status Latch	Byte Write: Byte Read:	BD0 = 0 PSLTCH = 0 BD0 = 1 PSLTCH = 1 PSL Status
00E6	MULTIBUS Interrupt	Byte Write: Byte Read:	BD = 1 Set MULTIBUS Interrupt BD = 0 Reset MULTIBUS Interrupt Read Interrupt Status
00E8	Parity Error Latch	Byte Write:	BD0 = X Reset Parity Interrupt
00EA	NMI Mask	Byte Write: Byte Read:	BD0 = 1 Set the NMI Mask BD0 = 0 Reset the NMI Mask Read NMI Status
00EC-EE	Reserved		
00F0-FF	Reserved for Math		

4.3.1 NUMERIC PROCESSOR EXTENSION (NPX -- 80287 Math Module)

The 386/20P board includes an 80287 math module for performing high-speed floating-point numeric processing. The NPX operates asynchronously with the CPU; the NPX has its own independent clock source. The clock rate to the 80287 NPX device is not configurable. It uses a 24 MHz clock generator, located on the math module. The 80287 has an internal divide by three, resulting in 8 MHz numeric processing.

CAUTION

Ensure that jumper E39 - E43 is removed when the math module is mounted. Failure to do so will damage the 80287 device.

The CPU communicates with the NPX via four word-wide I/O port addresses. You initiate an NPX operation by placing an NPX instruction into the execution code for the CPU. When the CPU decodes an NPX instruction, it generates an I/O sequence that starts instruction execution in the NPX. The CPU can execute several NPX nonreferencing instructions while the NPX is executing. This allows the NPX time to complete the instruction before it receives the next one. Failure to do so causes the CPU to wait for a "done" status from the NPX (for the previous operation). For additional details on programming the 80287 NPX, refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK.

NOTE

To avoid corrupting NPX operation, ensure that your software never attempts to access I/O addresses in the range 00F8H-00FFH.

4.3.2 PROGRAMMABLE INTERRUPT CONTROLLERS (PICs -- 8259A)

The iSBC 386/20P board contains two (a master and a slave) 8259A Programmable Interrupt Controller (PIC) devices that control the interrupt logic on the board. The slave PIC is cascaded to the master PIC.

The 386/20P board can use the PICs in direct-vectored mode, but not in bus-vectored mode. Direct-vectored mode uses the automatic vectoring capabilities of the 8259A PIC devices. In direct-vectored mode, the master 8259A PIC provides an interrupt request to the CPU. When the CPU acknowledges the interrupt from the master PIC, the master PIC either provides the interrupt vector to the CPU, or if the slave PIC generated the interrupt, lets the slave PIC provide the interrupt vector to the CPU.

4.3.2.1 Interrupt Jumper Matrix Configuration

The iSBC 386/20P board contains an array of stake pins to configure the interrupt functions (see Figure 4-3). This section explains the default and optional configurations for the interrupt matrix.

The MULTIBUS interface can send or receive interrupts using the eight MULTIBUS interrupt lines, E132 through E139. Because MULTIBUS interrupts are received as active-low, they must be inverted to active-high to be connected to the PIC interrupt lines. Table 4-10 lists the jumper connections for these eight inverters. The two interrupts that can be sent to the MULTIBUS interface are at stake pins E125 (MULTIBUS interrupt under program control- MBINT) and E124 (dual-port DRAM parity error- MBPERR).

Tables 4-11 and 4-12 list the interrupt sources, and Table 4-13 lists the interrupt destinations. Table 4-14 lists the default jumper configuration for the interrupt levels of each PIC device on the board.

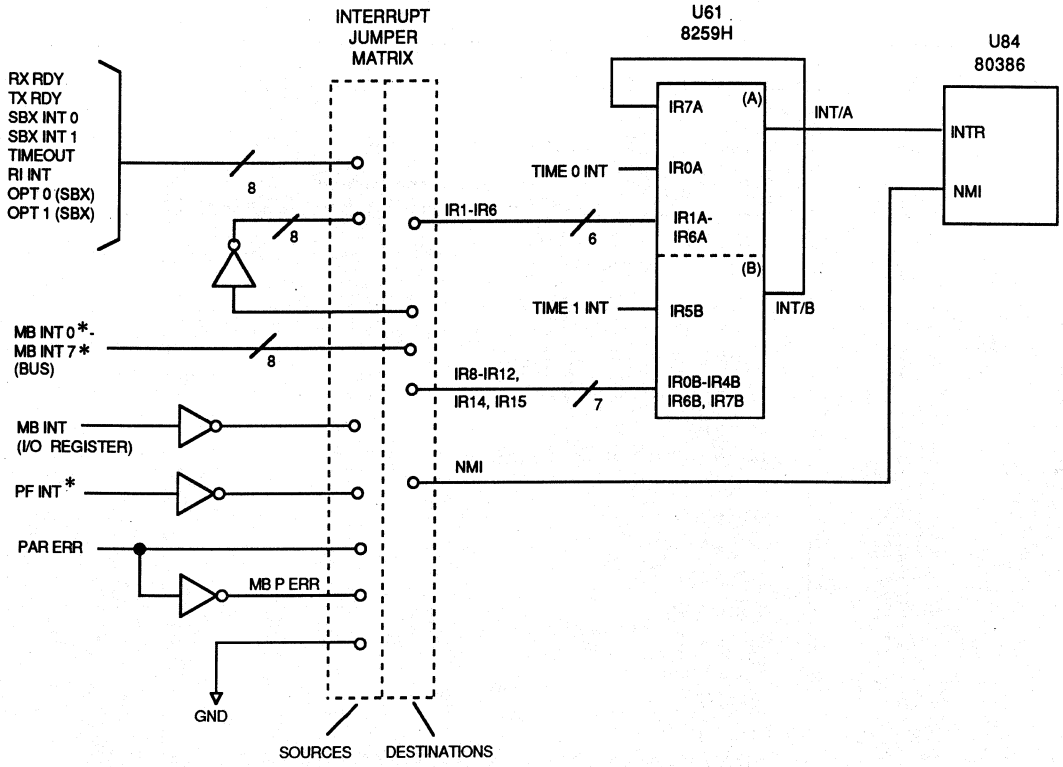


Figure 4-3. Interrupt Jumper Matrix

Table 4-10. Inverter Configuration for MULTIBUS® Interrupts

Input Jumper (connect to a MBINT)	Output Stake Pin (connect to a PIC input)	MULTIBUS Interrupt
E132-E141 §	E46	MBINT7*
E133-E142 §	E42	MBINT6*
E134-E143 §	E68	MBINT5*
E135-E144 §	E62	MBINT4*
E136-E145 §	E65	MBINT3*
E137-E146 §	E58	MBINT2*
E138-E147 §	E54	MBINT1*
E139-E148	E50	MBINT0*

§ identifies the default configuration.

Table 4-11. Interrupt Sources for the PICs

Stake Pin	Interrupt Sources
E38	Ringing indicator interrupt
E40	RxRDY receiver ready input for the 8251A
E48	TxRDY (Transmitter Ready) from the 8251A
E56	iSBX interrupt 1
E63	iSBX interrupt 0
E66	Time-out interrupt
E69	Power fail interrupt (input source for NMI)
E71	iSBX option 0 line
E73	Parity error input
E74	Ground
E76	iSBX option 1 line
E46†	MBINT7*
E42†	MBINT6*
E68†	MBINT5*
E62†	MBINT4*
E65†	MBINT3*
E58†	MBINT2*
E54†	MBINT1*
E50†	MBINT0*
HW	PIT Counter 0 to master PIC IR0
HW	Slave PIC interrupt request to master PIC IR7
HW	PIT Counter 1 to slave PIC IR5

† when configured according to Table 4-10.
HW designates a hard-wired (nonconfigurable) interrupt source.

Table 4-12. Interrupt Sources for the MULTIBUS® Interface

Stake Pin	Interrupt Sources
E124	Dual-port DRAM parity error interrupt
E125	Interrupt under program control, using I/O register address 00E6H

Table 4-13. Interrupt Destinations to the PICs, NMI, and MULTIBUS® Interface

Stake Pin	Interrupt Destinations
E41	IR1 of the Master PIC
E45	IR2 of the Master PIC
E49	IR3 of the Master PIC
E53	IR4 of the Master PIC
E57	IR5 of the Master PIC
E61	IR6 of the Master PIC
E64	IR0 of the Slave PIC
E75	IR1 of the Slave PIC
E70	IR2 of the Slave PIC
E67	IR3 of the Slave PIC
E60	IR4 of the Slave PIC
E52	IR6 of the Slave PIC
E44	IR7 of the Slave PIC
E72	NMI input into the 80386
E132	MBINT7*
E133	MBINT6*
E134	MBINT5*
E135	MBINT4*
E136	MBINT3*
E137	MBINT2*
E138	MBINT1*
E139	MBINT0*

Table 4-14. Default 8259A Interrupt Level Configuration

Level	PIC	Jumper	Location	Function
IR0		None	8254 PIT	Output from Counter 0 of the 8254 PIT
IR1	M	E41-E54	Interrupt Matrix	MULTIBUS Interrupt 1
IR2	A	E45-E58	Interrupt Matrix	MULTIBUS Interrupt 2
IR3	S	E49-E65	Interrupt Matrix	MULTIBUS Interrupt 3
IR4	T	E53-E62	Interrupt Matrix	MULTIBUS Interrupt 4
IR5	E	E57-E68	Interrupt Matrix	MULTIBUS Interrupt 5
IR6	R		Interrupt Matrix	Configurable
IR7		None	8259 Slave PIC	Interrupt signal from the slave PIC
IR0		E64-E42	Interrupt Matrix	MULTIBUS Interrupt 6
IR1		E75-E46	Interrupt Matrix	MULTIBUS Interrupt 7
IR2	S		Interrupt Matrix	Configurable
IR3	L		Interrupt Matrix	Configurable
IR4	A		Interrupt Matrix	Configurable
IR5	V	None	8254 PIT	Output from Counter 1 of the 8254 PIT
	E			
IR6			Interrupt Matrix	Configurable
IR7			Interrupt Matrix	Configurable

4.3.2.2 PIC Programming

You can use four I/O port addresses to program the operation of the PIC devices on the iSBC 386/20P board. Table 4-15 lists these addresses and the functions performed by each.

You select direct-vectored mode by initializing the 8259A PIC devices and by configuring the interrupt signals to the PIC interrupt inputs. Each PIC must specify the vector base (use CALL address interval of 4) in Interrupt Control Word Two (ICW2). The master PIC must specify in ICW3 that interrupt level 7 is the slave PIC. The slave PIC is programmed in ICW3 that its cascade ID number is 7. Each PIC must also specify in ICW4 that 8086 and buffered mode is selected. For more 8259A PIC programming details, refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK.

Table 4-15. Port Addresses for the 8259A PIC Devices

I/O Address	Device	Operation	Function Performed
00C0H	Master PIC	Byte Read: Byte Write: Word:	Status and Poll Registers ICW1, OCW2, and OCW3 Parameters N/A
00C2H	Master PIC	Byte Read: Byte Write: Word:	Mask Register or OCW1 Parameter Mask Register or ICW2, ICW3, ICW4, and OCW1 Parameters N/A
00C4H	Slave PIC	Byte Read: Byte Write: Word:	Status and Poll Registers ICW1, OCW2, and OCW3 Parameters N/A
00C6H	Slave PIC	Byte Read: Byte Write: Word:	Mask Register or OCW1 Parameter Mask Register or ICW2, ICW3, ICW4, and OCW1 Parameters N/A

NOTE

To avoid unexpected interrupts, you should mask all unused inputs to the PIC devices during initialization.

Each PIC must be programmed, even if only one is used. Otherwise, bus contention could result on the cascaded lines.

4.3.3 PROGRAMMABLE INTERVAL TIMER (PIT -- 8254)

An 8254 Programmable Interval Timer (PIT) provides three 16-bit interval timers used to generate real-time interrupts and baud rates on the iSBC 386/20P board. There are no jumper options, only programming options.

The timer's inputs and outputs are hard-wired and cannot be reconfigured by jumpers. The clock input to the timers is 1.23 MHz, which the counters can use to generate most common baud rates. Since the counter's outputs do not have jumper options, the counters cannot be cascaded. The outputs are configured as follows:

- Counter 0: interrupt timer for IR0 on the master PIC.
- Counter 1: interrupt timer for IR5 on the slave PIC.
- Counter 2: baud rate generator providing a Transmit/Receive Clock (TxC, RxC) for the serial controller (8251A PCI).

You program the 8254 PIT by using the even I/O port addresses between 00D0H and 00D6H as listed in Table 4-16.

Table 4-16. I/O Port Addresses for the 8254 PIT

I/O Address	Device	Operation	Function Performed
00D0H	PIT Counter 0	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
00D2H	PIT Counter 1	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
00D4H	PIT Counter 2	Byte Read: Byte Write: Word:	LSB or MSB of count value LSB or MSB of count value N/A
00D6H	PIT Control Word Register	Byte Read: Byte Write: Word:	N/A Control Word Register Parameter N/A

4.3.4 SERIAL INTERFACE PROGRAMMING (PCI -- 8251A)

You control the RS-232C channel on Connector J1 by programming the 8251A PCI device at the two I/O port addresses listed in Table 4-17. For more programming information, refer to Intel's MICROSYSTEM COMPONENTS HANDBOOK. There are no jumper configurations for the 8251A component.

Table 4-17. Serial I/O Port Addresses

Port Address	Type Of Operations Available
00D8H	Byte: Data Word: N/A
00DAH	Byte: Control Word: N/A

4.3.5 I/O REGISTERS

The I/O Control Registers allow the iSBC 386/20P to change as well as read the status of its environment. All the registers are contained in component U78. Table 1-1 summarizes the functions of the four LEDs, some of which are controlled by these I/O registers. The following sections explain each I/O register.

4.3.5.1 PROT Register (I/O Address 00E0H)

This register configures the board decode logic for operation in either Real mode or PVAM. Writing to this port with even data (bit 0 = 0) configures it for Real mode. Writing to this port with odd data (bit 0 = 1) configures it for PVAM.

When this port is read, it describes the board's operating mode. On power up, PROT = 00H (Real Mode). You have the choice, at that point, to either use the CPU in Real mode or further initialize the CPU into PVAM.

In addition to setting the decode logic to PVAM, you must also set the CPU to PVAM. The sequence to switch both the CPU and the board to PVAM is as follows:

1. Switch the CPU's mode to PVAM by setting bit 0 within the Machine Status Word register in the CPU using the LMSW instruction.

NOTE

Before performing the next step, you must store the descriptor tables into DRAM and adjust them for accessing EPROM at the top of 4 gigabytes. Refer to the iAPX 286 OPERATING SYSTEMS WRITER'S GUIDE for more specific information.

2. Switch the iSBC 386/20P board to PVAM by performing a byte write operation with an odd data value to the PROT register, at I/O address 00E0H.

NOTE

You must switch the CPU to PVAM before switching the iSBC 386/20P board to PVAM. Switching the board first will cause the system to hang, because the memory map is relocated.

4.3.5.2 Time-Out Register (I/O Address 00E2H)

This section explains the time-out protocol as well as how to use the time-out register.

For MULTIBUS requests, the time-out signal goes active for two reasons:

1. If the bus is not acquired 10 msec after the CPU requests a MULTIBUS cycle

2. If the bus is acquired and the MULTIBUS XACK signal is not received within 10 msec of acquiring the bus

For iSBX requests, the time-out signal is triggered if MWAIT* is still active 10 msec after the request.

Jumper E2-E4 enables the time-out register and ready signals. Jumper E4-E6 disables the time-out circuitry.

The red LED (DS2) comes on when a time-out occurs. You can turn off the LED and reset the time-out register by writing any value to I/O address 00E2H. The status of the LED cannot be read by software.

The time-out signal is available at the interrupt matrix at pin E66, which may be connected to a PIC interrupt input. The program can then recognize this interrupt as a time-out error and run a service interrupt routine, part of which would reset the time-out register. If the interrupt jumper is connected, the time-out interrupt will stay active (latched active high) until it is reset.

4.3.5.3 Processor Status Latch (I/O Address 00E4H)

This latch can set or reset the green LED (DS3) based on a state controlled by your program. A write to this location with odd data will turn on the LED. A write to this location with even data will turn off the LED. The same data can relay the status to the CPU when it is read from I/O address 00E4H.

4.3.5.4 MULTIBUS Interrupt Register (I/O Address 00E6H)

This feature enables the iSBC 386/20P to interrupt another processor within the MULTIBUS system. Stake pin E125 carries the interrupt signal, which may be connected to any MULTIBUS interrupt line.

A write to I/O address 00E6H with odd data will activate this interrupt line; a write with even data will deactivate the interrupt. The 386/20P board can determine if it has been serviced by reading the state of the register.

4.3.5.5 On-Board Parity Error Latch (I/O Address 00E8H)

When a parity error occurs during a dual-port DRAM operation, the parity latch is enabled, which produces an interrupt and lights the red LED (DS4). A write to I/O address 00E8H, regardless of the data, will reset this latch. This latch cannot be read.

4.3.5.6 NMI Mask Latch (I/O Address 00EAH)

This latch enables and disables parity. Writing odd data to this location disables parity error generation; writing even data enables the parity error generation circuitry. Reading from this location gives the NMI latch's status.

NOTE

Intel uses two registers at I/O addresses 00ECH and 00EEH for internal testing. Ensure your program never accesses these I/O locations, or your board will operate unpredictably.

4.4 INTERFACE CONFIGURATION

This section explains the three I/O interfaces on the iSBC 386/20P board and supplies the interface's pinouts and jumper configurations. The interfaces will be covered in this order:

- Serial I/O Interface
- MULTIBUS Interface
- Auxiliary Interface
- iSBX Interface

4.4.1 SERIAL I/O INTERFACE -- CONNECTOR J1

The iSBC 386/20P board provides one RS-232C 10-pin (9 lead) serial I/O interface on Connector J1. It is configured to operate as a Data Terminal Equipment (DTE) device which supports the IBM 9-pin DTE serial standard. Section 3.5 shows the cable assembly to interface J1 to a 9-pin DCE, 25-pin DCE, and 25-pin DTE connector. Table 4-18 lists the pin assignments and signals on each pin of Connector J1.

The serial interface has only one jumper option: the configuration of the Ringing Indicator (RI) from the interface to an interrupt. Section 4.3.2.1 explains how to connect RI to a PIC interrupt.

Refer to EIA standard RS-232C for the specific AC/DC specifications for the serial interface.

Table 4-18. Connector J1 RS-232C Pin Assignment

J1 Pin Number	RS-232C Signal Name	RS-232C Signal Function
1	nc	No Connection
2	GND	Ground
3	RI	Ring Indicator (input)
4	DTR	Data Terminal Ready (output)
5	CTS	Clear to Send (input)
6	TD	Transmit Data (output)
7	RTS	Request to Send (output)
8	RD	Receive Data (input)
9	nc	No Connection
10	CD	Carrier Detect (input)

4.4.2 MULTIBUS® INTERFACE -- CONNECTOR P1

The iSBC 386/20P board contains an 86-pin MULTIBUS connector (P1) for interfacing to other system's functions. Memory accessed off-board via the MULTIBUS interface is explained in Section 4.2.4. The following sections describe the interface and how you can change its operation.

Refer to the INTEL MULTIBUS SPECIFICATION for the pin assignments and AC/DC characteristics of Connector P1.

4.4.2.1 MULTIBUS® Interface Description

The MULTIBUS interface on the iSBC 386/20P board complies with the IEEE 796 Microcomputer Systems Bus Standard, as follows:

MULTIBUS compliance: MASTER D16 M24 I16 V0 L

- The "MASTER" means that the board supports either master or slave operation on the MULTIBUS interface.
- The "D16" means either an 8- or 16-bit data path.
- The "M24" means a 24-bit memory address path.
- The "I16" means either an 8- or 16-bit I/O address path.
- The "V0" means that the board supports only non-bus-vectored interrupt requests.
- The "L" means that the board supports level triggered interrupt sensing.

4.4.2.2 MULTIBUS® Interface Configurations

By configuring the jumpers listed in Table 4-19, you can control these MULTIBUS interface features:

- Lock -- enables you to prevent other MULTIBUS agents from acquiring the MULTIBUS interface.
- Initialize -- enables you to reset other agents on the MULTIBUS interface.
- Arbitration technique -- enables the iSBC 386/20P board to use MULTIBUS systems with parallel or serial arbitration techniques.
- Bus clocks -- enables the iSBC 386/20P board to drive MULTIBUS synchronization clocks.
- Bus release -- enables you to determine the conditions for releasing the interface.

Table 4-19. MULTIBUS® Interface Jumpers

Jumper	Signal Name	Description
E122-E123	BCLK* Bus clock	Provides a common Bus Clock from the iSBC 386/20P board to all MULTIBUS boards.
E118-E119	CCLK* Constant clock	Provides a common Constant Clock from the iSBC 386/20P board to all MULTIBUS boards (CCLK is 180 degrees out of phase with BCLK).
E116-E117	MBLOCK* MULTIBUS LOCK	Allows the iSBC 386/20P board to generate the MBLOCK* signal to the MULTIBUS interface. MBLOCK* prevents another master from gaining control of the MULTIBUS interface.
E140-E149	INIT Initialize	Allows the iSBC 386/20P board to drive INIT onto the MULTIBUS interface to initialize (reset) other masters or slaves.
E120-E121	BPRO* Bus Priority Out	Active only when the iSBC 386/20P board is passing control of the MULTIBUS interface to another board (useful only in serial priority resolution schemes and removed in parallel priority schemes).
E130-E131 E129-E131	CBRQ* Common Bus Request	Refer to Table 4-20.
E126-E127 E127-E128	ARQST* Any Request (ANYRQST)	Refer to Table 4-20.

Note: § identifies the default jumper configuration.

The bus clock jumpers (BCLK* and CCLK*) allow the iSBC 386/20P board to provide two clocks that supply timing for the bus contention and synchronization logic on other master boards on the MULTIBUS interface. By removing the clock jumpers, you can allow another master board to provide the system timing signals on the MULTIBUS interface. Ensure, however, that you have only one MULTIBUS system board driving each MULTIBUS interface clock signal.

You can select either parallel or serial arbitration for the MULTIBUS system bus. The bus priority resolution jumper (BPRO*) on the iSBC 386/20P board is installed for serial arbitration, and it is removed for parallel arbitration. (The MICROSYSTEM COMPONENTS HANDBOOK provides more information about the 8289 bus arbiter and its arbitration schemes).

Generally, higher priority masters can obtain the MULTIBUS interface when a lower priority master completes its present transfer cycle, and lower priority masters obtain the bus when a higher priority master is not using the system bus. However, the bus release jumpers (ARQST* and CBRQ*) allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. Table 4-20 lists the three release modes of the arbiter and their jumper configurations.

Table 4-20. MULTIBUS® Interface Release Modes

Release Mode	Jumper Connect	CBRQ* State	ARQST* State	Description
1	E127-E128	N/A	Low	The bus arbiter surrenders control only to a higher priority request.
2	E126-E127 E129-E130	Low	High	The bus arbiter releases control of the interface after each transfer cycle, whether or not there is another request.
3 §	E126-E127 E130-E131	Bus (High or Low)	High	The bus arbiter surrenders control on any request (higher or lower) after it completes its current bus cycle.

Note: The bus arbiter always releases the bus on sensing a HALT condition.
§ Identifies the default jumper configuration.

In release mode 1, the arbiter releases the bus only to a higher priority arbiter.

In mode 2, the arbiter releases the bus at the end of each transfer cycle. For multiple transfers, this requires the arbiter to acquire and release the bus for each transfer, even if another arbiter is not requesting the bus.

In mode 3 (the default configuration), the arbiter releases the bus only when another arbiter of higher or lower priority requests it. The major difference between modes 2 and 3 is that mode 3 does not waste time acquiring and releasing the bus for multiple transfers.

4.4.3 AUXILIARY INTERFACE -- CONNECTOR P2

The iSBC 386/20P board contains an auxiliary connector (P2) for additional system interfacing. The following sections describe this interface.

4.4.3.1 Auxiliary Interface Description

The connector supplies ALE to the front panel and the upper four address lines to the MULTIBUS interface, receives auxiliary reset from the front panel, receives console lock from the keyboard or system front panel, and receives the power fail interrupt signal from the system's power sensing circuitry. Table 4-21 shows the pin assignments and signal names of the connector. Table 4-22 shows the DC characteristics of the connector.

Table 4-21. Connector P2 Pin Assignments

Component Side		Solder Side	
Pin Number	Signal	Pin Number	Signal
19	PFIN*	32	ALE
		34	CONSLCK*
		38	AUXRES*
55	ADR22*	56	ADR23*
57	ADR21*	58	ADR20*

Note: All unlisted pin descriptions have no signals attached to them.

Table 4-22. Connector P2 Interface DC Characteristics

Signal	Parameter/Conditions	Minimum	Maximum	Units
PFINT* (input)	Vih	2.0	---	V
	Vil	---	0.8	V
	Iih @ 2.4V	---	40	uA
	Iil @ 0.4V	---	-1.6	mA
ALE* (output)	Voh @ Ioh = -200uA	2.4	-	V
	Vol @ Iol = 8mA	-	0.4	V
CONSLCK* (input)	Vih	2.0	---	V
	Vil	---	0.8	V
	Iih @ 2.4V	---	20	uA
	Iil @ 0.4V	---	0.6	uA
AUXRES* (input)	Vih	---	---	
	Vil	---	0.8	V
	Iih	---	50	uA
	Iil @ 0.4V	---	-2.0	mA
ADR20-23* (input/ output)	Vih	2.4	---	V
	Vil	---	0.8	V
	Iih @ 2.4V	---	125	uA
	Iil @ 0.4V	---	-5.5	mA

4.4.4 iSBX™ INTERFACE -- CONNECTOR J2

The iSBC 386/20P board contains one 36/44-pin iSBX bus connector, labeled Connector J2, for 8- or 16-bit I/O expansion. The following sections provide the interface description, configuring information, and programming information.

4.4.4.1 iSBX™ Bus Description

The iSBX bus interface complies with the INTEL iSBX BUS SPECIFICATION as follows:

D16/16 I

- The "D16/16" means this 16-bit baseboard can support either an 8- or 16-bit expansion module.
- The lack of a "D" means that the board does not support DMA operations to the iSBX bus connector.
- The "I" means it supports interlocked read and write operations (using MWAIT*).

Refer to the INTEL iSBX BUS SPECIFICATION for a description of the pin assignments and AC/DC characteristics of Connector J2.

4.4.4.2 iSBX™ Interface Configurations

You can configure the iSBX bus interface via programming and jumper configurations:

- Select either 8- or 16-bit interface operation for the iSBX bus interface. You do this when you select the type of MULTIMODULE board to interface to the iSBX connector (8- or 16-bit) and configuring the jumper as listed in Table 4-23.

- If required, configure the two jumper pins for the option signal lines (OPT0 and OPT1) and iSBX interrupt lines (SBXINT1 and SBXINT0) to a PIC interrupt. These jumpers are described further in Section 4.3.2.1.

Table 4-23. iSBX™ Interface Configuration

Jumper Number E5-E7	iSBX™ Function
IN	Accepts 16-bit iSBX MULTIMODULE boards
OUT	Accepts 8-bit iSBX MULTIMODULE boards

4.4.4.3 iSBX™ Interface Addressing

The iSBC 386/20P board reserves all I/O port addresses in the range 0080H through 009FH as on-board addresses for the iSBX bus connector.

Table 4-24 lists the iSBX I/O port addresses for the board. Notice that the port addresses are listed for two configurations: an iSBC 386/20P board with an 8-bit MULTIMODULE board, and an iSBC 386/20P board with a 16-bit MULTIMODULE board. You can find details on the functions available at each I/O port address by referring to the manual for the specific MULTIMODULE board that you are using.

Suppose, for example, the 8-bit iSBX 351 Serial MULTIMODULE board is installed. To program the MULTIMODULE board's PIT Counter 0 requires address Z0 or Z8 (Z designates the base address activating MCS1*-- 009 in this case), as found in the MULTIMODULE board's Hardware Reference Manual. Either address, 0090 or 0098, would be correct.

Table 4-24. I/O Port Addresses for iSBX™ Connector

Port addresses for the 386/20P board with an 8-bit MULTIMODULE board

MCS1* Active
009F or 009E
009D or 009C
009B or 009A
0099 or 0098
0097 or 0096
0095 or 0094
0093 or 0092
0091 or 0090

MCS0* Active
008F or 008E
008D or 008C
008B or 008A
0089 or 0088
0087 or 0086
0085 or 0084
0083 or 0082
0081 or 0080

Port addresses for the 386/20P board with a 16-bit MULTIMODULE board

MCS1* Active	MCS0* Active
008F	008E
008D	008C
008B	008A
0089	0088
0087	0086
0085	0084
0083	0082
0081	0080

***

CHAPTER 5
SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides schematic diagrams, and service and repair assistance instructions for the iSBC 386/20P Single Board Computer.

5.2 SERVICE DIAGRAMS

The parts location diagram for the iSBC 386/20P board is shown in Figure 3-1. Table 5-1 provides a schematic mini-index for the 386/20P board. The schematic diagrams for the 386/20P board and the 80287 math module are shipped with the 386/20P board. The schematics for the 402P or 404P memory board are shipped with the memory board. On the schematic diagram, a signal mnemonic ending with an asterisk (e.g., RIINT*) is active low. Conversely, a signal mnemonic without an asterisk (e.g., RIINT) is active high.

5.3 SERVICE AND REPAIR ASSISTANCE

Customer Support Service Engineering provides both a Return Replacement Authorization (RRA) and Direct Return Authorization (DRA) service.

The RRA service replaces a defective product. Return the defective product to Intel with the freight prepaid. Intel will replace the product, bearing a new serial number. This service is not offered on all products and is subject to availability. Typically, Intel ships the replacement product within 48 hours of receiving the defective product.

The DRA service provides repair work. Return the defective product to Intel, freight prepaid. Intel will repair, test, and update the product with Engineering Change Orders. The serial number will not change. Normal turnaround time is four to six weeks from receipt of the defective product.

Determine which service you need, RRA or DRA. Before calling Customer Support Service, have the necessary information ready (see Figure 5-1 for the telephone number for your area):

a. Part and serial number of the product.

b. Purchase order number, for repair and shipping charges.

c. If it is a warranty repair, the proof of purchase showing the product was received within 90 days of the service request date. Without proof, services will be billed at the current rate.

d. Your shipping and billing addresses.

e. Your telephone number.

In correspondence with Customer Support Service, reference the authorization number on the packing slip, the purchase order, and any other related documents.

Before shipping, remove all user modifications. Protect the equipment from damage in transit:

a. Place boards in antistatic bags and then in padded shipping bags. Wrap power supplies and other large items in antistatic material.

b. Protect the product with protective padding such as flow pack or foam.

c. Write the return authorization number on the outside of the box and label it "FRAGILE."

NOTE

Damage due to lack of compliance with safe return packaging could result in extra repair charges.

d. Forward the product and all correspondence to this address:

Intel Corporation
Customer Support Marketing Administration
Billing Department - DV-1-704
2402 W. Beardsley Road
Phoenix, Arizona 85027
Authorization # _____

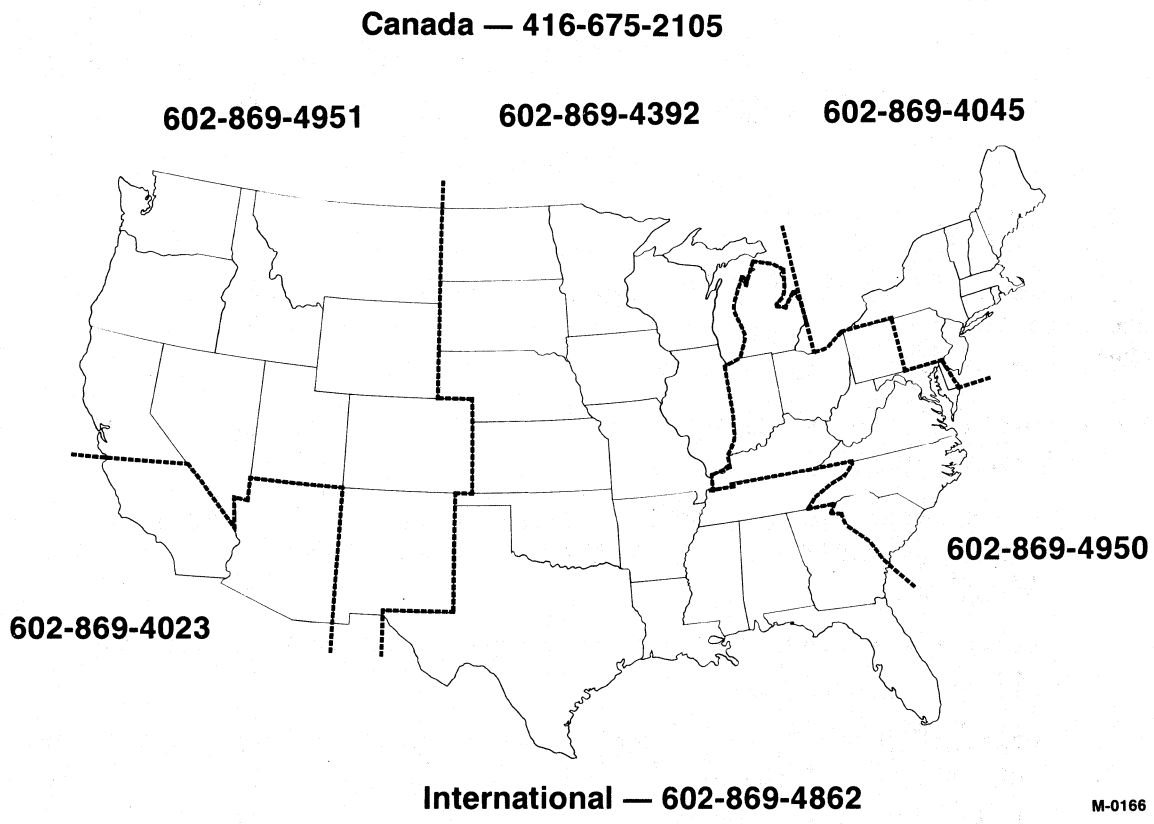


Figure 5-1. Territorial Service Telephone Numbers

Table 5-1. iSBC® 386/20P Board's Schematic Index

Item	Schematic Sheet Number
CPU AND SUPPORT	
CPU (80386)	6 & 7
Clock Generators (82284, GI)	8
80287 Math Module Socket	9
Status LEDs	30
MULTIBUS Arbiter (8289)	35
PROGRAMMABLE COMPONENTS	
PICa (Master) PICb (Slave) PITc (all on 8259H)	30
Interrupt Jumper Matrix	32
Serial Controller (8251A)	31
MEMORY	
Local EPROM	29
Cache Memory	23
CONNECTORS	
P1 MULTIBUS Connector	38
P2 Auxiliary Interface	39
P3 iSBC 402P/404P Memory Board Interface (MM2 interface for local and dual-port DRAM)	40
J1 RS-232C Serial Port	29
J2 iSBX Interface	33

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APPENDIX A
JUMPER AND DEFAULT INFORMATION

A.1 INTRODUCTION

This appendix provides an overview of the jumpers on the iSBC 386/20P board. It is designed as a quick reference; refer to Chapter 4 for specific configuration information. Table A-1 summarizes the board's default configuration. Table A-2 lists all the jumpers and their functions. Table A-3 lists the stake pin schematic index for the stake pins and default jumpers. Figure A-1 shows the location of the jumpers on the iSBC 386/20P board.

Table A-1. Default Summary for the iSBC® 386/20P Board

MEMORY

Local EPROM	Set for 27256 (32Kx8) components	
	F0000H - FFFFFH	(CPU in Real mode)
	FFFF0000H - FFFFFFFFH	(CPU in PVAM)
Cache Memory	Set for 4Kx4 SRAM devices (not configurable)	
Local DRAM	00000H - DFFFFH	(CPU in Real mode)
(using the 2M-byte 402P memory board)	000000H - 1FFFFFH	(CPU in PVAM)
Dual-port DRAM	000000H - 1FFFFFH	(independent of CPU mode)
	(The local CPU cannot access 0E0000H-1FFFFFH when in Real mode)	

MULTIBUS INTERFACING

The board is enabled to drive INIT* onto the MULTIBUS interface.
The board is enabled to drive MBLOCK* onto the MULTIBUS interface.
The board is enabled to drive CCLK* onto the MULTIBUS interface.
The 8289A ARQST* line is connected high.
The 8289A CBRQ* line is connected to the MULTIBUS system bus.

INTERRUPT MATRIX

Parity error interrupt is connected to NMI.
MBINT1* through MBINT7* are connected to inverters.
RxRDY is connected to IR6 of the slave PIC.
TxRDY is connected to IR7 of the slave PIC.
MBINT1 is connected to IR1 of the master PIC.
MBINT3 is connected to IR3 of the master PIC.
MBINT4 is connected to IR4 of the master PIC.
MBINT5 is connected to IR5 of the master PIC.
MBINT6 is connected to IR0 of the slave PIC.
MBINT7 is connected to IR1 of the slave PIC.
SBXINT0 is connected to IR3 of the slave PIC.
SBXINT1 is connected to IR4 of the slave PIC.

OTHER

Time-out circuitry is enabled.
Cache memory uses 4Kx4 SRAMs (not reconfigurable).

Table A-2. Numerical List of Jumpers and their Functions

Jumper Number	Functions
E1-E3 E8 thru E13	Selects EPROM size for U32/U33. See Section 4.2.1.
E2, E4, E6	Configures the time-out circuitry.
E5-E7	Selects an 8-bit or 16-bit iSBX module.
E14 thru E37	Configure the ending address for local DRAM. See Section 4.2.2.
E38	Ringing indicator interrupt
E39-E43	Must be out when the 80287 Math Module is installed.
E40	RxRDY (Receiver Ready) input for the 8251A
E41	IR1 of the Master PIC
E42	Inverts the signal connected to E142, which make a MULTIBUS interrupt input active high.
E44	IR7 of the Slave PIC
E45	IR2 of the Master PIC
E46	Inverts the signal connected to E141, which makes a MULTIBUS interrupt input active high.
E47-E51	Reserved. Pulls up 387CLK2 input.
E48	TxRDY (Transmitter Ready) output from the 8251A
E49	IR3 of the Master PIC
E50	Inverts the signal connected to E148, which makes a MULTIBUS interrupt input active high.
E52	IR6 of the Slave PIC
E53	IR4 of the Master PIC
E54	Inverts the signal connected to E147, which makes a MULTIBUS interrupt input active high.
E55-E59	Reserved. Causes 82384 to select EFI input to generate clocks.
E56	iSBX interrupt 1
E57	IR5 of the Master PIC
E58	Inverts the signal connected to E146, which makes a MULTIBUS interrupt input active high.
E60	IR4 of the Slave PIC
E61	IR6 of the Master PIC

(continued)

Table A-2. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E62	Inverts the signal connected to E144, which makes a MULTIBUS interrupt input active high.
E63	iSBX interrupt 0
E64	IR0 of the Slave PIC
E65	Inverts the signal connected to E145, which makes a MULTIBUS interrupt input active high.
E66	Time-out interrupt
E67	IR3 of the Slave PIC
E68	Inverts the signal connected to E143, which makes a MULTIBUS interrupt input active high.
E69	Power fail interrupt input
E70	IR2 of the Slave PIC
E71	iSBX option 0 line
E72	NMI input into the 80386 CPU
E73	Parity error input
E74	Ground
E75	IR1 of the Slave PIC
E76	iSBX option 1 line
E77-E78	Configures 80287 mth module for synchronous or asynchronous mode. Must be in for the preproduction board (asynchronous operation).
E79-E81 E82-E83 E85-E87 E88-E89 E91-E93 E94-E95 E97-E99 E100-E101 E103-E105	These jumpers configure the cache and tag with 4Kx4 Static RAM devices. This is the default configuration and is not reconfigurable.
E80-E81 E82-E84 E86-E87 E88-E90 E92-E93 E94-E96 E98-E99 E100-E102 E104-E105	These jumpers configure the cache and tag with 16Kx4 Static RAM devices. This is not a configurable option.

(continued)

Table A-2. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E106, E107 E108, E109	These jumpers configure the number of wait-states for local EPROM. See Section 4.2.1.
E110, E111 E112, E113	These jumpers determine the refresh timing for DRAM, which depends on the CPU's operating speed. Not configurable.
E114-E115	It enables the iSBC 386/20 board to use the 402P/404P board with 150 nsec or faster DRAMs (adds one wait-state to 120 nsec timing). Not configurable.
E116-E117	Drives lock to the MULTIBUS interface
E118-E119	Drives CCLK* to the MULTIBUS interface
E120-E121	Enables 8289 BPRO* pin to the MULTIBUS interface's BPRO* line
E122-E123	Drives BCLK* to the MULTIBUS interface
E124	Parity error connection for generating a MULTIBUS interrupt
E125	MULTIBUS interrupt under program control
E126-E127	Straps 8289 Any Request input high
E127-E128	Straps 8289 Any Request input low
E129-E130	Straps 8289 CBRQ* input low
E130-E131	Enables 8289 CBRQ* pin to the MULTIBUS interface's CBRQ* line
E132	MBINT7*
E133	MBINT6*
E134	MBINT5*
E135	MBINT4*
E136	MBINT3*
E137	MBINT2*
E138	MBINT1*
E139	MBINT0*
E140-E149	Drives INIT to the MULTIBUS interface
E141 thru E148	Intended for connection with the MULTIBUS input interrupts only; these lines invert the MULTIBUS interrupts so they can be connected to the PIC interrupt pins.
E150-E151 E152-E153 E154-E155 E156-E157 E163-E164 E165-E166	These jumpers configure the dual-port DRAM starting address within the configured local DRAM address space. See Section 4.2.3.

(continued)

Table A-2. Numerical List of Jumpers and their Functions (continued)

Jumper Number	Functions
E159-E160 E161-E162 E168-E169 E170-E171 E172-E173 E174-E175	These jumpers configure the dual-port DRAM ending address within the configured local DRAM address space. See Section 4.2.3.
E158-E167	Enables the self-test feature of the CPU on reset.

Table A-3. Stake Pin Schematic Index

ALL STAKE PINS

E1 /27	E2 /37	E3 /27	E4 /37
E5 /27	E6 /37	E7 /27	E8-E13 /29
E14-E37 /26	E38 /32	E39 /9	E40-E42 /32
E43 /9	E44-E46 /32	E47 /8	E48-E50 /32
E51 /8	E52-E54 /32	E55 /8	E56-E58 /32
E59 /8	E60-E76 /32	E77-E78 /9	E79-E84 /20
E85-E93 /22	E94-E105 /23	E106-E113 /19	E114-E115 /10
E116-E117 /37	E118-E123 /35	E124-E125 /32	E126-E131 /35
E132-E139 /32	E140 /9	E141-E148 /32	E149 /9
E150-E157 /28	E158 /8	E159-E166 /28	E167 /8
E168-E175 /28			

DEFAULT JUMPERS

E2-E4 /37	E8-E10 /29	E11-E13 /29	E14-E17 /26
E15-E18 /26	E20-E23 /26	E21-E24 /26	E26-E29 /26
E32-E35 /26	E33-E36 /26	E34-E37 /26	E40-E52 /32
E41-E54 /32	E42-E64 /32	E44-E48 /32	E45-E58 /32
E46-E75 /32	E49-E65 /32	E53-E62 /32	E56-E60 /32
E57-E68 /32	E63-E67 /32	E72-E73 /32	E79-E81 /20
E82-E83 /20	E85-E87 /22	E88-E89 /22	E91-E93 /22
E94-E95 /23	E97-E99 /23	E100-E101 /23	E103-E105 /23
E116-E117 /37	E118-E119 /35	E122-E123 /35	E126-E127 /35
E130-E131 /35	E132-E141 /32	E133-E142 /32	E134-E143 /32
E135-E144 /32	E136-E145 /32	E137-E146 /32	E138-E147 /32
E140-E149 /9	E168-E169 /28	E170-E171 /28	E172-E173 /28

Note: The table format: stake pin(s)/schematic sheet number

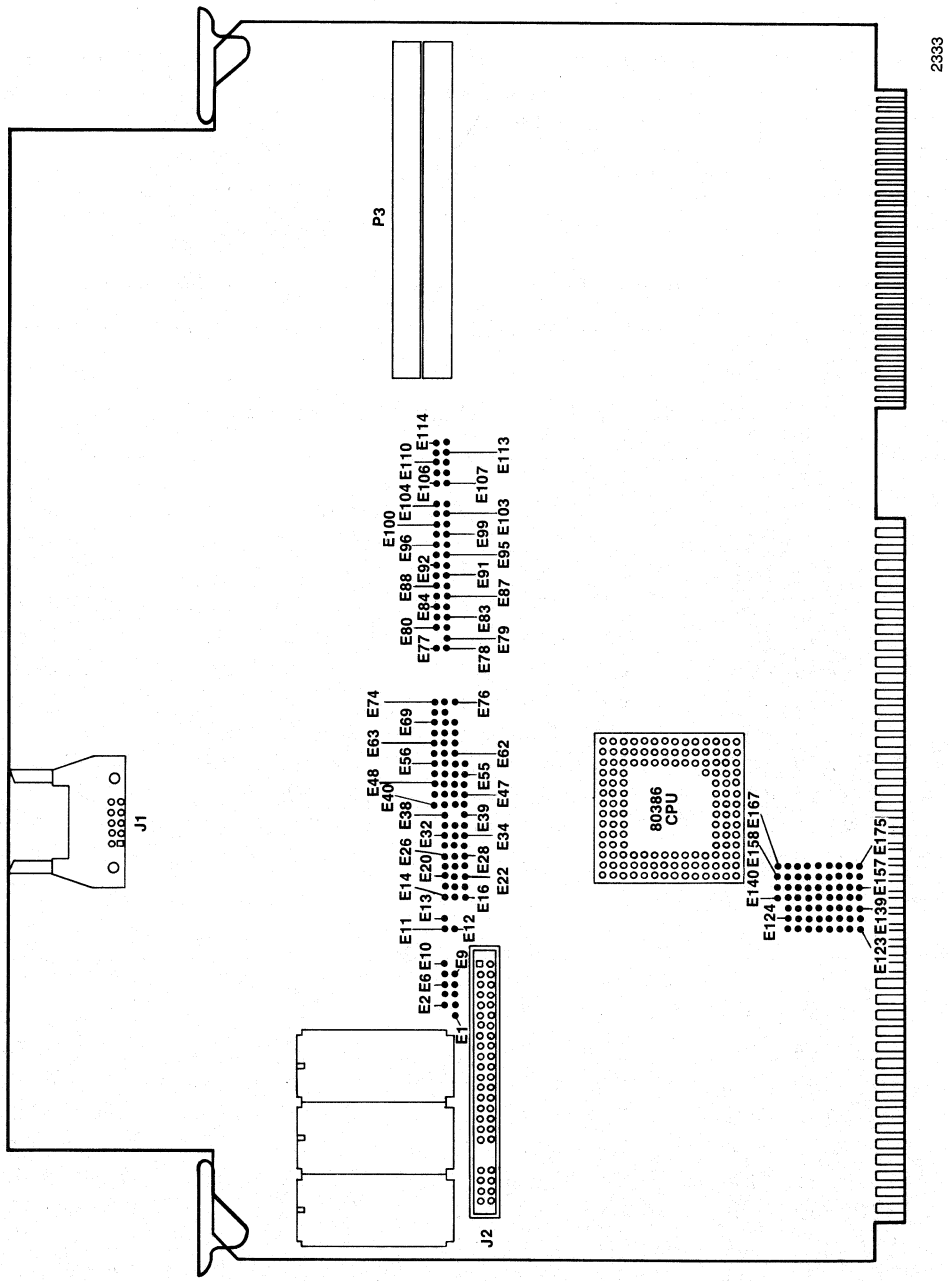

Figure A-1. iSBC® 386/20P Board Jumper Locations

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APPENDIX B
MEMORY BOARD DEFAULT JUMPERS

B.1 INTRODUCTION

This appendix provides the default jumper configuration for the iSBC® 402P (2M-byte) and the iSBC 404P (4M-byte) memory boards. The jumpers are set by the factory and are not user-configurable. Table B-1 lists the default jumper configuration for both boards. Chapter 4 explains how to configure the local and dual-port DRAM, which uses the memory boards. The schematics for the iSBC 402P/404P memory board are shipped with the starter kit.

Table B-1. Default Jumper Listing

iSBC 402P board	iSBC 404P board
E1-E2	E1-E2
E3-E4	E3-E4
E9-E10	E5-E6
E13-E14	E9-E10
	E13-E14

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INDEX

Primary references are underlined.

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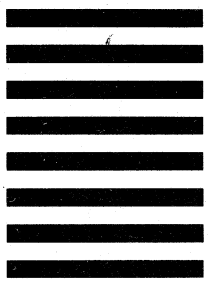

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