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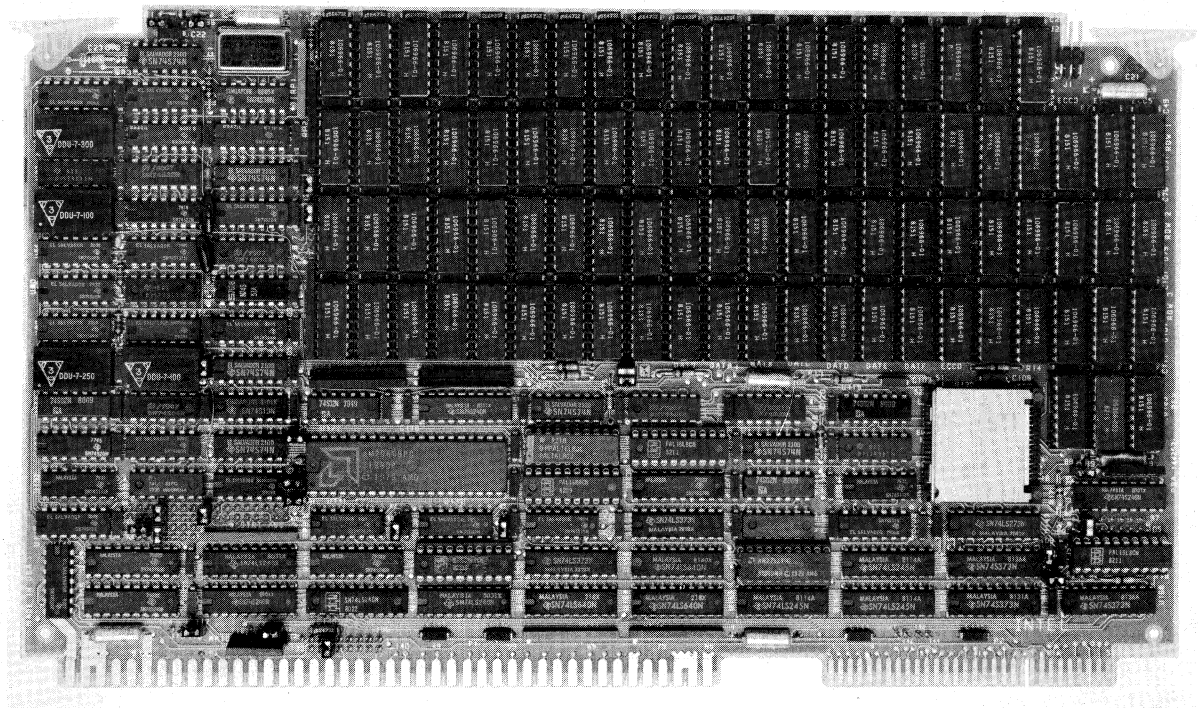
iSBC® 028CX/056CX/012CX RAM BOARDS HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 145158-001

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PREFACE

This manual describes the three "CX-Series" random access memory (RAM) memory boards: the iSBC 028CX board, the iSBC 056CX board, and the iSBC 012CX RAM board. The boards differ only in RAM capacity. Each board features error checking and correcting (ECC) circuitry, Multibus compatibility, and iLBX Bus compatibility. This manual explains how to use the features associated with a typical installation. For additional information, the following publications are available from the Intel Literature Department:

- Intel Multibus® Specification, Order Number: 9800683
- Intel iLBX™ Bus Specification, Order Number: 144456
- Intel Component Data Catalog

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FIGURES

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CHAPTER 1. GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC 028CX/056CX/012CX Random Access Memory (RAM) Boards provide dynamic memory storage capacities of 128k bytes, 256k bytes, and 512k bytes respectively (Figure 1-1). The boards can be used in 8-bit or 16-bit systems. This series of RAM boards (C-series) uses 64K bit dynamic RAM devices exclusively, and incorporates error checking and correction (ECC) circuitry on-board. The boards are Multibus and iLBX Bus compatible and can be used with battery backup.

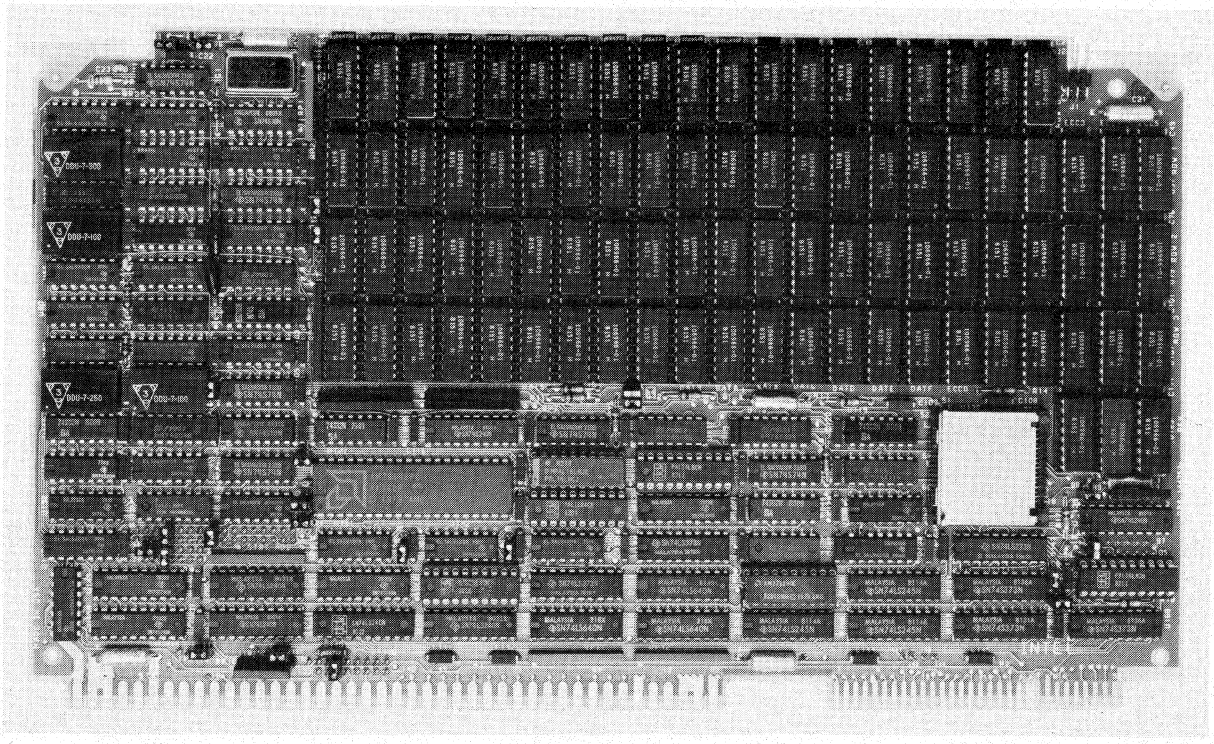

Figure 1-1. iSBC® 012CX Random Access Memory Board

1.2 DESCRIPTION

The iSBC 028CX/056CX/012CX RAM boards are physically and electrically compatible with the Multibus interface standard as outlined in the INTEL MULTIBUS SPECIFICATION. In addition, the boards feature iLBX bus compatibility. This new Intel Single Board Computer bus is a high-speed extension to the standard Multibus interface. The iLBX bus is described in the INTEL iLBX BUS SPECIFICATION.

The capacity of each RAM board in this series is determined by the number of RAM devices on-board. The iSBC 028CX board uses 16 devices for memory data and 6 devices for error checking and correcting (ECC) purposes; the iSBC 056CX board uses 32 devices for memory and 12 devices for ECC; and the iSBC 012CX board uses 64 devices for memory and 24 devices for ECC. Power requirements for each board are listed in Table 1-1.

Error checking and correcting (ECC) is accomplished with the Intel 8206 Error Detection and Correction Unit and other on-board circuitry. This ECC unit allows detection and correction of single-bit errors, detection of double-bit errors and detection of most multiple-bit errors. As used on this series of boards the ECC circuitry can be programmed to correct all correctable errors (double bit and multiple bit errors are not correctable), or to disregard errors. In addition, the board can be programmed to interrupt the processor on any error or to interrupt the processor only on uncorrectable errors.

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independent for the Multibus interface and the iLBX interface. For Multibus operations, on-board jumpers assign the board to one of four 4-megabyte pages. Each page is partitioned into 256 blocks of 16k bytes each. The smallest Multibus partition on any board in this series is 16k bytes. Jumpers assign the base address (lowest 16k block) within the selected 4-megabyte page. The 16k byte block should not cross the 4-megabyte boundary of the board.

The iLBX memory is partitioned into 64k byte blocks. As shipped, the iLBX Bus memory on the iSBC 028CX/056CX/012CX board base address is set to 000000 Hex. An on-board jumper selects the iLBX base address. Refer to Chapter 2 for complete base address jumper information.

This series of RAM boards operates in either 8-bit or 16-bit systems. All electrical connections to and from the boards are implemented via edge connectors P1, P2 and J1. Connector P1 (86-pin) is the Multibus interface connector and P2 (60-pin) is the iLBX Bus connector. Connector J1 is used for battery backup control signals.

1.3 DOCUMENTATION SUPPLIED

Each RAM board is shipped with a matching set of schematic diagrams. These diagrams should be kept for future reference. The diagrams shipped with the board may be more recent than the diagrams in Chapter 5 of this manual.

1.4 SPECIFICATIONS

General specifications for the RAM boards in this series are listed in Table 1-1. Board AC and DC specifications and Multibus timing information are provided in Appendix A.

Table 1-1. Specifications

BOARD CAPACITY:	
iSBC 028CX RAM Board:	128k Bytes (131,072 Bytes)
iSBC 056CX RAM Board:	256k Bytes (262,144 Bytes)
iSBC 012CX RAM Board:	512k Bytes (524,288 Bytes)
MULTIBUS® MEMORY PARTITIONING:	Maximum system RAM size: 16M bytes
Page Address (4M bytes):	1 of 4 Four megabyte pages, as follows: 0 - 4 Megabytes 4 - 8 Megabytes 8 - 12 Megabytes 12 - 16 Megabytes
Block Address (16K bytes):	
iSBC 028CX RAM Board:	8 contiguous 16k byte blocks (128k bytes)
iSBC 056CX RAM Board:	16 contiguous 16k byte blocks (256k bytes)
iSBC 012CX RAM Board:	32 contiguous 16k byte blocks (512k bytes)
	Note: Blocks cannot cross 4M byte boundary.
Base Address:	Any 16k byte boundary
REFRESH TIMES:	
Refresh Cycle Time:	15.6 usec.
Refresh Delay Time:	760 nsec. maximum

Table 1-1. Specifications (continued)

MULTIBUS® ACCESS TIMES:	
Read/Full Write:	350 nanoseconds (maximum)
Write Byte:	530 nanoseconds (maximum)
Cycle Times:	
Read/Full Write:	460 nanoseconds
Write Byte:	885 nanoseconds
Note: If an error is detected, read access time & cycle times are extended by 255 ns (maximum).	
iLBX™ BUS MEMORY PARTITIONING:	2 blocks of 64k bytes each on iSBC 028CX 4 blocks of 64k bytes each on iSBC 056CX 8 blocks of 64k bytes each on iSBC 012CX
Base Address:	Any 64k byte boundary. See Table 2-4.
iLBX™ ACCESS TIMES:	(ASTB/ or DSTB/ to ACK/)
Read/Full Write:	Jumper selectable; see Table 2-7 for details
Write Byte:	440 nanoseconds (maximum)
Data Access Time:	(ASTB/ to Valid Data on iLBX Bus) 300 nanoseconds (maximum)
Cycle Times:	
Read/Full Write:	375 nanoseconds (maximum)
Write Byte:	740 nanoseconds (maximum)
MEMORY PROTECTION/BACKUP:	An active low TTL memory protect signal generated by the power supply, (MPRO/) enters the board via J1. This signal disables read/write access to memory thereby protecting data during system power-down. An optional battery can be used to save data. See section 2.4.8.

Table 1-1. Specifications (continued)

POWER REQUIREMENTS:	
Voltage:	5VDC ±5%
Current:	iSBC 028CX: 6.5A Maximum
	iSBC 056CX: 6.6A Maximum
	iSBC 012CX: 6.8A Maximum
Battery Current:	iSBC 028CX: 2.2A Maximum (Standby mode)
	iSBC 056CX: 2.3A Maximum (Standby mode)
	iSBC 012CX: 2.5A Maximum (Standby mode)
ENVIRONMENTAL REQUIREMENTS:	
Operating Temperature:	0°C to 55°C (32°F to 130°F)
Operating Humidity:	To 90% without condensation
PHYSICAL DIMENSIONS:	
Width:	30.48 cm (12 in)
Height:	17.15 cm (6.75 in)
Thickness:	1.27 cm (0.50 in)
Weight:	
iSBC 028CX	469 gm (16.7 oz)
iSBC 056CX	532 gm (19.0 oz)
iSBC 012CX	658 gm (23.5 oz)

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CHAPTER 2. PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides instructions for preparing the iSBC 028CX/056CX/012CX RAM Boards for use in various environments. Included in this chapter are instructions on unpacking and inspection, installation considerations, jumper configurations, battery back-up configuration, and board installation information.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

Save the salvageable shipping cartons and packing material for future use in the event that the product must be shipped.

2.3 INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, physical size requirements, and interfacing requirements are outlined in the following paragraphs.

2.3.1 POWER REQUIREMENTS

The power requirements for the RAM boards depend on quantity of RAM chips installed onto the RAM boards. Table 1-1 lists the various current requirements for each configuration of the RAM boards.

2.3.2 COOLING REQUIREMENTS

The heat dissipation for the RAM boards varies with the configuration of the board; Table 2-1 shows the maximum power dissipation for each configuration. Adequate circulation of air must be provided to prevent a temperature rise above 55°C (130°F). The system chassis units available from Intel include fans that provide adequate intake and exhaust of ventilating air.

Table 2-1. Heat Dissipation

Board	Dissipation
iSBC® 028CX	463 gm-cal/minute (1.87 Btu)
iSBC® 056CX	470 gm-cal/minute (1.90 Btu)
iSBC® 012CX	484 gm-cal/minute (1.96 Btu)

2.3.3 MULTIBUS® INTERFACING REQUIREMENTS

The iSBC 028CX/056CX/012CX RAM Boards are designed for installation into a standard Intel iSBC cardcage or into an Intel Microcomputer Development System chassis. The 86-pin edge connector (P1) on the RAM boards provides interfacing to the Multibus structure. Appendix A lists the pin assignments for the P1 connector and provides a description of the function of each signal.

Edge connector P2 on the RAM boards is used for the iLBX Bus control, data, and address lines. Multibus battery back-up signals, and memory protection signals for the RAM boards are routed through connector J1, which is located in the upper right-hand corner of the board. Appendix B lists the pin assignments and signal definitions for connector P2.

2.4 JUMPER CONFIGURATIONS

The iSBC 028CX/056CX/012CX board is shipped from the factory with a specific default jumper configuration. The default configuration may require alteration to suit your particular application. The following sections describe the user jumper configurations in their default state and optional states.

2.4.1 MULTIBUS® MEMORY ADDRESSING

The iSBC 028CX/056CX/012CX RAM boards support several Multibus addressing modes: 16-bit, 20-bit, and 24-bit addressing. The board is structured to accept 24-bit address words, on Multibus lines ADR0/ through ADR17/. The two most significant lines (ADR16/ and ADR17/) are used to select a particular 4-megabyte page of addresses. This allows a maximum of 4-megabytes of direct addressing capability, using the remaining 22 address lines (ADR15/ through ADR0/). When a RAM board is installed in a system, jumpers specify where within the overall 16-megabyte Multibus address space the board is to reside.

Systems with 16 address lines should interface directly to Multibus address lines ADR0/ through ADRF/. This scheme allows addressing of up to 64k bytes of memory (0 hex through 00FFFF hex). Systems with 20 address lines should interface directly to Multibus address lines ADR0/ through ADR13/. This scheme allows addressing of up to 1 megabyte of memory (0 hex through 0FFFFF hex).

Four additional address lines are available on connector P2. These are Multibus address lines ADR14/ through ADR17/. Address lines ADR14/ and ADR15/ are used for decoding up to 4 megabytes of memory; lines ADR16/ and ADR17/ are used for full 16-megabyte direct addressing on fully compatible systems.

For universal addressing compatibility, Multibus address lines ADR10/ through ADR17/ are held high (+5VDC) with pull-up resistors. If these lines are not used in your system, board operation will not be adversly affected.

In order to select the correct address jumpers for your application, the overall addressing scheme for this board must be examined. Multibus memory address jumpers are configured with two sets of jumpers. The first set selects the particular 4-megabyte page within which the board is to reside. The second set of jumpers selects the base (starting) address for the board, within the selected page. Refer to Section 2.4.1.2 for more information.

When configuring the board for your application first examine the current status of the board. Your application may require changing only one jumper. Typically, the base address selection jumpers will be the most likely to change from application to application. The board is defaulted to the lowest base address (0 hex in page 0).

The following sub-sections discuss the four Multibus address jumper sets in more detail. Refer to Figure 5-1 for the physical location of the jumpers on the board.

2.4.1.1 Multibus® Page Address Selection Jumpers

This set of jumpers is used to select the 4-megabyte page in which the board is to reside. Multibus memory allows 16-megabytes, so there are four choices. These choices are shown in Table 2-2. The board will respond only to the code (formed by ADR16/ and ADR17/) which matches the jumper selected page, as described in section 2.4.1. The board is defaulted to page 0.

Table 2-2. Multibus® Page Select Jumpers

Jumper Pair	Function
70 - 76*	Page 0 (0 to 4-megabytes)
71 - 77	Page 1 (4 to 8-megabytes)
72 - 78	Page 2 (8 to 12-megabytes)
73 - 79	Page 3 (12 to 16-megabytes)
* Default Configuration	

2.4.1.2 Multibus® Base Address Jumpers

The 4-megabyte memory page selected with the jumpers in Section 2.4.1.1 consists of 256 individual 16-kilobyte blocks. Block 1 is located at the lowest point of the 4-megabyte page and block 256 is located at the highest point in the 4-megabyte page. Figure 2-1 illustrates this concept.

Board capacity will determine how many of the 256 blocks can be used. The iSBC 028CX board can use any 8 contiguous blocks; the iSBC 056CX board can use any 16 contiguous blocks; and the iSBC 012CX board can use any 32 contiguous blocks. Refer to Figure 2-1.

The base address is defined as the starting point of the lowest block you select. Board memory will then continue upward for the number of contiguous blocks according to capacity. Any 16k byte block can be selected for a base address. The base address is set by creating an eight-bit binary value with the base address selection jumpers. Installing a jumper in one of the digits equals a binary 1; conversely, absence of a jumper equals a binary 0. Table 2-3 correlates the jumpers to their binary equivalents.

A binary value of 00000000 selects the first 16k byte block and a binary value of 11111111 (255 decimal) selects the last 16k byte block. Any of the 256 blocks may be selected as the base address. The start of block 0 corresponds to hexadecimal address 000000 Hex and the end of block 255 corresponds to 3FFFFF Hex.

For example, if you want your base address to be at block 17, you would install jumpers between posts 47 - 63 and 51 - 67. This is a binary value of 00010001 or 17 decimal. Assuming you had a iSBC 028CX board (128k bytes capacity), your address space would extend from block 17 through block 25. This is equivalent to addresses 44000 - 63FFF hex.

NOTE

Remember that board RAM is shared by Multibus memory and iLBX Bus memory. Because of this sharing, we recommend that the address space selected for each bus fully overlap. For example, if the Multibus base address is set to 512k, then the iLBX Bus base address should also be set to 512k. If the memory is partially overlapped, or not overlapped at all, iLBX Bus data will be written into different Multibus locations under certain conditions.

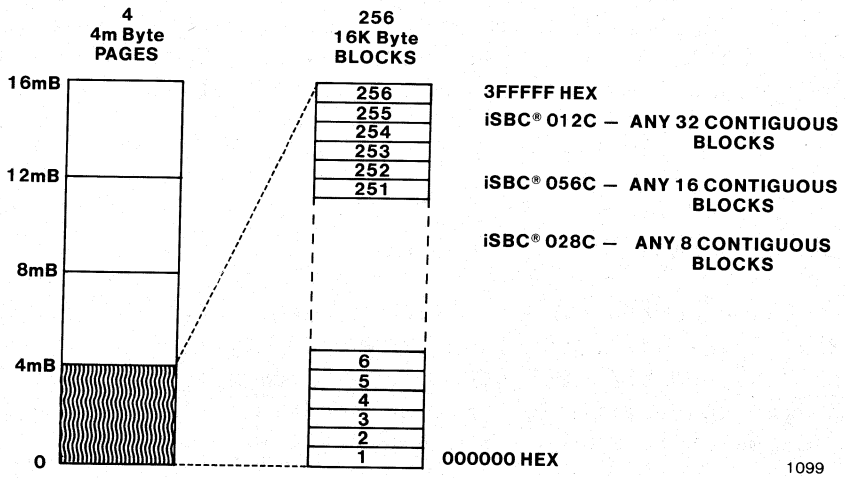


Figure 2-1. Multibus® Page & Base Address Concept

Another example of base address selection on an iSBC 012CX board is shown in Figure 2-2. See Section 2.4.2 for iLBX Bus addressing jumper configurations.

Table 2-3. Multibus® Base Address Selection Jumpers

Jumper Pair	Function
44 - 60	Base Address Bit 7 (MSB)
45 - 61	Base Address Bit 6
46 - 62	Base Address Bit 5
47 - 63	Base Address Bit 4
48 - 64	Base Address Bit 3
49 - 65	Base Address Bit 2
50 - 66	Base Address Bit 1
51 - 67	Base Address Bit 0 (LSB)
* Default Configuration. Jumper IN = 1; Jumper OUT = 0	

2.4.1.3 iLBX™ Bus Addressing

The iLBX Bus memory address space consists of 256 contiguous blocks of 64k bytes each. This is a total of 16 megabytes of memory. As shipped from the factory, each board is configured so that the board starts at address 000000 hex, and occupies the number of contiguous 64k blocks allowed for its capacity. The iSBC 028CX board occupies 128k bytes (0 to 1FFFF hex); the iSBC 056CX board occupies 256k bytes (0 to 3FFFF hex); and the iSBC 012CX board occupies 512k bytes (0 to 7FFFF hex).

2.4.1.4 iLBX™ Bus Base Address Jumpers

The default iLBX base address on all three memory boards is zero (000000). The iLBX base address is a function of on-board programmed array logic (PAL) device U158 and the iLBX base address jumpers selected. Three jumpers are used to select the iLBX Base address. Two define the range of addresses and the third specifies the actual base address.

The memory boards examine iLBX address lines AB10 - AB17 to determine if the address on the iLBX bus refers to on-board memory. If more than one iLBX memory board is used in your system, ensure that the base addresses of the boards do not cause memory space overlapping. There are 21 pre-programmed base addresses for the iSBC 028CX/056CX/012CX boards; 27 for the iSBC 012CX board.

The pre-programmed PAL can be reprogrammed to provide six additional base addresses for the board. PAL programming is discussed in Appendix C. When using the reprogrammed option, the following jumpers must be installed: 107 - 108 and 110 - 111.

Table 2-4 correlates the jumper connections to the iLBX base address selection. Figure 2-3 provides an example of a typical iLBX Bus base address configuration.

Table 2-4. iLBX™ Bus Base Address Jumpers

Base Address	iSBC® 028CX 128K BD. Range Select			iSBC® 056CX 256K BD. Range Select			iSBC® 012CX 512K BD Range Select			
	X*	Y	Z	X*	Y	Z	X*	Y	Z	W
99-91*	0	896	1792	0	1792	3584	0	3584	7168	0
100-92	128	1024	1920	256	2048	3840	512	4096	7680	64
101-93	256	1152	2048	512	2304	4096	1024	4608	8192	128
102-94	384	1280	2176	768	2560	4352	1536	5120	8704	192
103-95	512	1408	2304	1024	2816	4608	2048	5632	9216	256
104-96	640	1536	2432	1280	3072	4864	2560	6144	9728	320
105-97	768	1664	2560	1536	3328	5120	3072	6656	10240	384

Notes: * = Default jumpers installed

1. All addresses are shown in K-Byte values.
2. Base address starts at value shown.
3. Range Select Jumper Configurations: (X is factory default)

X =	Y =	Z =	W =
106-107	107-106	108-107	107-108
109-110	111-110	110-109	110-111 (iSBC 012CX only)

The configuration 107-108 and 110-111 is available for re-defining the base address structure on the iSBC 028CX/056CX boards only; see text for details.

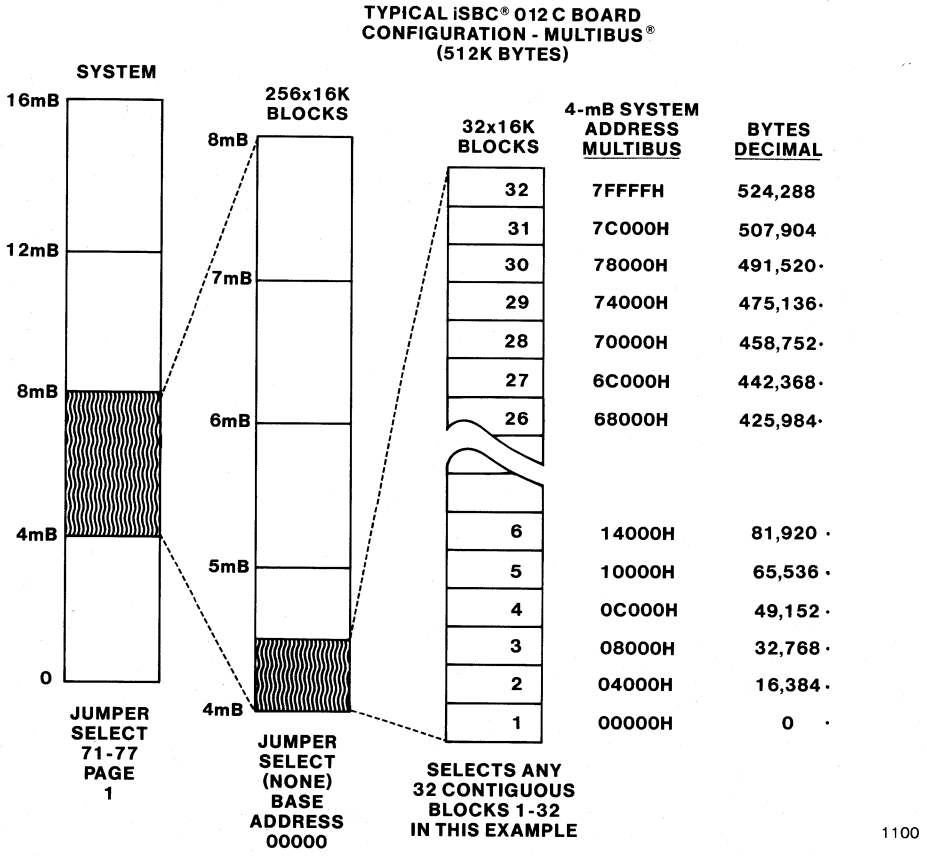


Figure 2-2. Multibus® Base Address Example

NOTE

Remember that board RAM is shared by Multibus memory and iLBX Bus memory. Because of this sharing, we recommend that the address space selected for each bus fully overlap. For example, if the Multibus base address is set to 512k, then the iLBX Bus base address should also be set to 512k. If the memory is partially overlapped, or not overlapped at all, iLBX Bus data will be written into different Multibus locations under certain conditions.

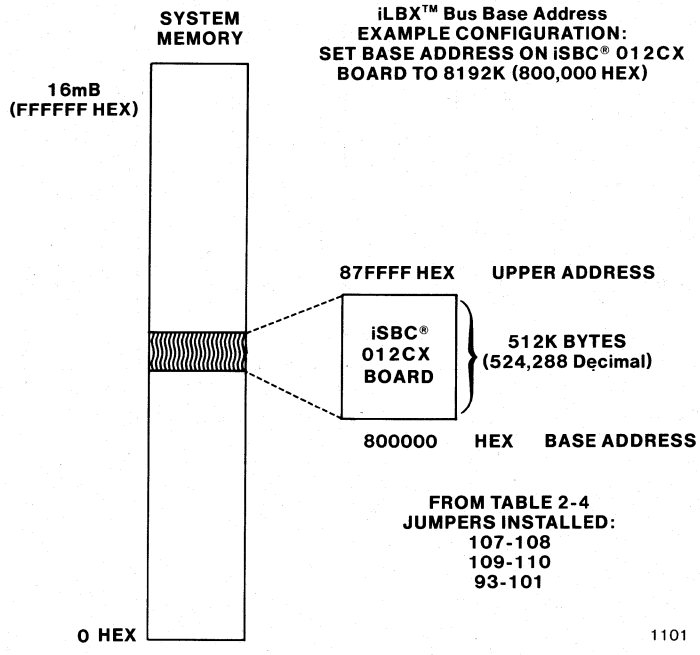


Figure 2-3. iLBX™ Bus Base Address Example

2.4.2 ECC I/O ADDRESS SELECTION

The Error Checking and Correction (ECC) circuitry communicates with the processor board through a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The iSBC 028CX/056CX/012CX board is shipped with a programmed array logic (PAL) device (U152) which allows selecting one of 9 possible addresses for the I/O port. The actual selection is done by jumper configuration. If your application requires an I/O address which is not listed in Table 2-5, the PAL at location U152 must be reprogrammed (refer to Appendix C).

Three sets of jumpers are used to select the desired I/O address that the board will recognize. Table 2-5 illustrates the 9 possible addresses and indicates the default I/O address (01C0 Hex). The table shows how to assign one of the 9 addresses to the board, using the three sets of jumpers. Figure 2-4 shows how the I/O address hex digits are derived.

Table 2-5. I/O Address Jumpers

Jumpers IN:	86-87*		85-86	
39-55*	01C0	01C1	40	User Programmable
40-56	41C0	41C1	40	
41-57	81C0	81C1	40	
42-58	C1C0	C1C1	40	
	83-84*	82-83	83-84	82-83

* Default Configuration; addresses shown in hexadecimal.

Refer to Figure 2-4 for the following discussion. The four digit hexadecimal I/O address which the board will recognize is formed by the 16 address lines ADR0/ - ADRF/. Address lines ADRF/ and ADRE/ form the two most significant bits of the four binary bits used to produce the "W" digit in the I/O address. Address lines ADRD/ and ADRC/ form the two least significant bits of the "W" digit. The remaining 12 address lines, ADRB/ through ADR0/ are used to form the other three hex digits, "X" "Y" and "Z."

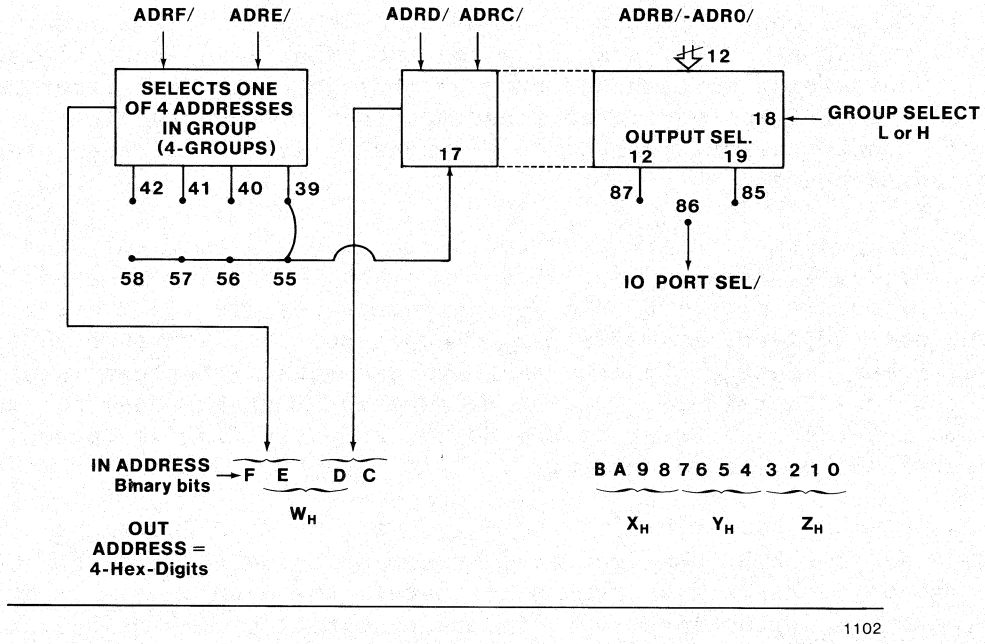


Figure 2-4. I/O Address Formation Diagram

2.4.3 iLBX™ BUS INTERFACE ADDRESS STROBE JUMPER

The memory board is shipped from the factory configured for iLBX Bus and Multibus operation. If your application is MULTIBUS-ONLY, install the following jumper:

90 - 98

2.4.4 iLBX™ BUS SPEED SELECTION JUMPER

The iLBX Bus interface on the iSBC 028CX/056CX/012CX boards can operate either in the slow mode or fast mode. The board is defaulted to the fast mode. To enable the slow mode perform the following jumper modifications:

Remove 10 - 11
Install 11 - 12

Refer to the INTEL iLBX BUS SPECIFICATION for additional details on slow and fast modes.

2.4.5 INTERRUPT LEVEL SELECTION JUMPERS

The on-board ECC circuitry will generate an interrupt as specified in Section 3.2. Each bus (Multibus and iLBX) generates its own interrupt. Each interrupt can be placed on a jumper-selected Multibus interrupt line. Jumpers are used to specify the interrupt level and Multibus line. The default setting for the Multibus-generated interrupt is INT5/. The iLBX Bus-generated interrupt is not connected in the factory default configuration. Table 2-6 provides a list of all the interrupt lines and jumpers.

Push-on jumper headers are used to select the Multibus-generated interrupt level, as shown in Table 2-6. The iLBX Bus-generated interrupt must be manually wired-in; the source jumper post is 122. Wire this post to the desired level in Table 2-6. Jumper posts 133 through 140 are the output posts. Notice that the iLBX Bus-generated interrupt is wired to a Multibus interrupt line. This is because the iLBX Bus does not support its own interrupts. Refer to the board schematic diagram (sheet 9) in Chapter 5 for more information.

For example, suppose you want the Multibus-generated interrupt to be at level 4 and the iLBX Bus-generated interrupt to be at level 6. Using the information in Table 2-6, you would install the push-on jumper at 126 - 136 for the Multibus interrupt, and then install a wire wrap type jumper from post 122 to post 134 (output post for level 6). Notice that if you select the same interrupt level for both the Multibus and iLBX Bus, the processor will be unable to determine which bus has experienced the interrupt condition.

Whenever an interrupt is generated the on-board indicator lamp (LED) will illuminate. This lamp can be used for test and diagnostic purposes.

Table 2-6. Interrupt Level Selection Jumpers

Jumper Pair	Level	M-BUS Pin
130 - 140	INT0/	P1 - 41
129 - 139	INT1/	P1 - 42
128 - 138	INT2/	P1 - 39
127 - 137	INT3/	P1 - 40
126 - 136	INT4/	P1 - 37
125 - 135*	INT5/	P1 - 38
124 - 134	INT6/	P1 - 35
123 - 133	INT7/	P1 - 36
122 - XXX	iLBX™ Bus Interrupt to Multibus®	

* Default connection. XXX = output jumper posts numbers 133 through 140.

2.4.6 EXTERNAL REFRESH (REFRQST) JUMPER

The iSBC 028CX/056CX/012CX board is configured at the factory for on-board refresh. If an external, off-board refresh is needed for test purposes, it is possible to disable the on-board refresh circuitry. The iLBX Bus cannot be used if an external refresh is employed. To enable external refresh, perform the following modifications:

a. Remove jumper 5 - 6
b. Install jumper 4 - 5
c. Install jumper 141 - 142
d. Connect the external refresh signal to P2 - 40.

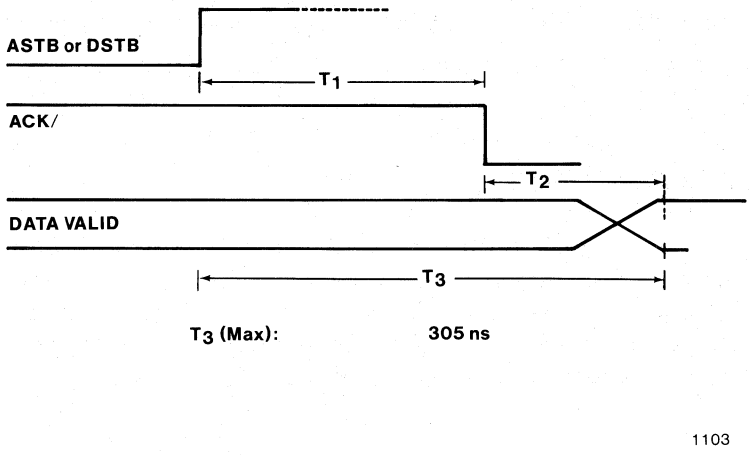
2.4.7 iLBX™ BUS ACKNOWLEDGE TIME SELECTION JUMPERS

The iSBC 028CX/056CX/012CX acknowledge time (ASTB/ or DSTB/ to ACK/ Valid) for iLBX Bus requests can be optimized for the application. Since the iSBC 028CX/056CX/012CX boards do not use a synchronous clock as a timing reference, the board must be configured according to master-slave interaction requirements. Table 2-7 provides the acknowledge times and their associated jumper connections. Figure 2-5 illustrates the timing waveforms for the associated activity.

The timing relationships shown in Figure 2-5 provide guidelines for optimizing the memory board acknowledge time to the system. Time T1 is defined as the interval between ASTB/ or DSTB/ valid and ACK/ valid. Time T2 is the interval between ACK/ valid and the data valid condition.

Configure your memory board to operate in the T1 range which best suits your application. However, you must also choose optimal T2 range. Therefore, examine both ranges before configuring the appropriate jumpers. Notice that the T1 minimum time must be greater than the maximum value of ASTB to DSTB + 10 nanoseconds. Refer to Table B-4 in Appendix B for more iLBX Bus timing data.

The maximum values for T2 are also given, according to T1 jumper configuration. The minimum and maximum values are shown for T1. Refer to the Intel iLBX BUS SPECIFICATION for more timing interaction information.



T1 & T2 Times: See Table 2 - 7

Figure 2-5. iLBX™ Bus Acknowledge Time Waveforms

Table 2-7. Acknowledge Time Selection Jumpers

Jumpers	T1 Min NS	T1 Max NS	T2 Max NS
38 - 68 and			
17 - 16	65	117	212
17 - 7	82	138	193
17 - 9	92	148	183
17 - 8	101	159	174
43 - 59 and			
68 - 54	135	196	140
68 - 69*	206	274	69
68 - 36	230	301	45
68 - 74	254	327	21
68 - 75	278	353	-3
68 - 53	301	379	-26
68 - 37	325	406	-50

Notes: 1. All times specified in nanoseconds
2. * = Default Configuration

2.4.8 BATTERY BACK-UP/MEMORY SAVE JUMPERS

In systems employing a battery back-up and memory save feature, the user must interface to connector J1. The system power supply must generate some type of power-failure signal, for full Multibus compatibility. Intel power supplies such as the iSBC 645 Power Supply generate an AC Low signal (ACLO/), and a Memory Protect (MPRO/) signal for this purpose. The timing of these two signals is critical for implementing a battery back-up scheme. The MPRO/ signal is used by the RAM boards to prevent access to memory during a power-down condition; the ACLO/ signal is not used by the RAM boards, but could be used by the CPU board. Refer to the INTEL MULTIBUS SPECIFICATION for guidelines on battery back-up schemes.

Connector J1 is not referenced in the INTEL MULTIBUS SPECIFICATION; however, the battery back-up signals referenced are supported by the iSBC 028CX/056CX/012CX boards. Connect the appropriate battery back-up, memory protect, and other control lines to the connector, as listed in Table 2-8.

NOTE

The memory protect signal (MPRO/) generated by the power supply during a power failure must not be issued during an active memory access cycle.

When battery back-up power is to be installed for use with the RAM board, remove the following factory installed jumpers:

22 - 23
24 - 25
80 - 81
88 - 89

Battery backup power enters the board at J1-1 and J1-3 on the auxiliary connector. Ground is on J1-2 and J1-4.

CAUTION

Always remove both battery back-up and system power from the RAM boards before installing or removing the boards from a system cardcage. Failure to do so could result in damage to the boards.

Table 2-8. Connector J1 Pin Assignments

J1-1	+5V Battery In
J1-2	Ground
J1-3	+5V Battery In
J1-4	Ground
J1-5	Memory Protect (MPRO/)
J1-6	Reserved

2.5 BOARD INSTALLATION

The iSBC 028CX/056CX/012CX RAM Boards are compatible with all Multibus backplanes and cardcages. For iLBX Bus compatibility a special iLBX connector must be used to link the processor board to the memory board. The iLBX Bus uses connector P2 and supercedes any previous P2 pin-out scheme. Refer to Section 2.4.9 for battery backup information.

CAUTION

Ensure power is removed from the cardcage before installing or removing Intel Single Board Computers and Multimodule boards. Failure to do so could result in damage to the boards.

***

CHAPTER 3. ECC OPERATION AND PROGRAMMING INFORMATION

3.1 INTRODUCTION

The iSBC 028CX/056CX/012CX RAM boards each use two special registers to pass ECC mode control and status information to and from the system master iSBC board. These registers are called the Control Status Register (CSR) and the Error Status Register (ESR). This chapter describes the two registers, and explains how to program them for the desired operations. Board initialization procedures are given in Section 3.5.

3.2 MODES OF ECC OPERATION

There are six ECC modes of operation on this series of RAM boards. Each mode is obtained by software programming from the master iSBC board. The six modes are:

a. Interrupt on any error mode;
b. Interrupt on non-correctable error only mode;
c. Correcting mode;
d. Non-correcting mode;
e. Diagnostic mode;
f. Examine syndrome word mode.

Modes (a) and (b) can be used in conjunction with modes (c) and (d). The modes are described in the following sections. Mode programming information is provided in Section 3.3.

3.2.1 INTERRUPT ON ANY ERROR MODE

In this mode the RAM board will interrupt the iSBC processor board when any error (single bit or multiple bit) is detected by the ECC circuitry. Interrupts are discussed in Section 2.4.5.

3.2.2 INTERRUPT ON NON-CORRECTABLE ERROR ONLY MODE

In this mode the RAM board will interrupt the iSBC processor board only when a non-correctable (multiple bit) error is detected by the ECC circuitry. A multiple bit error is not correctable by the ECC circuitry. Interrupts are discussed in Section 2.4.5.

3.2.3 CORRECTING MODE

In this mode the RAM board corrects any correctable error (single-bit error). Words which are not correctable are not modified. Interrupts are generated on any error only or on non-correctable errors only, depending on the mode selected. Interrupts are discussed in Section 2.4.5.

3.2.4 NON-CORRECTING MODE

In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described above. Interrupts are discussed in Section 2.4.5.

3.2.5 DIAGNOSTIC MODE

This mode is used for testing the on-board ECC circuitry. In this mode the Write Enable Strobe to the ECC RAM array is continously disabled. The diagnostic mode can be used to simulate errors and in conjunction with the examine syndrome word mode to examine the check bits generated by the ECC circuitry. Refer to Section 4.3.3 for more Diagnostic Mode information.

3.2.6 EXAMINE SYNDROME WORD MODE

This mode, in conjunction with the diagnostic mode, is used for testing the ECC memory. In this mode, the syndrome bits (check bits) are clocked into the Error Status Register (ESR) on every memory read or write cycle. The ESR translation PROM (U155) switches to a transparent mode in the Examine Syndrome Word mode. This allows the actual syndrome word generated by the 8206 device to be examined. The six ESR bits are gated onto Multibus data lines DAT0/ - DAT5/. Refer to Section 4.3.3 for more Examine Syndrome Word Mode information.

3.3 PROGRAMMING INFORMATION

The following five sections describe how to program the Control Status Register (CSR) and how to read the Error Status Register (ESR). The CSR and the ESR provide a means of controlling and viewing the status of ECC operations. These registers are accessed via the system master iSBC board's I/O port addresses. The CSR is written to by asserting IOWC/ to the Multibus lines and the ESR is read by asserting IORC/. Since the CSR and the ESR occupy the same I/O port, the CSR may not be read. The ESR is cleared by a write to the board I/O address.

CAUTION

The ECC circuitry could malfunction if the CSR is loaded at the same time an iLBX Bus memory access is taking place. In a single CPU system, this means that there must be no DMA activity on the iLBX bus while the CPU is loading the CSR. In a multiple CPU system, ensure that one CPU is not loading the CSR while another CPU board is accessing the memory board via the iLBX Bus.

3.3.1 CONTROL STATUS REGISTER (CSR) PROGRAMMING

The CSR is an eight-bit register (on the RAM board) which is programmed by the processor to select one of several operating modes. To program the CSR, assert IOWC/ when the port address and data are stable on the Multibus lines. CSR format is shown below; a summary of programming is given in Table 3-1; Table 3-2 provides a list of the most typical ECC modes, shown in hexadecimal format. The codes shown can be written directly to the CSR, during system initialization. Table 3-1 also gives the condition of the CSR after a RESET or POWER-UP condition.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0

Table 3-1. RAM Board Control Status Register Format Summary

Bit 0	Interrupt on Correctable Error: When this bit is low (0), a Multibus interrupt is asserted only on an uncorrectable error. When this bit is high (1), the RAM board asserts a Multibus interrupt on any data error (single or multiple-bit). POWER-UP & RESET CONDITION: HIGH (1)
Bit 1	Diagnostic Mode Select. When this bit is high (1), the diagnostic mode is deselected. When low (0), the diagnostic mode is selected. POWER-UP & RESET CONDITION: HIGH (1).
Bit 2	Correct/Non-Correcting Modes: When this bit is high (1) every correctable error which occurs will be corrected by the on-board circuitry. The RAM board will continue to overwrite even if an uncorrectable error occurs during write-byte cycles. An overwrite should be performed to clear errors during memory initialization. When this bit is low (0) the board will not correct any errors. The RAM board will abort write-byte cycles if an uncorrectable error is detected on the read portion of the cycle. Refer to Section 4.3 for additional information. POWER-UP & RESET CONDITION: HIGH (1)
Bit 3	Examine Syndrome Word Mode: When this bit is high (1), the Examine Syndrome Word mode is deselected. When this bit is low (0), the Examine Syndrome Word mode is selected. POWER-UP & RESET CONDITION: HIGH (1)
Bit 4	Reserved: must be low (0)
Bit 5	Reserved: must be low (0)
Bit 6	Reserved: must be low (0)
Bit 7	Reserved: must be low (0)

Table 3-2. Typical ECC Operating Modes (Hex)

Hex Code	Mode Description
0F	Correcting, Interrupt on Correctable Error
0E	Correcting, Interrupt on Non-Correctable Error
0B	Non-correcting, Interrupt on Correctable Error
0A	Non-correcting, Interrupt on Non-Correctable Error
00	Diagnostic mode, syndrome read selected

NOTE

Memory must be cleared after a RESET, and before starting system write or read operations. Refer to Section 3.5.

3.3.2 INTERRUPT ON ANY ERROR MODE PROGRAMMING

Bit 0 selects the interrupt mode. When bit 0 is high, the RAM board will issue an interrupt to the Multibus when any error is detected.

3.3.3 INTERRUPT ON NON-CORRECTABLE ERROR ONLY MODE PROGRAMMING

Bit 0 selects the interrupt mode. When bit 0 is low, the RAM board will issue an interrupt to the Multibus only when a non-correctable error is detected.

3.3.4 CORRECTING AND NON-CORRECTING MODE PROGRAMMING

Bit 2 selects the correcting mode when high, or the non-correcting mode when low.

3.3.5 DIAGNOSTIC MODE PROGRAMMING

Bit 1 deselects the diagnostic mode when high, or selects the diagnostic mode when low. This mode can be used for simulating errors in memory. The simulated errors should be detected by the ECC circuitry. In this mode the Write Enable strobe to the ECC RAM array is continously inactive.

3.3.6 EXAMINE SYNDROME WORD MODE PROGRAMMING

Bit 3 deselects the examine syndrome word mode when high (1), or selects the examine syndrome word mode when low (0). The examine syndrome word mode is used in conjunction with the diagnostic mode. This mode allows testing the check bit generation circuitry of the board. In this mode, the syndrome (check) bits are clocked into the error status register upon every read (or write) cycle. Refer to Section 4.3 for additional information on this mode.

Table 3-3. RAM Board Error Status Register Format

Bit 6	Bit 5	Meaning
0	0	Error in row 0
0	1	1
1	0	2
1	1	3

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Meaning
0	0	0	0	0	Error in data bit 0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	Error in check bit 0
1	0	0	0	1	1
1	0	0	1	0	2
1	0	0	1	1	3
1	0	1	0	0	4
1	0	1	0	1	5
1	1	1	1	0	No error
1	1	1	1	1	Non-correctable (multiple-bit) error

Note: Bit 7 is always high.

3.4 ERROR STATUS REGISTER (ESR)

This 7-bit register contains information about memory errors. The ESR reflects the latest error occurrance.

As shown in Table 3-3, bits 5 and 6 indicate the memory row number and bits 0 - 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome word) is in error. Bit 7 is always high.

3.5 SOFTWARE INITIALIZATION PROCEDURE

The following steps provide summarized programming information for the system initialization sequence.

Step 1:	Power on.
Step 2:	Reset.
Step 3:	Disable interrupts on the processor.
Step 4:	Clear the board memory.
Step 5:	Set the CSR to the desired operating mode, as described in Tables 3-1 and 3-2.
Step 6:	Enable interrupts on the processor.

***

CHAPTER 4. MEMORY BOARD OPERATION

4.1 INTRODUCTION

This chapter describes basic operations on the iSBC 028CX/056CX/012CX RAM boards. The boards operate in an identical manner; the difference among the boards is memory capacity (see Chapter 1). The boards can be accessed by both the Multibus interface and the iLBX Bus interface.

4.2 MEMORY OPERATIONS

Data is transferred between the Multibus interface or the iLBX Bus and the on-board RAM chips via bidirectional data buffers that maintain signal compatibility between the board and the bus. ECC operations are discussed separately in Section 4.3.

The following discussion refers generally to both iLBX Bus and Multibus interface operations. Although the two busses do not operate in an identical fashion, the scope of this discussion allows merging the two into one section. For additional information on the Multibus interface, refer to the INTEL MULTIBUS SPECIFICATION; for iLBX Bus information, refer to the INTEL iLBX BUS SPECIFICATION.

A typical operation on the iSBC 028CX/056CX/012CX RAM Boards is initiated when the bus master issues a memory address to all devices on the Multibus interface. The address is decoded by the select logic on the RAM boards to prepare the boards for the command that is following. After sending the address, the bus master may issue the READ or WRITE command to start the operation. The command is placed onto the Multibus interface a minimum of 50 nanoseconds after the address.

If a READ command is sensed (or $R/\overline{W} = 1$ in iLBX Bus operations) from the bus interface, the RAM boards perform a sequence of operations to READ data from the addressed memory location and place its contents onto the data lines (DAT0/ through DATF/). When the data has stabilized on the bus, the RAM boards issue a Transfer Acknowledge signal (XACK/ or ACK/ in iLBX Bus operations) to the bus master indicating that the data is available. In response to the Transfer Acknowledge signal, the bus master accepts the data from the bus interface and removes the READ command (MRDC/) and the RAM address from the bus control and address lines.

If a WRITE command is sensed (or $R/\overline{W} = 0$ in iLBX Bus operations) from the bus interface, the RAM boards perform a sequence of operations to WRITE a data byte into the memory at the address provided by the bus master via the bus interface address lines (ADR0/ through ADR17/). The bus master places the write data onto the bus interface coincident with issuing an address. The bus master then issues a WRITE command to the RAM boards after the data stablizes on the bus interface.

On receiving the command, the RAM board performs the WRITE operation: a sequence of events to write the data byte from the bus interface into the addressed RAM memory location.

On completion of the WRITE operation, the control logic for the RAM boards send a Transfer Acknowledge signal (XACK/) to the bus master indicating that the operation is completed. In response to the XACK/ signal, the bus master removes the WRITE command (MWTC/) from the Multibus interface. A minimum of 50 nanoseconds later, the bus master deactivates the data lines and the address lines on the Multibus interface.

The refresh logic required by the dynamic RAM chips is on the board. The refresh logic is capable of providing refresh for one row of memory cells each 15 milliseconds. An optional off-board RAM refresh request is sensed by the board logic when the REFRESH/ line on the P2 connector goes LOW. (The iLBX Bus cannot be used if the external refresh is enabled by jumper connection. Refer to section 2.4 for jumper information). After a refresh cycle is requested, the actual execution may be delayed, but never longer than one READ or WRITE cycle.

4.3 ERROR CHECKING AND CORRECTION (ECC) OPERATION

The basic function of the on-board ECC circuitry is to detect any memory errors which occur during read operations. In the correcting mode, the board will then correct any single-bit errors. In the non-correcting mode, errors are still detected, but no action is taken to correct any bits. A correction cycle adds about 255 nanoseconds to the overall read or write cycle.

ECC operations are performed by an on-board Intel 8206 Error Detection and Correction Unit (device U120). The 8206 unit uses a separate group of RAM devices for its own memory operations. The 8206 unit uses a modified Hamming code to generate check bits for each 16-bit data word. Each data word has a 6-bit check bit word associated with it, stored in ECC memory.

When a particular data word is read, the ECC circuitry generates a new group of check bits and compares these to the check bits already stored in ECC memory. If the two check bit words compare, no error has occured. If the words do not compare, an error has occured.

From this point, several optional actions take place. Assuming the board is in the correcting mode, and a single-bit (correctable) error occurs, the 8206 correction unit will correct the data word to its original value. The 8206 correction unit creates an 7-bit syndrome word which contains the location of the error. The syndrome word is latched into the Error Status Register (ESR). The ESR can then be read by the host processor board, through the board I/O port, for error logging purposes. Refer to Section 3.4 for more information about the ESR. If the interrupt mode has been enabled, a Multibus interrupt will be generated.

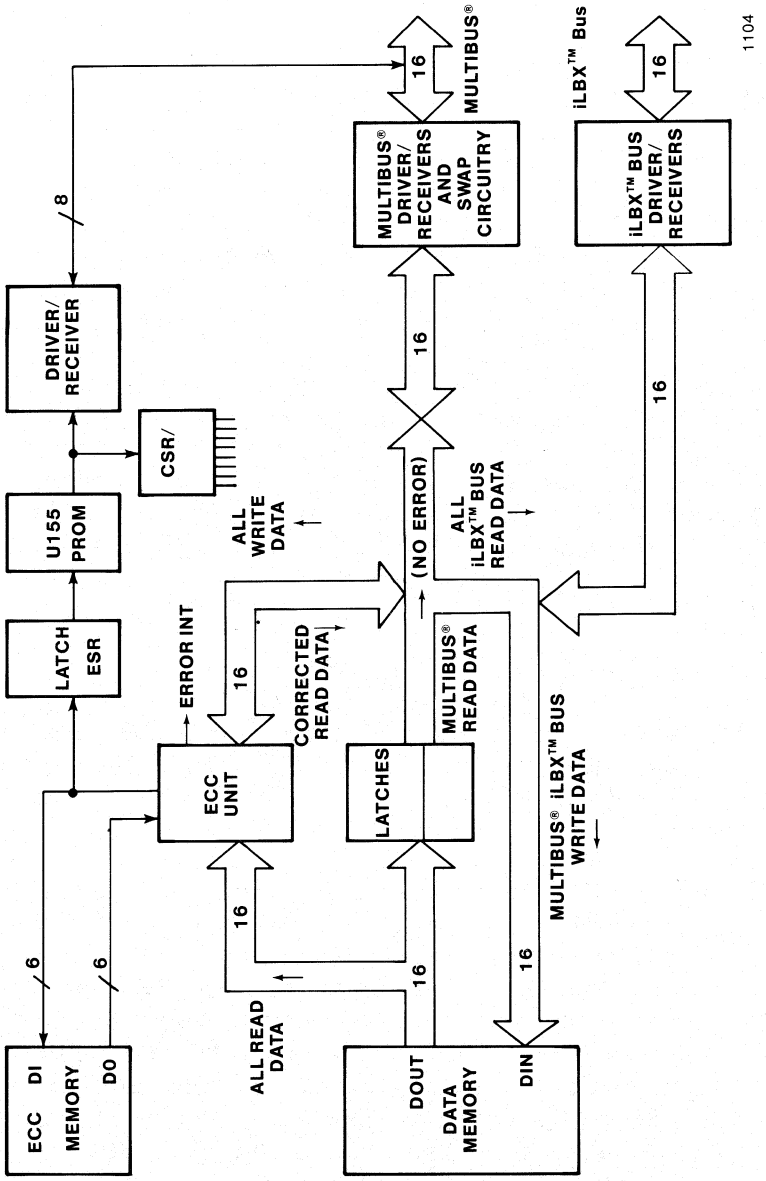


Figure 4-1. Data Path Simplified Diagram

When a multiple-bit error occurs, no correction action is possible. However, a syndrome word is generated for error logging purposes, and a Multibus interrupt is always generated when a non-correctable error occurs.

In a full 16-bit word write operation, data is written directly to memory and to the 8206 correction unit at the same time. The 8206 correction unit gererates the check bit word and places this into ECC memory.

For 8-bit byte write operations, part of the data word is overwritten and part is retained in memory. This is accomplished by performing a "write-byte" cycle. During this operation, the complete old word is read into the 8206 correction unit and corrected, with the syndrome word internally latched. Only that part of the word not to be modified is output. The part of the word to be overwritten is supplied by the Multibus or iLBX Bus. The 8206 correction unit then calculates check bits for the new word, using the byte from the previous read operation and the new byte from the system bus, and writes them into memory.

Board ECC operations are slightly different for Multibus and iLBX Bus operations. The following sections describe each bus ECC operation. During Multibus read and write operations, all ECC activity is carried on in parallel to data transfers. However, in iLBX read operations, ECC activity is carried on in a serial fashion. Figure 4-1 illustrates this concept, with a simplified block diagram. The following sections describe these operations in greater detail.

4.3.1 MULTIBUS® ECC OPERATION

During a Multibus write operation, the data word is written directly into memory. At the same time the data word is examined by the ECC circuitry to produce the corresponding check bit word. The check bit word is then stored in ECC memory. See Figure 4-1.

During a Multibus read operation, the data word is latched in a register and released to the Multibus buffers. While latched, the data word is also examined by the ECC circuitry. If the ECC check bit words compare (indicating no error), the Multibus XACK/ signal (Transaction Complete) is generated. If the check bit words do not compare (indicating an error), an error has occurred, and the board will respond as programmed previously by the Control Status Register. If the correcting mode was selected, and the error was a single-bit error, the corrected data word is gated from the ECC unit onto the Multibus path (refer to Figure 4-1). Notice that the corrected word is not placed into memory. In addition, when an error (Multibus interface only) is detected and corrected, the read access time and cycle times of the board are extended by a maximum of 255 nanoseconds. Refer to Section 4.3.

4.3.2 iLBX™ BUS ECC OPERATION

During an iLBX Bus write operation, the data word is written directly into memory. At the same time the data word is examined by the ECC circuitry to produce the corresponding check bit word. The check bit word is then stored in ECC memory. See Figure 4-1.

During an iLBX Bus read operation, the data word is not latched in a register before release to the buffers. Instead, the data word is transferred directly into the 8206 unit for ECC operations. This is done because of certain iLBX Bus timing requirements. Instead, the timing of the iLBX Bus is such that higher efficiency is obtained by allowing the data to be examined and/or corrected by the ECC circuitry in all read operations. This scheme permits the iLBX Bus read to operate at top speed on every cycle, regardless of error detection.

4.3.3 DIAGNOSTIC MODE

When the board is in the diagnostic mode, it is possible to verify several ECC operations. Typically, there are three diagnostic operations which can be performed:

a. Examine the check bits generated during the write cycle;

b. Generate error, and examine the syndrome word generated during a read cycle;

c. Examine the check bits stored in ECC memory.

The first two options (A & B) are typically the most useful diagnostic operations. All three operations are described in the following parargraphs. Refer to Figure 4-1 for related information.

To verify that the on-board ECC circuitry is generating the appropriate check bits during a write cycle (option A above), program the CSR to the examine syndrome mode (refer to Tables 3-1 and 3-2 for programming information), write some data to memory, and read the check bits in the ESR. Notice that the data in the CSR will be updated each cycle, since the latch which stores this data is clocked on each cycle. The check bits are routed through the syndrome word PROM encoder before reaching the ESR. However, this PROM is in the transparent mode while in the examine syndrome mode, allowing actual check bits to be examined.

To verify that the on-board ECC circuitry is generating the appropriate syndrome word during a read cycle (option B above), first write all zeros to memory. Next, enter the diagnostic mode, thus disabling any further changes to ECC memory, and change the data memory to any value other than zero, i.e., write 0001 to the data memory. Since you are in the diagnostic mode, no changes are made to ECC memory. Now, during a read cycle, each syndrome word will contain an error code.

4.4 MULTIBUS® LOCK/ AND iLBX™ BUS LOCK/ SIGNALS

The iSBC 028CX/056CX/012CX RAM boards can respond to two separate "LOCK" signals. The Multibus LOCK/ signal enters the board at P1-25. The iLBX Bus LOCK/ signal enters the board at P2-53. In each bus, the LOCK/ signal is asserted by a master CPU board to prevent another master from accessing the board through the other bus. For example, if master "A" is reading data from the board over the Multibus lines and needs to keep master "B" from accessing the board over the iLBX Bus, then master "A" must assert its Multibus LOCK/ signal.

To lock the iLBX Bus master off the RAM board, the Multibus master board must assert its LOCK/ signal at least 15 nanoseconds prior to the rising edge of the current command (MRDC/ or MWTC/). The LOCK/ signal must be held active until 100 nanoseconds after the falling edge of the command, of the last locked cycle. Similarly, to lock the Multibus master off the RAM board, the iLBX Bus master board must assert its LOCK/ signal at least 15 nanosecods prior to the rising edge of the DSTB/ (Data Strobe) · signal, and hold LOCK/ active until locked cycles are completed. In summary, when a CPU board asserts the LOCK/ signal, all "dual-ported" memory resources will be locked from access by another bus.

***

CHAPTER 5. SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides service assistance information, a parts list, and a schematic diagram for the iSBC 028CX/056CX/012CX memory board.

5.2 SERVICE AND REPAIR ASSISTANCE

United States Customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

Western Region	(602) 869 - 4951
Midwestern Region	(602) 869 - 4392
Eastern Region	(602) 869 - 4045
International	(602) 869 - 4391

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5.3 REPLACEMENT PARTS

Table 5-1 provides a list of replacement parts for the iSBC 028CX/056CX/012CX memory board. Figure 5-1 is a parts location diagram for the board. Figure 5-2 shows the RAM site locations.

5.4 SCHEMATIC DIAGRAMS

Figure 5-3 is the schematic diagram of the iSBC 028CX/056CX/012CX memory board. These diagrams are subject to change without notice. For this reason the latest version of the schematic is shipped with the board.

Table 5-1. iSBC® 028CX/056CX/012CX Replacement Parts List

Reference Desg.	Description	Qty
C1, 21, 106, 125 139, 143	Capacitor, 22 uf, 15V ±10%, Tant.	6
C2-20, 22, 24-52 54-76, 79-105, 107-124, 126-138, 140-142, 144-147	Capacitor, 0.1 uf, 50V +80%-20%	137
C23, 77	Capacitor, 330 pf, 50V, ±5%	2
C53, 78	Capacitor, 68 pf, 50V, ±5%	2
DS1	LED, Red	1
E1 - 144	Post, W/W Interconnect	140
G1	Crystal, 64.1 KHz	1
U1, 29, 110, 116 126, 130	IC, 74S74	6
U2, 80, 146	IC, 74S08	3
U3, 55, 125, 140	IC, 74S00	4
U4	IC, 74S38	1
U5-23, 49-51	IC, Intel 2164 (iSBC 028C)	22
U5-23, 30-51, 77-79	IC, Intel 2164 (iSBC 056C)	44
U5-23, 30-51, 77-79 86-107, 121-123	IC, Intel 2164 (iSBC 012C)	88
U24	Delay Line, 300ns	1
U25, 26	IC, 74S37	2
U27, 81, 131	IC, 74S11	3
U28, 114, 118	IC, 74S32	3
U52, 109	Delay Line, 100ns	2
U53, 54	IC, 74S22	2
U56	IC, 74S132	1
U57, 112, 117, 140	IC, 74S04	4
U82	IC, 74S51	1
U83, 84, 85	IC, 74S64	3
U108	Delay Line, 250ns	1
U111, 119, 137	IC, 74S02	3
U113	IC, 74S10	1
U115, 139, 149, 151 159, 160	IC, 74S240	6
U120	IC, Intel 8206	1
U124	IC, 74S20	1
U127	IC, 2964B	1
U128	Pre-Programmed PAL 16L8 (Intel 144893-001)	1
U129	Pre-Programmed PAL 16L8 (Intel 144895-001)	1
U132, 138	IC, 74S112	2
U133	IC, 74LS139	1
U134	IC, 74S260	1
U135	Pre-Programmed PAL 16R4 (Intel 144894-001)	1
U141, 142	IC, 74S283	2
U143	IC, 74S175	1

Table 5-1. iSBC® 028CX/056CX/012CX Replacement Parts List (continued)

Reference Desg.	Description	Qty
U144, 153	IC, 74LS373	2
U147	IC, 74LS273	1
U148	IC, 74S05	1
U150, 161, 162	IC, 74LS240	3
U152	Pre-Programmed PAL 16L8 (Intel 144892-001)	1
U154, 163, 164	IC, 74LS640	3
U155	Pre-Programmed PROM 7649-5 (Intel 144896-001)	1
U157, 167, 168	IC, 74S373	3
U156, 165, 166	IC, 74LS245	3
U158 (iSBC 028C)	Pre-Programmed PAL 16L8 (Intel 144889-001)	1
U158 (iSBC 056C)	Pre-Programmed PAL 16L8 (Intel 144890-001)	1
U158 (iSBC 012C)	Pre-Programmed PAL 16L8 (Intel 144891-001)	1

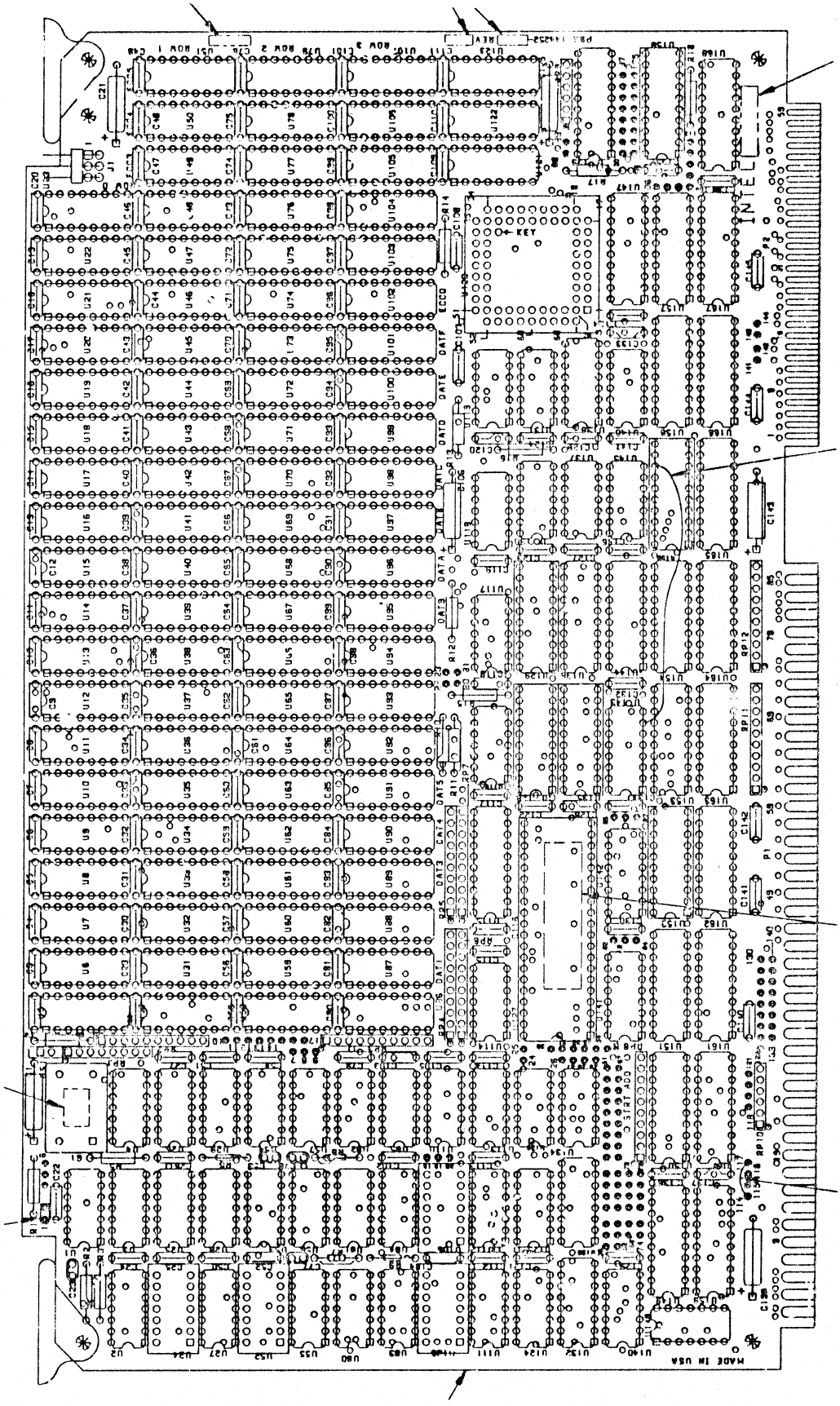


Figure 5-1. iSBC® 028CX/056CX/012CX Parts Location Diagram

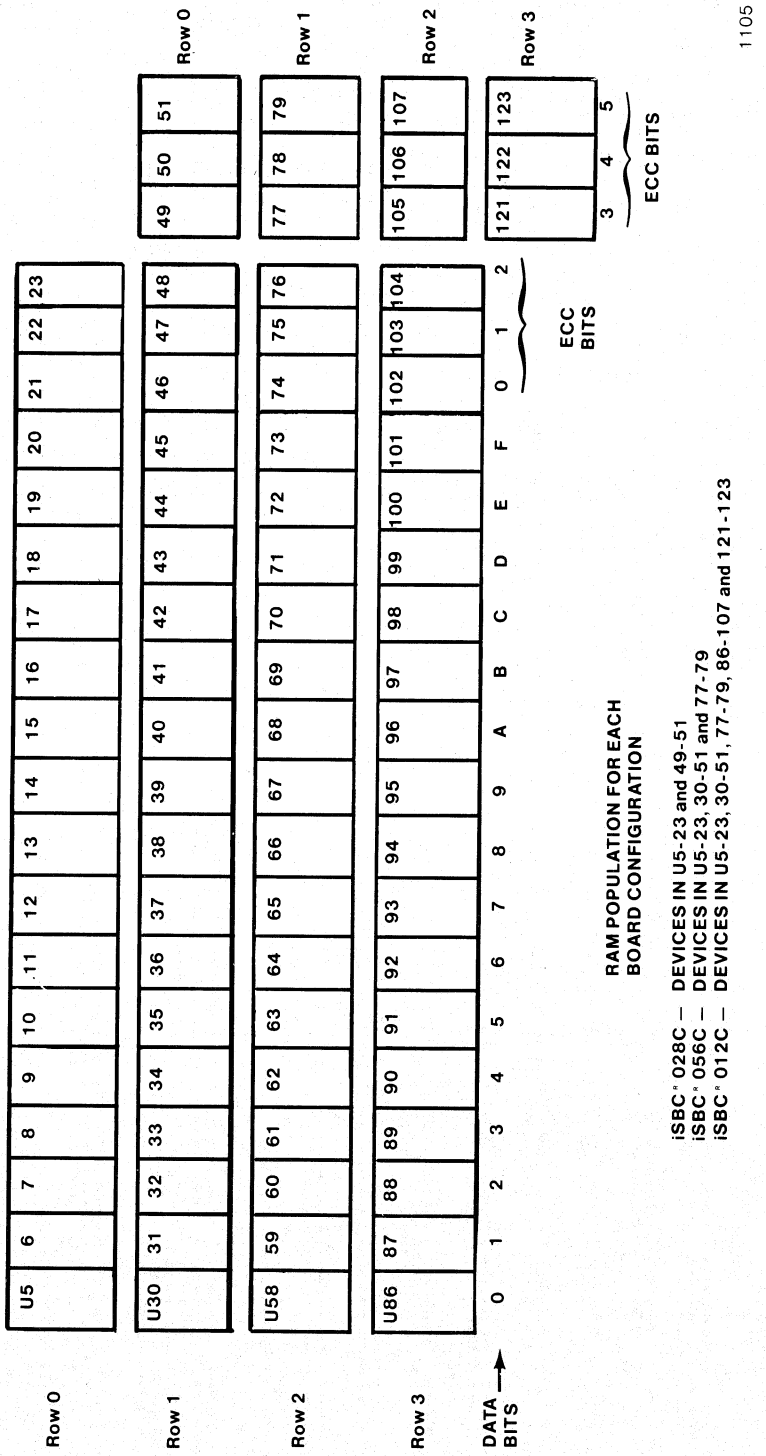


Figure 5-2. iSBC® 028CX/056CX/012CX RAM Device Location Diagram

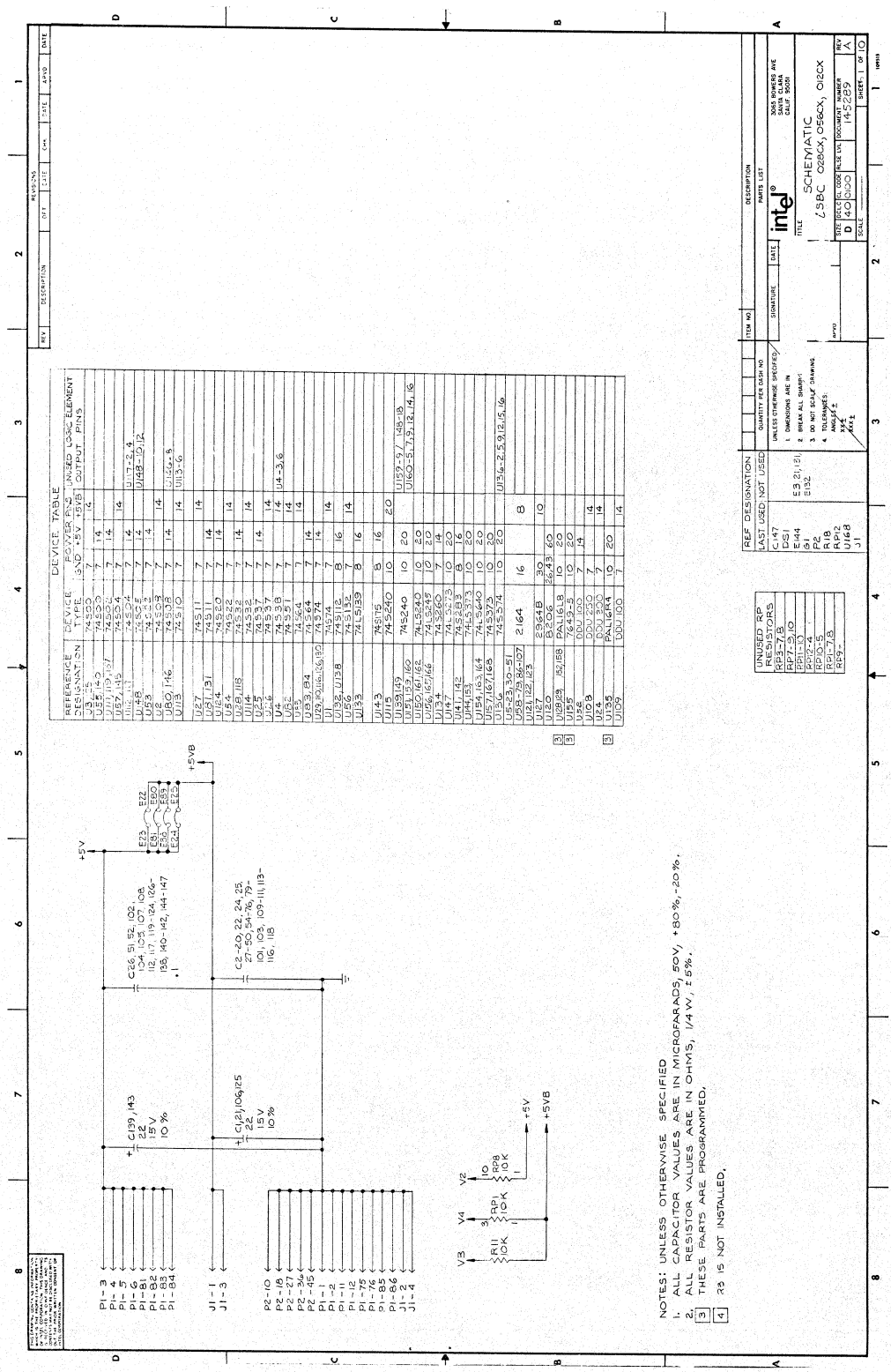


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 1)

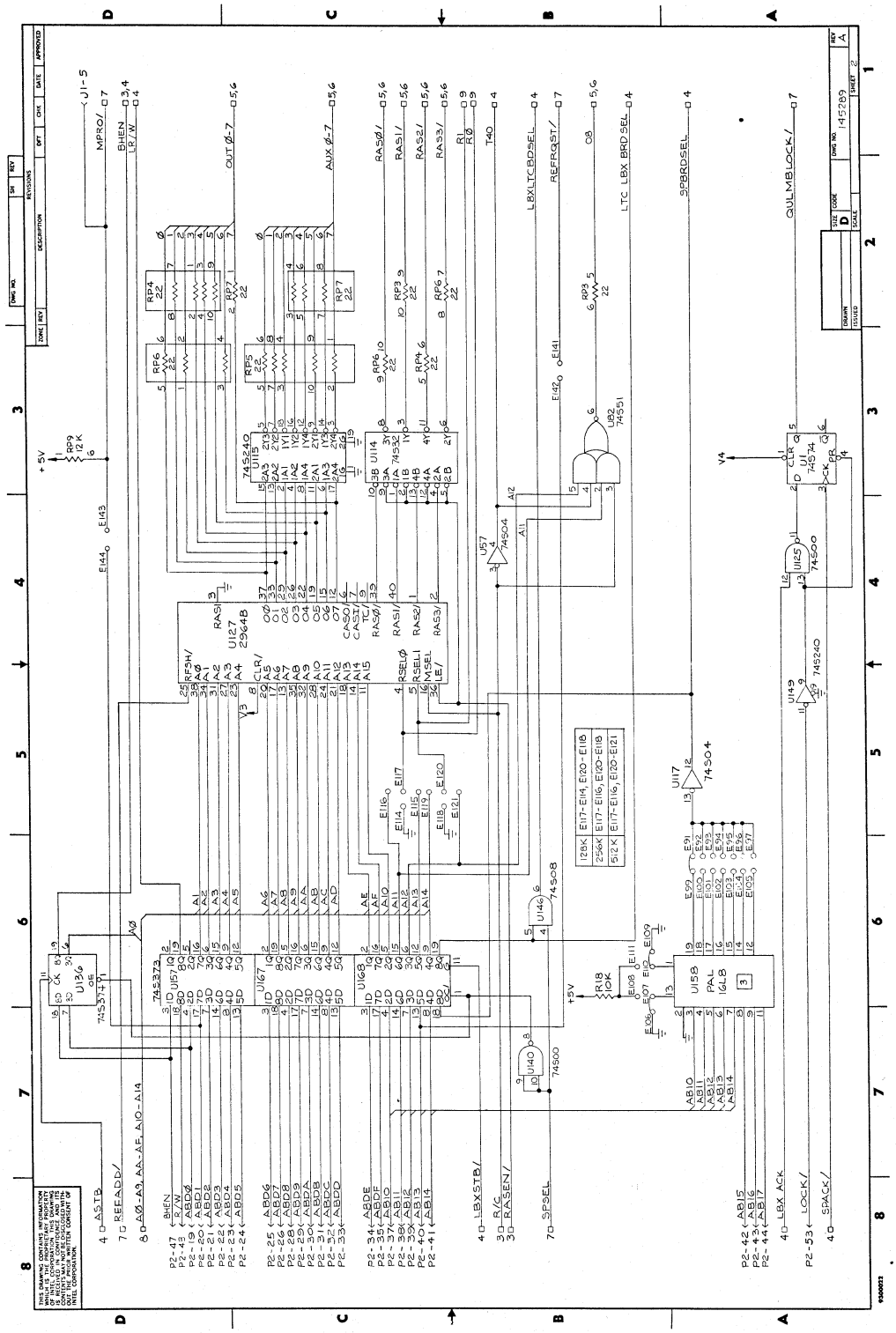


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 2)

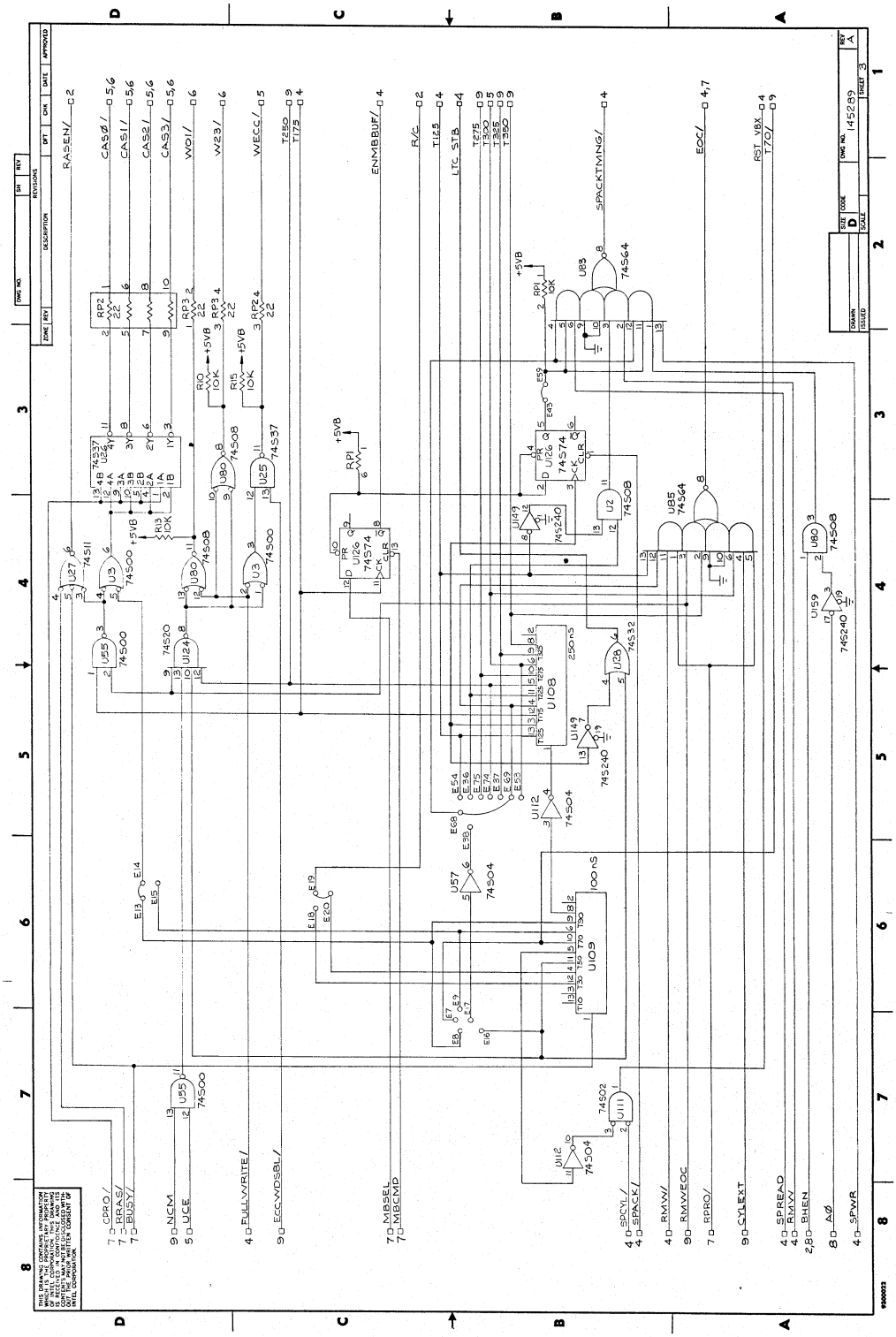


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 3)

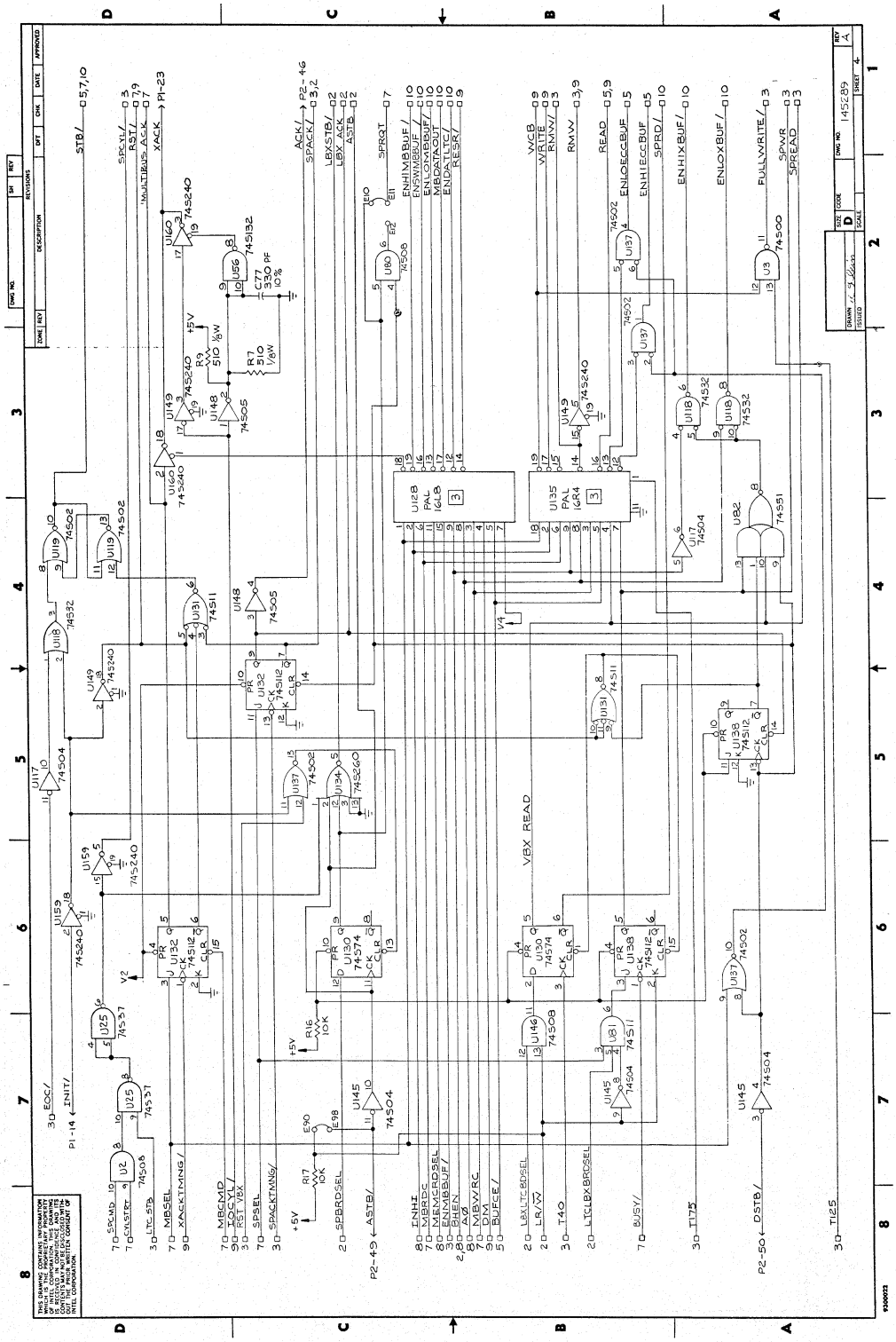


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 4)

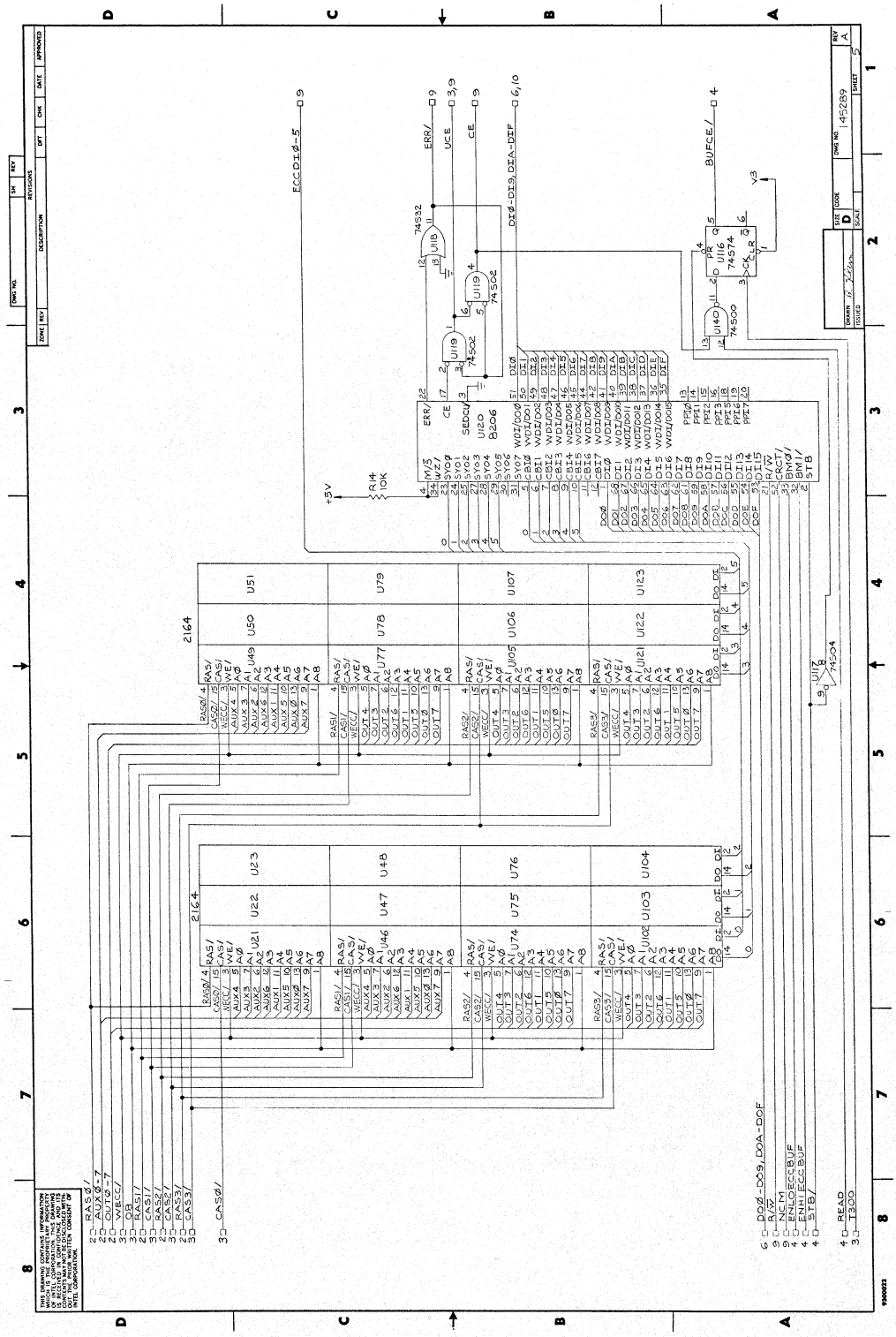


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 5)

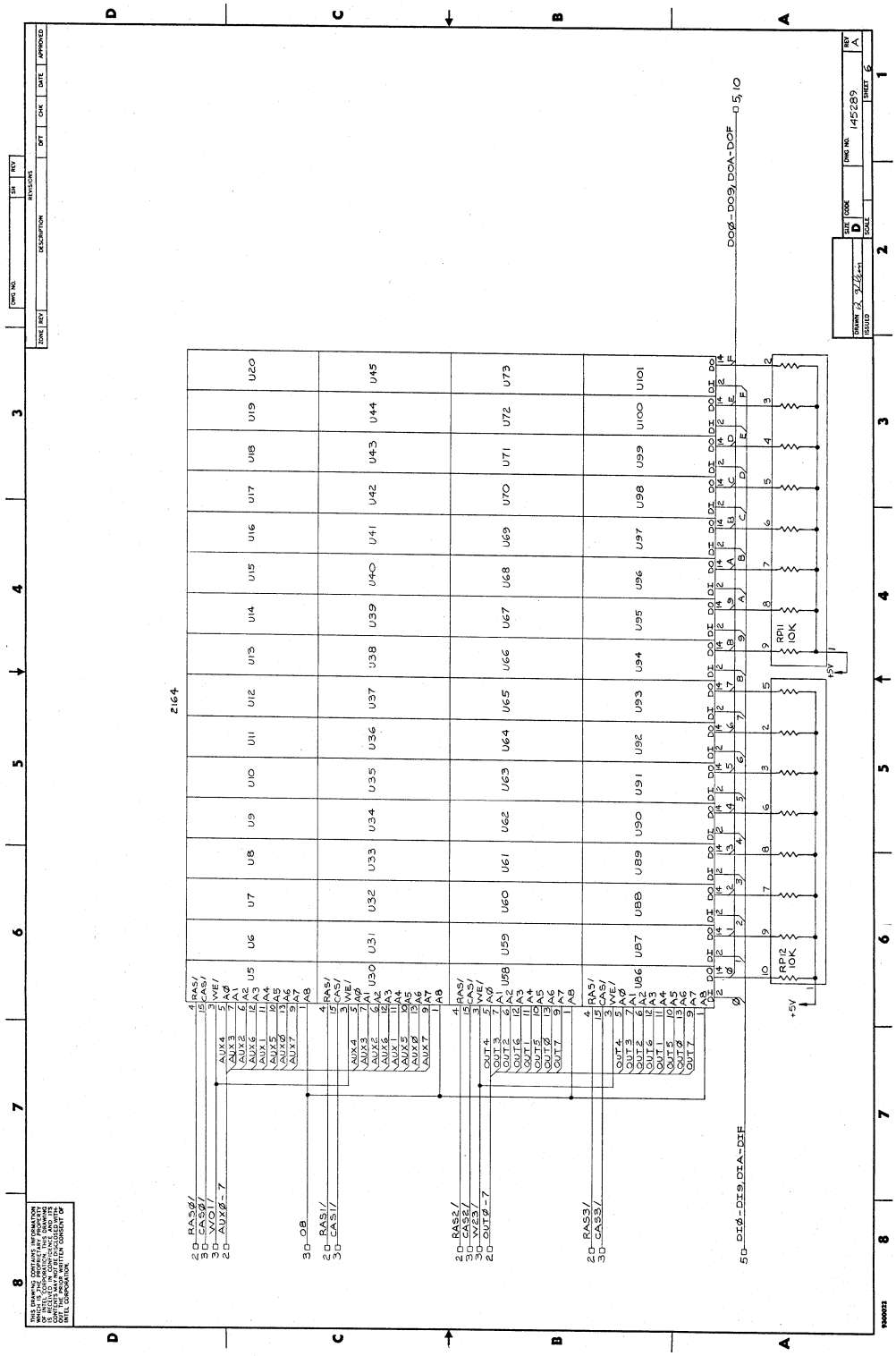


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 6)

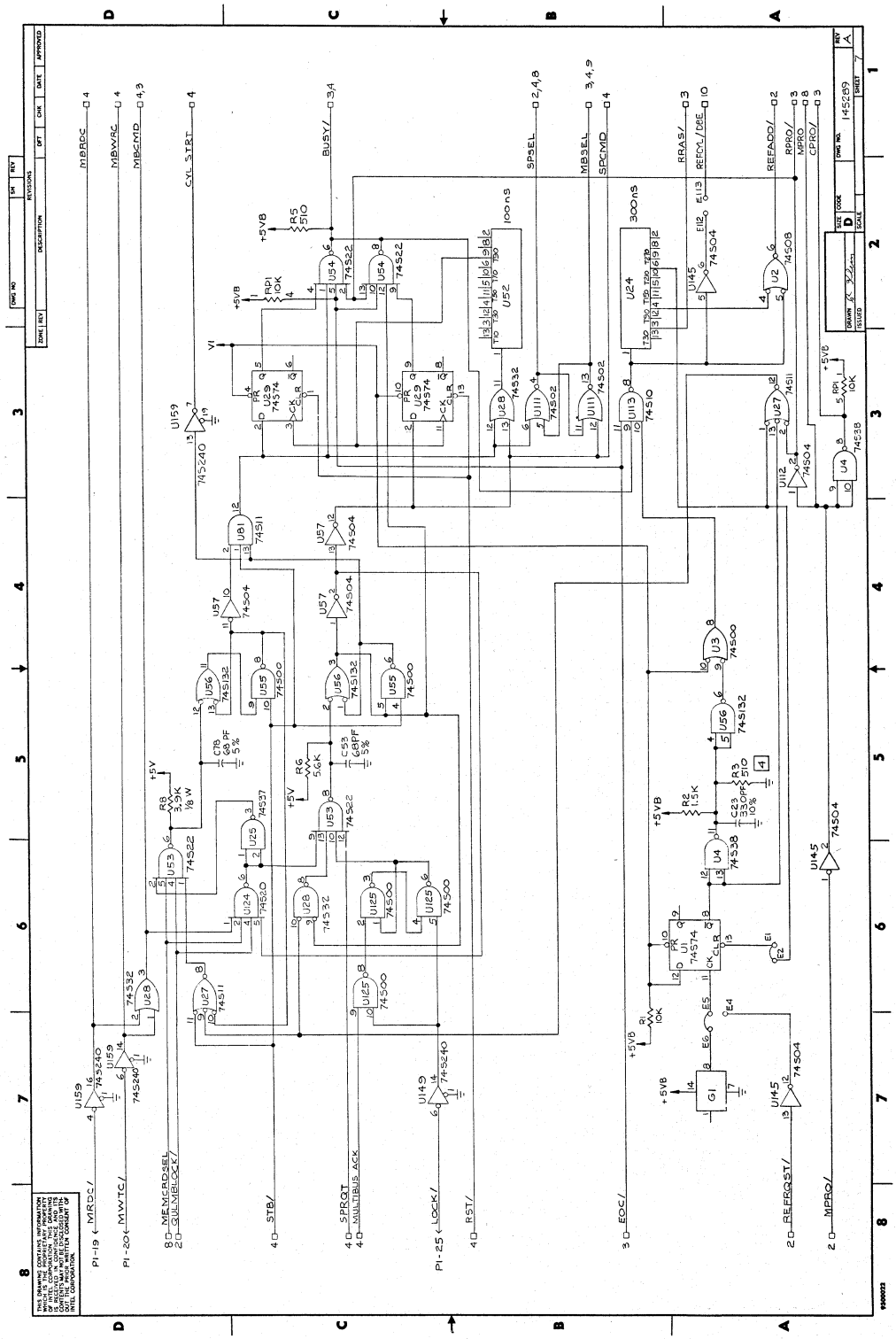


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 7)

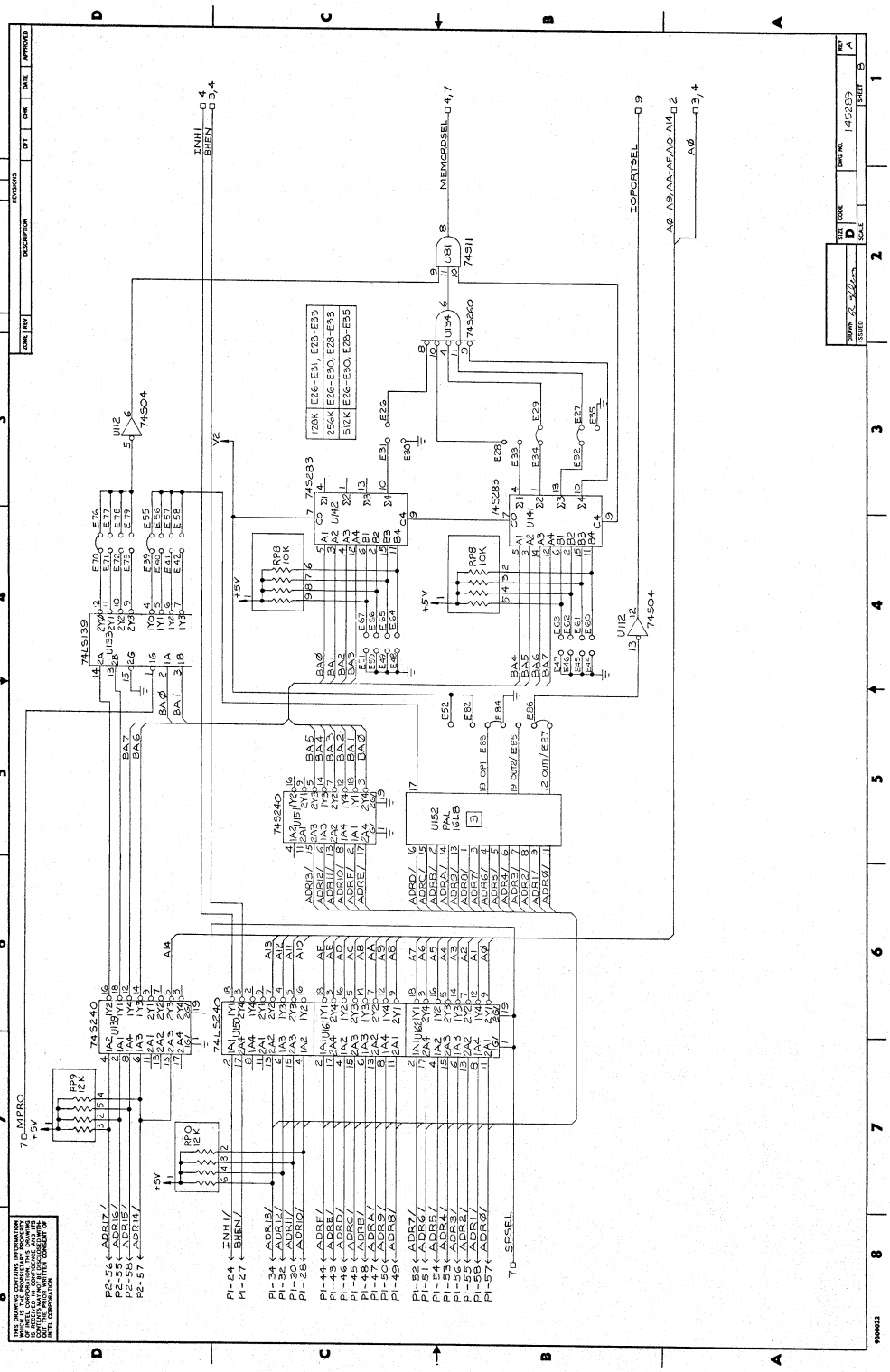


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 8)

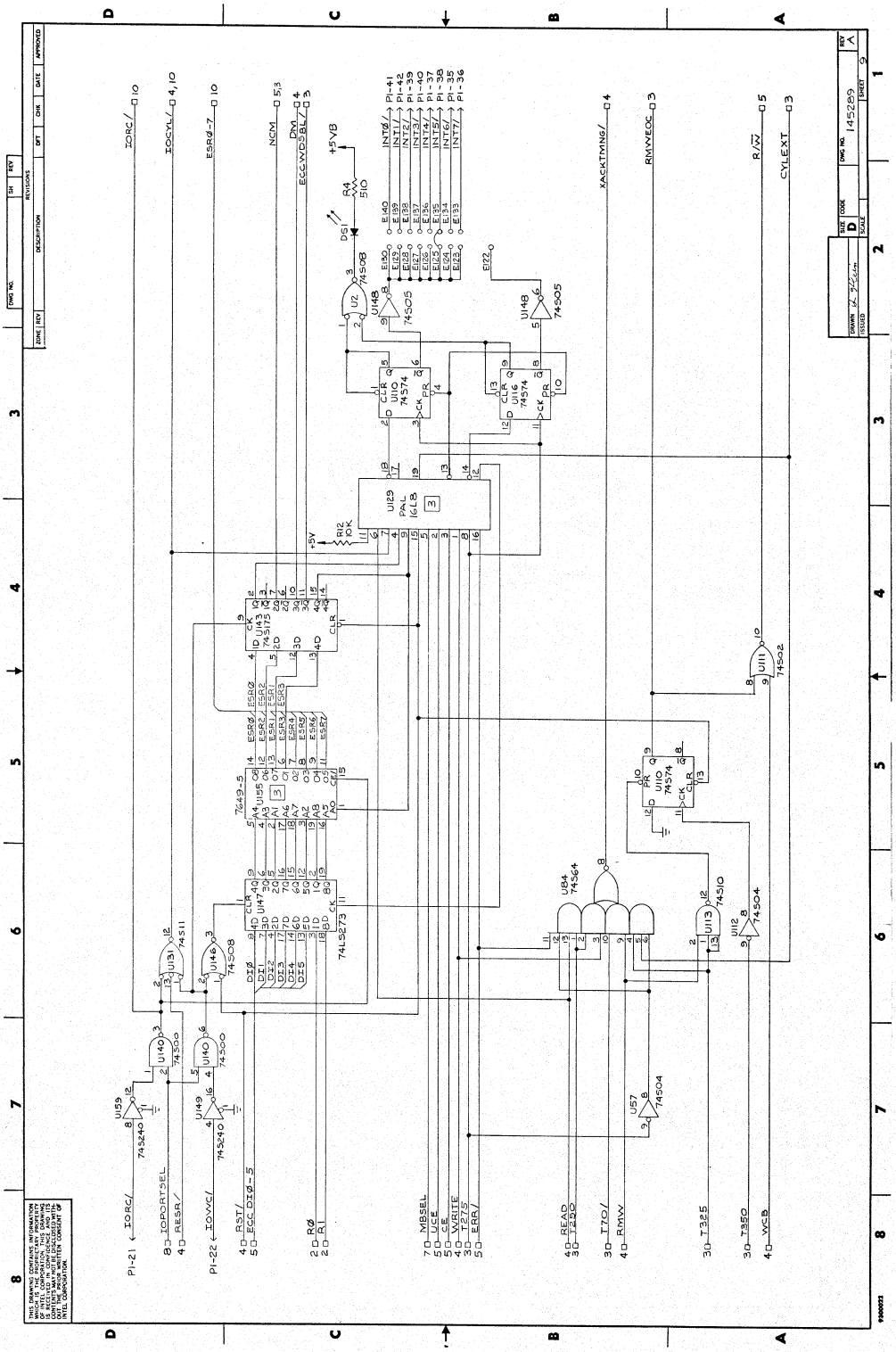


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 9)

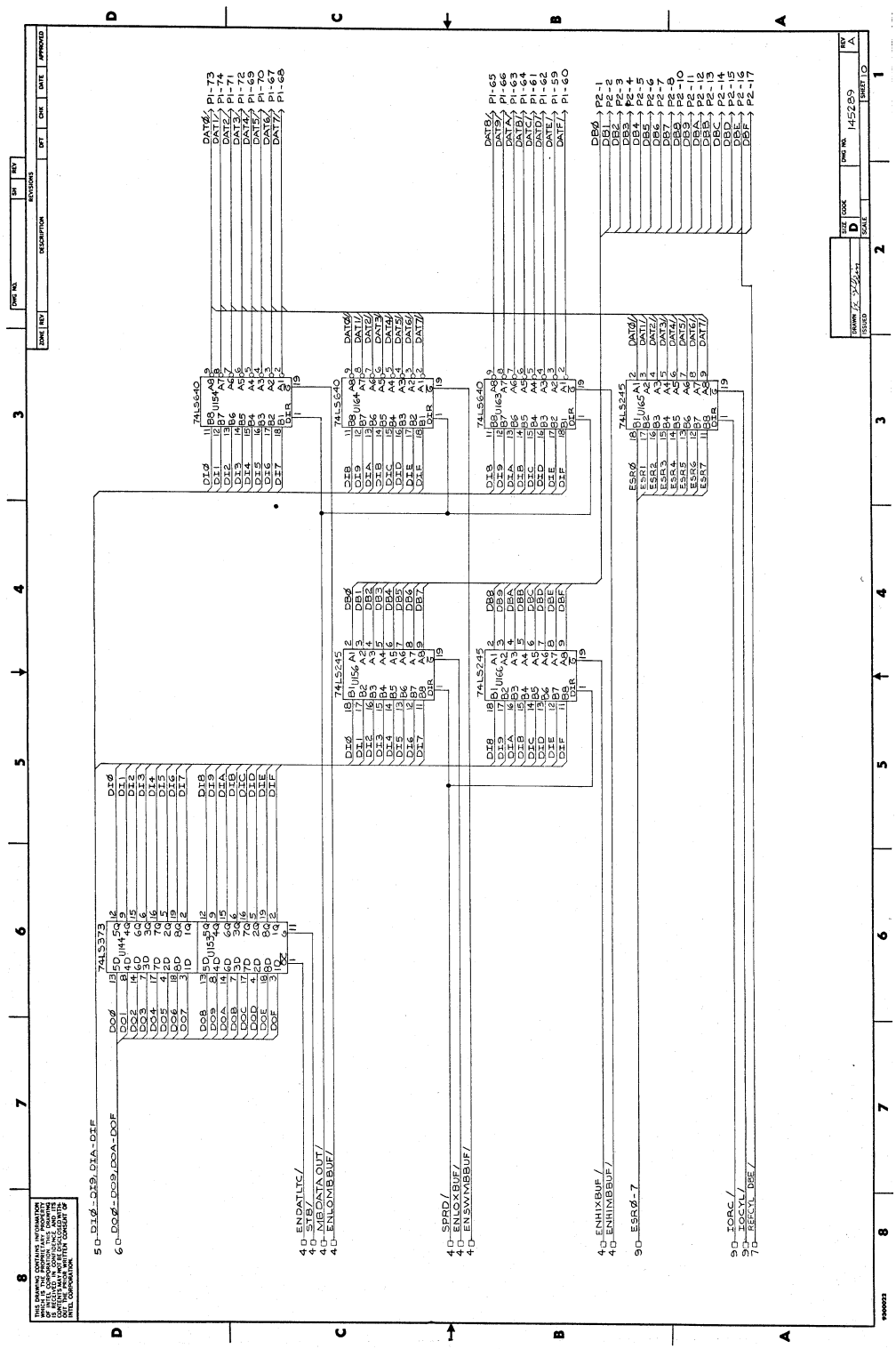


Figure 5-3. iSBC® 028CX/056CX/012CX Schematic Diagram (Sheet 10)

APPENDIX A. MULTIBUS® INFORMATION

Connector P1 pin assignments are listed in Table A-1 and descriptions of the signal functions are provided in Table A-2.

Signal names indicate the active state of the signal on the Multibus interface. If the signal name ends with a slash (/), the signal is active when LOW; if the signal does not end with a slash, the signal is active when HIGH.

AC characteristics for the P1 interface are provided in Table A-3. Table A-4 contains the DC characteristics for the P1 interface. Each parameter in the AC characteristics table appears in the timing diagram shown in Figure A-1.

For additional Multibus information, refer to the INTEL MULTIBUS SPECIFICATION document.

Table A-1. Multibus® Connector P1 Pin Assignments for iSBC® 028CX/056CX/012CX RAM Boards

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7			8		
	9		Reserved	10		Reserved
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13		Reserved	14	INIT/	Reset
	15		Reserved	16		Reserved
	17		Reserved	18		Reserved
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM

Table A-1. Multibus® Connector P1 Pin Assignments For iSBC® 028CX/056CX/012CX RAM Boards (continued)

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
BUS CONTROLS AND ADDRESS	25	LOCK/	Lock	26		Reserved
	27	BHEN/	Byte High Enable	28	AD10/	
	29		Reserved	30	AD11/	Address
	31		Reserved	32	AD12/	Bus
	33		Reserved	34	AD13/	
INTERRUPTS	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79		Reserved	80		Reserved
	81	+5V	+5Vdc	82	+5	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table A-2. Multibus® Connector P1 Signal Descriptions For iSBC® 028CX/056CX/012CX RAM Boards

Signal	Functional Description
ADR0/ - ADR17/	Address. These 24 lines transmit the address of the memory location or I/O port to be accessed. ADR17/ is the most significant address bit.
BHEN/	Byte High Enable. Used to select the upper byte (bits 8 through F) of a 10-bit word. The signal is functional only in systems that incorporate 16-bit memory and I/O devices.
DAT0/ - DATF/	Data. These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most-significant bit.
INH1/	Inhibit RAM. When issued by the processor board or PROM board, this signal will inhibit the RAM addresses on the iSBC 028CX/056CX/012CX board.
INIT/	Initialize. Resets the entire system to a known internal state.
INT0/ - INT7/	Interrupt Request Lines. These lines are parallel interrupt request lines. INT0/ is the highest priority, and INT7/ is the lowest priority.
IORC/	I/O Read. Indicates that the address of an I/O port is on the Multibus interface address lines and that the output of that port is to be read (placed) onto the Multibus interface data lines.
IOWC/	I/O Write. Indicates that the address of an I/O port is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be accepted by the addressed port.
LOCK/	Multibus Lock. When asserted, LOCK/ prevents access to dual ported RAM by any device except the asserting master. Do not confuse the Multibus LOCK/ signal with the iMBX Bus LOCK/ signal. See Appendix B for iMBX Bus signal information.
MRDC/	Memory Read Command. Indicates that the address of a memory loction is on the Multibus interface address lines and that the contents of that location are to be read (placed) on the Multibus interface data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the Multibus interface address lines and that the contents on the Multibus interface data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates to the bus master that the read or write operation is completed by the generating device and that valid data is available on the Multibus interface.

Table A-3. Multibus® AC Characteristics (Refer To Figure A-1)

Parameter	Description	Minimum	Maximum	Note
t_{AS}	Address setup time	45		
t_{DS}	Data setup time	0		
t_{AH}	Address hold time	0		
t_{DHW}	Write data hold time	50		
t_{DXL}	Read data setup to XACK	44		
t_{DHR}	Read data hold time	0	60	
t_{AX4H}	Acknowledge hold time	0	60	
t_{XACK}	Acknowledge time:			
	Memory Read/Full Write		350	1
	Write Byte		530	
	I/O		250	
t_{ID}	Inhibit delay from address		100	
t_{IS}	Inhibit setup time to CMD		-50	
t_{IH}	Inhibit hold time after CMD active		710	
t_{CS}	Command separation	50		
t_{CY}	Cycle time:			
	Memory read/write		460	1
	Memory byte-write		885	1
	I/O		500	1
t_{INIT}	INIT pulse width	50		
t_{RD}	Refresh delay time		760	
t_{RI}	Refresh interval		15.6us	

Notes: 1. Assume no error was detected, and no port switching took place. Cycle time and access time are extended by 105 ns when port switching takes place, and read cycle and access time are extended by 255 ns if an error is detected.

2. Unless noted, all units are in nanoseconds.

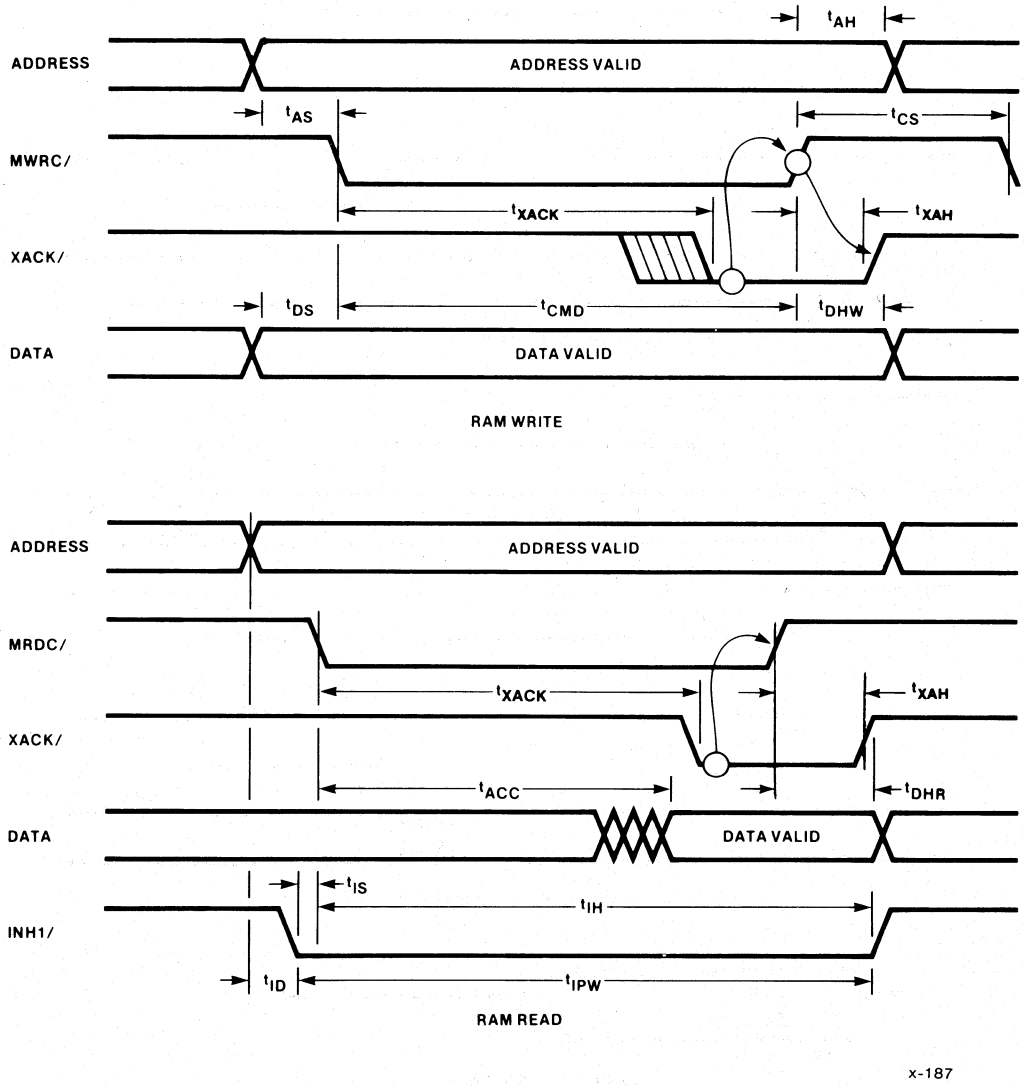


Figure A-1. Multibus® AC Timing

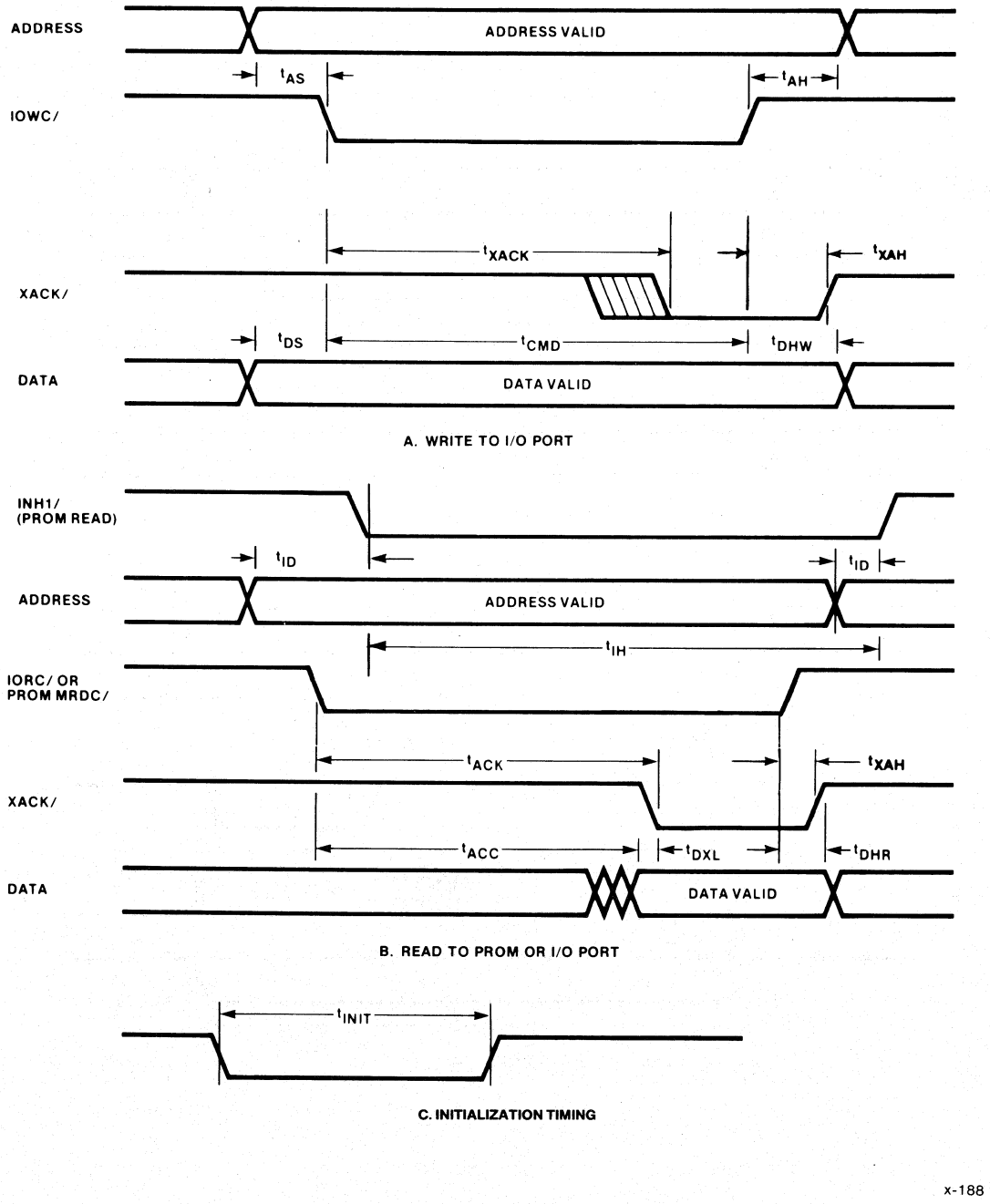


Figure A-1. Multibus® AC Timing (continued)

Table A-4. Multibus® Loading

Signal	Parameter	Test Condition	Minimum	Maximum	Units
MRDC/ MWRC/ IORC/ IOWC/ LOCK/ INIT/	VIL VIH IIL IIH CL	 VIN = 0.5V VIN = 2.7V 	 2 	0.8 -0.4 50 7	V V mA uA PF
INH1/ BHEN/	VIL VIH IIL IIH CL	 VIN = 0.4V VIN = 2.7V 	 2 	0.8 -0.2 20 7	V V mA uA PF
XACK/	VOL VOH CO	IOL = 64 mA IOH = -3 mA 	 2.4 300	0.55 	V V PF
DAT0/- DATF/	VIL VIH IIL IIH CL VOL VOH CO	 VIL = 0.4V VIH = 2.7V IOL = 24 mA IOH = -3 mA 	 2 2.4 300	0.8 -0.6 60 7 0.5 	V V mA uA pf V V PF
INT0/- INT7/	VOL VOH CL	IOL = 20 mA IOH = -250 uA 	 18	0.5 5.5 	V PF
ADR0/- ADR17/	VIL VIH IIL IIH CL	 VIN = 0.5V VIN = 2.7V 	 2 	0.8 -0.6 70 7	V V mA uA PF

***

APPENDIX B. iLBX™ BUS INFORMATION

Table B-1 lists the iLBX Bus pinout for connector P2. Table B-2 provides a brief description of each signal line in Table B-1. Table B-3 provides iLBX Bus DC loading characteristics. Figure B-1 gives the iLBX Bus AC timing and Table B-4 provides the corresponding times for this diagram. For additional iLBX Bus information, refer to the INTEL iLBX BUS SPECIFICATION document.

Table B-1. iLBX™ Bus Connector P2 Pin Assignments
For iSBC 028CX/056CX/012CX RAM Boards

Component Side			Solder Side		
Pin	Mnemonic	Signal Name	Pin	Mnemonic	Signal Name
1	DB0	DATA LINE 0	2	DB1	DATA LINE 1
3	DB2	DATA LINE 2	4	DB3	DATA LINE 3
5	DB4	DATA LINE 4	6	DB5	DATA LINE 5
7	DB6	DATA LINE 6	8	DB7	DATA LINE 7
9	GND	GROUND	10	DB8	DATA LINE 8
11	DB9	DATA LINE 9	12	DB10	DATA LINE 10
13	DB11	DATA LINE 11	14	DB12	DATA LINE 12
15	DB13	DATA LINE 13	16	DB14	DATA LINE 14
17	DB15	DATA LINE 15	18	GND	GROUND
19	ABD0	ADDRESS/DATA LINE 0	20	ABD1	ADDRESS/DATA LINE 1
21	ABD2	ADDRESS/DATA LINE 2	22	ABD3	ADDRESS/DATA LINE 3
23	ABD4	ADDRESS/DATA LINE 4	24	ABD5	ADDRESS/DATA LINE 5
25	ABD6	ADDRESS/DATA LINE 6	26	ABD7	ADDRESS/DATA LINE 7
27	GND	GROUND	28	ABD8	ADDRESS/DATA LINE 8
29	ABD9	ADDRESS/DATA LINE 9	30	ABD10	ADDRESS/DATA LINE 10
31	ABD11	ADDRESS/DATA LINE 11	32	ABD12	ADDRESS/DATA LINE 12
33	ABD13	ADDRESS/DATA LINE 13	34	ABD14	ADDRESS/DATA LINE 14
35	ABD15	ADDRESS/DATA LINE 15	36	GND	GROUND
37	AB16	ADDRESS EXT. LINE 16	38	AB17	ADDRESS EXT. LINE 17
39	AB18	ADDRESS EXT. LINE 18	40	AB19	ADDRESS EXT. LINE 19
41	AB20	ADDRESS EXT. LINE 20	42	AB21	ADDRESS EXT. LINE 21
43	AB22	ADDRESS EXT. LINE 22	44	AB23	ADDRESS EXT. LINE 23
45	GND	GROUND	46	ACK/	SLAVE ACKNOWLEDGE
47	BHEN	BYTE HIGH ENABLE	48	R/$\overline{W}$	READ NOT WRITE
49	ASTB/	ADDRESS STROBE	50	DSTB/	DATA STROBE
51	SMRQ/	Not Used On RAM Board	52	SMACK/	Not Used On RAM Bd.
53	LOCK/	ACCESS LOCK	54	GND	GROUND
55	ADR22/	MULTIBUS ADDRESS EXTENSION LINE 22	56	ADR23/	MULTIBUS ADDRESS EXTENSION LINE 23
57	ADR20/	MULTIBUS ADDRESS EXTENSION LINE 20	58	ADR21/	MULTIBUS ADDRESS EXTENSION LINE 21
59	RES	RESERVED	60	RES	RESERVED

Table B-2. iLBX™ Bus Signal Descriptions

DATA LINES (DB15 - DB0)	The 16 bi-directional data lines used to transfer data between the active bus master and the selected Slave device.
ADDRESS/DATA LINES (ABD15 - ABD0)	The 16 address/data lines used by the active bus master, along with the eight address extension lines, to select a Slave device and to specify a location in memory. For the 16-bit iLBX bus configuration, the address/data lines are single-direction lines used exclusively for addressing. For the 32-bit iLBX bus configuration, the address/data lines are time-multiplexed, bi-directional, lines used for memory addressing and data transfer.
ADDRESS EXTENSION LINES (AB23 - AB16)	The eight address extension lines used by the active bus master, along with the 16 address/data lines, to select a Slave device and specify a location in memory. The use of 24 address lines provides the ability to address 16-megabytes.
READ-NOT-WRITE ($R/\overline{W}$)	The active bus master controls the direction of data transfer with the Read-Not-Write line. When driven Low, the active bus master transmits the data and the selected slave device receives the data. Driving the Read-Not-Write line High reverses the transfer direction.
BYTE HIGH ENABLE (BHEN)	The active bus master in the 16-bit iLBX bus configuration controls the type of data transfer (8-bit or 16-bit) using the Byte High Enable (BHEN) element select line along with the low-order address bit (ABD0).
ADDRESS STROBE (ASTB/)	The active bus master drives the Address Strobe line Low to initiate a data transfer cycle.
DATA STROBE (DSTB/)	The active bus master drives the Data Strobe line Low to set-up the actual transfer of data.

Table B-2. iLBX™ Bus Signal Descriptions (continued)

ACKNOWLEDGE (ACK/)	The selected slave device responds to selection by the active bus master by driving the Acknowledge line low.
LOCK (LOCK/)	The active bus master restricts access through the Multibus port to dual port RAM memory on the iSBC 028CX/056CX/012CX board by driving the iLBX Bus LOCK line Low.

Table B-3. iLBX™ Bus Connector P2 DC Loading

Signal	Parameter	Test Condition	Minimum	Maximum	Units
ABD0 - ABDF					
BHEN, R/W	VIL			0.8	
	VIH		2		
	IIL	VIL = 0.5V		-0.25	mA
	IIH	VIH = 2.7		50	uA
	CL			18	PF
				0.8	V
AB10 - AB17	VIL		2.0		V
	VIH				
	IIL	VIL = 0.5V		-0.5	mA
	IIH	VIH = 2.4V		75	uA
	CL			18	PF
LOCK	VIL			0.8	V
BHEN/	VIH		2.0		V
	IIL	VIL = 0.4V		-400	uA
	IIH	VIL = 2.7V		50	uA
	CL			18	PF
ASTB/	VIL			0.8	V
DSTB/	VIH		2.0		V
	IIL	VIL = 0.5V		-2	mA
	IIH	VIH = 2.7V		50	uA
	CL			18	PF
ACK/	VOL	IOL = 20mA		0.5	V
	VOH	IOH = -250uA		5.5	V
	CO			40	PF
DB0 - DBF	VIO			0.8	V
	VIH		2		V
	IIL	VIL = 0.4V		-0.2	mA
	IIH	VIH = 2.7V		20	mA
	CL			18	PF
	VOL	IOL = 12mA		0.4	V
	VOH	IOH = -3mA	2.4		V
	CO			75	PF

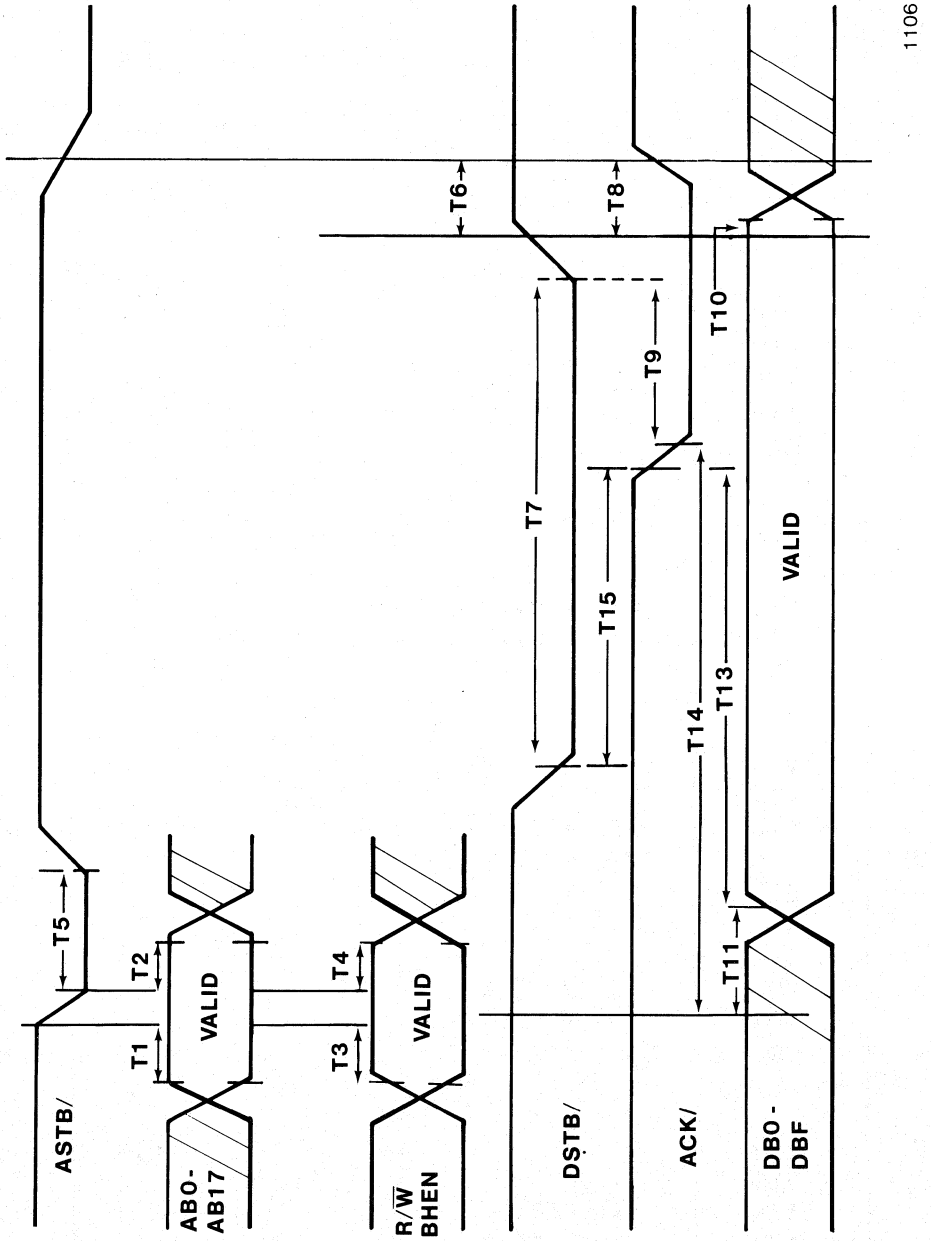


Figure B-1. iLBX™ Bus AC Timing

Table B-4. iLBX™ Bus AC Characteristics

Parameter	Description	Minimum	Maximum	Note
T1	AB0-17 setup to ASTB/	40	--	
T2	AB0-17 hold from ASTB/	25	--	
T3	R/W BHEN set-up to ASTB/	20	--	
T4	R/W BHEN hold time to ASTB/	25	--	
T5	ASTB pulse width	15	--	
T6	DSTB/ to ASTB/	25	--	
T7	DSTB pulse width	50	--	
T8	DSTB Inactive to ACK Inactive	0	40	
T9	DSTB hold time to ACK	80	--	
T14	ASTB to ACK			2,3
T15	DSTB Active to ACK	10		5
WRITE CYCLE				
T10	DATA hold time to DSTB	20		
T11	ASTB to data valid		80	4
READ CYCLE				
T10	DATA hold time to DSTB	0	45	
T13	DATA set-up to ACK			2

Notes:

1. All parameters are in nanoseconds.
2. For T13 and T14 see Section 2.4.7.
3. In the slow mode, T14 is related to DSTB instead of ASTB.
4. Required only for iLBX Bus fast mode.
5. System timing requirement. See Section 2.4.7.

APPENDIX C. PAL AND PROM PROGRAMMING

C-1. INTRODUCTION

The iSBC 028CX/056CX/012CX RAM boards utilize several programmed PAL devices for configuration selection purposes. Although these devices cover a wide range of options, they may not include the desired configuration for your application. These programmed devices may be removed and replaced with your own customized devices, to provide the desired configuration. In addition, a pre-programmed PROM is used for generating error status information. This appendix provides guidelines for programming the two user-alterable PAL devices, and provides a memory map of the pre-programmed PROM.

C-2. iLBX™ BASE ADDRESS PAL (U158)

This PAL is used to read the iMBX address lines and determine if the address on the lines is an on-board address. iMBX address lines AB10 through AB17 are connected directly to PAL inputs 3 through 11 (see Figure 5-3, sheet 2, and Section 2.4.1.4 of the text). Inputs 1 and 13 are used to select a range of addresses, and outputs 12, 14 through 19 select the specific group of 7 base addresses. Tables C-1A, B and C show the specific programming used on the default part, for each board. The PAL is programmed differently for each version of the board.

C-3. ECC CONTROL PORT ADDRESS PAL (U152 part number 144892-001)

This PAL is used to read Multibus address lines ADR0/ through ADRD/. In conjunction with other circuitry, the PAL decodes the address used for I/O control and status information (for ECC). Two other inputs (17 & 18) to the PAL select specific groups of addresses (refer to Figure 5-3, sheet 8, and Section 2.4.2 in the text). Table C-2 shows the specific programming used on the default part.

C-4. ERROR STATUS REGISTER ENCODING PROM (U155, part number 144896-001)

This pre-programmed PROM is used to encode the 6-bit syndrome word generated by the ECC unit into an 8-bit value for the ESR. Table 3-3 defines the purpose of each bit in the ESR. Table C-3 provides a memory map of this PROM.

Table C-1A. U158 PAL Programming For iSBC® 028CX Board

```
EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) /OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*/A20*A19*A18*A17
                EB*/EA*/IM*/A23*/A22*/A21*A20*A19*A18*/A17
IF (VCC) /OP1 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*/A18*/A17
                EB*/EA*/IM*/A23*/A22*/A21*A20*A19*A18*A17
IF (VCC) /OP2 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*/A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*/A17
IF (VCC) /OP3 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*A18*/A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*A17
IF (VCC) /OP4 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*A18*/A17
IF (VCC) /OP5 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*/A18*/A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*A18*A17
IF (VCC) /OP6 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*/A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*A19*/A18*/A17
DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC028C
 ACCORDING TO THE FOLLOWING TABLE:
EB    EA      OP #     STARTING ADDRESS

0     0       0          0K    (000000H)
0     0       1          128K  (020000H)
0     0       2          256K  (040000H)
0     0       3          384K  (060000H)
0     0       4          512K  (080000H)
0     0       5          640K  (0A0000H)
0     0       6          768K  (0C0000H)
0     1       0          896K  (0E0000H)
0     1       1          1024K (100000H)
0     1       2          1152K (120000H)
0     1       3          1280K (140000H)
0     1       4          1408K (160000H)
0     1       5          1536K (180000H)
0     1       6          1664K (1A0000H)
1     0       0          1792K (1C0000H)
1     0       1          1820K (1E0000H)
1     0       2          1948K (200000H)
1     0       3          2076K (220000H)
1     0       4          2204K (240000H)
1     0       5          2332K (260000H)
1     0       6          2560K (280000H)
```

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F 0 F 0 F F F F 5 A F F 3 C F F F 0 F F F 0 F F F 0 F 0 F 0 .
F 0 0 F F F F F A 5 F F 6 9 F F E 1 F F 1 E F F F 0 F 0 F 0 F 0 .
F 0 F 0 F F F F 5 A F F C 3 F F C 3 F F C 3 F F 3 C 0 F F 0 F 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B 0 B 0 B B B B 9 2 B B 3 8 B B 0 B B B B 0 B B B 0 B 0 B 0 .
B 0 0 B B B B B 2 9 B B A 1 B B 1 A B B 0 B B B B 0 B 0 B 0 B 0 .
B 0 B 0 B B B B 9 2 B B 8 3 B B 3 8 B B B 0 B B 0 B 0 B B 0 B 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

Table C-1B. U158 PAL Programming For iSBC® 056CX Board

```
EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) /OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*A18
                EB*/EA*/IM*/A23*/A22*A21*A20*A19*/A18
IF (VCC) /OP1 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*/A19*/A18
                EB*/EA*/IM*/A23*/A22*A21*A20*A19*A18
IF (VCC) /OP2 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*/A19*A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*/A19*/A18
IF (VCC) /OP3 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*A19*/A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*/A19*A18
IF (VCC) /OP4 = /EB*/EA*/IM*/A23*/A22*/A21*A20*/A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*A19*A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*A19*/A18
IF (VCC) /OP5 = /EB*/EA*/IM*/A23*/A22*/A21*A20*/A19*A18
                /EB*EA*/IM*/A23*/A22*A21*A20*/A19*/A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*A19*A18
IF (VCC) /OP6 = /EB*/EA*/IM*/A23*/A22*/A21*A20*A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*A20*/A19*A18
                EB*/EA*/IM*/A23*A22*/A21*A20*/A19*/A18

DESCRIPTION:
THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC056C
 ACCORDING TO THE FOLLOWING TABLE:
```

EB	EA	OP #	STARTING ADDRESS	
0	0	0	0K	(000000H)
0	0	1	256K	(040000H)
0	0	2	512K	(080000H)
0	0	3	768K	(0C0000H)
0	0	4	1024K	(100000H)
0	0	5	1280K	(140000H)
0	0	6	1536K	(180000H)
0	1	0	1792K	(1C0000H)
0	1	1	1948K	(200000H)
0	1	2	2204K	(240000H)
0	1	3	2460K	(280000H)
0	1	4	2716K	(2C0000H)
0	1	5	2972K	(300000H)
0	1	6	3228K	(340000H)
1	0	0	3484K	(380000H)
1	0	1	3740K	(3C0000H)
1	0	2	3996K	(400000H)
1	0	3	4252K	(440000H)
1	0	4	4508K	(480000H)
1	0	5	4764K	(4C0000H)
1	0	6	5020K	(500000H)

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F 0 F 0 F F F F F F F F 5 A F F 3 C F F F 0 F F F 0 F 0 F 0 F 0 .
F 0 0 F F F F F F F F A 5 F F 6 9 F F E 1 F F 1 E F 0 F 0 F 0 .
F 0 F 0 F F F F F F F F 5 A F F C 3 F F C 3 F F C 3 0 F 3 C F 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B 0 B 0 B B B B B B B B 9 2 B B 3 8 B B 0 B B B 0 B 0 B 0 B 0 .
B 0 0 B B B B B B B B B 2 9 B B A 1 B B 1 A B B 0 B B 0 B 0 B 0 .
B 0 B 0 B B B B B B B B 9 2 B B 8 3 B B 3 8 B B B 0 0 B 0 B B 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

Table C-1C. U158 PAL Programming for iSBC® 012CX Board

```
PAL16L8
PXADEC                          6/17/82  REVISED  9/3/82
LBX BUS ADDRESS DECODER  (512K)  COMPATIBILITY MODE

EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) /OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19  +
                /EB*EA*/IM*/A23*/A22*A21*A20*A19      +
                EB*/EA*/IM*/A23*A22*A21*A20*/A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19
IF (VCC) /OP1 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19   +
                /EB*EA*/IM*/A23*A22*/A21*/A20*/A19    +
                EB*/EA*/IM*/A23*A22*A21*A20*A19       +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A16+
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A17+
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17*/A16
IF (VCC) /OP2 = /EB*/EA*/IM*/A23*/A22*/A21*A20*/A19   +
                /EB*EA*/IM*/A23*A22*/A21*/A20*A19     +
                EB*/EA*/IM*A23*/A22*/A21*/A20*/A19    +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*A17+
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17
IF (VCC) /OP3 = /EB*/EA*/IM*/A23*/A22*/A21*A20*A19    +
                /EB*EA*/IM*/A23*A22*/A21*A20*/A19     +
                EB*/EA*/IM*A23*/A22*/A21*/A20*A19     +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A17*A16+
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A16
IF (VCC) /OP4 = /EB*/EA*/IM*/A23*/A22*A21*/A20*/A19   +
                /EB*EA*/IM*/A23*A22*/A21*A20*A19      +
                EB*/EA*/IM*A23*/A22*/A21*A20*/A19     +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18
IF (VCC) /OP5 = /EB*/EA*/IM*/A23*/A22*A21*/A20*A19    +
                /EB*EA*/IM*/A23*A22*A21*/A20*/A19     +
                EB*/EA*/IM*A23*/A22*/A21*A20*A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A16+
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A17*/A16+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18
IF (VCC) /OP6 = /EB*/EA*/IM*/A23*/A22*A21*A20*/A19    +
                /EB*EA*/IM*/A23*A22*A21*/A20*A19      +
                EB*/EA*/IM*A23*/A22*A21*/A20*/A19     +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18+
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A17
```

Table C-1C. U158 PAL Programming for iSBC® 012CX Board (continued)

DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC
ACCORDING TO THE FOLLOWING TABLE:

EB	EA	OP #	STARTING ADDRESS	
0	0	0	0K	(000000H)
0	0	1	512K	(080000H)
0	0	2	1024K	(100000H)
0	0	3	1536K	(180000H)
0	0	4	2048K	(200000H)
0	0	5	2560K	(280000H)
0	0	6	3072K	(300000H)
0	1	0	3584K	(380000H)
0	1	1	4096K	(400000H)
0	1	2	4608K	(480000H)
0	1	3	5120K	(500000H)
0	1	4	5632K	(580000H)
0	1	5	6144K	(600000H)
0	1	6	6656K	(680000H)
1	0	0	7168K	(700000H)
1	0	1	7680K	(780000H)
1	0	2	8192K	(800000H)
1	0	3	8704K	(880000H)
1	0	4	9216K	(900000H)
1	0	5	9728K	(980000H)
1	0	6	10240K	(A00000H)
1	1	0	0K	(000000H)
1	1	1	64K	(010000H)
1	1	2	128K	(020000H)
1	1	3	192K	(030000H)
1	1	4	256K	(040000H)
1	1	5	320K	(050000H)
1	1	6	384K	(060000H)

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F 0 F 0 F F F F F F F F F F F F 5 A F F 3 C F F F 0 F 0 F 0 F 0 .
F 0 0 F F F F F F F F F F F F F A 5 F F 6 9 F F E 1 F 0 1 E F 0 .
F 0 F 0 F F F F F F F F F F F F 5 A F F C 3 F F C 3 0 F C 3 3 C .
F 0 0 F 5 F F F 3 F F F F B F F F 0 F F F 0 F F F 0 0 F F 0 F 0 .
E 0 0 E E E E E C E E E 2 E E E E 0 E E E 0 E E E 0 0 E E 0 E 0 .
E 0 0 E E E E E E 2 E E C 2 E E 2 C E E E 0 E E E 0 0 E E 0 E 0 .
A 0 0 A A 0 A A A 8 A A A 0 A A 0 A A A A 0 A A A 0 0 A A 0 A 0 .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B 0 B 0 B B B B B B B B B B B B 9 2 B B 3 8 B B 0 B B 0 B 0 B 0 .
B 0 0 B B B B B B B B B B B B 2 9 B B A 1 B B 1 A B 0 0 B B 0 .
B 0 B 0 B B B B B B B B B B B 9 2 B B 8 3 B B 3 8 0 B B 0 0 B .
B 0 0 B 9 B B B 3 B B B 0 B B B B 0 B B B 0 B B B 0 0 B B 0 B 0 .
B 0 0 B B B B B 9 B B B 9 2 B B 2 9 B B B 0 B B B 0 0 B B 0 B 0 .
A 0 0 A A 8 A A A 0 A A A A A A 0 A A A A 0 A A A 0 0 A A 0 A 0 .
2 0 0 2 2 2 2 2 2 2 2 2 2 0 2 2 0 2 2 2 2 0 2 2 2 0 0 2 2 0 2 0 .
```

Table C-2. U152 PAL Programming

```
/A8 /AB /A7 /A6 /A5 /A4 /A3 /A2 /A1 GND /A0 /OUT1 /A9
/AA /AC /AD AEAF OP1 /OUT2 VCC

IF (VCC) /OUT1 = /OP1*/A0*/A1*/A2*/A3*/A4*/A5*A6*A7*A8*/A9*/AA*/AB*
                 /AC*/AD*/AEAF                                      +
                 OP1*A0*/A1*/A2*/A3*/A4*/A5*A6*A7*A8*/A9*/AA*/AB*
                 /AC*/AD*/AEAF
IF (VCC) /OUT2 = /OP1*/A0*/A1*/A2*/A3*/A4*/A5*A6*/A7

DESCRIPTION:

THE PROGRAM ASSIGNS AN IO ADDRESS ACCORDING TO THE FOLLOWING
TABLE:

OP1          OUT1                          OUT2

 0     01C0 41C0 81C0 C1C0 : 01C1 41C1 81C1 C1C1
                           :
 1       40   40   40   40 : USER PROGRAMMABLE
```

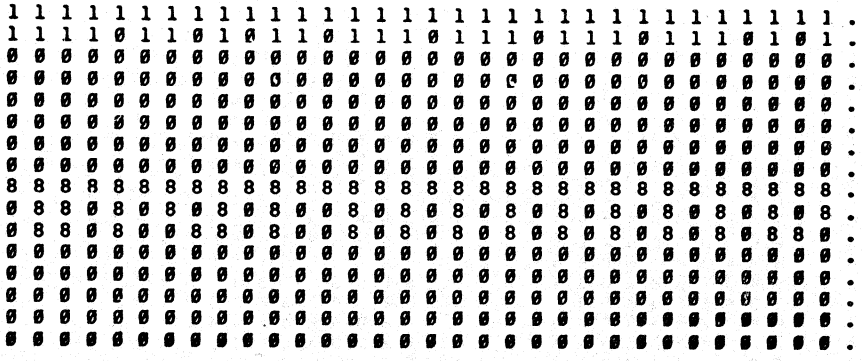


Table C-3. U155 PROM Memory Map

000	8C	3F	AD	1F	4D	3B	0C	1B	6D	7F	0C	5F	0C	7B	CE	5B
010	ED	BF	0C	9F	0C	BB	0C	9B	0C	FF	0C	DF	2E	FB	0C	DB
020	84	2F	A5	0F	45	2B	04	0B	65	6F	04	4F	04	6B	C6	4B
030	E5	AF	04	8F	04	AB	04	8B	04	EF	04	CF	26	EB	04	CB
040	2D	3E	0C	1E	0C	3A	AE	1A	0C	7E	AF	5E	6E	7A	0C	5A
050	0C	BE	6F	9E	EE	BA	0C	9A	EF	FE	0C	DE	0C	FA	0C	DA
060	25	2E	04	0E	04	2A	A6	0A	04	6E	A7	4E	66	6A	04	4A
070	04	AE	67	8E	E6	AA	04	8A	E7	EE	04	CE	04	EA	04	CA
080	CD	3D	0C	1D	0C	39	0E	19	0C	7D	0F	5D	8E	79	0C	59
090	0C	BD	8F	9D	4E	B9	0C	99	4F	FD	0C	DD	0C	F9	0C	D9
0A0	C5	2D	04	0D	04	29	06	09	04	6D	07	4D	86	69	04	49
0B0	04	AD	87	8D	46	A9	04	89	47	ED	04	CD	04	E9	04	C9
0C0	0C	3C	CF	1C	0C	38	0C	18	0C	7C	0C	5C	0C	78	0C	58
0D0	2F	BC	0C	9C	0C	B8	0C	98	0C	FC	0C	DC	0C	F8	0C	D8
0E0	04	2C	C7	0C	04	28	04	08	04	6C	04	4C	04	68	04	48
0F0	27	AC	04	8C	04	A8	04	88	04	EC	04	CC	04	E8	04	C8
100	88	37	A9	17	49	33	08	13	69	77	08	57	08	73	CA	53
110	E9	B7	08	97	08	B3	08	93	08	F7	08	D7	2A	F3	08	D3
120	80	27	A1	07	41	23	00	03	61	67	00	47	00	63	C2	43
130	E1	A7	00	87	00	A3	00	83	00	E7	00	C7	22	E3	00	C3
140	29	36	08	16	08	32	AA	12	08	76	AB	56	6A	72	08	52
150	08	B6	6B	96	EA	B2	08	92	EB	F6	08	D6	08	F2	08	D2
160	21	26	00	06	00	22	A2	02	00	66	A3	46	62	62	00	42
170	00	A6	63	86	E2	A2	00	82	E3	E6	00	C6	00	E2	00	C2
180	C9	35	08	15	08	31	0A	11	08	75	0B	55	BA	71	08	51
190	08	B5	8B	95	4A	B1	08	91	4B	F5	08	D5	08	F1	08	D1
1A0	C1	25	00	05	00	21	02	01	00	65	03	45	82	61	00	41
1B0	00	A5	83	85	42	A1	00	81	43	E5	00	C5	00	E1	00	C1
1C0	08	34	CB	14	08	30	08	10	08	74	08	54	08	70	08	50
1D0	2B	B4	08	94	08	B0	08	90	08	F4	03	D4	08	F0	08	D0
1E0	00	24	C3	04	00	20	00	00	00	64	00	44	00	60	00	40
1F0	23	A4	00	84	00	A0	00	80	00	E4	00	C4	00	E0	00	C0

***

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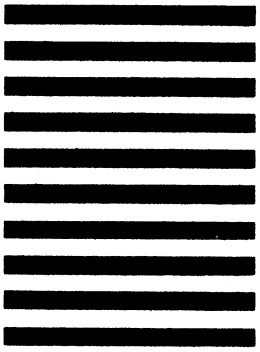

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