INTELLEC® SERIES II MICROCOMPUTER DEVELOPMENT SYSTEMS MODELS 220, 221, 222 AND MODELS 230, 231, 232 SERVICE INFORMATION

Manual Order Number: 9800878-01

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

PREFACE

This publication provides service information for the Intellec Series II Models 220/221/222 and Models 230/231/232 Microcomputer Development Systems.

This service information is organized to facilitate repair of the Development Systems by identification and replacement of faulty modules. For assistance from Intel Customer Engineers, refer to the "Repair and Service Assistance" section.

Other publications required for service of the Intellec Series II Development Systems are:

ISIS-II User's Guide
(Intel Order No. 9800306)

Intellec Series II Installation Manual
(Intel Order No. 9800559)

CRT Data Displays Service Manual
(Intel Order No. 9800622)

iSBC-032/048/064 RAM Board, Hardware Reference Manual
(Intel Order No. 9800488)

Intellec Series II, Models 710/711/712, Models 720/721/722, and Models 730/731/732 Diskette Subsystems, Service Information
(Intel Order No. 9800380)

MDS-DOS Diskette Operating System, Hardware Reference Manual
(Intel Order No. 9800212)

SA800/801 Diskette Storage Drive Maintenance Manual
(Intel Order No. 9800424)

More detailed information on the LSI IC's used in the Development Systems may be found in:

Intel 1978 Component Data Catalog
(Intel Order No. 110400)

Intel 1978 System Data Catalog
(Intel Order No. 610200)

MCS-80™ User's Manual
(Intel Order No. 9800153)

Peripheral Design Handbook
(Intel Order No. 9800676)

Other publications providing useful information are:

Intel Multibus Specification
(Intel Order No. 9800683)

Intel Memory Design Handbook
(Intel Order No. 111100)

A Guide to Microcomputer Development Systems
(Intel Order No. 9800558)

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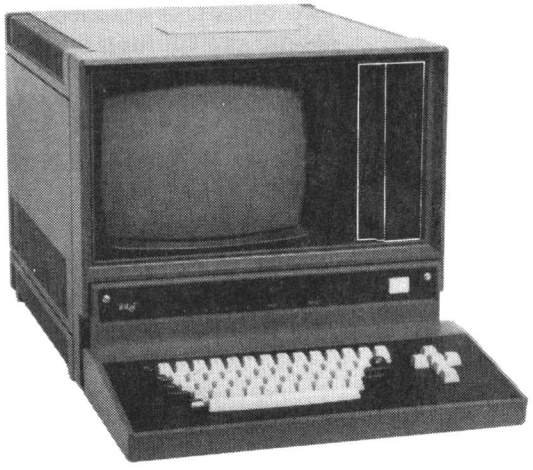
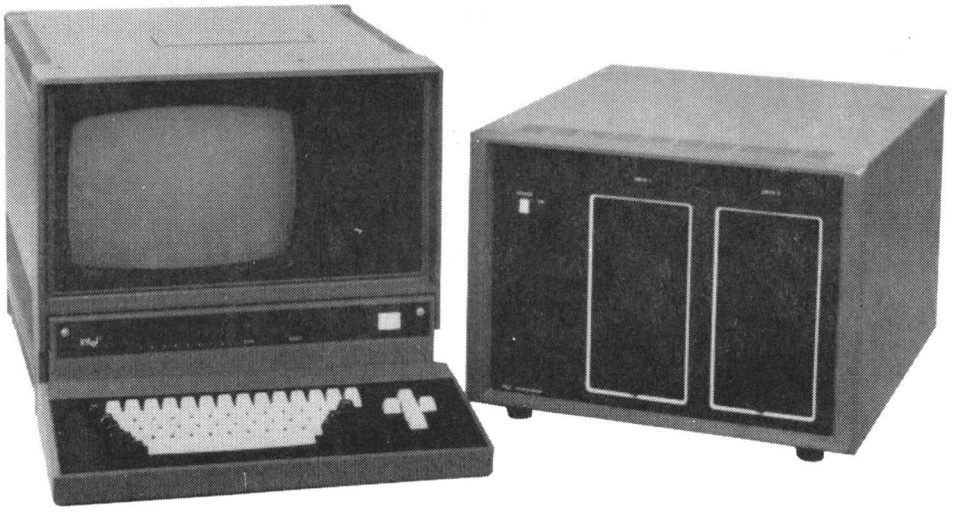
GENERAL INFORMATION

An Intellec Series II Microcomputer Development System is a basic development tool used to support design, development, and debugging of software and hardware based on a variety of microprocessor families. The Development Systems, with appropriate peripherals and In-Circuit Emulators (ICE), provide all the support needed for hardware and software development.

The Intellec Series II Models 220/221/222 Microcomputer Development Systems are complete systems with an integral diskette drive and 32K of RAM that can be used for program development. The Intellec Series Models 230/231/232 Microcomputer Development Systems are complete systems with a dual, external, double-density diskette drive and 64K of RAM. Any of the Development Systems can be easily updated by the addition of memory (to 64K bytes, maximum), diskette storage, I/O, or special-purpose modules.



MODEL 220 MICROCOMPUTER DEVELOPMENT SYSTEM



MODEL 230 MICROCOMPUTER DEVELOPMENT SYSTEM

GENERAL DESCRIPTION MODELS 220, 221, 222

SYSTEM COMPONENTS

Intellec Series II Models 220, 221, and 222 Microcomputer Development Systems each include a main chassis and a keyboard, and a diskette drive unit. The main chassis includes the following major components:

- CRT
- Integrated Processor Board (IPB)
- I/O Controller (IOC)

The IPB and the IOC are the primary controllers for the Development System. Each includes an 8080A-2 microprocessor.

EXPANSION CAPABILITY

The main chassis provides card slots for insertion of Multibus-compatible printed wiring assemblies (PWA's). The system's card capacity can be expanded by four card slots by adding an Intellec Series II Model 201 or Model 202 Expansion Chassis.

The Development System's random-access memory can be expanded to a total of 64K bytes by addition of an iSBC 032 32K byte RAM Memory board in an unused card slot of the main chassis.

The system's diskette capability can be expanded by adding diskette controller boards in unused card slots of the main chassis and connecting one or two drive units.

PERIPHERALS

The following peripherals can be connected to the Microcomputer Development Systems:

- Paper Tape Reader
- Paper Tape Punch
- Line Printer
- PROM Programmer
- TTY
- Modem
- Data Terminal

The TTY, modem, and data terminal are served by two serial I/O channels. As shipped, Channel 1 is a 20-mil current loop for TTY interface, but it can be reconfigured as an RS232C interface for modem or data terminal uses. Channel 2 is an RS232C interface.

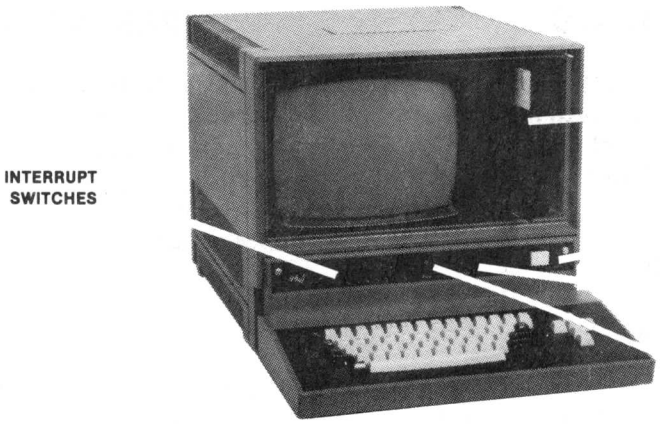
MULTIBUS

The Development Systems use the standard Multibus for communication between the IPB and any other boards that may be added to the main chassis or Expansion Chassis.

CONFIGURATION DIFFERENCES

The Models 220, 221, and 222 Development Systems differ as follows:

- Model 220: 110V, 60 Hz ac power, blue chassis
- Model 221: 230V, 50 Hz ac power, blue chassis
- Model 222: 230V, 50 Hz ac power, gray chassis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SINGLE DENSITY DISKETTE DRIVE
POWER SWITCH
RESET BUTTON
RUN INDICATOR
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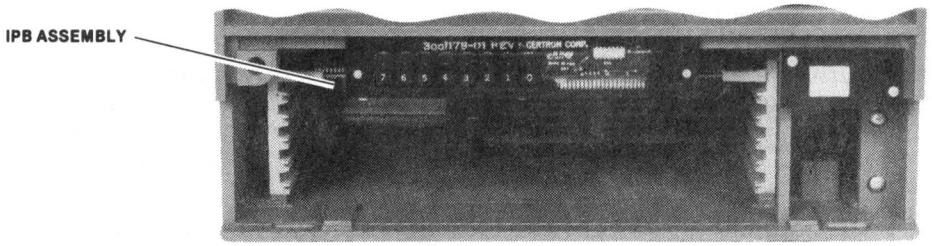
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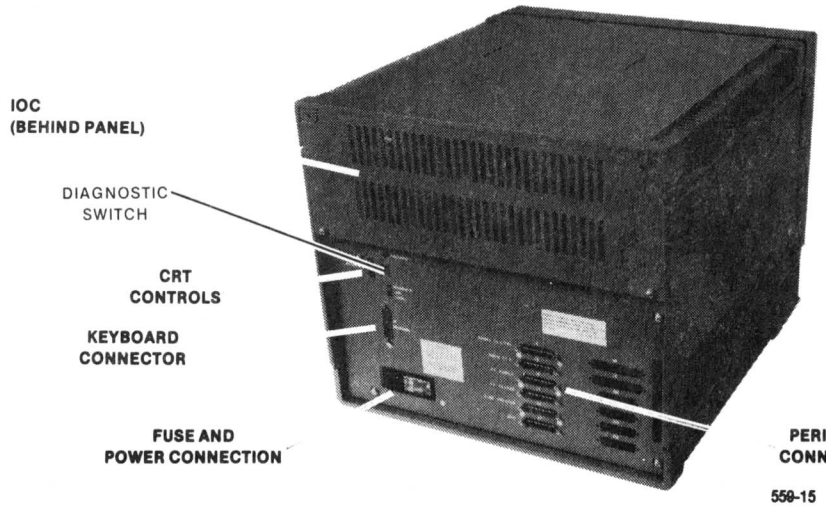
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GENERAL DESCRIPTION MODELS 230, 231, 232

SYSTEM COMPONENTS

Intellec Series II Models 230, 231, and 232 Microcomputer Development Systems each include a main chassis, a keyboard, and a diskette drive unit. The main chassis includes the following major components:

- CRT
- Integrated Processor Board (IPB)
- I/O Controller (IOC)
- iSBC 032 RAM Memory Board
- Floppy Diskette Controller

The IPB and the IOC are the primary controllers for the Development System. Each includes an 8080A-2 microprocessor.

The iSBC 032 adds 32K bytes of RAM memory to the 32K bytes provided on the IPB, for a system total of 64K bytes.

The Floppy Diskette Controller, consisting of an Interface Board and a Channel Board, provides double-density floppy diskette drive for four diskette drives, including the two in the diskette drive unit provided with the system.

EXPANSION CAPABILITY

The main chassis provides card slots for insertion of Multibus-compatible printed wiring assemblies (PWA's). The system's card capacity can be expanded by four card slots by adding an Intellec Series II Model 201 or Model 202 Expansion Chassis.

The system's diskette capacity can be expanded by connecting a second dual double-density diskette drive unit, or by installing a single-density drive in the main chassis, or both.

PERIPHERALS

The following peripherals can be connected to the Microcomputer Development Systems:

- Paper Tape Reader
- Paper Tape Punch
- Line Printer
- PROM Programmer
- TTY
- Modem
- Data Terminal

The TTY, modem, and data terminal are served by two serial I/O channels. As shipped, Channel 1 is a 20-mil current loop for TTY interface, but it can be reconfigured as an RS232C interface for modem or data terminal uses. Channel 2 is an RS232C interface.

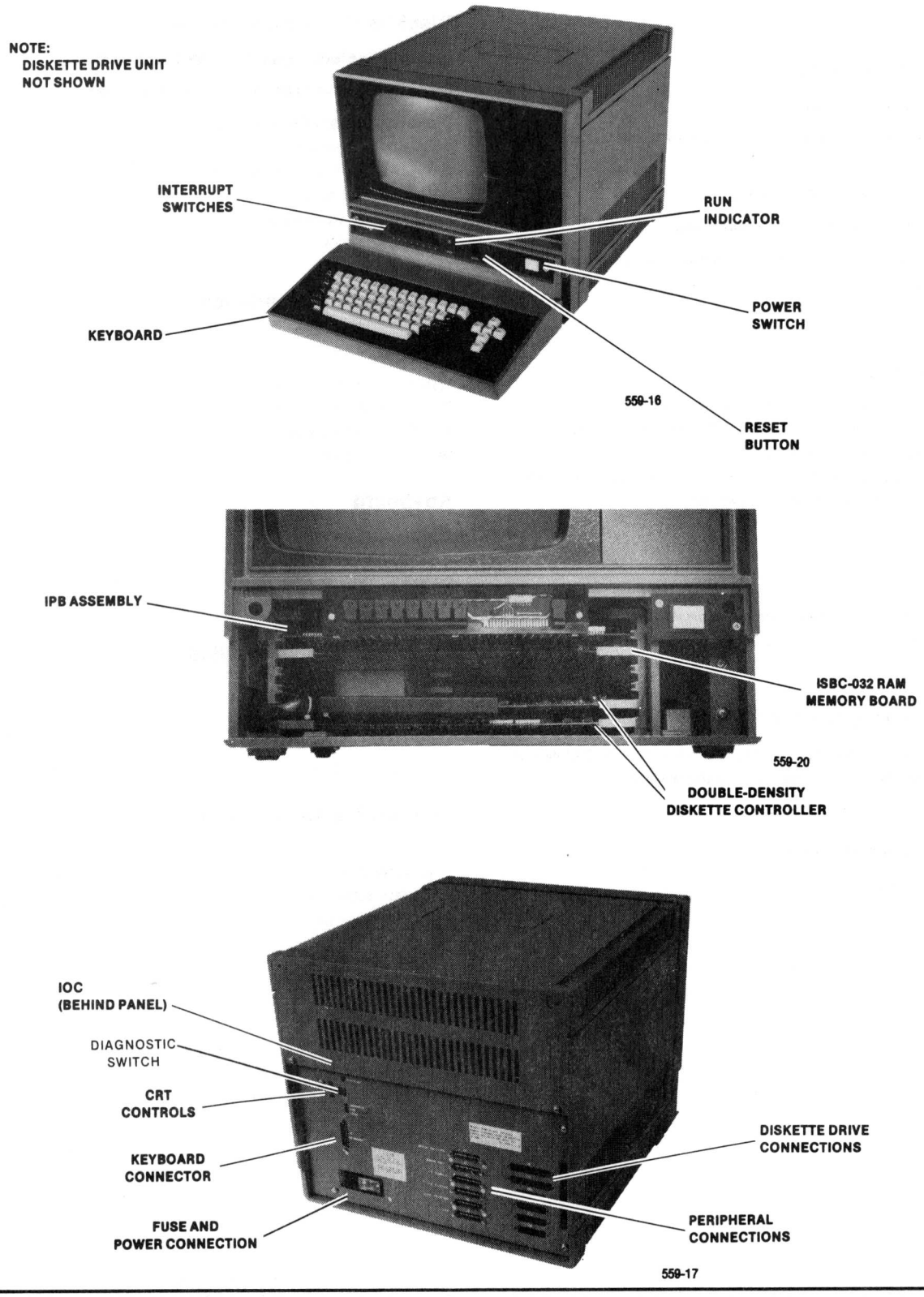
MULTIBUS

The Development Systems use the standard Multibus for communication between the IPB, the iSBC 032 RAM Memory, the Floppy Diskette Controller boards, and any other boards that may be added to the main chassis or Expansion Chassis.

CONFIGURATION DIFFERENCES

The Models 230, 231, and 232 Development Systems differ as follows:

- Model 230: 110V, 60 Hz ac power, blue chassis
- Model 231: 230V, 50 Hz ac power, blue chassis
- Model 232: 230V, 50 Hz ac power, gray chassis


NOTE:
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SPECIFICATIONS
MODELS 220, 221, 222

General

Host Processor (IPB)

8080A-2 based, operating at 2.600 Mhz.

RAM — 32K, expandable to 64K with iSBC 032 RAM boards (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

I/O Interfaces

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

Diskette (Single Density Drive)

Diskette System Capacity — 250K bytes (formatted)

Diskette System Transfer Rate — 160K bits/sec

Diskette System Access Time

Track-to-Track: 10 ms max

Average Random Positioning: 260 ms max

Rotational Speed: 360 rpm

Average Rotational Latency: 83 ms max

Recording Mode: FM

Physical Characteristics

Main Chassis

Width — 17.37 in. (44.12 cm)
Height — 15.81 in. (40. 16 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 86 lb (39 kg)

Keyboard

Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.0 cm)
Weight — 6 lb (3 kg)

Electrical Characteristics

AC Requirements

Model 220: 110V, 60 Hz

Model 221: 230V, 50 Hz

Model 222: 230V, 50 Hz

DC Power Available on Multibus

+5V (±5%): 22.5 amps

+12V (±5%): 2.3 amps

−12V (±5%): 0.25 amps

−10V (±5%): 0.8 amps

SPECIFICATIONS
MODELS 230, 231, 232

General

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 64K (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Bus — MULTIBUS, maximum transfer rate of 5 Mhz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

I/O Interfaces

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionaly provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

Diskette System Capacity (Double-Density Drives)

Unformatted

Per Disk: 6.2 megabits

Per Track: 82.0 kilobits

Formatted

Per Disk: 4.1 megabits

Per Track: 53.2 kilobits

Diskette Performance

Diskette System Transfer Rate — 500 kilobits/sec

Diskette System Access Time

Track-to-Track: 10 ms

Head Settling Time: 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm

Average Rotational Latency — 83 ms

Recording Mode — M^2FM

Physical Characteristics

Main Chassis

Width — 17.37 in. (44.12 cm)
Height — 15.81 in. (40.16 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 73 lb (33 kg)

Keyboard

Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.86 cm)
Weight — 6 lb (3 kg)

Dual Drive Chassis (Intellec DDR)

Width — 16.88 in. (42.88 cm)
Height — 12.08 in. (30.68 cm)
Depth — 19.0 in. (48.26 cm)
Weight — 64 lb (29 kg)

Electrical Characteristics

AC Requirements

Model 230: 110V, 60 Hz

Model 231: 230V, 50 Hz

Model 232: 230V, 50 Hz

DC Power Available on Multibus

+5V (±5%): 15.75 amps

+12V (±5%): 2.3 amps

−12V (±5%): 0.25 amps

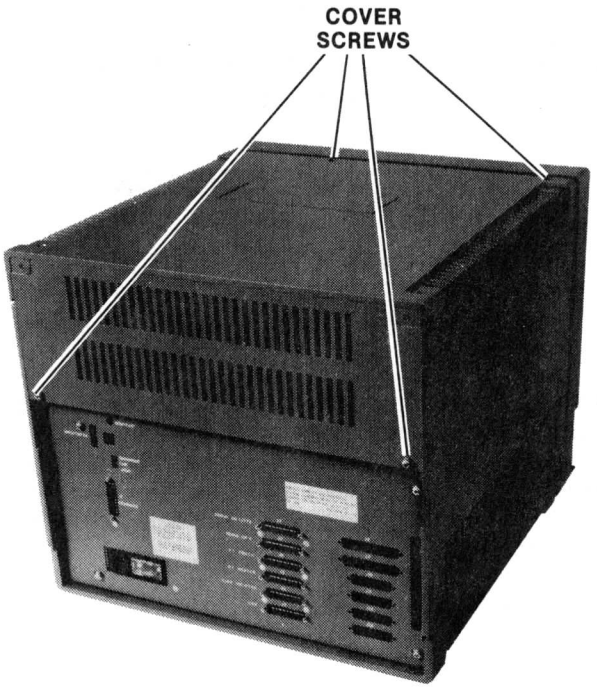
−10V (±5%): 0.8 amps

INSPECT THE EQUIPMENT

After receiving your Intel product, inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

After you have removed the unit from the shipping carton, inspect the exterior of the chassis, then remove the top cover to inspect the inside of the chassis.

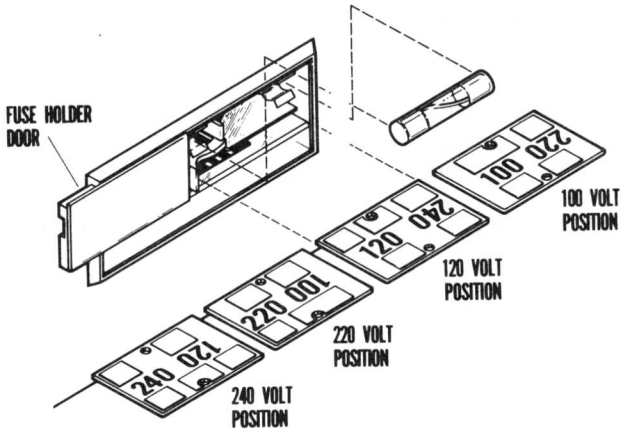
For repairs to a product damaged in shipment, contact the Intel Office in your area, or contact the Intel Service Center. (Refer to the Service and Repair Assistance section of this publication for details.)



CHECK YOUR LINE VOLTAGE SELECTION CARD AND FUSE

The line voltage selection card, located behind the plastic door next to the power cord receptacle on the rear panel, must be inserted so you can read your ac line voltage with the card in the slot. Slide the plastic fuse holder door to the left and check the placement. Also verify that the proper fuse is installed.

Voltage	Fuse
110 or 120 Volts	6.25 amps, slow blow
220 or 240 Volts	3 amps, slow blow



Power Switching Card

DEVELOPMENT SYSTEM OPERATION

GENERAL

Basic operational information required for service of the Series II Microcomputer Development System is very simple, and is explained on this page. For information on use of Monitor and ISIS-II for software development, refer to *ISIS-II User's Guide*, Intel Manual Order Number 9800306.

TURNING THE SYSTEM ON

WARNING

Do not turn the power on or off with a diskette installed in the drive. Data on the diskette may be destroyed.

To turn the system on, press the POWER switch. The indicator in the switch should light, the fans in the chassis should run, and the red RUN indicator should light. After the CRT warms up, the Monitor sign-on message and prompt should appear on the CRT as follows:

```
SERIES II MONITOR, Vx.y

.
```

x and y are numbers indicating the Monitor version and issue.

BOOTSTRAPPING AND RESETTING

The system bootstraps when power is turned on and resets when the RESET pushbutton is pressed.

Bootstrapping calls Monitor to take control of the system. Resetting also calls Monitor when there is not an ISIS-II system diskette installed in drive 0.

Diskette drive numbering is illustrated on the next page.

RESETTING WITH ISIS-II

The programs that make up ISIS-II are contained on an ISIS-II Operating System diskette.

When the Development System is reset with an ISIS-II diskette in drive 0, the ISIS-II Operating System is loaded and takes control of the system, but only the basic part of ISIS-II is loaded into the Development System's memory. The programs to perform specific functions remain on the ISIS-II diskette until you enter a command that requires their use. Then the required program or programs are loaded into the system's memory and executed. (This technique gives users the full capabilities of the operating system while it lets them have the majority of memory for the development program itself.) After the command program has completed its functions, the complete memory is again available.

General information on diskettes is provided on the following pages.

RECALLING MONITOR OR ISIS-II

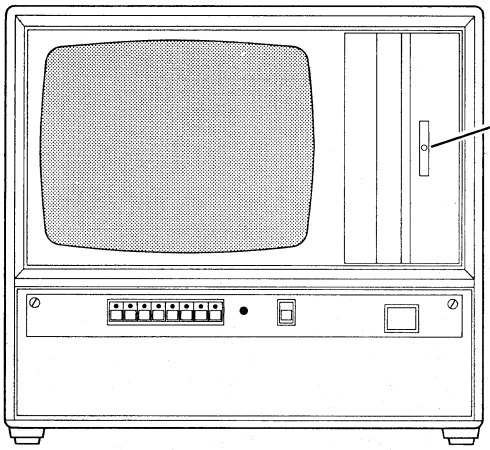
Press INTERRUPT switch 0 to recall Monitor when operating under control of ISIS-II.

Type G8 and strike the carriage return with an ISIS-II system diskette installed in drive 0 to recall ISIS-II, when operating under control of Monitor.

INTERRUPT SWITCHES

INTERRUPT switches 0 through 4 are used by Monitor and ISIS-II. INTERRUPT switches 5, 6, and 7 have no predetermined uses, but may be programmed during system development.

DISKETTE DRIVE NUMBERING

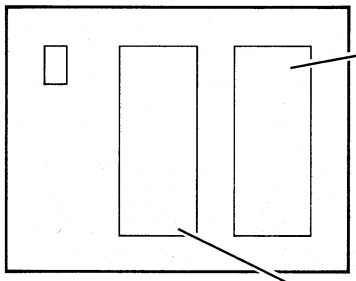


DRIVE 0 IF NO EXTERNAL DRIVES ARE USED.
DRIVE 4 IF EXTERNAL DRIVES ARE USED.

NOTE

If a single external drive unit is used, it must be connected to J8 of the Main Chassis, leaving J9 unused.

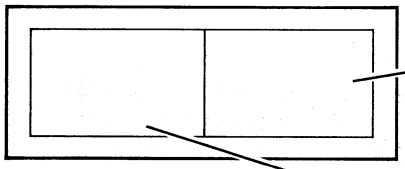
DDS/DDR/2DS/DRV DISKETTE DRIVE UNITS



DRIVE 0 IF UNIT IS CONNECTED TO MAIN CHASSIS J8.
DRIVE 2 IF UNIT IS CONNECTED TO MAIN CHASSIS J9.

DRIVE 1 IF UNIT IS CONNECTED TO MAIN CHASSIS J8.
DRIVE 3 IF UNIT IS CONNECTED TO MAIN CHASSIS J9.

LOW-PROFILE MODEL 7XX DISKETTE DRIVE UNITS



DRIVE 0 IF UNIT IS CONNECTED TO MAIN CHASSIS J8.
DRIVE 2 IF UNIT IS CONNECTED TO MAIN CHASSIS J9.

DRIVE 1 IF UNIT IS CONNECTED TO MAIN CHASSIS J8.
DRIVE 3 IF UNIT IS CONNECTED TO MAIN CHASSIS J9.

DISKETTE HANDLING

- Return the diskette to its envelope when not in use.
- Do not touch the recording surface.
- Do not smoke when handling the diskette.
- Do not clean the recording surface.
- Do not bend the diskette or deform its edges by using paper clips or other mechanical devices.
- Do not use pencil or ball point pen on the diskette label: use felt tip pen.

DISKETTE ENVIRONMENT

The environment of the diskette should meet the following criteria:

- No noticeable dirt, dust, or chemical fumes in the immediate area.
- Temperature between 50° F (10° C) and 125° F (52° C) (for storage).
- Relative humidity between 8 and 80 percent, with no condensation.
- Temperature of 85° F (30° C) maximum, for operation.
- No direct sunlight on diskette surface for prolonged periods.
- No magnetic field.

PRECAUTIONS

- Do not insert or remove a diskette unless power is applied to both the system and the diskette drive.
- Do not open the diskette drive door unless the DRIVE light is off (push INTERRUPT switch 0 or reset the system to disengage drive).
- Do not attempt loading of single-density diskettes from double-density drive or vice versa.
- Insert diskette with read/write access slot first.
- Close door of the drive after diskette insertion.
- Do not remove diskette unless the last output to console was a hyphen (ISIS-II is ready to receive a command).
- Do not attempt to write to a diskette unless it has been initialized.

DISKETTE ORGANIZATION

The floppy diskettes used with the Development System use either single-density or double-density recording techniques. The double-density recording technique packs the information at a higher density. A double-density diskette can hold twice the information that a single-density diskette can hold.

Diskettes written on a drive of one density cannot be read on a drive of the other density. Some diskettes are labeled as being single- or double-density; on a blank diskette, this only applies to the quality of the magnetic coating. You should use only double- density diskettes on double-density drives. You can use double- or single-density diskettes on single- density drives.

NOTE

If you record a diskette labeled double- density on a single-density drive, you should mark the label as being recorded at single-density. This is useful if you have both single- and double-density diskette drives.

All diskettes contain 77 tracks. Tracks on single- density diskettes each contain 26 sectors (blocks) of 128 bytes each (2022 blocks total). Tracks on double-density diskettes each contain 52 blocks of 128 bytes (4004 blocks total).

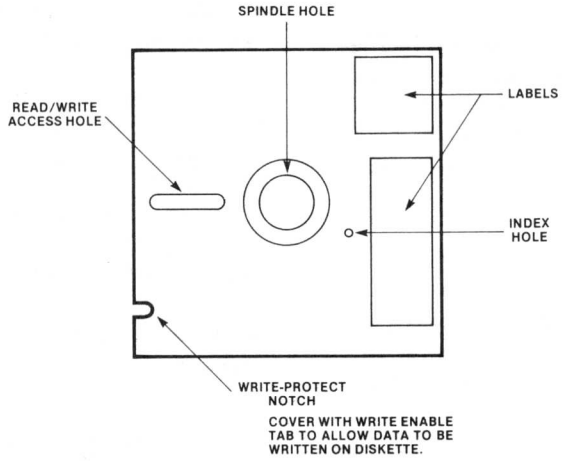
Single-density diskettes have a capacity of 250K bits; double-density diskettes have a capacity of 500K bits.

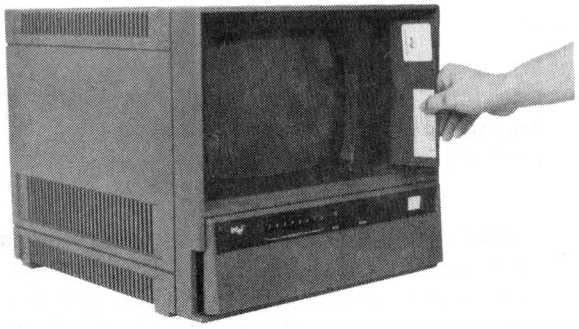
WRITE PROTECT AND WRITE ENABLE

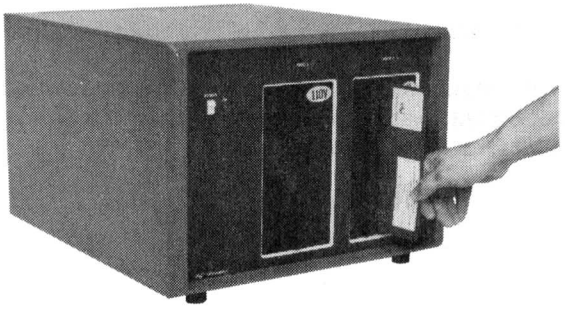
A write protect notch is cut in the diskette cover to prevent new information from accidently being written over information already stored on the diskette. The Development System will not write on the diskette as long as it detects the write protect notch.

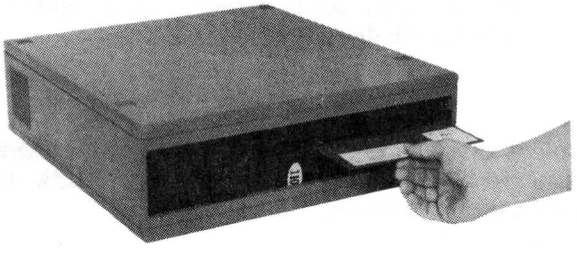
To be able to write information on a diskette, cover the write protect notch with a write enable tab. (The tabs are provided with new diskettes.)

Remove write enable tabs from diskettes you are not writing on.









WARNING

Do not turn power on or off when a diskette is in drive. Do not remove a diskette when the red light on the drive is lit. Reset the system to disengage the drive.

DISKETTE FILES AND INITIALIZATION

DISKETTE FILES

Programs and data are stored on diskettes in files. Each file on a diskette has a name. ISIS-II program files come with names already assigned; you must make up a name for each new file you create. To access a file, you don't have to know its position on the diskette, only its name.

There are four basic types of files that are used on diskettes:

- *Format files* contain information about the diskette itself. (The directory is a format file.) The system will not work with diskettes that do not have the required format files.
- *System files* contain the basic ISIS-II system programs and command programs. A diskette that contains the minimum files essential for ISIS-II operation is called a system diskette. A diskette that does not have these files is called a non-system (or data) diskette.
- *User-written* program files.
- *Data files*.

For information on management of diskette files in a Development System refer to *ISIS-II User's Guide*, Manual Order Number 9800306.

DIRECTORY FILE

All diskettes have a directory file that contains the names of all files on the diskette. To display the directory file, type DIR n I and strike CARRIAGE RETURN, where n is the drive number.

INITIALIZING A DISKETTE

A blank diskette must be initialized before it can be used in the Development System. There are two types of initialized diskettes: system diskettes and non-system diskettes.

A diskette must be initialized as a system diskette if it is to be used for Development System Functions. A system diskette contains ISIS-II software necessary for operating the system.

A diskette may be initialized as a non-system diskette if it is to be used to store a program under development or data required for a program. When a non-system diskette is initialized, it contains only the information necessary for maintaining the directory of files on the diskette, leaving more space for data.

A non-system diskette cannot operate in drive 0 in multiple-drive systems. In single-drive systems, a non-system diskette may be used in drive 0 for input or output of data or the developed programs; however, this input or output is controlled by the ISIS-II programs on the system diskette, which must also be used in drive 0.

You use the ISIS-II IDISK command to initialize a diskette.

IDISK COMMAND SYNTAX

The syntax of the IDISK command is:

```
IDISK  <device>  <label>  [S]
```

where

<device> specifies the drive containing the diskette to be initialized. Permissible identifications are F0, F1, . . ., F4.

<label> specifies how you want to identify the diskette to be initialized. The label consists of a name (1 to 6 alphanumeric characters) and an extension (1 to 3 alphanumeric characters), separated by a period. For example: NSYS.V1

[S] is a variable that indicates the initialization is a system initialization. The S is not included in the command if the diskette is to be initialized as a non-system diskette.

Colons must be typed before and after the device identifier. A space must be typed after IDISK and before the S if it is used. For example:

```
IDISK :F0:NSYS.V1 S
```

Execute the command by striking CARRIAGE RETURN.

SYSTEM OVERVIEW AND FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

From an operational viewpoint, the Intellec Series II Microcomputer Development Systems consist of a central microcomputer whose memory and I/O may be expanded to increase processing power and/or to allow the addition of peripherals or other special-purpose devices.

Internally, the Development System is a multi-processor system whose master processor integrates all other system elements.

Two microprocessors are contained within the Development System chassis and others may be added. Also, some of the more complex LSI IC's used in the system are essentially special-purpose processors whose operations are controlled by internal programs and/or commands from a true microprocessor.

In most cases, the microprocessors and the special-purpose processors operate simultaneously but remain under control of the master processor. This is not true, however, of external processors such as those in an In-Circuit Emulator (ICE). The entire system is, at times, controlled by the external ICE processor. This allows the external processor to use system resources and to have uninhibited access to the user program in the system RAM.

The primary communication path for devices added to the system is the Multibus, which is a collection of 86 lines that provide for inter-board communication and adhere to signal and pin assignment standards of the Intel Corporation.

In the Models 22X and Models 23X Development Systems, the Multibus is a multi-master bus because it allows any one of ten master processors to assume control. In doing so, each master processor has access to resources of each of the other bus masters. In the Models 22X and Models 23X Development Systems, the accessible system resources are RAM, and the CRT, keyboard, diskette, paper tape, line printer, and PROM programmer interface controllers.

FUNCTIONAL DESCRIPTION

The primary components of the Intellec Series II Microcomputer Development Systems are the IPB (Integrated Processor Board) and the IOC (I/O Controller). The IPB is the master processor of the Development System. It executes the operating system (Monitor or ISIS-II), the support programs (assembler, PL/M compiler, ICE drivers, etc.), and the user program. The IOC controls most of the system's I/O.

In dealing with most I/O devices, the IPB has very little concern with the special timing and format requirements of these devices. With the exception of the two serial I/O channels, the IPB merely directs the IOC to transfer one or more bytes to or from a specified device. The IOC is generally inactive except when responding to a command from the IPB.

Control information from the IPB to the IOC is provided in the form of single-byte commands, each of which may or may not be associated with a data byte. Commands without data bytes provide for resetting, enabling/disabling, service request acknowledgements, etc. A data byte associated with a command may be actual data to or from a device, a status return, or a control parameter required by a device controller prior to a data transfer.

The IPB and the IOC are interconnected by the backplane PWA, which is the motherboard for the card cage. The IPB plugs into two connectors on the backplane; the IOC, which is attached to the inside of the rear panel of the Development system, is connected to the backplane by cables.

The cardcage provides six Multibus card slots, one of which is used by the IPB. Addition of an Intellec Series II Expansion Chassis will provide another four Multibus card slots, for a possible total of ten. The Multibus is the standard bus structure that allows interaction between the Development System itself, additional memory boards, ICE (In-Circuit Emulator) boards, user-developed Multibus boards, and Multibus boards being developed.

An integral power supply provides power to all active modules of the Development System.

The Models 23X Development Systems include an iSBC-032 RAM Memory Board and a Flexible Diskette Subsystem consisting of two floppy diskette controller boards and one or two external drive units.

IPB

The IPB is the Development System's primary controller. The IPB also provides memory for the Development System and two serial communications channels.

Primary circuits of the IPB are: the IPB processor, timing and general control, interrupt, ROM, RAM, serial I/O, and bus priority resolution.

IPB Processor, Timing and General Control

The IPB processor, with the associated timing and general control circuits, form the basic control center for the Development System. The IPB processor is based on an 8080A-2 microprocessor, with other LSI IC's of the Intel MCS-80 family.

Interrupt Circuits

Three types of interrupts are used in the system: front-panel switch interrupts, system interrupts, and local interrupts.

Front-panel INTERRUPT switch 0 puts the system under Monitor control and INTERRUPT switch 1 puts the system under ISIS-II control. The other INTERRUPT switches are available for program development.

System interrupts 2 through 6 are available for Multibus use. System interrupt level 7 is reserved for local interrupt requests, which may be: a serial channel receive or transmit data request, a PIO request (line printer, paper tape punch, paper tape reader, or UPP), an IOC request (CRT, keyboard, or integral diskette), or a real time clock request.

IPB ROM

The IPB ROM contains firmware for bootstrapping, diagnostics, and Monitor. Capability for adding an auxiliary ROM board to the IPB is also provided.

IPB RAM

The IPB RAM provides 32K of memory for program development. In the Models 23X Development Systems, an iSBC-032 RAM Memory Board is added to the card cage to expand the system's memory to 64K. This additional 32K of memory, interfaced with the IPB through the multibus, functions as a direct extension of the 32K of memory on the IPB.

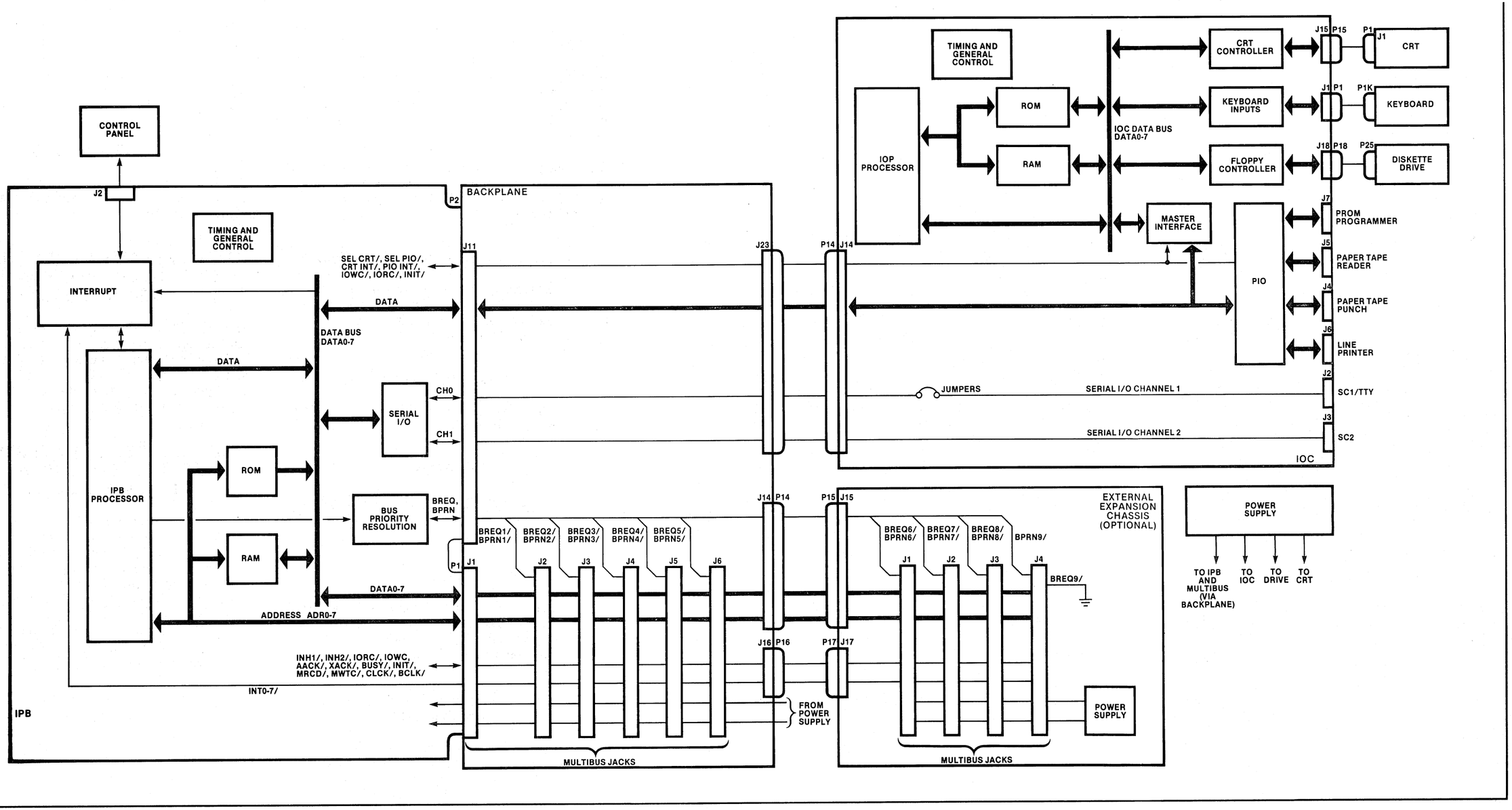
Serial I/O

The IPB provides two serial communication channels. Channel 1 is initially configured (by jumpers) as a 20-mil channel for TTY interface, but can be reconfigured as an RS232C channel. Channel 2 is configured as an RS232C interface.

Bus Priority Resolution

The IPB provides priority resolution logic for all Multibus boards used in the system. The IPB maintains the lowest bus priority. Priority is then highest for boards plugged into the highest numbered slots in the card cage (the board in J6 has higher priority than the board in J5, etc.). Boards in the Expansion Chassis (if used with the system) have higher priority than boards in the main chassis.

MICROCOMPUTER DEVELOPMENT SYSTEMS MODELS 220, 221, 222 BLOCK DIAGRAM



IOC

The IOC provides system interface with the integral diskette drive (Model 22X), the integral CRT, the integral keyboard, a universal PROM programmer (UPP), a line printer, a paper tape reader, and a paper tape punch. The IOC also provides the interface path between the IPB's serial communications channels and the peripheral devices connected to them.

The primary circuits of the IOC are: IOC processor, timing and general control, ROM, RAM, CRT controller, floppy controller, keyboard inputs, PIO, and master interface.

IOC Processor, Timing and General Control

The IOC processor, timing and general control circuits control the IOC. The IOC processor is based on the 8080A-2 microprocessor and includes other LSI IC's from the Intel MCS-80 family.

Master Interface

The master interface circuit handles exchange of data between the IOC and the IPB.

IOC ROM

The IOC ROM provides IOC initialization, diagnostic, IOC control, and I/O device control firmware.

IOC RAM

The IOC RAM stores data to facilitate I/O transfers. Most of the data storage is maintained on an as- required basis, while the data for the CRT is stored in a predetermined block of the RAM.

CRT Controller and Floppy Keyboard Inputs

The CRT controller takes data stored in the IOC RAM and converts it to inputs required by the CRT for character display. The keyboard inputs transfer data from the keyboard to the IOC data bus.

Floppy Controller

The floppy controller circuits control writing and reading to/from the flexible diskettes in the integral diskette drive of the Development System. An integral drive is not a deliverable component of the Models 23X Development Systems, although it may be added if desired.

PIO (Parallel I/O)

The PIO controls inputs and outputs to/from the UPP, the paper tape reader, the paper tape punch, and the line printer.

iSBC-032 RAM MEMORY BOARD (MODELS 23X OR EXPANSION FOR MODELS 22X)

The iSBC-032 RAM Memory Board is a complete Multibus-compatible module used to expand the Development System's memory to 64K. It is a deliverable component of the Models 23X Development Systems, and can be added directly to the Models 22X Development Systems.

FLEXIBLE DISKETTE SUBSYSTEM (MODELS 23X OR EXPANSION FOR MODELS 22X)

The flexible diskette subsystem consists of a set of two floppy diskette controller boards and one or two dual, double-density floppy diskette drive units, with appropriate interconnecting cabling. This flexible diskette subsystem provides two or four 500K byte double-density diskette drives to the system. The subsystem (with a single drive unit) is a deliverable component of the Models 23X Development Systems, and can be added directly to the Models 22X Development Systems.

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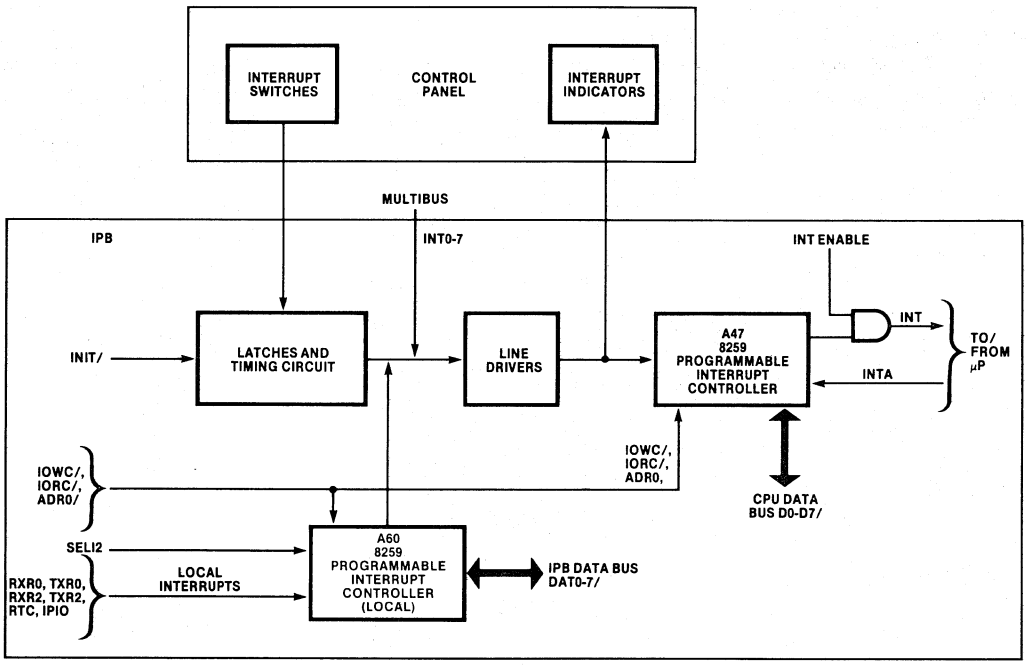

INTERRUPT SWITCHES
CONTROL PANEL
INTERRUPT INDICATORS
MULTIBUS
IPB
INT0-7
INT ENABLE
INIT/
LATCHES AND TIMING CIRCUIT
LINE DRIVERS
A47 8259 PROGRAMMABLE INTERRUPT CONTROLLER
INT
INTA
TO/ FROM μP
IOWC/, IORC/, ADR0/
IOWC/, IORC/, ADR0,
CPU DATA BUS D0-D7/
SELI2
LOCAL INTERRUPTS
RXR0, TXR0, RXR2, TXR2, RTC, IPIO
A60 8259 PROGRAMMABLE INTERRUPT CONTROLLER (LOCAL)
IPB DATA BUS DAT0-7/

The IPB contains two 2716 2K ROM IC's: A57 provides the bootstrap and diagnostic firmware and A48 provides the Monitor firmware. An additional auxiliary 20K ROM board may be mounted piggyback to the IPB, connected to the primary IPB ROM through J2 of the IPB. This auxiliary ROM, when used, provides special firmware.

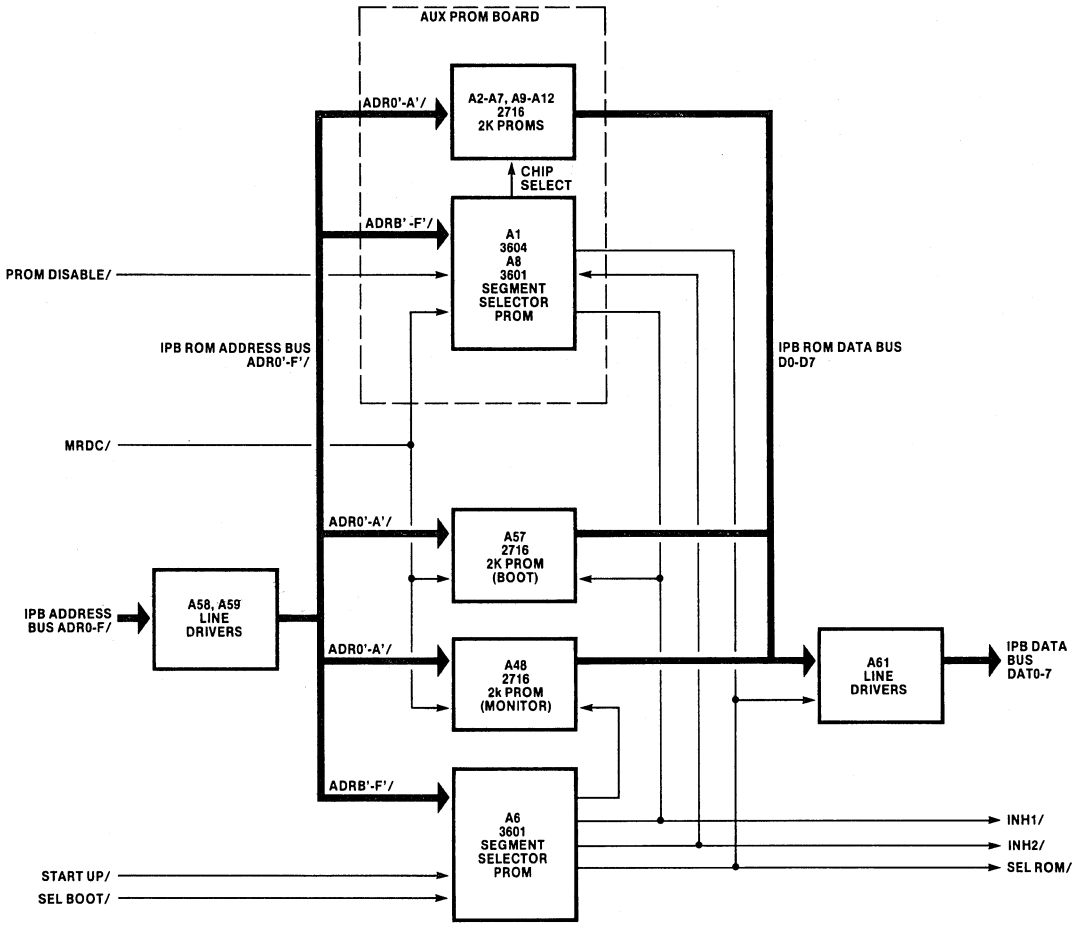
The IPB ROM is controlled by the MRDC/ signal from the bus controller or the Multibus, and three signals from 74LS259 addressable latch A73: START UP/, SELECT BOOT/, and PROM DISABLE/.

The ROM control circuits generate two inhibit signals when ROM is being used: INH1/ and INH2/. INH1/ inhibits RAM operations. When boot/diagnostic ROM A57 is selected, INH2/ is generated to allow the bootstrap or diagnostic routine to shadow other possible ROM in the same address space. Both INH1/ and INH2/ are applied to the Multibus.

The boot/diagnostic ROM A57 occupies addresses E800-EFFF. Monitor ROM A48 occupies addresses F800-FFFF.

The diagnostic is run when power is first applied to the IPB or when commanded from the keyboard by a Z$ input. The system is bootstrapped when power is applied and when the RESET switch is pressed.

Monitor is always available to all bus masters, and the address space used by Monitor (F800-FFFF) is unavailable within RAM.



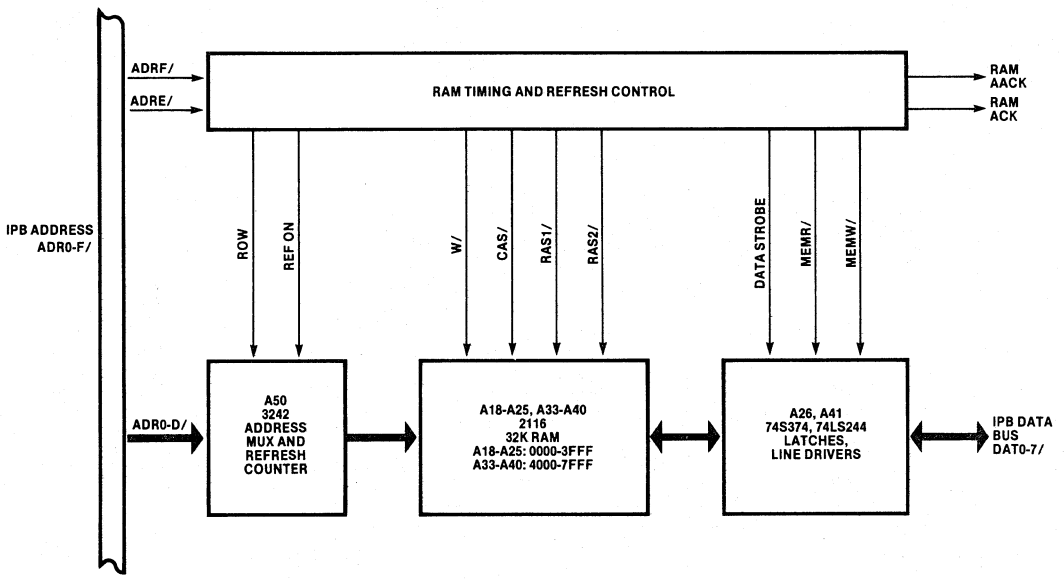
The IPB controls either 32K or 64K of RAM. Standard configurations of the Models 22X Development Systems include 32K of RAM on the IPB. Standard configurations of the Models 23X Development Systems include an additional 32K of RAM on an iSBC-032 RAM board inserted in the card cage and connected to the IPB through the Multibus. The basic Model 22X configuration can be expanded by addition of 16K or 32K of RAM with an iSBC-016 or iSBC-032 RAM boards to the card cage.

The 32K IPB RAM is implemented by 2116 or 2117 IC's A18-A25 and A33-A40. These IC's are each 16K by 1 bit RAM's. They are arranged in two blocks of 16K each. Selection of a 16K memory block is accomplished by the 2nd MSB of the address (ADRE). The remaining 14 LSB's of the address are multiplexed through Intel 3242 address multiplexer and refresh counter A50 in the form of a 7-bit row address and a 7-bit column address.

A given byte is accessed by the RAS1/ or RAS2/ (row address strobe) signals and CAS/ (column address) signal. The memory is refreshed by rows, using RAS1/ or RAS2/ without CAS/. The refresh cycle occurs once every 15 microseconds; the entire 32K RAM is refreshed within 2 milliseconds.

Read/write operations are initiated by MRDC/ (memory read command) or MWTC (memory write command) if the RAM is enabled by an inactive INH1/ and the address specifies the internal RAM block (ADRF is inactive/low).

If a read operation is specified, MEMR/ is applied to output read data latches A26, which then puts the addressed data on the IPB data bus. If a write operation is specified, a MEMW/ is applied to write data drivers A41, which drives the RAM from the data bus.



IPB SERIAL I/O CHANNELS

The IPB provides two serial I/O channels, both through connectors on the IOC.

NOTE

The rear panel of the equipment identifies the first channel as CHANNEL 1 and the second channel as CHANNEL 2. The schematics identify the first channel as channel 0 and the second channel as channel 1. This publication adopts the convention used in the schematics, and identifies the first channel as channel 0 and the second channel as channel 1.

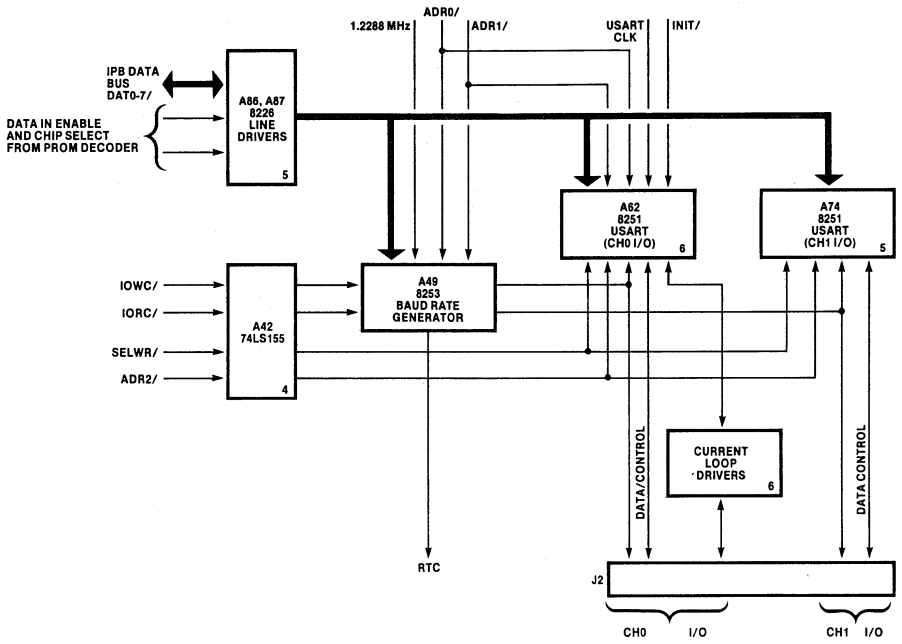
In addition to providing the connectors for the serial I/O channels, the IOC provides jumpers that permit alteration of signal routing to meet specific requirements of the serial device being used.

Although the serial channels are provided as common interfaces for the Development System, note that a teletypewriter or terminal connected to channel 0 automatically becomes the system console when the keyboard cable is disconnected from the main chassis.

The serial I/O circuits are designed around two Intel 8251 programmable USART's (Universal Synchronous/Asynchronous Receiver/Transmitter): A62 and A74. The other major component of the serial I/O is Intel 8253 Programmable Interval Timer A49, which functions as the circuit's baud rate generator.

USART A62 provides the channel 0 I/O. Commands to the programmable USART permit full duplex asynchronous communications from 110 to 9600 baud using 7 bits plus parity for teletypewriter compatibility. The commands can also establish full duplex synchronous communication from 150 to 56K baud for compatibility with RS232 or Bi-Sync terminals or modems. The associated circuitry may be jumpered to establish current loops for receive data, transmit data, and a paper tape reader control signal. The channel may use internal or external baud rate clocks as established by jumpers. Status bytes returned on command indicate the state of the present transfer and the occurrence of any transmission error. As initially configured, the interface is compatible with a current loop teletypewriter.

USART A74 provides the channel 1 I/O. This is identical with the channel 0 I/O except that no circuits are provided to establish the current loops required by teletypewriters.



The IOC processor, the control center for the IOC, executes ROM-resident device control programs in response to commands from the IPB.

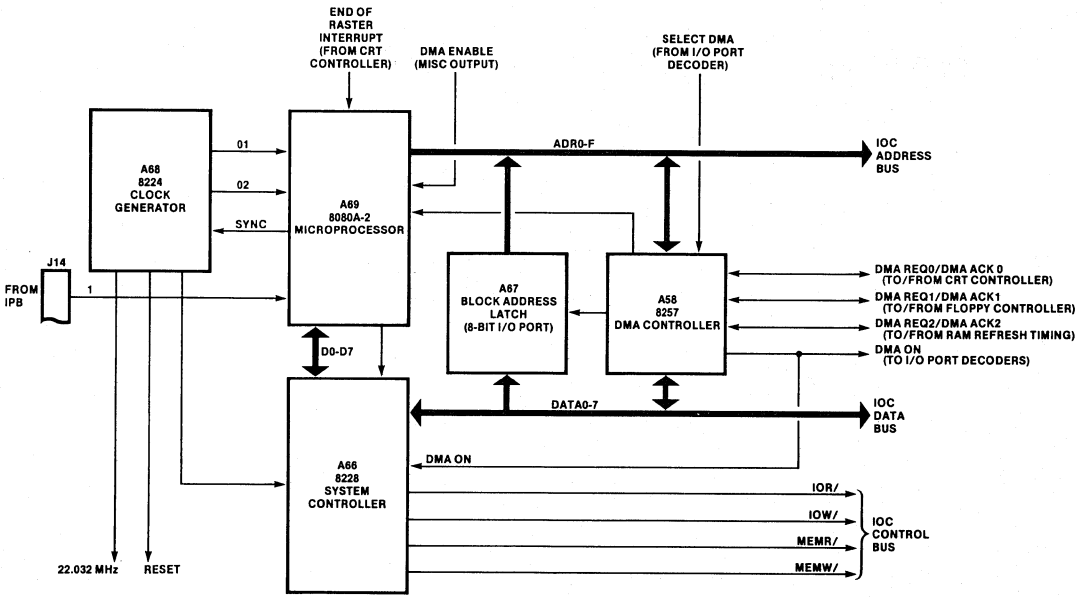
The IOC processor's major components are: 8080A-2 microprocessor A69, 8224 clock generator A68, 8228 system controller A66, and DMA controller A58.

The 8080A-2 microprocessor is the IOC's CPU.

System controller A66, except during DMA operations, decodes the data outputs of the 8080A-2 CPU during each machine cycle to determine the type of machine cycle and accordingly generates an active IOR/ (I/O read), IOW/ (I/O write), MEMR/ (memory read), or MEMW/ (memory write) control signal. The system controller then gates the CPU's data output onto the IOC data bus for transfer.

The 8257 DMA controller A58 is the only IOC chip other than the IOC processor itself that can assume full control of the IOC bus (when allowed by the processor). When the DMA controller assumes control, the address lines of the 8080A-2 processor and the data lines of both the processor and the system controller are allowed to float. The DMA controller chip then generates the RAM address and the control signals required to accomplish a data byte transfer between RAM and the requesting device. DMA is used for RAM refresh, for data transfer with the integral floppy diskette, and for CRT display generation.

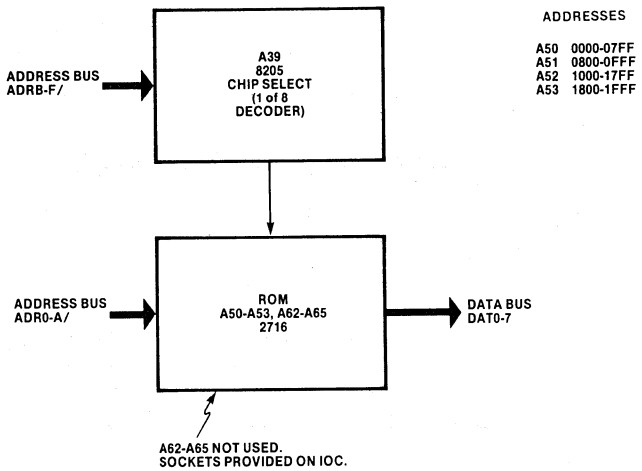
Other circuits of the IOC related to the IOC processor are timing, I/O port decoders, and miscellaneous input/output decoders.



The IOC ROM stores the firmware used for the IOC diagnostics and for control of the I/O executed by the IOC.

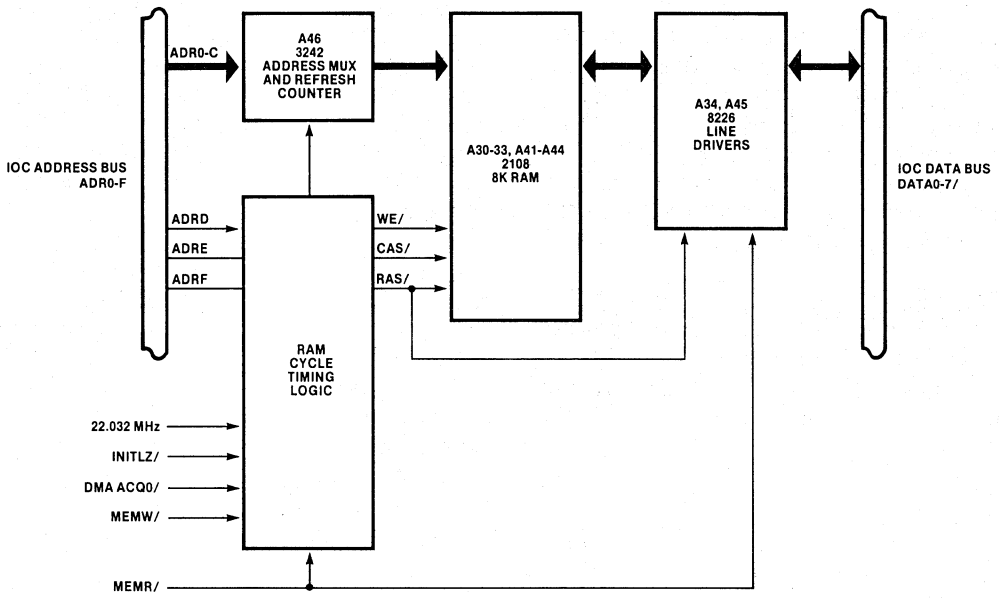
The IOC ROM consists of four 2716 2K by 8 EPROM chips (A50-A53). Space is provided on the IOC for an additional four 2716 EPROM's (A62-A65), but these are not used in the present configuration of the Development System.

In addition to the EPROM chips, the IOC ROM circuit includes an 8205 1-of-8 decoder used as a ROM chip selector. Information stored in the ROM is addressed by the IOC address bus, and gated out of the ROM by MEMR/.



The IOC RAM provides the storage required for diskette data transfer and for CRT data storage.

The IOC RAM consists of eight 8K by 1 bit dynamic RAM IC's (A30 through A33 and A41 through A44). Associated with these components are a 3242 address multiplexer and refresh counter (A46), discrete logic RAM cycle timing circuits, and two 8226 bi-directional line drivers (A34 and A45). The RAM is addressed from the IOC address bus and RAM read/write functions are controlled by MEMW/ and MEMR/. The DMAACK0 signal initiates the RAM refresh cycle.



The master interface handles all exchanges with the IPB, receiving and transmitting data, command, or status bytes in response to IPB commands.

The central element of the master interface is the data byte buffer (DBB) which are two 8-bit buffers that provide storage for one input byte and one output byte.

Control signals from the IPB are the COMMAND/DATA signal, IOWC/ (I/O write command), IORC/ (I/O read command), and SEL IOC/. These command signals are decoded by discrete control logic in the master interface to generate control signals that gate information into or out of the input or output data byte buffers.

The data byte buffers completely isolate the data lines of IOC data lines from the IPB data lines while allowing either the IOC processor or the IPB processor to access the four flags to determine when a transfer is in pending, in process, or completed.

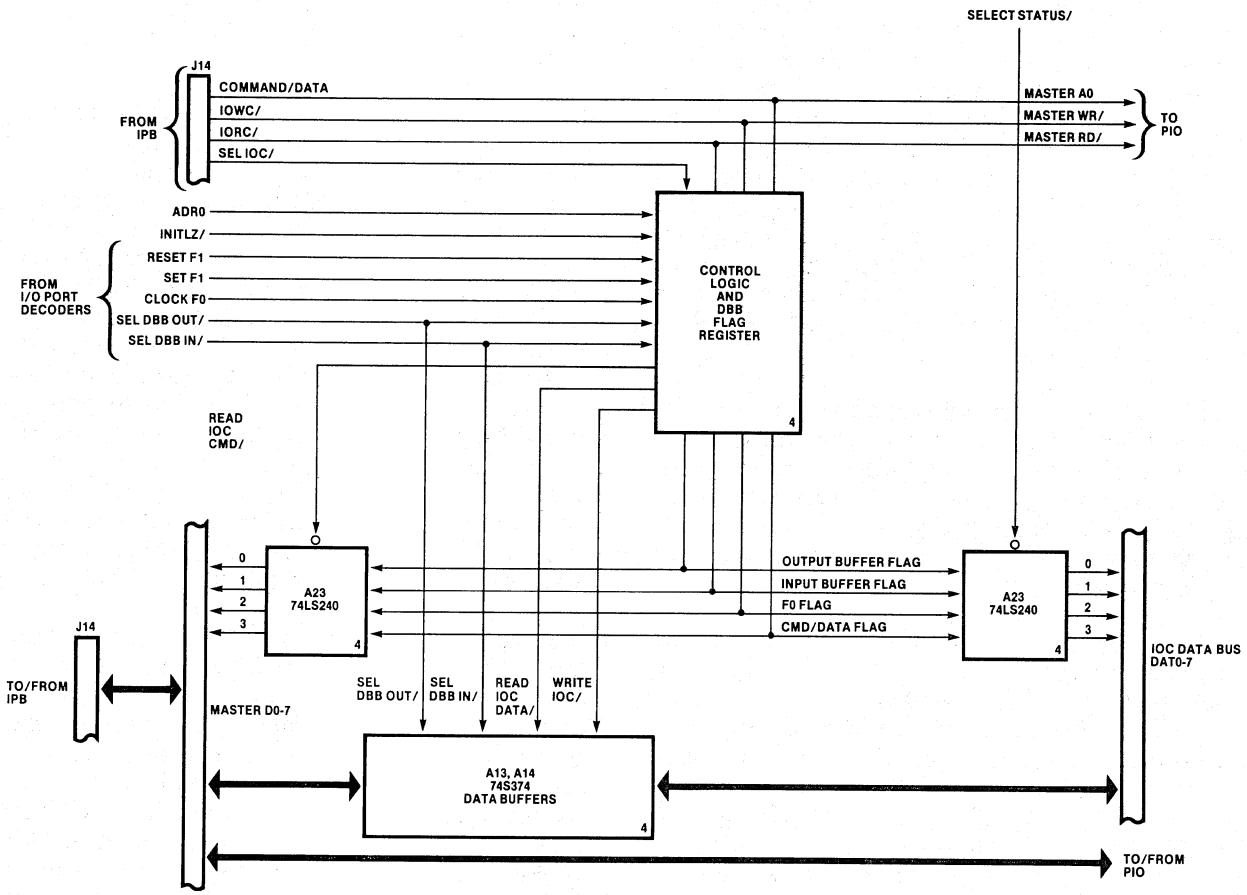
Both processors examine the flags prior to using the DBB. The IOC processor examines the flags to detect the presence of a new command and then, if necessary, polls the flags to detect the presence of data in the input buffer. Conversely, the IPB looks at the flags if the preceding command required data or status returns and then awaits an indication that the command has been completely processed.

Two of the flags, the output buffer full (OBF) flag and the input buffer full (IBF) flag directly indicate the presence of valid data in the DBB. The IBF flag is set by the IPB's master processor when a command or data byte is clocked into the input buffer (SELIOC, IOWC). This flag is reset by the IOC when the byte is accessed via port address Bx (SELECT DBBIN).

The OBF flag is set by the IOC when a status or data byte is clocked to the output buffer via port address 00 (SELECT DBBOUT). The OBF flag is reset by the IPB when the byte is accessed (SELIOC, IORC, and A0 all low). When status (i.e., the flag states) are read by the IPB, the control signals are SELIOC and IORC low and A0 high, in which case the flags are gated to the IPB data lines and neither the input buffer nor the IBF flag are affected. Flag reading by the IOC is accomplished when SELECT STATUS is low (port address Ax).

The third flag, the command/data flag (F1) is set or reset by either processor. For inputs from the IPB (SELIOC, IOWC) this flag is controlled by the state of A0. For outputs, the IOC processor software uses port addresses 3x and 4x to respectively generate SETF1 and RESETF1 to set and reset the C/D flag flip-flop. Note that while the function of A0 from the IPB remains the same for inputs and outputs (that of identifying a byte as either data or command/status) its use on inputs is solely to set the flag whereas on outputs A0 selects the byte source. The byte containing flag status is the only true status byte returned to the IPB; all other IOC status is returned within data bytes.

The fourth flag associated with the DBB is the IOC busy (F0) flag that is set by the IOC when a command is accepted and is reset by the IOC when the command is fully processed. Port address 00 and 01 respectively set and reset the flag. The IPB has no control over this flag and does not attempt a command output to the IOC when the flag is set, but waits in a monitor loop.


SELECT STATUS/
J14
FROM IPB
COMMAND/DATA
IOWC/
IORC/
SEL IOC/
MASTER A0
MASTER WR/
MASTER RD/
TO PIO
ADR0
INITLZ/
RESET F1
SET F1
CLOCK F0
SEL DBB OUT/
SEL DBB IN/
FROM I/O PORT DECODERS
CONTROL LOGIC AND DBB FLAG REGISTER
4
READ IOC CMD/
0
1
2
3
A23 74LS240
4
OUTPUT BUFFER FLAG
INPUT BUFFER FLAG
F0 FLAG
CMD/DATA FLAG
A23 74LS240
4
0
1
2
3
IOC DATA BUS DAT0-7
J14
TO/FROM IPB
MASTER D0-7
SEL DBB OUT/
SEL DBB IN/
READ IOC DATA/
WRITE IOC/
A13, A14 74S374 DATA BUFFERS
4
TO/FROM PIO

The parallel input-output subsystem (PIO) consists of all hardware elements required to establish IPB communications with four types of standard peripherals: a paper tape reader, a paper tape punch, a line printer, and a PROM programmer.

Circuit elements of the PIO include an 8041 universal peripheral interface (the PIO processor), eight 8226 bidirectional line drivers, and a single 74154 demultiplexer. The PIO processor is the only element with the "intelligence" necessary to actively participate in the control and monitoring of the four external devices; other elements either provide isolation of the processor or demultiplex its outputs. The role of the PIO processor is to accept general directives from the master (IPB) processor and convert these directives into the detailed signal sequences required by the external devices. Only one device can be serviced at a given time and no action is normally taken by the PIO processor without prior direction from the master processor.

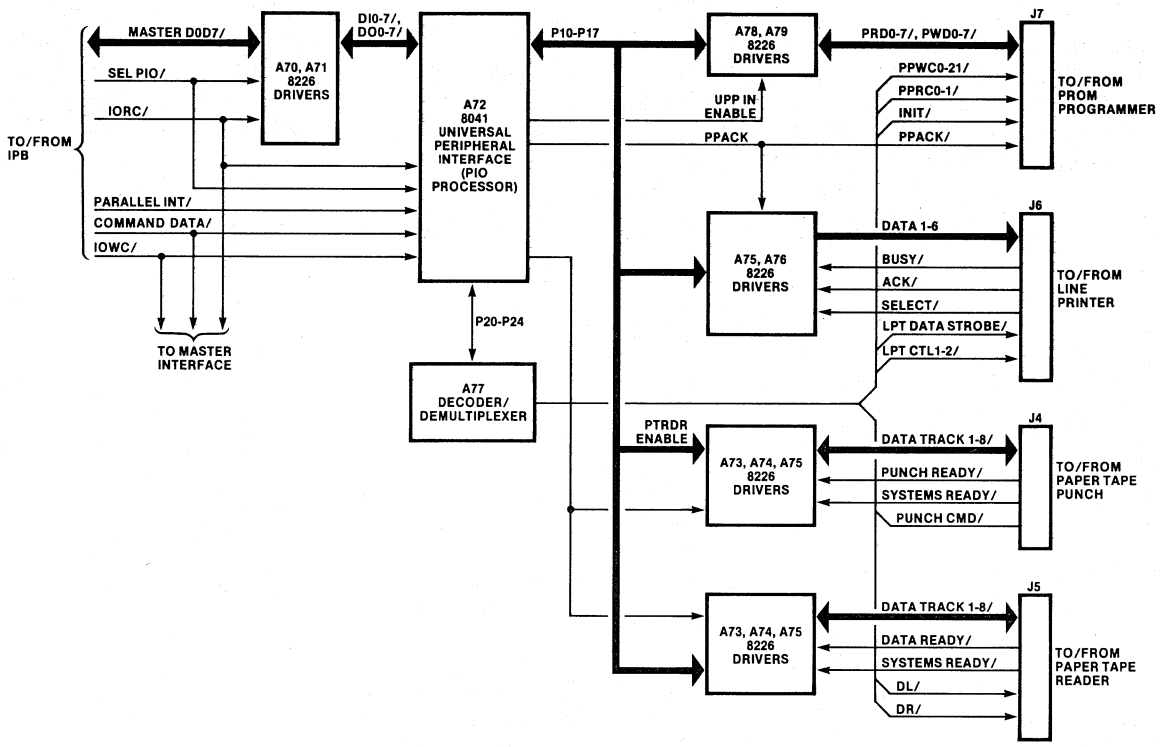
The PIO/IPB interface provides a direct communications path between the master processor and the PIO processor. All such communications are initiated by the master processor because all operations of the PIO and its subordinate peripheral devices are performed only in response to commands from the master processor.

A distinct protocol is used to accomplish interprocessor transfers. This protocol is based on requirements of a buffer within the 8041 that provides storage for data and four flags that are independently accessable to both the PIO and master processors. The flags include IBF (input buffer full), OBF (output buffer full), F0 (8041 busy), and C/D (a flag that identifies PIO input data as a command or a data byte and PIO output data as either a status or a data byte).

The flags are used by both processors to establish a master/slave relationship. The master processor reads the flags to determine when the PIO has accepted an input byte, when a data or status byte is being returned, and when a prior PIO operation has been completed. The PIO processor reads the flags to determine when a command or input data byte has been received and when a status or output byte has been accepted by the IPB. Both processors set and reset the flags as necessary to properly indicate local status.

The 8041 microprocessor is one of a family of microprocessors that provide true general-purpose processing while requiring a minimum of external circuits. Because the 8041 employs internal memory there are no pins reserved for addressing. Instead there are three byte-parallel I/O channels. The first of these (DB0-7) is very similar to the bi-directional bus of the 8080. The PIO processor uses this bus for communications with the IPB's master processor. The other two I/O channels of the 8041 are I/O ports consisting of eight lines each. The first I/O port (pins P10-17) is used by the PIO processor to transfer data to or from the four external devices. The second I/O port (pins P20-27) is used to provide signals that augment or control the information that is transferred over the first I/O port (port 1). Signals of the two ports are collectively known as the PIO bus.

The eight pins of the second I/O port (port 2) are too few for the needs of the PIO. For this reason, thirteen control signals are multiplexed by PIO software and demultiplexed by A77. These thirteen multiplexed control signals, plus four control signals that are not multiplexed, make a total of 17 control signals generated by the PIO. Of these 17 control signals, four are used within the PIO to control data routing, one is an interrupt request to the IPB, and the remaining 12 are used directly by the external peripheral devices.


MASTER D0D7/
SEL PIO/
IORC/
TO/FROM IPB
PARALLEL INT/
COMMAND DATA/
IOWC/
TO MASTER INTERFACE
A70, A71 8226 DRIVERS
DI0-7/, DO0-7/
A72 8041 UNIVERSAL PERIPHERAL INTERFACE (PIO PROCESSOR)
P20-P24
A77 DECODER/ DEMULTIPLEXER
P10-P17
A78, A79 8226 DRIVERS
PRD0-7/, PWD0-7/
J7
TO/FROM PROM PROGRAMMER
UPP IN ENABLE
PPACK
PPWC0-21/
PPRC0-1/
INIT/
PPACK/
A75, A76 8226 DRIVERS
DATA 1-6
J6
BUSY/
ACK/
SELECT/
LPT DATA STROBE/
LPT CTL1-2/
TO/FROM LINE PRINTER
PTRDR ENABLE
A73, A74, A75 8226 DRIVERS
DATA TRACK 1-8/
J4
PUNCH READY/
SYSTEMS READY/
PUNCH CMD/
TO/FROM PAPER TAPE PUNCH
A73, A74, A75 8226 DRIVERS
DATA TRACK 1-8/
J5
DATA READY/
SYSTEMS READY/
DL/
DR/
TO/FROM PAPER TAPE READER

The CRT Controller circuits are designed around an 8275 Programmable CRT Controller (A20) and an associated 2708 EPROM (A19) programmed as a character generator.

Data is displayed on the CRT in 24 rows of 80 characters each. Characters are displayed in a 5 by 7 dot pattern, with a 2-dot separation between characters. Systems using 60 Hz ac power have a 3-line separation between rows; systems using 50 Hz ac power have a 4-line separation between rows. Underlines are written two lines under the row. (A line is a row of dots).

The IOC RAM stores the full 25 rows of 80 characters (including blank characters as spaces) in a CRT table. Data is taken periodically from this CRT table, through DMA, and is transferred to CRT controller A20 one complete row at a time. The CRT controller then converts the data into the video signal (dot on or off) required by the CRT for display of that row of characters while the next row of characters are transferred to the CRT controller.

Each row of characters is divided into seven lines of dots for display. The characters comprising the row being displayed are output to a PROM character generator A19 as each line is written. The character generator then produces the pattern of dots that will form the characters on the CRT.

CRT timing circuits provide the timing signals associated with CRT control, including the HORIZONTAL DRIVE and VERTICAL DRIVE/ signals applied to the CRT to trigger the sweeps. Basic timing is provided to the CRT controller circuits by the programmable interval timer (A35).

KEYBOARD INPUTS

The IOC keyboard inputs circuits consist of gated line drivers (A80) that control data entry from the 8041 Universal Peripheral Interface 8-Bit Microcomputer IC used on the keyboard.

The line drivers are enabled to transfer a status byte or a character byte from the keyboard to the IOC by the SELECT KB/ signal from the I/O port decoders.

The SELECT KB/ signal, the STATUS/DATA signal, and the KB RESET/ signal are applied to the keyboard for its control. The SELECT KB/ signal commands the transfer, the STATUS/DATA signal indicates whether a data byte (an ASCII character) or a status byte is to be transferred, and the KB RESET/ signal indicates that the IOC has accepted the transfer.

The Floppy Controller circuits are designed around an 8271 Programmable Floppy Disk Controller (A1). TTL IC's comprise an associated data separator. Note that the Flopper Controller circuits provide only the system's interface with the integral disk drive (Models 22X or expanded Models 23X). System interface with external disk drives is provided by a 2-board floppy disk controller installed in the Multibus card slots.

During transfer of a block of data to or from the diskette, the IOC processor first initializes the DMA controller for the transfer. The IOC processor then initializes floppy disk controller A1, identifying the track and sector of the first byte in the data block to be transferred. When the floppy disk controller locates the track, the IPB and the IOC processor are effectively disconnected from the data and address lines, and the DMA and the floppy disk controller effect the data transfer, one byte at a time. After the complete block of data is transferred, the IPB resumes control of the system.

DMA channel 1 is used for diskette data transfer. I/O port decoder A59 decodes the I/O port address MSB's to generate the SELECT 8271/ signal that enables the floppy disk controller IC. The ADR0 signal identifies the data input to the controller is command or data, and ADR1 defines a reset command.

The data separator separates data from the unseparated data/clock input from the diskette drive.

CRT ADJUSTMENT

The CRT brightness and contrast controls are accessable on the rear of the main chassis. The brightness control is manually adjustable; the contrast control requires a screwdriver.

Set the brightness and contrast controls to provide the viewing characteristics you desire.

Refer to *CRT Data Displays Service Manual* (Intel Manual Order Number 9800622) for information on the following adjustments:

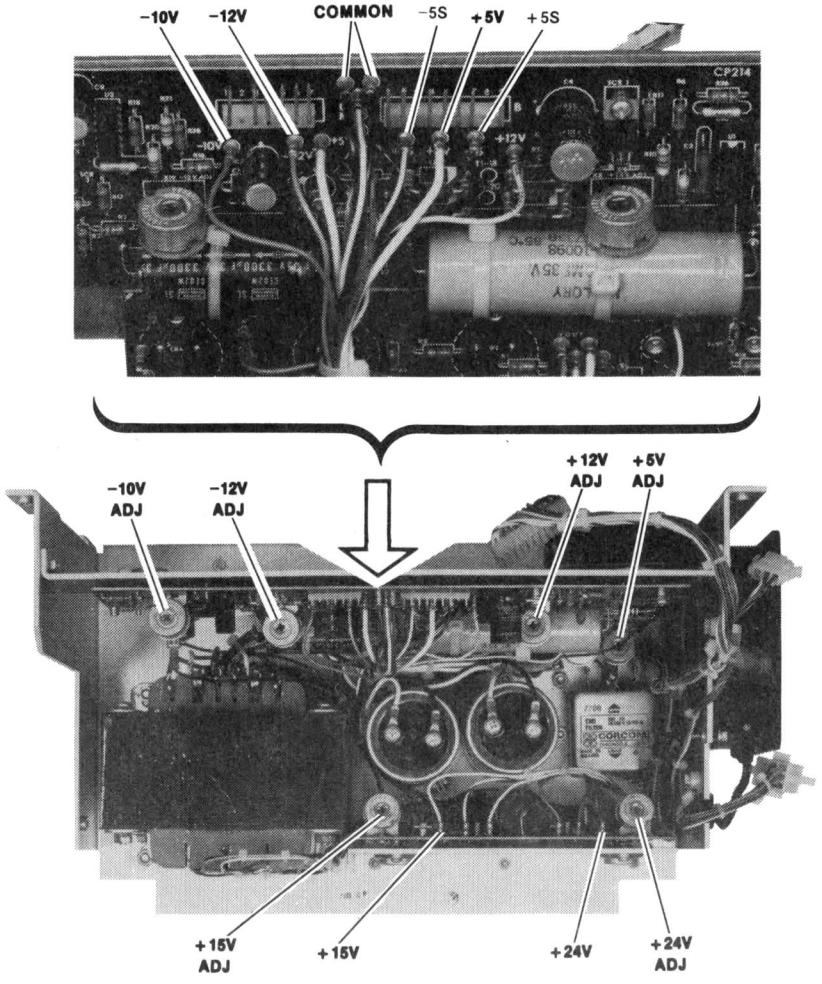
Vertical and Horizontal (frequency, linearity, size)
Focus
Centering

POWER SUPPLY ADJUSTMENT

It is very difficult to gain access to the adjusting potentiometers for the +15V and +24V outputs of the power supply. (You must slide the power supply out from under the CRT shelf, after first removing the rear panel/IOC assembly.) Fortunately, the power supply rarely needs adjustment.

Measure the voltages at power supply connector A (connected to J16 of the IOC). ADJUST THE POWER SUPPLY ONLY WHEN THE VOLTAGES ARE OUT OF TOLERANCE.

Voltage	Tolerance	Point of Measurement (PS Connector A)	Reference (PS Connector A)
−10V	±0.5V	pin 8	pin 5 or 6
−12V	±1.0V	pin 9	pin 5 or 6
+12V	±1.0V	pin 7	pin 5 or 6
+5V	±0.1V	pin 3	pin 5 or 6
+24V	±2.0V	pin 1	pin 2
+15V	±1.0V	pin 11	pin 12



GENERAL INFORMATION ON SERVICING

PROCEDURES ISOLATE TROUBLES TO A FAULTY MODULE

The information provided here is organized for isolating faults to a module (PWA, diskette drive, power supply, etc.), replacing the faulty module with a good spare module, and returning the faulty module to the Intel Service Center for component-level repair. (See page _____ for information on obtaining service and repair assistance from Intel.)

NOTE

Many faults are caused by dirty contacts on PWA's and cable connectors. Make sure the contacts are clean and free of oil.

RECOMMENDED SPARES

Intel recommends the following spare modules be stocked for effective service of the Development System:

IPB Assembly (Includes IPB and Control Panel PWA's)

IOC PWA

Diskette Drive

Keyboard PWA

The following modules are optionally spared

CRT Assembly

Power Supply

Backplane PWA

CHECKING OUT THE DEVELOPMENT SYSTEM

To verify the operation of the Development System when no fault is suspected, run the diagnostics and Confidence Test in this order:

IPB (Z$) Diagnostic

IOC (5-Beep) Diagnostic

Confidence Test

For a quick check of most major functions, run the IPB (Z$) diagnostic. This diagnostic is easy to command and provides a significant (though not totally comprehensive) test of the system's primary circuits.

RUNNING DIAGNOSTICS AND TESTS FOR TROUBLESHOOTING

When there is a fault in the system, run the tests in the following order, analyze the results and replace the most probable faulty module:

IOC (5-Beep) Diagnostic

IPB (Z$) Diagnostic

Confidence Test

More specifically, the basic sequence is as follows:

1. Run the IOC (5-Beep) diagnostic. This diagnostic tests only circuits on the IOC and thus provides a good foundation upon which to build the troubleshooting procedure. If you get an error indication from the IOC diagnostic, replace the IOC.
2. If the IOC diagnostic does not produce an error message, run the IPB (Z$) diagnostic. If that diagnostic produces an error message, replace the IPB.
3. If the IOC and IPB diagnostics produce no error message, run the Confidence Test.

SERVICE AND REPAIR ASSISTANCE

The best service for your Intel product will be provided by an Intel Customer Engineer. These trained professionals will provide prompt, efficient on-site installation, preventive maintenance, or corrective maintenance services that will keep your equipment in the best possible operating condition.

Your Intel Customer Engineer can provide the service you need through a prepaid service contract or on an hourly-charge basis. For further information, contact your local Intel office.

When it is impossible for you to use the services of an Intel Customer Engineer or when Intel service is not available in your local area, you may contact the Intel Service Center directly, at one of the following numbers:

Telephone:
From Alaska or Hawaii call—
(408) 987-8080
From locations within California call toll free—
(800) 672-3507
From all other U.S. locations call toll free—
(800) 538-8014
TWX: 910-338-0026
TELEX: 34-6372

Never return equipment to Intel for service or repair before you contact an Intel Customer Engineer or the Intel Service Center.

If return of your equipment is necessary, you will be given a Repair Authorization Number, shipping instructions, and other important information that will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment, or if the product is out of warranty, a purchase order is necessary in order for the Intel Service Center to make the repair.

When preparing the product for shipment to the Service Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. (or equivalent) and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by the Intel Service Center.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

U.S. AND CANADIAN OFFICES

ALABAMA
Intel Corp.
3322 S. Parkway, Ste. 71
Holiday Office Center
Huntsville 35802
Tel: (205) 883-2430

ARIZONA
Intel Corp.
8650 N. 35th Avenue, Suite 101
Phoenix 85021
Tel: (602) 242-7205

CALIFORNIA
Intel Corp.
7670 Opportunity Rd.
Suite 135
San Diego 92111
Tel: (714) 268-3563

Intel Corp.*
1651 East 4th Street
Suite 105
Santa Ana 92701
Tel: (714) 835-9642
TWX: 910-595-1114

Intel Corp.*
15335 Morrison
Suite 345
Sherman Oaks 91403
(213) 986-9510
TWX: 910-495-2045

Intel Corp.*
3375 Scott Blvd.
Santa Clara 95051
Tel: (408) 987-8086
TWX: 910-339-9279
TWX: 910-338-0255

COLORADO
Intel Corp.*
6000 East Evans Ave.
Bldg. 1, Suite 260
Denver 80222
Tel: (303) 758-8086
TWX: 910-931-2289

CONNECTICUT
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Peacock Alley
1 Padanaram Road, Suite 146
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TWX: 710-456-1199

FLORIDA
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1001 N.W. 62nd Street, Suite 406
Ft. Lauderdale 33309
Tel: (305) 771-0600
TWX: 510-956-9407

Intel Corp.
5151 Adanson Street, Suite 203
Orlando 32804
Tel: (305) 628-2393
TWX: 810-853-9219

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Oakbrook 60521
Tel: (312) 325-9510
TWX: 910-651-5881

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TWX: 710-862-1944

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Chelmsford 01824
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TWX: 710-343-6333

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26500 Northwestern Hwy.
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Southfield 48075
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TELEX: 2 31143

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TWX: 710-480-6238

NEW YORK
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350 Vanderbilt Motor Pkwy.
Suite 402
Hauppauge 11787
Tel: (516) 231-3300
TWX: 510-227-6236

Intel Corp.
80 Washington St.
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Tel: (914) 473-2303
TWX: 510-248-0060

Intel Corp.
474 Thurston Road
Rochester 14619
Tel: (716) 328-7340
TWX: 510-253-3841

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8312 North Main Street
Dayton 45415
Tel: (513) 890-5350
TWX: 810-450-2528

Intel Corp.*
Chagrin-Brainard Bldg. #201
28001 Chagrin Blvd.
Cleveland 44122
Tel: (216) 464-2736

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275 Commerce Dr.
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Fort Washington 19034
Tel: (215) 542-9444
TWX: 510-661-2077

TEXAS
Intel Corp.*
2925 L.B.J. Freeway
Suite 175
Dallas 75234
Tel: (214) 241-9521
TWX: 910-860-5487

Intel Corp.*
6776 S.W. Freeway
Suite 550
Houston 77074
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Intel Corp.
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Suite 233, Bell Mews
39 Highway 7, Bell Corners
Ottawa, Ontario K2H 8R2
Tel: (613) 829-9714
TELEX: 053-4419

WHAT TO DO WHEN NOTHING WORKS

If there is no RUN light on the IPB, no five beeps from the IOC diagnostic, and no cursor on the CRT . . .

Check for fuse being in place and intact.

Check for voltage select card in place inside the line filter and at the correct voltage setting.

Check the ac power harness on the power supply to be sure that connector's female pins are making complete contact with their mating pins.

Check for pinched or broken internal wiring harnesses.

Check the ac power switch.

If the system powers up but does not sign on . . .

Check to be sure the IPB is properly seated in the uppermost slot of main card cage and that the contacts are clean.

To be sure that the IOC diagnostic switch is in the line (center) position.

Check the 3M Scotch-Flex cable from the card-cage to the top of the IOC for secure connections.

Be sure the keyboard is plugged in.

Be sure the two 2716 PROMS on the IPB (A48 and A57) are correctly seated with pin polarity correctly observed.

Check for all required voltages present and with tolerances on the IOC.

Is the CRT controller chip on the IOC (A20) in place with polarity observed?

If the sign on message is scrambled . . .

Check the iSBC-032 RAM board address jumpers.

Check IPB for dirty contacts and proper seating. Check Boot and MONITOR PROM A48 and A57 for proper seating.

If system signs on but keyboard entry is not possible . . .

Be sure the control key labeled TPWR is not locked in down position.

If the system will not boot from a system diskette . . .

Note that a system with an integral diskette drive will not boot ISIS-II from the integral drive when diskette controller boards are plugged into the Multibus.

For systems with an external drive chassis: Is the cable connected properly to the interface board?

Is the diskette of the correct software version and the correct density for the drive?

If a program being written in the text editor will not assemble or if the program errors as the system warms up . . .

Check the location of the external controller board. The interface board should be in the lowest slot and the channel board in the slot directly above the interface board.

The RAM on IPB may be bad, ISIS resides in the first 12K of RAM. Run the IPB (Z$) diagnostic.

Check fans for operation, and be sure air flow is not restricted.

GENERAL DESCRIPTION OF DIAGNOSTICS AND CONFIDENCE TEST

There are four diagnostics and a Confidence Test for the Development System. Although each will detect errors in the system, all must be run to provide complete verification of system performance.

POWER-UP/RESET DIAGNOSTIC

The power-up/reset diagnostic runs automatically when power is first applied to the system or when the system is reset. This diagnostic verifies operation of the basic IPB and IOC circuits, but is not comprehensive. If there is any question about the system's operation, perform the IPB (Z$) and IOC diagnostics.

The system gives no indication that it has passed the power-up/reset diagnostic. If failures are detected, an error message or messages will be displayed on the CRT.

IPB (Z$) DIAGNOSTIC

The IPB (Z$) diagnostic tests circuits on both the IPB and the IOC. It is more comprehensive than the power-up/reset diagnostic and is easily called, but does not test all system functions. Also, since it tests circuits on both of the major modules of the system (the IPB and the IOC), it cannot be used—by itself—to isolate faults to one of these two modules.

Use the IPB diagnostic in conjunction with the IOC diagnostic and the Confidence Test.

IOC (5-BEEP) DIAGNOSTIC

The IOC diagnostic tests circuits that (except for the reset) are exclusively located on the IOC. It therefore is a good test to use to isolate troubles to either the IOC or the IPB. The IOC diagnostic also provides an audible indication of the test and can therefore be run as a starting point when the CRT is not providing correct indications.

In addition to testing the IOC, the IOC diagnostic also tests the integral diskette drive, the keyboard and the CRT. The diagnostic requires placement of the LOCAL-LINE-DIAGNOSTIC switch on the IOC (rear panel) in the DIAGNOSTIC position.

LOCAL KEYBOARD/CRT TEST

The local keyboard/CRT test is a simple test of the circuits used for keyboard input and character display. Although it is limited in function, it is very valuable for isolation of faults to the keyboard or IOC. The test requires placement of the LOCAL-LINE-DIAGNOSTIC switch on the IOC (rear panel) to the LOCAL position.

CONFIDENCE TEST

The Confidence Test includes the peripherals connected externally to the system, and thus tests the complete system-peripheral loop. (The IPB and IOC diagnostics tests only the reaction of peripheral control components to commands, and not the complete loop.) The Confidence Test is therefore a comprehensive test that should be run after the IPB and IOC diagnostics have verified correct operation of the basic circuits. Note, however, that the Confidence Test will yield error messages when a problem is in the peripheral itself. Make sure the peripheral works before troubleshooting the Development System.

General Information and Instructions:

1. This diagnostic requires a write-enabled scratch diskette when run on a Model 22X Development System. Do not insert diskette into drive until the procedure indicates.
2. After completion of the Basic IOC Components Test (Beep Test) and Keyboard Cable Test, the Disk (D), General (G), and Keyboard (K) tests may be run in any sequence.
3. The Disk (D) Test runs only on the integral, single-density disk drive of the Models 22X or expanded Models 23X, not on the external double-density drives.
4. The menu of available tests is:

   D—DISK
   G—GENERAL
   K—KEYBOARD
5. At end of test sequence, release TPWR key and return 3-position slide switch on rear panel (IOC) to LINE (center) position.

Basic IOC Components Test (5-Beep Test)

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
1	On rear panel (IOC) place 3-position slide switch in DIAGNOSTIC (up) position. Press RESET. The system runs the 5-Beep Test automatically when RESET is pressed. If the test runs correctly you will hear five beeps spaced: two beeps, slight pause, three beeps. Press RESET and listen carefully for the beeps. After the 5th beep, the CRT will display the sign-on message INTELLEC SERIES II IOC DIAGNOSTIC Vx.y and TYPE CNTL-@, RUBOUT, "U" AND "*" REQUESTED RECEIVED where x and y are numbers indicating the diagnostic's version and release.	If you hear no beeps, turn power off then on again, listening carefully for the beeps. If there are still no beeps, the problem is most probably the power supply or the IOC. **If you hear fewer than five beeps or if you hear no beeps but the IPB reset logic checks OK, the problem is most likely on the IOC.** If you hear all five beeps but the sign-on message is not displayed, check CRT brightness and contrast controls. If adjusting these controls does not produce display, **a. CRT is faulty** **b. IOC CRT Controller circuit is faulty**

KEYBOARD CABLE TEST

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
2	Type: CNTL-@ (CNTL and @ keys simultaneously) RUBOUT U * System displays: REQUESTED RECEIVED @ 00000000 @ 00000000 R0 01111111 R0 01111111 U 01010101 U 01010101 * 00101010 * 00101010 D — DISK G — GENERAL K — KEYBOARD	REQUESTED and RECEIVED data should match. If they do not match: a. You typed the wrong character b. The IOC keyboard circuit is faulty c. The keyboard is faulty d. The keyboard cable is faulty If the REQUESTED and RECEIVED data do not match, the CRT will display ERROR and indicate faulty bits. For example: REQUESTED RECEIVED @ 00000000 @ 00000000 R0 01010101 w 01110111 ERROR 00001000 U 01010101 U 01010101 * 00101010 " 00100010 ERROR 00001000 A "1" bit in the byte displayed following ERROR indicates a faulty bit. The example given could be caused by an open KB DATA 3/ wire in the keyboard cable. If you do not have a spare keyboard available for substitution, you can further isolate the trouble by examining the KB DATA signals and keyboard control signals at the IOC/keyboard on the IOC.

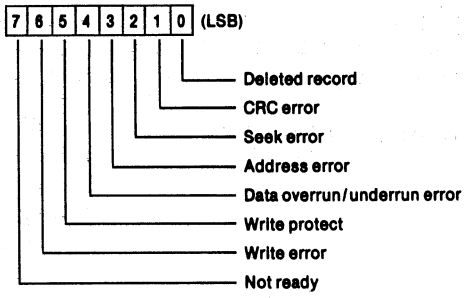
KEYBOARD (K) TEST
(Enter from menu)

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
3	Type: K System displays: Full screen of characters including both capital letters and small letters.	Single bad character indicates faulty keyboard. Multiple bad characters indicates faulty keyboard or IOC.
4	Type: Each keyboard character System displays: Full screen of each typed character Letters are displayed as capitals unless TPWR key is depressed. Letters follow SHIFT key when TPWR key is released. RUBOUT is displayed as R0. Pressing CNTL (control) and any letter key or the @ key displays ↑x, where "x" is other key. Characters are echoed on CRT until you press the space bar or the ESC key. Sign-on message and menu of tests available is then displayed.	Same as above.
5	Release TPWR key. Press space bar.	

GENERAL (G) TEST
(Enter from menu)

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
6	Type: G System runs test, then displays: TEST PASSED or TEST FAILED and menu.	TEST FAILED indicates faulty IOC.

INTEGRAL DISK (D) TEST
(Enter from menu; run only on integral single-density drive)

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
7	**Type:** **D** **System prompts:** **DISK TEST** **Insert SCRATCH disk and type "#".** If system does not have an integral disk drive (as in the basic Model 23X), the disk test automatically terminates after you type "D" and displays "NO DRIVE."	
8	**Insert scratch diskette and type "#". Be sure diskette is write enabled.** **System runs test. Approximate time 40 seconds. Indicator on drive lights during test; you can hear the drive operating during the test.** If the system passes the test, the test menu is displayed. If there is a failure, READ ERROR or ERROR nnnnnnnn will be displayed.	**Failure of disk drive or floppy controller circuits on IPB indicated by** **a. Drive failing to operate (drive's "run" indicator not lit and no aural indication of operation)** **b. READ ERROR** **c. ERROR nnnnnnnn** **Fields of result byte nnnnnnnn are**  **You can isolate the fault to the IOC or the disk drive by examining signals at IOC/disk drive interface.**

STEP	PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
1	On rear panel (IOC) place 3-position slide switch in LOCAL (down) position and press RESET switch. System displays: Flashing cursor at home position.	If no cursor appears, turn system off, then on again. If there is still no cursor, run the IOC diagnostic.
2	Type on the keyboard. The CRT will display all characters typed. Make sure characters are displayed properly. Letters are displayed as capitals unless TPWR (typewriter) key on keyboard is depressed. Letters follow SHIFT key when TPWR key is released.	Incorrect display of characters on CRT indicates keyboard or keyboard cable failure. Run IOC Diagnostic to further identify problems.
3	Release TPWR key and return 3-position slide switch on rear panel (IOC) to LINE (center) position.	

IPB (Z$) DIAGNOSTIC

GENERAL INFORMATION

The IPB (Z$) diagnostic runs automatically, without any operator intervention, and tests the following:

1. Checksums
   a. Boot ROM Checksums (IPB)
   b. IOC ROM Checksums (IPB)
   c. Monitor ROM Checksums (IPB)
   d. PIO Checksums (IOC)
2. IOC
   a. IOC Interrupts. Checks interrupt circuits on IPB as well as interrupt from IOC.
   b. IOC RAM
3. PIO (Part of IOC)
   a. PIO Interrupts. Checks interrupt circuits on IPB as well as interrupt from PIO section of IOC.
   b. PIO RAM
4. RAM (IPB and add-on RAM boards)

PROCEDURE

Remove diskettes from all drives in the system.

Turn power on and reset the system. You should see the Monitor sign-on message on the CRT:

```
SERIES II MONITOR, Vx.y
```

where x and y indicate the version and release of Monitor.

Initiate the IPB (Z$) diagnostic by typing

```
Z$ (cr)
```

If your system has 64K of RAM memory and no errors are detected, the CRT will display:

```
.Z$
INTELLEC SERIES II DIAGNOSTIC Vx.y
  TESTING CHECKSUMS—PASSED
  TESTING IOC—PASSED
  TESTING PIO—PASSED
  TESTING RAM—PASSED
END DIAGNOSTIC
```

If your configuration has less than 64K of RAM memory, the memory test will produce an error message indicating a "failure" of the 32-48K memory block and/or 48-62K memory block, as follows:

```
TESTING RAM
    FAILURE—RAM BANK 32-48K
    FAILURE—RAM BANK 48-62K
```

This does not indicate a real failure; it indicates only a recognition of the system configuration.

If the diagnostic detects errors, error messages will be displayed under the TESTING CHECKSUMS, TESTING IOC, TESTING PIO, or TESTING RAM messages as appropriate. The error messages and recovery are as shown on the facing page.

IPB (Z$) DIAGNOSTIC ERROR MESSAGES

Error Messages	Description and Recovery
FAILURE—BOOT CHECKSUM	Replace IPB.
FAILURE—IOC CHECKSUM	Replace IPB.
FAILURE—IOC INTERRUPTS	Most probable trouble on IPB, but may be IOC. Replace IPB first, then IOC if necessary.
FAILURE—IOC NOT RESPONDING	Replace IOC.
FAILURE—IOC RAM	Replace IOC.
FAILURE—MONITOR CHECKSUM	Replace IPB.
FAILURE—PIO CHECKSUM	Replace IOC.
FAILURE—PIO INTERRUPTS	Most probable trouble on IPB, but may be IOC. Replace IPB first, then IOC if necessary.
FAILURE—PIO NOT RESPONDING	Replace IOC.
FAILURE—PIO RAM	Replace IOC.
FAILURE—RAM BANK mmK-nnK	Replace IPB if error shows RAM bank 0K-32K. Replace appropriate RAM board if other errors are indicated.

NOTE

Before replacing modules as indicated, run the IOC diagnostic to provide a complete set of test results. Replace the module indicated as a result of all tests available.

CONFIDENCE TEST

GENERAL INFORMATION

The confidence tests run consecutively, with no operator interaction required to initiate the different tests. Operator interaction is required for the completion of some tests, however, and the test sequence stops if an error is detected during the processor test, which is the first test run. The test program prompts for the required operator interaction.

SIMPLIFIED PROCEDURE

The procedure provided here provides detailed information on how to run the confidence test. You can achieve the same results simply by inserting the Confidence Test diskette into drive 0, resetting the system, and following the test's prompts. Check the detailed procedure for appropriate responses to error messages.

ABORTING A TEST

To abort a confidence test, press CONTROL and C keys simultaneously. If any other key is pressed during the test, the CRT will display the message TEST RUNNING, STRIKE CONTROL/C TO ABORT.

RERUNNING THE TEST

After the confidence test has been completed, you can re-run it by typing G and carriage return.

EQUIPMENT AND MATERIALS REQUIRED

Confidence Test Diskette
Scratch Diskettes (1 for each drive)
*TTY with Punch and Reader
*Line Printer
*High Speed Paper Tape Punch
*High Speed Paper Tape Reader

*Required for complete test. Are necessary only if used with system being tested.

LIST OF TESTS

Processor Test	Executes and verifies IPB 8080 instructions.
Memory Test	Tests all RAM except that used by Confidence Test.
CRT Test	Displays full character set on CRT and echos keyboard inputs.
TTY Test	Tests TTY keyboard, printer, punch, and reader.
Diskette Test	Checks all drives in system.
Line Printer Test	Checks high- and low-speed printers.
High Speed Punch Test	Checks high speed punch.
High Speed Reader Test	Checks high speed reader.

WARNING

Turn system power off before taking boards out of or putting boards into the system.

CONFIDENCE TEST PROCEDURE

LOADING THE TEST PROGRAM

PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
Insert the Confidence Test diskette in drive 0 and reset the system. When the test program is stored in the system's memory, the CRT will display the sign-on message INTELLEC SERIES II CONFIDENCE TEST, Vx.y where x and y indicate the version and release of the test.	

PROCESSOR TEST

PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
The processor test runs immediately after the test program is loaded. The test runs so fast you will not be able to observe that it is running. If the test detects no errors, you will see PROCESSOR TEST PASSED on the CRT.	If an error is detected during the processor test, the test will stop and the CRT will display PROCESSOR TEST nnnn where nnnn is the address at which the error was detected and the test halted. If you get this error message, replace the IPB. You can verify the results of this test by performing the IPB (Z$) diagnostic.

MEMORY TEST

PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
If the processor test passes, MEMORY TEST (1 MIN) TESTING RAM xxxx-yyyy will appear on the CRT the same time as PROCESSOR TEST PASSED. The xxxx-yyyy indicates the beginning and ending hex addresses of the RAM being tested. All IPB RAM and all additional RAM is tested except that being used by the confidence test itself. If no errors are detected during the memory test, the CRT adds PASSED to the display and the program goes to the next test.	If an error is detected during the memory test, the CRT will add #FAILED# after the RAM addresses. If you get this error message, remove all RAM external to the IPB and repeat the test. If the memory test fails with all RAM except the IPB RAM removed from the system, replace the IPB. If the memory test fails only when RAM external to the IPB is installed, replace the external RAM boards. You can verify results of this test by performing the IPB (Z$) test.

CRT TEST

PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
The CRT test runs after the memory test, with the CRT displaying CRT TEST and two identical lines of ASCII characters, then ECHO CHARACTERS FROM KEYBOARD UNTIL ESC KEY ENTERED Type on the keyboard. The CRT should display all characters typed except the "}" character. Typing "}" aborts the test. Press ESC (escape) key to end test. If no character is typed for 10 seconds, the CRT displays TIME OUT, NO KEYBOARD INPUT FOR 10 SECONDS and the program proceeds to the next test.	Incorrect characters in the ASCII set indicates a faulty IOC. Failure of the CRT to echo keyboard inputs indicates a faulty IOC or keyboard. Replace the IOC or keyboard. You can verify results of the test by performing the IOC diagnostic.

TTY TEST

PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
The TTY test runs after the CRT test, with the CRT displaying TTY TEST If a TTY is not connected to the system, the CRT displays TTY TEST #TTY NOT READY# and the program continues to the next test. If a TTY is connected to the system it should print two lines of ASCII characters, then the message ECHO CHARACTERS FROM TTY KEYBOARD UNTIL ESC KEY ENTERED Type on the TTY keyboard. The TTY will type all characters typed. Press ESC (escape) key to end test. If no character is typed on the TTY for 10 seconds, the CRT displays the message TIME OUT, NO KEYBOARD INPUT FOR 10 SECONDS The CRT then displays TURN ON TTY PUNCH STRIKE CONSOLE ESC KEY (1 MIN) If the punch/reader is not turned on and the ESC key not pressed in 1 minute, the CRT displays TIME OUT, NO KEYBOARD INPUT FOR 1 MINUTE and the program proceeds to the diskette test. If you press the ESC key within the allotted 1 minute, the punch punches a null header, two lines of the ASCII character set, and a null trailer. It then displays the message TURN OFF TTY PUNCH LOAD PUNCHED TAPE IN TTY READER STRIKE CONSOLE ESC KEY Load the tape that was just punched and press ESC. The system will read the tape. If the ESC key is not pressed within the allotted 1 minute, the CRT displays TIME OUT, NO KEYBOARD INPUT FOR 1 MINUTE and the program proceeds to the next test.	**NOTE** The serial channel 1 interface at J2, to which the TTY must be connected, must be configured properly and the baud rate set properly for the TTY to operate correctly. Also, a Model ASR-35 Teletypewriter must be modified appropriately to work with the system. Refer to Appendix A for details. Errors in the typed characters indicate a fault on the IPB or the serial channel connections on the IOC. If the system detects errors when the tape is read, the CRT displays #TTY DATA ERRORS# If errors are detected, replace the IPB.

CONFIDENCE TEST PROCEDURE (Continued)

DISKETTE TEST

PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
The diskette test runs after the TTY test, with the CRT displaying DISKETTE TEST WARNING: DISKETTE FILES ON DRIVES WILL BE DESTROYED LOAD WRITE ENABLED SCRATCH DISKETTE INTO ANY DRIVE TO BE TESTED STRIKE CONSOLE ESC KEY (1 MIN) **WARNING** Remove the Confidence Test diskette from drive 0 to protect it. If it is not write protected, it's contents will be destroyed during this test. If the ESC key is not pressed within 1 minute, the CRT displays TIME OUT, NO KEYBOARD INPUT FOR 1 MINUTE DISKETTE DRIVES NOT TESTED and the system continues to the line printer test. To test the drives, load write enabled scratch diskettes in all drives in the system, then press ESC. The system will test each drive, starting with drive 0, displaying TESTING DRIVE #n where n is the drive number. **WARNING** The start of the test is delayed 3 seconds after the ESC key is pressed. This is your last change to abort the test (CONTROL/C) if you did not load a scratch diskette. If the test is successful, the CRT displays PASSED, as TESTING DRIVE #n PASSED If a diskette is not inserted in a drive, the CRT will add the error message #DRIVE NOT READY# or #SEEK ERROR#	Diskette test error codes are: #NO DISKETTE CONTROLLER PRESENT# #UNEXPECTED I/O COMPLETE# #DRIVE STATUS CHANGE# #TIME OUT# #DRIVE NOT READY# #WRITE ERROR# #WRITE PROTECTED# #DATA OVERRUN# #DATA/ADDRESS MARK ERROR# #ADDRESS MARK ERROR# #ID CRC ERROR# #SYNC ERROR# #ADDRESS ERROR# #SEEK ERROR# #DATA CRC ERROR# #DELETED RECORD ERROR# If an error code is displayed for an integral drive, replace the IOC or the drive. If an error code is displayed for an external drive, replace the flexible diskette controller boards or the drive. The drives can be isolated by reidentifying them by changing the drive identification jumpers. (Refer to the appropriate Flexible Diskette Subsystem service publication for details.)

LINE PRINTER TEST

PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
The line printer test runs after the diskette test, with the CRT displaying LINE PRINTER TEST If no line printer is connected or if it is turned off, the CRT adds #LINE PRINTER NOT READY# TEST WAITING 10 SECONDS FOR DEVICE "READY" This gives you 10 seconds to make the printer ready. If you make the printer ready within the 10 seconds allotted or if it is ready when the test starts, the CRT will display NOW PRINTING ASCII CHARACTER SET and 20 lines of the ASCII character set will be printed by the line printer. If you do not make the printer ready in the 10 seconds allotted, the test program continues to the next test.	If there are errors in the printout, replace the IOC.

CONFIDENCE TEST PROCEDURE (Continued)

HIGH SPEED READER TEST

PROCEDURE AND NORMAL SYSTEM RESPONSE	ERROR MESSAGES AND RECOVERY
The high speed reader test runs after the high speed punch test, with the CRT displaying HIGH SPEED READER TEST If no high speed reader is connected to the system or if it is turned off, the CRT will add #HIGH SPEED READER NOT READY# TEST WAITING 10 SECONDS FOR DEVICE "READY" You have 10 seconds to make the reader ready. If you make the reader ready in the allotted 10 seconds or if it is ready when the test started, the CRT will display LOAD HIGH SPEED READER WITH TAPE FROM TTY OR HIGH SPEED PUNCH TEST STRIKE ANY CONSOLE KEY (1 MIN) Do what it says. The reader will read the tape when you strike the key. If you do not make the reader ready in the allotted 10 seconds, the test program will terminate with the message END OF CONFIDENCE TEST	If the system detects an error, the CRT will display #HIGH SPEED READER DATA ERROR# and the test program will terminate. Replace the IOC if errors are detected.

HIGH SPEED PUNCH TEST

PROCEDURE AND NORMAL SYSTEM RESPONSES	ERROR MESSAGES AND RECOVERY
The high speed punch test runs after the line printer test, with the CRT displaying HIGH SPEED PUNCH TEST If no high speed punch is connected to the system or if it is turned off, the CRT will add #HIGH SPEED PUNCH NOT READY# TEST WAITING 10 SECONDS FOR DEVICE "READY" You have 10 seconds to make the device ready. If you make the punch ready within the 10 seconds allotted or the punch was ready when the test started, the CRT will display NOW PUNCHING ASCII CHARACTER SET and the test program will punch a null header, two lines of the ASCII character set, and a null trailer. If you do not make the punch ready in the allotted 10 seconds, the program proceeds to the next test.	Check the punched tape visually or with the high speed reader test. Replace the IOC if the tape has errors.

REMOVAL AND REPLACEMENT PROCEDURES

GENERAL INFORMATION

1. Read the complete procedure before doing it.
2. All screws should have flat washers and lock washers.
3. When removing something, keep the screws and washers so you can replace it properly.

WARNING

There are dangerous voltages in the Development System. Remove all power when removing and replacing components. Use caution when working on the equipment with power on and the cover off.

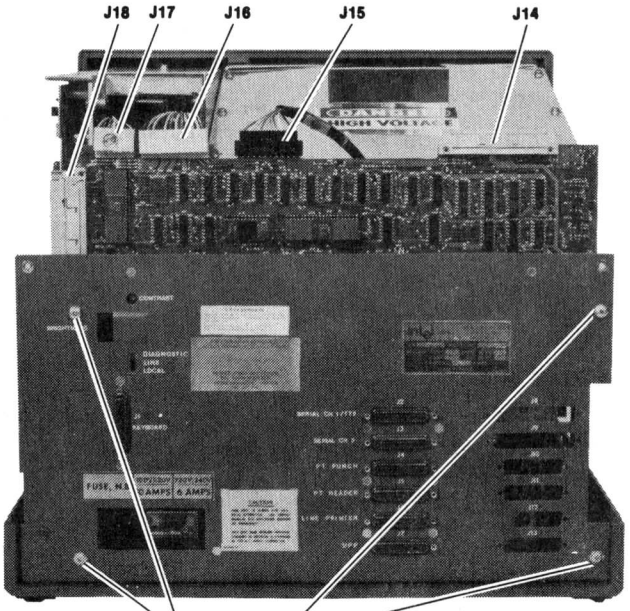
REMOVAL AND REPLACEMENT PROCEDURES (CONTINUED)

REMOVING THE IOC

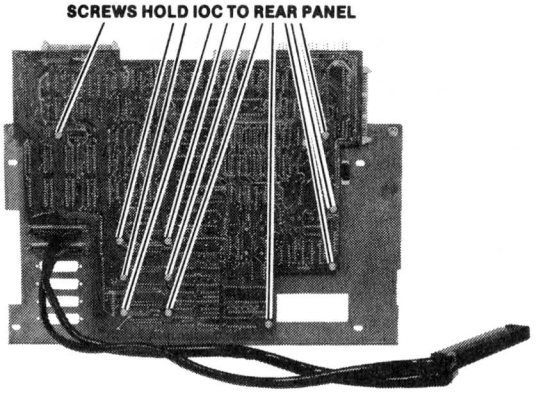
1. Disconnect the ac power cord from the Development System.
2. Remove the top cover from the chassis.
3. Remove the cables from J16, J15, and J14 of the IOC. Use 3M Scotchflex Tool No. 3438 or equivalent to remove the ribbon cable connector from J14.
4. If the chassis has an integral diskette drive, remove the cables from J17 and J18 of the IOC. Use the Scotchflex tool on the ribbon cable connector from J18.
5. If the chassis has diskette drive controller boards installed, remove the front panel and disconnect the cable leading to the front of the controller interface board. Pass the connector and cable through the opening at the side of the card cage so it is lying outside the chassis.
6. Remove the four screws holding the rear panel/IOC assembly to the chassis. Remove the rear panel/IOC assembly from the chassis, withdrawing the floppy diskette controller cable and connector (if there) through the opening the power supply.
7. Place rear panel/IOC assembly on work surface with the rear panel down. Remove the eleven screws holding the IOC to the rear panel.
8. Lift the IOC free of the rear panel.
9. If you are removing the IOC to measure signals on it, prop it against the rear of the power supply assembly, isolating it from the power supply by a soft non-conducting material. (1/2-inch thick foam packing material works good.) It may be convenient to replace the rear panel and prop the IOC against it. BE SURE THE IOC DOES NOT MAKE ELECTRICAL CONTACT WITH THE CHASSIS. Reconnect the IOC to make your measurements.

REPLACING THE IOC

1. Secure the IOC to the back of the rear panel with eleven screws. The component side of the IOC goes toward the rear panel.
2. Place the rear panel/IOC assembly against the power supply chassis, passing the floppy diskette controller cable and connector (if there) through the opening in the power supply. It is easier if you fit the rear panel/IOC assembly around the power and fuse assembly on the power supply first. Make sure the cables that will be connected to the IOC are not caught between the power supply and the IOC.
3. Secure the rear panel to the power supply by four screws.
4. Connect power supply connector A to J16 of the IOC. Connect P15 (from the CRT) to IOC J15.
5. If the chassis has an internal diskette drive, connect drive connector P17 to IOC connector J17 and drive connector P18 to IOC connector J18.
6. Replace the top cover on the chassis.
7. Connect the Development System to its ac source, and check it out.



878-27



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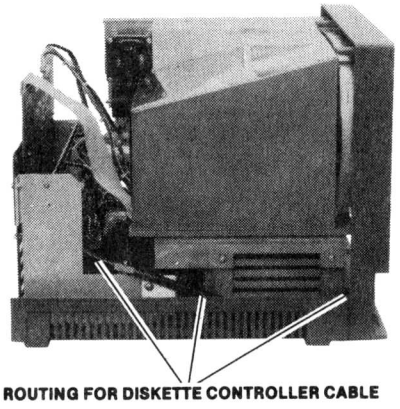


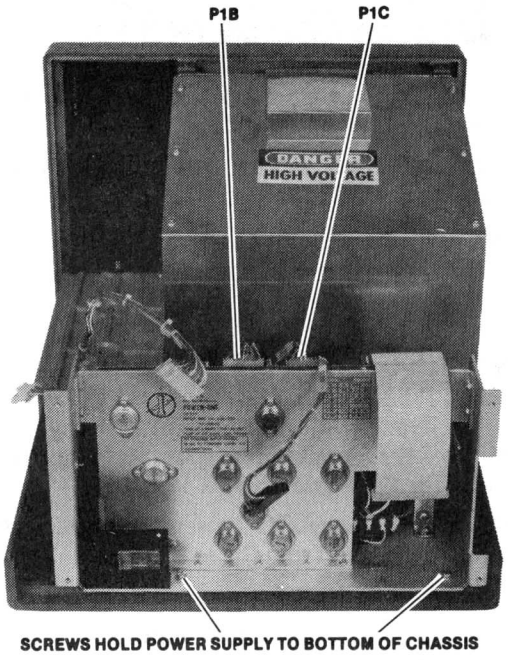
878-28

REMOVING THE POWER SUPPLY

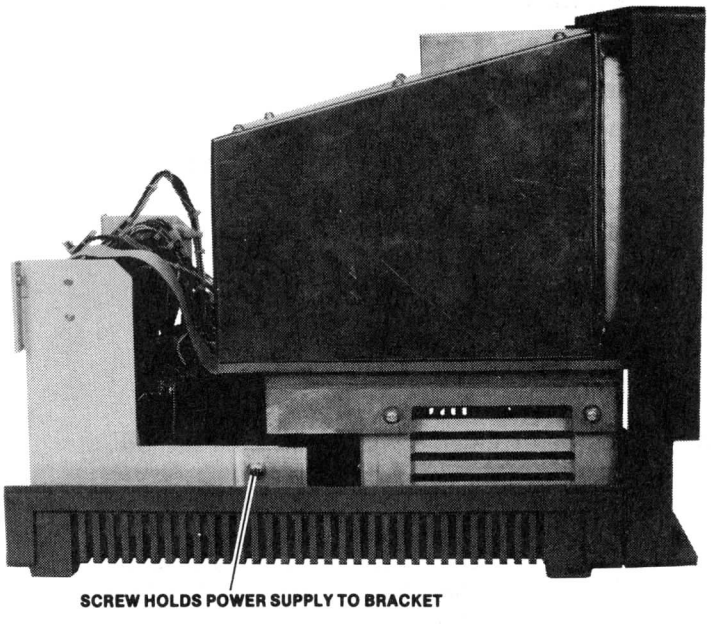
1. Disconnect the ac power cord from the Development System.
2. Remove top cover from the chassis.
3. Remove rear panel/IOC assembly. (You need not remove the IOC from the rear panel.)
4. Remove two screws holding the power supply to the bottom of the chassis.
5. Remove two screws holding the power supply to the power supply bracket. One screw is on each side of the unit.
6. Remove connectors P1C and P1B from the power supply.
7. If the chassis has an integral diskette drive, disconnect the cable supplying power to the drive. The connector in this cable is located at the lower rear of the drive, toward the CRT.
8. Slide the power supply toward the rear of the chassis approximately 2 inches to give better access to the connector in the cable supplying power to the card cage fan. This connector is adjacent to the fan on the power supply. It will be fairly difficult to slide the power supply out as the transformer makes it very heavy.
9. Disconnect the connector in the cable connected to the card cage fan and POWER switch.
10. Remove power supply from chassis.

REPLACING THE POWER SUPPLY

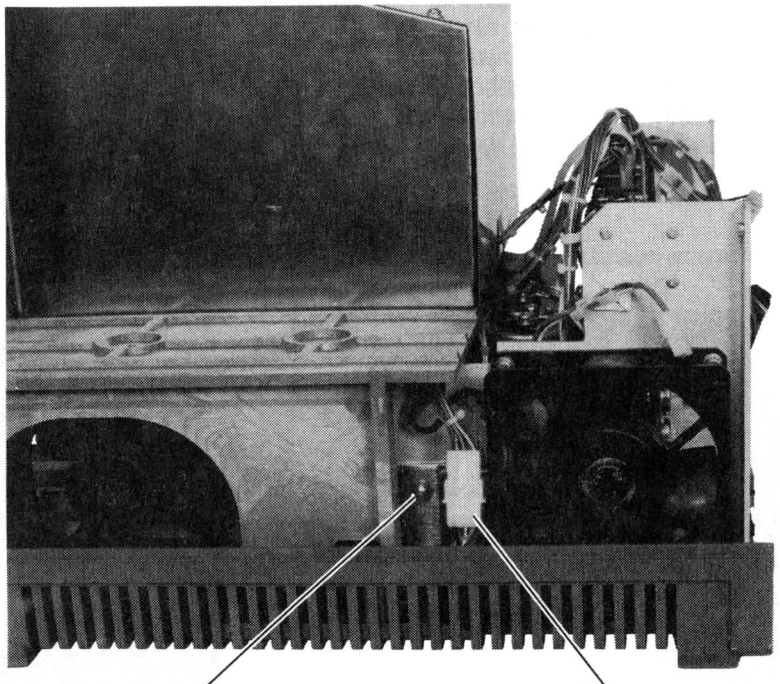
1. Make sure rear panel/IOC assembly is removed from chassis.
2. Slide power supply into chassis, with the shorter regulator board toward the CRT, until the shorter board is within approximately one inch of the CRT shelf.
3. Connect the two ends of the cable connected to the card cage fan and POWER switch, making sure that the missing pin aligns with the hole in the mating connector.
4. Slide the power supply on into the chassis, making sure that no cables are caught between the power supply and the CRT shelf.
5. Secure the power supply to the chassis with two screws.
6. Secure the power supply to the power supply bracket at each side of the chassis. One screw is required in each side.
7. Connect connector P1B to the row of stake pins labeled B on the power supply and connect connector P1C to the row of stake pins labeled C.
8. If the chassis has an integral diskette drive, connect connector D2 to the drive power connector located at the lower rear of the drive, toward the CRT.
9. If the chassis does not have an integral diskette drive, connector D2 is not connected. Position it above the power supply fan.
10. Replace the rear panel/IOC assembly.
11. Replace the top cover on the chassis.
12. Connect the Development System to its ac source and check it out.



878-29



878-30



878-31

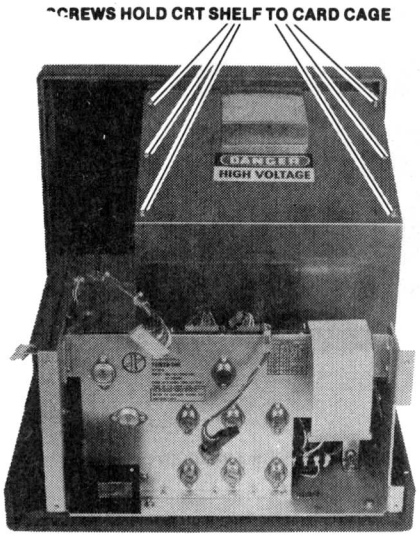
REMOVING THE CRT ASSEMBLY (PRELIMINARY INSTRUCTIONS)

1. Disconnect the ac power cord from the Development System.
2. Remove the top cover from the chassis.
3. Remove the six screws securing the CRT cover, and remove the CRT cover.

WARNING

If you are working inside the CRT assembly, heed the HIGH VOLTAGE warning label. The CRT operates with a 12KV anode voltage.

4. There are two methods used to fasten the CRT assembly to the CRT shelf. Method A uses screws inserted from the top inside of the CRT assembly, through the CRT assembly's baseplate, into captive fasteners mounted in the CRT shelf. Method B uses screws inserted from the bottom, up through the CRT shelf into captive fasteners mounted in the CRT assembly's baseplate. Look into the CRT assembly. If you see four screws in the baseplate, two located at the back corners and two located close to the CRT, Method A has been used for the installation. If you do not see these screws, Method B has been used. Proceed now to the Method A procedure or the Method B procedure as appropriate for your equipment.



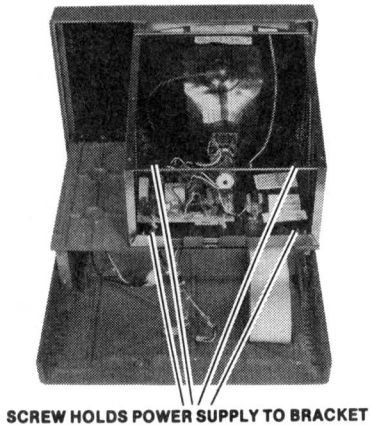
878-39

REMOVING THE CRT ASSEMBLY (INSTALLATION METHOD A)

1. Refer to the preliminary instructions for removing the CRT assembly.
2. Remove the four screws holding the CRT baseplate to the CRT shelf.
3. Remove the CRT assembly.

REMOVING THE CRT ASSEMBLY (INSTALLATION METHOD B)

1. Refer to the preliminary instructions for removing the CRT assembly.
2. Remove the rear panel/IOC assembly. (You need not remove the IOC from the rear panel.)
3. Remove the power supply.
4. Remove the front panel and remove all cards from the card cage.
5. Reach into the card cage and, with a stubby Phillips screwdriver, remove two screws holding the CRT assembly to the CRT shelf. The screws are approximately 6 inches from the front of the chassis, and can be seen by looking into the card cage.
6. Working from the rear of the unit, under the rear lip of the CRT shelf, remove two screws holding the CRT assembly to the CRT shelf.
7. Lift the CRT assembly from the chassis.



878-30

REPLACING THE CRT ASSEMBLY (PRELIMINARY INSTRUCTIONS)

1. As described in the preliminary instructions for removing the CRT assembly, there are two methods for installation of the assembly to the CRT shelf. Method A is the easier of the two, but will not work in all cases. Try Method A to replace the CRT assembly; if it doesn't work, use Method B.

REPLACING THE CRT (INSTALLATION METHOD A)

1. Refer to the preliminary instructions for replacing the CRT assembly.
2. Place the CRT assembly on the CRT shelf.
3. Start the four screws that secure the CRT assembly to the CRT shelf.
4. Position the CRT assembly so the CRT makes good alignment with the bezel.
5. Tighten the four screws securing the CRT assembly.
6. Make sure P1 of the cable connecting the CRT assembly to the IOC is firmly connected to J1 of the CRT assembly. J1 is located at the rear of the printed wiring assembly in the CRT assembly.
7. Replace the CRT cover, making sure it fits into the tabs at the bottom rear of the CRT assembly and that the cable connecting the CRT to the IOC is not pinched.
8. Secure the CRT cover with six screws.
9. Replace the top cover on the chassis.
10. Connect the Development System to its ac power source and check it out.

REPLACING THE CRT ASSEMBLY (INSTALLATION METHOD B)

1. Refer to the preliminary instructions for replacing the CRT assembly.
2. Make sure all cards are removed from the card cage.
3. Position the CRT assembly on the CRT shelf so the captive fasteners in the base of the assembly are aligned over the four small slots in the CRT shelf.
4. From the rear of the chassis, using a stubby Phillips screwdriver, fit two screws into the captive fasteners in the base of the CRT assembly. Do not tighten these screws yet; leave play so you can fit the other screws and align the assembly easier.
5. Reaching in through the front of the card cage, fit two screws through slots in the CRT shelf, into the captive fasteners in the base of the CRT assembly. Leave the screws loose until the CRT assembly is positioned properly.
6. Position the CRT assembly to align the CRT properly with the bezel, then tighten the four screws holding the CRT assembly to the CRT shelf.
7. Make sure P1 of the cable connecting the CRT assembly to the IOC is firmly connected to J1 of the CRT assembly. J1 is located at the rear of the printed wiring assembly in the CRT assembly.
8. Replace the CRT cover, making sure it fits into the tabs at the bottom rear of the CRT assembly and that the cable connecting the CRT to the IOC is not pinched.
9. Secure the CRT cover with six screws.
10. Replace the power supply.
11. Replace the rear panel/IOC assembly.
12. Replace the top cover on the chassis.
13. Replace the system cards in the card cage, then replace the front panel.
14. Connect the Development System to its ac source, and check it out.

REMOVING THE INTEGRAL DISKETTE DRIVE

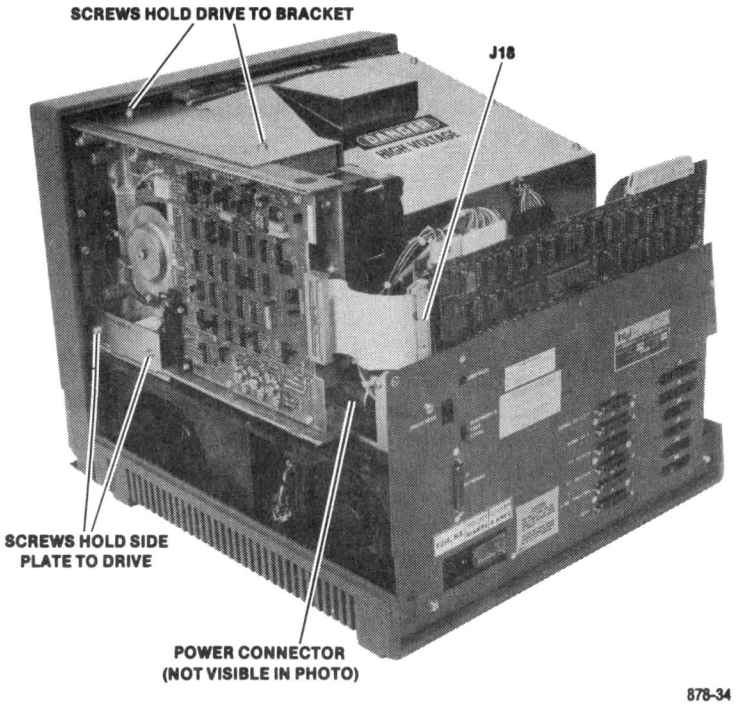
1. Disconnect the ac power cord from the Development System.
2. Remove the top cover from the chassis.
3. Disconnect the cable supplying power to the drive. The connector in this cable is located at the lower rear of the drive, toward the CRT.
4. Remove the control cable connector from J18 of the IOC. Use 3M Scotchflex Tool No. 3438 or equivalent to remove the ribbon cable connector.
5. Remove the two screws holding the top of the drive to the bracket extending over the top of the drive.
6. Remove the two screws holding the plate on the side of the drive.
7. Remove the drive.

NOTE

In some units, the drive will not slip past the power supply and you must remove the rear panel/IOC assembly and power supply to remove the drive.

REPLACING THE INTEGRAL DISKETTE DRIVE

1. Place the diskette drive on the CRT shelf, in its bracket and align it with the front of the chassis.
2. Secure the top bracket to the top of the drive with two screws.
3. Insert the side plate into the slots in the drive bracket and secure it to the side of the drive with two screws.
4. If necessary, replace the power supply and rear panel/IOC assembly.
5. Reconnect cable supplying power to the drive to connector at lower rear of drive, toward the CRT.
6. Reconnect the ribbon control cable from the drive to J18 of the IOC.
7. Replace the top cover on the chassis.
8. Connect the Development System to its ac source and check it out.



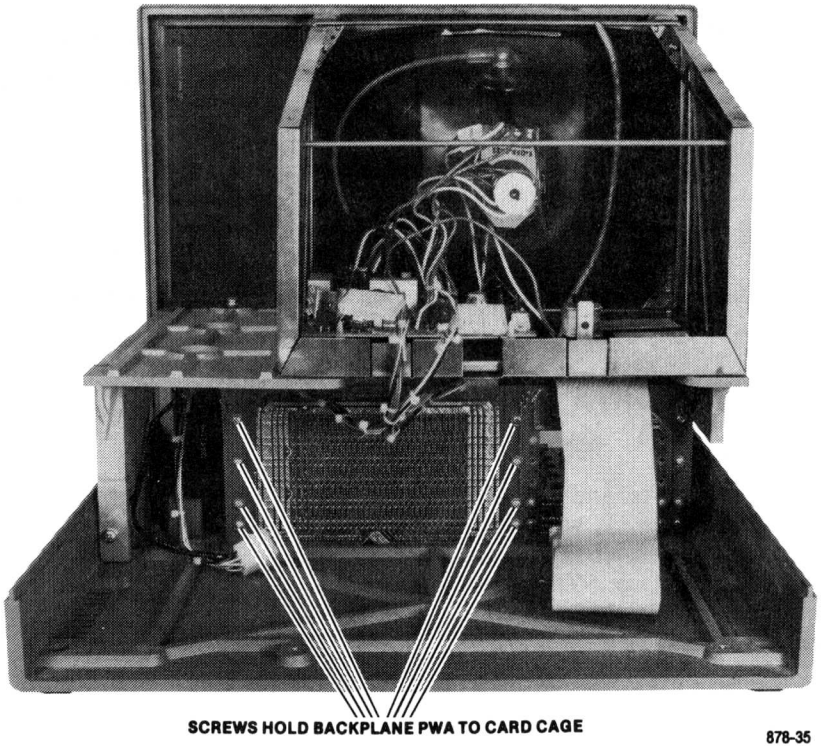
REMOVAL AND REPLACEMENT PROCEDURES (CONTINUED)

REMOVING THE BACKPLANE PWA

1. Remove the power from the Development System.
2. Remove the front panel and all cards from card cage.
3. Remove the top cover from the chassis.
4. Remove the rear panel/IOC assembly. (You need not remove the IOC from the rear panel.)
5. Remove the power supply.
6. Remove the two screws holding the power supply bracket to the bottom of the chassis. (Use a stub-by Phillips screwdriver.)
7. Remove the 12 screws holding the backplane to the card cage. If the chassis has an integral power supply, do not remove screws holding controller board connectors to backplane.
8. Withdraw the backplane PWA from the chassis.

REPLACING THE BACKPLANE PWA

1. Make sure all cards are removed from the card cage.
2. Secure the backplane PWA to the rear of the card cage with 12 screws.
3. Replace the power supply bracket with two screws.
4. Replace the power supply.
5. Replace the rear panel/IOC assembly.
6. Replace the top cover on the chassis.
7. Apply power and check out the Development System.



SCREWS HOLD BACKPLANE PWA TO CARD CAGE

878-35

REMOVING THE CARD CAGE FAN

1. Remove power from the Development System.
2. Remove the top cover from the chassis.
3. Remove the rear panel/IOC assembly. (You need not remove the IOC from the rear panel.)
4. Remove the power supply.
5. If an integral diskette drive is installed:
   a. Remove the CRT assembly
   b. Remove the diskette drive
   c. Remove the five screws holding the diskette drive bracket to the chassis and CRT shelf.
6. If an integral diskette drive is not installed, remove the screw holding the plate covering the diskette drive opening (at the side of the CRT) to the drive CRT shelf.
7. From the front of the unit, remove two screws hold securing the CRT shelf to the chassis.
8. From the rear of the chassis, remove one screw securing the CRT shelf to the chassis.
9. On the left side of the chassis, remove two screws securing the CRT shelf to the card cage.
10. Slide CRT shelf to the rear and remove it from the chassis.
11. Remove the two screws holding the card cage fan to the card cage.

REMOVING AND REPLACING THE POWER SWITCH

The POWER switch may be removed and replaced from the front of the chassis. However, wires connecting the POWER switch to the power supply are attached to the top of the card cage. You must remove the CRT shelf as described in the procedure for removing the card cage fan to get to these wires.

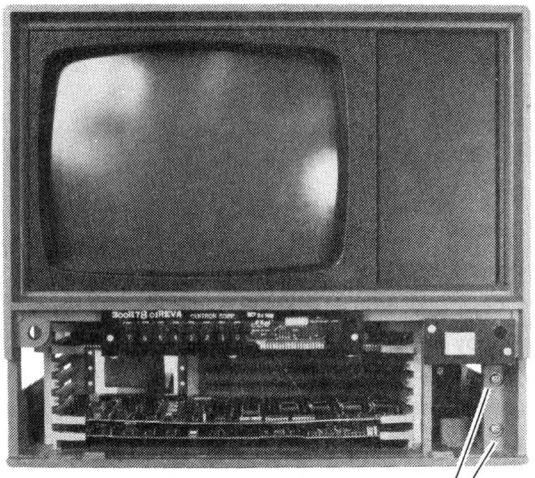
REPLACING THE CARD CAGE FAN

1. Secure the card cage fan to the card cage with two screws.
2. Place the CRT shelf in place, guiding the power cable for the card cage fan between the rear leg of the shelf and the card cage.
3. On the left side of the chassis, secure the CRT shelf to the card cage with two screws.
4. Secure the rear leg of the CRT shelf to the chassis with one screw.
5. At the front of the chassis, secure the CRT shelf to the chassis with two screws.
6. If a the chassis does not have an integral diskette drive, secure the plate covering the diskette drive opening to the CRT shelf if the chassis does not have an integral diskette drive:
   a. Secure the plate covering the diskette drive opening to the chassis with two screws.
   b. Secure the plate covering the diskette drive opening to the CRT shelf with one screw.
7. If the chassis has an integral diskette drive:
   a. Replace the diskette drive
   b. Replace the CRT assembly
   c. Secure the drive bracket to the chassis with two screws.
   d. Secure the drive bracket to the CRT shelf with three screws.
8. Replace the power supply.
9. Replace the rear panel/IOC assembly.
10. Replace the top cover on the chassis.
11. Apply ac power to the Development System and check it out.

REMOVAL AND REPLACEMENT PROCEDURES (CONTINUED)

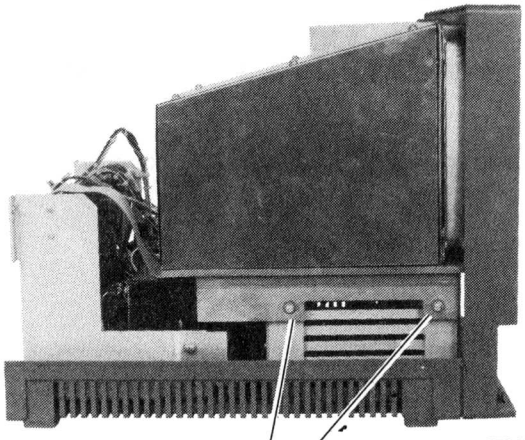
SCREWS HOLD DISKETTE DRIVE PLATE TO CHASSIS

878-36



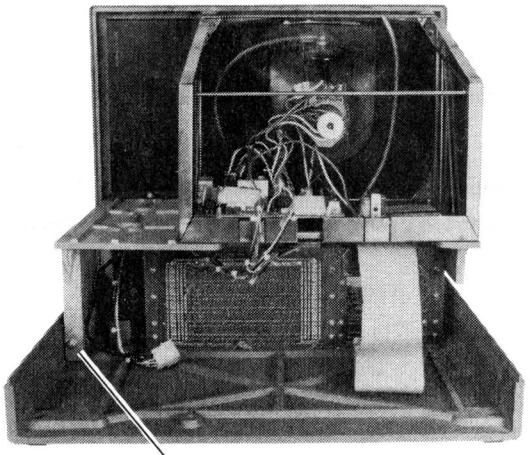
878-37

SCREWS HOLD CRT SHELF TO CHASSIS



878-39

SCREWS HOLD CRT SHELF TO CARD CAGE



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SCREW HOLDS CRT SHELF TO CHASSIS

REPLACEABLE PARTS
MODELS 220, 221, 222
MICROCOMPUTER DEVELOPMENT SYSTEMS

Description	Intel Part No.	Qty/Assy	Used On
IOC PWA	1001241-04	1	
IPB Assy (Note 1)	4001246-03	1	
IPB PWA	1001194-01	1	
Control Panel PWA	1001200-01	1	
Backplane PWA	1001223-01	1	
CRT Assy	4501244-01	1	
Keyboard Assy	4501240-01	1	220, 221,
Keyboard Assy	4501240-02	1	222
Keyboard Cable Assy	4001261-01	1	
Disk Drive	4500963-01	1	220
Disk Drive	4500963-02	1	221, 222
Power Supply	4501253-01	1	
Floppy Disk Signal Cable	4001256-01	1	
Floppy Disk Power Cable	4001522-01	1	
7-Position DC Cable Assy (Backplane J12 to Power Supply P1C)	4001515-01	1	
9-Position DC Cable Assy (Backplane J13 to Power Supply P1B)	4001608-01	1	
Power Switch Cable Assy	4001614-01	1	
CRT Cable Assy	4001615-01	1	
Fuse, 6.25 amp, slow blow	70-013	1	220
Fuse, 3 amp, slow blow	70-010	1	221, 222
Fan	74-008	2	
Power Switch	66-048	1	
ISIS-II System Diskette, Single Density	9500007-02	2	220, 221, 222
Confidence Test Diskette, Single Density	9500023	1	220, 221, 222

Notes:

1. Replace IPB Assy 4001246-03. IPB PWA and Control Panel PWA part numbers provided for reference only.
2. Parts are used on all models unless otherwise indicated.

REPLACEABLE PARTS
MODELS 230, 231, 232
MICROCOMPUTER DEVELOPMENT SYSTEMS

Description	Intel Part No.	Qty/Assy	Used On
IOC PWA	1001241-04	1	
IPB Assy (Note 1)	4001246-03	1	
IPB PWA	1001194-01	1	
Control Panel PWA	1001200-01	1	
Backplane PWA	1001223-01	1	
CRT Assy	4501244-01	1	
Keyboard Assy	4501240-01	1	230, 231
Keyboard Assy	4501240-02	1	232
Keyboard Cable Assy	4001261-01	1	
Power Supply	4501253-01	1	
Floppy Disk Signal Cable	4001256-01	1	
Floppy Disk Power Cable	4001522-01	1	
7-Position DC Cable Assy (Backplane J12 to Power Supply P1C)	4001515-01	1	
9-Position DC Cable Assy (Backplane J13 to Power Supply P1B)	4001608-01	1	
Power Switch Cable Assy	4001614-01	1	
CRT Cable Assy	4001615-01	1	
Fuse, 6.25 amp, slow blow	70-013	1	230
Fuse, 3 amp, slow blow	70-010	1	231, 232
Fan	74-008	2	
Power Switch	66-048	1	
Floppy Disk Controller Channel PWA	1000-467-04	1	
Floppy Disk Controller Interface PWA, Dual Density	1001036-01	1	
32K RAM PWA	iSBC-032	1	
Dual Aux PWA (Connects Floppy Disk Controller PWA's)	1000751-01	1	
Dual Floppy Control Cable Assy	4001516-01	1	
ISIS-II System Diskette, Double Density	9700003-03	2	
Confidence Test Diskette, Double Density	9700023	1	

REPLACEABLE PARTS
INTEGRATED PROCESSOR (IPB)
PWA 1001194-03

This list provided for reference only. PWA configuration may vary. Intel recommends replacement of complete IPB Assembly, which includes IPB PWA.

Ref. Desig	Description	Intel Part No.	Qty/Assy	Notes
A1	IC, 7406, Hex Inverters	54-092	3	2
A2	IC, 74S00, Quad 2-Input NAND Gates	54-054	3	2
A3	Same as A1			
A4	IC, 74LS157, Quad 2-to-1 Data Selectors	54-170	1	2
A5	IC, 74148, 8-to-3 Encoder	54-080	2	2
A6	IC, 3601 Type, 256x4 bit Programmed ROM	9100016	1	1
A7	IC, 74S174, Hex D-type Flip-Flops	54-146	2	2
A8	IC, 774S257, Quad 2-to-1 Data Selectors	54-052	1	2
A9	Same as A7			
A10	IC, 74LS51, AND-OR-Invert Gates	54-200	1	2
A11	IC, 74LS74, Dual D-type Flip-Flops	54-097	1	2
A12	IC, 74S05, Hex Inverters	54-064	1	2
A13	Same as A2			
A14	IC, 9602	54-016	2	
A15	IC, 7474, Dual D-type Flip-Flops	54-025	1	2
A16	IC, 9LS10, Quad 2-Input NAND-Gate	54-198	1	
A17	IC, 74LS109, Dual J-K Flip-Flops	54-184	1	2
A18-A25	IC, 2117-5, 16K Bit RAM	52-197	16	1
A26	IC, 74S374, Octal D-type Flip-Flops	54-193	1	2
A27	IC, 3222, Refresh Controller	52-152	1	1
A28	IC, 8224, Clock Generator and Driver	52-045	1	1
A29	Same as A14			
A30	IC, 74LS20, Dual 4-Input NAND Gates	54-199	1	2
A31	IC, 74LS155, Dual 2-to-4 Decoder/Demultiplexer	54-126	2	2
A32	IC, 74S74, Dual D-type Flip-Flops	54-061	1	2
A33-A40	Same as A18			
A41	IC, 74LS244, Octal line Drivers	54-239	1	2
A42	Same as A31			
A43	IC, 74S112, Dual J-K Flip-Flop	54-118	1	2
A44	IC, 74LS10, Triple 3-Input NAND Gate	54-111	1	2
A45	IC, 74S08, Quad 2-Input AND Gate	54-129	1	2
A46	IC, 74LS240, Octal Line Drivers	54-203	4	2
A47	IC, 8259, Programmable Interrupt Controller	52-105	2	1
A48	IC, 2716 Type, 2K byte Programmed ROM	9100121	1	1
A49	IC, 8253, Programmable Interface Timer	52-106	1	1
A50	IC, 3242, Address Mux and Refresh Counter	52-153	1	1
A51	IC, 74177, Binary Counter/Latch	54-127	2	2
A52	Same as A2			

A53	IC, 74S05, Hex Inverters	54-201	1	2
A54	IC, 74S32, Quad 2-Input OR Gates	54-143	1	2
A55	IC, 74S03, Quad 2-Input NAND Gates	54-110	1	2
A56	Not Used			
A57	IC, 2716 Type, 2K byte Programmed ROM	9100122	1	1
A58, A59	IC, 74S240, Octal Line Drivers	54-209	2	2
A60	Same as A47			
A61	Same as A46			
A62	IC, 8251, Programmable Communication Interface	52-035	2	1
A63	IC, 75188/1488, Quad Receivers	54-140	2	
A64, A65	IC, TIL 113, Optoisolator	54-159	3	
A66	IC, 8218, Bus Controller	52-104	1	1
A67	IC, 8080A-2, Microprocessor	52-100	1	1
A68	IC, 8228, System Controller and Bus Driver	52-088	1	1
A69	IC, 3601 Type, 256x4 bit Programmed ROM	9100007	1	1
A70	IC, 3601 Type, 256x4 bit Programmed ROM	52-789	1	1
A71	IC, 3601 Type, 256x4 bit Programmed ROM	52-788	1	1
A72	IC, 8216, Bidirectional Bus Driver	52-044	2	1
A73	IC, 74LS259, 8-Bit Addressable Latches	54-252	1	2
A74	Same as A62			
A75	IC, 74LS241, Octal Line Drivers	54-186	1	2
A76	Same as A64			
A77	IC, 75189A/1489A, Quad Line Receivers	54-141	3	
A78	Same as A51			
A79	IC, 74S37, Quad 2-Input NAND Gates	54-120	1	2
A80	IC, 74259, 8-Bit Addressable Latches	54-202	1	2
A81	Same as A1			
A82, A83	Same as A46			
A84-A87	IC, 8226, Bidirectional Bus Driver	52-033	4	1
A88	Same as A72			
A89	Same as A63			
A90, A91	Same as A77			
A92	IC, 74S138, 3-to-8 Decoder/Multiplexer	54-113	1	2
A93	Same as A5			
C1-C7 C10, C11, C38, C39, C41, C53, C54, C72, C73, C75-C77	Capacitor, ceramic, 0.01 μF, 25V, ±5%	64-007	19	3

C8, C12-C20, C23, C25, C27, C29, C31, C33 C35, C37, C42, C45-C52, C56, C58, C60, C62, C64, C66, C68, C70, C78, C80-C84, C87-C95, C98, C100-C111	Capacitor, mono, 0.1 μF, +80%, −20%, 50V	64-050	63	3
C9	Capacitor, mica, 100 pF, ±5%, 500V	64-016	1	3
C21, C79	Capacitor, mica, 15 pF, ±5%, 500V	64-026	2	3
C22, C26, C30, C34, C43, C44, C55, C59, C63, C67	Capacitor, mono, 1.0 μF, +80%, −20%, 50V	64-058	10	3
C24, C28, C32, C36, C57, C61, C65, C69	Capacitor, mono, 0.01 μF, +80%, −20%, 50V	64-075	8	3
C40	Capacitor, ceramic, 0.02 μF, ±20%, 100V	64-004	1	3
C71	Capacitor, mono, 0.0047 μF, ±20%, 100V	64-069	1	3
C74	Capacitor, tantalum, 2.2 μF, +10%, 20V	64-009	1	3
C86	Capacitor, mica, 220 pF, ±5%, 500V	64-039	1	3
C96, C97, C99	Capacitor, mica, 330 pF, ±5%, 500V	64-043	3	3
C112-C116	Capacitor, tantalum, 22 μF, +10%, 15V	64-012	4	3
CR1-CR3	Diode 1N914	60-003	3	3
DL1	IC, 9824, Delay Line	54-204	1	
J1	Connector, 21 pin	68-264	1	
J2	Header post, 34 pin	68-253	1	
L1	Inductor, RF, 0.22 μH	50-004	1	3
Q1, Q2	Transistor, 2N3904	58-007	2	3
Q3	Transistor, 2N3906	58-008	1	3
R1	Resistor, composition, 33 ohms, 1/4W, ±5%	56-003	1	3
R2-R4, R23	Resistor, composition, 1.2K, 1/4W, ±5%	56-026	4	3

R5, R15, R16 R18-R20, R26, R29, R32, R33, R36, R37, R40, R41, R43, R44	Resistor, composition, 1K, 1/4W, ±5%	56-024	16	3
R6	Resistor, composition, 330K, 1/4W, ±5%	56-102	1	3
R7, R11	Resistor, composition, 33K, 1/4W, ±5%	56-053	2	3
R8	Resistor, composition, 220 ohms, 1/4W, ±5%	56-011	1	3
R9	Resistor, composition, 180 ohms, 1/4W, ±5%	56-190	1	3
R10	Resistor, composition, 180 ohms, 1/4W, ±5%	56-324	1	3
R12	Resistor, composition, 15K, 1/4W, ±5%	56-047	1	3
R13	Resistor, composition, 22 ohms, 1/4W, ±5%	56-003	1	3
R14	Resistor, composition, 820 ohms, 1/4W, ±5%	56-003	1	3
R17	Resistor, metal film, 4.75K, 1/4W, ±1%	56-171	1	3
R21	Resistor, composition, 21 ohms, 1/4W, ±5%	56-134	1	3
R22, R47	Resistor, composition, 560K, 1/4W, ±5%	56-209	2	3
R24, R25, R48	Resistor, composition, 2.2K, 1/4W, ±5%	56-031	3	3
R27	Resistor, composition, 330 ohms, 1/4W, ±5%	56-016	1	3
R28	Resistor, metal film, 274 ohms, 1/8W, ±1%	56-292	1	3
R30, R31, R38	Resistor, composition, 6.8K, 1/4W, ±5%	56-042	3	3
R34	Resistor, composition, 82 ohms, 1/4W, ±5%	56-241	1	3
R35	Resistor, composition, 300 ohms, 1/2W, ±5%	56-240	1	3
R39, R42	Resistor, composition, 560 ohms, 1/2W, ±5%	56-239	2	3
R45	Resistor, wire-wound, 300 ohms, 1W, ±5%	56-242	1	3
R46	Resistor, wire-wound, 82 ohms, 2W, ±5%	56-243	1	3
RP1	Resistor pack, 16 pin, 1K, ±5%, 1.5W	56-054	1	3
RP2, RP4	Resistor pack, 14 pin, 1K, ±5%	56-055	2	3
RP3	Resistor pack, 14 pin, 47 ohms, ±5%	56-291	1	3
RP5	Resistor pack, 6 pin, 2.2K, ±5%	56-324	1	3
RP6, RP7, RP9	Resistor pack, 10 pin, 2.2K, ±5%	56-103	3	3
RP8, RP10	Resistor pack, 10 pin, 1K, ±5%	56-108	2	3
VR1	Voltage regulator, μA79MO5AUC	54-134	1	3
Y1	Crystal, 19.6608 MHz	62-006	1	3
Y2	Crystal, 23.4000 MHz	62-022	1	3

REPLACEABLE PARTS
I/O CONTROLLER (IOC)
PWA 1001241-04

NOTE

This list provided for reference only. PWA configuration may vary. Intel recommends replacement of complete PWA.

Ref. Desig	Description	Intel Part No.	Qty/Assy
A1	IC, 8271, Programmable Floppy Disk Controller	52-165	1
A2	IC, 74S175, Quad D-Type Flip-Flops	54-201	1
A3	IC, 74S74, Dual D-Type Flip-Flops	54-061	3
A4	IC, 74LS166, 8-bit Shift Register	54-242	1
A5	IC, 74LS151, 1-of-8 Data Selector/Multiplexer	54-243	1
A6	IC, 7437, Quad 2-Input NAND-Gates	54-068	1
A7	IC, 74LS74, Dual D-Type Flip-Flops	54-097	4
A8	IC, 74LS02, Quad 2-Input NOR-Gates	54-142	3
A9	IC, 74LS174, Hex D-Type Flip-Flops	54-146	2
A10	IC, 74LS04, Hex Inverters	54-096	2
A11	IC, 74LS195, 4-bit Parallel-Access Shift Register	54-150	1
A12	IC, 74LS00, Quad 2-Input NAND-Gates	54-099	3
A13, A14	IC, 74S374, Octal D-Type Flip-Flops	54-193	2
A15	Not used		
A16	Same as A3		
A17	IC, 74S163, 4-bit Counter	54-175	2
A18	IC, 74S00, Quad 2-Input NAND-Gates	54-054	2
A19	IC, Type 2708, 1K byte Programmed ROM	9100064	1
A20	IC, 8275, Programmable CRT Controller		1
A21	Same as A12	52-166	
A22	Not used		
A23	IC, 74LS240, Octal Line Drivers	54-203	3
A24, A25	Same as A7		
A26	IC, 74LS32, Quad 2-Input OR-Gates	54-130	1
A27	Same as A10		
A28	IC, 7416, Hex Inverters	54-244	1
A29	Same as A17		
A30-A33	IC, C2108AGL, 8K bit RAM	52-111	8
A34	IC, 8226, Bidirectional Bus Driver	52-033	10
A35	IC, 8253, Programmable Interface Timer	52-106	1
A36	Same as A8		
A37	IC, 74LS08, Quad 2-Input AND-Gates	54-087	2
A38	Same as A12		
A39	IC, P8205, 1 of 8 Binary Decoder	52-016	3
A40	IC, 74S140, Dual 4-Input Line Drivers	54-098	1
A41-A44	Same as A30		
A45	Same as A34		
A46	IC, 3242, Address Mux and Refresh Counter	52-153	1

A47	Same as A3		
A48	Same as A9		
A49	Same as A7		
A50	IC, Tyep 2716, 2K byte Programmed ROM	9100087	1
A51	IC, Tyep 2716, 2K byte Programmed ROM	9100088	1
A52	IC, Type 2716, 2K byte Programmed ROM	9100089	1
A53	IC, Type 2716, 2K byte Programmed ROM	9100090	1
A54	Not used		
A55	Same as A18		
A56	Same as A37		
A57	IC, 74LS37, Quad 2-Input NAND-Gates	54-017	1
A58	IC, P8257, Programmable DMA Controller	52-119	
A59, A60	Same as A39		
A61	Same as A8		
A62-A65	Not used		
A66	IC, C8226, Bidirectional Bus Driver	52-046	1
A67	IC, P8212, 8-bit I/O Port	52-019	1
A68	IC, D8224, Clock Generator and Driver	52-045	1
A69	IC, 8080A-2, Microprocessor	52-100	1
A70, A71	Same as A34		
A72	IC, 8741-4, Programmed Universal Peripheral Interface		1
A73-A76	Same as A34		
A77	IC, 74154, 4-to-16 Decoders/Demultiplexers	54-234	1
A78, A79	Same as A34		
A80, A81	Same as A23		
A82	IC, 74LS174, Hex D-Type Flip-Flops	54-169	1
A83	IC, 7432, Quad 2-Input OR-Gates	54-035	1
A84	IC, 74LS175, Quad D-Type Flip-Flops	54-167	1
C1, C14 C19-C22, C28, C30, C32, C34, C36-C40, C43-C46, C51, C53, C55, C57, C58, C61, C64-C68, C70-C72, C77, C78	Capacitor, ceramic, mons, 0.1 μF	64-050	35

C2-C13, C15-C18, C23-C27, C31, C35, C47-C49, C52, C56, C59, C60, C62, C63, C73, C74, C79-C82, C84-C88	Capacitor, cermaic, 0.01 μF	64-007	44
C29, C33, C50, C54	Capacitor, mono, 1.0 μF, +80%, −20%, 50V	64-058	4
C41, C42, C76	Capacitor, tantalum, 2.2 μF, 20V, ±10%	64-009	3
C69, C75, C83	Capacitor, mica, 20 pF, 500V, ±10%	64-073	3
C89	Capacitor, tantalum, 47 μF, 20V, ±10%	64-011	1
CR1	Diode, 1N914B	60-003	1
J1-J7	Connector, receptacle, 25 contact	68-275	7
J14, J18	Connector, 50 pin	68-023	2
J16	Connector, header, 12 pin	68-298	1
J17	Connector, header, 7 pin	68-912	1
LS1	Buzzer, 3.3 kHz	62-026	1
R1-R5, R38	Resistor, composition, 150 ohms, 1/4W, ±5%	56-024	6
R6-R11, R13, R15, R17-R21, R23-R30, R32-R34, R37, R39-R43, R53, R54	Resistor, composition, 1K	56-024	33
R12, R35, R45, R47, R49, R51, R55	Resistor, composition, 470 ohms	56-019	7
R14, R36, R46, R48, R50, R52	Resistor, composition, 330 ohms, 1/4W, ±5%	56-016	6
R22	Resistor, trimpot, 500 ohms, 1/2W, ±10%	56-309	1
R31	Resistor, trimpot, dual, 100K	56-317	1
R44	Resistor, composition, 560K, 1/4W, ±5%	56-209	1
RP1	Resistor pack, 10 pin SIP, 470 ohms, 2.7W, ±10%	56-290	1
RP2	Resistor pack, 8 pin SIP, 1K, 2W	56-204	1
S1	Switch, slide, DP3T	66-050	1
VR1	Voltage regulator (79M05-05)	54-135	1

W1-W7	Header, post, 34 pin	68-253	1
W8	Header, straight, 2 pin	68-254	1
Y1	Crystal, 8 MHz, 14 pin DIP	62-014	1
Y2	Crystal, 22.032 MHz, HC 18/U	62-025	1
Y3	Crystal, 6 MHz, HC 18/U	62-015	1

REPLACEABLE PARTS
CONTROL PANEL PWA 1001200-01

NOTE

This list provided for reference only. PWA configurations may vary. Intel recommends replacement of complete IPB Assembly, which includes Control Panel PWA.

Ref. Desig	Description	Intel Part No.	Qty/Assy
DS1	LED, Red	60-019	1
R1	Resistor, 240 ohms, 1/4W, ±5%	56-012	1
RP	Resistor Pack, 14 pin DIP, 1K, ±2%	56-055	1
SW1	Switch, "0"	3001535-01	1
SW2	Switch, "1"	3001535-02	1
SW3	Switch, "2"	3001535-03	1
SW4	Switch, "3"	3001535-04	1
SW5	Switch, "4"	3001535-05	1
SW6	Switch, "5"	3001535-06	1
SW7	Switch, "6"	3001535-07	1
SW8	Switch, "7"	3001535-08	1
SW9	Switch, "Reset"	66-045	1

REPLACEABLE PARTS
BACKPLANE PWA 1001223-01

NOTE

This list provided for reference only. PWA configuration may vary. Intel recommends replacement of complete PWA.

Ref. Desig	Description	Intel Part No.	Qty/Assy
J1-J6	Connector, 86-pin, 0.156 ctr	68-182	6
J11	Connector, 60 pin, 0.100 ctr	68-134	1
J12	Header, 7 pin	68-192	1
J13	Header, 9 pin	68-280	1
J14, J16	Header, 50 pin	68-203	2
P14	Connector, 50 pin	68-031	1
P23	Connector, 50 pin	68-279	1
R1	Resistor, carbon, 220 ohms, 5%, 1/4W	56-011	2
R2	Resistor, carbon, 330 ohms, 5%, 1/4W	56-016	2
R3	Same as R1		
R4	Same as R2		

REPLACEABLE PARTS
KEYBOARD 4501240

This list provided for reference only. Keyboard configuration may vary. Intel recommends replacement of complete keyboard.

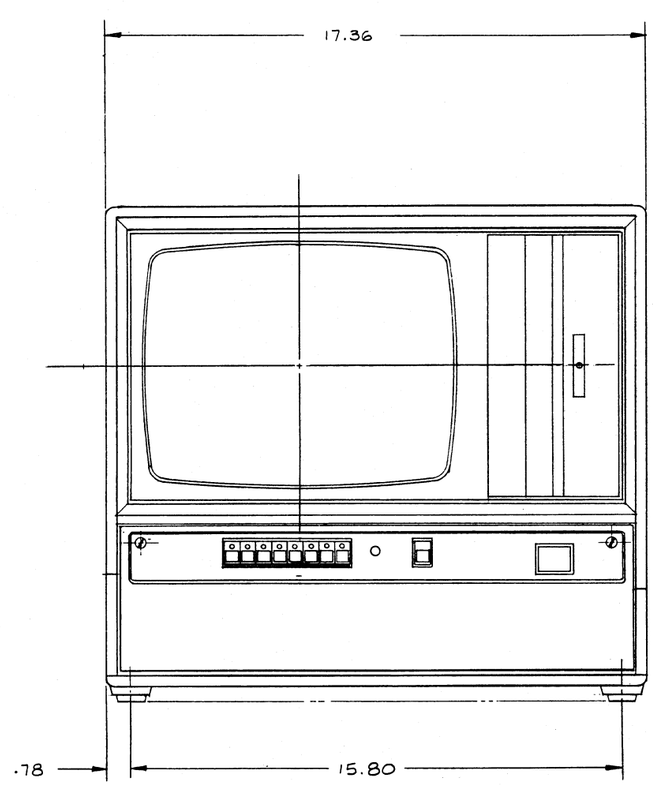
Ref. Desig	Description	Intel Part No.	Qty/Assy
A1	IC, Type 8741, Programmed	9100101	1
A2	IC, 74154, 4-to-16		1
A3, A4	IC, 7404, Hex Inverters		2
C22, C23	Capicitor, 20 pF, ±5%, 500V		2
C24	Capacitor, 0.1 μF, 16V		1
C25	Capacitor, 15 μF, 35V		1
C26, C28	Capacitor, 0.01 μF, 25V		3
R5-R12	Resistor, 4.7K, ¼W, ±5%		8
R13	Resistor, 1K, ¼W, ±5%		
R14-R16	Resistor, 339 ohm, ¼W, ±5%		3
R17-R19	Resistor, 470 ohms, ¼W, ±5%		3
Y1	Oscillator, 3.58 MHz, Case size HC 13 or HC 25, series resonant fundamental mode		1

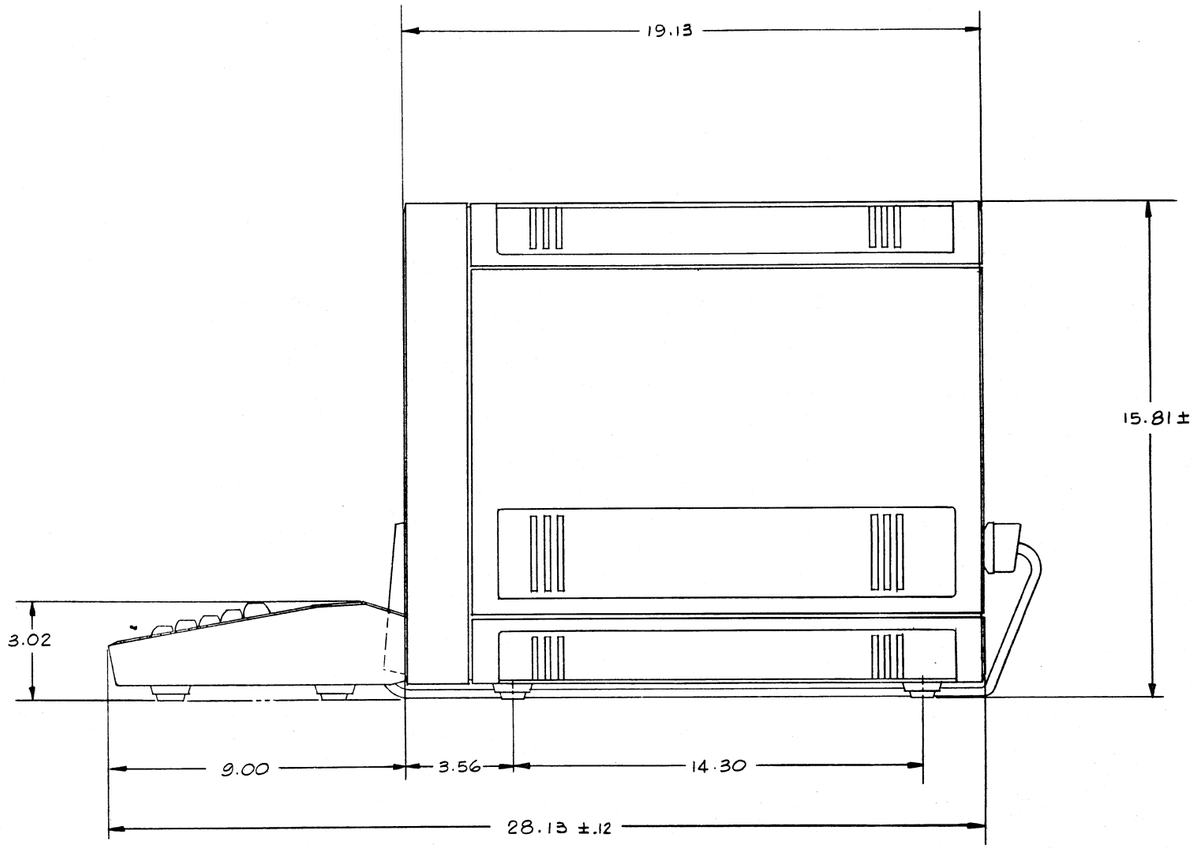
DIAGRAMS

The interconnection diagrams and schematics provided on the following pages document a baseline configuration of the equipment covered by this manual. There may be minor differences between the equipment you receive and this baseline equipment. If you require documentation of your exact configuration, contact your Intel Customer Engineer for information on its procurement.

NOTE

On the schematic diagrams, a signal mnemonic that ends with a slash (e.g., IOWC/) is active low. Conversely, a signal mnemonic without a slash (e.g., BTMO) is active high.

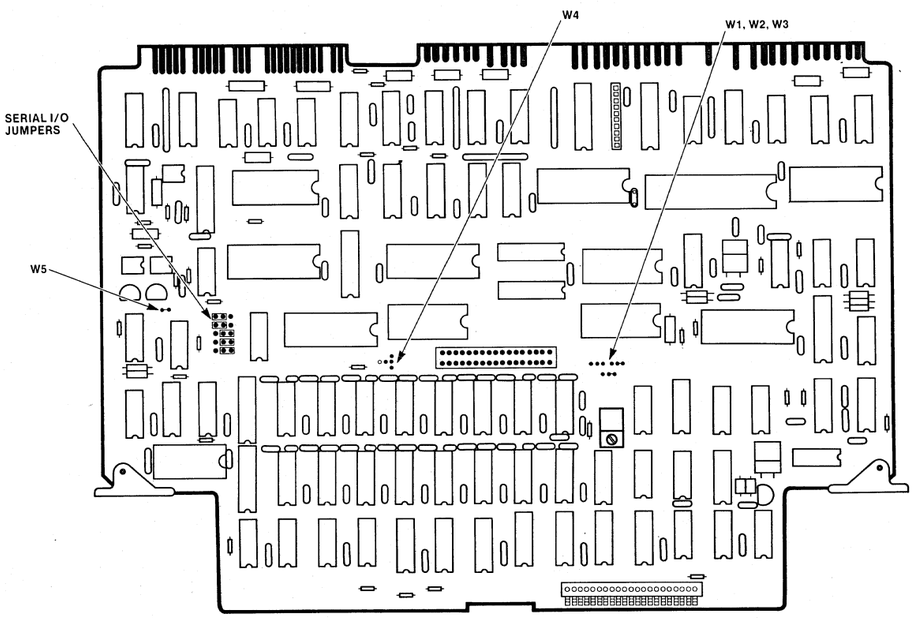


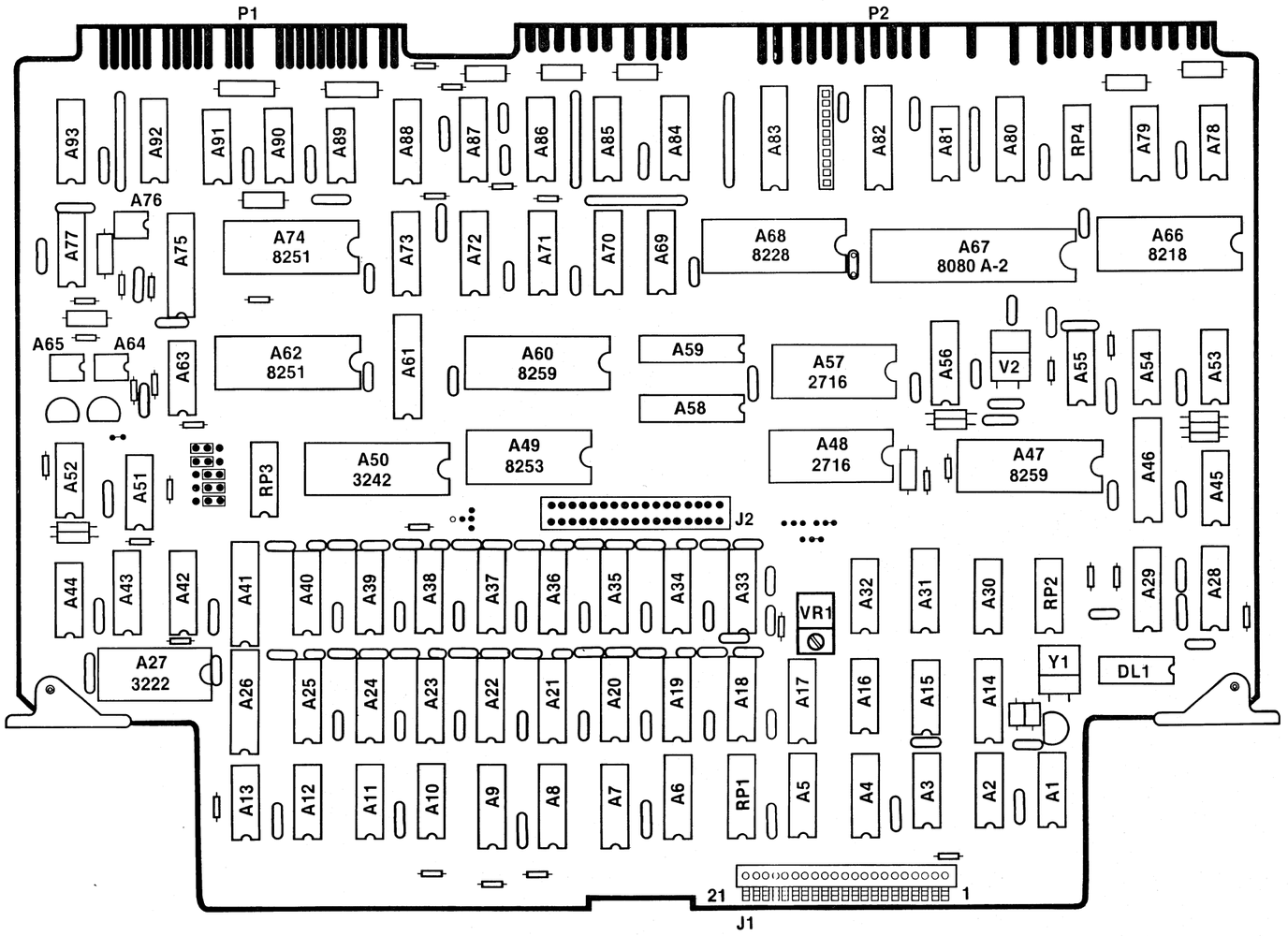


DIMENSIONS IN INCHES

Models 22X, 23X Main Chassis Outline Drawing

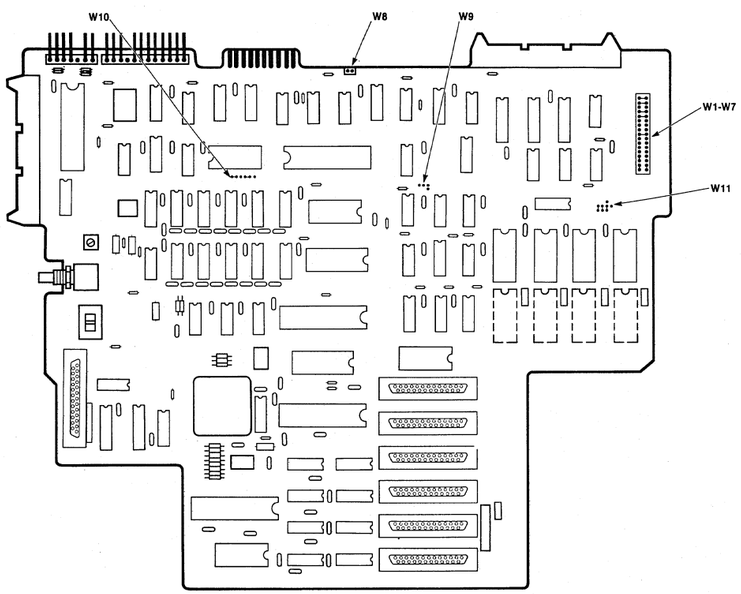
JUMPER LOCATIONS

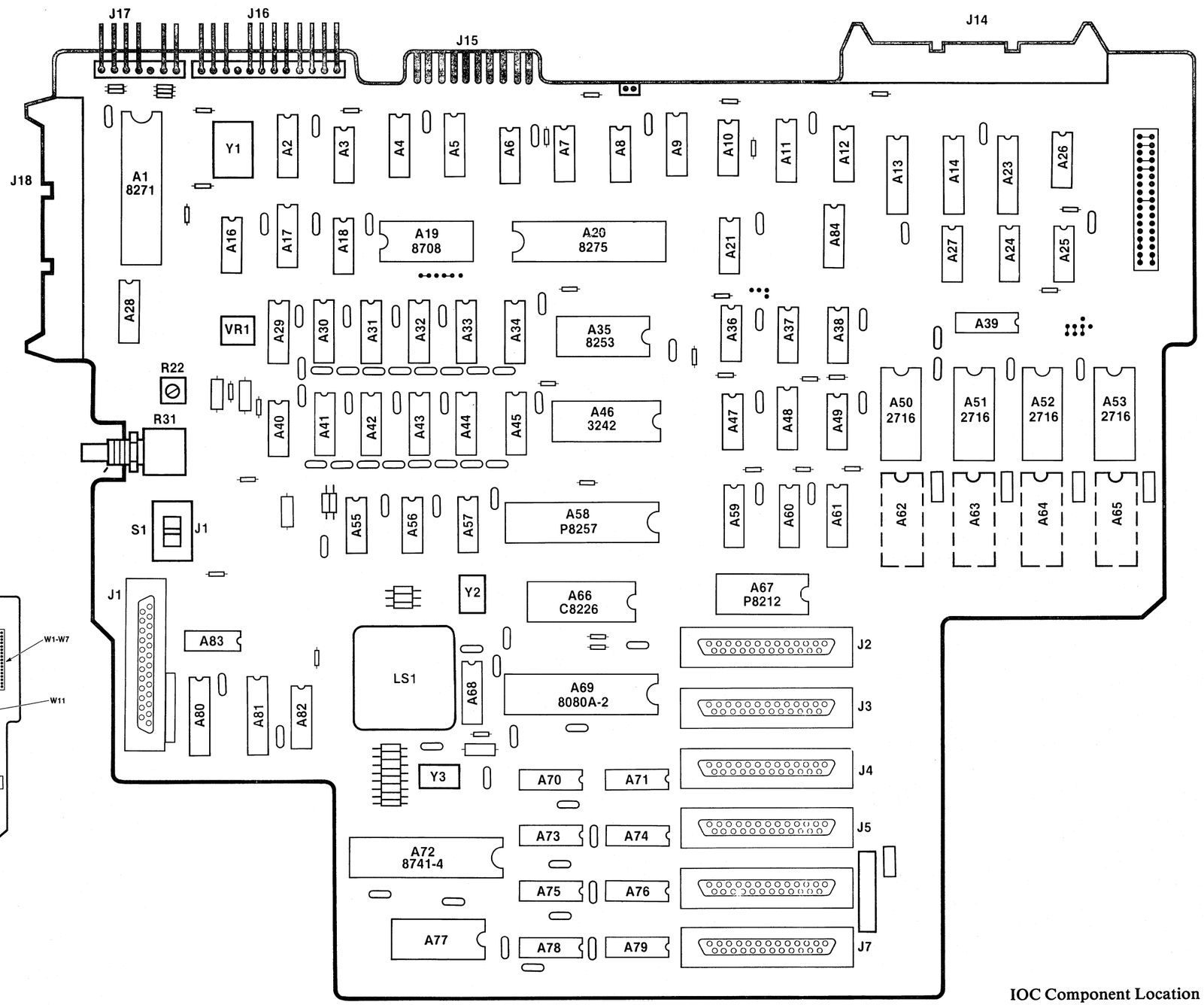




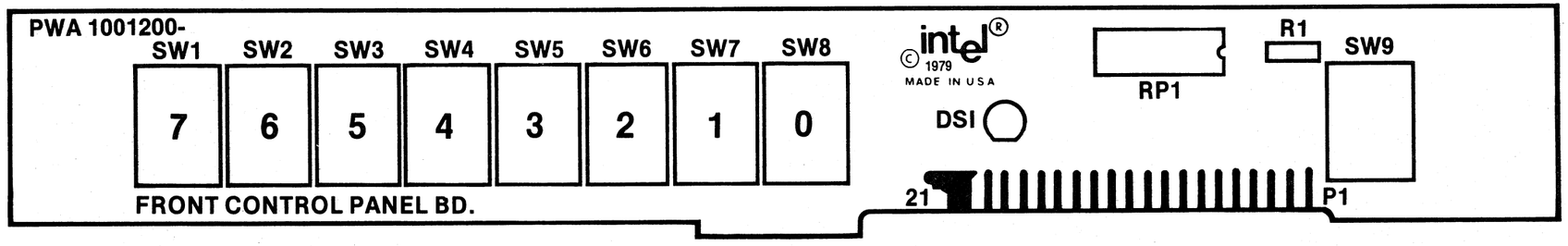
IPB Component Location

JUMPER LOCATIONS

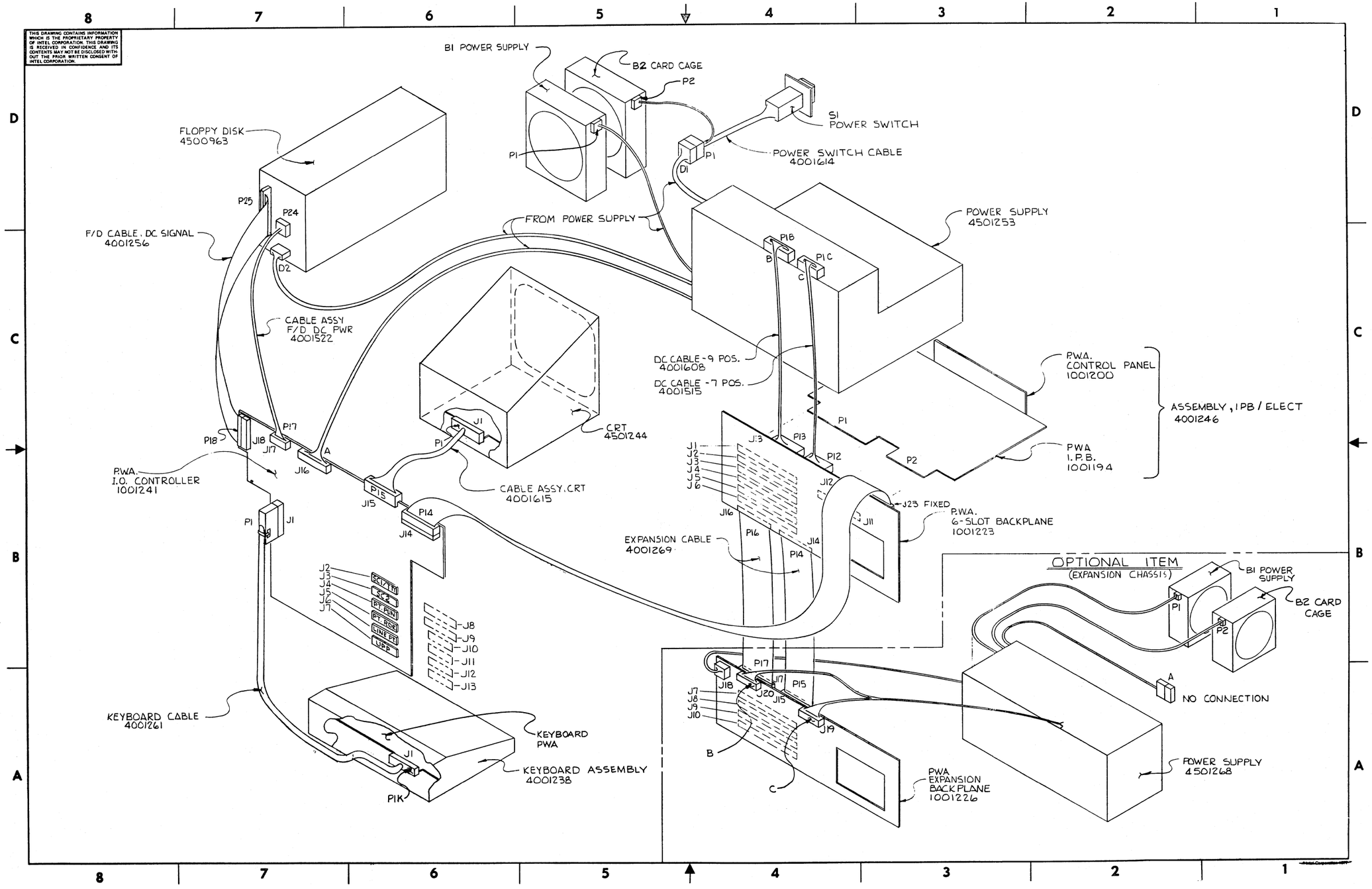




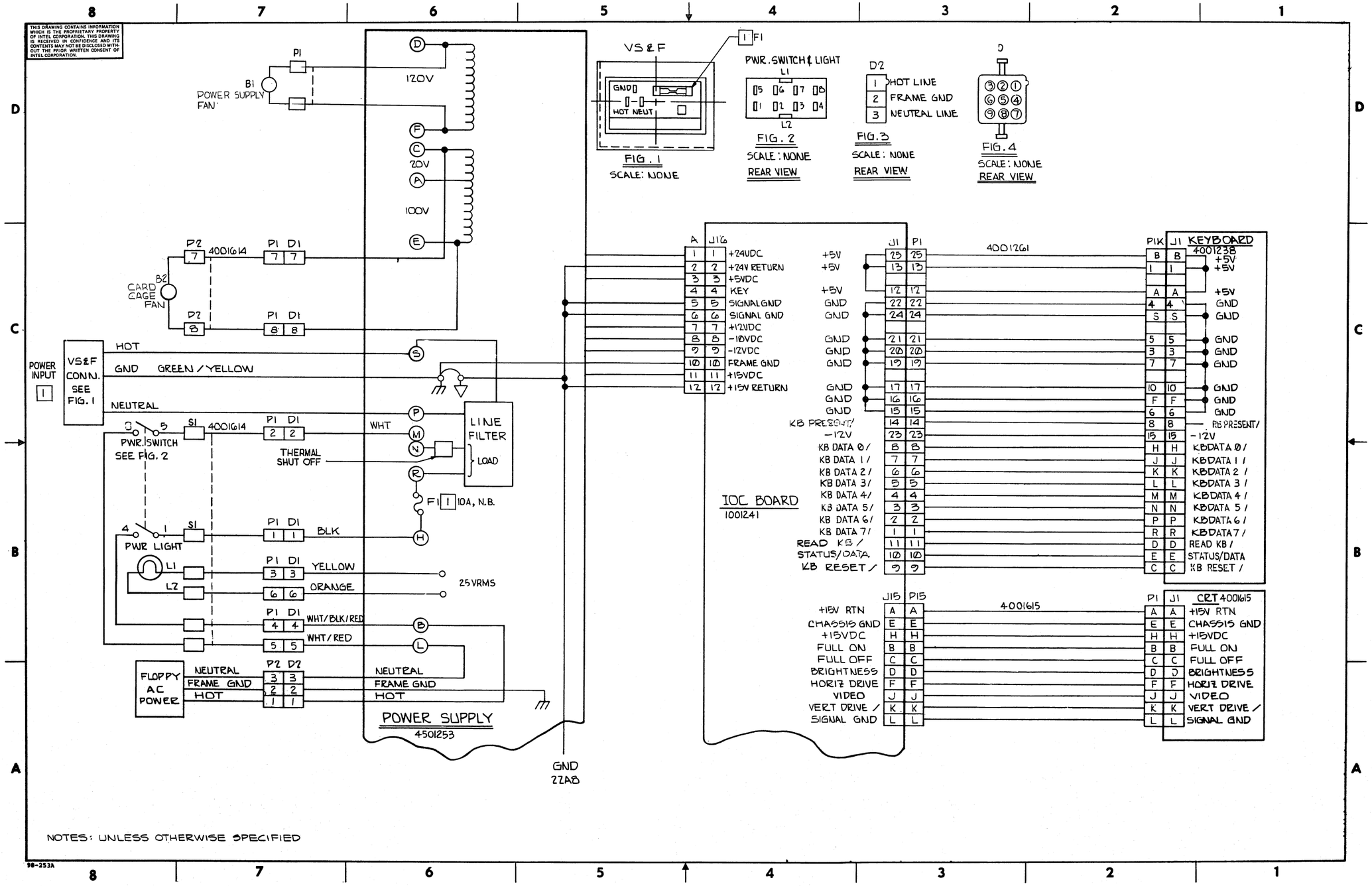
IOC Component Location



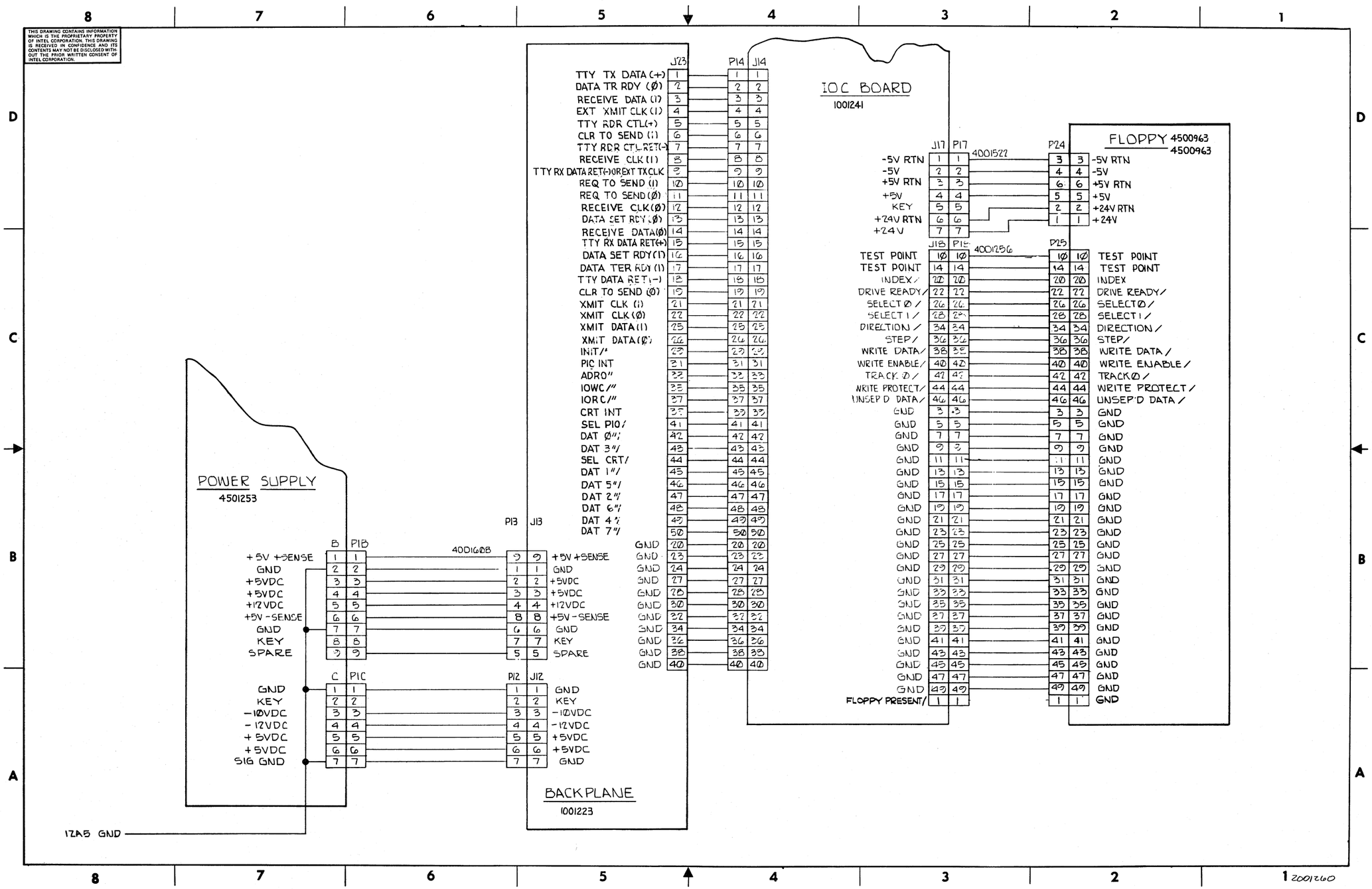
Front Panel Component Location



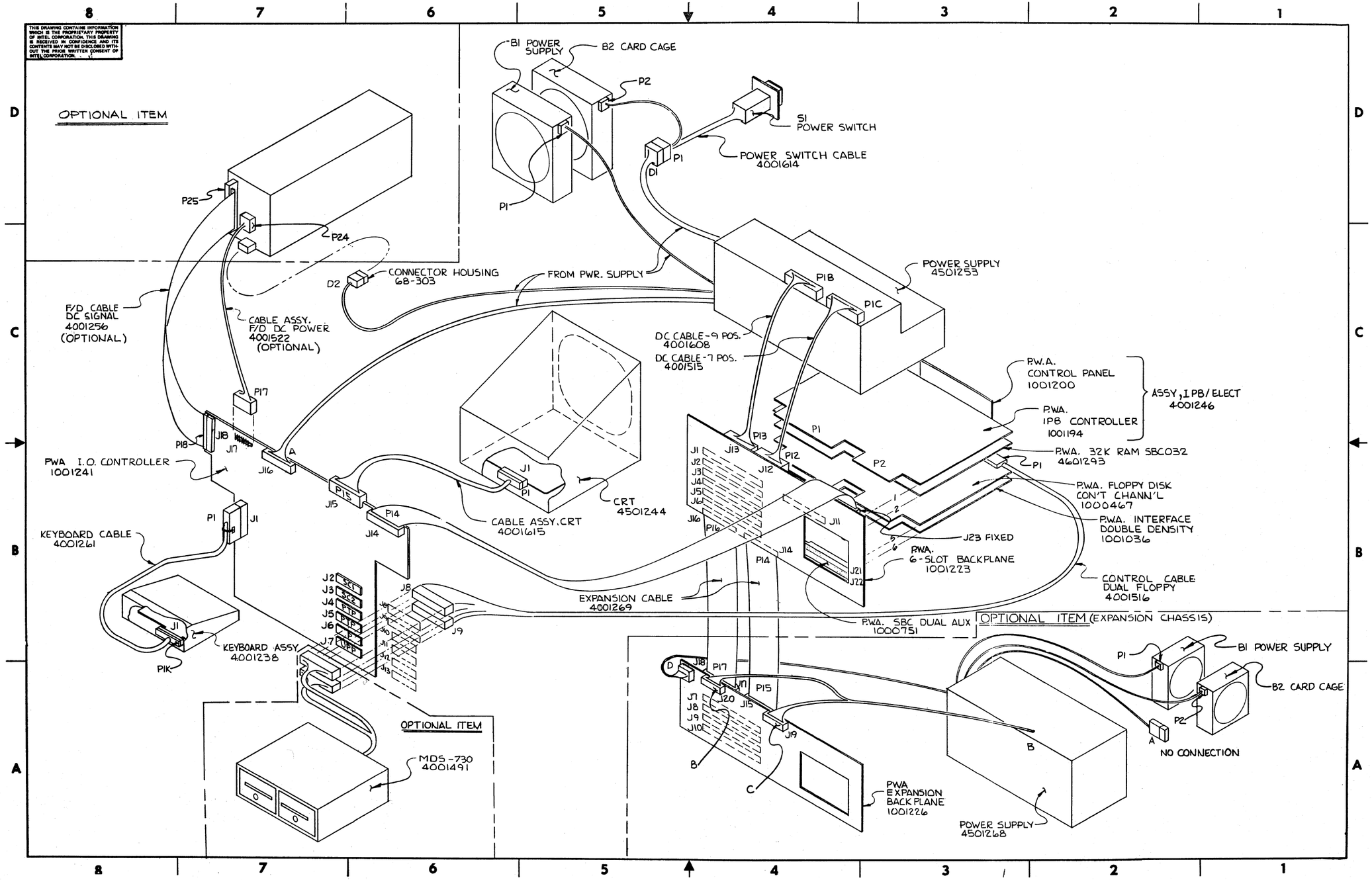
Model 22X Interconnection Diagram (Sheet 1 of 3)



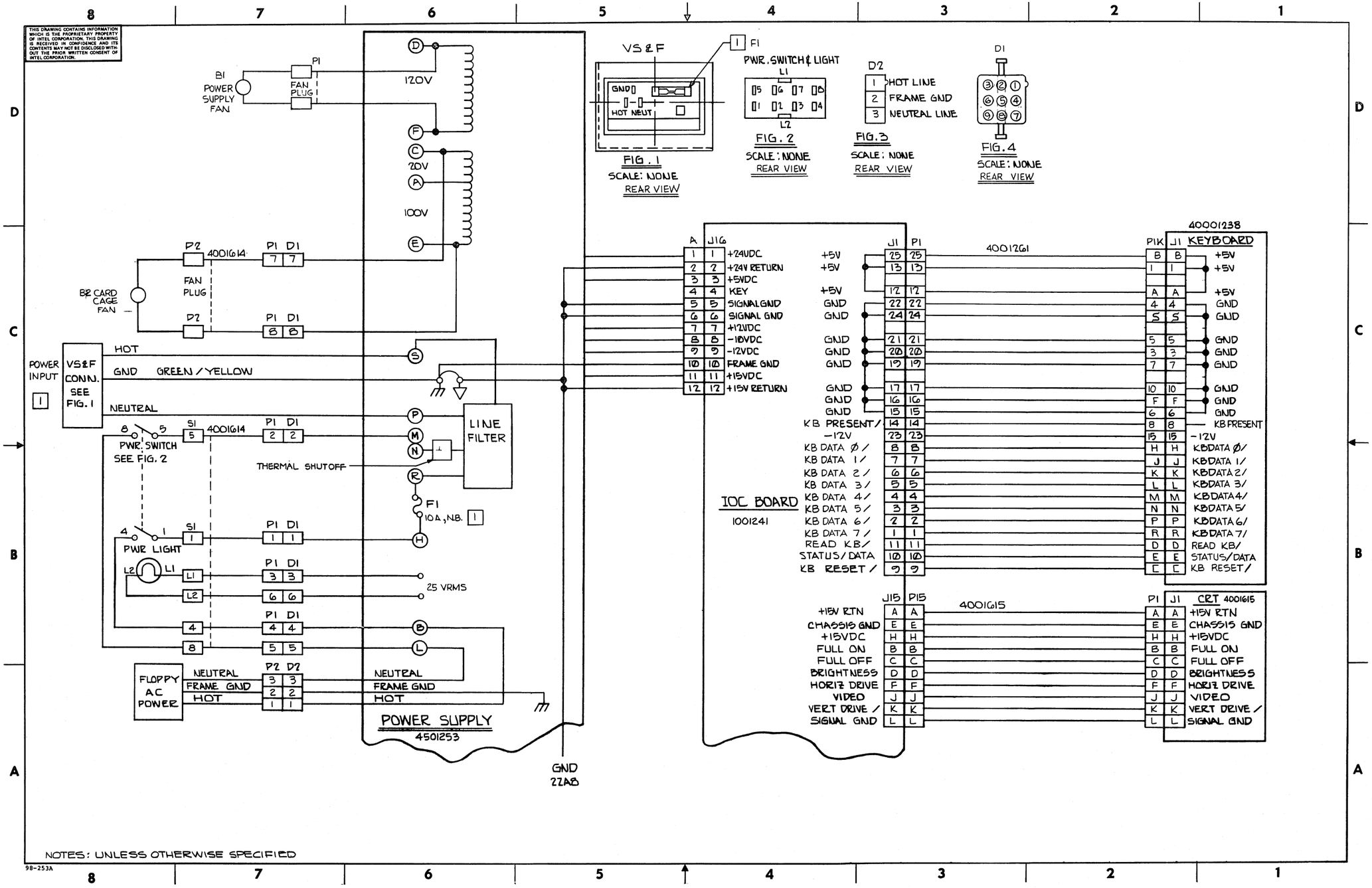
Model 22X Interconnection Diagram (Sheet 2 of 3)



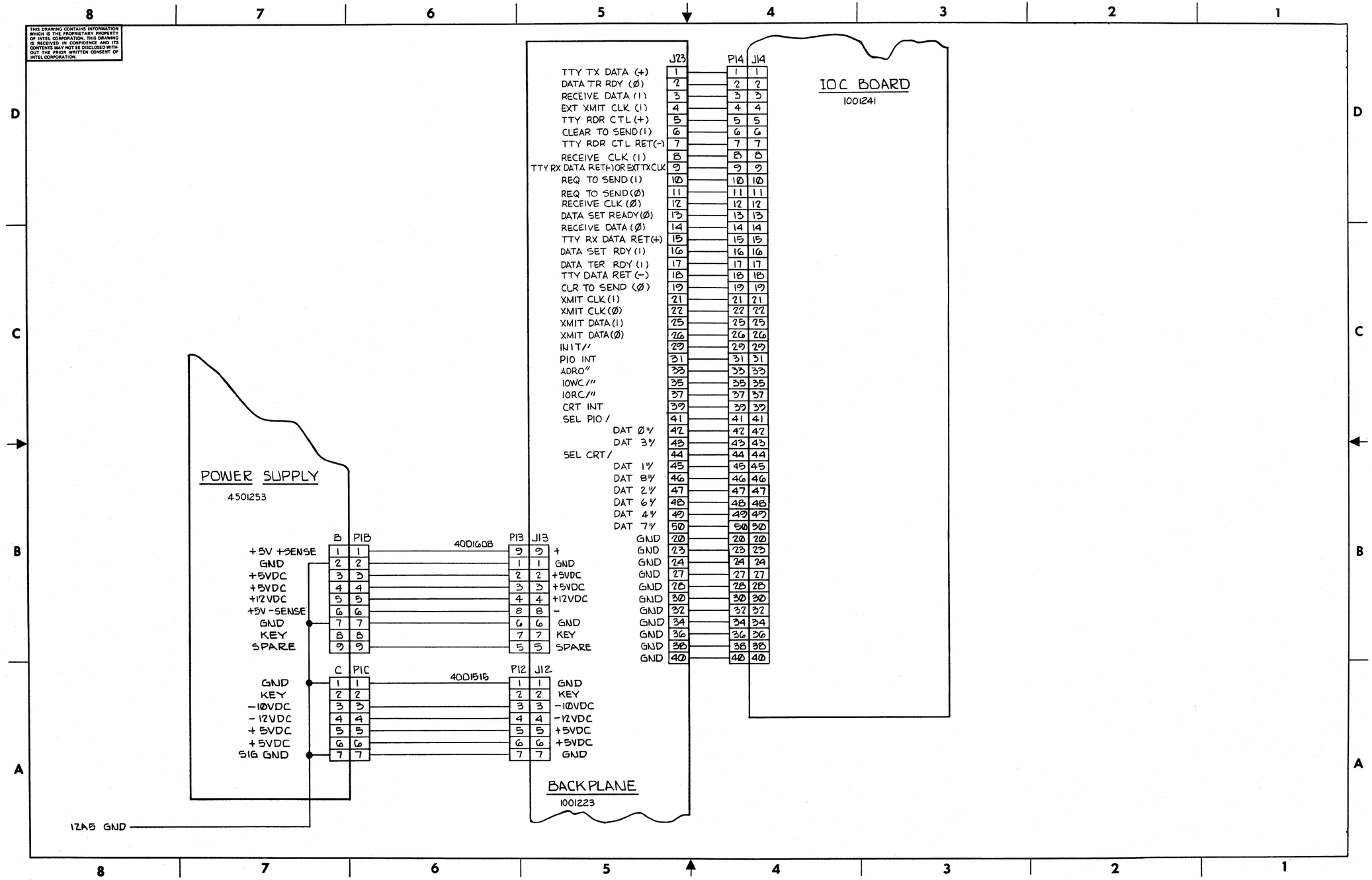
Model 22X Interconnection Diagram (Sheet 3 of 3)



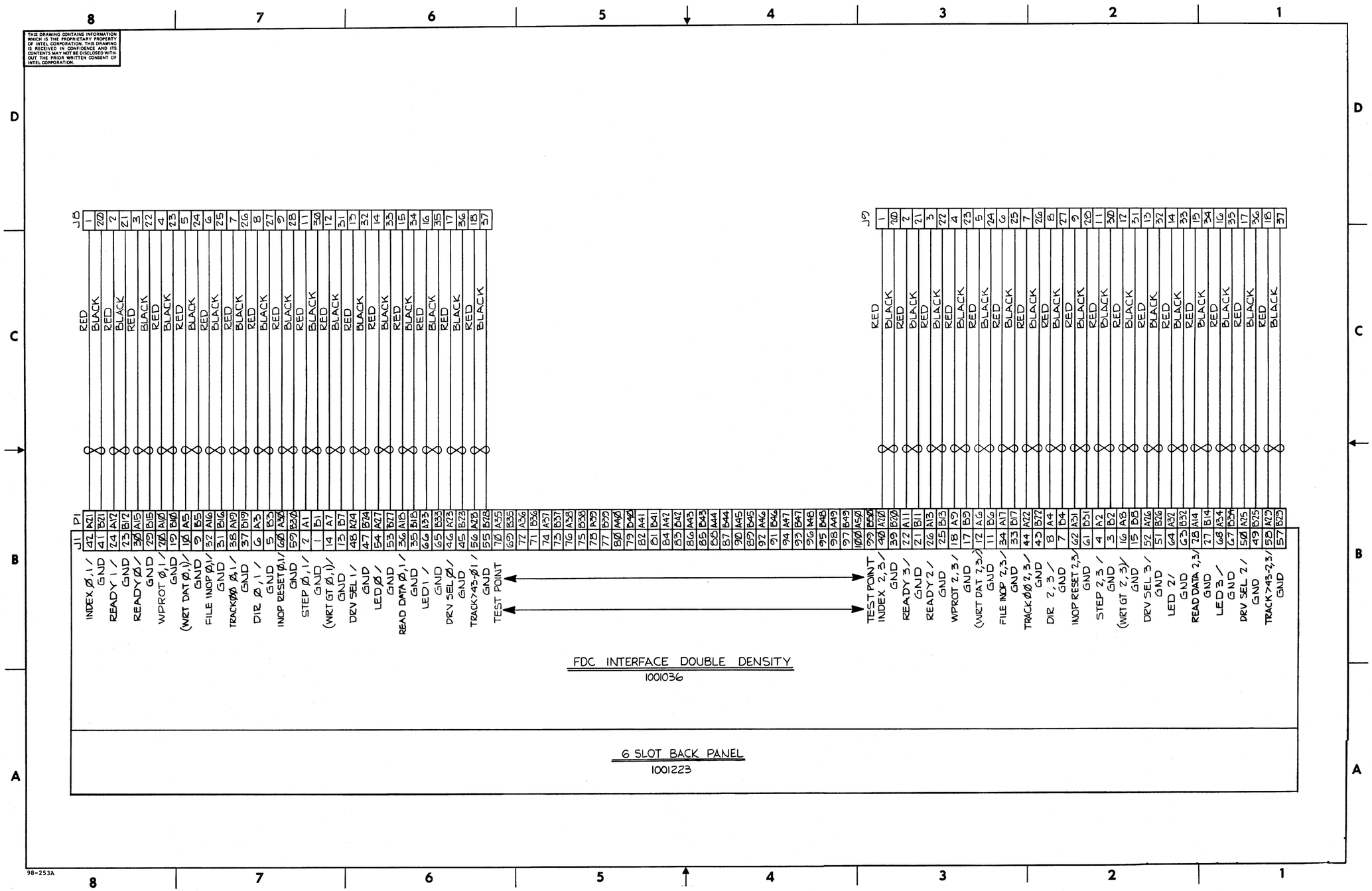
Model 23X Interconnection Diagram (Sheet 1 of 4)



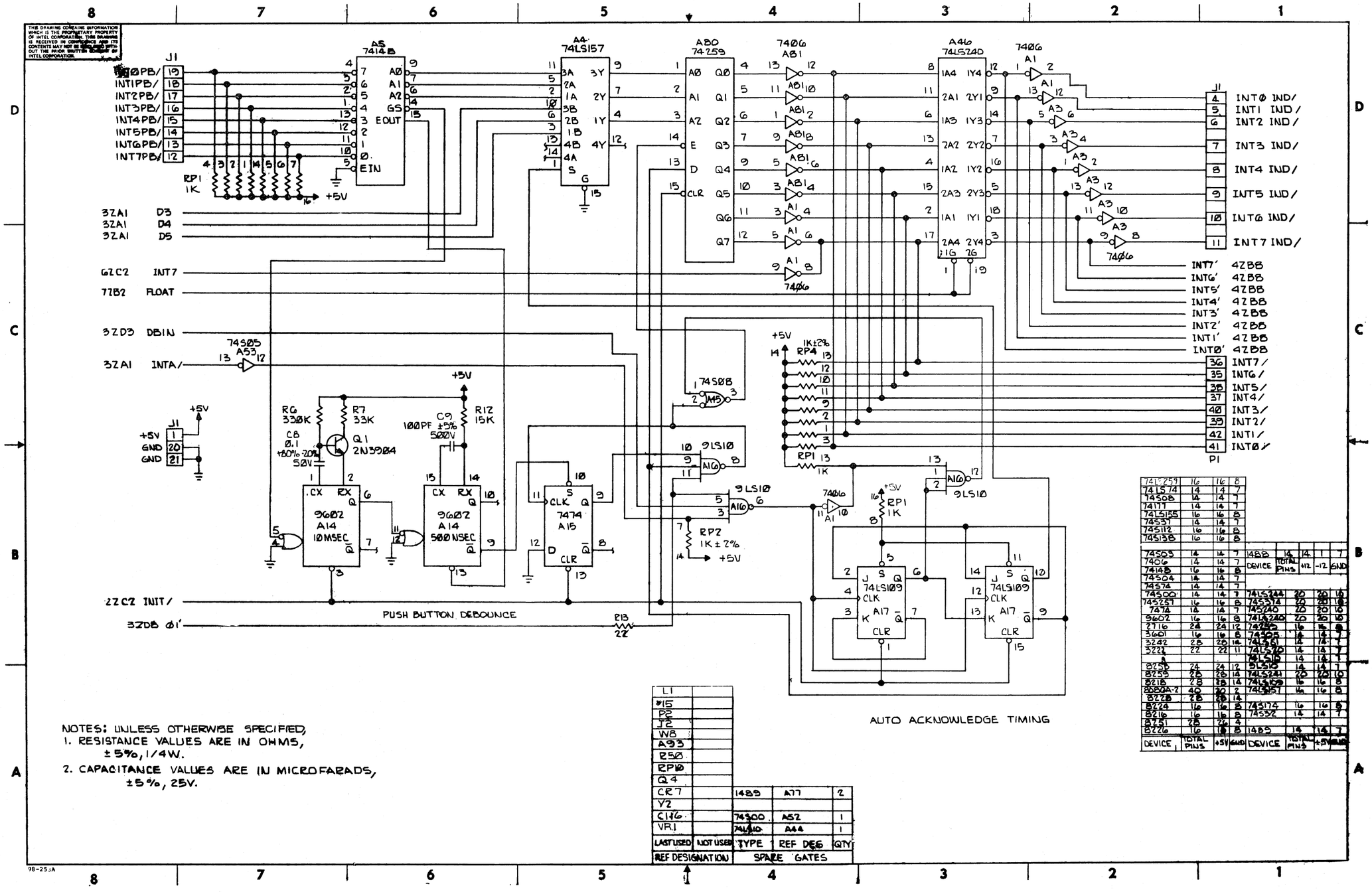
Model 23X Interconnection Diagram (Sheet 2 of 4)



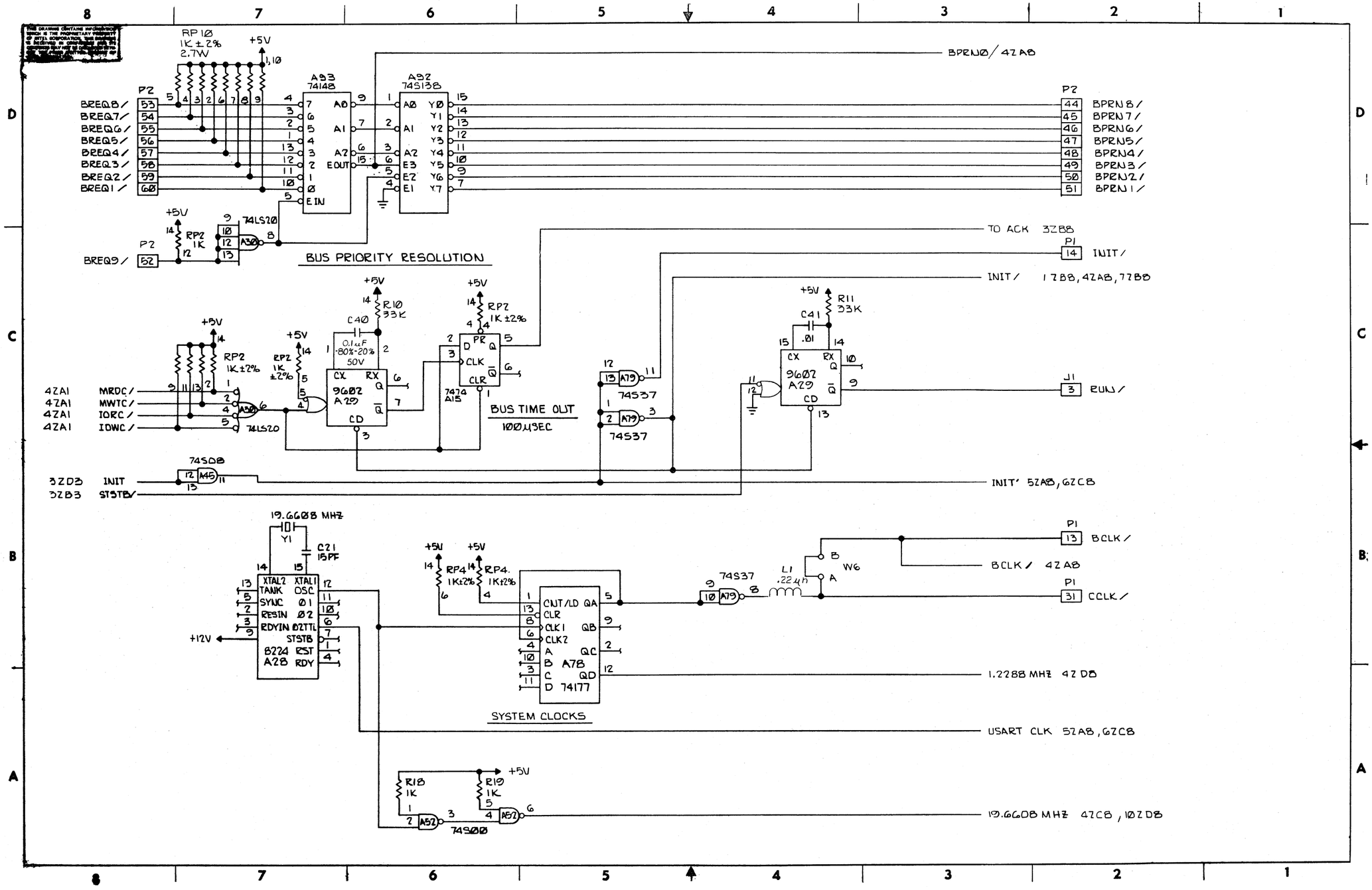
Model 23X Interconnection Diagram (Sheet 3 of 4)



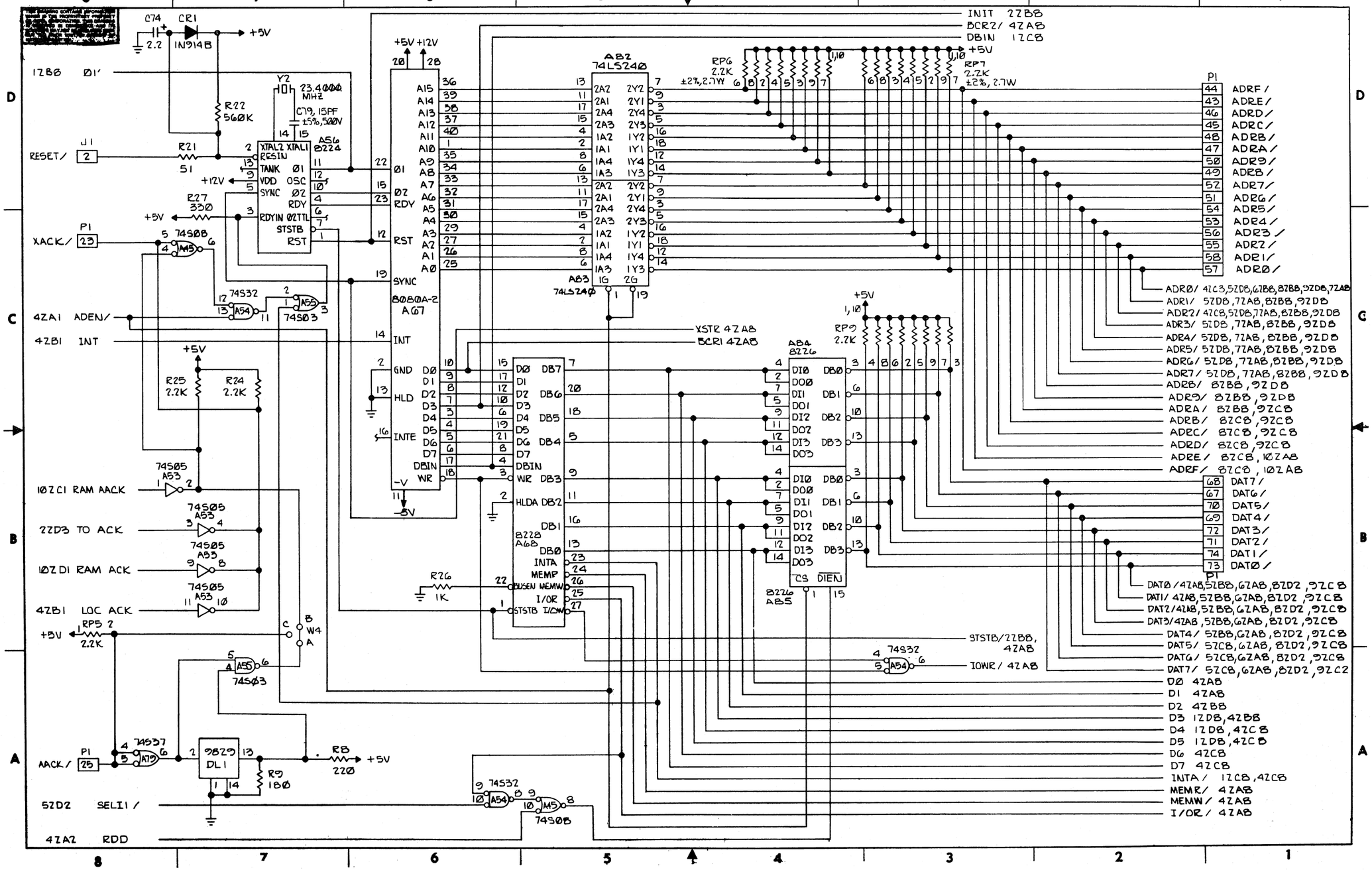
Model 23X Interconnection Diagram (Sheet 4 of 4)



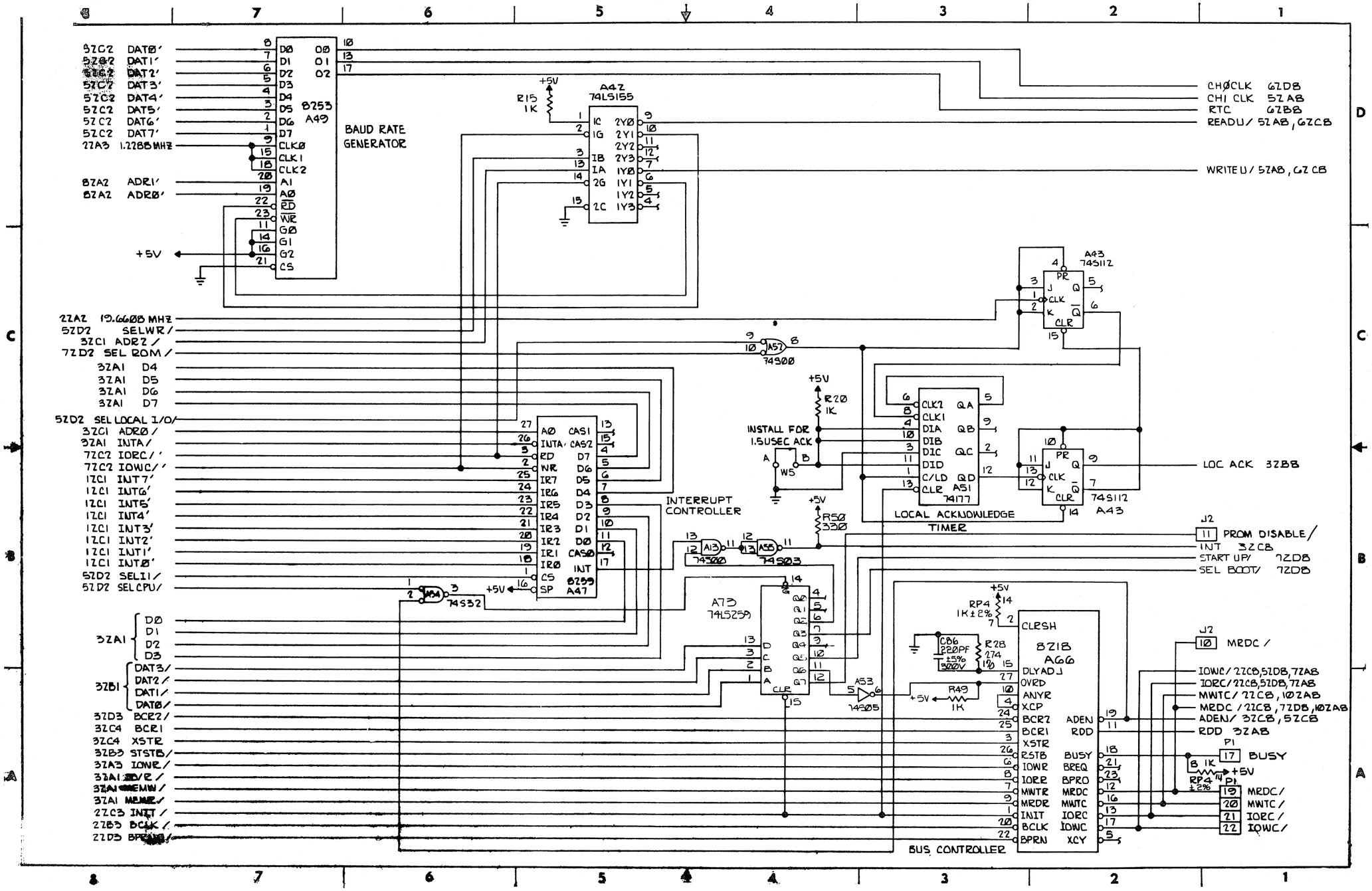
IPB Schematic (Sheet 1 of 10)



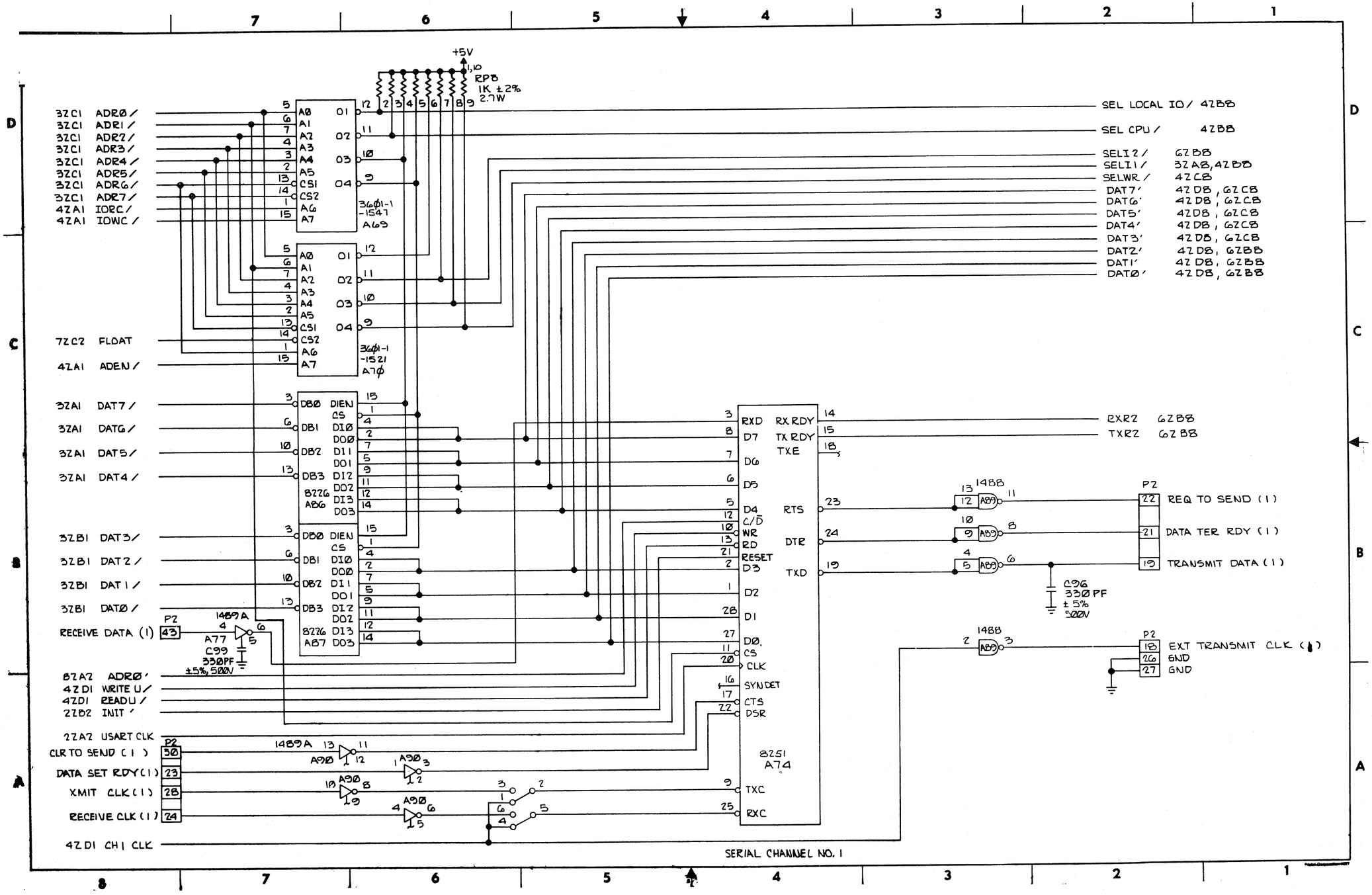
IPB Schematic (Sheet 2 of 10)



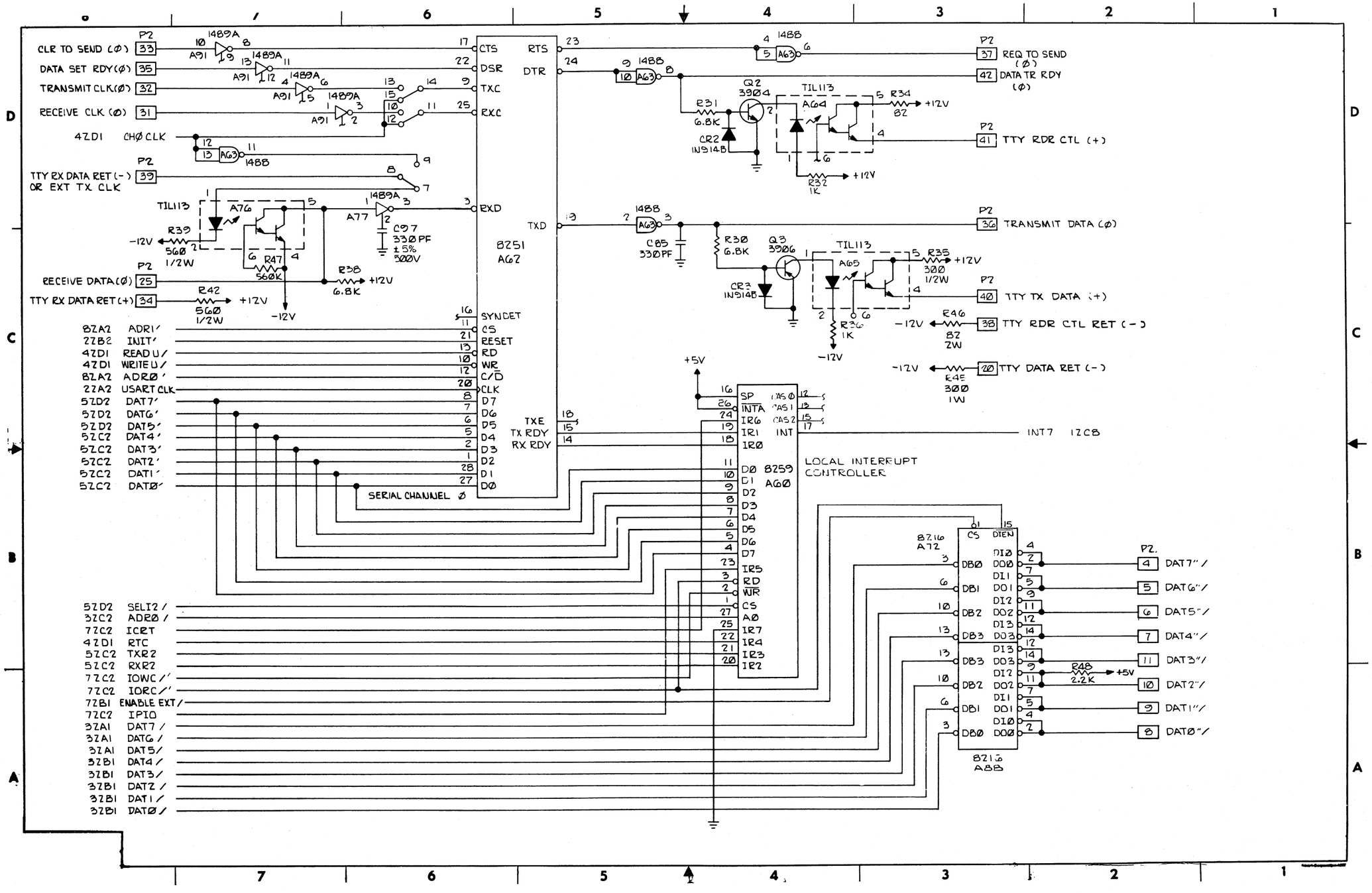
IPB Schematic (Sheet 3 of 10)



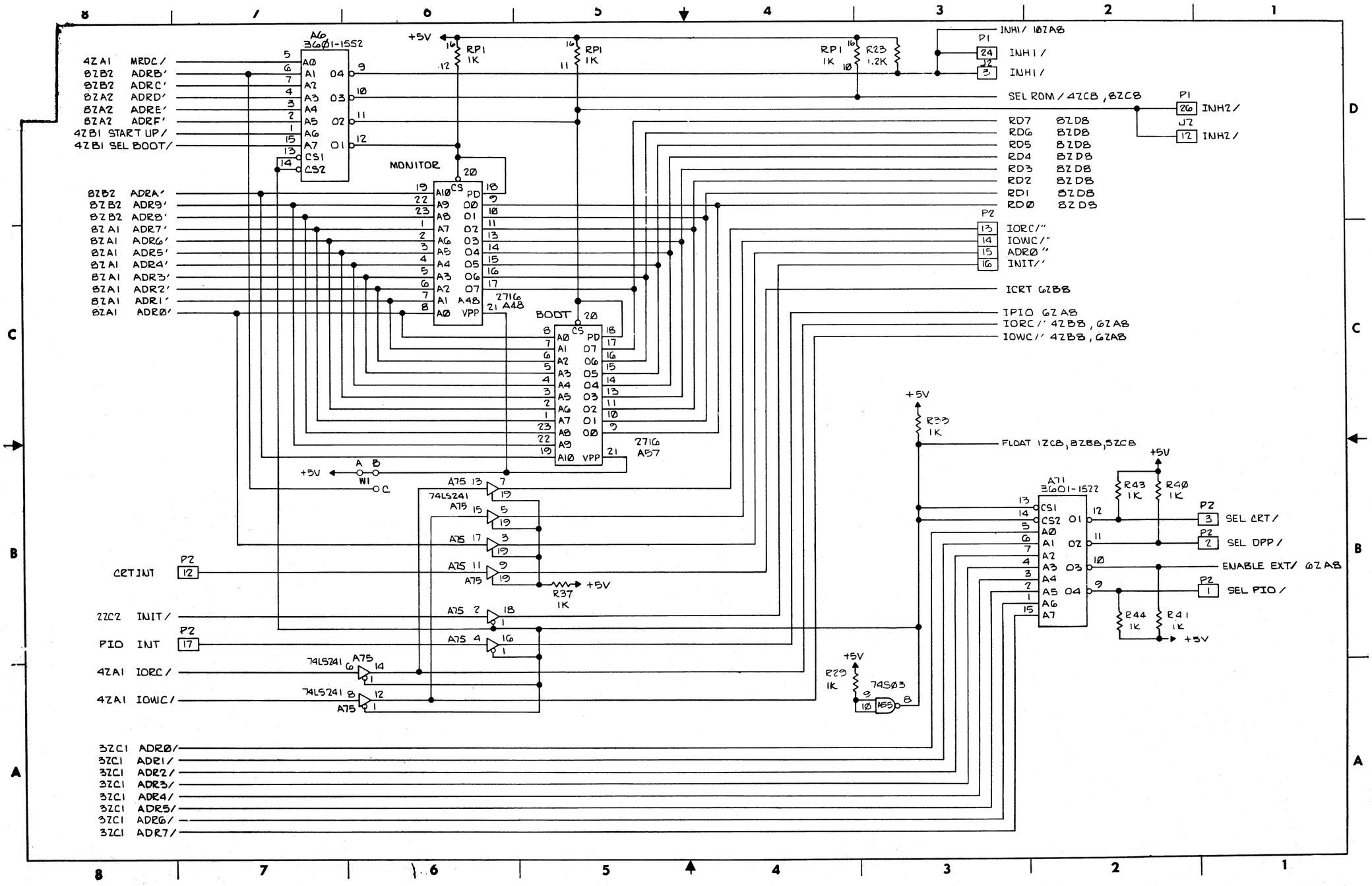
IPB Schematic (Sheet 4 of 10)



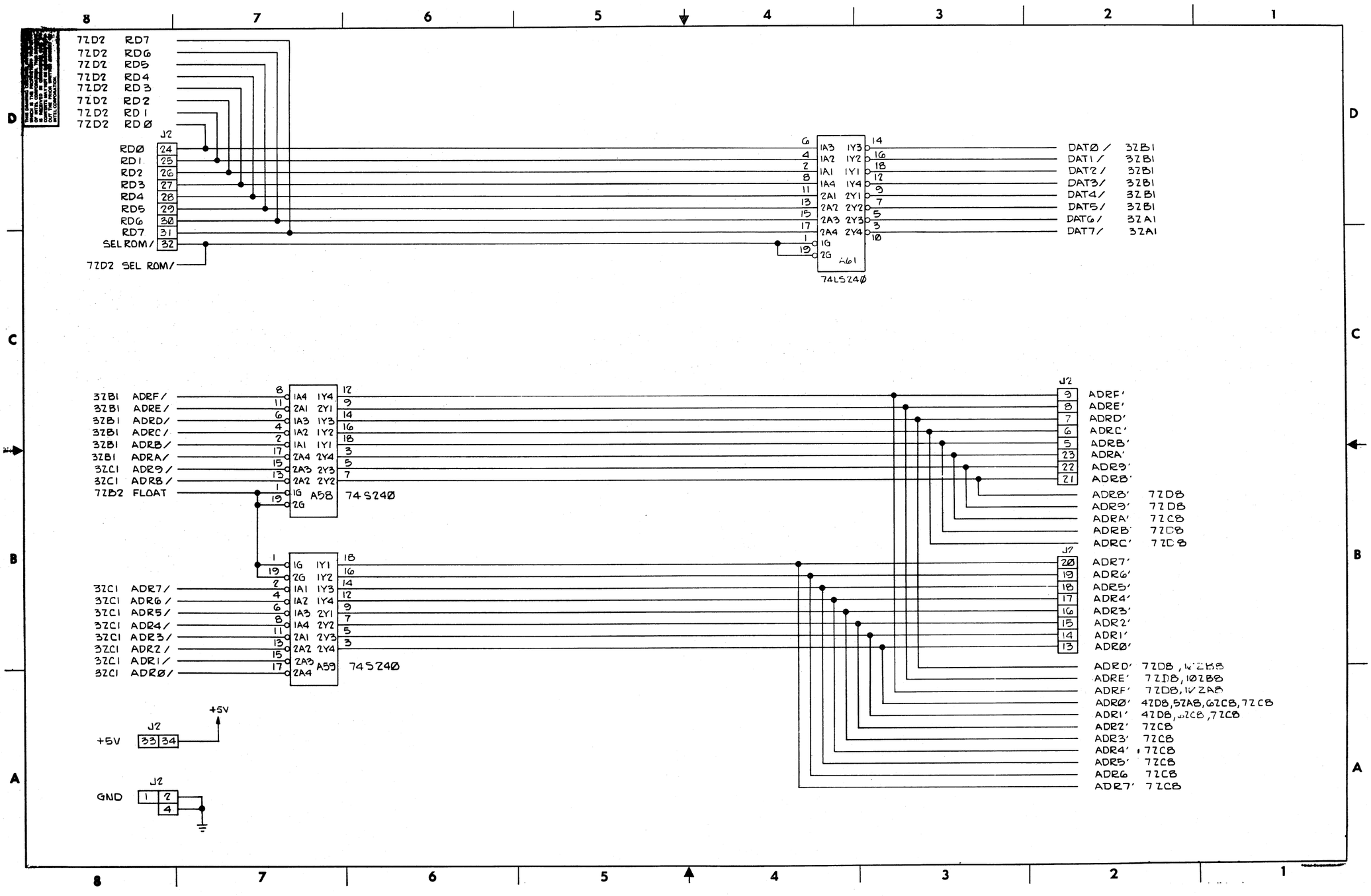
IPB Schematic (Sheet 5 of 10)



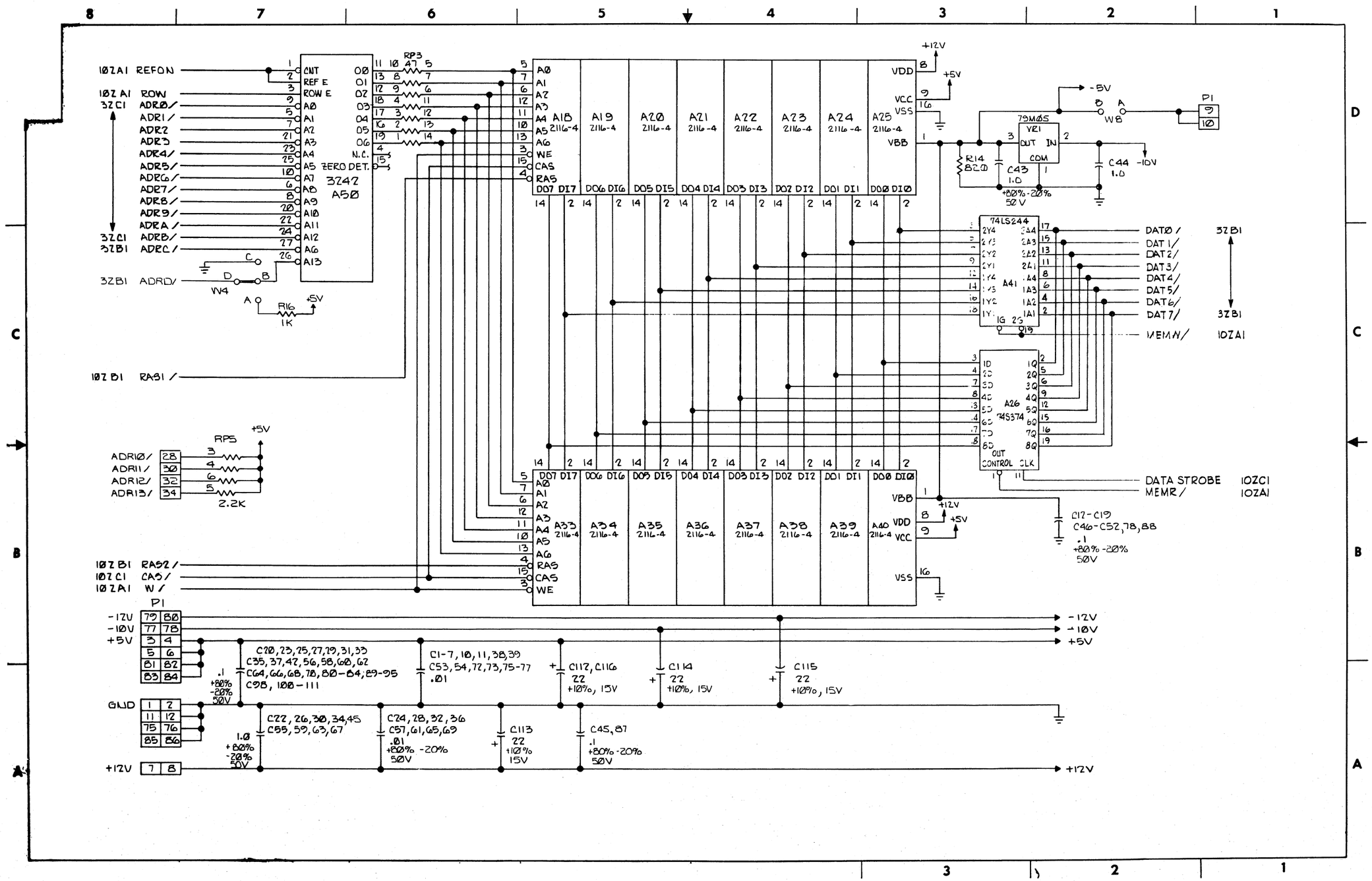
IPB Schematic (Sheet 6 of 10)



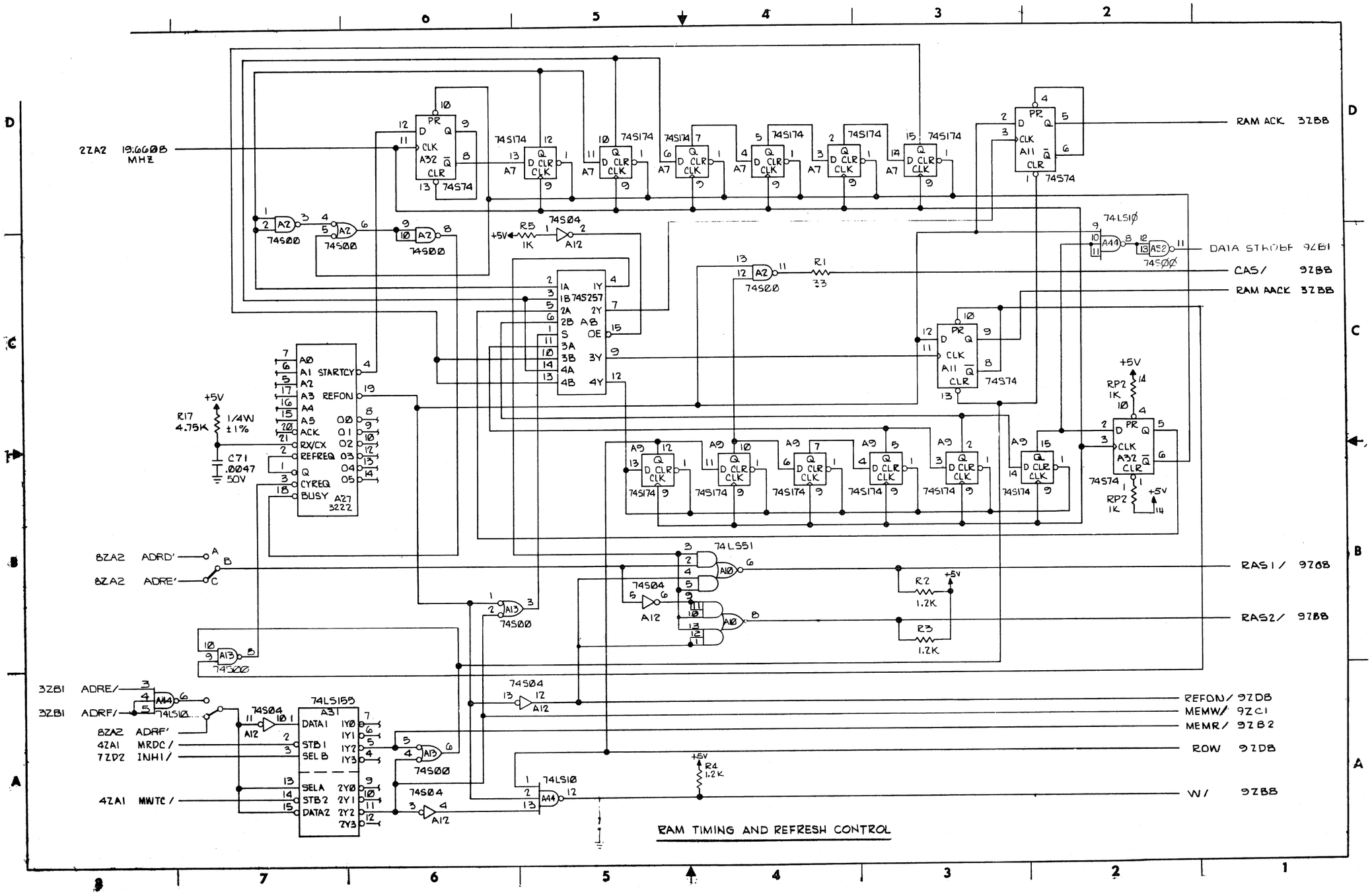
IPB Schematic (Sheet 7 of 10)



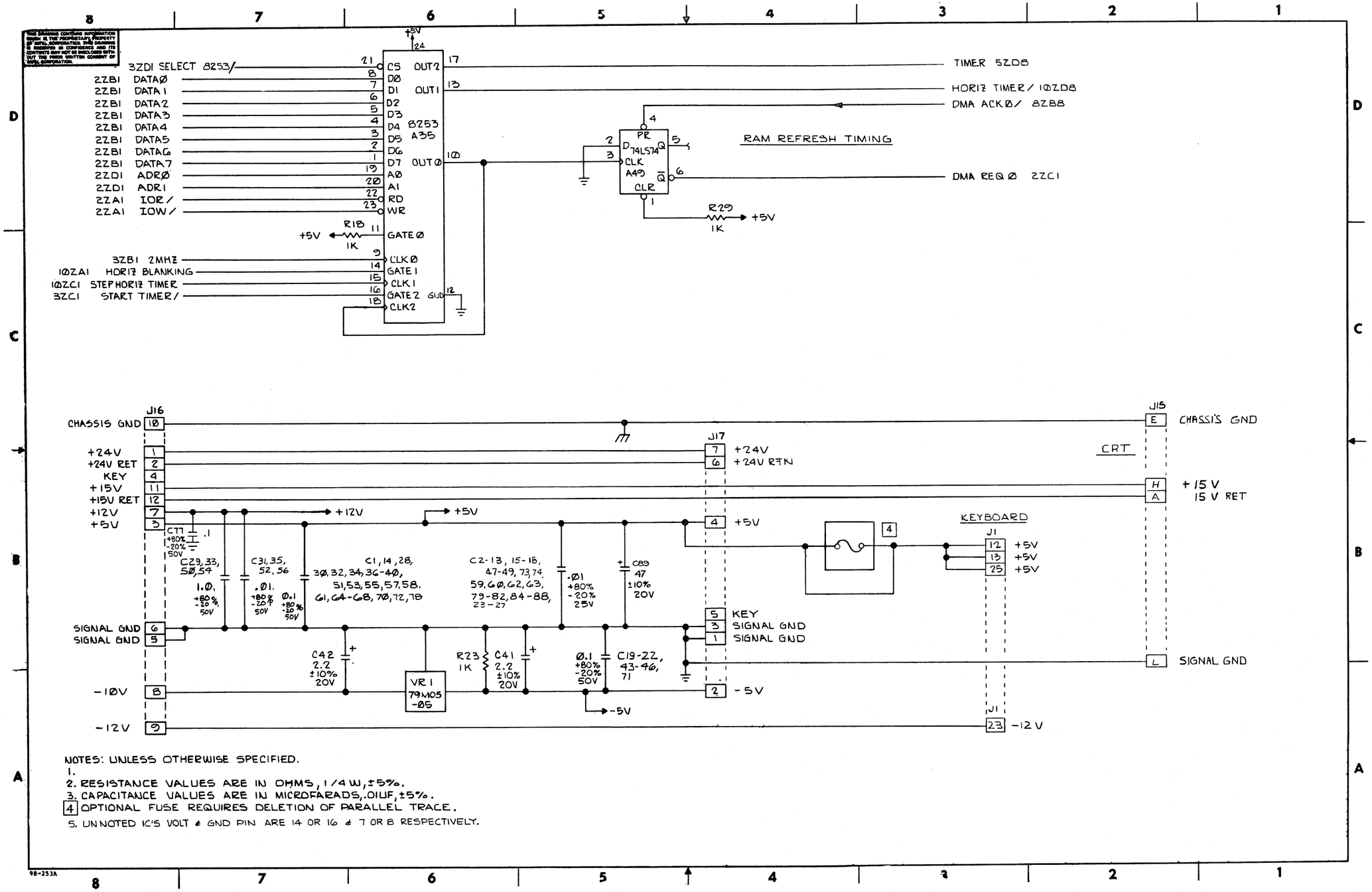
IPB Schematic (Sheet 8 of 10)



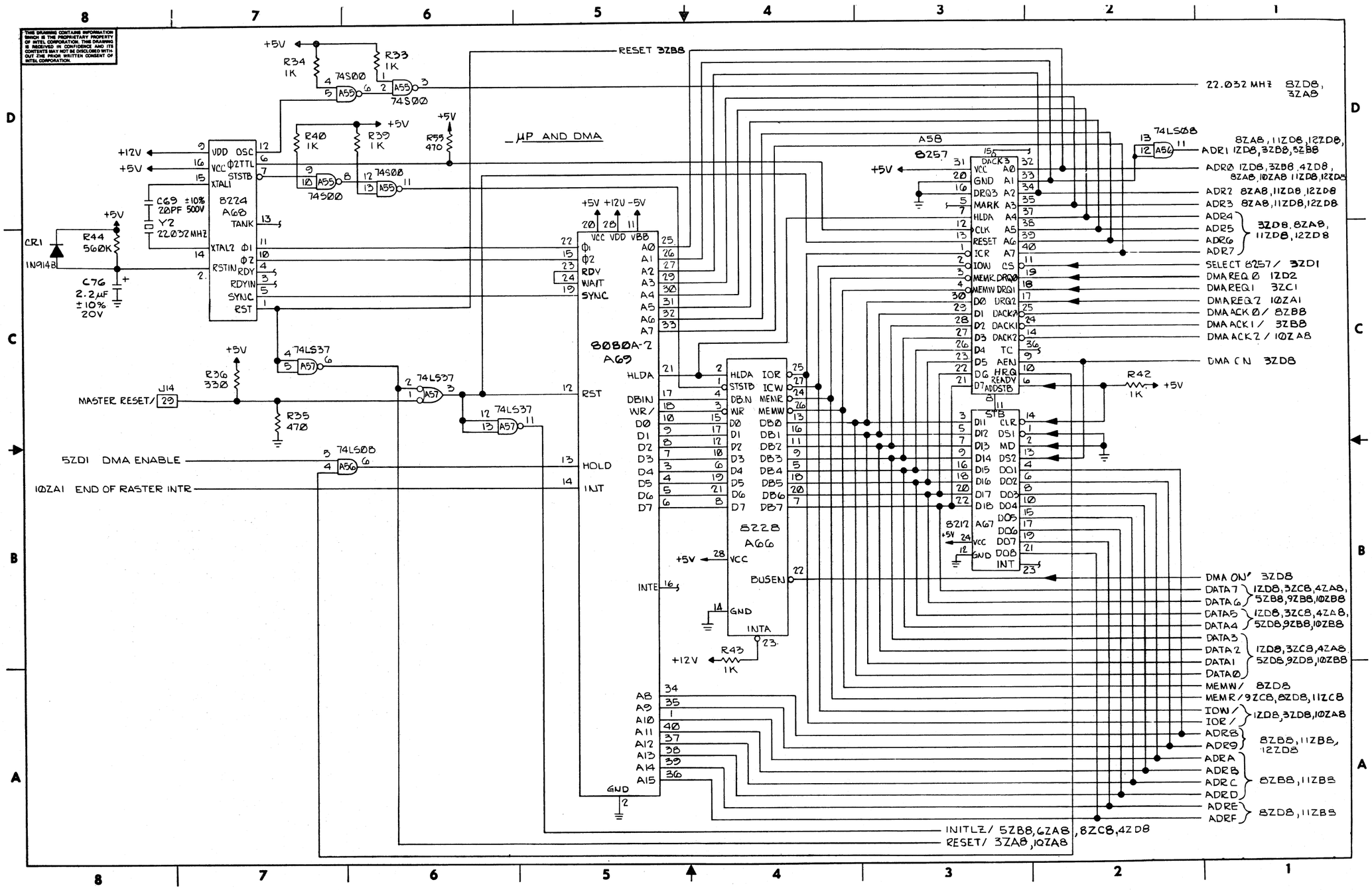
IPB Schematic (Sheet 9 of 10)



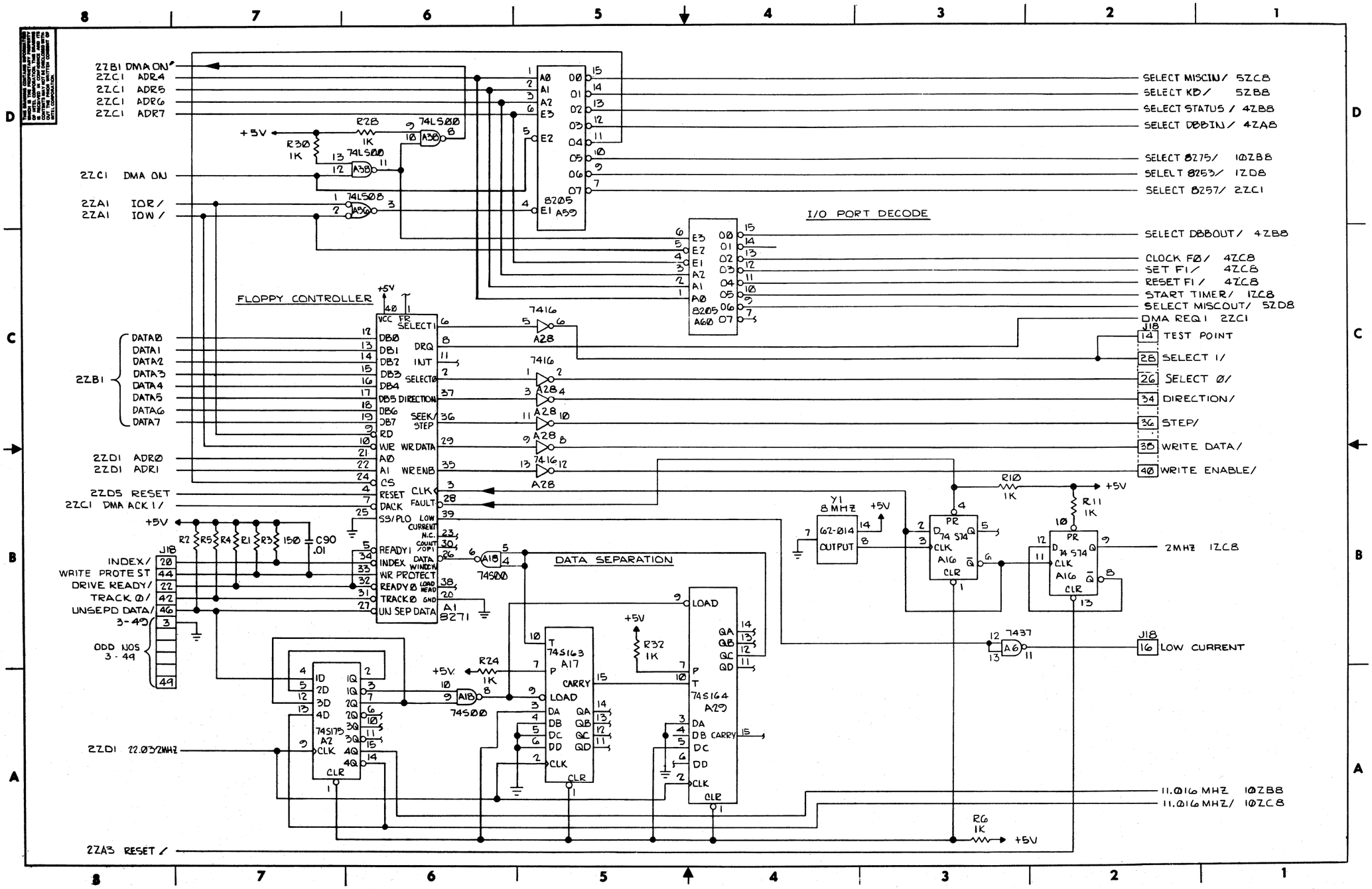
IPB Schematic (Sheet 10 of 10)



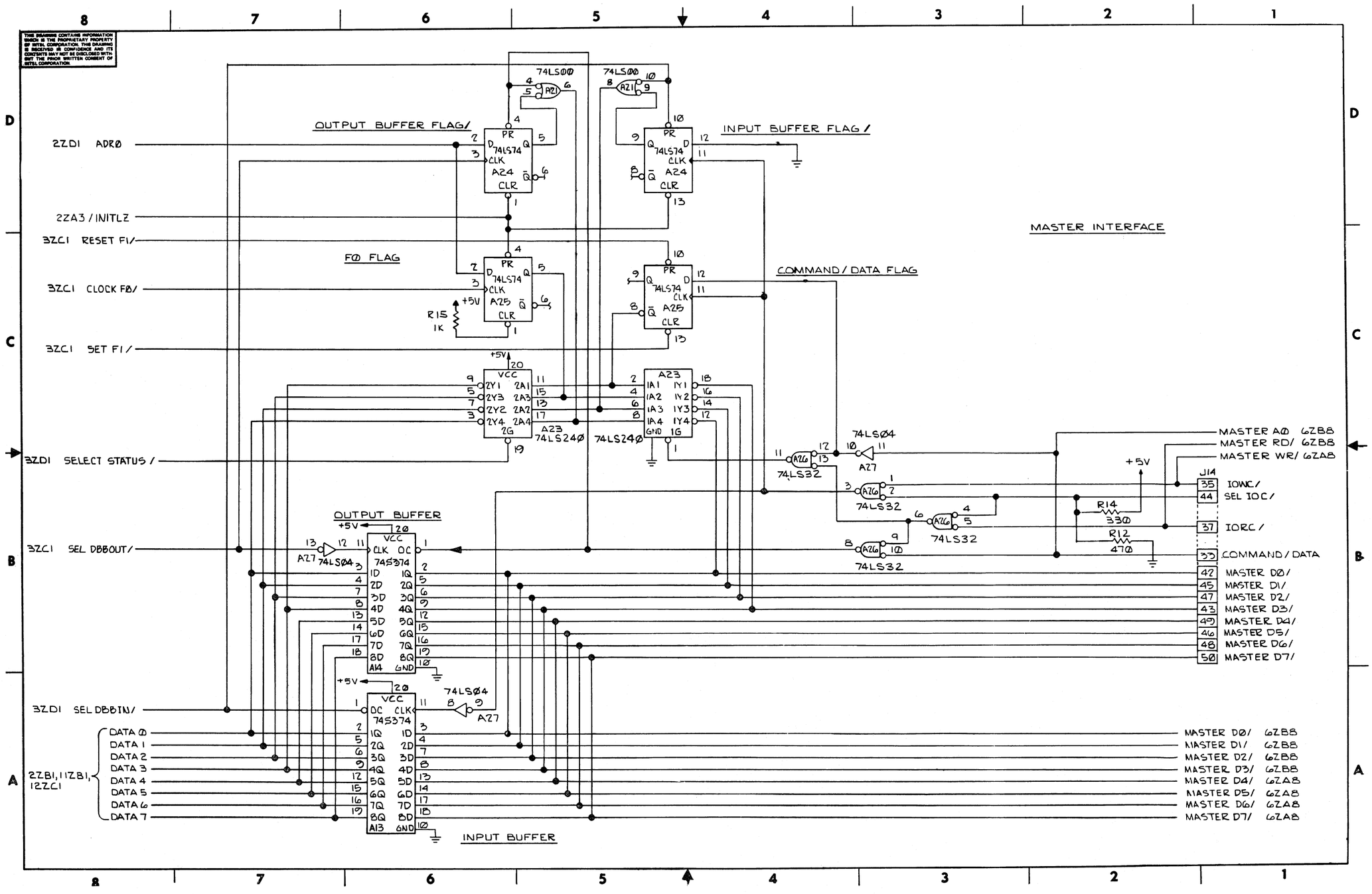
IOC Schematic (Sheet 1 of 12)



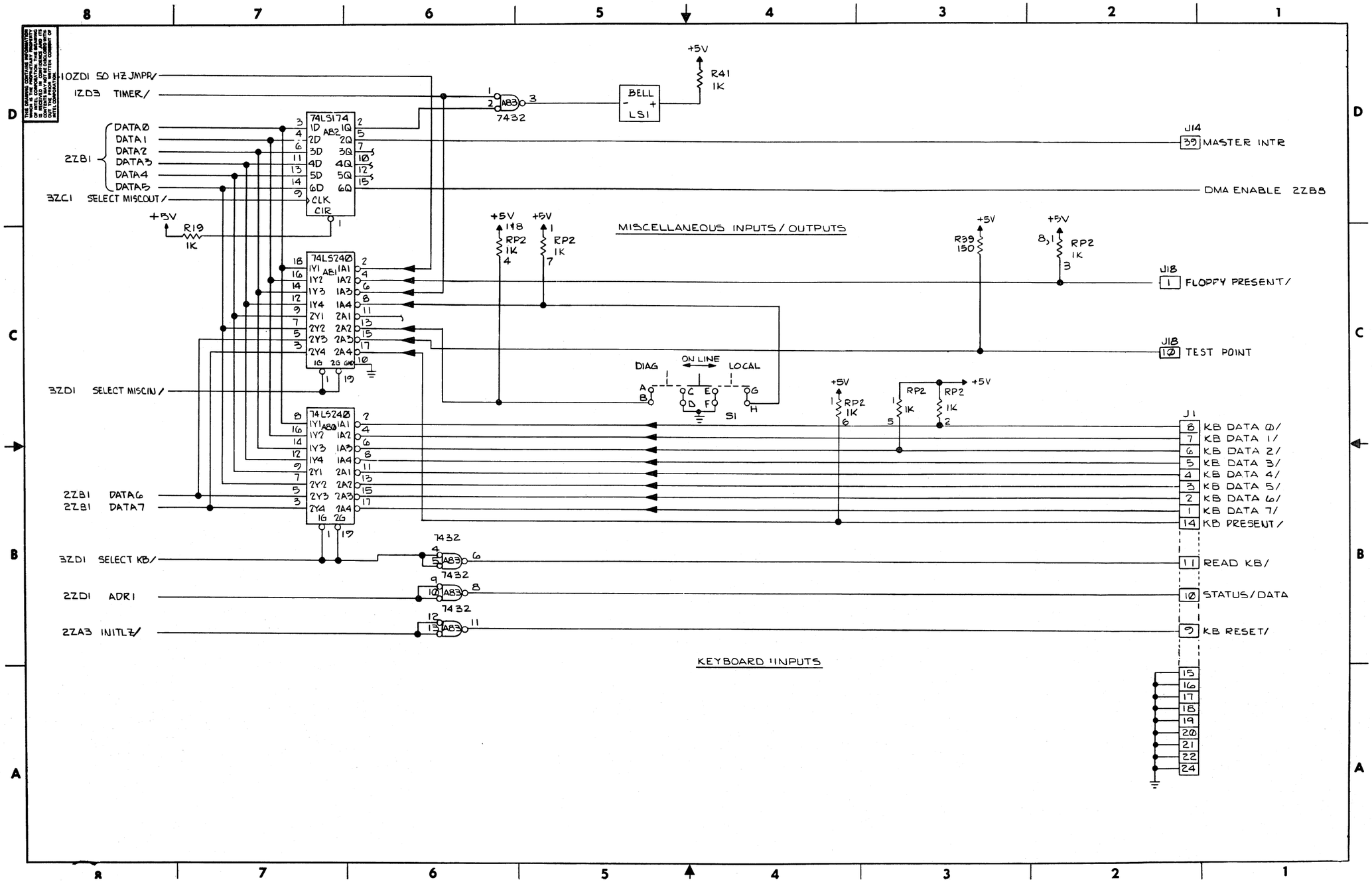
IOC Schematic (Sheet 2 of 12)



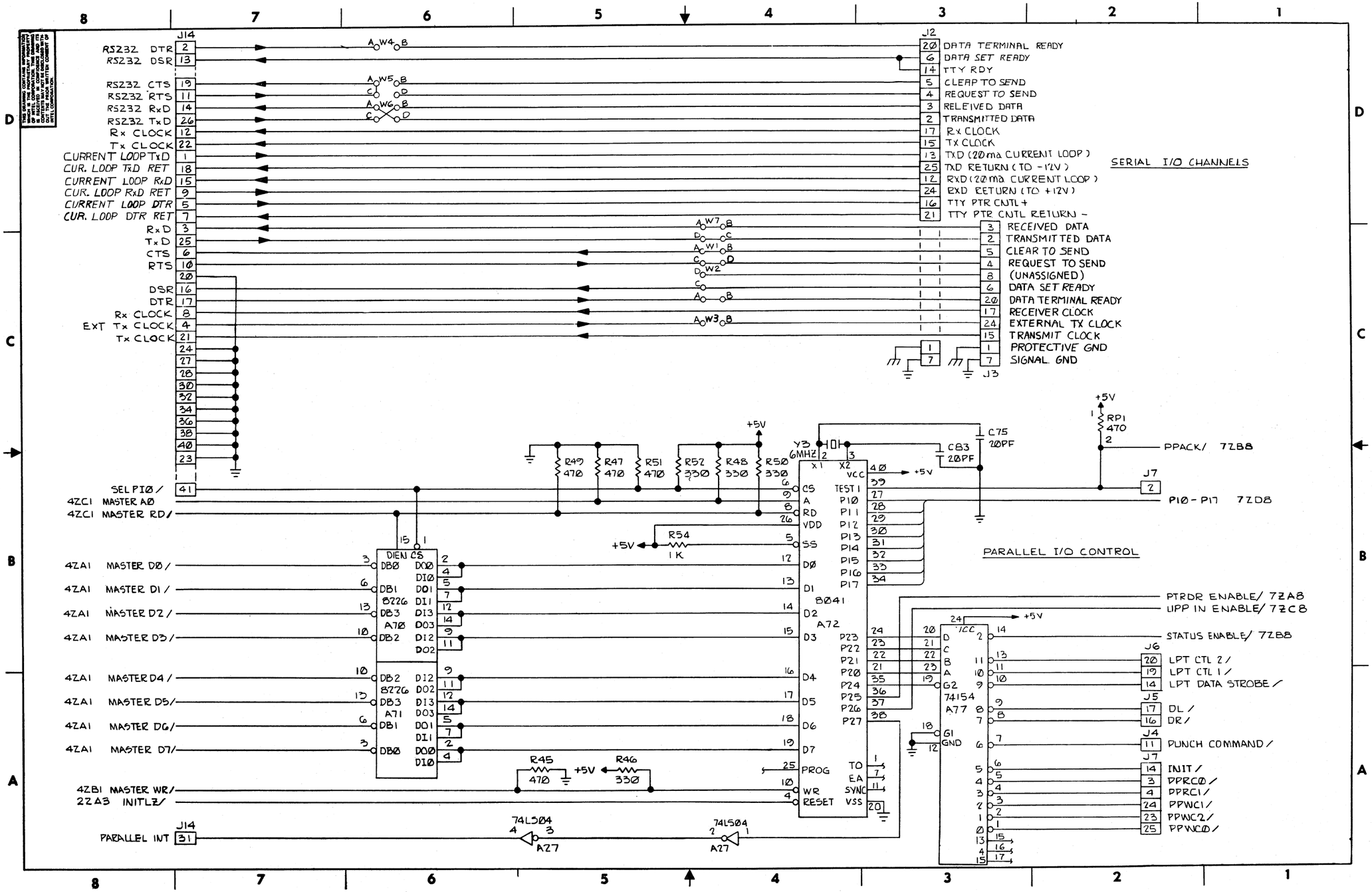
IOC Schematic (Sheet 3 of 12)



IOC Schematic (Sheet 4 of 12)



IOC Schematic (Sheet 5 of 12)



IOC Schematic (Sheet 6 of 12)

PARALLEL I/O

6ZB1 P1Ø–P17

8226 A78 — A79 8226 — A75 — A76 8226

6ZB1 UPP IN ENABLE/

6ZB1 STATUS ENABLE/

6ZC1 PPACK/

6ZB1 PTRDR ENABLE/

8226 A73 — A74 8226

J7
22 PWDØ/
12 PRDØ/
21 PWD1/
1 GND
13 GND

J6
9 GND
10 GND
11 GND
12 GND
15 GND
25 CHASSIS GND

PAPER TAPE READER J8
1 DATA TRACK 1/
2 DATA TRACK 2/
3 DATA TRACK 3/
4 DATA TRACK 4/
5 DATA TRACK 5/
6 DATA TRACK 6/
7 DATA TRACK 7/
8 DATA TRACK 8/

PAPER TAPE PUNCH J4
1 DATA TRACK 1/
2 DATA TRACK 2/
3 DATA TRACK 3/
4 DATA TRACK 4/
5 DATA TRACK 5/
6 DATA TRACK 6/
7 DATA TRACK 7/
8 DATA TRACK 8/

PROM PROGRAMMER J7
11 PRD1/
20 PWD2/
10 PRD2/
19 PWD3/
9 PRD3/
18 PWD4/
8 PRD4/
17 PWD5/
7 PRD5/
16 PWD6/
6 PRD6/
15 PWD7/
5 PRD7/

J6
11 GND
12 GND
13 GND
24 GND
25 CHASSIS GND

R53 1K +5V
10 DIRECTION
14 INPUT MOVE SELECT
15 OUTPUT MOVE SELECT
18 GND
23 GND
25 GND
16 CHASSIS GND
17 CHASSIS GND

J6
1 DATA 1
2 DATA 2
3 DATA 3
4 DATA 4
5 DATA 5
6 DATA 6
7 DATA 7
8 DATA 8
LINE PRINTER

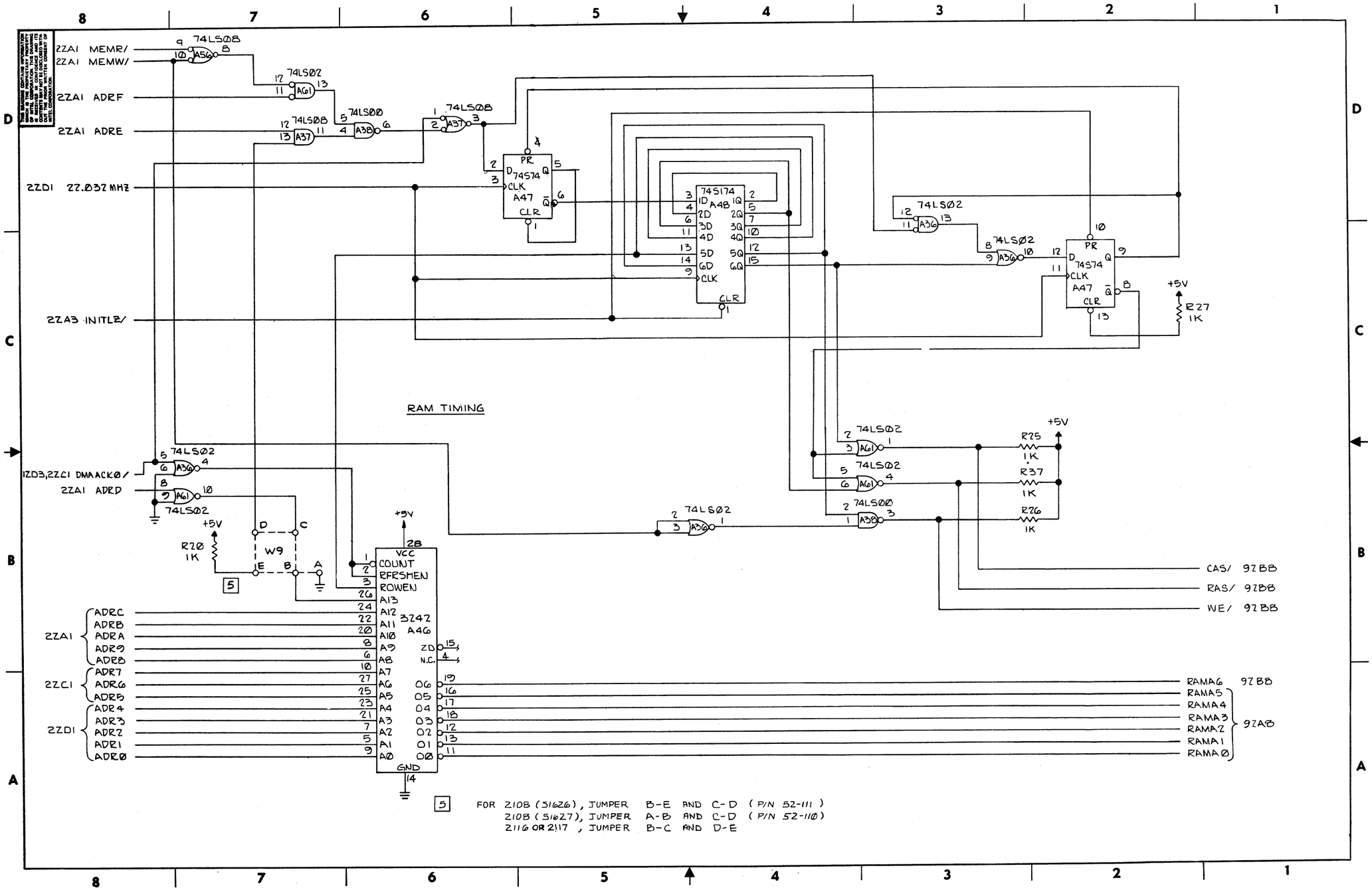
RPI 470Ø ×9 +5V

J4
12 PUNCH READY/
13 SYSTEMS READY/

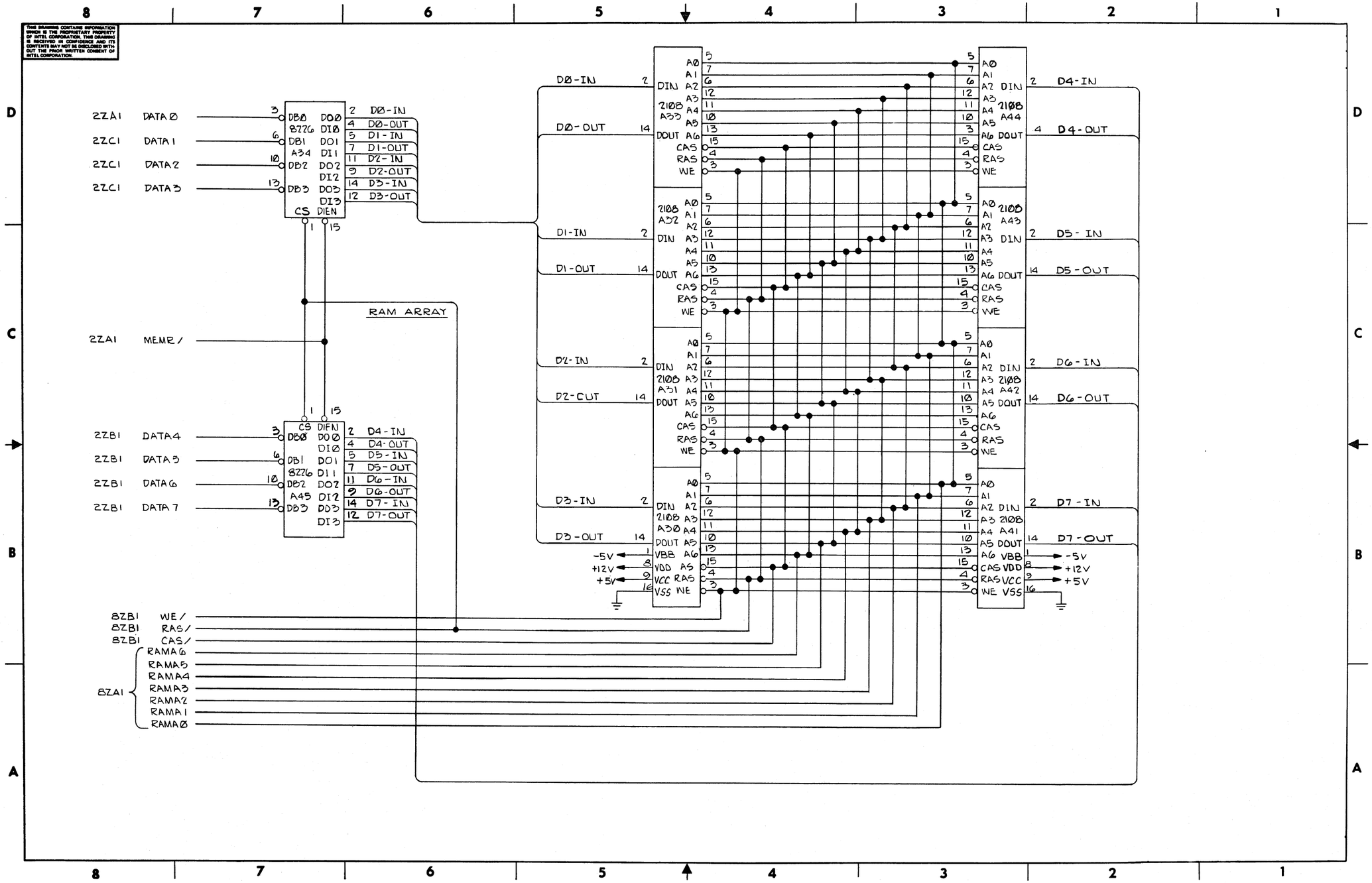
J5
9 DATA READY/
14 SYSTEMS READY/

J6
17 BUSY/
16 ACKNOWLEDGE/
22 SELECT/

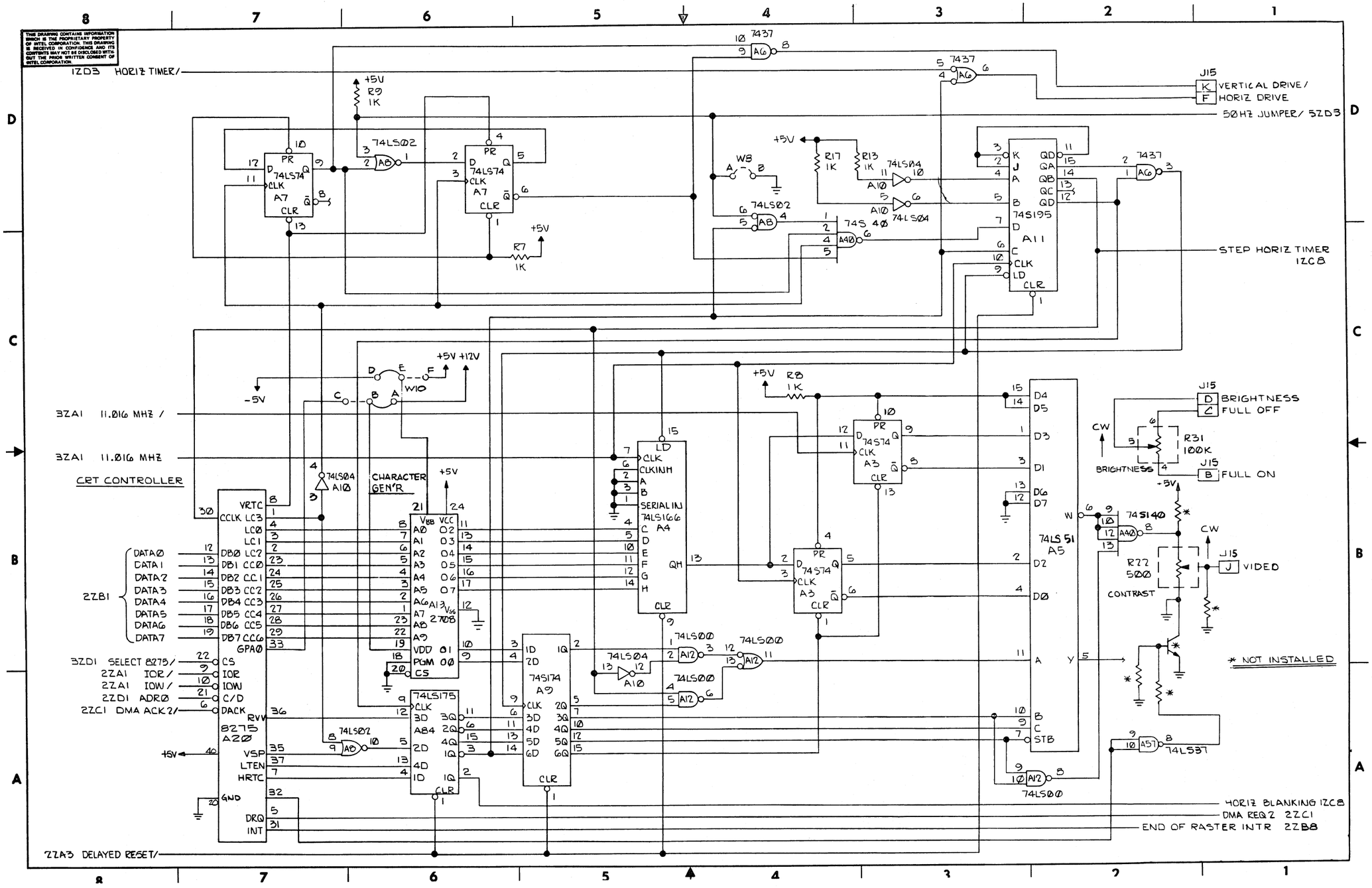
IOC Schematic (Sheet 7 of 12)



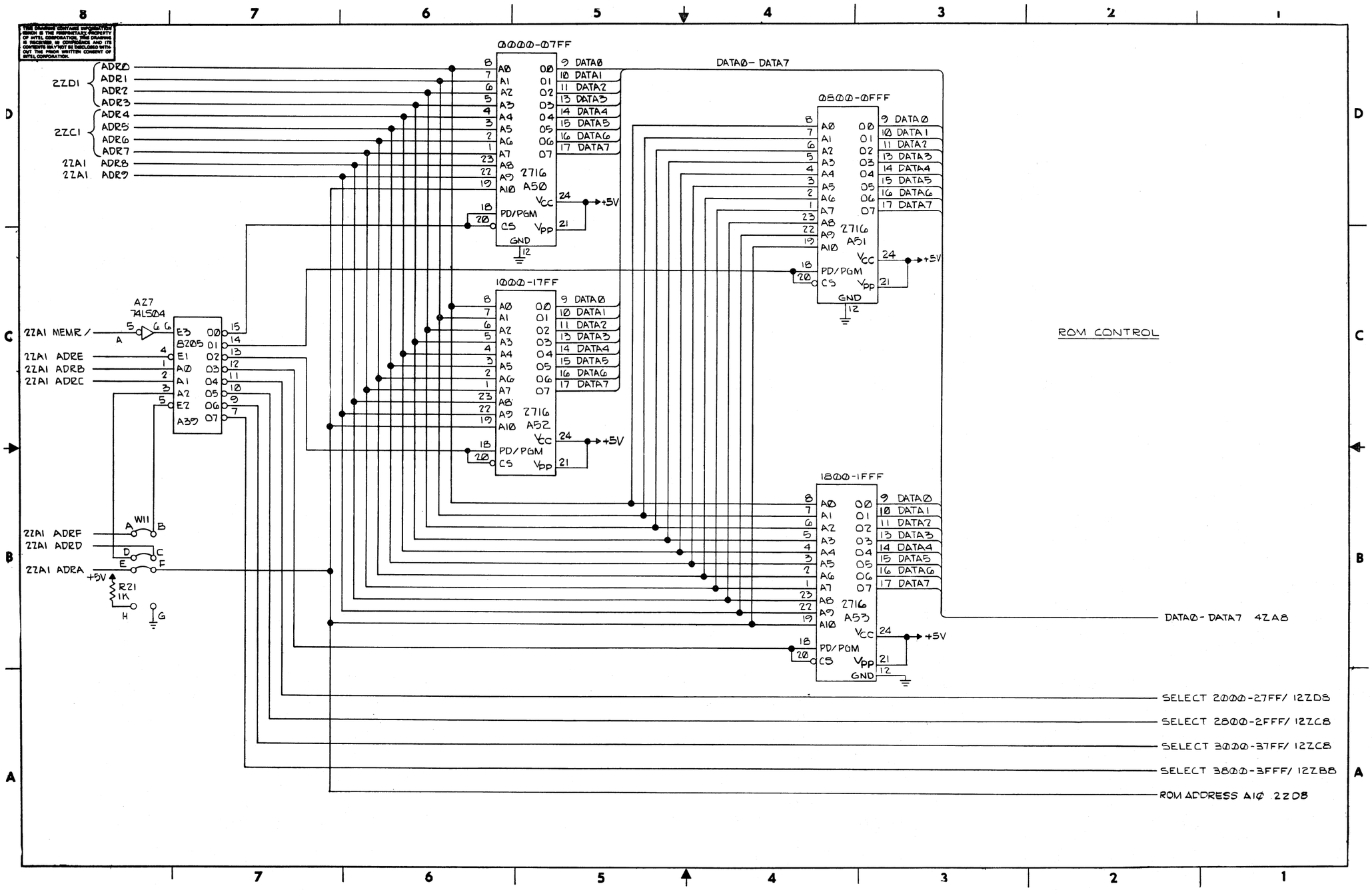
IOC Schematic (Sheet 8 of 12)



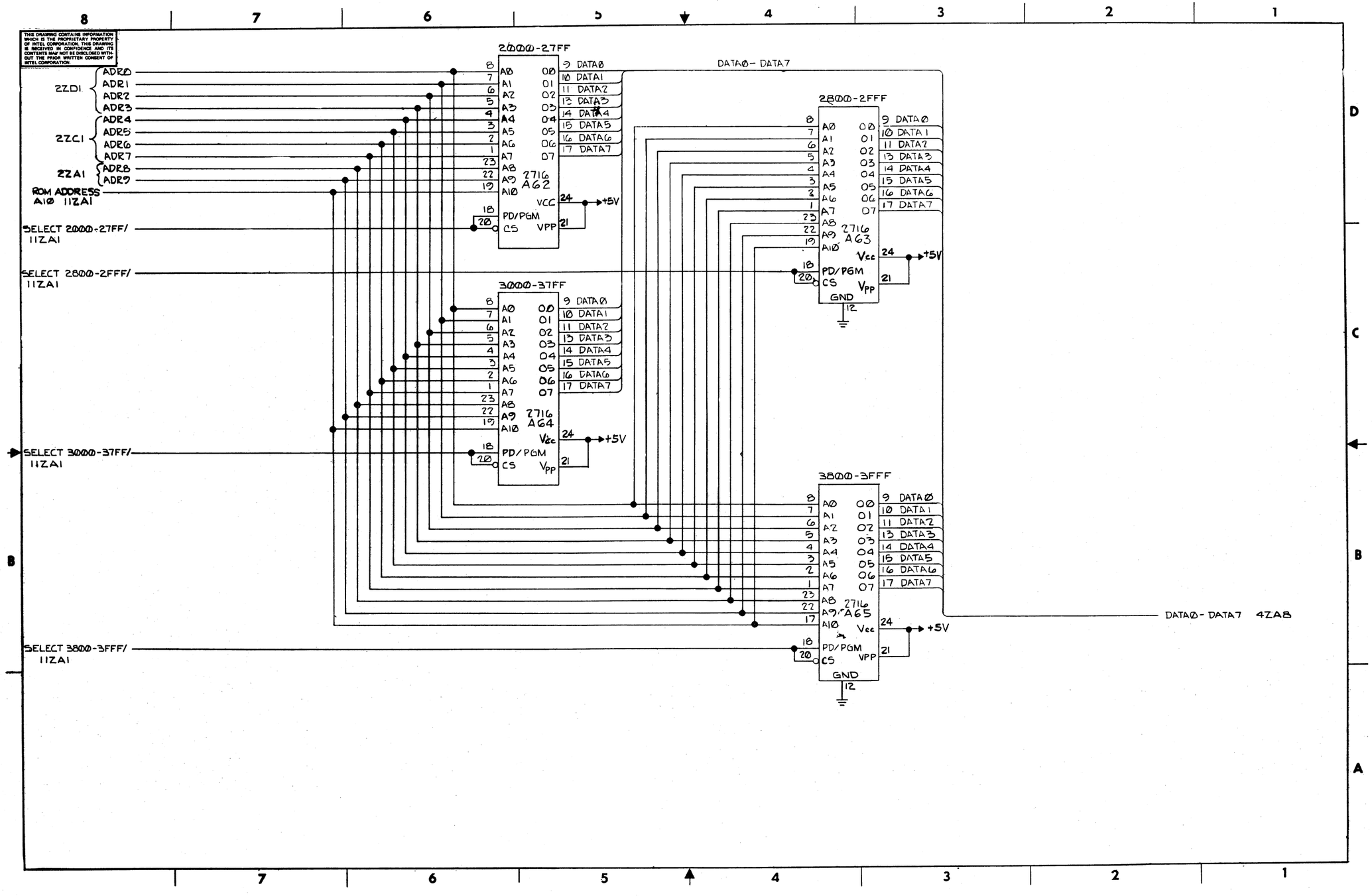
IOC Schematic (Sheet 9 of 12)



IOC Schematic (Sheet 10 of 12)



IOC Schematic (Sheet 11 of 12)



IOC Schematic (Sheet 12 of 12)