ICL

International Computers Limited

Training Division C.E.S.O.

Training Manual

BB006 : 1904A - Module 4

Dilin Test E. tube 588827

Test Slip 588775.

Issued by:-

Engineering Training Division,
International Computers Ltd.,
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Letchworth,
Herts. SG6 4AS.

(Letchworth 6141)

ISSUE

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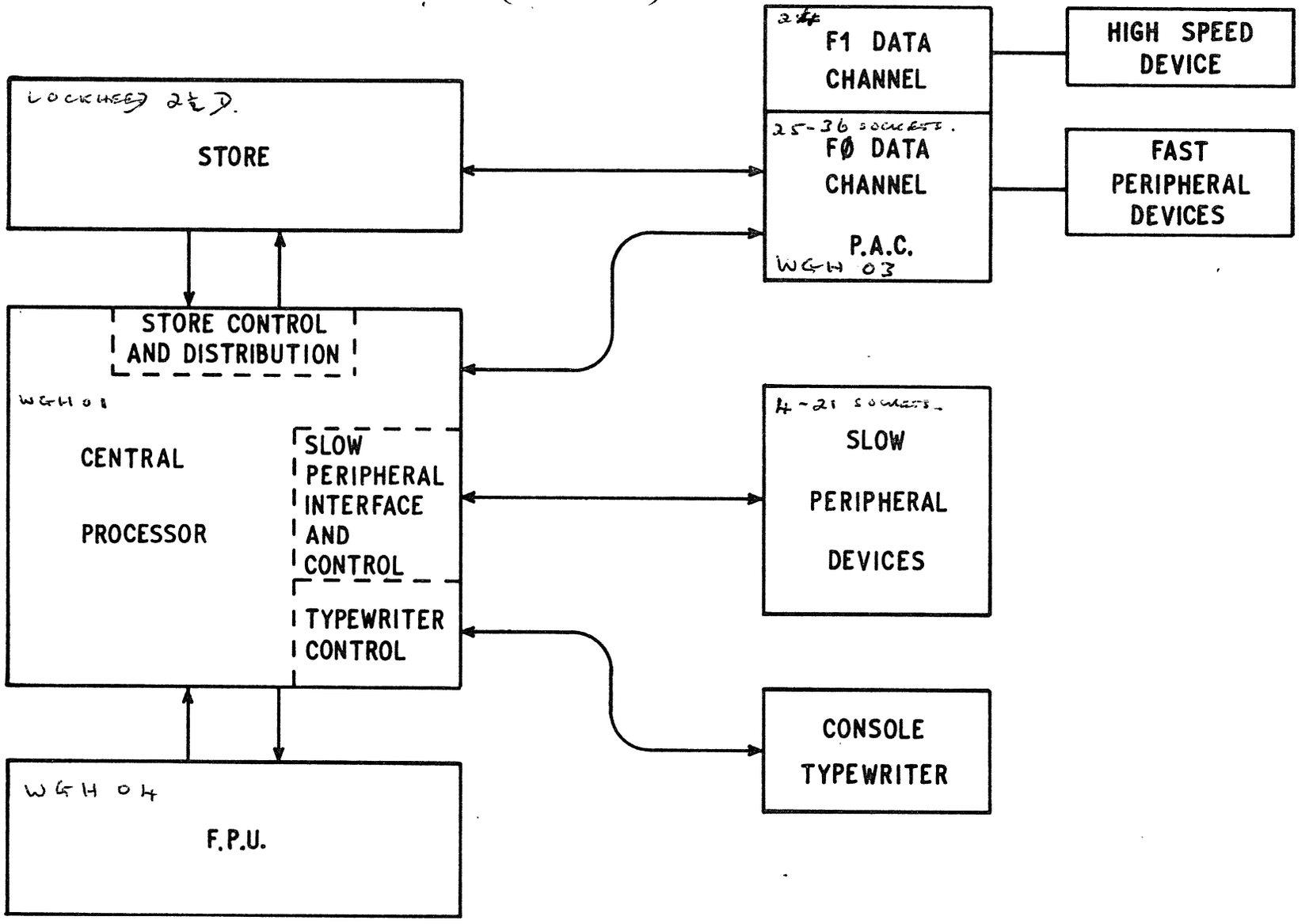
ETD.346

1904A SYSTEM BLOCK DIAGRAM

Iss 1.

WGH 09 PAGING FEATURE.

STORE EXTENSION LOGIC. (WCH02 ?)



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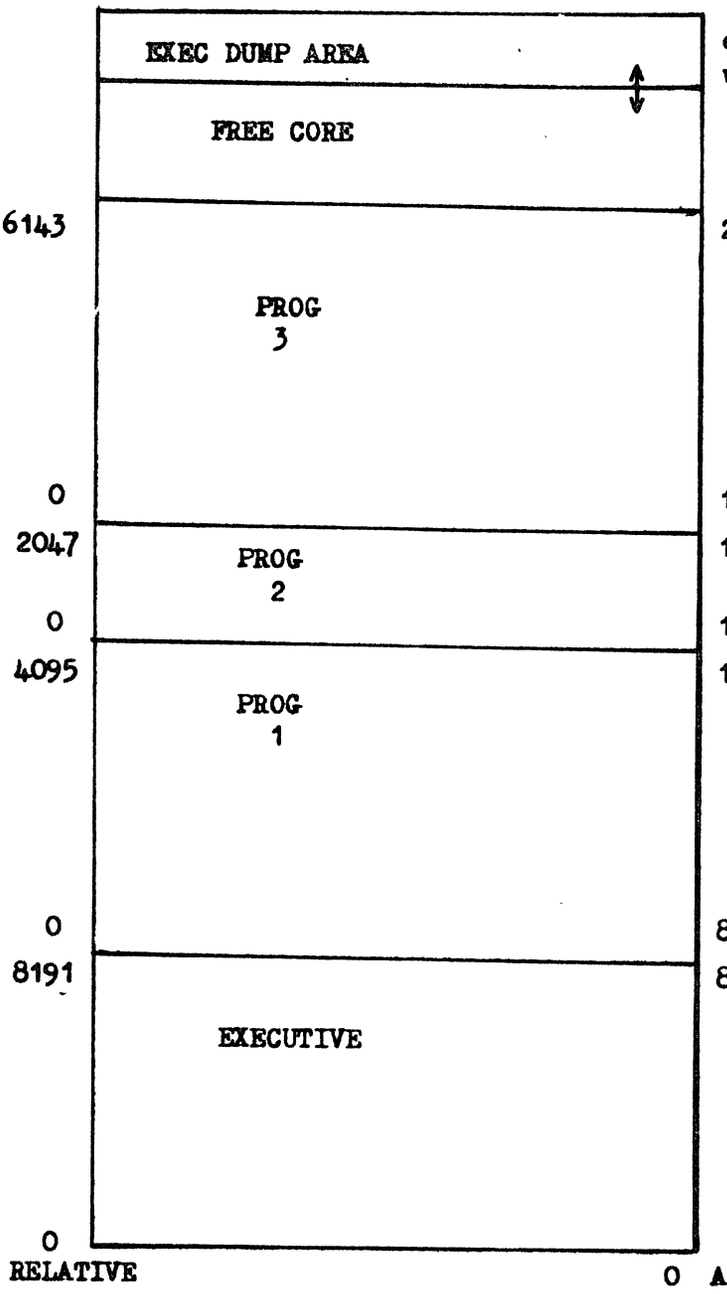
1904A MODULE 4.

No. BB006
Sheet 1.1

 ETD 3468 FORM 8/133/B(2.69)

LAYOUT OF PROGRAMS IN STORE



eg. Holds Request Block when loading Program.

To protect program areas a DATUM & LIMIT system is used.
Any object program must address within its prog. area.
Any address must be ≥ DATUM & < LIMIT.
∴ LIMIT OF PROG 1 is DATUM of PROG 2.

RESPONSIBILITIES OF EXECUTIVE

1. Performance of Extracodes (see Voluntary Entry)
2. The handling of incidents (see Involuntary Entry)
3. Communicating via the console typewriter with the operator to allow object programs to run.
4. General Utilities such as, the loading and dumping of programs, the searching of magnetic files and the outputting of programs for post mortems.
5. The over-all supervision of the system.

   e.g. Housekeeping
   Multiprogramming
   etc.

VOLUNTARY ENTRY TO EXECUTIVE

A voluntary entry is made to executive when an object program requires the use of executive to implement an instruction for which hardware is not available either because the hardware would be too complex or too expensive or would show little increase in efficiency.
Such instructions are called EXTRACODES.

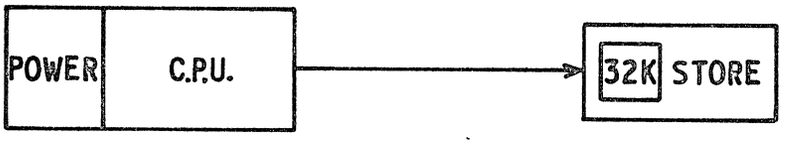
INVOLUNTARY ENTRY TO EXECUTIVE

An involuntary entry is made to Executive as a result of an "incident" occurring somewhere within the system. An incident can be defined as an event which requires some action to be taken initially by Executive, and then by object program or by the operator.
Incidents are without exception signified by INTERRUPTS. (e.g. B-line from peripheral).

Iss /.

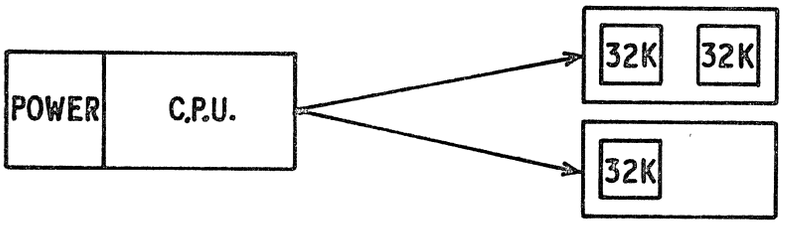
CONFIGURATIONS

2044/1

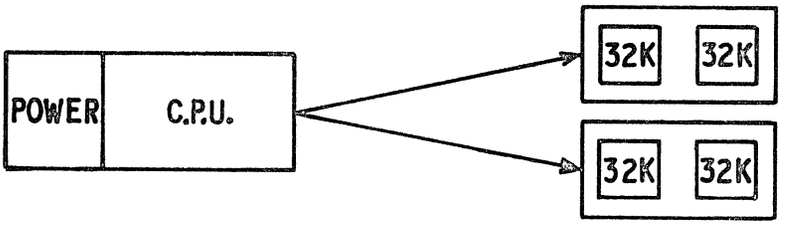


2044/3

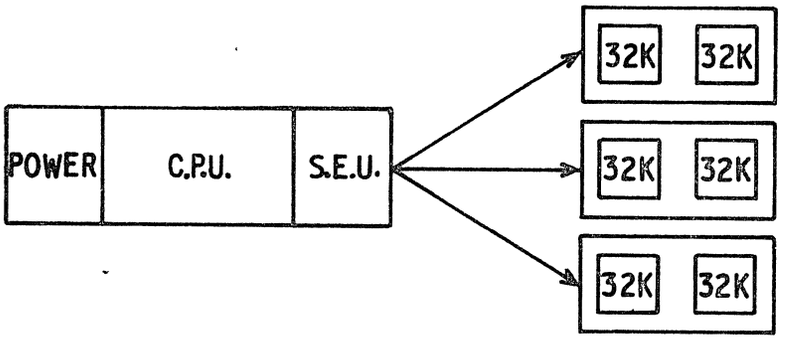
2044/5



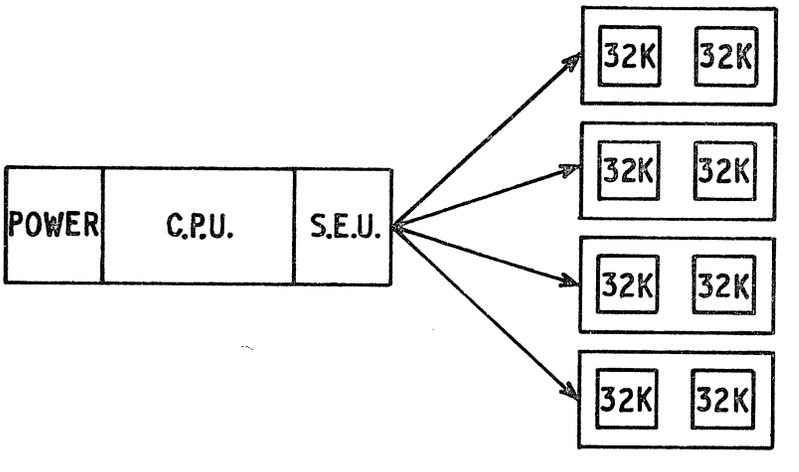
2044/6



2044/8



2044/9



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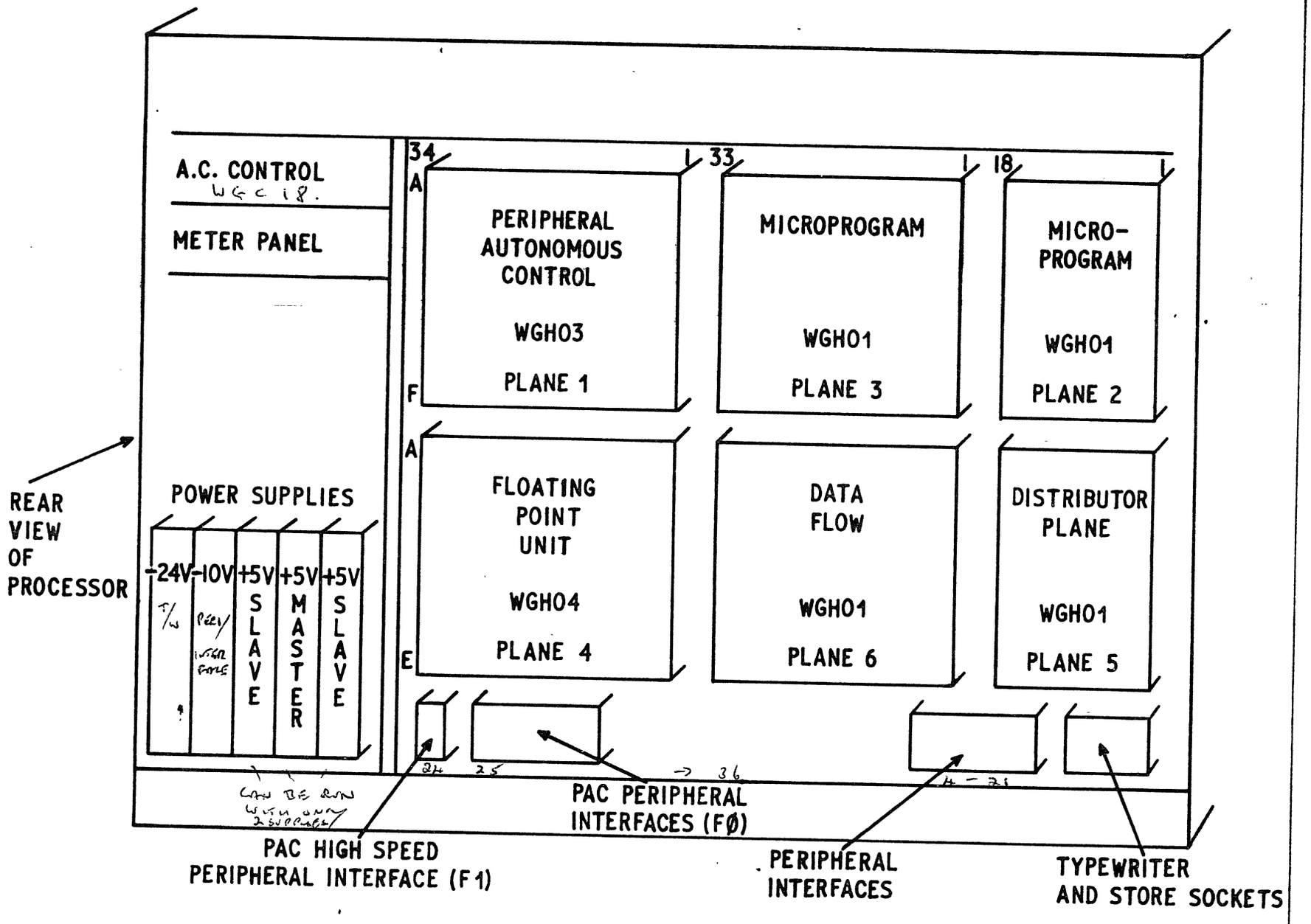
LAYOUT OF LOGIC PLANES

Iss 1.



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ETD 3472 FORM 8/133/B(2.69)

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1904A MODULE 4

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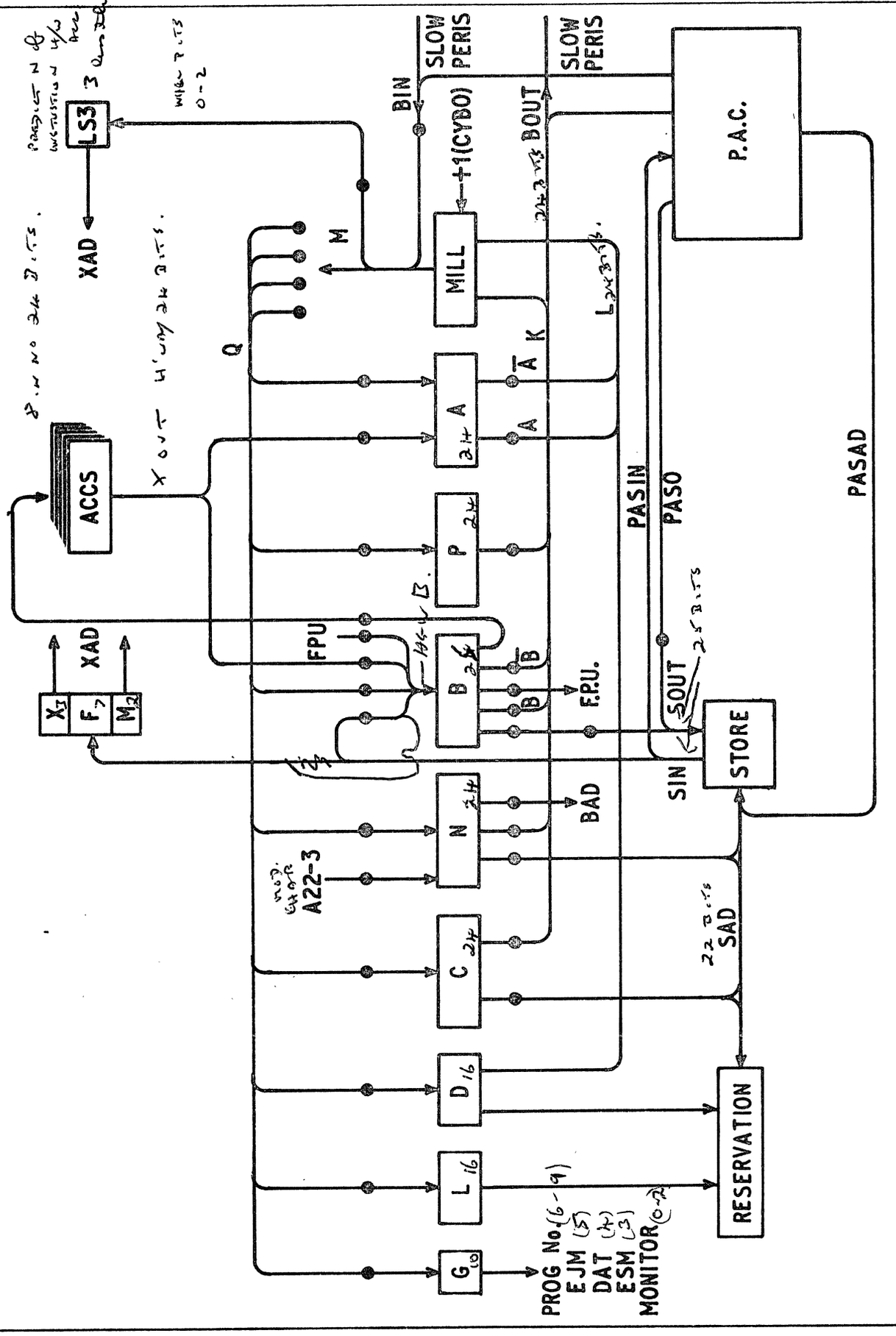
Sheet 1.6

Iss 1

1904A DATA FLOW



 ETD 3473 FORM 8/133/B(2.69)

1904A - USE OF REGISTERS.

'B' REGISTER - Used as Store Buffer. All data to & from store must pass through 'B'.
Used also as WORKING register.

'C' REGISTER - Used to hold Current Instruction Address & state of Overflow & Carry. Used occasionally as a WORKING register.
Used to Address Store.

'N' REGISTER - Used to address store. Also used as decremental counter in certain functions. Bits 22 & 23 used to hold CHARACTER address for use with character handling instructions.

'A' REGISTER - Used as working register.

'P' REGISTER - Used as working register for instructions invloving double length operands. (Shifts - Mult - Div).

'D' & 'L' REGISTERS - Used to contain program boundary addresses necessary in a multiprogram environment.

'G' REGISTER - Holds information peculiar to current program such as:- Mode, Prog. No.

HARDWARE ACCUMULATORS.

8, 24 bit registers used in place of store locations 0-7 during program running. These are time shared by programs; therefore when entry to Executive is made the M'ware accs must be stored to the current object programs store locations 0-7. When re-entering an object program, that programs locations 0-7 are placed in the Hardware accs.

Access to the Accumulators is totally independent of store, ∴ It is possible to read or write to store & access the Hardware Accs simultaneously.

MILL. Full 24 bit Parallel Adder with Block carry system.

HIWAYS K. L. hiways carry data from registers to the MILL.

Q. hiway carries data to the registers.

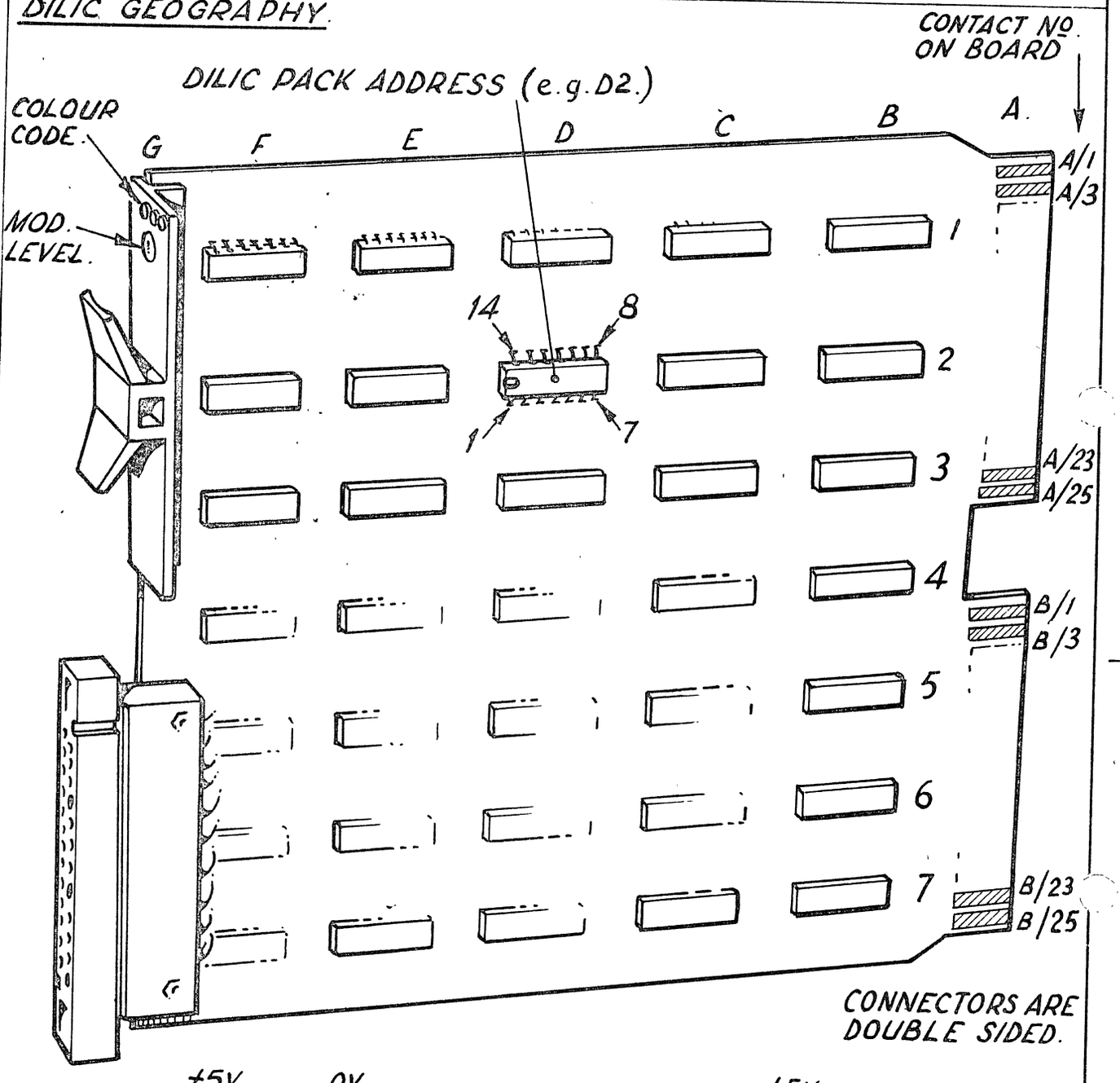
'F' REGISTER
Holds current function number throughout instruction.

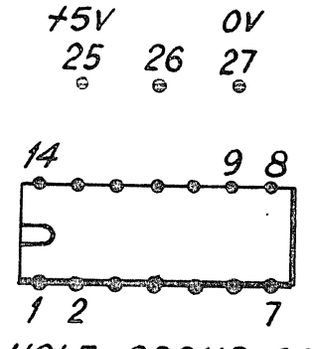
'X' REGISTER
Holds Accumulator Address or Literal value of X field throughout instruction.

'M' REGISTER
Holds address of Accumulator holding modifier.

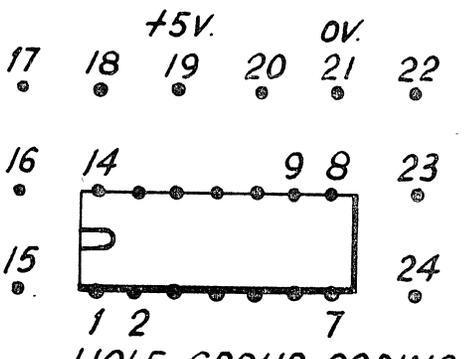
Iss 1.

DILIC GEOGRAPHY.



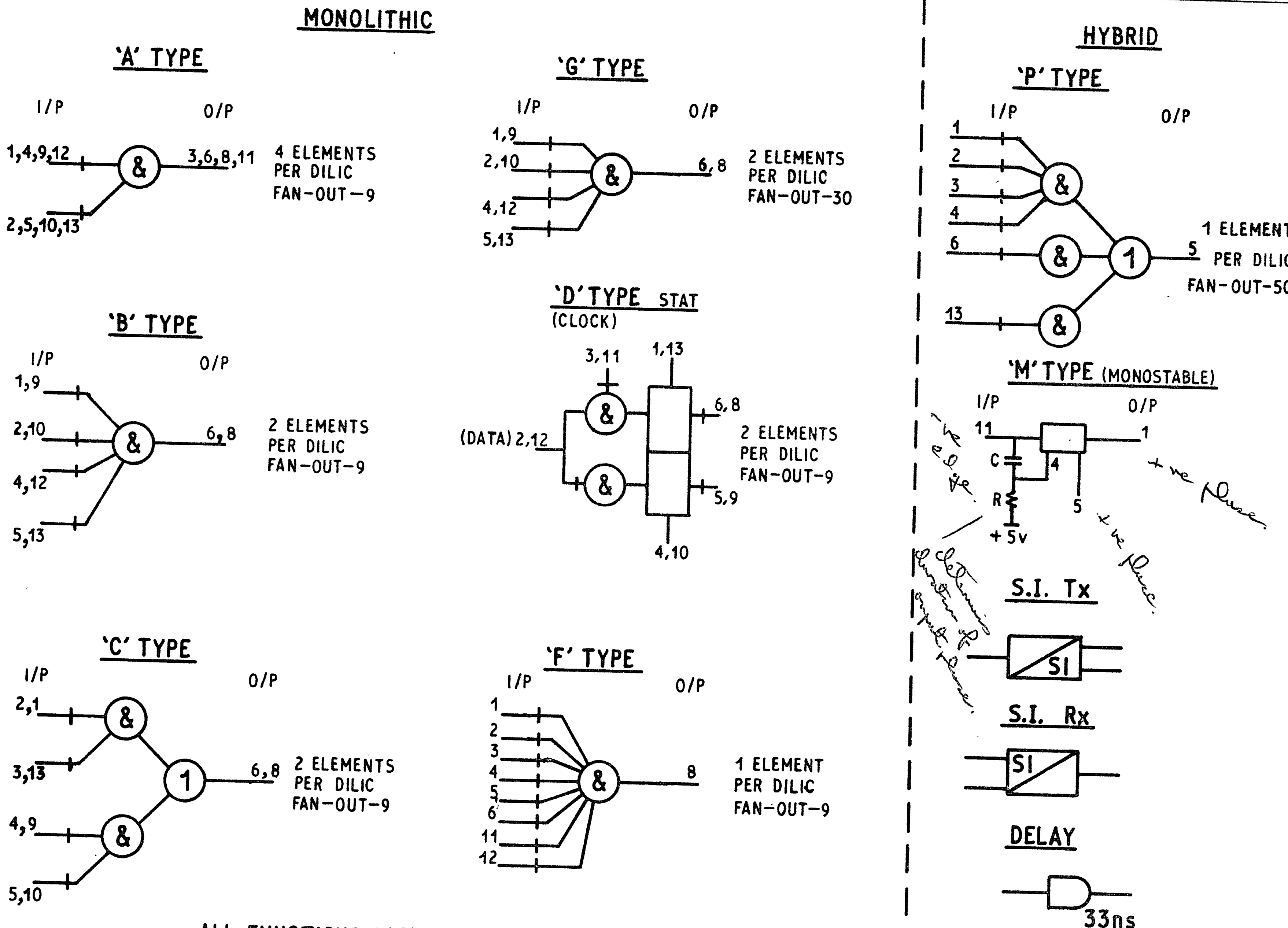


HOLE GROUP CODING
ROWS C & E.



HOLE GROUP CODING
ROWS B, D & F.

1904A INTEGRATED CIRCUIT FAMILY



ALL FUNCTIONS PACKAGED IN STANDARD 14 LEAD DUAL-IN-LINE PACKAGE-DILIC

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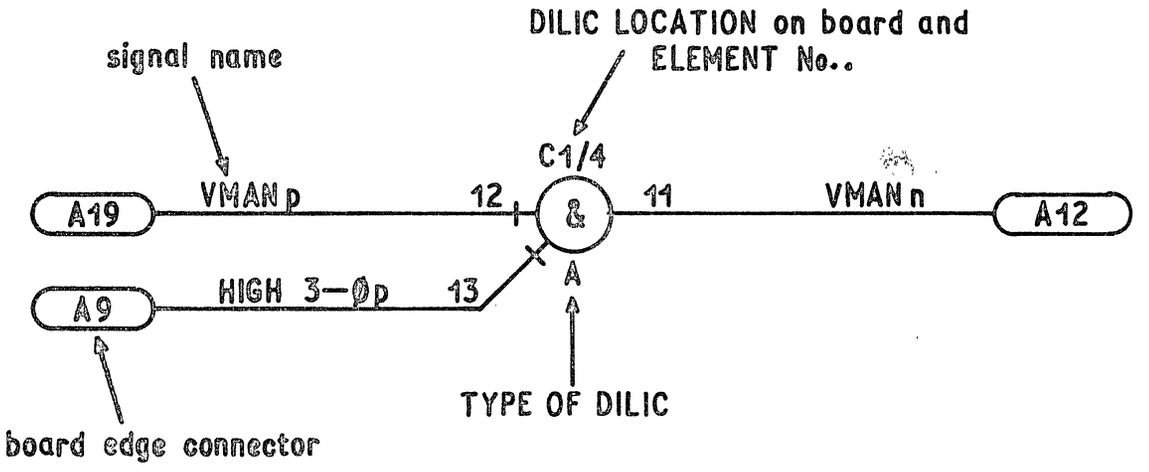
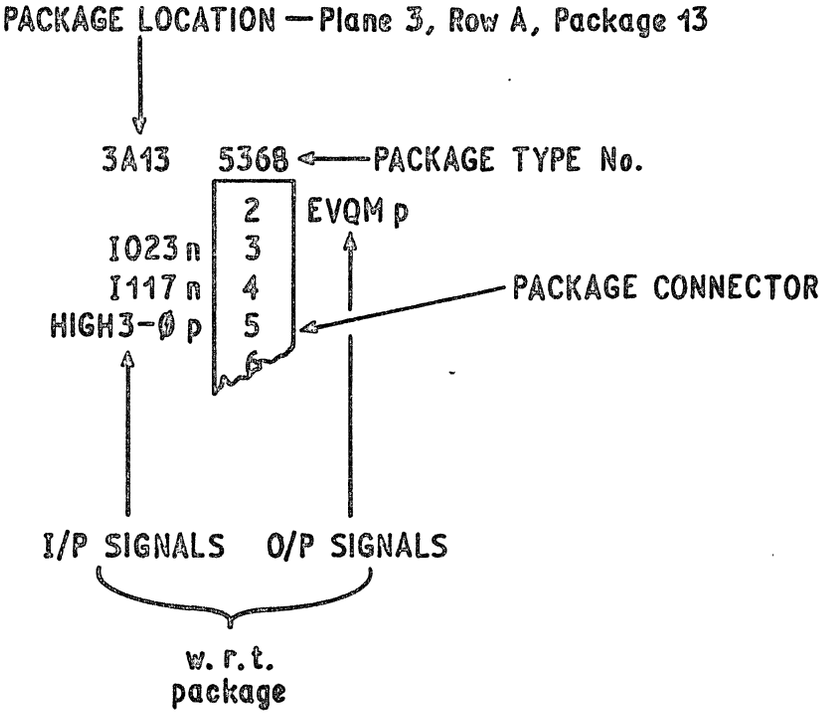
1904A MODULE 4.

No. BB006 Sheet 1.9

Iss 1

1. MACRO BOARDS

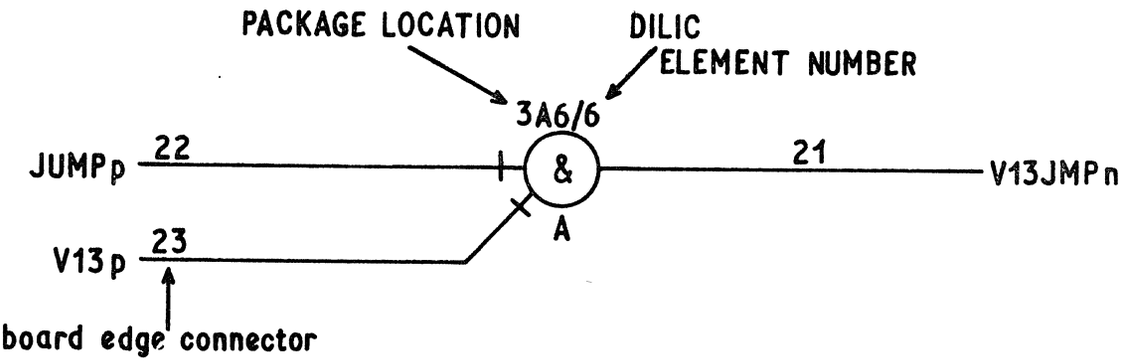




INFORMATION ON LOGIC DIAGRAMS

Iss 1.

2. OMNI BOARDS



There are 2 'A' type DILICS on an 'A' OMNI BOARD.

ELEMENT NUMBERING:- 1st DILIC 1–4, 2nd DILIC 5–8.

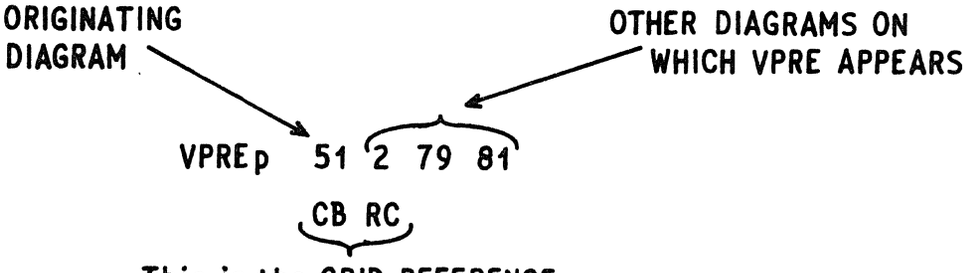
The number of dilics per package is limited by the number of edge connexions.

'A' dilics have 12 signal pins, thus giving a total of 24 signal pins.

BOARDS have 26 edge connectors thus allowing 2 spare for SUPPLY and EARTH

IN THE MARGIN

a) EARLY DIAGRAMS



This is the GRID REFERENCE to VPRE on this page.

NOTE :- When a CONNECTOR is REFERENCED, the GRID refers to the TOP of the connector.

[ ] usually indicates a signal from an external source, e.g. ENGINEERS PANEL.

b) LATER DIAGRAMS

Reference to originating diagram and grid reference on current diagram given only.

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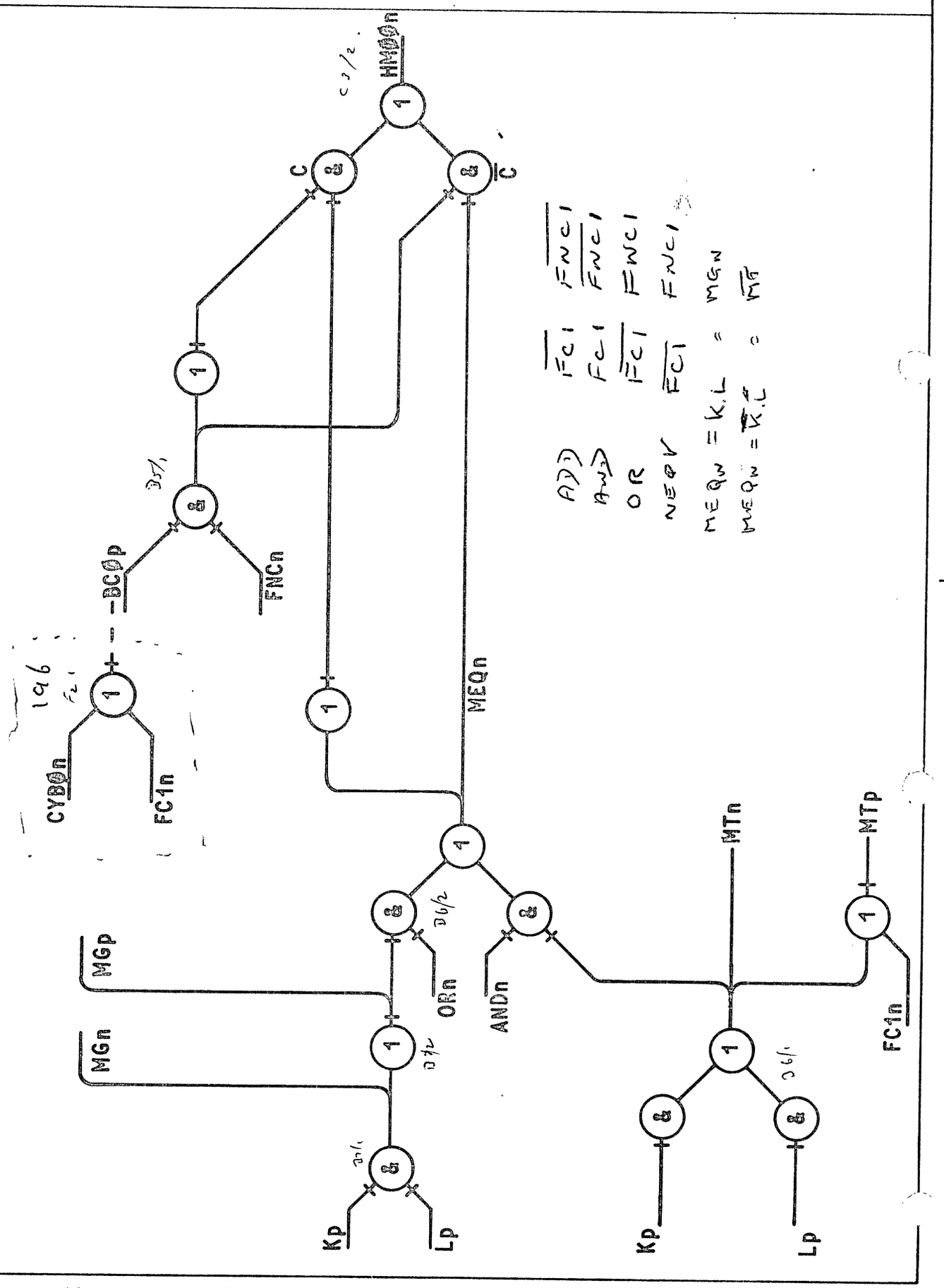
Iss 1.

MILL SIMPLIFIED — SLICE 0



 ETD 3479 FORM 8/133/B(2.69)

BLOCK CARRY SYSTEM.

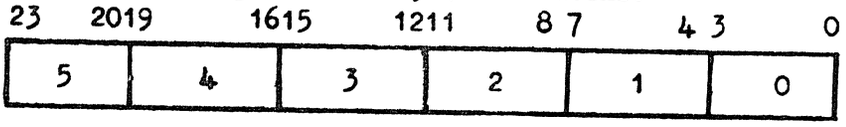
TYPE - ANTICIPATORY

So called because the 'CARRY' to each slice is calculated from the INPUTS to the MILL.

A full ANTICIPATORY system while being fast is also costly; therefore a system compromising between SPEED & COST is used. This is the BLOCK CARRY SYSTEM.

The MILL is split into 6, 4 bit blocks:-

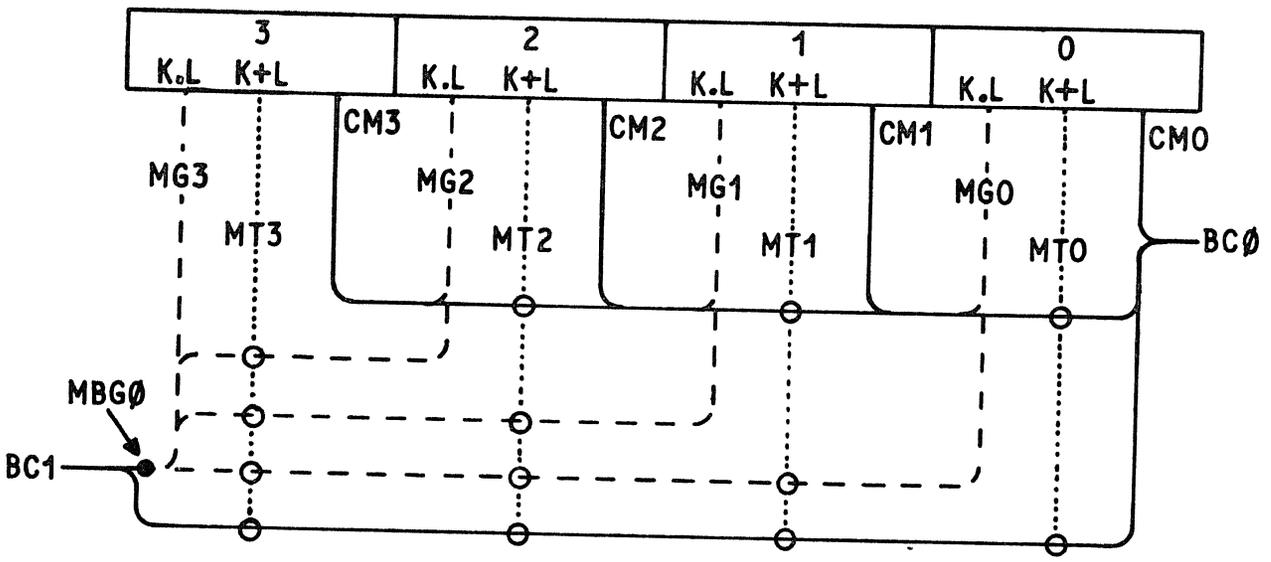
EG.



For any slice, carry will be generated if :-

1. K.L. active, GENERATE carry to next slice (MG)
2. K+L active, TRANSMIT any carry through this slice (MT).

CARRY WITHIN A BLOCK (EG Ø)



From above it can be seen that

Carry to Slice Ø(CMO) = BCØ
" " Slice 1(CM1) = MGØ OR BCØ.MTØ
" " Slice 2(CM2) = MG1 OR MGO.MT1 OR BCØ.MTØ.MT1

etc.

Carry to the next block (BC1) is anticipatory.
BC1 given by MBGØ OR BCØ. MBTØ (MT0.MT1.MT2.MT3)
Therefore at no time is the o/p of the MILL used to generate carry.

The levels MBGØ (Block Generate) and MBTØ (Block Transmit) are produced on the mill slices.

BC levels are produced by the MILL Block carry logic and are used to link the 6,4 bit blocks together.

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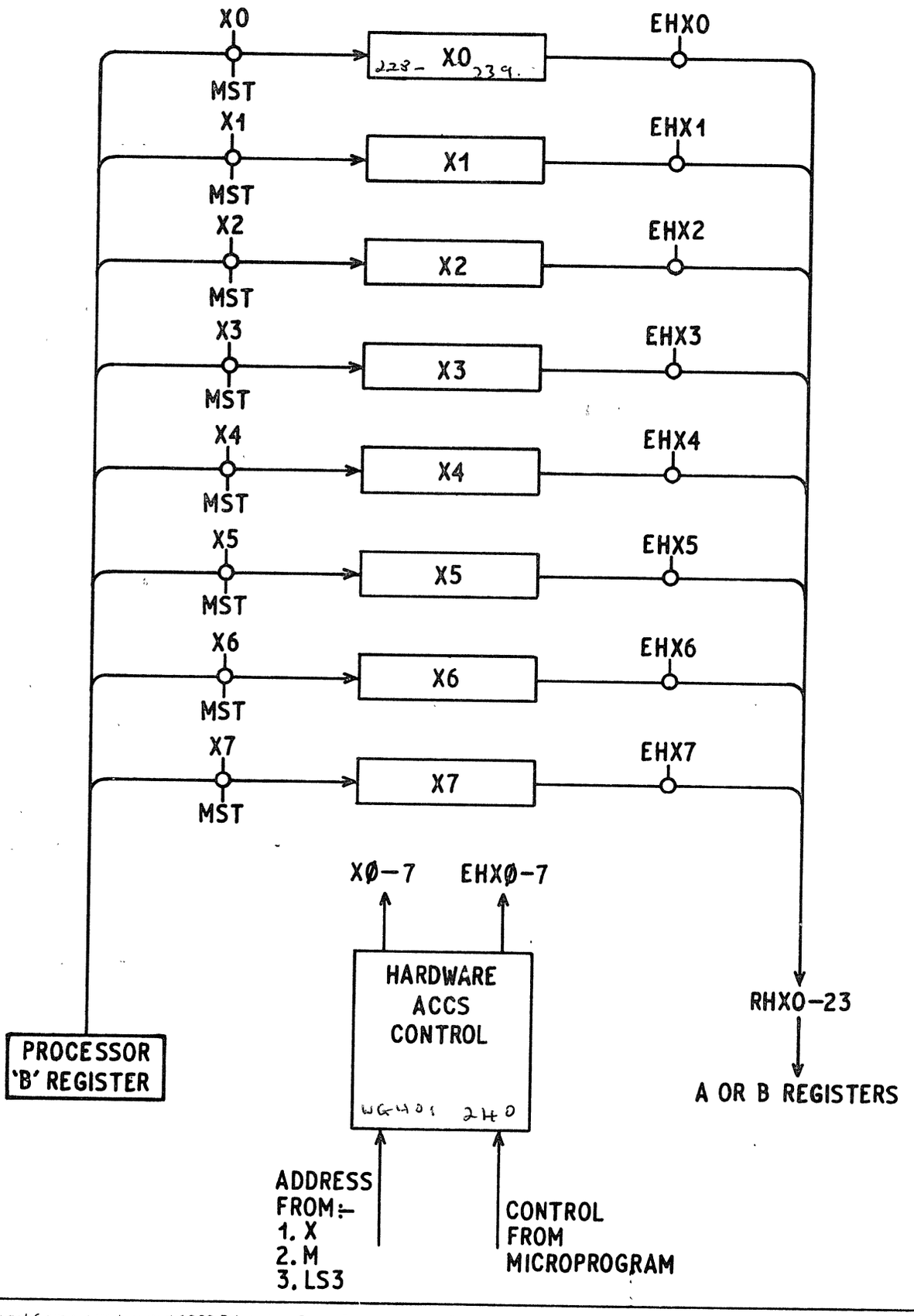
Iss /.

HARDWARE ACCUMULATORS — BLOCK DIAGRAM

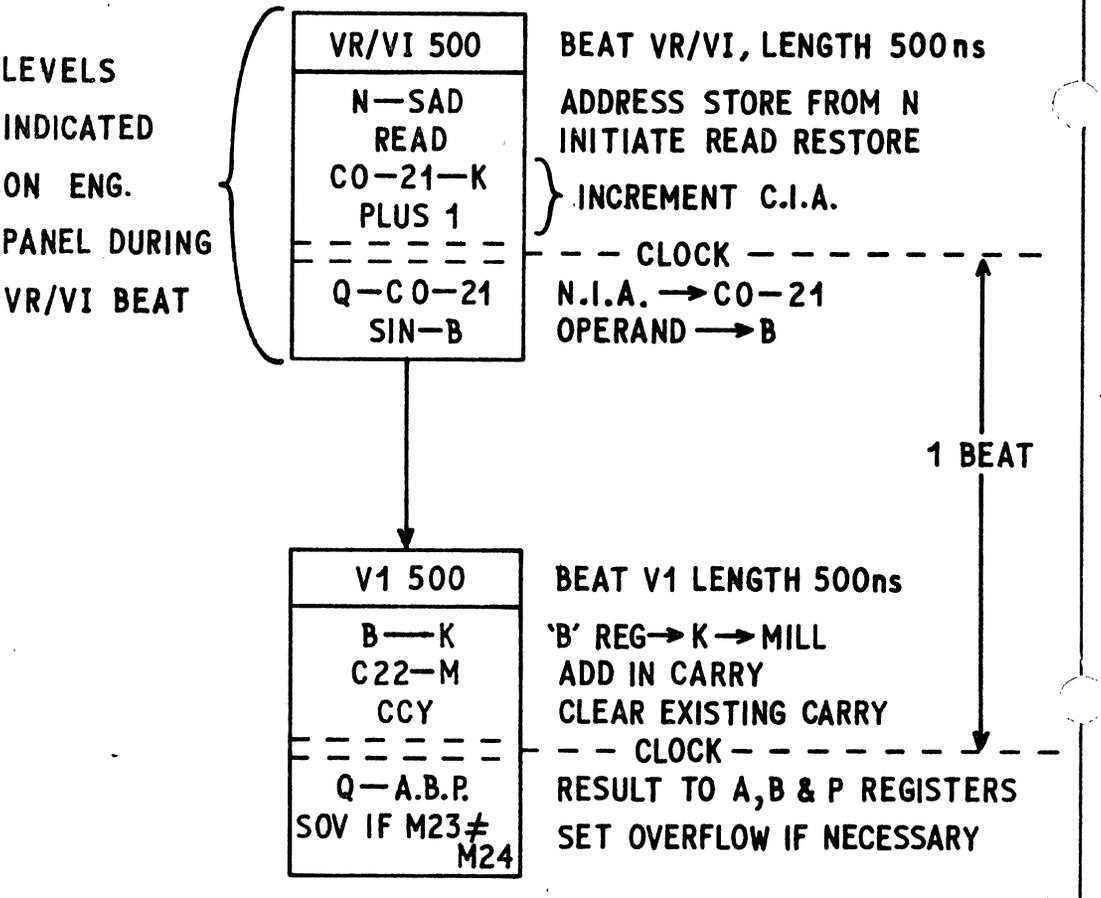


 ETD. 3482 FORM 8/133/B(2 69)

1904A C.P.U. FLOWCHARTS

THESE DESCRIBE THE LOGICAL SEQUENCE OF FUNCTIONS FOR THE C.P.U. ETC. (I.e. MICROPROGRAM)

EXAMPLE OF FORMAT



NOTE: IF THE STORE IS BUSY WHEN READ INITIATE IS GIVEN, BEAT VR/VI WILL BE LENGTHENED.

INSTRUCTION PHASE (SIMPLIFIED) BRANCH ORDERS.

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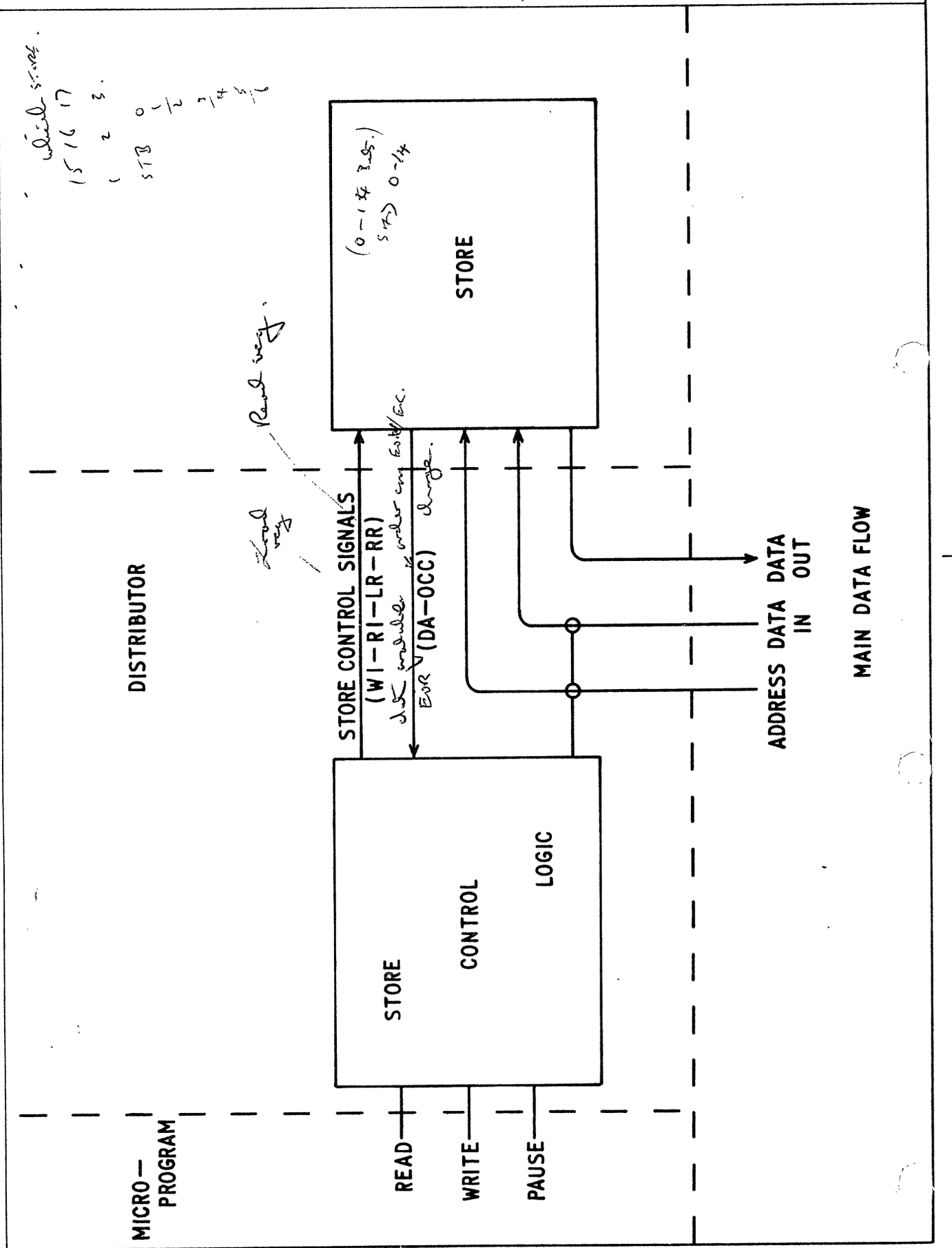
Iss 1

STORE CONTROL—BASIC PRINCIPLE



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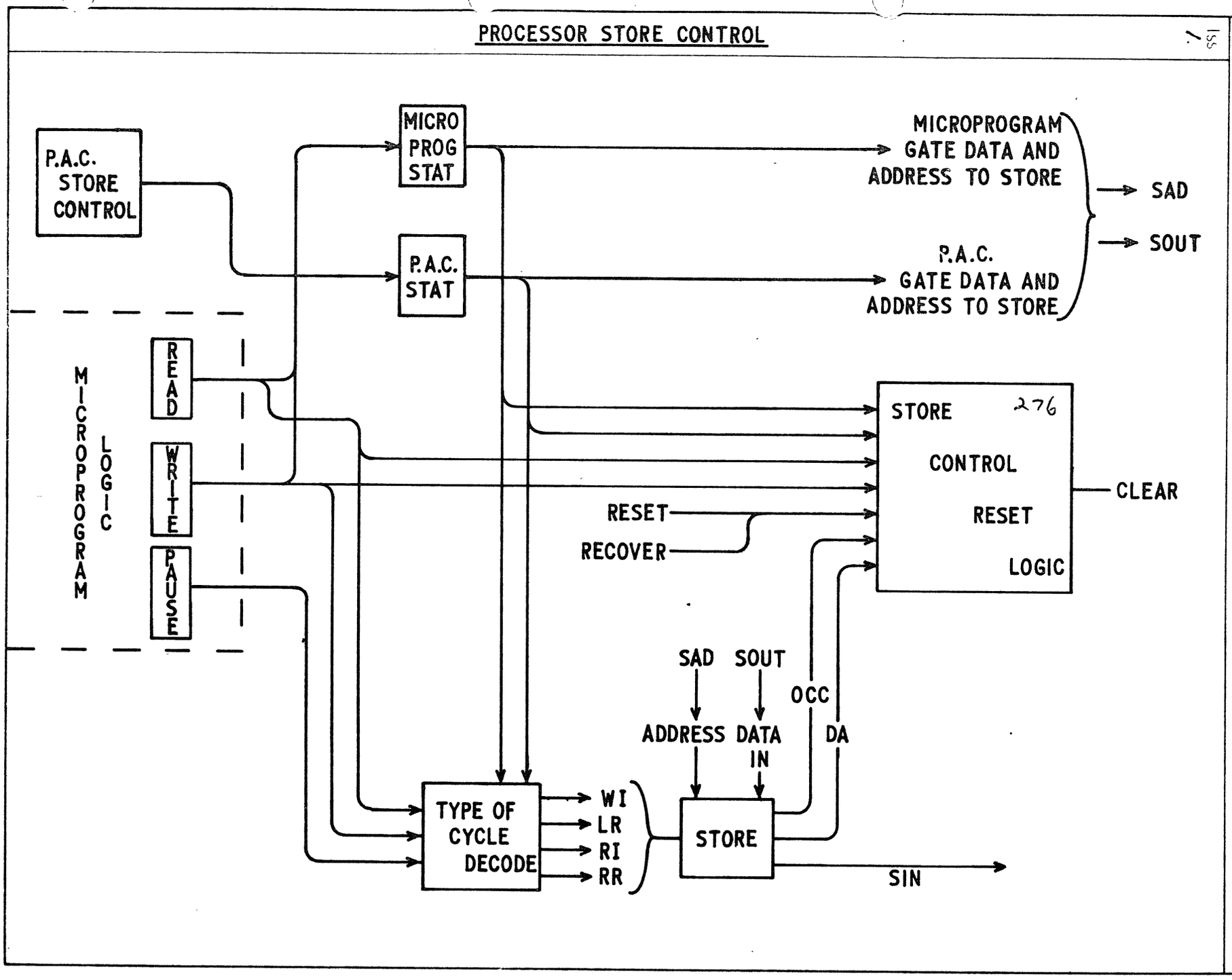


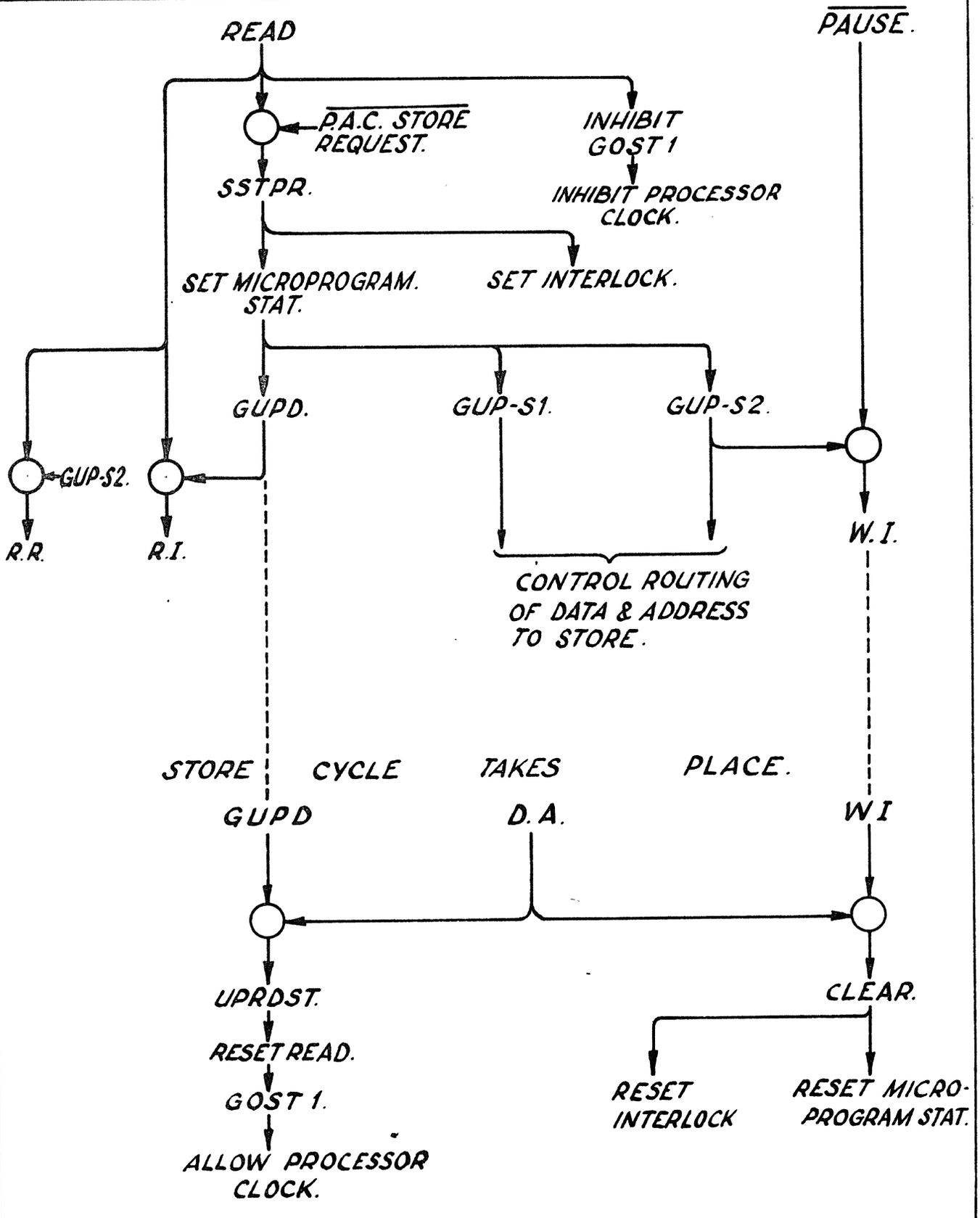
ETD 3486 FORM 8/133/B12 69

STORE CONTROL ~ SUMMARY OF SIGNALS.

TYPE OF CYCLE.	SIGNALS TO STORE.				SIGNALS FROM STORE.	
	R.I.	WI	R.R.	L.R.	D.A.	OCC.
READ RESTORE.	✓	✓	✓	✓	✓	✓
READ PAUSE.	✓	✓	✓	✓	✓	✓
PAUSE WRITE	✓	✓	✓	✓	✓	✓
CLEAR WRITE.	✓	✓	✓	✓	✓	✓

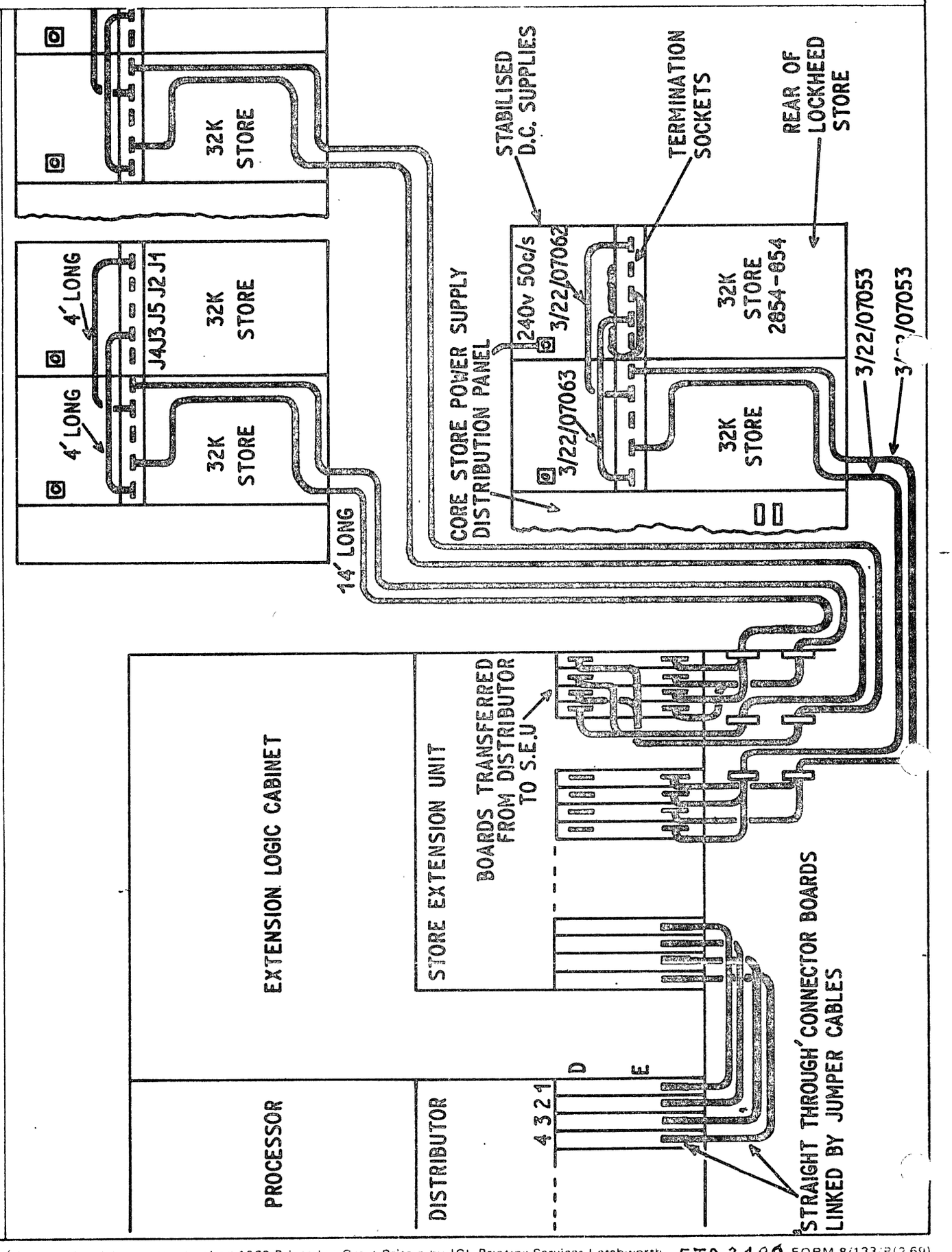
ISS 1.

STORE CONTROL
ACTION FOR READ RESTORE.



Iss 1.

CORE STORE – PROCESSOR CABLING



 ETD 3489

Iss 1.

LOCKHEED 2½d. (I.C.L. 650 ns) STORE.

General Details.

I.C.L. No. 2042/2

3 types available dependent on Processor type.

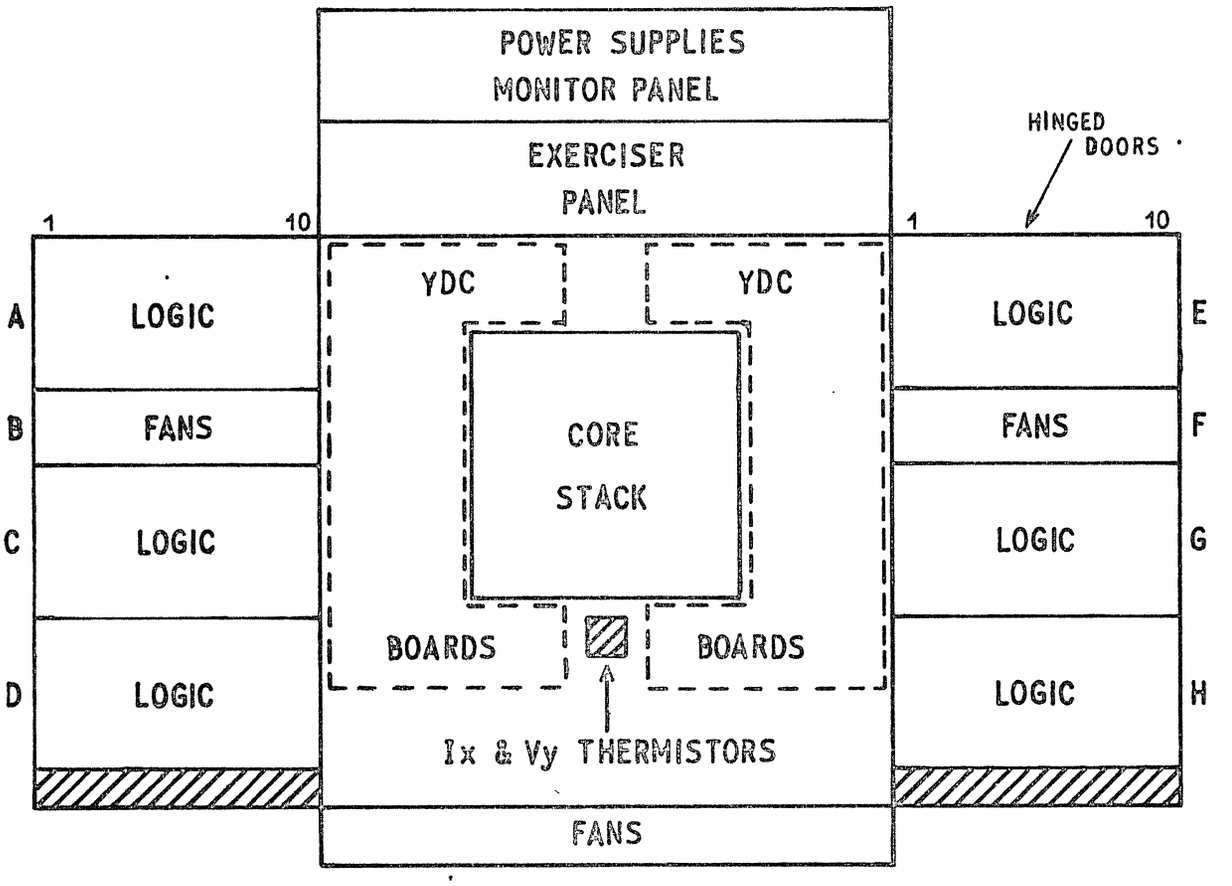
1904F - Interfaced to -6v (700 series).
1904A - Interfaced to TTL.
1906A - Interfaced to ECL.

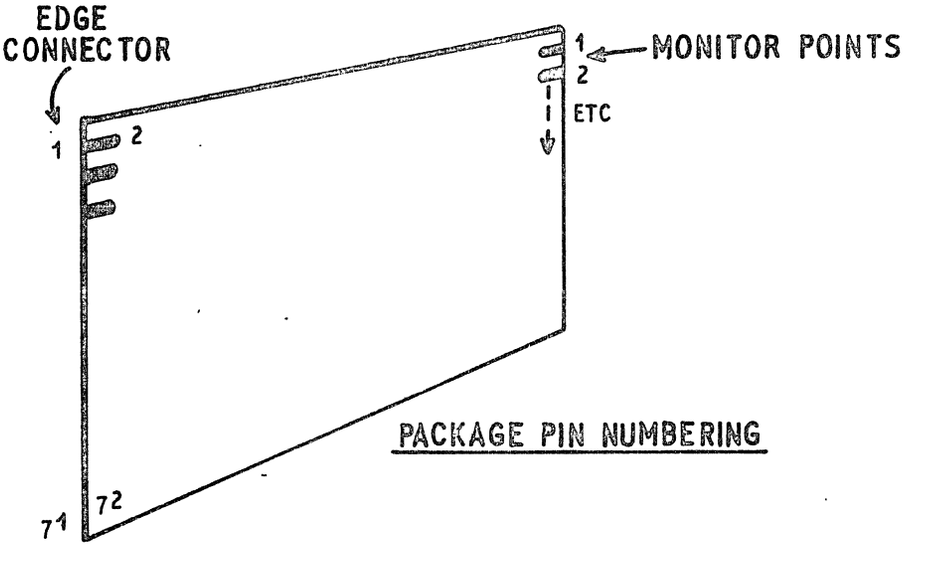
Capacity	-	32K words, 25 bits per word.
Type of Access	-	Random.
Method of Access	-	Co-incident ½ currents (≏500 ma).
Access Time	-	325 ns (Core Switch 205ns).
Cycle Time	-	650ns

Power Requirement	-	240v Single Phase.
Power Consumption	-	2·1 KVA.

Iss 1.

PHYSICAL CONSTRUCTION

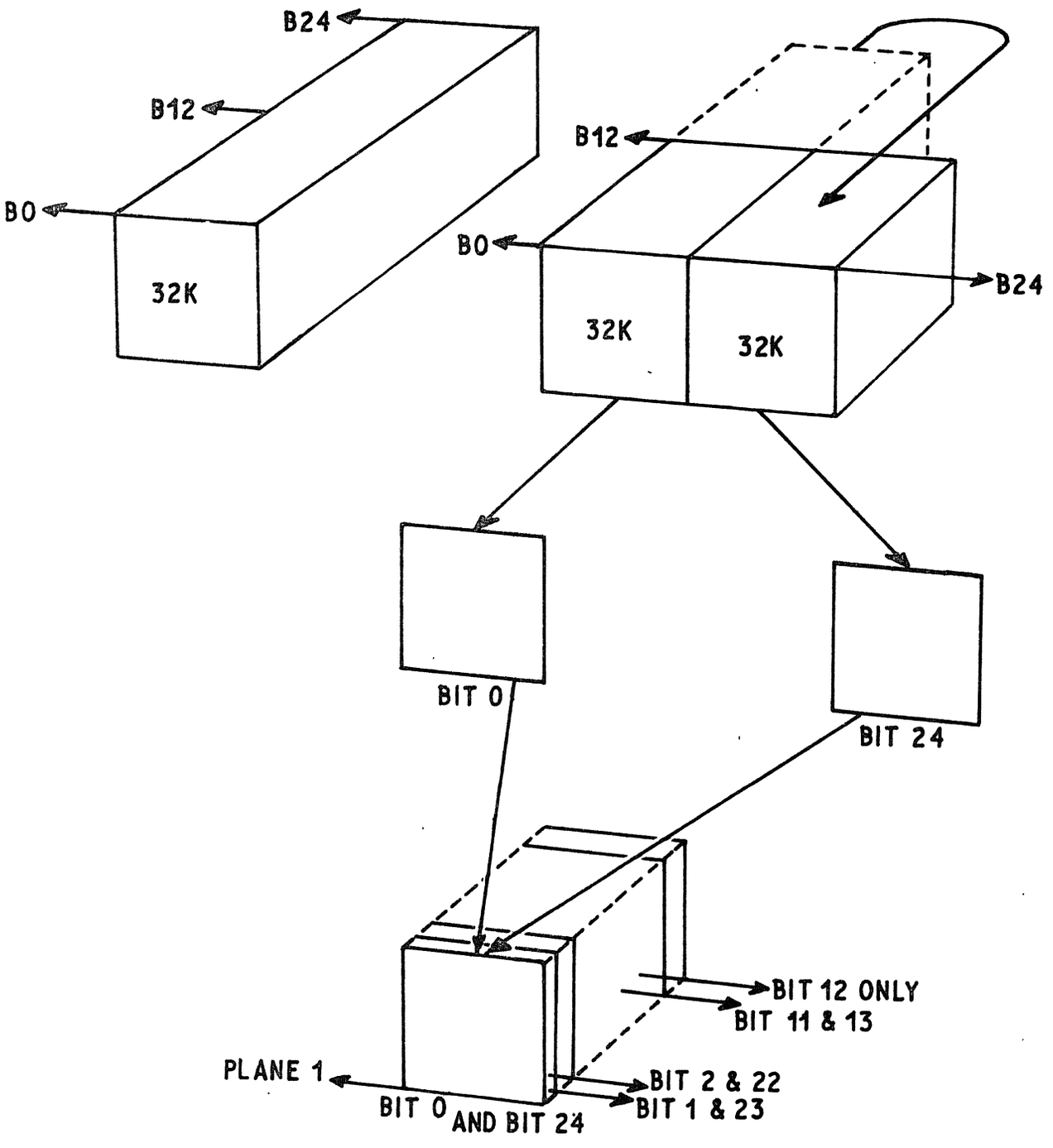




PACKAGE PIN NUMBERING

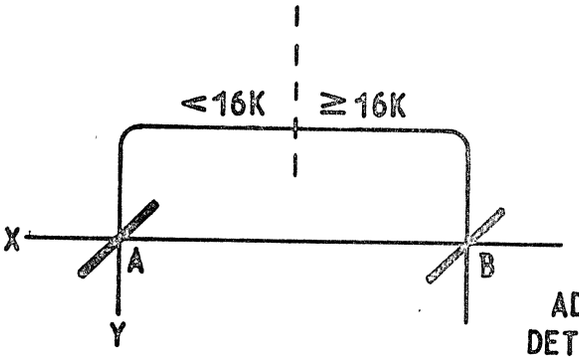
Iss 1.

$2\frac{1}{2}$D STORE SIMPLIFIED APPROACH



MATRICES OVERLAP SO THAT THE 2 BITS PER PLANE FORM A MORE COMPACT CONFIGURATION.

CORE SELECTION



ADDRESS BIT 14
DETERMINES < OR ≥ 16K

READ A $(\overline{2^{14}})$

READ B (2^{14})

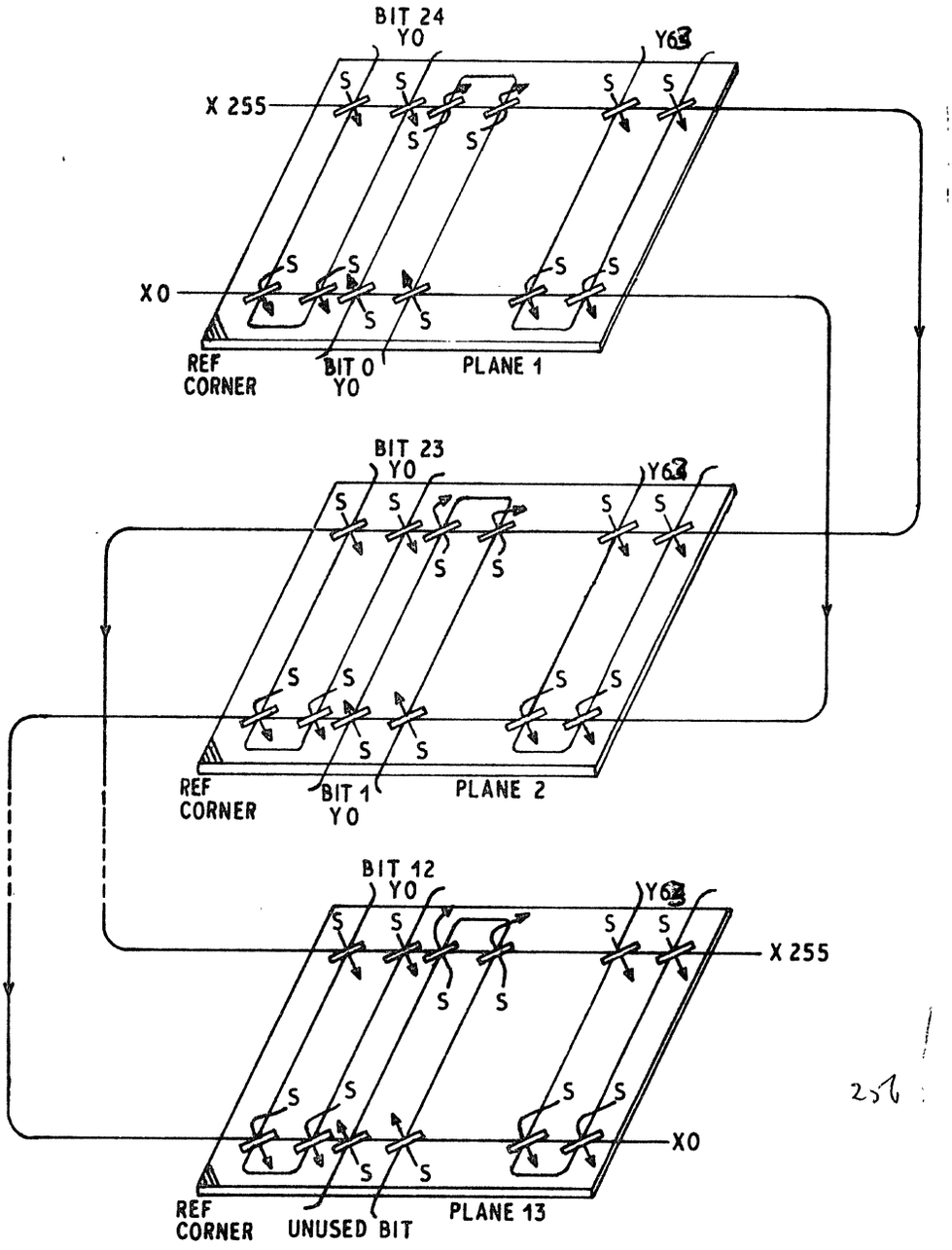
WRITE A $(\overline{2^{14}})$

WRITE B (2^{14})

NOTE 'Y' current reverses dependent on READ or WRITE.

'X' current reverses dependent on READ or WRITE and on the state of ADDRESS BIT 14

STACK WIRING



NOTE : S = SENSE LINE

256

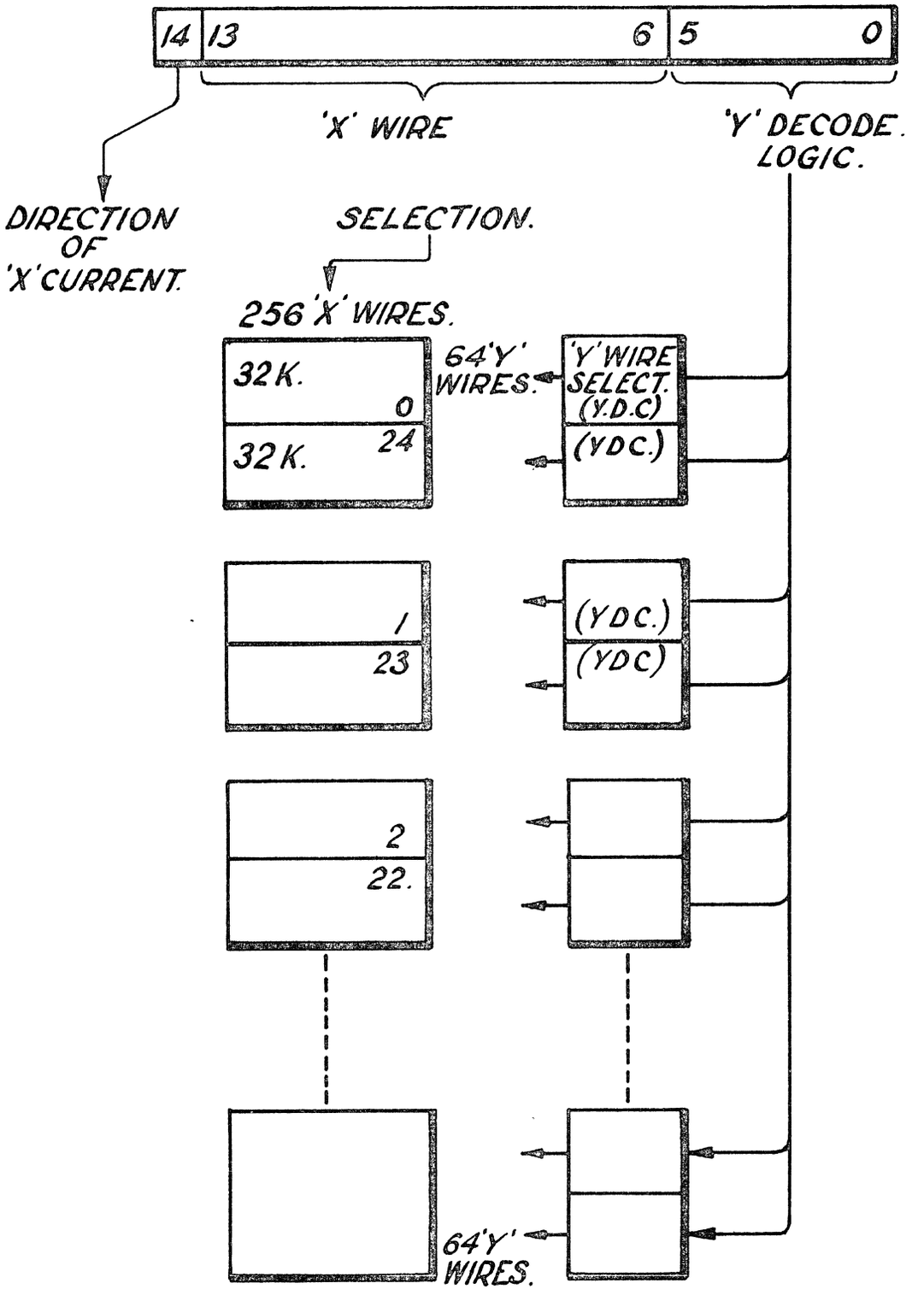
256 32K.

14 | 13 6 | 5 0

16K or ≥ 16K 255 words 63 words.

Iss 1.

BASIC ADDRESSING ~ (2½ D)



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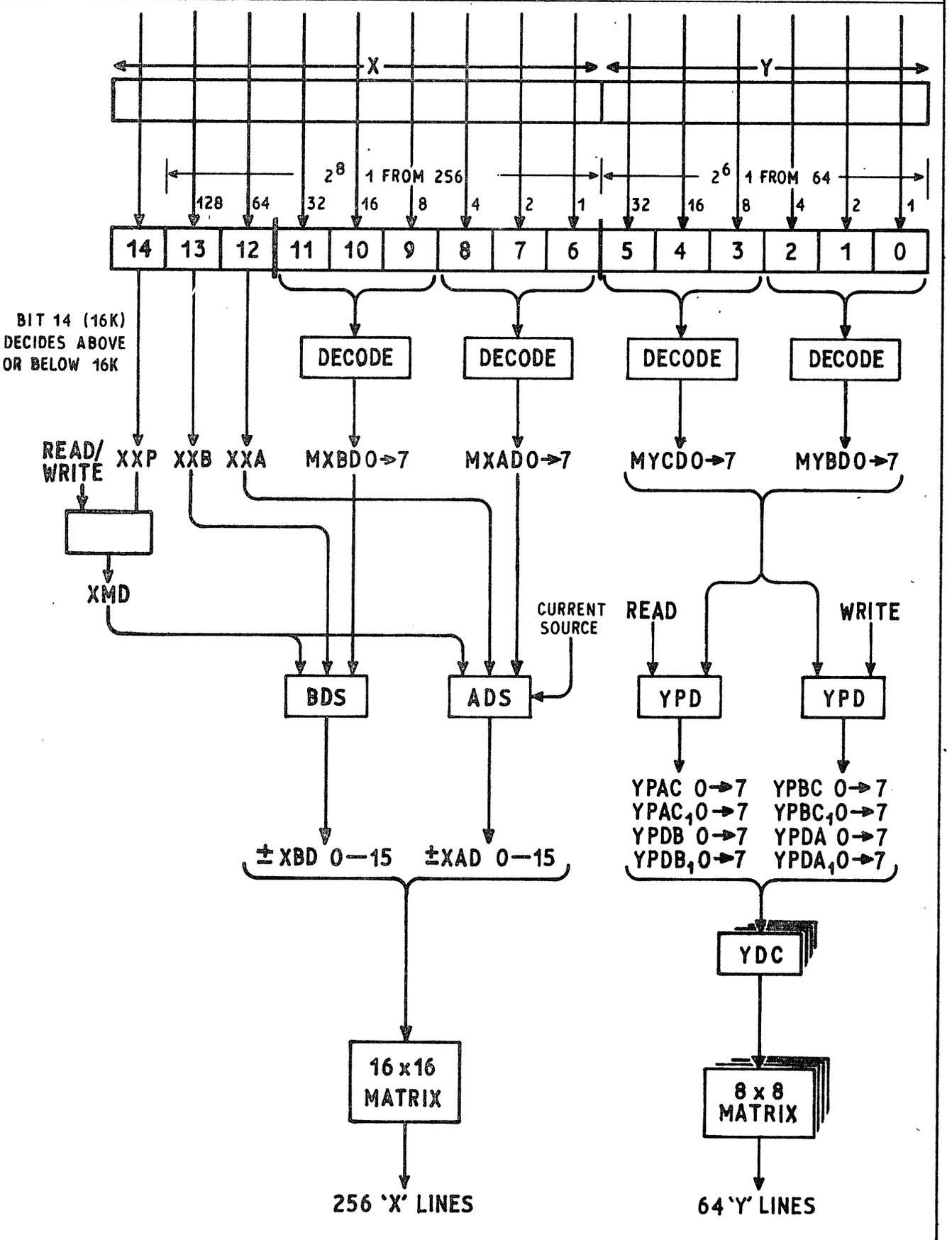
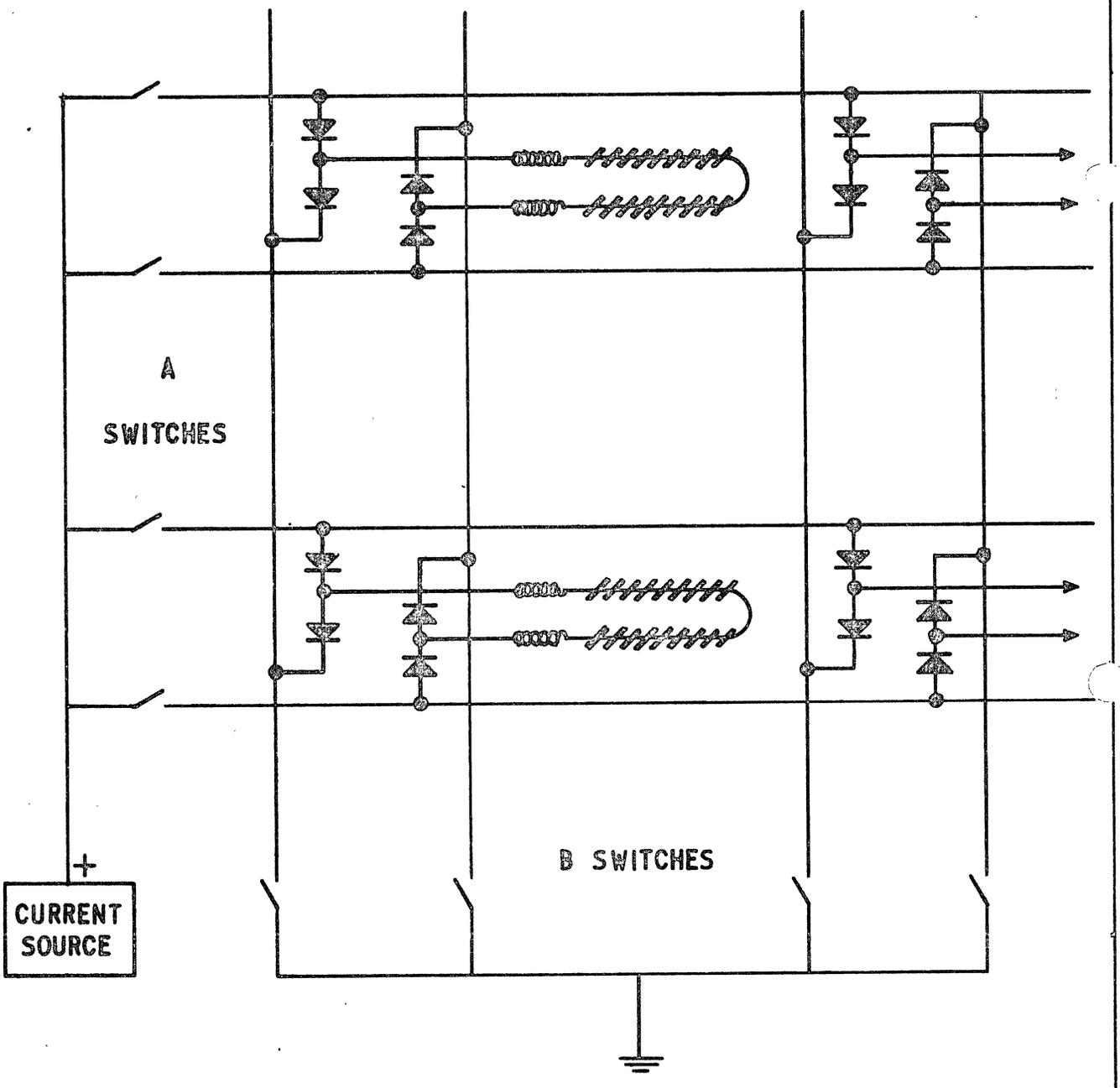
ADDRESS DECODE

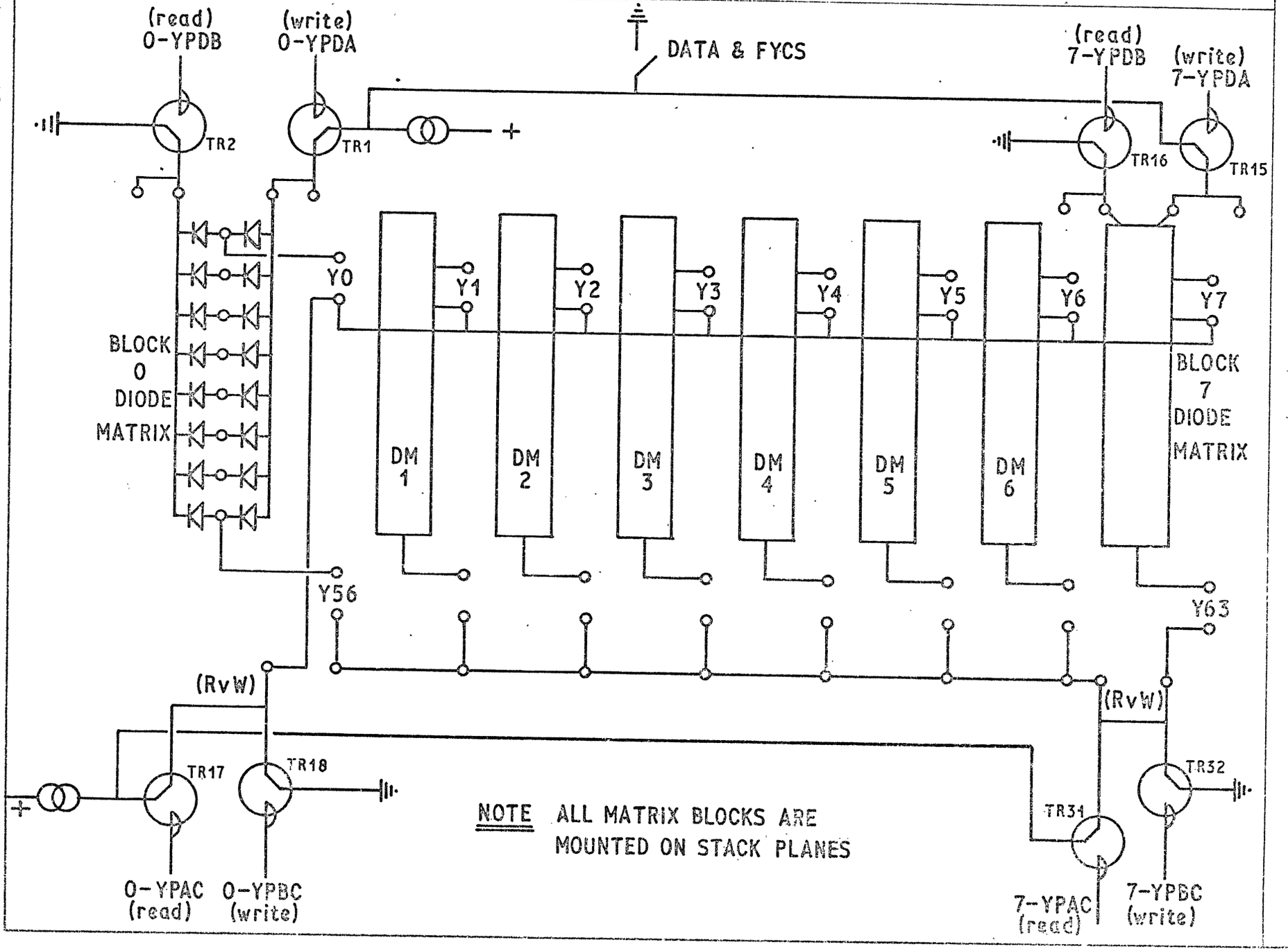
Iss 1.



X DRIVE AND MATRIX



Y ADDRESS DECODING



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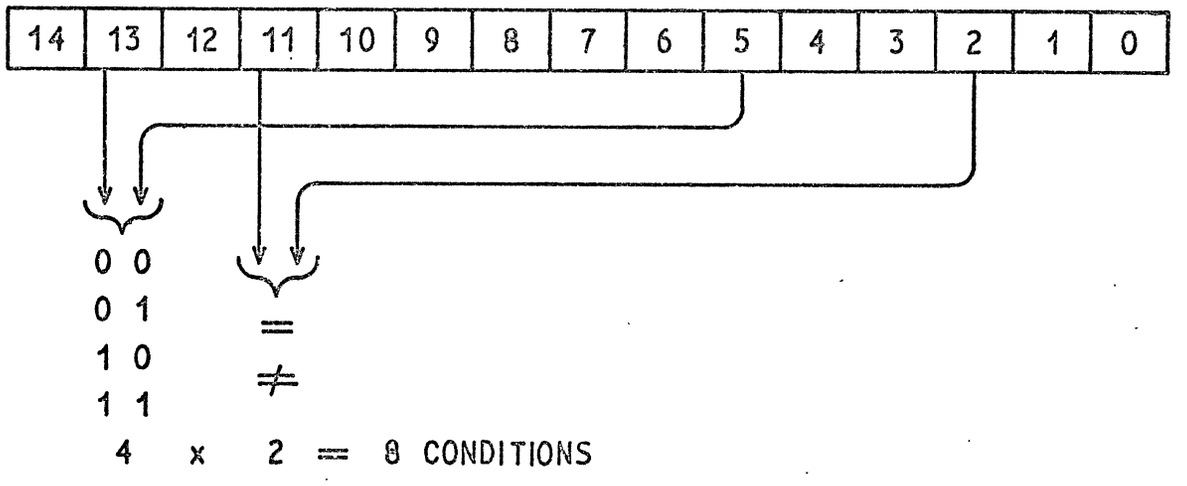
Iss 1.2

SENSE WIRING

Iss 1.

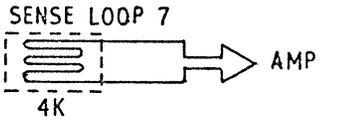
EACH PLANE HAS 16 SENSE WIRES AND SINCE THE PLANE HAS 64K AS 2 BITS OF 32K, THERE ARE 8 SENSE WIRES FOR EACH BIT.



4 x 2 = 8 CONDITIONS

−6v AND TTL LOGIC

SYSTEM 893		BITS 0−11		BITS 12−24	
2^{13}	2^5	$2^{11}=2^2$	$2^{11}\neq 2^2$	$2^{11}=2^2$	$2^{11}\neq 2^2$
0	0	S7	S5	S6	S8
0	1	S4	S2	S3	S1
1	0	S8	S6	S5	S7
1	1	S3	S1	S2	S4



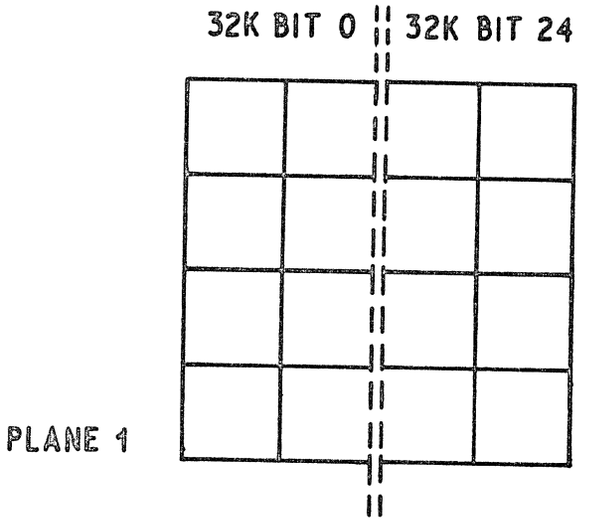
ECLE

SYSTEM 894		BITS 0−11		BITS 12−24	
2^{13}	2^5	$2^{11}=2^2$	$2^{11}\neq 2^2$	$2^{11}=2^2$	$2^{11}\neq 2^2$
0	0	S3	S1	S2	S4
0	1	S8	S6	S5	S7
1	0	S4	S2	S1	S3
1	1	S5	S7	S8	S6

FOR LOGIC ABOVE USED WITH 2^5 INVERTED

SIMPLIFIED SENSE WIRE DISTRIBUTION

not as on actual plane



NOTES:

SENSE LINES FOR EACH 4K OF BIT ARE SPECIALLY INTERCONNECTED TO REDUCE INTERACTION.

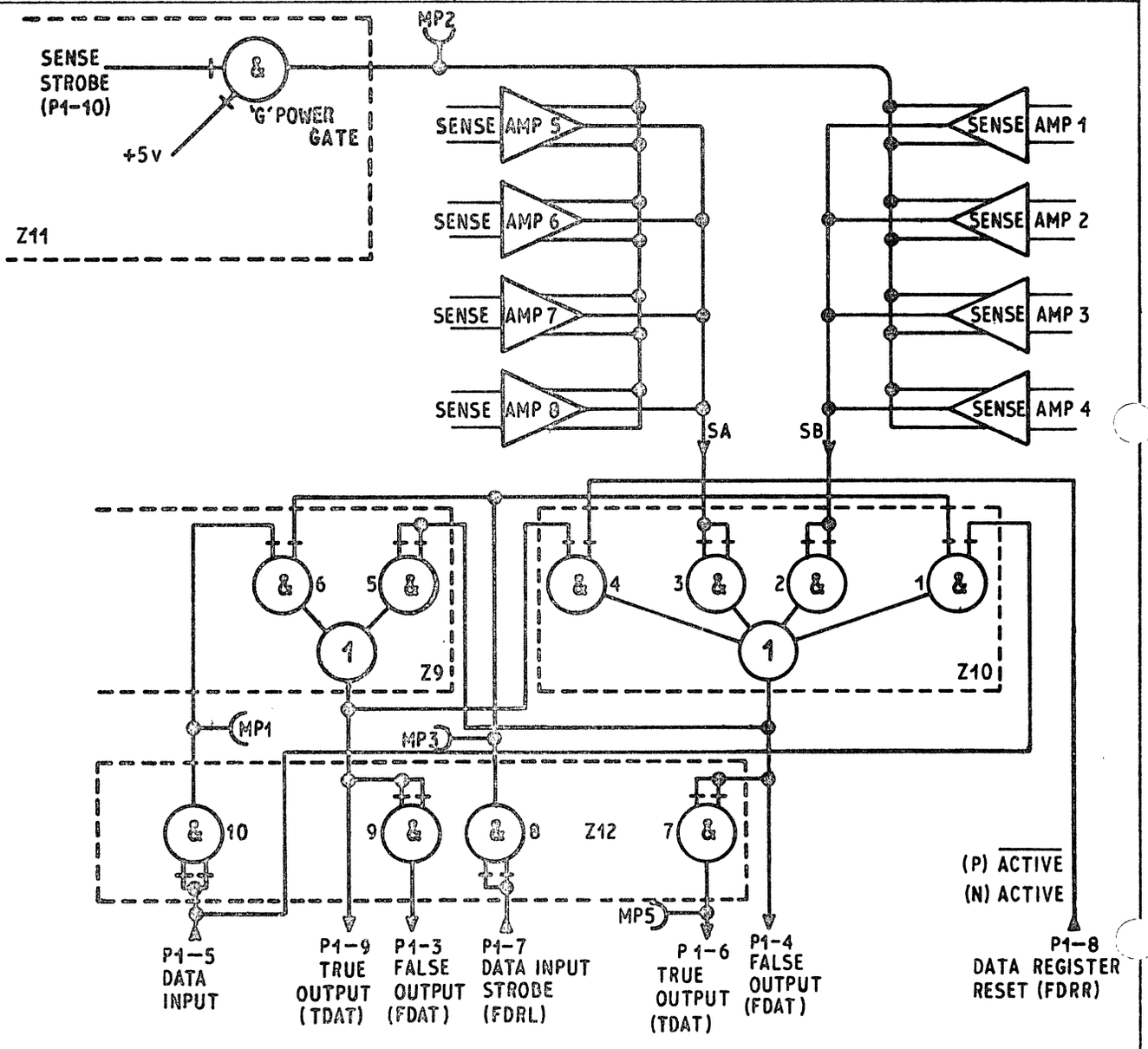
THE YDC BOARDS HAVE THE 8 SENSE AMPLIFIERS DEALING WITH A PARTICULAR BIT,

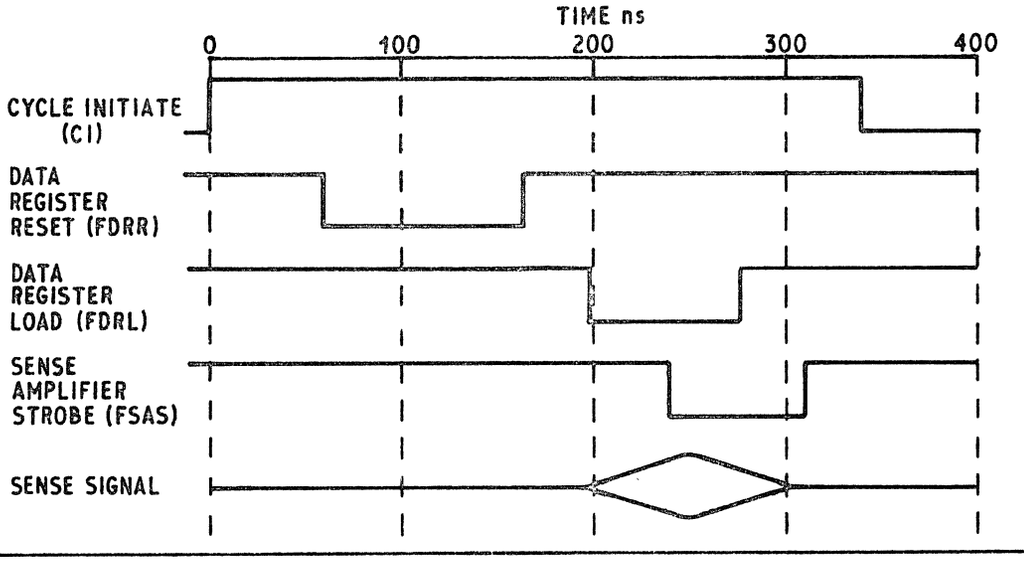
E.G.

BIT 0 IS ASSOCIATED WITH YDC BOARD IN POSITION 2 AT THE RIGHT HAND SIDE OF THE STORE LOOKING FROM THE FRONT.
REFERENCE. LOP 0270.

DATA REGISTER AND TIMING

Iss 1.





LOC	PIN
C09	49
A01	68
D03	12
A01	58

 ETD 3451

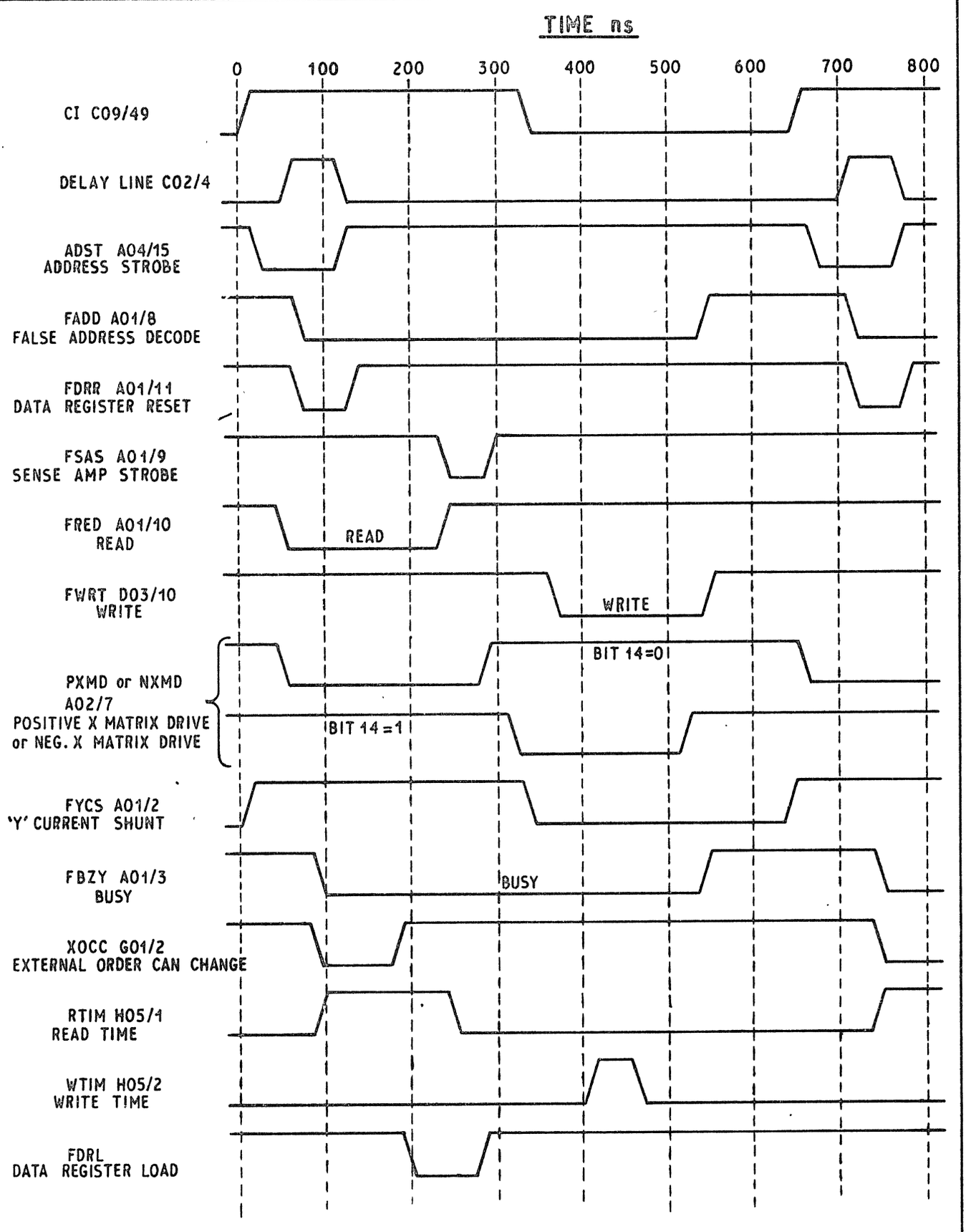
International Computers Limited

1904A MODULE 4.

No. BB006
Sheet 2.13

MAJOR CONTROL WAVE-FORMS RELATIVE TIMING DIAGRAM

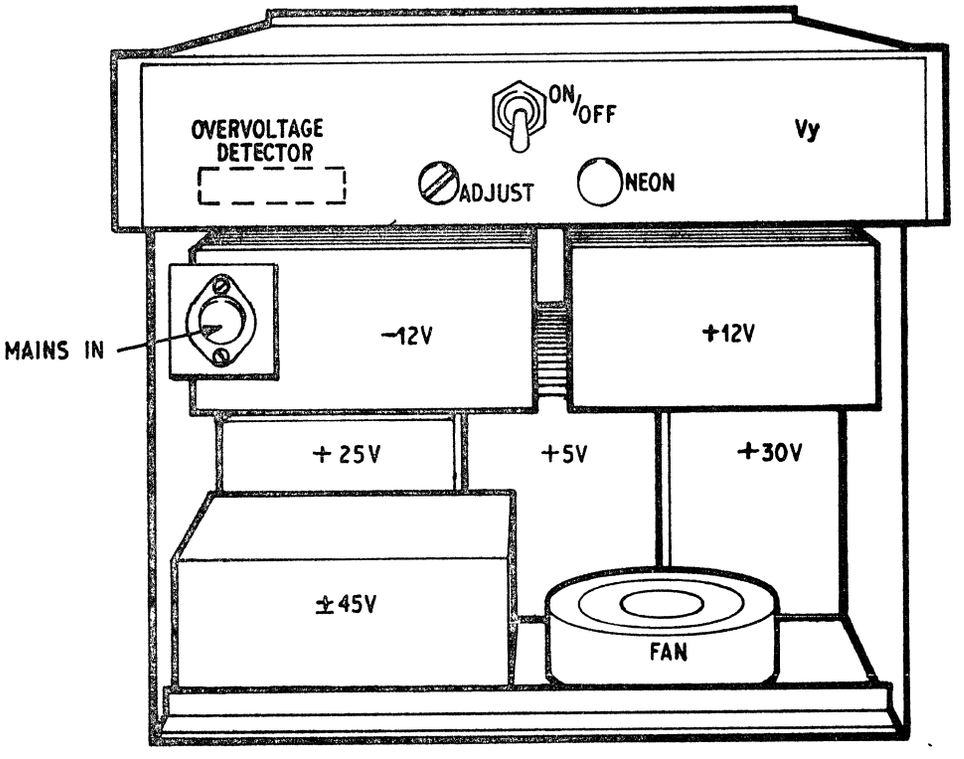
Iss 1.



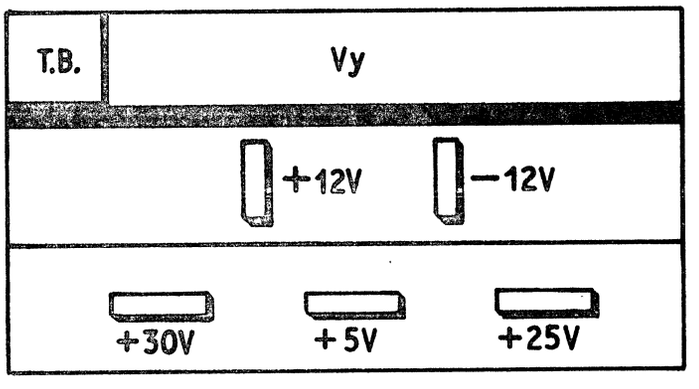
Self Test

 ETD 3452 FORM 8/133/B(2.69)

POWER SUPPLY UNIT REAR VIEW



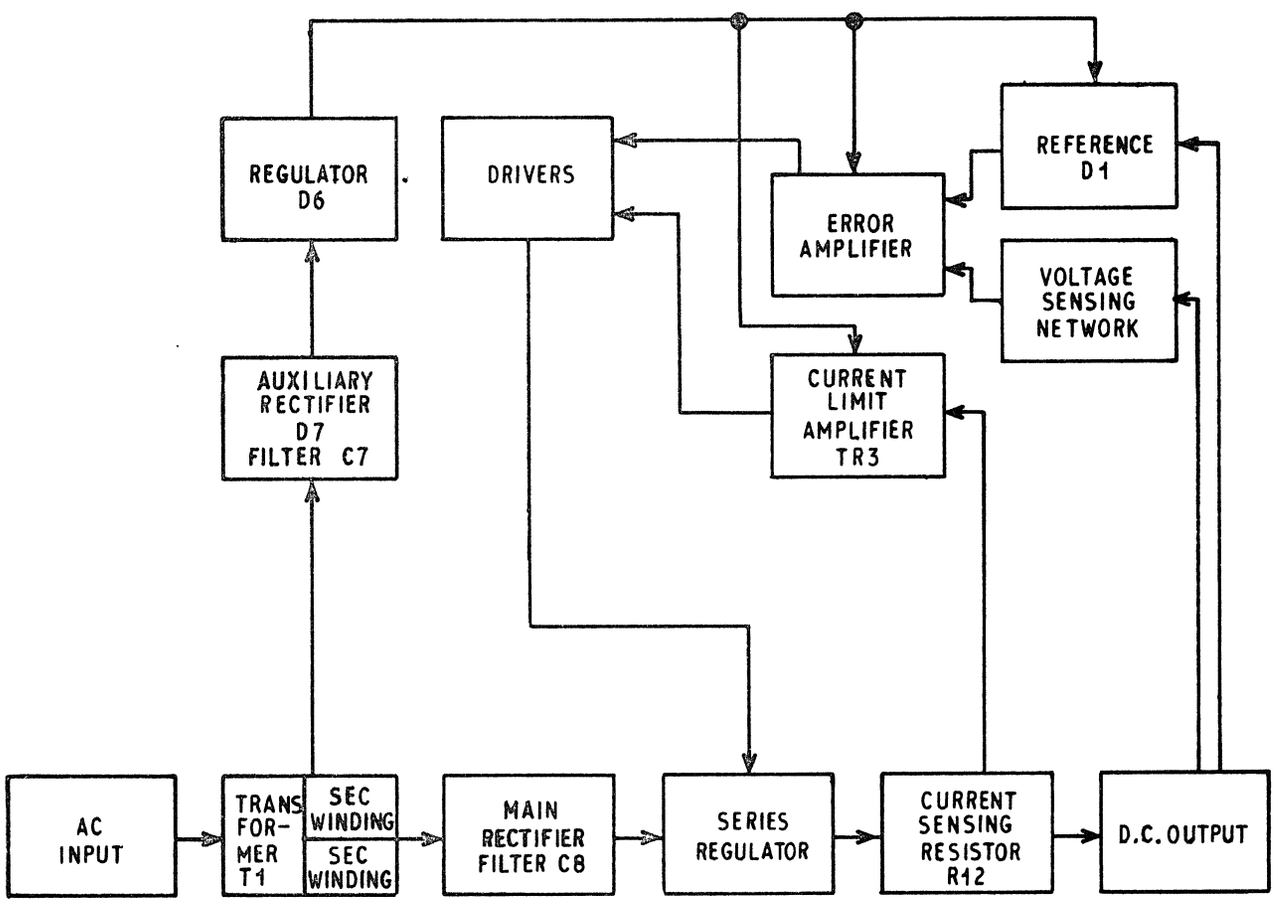
OVERVOLTAGE PROTECTION UNITS FRONT VIEW



Vy PROTECTION UNIT MOUNTED BEHIND REAR PANEL.

LAMBDA POWER SUPPLY MODULE—BLOCK DIAGRAM

Iss
1.
2

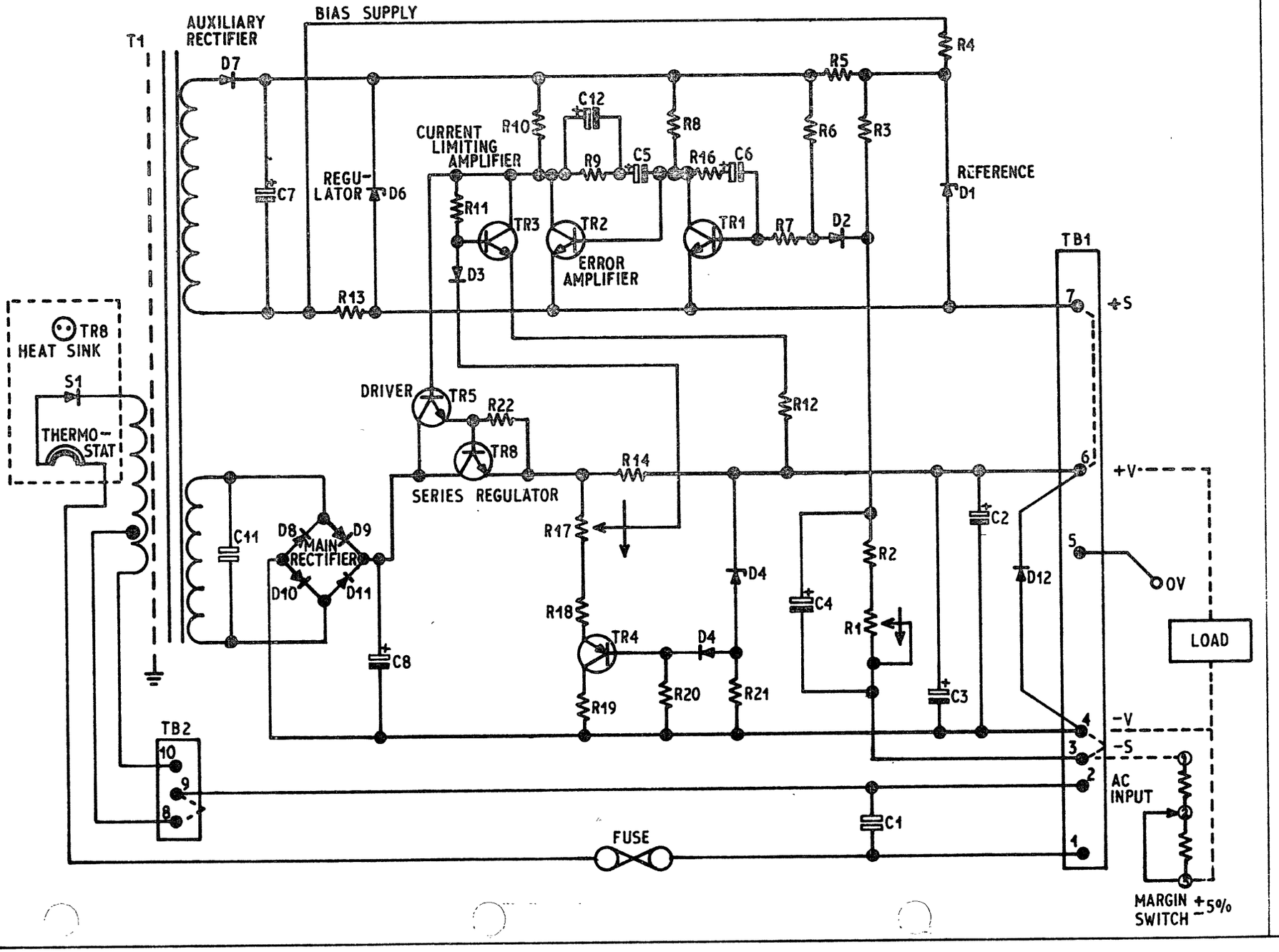


 ETD 3454A

ETD 3455

LAMBDA POWER SUPPLY MODULE—TYPICAL CIRCUIT DIAGRAM

Iss 1.



International Computers Limited

1904A MODULE 4

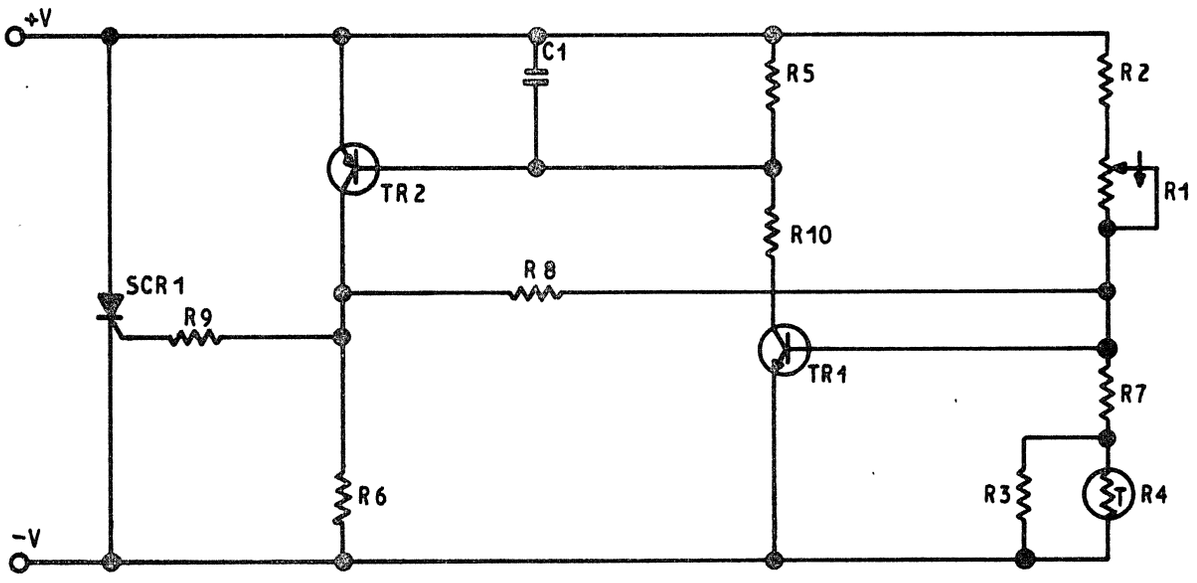
No. BB006
Sheet 2.16

ETD 3455 FORM 8/133/B(12 69)

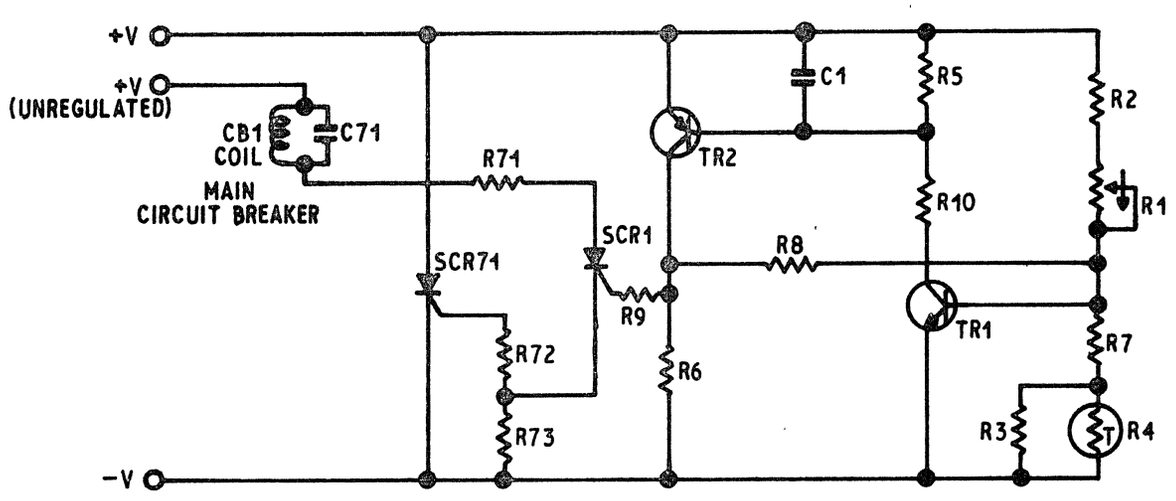
OVERVOLTAGE PROTECTION

Iss 1.

TYPICAL CIRCUIT DIAGRAM



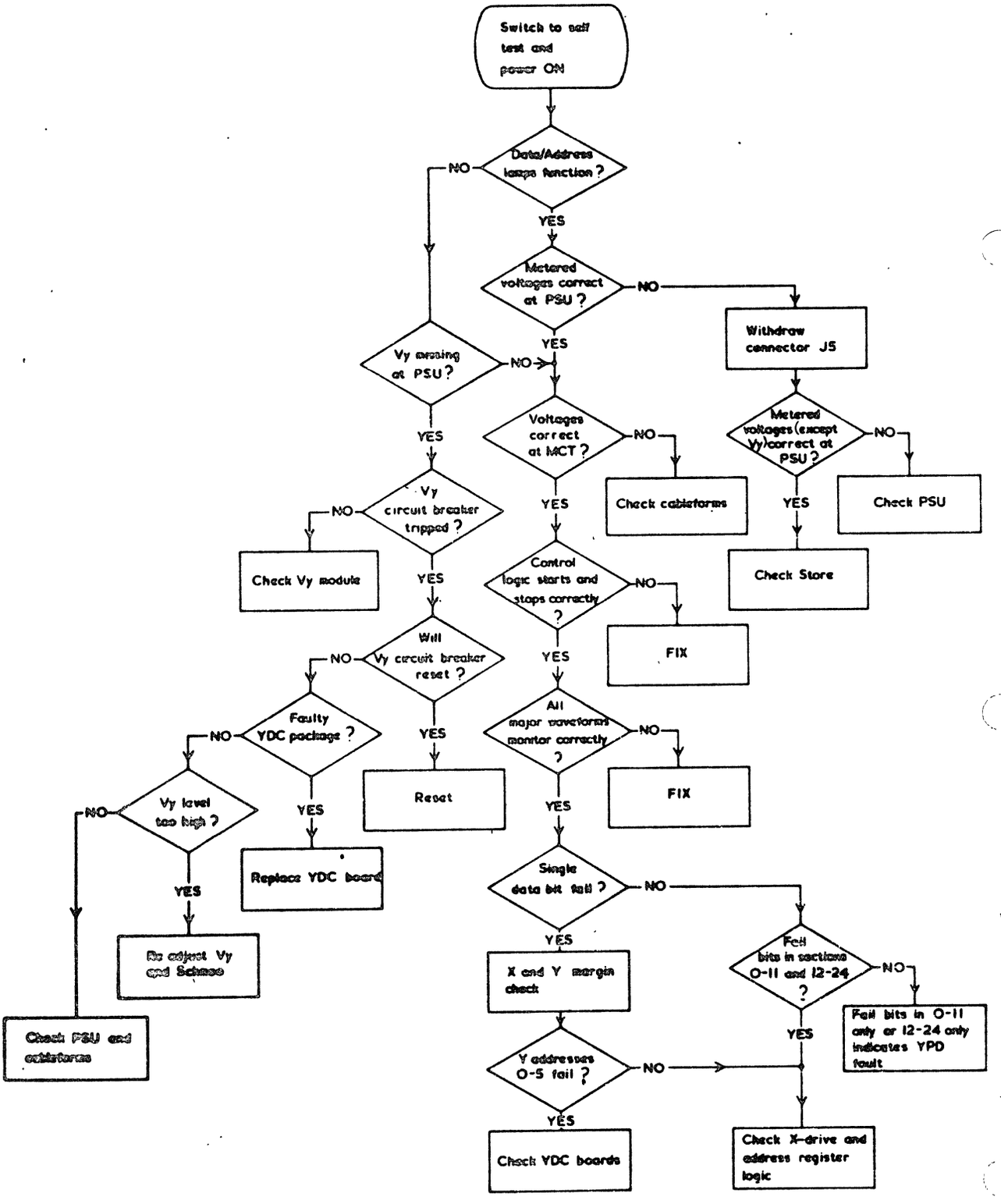
+Vy CIRCUIT DIAGRAM



 ETD 3456

Iss 1.

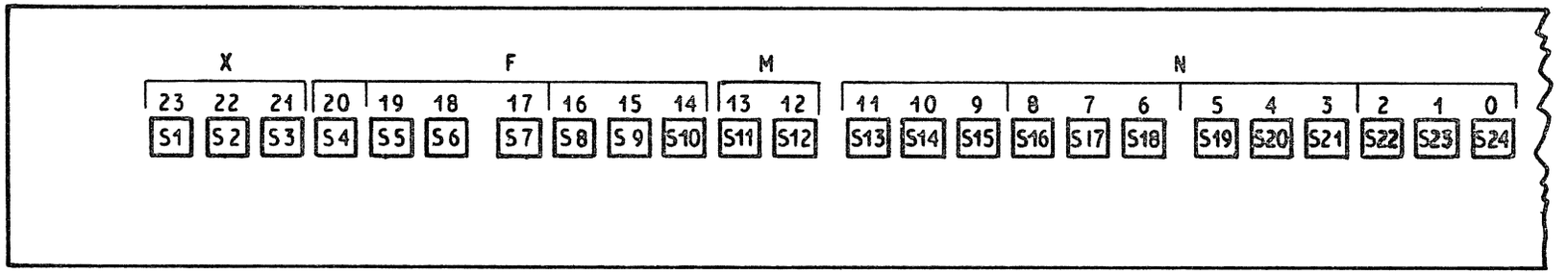
SIMPLIFIED FAULT FINDING FLOWCHART

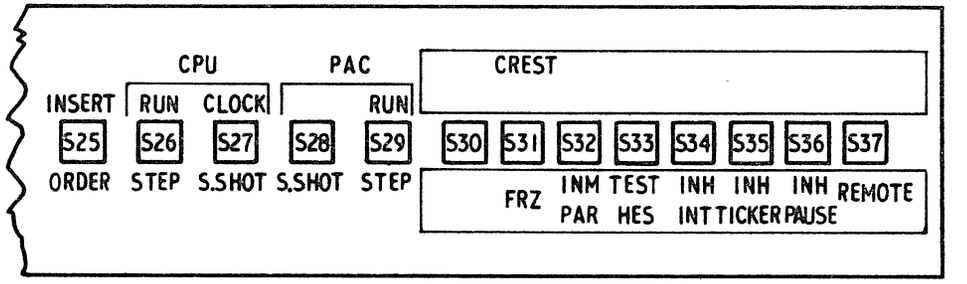


 ETD 3457

ENGINEERS SWITCHES

Iss 1.





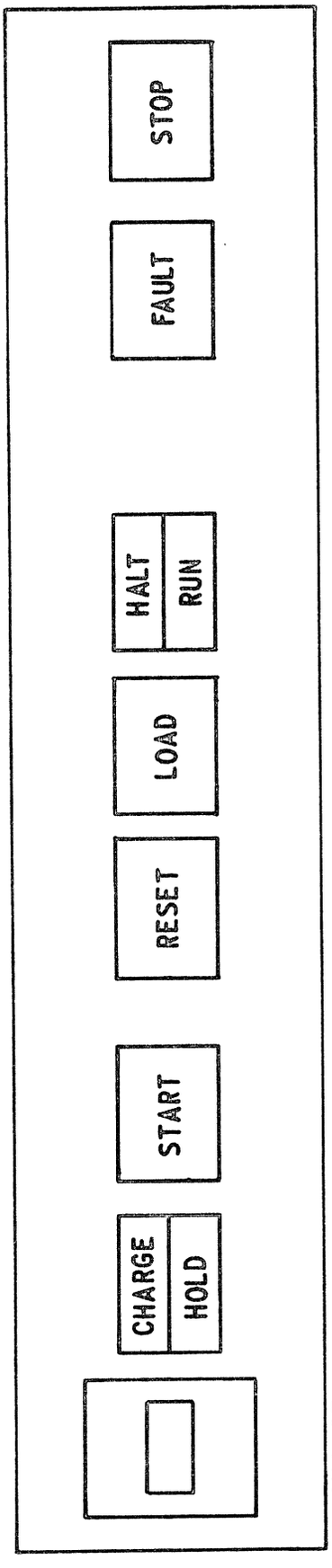
International Computers Limited

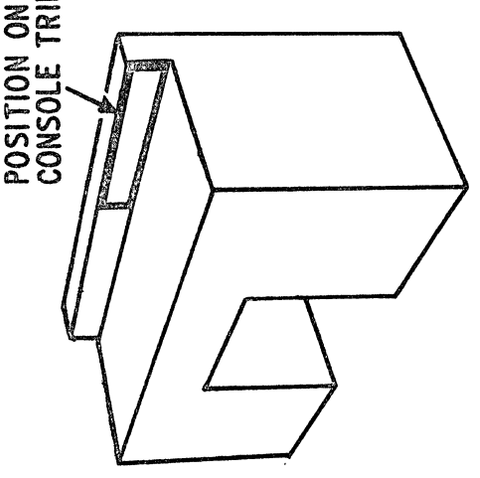
1904A MODULE 4

No. BB006
Sheet 3.1

Iss 1.

LAYOUT OF REMOTE SWITCH PANEL





 ETD.3459

FUNCTION OF ENGINEER'S PANEL.

The Engineers Panel

This panel carries a number of switches and indicator lights intended for use by the engineer when testing the machine. The panel is hinged at one edge to form a door which, when opened, allows access to the inter-connecting wiring of the black planes behind it. In the normal operating state the door is closed and covered by a panel.

The Handkeys A row of switches numbered 1 to 37 (see Diagram 10) is fitted across the top of the engineers panel and the functions of these switches are described below.

S1 to S24

Can be used either as an instruction or data depending upon the position of S25. The switches are marked according to their bit significance in descending order from the left and the grouping of the bits into parts of an instruction (XFMN) is also indicated.

S25 INSERT/ORDER

With S25 in the ORDER position and assuming S26 is in the ONE INSTRUCTION position then, when the S.SHOT switch is depressed, the CPU will obey the instruction set on the handkeys S1 to S24. In order to write some data to a particular store address, this address must first be fed in on the handkeys as an instruction.

The data is then fed in by setting the switches S1 to S24 as required, placing S25 in the INSERT position and depressing the S.SHOT switch.

The switch is placed in the OFF (centre) position for normal operation of PAC.

S26 RUN/ONE INSTRUCTION/STEP

If RUN is selected then the CPU runs normally. When ONE INSTRUCTION is selected and the S.SHOT switch depressed, sufficient pulses are produced to allow one instruction to be carried out. The STEP position enables one V beat for each depression of the S.SHOT switch.

S27 CLOCK/S.SHOT

CLOCK is a facility for slowing the clock pulse rate to ten pulses per second. This is useful for test purposes. The S.SHOT position, as already indicated, is used to trigger the single shot and single instruction facilities.

S28 PAC S.SHOT

As indicated above the S.SHOT switch triggers the step or step pairs which enables the engineers to work through the functions which occur by observing the indicator lamps.

S29 RUN/ONE INSTRUCTION/STEP

When RUN is selected, PAC functions normally. In the central position, i.e. ONE INSTRUCTION, sufficient clock pulses are produced to enable a complete instruction to be carried out (e.g. one step pair) when the PAC S.SHOT switch is depressed. If STEP is selected, then one step occurs for each depression of the PAC S.SHOT switch.

S30 NOT USED.

S31 CREST/FREEZE

In the 'UP' position, CREST is selected which first applies a general reset and then initiates the input of a bootstrap program from a peripheral whose absolute number and style bits have been included in a control word, previously set up on S1 to S24.

When the 'DOWN' position is selected, (i.e.FREEZE) a general reset occurs to put the machine in a suitable starting condition after a fault has occured, or after switching on initially. It also activates the 'G' line in the standard interface to reset all peripherals.

S32 (INHIBIT PARITY)

The switch has two functions:-

a) To inhibit the action of the parity fail logic

b) to restart the CPU and PAC after a parity fail has occured.

S33 TEST HESITATION

Simulates a hesitation request for test purposes. The hesitation request produced has a high priority status but otherwise is dealt with normally.

S34 INHIBIT INTERRUPT

Inhibits all interrupts when ON.

S35 INHIBIT TICKER

Inhibits the action of the Real Time Clock.

S36 INHIBIT PAUSE

In a normal Read Pause Write cycle, the 'Read' portion of the cycle clears the store location. During the 'pause' following the store control takes no action, but the main microprogram may perform an operation. The pause is normally of one beat duration and during this period the microprogram retains control of the store.

New information is then written into the cleared location. This method of writing to store reduces the central processor time required to complete the operation, but results in an increase in total time the store is occupied.

The alternative method of writing to store is to carry out two separate operations, first a 'read store' and then a 'clear write'.

This sequence is automatically followed when INHIBIT PAUSE is made. It is less economical in central processor time but more economical in store time and it may therefore be used in conditions where the store is likely to be very busy, i.e. where the P.A.C. has a large number of peripherals or where dual processors are in use.

S37 (REMOTE LOCAL)

Enables power supplies to be switched ON or OFF from either a remote position or at the power supply unit. This switch has its main application in multi-processor systems. Two safety precautions are incorporated in the switching arrangements:-

a) If any switch with the exception of the RUN switches, is left in the ON position, the ENGINEER light on the console typewriter is automatically illuminated.

b) With the RUN switch in the ON position, operation of the FREEZE switch has no effect. With the FREEZE switch in the ON position, operation of the RUN switch removes the FREEZE signal.

Indicator Lamps The engineers panel carries 26 rows of indicator lights, 25 of which are used (the bottom row is spare). Each light is illuminated when the signal it represents is active, whatever its phase. The lights show the contents of all registers, mills and highways, throughout the computer, with the exception of the store, which has its own 'indicators'.

For convenience of reference, the rows of indicator lights are grouped so as to show operations in three main areas of the processor as follows:-

Rows 1 - 11 - Central Processor
Rows 12 - 17 - PAC
Rows 18 - 26 - FPU

A list of these signals monitored on rows 12 to 17 is given at the end of the section.

Iss 1.

LOADING 'EXECUTIVE' PROGRAM

1. Load 'EXECUTIVE' program to desired INPUT media.
   i.e. Program may be on Paper Tape, Cards or held on the Engineers Library tape PROGRAM ELIB.

2. C.P.U. and P.A.C. clocks off "RUN".

3. Set SOCKET No. of I/P device to Handkeys.

4. Operate FRZ and CREST switches.

5. P.A.C. Clock RUN.

6. C.P.U. Clock RUN.

7. Block of program read into Store and program obeyed. (BOOTSTRAP program).

8. If P.T. or CARDS, EXECUTIVE then loaded to Store.

9. If M.T., following message o/p on Console Typewriter:-

   LIB NUMBER/HOW MANY K?
   Answer:- EXECUTIVE LIB. NUMBER/SIZE OF CORE
   e.g. 0002/32
   On pressing ACCEPT, the Bootstrap program searches tape for desired EXECUTIVE program.
   The next step common to all methods of loading EXECUTIVE.

10. When EXECUTIVE loaded, details of the program are o/p on the Console Typewriter ending with the question:-
    ANY MODIFICATIONS?
    If No, Type 'N' and press Accept.
    If Yes, Type 'Y' and press Accept.

    For full details, see 'EXEC MK5 LOADING FACILITIES'.

11. If no modifications required or when all modifications have been input, the following messages are output:-

    (a) DATE PLEAST - Answer with correct date in format:- FRI17MAR72
    (Spaces between are allowed)

    (b) TIME PLEASE - Answer with correct time in format:- 1149

12. Having input this information, EXECUTIVE may be considered to be loaded.

    All Mag Tapes or Discs on line are searched and their Names and/or Ser No's are printed on T/W Console.

Iss 1.

ORDER AND INSERT FACILITIES

1. Order

The instruction is taken from the handkeys and data (inc. modifier) from store or H'ware Accs.

2. Insert

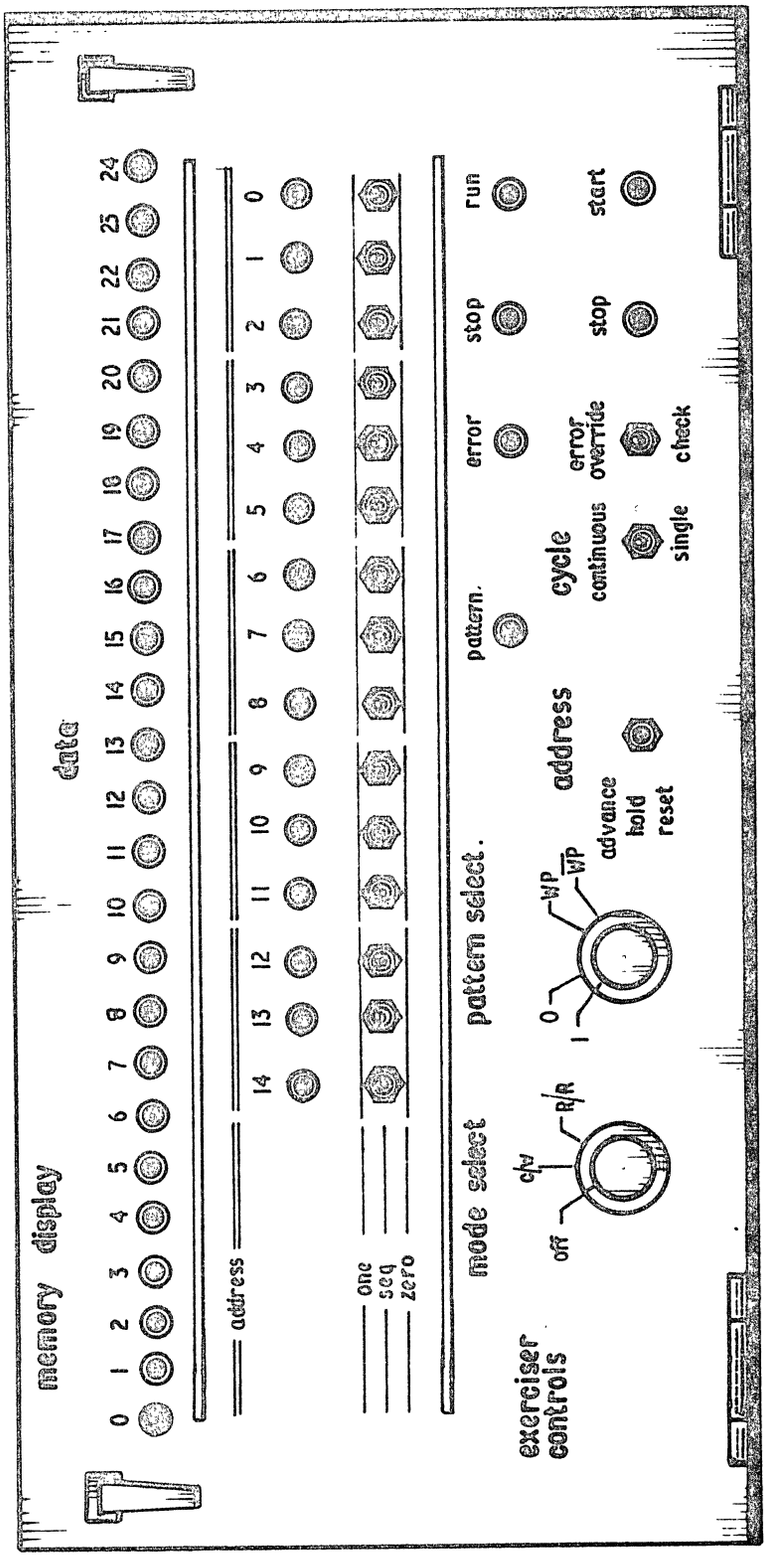
Data set up on handkeys may be loaded to a selected store location.

Using Insert Facility

1. Set 074 0 /N (where 'N' = store address) on handkeys.
2. Using ORDER, perform operation.
3. Switch to INSERT.
4. Set Required data to handkeys.
5. Press SSHOT
The operation loads store and increments address by 1. Therefore if consecutive locations to be loaded, continue from No.4.
Otherwise continue from No.1.

Iss
1.

LAYOUT OF SELF TEST PANEL



Iss 1.

ICL 650ns (LOCKHEED) STORE

SELF EXERCISER

1. CONTROLS

a) Mode Select

OFF - Normal ON-LINE operation.
CW - Clear Write - No checks.
RR - Read Restore - Check on data read out.

b) Pattern Switch

Selects pattern written to store
All ONES, All ZEROES, WORST PATTERN OR WORST PATTERN COMPLEMENTED.

c) Address Switch

Advance - Memory cycles through all addresses.
Hold - Memory cycles on one fixed address.
Reset - Clear Address Register.

d) Cycle Switch

Selects single or continuous store cycles.

e) Error Switch

Check - Memory stops cycling if fault detected; Fault lamp lit.
Override - Memory does not stop cycling if fault detected; Fault lamp lit for faulty locations.

f) Start/Stop buttons

g) Address Switches

May be used to hold selected address bits to their 'zero' or 'one' state if required.

2. VISUAL INDICATORS

Indicators are provided for the following:-

a) Data
b) Address
c) Start/Stop
d) Error
e) Pattern

Note - On early LOCKHEED STORES the DATA & PATTERN lamps have reverse meaning (i.e. GO OUT for logic '1')

STORE - POWER SUPPLY

The following facilities are provided:-

1. Monitoring of all voltages.
2. Margin switches for all supplies.

INTERRUPTS.

The Normal Mode Interrupt sequence provides a means of entry to EXECUTIVE when an incident occurs during Object Program running requiring Executive action.
There are two types of entry to EXECUTIVE.

1. VOLUNTARY.

Any Extracode order given in OBJECT prgoram will cause a VOLUNTARY entry to EXECUTIVE. These orders are performed by EXECUTIVE ROUTINES.

(ENTRY POINT - *40)

2. INVOLUNTARY.

Any Peripheral or Processor incident occuring whilst running in Object mode will cause an INVOLUNTARY entry to EXECUTIVE.

E.G. Peripheral raises 'B' line (STOP HOLD BUTTON)
Ticker
Monitor Mode
Reservation Fail or Illegal Order.

EXECUTIVE investigates incident and takes appropriate action.

(ENTRY POINT - *20)

Before entry to Executive, certain Object program data must be preserved. This performed by a hardware INTERRUPT SEQUENCE.

Action of Interrupt Sequence.

1. Store Hardware Accumulators to Object Program locations Ø - 7.
2. Extracode 'N' field ⟶ EXEC ACC 1.
3. Relative C.I.A. to D+8.
4. ZS & ASTAT ⟶ D+9.
5. F.P.U. to D+12 & 13.
6. Extracode FXMN ⟶ Exec Acc 2 (If EXCD entry).
7. SET EXECUTIVE MODE.
8. Generate desired Entry Point Address.
9. Enter EXECUTIVE PROGRAM.

For INVOLUNTARY entries Executive must ascertain 'WHO' interrupted.

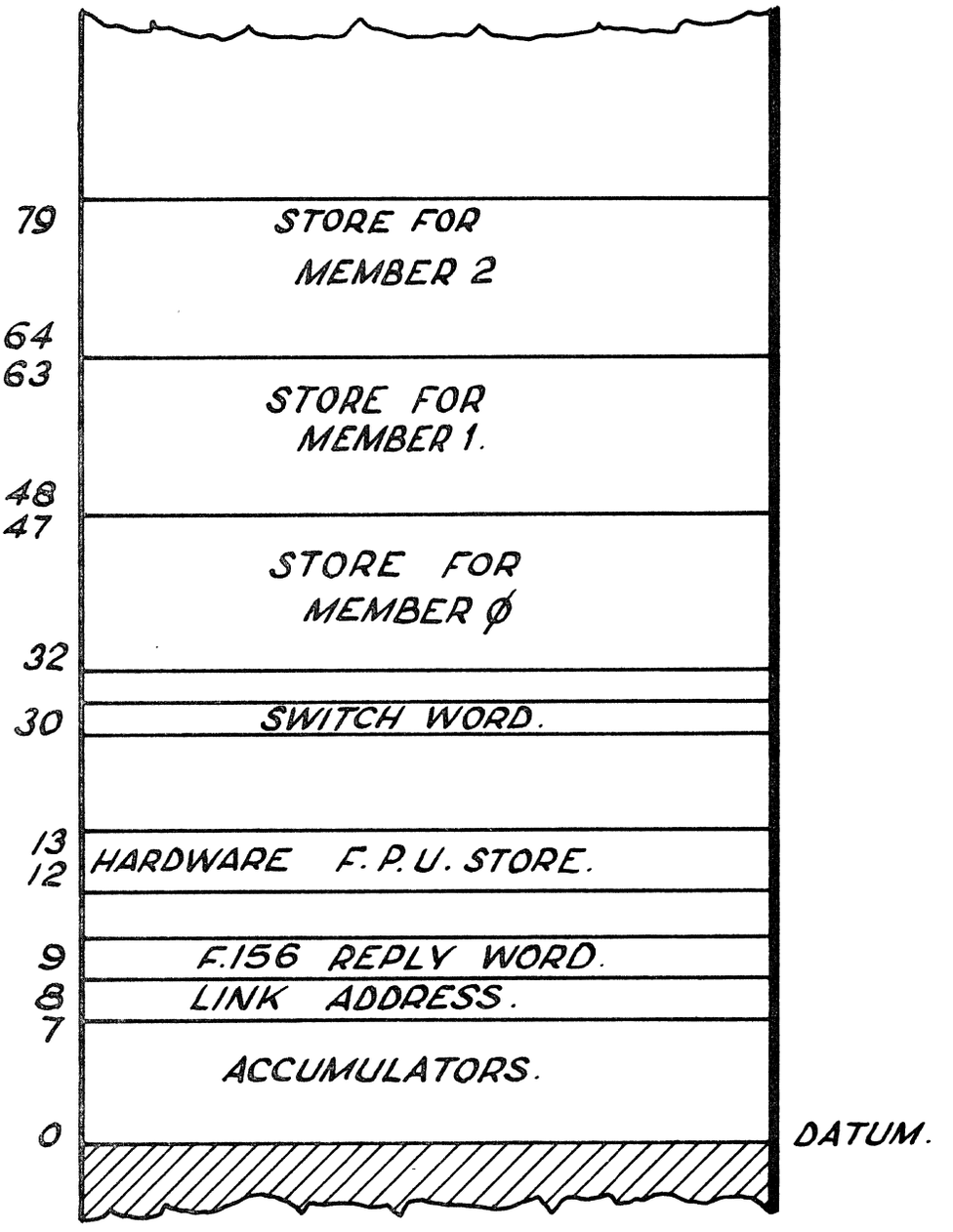
Information on WHO interrupted is available to EXECUTIVE from "SPECIAL REGISTERS".

For Basic Processor & Peripherals these are known as SPECIAL REGISTER 64 & 65. These registers are formed by the devices INTERRUPT lines.

1

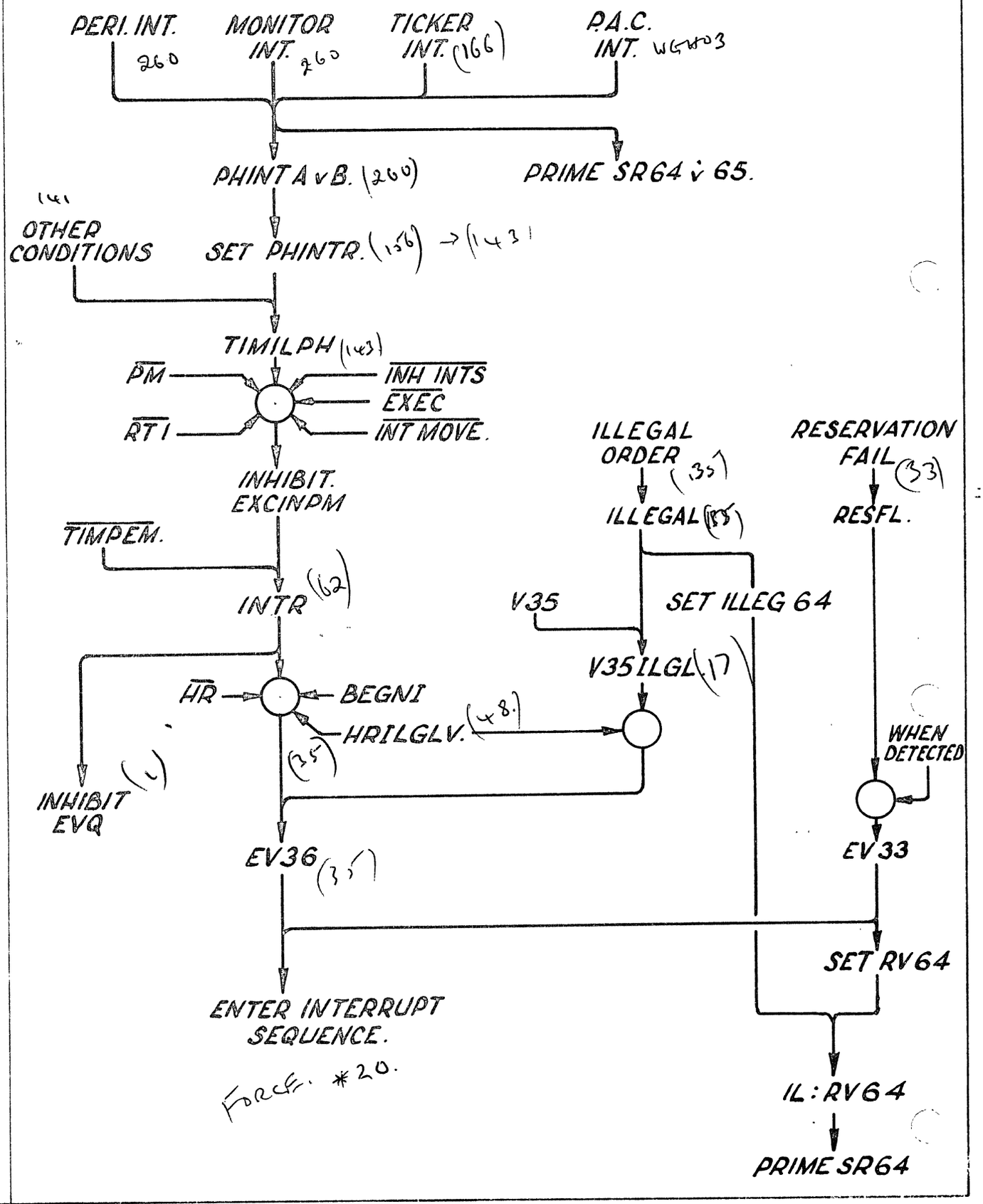
RESERVED AREAS IN OBJECT PROGRAM.

e.g. A THREE MEMBER PROGRAM.

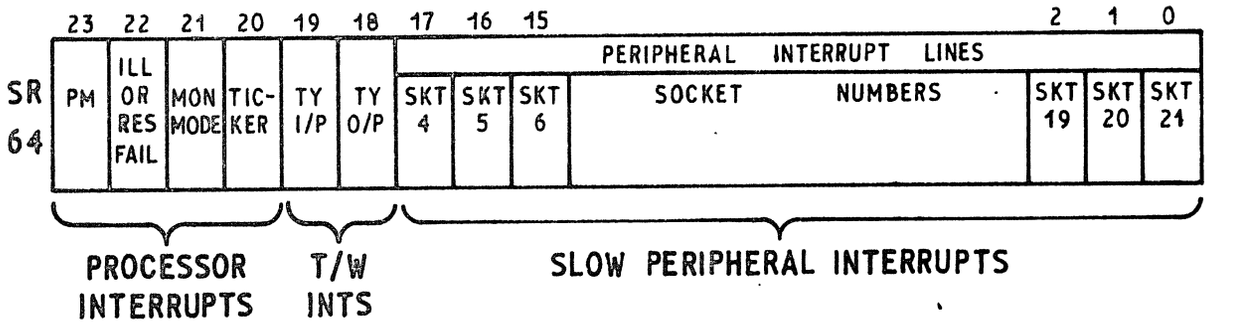


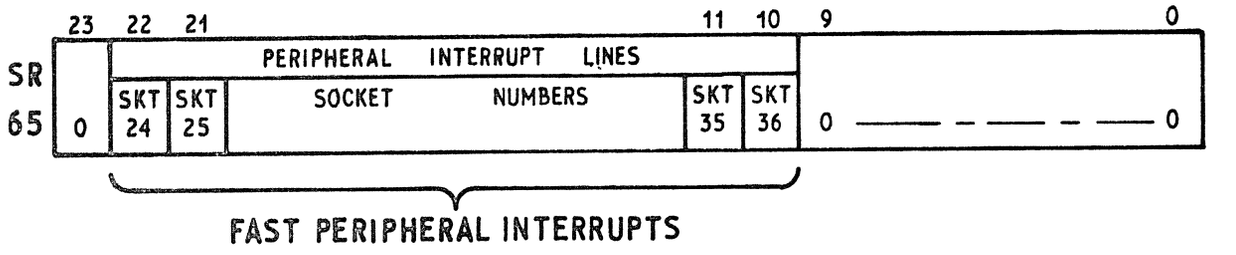
INTERRUPTS.

1. EFFECT OF A PERIPHERAL OR PROCESSOR INCIDENT.

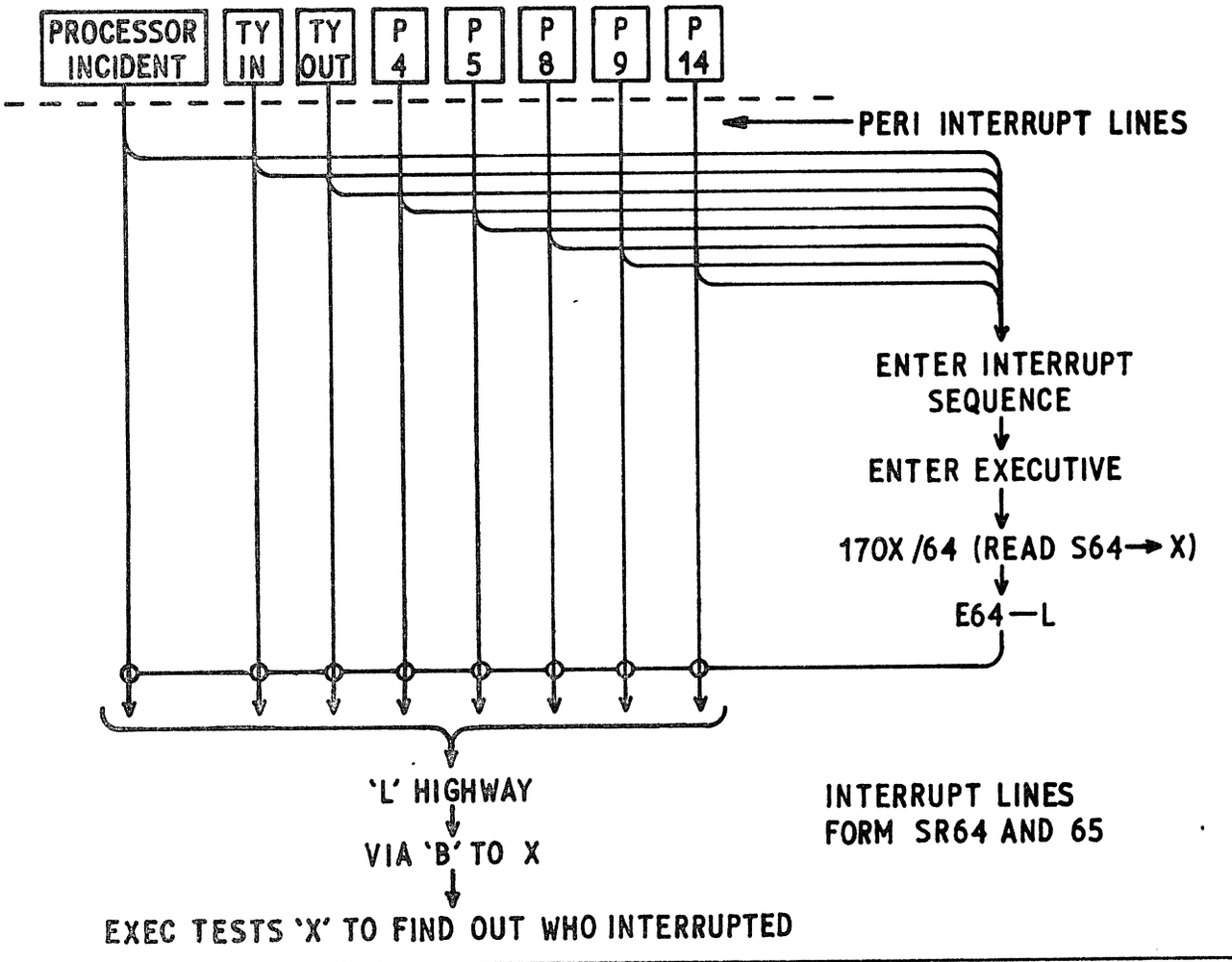


FORMAT OF SPECIAL REGISTER 64 & 65





SIMPLIFIED ACTION OF USE OF SR64



Iss /.

SPECIAL EXECUTIVE FUNCTIONS (GP17)

1. F17OE

Format - Normal

The 'N' field is literal and its value determines the action of this function.

a) N ≥ 64

Sense the state of S.R64 or 65 and place this information in X.

b) N < 64

Sense the state of :-

1. Mill Timer if N = 1
2. Typewriter I/P if N = 2
3. Typewriter O/P if N = 3

Place information in X.

2. F171E

Format - Normal

Action Send a command to the console Typewriter. X contains the command. N is literal and it's value determines the I/P or O/P side of the typewriter.

N = 2 - I/P
N = 3 - O/P

Summary of Commands and Responses.

1. Commands.

Bit Ø of X = 1 - Start
Bit 1 of X = 1 - Stop

2. Responses.

Bit Ø - End of Transfer
Bit 5 - Busy
Bit 6 - I/P Push Button
Bit 7 - Cancel Push Button
Bit 8 - Accept " "
Bit 9 - F1 " "
Bit 10 - F2 " "
Bit 11 - F3 " "
Bit 12 - F4 " "
Bit 13 - F5 " "

3. F172E

Format - Normal

Used by Executive to exit to an Object program.

X is zero by convention.

N(m) specifies the start address of a two word area in Executive holding selected programs. DATUM, LIMIT and 'G' Register information.

Action

1. Load D, L and G registers from n and n + 1.
2. Load F.P.U. from D + 12 and 13.
3. Retrieve ZS information from D + 9.
4. Retrieve link address from D + 8.
5. Unload D + Ø to D + 7 to Hardware Accs.
6. Exit to object program.

4. F 173E

Format - Normal

Action

Load D, L and G registers from n and n +1; remain in Executive program.

5. F174E

Format - Normal

Used to send a command to a S.I peripheral specified by literal N(m).

The command is held in char 3 of X.

The response to the command will be placed in a selected char position of X.

If the instruction is not modified the response will be placed in char 3 of X overwriting the command.

Typical Commands and Responses.

1. Commands.

*31 - Read) Not P.T. — depends upon mode ref 17 Manual.
*32 - Write)
*20 - SSQ
*24 - SSP
*36 - Disconnect.

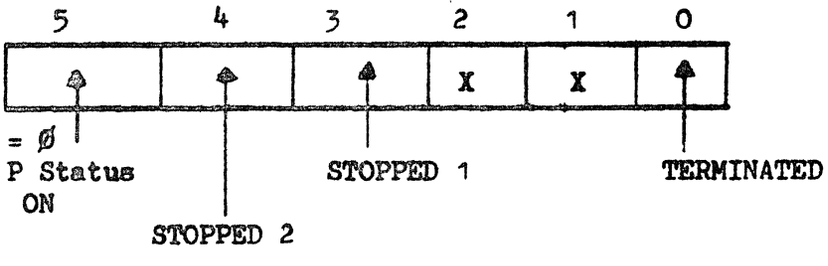
2. Responses.

a) Direct.

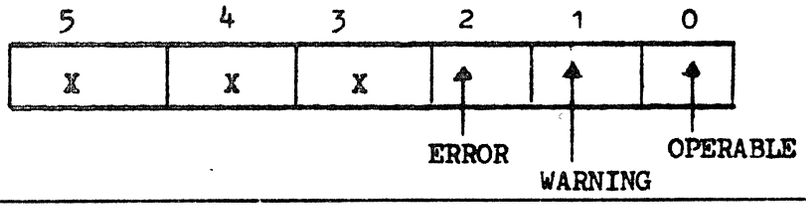
*05 - Accepted
*03 - Rejected
*00 - Inoperable

b) Status

Status Q (Basic Peris)



Status P (Basic Peris)



Iss 1.

6. F175 & 176

Null on 1904A.

7. F177E

Format - Normal

Set 'C' if the absolute address in X is < Datum and ≥ limit.

Data Transfers.

In the 1904A two types of data transfer systems are used.

1. SLOW HESITATION CONTROL for Slow Peripheral Transfers.
   (Transfer rate $\leq$ 60Kc/s)
2. PERIPHERAL AUTONOMOUS CONTROL for Fast Peripheral Transfers.
   (Transfer rate $\geq$ 60Kc/s)

SLOW HESITATION CONTROL

This system controls the transfer of data utilising a part of the processor MAIN DATA flow hence when a char or word is being transferred, the processor must "HESITATE" until the char or word has been transferred.

When a peripheral raises its 'R' line, the slow Hes Control requests a 'HESITATION'.

At a suitable point this will be granted & the Slow Hes Sequence is entered.

A word or char is transferred and the processor carries on until again the peripheral raises its 'R' line.

The Control Words for this device are accessed during the Slow Hes Sequence to determine :-

1. Location of Data Area.
2. Type of Transfer Req'd.
3. When to Terminate Transfer ('L' line).

CONTROL AREA ANALYSIS

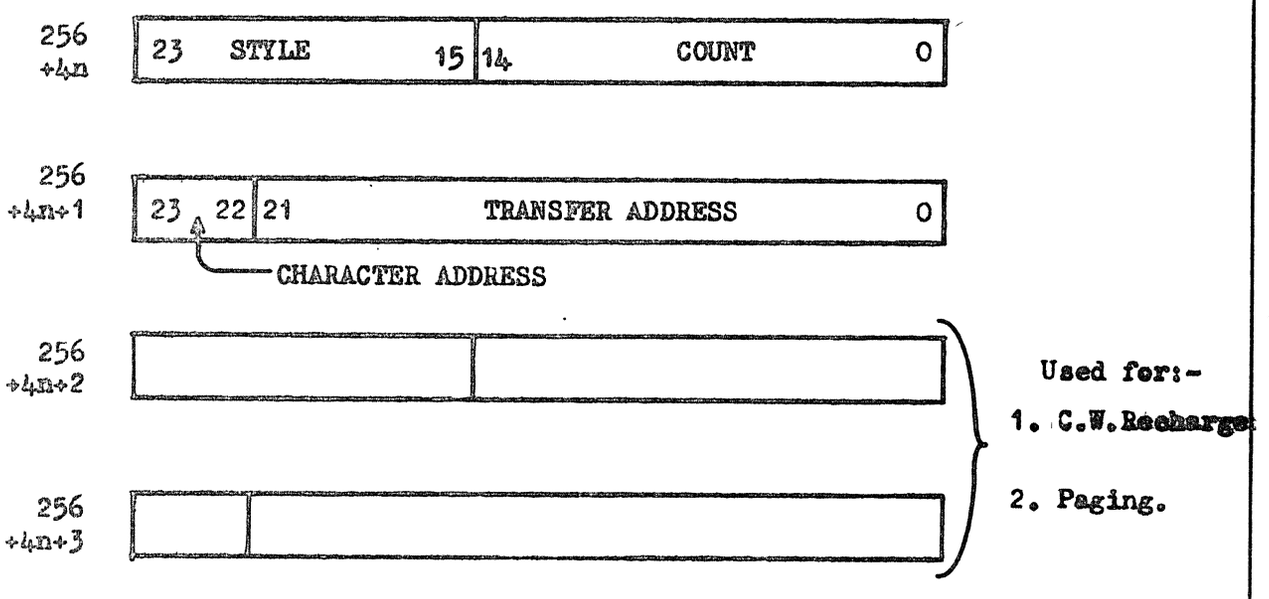
1. Is Control Area within Program Limits ?
2. X or x ?
3. Is there a peripheral of the type specified ?
4. Is peripheral assigned to this program ?
5. Is data area within program limits ?
6. Is transfer count O.K. ?
7. Is Peripheral busy ?
8. Form Hesitation Control Words.
9. Form Command.
10. Send Command to peripheral.

CONTROL WORDS (SLOW PERIPHERALS).

PURPOSE.

To control data transfers to or from a peripheral.
Each device has 4 store locations reserved for it's CONTROL WORDS.
Location of C. Words given by formula:-
256 +4n, 256+4n+1, 256+4n+2, 256+4n+3
Where n=PERIPHERAL SOCKET No.

FORMAT.



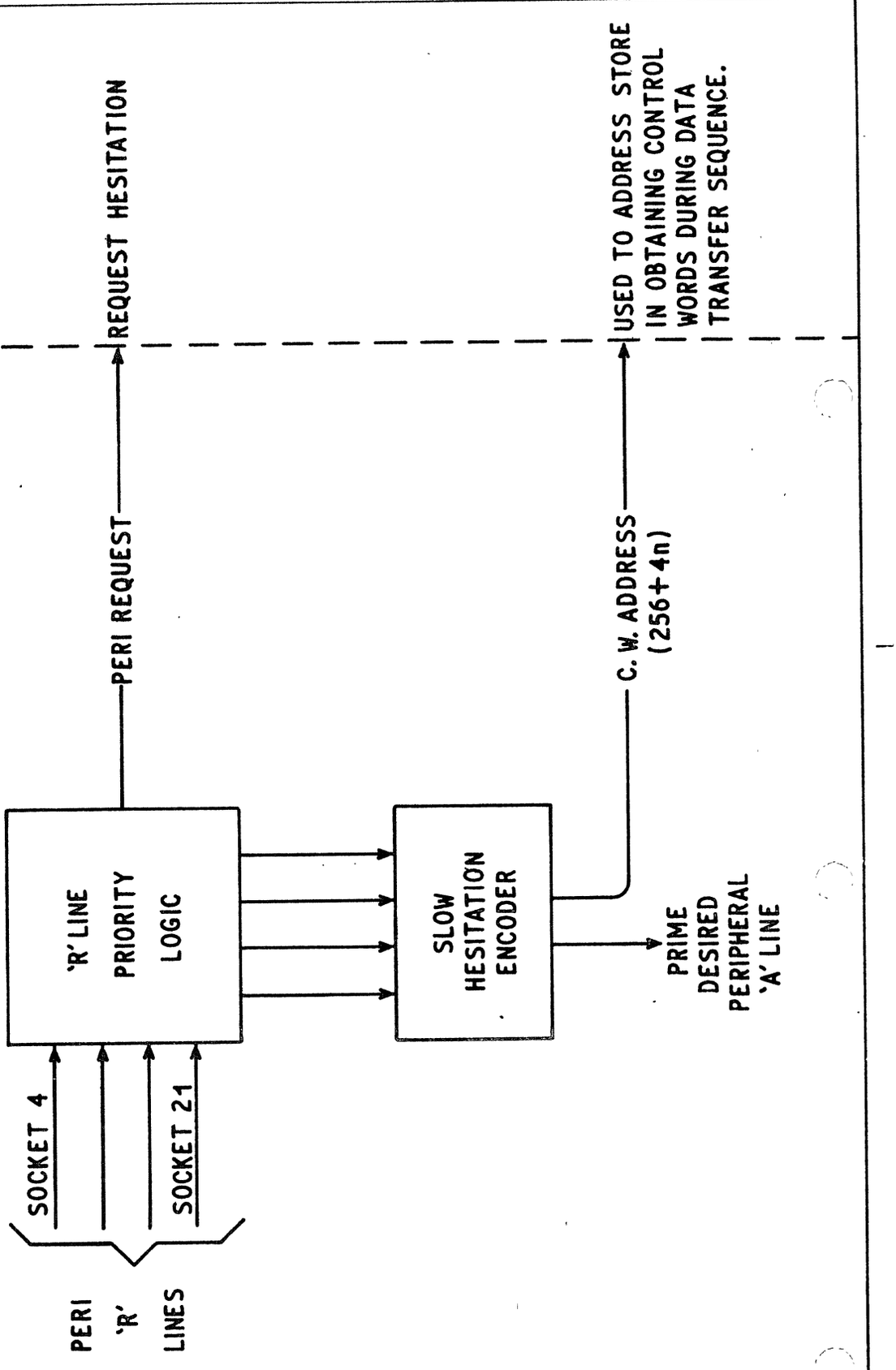
STYLE FIELD

Indicates 'type' of transfer.

BIT 15-17 - Not Used.
BIT 18 - 0=Normal =1-Scatter Gather.
BIT 19 = 0- " =1-C.W. Recharge.
BIT 20 = 0-Single Channel =1-Multichannel.
BIT 21 = 0-Character = 1-Word (Burst Mode)
BIT 22 = 0-Forward = 1-Backward
BIT 23 = 0-Input = 1-Output.

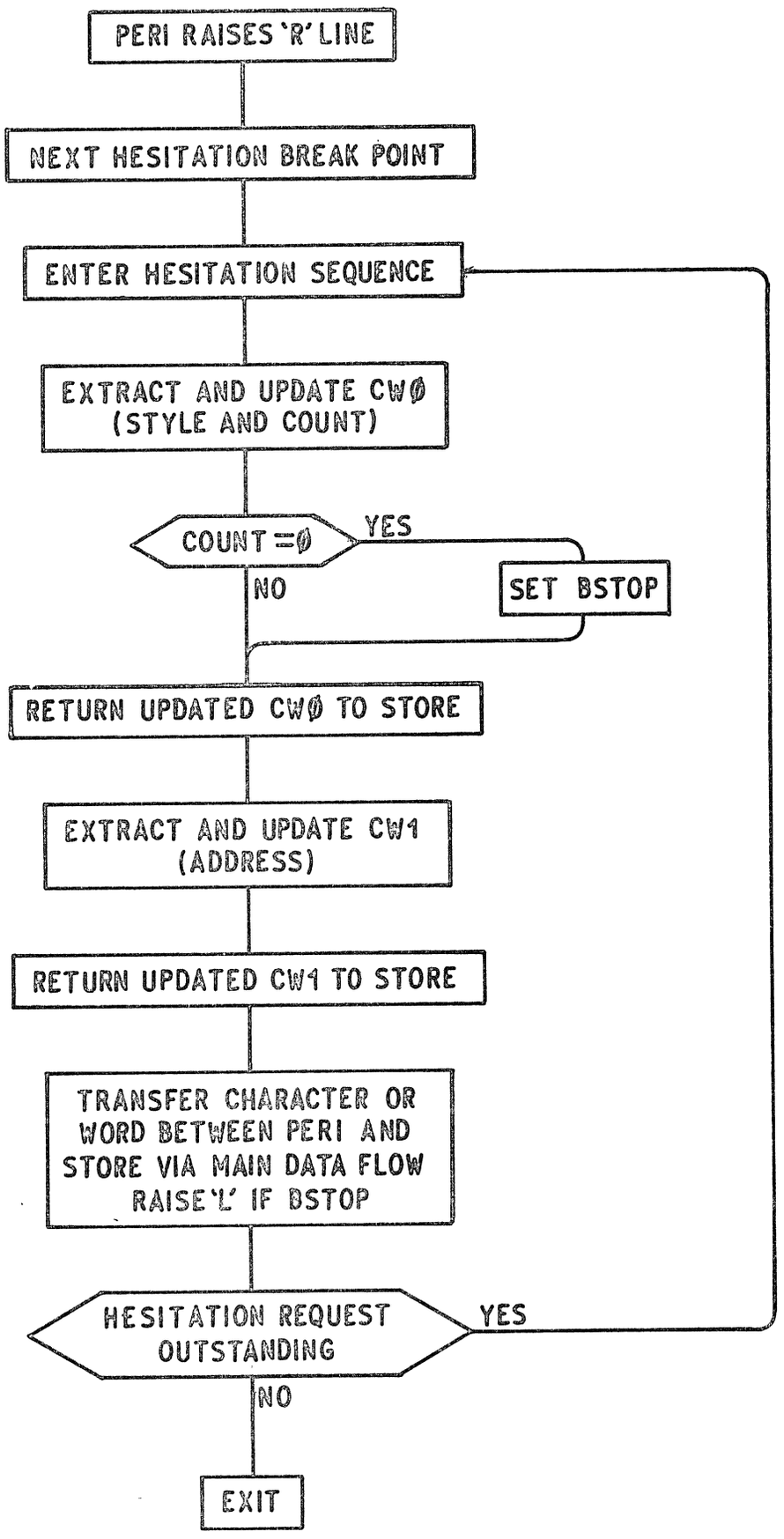
Iss 1.

SIMPLIFIED ACTION PRIOR TO DATA TRANSFER



Iss 1.

HESITATION SEQUENCE



SLOW HESITATION CONTROL

EFFECT OF RAISING AN 'R' LINE.

Having received a command a peripheral will obey that command and when a data transfer is required it will raise its 'R' line.

The peripheral control logic will staticise the request and select the request of the highest priority if more than one 'R' line raised at the same time.

The selected request will :-

1. ask for a HESITATION
2. Generate the basic C.W. address for the selected peripheral (256+4n)
3. Prime the 'A' line to selected peripheral.

A HESITATION is the period of time when the processor will pause (ie. HESITATES) while the data transfer takes place.

At a suitable opportunity the HESISTATION will be granted and the DATA TRANSFER takes place. When transfer complete, the processor continues with its own work.

As the Slow Hesitation Sequence involves the processor MILL, HIWAYS & SOME REGISTERS some action may be necessary on entry to the sequence.

This action depends on the point at which the processor paused to allow the data transfer.

1. At the end of an instruction.
   If the results were to be strobed to X or X+1 then this action must be catered for on entry to Hesitation Sequence.
2. In the middle of a long order.
   The contents of registers used by the Hesitation sequence must be preserved.

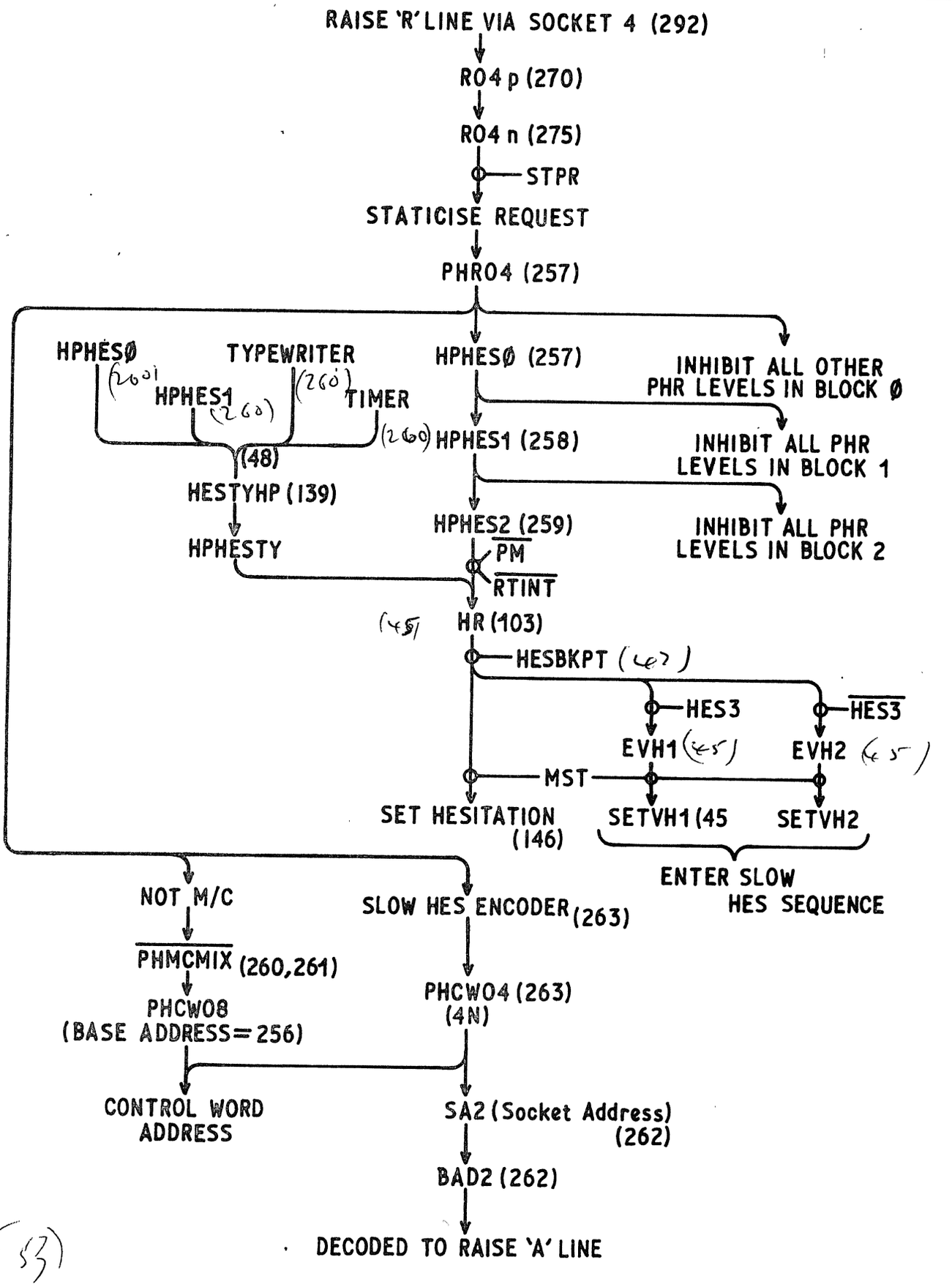
Entry to the sequence is governed by 2 logic levels.
HES4 or HES3
If HES4, It may be necessary to store result to X or X+1.
If HES3, Store B & N to absolute store locations 9 & 10.

These levels also control EXIT from sequence. There are two more levels which may be active on entry, HES1 & HES2 but these control EXIT from sequence only.

Note: A peri raises its 'R' line for each char or word.
∴ Hesitation sequence entered for each word or char.

'R' LINE ACTION

Iss 1.



 ETD 3484

SUMMARY OF HES LEVELS

One of these levels will be active at any one time when the computer is operating. If entry to the Hesitation sequence is made they will be used to effect correct entry and exit.

HES 4 - Active at the end of an instruction or during a hesitation occuring at the end of an instruction.
Result of an instruction may need storing to X or X+1 on entry to sequence. No action on exit.

HES 2 - Active during certain orders. Data that may be lost during the Hesitation sequence is duplicated in other registers so only action necessary is on exit where B & N are restored from X+1 & A.

HES 1 - Active during certain orders where no storing action necessary. This level used to differentiate between this & entry to Hesitation sequence at the end of Instruction.

HES 3 - Active if all other HES levels inactive. If this level is active and entry to the Hesitation sequence is made it signifies entry during a LONG ORDER. Therefore it is necessary on entry to:-

1) Store B --- Absolute Loc^{n} 9
2) Store N --- " " 10

On exit B & N restored from Loc^{ns} 9 & 10

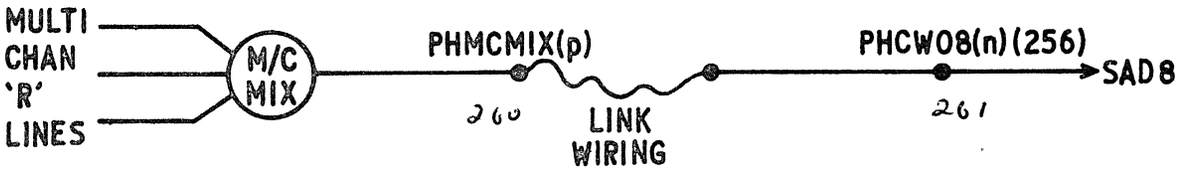
For an 023 the address of the instruction to be obeyed is placed in N & P. If Hesitation Sequence entered at the end of an 023 this address must be restored to N from P.

SLOW HES CONTROL

C.W. Addressing

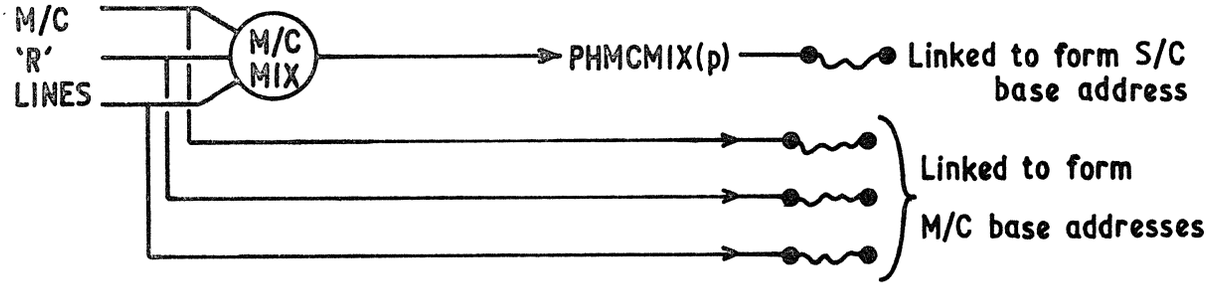
Obtaining BASE ADDRESS.

1. Single Processor
   a. Single Channel.



If all M/C 'R' lines inactive PHMCMIX p inhibitted generating PHCW08N. This gives a base of 256.

b) Multi Channel.



If any M/C 'R' line active, PHMCMIXp active inhibitting S/C Base address of 256. The 'R' line raised via linkwiring generates the desired base address.

2. Dual Processor

The link system is very flexible allowing for Dual processors where both processors are sharing the same store.

a) Single Channel

Processor 1 - Base address of 256
Processor 2 - Base address of 512

b) Multi channel

Processor 1 - Base address of 1024
Processor 2 - Base address of 2048

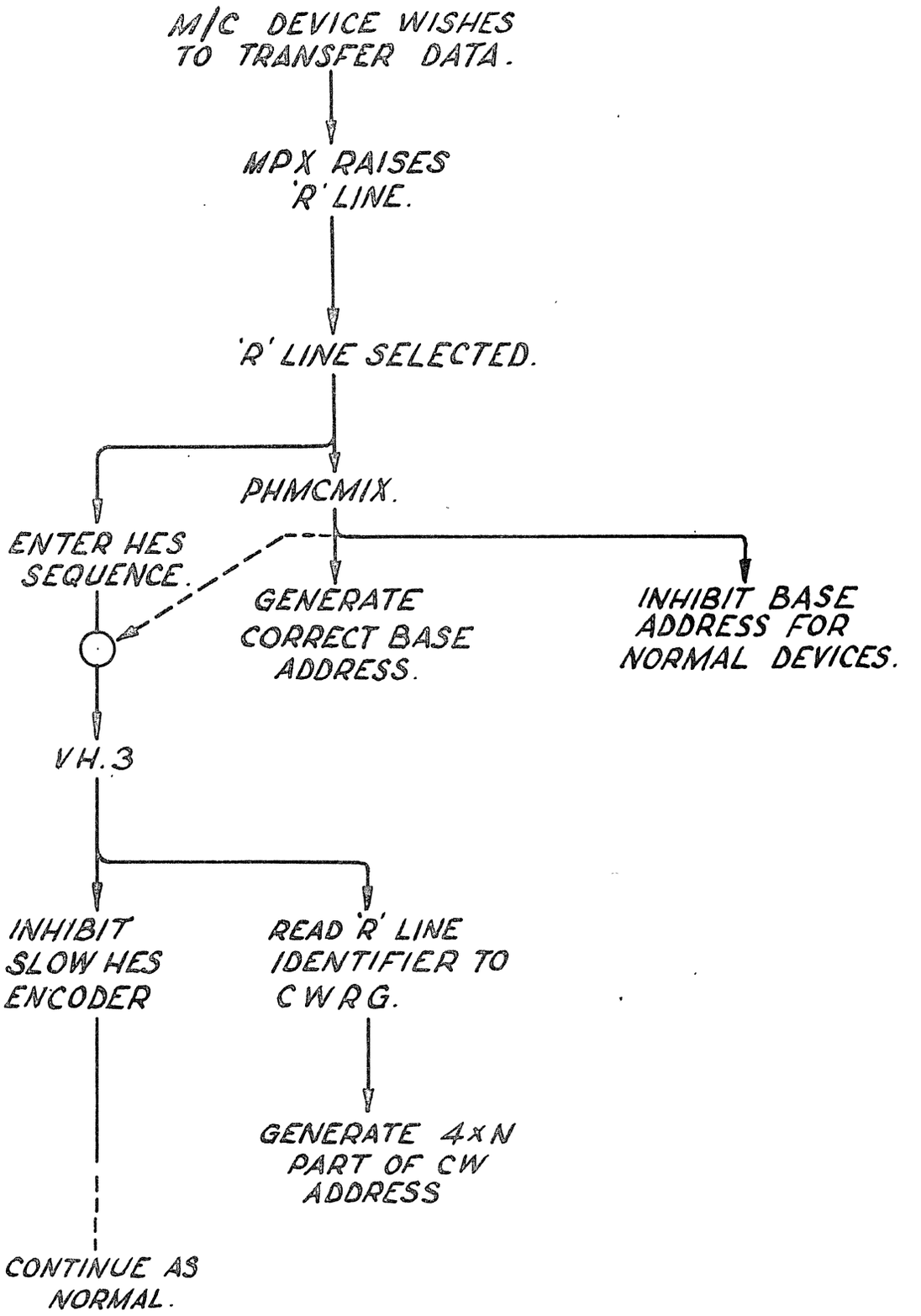
Note - the above figures are examples only.

The 4N part of C.W. address generated by the Slow Hes Encoder.

+1, +2, +3 generated during Slow Hes Sequence.

Iss 1.

SLOW HES. SEQUENCE MULTICHANNEL DEVICES.

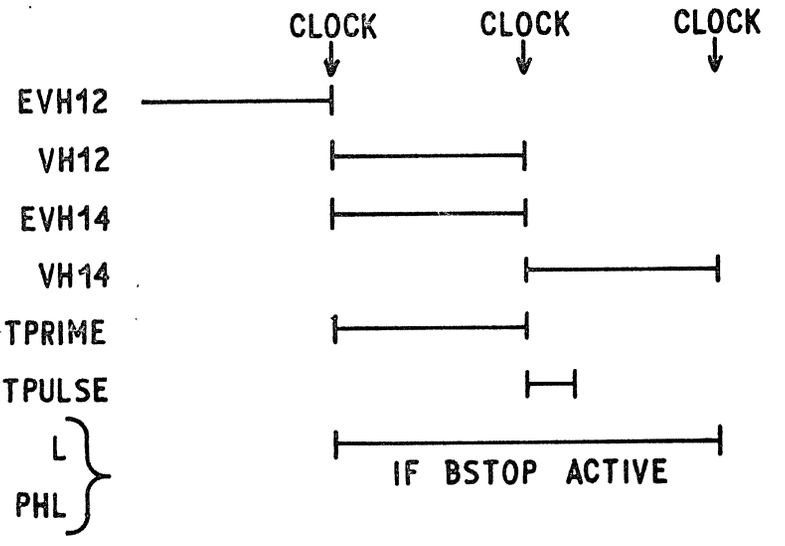


 ETD 3488

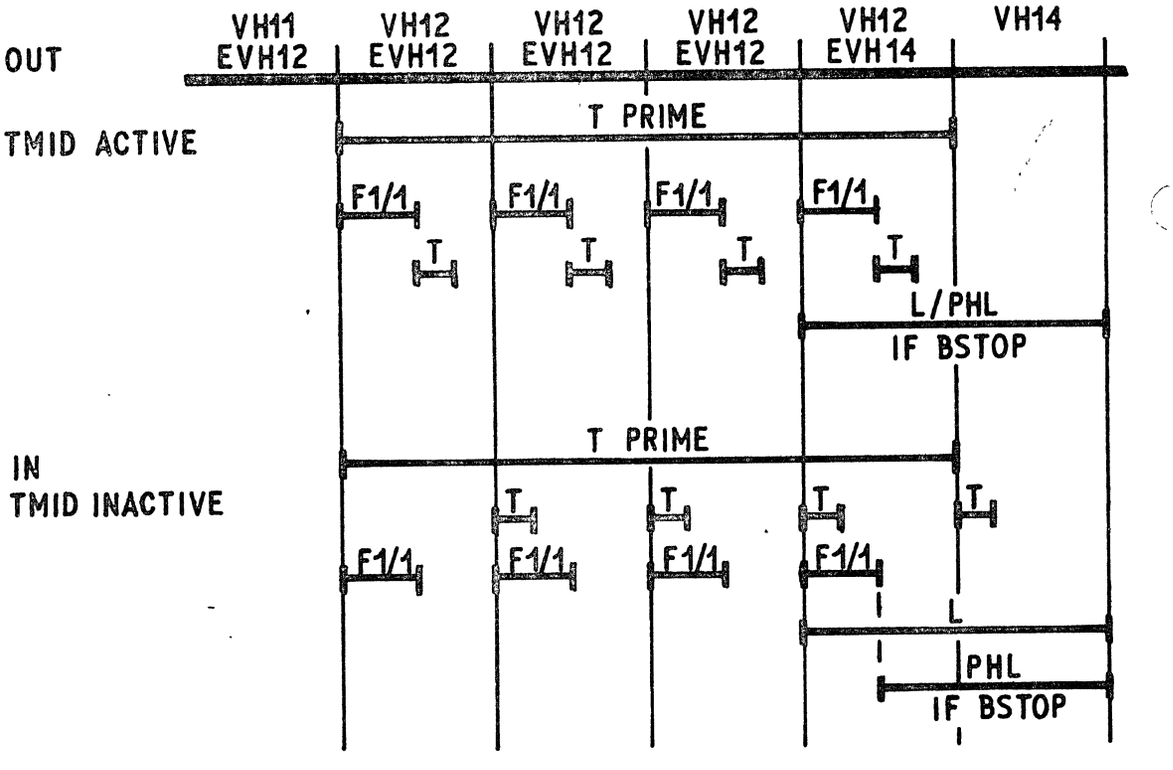
DATA TRANSFER TIMING

Iss /.

CHARACTER (IN OR OUT)



WORD



 ETD.3489 FORM 8/133/B(2 69)

P.A.C. (Peripheral Autonomous Control)

Purpose :- To control transfer of data to and from fast ($\geq$ 60K ch/s) peripherals.

Advantages :-

1. Has direct access to store.
2. No processor registers are involved in P.A.C. transfers ; therefore P.A.C. & Processor may work simultaneously unless store access required together. P.A.C. is then given priority.
3. Can control data transfer to more than one peripheral simultaneously.
4. Store accesses are cut down due to :-

    a) Control Words held by hardware registers & updated by P.A.C. hardware. (1 Pair per Peripheral).

    b) Data sent or received as a word, therefore one store access per 4 chars.

P.A.C.

WGH03 or WGH03FN logic.

Basic P.A.C. has provision for 4 fast channels but may be enhanced to cater for 12 Fast channels & 1 HiSpeed channel. (F1)

P.A.C. may have up to 6 Data buffers but will only be provided with those required as one buffer can be shared by up to 8 peripherals.

The number of peripherals sharing a data buffer is governed by their combined transfer rate.

Max single buffer transfer rate = 380Kø/s
Max overall = 1.5mø/s
With F1 channel = 3 mø/s

F1 channel has its own data buffer.

ALL DEVICES ON P.A.C. MUST BE WORD DEVICES.

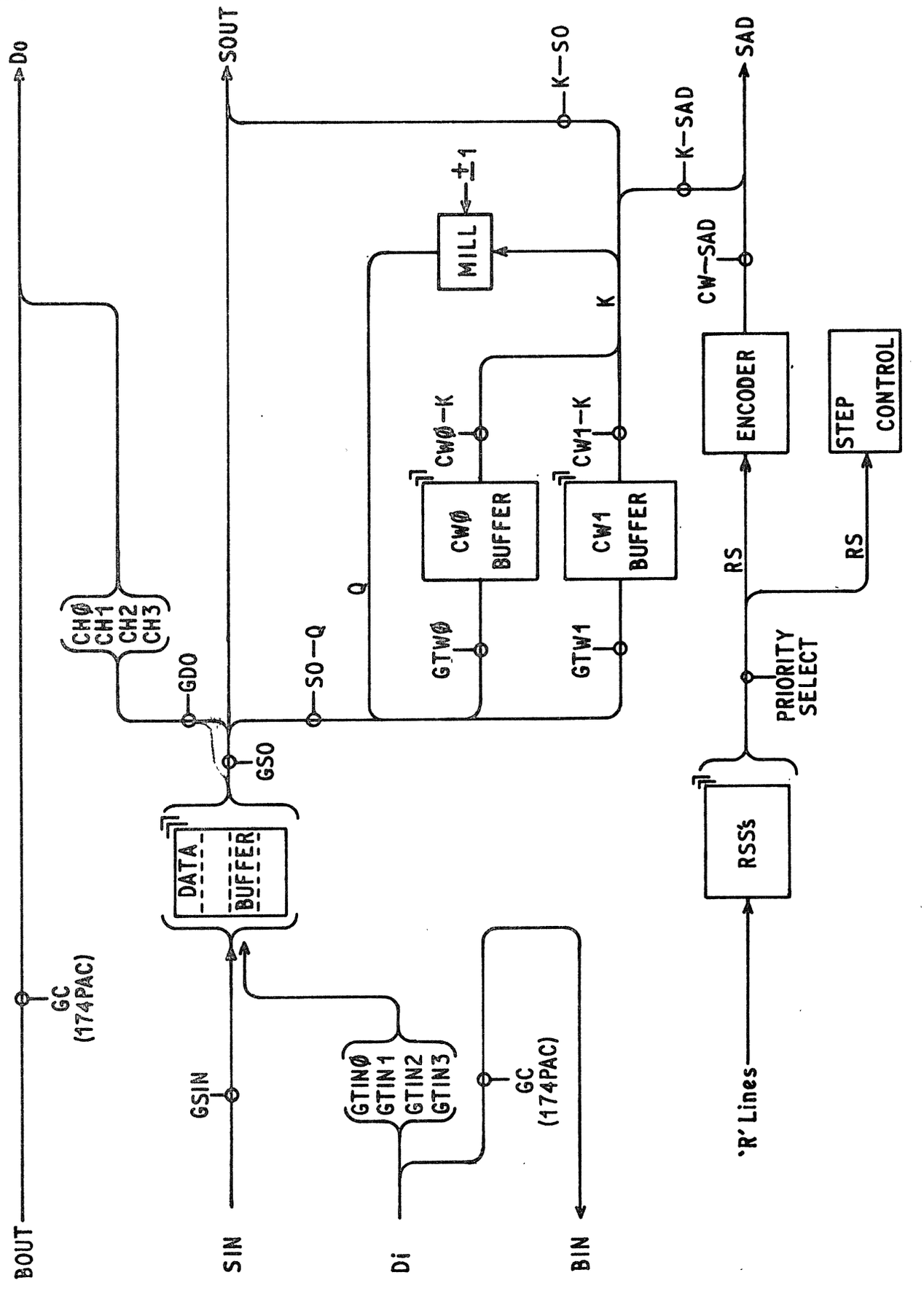
Each device has its Control Words located in Hardware Buffers. The control words are loaded when a device raises its 'R' line for the first time and returned to store at the end of the transfer.

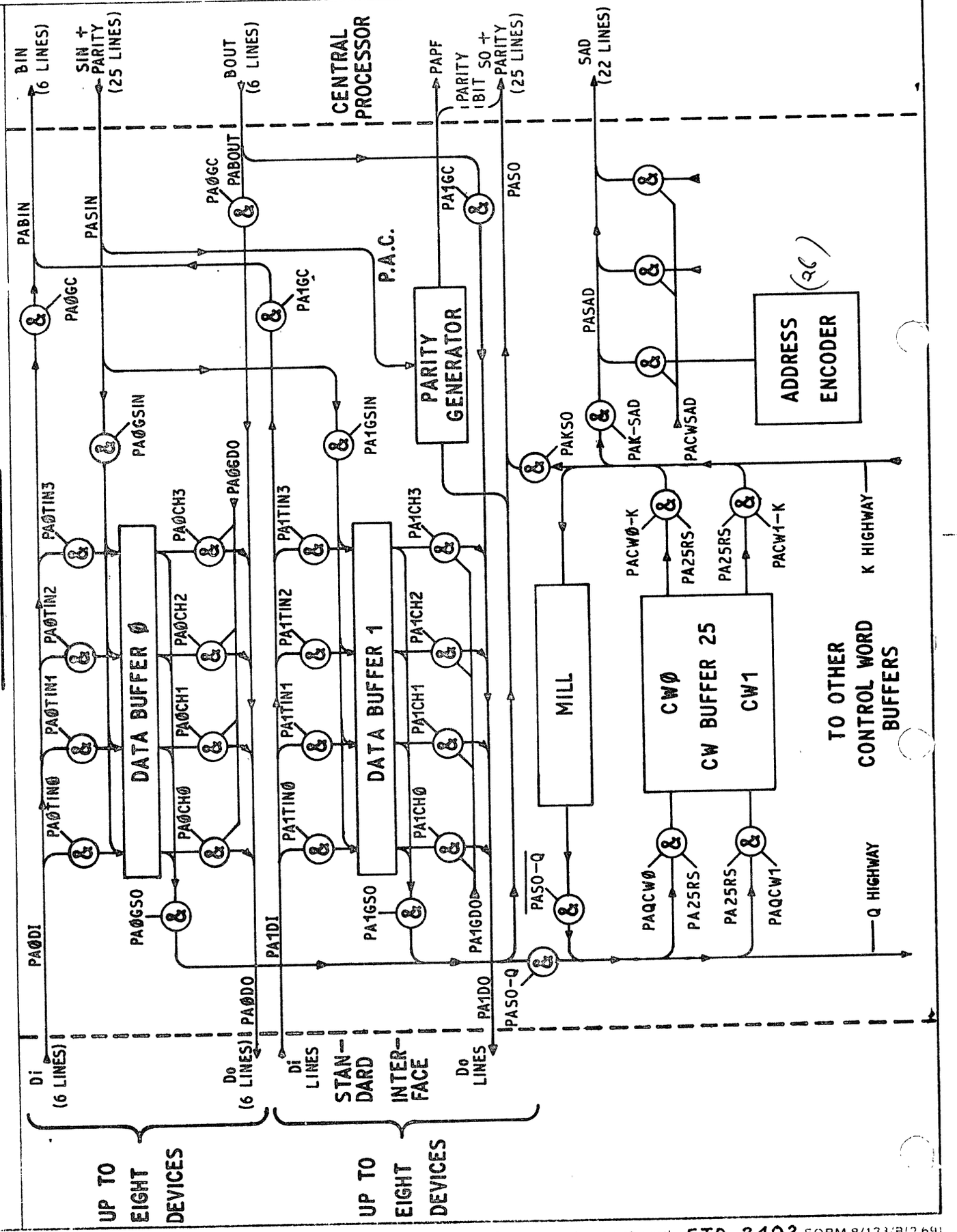
When EXECUTIVE makes a 174, P.A.C. will raise A.C.T. & pass the command to the device. Response returned via P.A.C.

When a device raises an 'R' line, P.A.C. deals with transfer on a priority basis using store direct. Therefore P.A.C. & PROCESSOR may work simultaneously except where both require Store Access together.

Iss 1.

6. SIMPLIFIED DATA FLOW

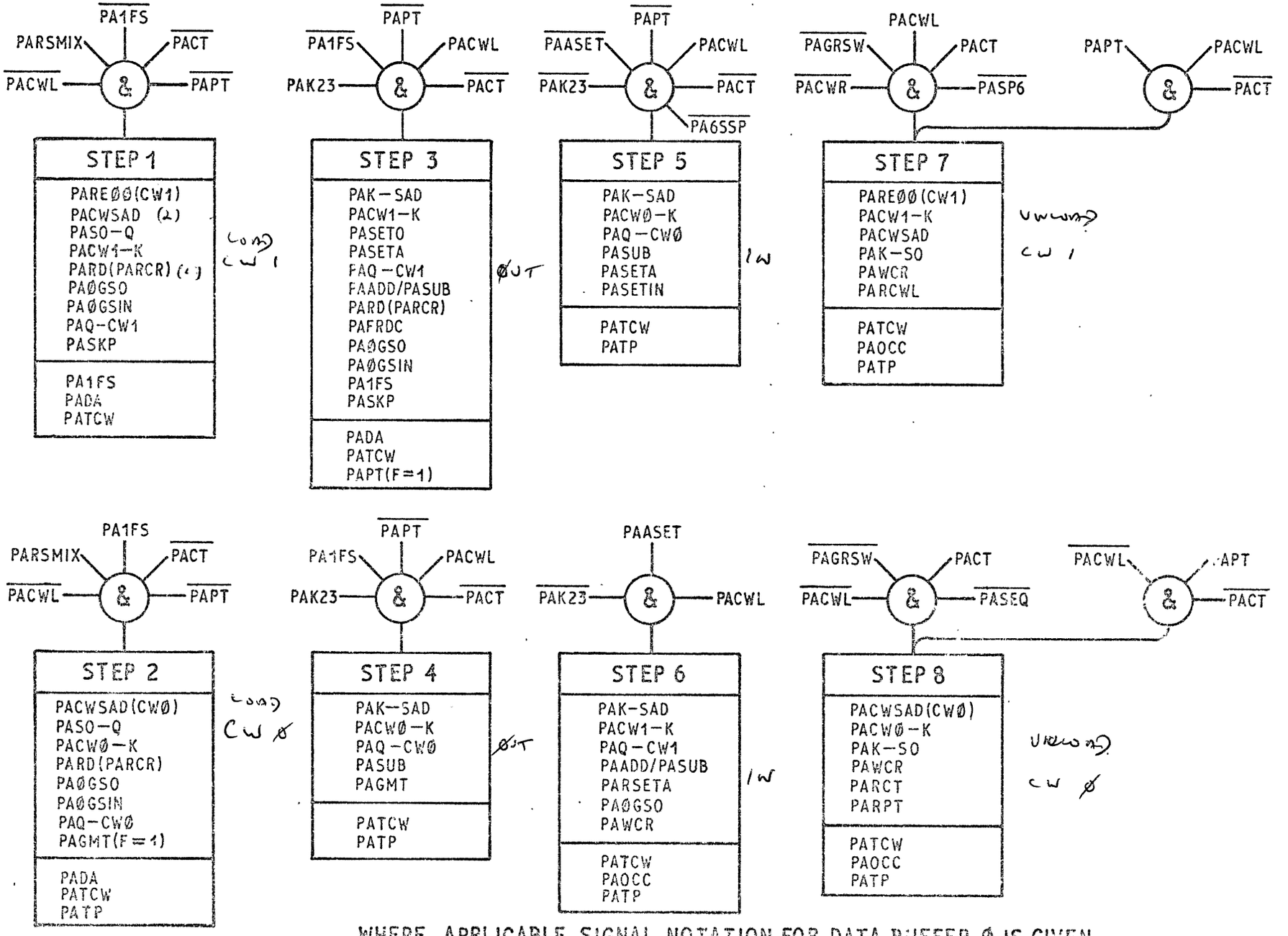




 ETD. 3493

MICROPROGRAM STEPS

ISS 2.1



WHERE APPLICABLE SIGNAL NOTATION FOR DATA BUFFER Ø IS GIVEN.

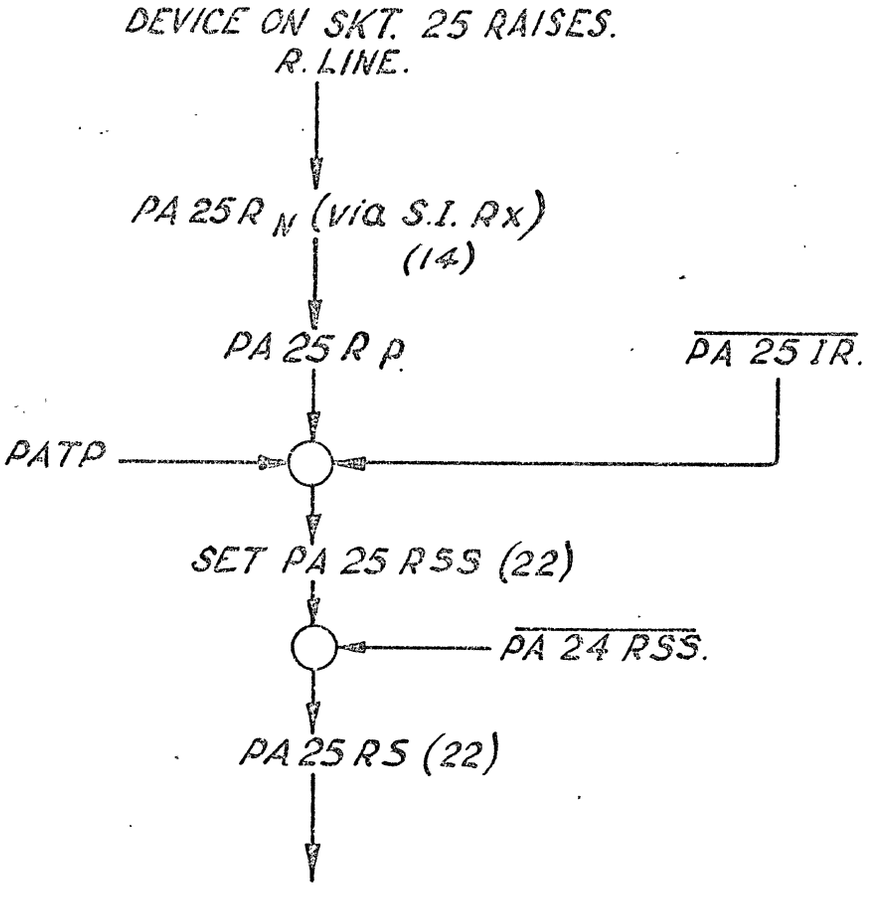
International Computers Limited

1904A MODULE 4.

No. BB905 Sheet 6.5

Iss 1.

P.A.C. - EFFECT OF RAISING AN 'R' LINE.



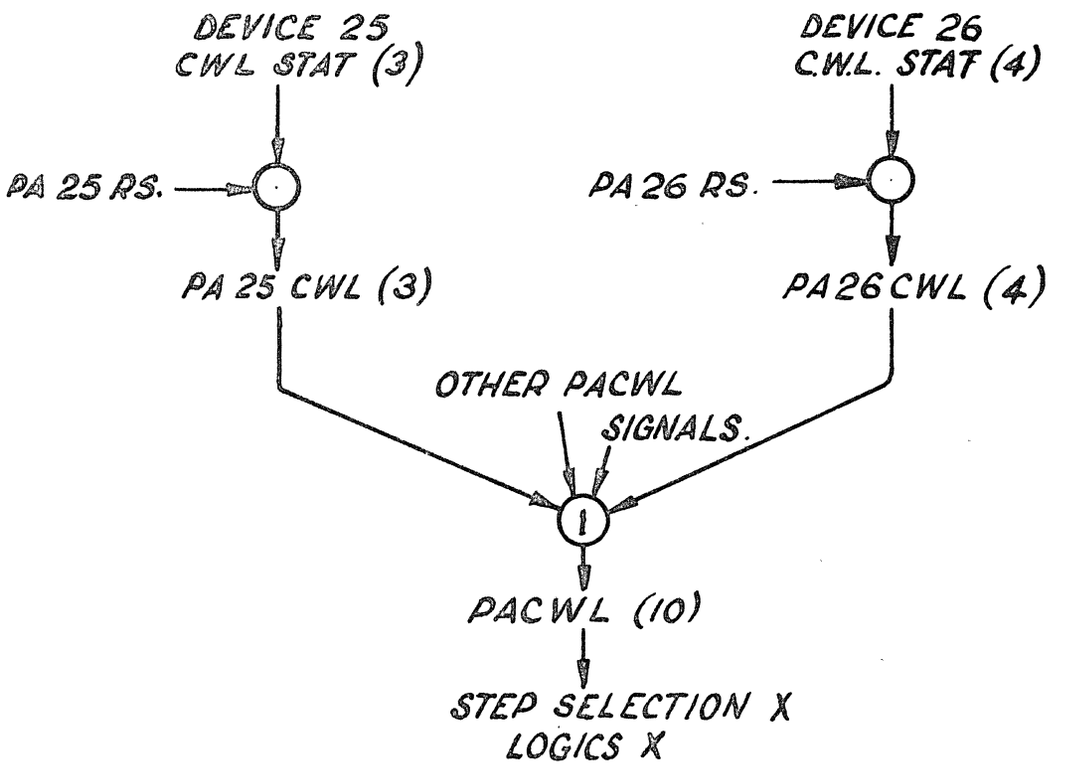
THIS SIGNAL ENABLES ALL CONTROL LEVELS RELEVANT TO THIS PERIPHERAL SOCKET & FROM THIS INFORMATION THE NEXT STEP TO BE PERFORMED IS SELECTED.

E.G. STYLE (IN OR OUT)
C.W.L.
P.T.
C.T.

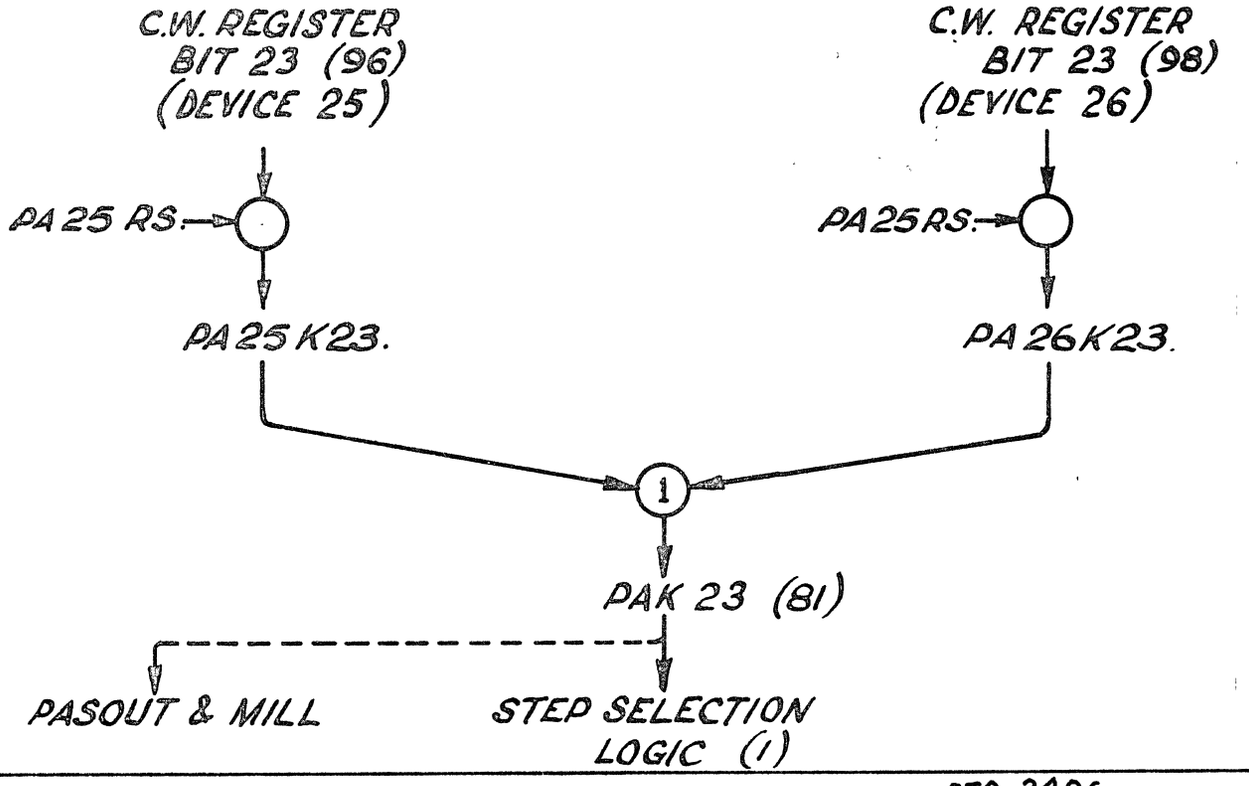
Iss 1.

ROUTING OF CONTROL INFORMATION TO STEP SELECTION LOGIC.

E.G. 1. CWL.



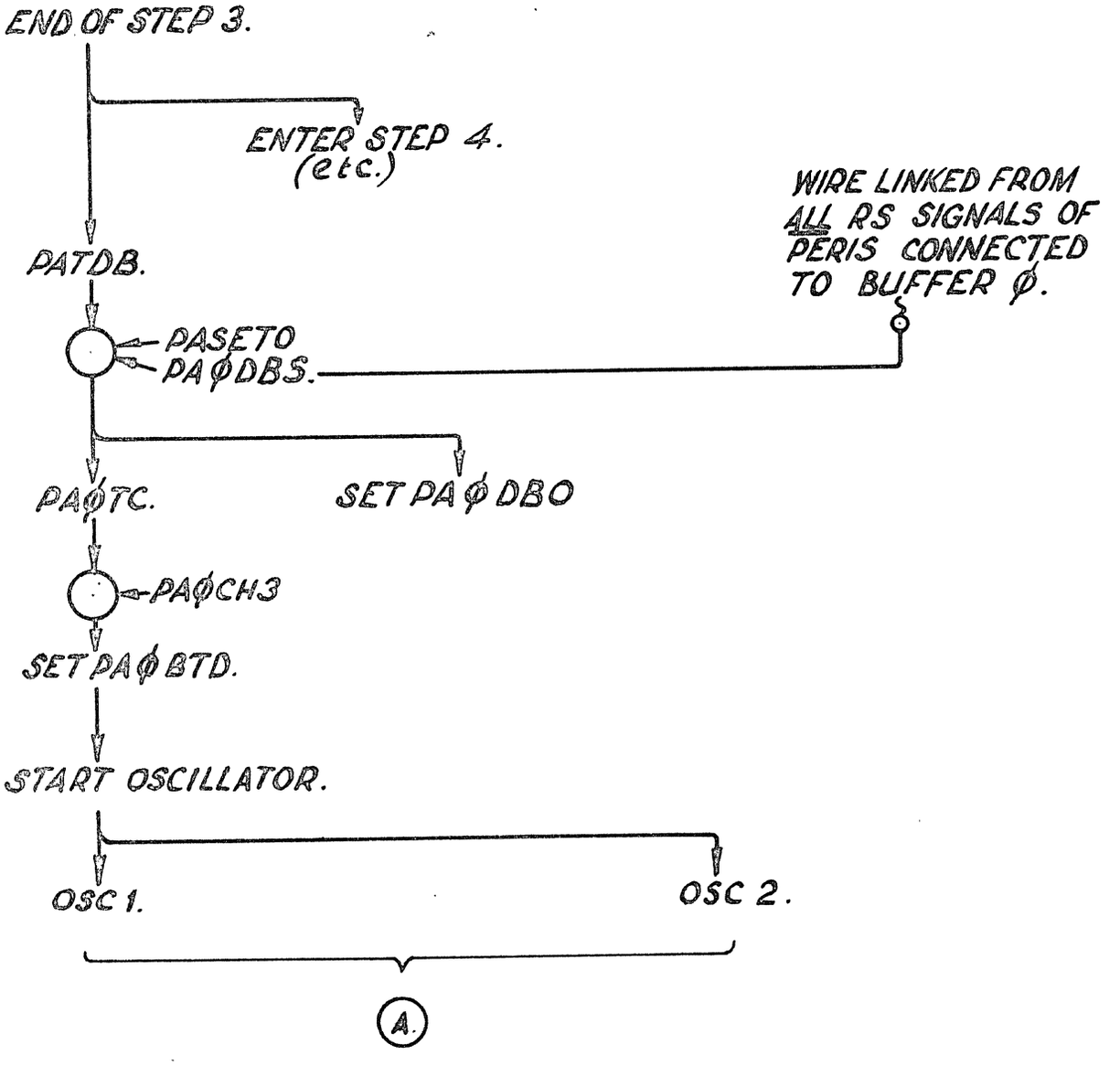
2. STYLE (BIT 23)



Iss 1.

BUFFER SELECTION & OPERATION (O/P.)

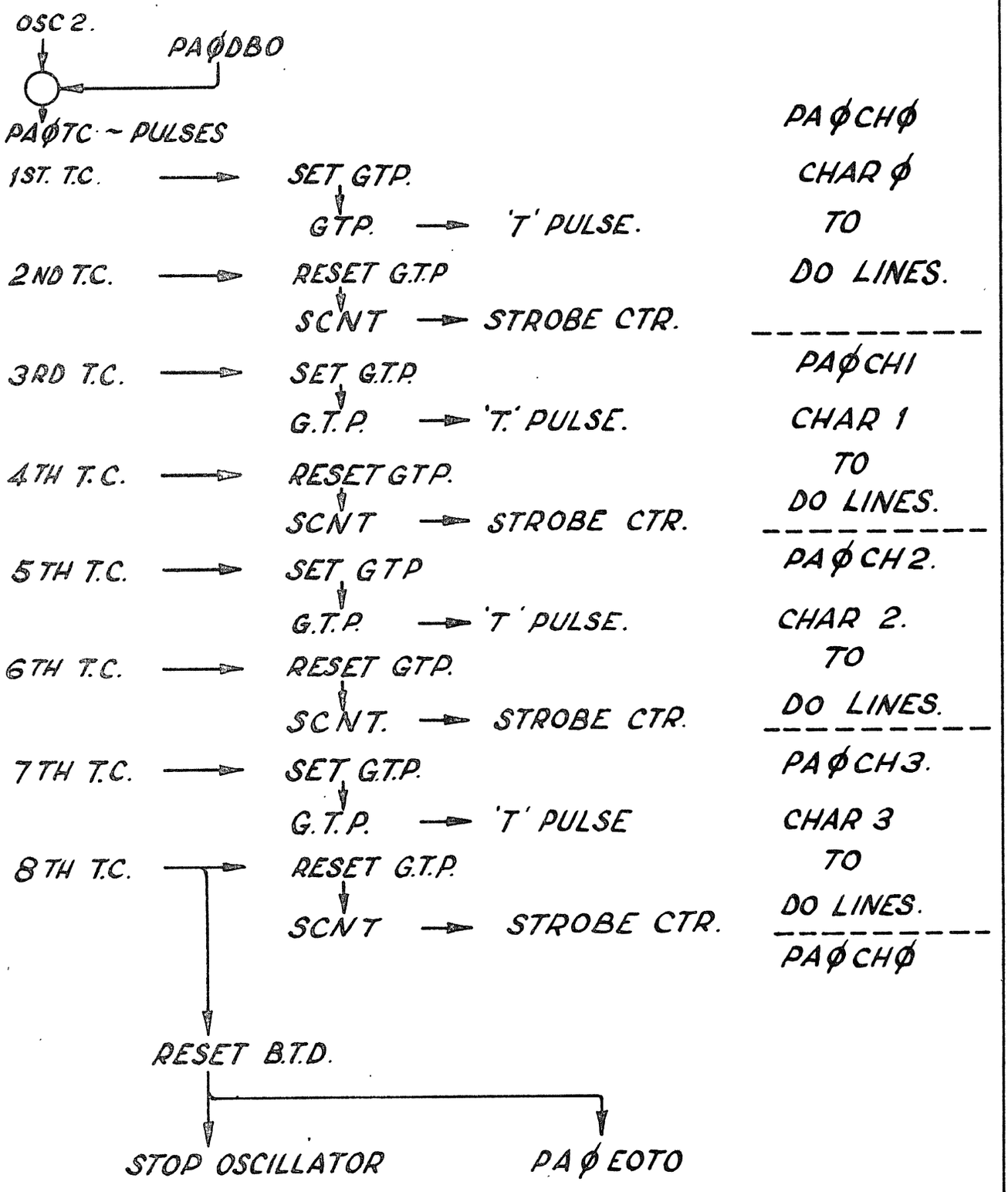
ASSUME BUFFER Ø.



Iss 1

BUFFER ACTION. (O/P.)

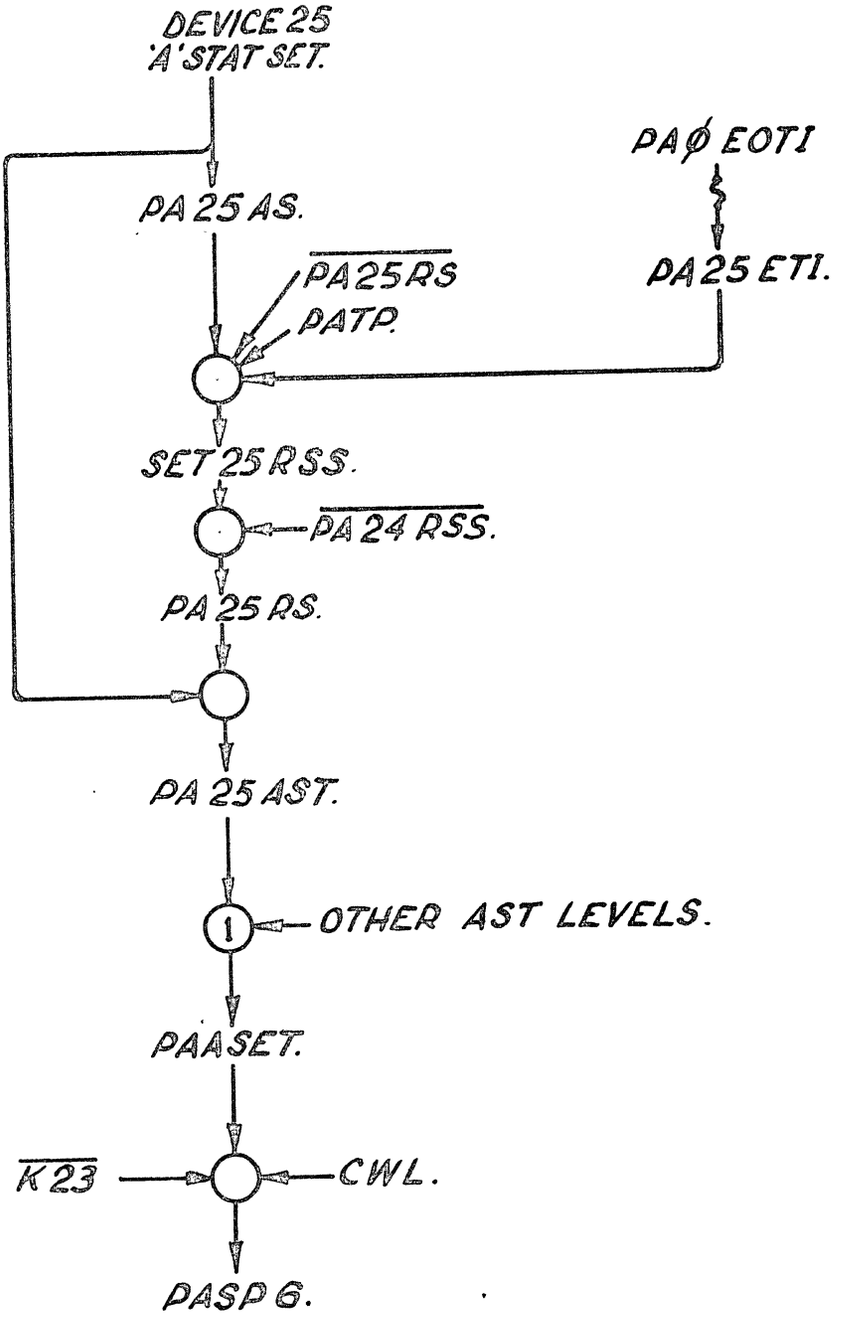
(A)



Iss 1.

SELECTION OF STEP 6 (SKT 25 ~ BUFFER Ø)

STEP 5 INITIATES BUFFER ACTION. AT THE END OF THE 4 CHARACTER BURST THE 'A' LINE IS LEFT ACTIVE ∴ IF 'A' LINE ACTIVE FOR A DEVICE & EOT I. SIGNAL BECOMES ACTIVE, STEP 6 REQUIRED FOR THAT DEVICE.



Iss 1.

PAC. ~ UNLOADING CONTROL WORDS ~ STEPS 7 & 8.

INITIATED BY :-

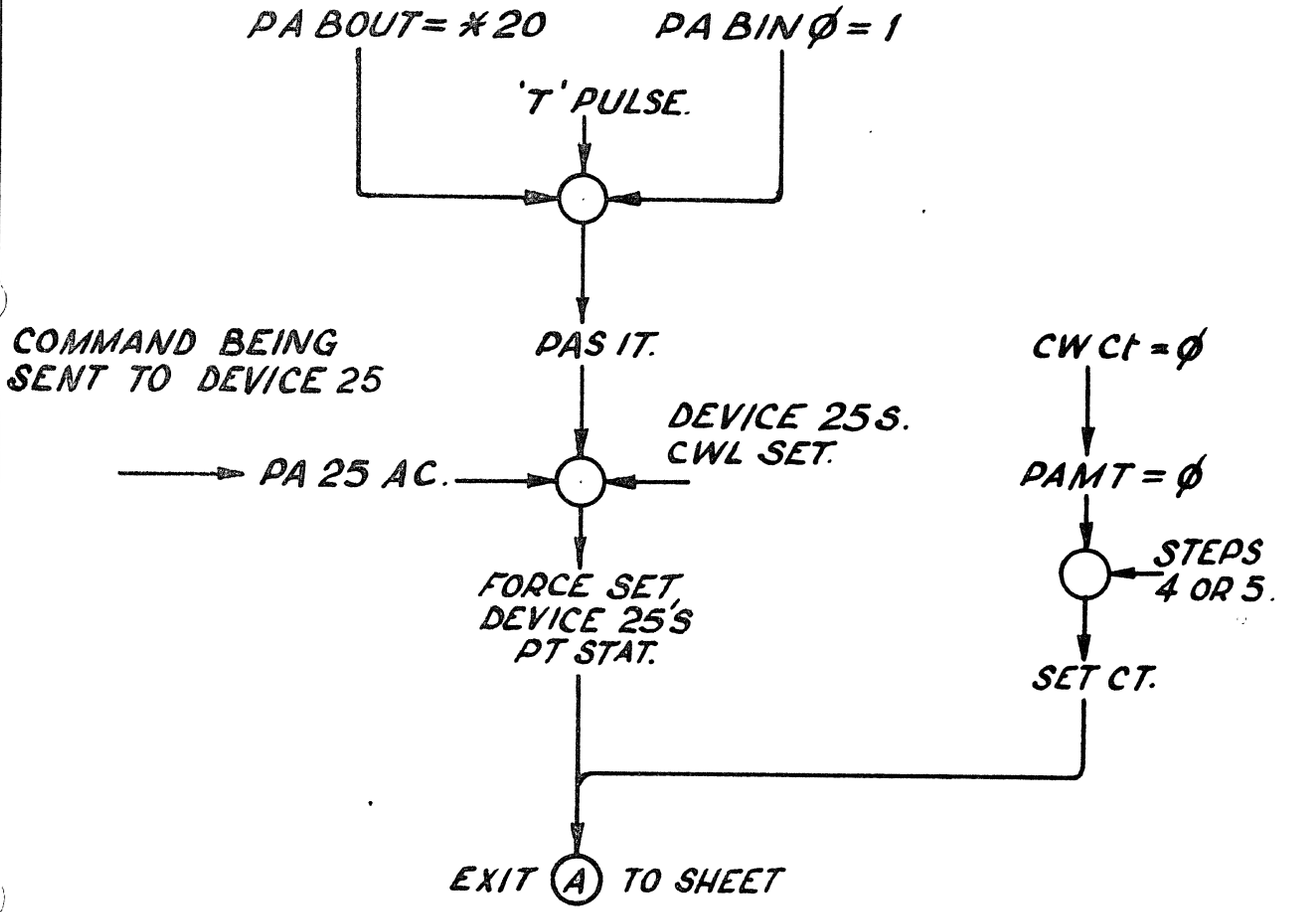
1. C.W. Ct. = Ø (PAMT = Ø)

THIS RESULTS IN CT STAT FOR DEVICE BEING SET.

2. DEVICE TERMINATING BEFORE CW Ct = Ø
(i.e. IN ERROR, END OF BLOCK ETC.)

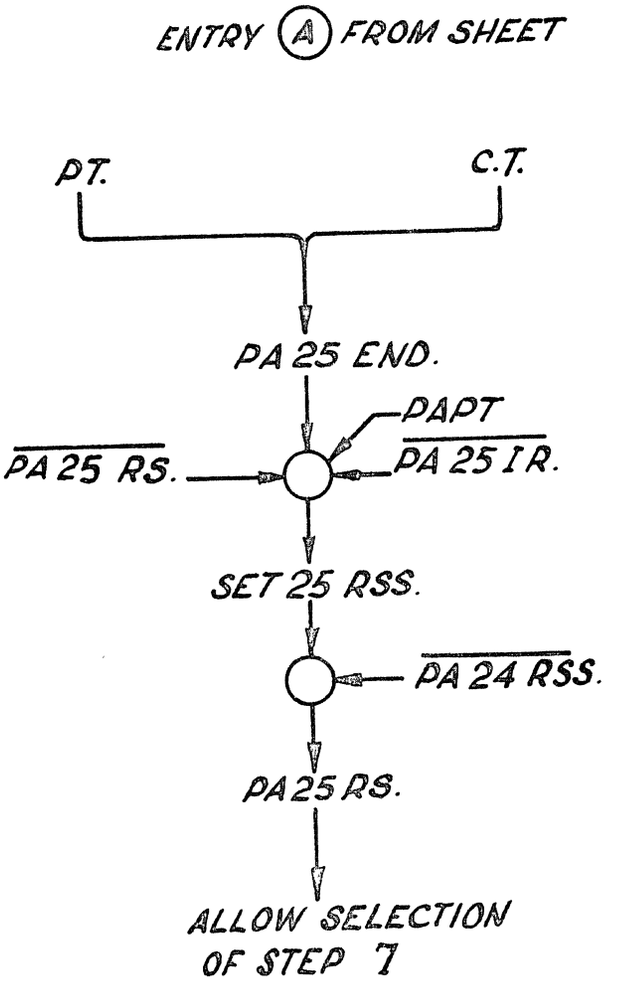
IF COMMAND * 20 (SSQ) SENT TO A DEVICE AND RESPONSE BIT Ø (TERMINATED) = 1, SET PT STAT FOR THAT DEVICE.

(ASSUME DEVICE 25)



Iss 1.

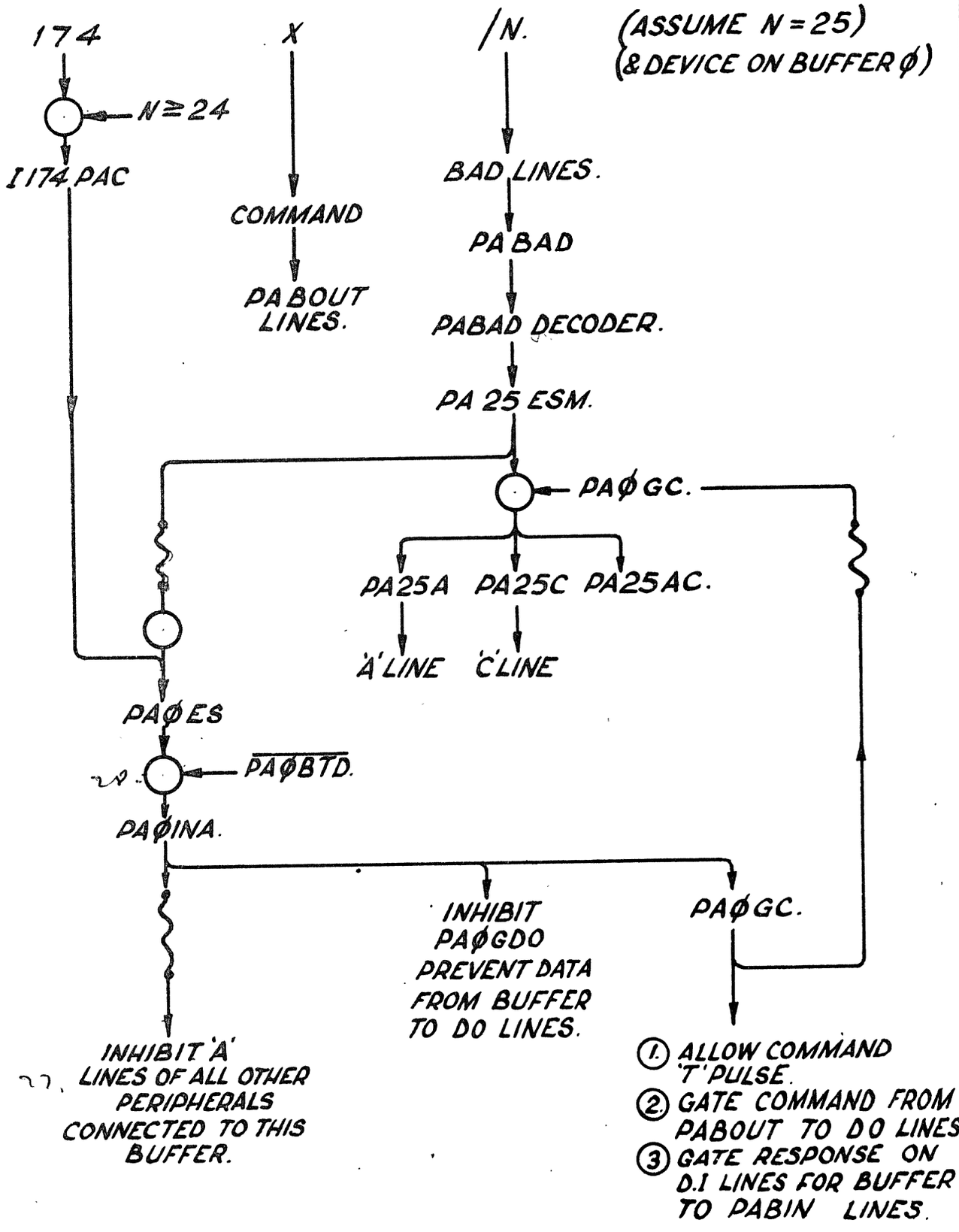
PAC. ~ UNLOADING CONTROL WORDS ~ STEPS 7 & 8 (Cont.)



Iss 1.

PAC – COMMANDS.

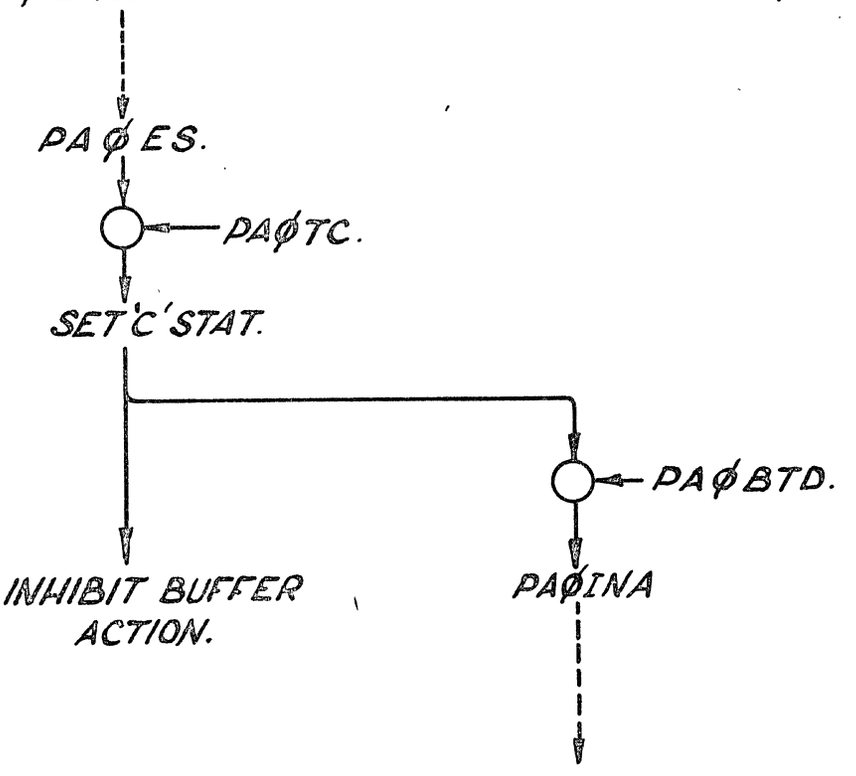
1. BUFFER NOT TRANSFERRING DATA.



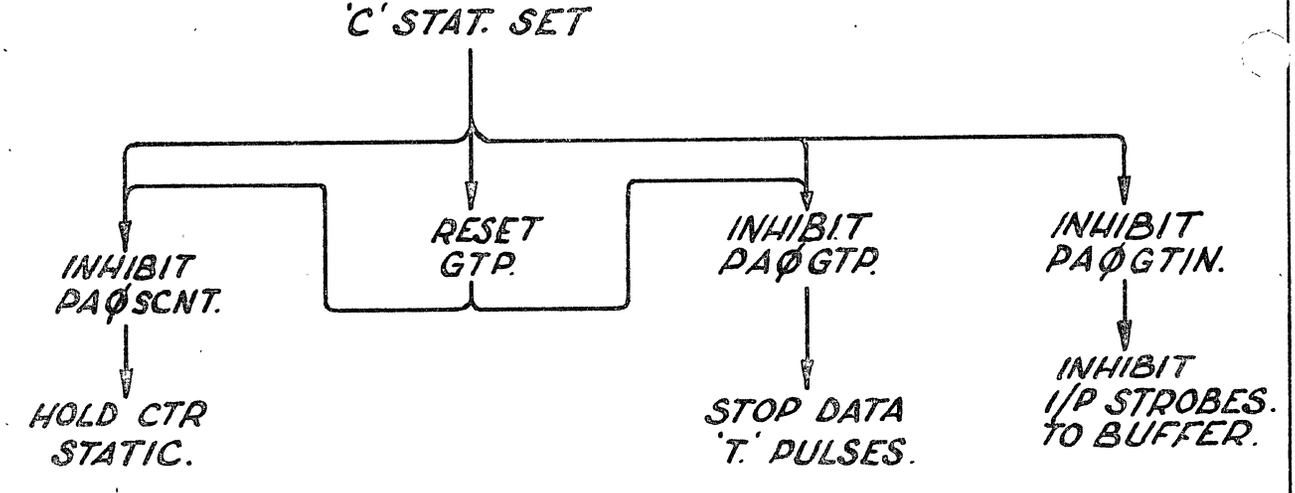
Iss 1.

2. BUFFER TRANSFERRING DATA.

ACTION AS FOR 1, EXCEPT FOR GENERATION OF PAØINA.



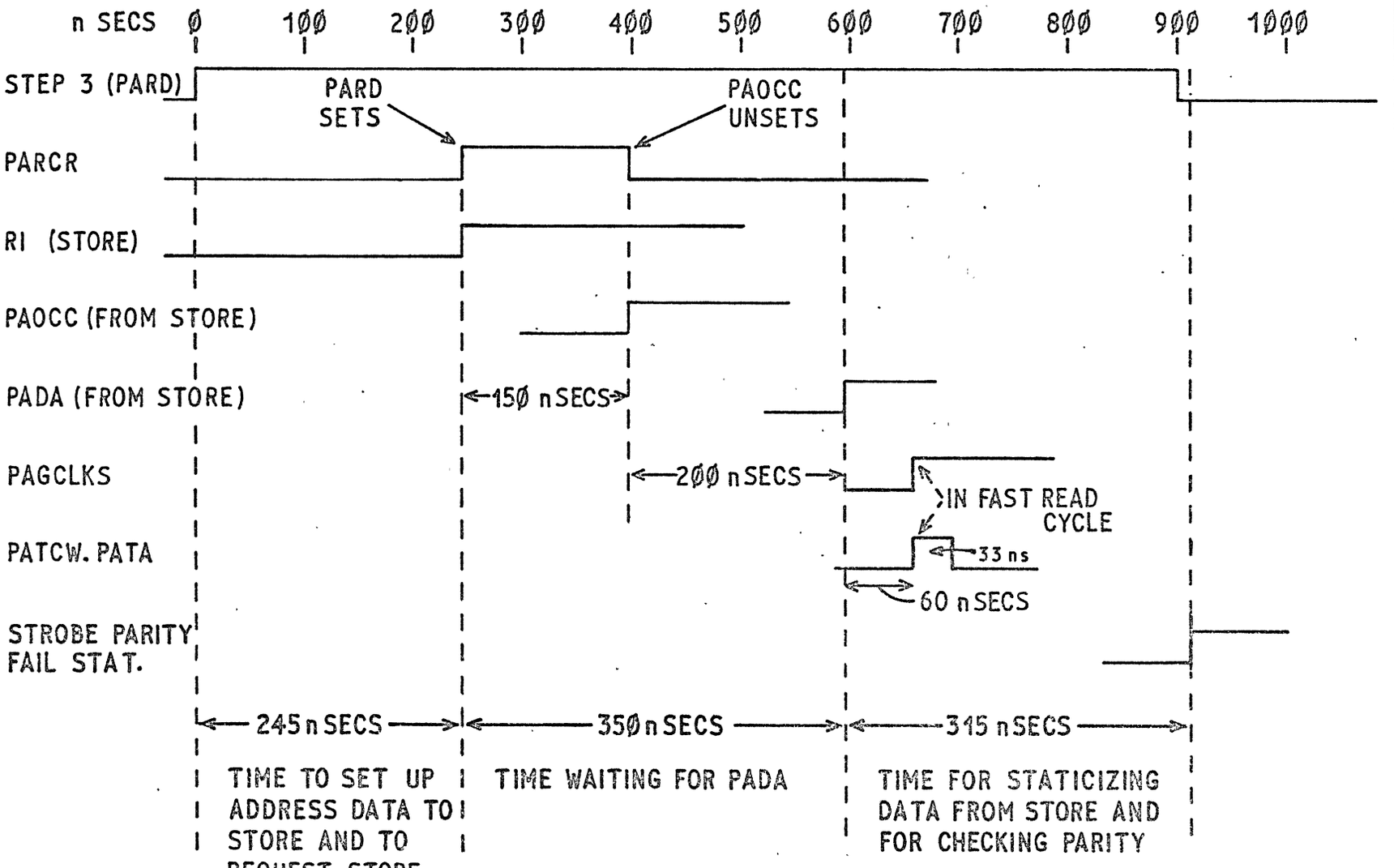
EFFECT OF 'C' STAT.



WHEN F.174 ENDS, PAØES LOST, 'C' STAT. RESET & BUFFER ALLOWED TO RESTART.

INITIATING THE CLOCK PULSES (READ MODE, STEP 3)

Iss 1. 2.



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1904A MODULE 4.

No. BE006
Sheet 6.15

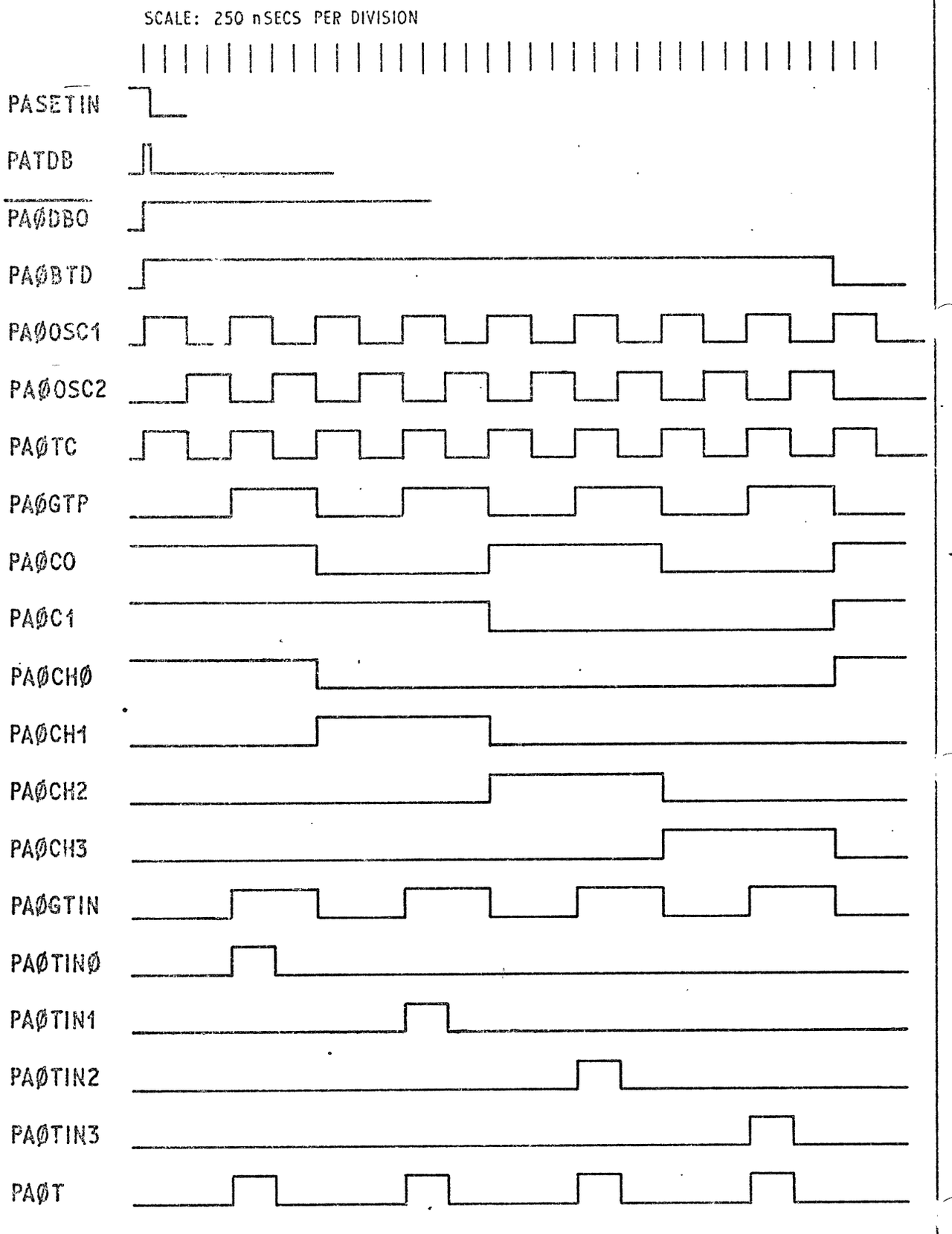
International Computers Limited

1904A MODULE 4.

No. BB006
Sheet 6.16

INWARD TRANSFER DATA BUFFER Ø CONTROL

Iss
1.
2.



 ETD 3505

ETD 3506

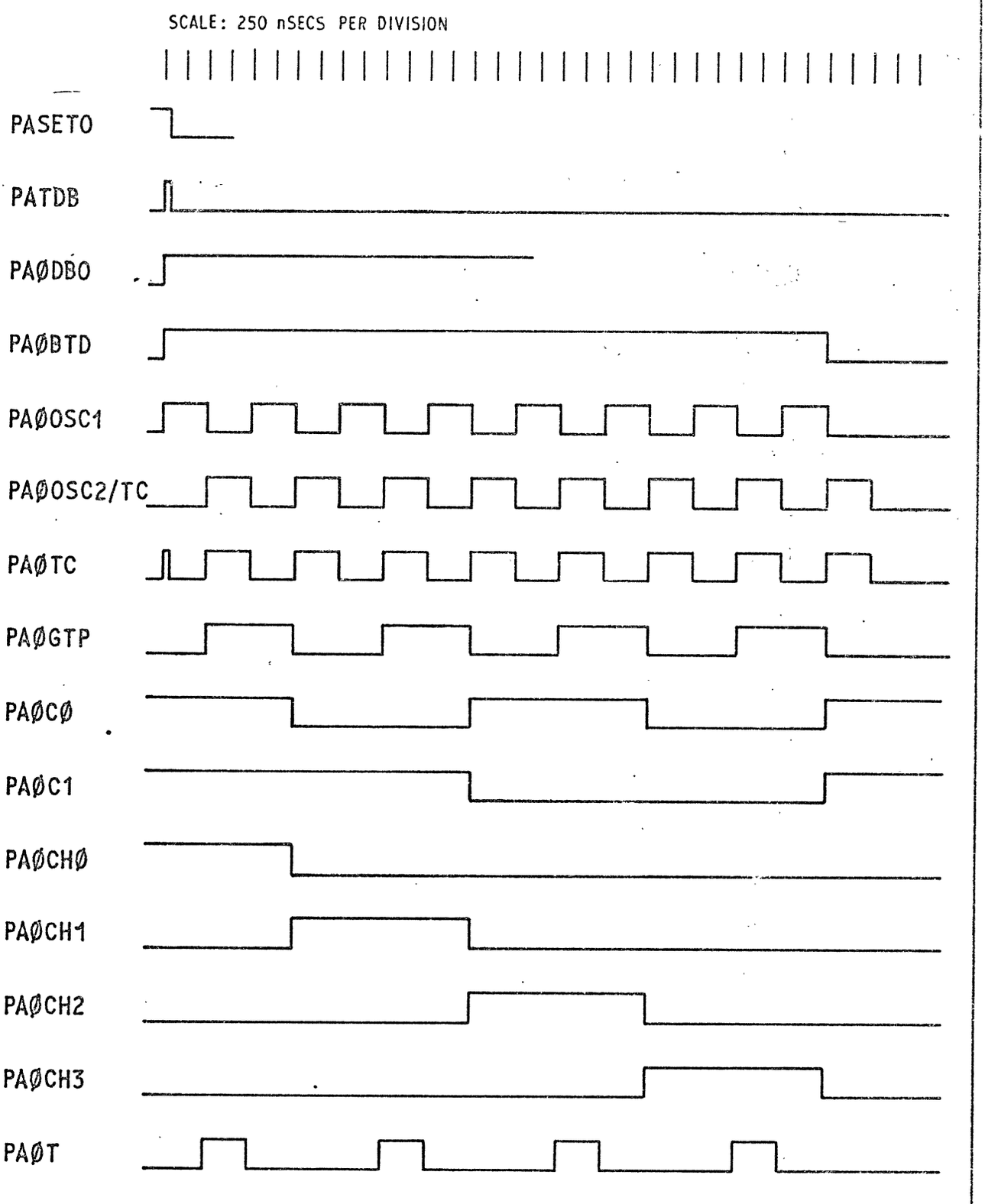
International Computers Limited

1904A MODULE 4.

No. BB006
Sheet 6.17

OUTWARD TRANSFER DATA BUFFER Ø CONTROL

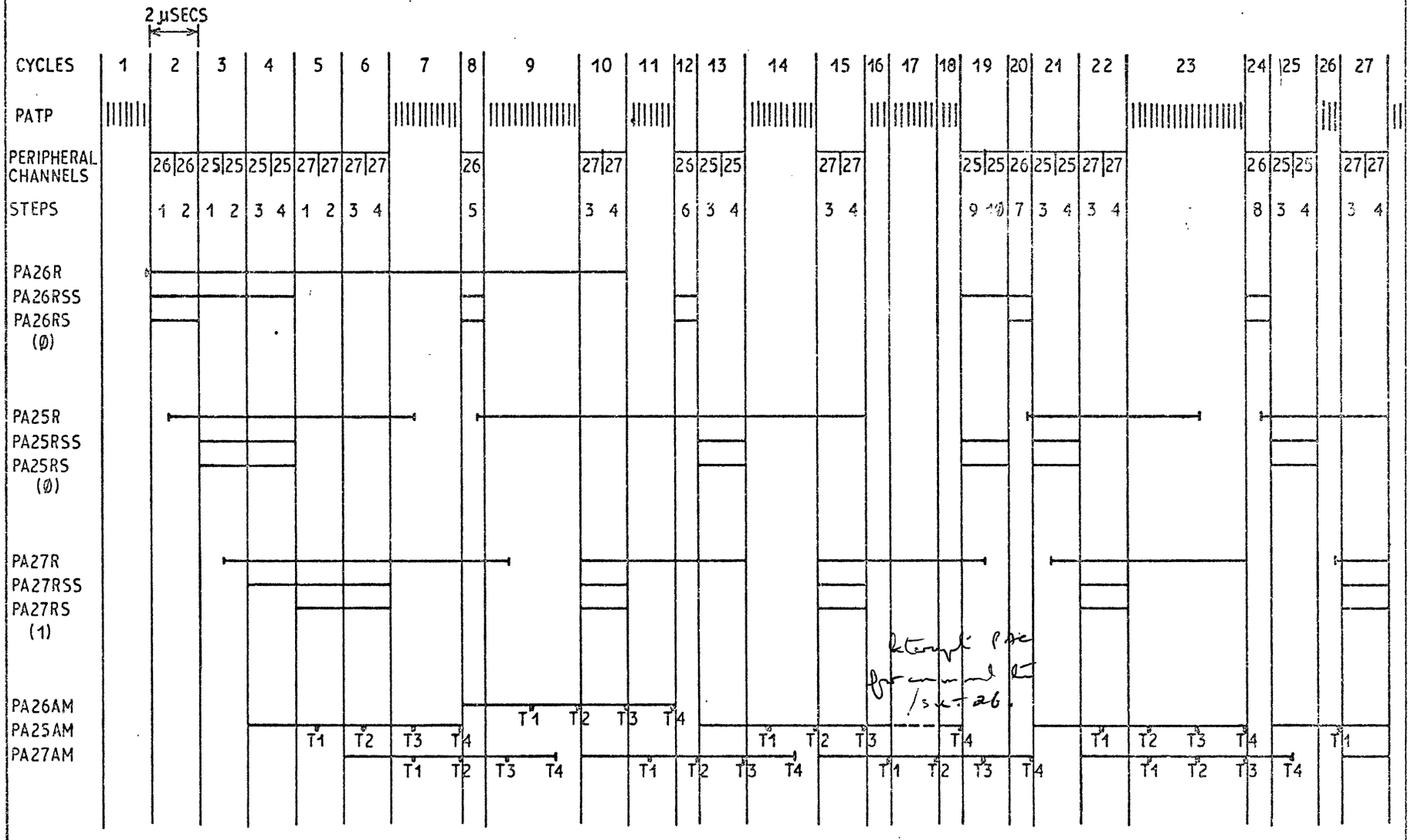
Iss
1.
2.



 ETD 3506 FORM 8/133/B12 69

P.A.C. TIME SHARING

Iss 1.



International Computers Limited

1904A MODULE 4.

No. BB006 Sheet 6.18

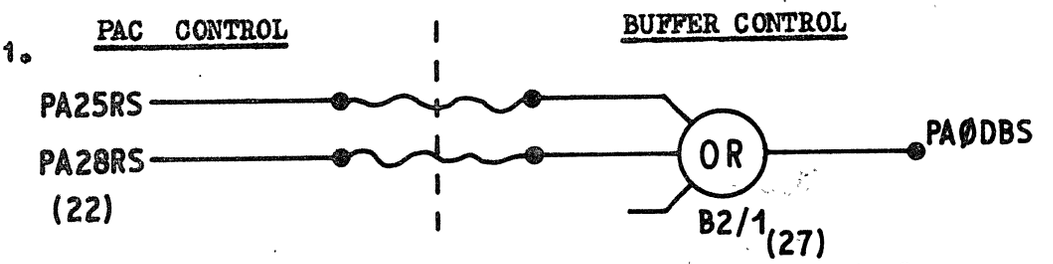
ETD 3507 FORM 8/133/B(2.69)

P.A.C.

LINK WIRING

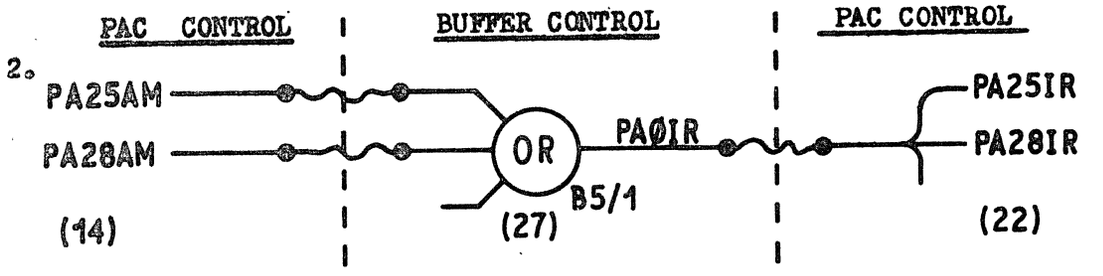
(REF.SKTS 25 & 28 CONNECTED TO BUFFER Ø)

1.



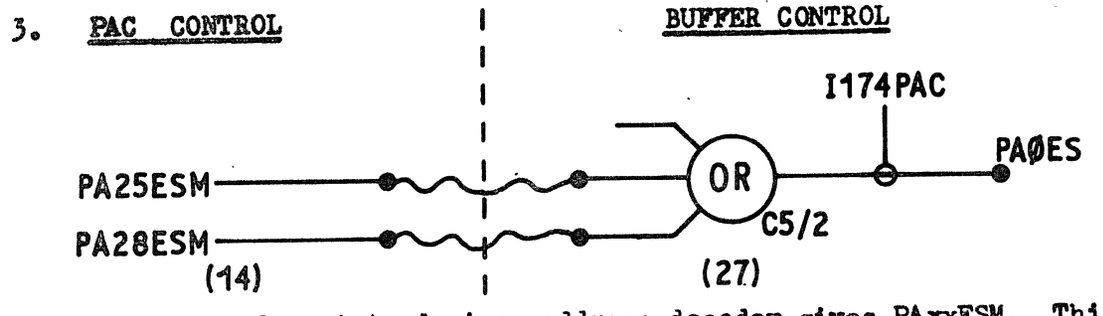
Peri RS levels connected into relevant Buffer control.

2.

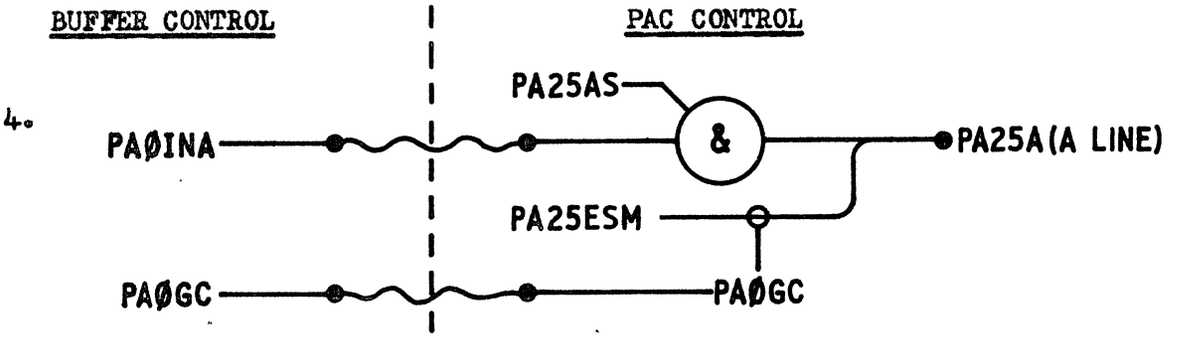


When any peri of a group connected to BUFFER 'Y' is addressed, the 'R' lines of ALL peri's in the group inhibited.

3.



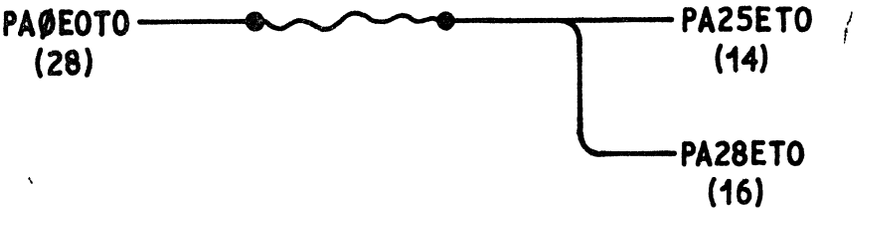
When command sent to device, address decoder gives PAxxESM. This signal passed to relevant BUFFER control.



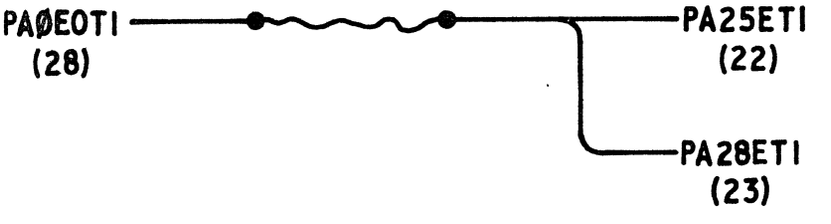
When a command sent to a peri, all 'A' lines of peris connected to a buffer are inhibitted except the 'A' line of the peri receiving the command.

5. END OF TRANSFER SIGNALS

a) O/P



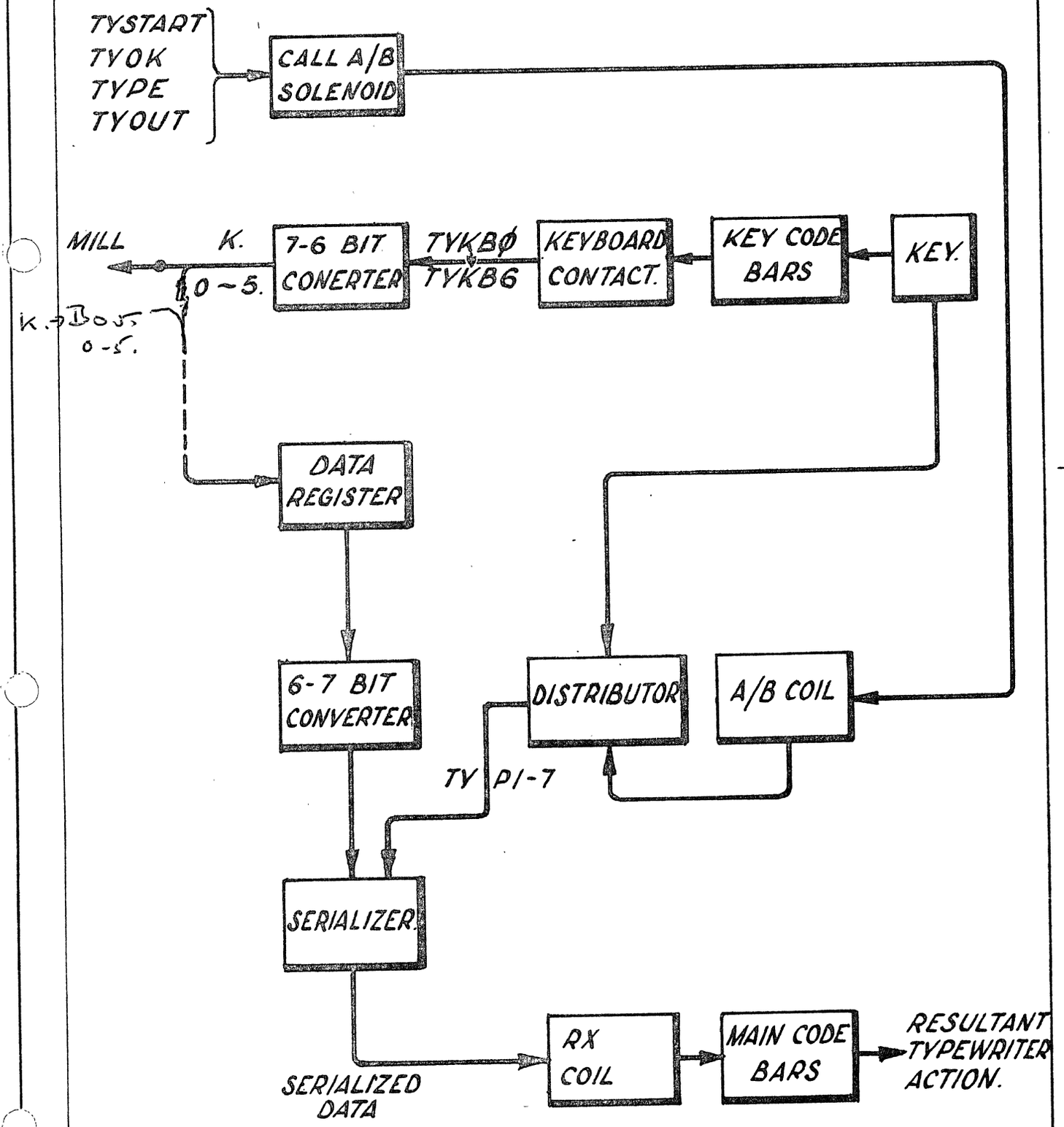
b) I/P



When Buffer Control has dealt with a BURST of 4 characters the End of Transfer signals are generated to inform logic relevant to peripheral.

Iss 1.

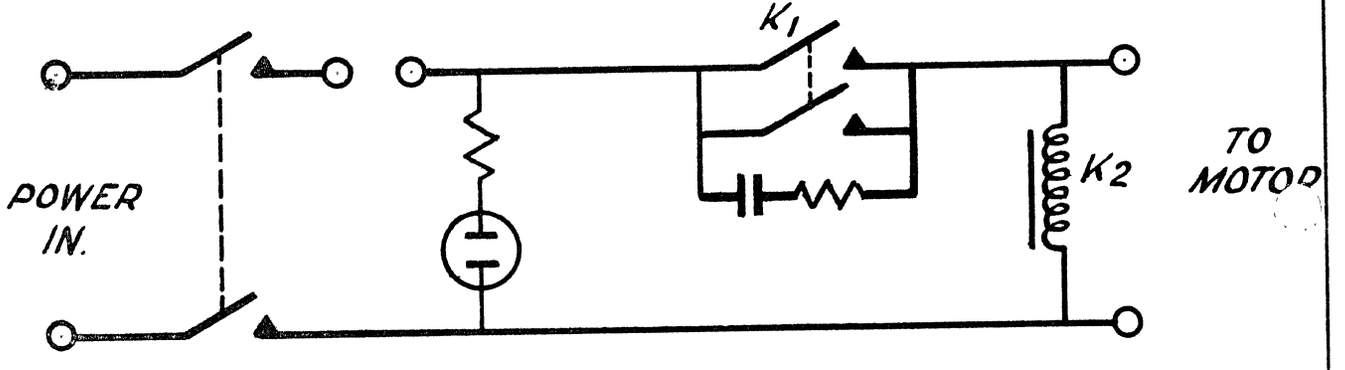
TYPEWRITER. ~ BASIC BLOCK DIAGRAM.

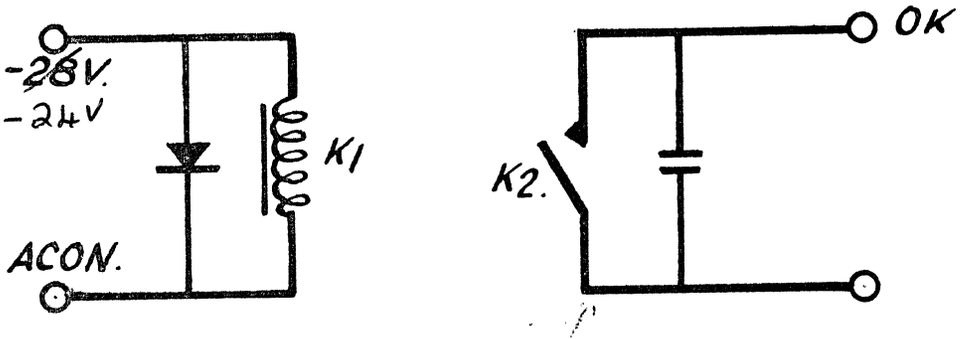


 ETD 3510 FORM 8/133/B(2.69)

Iss 1.

TYPEWRITER MOTOR SUPPLY.



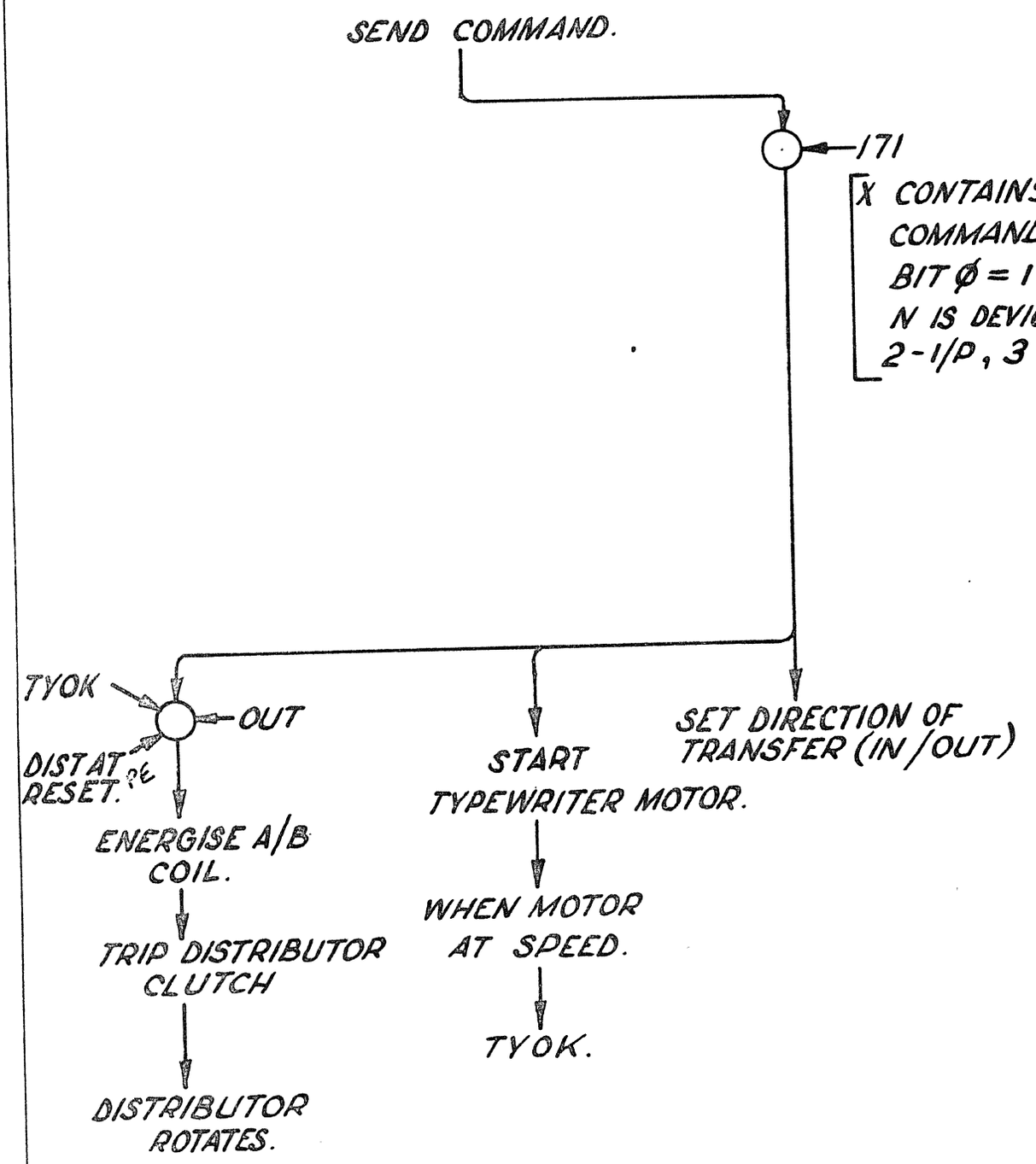


K1.- CONTACTS CLOSE IMMEDIATELY ON ENERGISING OPEN AFTER 5~180 SECS ON DE-ENERGISING.

K2.- CONTACT OPENS AFTER 3 SECS ON ENERGISING CLOSES IMMEDIATELY ON DE-ENERGISING.

Iss 1.

CONSOLE TYPEWRITER
1. COMMANDS.
(a. ~ 171)

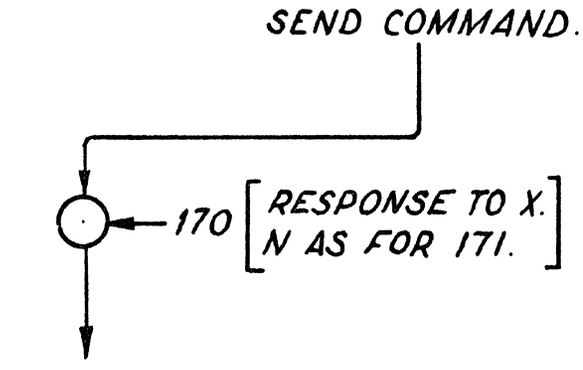


Iss 1.

CONSOLE TYPEWRITER.

1. COMMANDS.

(b. ~ 170)



SENSE STATUS
RESPONSE.

BIT Ø ~ END OF TRANSFER
BIT 5 ~ BUSY.
} I/P.

BITS 6~13 CONSOLE PUSHBUTTONS ~ I/P ONLY.

Iss 1.

2. DATA TRANSFER

a.) NORMAL O/P

DISTRIBUTOR REACHES P.I.

SET HES REQ. INTERLOCK.

RESET AT END OF DISTRIBUTOR CYCLE.

SET HES. REQ.STAT.

REQUEST HESITATION

BREAKPOINT (ALLOW INT.)

ENTER HES SEQUENCE MICROPROGRAM

FETCH & UPDATE CONTROL WORDS.

ENTER TYPE HES.SEQ.

RESET HES. REQ. STAT.

GENERATE.

1. CW. ADDRESS. WHEN HESITATION SELECTED.
2. PERIPHERAL ADDRESS ON 'BAD' LINES.

FETCH DATA CHAR.

TEST CHAR. FOR:-

1. NIL SHIFT NEW LINE CHAR (*77)
2. SHIFT CONTROL CHAR (*76, 5 OR 4)
3. DATA CHAR. PROPER.

(A)

ROUTE CHAR. TO TYPEWRITER.

EXIT FROM SEQUENCE.

b.) NORMAL I/P.

OPERATOR PRESSES KEY.

↓

MECHANICALLY TRIP DISTRIBUTOR. CLUTCH.

↓

DISTRIBUTOR REACHES P.1.

↓

SET HES REQ. INTERLOCK.

↓

RESET AT END. OF DISTRIBUTOR CYCLE.

SET HES. REQ. STAT.

↓

REQUEST HESITATION

↓

BREAKPOINT.

↓

ENTER HESITATION SEQUENCE MICROPROGRAM.

↓

FETCH AND UPDATE CONTROL WORDS

↓

ENTER TYPEWRITER HESITATION SEQUENCE.

↓

1. ROUTE CHAR TO STORE
2. CHARACTER GATED INTO DATA REGISTER & ROUTED TO TYPEWRITER VIA 6~7 BIT CONVERTER.

↓

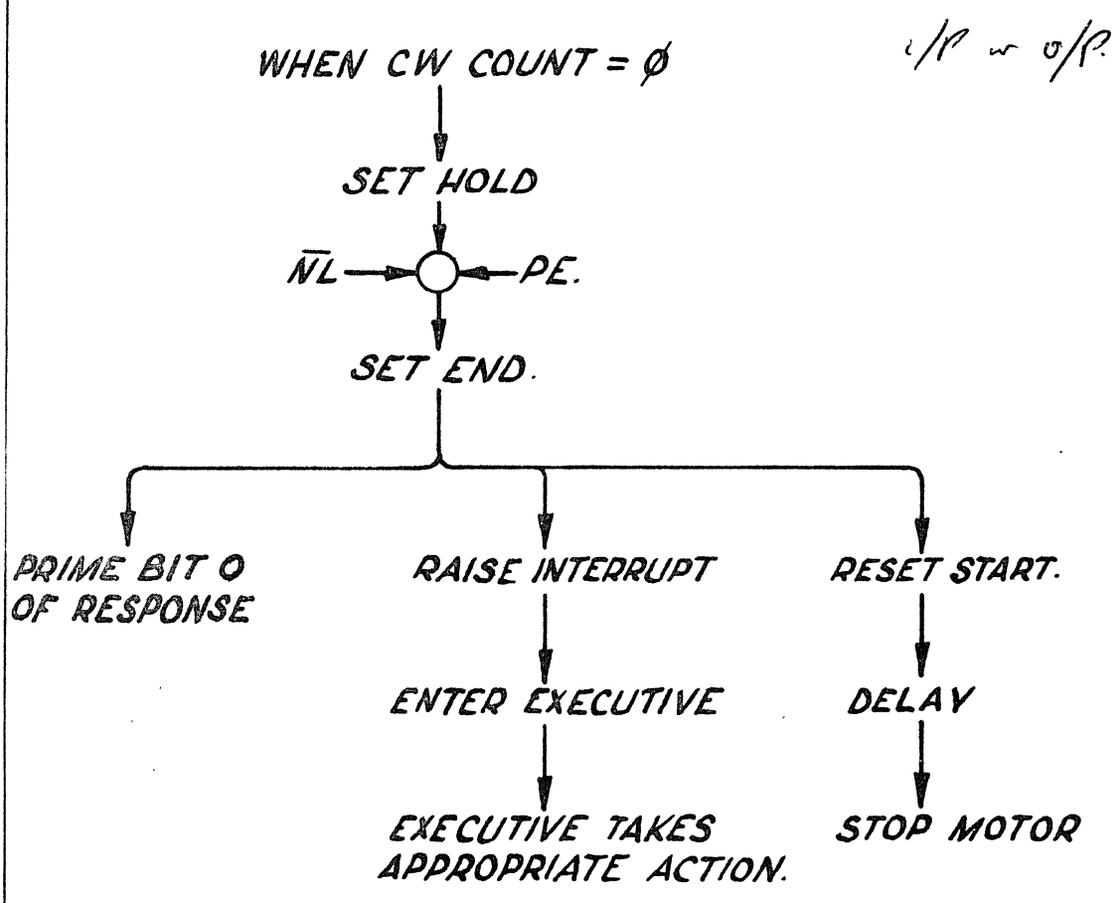
EXIT FROM SEQUENCE.

GENERATE :-

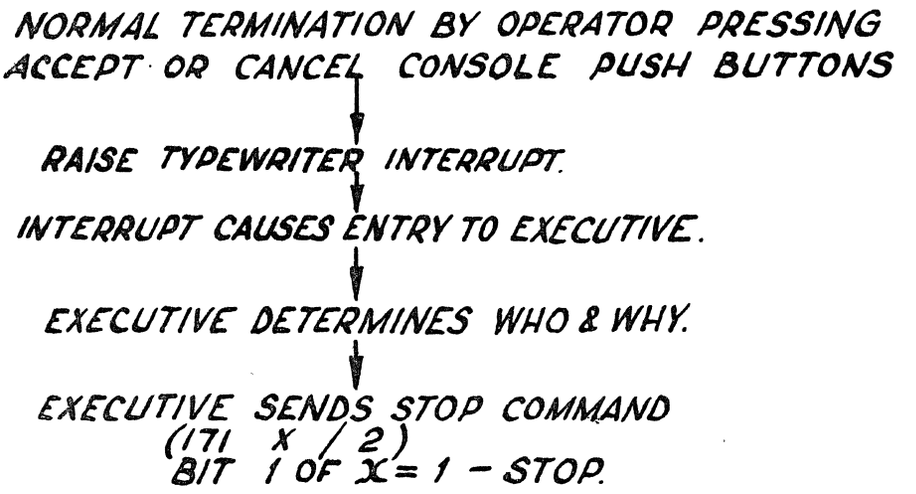
1. CW ADDRESS. WHEN HESITATION REQUEST SELECTED.
2. PERIPHERAL ADDRESS ON BAD LINES

Iss 1.

3. TERMINATION OF TRANSFER



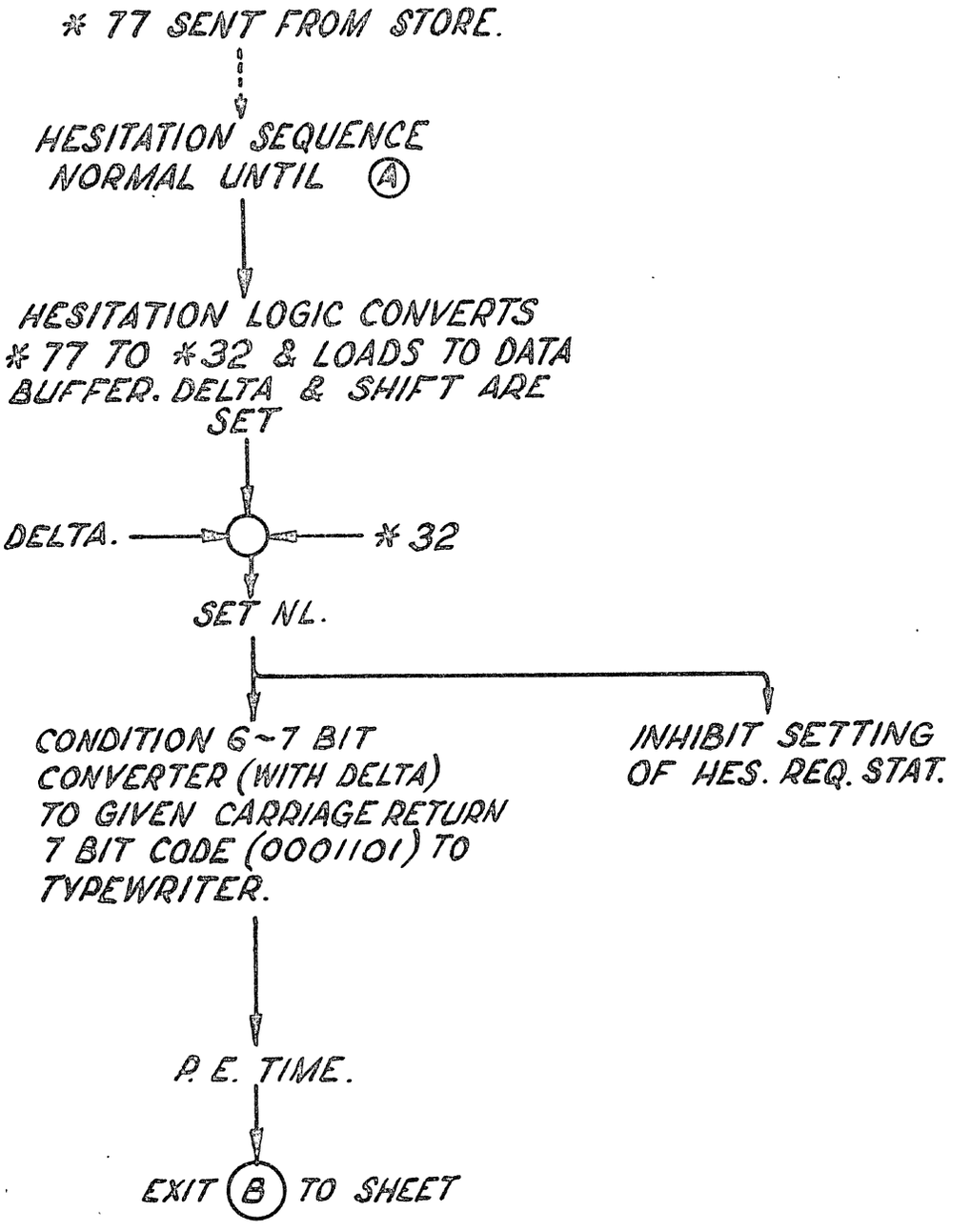
b) I/P



ISS 1.

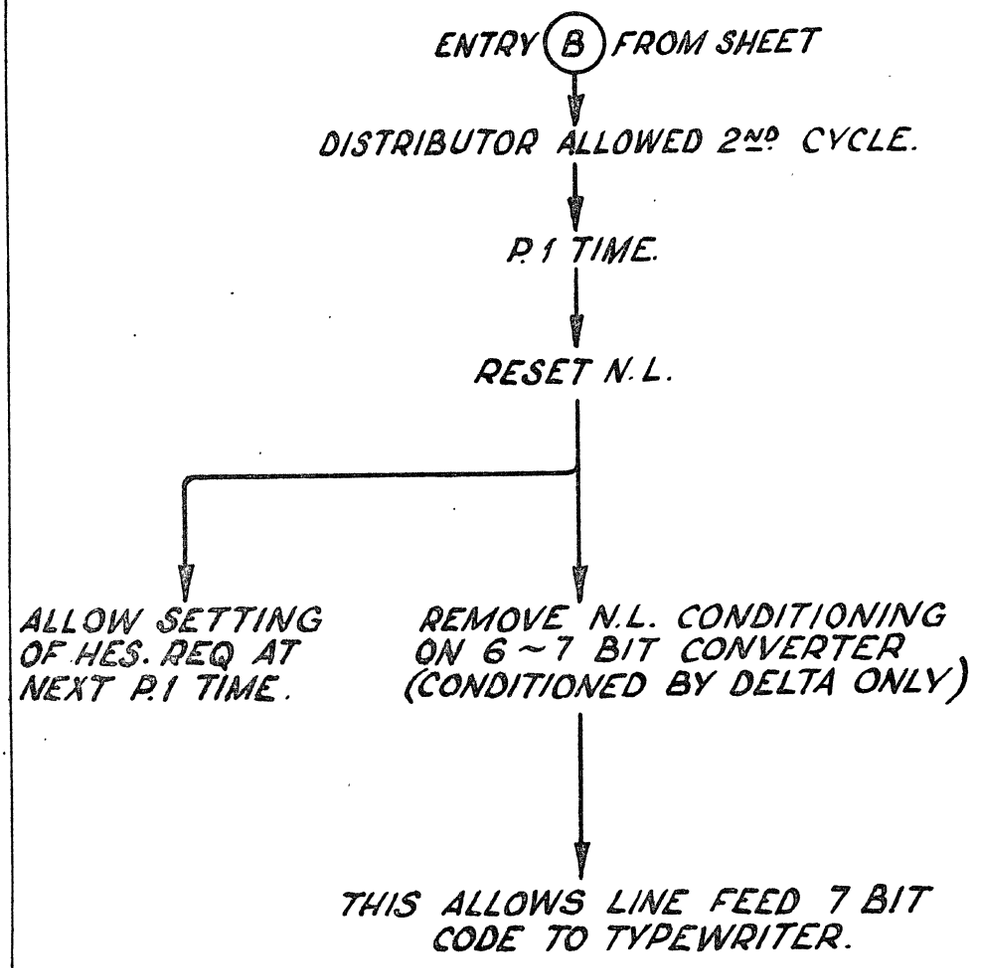
O/P OF NIL SHIFT NEWLINE CHAR. (*77)

NEW LINE IS NORMALLY A DELTA SHIFT CHAR (*32) & THEREFORE 2 CHARS WOULD BE SENT FROM STORE TO OBTAIN THIS ACTION. THE TYPEWRITER CONTROL LOGIC IS DESIGNED HOWEVER TO RECOGNISE *77 AS A NEWLINE CHAR.



Iss 1.

O/P OF NIL SHIFT NEWLINE CHAR. (*77) (CONT.)



MULTIPLY

Computer method very similar to normal pencil and paper method.

ie.

0101	MCD	
0011	MPR	Note. P.P. kept in correct perspective to bit of M.P.R.
0101	P.P.1.	
0101	P.P.2.	
0000	P.P.3.	
0000	P.P.4.	
0001111	Final Product = Sum of P.P.	

The computer method varies in one basic aspect, the partial products are summed as the multiply proceeds.

ie.

0101 0011

0000		(Initial product = 0).
0101		Add MCD & Shift P.P.
0101		
0010	1	
0101		
0111		
0011	11	SHIFT P.P.
0000		
0011		
0001	111	

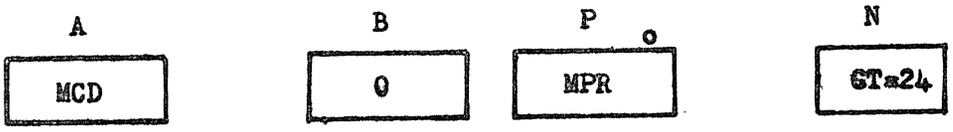
Note.

SHIFT keeps sum of P.Ps in correct perspective to M.C.B.

Rule:- Test each bit of MPR
=1 - Add MCD & SHIFT P.P.
=0 - SHIFT P.P.

USE OF REGISTERS.

INITIAL CONTENTS

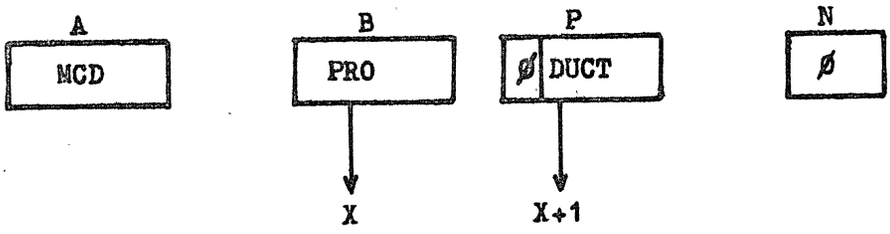


Action

Test L.S. bit of M.P.R.
If=1, Add MCD in A to Sum of P.P. in B & Shift B2P one place right. P.P. expands into P as M.P.R. is shifted out.

After 24 shifts Final Products contained in B & P.

FINAL CONTENTS.



DIVIDE

Use 1904 Division notes to explain principle.

USE OF REGISTERS

INITIAL CONTENTS.

Action.

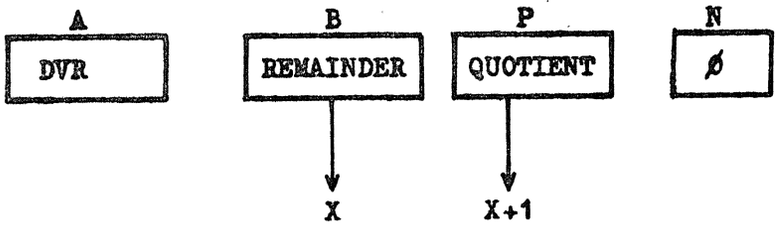
1. Test DVR & DVD or P.R. signs.
   If equal, subtract DVR from DVD or P.R.
   If unequal, Add DVR to DVD or P.R.

2. Test Sign of Arithmetic result against DVR sign, if equal set '1' to Quotient.

3. Shift B & P left one place, Quotient Bit set to PØ.

4. After 24 Shifts division complete with Quotient in P & Remainder in B.

FINAL CONTENTS.



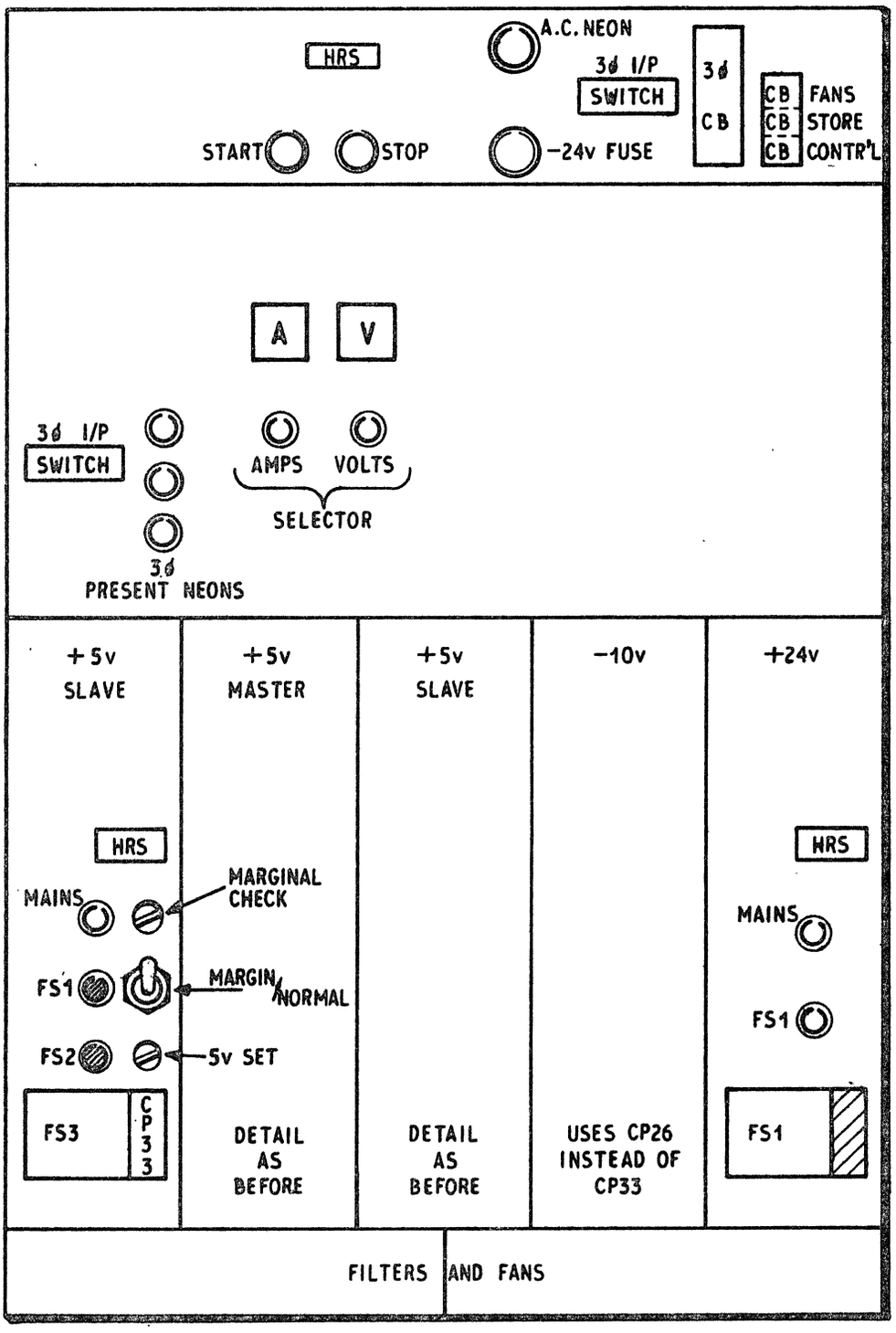
POWER SUPPLY UNIT

Iss 1.

A.C. CONTROL

METER PANEL

POWER SUPPLY UNITS



 ETD 3522

Power Supplies.

Consists of 3 Units.

1. +5v - Basic Logic Supply
2. +24v - Typewriter
3. -10v - Hybrid Gets & Interface supply.

+5v. Supply

Derived from a MASTER UNIT & 2 SLAVE UNITS.

Master / Slave Relationship.

Main BUSBAR sensing performed by Master. The master has a stabilised Reference Voltage. The Regulated o/p of the Master is used as a Reference voltage for the Slave Units.

As BUSBAR voltage varies, the Master will compensate altering the Reference to the slaves correcting their o/p.

+5v - MASTER / SLAVE LINKING.

PIN M - Sense for MASTER from +5v BUSBAR

PIN D - Sense for SLAVES, taken from PIN A. Which is equivalent to their own o/p.

PINS E&L - Common Reference (0V) ; linked to PIN E on SLAVE UNITS from E & L on MASTER.

B&C - Linked on MASTER only. Provides Reference voltage by linking REF IN TO REF OUT.

A&K - On MASTER. Linked to B on SLAVES to provide SLAVES REFERENCE VOLTAGE from MASTERS +5v STABILISED O/P.

J&F - Carry +5vto +5v UNDER VOLTAGE PROTECTION CCT in - 10v SUPPLY. Inhibits drive to - 10v series regulator in event of +5v failure.

N - Not connected.

H - Pin H on MASTER & SLAVES interconnected. INT. SCR GATE connection fires S.C.Rs in all units if any one fires. EXT SCR GATE O/P fires SCR across +5v o/p.

+5v - SERIES REGULATOR.

HS1-4

VT3&4 - Series Regulator Transistors
1&2

Each pair gives two equivalent o/ps ;
one to + 5v BUSBAR, the other for
Internal use.

Internal Uses

1. Master
Provides Reference voltage for slaves.
(via SKB pins A & K to SKT3 pin B on Slaves)

2. Slaves.
Provides sense for slaves.
(Pin A - Pin D)

Cct External to CP33 HS1-4

VT1, 2 & 3. Emitter Follower driven by VT1 in CP33.
VT1 drives HS1&2
VT2 drives HS3&4

RV1 - Marginal Voltage Adjust used to set o/p 10% below nominal for Test Purposes.

RV2 - Normal Voltage Adjust.

RV3 - Sets level at which overload cct to operate

DZ1 - Final stage of reference stabilisation on Master - not used on Slaves.

CP33 (+5v STABILISER)

Major Components.

VT1 - Drive to Series Regulator (via Emitter Follower).

VT2 - Normal feedback control to VT1

VT3 - Current Source

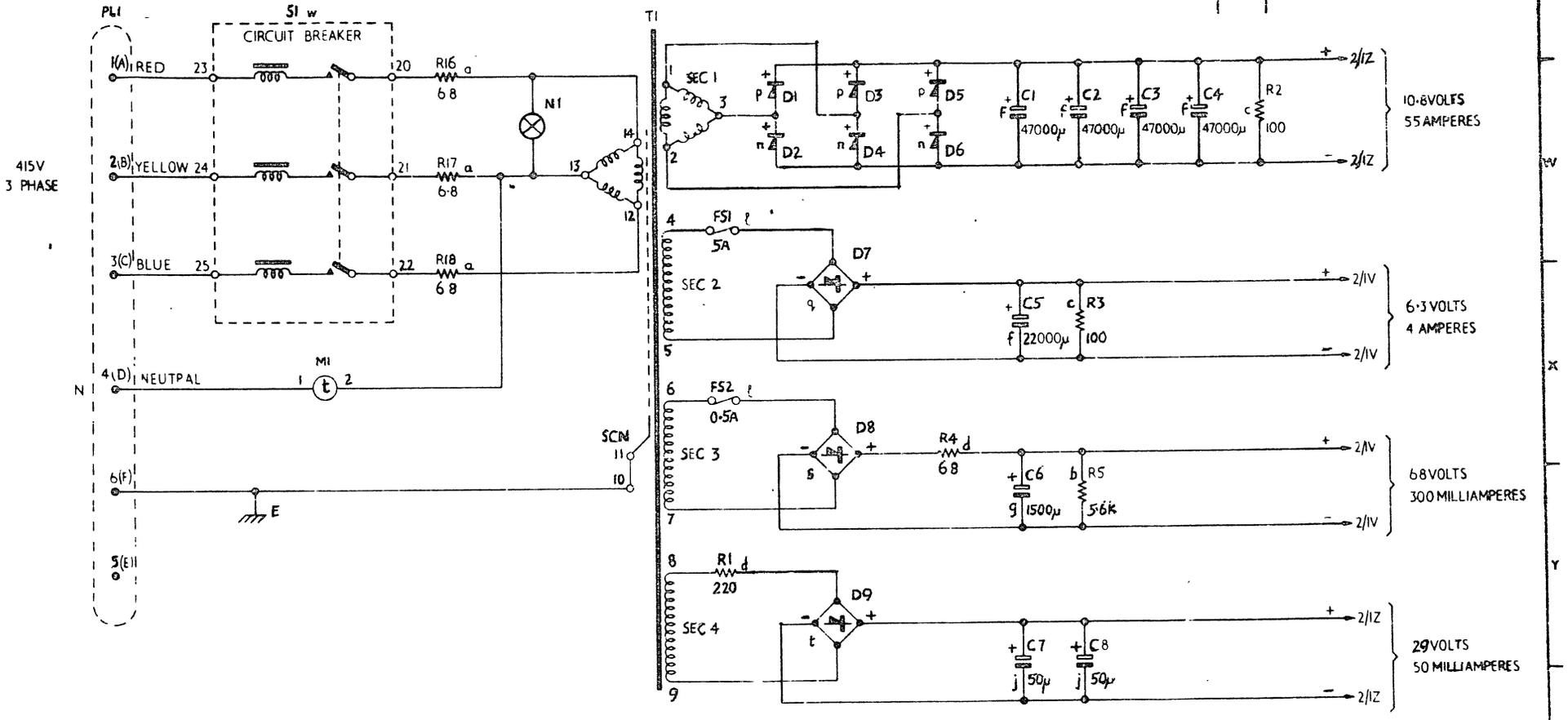
VT4 - Overload drive to VT1. Set to cut in when surge current results in VT2 giving insufficient drive to VT1. Increases current through Series Regulator.

SR1 - Internal S.C.R. When fired cuts off drive to VT1 & hence to Series Regulator.
SR1 is fired by OVERVOLTAGE PROTECTION CCT.

VT6-9 - overvoltage Protection Circuit. If +5v goes too high, Base B of VT6 goes high (Base A = Reference) switching on VT7. Amplified through VT7,8 & 9; this fires SR1 and SCR1 (5030229,SW2).
Normal condition - VT7, 8 & 9- OFF.

DRG. No. 5030229

ISS.	CHANGES
9	XC-PSU 3" REDRAWN AS TECH. CHANGE 5-68
10	P470 32 7 69
11	7609 8-69



RECTIFIER & CAPACITOR (5V CRUDE)

MATERIAL	HEAT TREATMENT	SURFACE TREATMENT

I.C.T.

TITLE: POWER SUPPLY CIRCUIT DIAGRAM

5030229/11 ISSUE | 1 SHEET | D CAT.

ISSUE 11

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

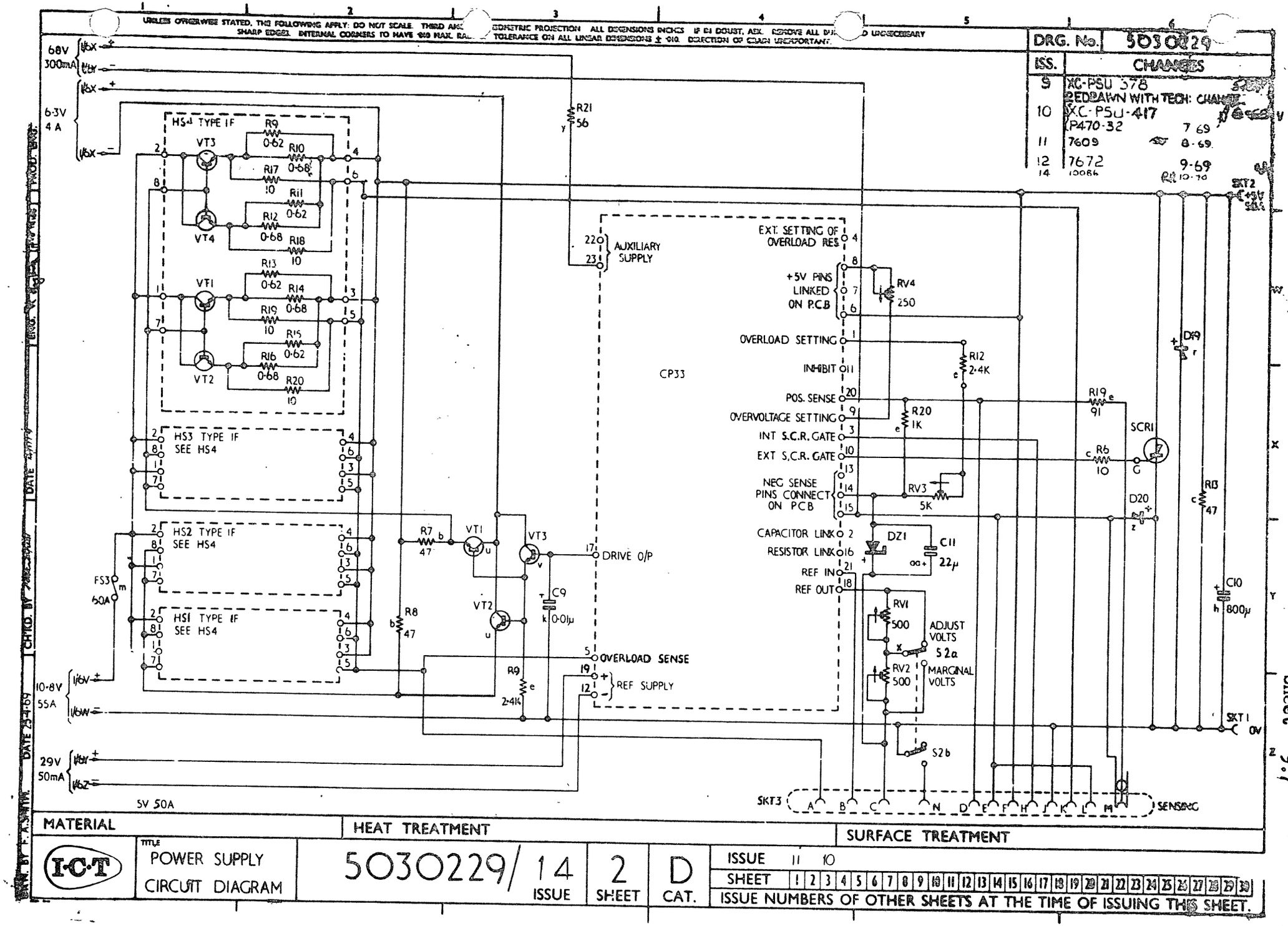
ISSUE NUMBERS OF OTHER SHEETS AT THE TIME OF ISSUING THIS SHEET.

DATE 12 12 68 | CH'KD BY | DATE | ENG. | PROD ENG

ETD.3527

Sheet 9.6

ETD 3528



MATERIAL	HEAT TREATMENT	SURFACE TREATMENT

I·C·T	TITLE: POWER SUPPLY CIRCUIT DIAGRAM	5030229/14 ISSUE	2 SHEET	D CAT.

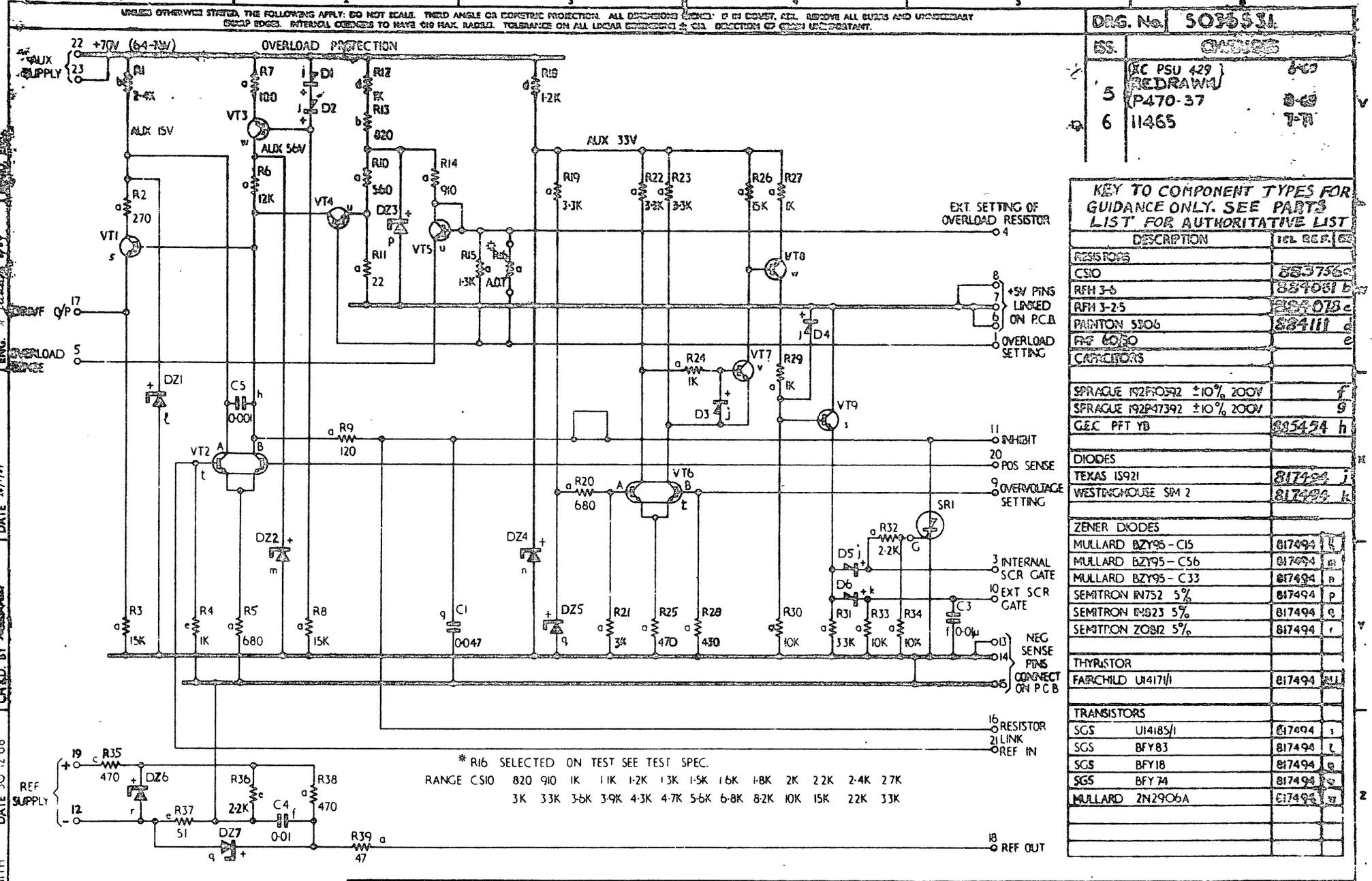
ISSUE 11 10

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

ISSUE NUMBERS OF OTHER SHEETS AT THE TIME OF ISSUING THIS SHEET.

Sheet 9.7

ETD 3528



DRG. No.	5036531
ISS.	[illegible]
5	IC PSU 429 REDRAWN
6	P470-37 11465

KEY TO COMPONENT TYPES FOR GUIDANCE ONLY. SEE PARTS LIST FOR AUTHORITATIVE LIST

DESCRIPTION	REL. REF.	CC
RESISTORS		
CS10	883756	a
RFH 3-6	884081	b
RFH 3-2·5	884078	c
PAINTON 5206	884111	d
PHC 60/50		e
CAPACITORS		
SPRAGUE 192P10392 ±10% 200V		f
SPRAGUE 192P47392 ±10% 200V		g
G.E.C. PFT YB	885454	h
DIODES		
TEXAS IS921	817494	j
WESTINGHOUSE SM 2	817494	k
ZENER DIODES		
MULLARD BZY95 - C15	817494	l
MULLARD BZY95 - C56	817494	m
MULLARD BZY95 - C33	817494	n
SEMITRON IN752 5%	817494	p
SEMITRON IN823 5%	817494	q
SEMITRON ZO8I2 5%	817494	r
THYRISTOR		
FAIRCHILD U14171/1	817494	N.U.
TRANSISTORS		
SGS U14185/1	817494	s
SGS BFY83	817494	t
SGS BFY18	817494	u
SGS BFY74	817494	v
MULLARD 2N2906A	817494	w

1904A MODULE 4

Sheet 9.8

DRN. BY V.M.SMITH	DATE 30.12.68	CHKD. BY	DATE	ENG.	DRWG.

E70. 3529

5V STABILISER

HEAT TREATMENT

SURFACE TREATMENT

I·C·T

TITLE CIRCUIT DIAGRAM CP33

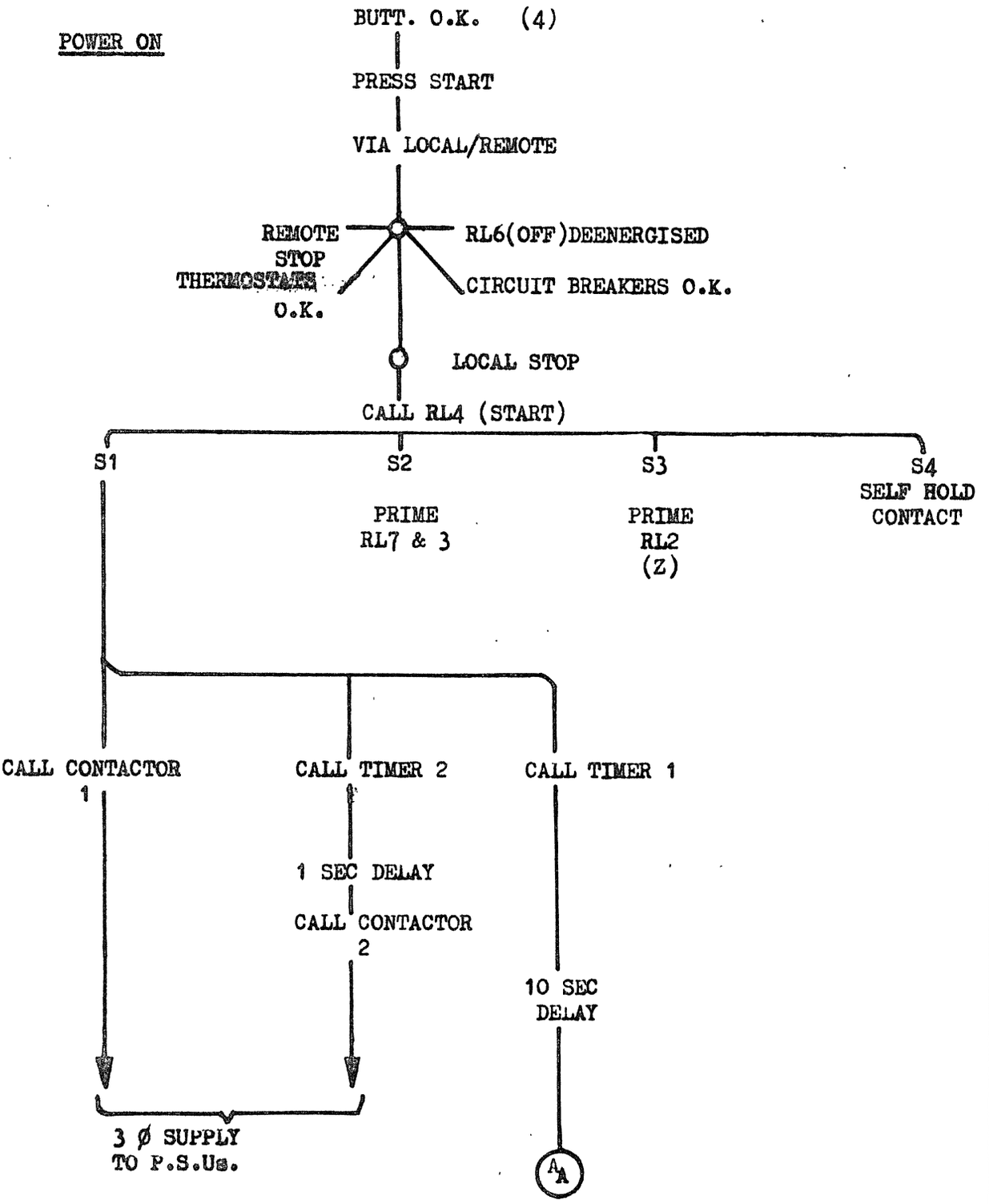
5036531/6 ISSUE | 1 SHEET | D CAT.

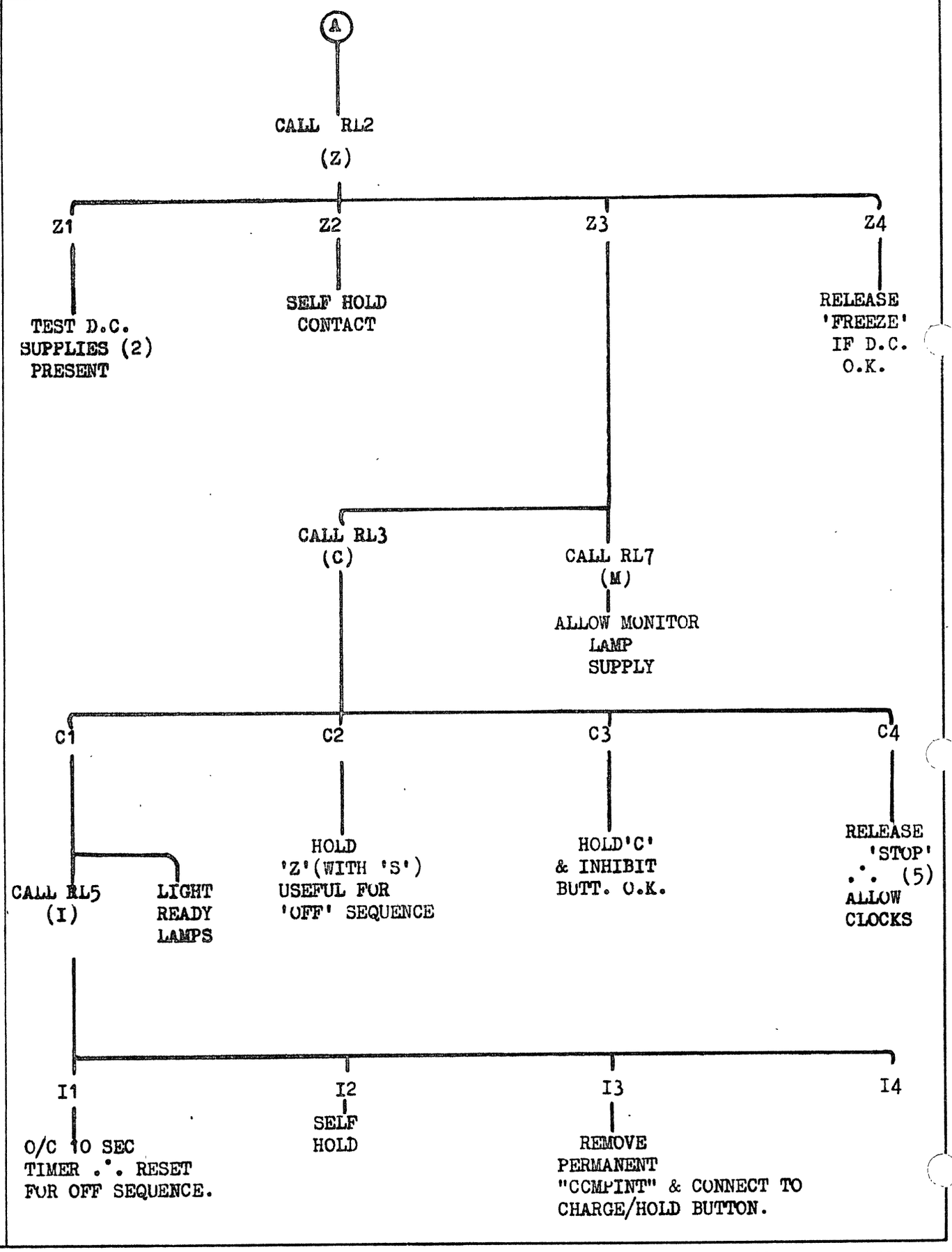
ISSUE

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29

ISSUE NUMBERS OTHER SHEETS AT THE TIME OF ISSUING THIS SHEET.

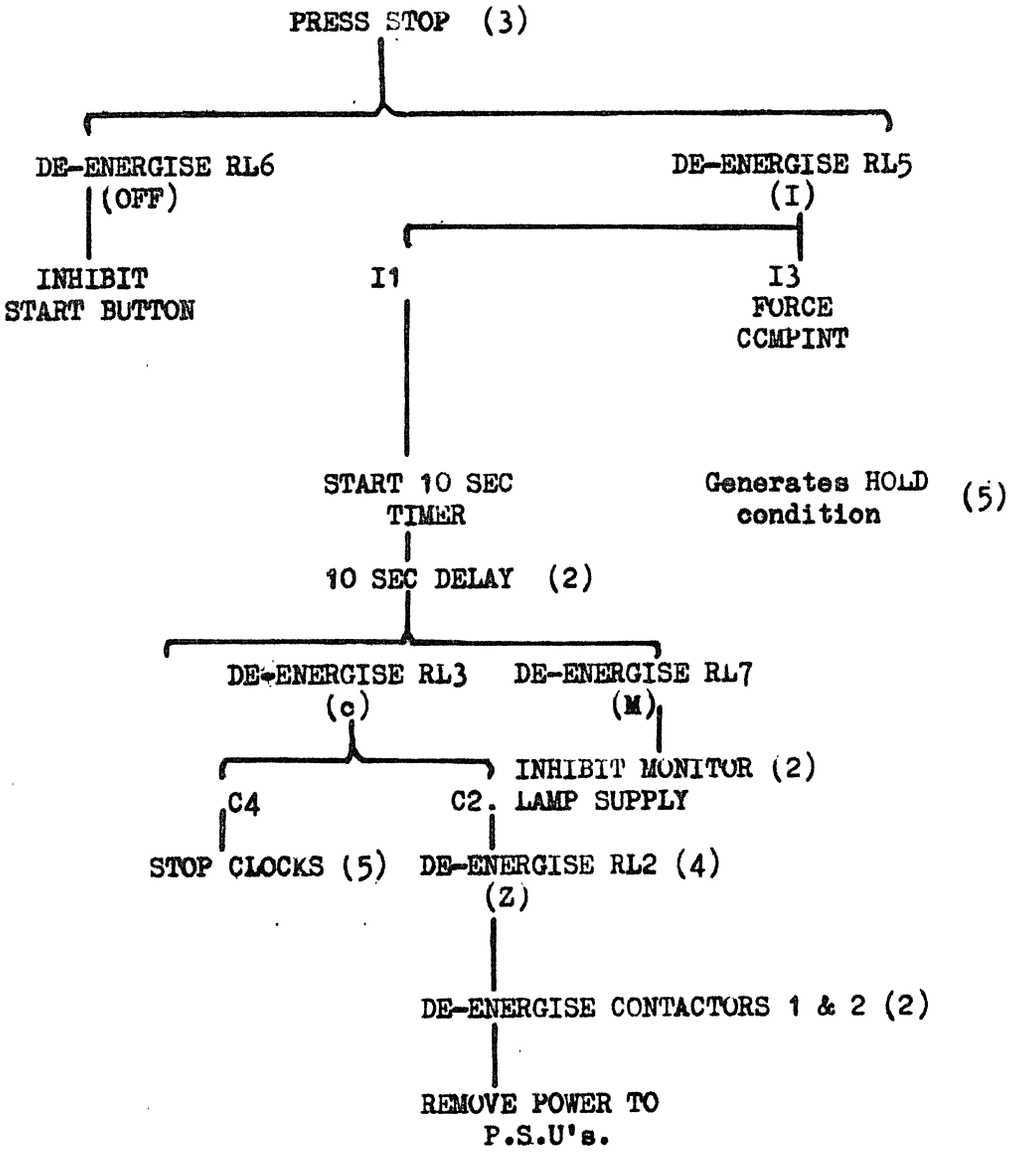
POWER ON/OFF SEQUENCE





 ETD3531

POWER OFF



Iss 1.

USE OF TEST MANUAL INDEX

1. To obtain an INDEX if required.
The program ≠≠STEL may be used to output on a L.P. the programs contained on an Engineers Library Tape (PROGRAM ELIB) in:-

   a) ALPHABETIC order

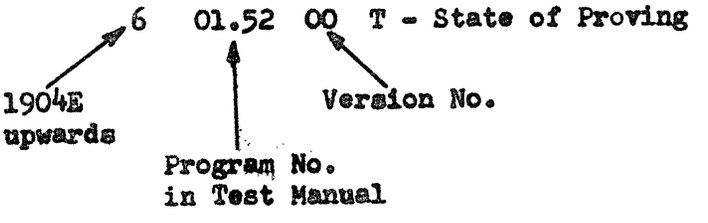
   b) NUMERIC order.

2. The Test Manual refers to programs by a numbering system.

   M . GG . NN . VV . P

   M = Machine(s) on which programs will run.
   GG = Program Group) Form program
   NN = No. within group) number.
   VV = Version No.
   P = State of proving (may not be present in manual).

   EG.



See INFORMATION SHEET obtained using ≠≠A000 for full details.

 ETD 3533

Iss 1

INFORMATION NOTICE SYSTEM

Purpose

To provide a system of Program error reporting and amendments to Test Program Manual.

Method

Each notice is contained in an object program as data to be printed. Programs are currently in the series:-

AØØØ onwards.

Access

Information obtained by Finding the desired program.

Action

EG. F1,≠≠AØØØ≠≠ELIB.

The program AØØØ is found, loaded to store and entered automatically. On completion it generates the message:-

F1≠≠AØØ1≠≠ELIB and deletes ≠≠AØØØ

The same action occurs for this program and remainder until last notice is output.

Note: To o/p a single notice.

EG AØØ6

F1,≠≠AØØ6≠≠ELIB

on completion of o/p

F1≠≠AØØ7ØELIB is issued and ≠≠A006 deleted.

To terminate search for ≠≠A007,DE≠≠ELIB.

Iss 1.

NAME ≠CORE

TEST PROG No. 003.50.00

PURPOSE

To provide, in conjunction with other test programs, more complete confidence checks on the system.

ACTION

The program expands and/or contracts its core allocation, thereby moving programs above it up and down the remaining store.

Note: Test progs must be loaded after ≠CORE and be in a running condition.

OPERATING INSTRUCTIONS

1. F1,≠CORE,≠ELIB.

2. Set Word Ø = to multiple of 128
AL,≠CORE Ø 512
Each change in core size will be equal to 512 words.

3. Entry Points:-

GO,≠ CORE N
N=20 - Increases store size by set amount until all free core used and restarts from minimum allocation.

N=21 - Commences at maximum and contracts to minimum.

N=22 - Combination of 20 and 21.

To operate successfully the program requires a peripheral.
If SW. =Ø, program reserves a LP.
If none available a scratch tape is requested and M.T. will be used.
If SW. ≠0 program suspended after core size change and must be restarted by GO,≠CORE.

Iss 1.

NAME ≠≠FLIT (FUNCTIONAL & LOGICAL INSTRUCTIONS TEST).

TEST PROG No. 601.52.00

PURPOSE

To provide a basic processor and store confidence test with diagnostic facilities on machines 1904E upwards.

OPERATING INSTRUCTIONS

Set S.W. to following value if required:-

ON ≠≠FLIT Ø - Dont test F.P.U.
1 - Display name of each routine at its exit.
2 - Loop on failures.

Entry Points:-

GO ≠≠FLIT 20 - 1904A, 1907, 1905F.
21 - 1906, 1904E, 1904F with Extracode F.P.
22 - 1905E.
23 - 1906A (Switch Ø must be ON because of Ext. Precision F.P.U.).

ERROR messages - See FLIT manual.

Exceptions for ≠≠FLIT

1. JUMN - where n is the starting address of the last successfully entered routine.

2. After a failure in X2 the program does not halt.

Iss 1.

NAME ≠≠ENGL.

TEST PROG No. 072.14.03

PURPOSE

1. To create or update an Engineers Library tape (PROGRAM ELIB) listing new version on L.P.

2. To list contents of an existing PROGRAM ELIB on L.P.

METHOD

Steering lines are punched on cards or P.T. to control each run of ENGL.

For full description of steering lines see TEST PROG MANUAL.

EG 1) To copy current PROGRAM ELIB tape.

P.T. Steering Lines

```
B/6  NL    Type of Bootstrap
C    NL    Copy from current position to End
E    NL    End of Steering lines
```

2) To add ≠≠DUPL after ≠≠CORE on current PROGRAM ELIB.

P.T Steering Lines

```
B/6
C/CORE≠≠Ø35ØØØC
P/DUPL≠72Ø6Ø1T
C
E
```

Note: Prog names must be in full 12 char format as shown in T.P. manual.

If Steering lines from cards then one line per card.

OPERATING INSTRUCTIONS

1. Create a Scratch Tape (See ≠≠XQMY for details).
2. Load steering lines on appropriate device.
3. Ensure Program Elib and Scratch Tape on line.
4. Entry Points:-
   GO≠≠ENGL N
   N = 20 - Steering lines and programs to be added on P.T.
   N = 21 - As above but cards.
   Listing of new version automatic in above cases.
   N = 22 - List current Program Elib tape (Steps 1 and 2 not required and only Program Elib required on line).
   N = 29 - Abandon current ru.
   For full details of ERROR messages etc. see T.P. Manual.

Iss 1.

NAME ≠≠FPU2.

TEST PROG No. 001.04.00

PURPOSE

To test Hardware Floating Point Unit.

OPERATING INSTRUCTIONS

1. GO≠≠FPU2 20 - Start Test.

2. After error

   a) GO≠≠FPU2 or GO≠≠FPU2 21 - repeat failed instruction before continuing test.

   b) GO≠≠FPU2 22 - Continue test without repeating failed instruction.

   c) GO≠≠FPU2 23 - Output details of failed instruction.

   Format:-

   A) After initial error
      GP Addr - Address of 1st instruction in Group
      ANS - Actual Answer (Double Length).

   B) After GO@23
      Instruction
      1st and 2nd Operands
      Expected results.

For complete facilities see T.P. Manual.

Iss 1.

NAME ØØLBRY

TEST PROG No. 072.01.03

PURPOSE

To take object or Executive mode programs from a LIBRARY tape and punch them out on paper tape or cards.

METHOD

Steering lines are punched to control each run of the program.
LBRY reads in the steering lines and opens PROGRAM ELIB unless otherwise specified.
Programs are then punched out on desired medium.
See T.P. manual for full steering line details.

OPERATING INSTRUCTIONS

1. Load appropriate library tape.

2. Load Steering lines to P.T.R. or C.R.

3. GO ØØLBRY 20 for P.T.
   or 21 for Cards.

4. When first program punched the following message is output:

   ØØLBRY DISPLAY : LOAD O/P ON READER
   ØØLBRY UNIT n FIX.

   This is the invitation to load the punched program for checking.
   If O.K. message o/p will be

   ØØLBRY DISPLAY : name CHECKED OK

When all programs punched and checked the following message is output:

ØØLBRY HALTED :- END OF RUN.

See T.P. Manual for full details of:-

1. Error messages.
2. Restart procedures.
3. Abandonment.

Iss
1.

NAME ≠ IOHS

TEST PROG No. 001.10.00

PURPOSE

To test each of the large orders using variable operands

e.g.	MULTIPLY	SHIFTS (LOG & ARITH)
	DIVIDE	NORMALISE
	DEC BIN	MOVE (126)
	BIN DEC	SUM (127)

OPERATING INSTRUCTIONS

1. Load program.

2. Enter program at location determined by order to be tested (See T.P. Manual for details).

ERRORS

If error, message o/p will be:-

≠IOHS: HALTED :- XY
Where XY indicates function in error
(See T.P. Manual for details).

Iss 1.

NAME MCST

LIB No. 9813 (For 1904A)

TEST PROG No. 6033402 (For 1904A)

PURPOSE

To provide a comprehensive Store test.

METHOD

The program occupies an area in store (D to D+°3777) and tests the remainder of Store around this area working forwards and backwards. Four patterns are used in the tests (see T.P Manual for detail). There are 16 subtests forming a cycle. When a cycle of tests is complete, the program copies itself °4000 locations up the store and starts again.

OPERATING INSTRUCTIONS

1. Load Program using FRZ & CREST routine.
2. HOW MANY K? O/P on console.
3. Type answer (EG. 32, 64 or 96 as appropriate.

ERROR INDICATION

Basic o/p message in format:-

P1 B T2 A _ _ _ _ W _ _ _ _ R _ _ _ _

Pattern No.		Test No.	Written Pattern	Pattern Read
	Forwards or backwards thro' Store		Failed location address	

OTHER FACILITIES

See T.P. Manual.

Iss 1

NAME PACT

LIB No. 9575

TEST PROG No. 6012202

PURPOSE

To measure the character data transfer rate on the 1904E and 1904A P.A.C.

By using 'TEST HES' switch the S.H.C. may also be tested.

OPERATING INSTRUCTIONS

1. Load program using FRZ & CREST routine (Timer inhibited).
2. Timer ON & P.A.C. clock to RUN.
3. Activate desired 'R' line.
4. Press F1 or F2 buttons as required by program.

Individual buffers may be tested or several buffers may be tested simultaneously.

For label of expected results and restart procedure see T.P. Manual.

Iss 1.

NAME PM6X

AVAILABLE ON PAPER TAPE

PURPOSE

To output on the line printer a POST MORTEM of EXECUTIVE. (E6BM)

PROCEDURE

See notes attached to "Loading Facilities for MK5 EXECUTIVE.

Iss 1.

NAME ≠SENG (Sort Eng. Lib. Tape)

TEST PROG No. 072.07.01

PURPOSE

To copy an Engineers Library (PROGRAM ELIB tape) putting programs on the tape into the order specified on steering lines input by P.T. or cards.

OPERATING INSTRUCTIONS

1. Decide on desired order or programs and punch up steering lines on desired medium.
(See T.P. Manual for details)
(of steering line format)

2. Load steering lines to reader and put desired Mag. Tapes on line.

3. Enter program at:-

locn 20 - steering lines on P.T.
21 - " " " Cards.

To abandon run enter at any time at locn 29.

4. The new version is listed in the same way as ≠ENGL.

See T.P. Manual for error recovery procedure.

Example of steering lines

A program tape has 400 programs. It is required to place 294 after 129 and 308 after 221 (use ≠ENGL listing to obtain Numbers)

MTIN = PROGRAM ELIB / REEL No. / GEN No.

Mandatory

Both optional, assumed Ø if omitted. Describes input tape

MTOU = xxxxxxxxxxxx/yyyy/zzzz

Optional - Describes tape to be used for o/p.
If omitted, a scratch will be opened.

MTRN = ----------/xxxx/1111

Optional - Name to be given to new tape.
If omitted assumes i/p tape name with GEN No.+1

Iss 1.

```
****
1 - 129
294
130 - 221
308
:
```

(Note: Switch Ø unset results in unlisted programs being copied to new tape).

Numbering must always begin with 1, since ≠≠LIB must be the first program on tape.

Iss 1.

NAME ≠STEL.

TEST PROG No. 072.16.03

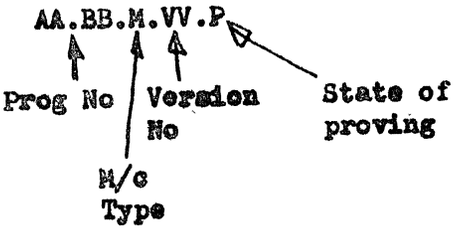
PURPOSE

To sort the descriptions of programs on the Engineers Library using the description in each programs Information block (see ≠ENGL description in T.P. Manual for detail) into:-

1. Alphabetic order (Prog Names)

2. Numeric order (Prog No's)

Format AA.BB.M.VV.P



Useful to provide a T.P. Manual Index.

OPERATING INSTRUCTIONS

To obtain a single copy of sorted descriptions on Line Printer

GO≠STEL 22 - Numeric Sort

GO≠STEL 23 - Alphabetic Sort

To abandon run

GO≠STEL 29

For a full description of all other facilities offered see T.P. Manual.

Iss 1.

NAME ⫽XQMY

REFERENCE LIBRARY SPECIFICATIONS MANUAL (TP4011)

PURPOSE

To write a SCRATCH label to tape with Serial No. if a Virgin tape.

OPERATING INSTRUCTIONS

1. To relabel a tape which has a valid header.

   a) Load Tape to a deck.

   b) G1⫽XQMY n 0 where n = Deck Unit No.

   c) GO⫽XQMY 20 Start program.
   The existing label is read and words 1-7 are o/p on console:-

   O⫽XQMY ; DISPLAY - HR°TSN/NAME/RSN/FGN/XRP
   (See T.P.4011 for full details).

   d) GO⫽XQMY 21 - Write Scratch Label Message on console if O.K.
   O⫽XQMY ; HALTED n SCRATCH

   If read only required Unit n may be closed by GO⫽XQMY

2. To label a Virgin tape.

   a) A steering tape containing the serial number(s) must be punched on P.T. or cards.

   Format

   No's may be Dec or Octal, the latter preceded by an °

   EG Two virgin tapes to be labelled with serial no's 8 & °11

P.T.	Cards	
8NL	8	(Cols 1)
°11NL	°11	(Cols 1-3)
****NL	****	(Cols 1-4)

   No. Range - Decimal 7 digits
   Octal 8 digits.

   b) Load Virgin Tape(s).

   c) Load Steering Tape.

   d) G1⫽XQMY n Ø n = Deck Unit No.

   e) GO⫽XQMY 28 - Steering lines on PT
   29 - " " " Cards.
   Selected tape is labelled, if OK message o/p will be:-

   O⫽XQMY; HALTED:- N LABELLED.

   f) If more tapes to be labelled on Same run, re-enter Sequence at (d)
   When Terminator read, program halts with:-
   O⫽XQMY; HALTED:- OK

Iss 1.

NAME TYA

LIB No. 1201

TEST PROG No. 012.01.02

PURPOSE

To Test correct functioning of all Console Typewriter interrupts and that messages may input and output.

ENVIRONMENT

TYA is an EXECUTIVE MODE program which is loaded using FREEZE & CREST routine.

OPERATING INSTRUCTIONS

To start the program press any Console Push button. The program outputs the name of the button pressed.

i.e. Press INPUT, program outputs IN. After message output, INPUT lamp is lit and a message may be input. Message to be terminated with a NEWLINE operation. The message will output continuously until a console pushbutton is pressed.

Input may be terminated by pressing a console pushbutton.

Ticker must be inhibited.

For fuller details see Test Program Details.

Iss 1.

NAME ≠≠RFPD

TEST PROG No. NOT IN MANUAL.

PURPOSE

To provide a very stringent Hardware F.P.U. test.

OPERATING INSTRUCTIONS

GO≠≠RFPD 27 to obtain full driving instructions on Line Printer.

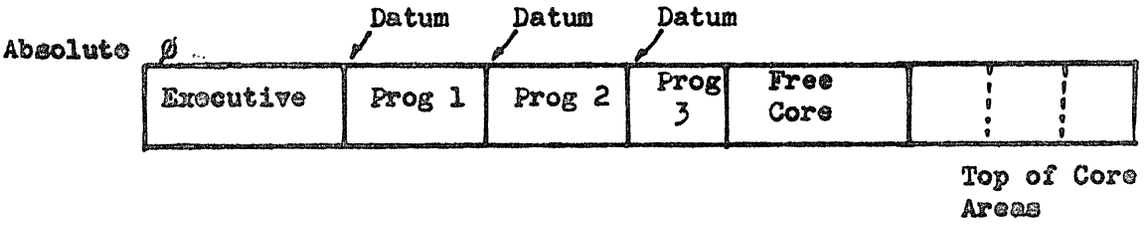
E6BM EXECUTIVE

1. Some general facts

1.1 Purpose of Executive.

a) To implement extracodes.
b) To control peripherals via B-Line Interrupt System.
c) To communicate with operator.
d) To 'Time-share' object programs.

1.2 Use of core.



1.3 Content of Executive Area.

a) Hesitation Control Words.
b) Tables, in two major groups:-

i) Concerned with programs.
ii) " " peripherals.

c) Sub-routines.
d) Main coding, with two entry points:-

°20 Involuntary entry.
°40 Voluntary entry.

1.4 Format of Executive on arrival.

Bootstrap.
Compiler.
Codeword List.
Executive in 'packages'.

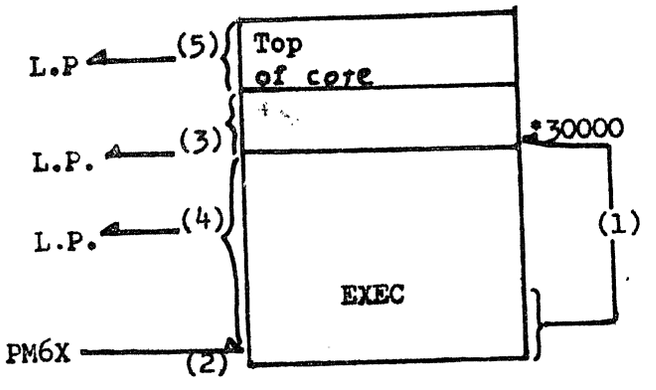
Note that lines in some packages may over-write lines in previous packages - or "TRED" on.

Iss 1.

E6BM Executive

General facts (cont)

1.5 Format of Post-mortem, and obtaining print.



(1) Routine at *377 moves 512 words up.
(2) Load PM6X by Freeze & Crest.
(3) 1st 2 pages of Exec printed.
(4) PM6X and bulk of Exec printed, also object program(s).
(5) Top of core area(s) printed.

2.0 A Broad Look at Executive

2 major entries:-

1) Voluntary (Extracode) at *40:- 'VOL'.

2) Involuntary at *20:- 'PERI'.

2.1 Voluntary entry. See Diagram 1.

General notes.

2.1.1 Before creating *40, hardware has stored
X F M N in absolute location 2
N(M) in " " 1.
In both cases, N(M) is relative.

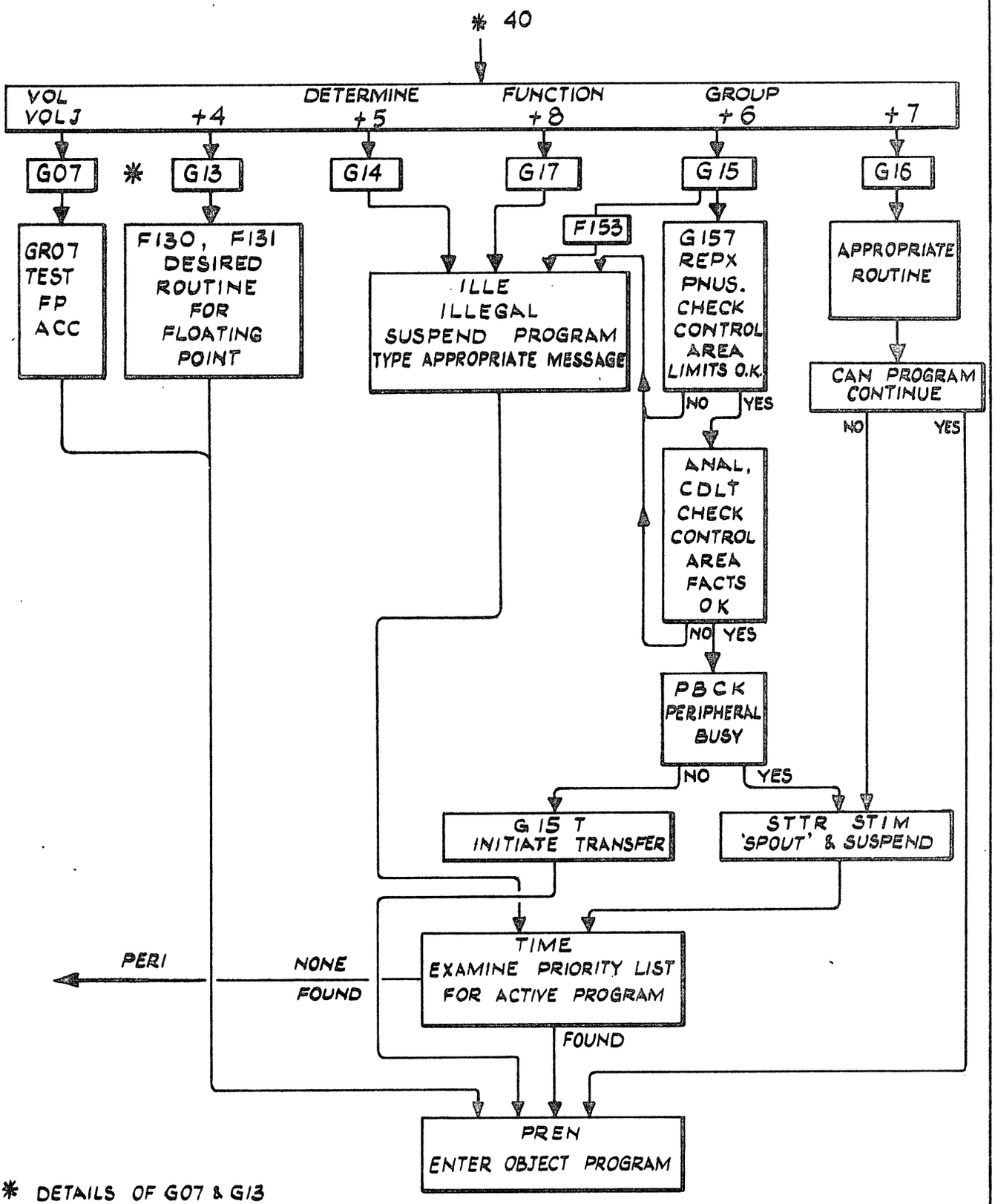
2.1.2 VOLJ is a table of branch orders, accessed by F023 (OBEY) using GROUP as a modifier.

2.1.3 TIME is the time-sharing routine, which searches through PLST, the priority list containing a 2-word entry for each member in priority sequence.
Note the 3 states a program may be in:-

Iss 1.

VOLUNTARY ENTRY TO E6BM (GREATLY SIMPLIFIED)

DIAG. 1



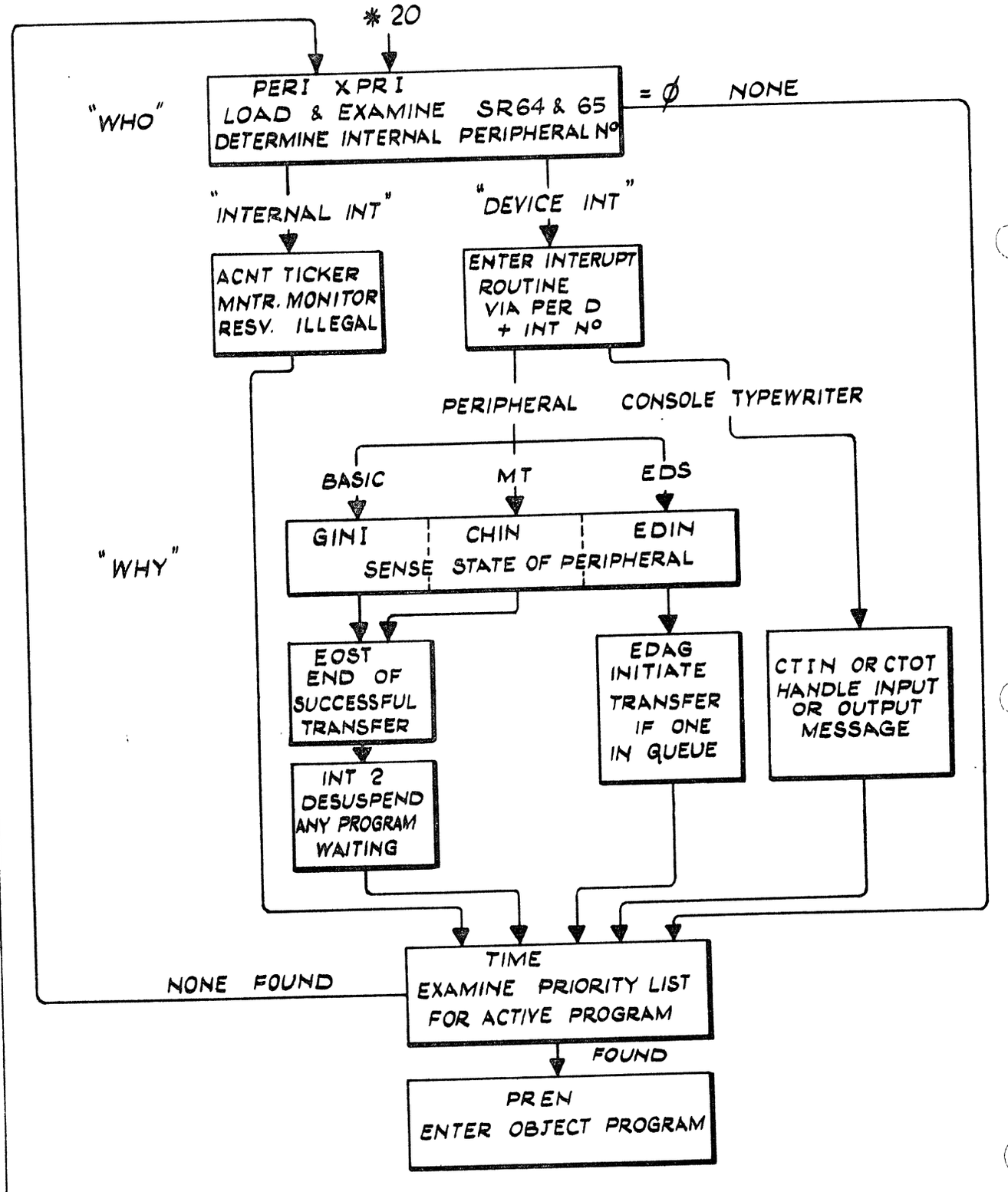
* DETAILS OF G07 & G13 VARY ACCORDING TO F.P. HARDWARE FITTED

 ETD 3552

Iss 1.

INVOLUNTARY ENTRY TO E6BM (GREATLY SIMPLIFIED)

DIAG. 2



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E6BM Executive

2.1 Voluntary entry (cont).

a) Suspended - the reason is indicated in PLST+1.
b) Active - PLST+1 = zero.
c) Running - has been entered via F172.

Only one program may be running at one time, but several may be suspended or active.

2.1.4 PREN is a routine of only 2 instructions, the second being F172.

2.2 Involuntary entry. See Diagram 2.

General notes:- 2.2.1 °20 is created by hardware.
For each entry to EXEC, all "INTERNAL INTERRUPTS" will be dealt with; if none of these exist only one peripheral interrupt will be serviced.

2.2.2 If no active program is found by TIME, Exec remains in loop, examining state of SR64 and 65. Most likely way out of this loop is TICKER interrupt, initiating "Spring-clean" action.

3.0 Tables.

3.1 Those concerning programs. (sample)

3.1.1 Useful single word entries

CUMP Current 'main' program number times 2.
CURP Char.2 as CUMP, Char 3 = member number.
PRGN Copy of CURP, used when changing member.

3.1.2 The 'Program Details' group (formerly PROD in E4BM) (see page 34 of "Gray's Elegy").

a) DLG Datum, Limit, G Register.

b) TOCA Top of Core Area Address

PMEM Number (times 16) of Last and highest member

c) PFOR Exec. Job No. (representing LOAD, DUMP, etc) with associated peripheral number.

PLWD Each 3 bits represent a SUB-JOB No; obtained from PLAN table, indexed according to job. "Cycled" as sub-jobs are performed.

3.1.2 (cont)

d) PSIX These vary according to EXEC job.
PSEV Usually details about a transfer (e.g. address and count for DUMP).

e) NAME Four characters of name.
TRUS Used only for Double Slot Trusteds.

f) MLST 2 words. Memory list for members. (F163's and Flag events)

g) MOMT 2 words Mode memory for members

3.1.3 PLST:- the Priority list

Has a 2-word entry for each member. If member is active, 2nd word is zero (see 2.1.3)
Note current terminology:-

Old	Current
Main program	Member 0
Sub-program 1	" 1
" " 2	" 2

etc.

Simplification of member system.
Members of a program have same datum, limit, peripherals. Each 'appears' to have its own accumulators, and may have different priority. The member system overcomes the disadvantage of having only 8 accumulators when using many sub-routines.
Member 7 of a program is a Pseudo member created for Exec action concerning program.

3.2 Tables concerning peripherals.

These are in two groups,

a) indexed by internal Type number.

b) " " " device number.

Conversion tables are needed to convert external to internal numbers.

E6BM Executive

3.2 (cont)

a) TTBL - External Type to Internal Type.
Result is "compacted" number sequence, starting at 1 (therefore Ø means 'no peripheral on site'.)

b) PTBL - External device (socket) to Internal number
Includes Typewriter, Mag Tape Channels and EDS Controls.

c) OTBL - External device (Operaters No). Includes decks and transports.

3.2.1 Tables indexed by Type.

a) PERC Count of peripherals of this type

b) PERS Internal device number of first
These two will be used to control the search through device tables.

c) ANAL Branch table to appropriate analysis routine.

3.2.2 Tables indexed by device number.

a) PERD Interrupt Routine Address.

b) PRDA Allocation of peripheral (Program & unit number)

Note Peripherals may be allocated to program in 3 ways.

i) Request block) static allocation
ii) GIVE message)
iii) F156 in conjunction with F151) dynamic allocation.
or Open and Close Mode F157)

c) PRDW External number, qualifier and general transfer information.

d) PRDX "Busy" word. Zero if peripheral not busy.

e) PRDY Program using, or waiting for, device.

f) PRDZ Operators number, and properties.

g) CWSA For typewriter, controls cyclic message buffer
For other devices, address of current transfer.

h) CWSC Count of current transfer.

i) CCS Control Code, qualifiers, modes.