Waveform names

The following conventions have been used for 1904E waveforms, there are of course many exceptions.

[Ø] [Name]	Signals on Standard I/F Cable.
[X, Y or Z] [Ø]	Fixed Store data for addresses.
[FS] [BA, XA, or YA] [Ø]	Fixed Store address waveforms.
[FS] [Ø]	Fixed Store Data waveforms.
[R] [λ] [Ø]	Register Waveforms (i.e. Staticised data).
[H] [λ] [Ø]	Highways (i.e. data with more than one source).
[T] [Ø] [λ(s)] [Ø]	Clock Pulse, generation, purpose, version.
SAD, SIN, SOUT	Store highways (traditional)
[W] [λ(s)] [Ø]	Condition waveforms from Dataflow to microprogram.
[C] [λ(s)] [Ø]	Partially decoded control signals to dataflow.
[D] [λ(s)] [Ø]	Decoded Control signals to Dataflow.
[E] [λ(s)] [Ø]	Dataflow control signals.
[PH] [λ(s)] [Ø]	Signals in hesitation peripheral controls.
[PA] [λ(s)] [Ø]	Signal in autonomous " "
[F] [λ(s)] [Ø]	Floating point wavdforms.

where :-

1) λ(s)	denotes a letter or letters.
2) Ø	" " numeric quantity.
3) [----]	" " mandatory quantity.
@) Name	" the symbol by which a Standard Interface signal is known.

ENA 0-14 L

ENABLE NOT A BIT 0-14 TO L

T3 Q12-21 N

CLOCK 3rd GENERATION STROBE Q BITS 12-21 INTO N

I.C.T. 1904E Central Control (WGC.01)

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I N D E X

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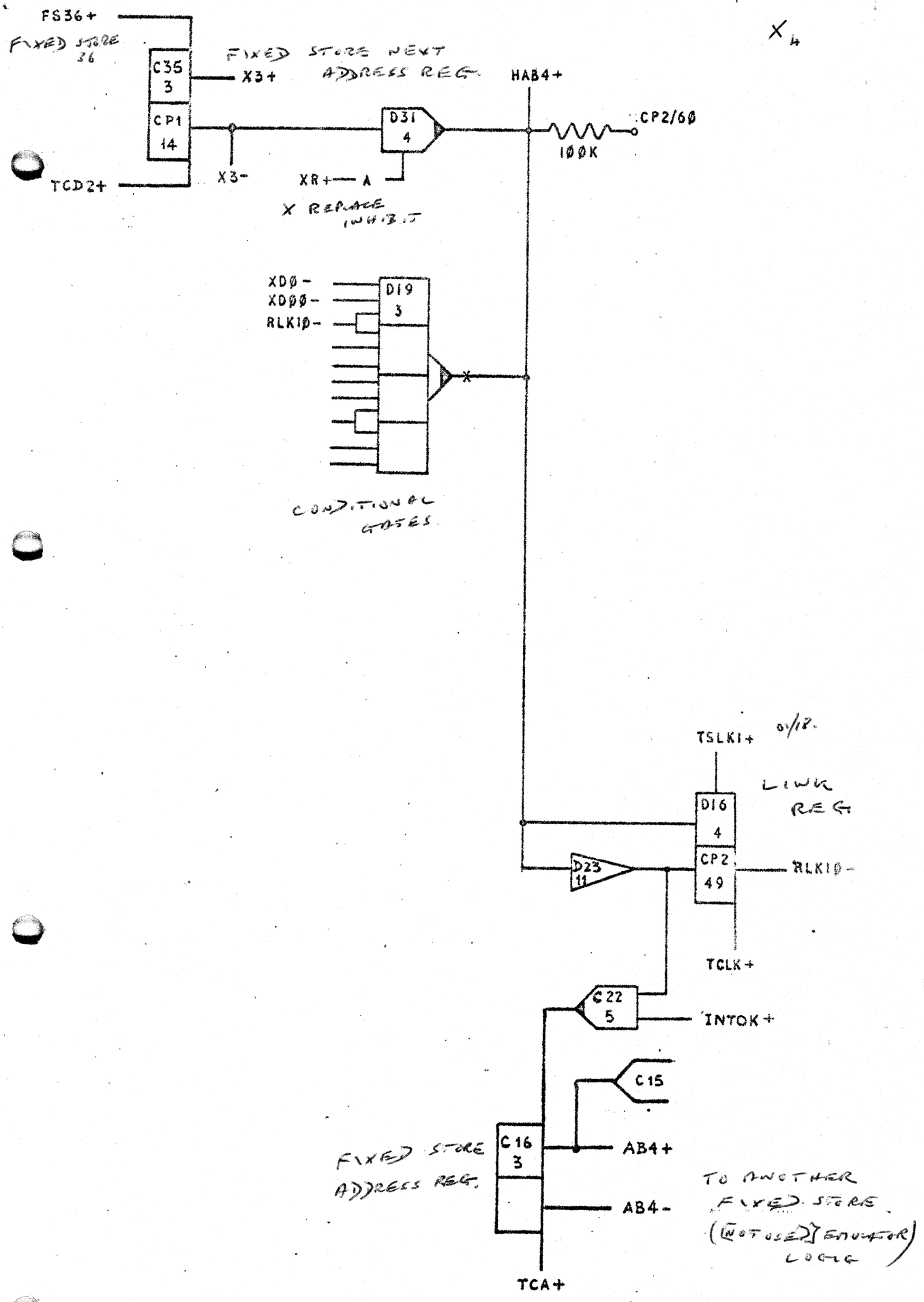
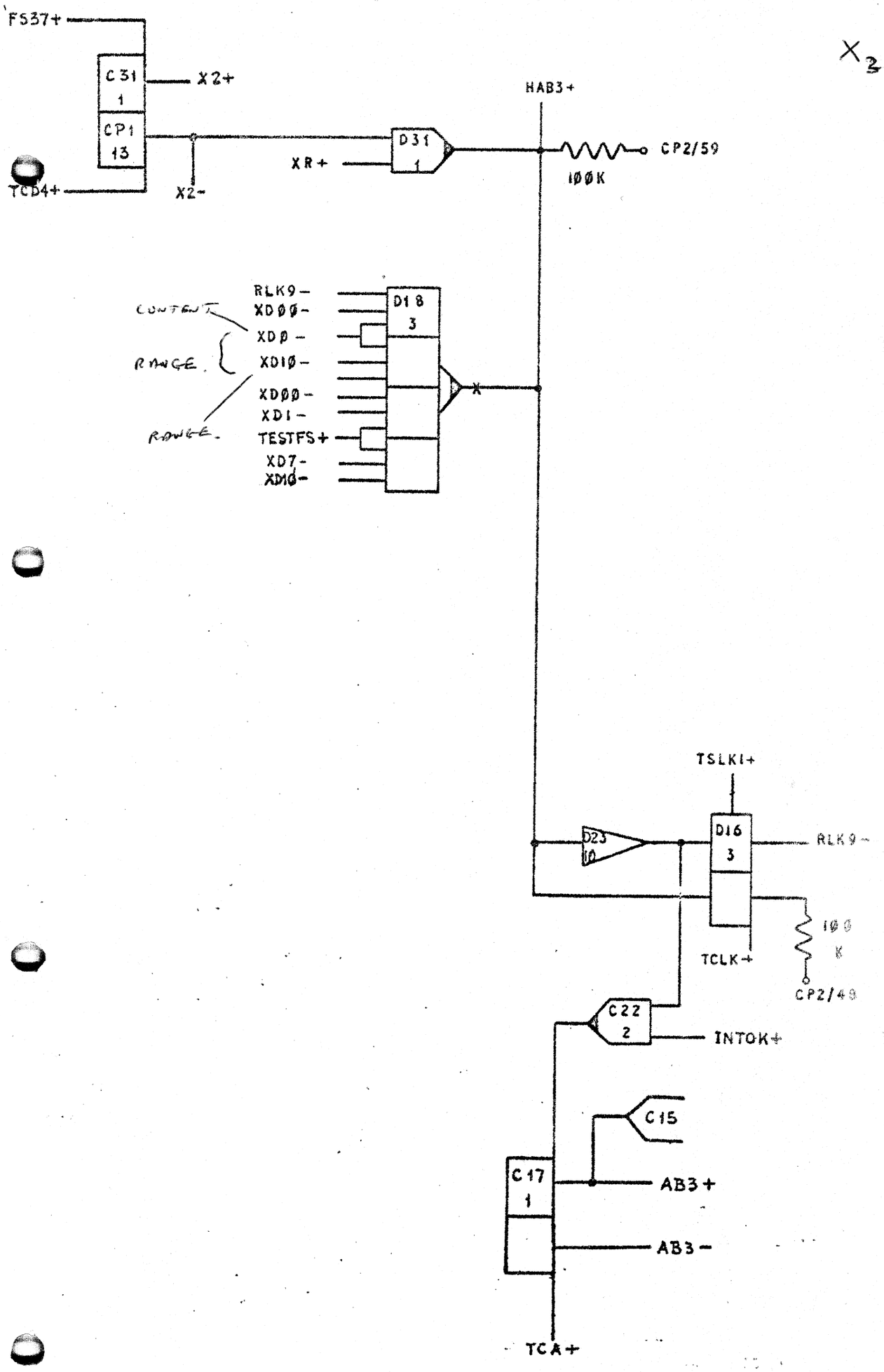
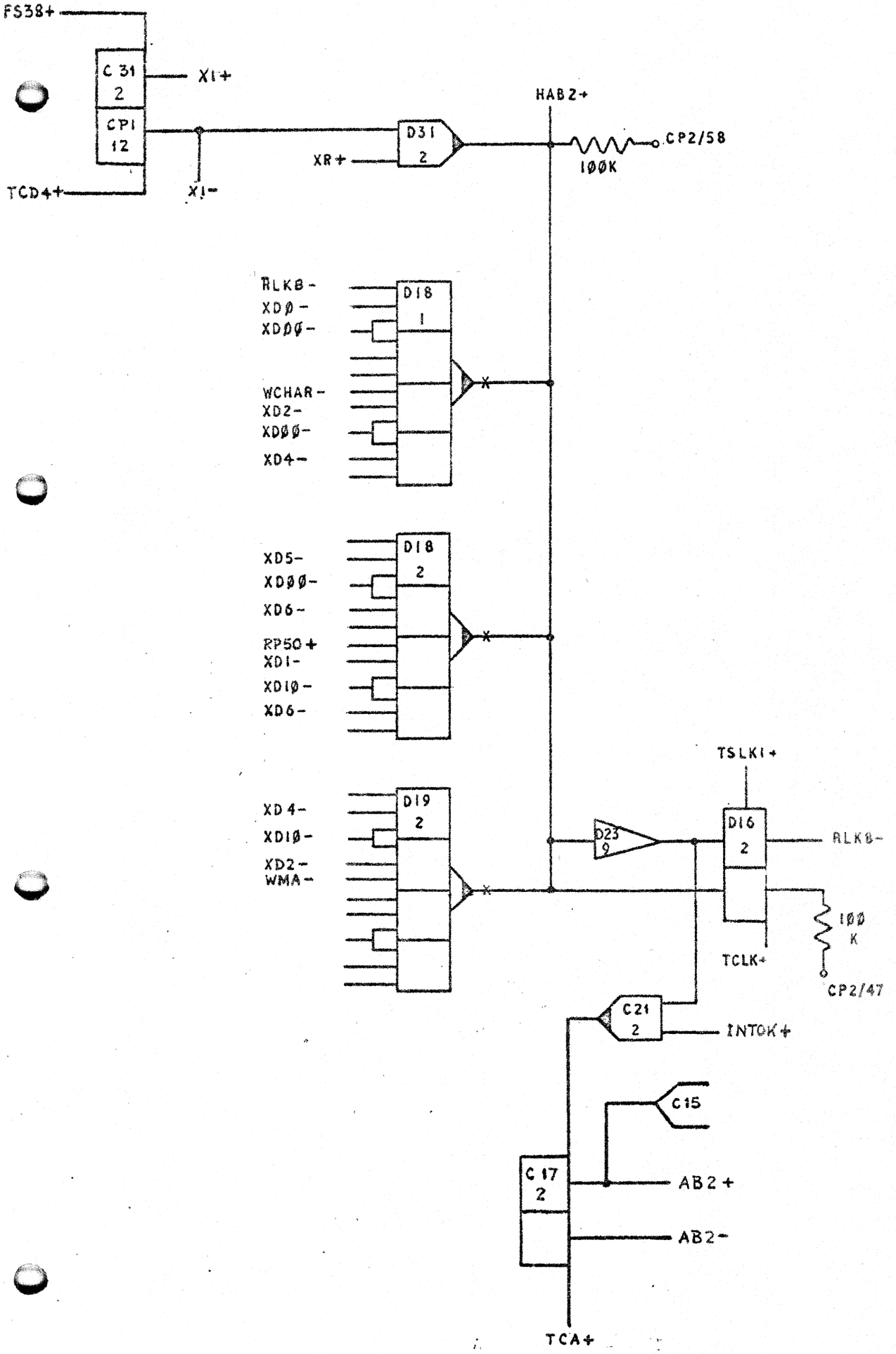

FS36+
FIXED STORE 36
C35 3
CP1 14
TCD2+
X3+
X3-
FIXED STORE NEXT ADDRESS REG.
D31 4
XR+ — A
X REPLACE INHIB.T
HAB4+
CP2/60
100K
XD0-
XD00-
RLK10-
D19 3
CONDITIONAL GATES
TSLK1+
0/18.
LINK REG
D16 4
D23 11
CP2 49
RLK10-
TCLK+
C22 5
INTOK+
C15
C16 3
AB4+
AB4-
FIXED STORE ADDRESS REG.
TO ANOTHER FIXED STORE (NOT USED) EMULATOR LOGIC
TCA+

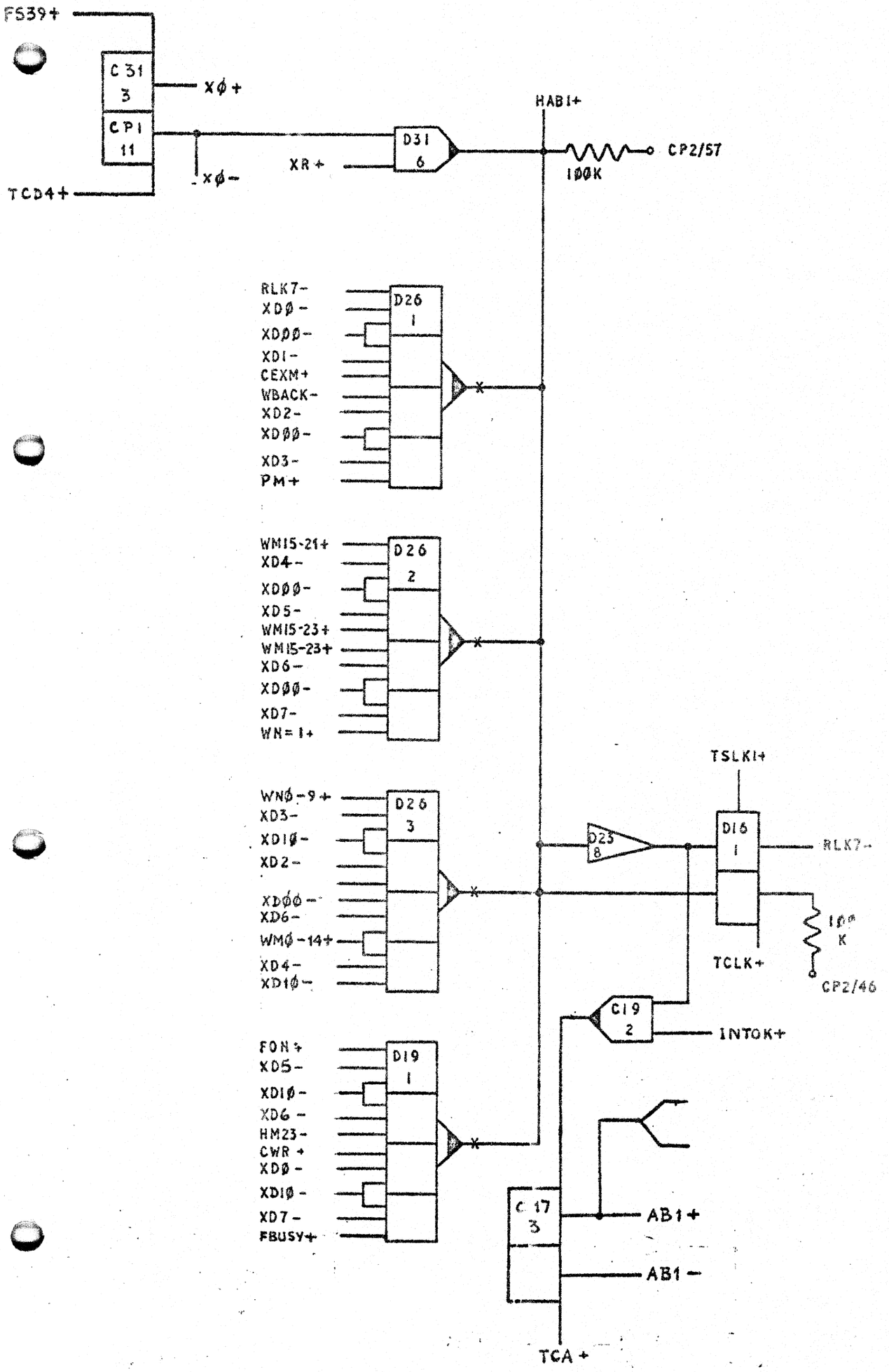

FS37+
C31
1
CP1
13
X2+
X2-
TCD4+
XR+
D31
1
HAB3+
CP2/59
100K
RLK9-
XD00-
XD0-
XD10-
XD00-
XD1-
TESTFS+
XD7-
XD10-
D18
3
CONTENT
RANGE
RANGE
X
TSLKI+
D23
10
D16
3
RLK9-
100
K
TCLK+
CP2/49
C22
2
INTOK+
C15
C17
1
AB3+
AB3-
TCA+

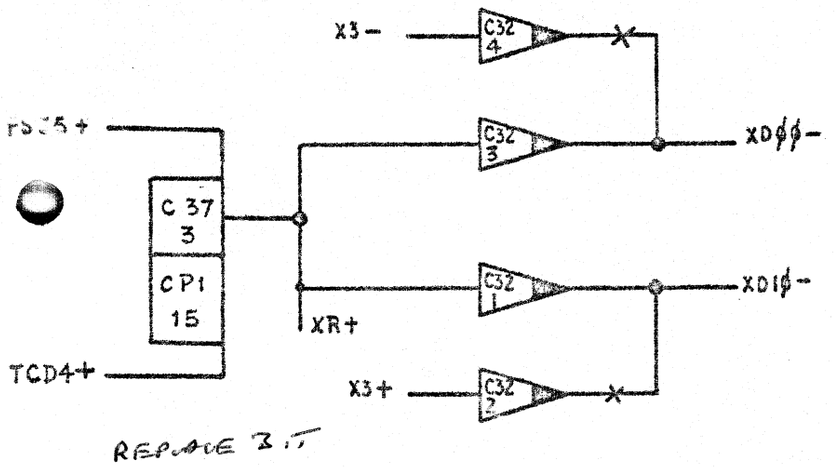


XI ADDRESS SLICE

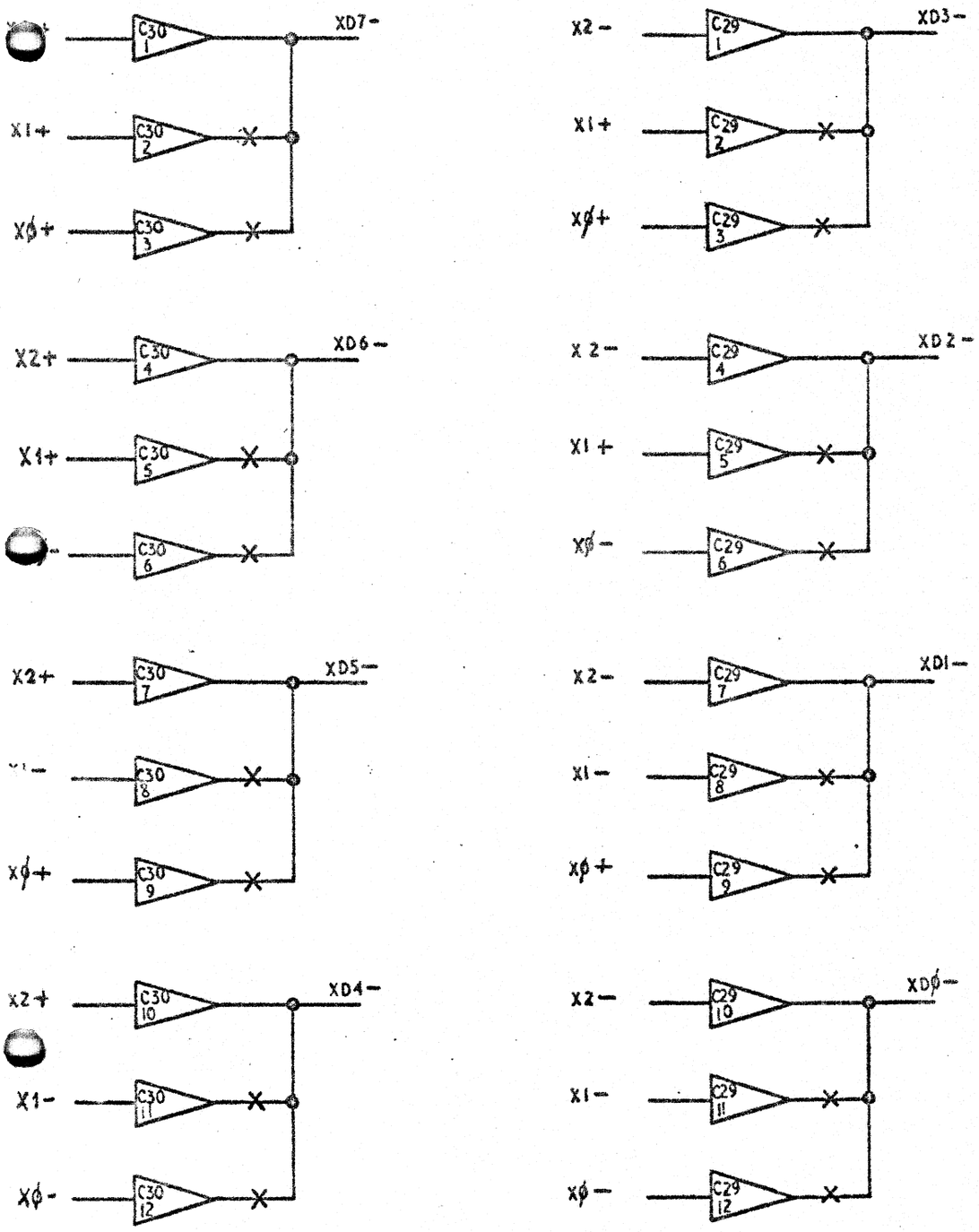
WGC01/3

SUB	155
ACW	0836


FS39+
C31
3
CP1
11
TCD4+
XØ+
XØ-
XR+
D31
6
HAB1+
100K
CP2/57
RLK7-
XDØ-
XDØØ-
XDI-
CEXM+
WBACK-
XD2-
XDØØ-
XD3-
PM+
D26
1
WM15-21+
XD4-
XDØØ-
XD5-
WM15-23+
WM15-23+
XD6-
XDØØ-
XD7-
WN=1+
D26
2
WNØ-9+
XD3-
XDIØ-
XD2-
XDØØ-
XD6-
WMØ-14+
XD4-
XD1Ø-
D26
3
FON+
XD5-
XDIØ-
XD6-
HM23-
CWR+
XDØ-
XDIØ-
XD7-
FBUSY+
D19
1
D23
8
TSLKI+
DI6
1
RLK7-
TCLK+
10Ø
K
CP2/46
C19
2
INTOK+
C17
3
AB1+
AB1-
TCA+

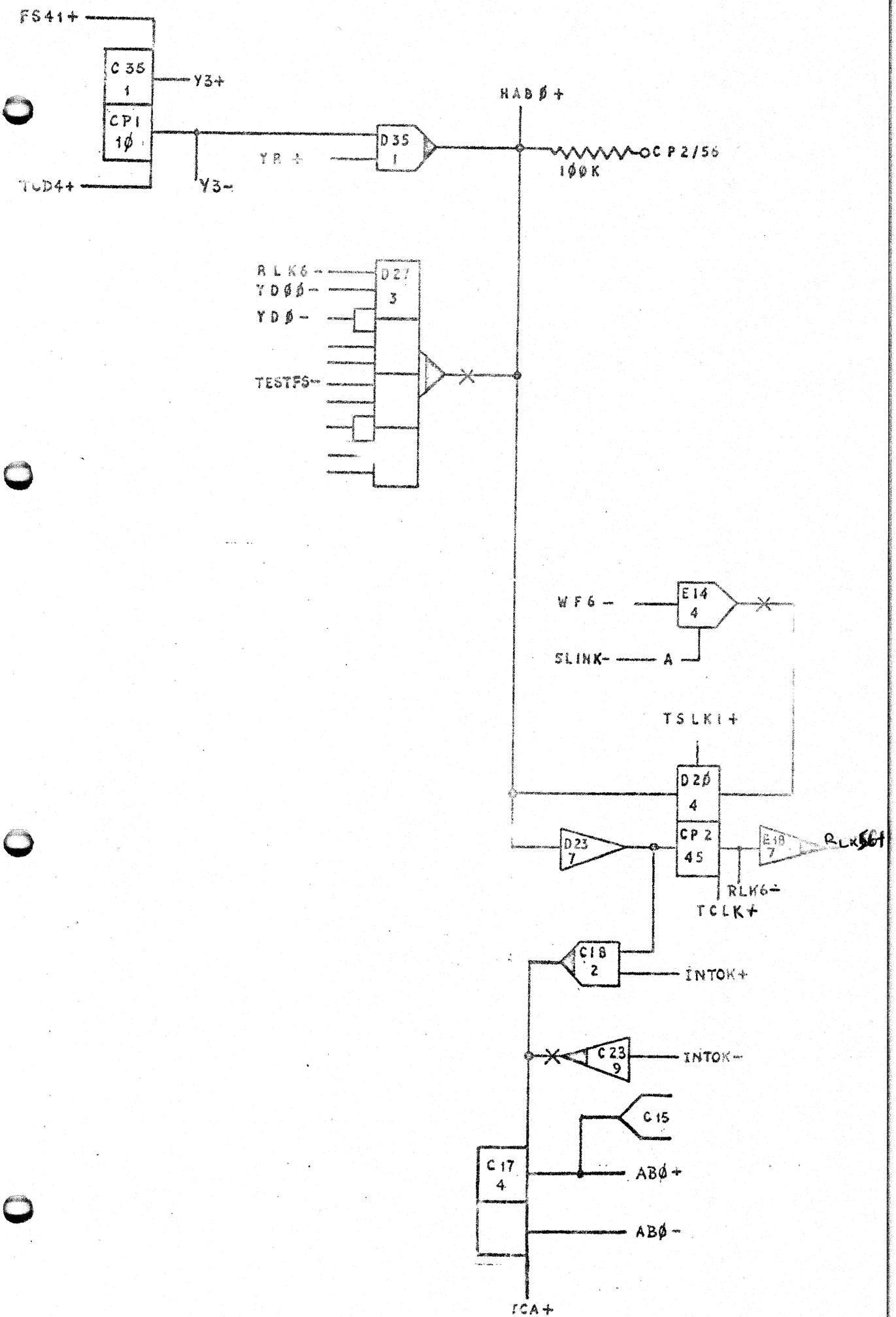


REPLACE 3.7



X CONDITION DECODE WGC01/5

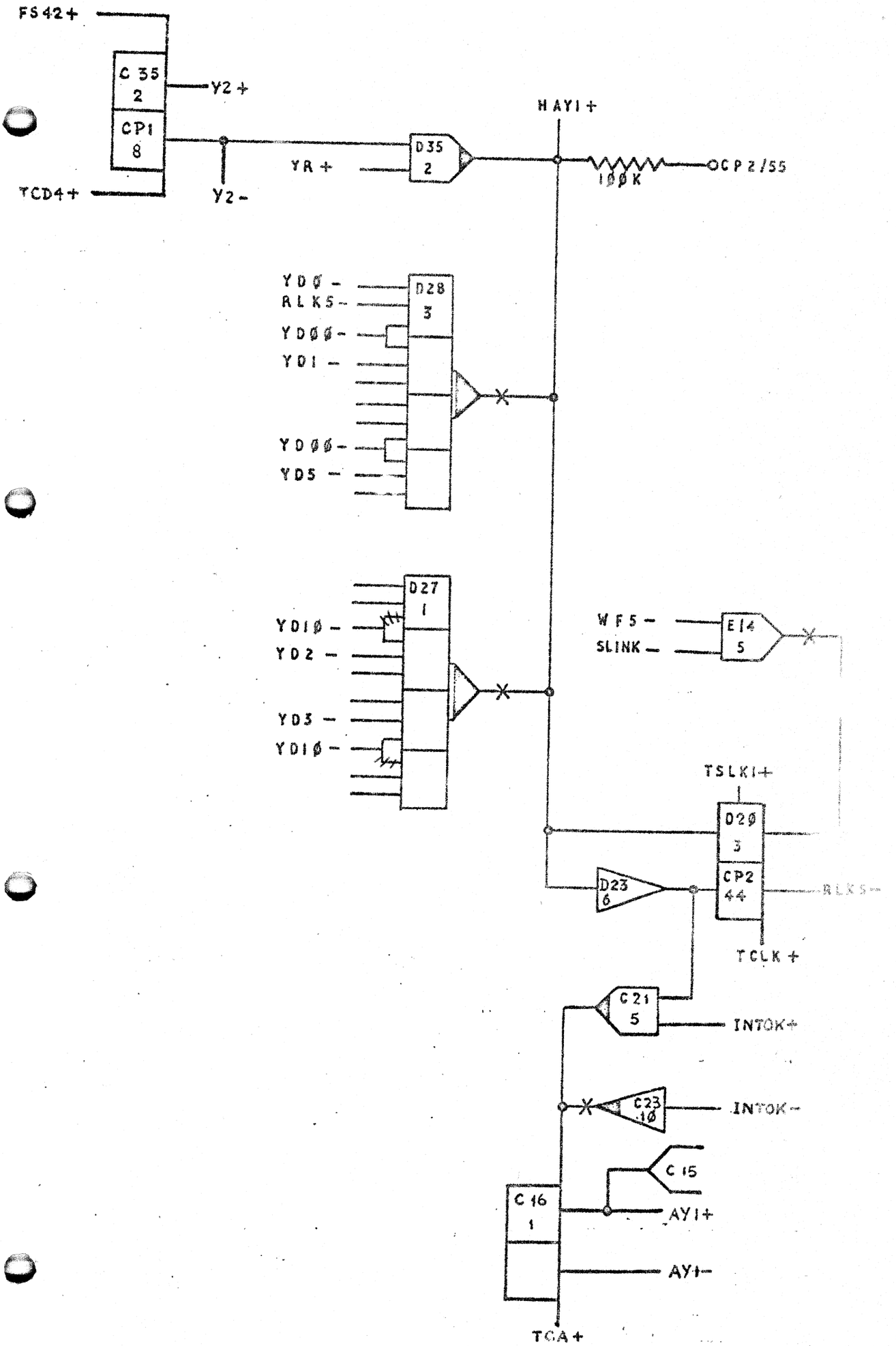
SUB	ISS															
MCW	0934															



ADDRESS SLICE.

W.G.C.01/6.

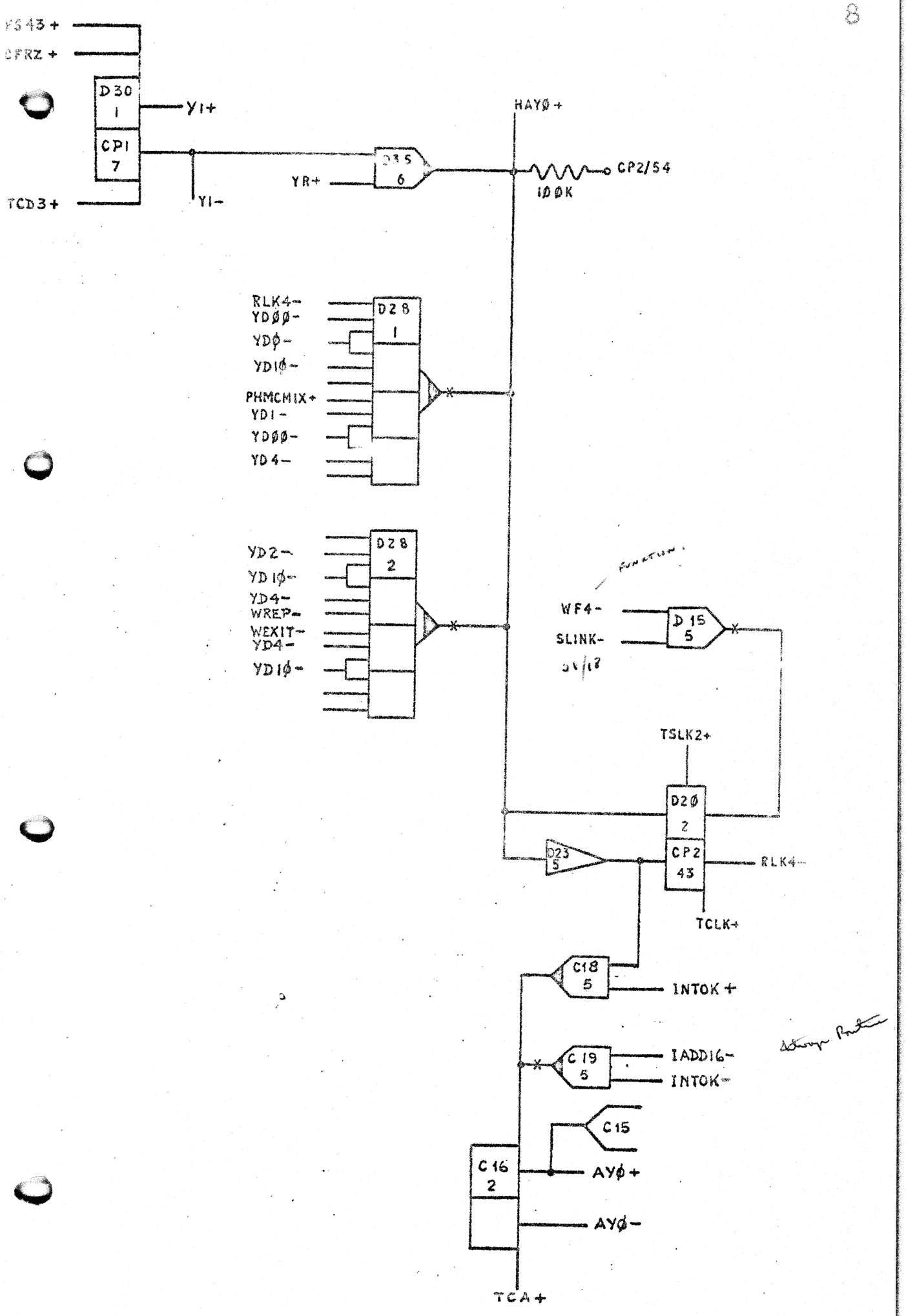
SUB. ISS



Y2 ADDRESS SLICE.

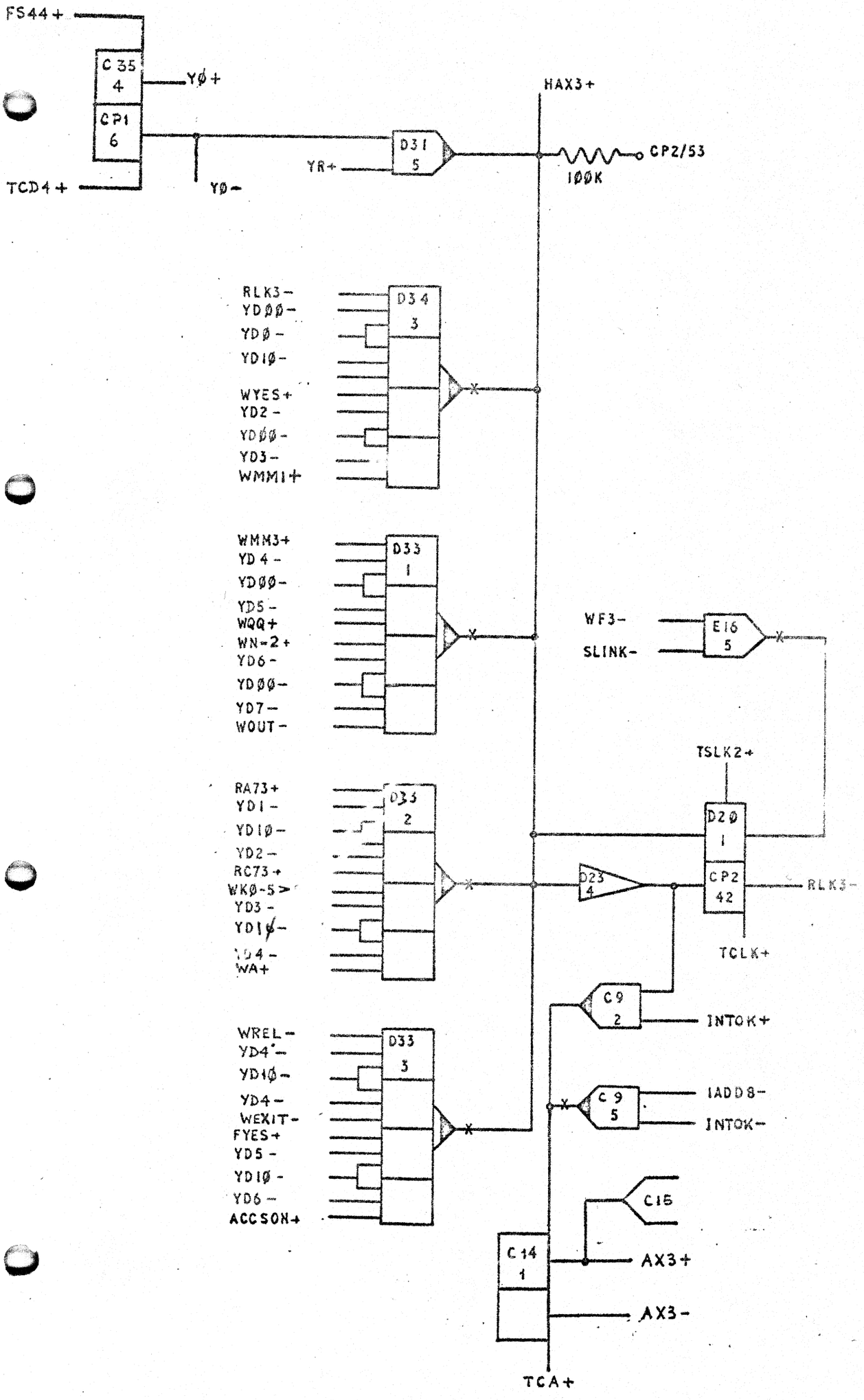
W.G.C

SUB.	ISS														
A.C.W.	0836														



ADDRESS SLICE

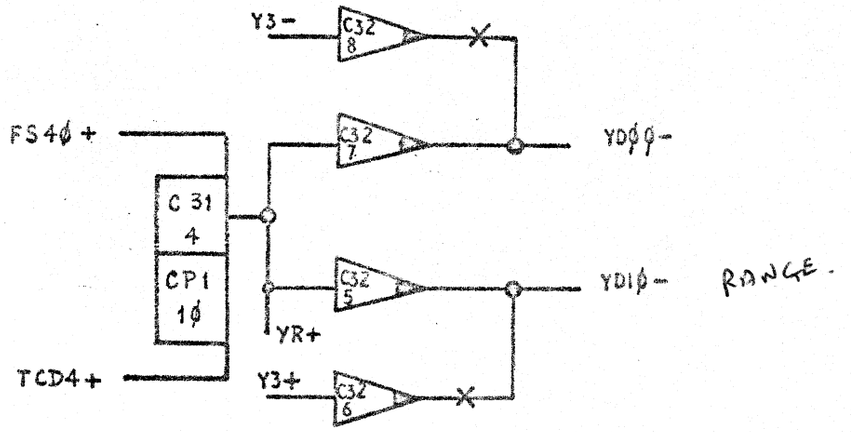
ISS

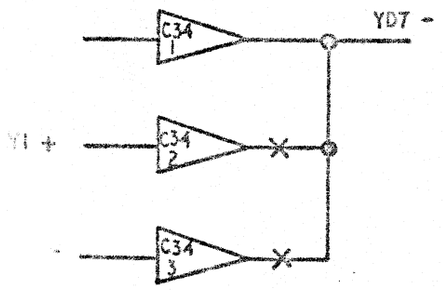


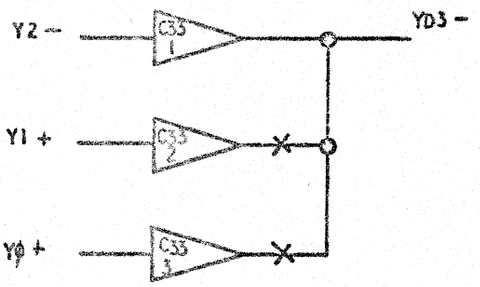
Ø ADDRESS SLICE

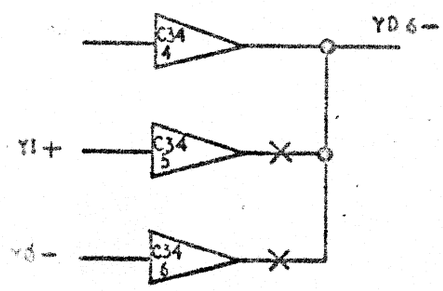
WGC01/9

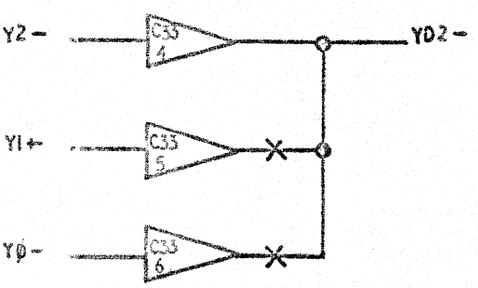
UB	ISS

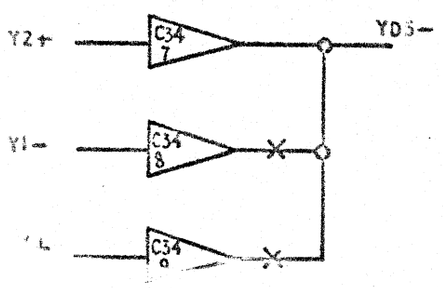


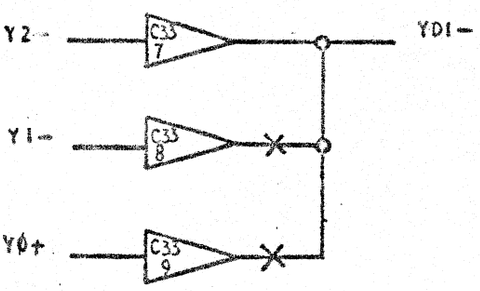


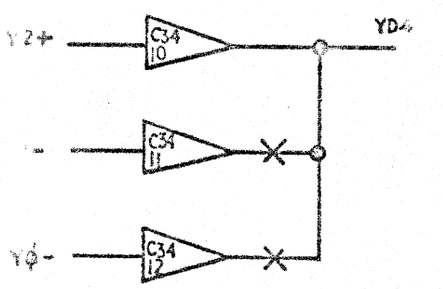


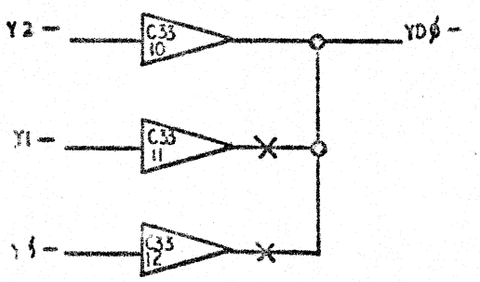








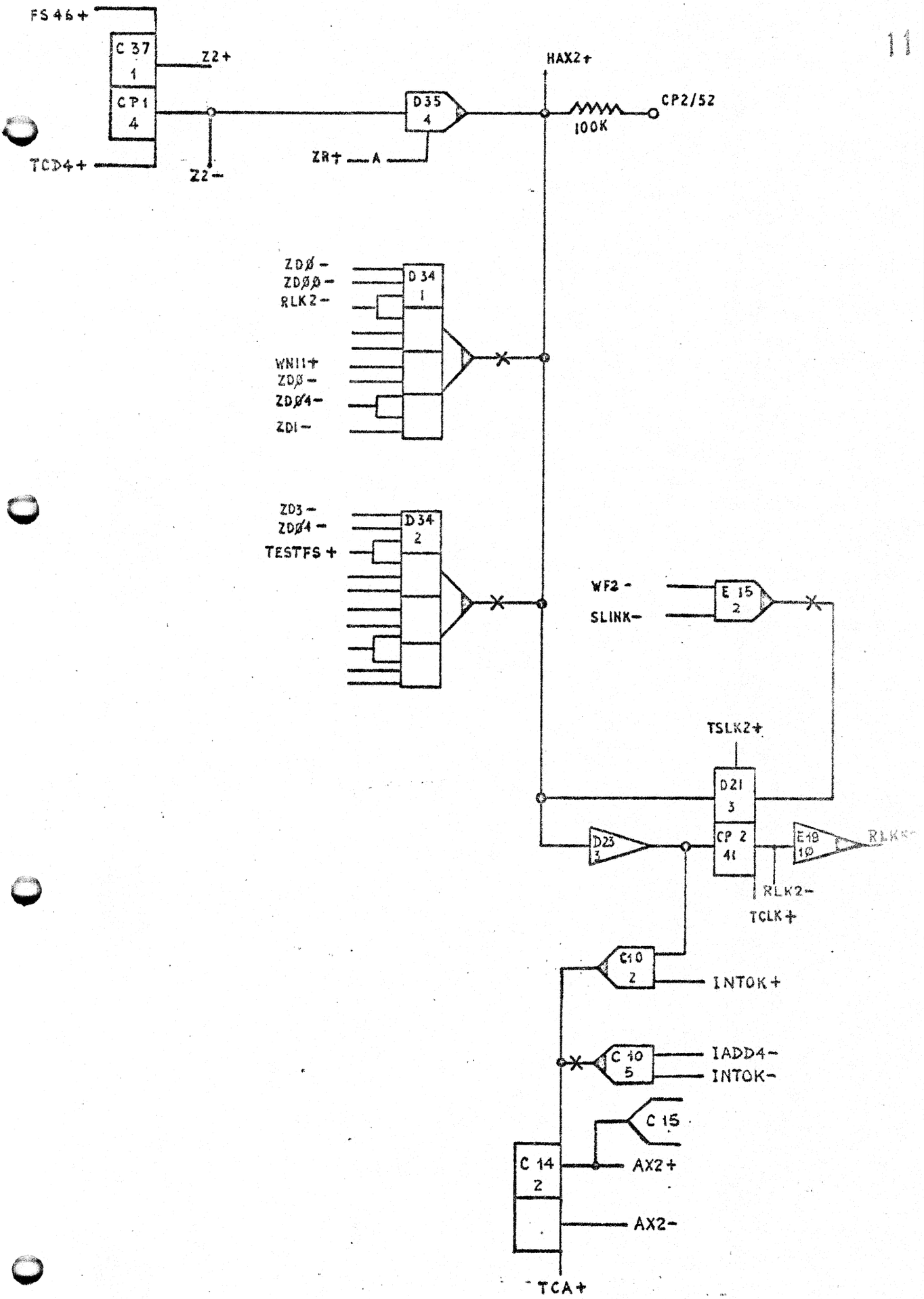


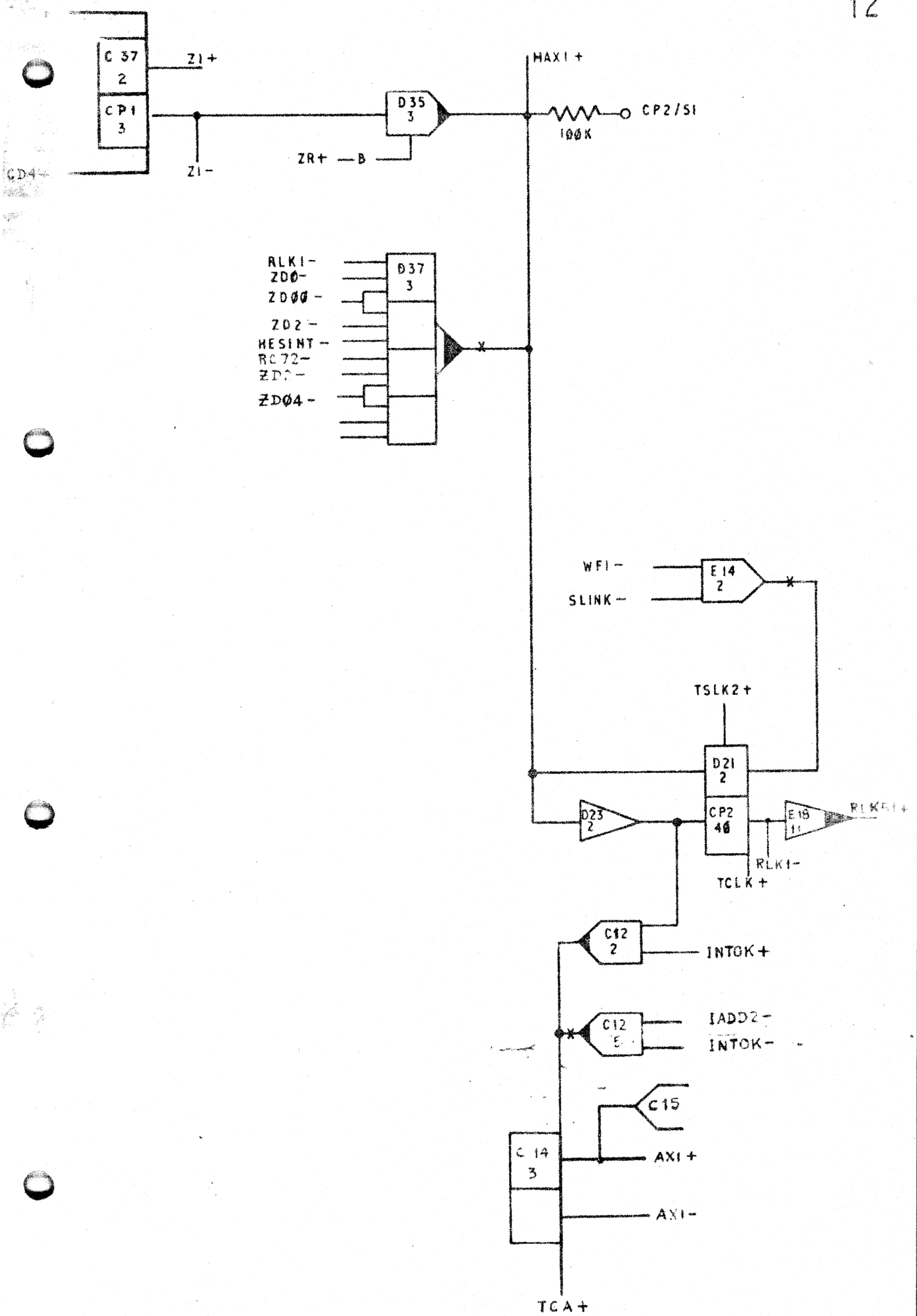


Y CONDITION DECODE

WC01 / 10

ISS


FS46+
C37 1
CP1 4
Z2+
Z2-
TCD4+
D35 4
ZR+
A
HAX2+
100K
CP2/52
ZDØ-
ZDØØ-
RLK2-
D34 1
WN11+
ZDØ-
ZDØ4-
ZD1-
ZD3-
ZDØ4-
TESTFS+
D34 2
WF2-
SLINK-
E15 2
TSLK2+
D21 3
D23 3
CP2 41
E18 19
RLK2-
TCLK+
C10 2
INTOK+
C10 5
IADD4-
INTOK-
C15
C14 2
AX2+
AX2-
TCA+



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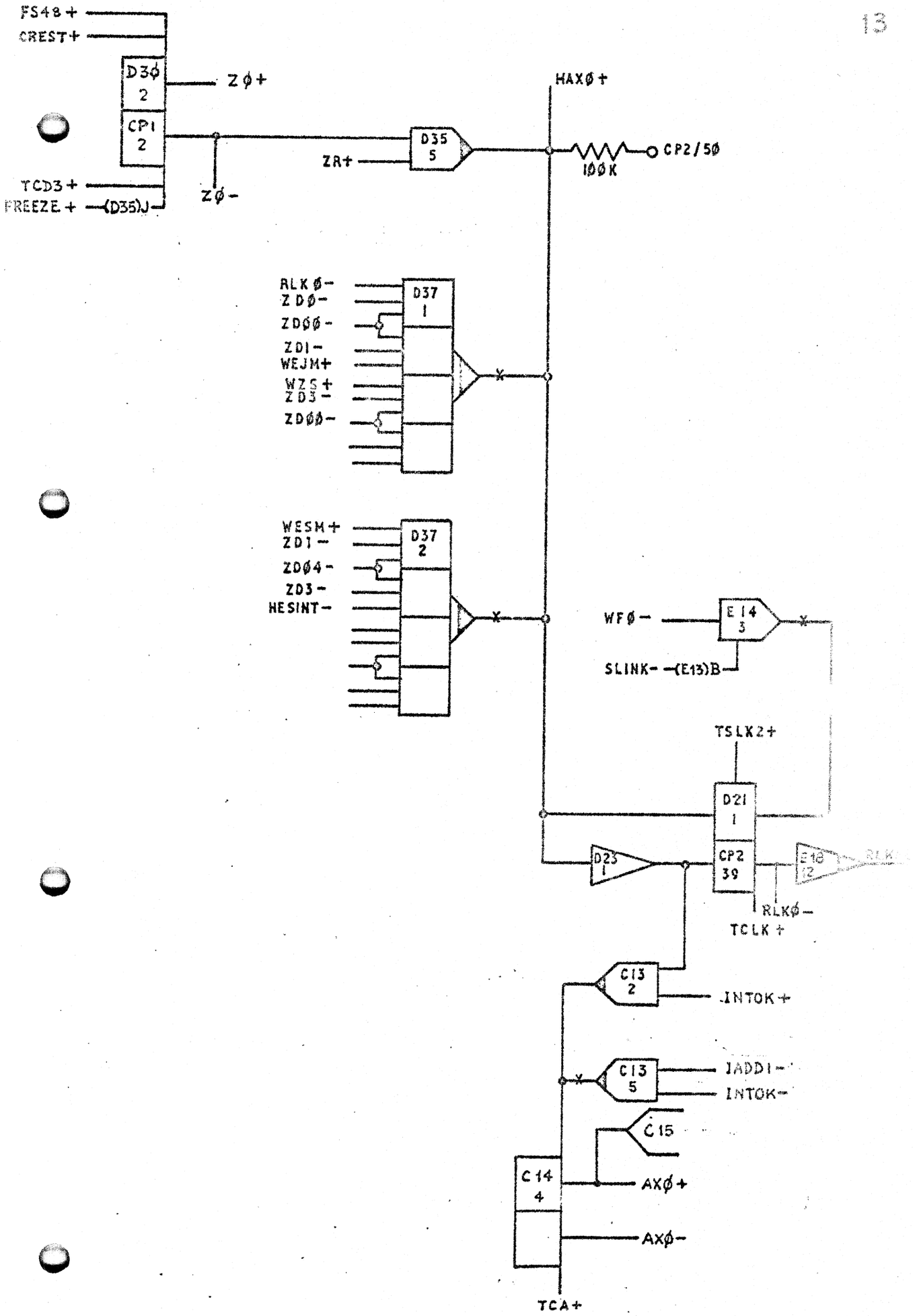
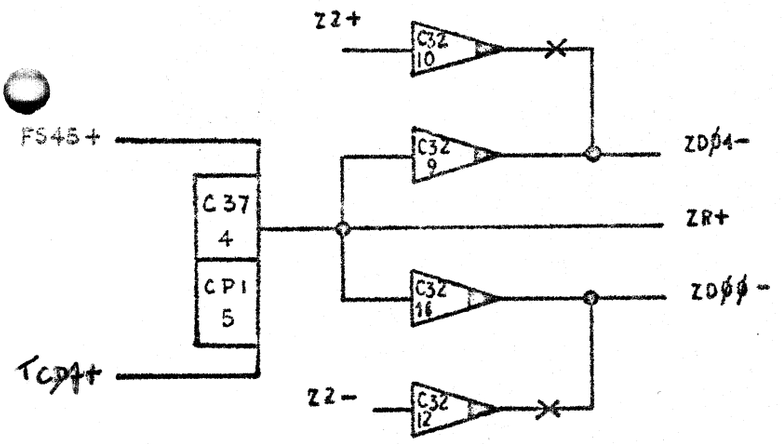
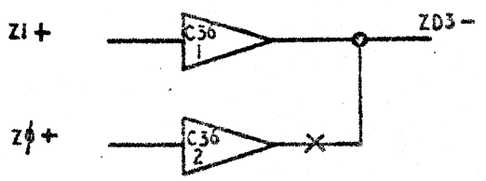


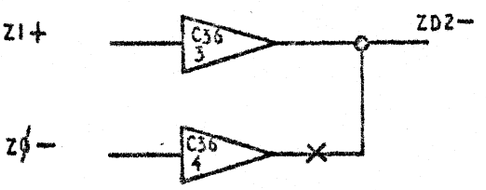
ADDRESS SLICE.

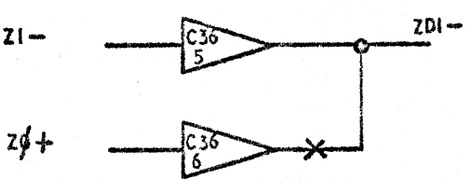
WGCØ1/13

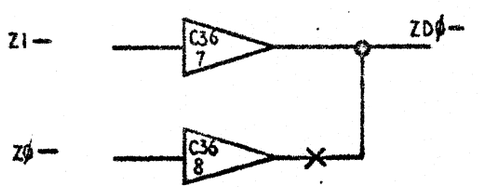
18.	ISS	1													


Z2+
C32 10
FS45+
C32 9
ZDØ4-
C37 4
ZR+
CP1 5
C32 16
ZDØØ-
TCP4+
Z2-
C32 12

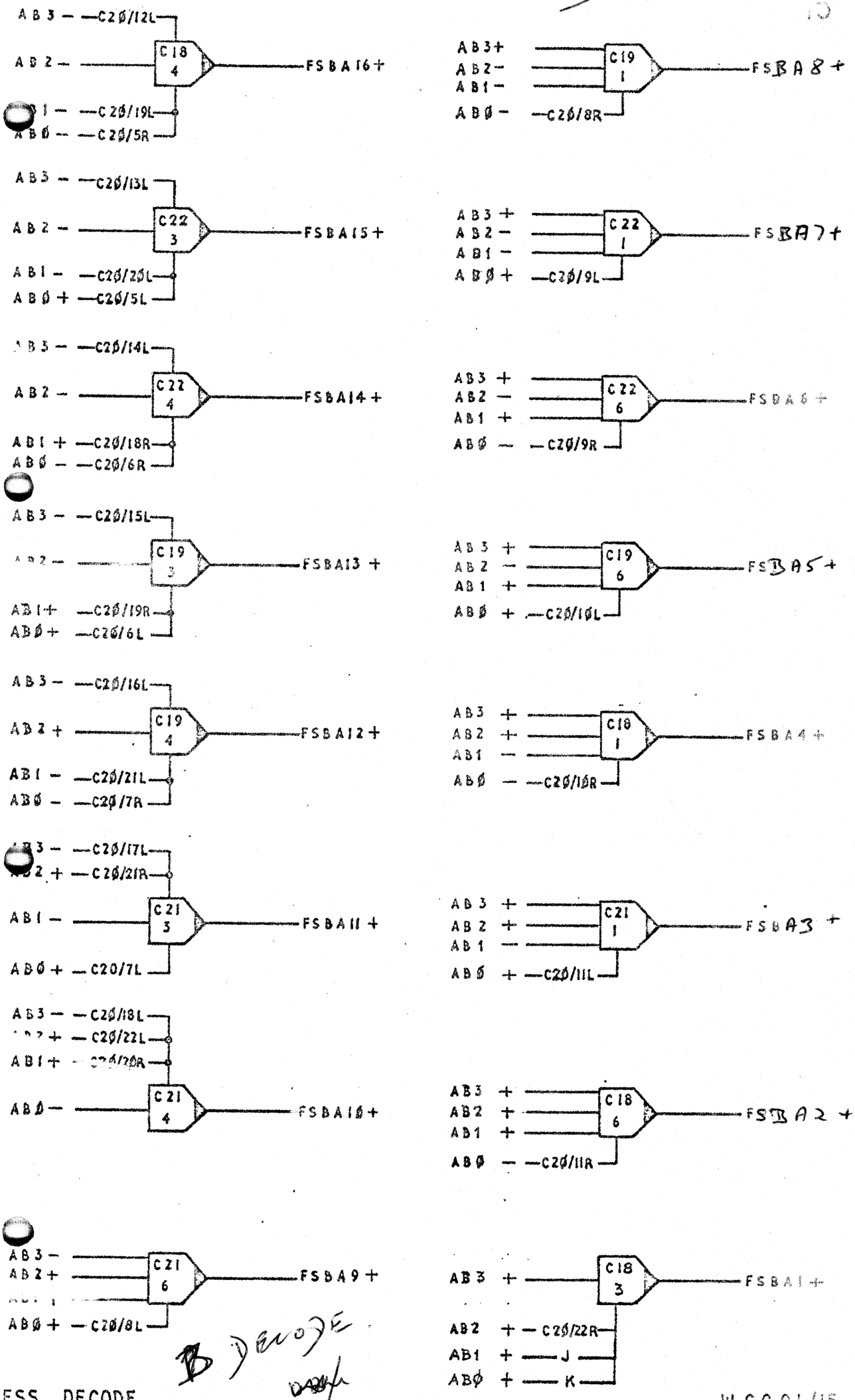

Z1+
C36 1
ZD3-
ZØ+
C36 2


Z1+
C36 3
ZD2-
ZØ-
C36 4


Z1-
C36 5
ZD1-
ZØ+
C36 6


Z1-
C36 7
ZDØ-
ZØ-
C36 8

FIXED STORE.
B ADDRESS DECODE.

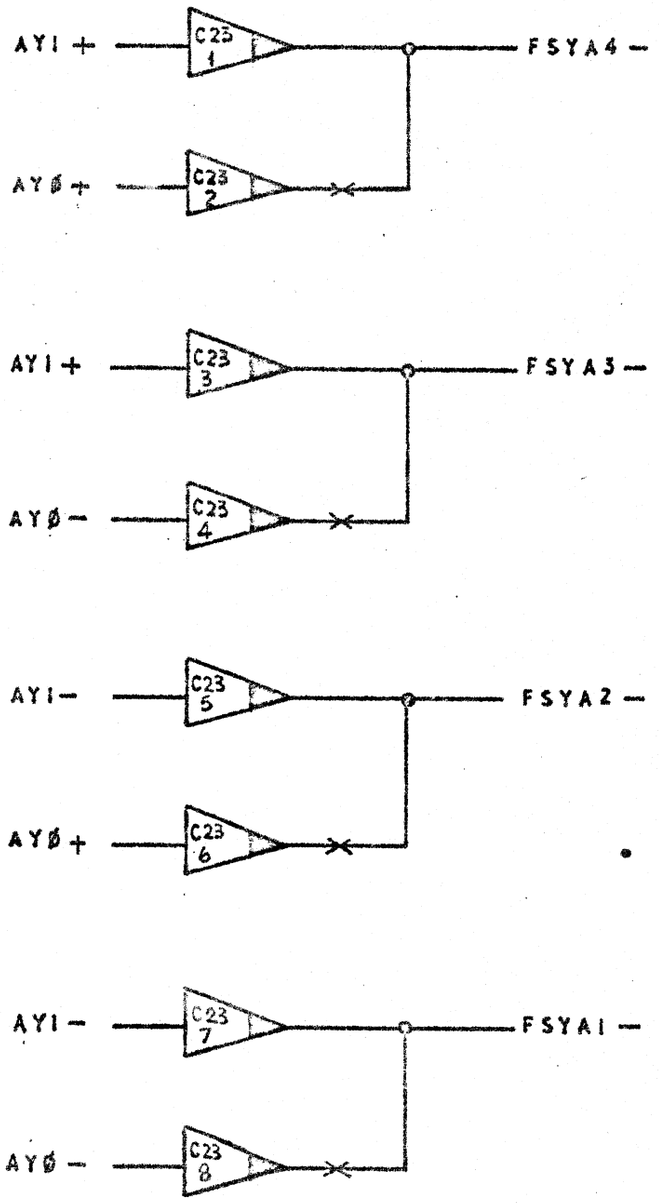


B DECODE

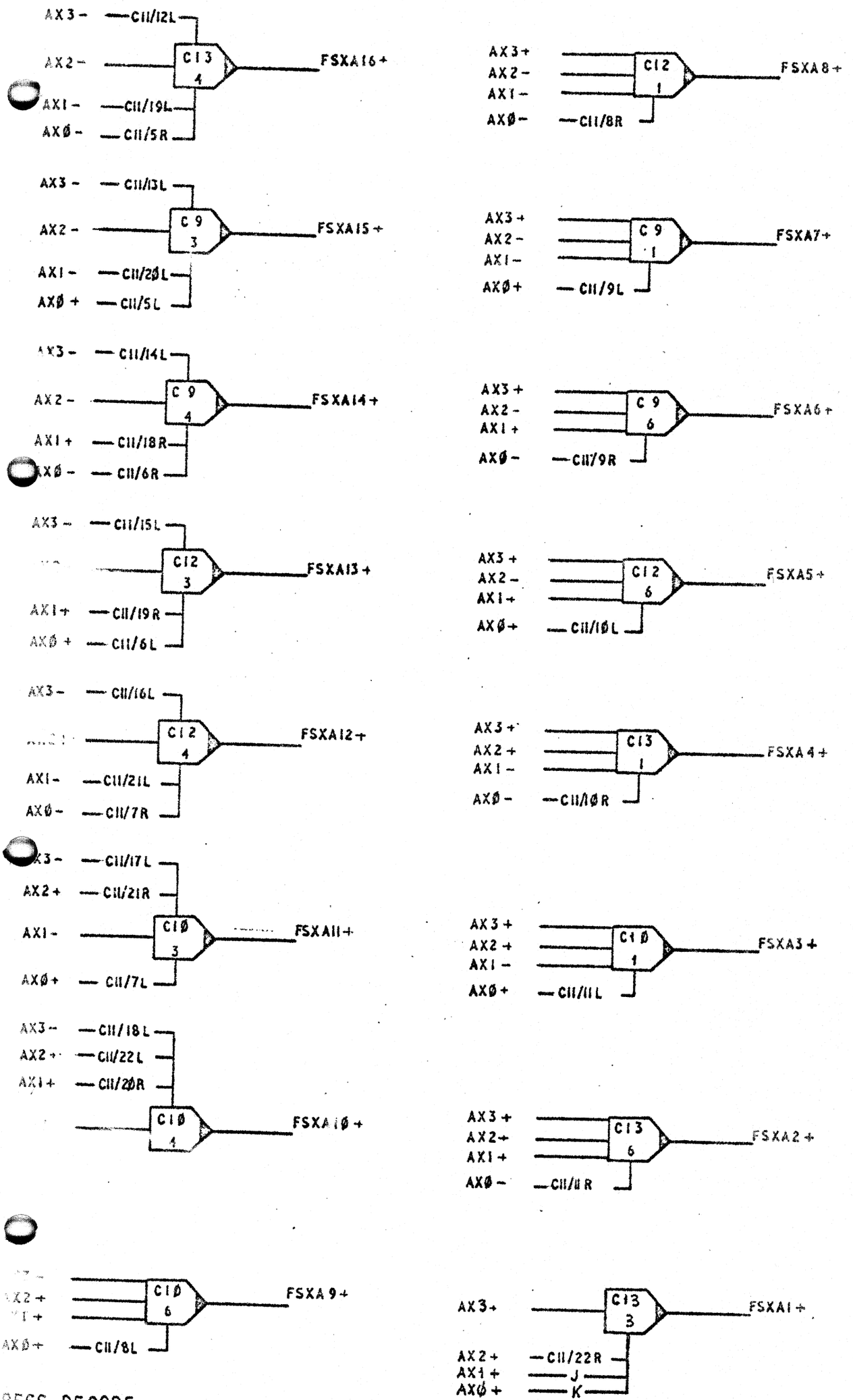
ADDRESS DECODE

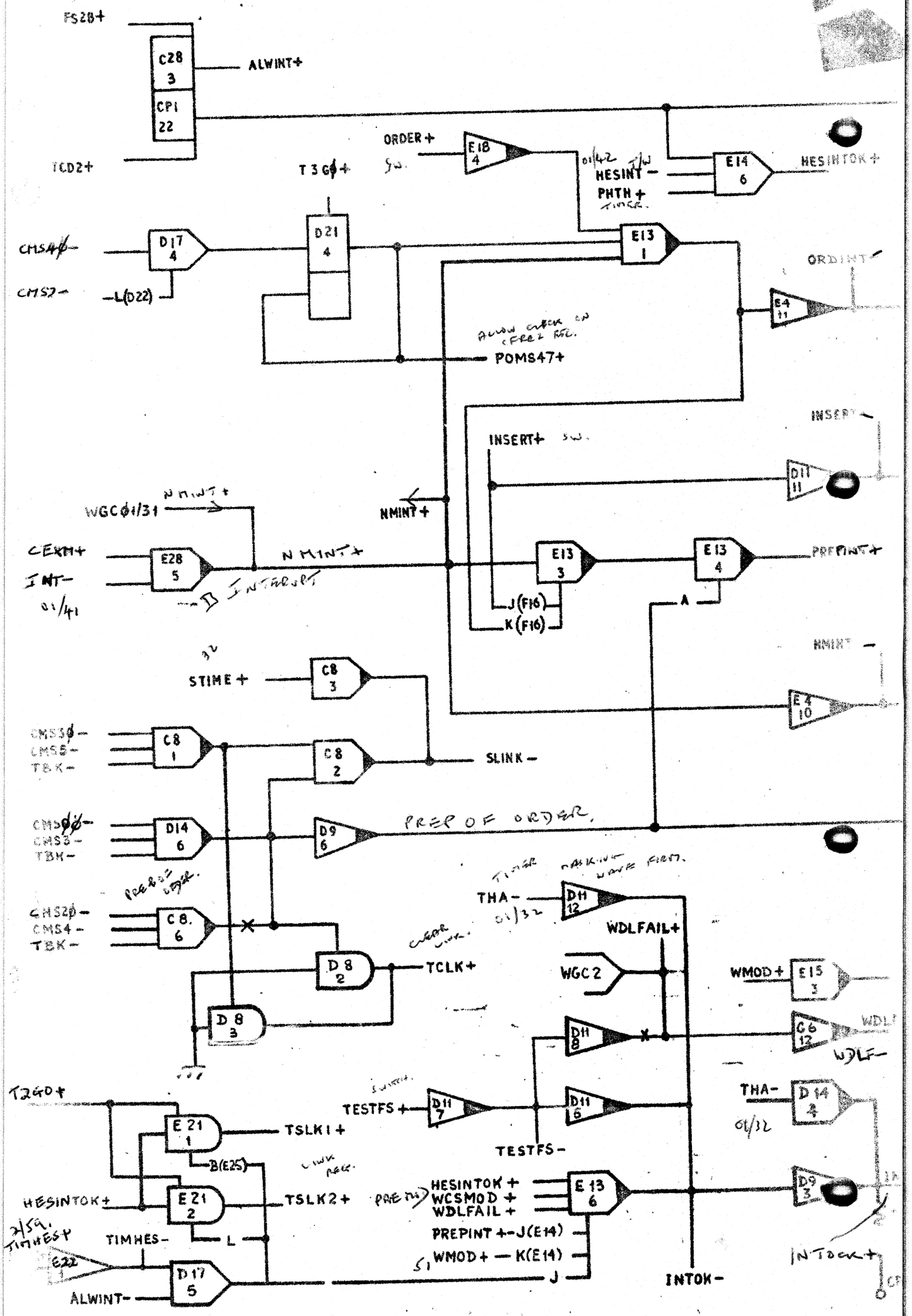
W.G.C.01/15.

ISS															


AY1 +
C25 1
FSYA4 —
AYØ +
C23 2
AY1 +
C23 3
FSYA3 —
AYØ —
C23 4
AY1 —
C23 5
FSYA2 —
AYØ +
C23 6
AY1 —
C23 7
FSYA1 —
AYØ —
C23 8

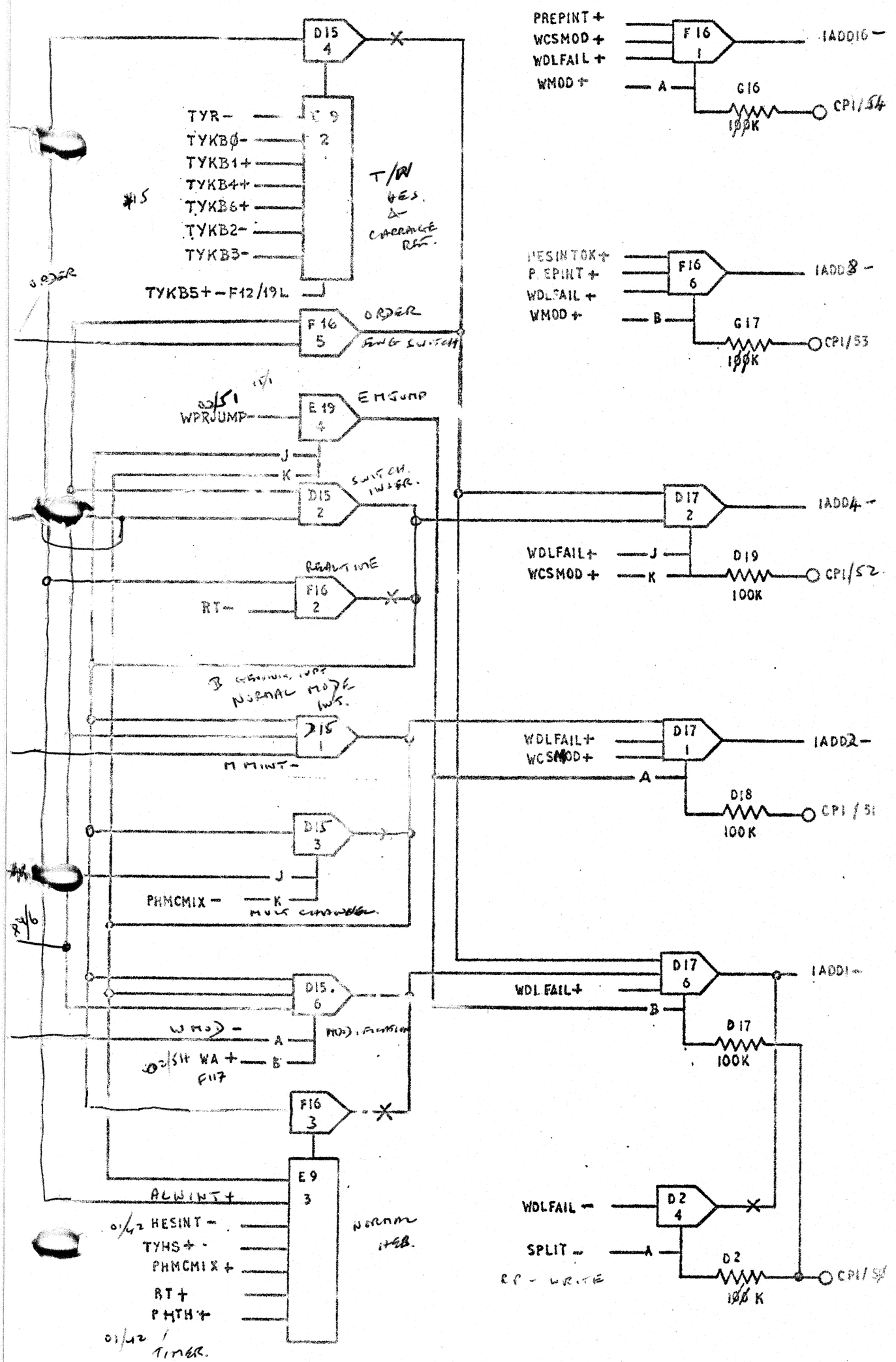
FIXED STORE ADDRESS DECODE
X ADDRESS.





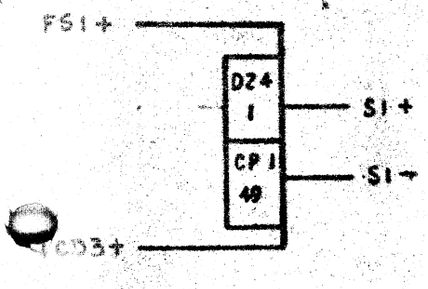
WGC01/18

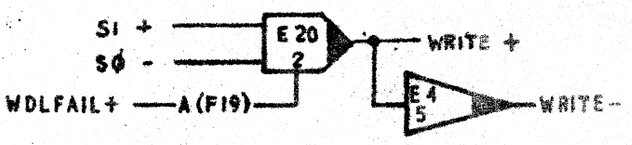
19	1SS	1	2	6															

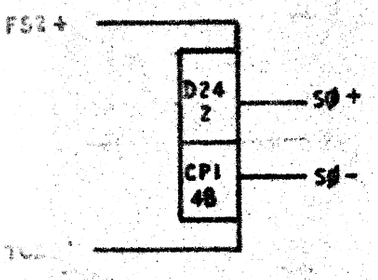

D15 4
E 9 2
TYR-
TYKBØ-
TYKB1+
TYKB4+
TYKB6+
TYKB2-
TYKB3-
T/W
TYKB5+ — F12/19L
F16 5
ORDER
E19 4
WPRJUMP-
EMJUMP
J
K
D15 2
SWITCH. INTGR.
F16 2
RT-
REALTIME
D15 1
MMINT-
D15 3
PHMCMIX-
D15 6
WMOD-
A
B
F16 3
E9 3
ALWINT+
HESINT-
TYHS+
PHMCMIX+
RT+
PMTH+
PREPINT+
WCSMOD+
WDLFAIL+
WMOD+
F16 1
G16
100K
CP1/54
HESINTOK+
PREPINT+
F16 6
G17
CP1/53
D17 2
D19
CP1/52
D17 1
D18
CP1/51
D17 6
D17
D2 4
SPLIT-
D2
CP1/50

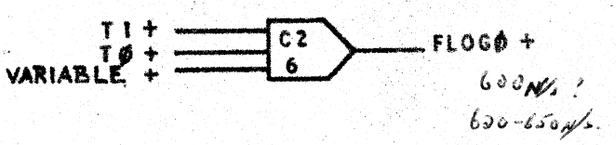
WGC01 / 19

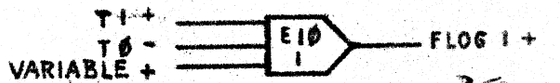
S & T FIELD DECODES 01/31

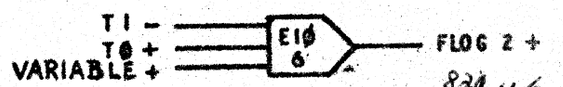


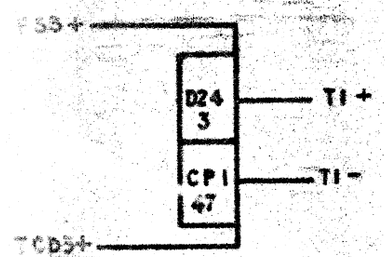


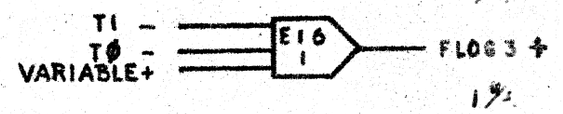


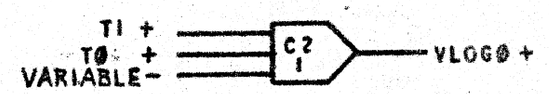


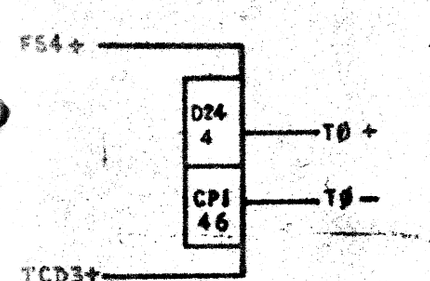


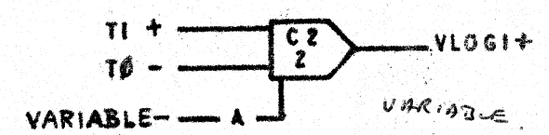


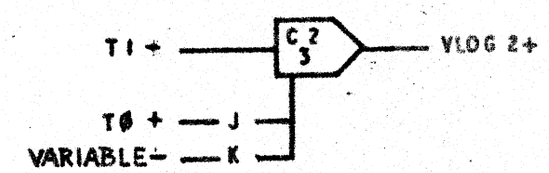


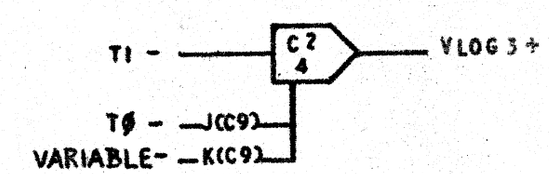


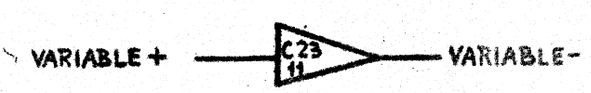






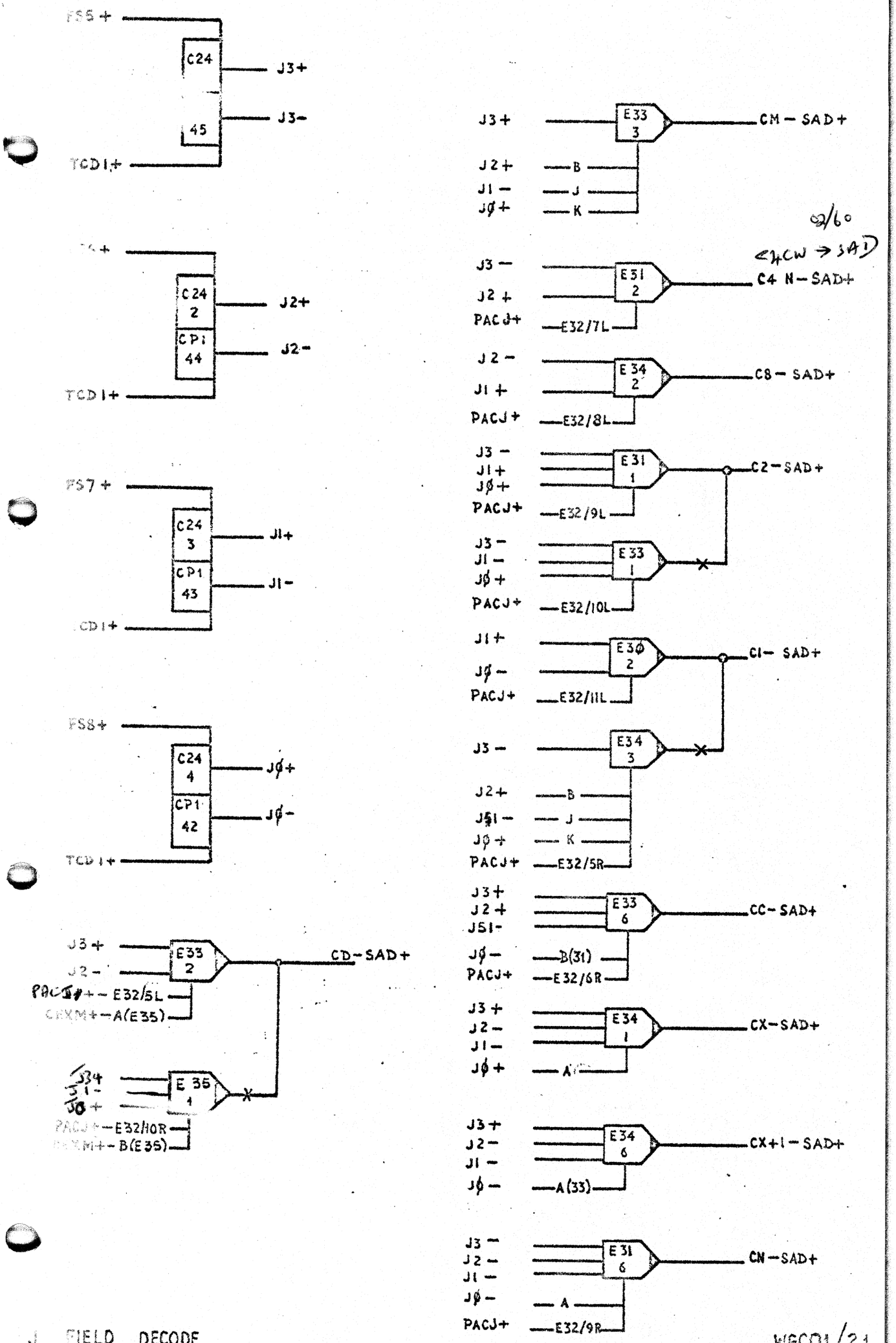






S & T FIELD DECODES WGC01/20

ISS	1	2	3										
A.C.W.	0836	0929	0964	1563									
DATE	11/9/67	19/1/68	16/3/68	23/9/68									



2/60

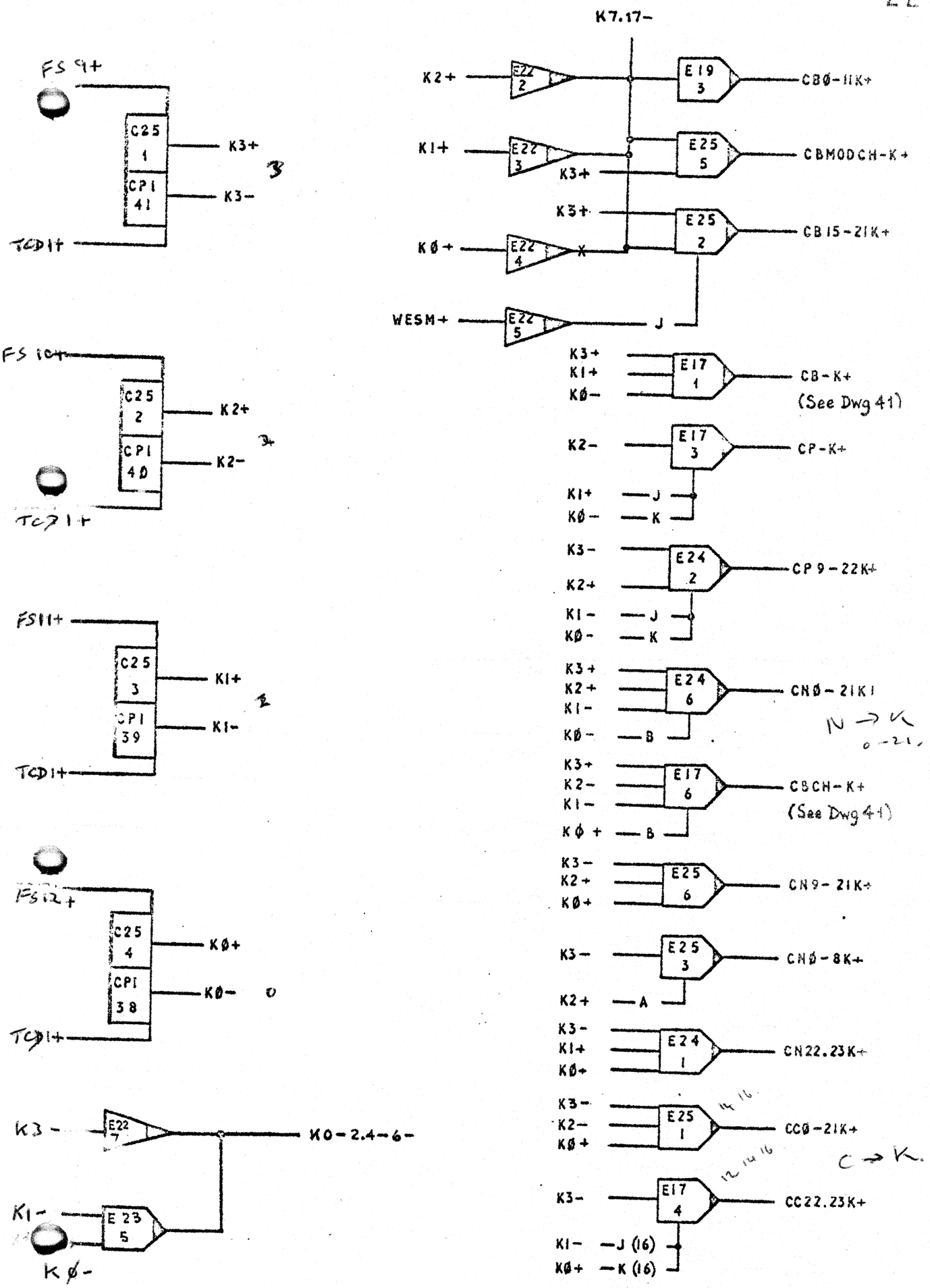
<HCW → SAD>

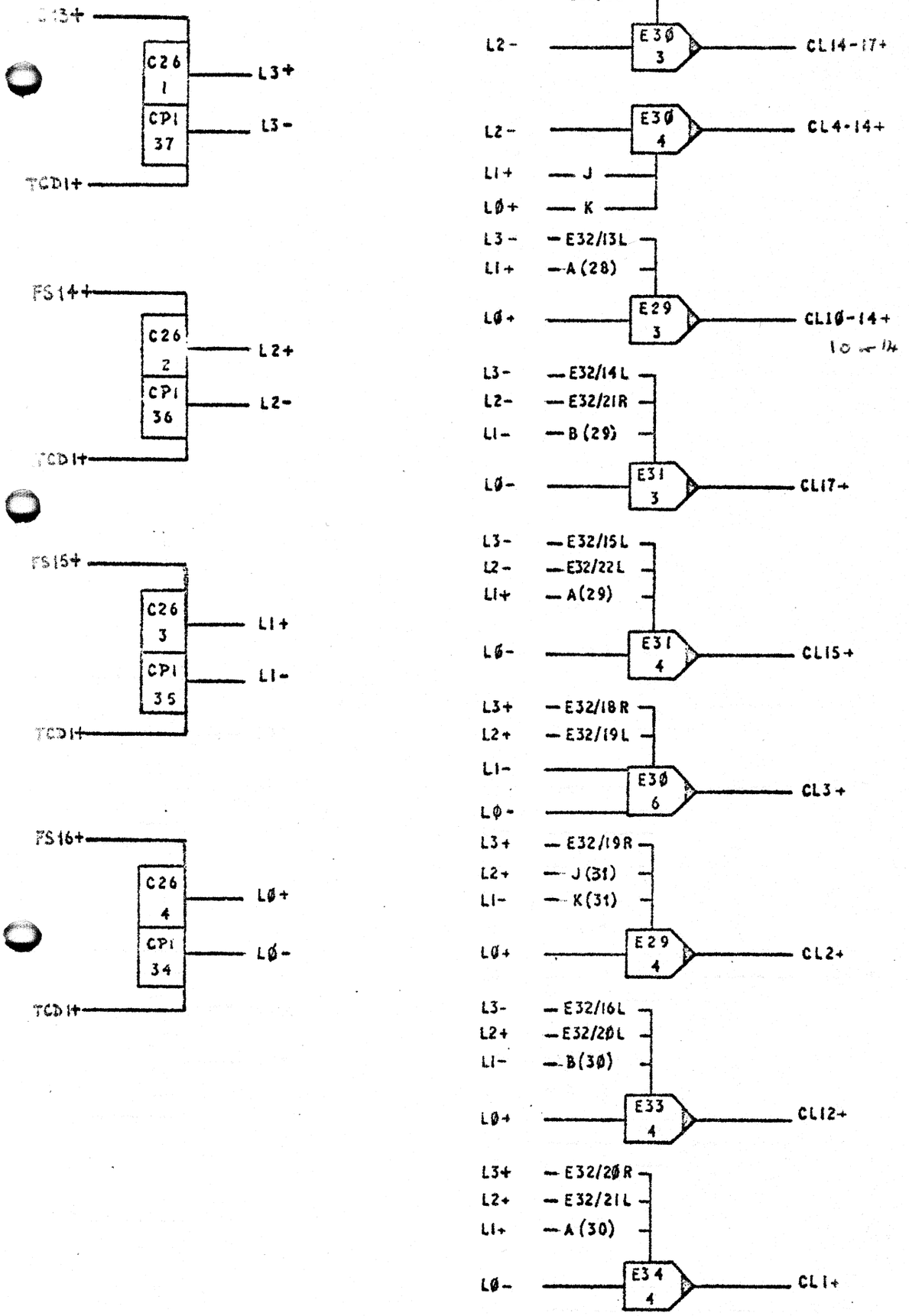
J FIELD DECODE

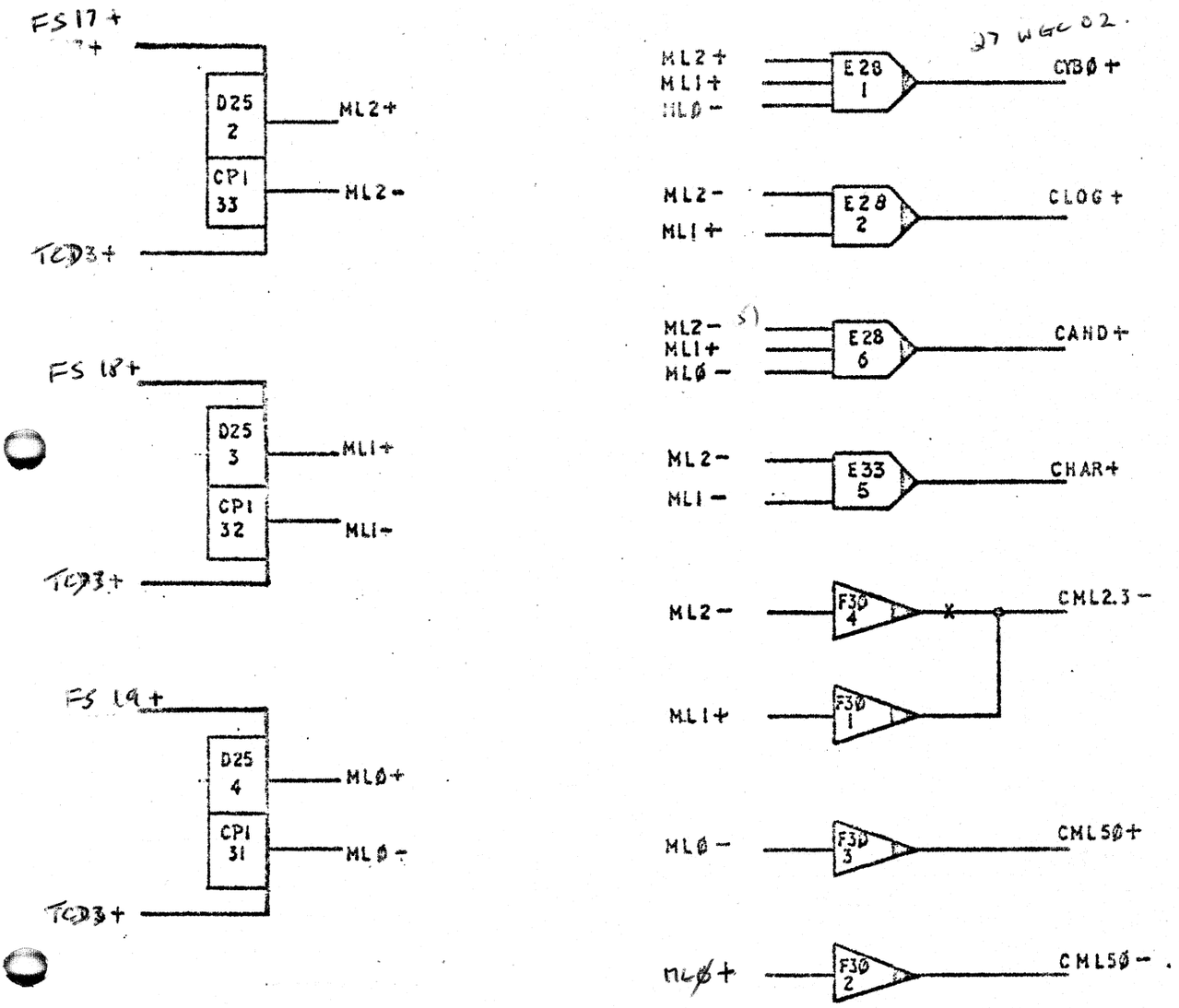
WGC01/21

ISS	1
0836	0929

K Field.

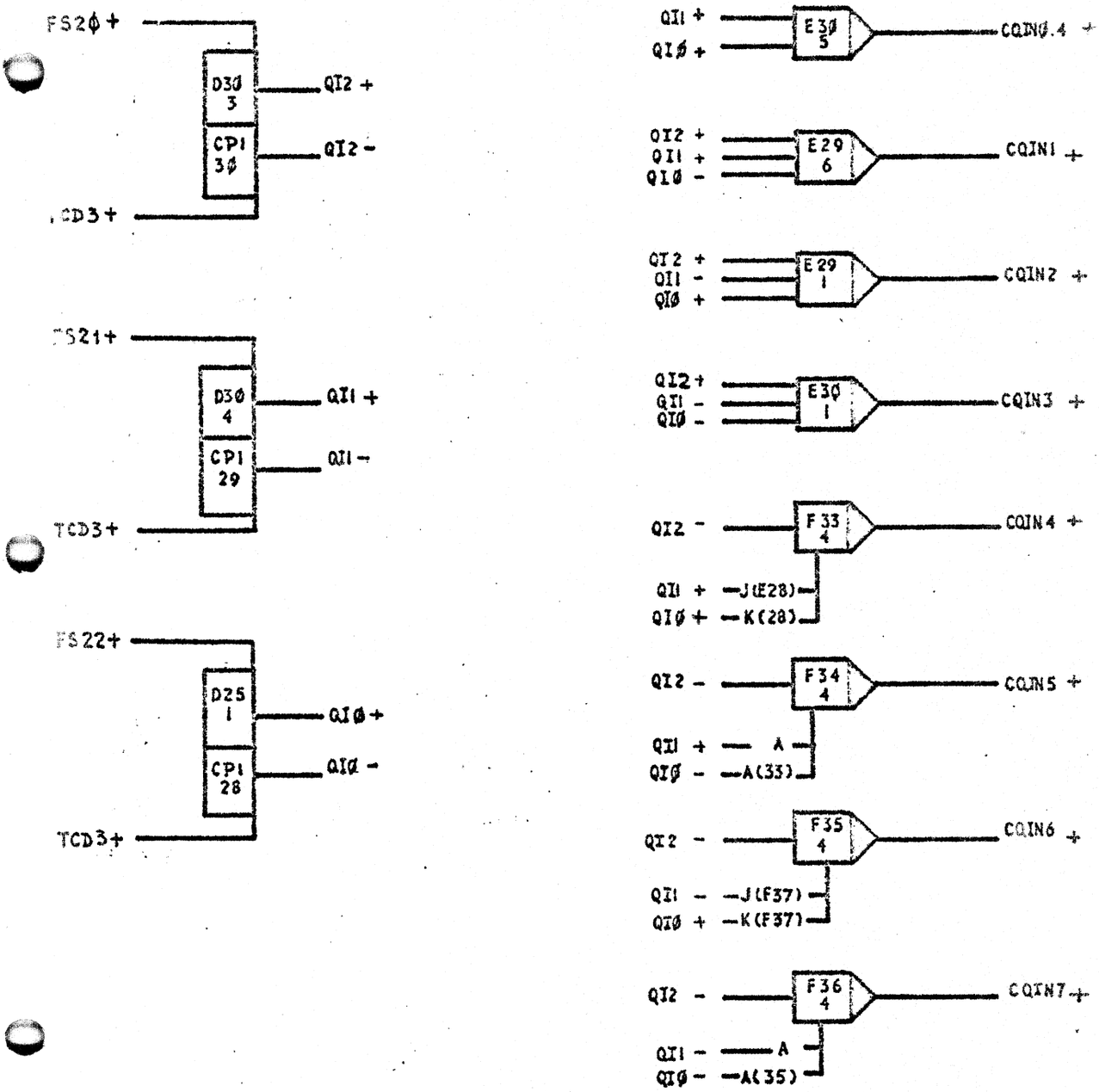

K7.17-
FS 9+
C25 1
CP1 41
K3+
K3-
TCD1+
FS 10+
C25 2
CP1 40
K2+
K2-
TCD1+
FS11+
C25 3
CP1 39
K1+
K1-
TCD1+
FS12+
C25 4
CP1 38
KØ+
KØ-
TCD1+
K3-
E22 7
KØ-2.4-6-
K1-
E23 5
KØ-
K2+
E22 2
K1+
E22 3
K3+
KØ+
E22 4
X
WESM+
E22 5
J
E19 3
CBØ-11K+
E25 5
CBMODCH-K+
E25 2
CB15-21K+
K3+
K1+
KØ-
E17 1
CB-K+
(See Dwg 41)
K2-
E17 3
CP-K+
K1+ J
KØ- K
K3-
K2+
E24 2
CP9-22K+
K1- J
KØ- K
K3+
K2+
K1-
KØ- B
E24 6
CNØ-21K1
N → K
0-21.
K3+
K2-
K1-
KØ+ B
E17 6
CBCH-K+
(See Dwg 41)
K3-
K2+
KØ+
E25 6
CN9-21K+
K3-
K2+ A
E25 3
CNØ-8K+
K3-
K1+
KØ+
E24 1
CN22.23K+
K3-
K2-
KØ+
E25 1
CCØ-21K+
C → K.
K3-
E17 4
CC22.23K+
K1- J (16)
KØ+ K (16)


L3+
C26 1
CP1 37
L3+
L3-
TCD1+
FS14+
C26 2
CP1 36
L2+
L2-
TCD1+
FS15+
C26 3
CP1 35
L1+
L1-
TCD1+
FS16+
C26 4
CP1 34
LØ+
LØ-
TCD1+
L3- E32/2L
L2- E3Ø 3 CL14-17+
L2- E3Ø 4 CL4-14+
L1+ J
LØ+ K
L3- E32/13L
L1+ A(28)
LØ+ E29 3 CL1Ø-14+
10 → 14
L3- E32/14L
L2- E32/21R
L1- B(29)
LØ- E31 3 CL17+
L3- E32/15L
L2- E32/22L
L1+ A(29)
LØ- E31 4 CL15+
L3+ E32/18R
L2+ E32/19L
L1-
LØ- E3Ø 6 CL3+
L3+ E32/19R
L2+ J(31)
L1- K(31)
LØ+ E29 4 CL2+
L3- E32/16L
L2+ E32/2ØL
L1- B(3Ø)
LØ+ E33 4 CL12+
L3+ E32/2ØR
L2+ E32/21L
L1+ A(30)
LØ- E34 4 CL1+



MILL FIELD DECODE. WGC01/24

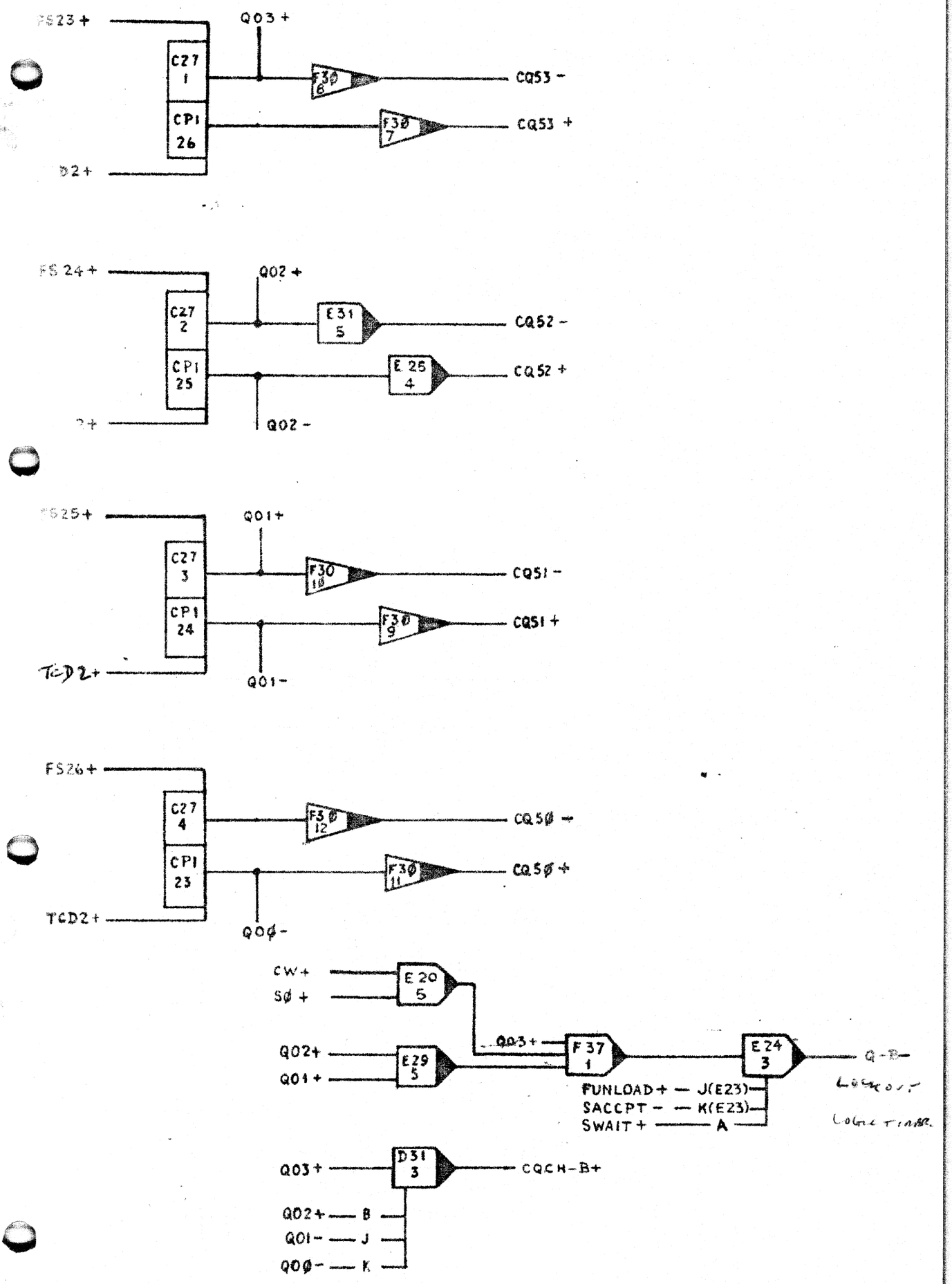
SUB.	ISS	1													
DRW.	0836	0929													



Q IN FIELD DECODE

WGCØ1/25

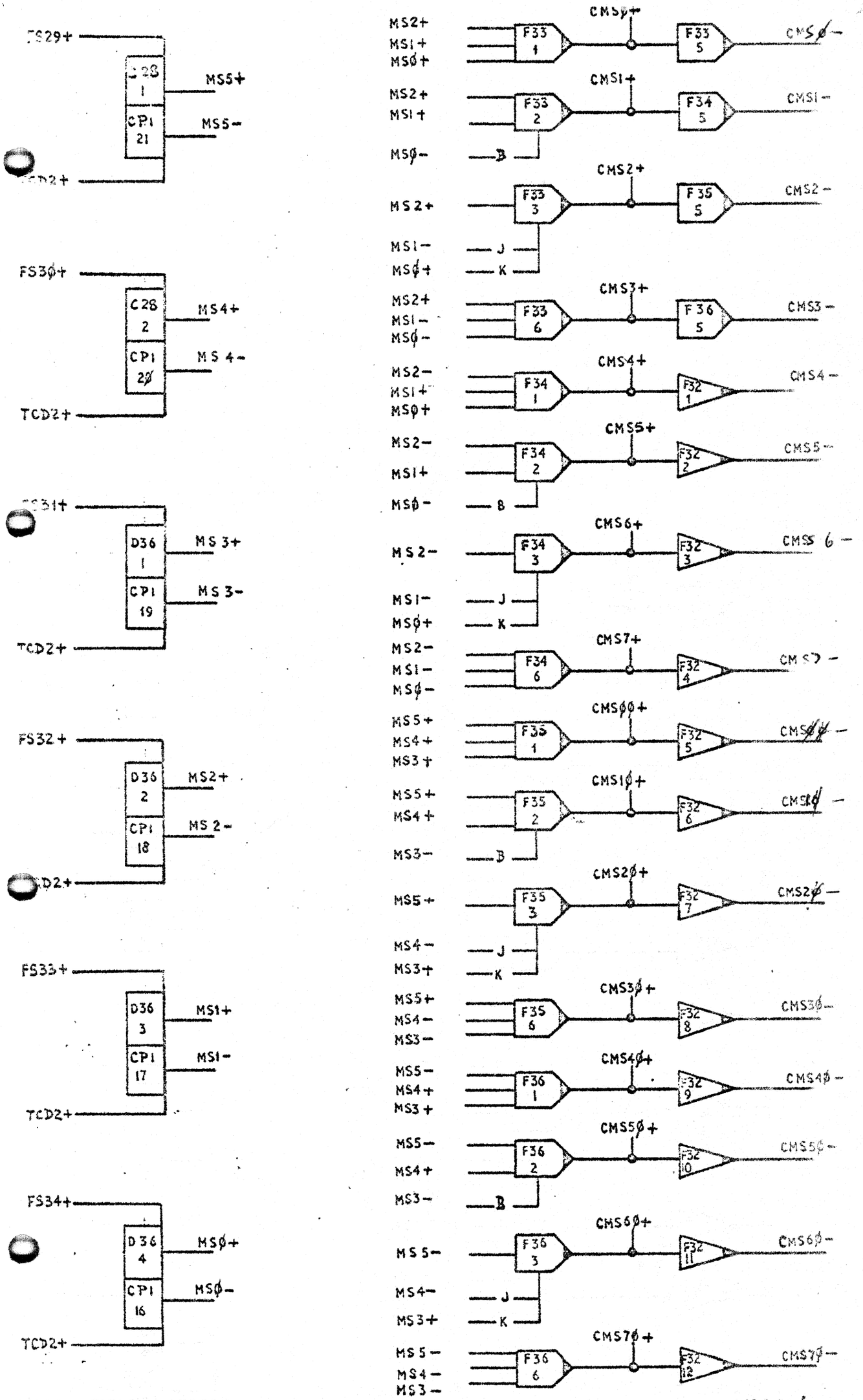
SUB	ISS	1
ACW.	0836	0929



OUT FIELD DECODE.

WGC01/26

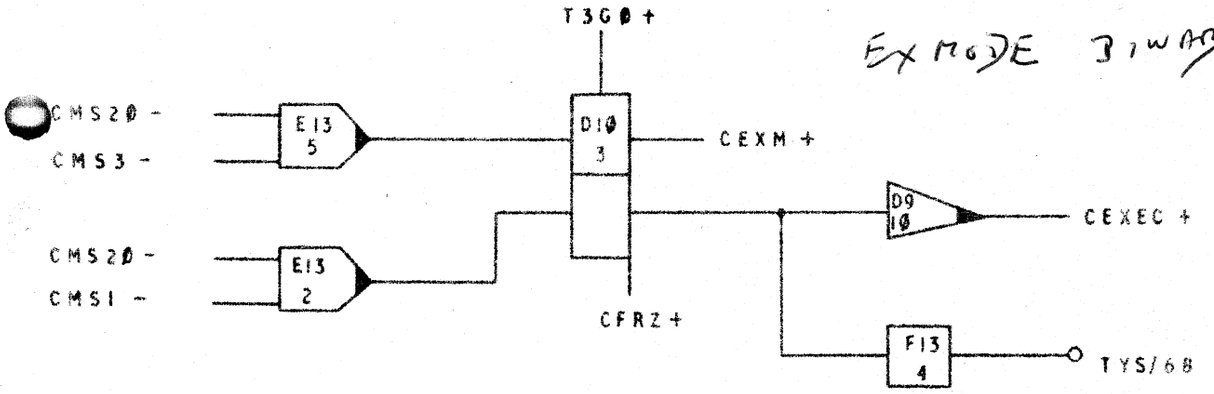
ISS	1	2
836	0929	0964

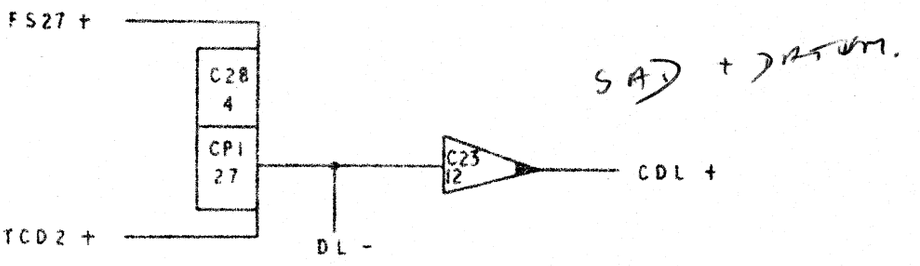


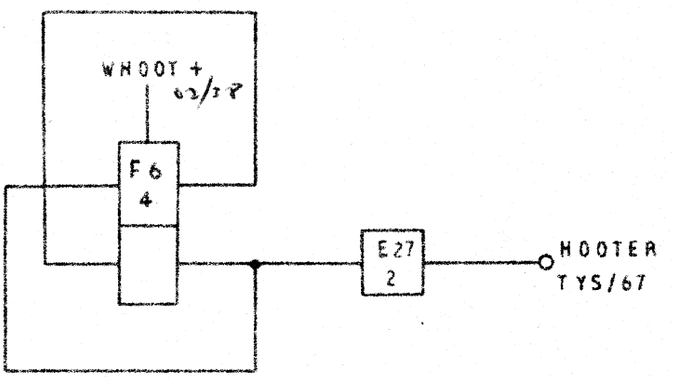
MISC FIELD DECODE

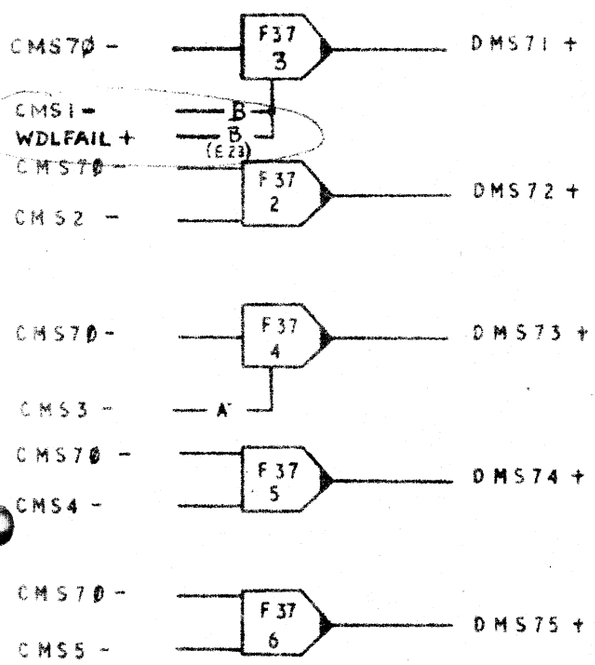
WGC 01/27

SUB	ISS









Flowing down

SUB	ISS	1	2	3	4									
ACW	0836	0876	0929	0964	1545									

1904A SETTING UP INSTRUCTIONS

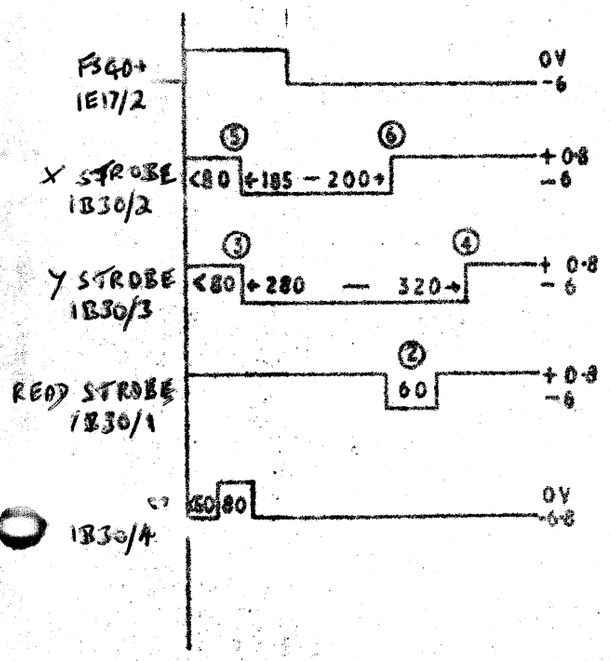
FIXED STORE

a) Voltage supplies - these supplies must be set when the machine supplies are at nominal

Package	Position	Setting	
237	C3/1	+ 1.6V	Initial Setting
	C3/2	-18V	
755	C4/1	+ 2.4V	
	C4/2	+ 1.3V	
759	C5/1	- 4.7V	
	C5/2	Unused	
	C5/3	- 1.8V	

NOTE:- C3/1 is the Read Amplifier Sensitivity and must be set to the middle of its working range measured using FLIT and FLIT + HMS. The working range should be ≥ 1V

b) TIMINGS

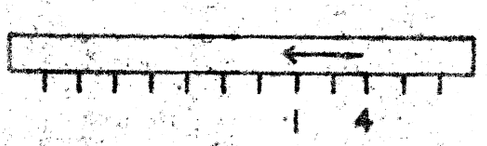


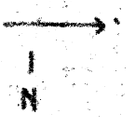
Times in NSEC

Read Strobe is set to the middle of a '1' out of bit 24, measured with a current probe on 1B34/15L

(N) Number of tap on 745 in 1B31

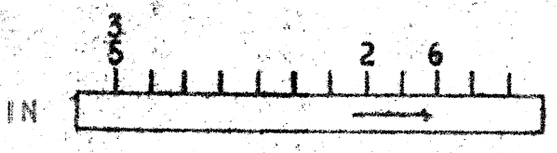
o) NOMINAL SETTINGS OF 1B31



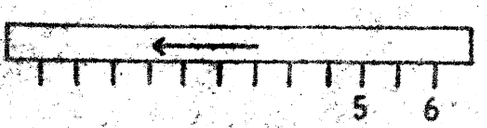


Direction of Delay

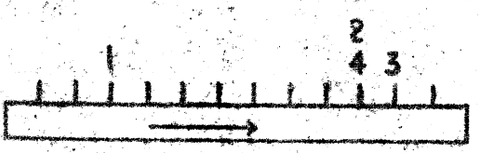
Number of Tap

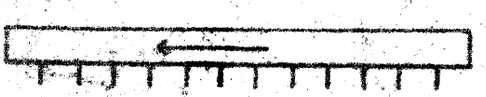


WGC01 NOMINAL SETTINGS

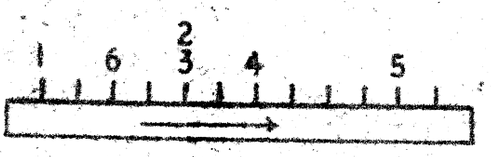


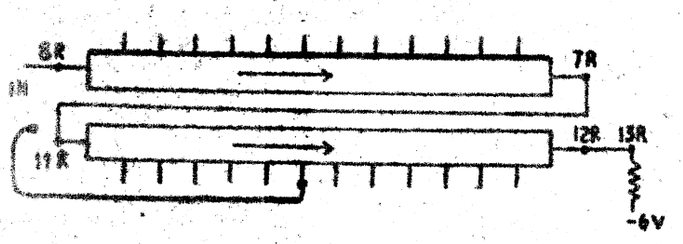
1D6 745
Fixed Store Timing



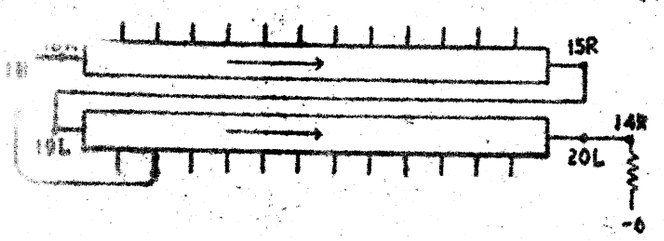


1E6 745
Core Store Timing

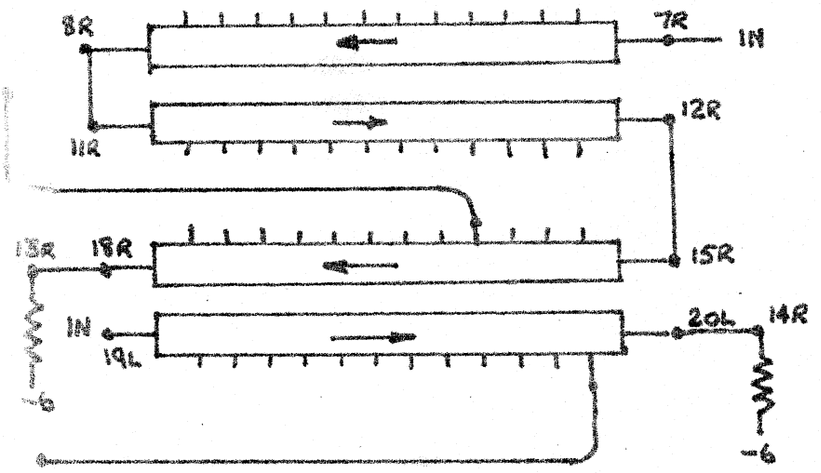




1E5/1 758
EOW Delay

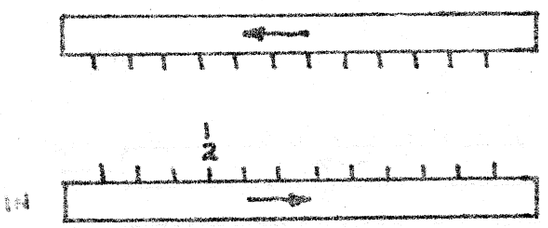


1E5/2
EOR Delay



1F25/1 758
C LINE Delay

1F25/2
T Pulse Width.



1E26
Accumulator Access

WGC 01/29₂

SUB	155	1	
ACW	1519	1550	
RCD	-		
DATE	29/5/68	19/8/68	

BOW & BOR, REMOTE INSTRUCT.

INC. 2/7, 1962 M.

✓ = USED AND REQUIRES SETTING

BASIC			REMOTE			SPEED
BOR	BOW	BFA	BOR	BOW	BFA	
✓	✓	—	✓	✓	—	1.8μs
✓	—	—	✓	✓	✓	6μs

THE ABOVE TABLE INDICATES HOW THE VARIOUS SIGNALS FROM THE STORES ARE USED, AND THUS NEED SETTING UP.
REMOTE BOR & BOW IS ADJUSTED IN SAME MANNER AS FOR BASIC STORE (89). BFA IS SET IN STORE.
IS SET AS EARLY AS POSSIBLE ON DELAY BOARD, FOR FAST REMOTE STORES.
IS GIVEN BY FAST STORE, IN CONTINUOUS CYCLES ONLY, VIA DIFFERENT PINS THAN 1.8μs STORE.
ALL PULSE WIDTHS 150 - 200 nsec.

CORRELATION OF PROCESSOR/STORE PAIRS

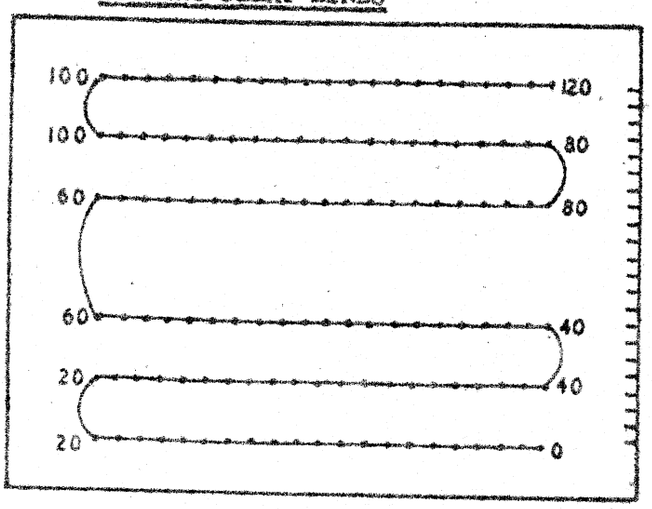
C. P. U. / E$U	FAIRCHILD	LOCKHEED	PLESSEY
SRWU + SRWL + SRWS +	END READ	DATA AVAIL	END READ
SRWU + SRWL + SRWS +	END WRITE	—	END WRITE
SFRWU + SFRWU +	—	WRITE TIMING	—
SFA +	—	STORE BUSY	—
SFAU + SFAL +	LINK IN J2 / 69 (66)	—	LINK IN J2 / 65 (66)

MBC 01/ 89

	1&S	1	
	1519	1550	

SETTING EOR and EOW IN PLESSEY 3D CORE STORES.

PLESSEY DELAY LINES



15nS/Tap

EOR

Package Type 543 in 5/16
The wire attached to Pin 9 is the timing of END READ 1 which determines the Front Edge of EOR. The wire attached to Pin 8 is the timing of END READ 2 which determines the Back Edge of EOR.

Nominal Settings:

END READ 1	Tap 9
END READ 2	Tap 21

ISS	155	1	2	
ALN	1519	1536	1550	
ACD				
DATE	24/5/68	22/7/68	19/8/68	

BOW Package type 543 in 5/15

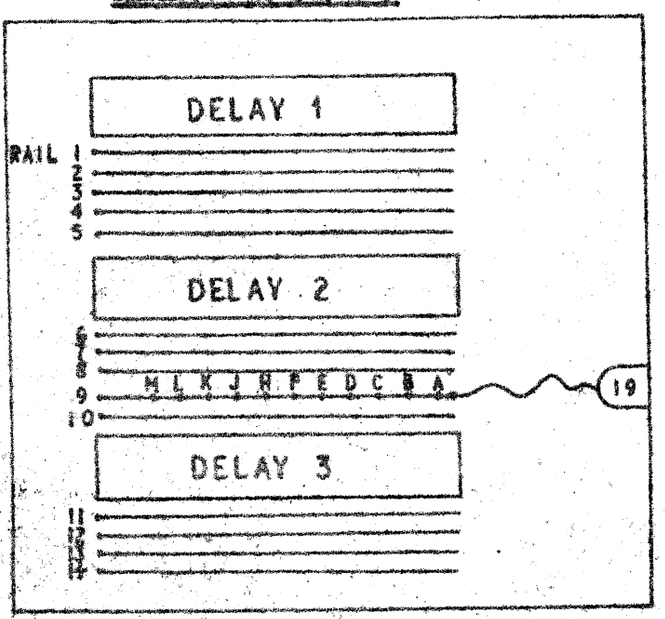
Pin 7 END WRITE 1 Front Edge Nominal Tap 51
Pin 25 END WRITE 2 Back Edge Nominal Tap 64

FARNITEK 1.8uSec STORE

EOR 845 PACKAGE in C29

EOR

FARNITEK E.O.R. C29 A30

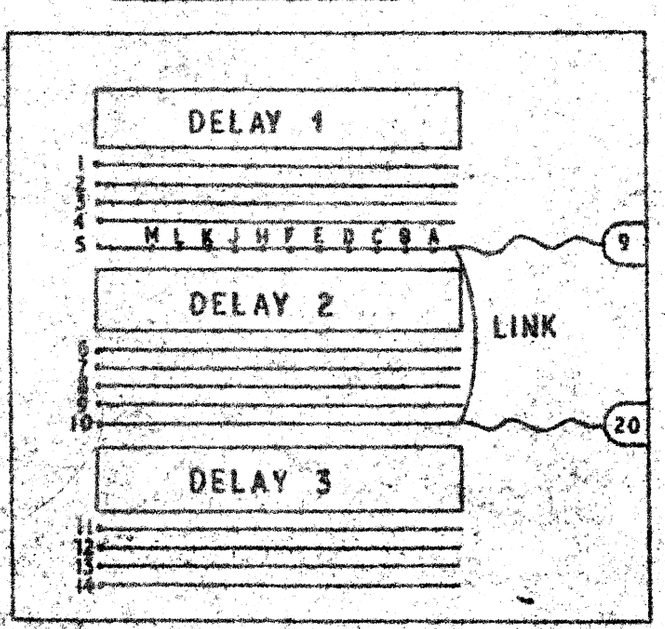


Nominal Setting 'A' L

Delay Line 2, Rail 9, Pin 19 determines the front edge of EOR

BOW 845 PACKAGE in C31

FARNITEK E.O.W. C31 A32



A Remote ~~Local~~
Nominal Setting 'D' ~~Remote~~ Local

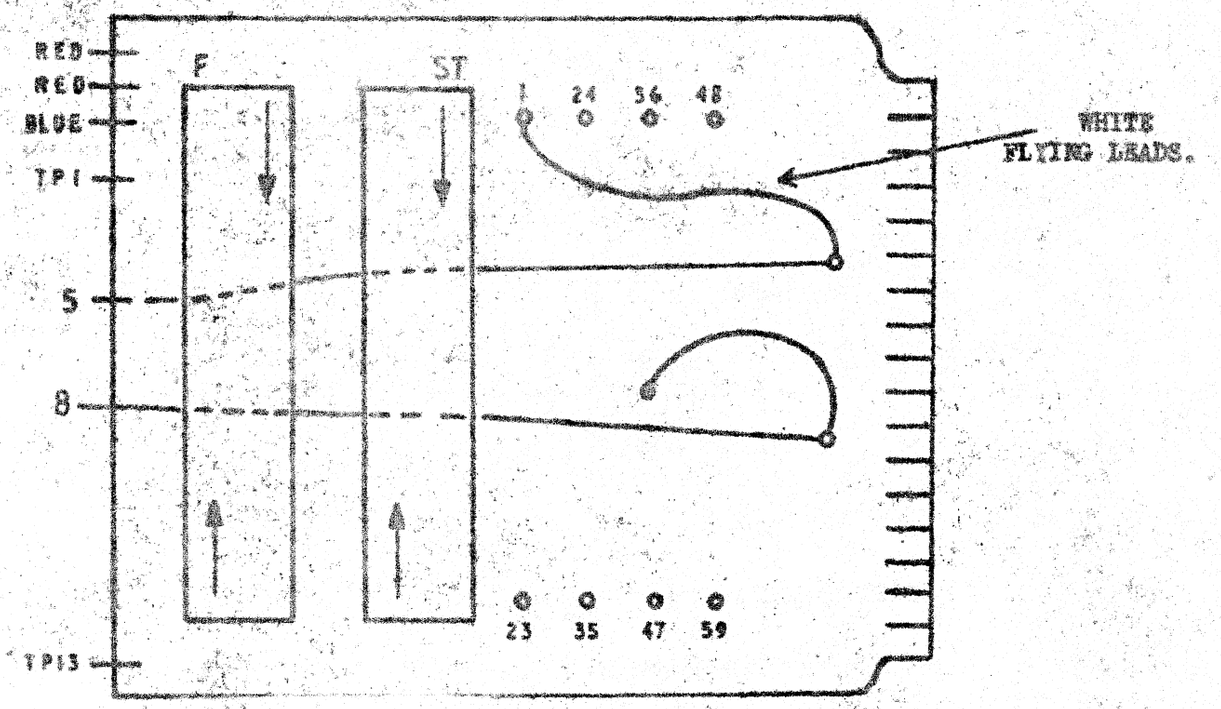
The Link may be replaced by a Mod.

EOR	1559	1	2
EOW	1519	1535	1550
BOR			
BOW	1-46 low	2nd 1/2	1st 1/2

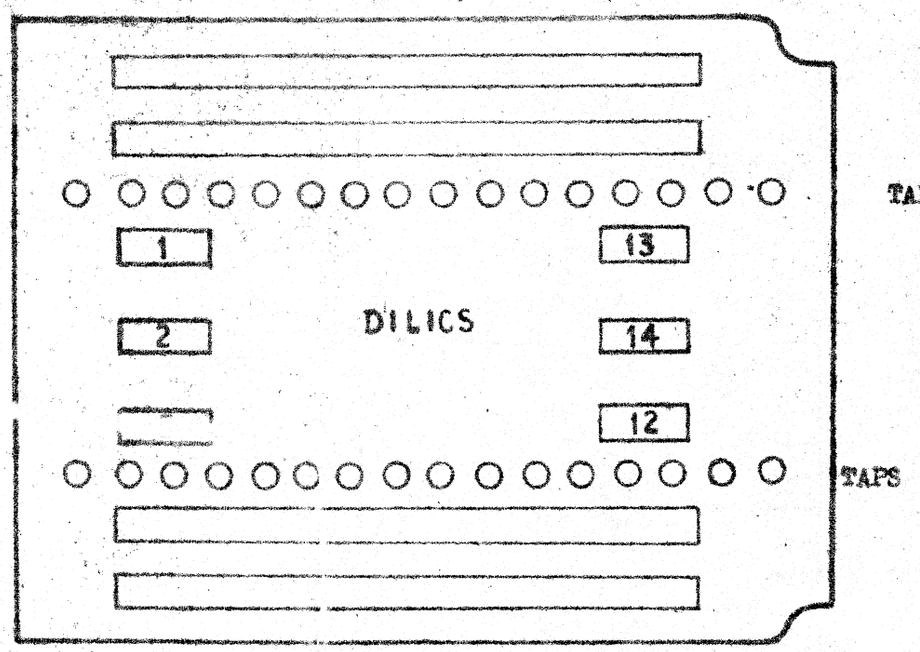
LOCKHEED 650NS

NOR. SET SIDE ON PACKAGE C2 TP/8 WHICH HAS A NOMINAL SETTING OF TAP 42 . WIDTH IS SET TO 200NS BY POT 3 ON H5.

NOW. SET SIDE ON C2 TP/5 WHICH IS SET AS EARLY AS POSSIBLE AND GIVES AN END OF WRITE ONLY USED WHEN IN REMOTE POSITION. THE ONLY CRITERIA IS THAT WHEN SO SET, NOR IN MACHINE MUST HAVE SOME AWAY BEFORE TRUE NOW POPS OUT OF D3/2.



	PLESSEY 2½ D	DILIC I/C
NOR.	SET SIDE IS ON BOARD A7/ TAP 7	14
	RESET SIDE IS ON BOARD A9/TAP 1	6
NOW	SET SIDE IS ON A8/TAP 27	12
	RESET SIDE IS ON A8/TAP 42	4



ALL DILICS AND TAPS ARE SIGNWRITTEN.
NOTE THIS NOMINAL FOR NOW WOULD NOT SUIT A REMOTE STORE.
REFER TO SETTING UP INSTRUCTIONS.

WGC 01/29.

SUB	155	1	2		
ACW	1519	1535	1550		

Check the following timings with FLIT running where possible. If any delay needs to be changed more than one tap then the reason must be thoroughly investigated.

Delay Line 1D6 (Trigger 1D5/2+)

Tap 1

Ensure that all BA signals (1B14/1 - 1B14/16) are true before Y Strobe (1B30/3) is negative.

Tap 4

TCD2+ (1D22/3) should go negative at least 50ns before FS data bit 25 (1B35/3) goes negative.

Tap 3

This is the machine clock and should be 1 tap later than tap 4. The third generation clock should be at the same time as the earliest decode changes.

Tap 2

TSR+ (1D9/2) should go negative after ACCS+(1E29/2) [or STORE - (1E23/2) when no ACCS] goes negative to prevent 1E7/6 and 1E14/1 from snigging and must never be on a tap earlier than TCD2+(tap4)

Tap 5

Should be set so that no negative snigs appear in TEN+ (1D11/9) which is a stretched version of TSR+ (1D9/2) (see 29g E5 tap 1)

Tap 6

TBK- (1D9/5) must go negative after BUSYB+ (1D10/4) has gone positive.

1D4/2 Bottom pot on 772 package THA-

INTOK+ (1D9/3) goes negative at the same time as Y Strobe (1B30/3) goes positive.

SUB	ISS					
ACW	1550					
ACD	-					
DATE	19/8/68					

Delay Line 1E6

Tap 1 (Trigger 1E10/3+)

All 'Jangle' on SENU- (2F2/4) must have ceased by the time of SCI+ (1E1/5). Adjusted by TEN+ (Tap 5 on 1D6). Only adjust tap 1 if it is impossible to move TEN+ late enough. If there is only one store use SENL- (2F2/1).

Tap 2 (Trigger 1E6/3-)

SOUT24L- (2G9/3) must be true at the time of SWCI+ (1E8/6).

Tap 3 (Trigger 1E10/3+)

Set the width of SCI+ (1E1/5) to be 150 nS, with no SMAC connected.

Tap 4

ACC-B+ (1E17/5) should go positive just after WSAD <8+ (2A1/1) goes positive with ACCS ON. 2/44.

Tap 5 (Trigger 2C25/1+)

1E6/5 should go negative just after SINH- (2F2/6).

Tap 6

See Note on EOW in Core Store.

EOR IN CORE STORE (Trigger 1D10/4+)

The width of EORC- (1E15/1) should be 200-300nsec.
SIN-B- (2C23/3) should go negative after the last data bit (2C2 & 2D2) goes negative.
(NOTE: A nominal setting is used for FERRITEK Stores which have a very fast access, cycle init. to DATA in B REG = 750 NS).

EOR For ACCS (Trigger 1E23/6+)

Tap 2

ACC- B+ (1E17/5) should be 150nS wide when ACCS- (1E22/9) is present.

Tap 1

ACC-B- (2A1/3) should go negative after the last HXB- (Slices WGC02).

1E5/2 Parity Checking (Trigger 1E19/2+)

C Check that PGEN+ (2H10/3) and PGEN- (2B10/2) are true before SPAR- (2F8/12).

EOW In Core Store (Trigger 2G12/7-)

The width of 1E15/6 should be 200 - 300 nsec. (150NS in Lockheed).
Insert in address 0 *25252525 and
in address 1 *52525252
obey a 111 0/1 order on the Handkeys.
For a 1.8uSec store SOUT- (say 2C5/5) should change 1.75uSec after SCI+ (1E1/5) on the first of the two WRITE cycles.

For a 650nS Store SOUT- should change 650nS after SCI+ (Adjust 1E6/6) and EOW+ (1D3/2) must be later than EORC- (1E15/1) disappears.

1E5/1 EOW IN MACHINE (Trigger 2G12/7-)

Obey a 100 0/0 order on the Handkeys
SNR+ (1E1/3) should go negative either 650ns or 1.8uS after SCI+ (1E1/5) on the WRITE cycle.

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LOGIC TIMINGS (Trigger 1D5/2)

Set 1D4/2 to be -4.5v measured with an AVO 772 Package in 1D4

L0 Fixed should be set to be about 620-650nS by replacing the top potentiometer by fixed resistors or wire.

L0 Variable should be set as fast as possible.

L1 & L2 Variable (Potentiometers 6 & 7) should be set so that the machine just works with FLIT and nominal voltages.

L1 and L2 fixed (Potentiometers 2 & 3) should be set 10% slower.

The times should be L1 fixed $\simeq$ 750nS
L2 fixed $\simeq$ 820nS

Potentiometers 2 & 3 should then be replaced by fixed resistors to give the same timings.

L3 fixed and variable (potentiometers 4 & 8) should be set to 1uSec. Potentiometer 4 should then be replaced by a resistor to give the same timing.

Any machine needing settings significantly different must be investigated more closely.

The times should be measured by accessing a single fixed store address.

L0	5, 16, 5
L1	0, 17, 5
L2	3, 1, 4
L3	3, 13, 3

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WGC 01/29$_9$.

1904/5 E/F MAINTENANCE ROUTINE.

WEEKLY

W1 Systems Margins

1 hour

The system is to be loaded with ≠ Flit and normal mode programmes to exercise all allocated peripheral channels simultaneously. It should be ensured that programmes are spread over the whole of the core store. There should be no failures with the power rails set to the following margins in turn.

a) All +6v supplies at +6.6v
b) All +6v supplies at +5.4v
c) All -6v supplies at -6.6v
d) All -6v supplies at -5.4v
e) All -28v supplies at -29.2v
f) All -28v supplies at -26.6v

Voltages should be measured in the backwiring using an AVO, and each parameter should be held at its margin for 5 minutes.

½ hour — W2 Check fans for correct operation.

MONTHLY

M1 Performance tests

30 minutes — Run the programmes TTOL, TIME, ≠ POWU and if hardware Floating Point is fitted ≠ GIBS. Compare the outputs with those listed in the machine logic drawings.

M2 Core Store Margins

10 minutes for first store, 5 minutes each subsequent store) — Using the core store test programme at the end of NCRs (shortly to be re-issued as a separate programme) establish that no faults occur with each switched core store parameter separately in the marginal condition.

M3 Fixed Store Margins

5 minutes — Using Flit with timer running and monitoring test point on 237 package, no fails should occur with the read amplifier bias ± 0.5v on nominal. Repeat with hesitation switched on.

M4 Central Processor Margins

30 minutes — Using Flit, with timer running, establish the following margins:-

a) All +6v supplies at 6.8v
b) All +6v supplies at 5.2v
c) All -6v supplies at 6.8v
d) All -6v supplies at 5.2v
e) All -28v supplies at 29.6v
f) All -28v supplies at 26.4v

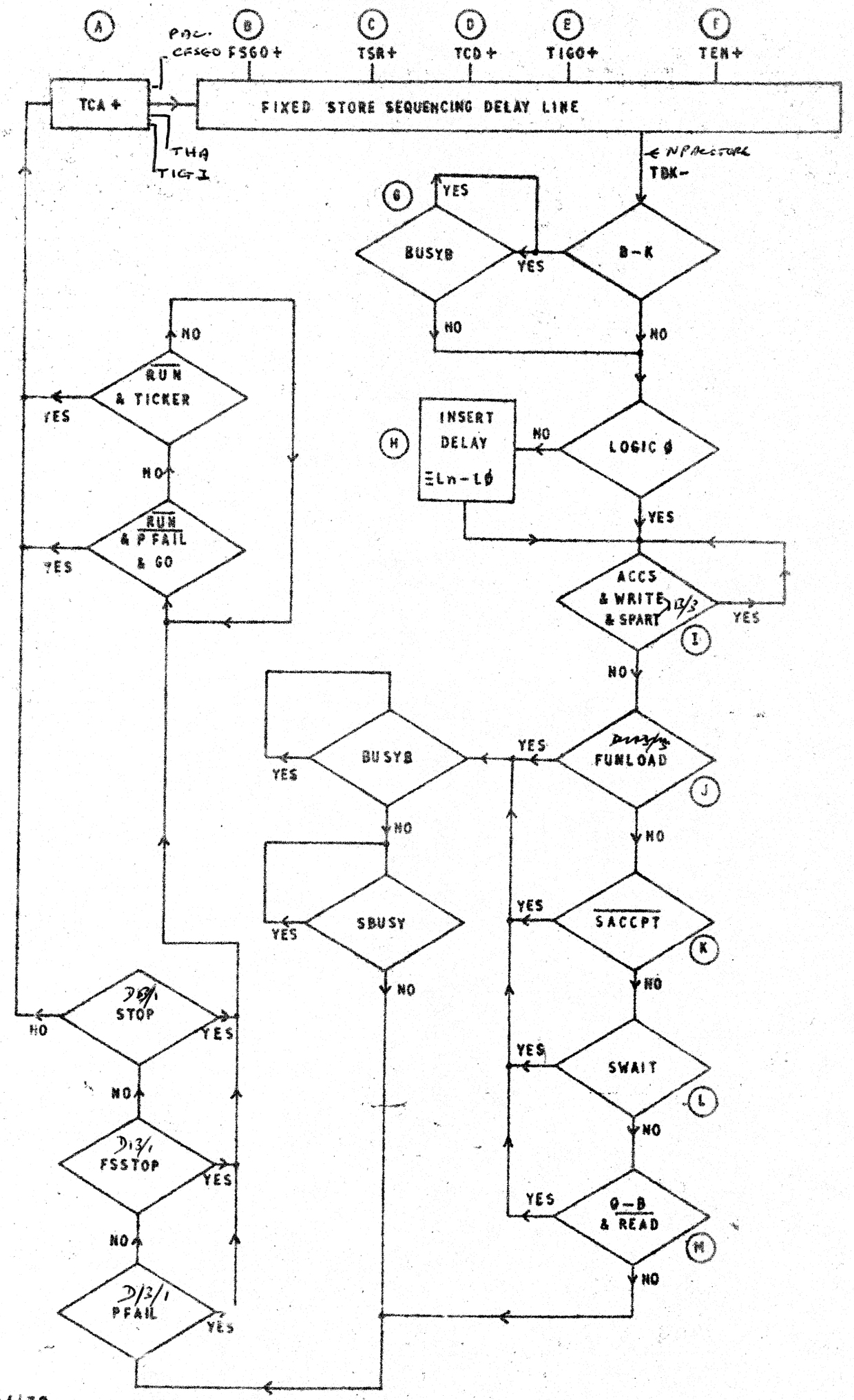
Repeat with hesitation switched on. Voltages should be measured in the backwiring using an AVO.

5 minutes — M5 Machines with WGA 07 only (Slow Floating Point)
As in M4 but additional vary -6 variable supply ± 1 volt.

M6 Filters
Clean Air Filters.

M7 Carry out W1, opening & closing all logic doors whilst so doing.

6 monthly — Air Filters Replace all air filters.



WGC 01/30ø

SUB	ISS
ACV	1519

NOTES ON INTERLOCK LOGIC.

A) TCA — Resets unused fixed store address stats.

B) FSGO — Timed to occur when the the decoded fixed store address is true.

C) TSR — Masks snigs at the time the fixed store speaks.

D) TCD — Resets unused FS data stats.

E) TIGO — Machine clock, set to occur just before the decodes collapse as a result of TCD.

F) TEW — Sets a time for the core store enable to be decoded before a store cycle Initiate can be given.

G) Wait for the Core Store Data during a core store read.

H) Time a delay dependant on the Mill Operation being carried out.

I) Wait for parity to be calculated before writing to the Accumulators

J) When unloading the Floating Point it waits for Data and Parity.

K) Waits for the store accept which is important if SMAC is being used.

L) Waits for the previous store cycle to finish

M) Prevents the machine clock overwriting the B register before the core store store has completed writing.

WGC 01/3

SUB	155		
ACV	15.9		

SO2

MACHINE CONFIDENCE CHECKS

FOR

1904/5-E/F

1. Criteria

1.1. Performance Figures

These shall meet the targets laid down as per WGC01/30 4..

1.2. Margin Tests

The appropriate programs shall be run for five minutes at each setting of the margins without failure. All voltages are to be measured in the back wiring using a calibrated Avometer.

1.3. Overall Criteria

The tests are to be carried out in the order shown and will be continuous. That is, there shall be no interruption of the tests other than normal breaks between shifts. The failure of any one test will necessitate the repetition of all those tests which cover aspects of the machine which are likely to have been affected by the cause and rectification of the failure.

2. TIMINGS

2.1. Logic Beat Timings

Check that these are set up as per WGC01/29 0-6.

2.2. PAC Timings

Check that these are set up as per WGC07/PAC/3.

3. PERFORMANCE TESTS

Run the programs TTOL, TIME, PAC-T, # POWU, Bamford mix and if hardware floating point is fitted run also # GIBS.

4. Margins Tests

During these tests whilst the voltages/current are still at nominal and the appropriate programs are running all doors shall be opened and closed and the packages vibrated in a sensible manner to test for intermittencies.

4.1. Core Store Margins with C.P.U.

Programs-WCR Store Tests."
Margin settings-a) Each switched Core Store Parameter seperately in the Marginal Condition.

4.2. Fixed Store Margins IC3/1

Programs-FLIT with timer running.

Margin Settings a) nominal plus 0.5V.
b) nominal minus 0.5V.

Repeat with hesitations switch on.

4.3. C.P.U. Margins

Programs-FLIT with the timer running.
The voltage over the whole machine should be varied at the same time.

Margin Settings
a) +6V set to +6.5V
b) +6V set to +5.5V
c) -6V set to -6.5V
d) -6V set to -5.5V
e) -28V set to -29.0V
f) -28V set to -26.4V

Repeat with hesitations switched on.

WGC04/30

4.4. Slow F.P.U.

Additional to Section 4.3.

Margin Settings a) - 6V Variable Supply nominal plus 1V
b) - 6V Variable Supply nominal minus 1V

4.5 PAC Margins

Program - PAC-B. To be run on every PAC channel, and with Test Hesitations on channel 4. Margin settings - as in 4.3.

4.6. System Margins

Programs - The system is to be loaded up with normal mode test programs so as to exercise all allocated peripheral channels simultaneously. This shall be carried out in two stages if there are more than 8 channels‡FLIT should be one of the programs and it should be ensured that the programs are spread over the whole area of Core Store.

Margin Settings.
a) + 6V set to + 6.6V
b) + 6V set to + 5.4V
c) - 6V set to - 6.6V
d) - 6V set to - 5.4V
e) - 28V set to -29.2V
f) - 28V set to -26.6V

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1904/5 R/T PERFORMANCE

The figures obtained by running the Normal Mode Programs #POWU and #[illegible], with no other programs running, will be less than those listed below.

1904/5E					1905/5F			
-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's		-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's
< 6550	6800	5300	5600	# POWU 4 Secs (RAMFORD)	< 4550	5550	4300	4850
< 570	610	520	560	# GIBS 4 Secs (GIBSON MIX)	< 360	430	340	400

1904/5 R/T PERFORMANCE

1. Instruction Times

The times quoted ± 5% are those measured by an Executive Mode Program (TIME). The instruction time quoted includes the preparation of order time.
It should be noted that there is a ± 2% tolerance of the Timer Interrupts.

2. The Slow Floating Point Unit Times ± 5%

Phases 1, 2 and 3 are performed inside the processor and phase 4 inside the F.P.U. Phase 4 cannot start until phase 3 is complete, and the next phase 3 cannot start untill phase 4 is complete, but phases 1 & 2 can be performed in parallel with phase 4.

3. The Fast-Floating Point Unit Times ± 5%

Phase 1, 2 and 3 are performed inside the processor and phase 4 inside the F.P.U. Phase 4 cannot start until phase 3 is complete, and the next phase 3 cannot start until phase 4 is complete, but phases 1 and 2 can be performed in paralled with phase 4
But in Normal Mode the F.P.U. has a buffer which can queue 1 phase 3 (Load) in Add/Subtract and Division.

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AGD		
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1904E INSTRUCTION TIMES μ Secs

-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's	ORDER MODIFICATION
1.8	1.9	1.0	1.0	
5.4	5.9	3.7	4.1	000
6.4	7.0	4.9	5.5	001
5.8	6.6	4.7	5.2	002
6.4	7.0	4.9	5.5	003
5.4	5.9	4.7	4.6	004
6.4	7.0	4.9	5.5	005
5.8	6.6	4.7	5.2	006
6.4	7.0	4.9	5.5	007
5.4	5.9	4.8	5.3	010
6.4	7.0	5.0	6.0	011
5.8	6.6	4.9	5.4	012
6.4	7.0	5.0	6.0	013
5.4	5.9	4.8	5.3	014
6.4	7.0	5.0	6.0	015
5.8	6.6	4.9	5.4	016
6.4	7.0	5.0	6.0	017
6.4	7.0	4.9	5.5	020
6.2	6.9	4.8	5.4	021
6.4	7.0	4.9	5.5	022
1.8	1.9	1.8	1.9	023
5.4	5.9	4.0	4.5	024
6.4	7.1	5.2	5.9	025
6.0	6.5	5.5	6.0	026
5.4	5.9	4.7	5.2	027
6.4	7.0	5.0	6.0	030
6.4	6.9	4.9	5.9	031
6.4	7.0	5.0	6.0	032
4.0	4.6	4.0	4.6	033
6.3	6.8	4.8	5.8	034
6.3	6.8	4.8	5.8	035
8.5	9.6	7.8	8.6	036
6.3	6.8	4.8	5.8	037
25	26	21	22	040
26	27	22	23	041
25	26	21	22	042
17	19	12	13	043
32	33	28	27	044
36	37	32	31	045
31	32	28	28	046

1904F INSTRUCTION TIMES μ Secs

-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's
1.3	1.7	0.9	0.9
2.9	3.9	2.8	3.5
4.5	6.0	4.1	5.0
4.0	5.1	3.9	4.8
4.5	6.0	4.1	5.0
3.3	4.5	3.3	4.1
4.5	6.1	4.1	5.1
4.0	5.1	3.9	4.8
4.5	6.0	4.1	5.0
3.6	4.5	3.5	4.3
4.5	6.0	4.2	5.2
4.0	5.2	3.6	4.3
4.5	6.0	4.2	5.2
3.6	4.5	3.6	4.3
4.5	6.0	4.2	5.2
4.0	5.2	3.6	4.3
4.5	6.0	4.2	5.2
4.5	6.0	4.1	5.0
4.4	5.9	4.0	4.9
4.5	6.0	4.1	5.0
1.5	1.7	1.5	1.7
3.2	4.4	3.2	4.1
4.5	5.7	4.4	5.3
4.7	5.8	4.7	5.6
3.9	5.0	3.9	4.8
4.5	6.0	4.2	5.2
4.4	5.9	4.1	5.1
4.5	6.0	4.2	5.2
2.7	3.5	2.7	3.5
4.3	5.8	4.0	5.0
4.3	5.8	4.0	5.0
6.6	8.0	6.3	7.2
4.3	5.8	4.0	5.0
22	24	21	22
23	25	22	23
22	24	21	22
12	16	11	13
28	31	27	28
32	35	31	32
28	30	27	28

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1904E INSTRUCTION TIMES μ Secs

-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's	ORDER
25.9	27.5	22	23.3	047
4.3	4.8	3.8	4.2	050 N
3.6	4.1	3.1	3.5	050 Y
4.3	4.8	3.8	4.2	052 N
3.6	4.1	3.1	3.5	052 Y
4.3	4.8	3.8	4.2	054 N
3.6	4.1	3.1	3.5	054 Y
4.3	4.8	3.8	4.2	056 N
3.6	4.1	3.1	3.5	056 Y
5.4	6.0	3.8	4.2	060 N
5.4	6.0	3.8	4.2	060 Y
5.4	6.0	3.8	4.2	062 N
5.4	6.0	3.8	4.2	062 Y
5.4	6.0	3.8	4.2	064 N
5.4	6.0	3.8	4.2	064 Y
5.8	6.2	4.4	4.8	066 N
5.8	6.2	4.4	4.8	066 Y
5.5	6.0	4.3	4.8	070
5.3	6.0	5.1	5.5	072
2.4	2.7	2.4	2.7	074
4.1	4.7	3.0	3.4	100
4.7	5.1	3.2	3.6	101
4.1	4.7	3.0	3.4	102
4.7	5.1	3.2	3.6	103
4.1	4.5	3.0	3.4	104
4.7	5.1	3.2	3.6	105
4.1	4.5	3.0	3.4	106
4.7	5.1	3.2	3.6	107
5.4	5.9	3.6	4.0	110
←———	+0.65(N-1)	———	→	
9.1	10.0	5.6	6.1	111
←———	+0.65(N-1)	———	→	
5.9	6.5	4.3	4.7	112
←———	+0.65(N-1)	———	→	

1904F INSTRUCTION TIMES μ Se

-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's
20.6	23.8	19.6	22.4
3.9	4.2	3.8	4.0
3.2	3.5	3.1	3.3
3.9	4.2	3.8	4.0
3.2	3.5	3.1	3.3
3.9	4.2	3.8	4.0
3.2	3.5	3.1	3.3
3.9	4.2	3.8	4.0
3.2	3.5	3.1	3.3
3.7	4.6	3.5	4.0
4.0	4.6	3.7	3.9
3.7	4.6	3.5	4.0
4.0	4.6	3.7	3.9
3.7	4.6	3.5	4.0
4.0	4.6	3.7	3.9
4.3	5.1	4.1	4.6
4.6	5.1	4.4	4.6
4.5	4.9	4.3	4.5
5.2	5.5	5.1	5.3
2.3	2.5	2.3	2.5
2.8	3.6	2.7	3.2
3.3	4.4	2.9	3.4
2.8	3.6	2.7	3.2
3.3	4.4	2.9	3.4
2.8	3.6	2.7	3.2
3.3	4.4	2.9	3.4
2.8	3.6	2.7	3.2
3.3	4.4	2.9	3.4
3.5	4.5	3.3	3.8
←———	+0.65(N-1)	———	→
5.8	7.4	5.3	5.8
←———	+0.65(N-1)	———	→
4.3	5.2	4.1	4.5
←———	+0.65(N-1)	———	→

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1904E INSTRUCTION TIMES μSecs

-RSU -ACC's	+RSU -ACC's	-RSU +ACC's	+RSU +ACC's	ORDER
9.2	10.0	5.6	6.1	113
←———	+0.65(N-1)	———	→	
8.6	9.2	6.7	7.2	114
←———	+0.82N	———	→	
9.9	11.0	6.9	7.4	115
←———	+0.82N	———	→	
26.6	29.0	23.0	24.3	116
+7.8(N-1)	+8.4(N-1)	+7.8(N-1)	+8.3(N-1)	
4.9	5.3	4.9	5.3	117
4.7	5.1	3.2	3.6	120
4.6	5.0	3.6	4.0	121
4.7	5.1	3.2	3.6	122
2.4	2.6	2.4	2.6	123
9.2	9.6	8.2	8.5	124
3.0	3.3	3.0	3.3	125
16.2	18.0	15.5	16.3	126
+3.6(N-1)	+3.8(N-1)	+3.6(N-1)	+3.8(N-1)	
10.6	12.0	9.1	10.0	127
+1.8(N-1)	+1.9(N-1)	+1.8(N-1)	+1.9(N-1)	
10.1	10.5	9.0	9.4	170N=1
5.7	5.8	4.6	4.7	170N≠1
4.2	4.3	3.7	3.7	171
9.0	9.2	30.0	32.7	172-FPU
17.2	17.4	38.0	40.9	172+FPU
5.4	6.5	5.4	6.5	173
10.8	11.4	9.1	9.4	174
4.7	4.8	4.2	4.2	177
7.2	7.5	32.8	36.4	INTERRUPTS -FPU
+7.3	———	→		+FPU
+6.1	———	→		MACRO INTS

1904F INSTRUCTION TIMES μ Secs

-RSU -ACC'S	+RSU -ACC'S	-RSU +ACC'S	+RSU +ACC'S
5.8	7.4	5.3	5.8
←———	+0.65(N-1)	———	→
6.7	7.4	6.5	6.9
←———	+0.82N	———	→
7.2	8.5	6.6	7.1
←———	+0.82N	———	→
23.0	25.5	22.0	23.4
+7.4(N-1)	+8.0(N-1)	+7.4(N-1)	+8.0(N-1)
4.5	4.8	4.5	4.8
3.3	4.4	2.9	3.4
3.5	4.3	3.3	3.8
3.3	4.4	2.9	3.4
2.0	2.5	2.0	2.5
7.9	8.6	7.8	8.3
2.6	3.1	2.6	3.1
13.4	14.9	13.0	14.1
+2.5(N-1)	+2.7(N-1)	+2.5(N-1)	+2.7(N-1)
9.1	10.2	9.0	9.5
+1.6(N-1)	+1.7(N-1)	+1.6(N-1)	+1.7(N-1)
6.6	7.7	6.4	7.3
4.4	5.0	4.3	4.7
3.8	4.7	3.5	3.9
7.5	9.5	22.0	28.0
13.5	16.5	28.0	35.0
4.8	6.1	4.8	6.1
9.1	10.1	8.7	9.1
4.0	4.9	3.7	4.1
5.4	6.4	23.0	29.0
9.4	10.7	28.0	34.5
+7.0	+8.0	+7.0	+8.0

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ACW	1535		

Cont:- From 30₇

1904E INSTRUCTION TIMES μ Secs

Store Mode

-RSU -ACC's	+RSU -ACC's	-RSU +ACC'S	+RSU +ACC'S	ESM CORRECTION FACTORS
+1.1	+1.3	+1.0	+1.0	060
+1.1	+1.3	+1.0	+1.0	062
+1.1	+1.3	+1.0	+1.0	064
+2.2	+2.5	+2.1	+2.1	066
				RJM CORRECTION FACTORS
+1.8	+2.0	+1.8	+2.0	050
+2.2	+2.6	+2.2	+2.5	051
+1.8	+2.0	+1.8	+2.0	052
+2.2	+2.6	+2.2	+2.5	053
+1.8	+2.0	+1.8	+2.0	054
+2.2	+2.6	+2.2	+2.5	055
+1.8	+2.0	+1.8	+2.0	056
+2.2	+2.6	+2.2	+2.5	057
+1.8	+2.0	+1.8	+2.0	060
+2.3	+2.6	+2.3	+2.5	061
+1.8	+2.0	+1.8	+2.0	062
+2.3	+2.6	+2.3	+2.5	063
+1.8	+2.0	+1.8	+2.0	064
+2.3	+2.6	+2.3	+2.5	065
+1.8	+2.0	+1.8	+2.0	066
+2.3	+2.6	+2.3	+2.5	067
+3.4	+3.4	+3.4	+3.4	070
+3.7	+3.9	+3.7	+3.9	071
+1.3	+1.2	+0.8	+0.7	072
+2.0	+2.2	+2.0	+2.0	074
+2.2	+2.8	+2.2	+2.5	075
				HESITATION TIMES
8.5	9.4	8.5	9.4	CH IN
8.1	9.0	8.1	9.0	CH OUT
14.4	15.0	14.4	15.0	WD IN
15.4	15.3	15.4	15.3	WD OUT
←——— +7.2 ———→				CWR
←——— +4.7 ———→				M/C

1904F INSTRUCTION TIMES μ Secs

-RSU -ACC'S	+RSU -ACC'S	-RSU +ACC'S	+RSU +ACC'S
+1.2	+1.6	+0.9	+0.9
+1.2	+1.6	+0.9	+0.9
+1.2	+1.6	+0.9	+0.9
+2.1	+2.3	+2.1	+2.1
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
+3.4	+3.4	+3.4	+3.4
+3.3	+3.8	+3.3	+3.7
+1.0	+1.3	+0.8	+0.8
+2.0	+2.0	+2.0	+2.0
+1.9	+2.3	+1.9	+2.3
4.6	6.1	4.6	6.1
4.9	6.3	4.9	6.3
10.9	12.0	10.9	12.0
11.2	12.6	11.2	12.6
+2.8	+3.8	+2.8	+3.8
←——— +4.7 ———→			

WCC 01/30₂

SUB	155		
ACW	1635		

1905E

F.P.U. TIMES

1.8 μ s Store - Slow F.P.U.

		μ s
PHASE 1		
FETCH INSTRUCTION	FROM STORE DIRECT	1.8
	FROM STORE VIA SEU	1.9
PHASE 2		
MODIFY N ADDRESS	ACC. IN STORE DIRECT	1.8
	ACC. IN STORE VIA SEU	1.9
	ACC. IN H/A ACC.	1.0
PHASE 3 (130-136)		
LOAD DOUBLE LENGTH OPERAND		6.1
PHASE 3 (137)		
UNLOAD DOUBLE LENGTH OPERAND		6.1

PHASE 4

EXECUTION TIMES

	130 E'code	131 E'code	132	133	134	135	136 0	137 0
MIN/N			7	7	24	45		
MAX/N			44	44	25	49		
MIN/U			7	7	24	46		
MAX/U			79	79	27	84		

/N= NORMALISED OPERANDS } ASSUME ANSWER
/U= UNNORMALISED OPERANDS } HAS TO BE
MIN= MINIMUM CALCULATION } NORMALISED
MAX= MAXIMUM CALCULATION }

WGC 01/304

WGC 01/

SUB	155		
ACW	1535	.	

1905F

750 n Sec Store - Fast F.P.U.

PHASE 1		μ Sec
FETCH INSTRUCTION	FROM STORE DIRECT	1.15
	FROM STORE VIA SEU	1.45
PHASE 2		
MODIFY N ADDRESS	ACC.IN STORE DIRECT	1.15
	ACC.IN STORE VIA SEU	1.45
	ACC.IN H/A ACC.	0.9
PHASE 3 (130-136) (LOAD)		
LOAD DOUBLE LENGTH	FROM STORE DIRECT	4.0
OPERAND	FROM STORE VIA SEU	4.5
PHASE 3 (137) (UNLOAD)		
UNLOAD DOUBLE LENGTH	TO STORE DIRECT	4.0
OPERAND	TO STORE VIA SEU	4.5

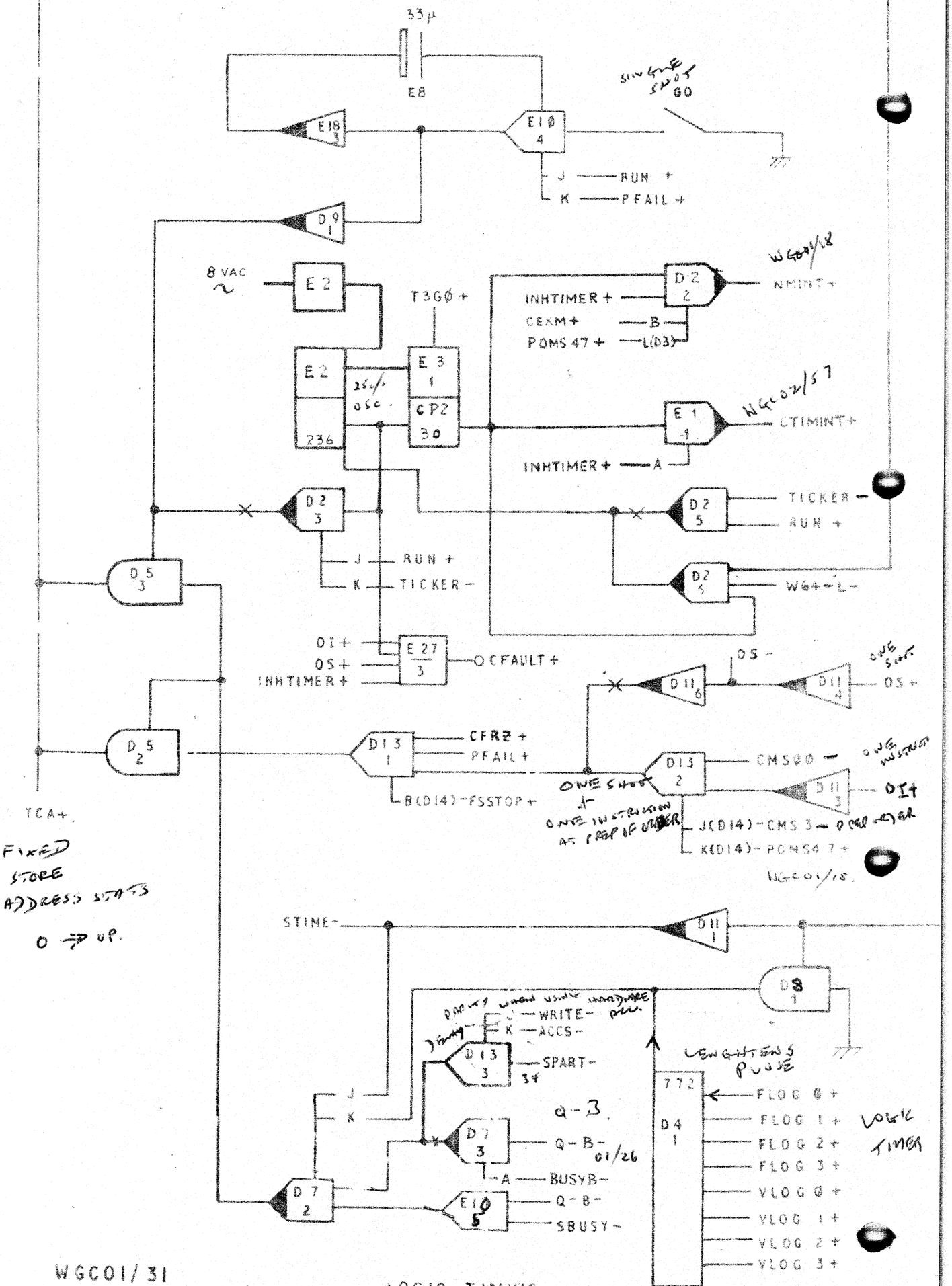
PHASE 4

EXECUTION TIMES μ Secs.

	130	131 E'code	132	133	134	135	136 0	137 0
MIN/N			2.5	2.5	12	26		
MAX/N			11	11	12	28		
MIN/U	1.3		2.5	2.5	12	28		
MAX/U	23		33	33	55	49		

/N NORMALISED OPERANDS
/U UNNORMALISED OPERANDS
MIN MINIMUM CALCULATION
MAX MAXIMUM CALCULATION

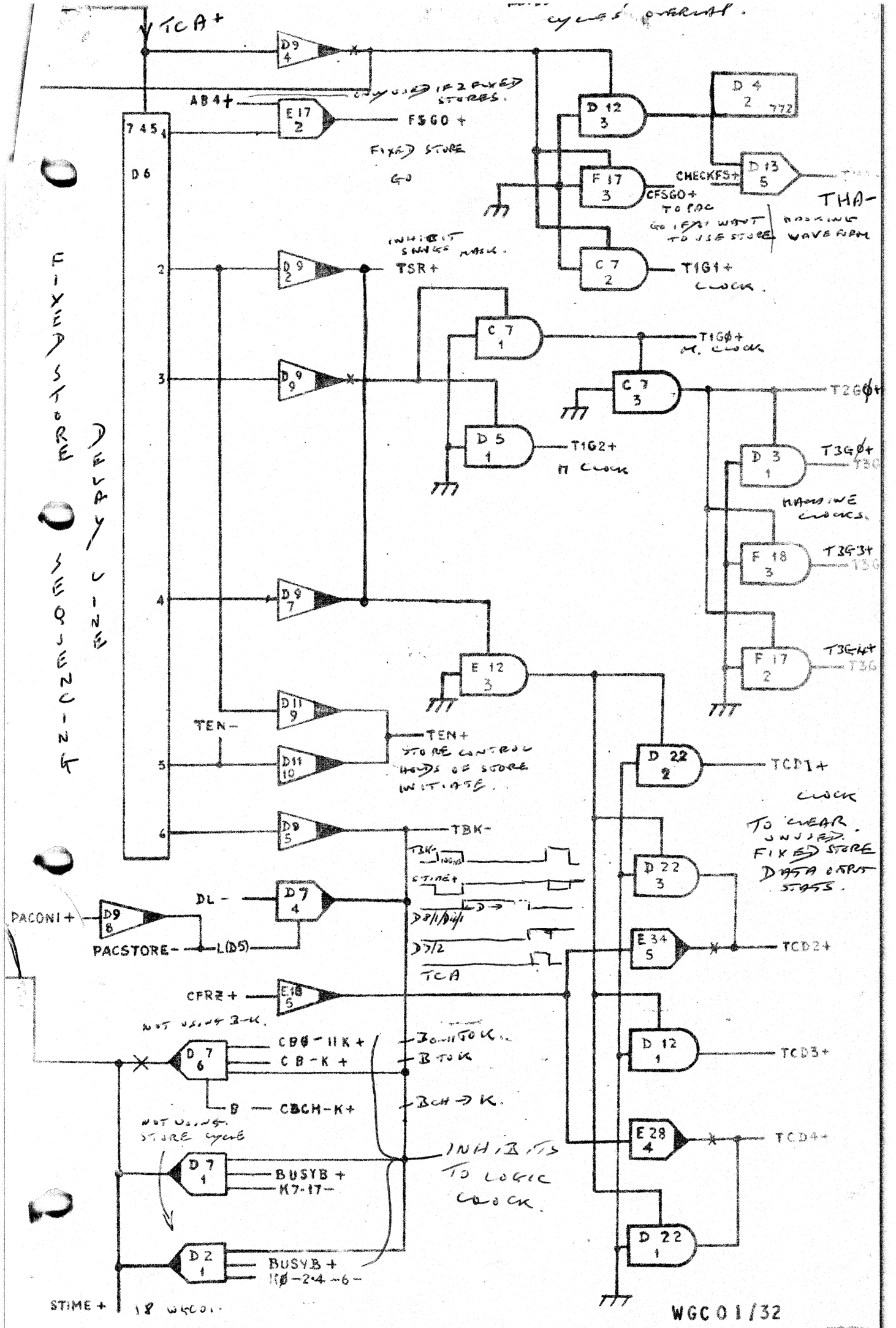
} ASSUME ANSWER HAS TO BE NORMALISED



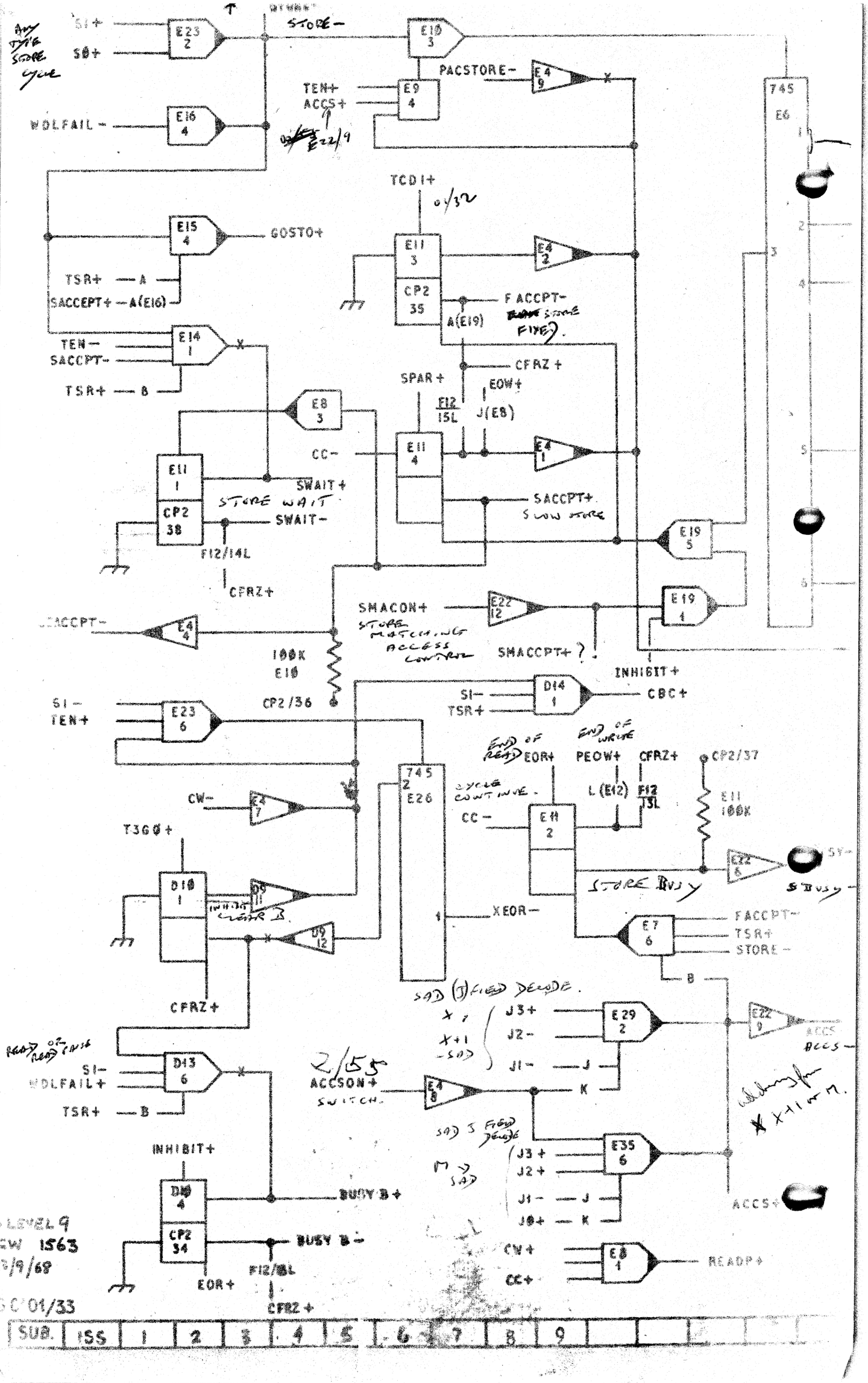
WGC01/31

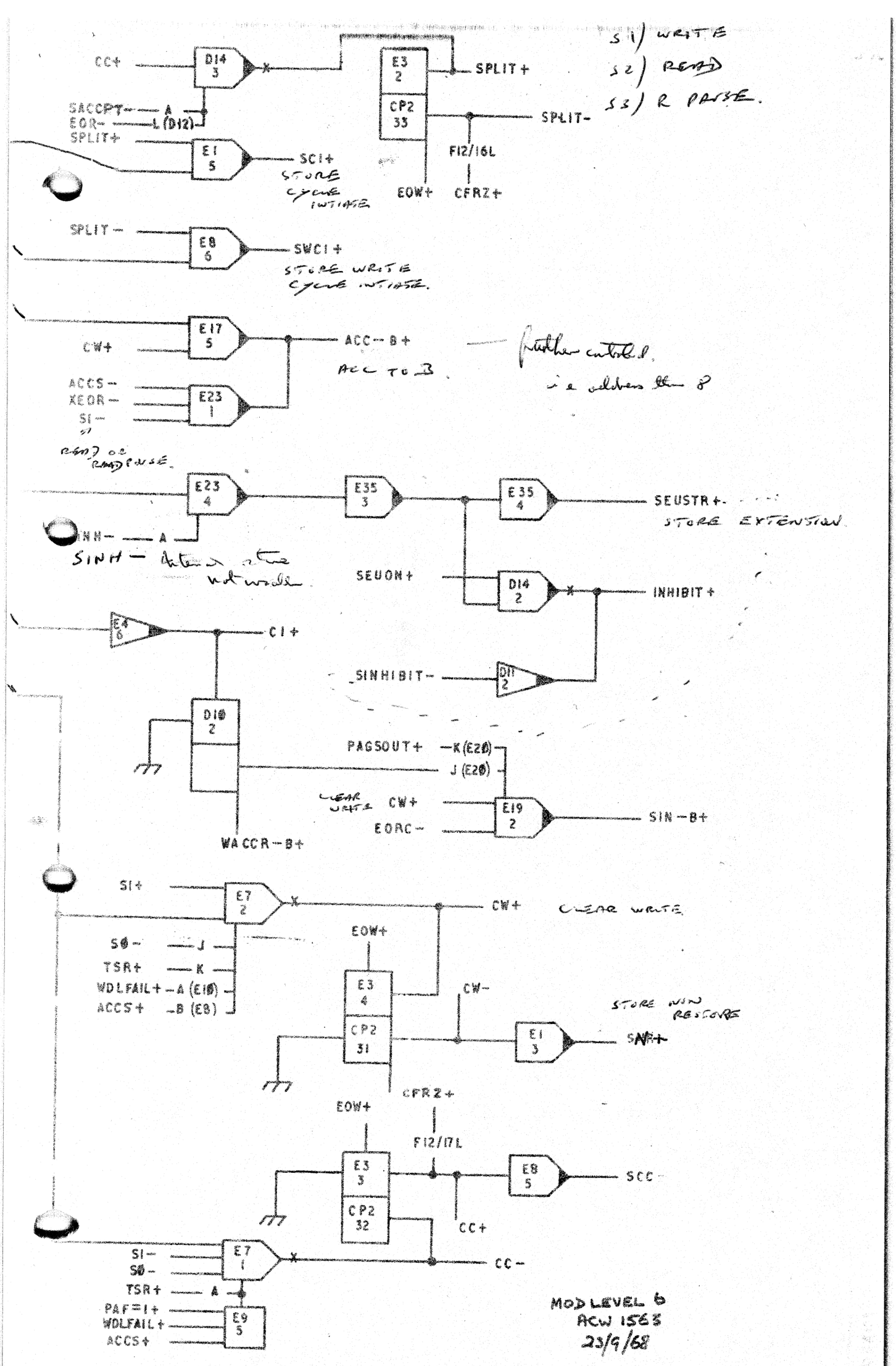
LOGIC TIMING

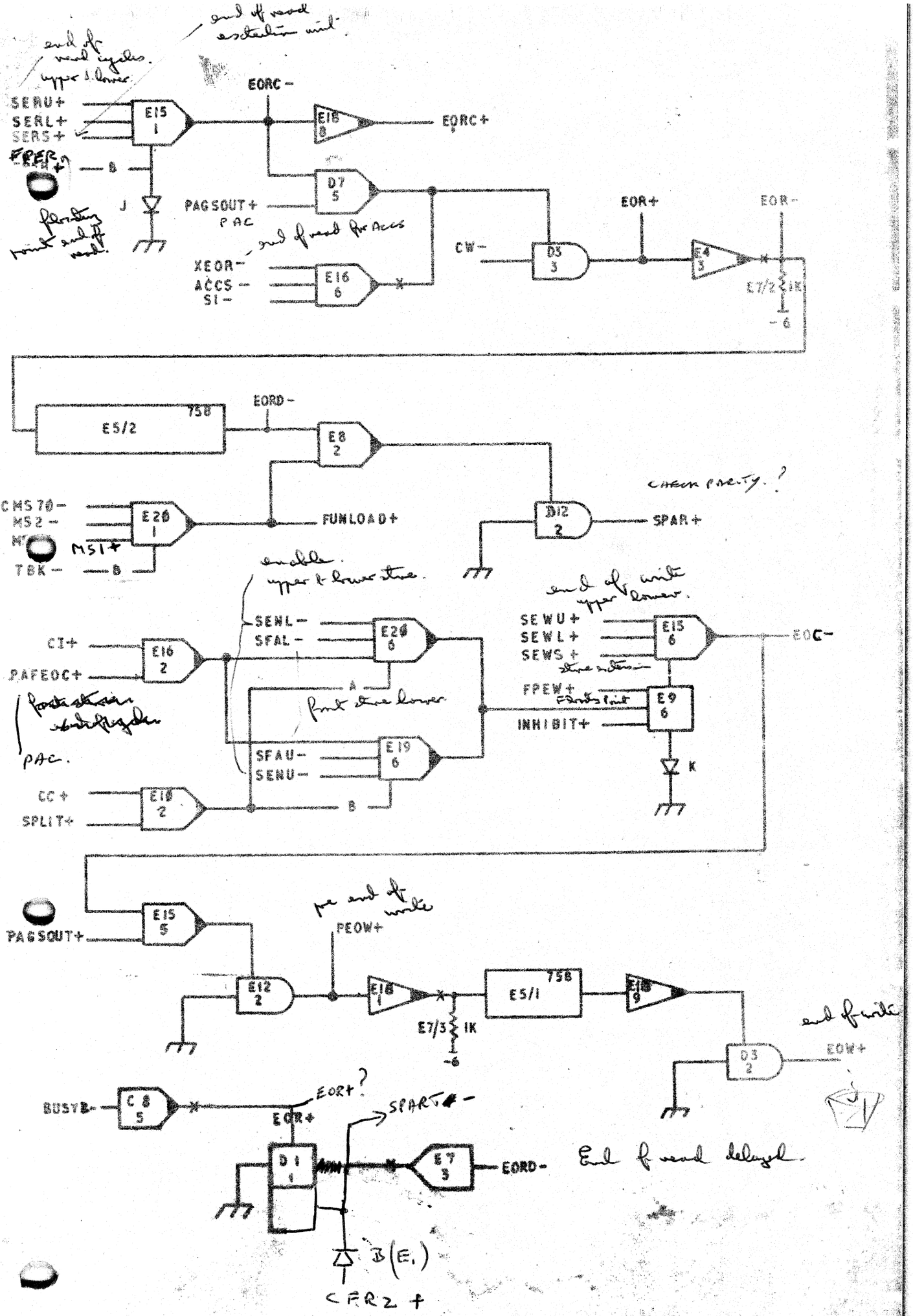
SUB	ISS	1	2	3	4	5	6	7							
ACW	0836	0898	0929	0964	0996	1507	1519	1549							
DATE	11/9/67	21/11/67	19/1/68	18/3/68	8/4/68	23/4/68	17/5/68	12/8/68							

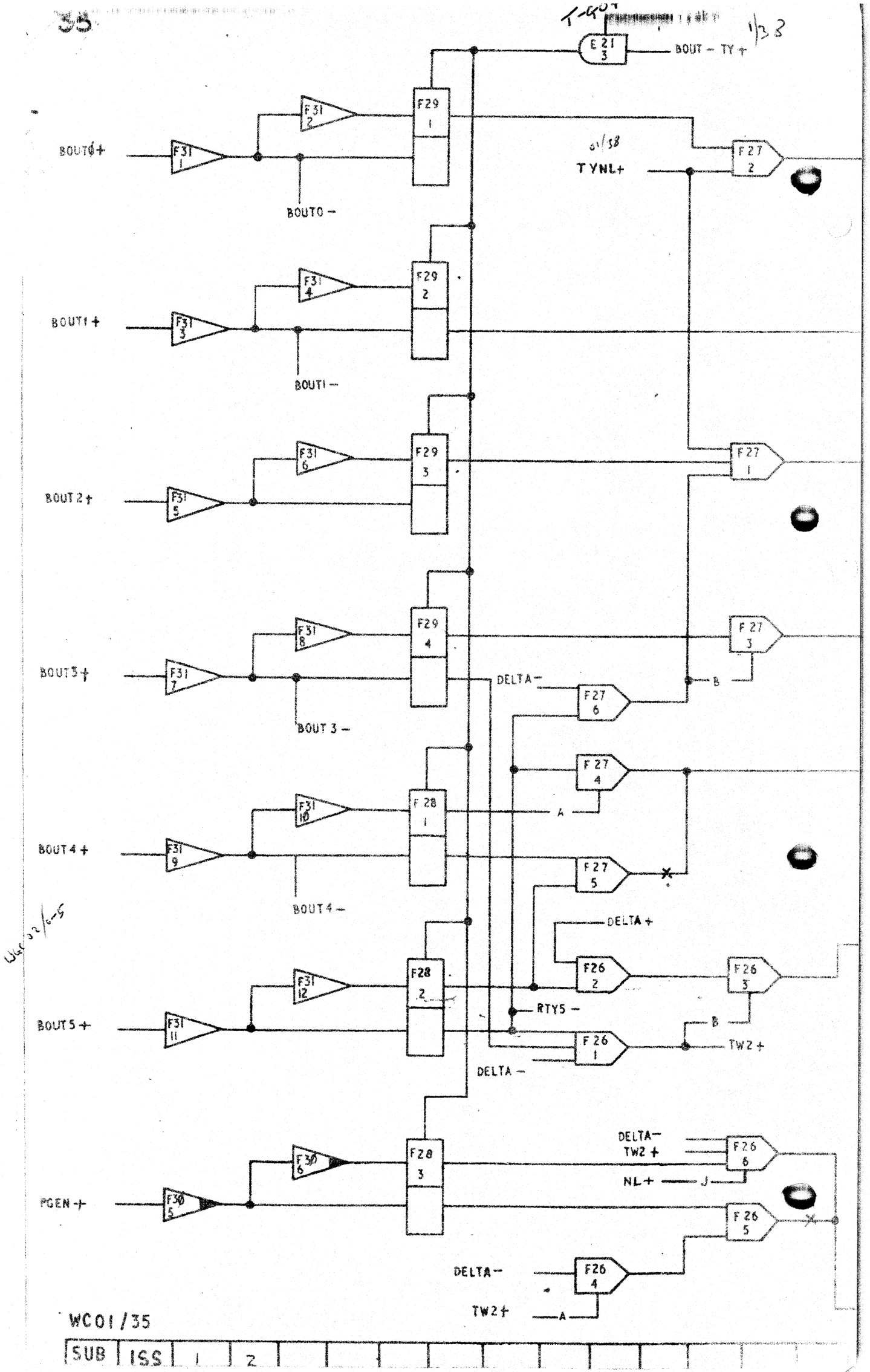


SUB	ISS	1	2	3	4	5	6	7							
ADDR	0836	0876	0898	0929	0964	0997	1507	1535							


Any TYPE STORE cycle
SI+
SØ+
E23 2
STORE-
E10 3
PACSTORE-
E4 9
TEN+
ACCS+
E9 4
WDLFAIL-
E16 4
E22/9
TCD1+
0/32
E15 4
GOSTO+
TSR+ — A
SACCEPT+ — A(E16)
E11 3
E4 2
CP2 35
FACCPT-
A(E19)
FIXED.
TEN-
SACCPT-
E14 1
TSR+ — B
SPAR+
F12 15L
EOW+
J(E8)
CFRZ+
E8 3
CC-
E11 4
E4 1
E11 1
CP2 38
SWAIT+
STORE WAIT
SWAIT-
SACCPT+.
SLOW STORE
F12/14L
CFRZ+
E19 5
SMACON+
E22 12
E19 1
STORE MATCHING ACCESS CONTROL
SMACCPT+ ?
INHIBIT+
100K E10
CP2/36
SI-
TEN+
E23 6
SI-
TSR+
D14 1
CBC+
END OF READ
EOR+
END OF WRITE
PEOW+
CFRZ+
CP2/37
745 2 E26
CW-
E4 7
CYCLE CONTINUE.
CC-
E11 2
L(E12)
F12 13L
E11 100K
T3GØ+
D10 1
D9 11
INHIBIT CYCLE 2
D9 12
STORE BUSY
E22 6
SY-
STBUSY
XEOR-
E7 6
FACCPT-
TSR+
STORE-
B
CFRZ+
SAD (J) FIELD DECODE.
X, X+1 -SAD
J3+
J2-
J1- — J
E29 2
E22 9
ACCS
BCCS-
READ OR READ/WRITE
SI-
WDLFAIL+
TSR+ — B
D13 6
2/55
ACCSON+ SWITCH.
E4 8
K
X+1 INTO M.
SAD 5 FIELD DECODE
M = SAD
J3+
J2+
J1- — J
J0+ — K
E35 6
ACCS+
INHIBIT+
D10 4
CP2 34
BUSY B+
BUSY B-
EOR+
F12/8L
CFRZ+
CW+
CC+
E8 1
READP+
LEVEL 9
CW 1563
23/9/68
GC 01/33
SUB. ISS 1 2 3 4 5 6 7 8 9

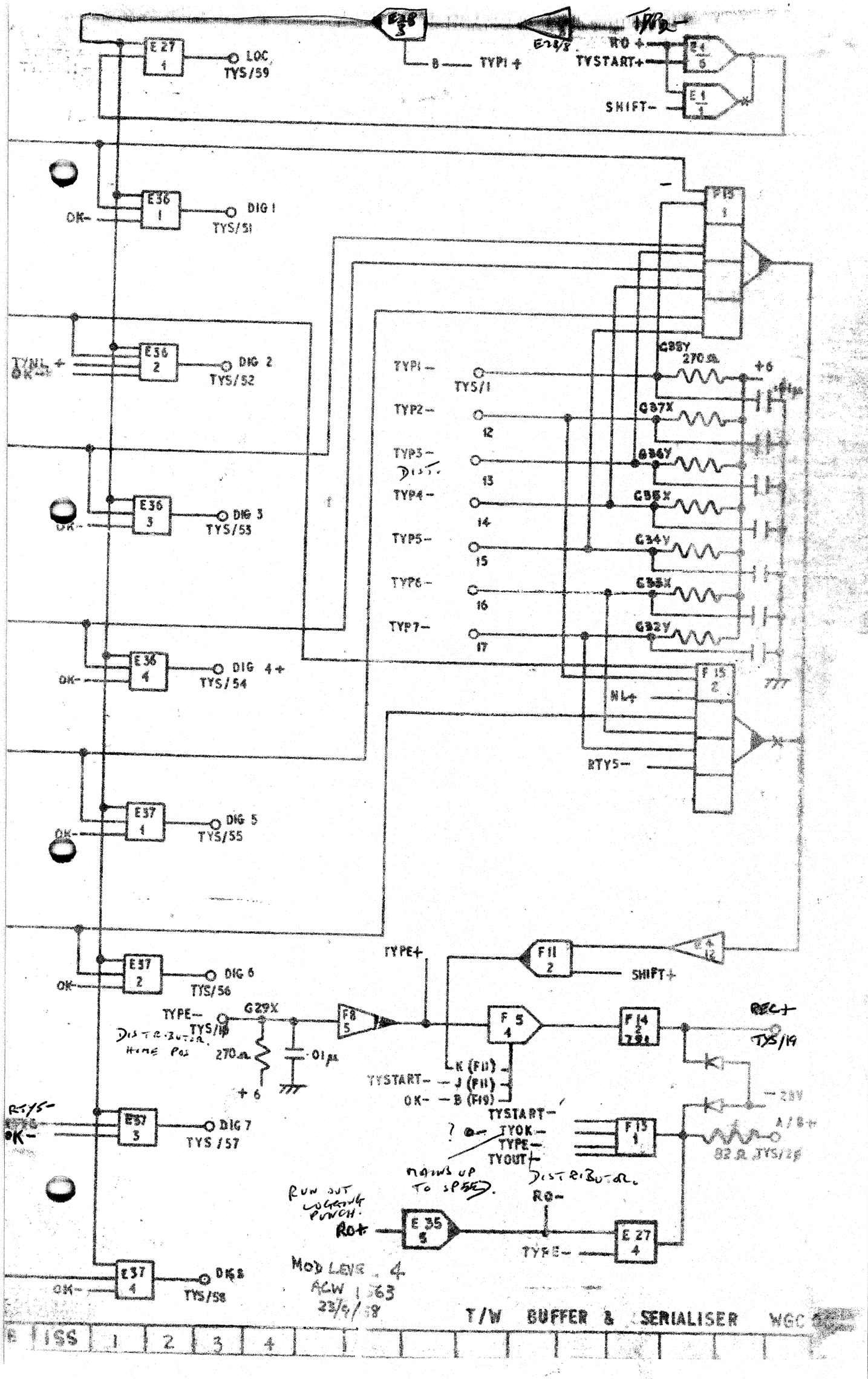

S1) WRITE
S2) READ
S3) R PARSE.
CC+
D14 3
E3 2
SPLIT+
CP2 33
SPLIT-
SACCPT- A
EOR- L(D12)
SPLIT+
E1 5
SC1+
STORE CYCLE INITIATE
F12/16L
EOW+
CFRZ+
SPLIT-
E8 6
SWC1+
STORE WRITE CYCLE INITIATE.
E17 5
CW+
ACC-B+
ACC TO B.
further controls
i.e. address the S
ACCS-
XEOR-
SI-
E23 1
S1
READ OR RESPONSE.
E23 4
E35 3
E35 4
SEUSTR+
STORE EXTENSION
INH- A
SINH - Inhibit store network
SEUON+
D14 2
INHIBIT+
E4 6
C1+
SINHIBIT-
D11 2
D10 2
PAGSOUT+ K(E20)
J(E20)
CLEAR WRITE CW+
EORC-
E19 2
SIN-B+
WACCR-B+
SI+
E7 2
CW+
CLEAR WRITE
EOW+
S0- J
TSR+ K
WDLFAIL+ A(E10)
ACCS+ B(E8)
E3 4
CP2 31
CW-
STORE NON RESTORE
E1 3
SNR+
CFRZ+
EOW+
F12/17L
E3 3
CP2 32
E8 5
SCC-
CC+
SI-
S0-
E7 1
CC-
TSR+ A
PARITY+
WDLFAIL+
ACCS+
E9 5
MOD LEVEL 6
ACW 1565
23/9/68

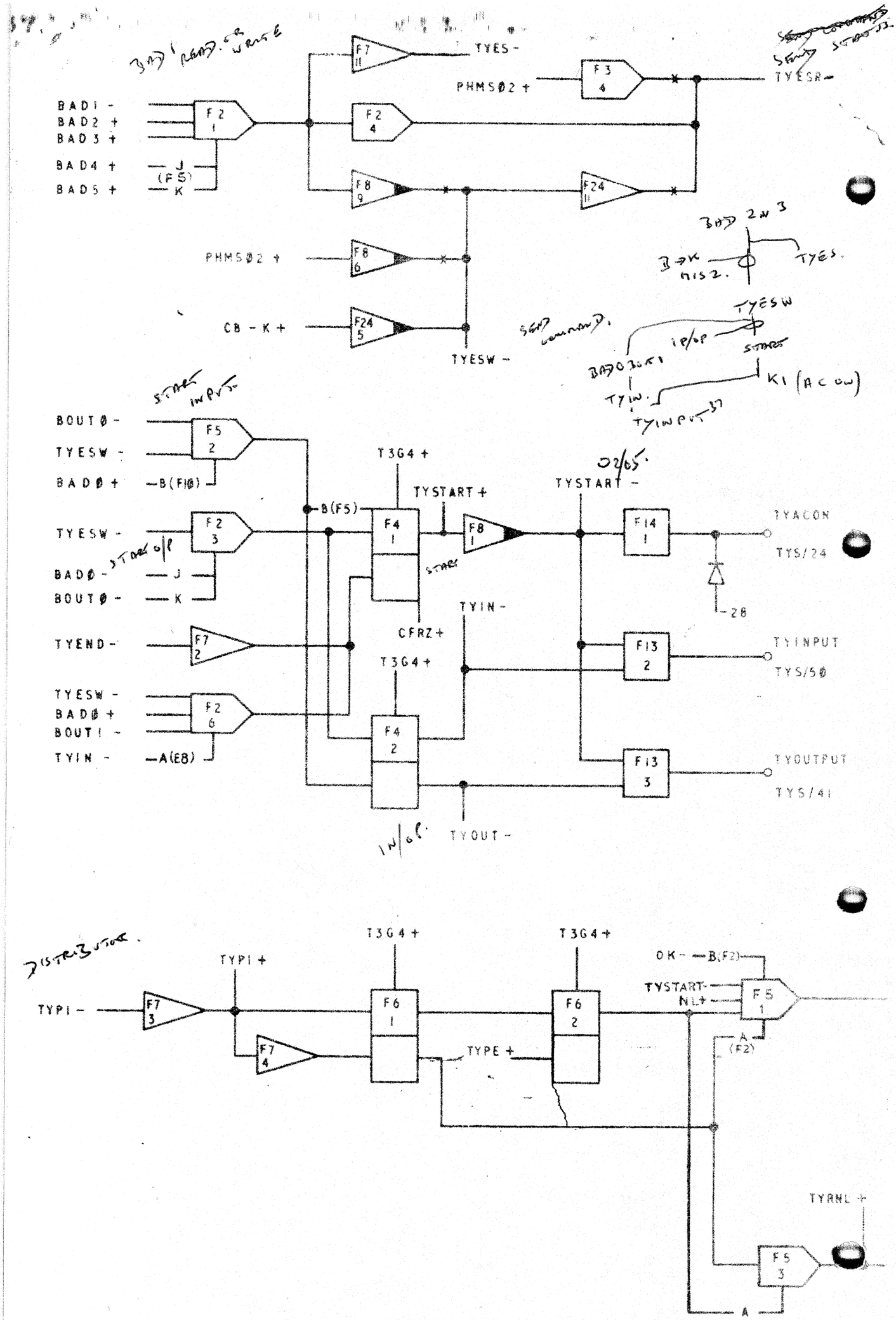

end of word establish unit.
end of read cycles upper & lower.
EORC-
SERU+
SERL+
SERS+
E15 1
E18 8
EORC+
FRER+
B
J
floating point end of word.
D7 5
PAGSOUT+
PAC
end of read for ACCS
XEOR-
ACCS-
S1-
E16 6
CW-
D3 3
EOR+
E4 3
EOR-
E7/2 1K
-6
E5/2
75B
EORD-
E8 2
CMS70-
MS2-
MS1+
TBK-
B
E20 1
FUNLOAD+
D12 2
SPAR+
check parity?
enable upper & lower stre.
end of write upper lower.
SENL-
SFAL-
E20 6
CI+
PAFEOC+
E16 2
A
first stre lower
SFAU-
SENU-
E19 6
CC+
SPLIT+
E18 2
B
PAC.
SEWU+
SEWL+
SEWS+
E15 6
EOC-
FPEW+
E9 6
INHIBIT+
K
PAGSOUT+
E15 5
pe end of write
PEOW+
E12 2
E18 1
E7/3 1K
-6
E5/1
75B
E18 9
end of write
D3 2
EOW+
BUSYB-
C8 5
EOR+?
EOR+
SPARE-
D1 1
E7 3
EORD-
End of word delayed
B(E1)
CFR2+
W.G.C.01/34
SUB.
ISS.
1
2
3
L.C.W.
0851
0876
0898
0949
DATE

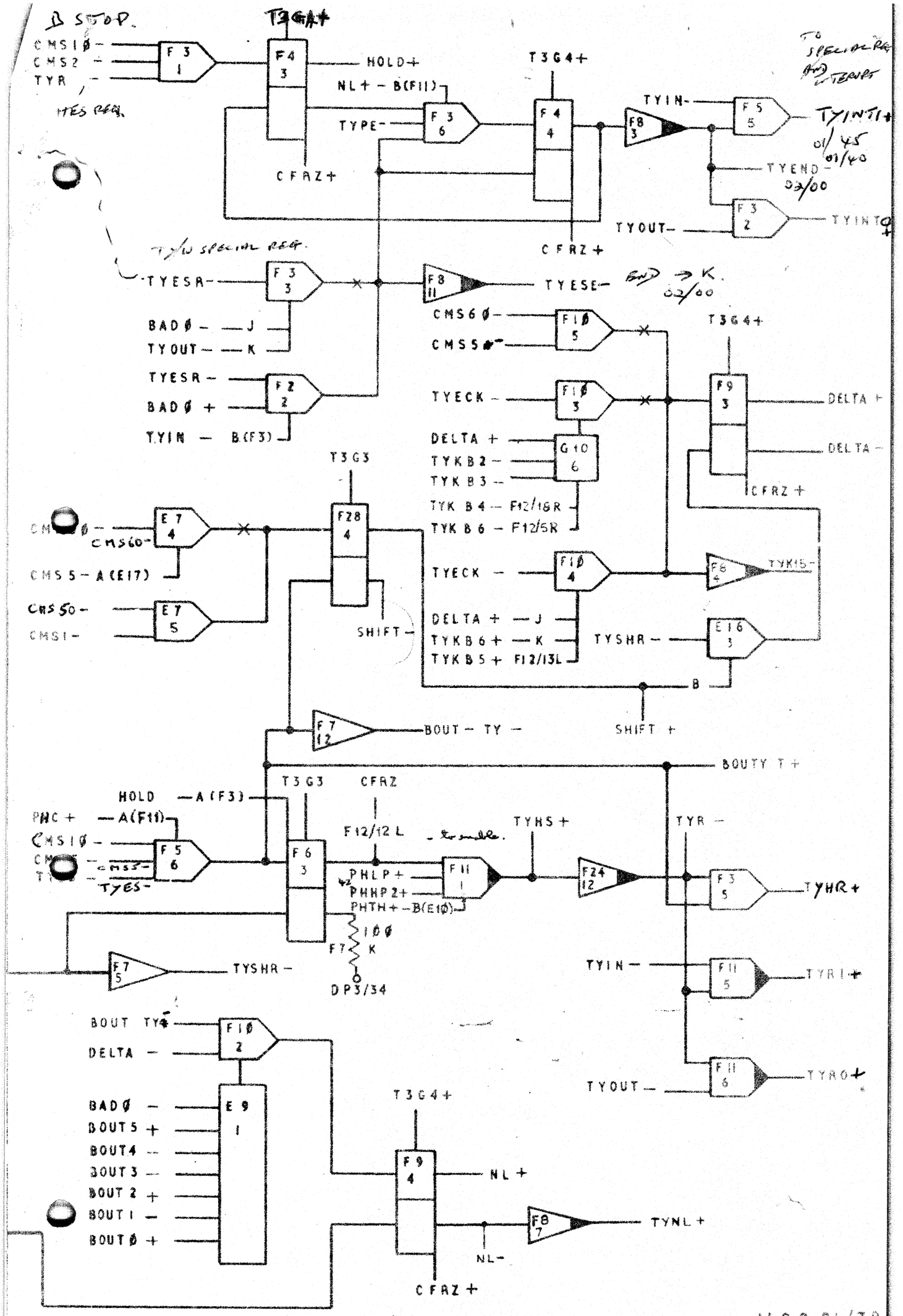


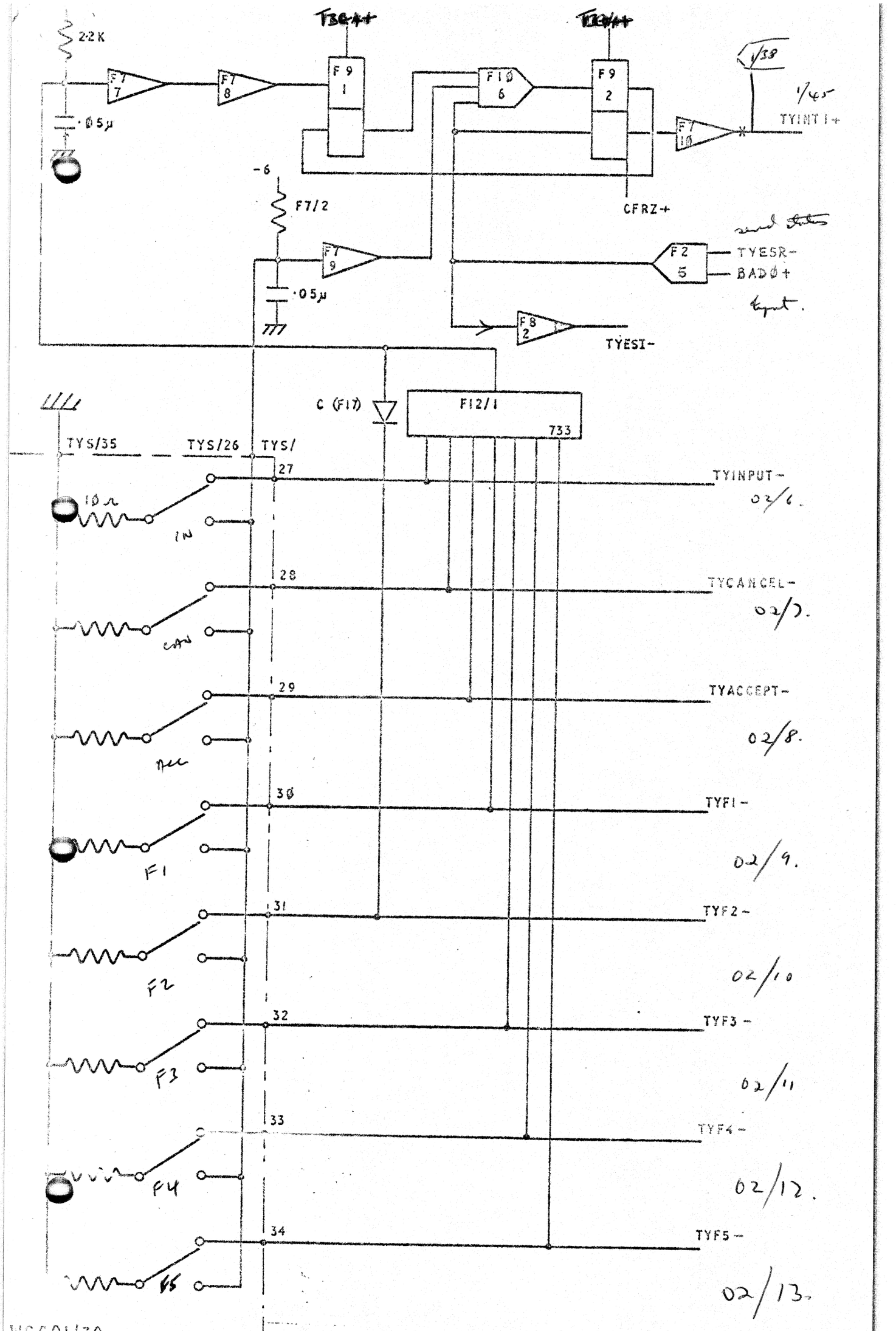
WC01/35

SUB	ISS	1	2


E27 1
LOC
TYS/59
E38 3
E28/8
TYP1+
RO+
TYSTART+
SHIFT-
E1 6
E1 4
E36 1
OK-
DIG 1
TYS/51
F13 1
E36 2
TYN1+
OK-
DIG 2
TYS/52
TYP1-
TYS/1
TYP2-
12
TYP3-
DIST.
13
TYP4-
14
TYP5-
15
TYP6-
16
TYP7-
17
G38Y 270Ω
+6
G37X
G36Y
G35X
G34Y
G33X
G32Y
E36 3
OK-
DIG 3
TYS/53
E36 4
OK-
DIG 4+
TYS/54
F15 2
NL4
RTY5-
E37 1
OK-
DIG 5
TYS/55
E37 2
OK-
DIG 6
TYS/56
TYPE+
F11 2
SHIFT+
TYPE-
TYS/18
DISTRIBUTOR HOME POS
G29X
270Ω
·01μ
+6
F8 5
F5 4
F14 2 7 9 1
REC+
TYS/19
K (F11)
TYSTART-
J (F11)
OK-
B (F19)
TYSTART-
TYOK-
TYPE-
TYOUT+
F15 1
-28V
A/B+
82Ω TYS/18
RTY5-
E37 3
OK-
DIG 7
TYS/57
RUN OUT PUNCH
RO+
E35 5
RO-
TYPE-
E27 4
DISTRIBUTOR
E37 4
OK-
DIG 8
TYS/58
MOD LEVEL 4
ACW 1363
23/4/68
T/W BUFFER & SERIALISER
ISS 1 2 3 4


BAD 1 READ. or WRITE
BAD1 -
BAD2 +
BAD3 +
BAD4 +
BAD5 +
F2 1
J
(F5)
K
F7 11
TYES -
F2 4
F8 9
F24 11
PHMSØ2 +
F3 4
TYESR -
PHMSØ2 +
F8 6
CB - K +
F24 5
TYESW -
BAD 2 or 3
3 → K
MIS 2.
TYES.
SCAN command.
TYESW
I P/OP
STORE
BADØ 1 or 4
TYIN.
K1 (ACOW)
TYINPUT-37
STORE INPUTS
BOUTØ -
TYESW -
BADØ +
B(FIØ)
F5 2
T3G4 +
TYSTART +
B(F5)
F4 1
F8 1
TYSTART -
02/05.
F14 1
TYACON
TYS/24
-28
TYESW -
BADØ -
BOUTØ -
F2 3
STORE O/P
J
K
STORE
TYIN -
CFRZ +
TYEND -
F7 2
T3G4 +
F13 2
TYINPUT
TYS/5Ø
TYESW -
BADØ +
BOUT1 -
TYIN -
F2 6
A(E8)
F4 2
F13 3
TYOUTPUT
TYS/41
IN/OL
TYOUT -
DISTRIBUTOR.
TYPI +
TYPI -
F7 3
F7 4
T3G4 +
F6 1
TYPE +
T3G4 +
F6 2
OK - B(F2)
TYSTART-
NL+
F5 1
A
(F2)
TYRNL +
F5 3
A

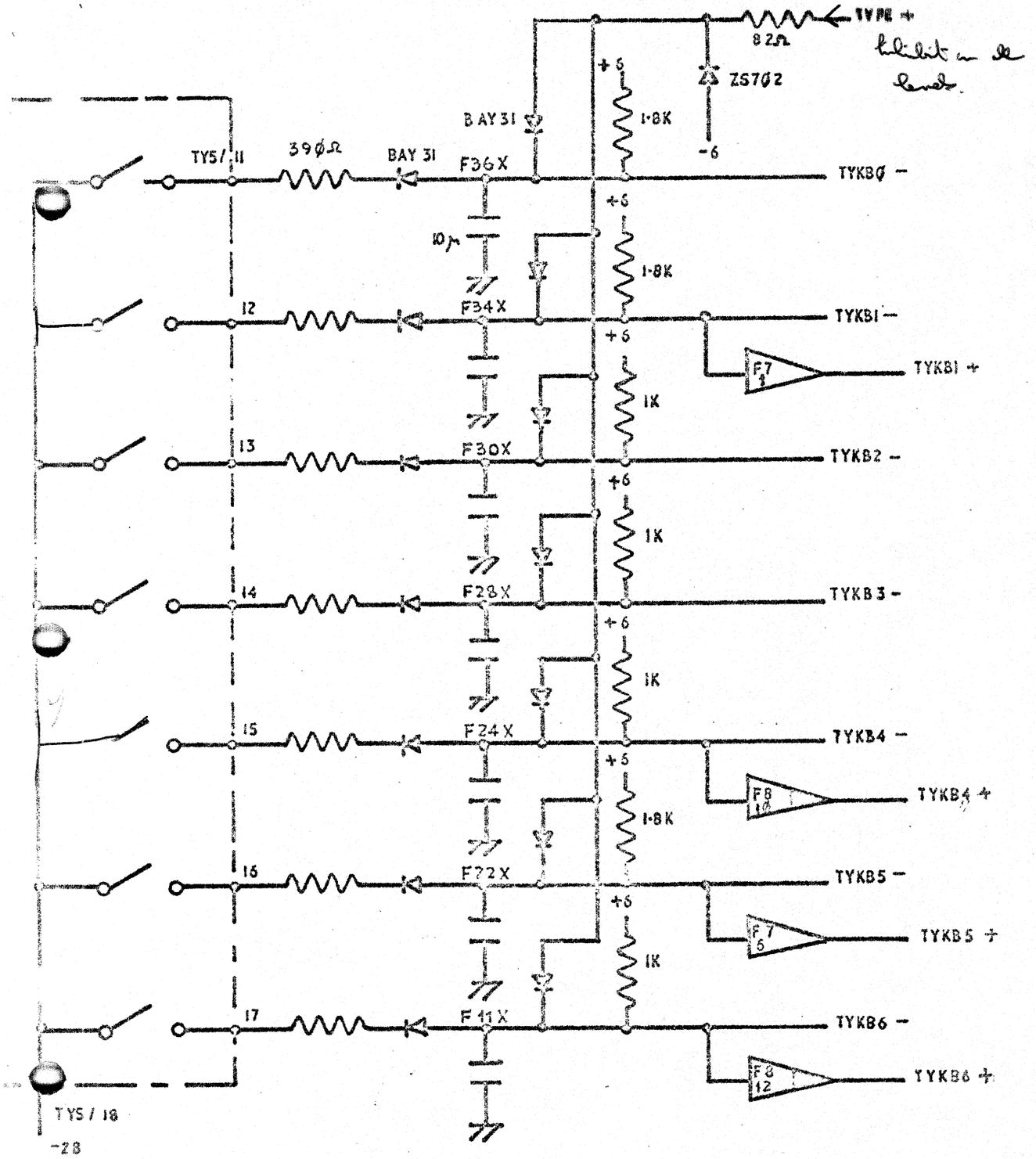

D STOP.
T3G4+
CMS1Ø –
CMS2 –
TYR –
F3 1
F4 3
HOLD+
NL+ – B(F11)
TYPE–
F3 6
T3G4+
F4 4
TYIN–
F8 3
F5 5
TYINTI+
01/45
01/40
TYEND–
02/00
F3 2
TYINTØ+
TYOUT–
CFRZ+
CFRZ+
TO SPECIAL REQ AND INTERRUPT
YES REQ.
T/W SPECIAL REQ.
TYESR–
F3 3
F8 11
TYESE–
END → K.
02/00
BADØ – J
TYOUT – K
TYESR –
BADØ +
FZ 2
TYIN – B(F3)
CMS6Ø–
CMS5Ø–
F1Ø 5
T3G4+
TYECK –
F1Ø 3
F9 3
DELTA +
DELTA –
CFRZ+
DELTA +
TYKB2 –
TYKB3 –
TYKB4 – F12/18R
TYKB6 – F12/5R
G10 6
T3G3
CMSØ –
CMS6Ø–
E7 4
FZ8 4
CMS5 – A(E17)
CMS5Ø –
CMS1 –
E7 5
SHIFT –
TYECK –
F1Ø 4
F8 4
TYK15–
DELTA + – J
TYKB6 + – K
TYKB5 + F12/13L
TYSHR –
E16 3
B
SHIFT +
F7 12
BOUT – TY –
BOUTY T+
T3G3
CFRZ
HOLD – A(F3)
PHC + – A(F11)
CMS1Ø –
CMS5–
TYES–
F5 6
F6 3
F12/12L
PHLP+
PHHP2+
PHTH+ – B(E1Ø)
F11 1
TYHS+
FZ4 12
TYR –
F3 5
TYHR+
1ØØ
F7 K
DP3/34
F7 5
TYSHR –
TYIN –
F11 5
TYR1+
BOUT TY
DELTA –
F1Ø 2
E9 1
BADØ –
BOUT5 +
BOUT4 –
BOUT3 –
BOUT2 +
BOUT1 –
BOUTØ +
T3G4+
F9 4
NL+
NL–
F8 7
TYNL+
CFRZ+
TYOUT –
F11 6
TYRØ+
T/W CONTROL
W.G.C. 01/38.

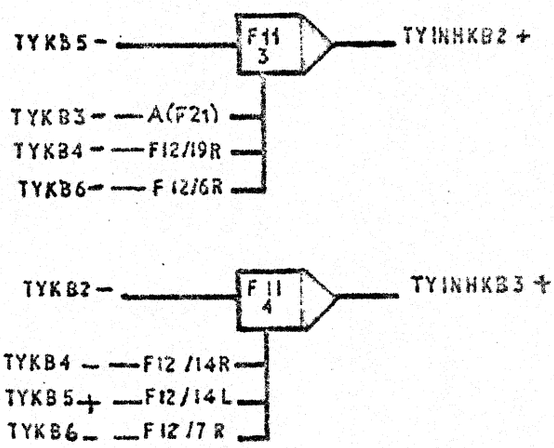


WGC01/39

T/W PUSH BUTTONS

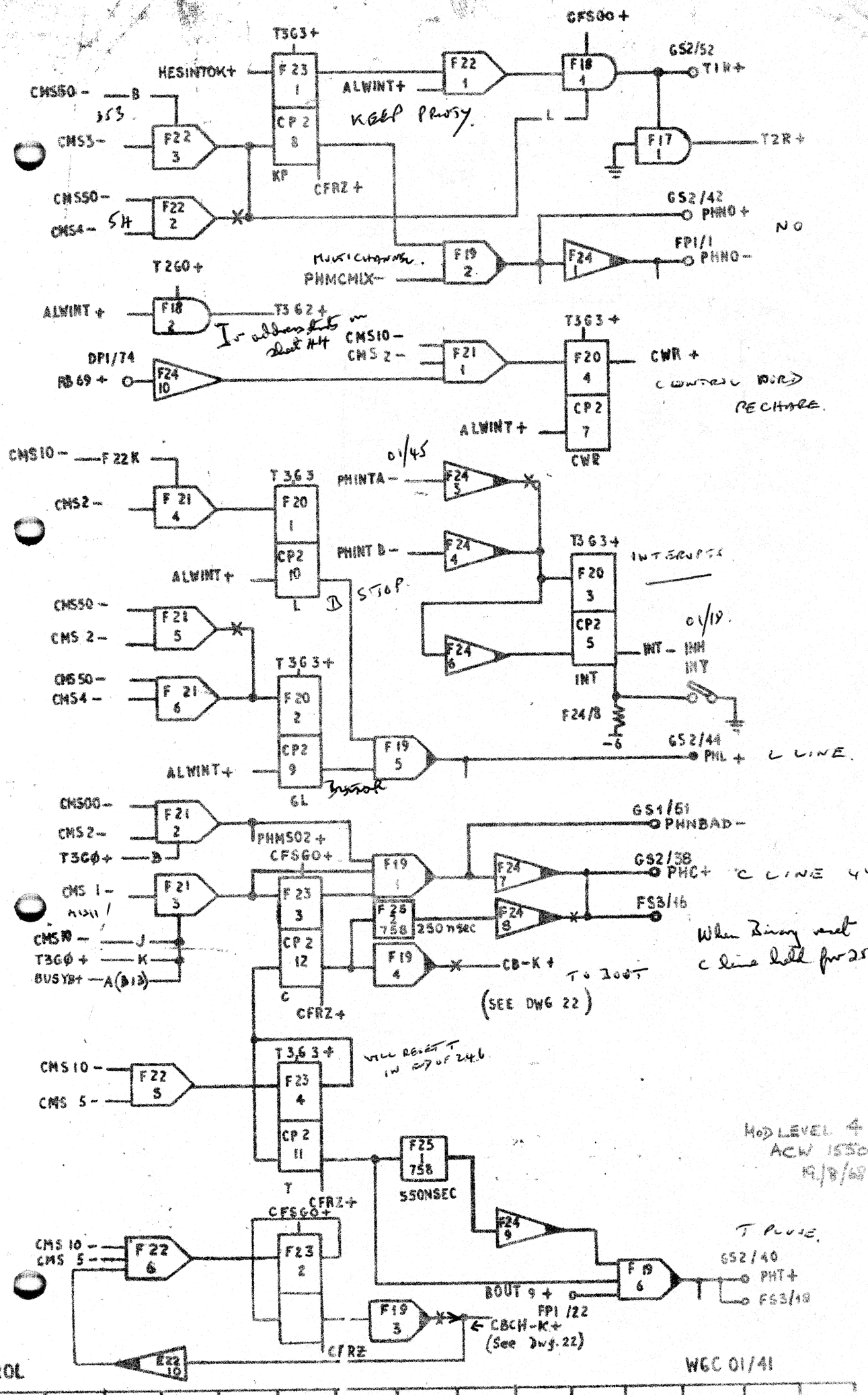
SUB	ISS

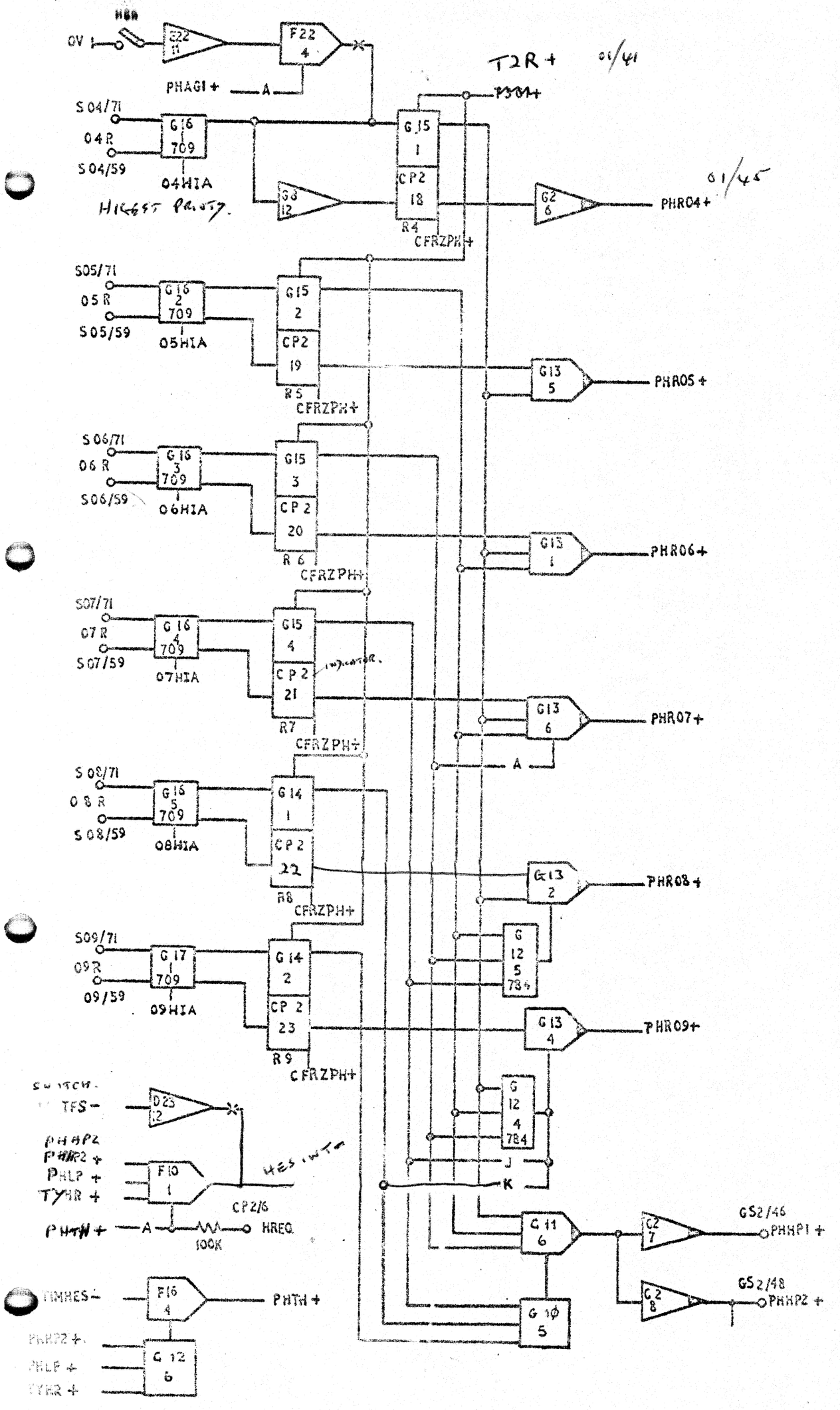


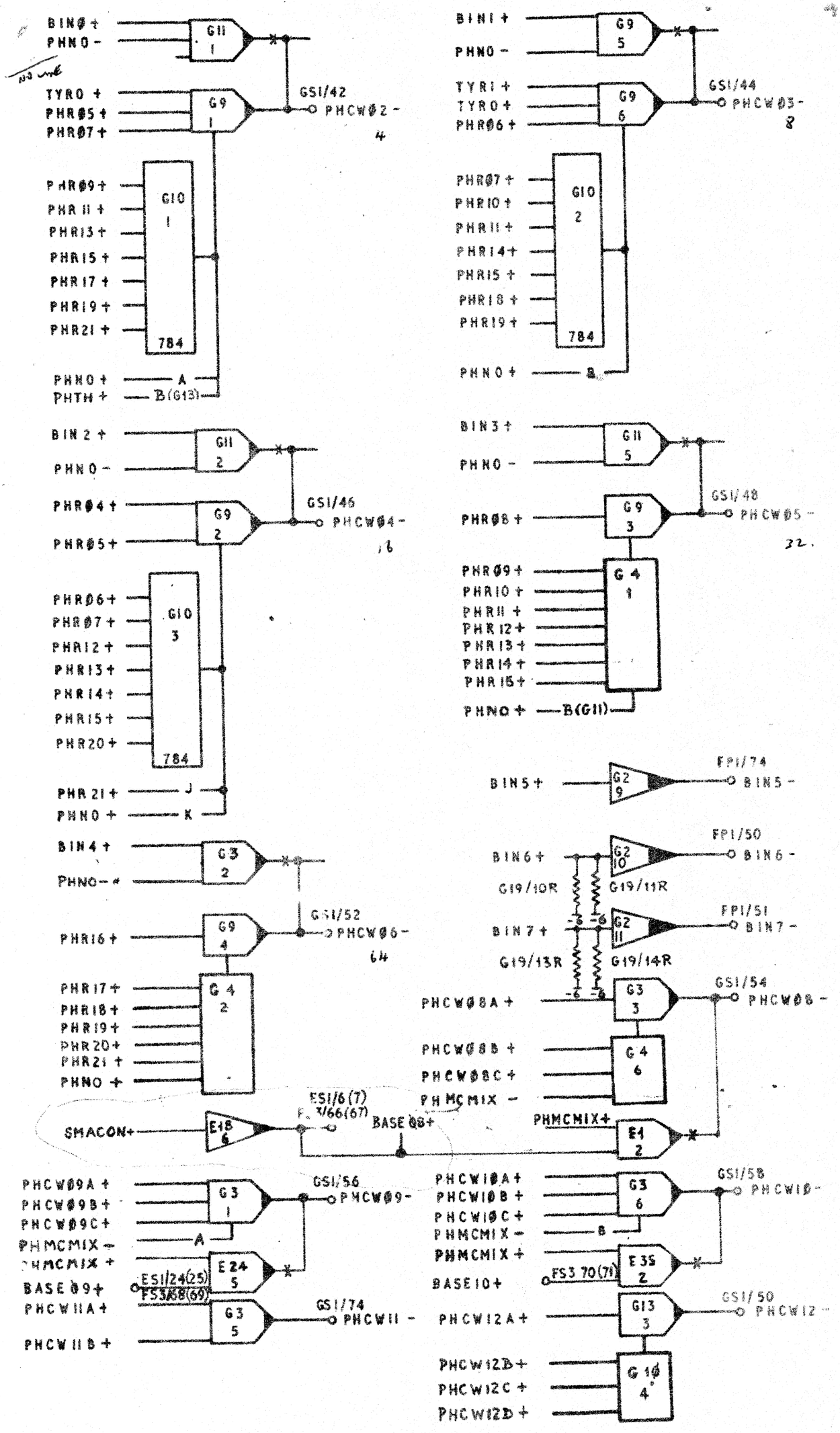


T/W KEYBOARD WGCØ1/4Ø

[illegible]	ISS	1																
ACW	0836	0929																


CFSGO+
T3G3+
GS2/52
T1R+
HESINTOK+
F23 1
ALWINT+
F22 1
F18 4
CMS50- B
353
CMS5-
F22 3
CP2 8
KP
CFRZ+
KEEP PRGSY.
L
F17 1
T2R+
CMS50-
CMS4- SH
F22 2
GS2/42
PHNO+
NO
MULTICHANNEL
PHMCMIX-
F19 2
F24 1
FP1/1
PHNO-
T2G0+
ALWINT+
F18 2
T3G2+
I/O address shift on Sheet #14
CMS10-
CMS2-
F21 1
T3G3+
F20 4
CWR+
DP1/74
RB69+
F24 10
COUNTER WORD RECEIVE.
CP2 7
ALWINT+
CWR
CMS10- F22K
CMS2-
F21 4
T3G3
F20 1
CP2 10
L
01/45
PHINTA-
F24 5
PHINTB-
F24 4
T3G3+
F20 3
CP2 5
INT
INTERRUPTS
ALWINT+
STOP
CMS50-
CMS2-
F21 5
F24 6
01/19
INT-
INH
INT
CMS50-
CMS4-
F21 6
T3G3+
F20 2
CP2 9
GL
F24/8
-6
GS2/44
PHL+
L LINE.
ALWINT+
F19 5
CMS00-
CMS2-
T3Gφ+ B
F21 2
PHMS02+
CFSGO+
F19 1
GS1/61
PHNBAD-
F24 7
GS2/38
PHC+
C LINE 44-51
CMS1-
F21 3
F23 3
F25 2 758
250nsec
F24 8
FS3/46
When Binary word C line held for 250n/s.
CMS10- J
T3Gφ+ K
BUSYB+ A(B13)
CP2 12
C
F19 4
CB-K+
To Iodt
CFRZ+
(SEE DWG 22)
T3G3+
WILL RESET T IN CP OF 24.6
CMS10-
CMS5-
F22 5
F23 4
CP2 11
T
F25 1 758
550NSEC
MOD LEVEL 4
ACW 1550
19/8/68
CFRZ+
CFSGO+
T PULSE.
CMS10-
CMS5-
F22 6
F23 2
F24 9
F19 6
GS2/40
PHT+
FS3/18
BOUT9+
FP1/22
F19 3
CBCH-K+
(See Dwg. 22)
CFRZ
F22 10
NTROL
WGC 01/41
SS 1 2 3 4

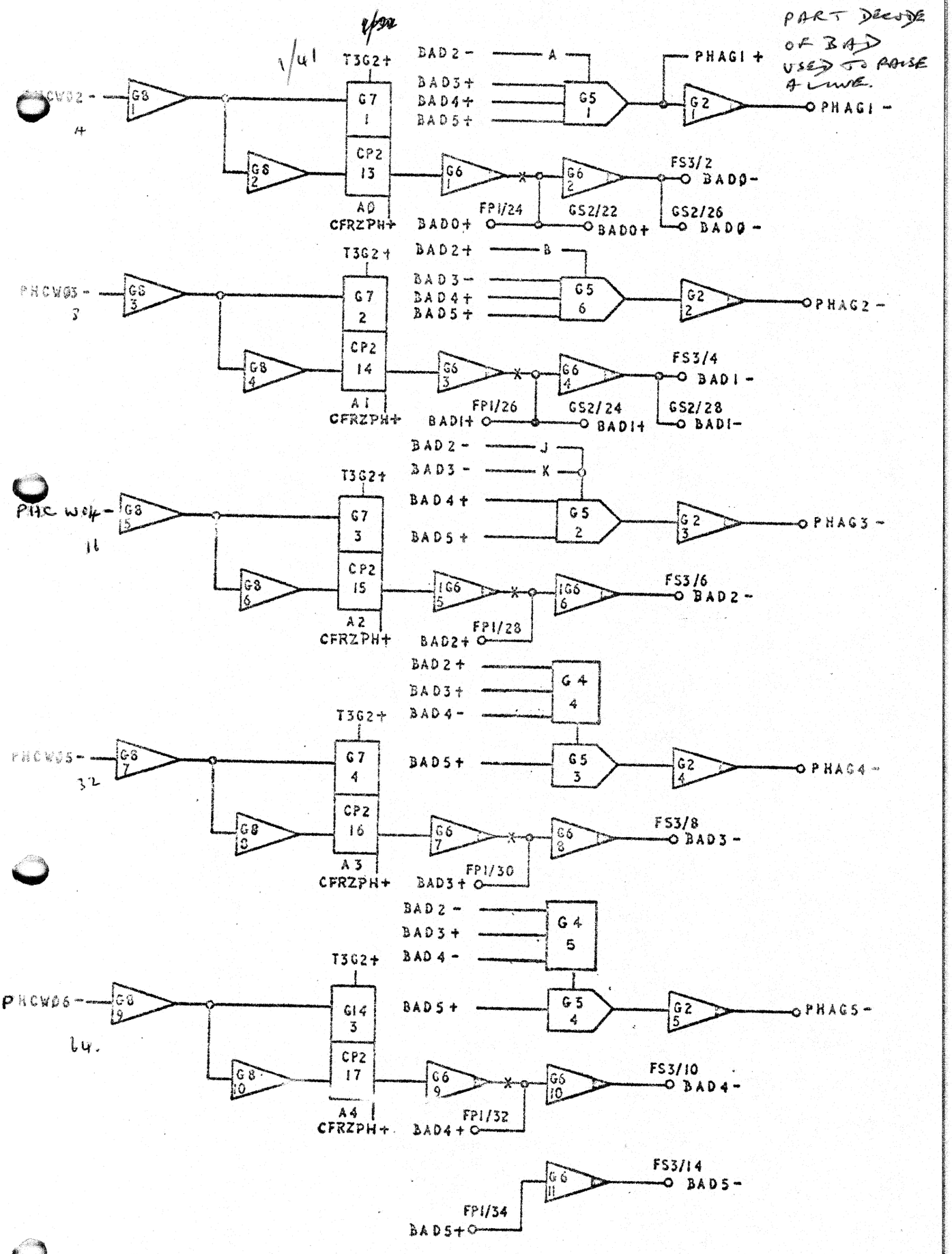

T2R+
01/41
PHAGI+
A
S04/71
04R
S04/59
04HIA
HIGHEST PRIORITY
PSM+
01/45
PHR04+
CFRZPH+
S05/71
05R
S05/59
05HIA
PHR05+
S06/71
06R
S06/59
06HIA
PHR06+
S07/71
07R
S07/59
07HIA
PHR07+
S08/71
08R
S08/59
08HIA
PHR08+
S09/71
09R
09/59
09HIA
PHR09+
TFS-
PHBP2
PHRP2+
PHLP+
TYHR+
PHTN+
100K
HREQ
CP2/6
TIMRES-
PHTN+
PHRP2+
PHLP+
TYHR+
GS2/46
PHHP1+
GS2/48
PHHP2+
PRIORITY



CONTROL WORD ENCODER

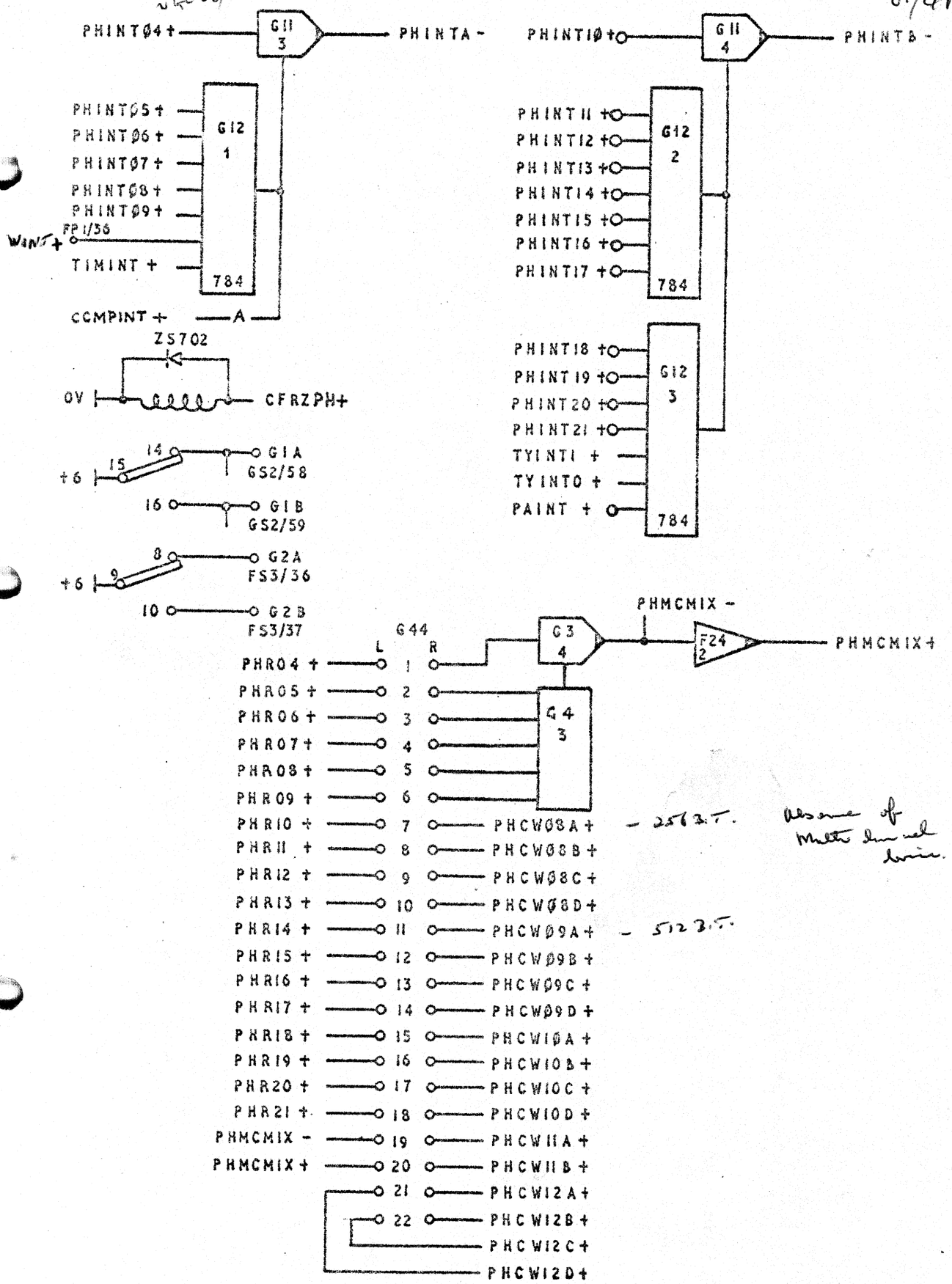
WGC 01/43

SUB	ISS	1	2


PART DECODE OF BAD USED TO RAISE A LINE.
T3G2+
BAD2 - A
BAD3+
BAD4+
BAD5+
G5 1
G2 1
PHAG1 +
PHAG1 -
G8 1
G7 1
CP2 13
G8 2
G6 1
G6 2
FS3/2
BAD0-
A0
CFRZPH+
FP1/24
BAD0+
GS2/22
BAD0+
GS2/26
BAD0 -
T3G2+
BAD2+ B
BAD3 -
BAD4+
BAD5+
G5 6
G2 2
PHAG2 -
G8 3
G7 2
CP2 14
G8 4
G6 3
G6 4
FS3/4
BAD1 -
A1
CFRZPH+
FP1/26
BAD1+
GS2/24
BAD1+
GS2/28
BAD1-
BAD2 - J
BAD3 - K
T3G2+
BAD4+
BAD5+
G5 2
G2 3
PHAG3 -
G8 5
G7 3
CP2 15
G8 6
G6 5
G6 6
FS3/6
BAD2 -
A2
CFRZPH+
FP1/28
BAD2+
BAD2+
BAD3+
BAD4 -
G4 4
T3G2+
BAD5+
G5 3
G2 4
PHAG4 -
G8 7
G7 4
CP2 16
G8 8
G6 7
G6 8
FS3/8
BAD3 -
A3
CFRZPH+
FP1/30
BAD3+
BAD2 -
BAD3+
BAD4 -
G4 5
T3G2+
BAD5+
G5 4
G2 5
PHAG5 -
G8 9
GI4 3
CP2 17
G8 10
G6 9
G6 10
FS3/10
BAD4 -
A4
CFRZPH+
FP1/32
BAD4+
G6 11
FS3/14
BAD5 -
FP1/34
BAD5+

WGC02/57

01/41



TO SPECIFY THE CONTROL WORD BASE ADDRESS OF NORMAL PERIPHERALS LINK FROM PHMCMIX- TO THE PHCW SIGNALS E.G. 19L TO 7R MAKES A BASE ADDRESS OF 256.

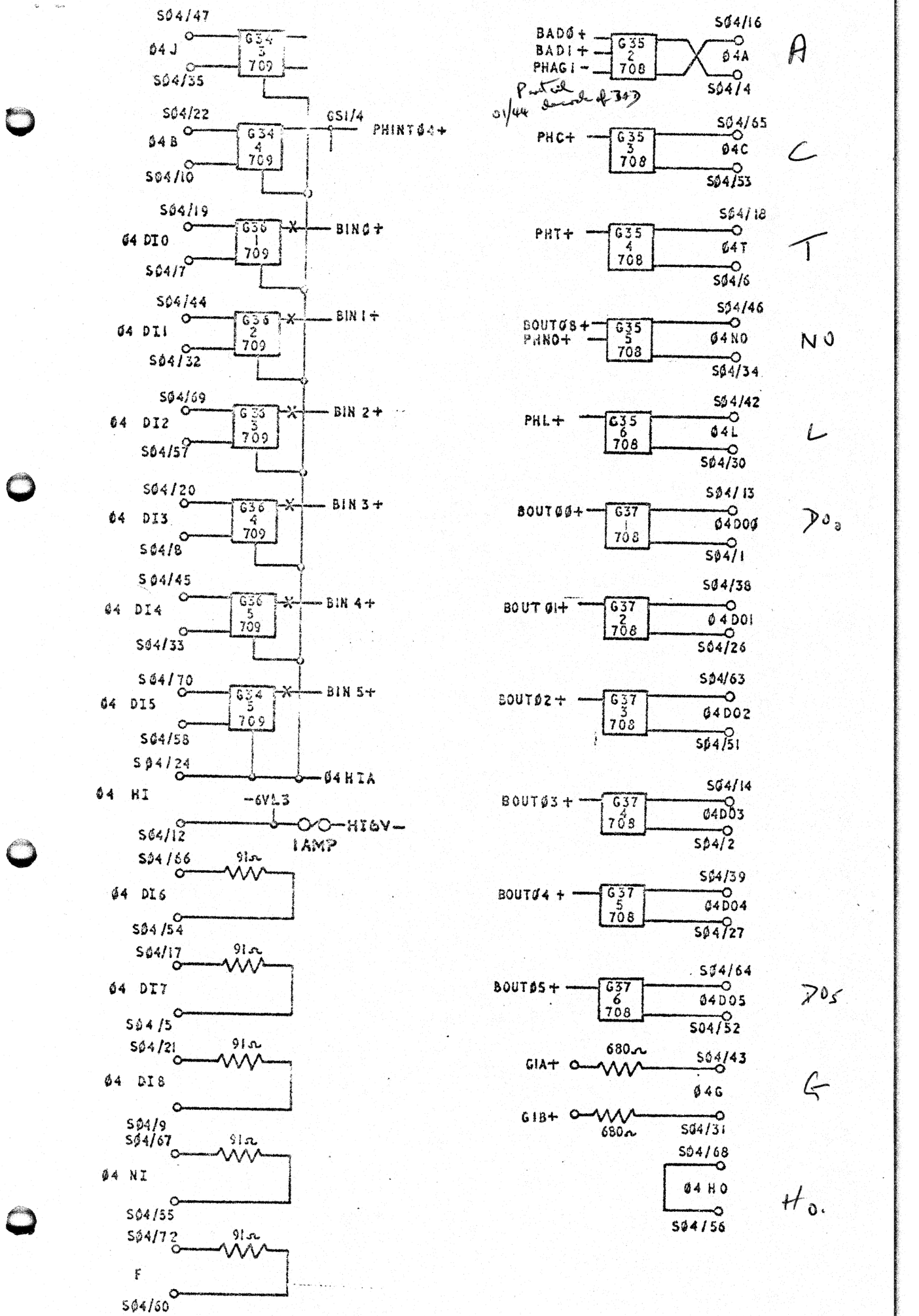
TO SPECIFY THE CONTROL WORD BASE ADDRESS OFAMULTICHANNEL PERIPHERAL, LINK FROM THE PHR TO THE MULTICHANNEL MIX AND THE BASE ADDRESS. E.G. 6L TO IR TO IIR MAKES SOCKET 9 MULTICHANNEL WITH A BASE ADDRESS OF 512.

BASE ADDRESS LINKS

WGC01/45

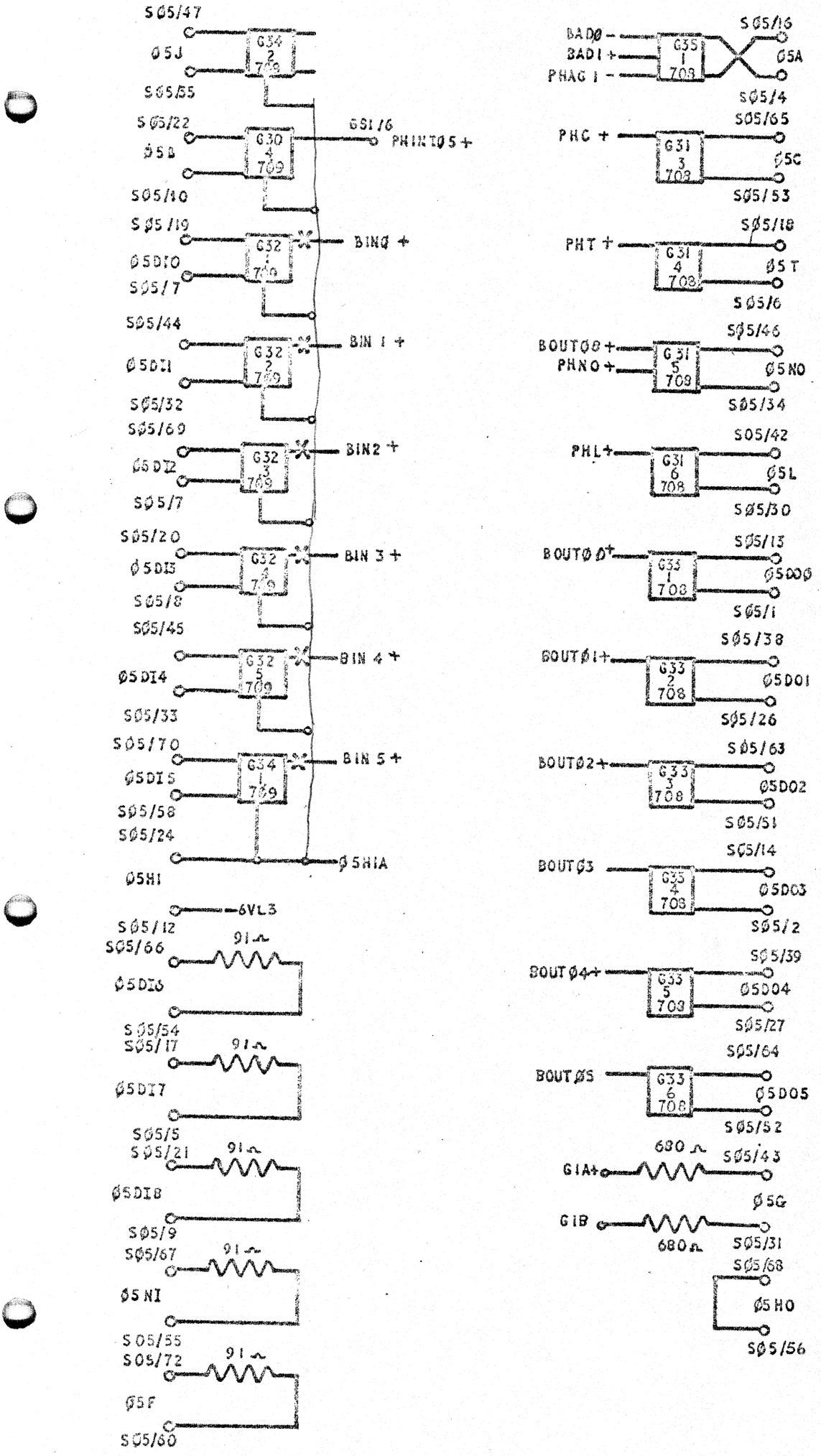
SUB	ISS
	0836

SOCKET 1

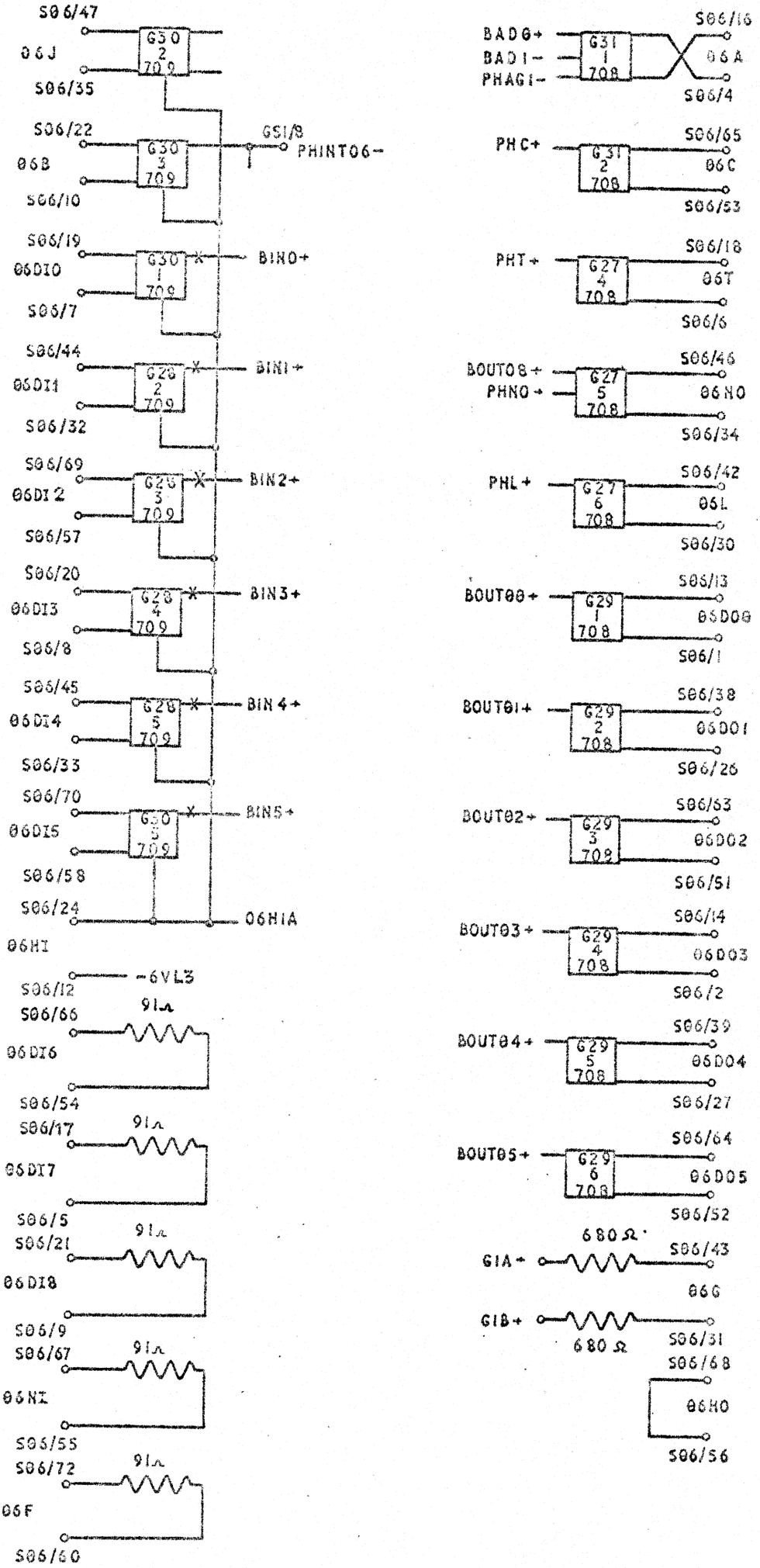


WGC01/46

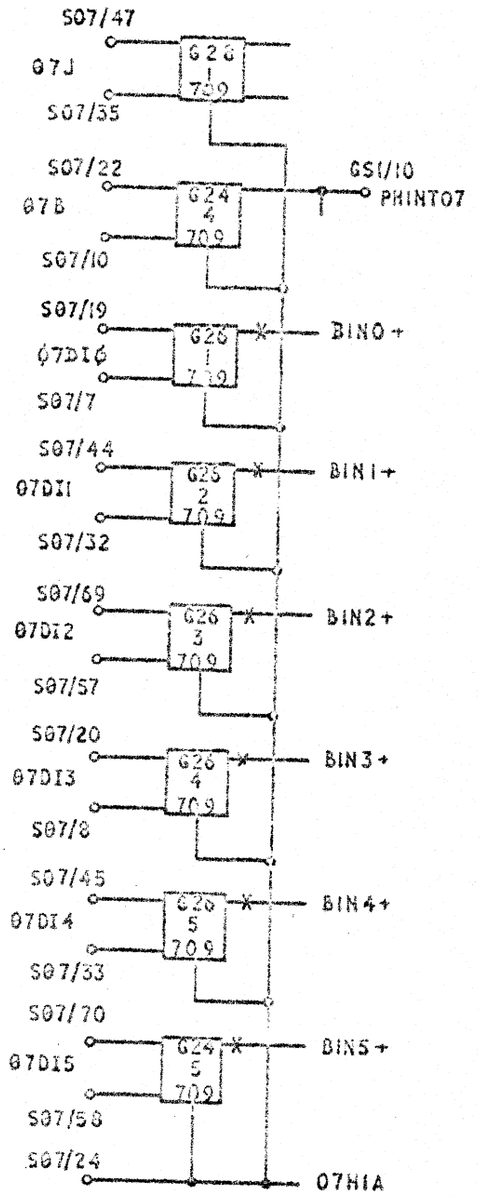
SUB	ISS	1
A.C.W.	0836	0945

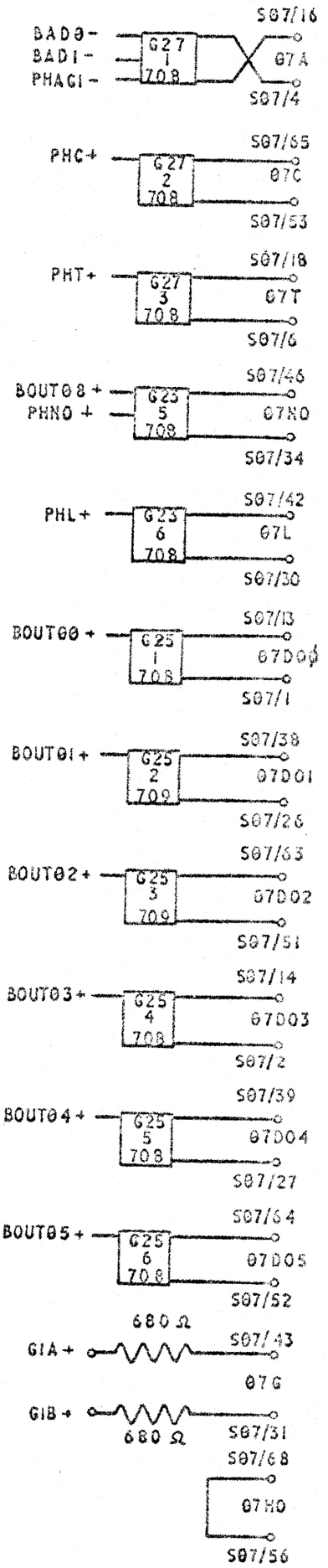

SØ5/47
G34 2 709
ØSJ
SØ5/55
SØ5/22
G30 4 709
ØSB
GSI/6
PHINTØ5+
SØ5/10
SØ5/19
G32 1 709
BINØ+
ØSDIØ
SØ5/7
SØ5/44
G32 2 709
BIN 1+
ØSDI1
SØ5/32
SØ5/69
G32 3 709
BIN2+
ØSDI2
SØ5/7
SØ5/20
G32 4 709
BIN 3+
ØSDI3
SØ5/8
SØ5/45
G32 5 709
BIN 4+
ØSDI4
SØ5/33
SØ5/70
G34 1 709
BIN 5+
ØSDI5
SØ5/58
SØ5/24
ØSHIA
ØSHI
-6VL3
SØ5/12
SØ5/66
91Ω
ØSDI6
SØ5/54
SØ5/17
91Ω
ØSDI7
SØ5/5
SØ5/21
91Ω
ØSDIB
SØ5/9
SØ5/67
91Ω
ØSNI
SØ5/55
SØ5/72
91Ω
ØSF
SØ5/60
BADØ-
BADI+
PHAG I-
G35 1 708
SØ5/16
ØSA
SØ5/4
PHC+
G31 3 708
SØ5/65
ØSC
SØ5/53
PHT+
G31 4 708
SØ5/18
ØST
SØ5/6
BOUTØØ+
PHNO+
G31 5 709
SØ5/46
ØSNO
SØ5/34
PHL+
G31 6 708
SØ5/42
ØSL
SØ5/30
BOUTØØ+
G33 1 708
SØ5/13
ØSDØØ
SØ5/1
BOUTØ1+
G33 2 708
SØ5/38
ØSDOI
SØ5/26
BOUTØ2+
G33 3 708
SØ5/63
ØSDO2
SØ5/51
BOUTØ3
G33 4 708
SØ5/14
ØSDO3
SØ5/2
BOUTØ4+
G33 5 709
SØ5/39
ØSDO4
SØ5/27
BOUTØ5
G33 6 708
SØ5/64
ØSDO5
SØ5/52
680Ω
GIA+
SØ5/43
ØSG
GIB
680Ω
SØ5/31
SØ5/68
ØSHO
SØ5/56

WGC01/47


S06/47
06J
S06/35
G30 2 709
S06/22
06B
S06/10
G30 3 709
GSI/8
PHINT06-
S06/19
06DI0
S06/7
G30 1 709
BIN0+
S06/44
06DI1
S06/32
G28 2 709
BIN1+
S06/69
06DI2
S06/57
G28 3 709
BIN2+
S06/20
06DI3
S06/8
G28 4 709
BIN3+
S06/45
06DI4
S06/33
G28 5 709
BIN4+
S06/70
06DI5
S06/58
G30 5 709
BIN5+
S06/24
06HIA
06HI
-6VL3
S06/12
S06/66
91Ω
06DI6
S06/54
S06/17
91Ω
06DI7
S06/5
S06/21
91Ω
06DI8
S06/9
S06/67
91Ω
06NI
S06/55
S06/72
91Ω
06F
S06/60
BADG+
BADI-
PHAGI-
G31 1 708
S06/16
06A
S06/4
PHC+
G31 2 708
S06/65
06C
S06/53
PHT+
G27 4 708
S06/18
06T
S06/6
BOUT08+
PHNO+
G27 5 708
S06/46
06NO
S06/34
PHL+
G27 6 708
S06/42
06L
S06/30
BOUT00+
G29 1 708
S06/13
06D00
S06/1
BOUT01+
G29 2 708
S06/38
06D01
S06/26
BOUT02+
G29 3 708
S06/63
06D02
S06/51
BOUT03+
G29 4 708
S06/14
06D03
S06/2
BOUT04+
G29 5 708
S06/39
06D04
S06/27
BOUT05+
G29 6 708
S06/64
06D05
S06/52
680Ω
GIA+
S06/43
06G
GIB+
680Ω
S06/31
S06/68
06H0
S06/56

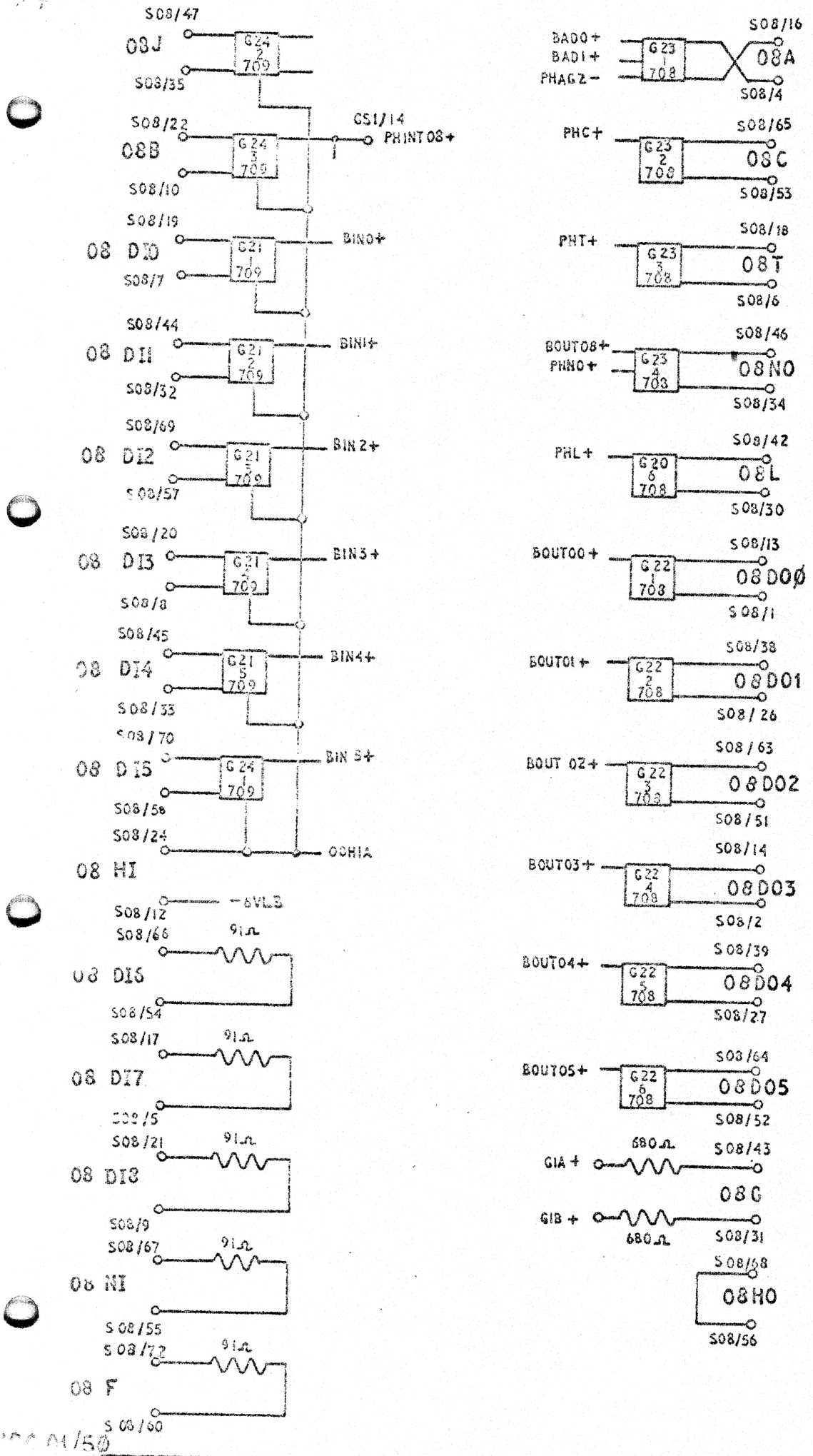
SUB	ISS	1





SUB	155	1															
ADW	10855	0929															

50



50 01/50

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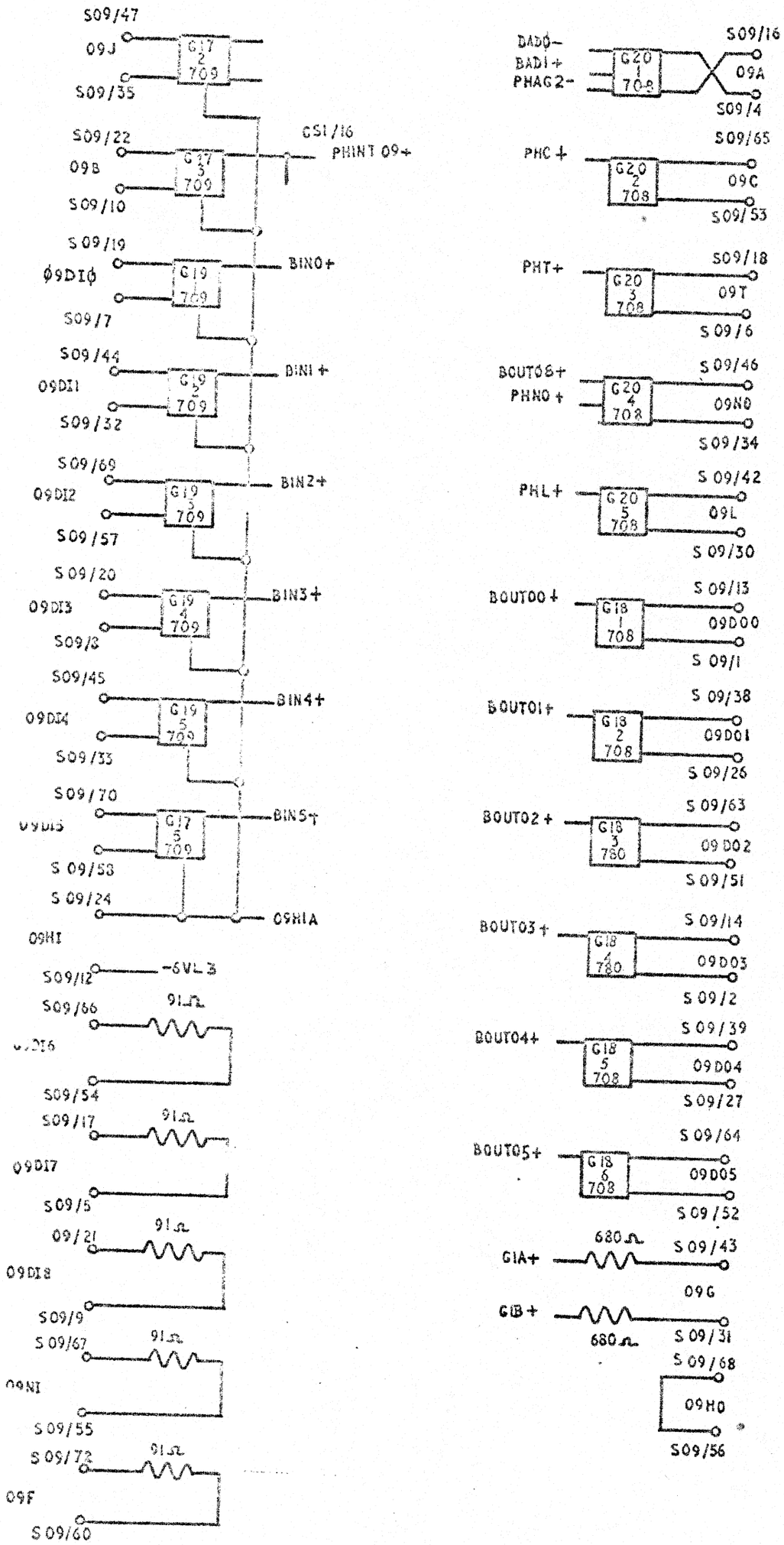
ACN	0836	0945													



WGC01/51

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IACM 10 33/	0945	