IBM Maintenance Library

IBM System /3
5410 Processing Unit
Diagrams

SY31-0202-1

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5410 Processing Unit
Field Engineering Diagrams Manuals

This Technical Newsletter provides replacement pages for the subject publication. These replacement pages remain in effect unless specifically altered. Pages to be inserted and/or removed are:

Front Cover
Title Page, Preface
2-040, 2-050
3-010, 3-020
4-076–4-082
4-100, 4-105
6-010–Index
Reader's Comment
Back Cover

Summary of Amendments

This change adds 48K storage and +6V replacement bulk supply information to the diagrams. It also adds new covers in compliance with recent specification changes. This changes the title to:

IBM Maintenance Library
IBM System/3
5410 Processing Unit
Diagrams

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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5410 Processing Unit
Diagrams

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Preface

Diagrams and flowcharts in this manual are at engineering change level 816614.

The diagrams in this manual are organized by operation. Thus, the details of machine operations are presented in operational flowcharts, most of which are *two-level.* The general flow path of the two-level charts (heavy line) shows the major objectives of an operation or instruction. Detailed flow paths of major objectives are located to the right of the general flow path.

Positive-logic diagrams support the operational flowcharts. They show logical circuit operation without regard to signal levels. Most of the logic diagrams in this manual are not block for block representations of Automated Logic Diagrams. Rather, only blocks necessary for a logical understanding of the operation are shown.

Other manuals needed to understand and service the 5410 are:

1. The *IBM 5410 Processing Unit, Field Engineering Theory of Operations Manual.*
2. The *IBM 5410 Processing Unit, Field Engineering Maintenance Manual.*

Second Edition

This is a major revision of, and obsoletes, SY31-0202-0.

Changes are continually made to the specifications herein; any such change will be reported in subsequent revisions or TNLs.

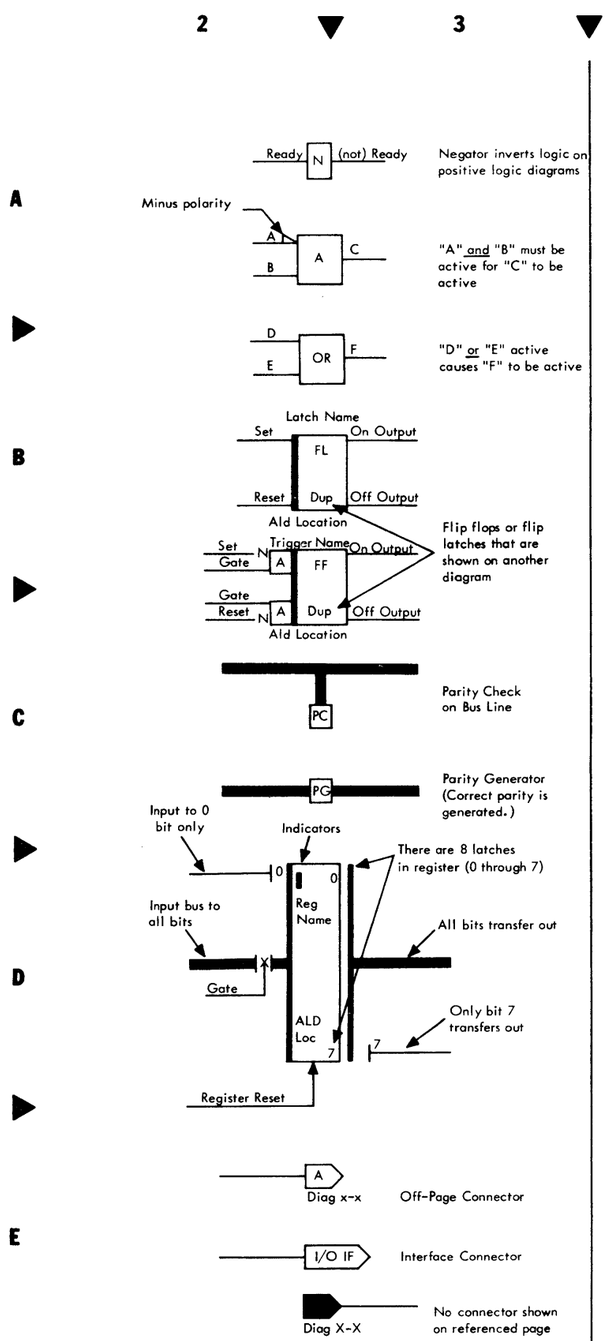
A form for reader's comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

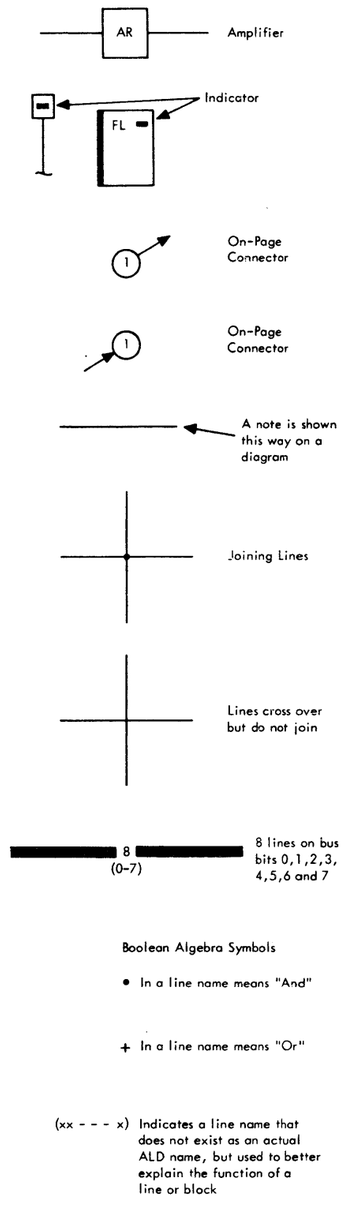
Abbreviations

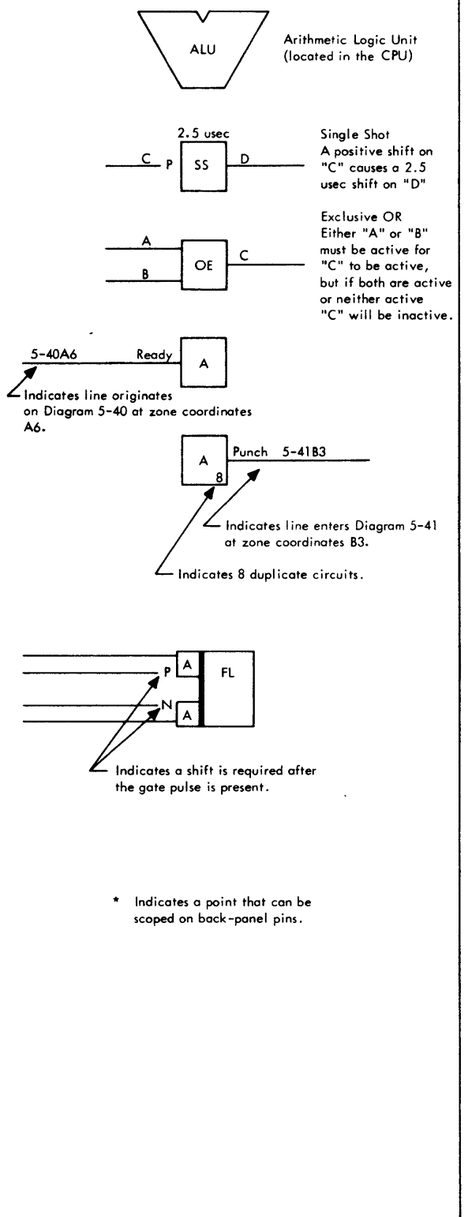
AAR	A field Address Register
ALD	Automated Logic Diagram
ALU	Arithmetic and Logic Unit
ARR	Address Recall Register
BAR	B field Address Register
BSM	Basic Storage Module
CPU	Central Processing Unit
CR	Condition Register
CRR	Condition Recall Register
DA	Device Address
DBI	Data Bus In
DBO	Data Bus Out
DFCR	Disk File Control Address Register
DFDR	Disk File Data Address Register
DPF	Dual Program Feature
DRR	Data Recall Register
EBCDIC	Extended Binary Coded Decimal Interchange Code
IAR	Instruction Address Register
I/O	Input-Output
K	Thousand
LCR	Length Count Register
LCRR	Length Count Recall Register
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LSR	Local Store Registers
MAP	Maintenance Analysis Procedure
MFCU	Multi-Function Card Unit
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MRDAR	MFCU Read Data Address Register
MST	Monolithic System Technology
PC	Parity Check
PG	Parity Generate
POR	Power on Reset
PSR	Program Status Register
SAR	Storage Address Register
SDR	Storage Data Register
XR	Index Register

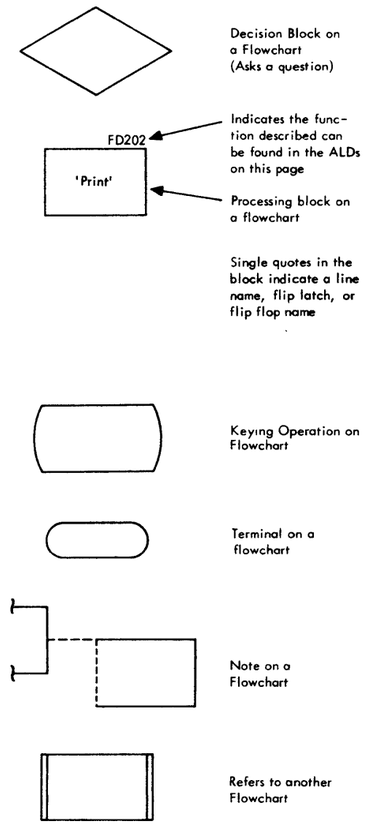
Contents

Legend









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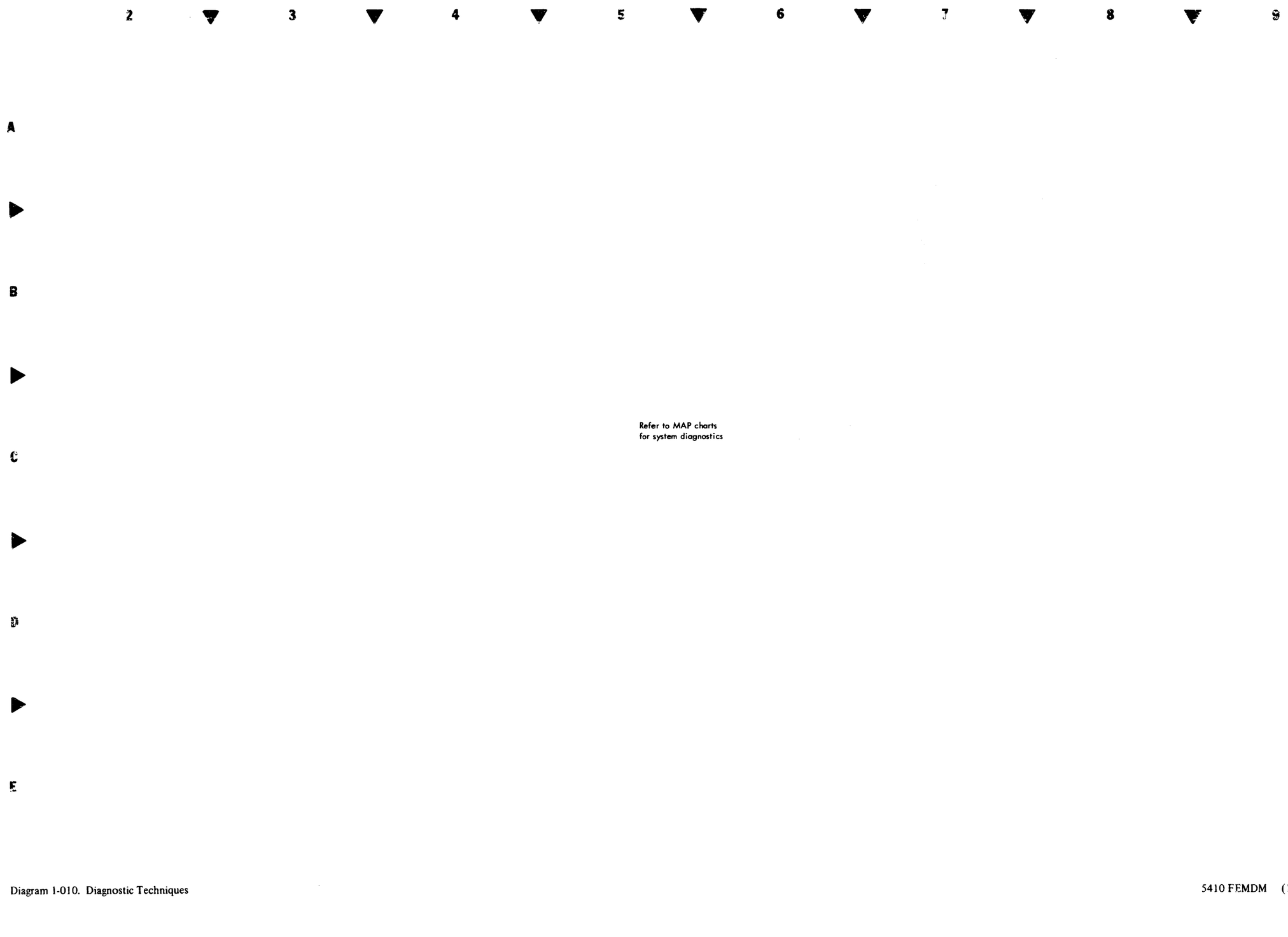
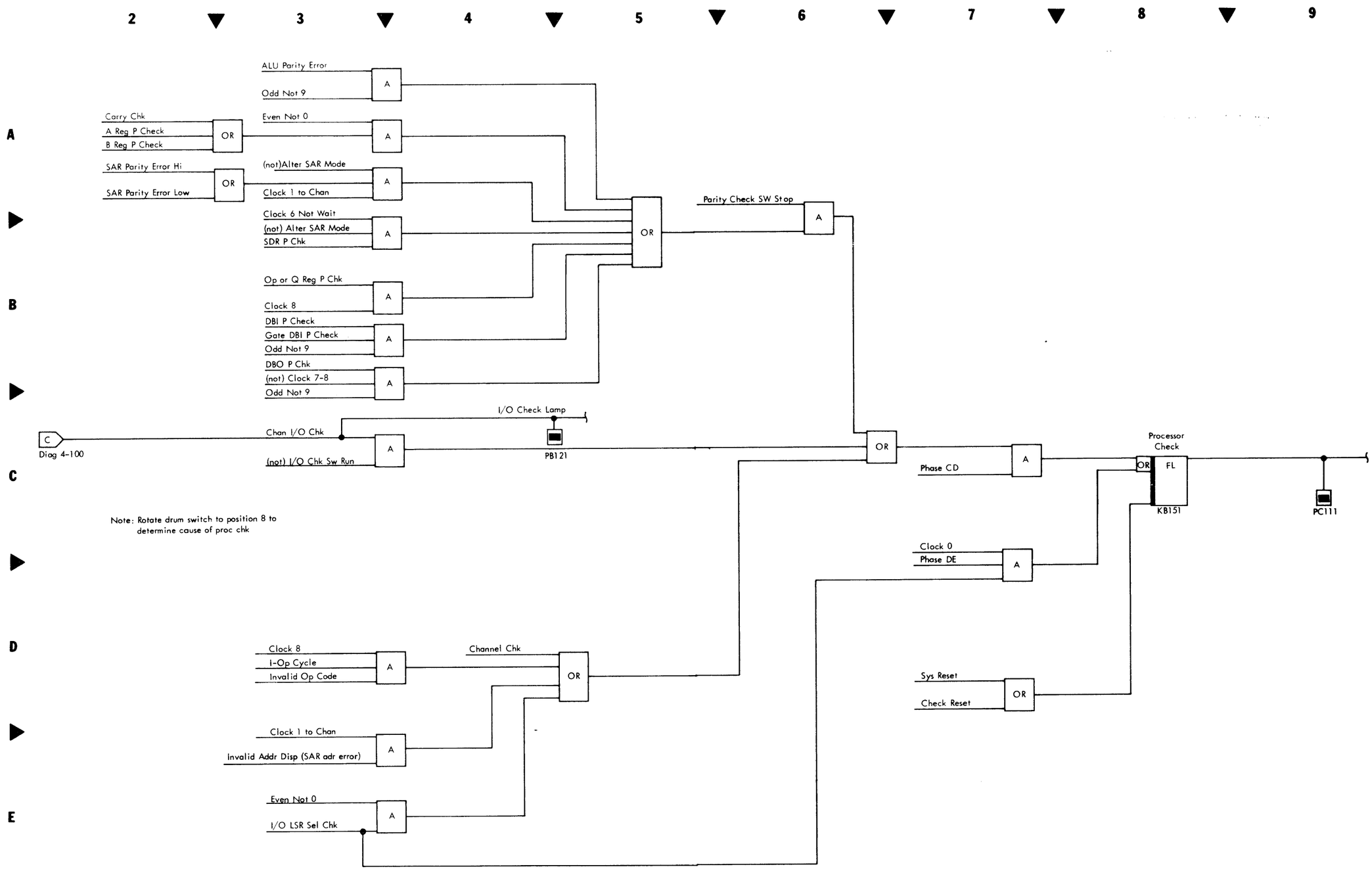


Diagram 1-010. Diagnostic Techniques


2
3
4
5
6
7
8
9
A
B
C
D
E
ALU Parity Error
Odd Not 9
Carry Chk
A Reg P Check
B Reg P Check
OR
Even Not 0
SAR Parity Error Hi
SAR Parity Error Low
(not)Alter SAR Mode
Clock 1 to Chan
Clock 6 Not Wait
(not) Alter SAR Mode
SDR P Chk
Op or Q Reg P Chk
Clock 8
DBI P Check
Gate DBI P Check
Odd Not 9
DBO P Chk
(not) Clock 7-8
Odd Not 9
A
OR
Parity Check SW Stop
I/O Check Lamp
Chan I/O Chk
(not) I/O Chk Sw Run
C
Diag 4-100
PB121
Note: Rotate drum switch to position 8 to determine cause of proc chk
Phase CD
Processor Check
OR
FL
KB151
PC111
Clock 0
Phase DE
Sys Reset
Check Reset
Clock 8
I-Op Cycle
Invalid Op Code
Channel Chk
Clock 1 to Chan
Invalid Addr Disp (SAR adr error)
Even Not 0
I/O LSR Sel Chk

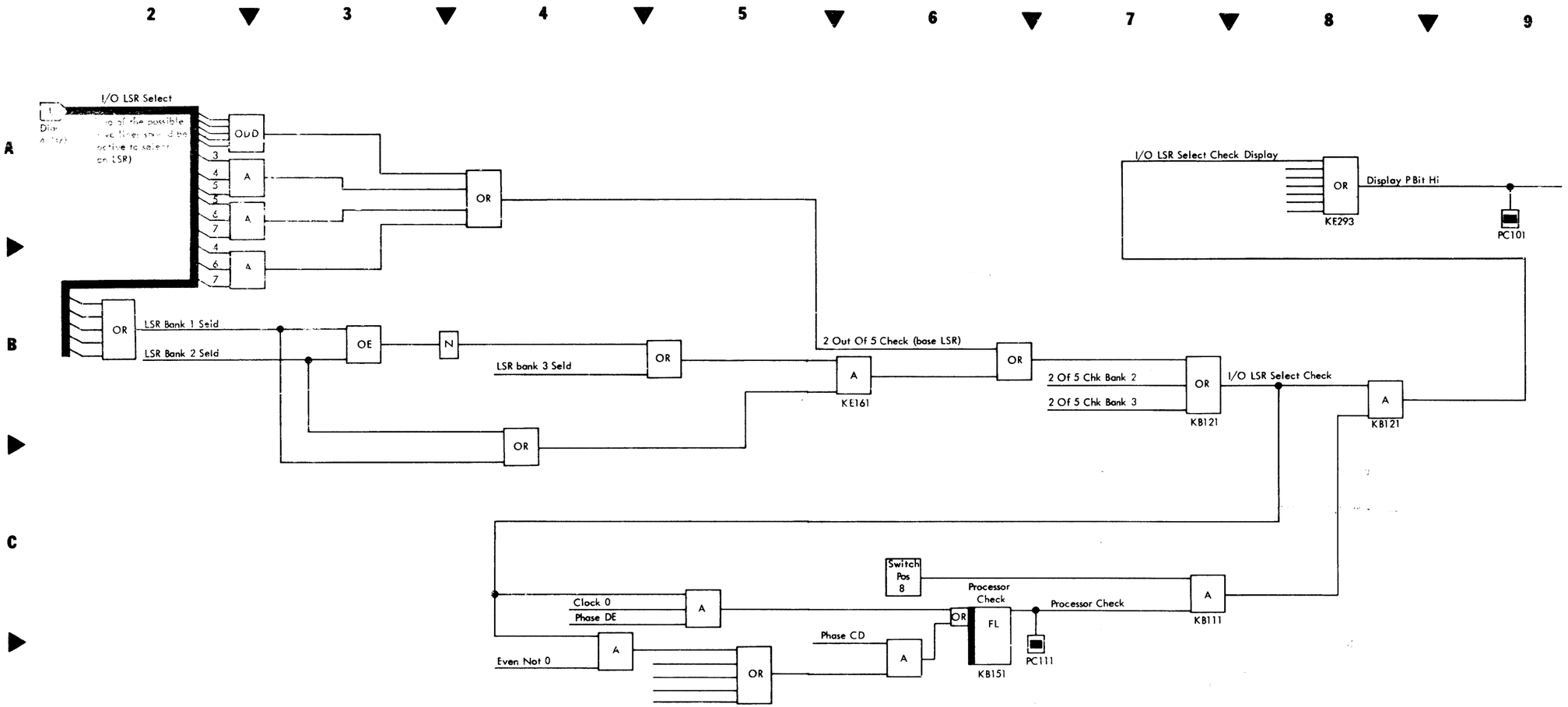
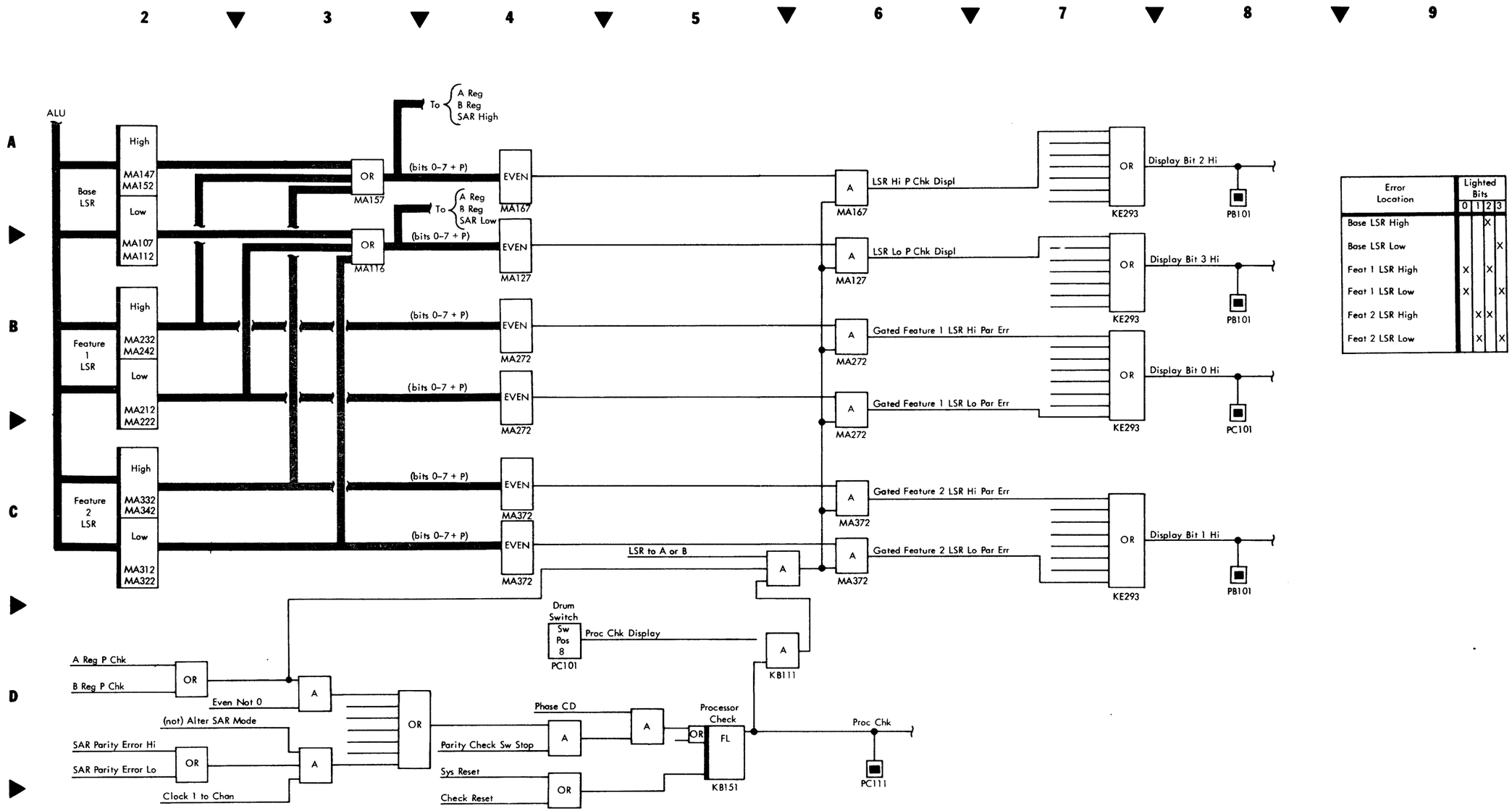


Diagram 2-020. I/O LSR Select Check

Diagram 2-030. LSR Parity



Error Location	Lighted Bits 0	1	2	3
Base LSR High			X	
Base LSR Low				X
Feat 1 LSR High	X		X	
Feat 1 LSR Low	X			X
Feat 2 LSR High		X	X	
Feat 2 LSR Low		X		X

Note: Machine is stopped by either A register, B register or SAR parity error. Drum switch position 1 displays SAR contents, 2 displays LSR contents, 4 displays B register contents, and 5 displays A register contents

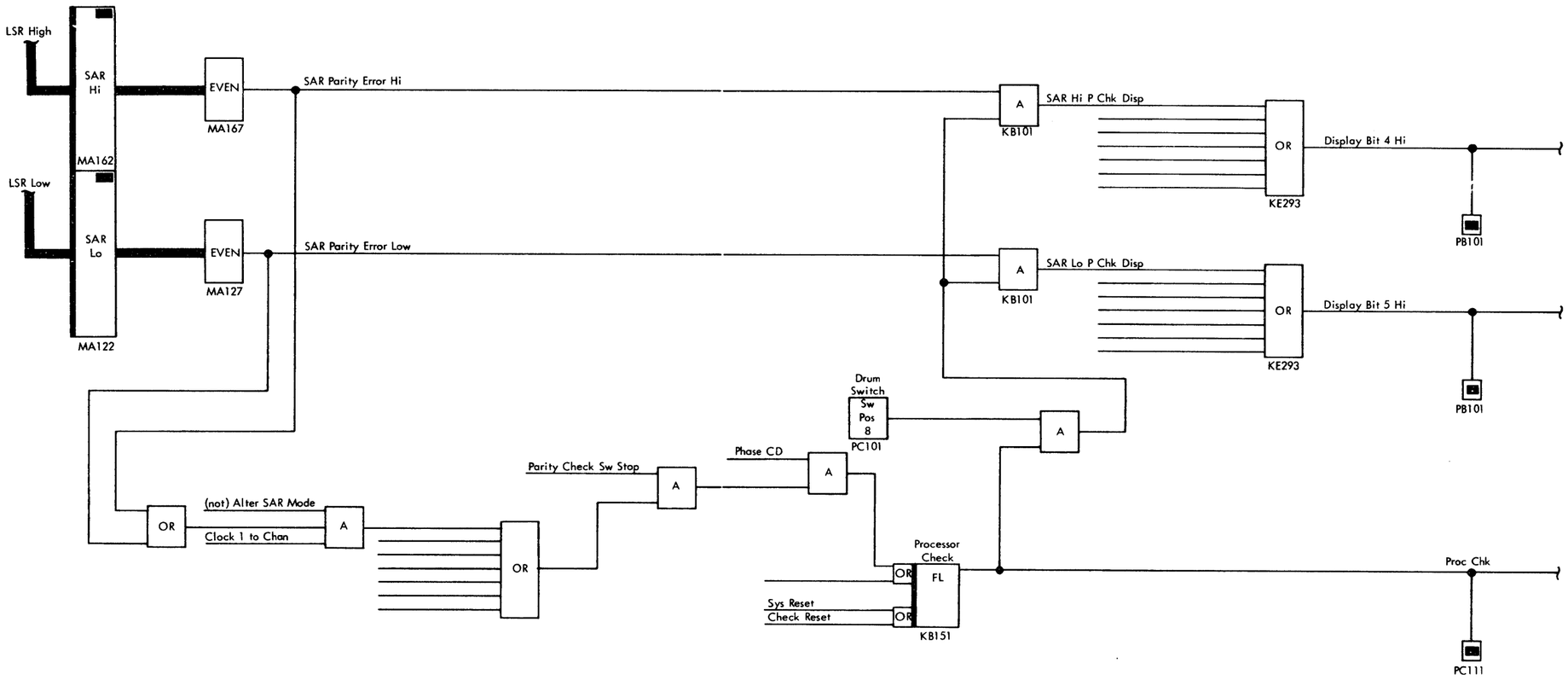
A

B

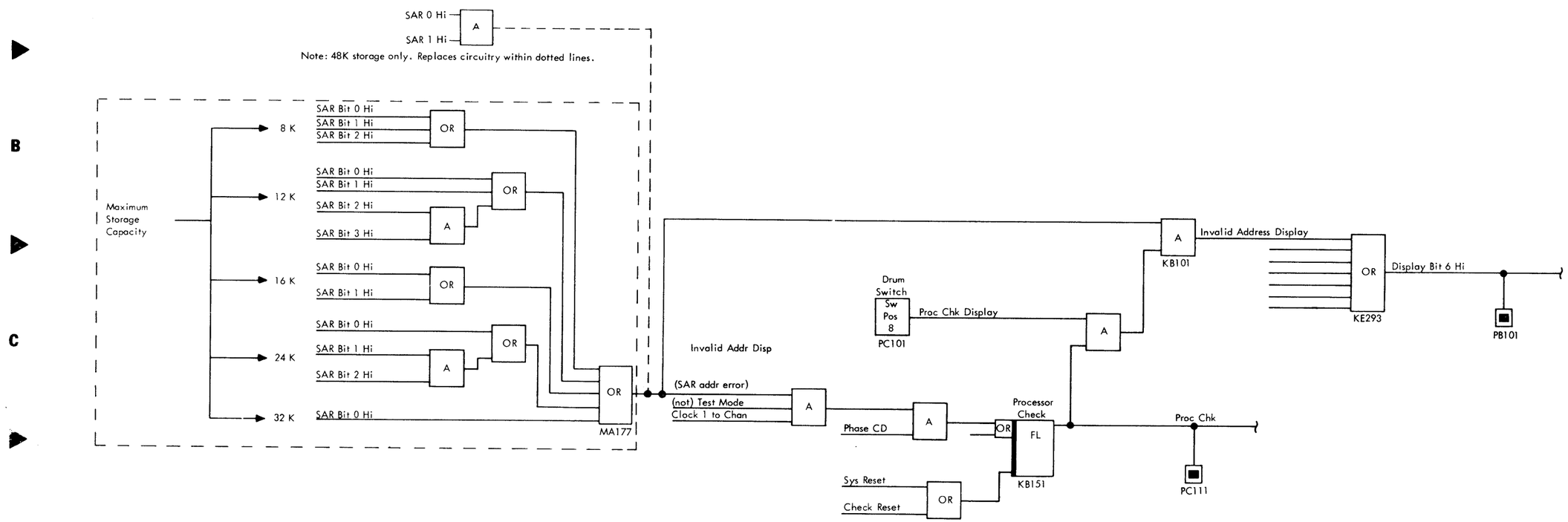
C

D

E



Note: Rotate drum switch to position 1 to display SAR contents



Note: Rotate drum switch to position 1 to display SAR contents

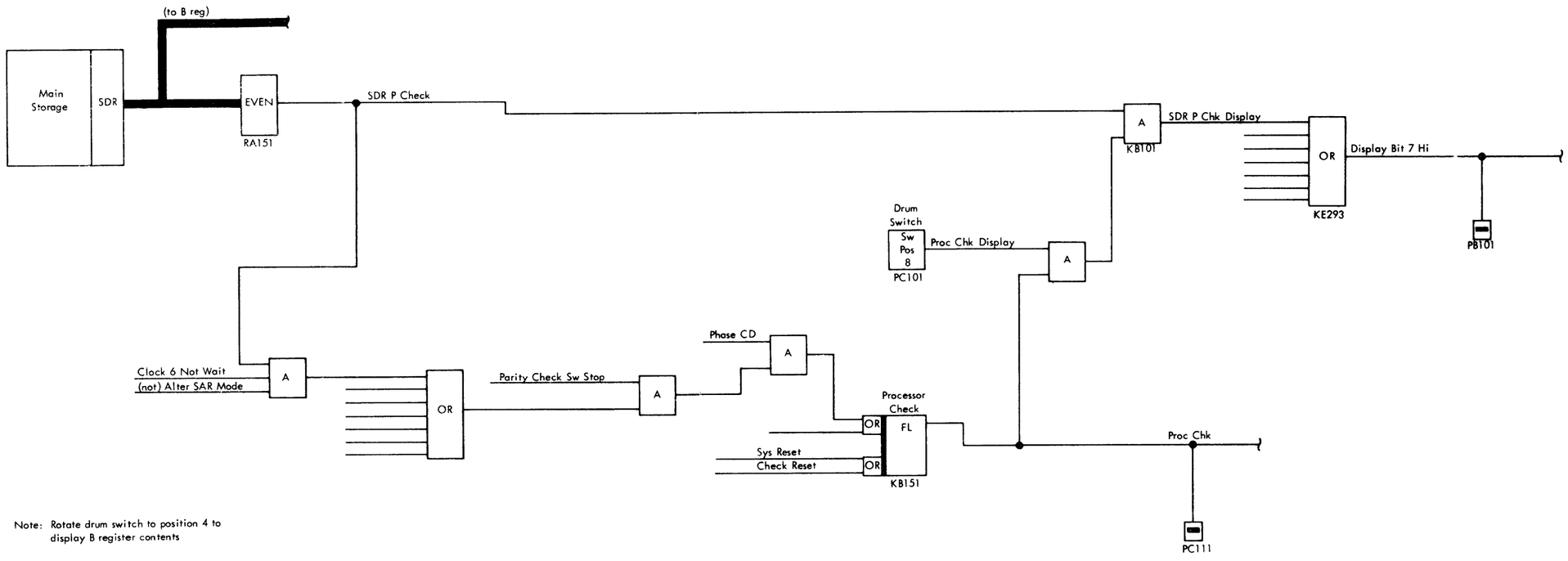
A

B

C

D

E



Note: Rotate drum switch to position 4 to display B register contents

Diagram 2-060. SDR Parity

2 3 4 5 6 7 8 9

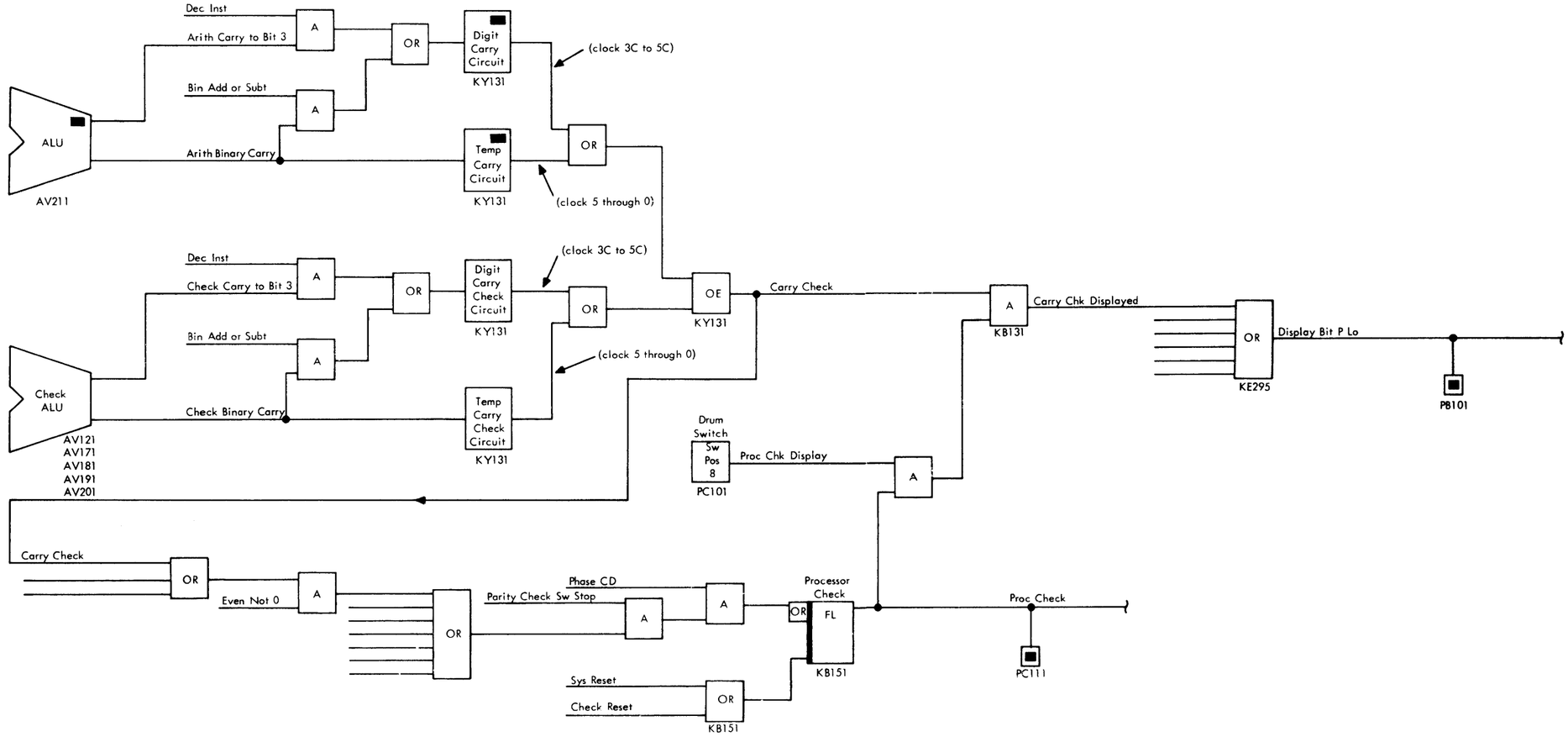
A

B

C

D

E



Note: Rotate drum switch to position 5 to display ALU output, position 4 to display ALU controls and carrys

2 3 4 5 6 7 8 9

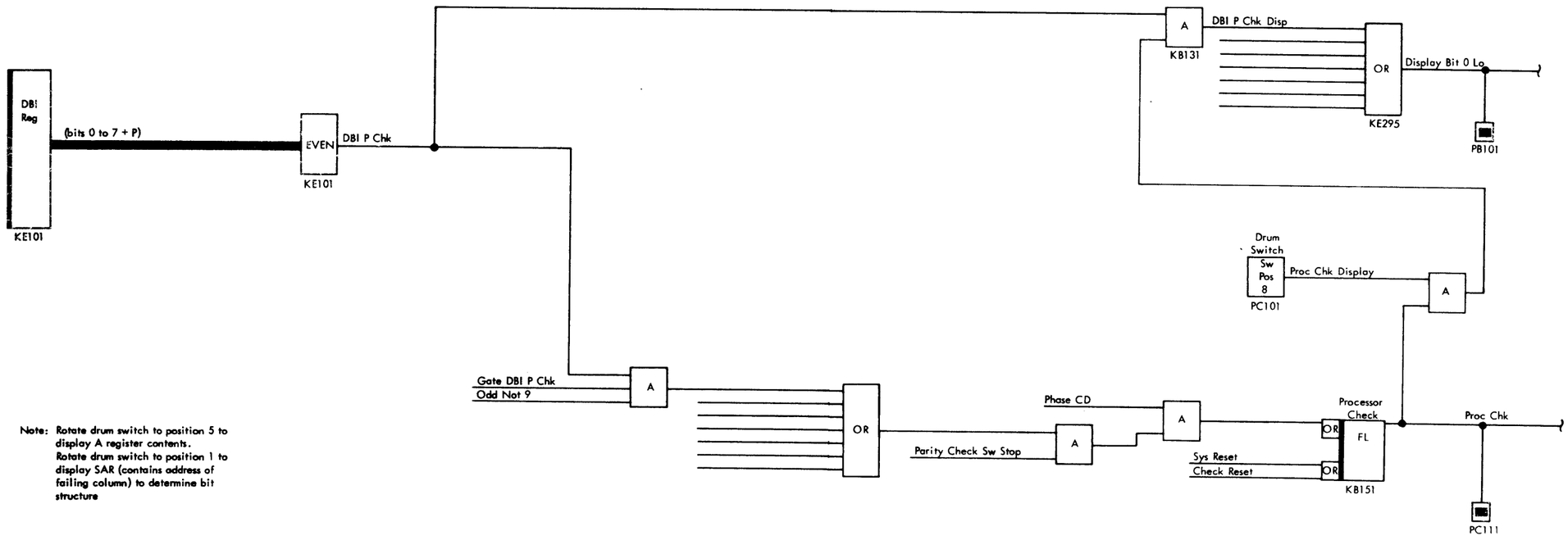
A

B

C

D

E

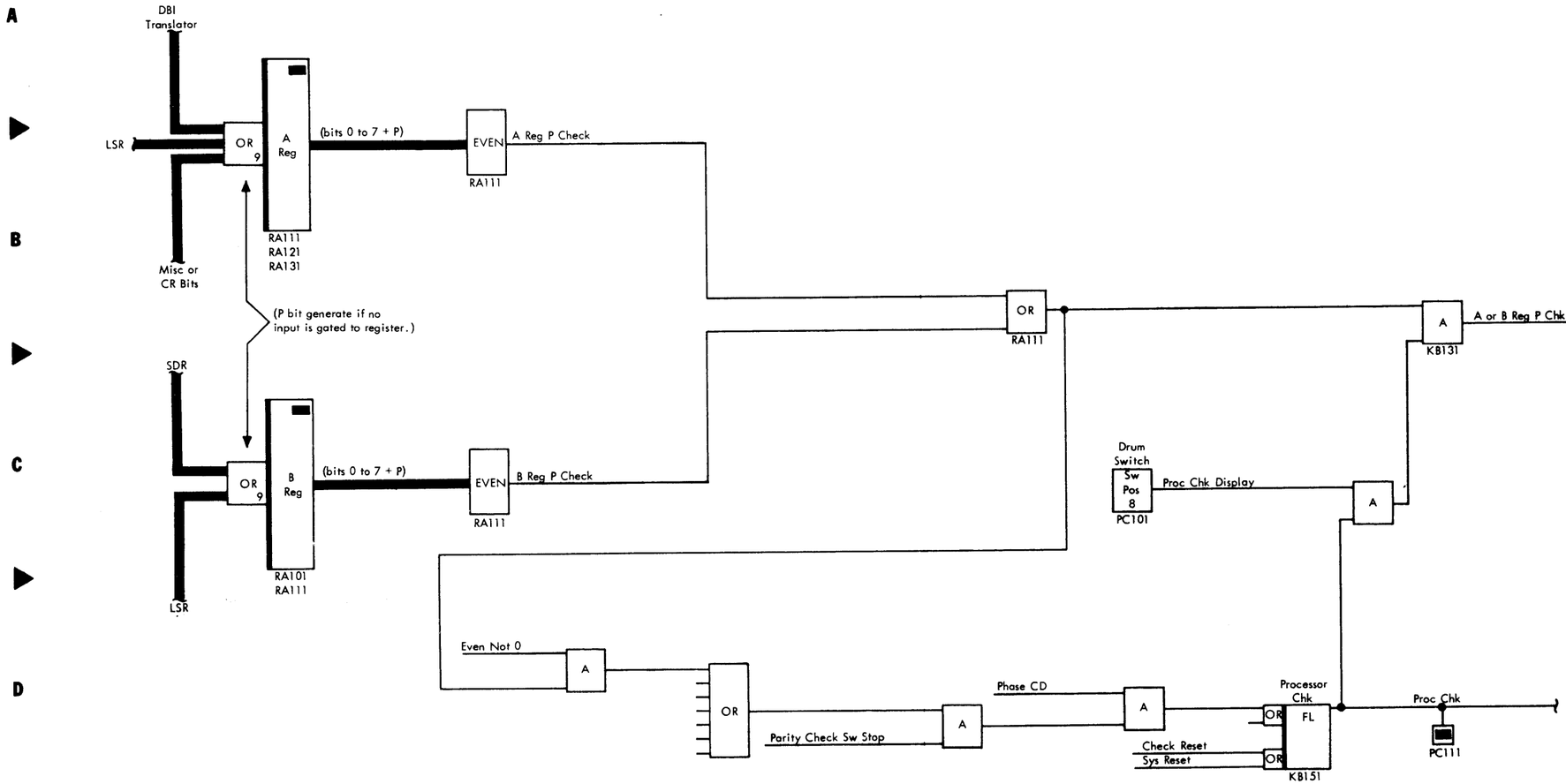


Note: Rotate drum switch to position 5 to display A register contents. Rotate drum switch to position 1 to display SAR (contains address of failing column) to determine bit structure

Diagram 2-080. DBI Parity

2 3 4 5 6 7 8 9

A B C D E



Note: Rotate drum switch to position 5 to display A register contents, position 4 to display B register contents

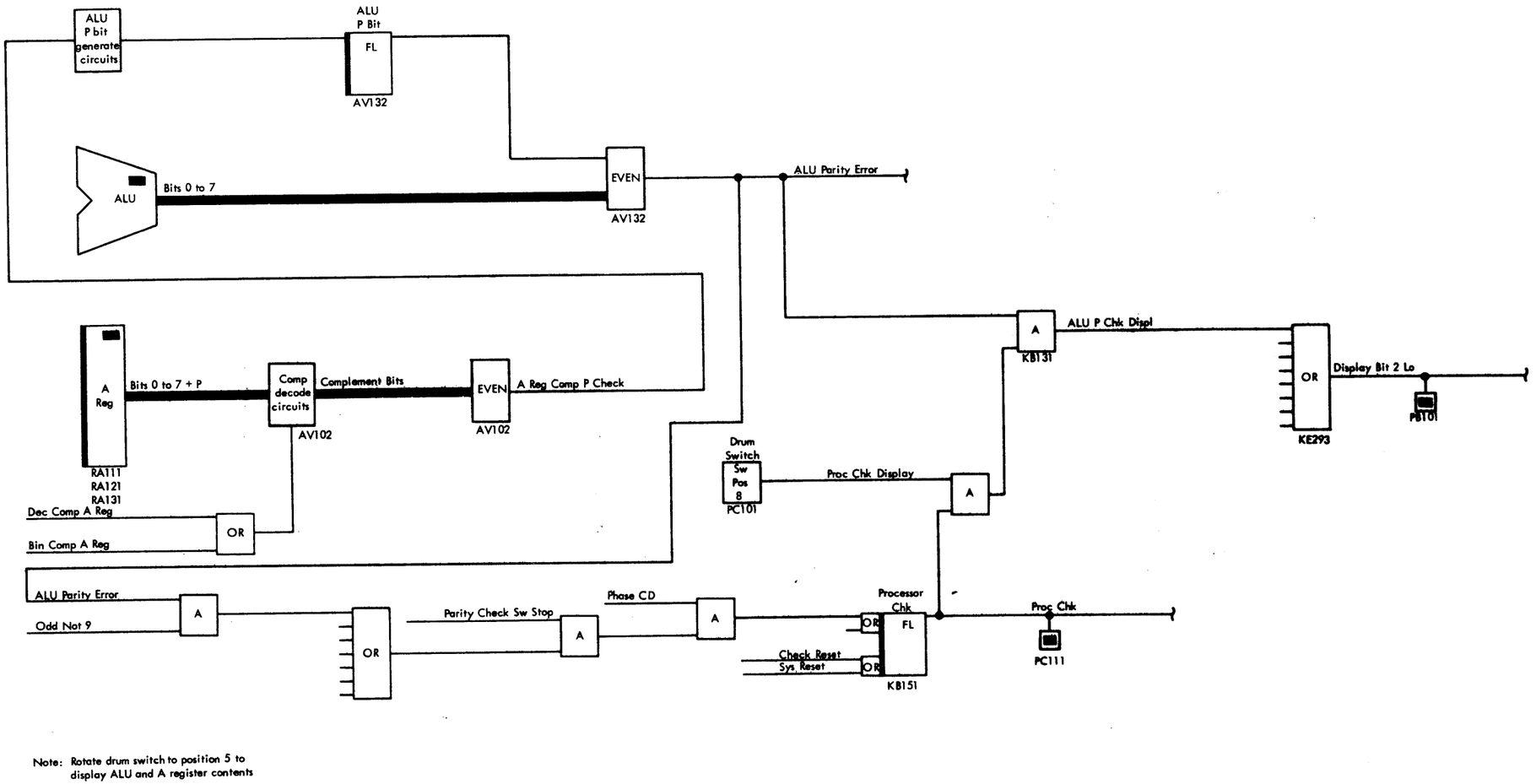
A

B

C

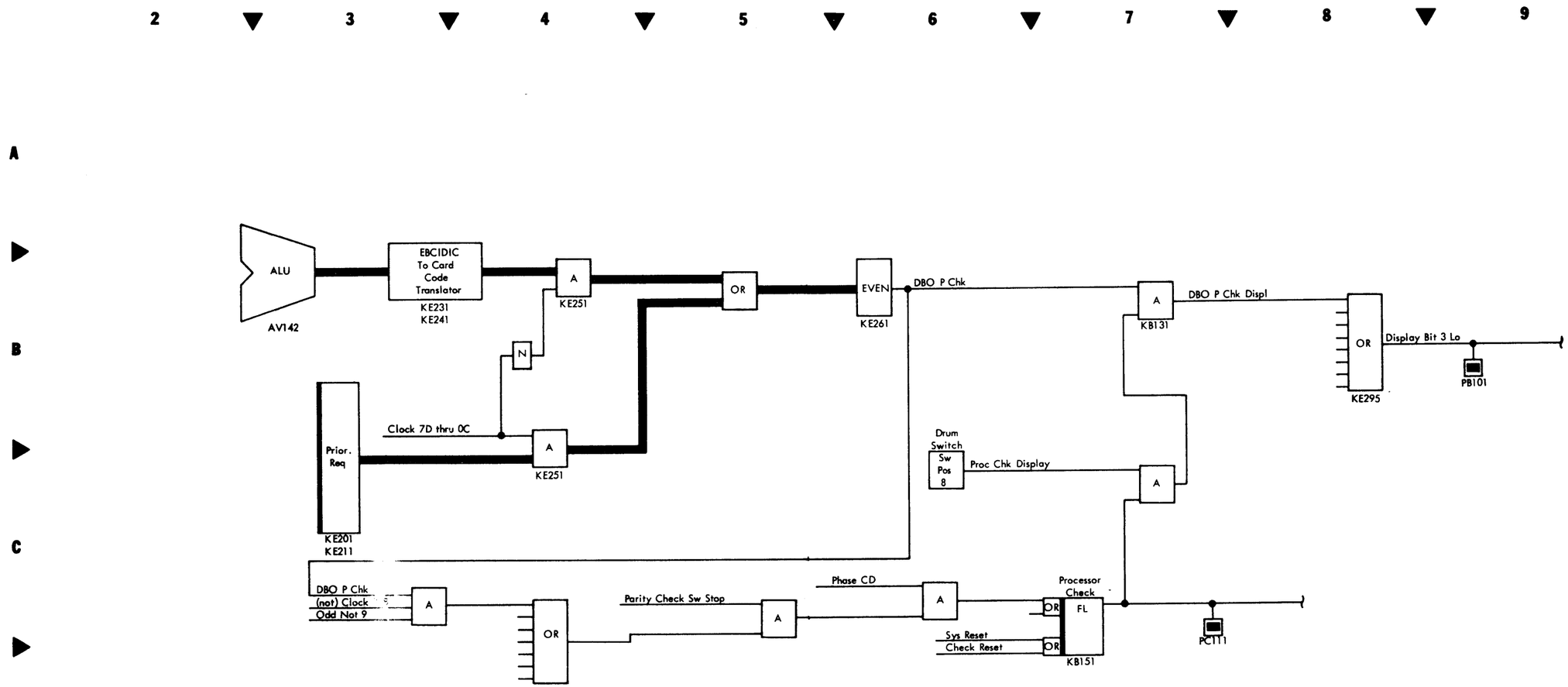
D

E

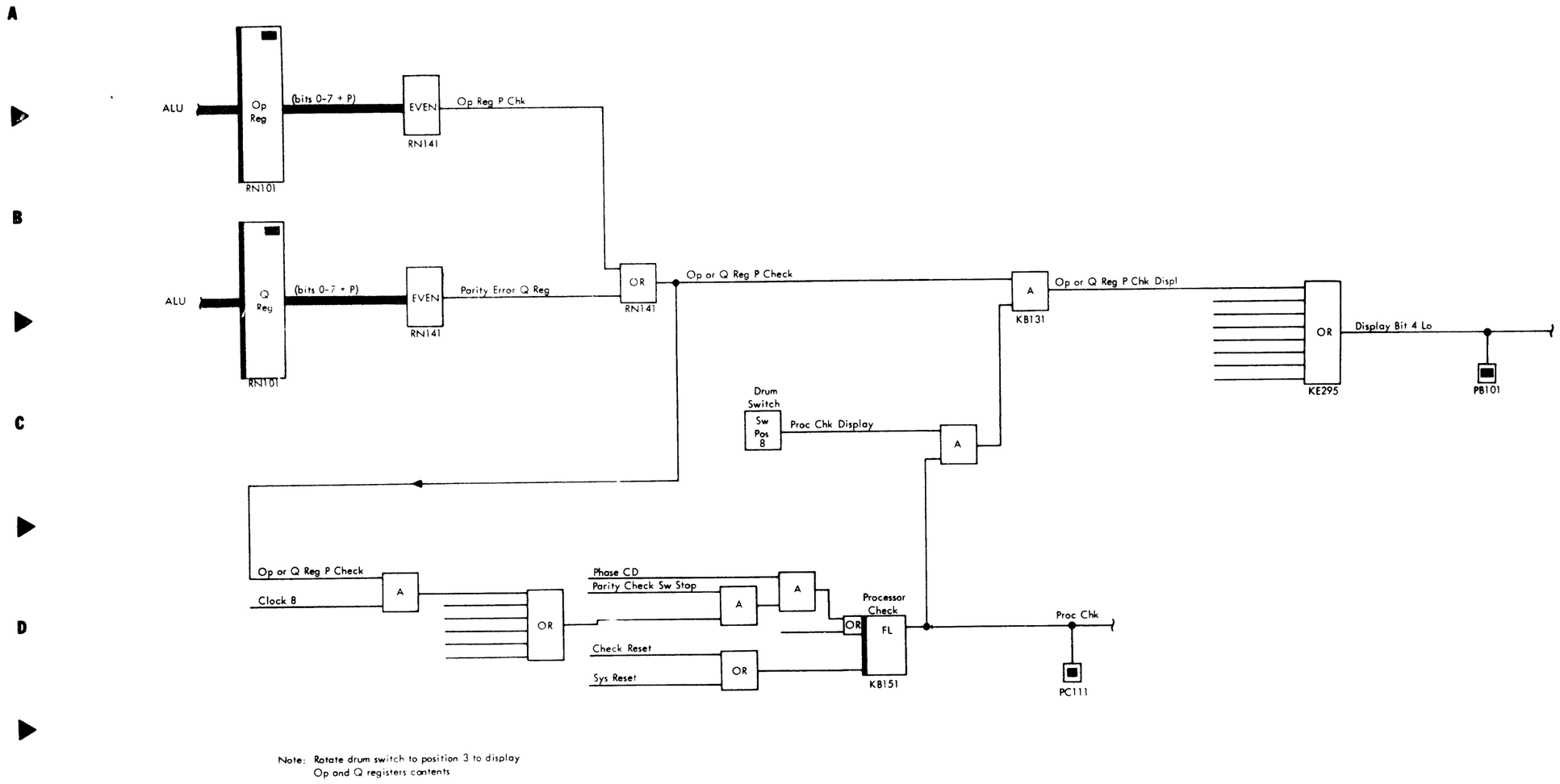


Note: Rotate drum switch to position 5 to display ALU and A register contents

Diagram 2-100. ALU Parity



Note: Rotate drum switch to position 7 to display CS priority bits, position 5 to display ALU output

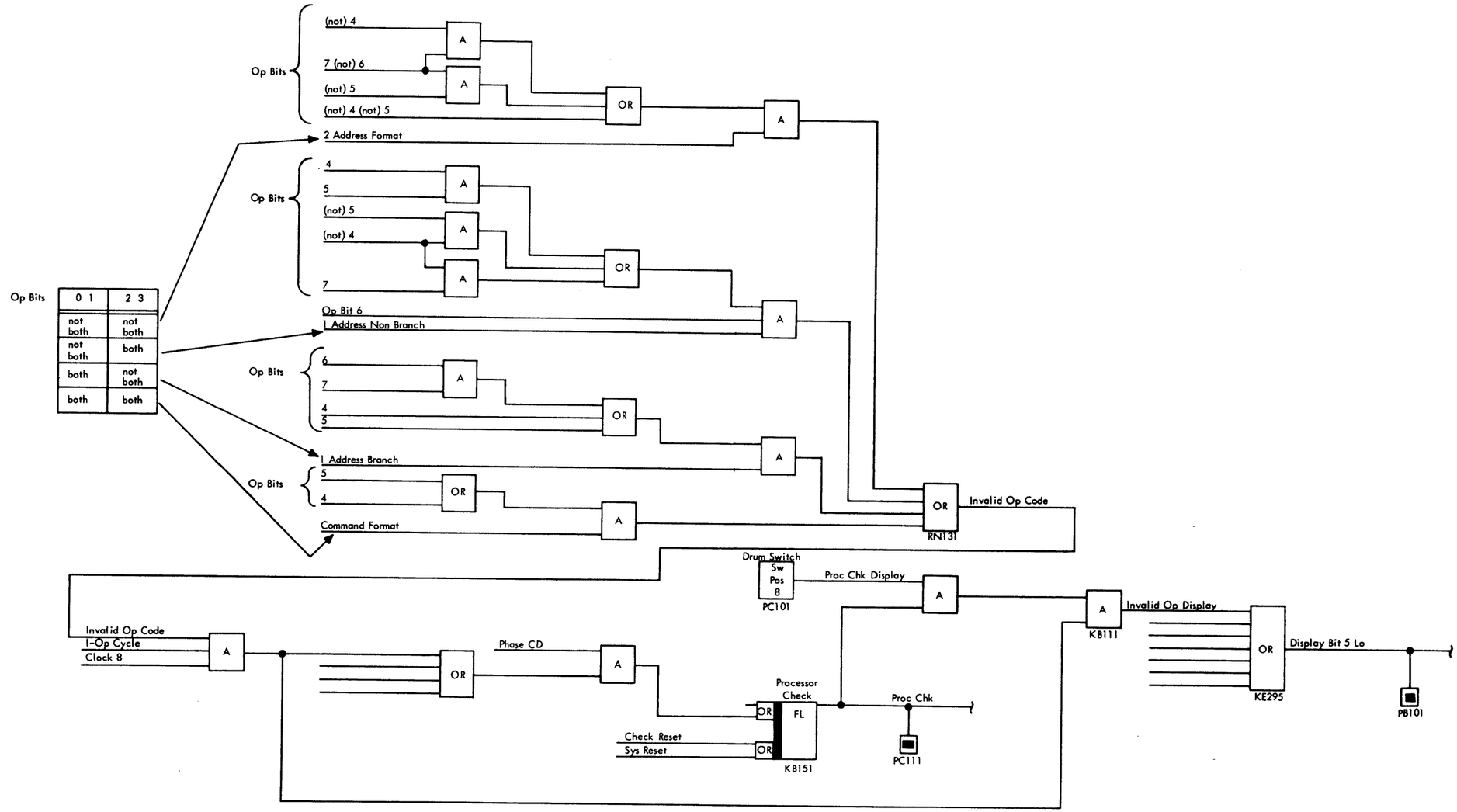


Note: Rotate drum switch to position 3 to display Op and Q registers contents

Diagram 2-120. Op and Q Register Parity

2 3 4 5 6 7 8 9

A B C D E



Note: Rotate drum switch to position 3 to display Op register contents

2 3 4 5 6 7 8 9

A

B

C

D

E

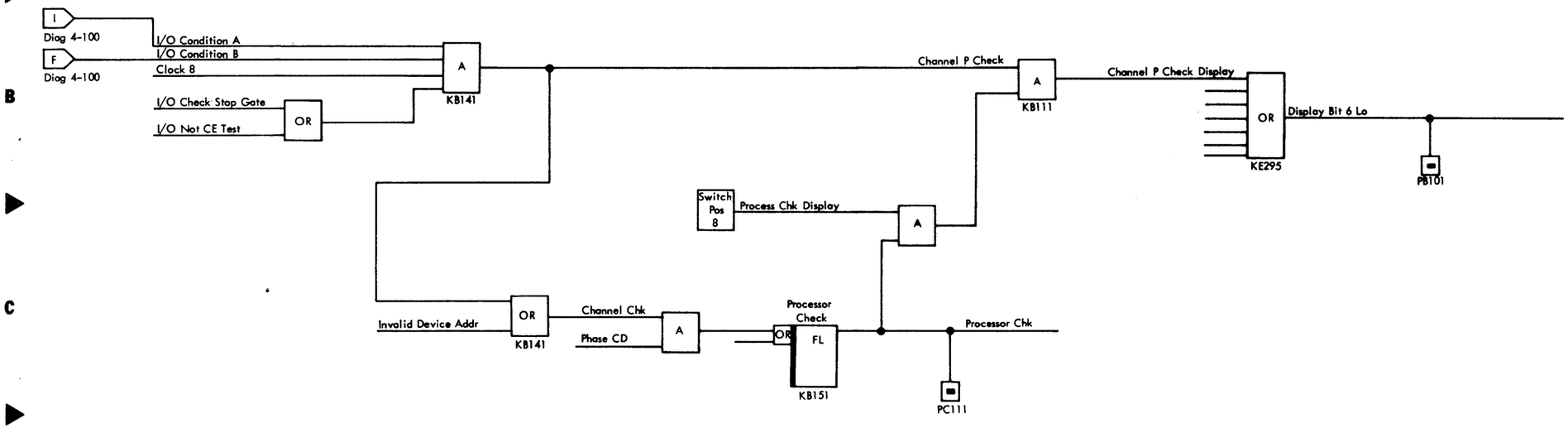


Diagram 2-140. Channel P Check

2 3 4 5 6 7 8 9

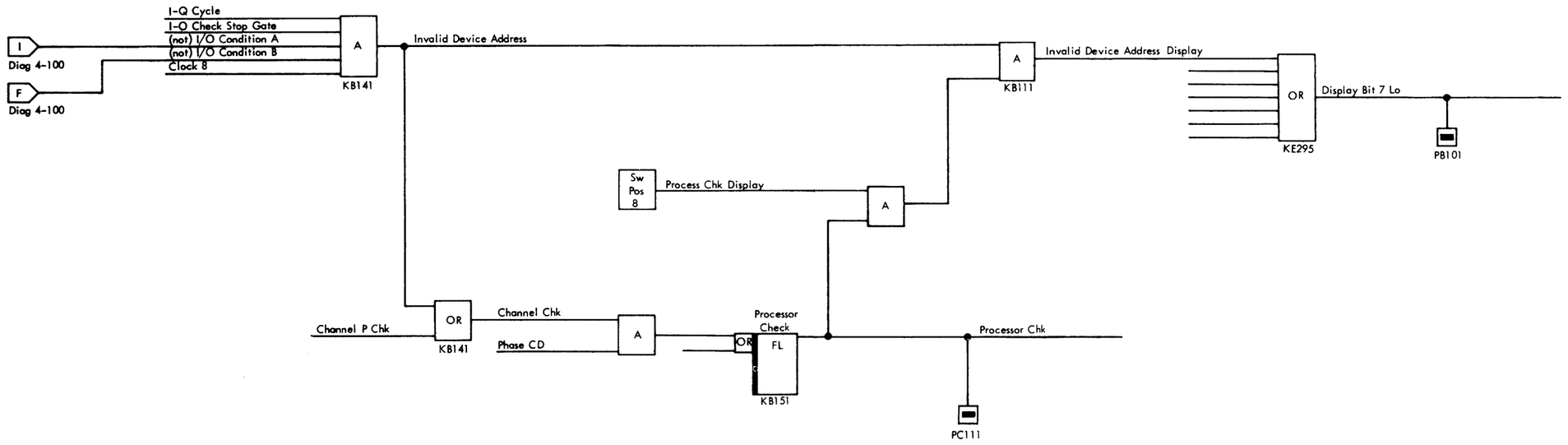
A

B

C

D

E



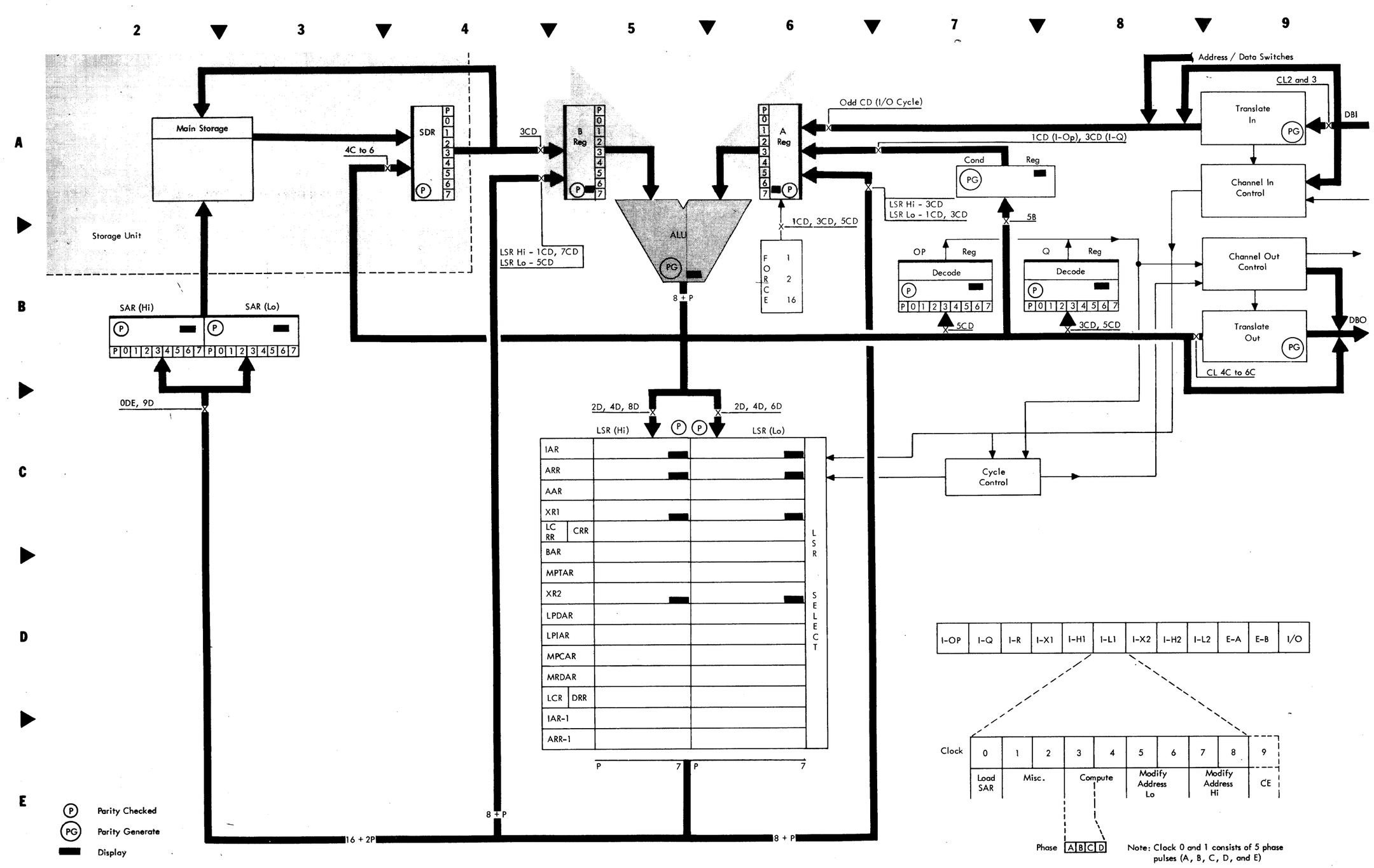
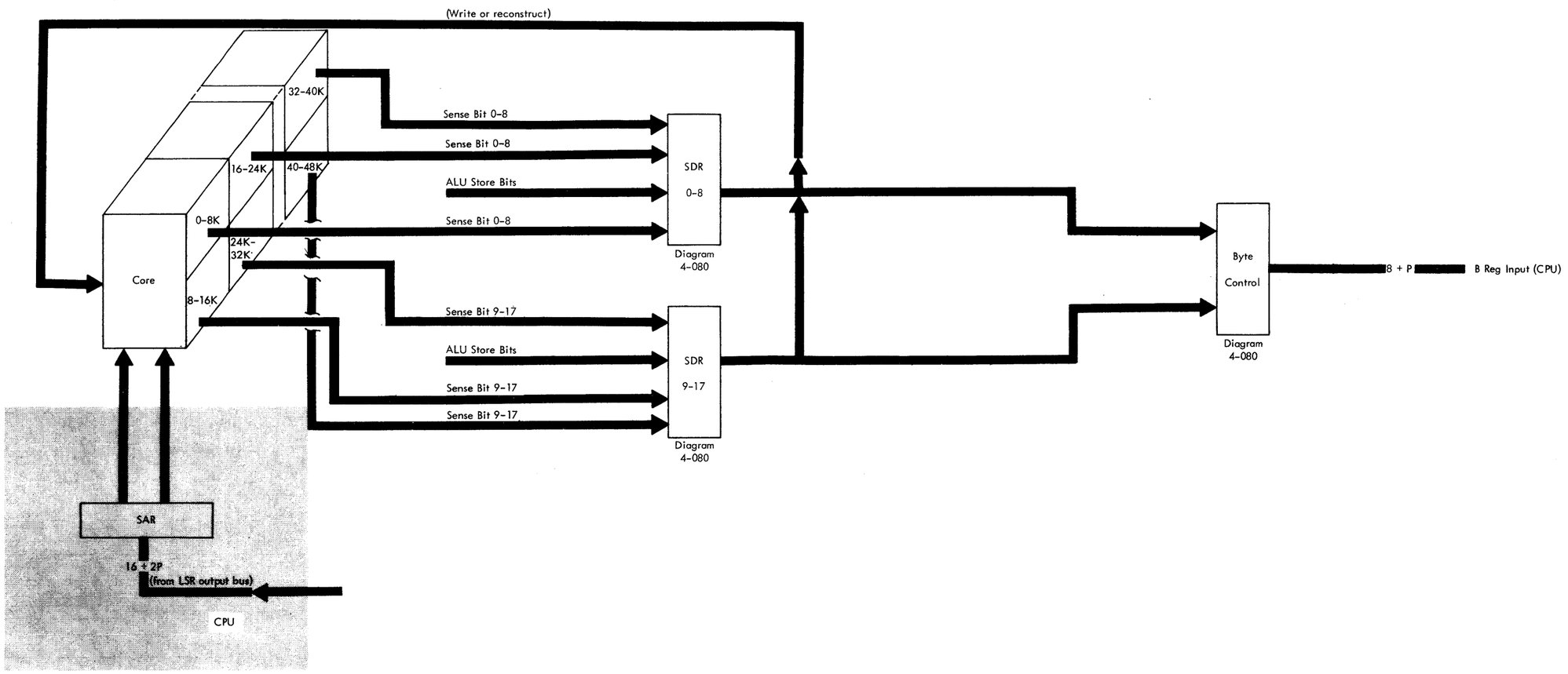


Diagram 3-010. CPU Data Flow

Diagram 3-020. Storage Data Flow



2 3 4 5 6 7 8 9

A

CE Control Panel

P1 On/Off (PA101)
P
P2 On/Off (PA101)

CE Key (PC111)

File Write On/Off (WF020)
(Model D only)

I/O Check Stop/Run (PA101)

Parity Check Run/Stop (PA101)

Storage Test Run/Stop (PA101)

Address Increment Off/On (PA101)

B

Address Complement Stop/RU

Address Complement Stop/Run (PA101)

System Reset (+)/(-) (PC101)

Check Reset (+) (PC101)

LSR Display Selector (PC111)

CE Mode Selector (PA101)

Address Compare Light (PB121)

I/O Check Light (PB121)

C

D

E

CPU Display Panel

Lamp Test Switch (YA102)

Rotary Switch (PA111)

Register Display (PC101)

Drum Indicators (PB101)

Emergency Power Off (YA102)

Meter Panel (YA104)

System Control (PC111)

Power On/Off

Start (+)/(-)

Stop

Load (+)/(-)

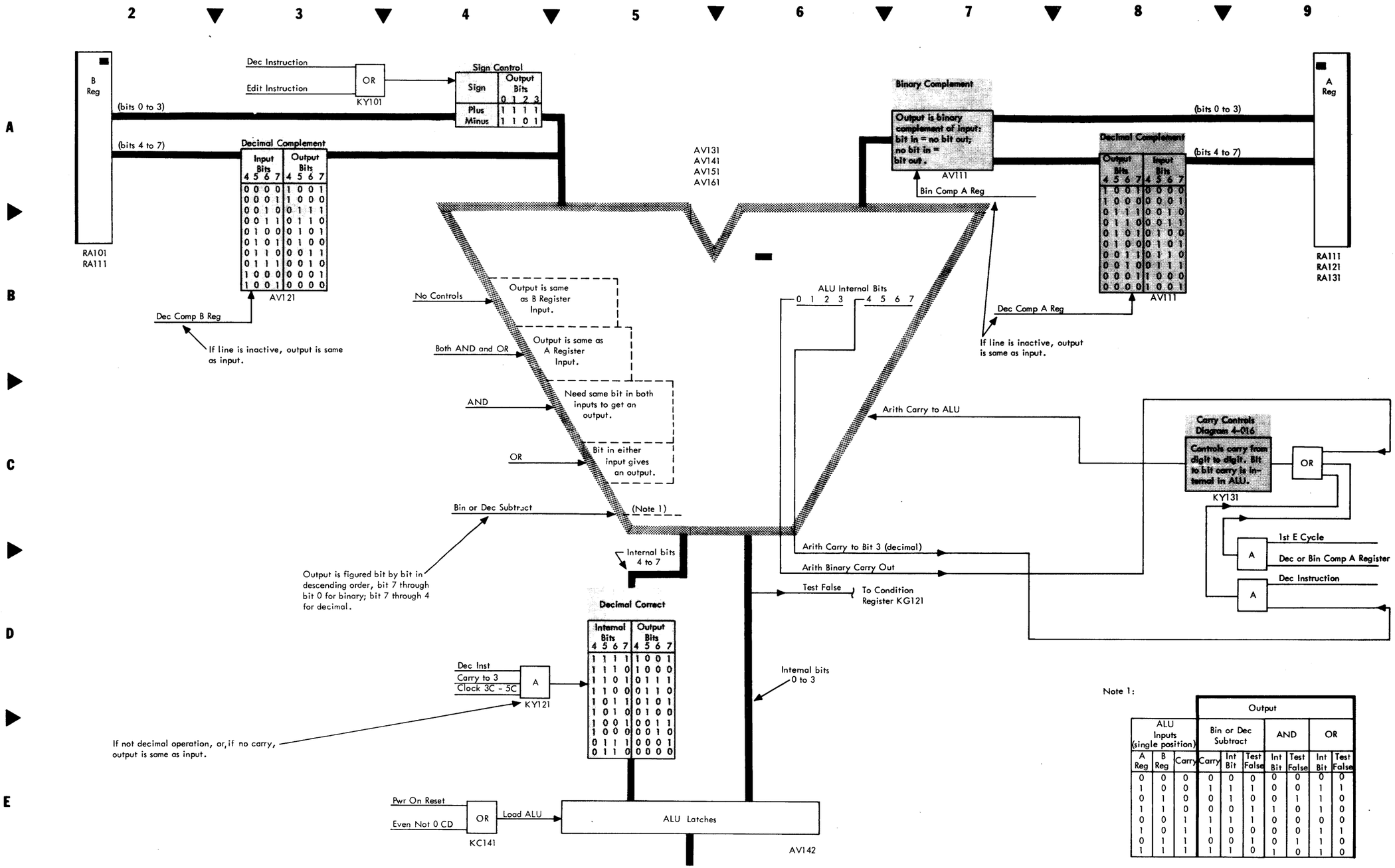
Processor Check Light

I/O Attention Light

Stop Light

Dual Program Control Panel (PC121)

Diagram 4-005. CPU Control Panel



Note 1:

ALU Inputs (single position)			Output						
			Bin or Dec Subtract			AND		OR	
A Reg	B Reg	Carry	Carry	Int Bit	Test False	Int Bit	Test False	Int Bit	Test False
0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	0	1	1
0	1	0	0	1	0	0	1	1	0
1	1	0	0	0	1	1	0	1	0
0	0	1	1	1	0	0	0	0	0
1	0	1	1	0	1	0	1	1	0
0	1	1	1	0	0	0	1	1	0
1	1	1	1	1	0	1	0	1	0

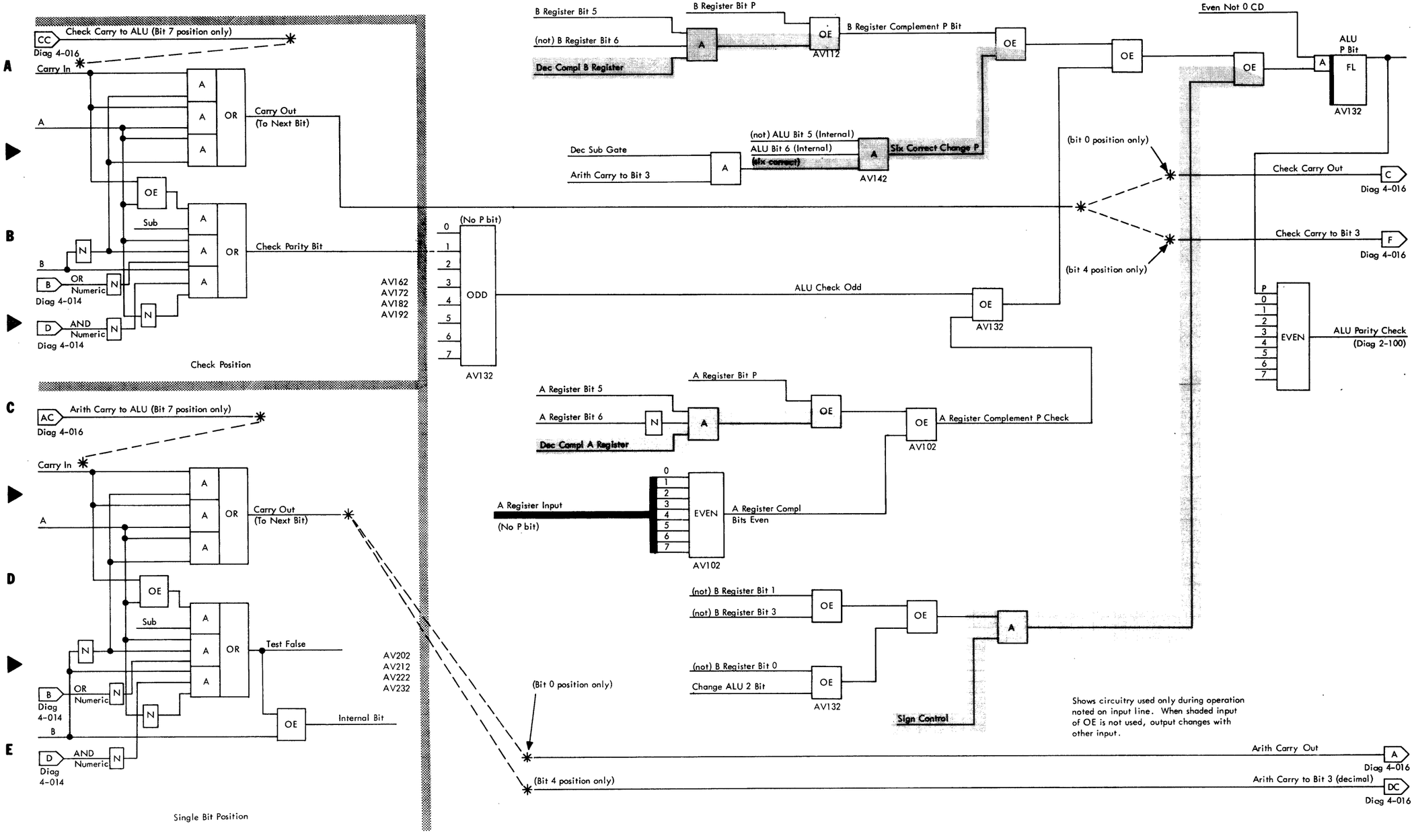
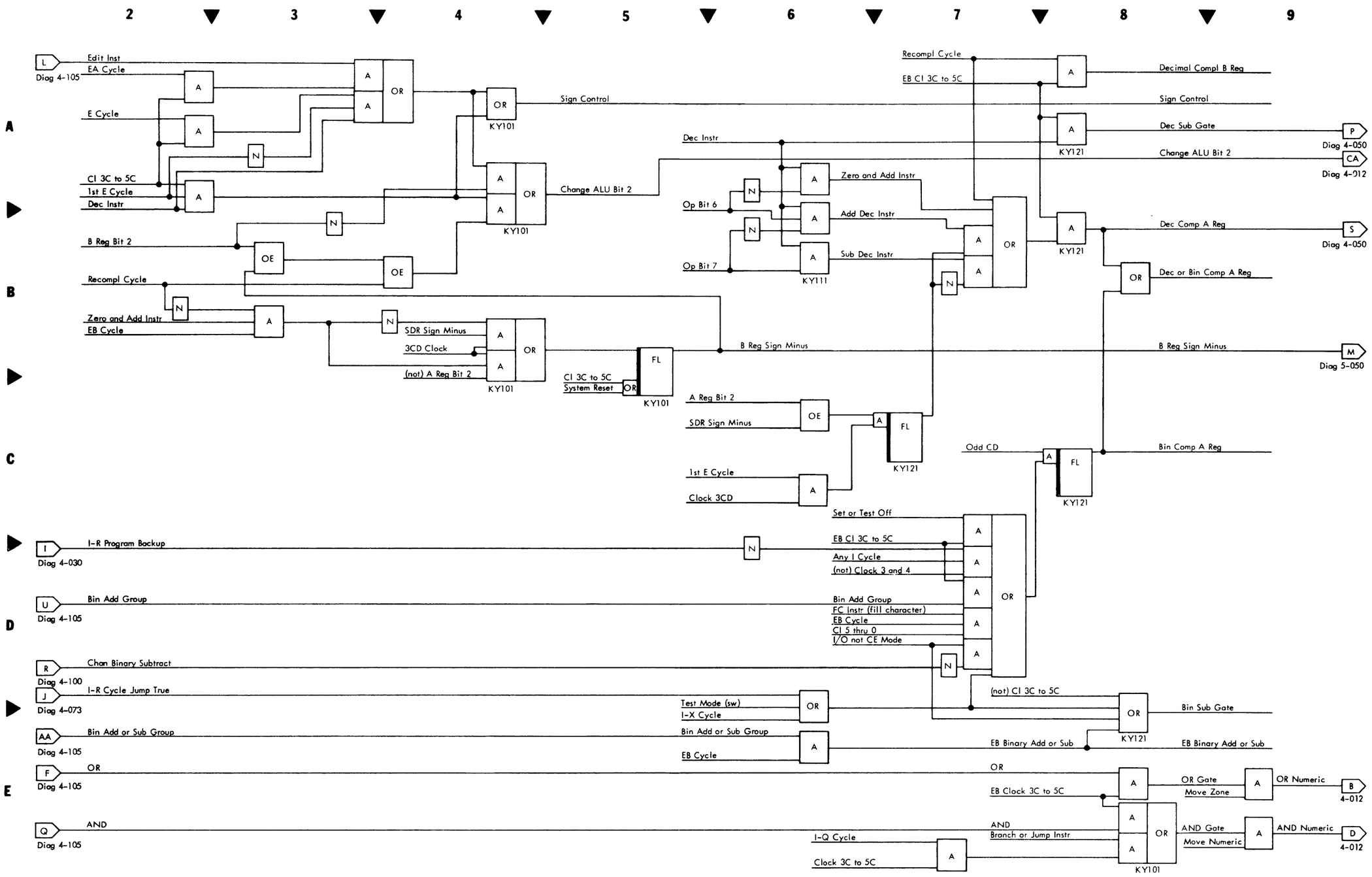


Diagram 4-012. ALU P Bit Generation


2
3
4
5
6
7
8
9
A
B
C
D
E
L
Diag 4-105
Edit Inst
EA Cycle
E Cycle
CI 3C to 5C
1st E Cycle
Dec Instr
B Reg Bit 2
Recompl Cycle
Zero and Add Instr
EB Cycle
SDR Sign Minus
3CD Clock
(not) A Reg Bit 2
CI 3C to 5C
System Reset
KY101
Sign Control
Change ALU Bit 2
Op Bit 6
Op Bit 7
Zero and Add Instr
Add Dec Instr
Sub Dec Instr
KY111
B Reg Sign Minus
A Reg Bit 2
SDR Sign Minus
1st E Cycle
Clock 3CD
Set or Test Off
EB CI 3C to 5C
Any I Cycle
(not) Clock 3 and 4
Recompl Cycle
EB CI 3C to 5C
Decimal Compl B Reg
Sign Control
Dec Sub Gate
Change ALU Bit 2
KY121
Dec Comp A Reg
Dec or Bin Comp A Reg
B Reg Sign Minus
Odd CD
Bin Comp A Reg
I
I-R Program Backup
Diag 4-030
U
Bin Add Group
Diag 4-105
R
Chan Binary Subtract
Diag 4-100
J
I-R Cycle Jump True
Diag 4-073
AA
Bin Add or Sub Group
Diag 4-105
F
OR
Diag 4-105
Q
AND
Diag 4-105
Test Mode (sw)
I-X Cycle
Bin Add or Sub Group
EB Cycle
Bin Add Group
FC Instr (fill character)
EB Cycle
CI 5 thru 0
I/O not CE Mode
I-Q Cycle
Clock 3C to 5C
(not) CI 3C to 5C
Bin Sub Gate
EB Binary Add or Sub
OR
EB Clock 3C to 5C
OR Gate
Move Zone
OR Numeric
AND
Branch or Jump Instr
AND Gate
Move Numeric
AND Numeric
P
Diag 4-050
CA
Diag 4-012
S
Diag 4-050
M
Diag 5-050
B
4-012
D
4-012

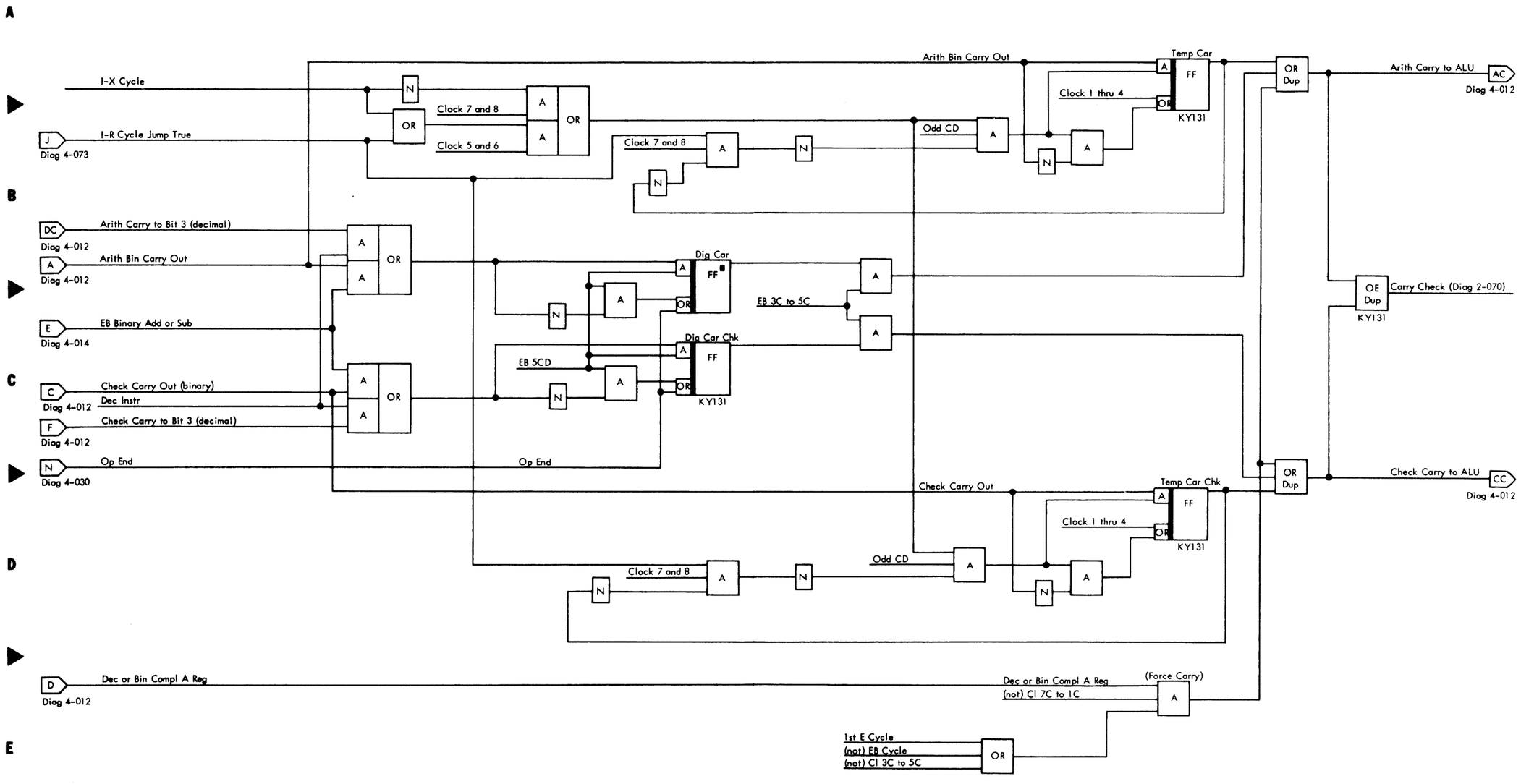
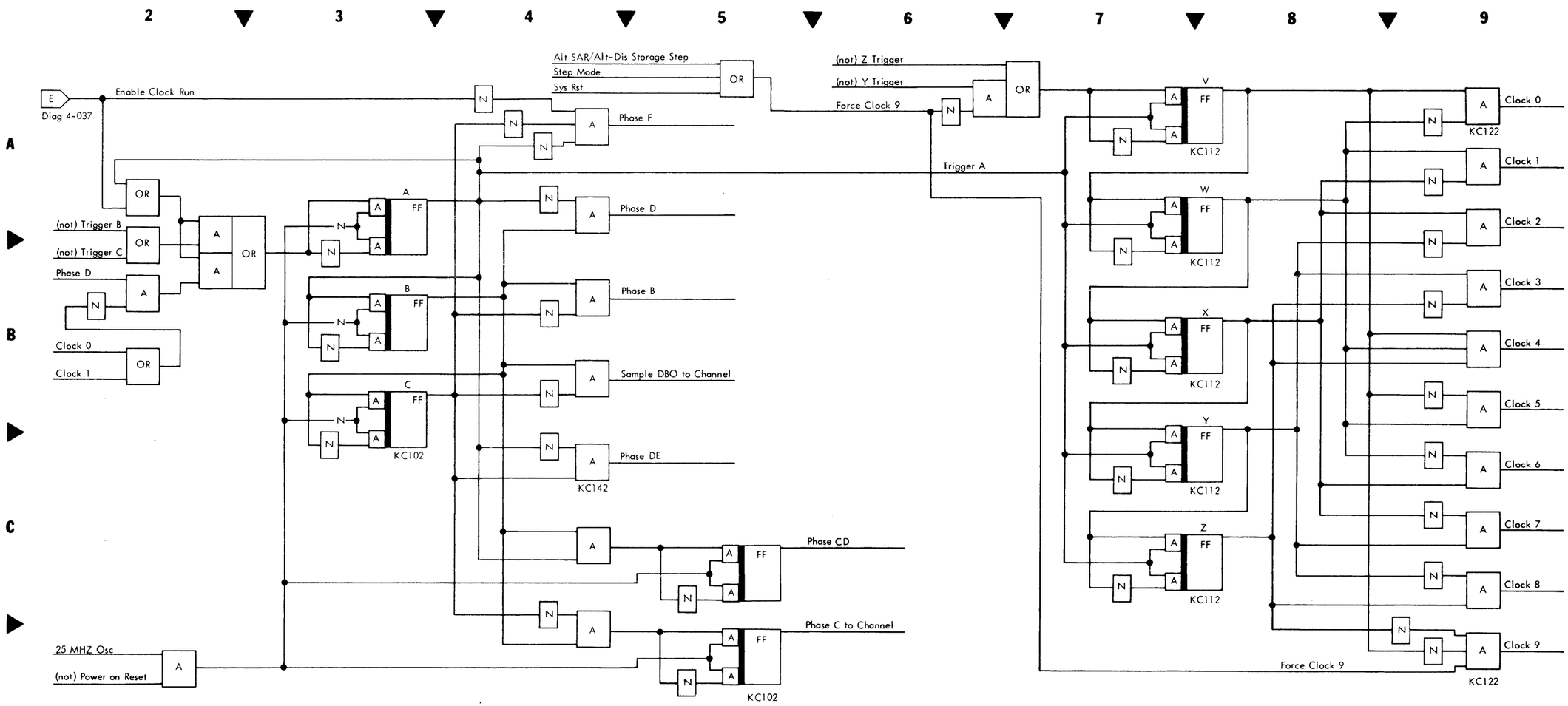


Diagram 4-016. ALU Controls (Part 2 of 2)


2
3
4
5
6
7
8
9
A
B
C
D
E
E
Diag 4-037
Enable Clock Run
Alt SAR/Alt-Dis Storage Step
Step Mode
Sys Rst
(not) Z Trigger
(not) Y Trigger
Force Clock 9
Trigger A
(not) Trigger B
(not) Trigger C
Phase D
Clock 0
Clock 1
Phase F
Phase D
Phase B
Sample DBO to Channel
Phase DE
Phase CD
Phase C to Channel
KC102
KC142
KC112
KC122
25 MHZ Osc
(not) Power on Reset
Force Clock 9
Clock 0
Clock 1
Clock 2
Clock 3
Clock 4
Clock 5
Clock 6
Clock 7
Clock 8
Clock 9
Cl 0
Cl 1
Cl 2
Cl 3
Cl 4
Cl 8
Cl 9
25 MHZ Osc
Enable Clock Run
Trigger A
B
C
Phase A
B
C
D
E
F
40 ns
200 ns
200 ns
160 ns
160 ns
160 ns
Trigger
V
W
X
Y
Z
Clock
0
1
2
3
4
5
6
7
8
9

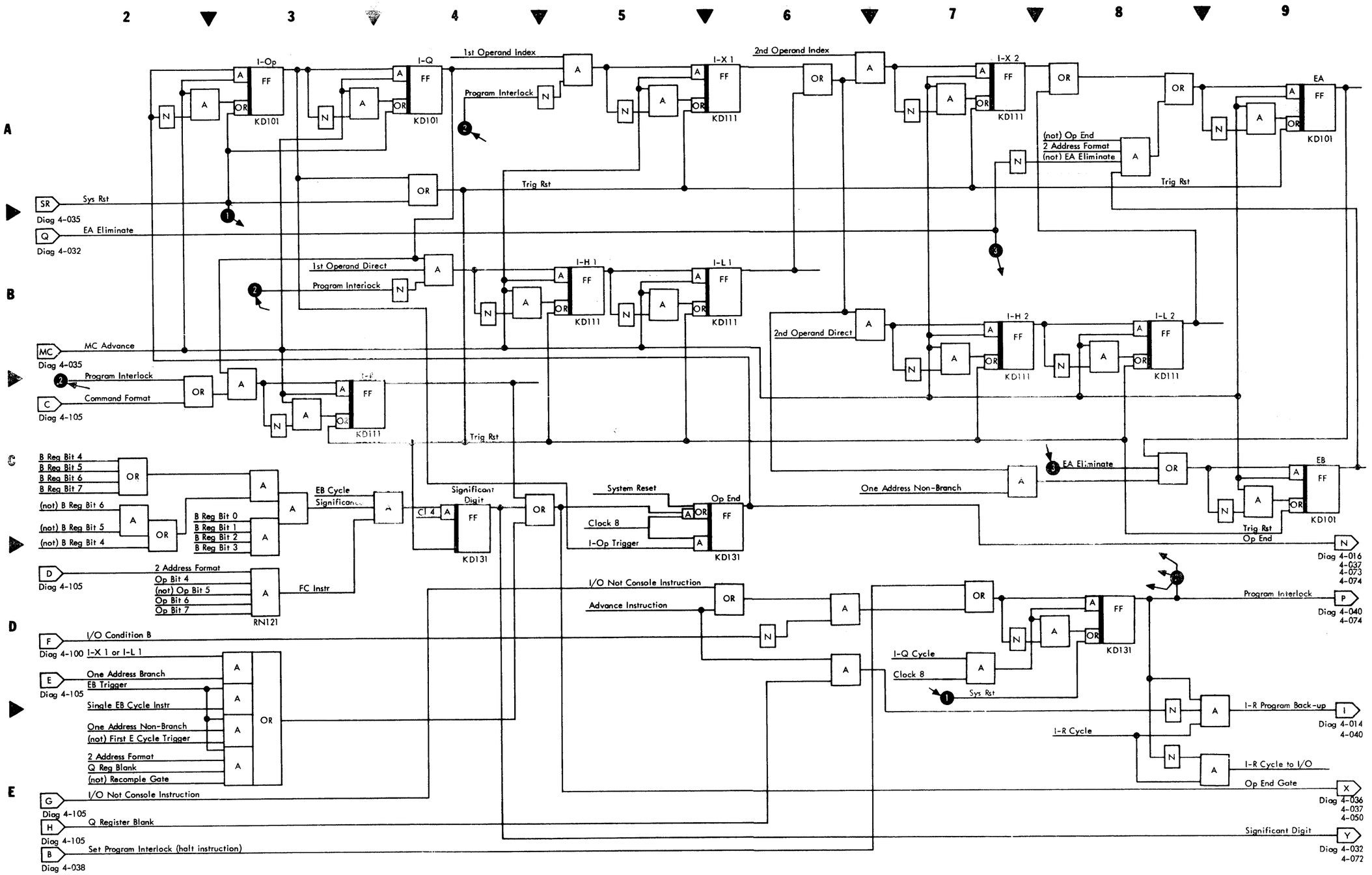
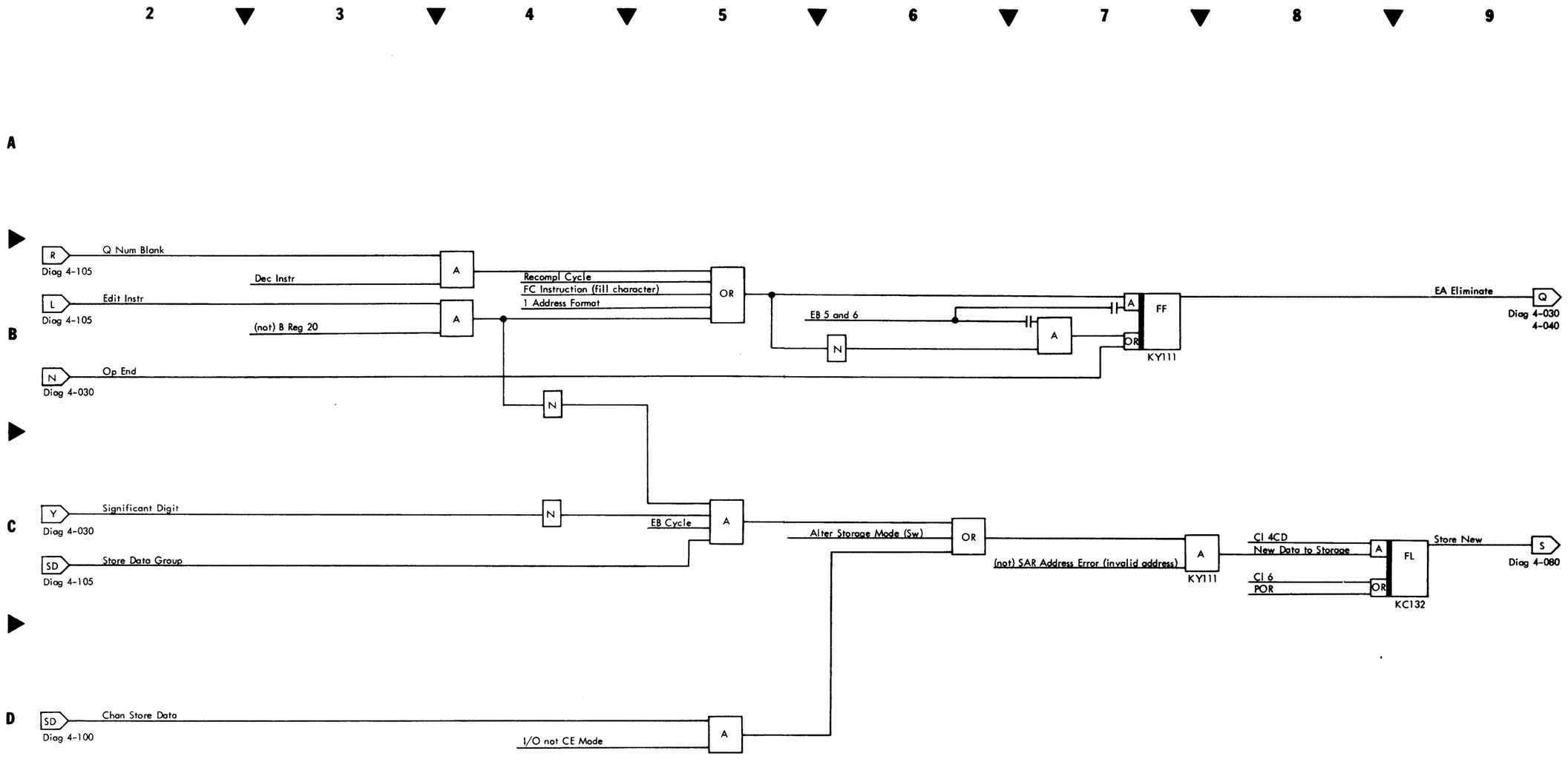


Diagram 4-030. Cycle Controls (Part 1 of 2)


2
3
4
5
6
7
8
9
A
B
C
D
E
R
Q Num Blank
Diag 4-105
Dec Instr
A
L
Edit Instr
Diag 4-105
(not) B Reg 20
A
Recompl Cycle
FC Instruction (fill character)
1 Address Format
OR
EB 5 and 6
N
A
A
FF
OR
KY111
EA Eliminate
Q
Diag 4-030
4-040
N
Op End
Diag 4-030
N
Y
Significant Digit
Diag 4-030
N
EB Cycle
A
Alter Storage Mode (Sw)
OR
(not) SAR Address Error (invalid address)
A
KY111
CI 4CD
New Data to Storage
CI 6
POR
A
OR
FL
KC132
Store New
S
Diag 4-080
SD
Store Data Group
Diag 4-105
SD
Chan Store Data
Diag 4-100
I/O not CE Mode
A

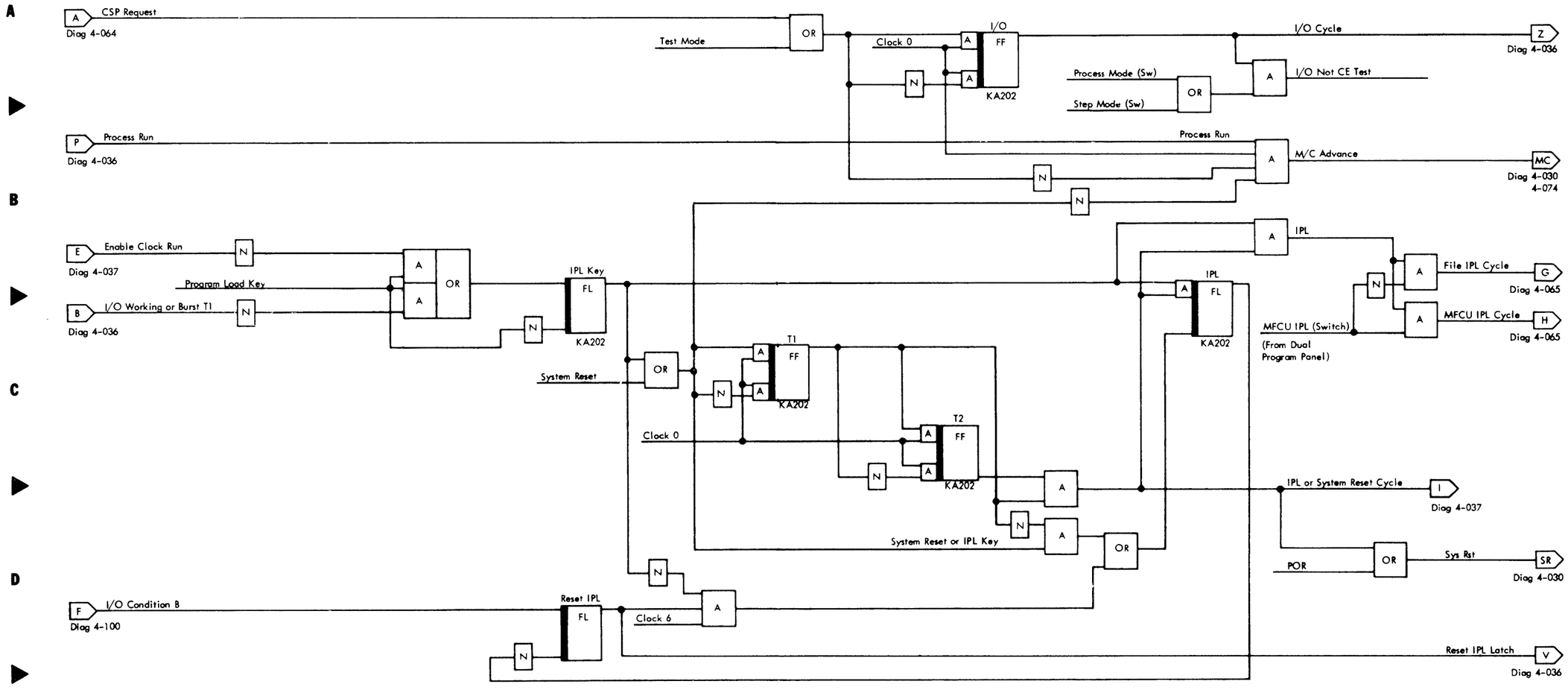
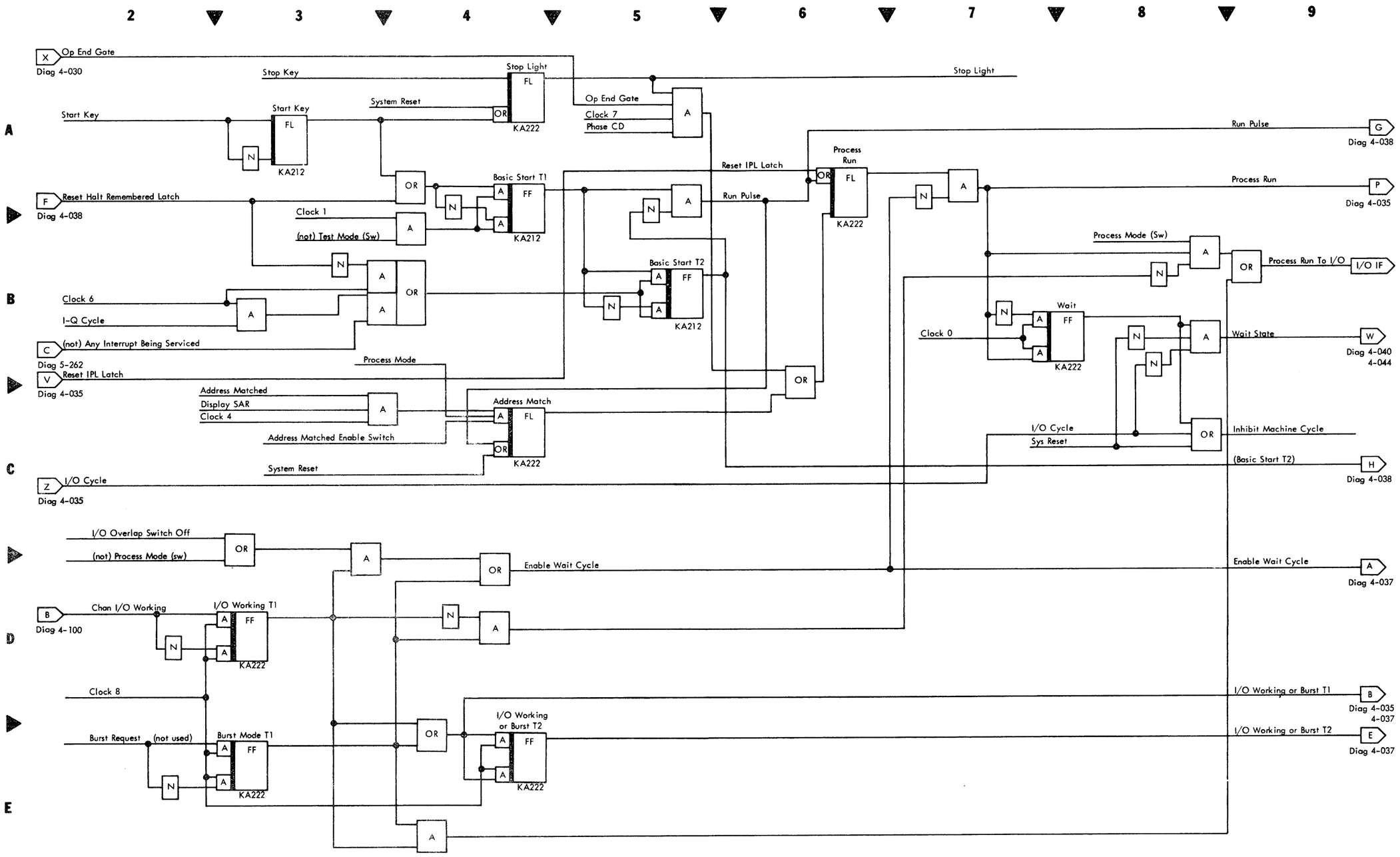


Diagram 4-035. Run Controls (Part 1 of 4)


2
3
4
5
6
7
8
9
A
B
C
D
E
X Op End Gate
Diag 4-030
Stop Key
Stop Light
FL
System Reset
OR
KA222
Op End Gate
Clock 7
Phase CD
A
Stop Light
Start Key
Start Key
FL
N
KA212
Run Pulse
G
Diag 4-038
Process Run
OR
FL
KA222
Reset IPL Latch
Run Pulse
F Reset Halt Remembered Latch
Diag 4-038
OR
Basic Start T1
A
FF
A
KA212
N
A
Clock 1
(not) Test Mode (Sw)
A
N
A
A
OR
Process Run
P
Diag 4-035
Process Mode (Sw)
A
N
OR
Process Run To I/O
I/O IF
Basic Start T2
A
FF
A
KA212
N
Clock 6
I-Q Cycle
A
N
A
Wait
FF
KA222
Clock 0
Wait State
W
Diag 4-040
4-044
C (not) Any Interrupt Being Serviced
Diag 5-262
V Reset IPL Latch
Diag 4-035
Process Mode
OR
Address Matched
Display SAR
Clock 4
A
Address Match
A
FL
OR
KA222
Address Matched Enable Switch
System Reset
I/O Cycle
Sys Reset
OR
Inhibit Machine Cycle
(Basic Start T2)
H
Diag 4-038
Z I/O Cycle
Diag 4-035
I/O Overlap Switch Off
(not) Process Mode (sw)
OR
A
OR
Enable Wait Cycle
Enable Wait Cycle
A
Diag 4-037
B Chan I/O Working
Diag 4-100
I/O Working T1
A
FF
A
KA222
N
N
A
Clock 8
I/O Working or Burst T1
B
Diag 4-035
4-037
Burst Request
(not used)
Burst Mode T1
A
FF
A
KA222
N
OR
I/O Working
or Burst T2
A
FF
A
KA222
I/O Working or Burst T2
E
Diag 4-037
A

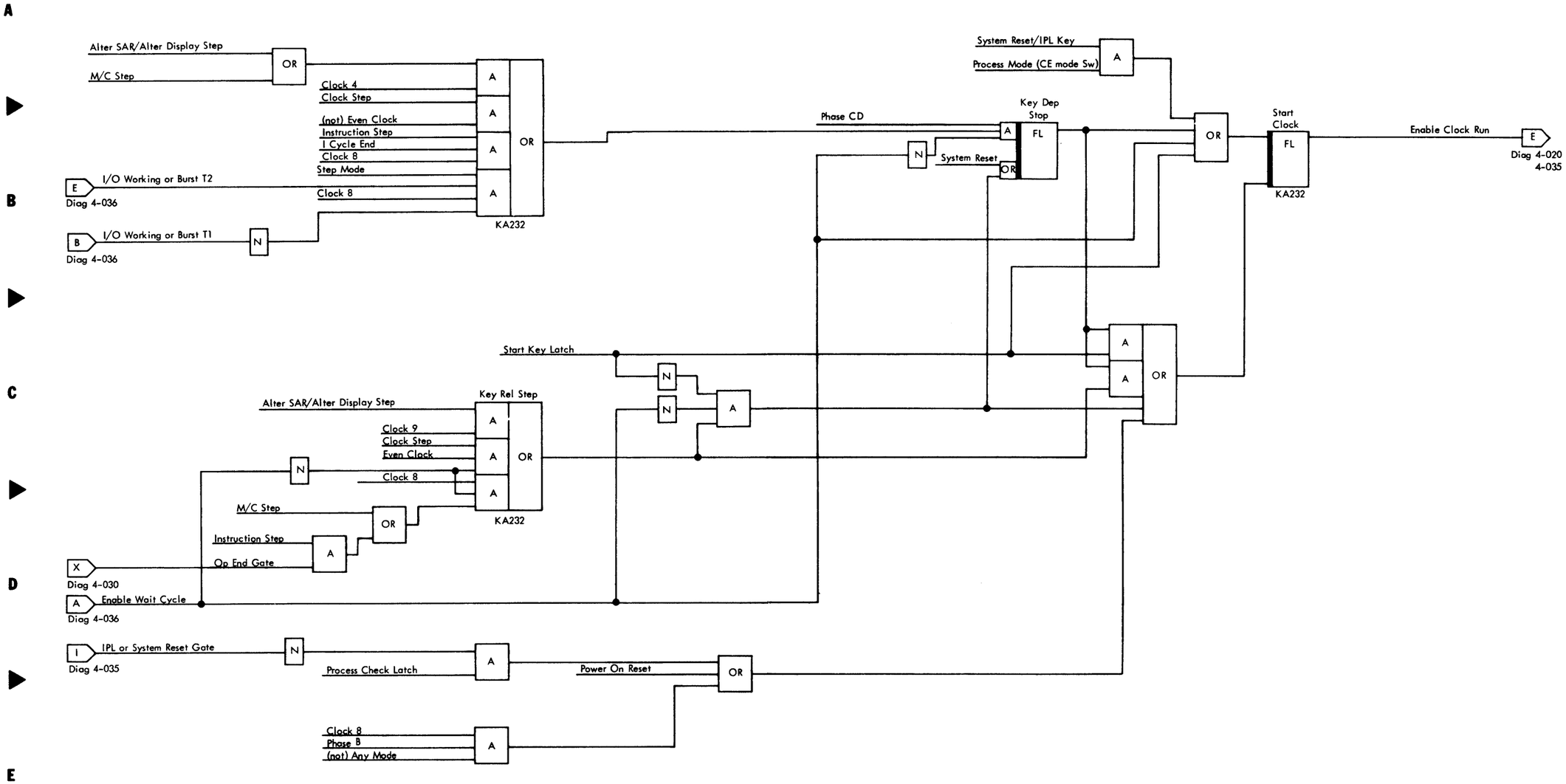
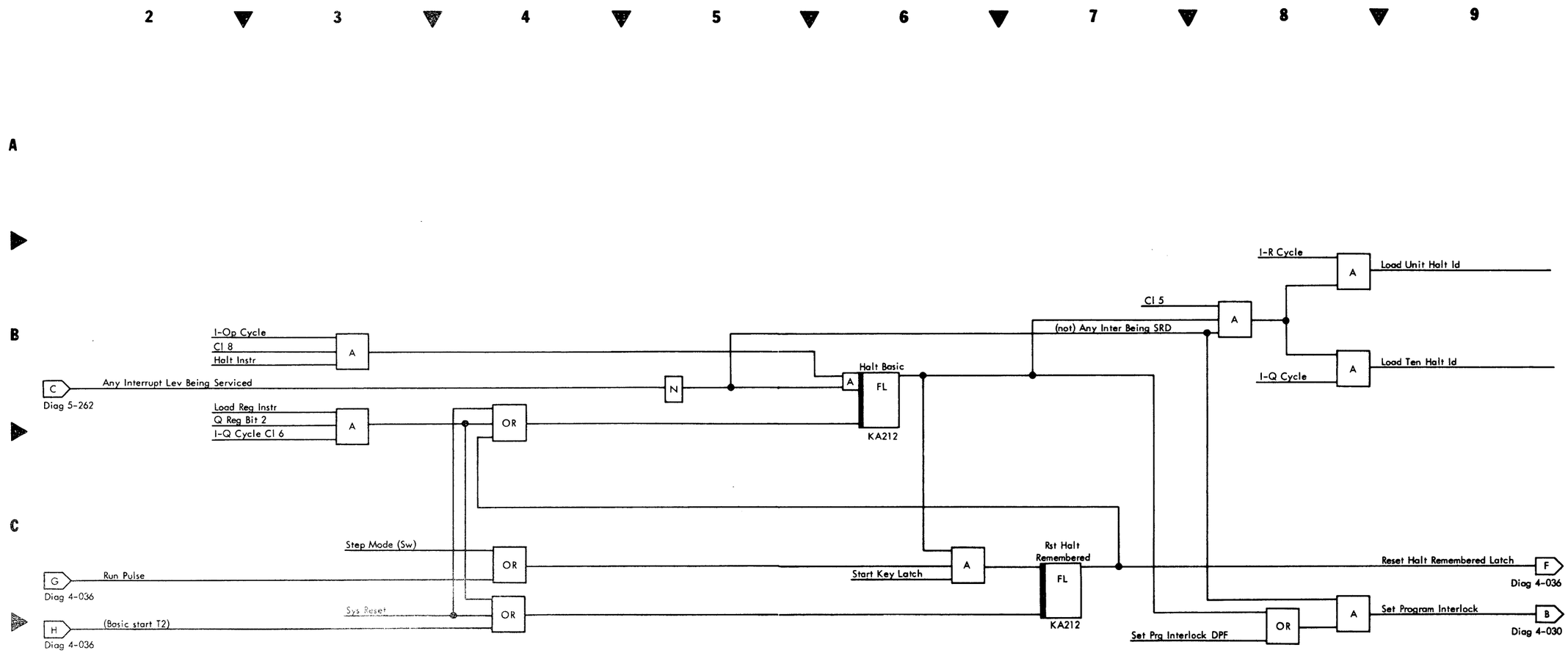


Diagram 4-037. Run Controls (Part 3 of 4)


2
3
4
5
6
7
8
9
A
B
C
D
E
1-Op Cycle
Cl 8
Halt Instr
A
C
Any Interrupt Lev Being Serviced
Diag 5-262
N
Load Reg Instr
Q Reg Bit 2
1-Q Cycle Cl 6
A
OR
Halt Basic
A
FL
KA212
Cl 5
(not) Any Inter Being SRD
A
1-R Cycle
A
Load Unit Halt Id
1-Q Cycle
A
Load Ten Halt Id
Step Mode (Sw)
OR
G
Run Pulse
Diag 4-036
Sys Reset
OR
H
(Basic start T2)
Diag 4-036
Start Key Latch
A
Rst Halt
Remembered
FL
KA212
Reset Halt Remembered Latch
F
Diag 4-036
Set Prg Interlock DPF
OR
A
Set Program Interlock
B
Diag 4-030

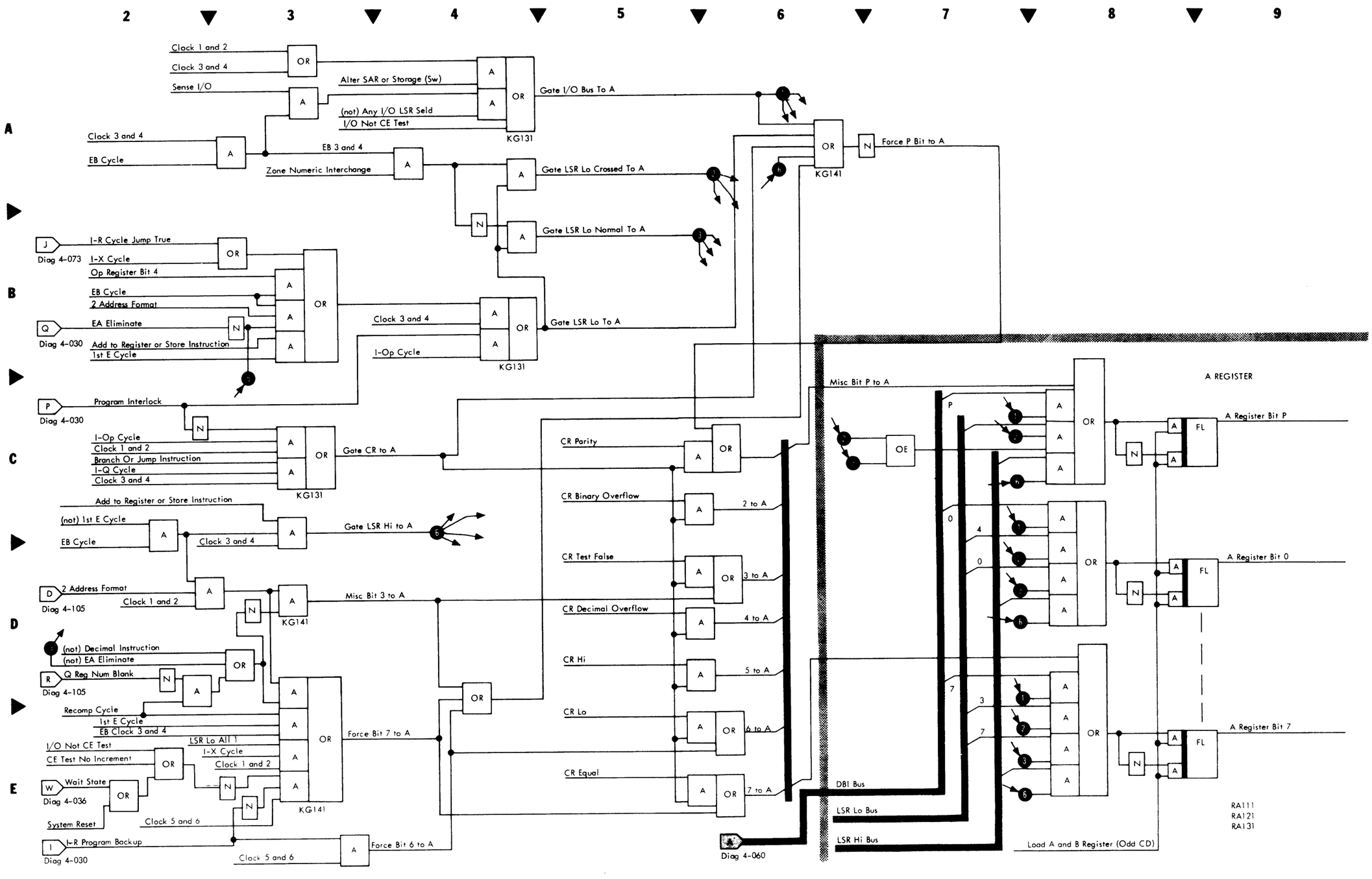
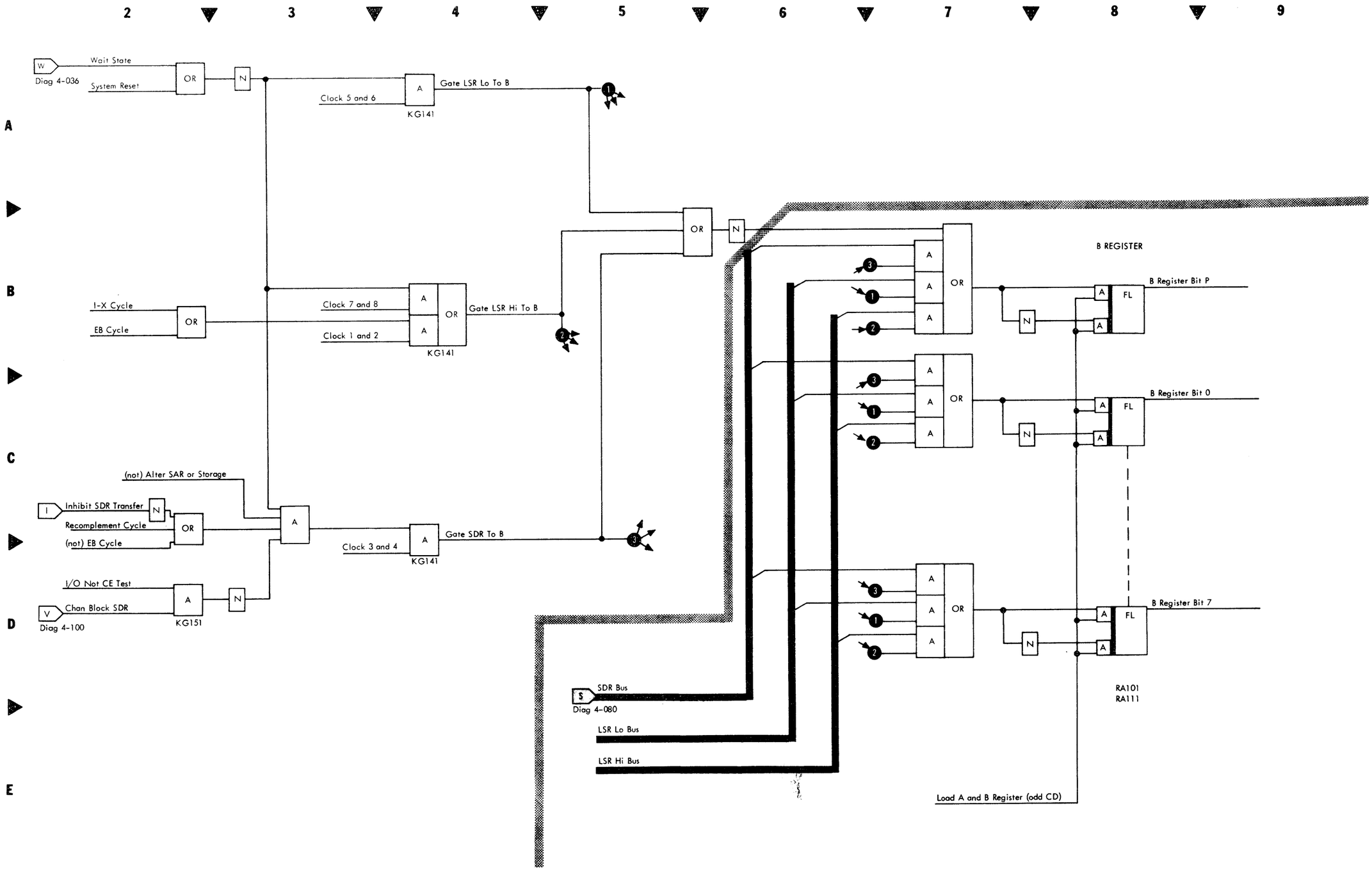
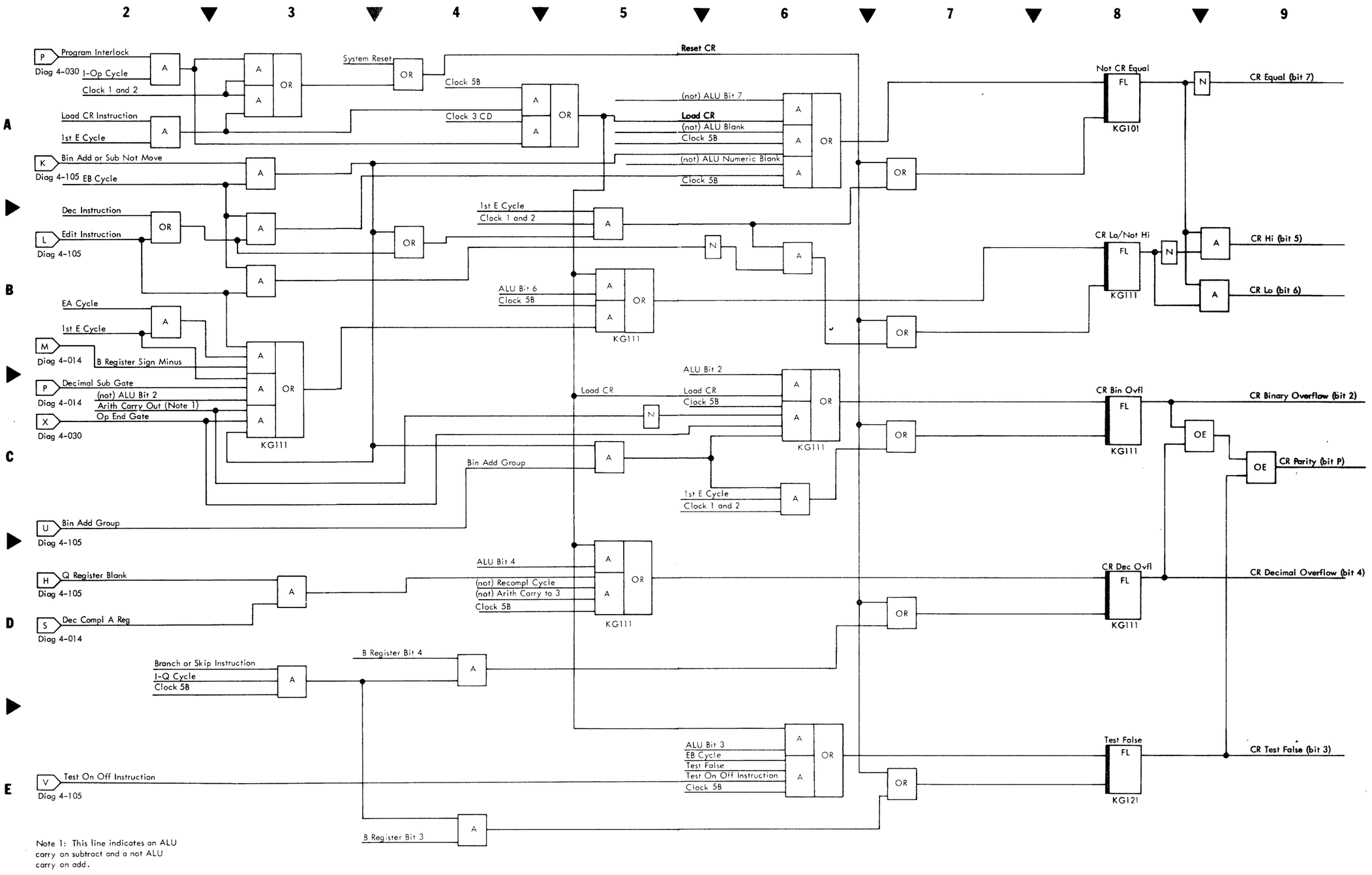


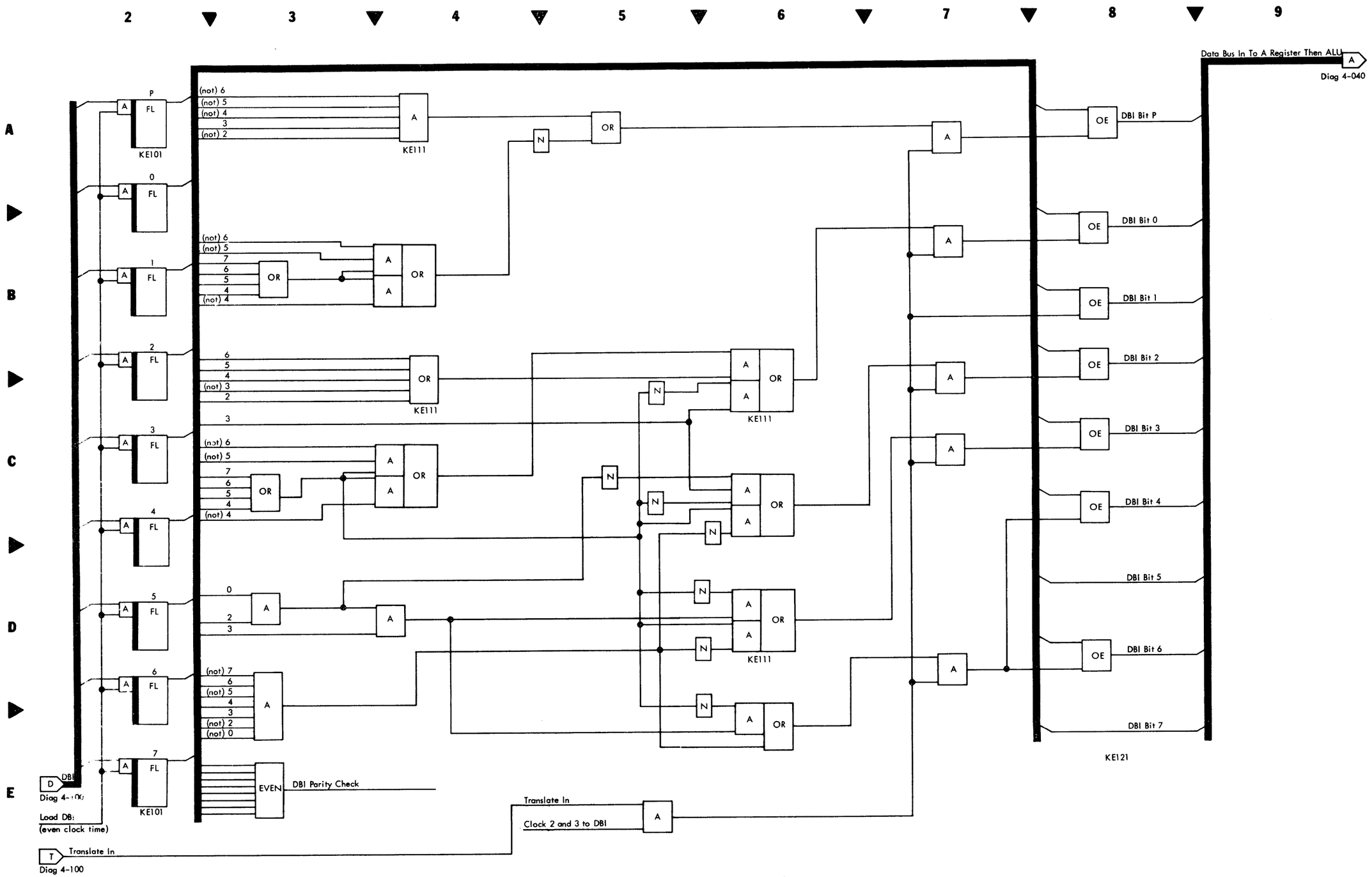
Diagram 4-040. A Register Controls

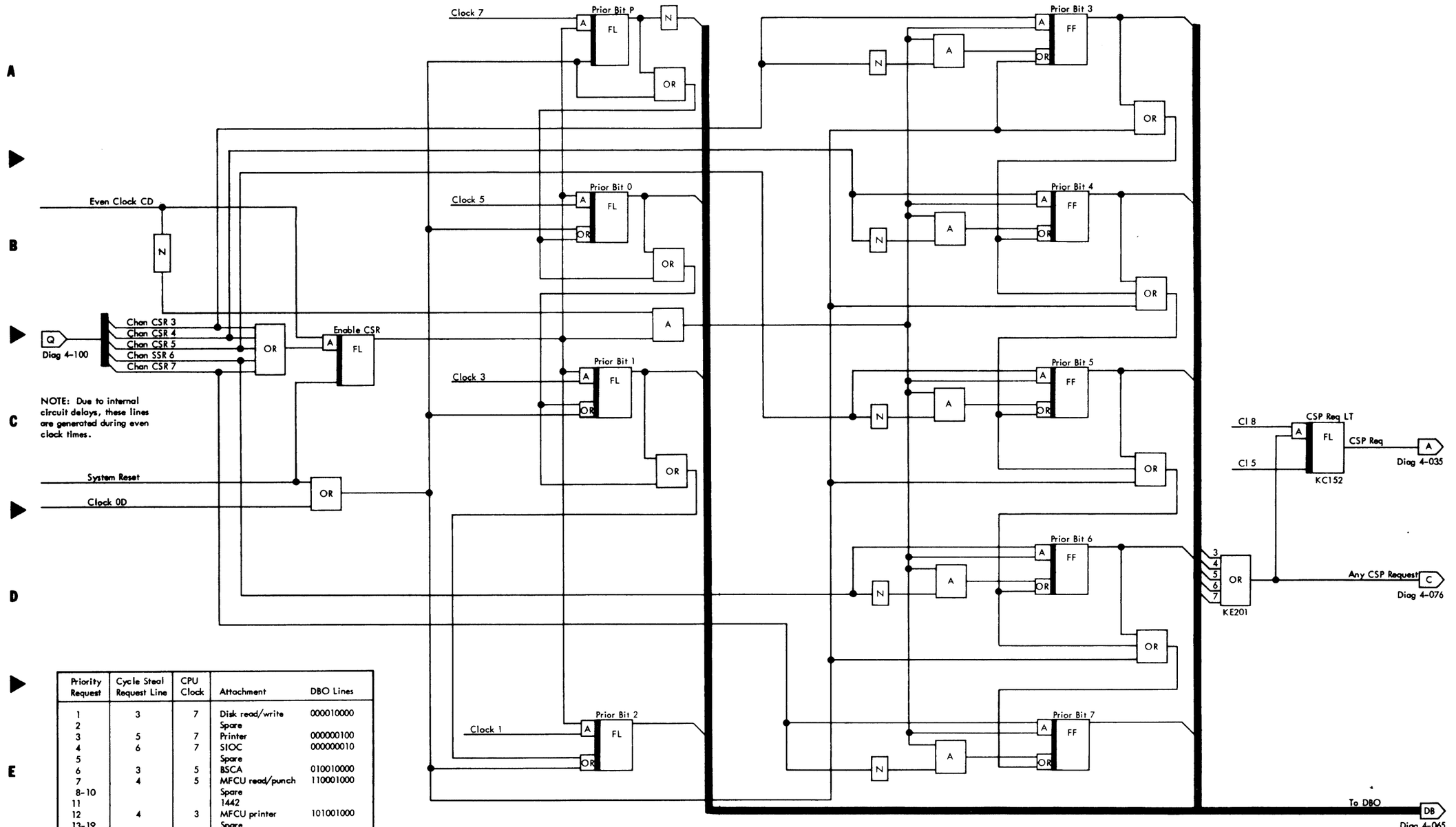

2
3
4
5
6
7
8
9
A
B
C
D
E
W
Diag 4-036
Wait State
System Reset
OR
N
Clock 5 and 6
A
Gate LSR Lo To B
KG141
1-X Cycle
EB Cycle
OR
Clock 7 and 8
Clock 1 and 2
A
A
OR
Gate LSR Hi To B
KG141
(not) Alter SAR or Storage
I
Inhibit SDR Transfer
Recomplement Cycle
(not) EB Cycle
N
OR
A
Clock 3 and 4
A
Gate SDR To B
KG141
I/O Not CE Test
V
Chan Block SDR
Diag 4-100
A
KG151
N
OR
N
B REGISTER
A
A
A
OR
B Register Bit P
FL
N
A
A
A
OR
B Register Bit 0
FL
N
A
A
A
OR
B Register Bit 7
FL
N
RA101
RA111
S
SDR Bus
Diag 4-080
LSR Lo Bus
LSR Hi Bus
Load A and B Register (odd CD)



Note 1: This line indicates an ALU carry on subtract and a not ALU carry on add.

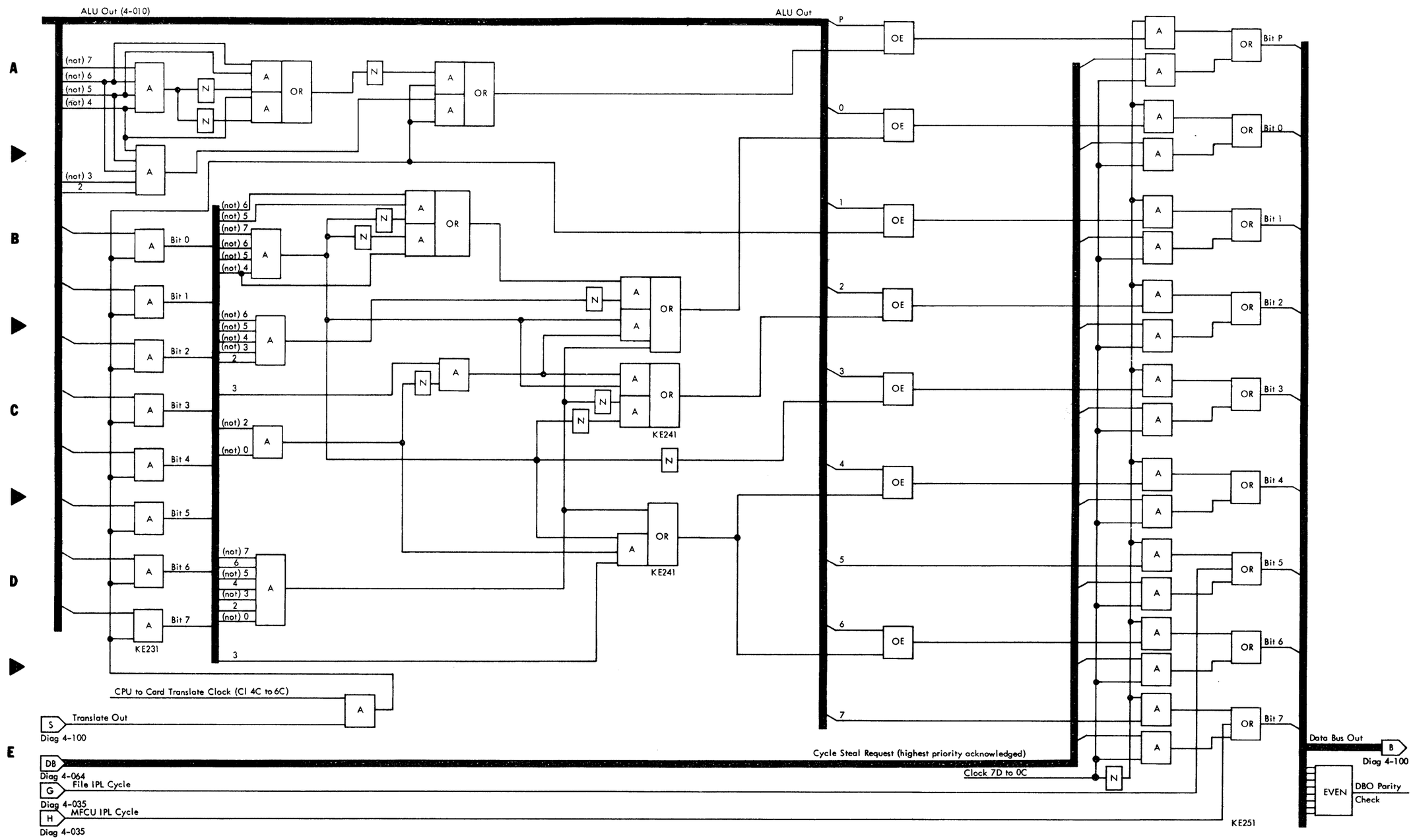
Diagram 4-050. Condition Register


2
3
4
5
6
7
8
9
A
B
C
D
E
Data Bus In To A Register Then ALU
A
Diag 4-040
P
FL
KE101
(not) 6
(not) 5
(not) 4
3
(not) 2
A
KE111
N
OR
OE
DBI Bit P
0
1
7
6
5
4
DBI Bit 0
DBI Bit 1
2
3
DBI Bit 2
DBI Bit 3
4
DBI Bit 4
5
DBI Bit 5
6
DBI Bit 6
7
DBI Bit 7
KE121
EVEN
DBI Parity Check
D
DBI
Load DBI
(even clock time)
Translate In
Clock 2 and 3 to DBI
T
Translate In
Diag 4-100



Priority Request	Cycle Steal Request Line	CPU Clock	Attachment	DBO Lines
1	3	7	Disk read/write	000010000
2			Spare	
3	5	7	Printer	000000100
4	6	7	SIOC	000000010
5			Spare	
6	3	5	BSCA	010010000
7	4	5	MFCU read/punch	110001000
8-10			Spare	
11			1442	
12	4	3	MFCU printer	101001000
13-19			Spare	
20	7	1	Disk control	100100001

Diagram 4-064. Cycle Steal Request Priority Assignment


2
3
4
5
6
7
8
9
A
B
C
D
E
ALU Out (4-010)
ALU Out
(not) 7
(not) 6
(not) 5
(not) 4
(not) 3
2
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
KE231
KE241
KE241
KE251
A
N
OR
OE
P
0
1
2
3
4
5
6
7
Bit P
CPU to Card Translate Clock (C1 4C to 6C)
S
Translate Out
Diag 4-100
DB
Diag 4-064
File IPL Cycle
G
Diag 4-035
MFCU IPL Cycle
H
Diag 4-035
Cycle Steal Request (highest priority acknowledged)
Clock 7D to 0C
Data Bus Out
B
Diag 4-100
EVEN
DBO Parity
Check

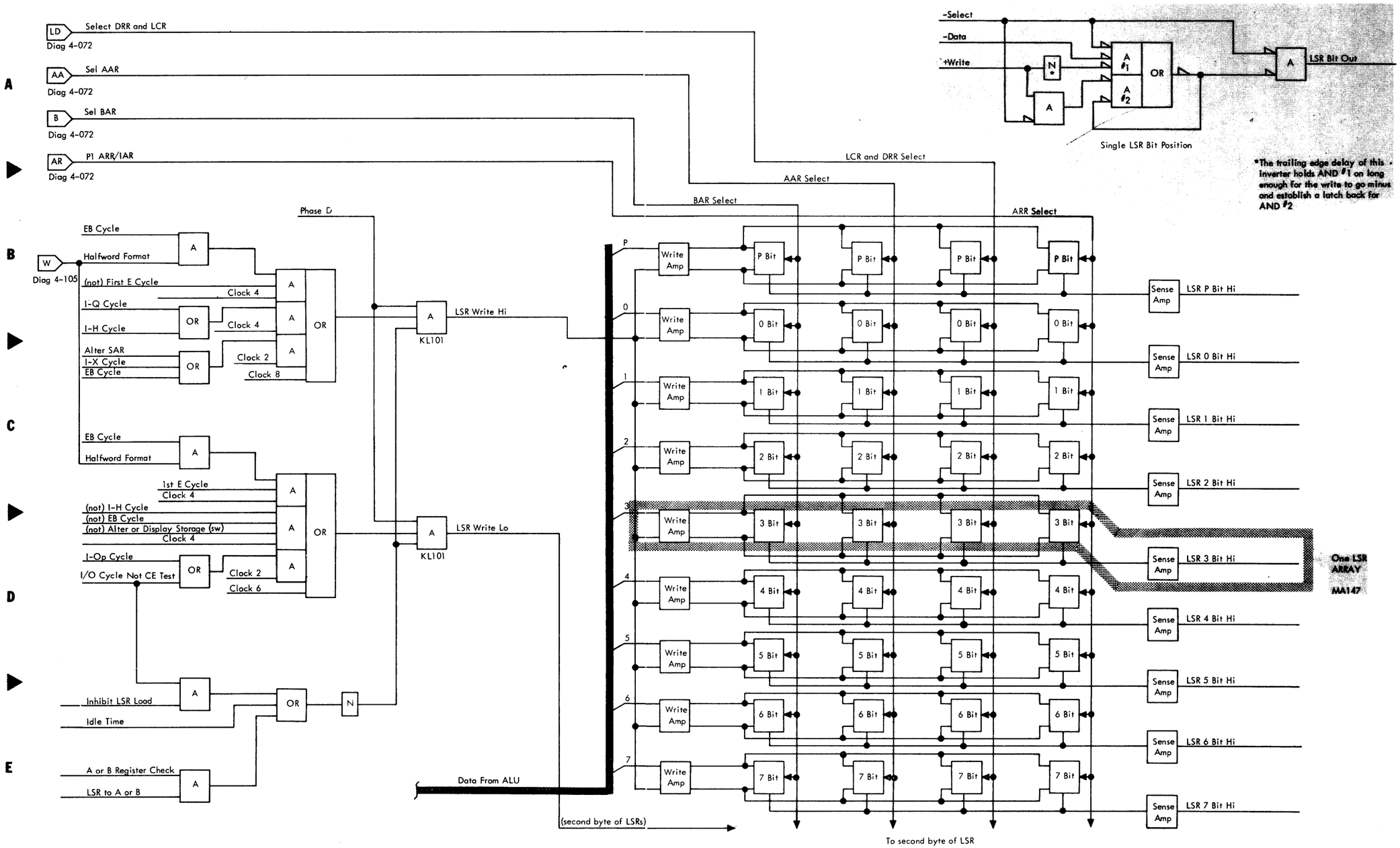
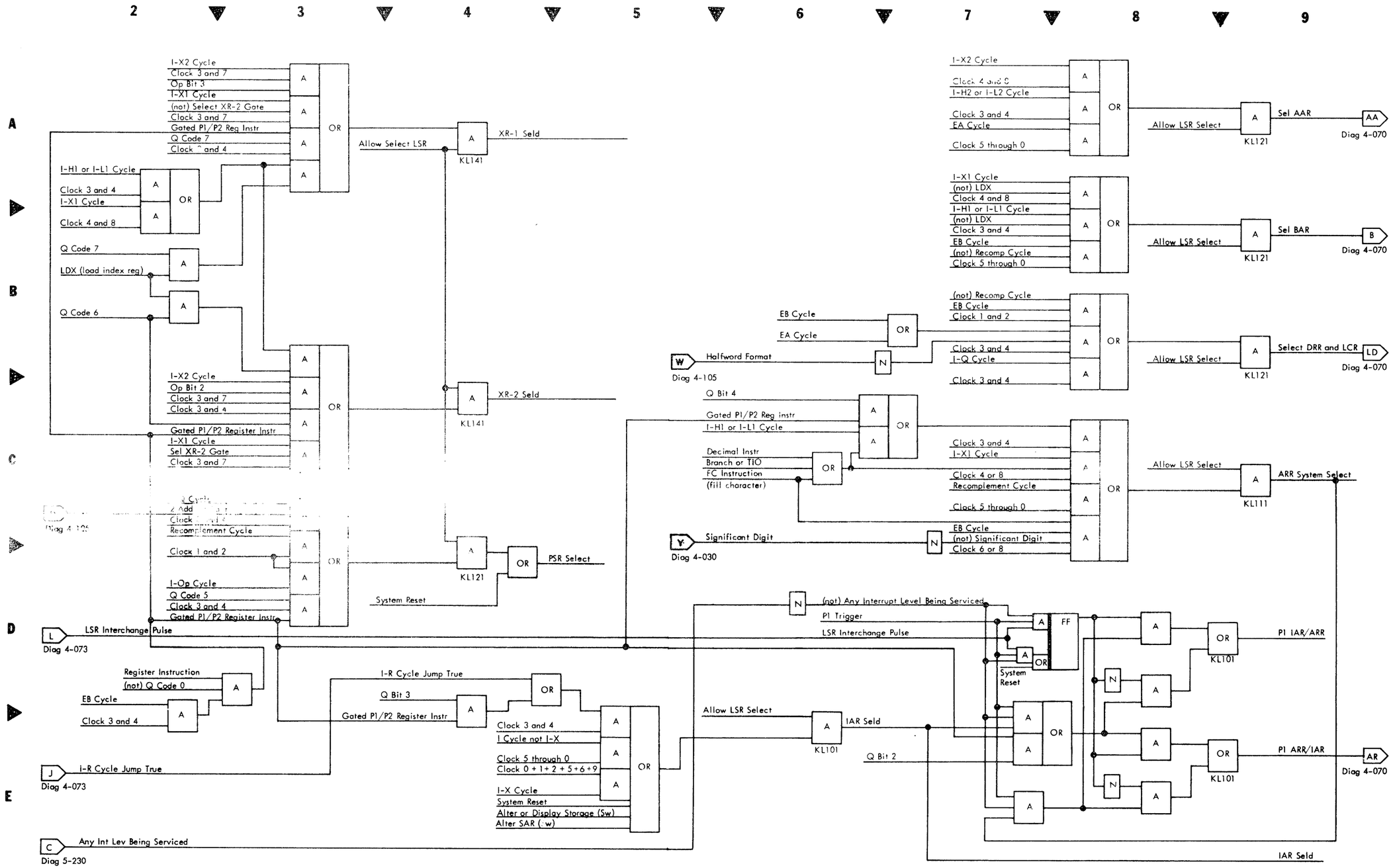


Diagram 4-070. Local Storage Registers (LSR)


2
3
4
5
6
7
8
9
A
B
C
D
E
1-X2 Cycle
Clock 3 and 7
Op Bit 3
1-X1 Cycle
(not) Select XR-2 Gate
Clock 3 and 7
Gated P1/P2 Reg Instr
Q Code 7
Clock ^ and 4
OR
Allow Select LSR
XR-1 Seld
KL141
1-H1 or 1-L1 Cycle
Clock 3 and 4
1-X1 Cycle
Clock 4 and 8
Q Code 7
LDX (load index reg)
Q Code 6
1-X2 Cycle
Op Bit 2
Clock 3 and 7
Clock 3 and 4
Gated P1/P2 Register Instr
1-X1 Cycle
Sel XR-2 Gate
Clock 3 and 7
XR-2 Seld
Diag 4-105
Add Cycle
Clock
Recomplement Cycle
Clock 1 and 2
1-Op Cycle
Q Code 5
Clock 3 and 4
Gated P1/P2 Register Instr
KL121
PSR Select
System Reset
L
LSR Interchange Pulse
Diag 4-073
Register Instruction
(not) Q Code 0
EB Cycle
Clock 3 and 4
J
1-R Cycle Jump True
Diag 4-073
1-R Cycle Jump True
Q Bit 3
Gated P1/P2 Register Instr
Clock 3 and 4
1 Cycle not 1-X
Clock 5 through 0
Clock 0 + 1 + 2 + 5 + 6 + 9
1-X Cycle
System Reset
Alter or Display Storage (Sw)
Alter SAR (Sw)
C
Any Int Lev Being Serviced
Diag 5-230
1-X2 Cycle
Clock 4 and 8
1-H2 or 1-L2 Cycle
Clock 3 and 4
EA Cycle
Clock 5 through 0
Allow LSR Select
Sel AAR
AA
Diag 4-070
KL121
1-X1 Cycle
(not) LDX
Clock 4 and 8
1-H1 or 1-L1 Cycle
(not) LDX
Clock 3 and 4
EB Cycle
(not) Recomp Cycle
Clock 5 through 0
Allow LSR Select
Sel BAR
B
Diag 4-070
KL121
EB Cycle
EA Cycle
W
Halfword Format
Diag 4-105
N
(not) Recomp Cycle
EB Cycle
Clock 1 and 2
Clock 3 and 4
1-Q Cycle
Clock 3 and 4
Allow LSR Select
Select DRR and LCR
LD
Diag 4-070
KL121
Q Bit 4
Gated P1/P2 Reg instr
1-H1 or 1-L1 Cycle
Decimal Instr
Branch or TIO
FC Instruction
(fill character)
Clock 3 and 4
1-X1 Cycle
Clock 4 or 8
Recomplement Cycle
Clock 5 through 0
Allow LSR Select
ARR System Select
KL111
Y
Significant Digit
Diag 4-030
EB Cycle
(not) Significant Digit
Clock 6 or 8
N
(not) Any Interrupt Level Being Serviced
P1 Trigger
LSR Interchange Pulse
FF
System Reset
P1 IAR/ARR
KL101
P1 ARR/IAR
AR
Diag 4-070
KL101
Allow LSR Select
IAR Seld
KL101
Q Bit 2
IAR Seld

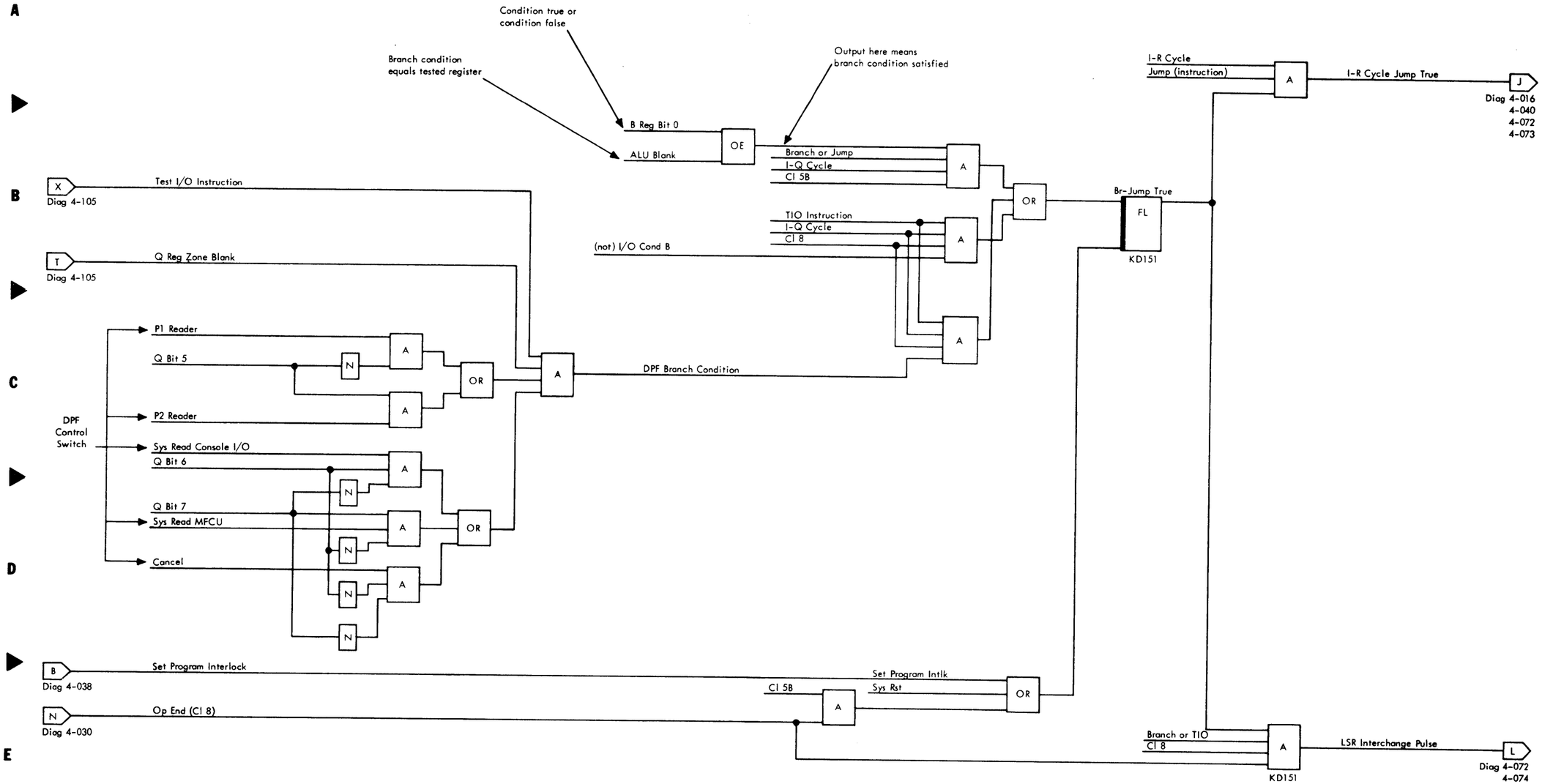
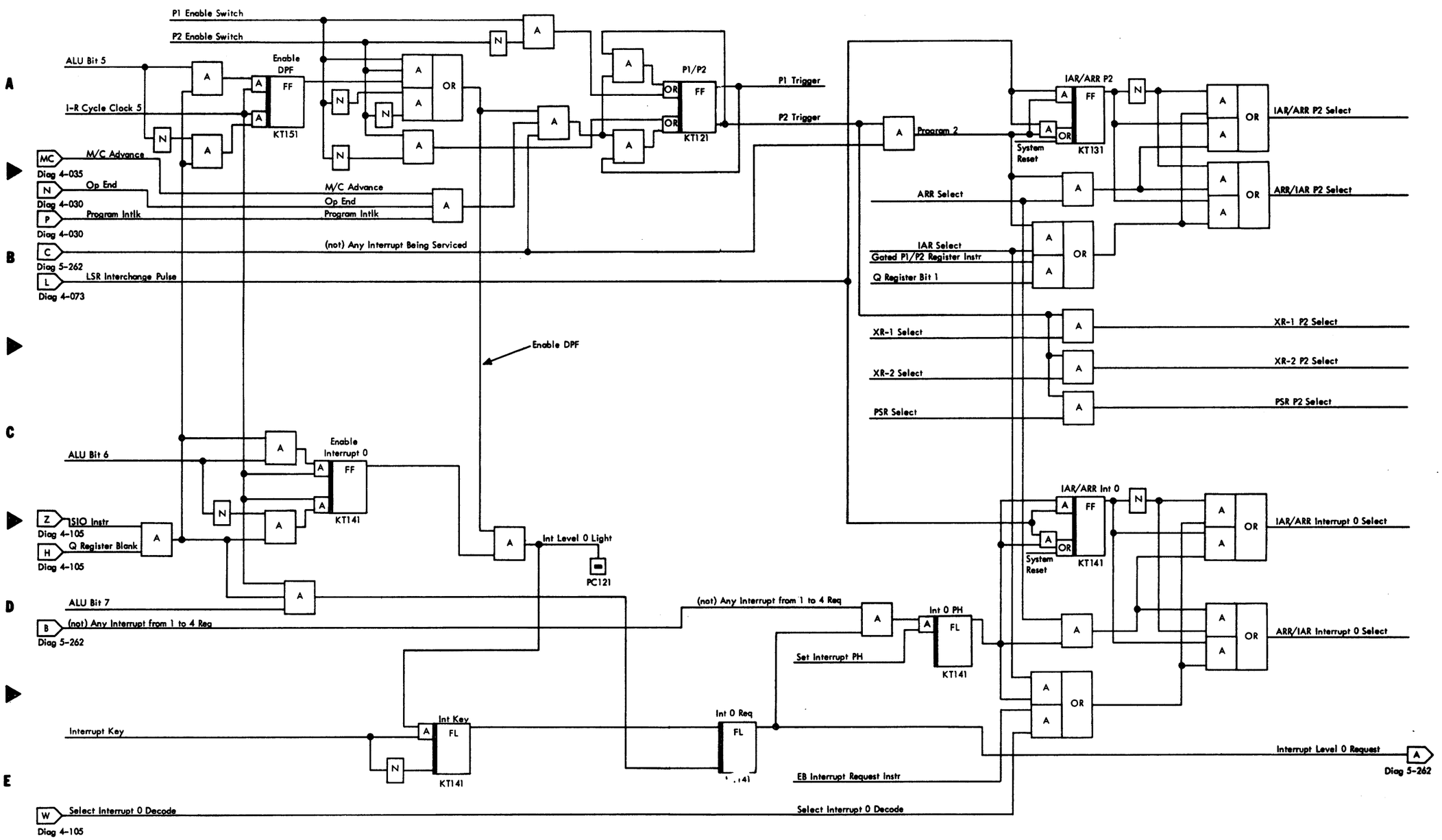


Diagram 4-073. LSR Control


2
3
4
5
6
7
8
9
A
B
C
D
E
P1 Enable Switch
P2 Enable Switch
ALU Bit 5
I-R Cycle Clock 5
Enable DPF
FF
KT151
M/C Advance
Diag 4-035
Op End
Diag 4-030
Program Intlk
Diag 4-030
C
Diag 5-262
LSR Interchange Pulse
L
Diag 4-073
M/C Advance
Op End
Program Intlk
(not) Any Interrupt Being Serviced
P1/P2
OR
FF
KT121
P1 Trigger
P2 Trigger
Program 2
IAR/ARR P2
FF
KT131
System Reset
IAR/ARR P2 Select
ARR/IAR P2 Select
ARR Select
IAR Select
Gated P1/P2 Register Instr
Q Register Bit 1
XR-1 Select
XR-2 Select
PSR Select
XR-1 P2 Select
XR-2 P2 Select
PSR P2 Select
Enable DPF
ALU Bit 6
Enable Interrupt 0
FF
KT141
Z
SIO Instr
Diag 4-105
H
Q Register Blank
Diag 4-105
Int Level 0 Light
PC121
IAR/ARR Int 0
FF
KT141
System Reset
IAR/ARR Interrupt 0 Select
ARR/IAR Interrupt 0 Select
ALU Bit 7
B
(not) Any Interrupt from 1 to 4 Req
Diag 5-262
(not) Any Interrupt from 1 to 4 Req
Int 0 PH
FL
KT141
Set Interrupt PH
Interrupt Key
Int Key
FL
KT141
Int 0 Req
FL
KT141
EB Interrupt Request Instr
Interrupt Level 0 Request
Diag 5-262
W
Select Interrupt 0 Decode
Diag 4-105
Select Interrupt 0 Decode

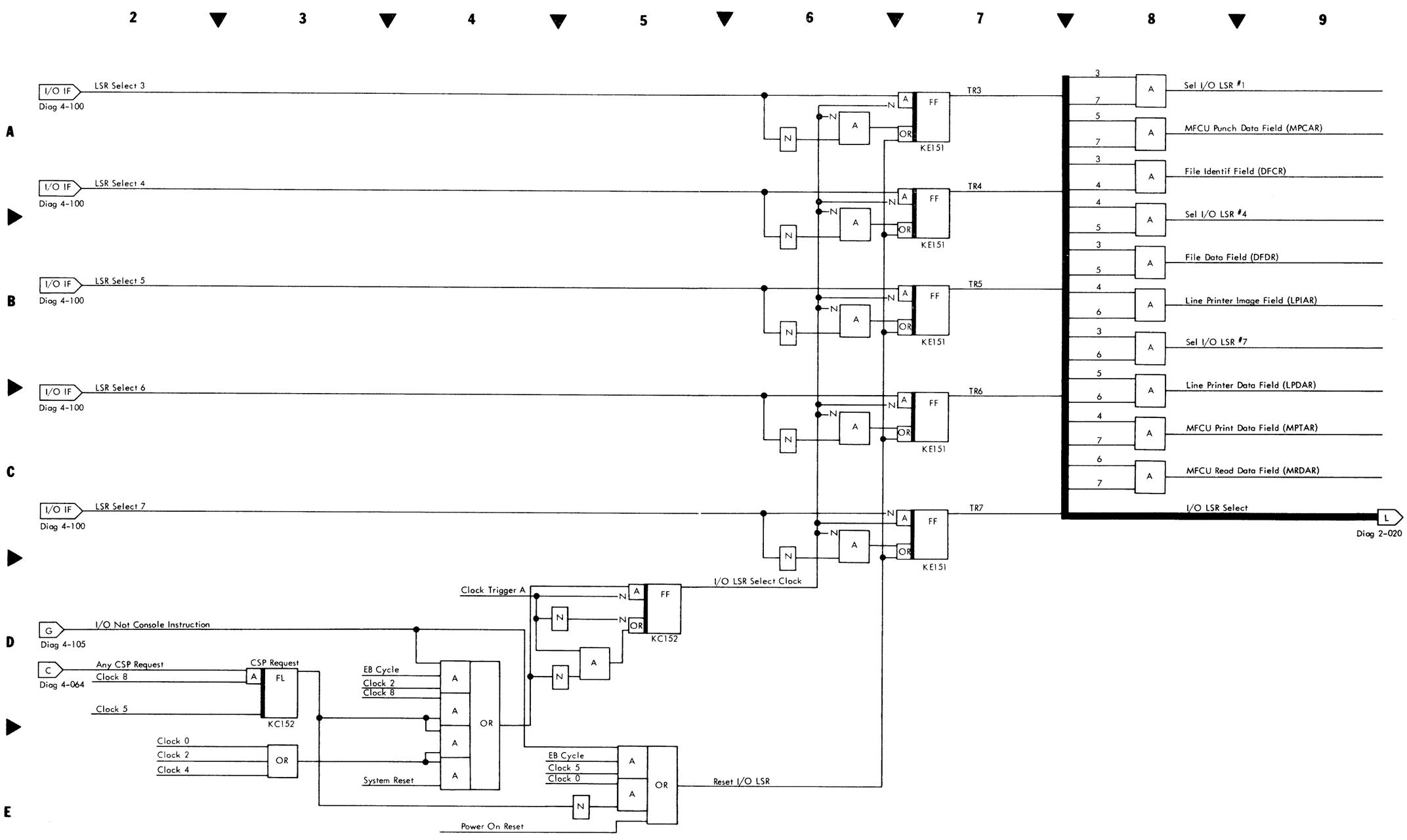
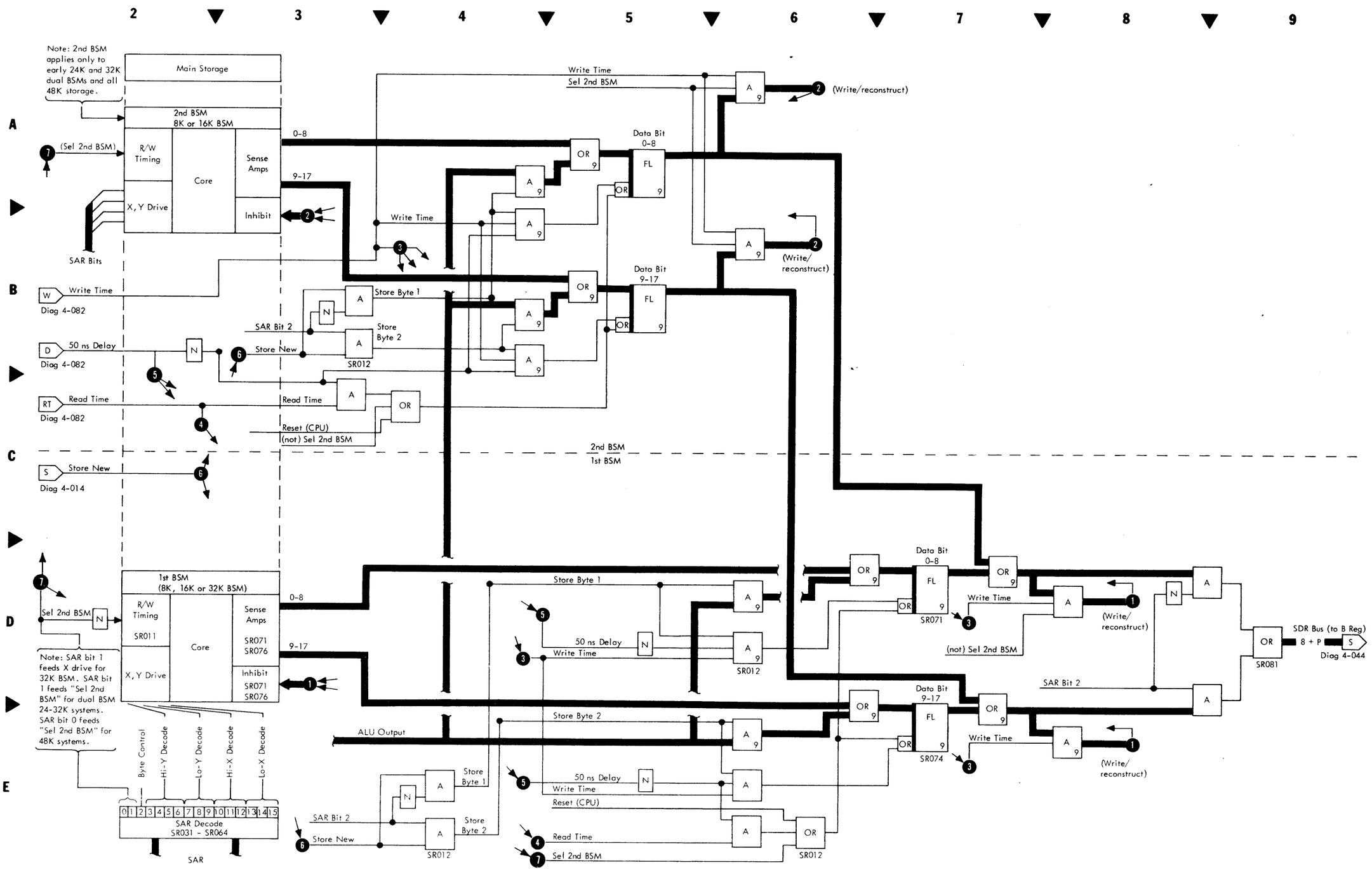
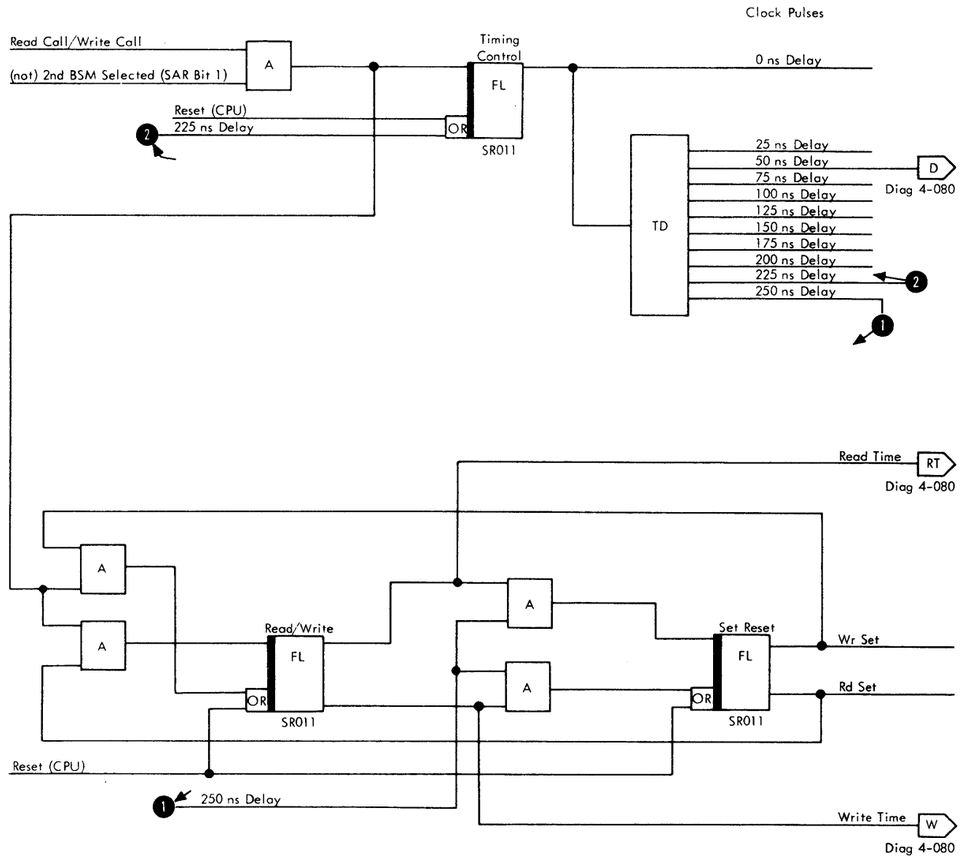


Diagram 4-076. LSR Select (I/O)


2
3
4
5
6
7
8
9
A
B
C
D
E
Note: 2nd BSM applies only to early 24K and 32K dual BSMs and all 48K storage.
Main Storage
2nd BSM
8K or 16K BSM
R/W Timing
Core
Sense Amps
X, Y Drive
Inhibit
(Sel 2nd BSM)
SAR Bits
0-8
9-17
Write Time
Sel 2nd BSM
(Write/reconstruct)
Data Bit 0-8
Data Bit 9-17
FL
OR
A
N
Store Byte 1
Store Byte 2
SAR Bit 2
Store New
SR012
50 ns Delay
Diag 4-082
Read Time
Reset (CPU)
(not) Sel 2nd BSM
2nd BSM
1st BSM
Store New
Diag 4-014
1st BSM
(8K, 16K or 32K BSM)
SR011
SR071
SR076
Sel 2nd BSM
Note: SAR bit 1 feeds X drive for 32K BSM. SAR bit 1 feeds "Sel 2nd BSM" for dual BSM 24-32K systems. SAR bit 0 feeds "Sel 2nd BSM" for 48K systems.
Byte Control
Hi-Y Decode
Lo-Y Decode
Hi-X Decode
Lo-X Decode
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
SAR Decode
SR031 - SR064
SAR
ALU Output
SR071
SR074
SR081
(Write/ reconstruct)
SDR Bus (to B Reg)
8 + P
Diag 4-044



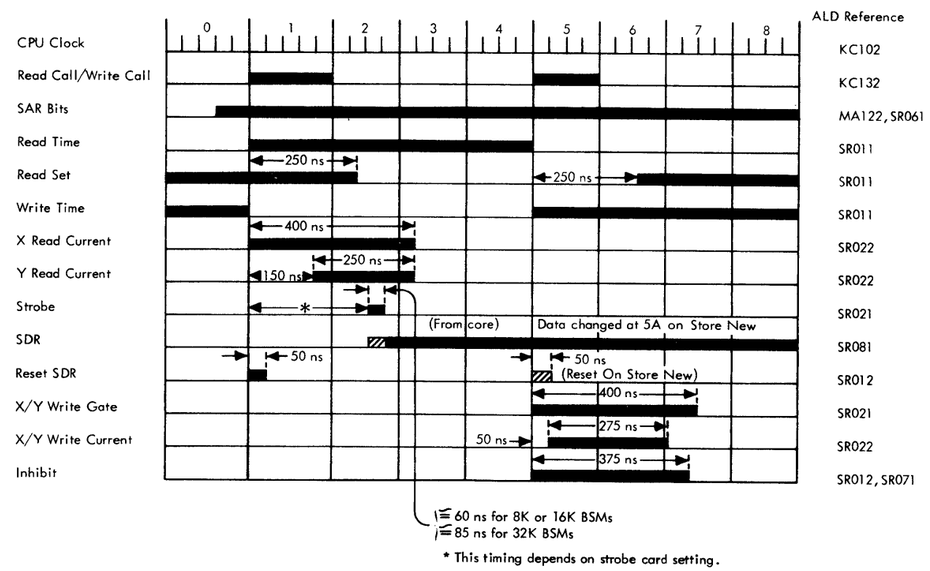


Diagram 4-082. Storage Delay Clock and Timing

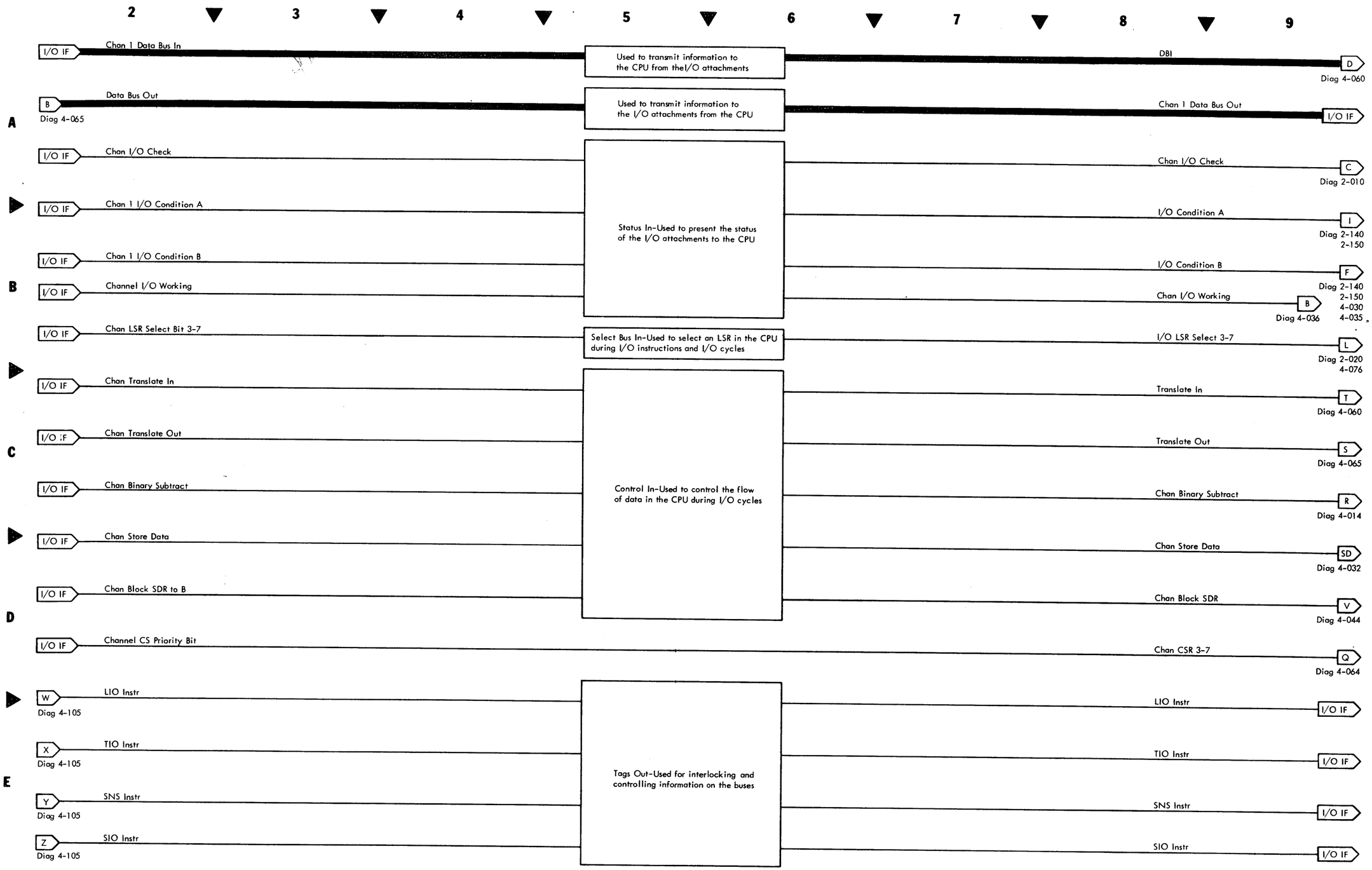


Diagram 4-100. I/O Interface Lines

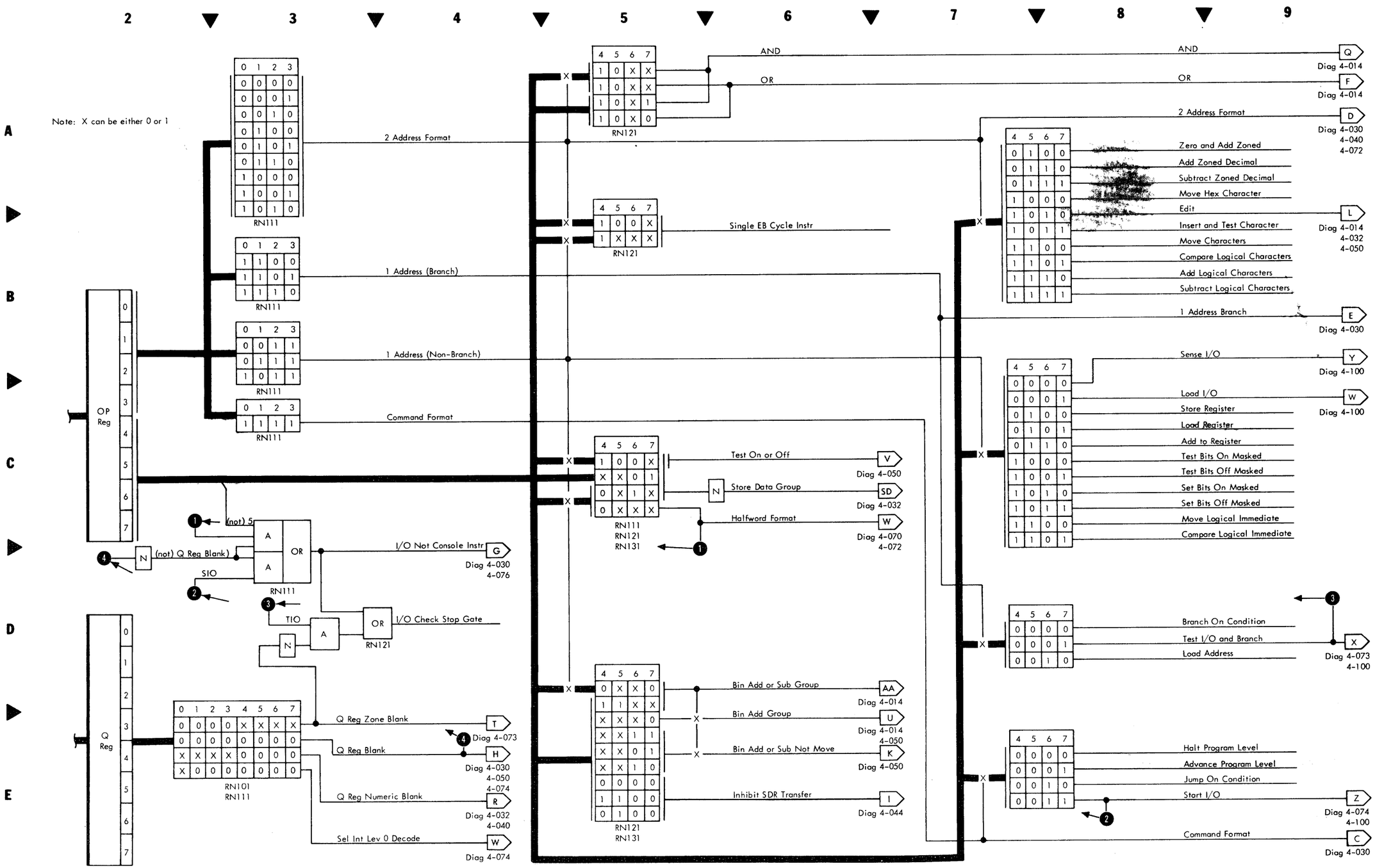

2
3
4
5
6
7
8
9
A
B
C
D
E
Note: X can be either 0 or 1
OP Reg
Q Reg
RN111
RN121
RN101
RN131
2 Address Format
1 Address (Branch)
1 Address (Non-Branch)
Command Format
Single EB Cycle Instr
Test On or Off
Store Data Group
Halfword Format
Bin Add or Sub Group
Bin Add Group
Bin Add or Sub Not Move
Inhibit SDR Transfer
(not) Q Reg Blank
SIO
TIO
I/O Not Console Instr
I/O Check Stop Gate
Q Reg Zone Blank
Q Reg Blank
Q Reg Numeric Blank
Sel Int Lev 0 Decode
AND
OR
Zero and Add Zoned
Add Zoned Decimal
Subtract Zoned Decimal
Move Hex Character
Edit
Insert and Test Character
Move Characters
Compare Logical Characters
Add Logical Characters
Subtract Logical Characters
1 Address Branch
Sense I/O
Load I/O
Store Register
Load Register
Add to Register
Test Bits On Masked
Test Bits Off Masked
Set Bits On Masked
Set Bits Off Masked
Move Logical Immediate
Compare Logical Immediate
Branch On Condition
Test I/O and Branch
Load Address
Halt Program Level
Advance Program Level
Jump On Condition
Start I/O
Command Format
Diag 4-014
Diag 4-030
4-040
4-072
Diag 4-032
4-050
Diag 4-100
Diag 4-073
4-100
Diag 4-074
Diag 4-076
Diag 4-070
Diag 4-044

DIAGRAM	INSTRUCTIONS		OP BITS 0 1 2 3	OP BITS 4 5 6 7	SIGNAL NAME	AND	OR	STORE DATA GRP	BIN ADD OR SUB GRP	BIN ADD GROUP	BIN ADD/SUB NOT MOVE	INH SDR X-FER	SINGLE EB CY INST	I/O NOT CONSL INST	I/O CHK STOP GATE	TIO INST (ADV OR TIO)	BR OR SKIP	HALT	ADVANCE	SKIP	SIO INST	BR OR TIO INST	1 ADDRESS BRANCH	TEST I/O	LDX INST (LOAD INDEX REG)	HALFWORD FORM	SET OR TEST OFF	TEST ON OR OFF	REGISTER INSTR	ADD TO REG OR STORE INST	SENSE I/O INST	CHAN LOAD I/O INST	LOAD REG INST	LOAD CR	EDIT INSTR	FILL CHARAC INST	MOVE ZONE	MOVE NUM	ZONE NUM INTCHG	DECIMAL INSTR
					ALD REFERENCE	KY101	KY101	RN131	RN131	RN131	RN131	RN121	RN121	RN111	RN121	RN111	RN111	RN111	RN111	RN111	RN111	RN121	RN111	RN111	RN131	RN111	RN121	RN121	RN111	RN111	RN111	RN111	RN111	KG101	RN121	RN121	RN121	RN121	RN121	RN131
5-100	Zero and Add Zoned	ZAZ	X	0100			X				X																											X
5-100	Add Zoned Decimal	AZ	X	0110			X																															X
5-100	Subtract Zoned Decimal	SZ	X	0111			X																															X
5-070	Move Hex Character	MVX	X	1000	X	X	X						X																							✱ (Q̄6)	✱ (Q6)	✱ (Q6 + Q7)	X
5-110	Edit	ED	X	1010	X	X	X																											X					
5-120	Insert & Test Characters	ITC	X	1011	X	X	X																												X				
5-080	Move Characters	MVC	X	1100			X	X	X		X																												
5-080	Compare Logical Character	CLC	X	1101				X		X																													
5-080	Add Logical Character	ALC	X	1110			X	X	X	X																													
5-080	Subtract Logical Character	SLC	X	1111			X	X		X																													
5-170	Sense I/O	SNS	Y	0000			X	X	X		X		✱	✱																			X		X	X			
5-160	Load I/O	LIO	Y	0001									✱	✱																			X				X		
5-060	Store Register	ST	Y	0100			X	X	X		X																						X		X	X	(Q̄0)	(Q̄0 Q5)	
5-060	Load Register	L	Y	0101																													X			✱	✱		
5-060	Add to Register	A	Y	0110				X	X	X																							X		X	X			
5-050	Test Bits On Masked	TBN	Y	1000		X							X																					X					
5-050	Test Bits Off Masked	TBF	Y	1001	X								X																					X	X				
5-050	Set Bits On Masked	SBN	Y	1010		X	X						X																										
5-050	Set Bits Off Masked	SBF	Y	1011	X		X						X																					X					
5-090	Move Logical Immediate	MVI	Y	1100			X	X	X		X	X																											
5-090	Compare Logic Immediate	CLI	Y	1101				X		X		X																											
5-130	Branch On Condition	BC	Z	0000			⊗				⊗				X									X	X														
5-180	Test I/O and Branch	TIO	Z	0001										✱	X									X		X													
5-190	Load Address	LA	Z	0010			⊗									X																						
5-210	Halt Program Level	HPL	F	0000			⊗				⊗							X																					
5-200	Advance Prog Level	APL	F	0001											X				X																			
5-140	Jump On Condition	JC	F	0010			⊗									X				X																	
5-150	Start I/O	SIO	F	0011			⊗							✱	✱						X																	

(Q REG NOT BLK) (Q REG NOT BLK) (NOT Q ZONE BLNK) (Q REG NOT BLK) (Q REG NOT BLK)

Notes: ✱ Conditioned by Q Reg Bits

⊗ Line developed but not used in this operation

OP BITS 0123

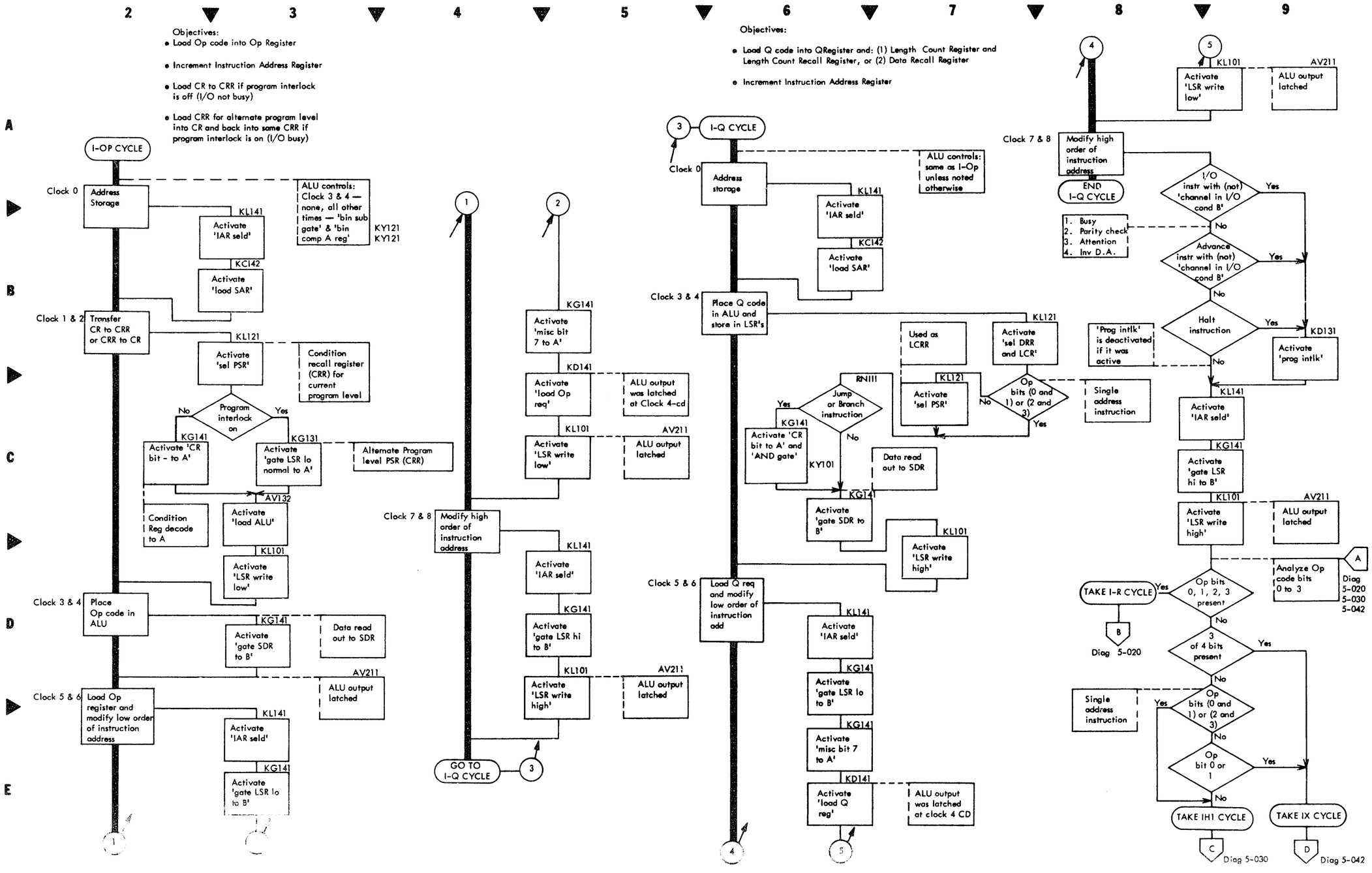
X 2 address instruction (can be indexed by bits 0-3)

Y 1 address instruction (can be indexed by bits 0 and 1)

Z 1 address instruction (can be indexed by bits 2 and 3)

F Command instruction

Diagram 5-005. Instructional/Functional Signal Reference


2
3
4
5
6
7
8
9
A
B
C
D
E
Objectives:
• Load Op code into Op Register
• Increment Instruction Address Register
• Load CR to CRR if program interlock is off (I/O not busy)
• Load CRR for alternate program level into CR and back into same CRR if program interlock is on (I/O busy)
I-OP CYCLE
Clock 0
Address Storage
KL141
Activate 'IAR seld'
KC142
Activate 'load SAR'
ALU controls: Clock 3 & 4 — none, all other times — 'bin sub gate' & 'bin comp A reg'
KY121
KY121
Clock 1 & 2
Transfer CR to CRR or CRR to CR
KL121
Activate 'sel PSR'
Condition recall register (CRR) for current program level
Program interlock on
No
Yes
KG141
Activate 'CR bit - to A'
KG131
Activate 'gate LSR lo normal to A'
Alternate Program level PSR (CRR)
AV132
Condition Reg decode to A
Activate 'load ALU'
KL101
Activate 'LSR write low'
Clock 3 & 4
Place Op code in ALU
KG141
Activate 'gate SDR to B'
Data read out to SDR
AV211
ALU output latched
Clock 5 & 6
Load Op register and modify low order of instruction address
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR lo to B'
1
2
KG141
Activate 'misc bit 7 to A'
KD141
Activate 'load Op req'
ALU output was latched at Clock 4-cd
KL101
Activate 'LSR write low'
AV211
ALU output latched
Clock 7 & 8
Modify high order of instruction address
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR hi to B'
KL101
Activate 'LSR write high'
AV211
ALU output latched
GO TO I-Q CYCLE
3
Objectives:
• Load Q code into QRegister and: (1) Length Count Register and Length Count Recall Register, or (2) Data Recall Register
• Increment Instruction Address Register
3
I-Q CYCLE
Clock 0
Address storage
ALU controls: same as I-Op unless noted otherwise
KL141
Activate 'IAR seld'
KC142
Activate 'load SAR'
Clock 3 & 4
Place Q code in ALU and store in LSR's
KL121
Activate 'sel DRR and LCR'
Used as LCRR
KL121
Activate 'sel PSR'
RN111
Jump or Branch instruction
Yes
No
KG141
Activate 'CR bit to A' and 'AND gate'
KY101
Data read out to SDR
KG141
Activate 'gate SDR to B'
KL101
Activate 'LSR write high'
Clock 5 & 6
Load Q req and modify low order of instruction add
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR lo to B'
KG141
Activate 'misc bit 7 to A'
KD141
Activate 'load Q reg'
ALU output was latched at clock 4 CD
4
5
Op bits (0 and 1) or (2 and 3)
No
Yes
Single address instruction
'Prog intlk' is deactivated if it was active
Clock 7 & 8
Modify high order of instruction address
END I-Q CYCLE
1. Busy
2. Parity check
3. Attention
4. Inv D.A.
I/O instr with (not) 'channel in I/O cond B'
Yes
No
Advance instr with (not) 'channel in I/O cond B'
Yes
No
Halt instruction
Yes
No
KD131
Activate 'prog intlk'
KL141
Activate 'IAR seld'
KG141
Activate 'gate LSR hi to B'
KL101
Activate 'LSR write high'
AV211
ALU output latched
A
Analyze Op code bits 0 to 3
Diag 5-020 5-030 5-042
Op bits 0, 1, 2, 3 present
Yes
No
TAKE I-R CYCLE
B
Diag 5-020
3 of 4 bits present
Yes
No
Single address instruction
Op bits (0 and 1) or (2 and 3)
Yes
No
Op bit 0 or 1
Yes
No
TAKE IH1 CYCLE
TAKE IX CYCLE
C
Diag 5-030
D
Diag 5-042

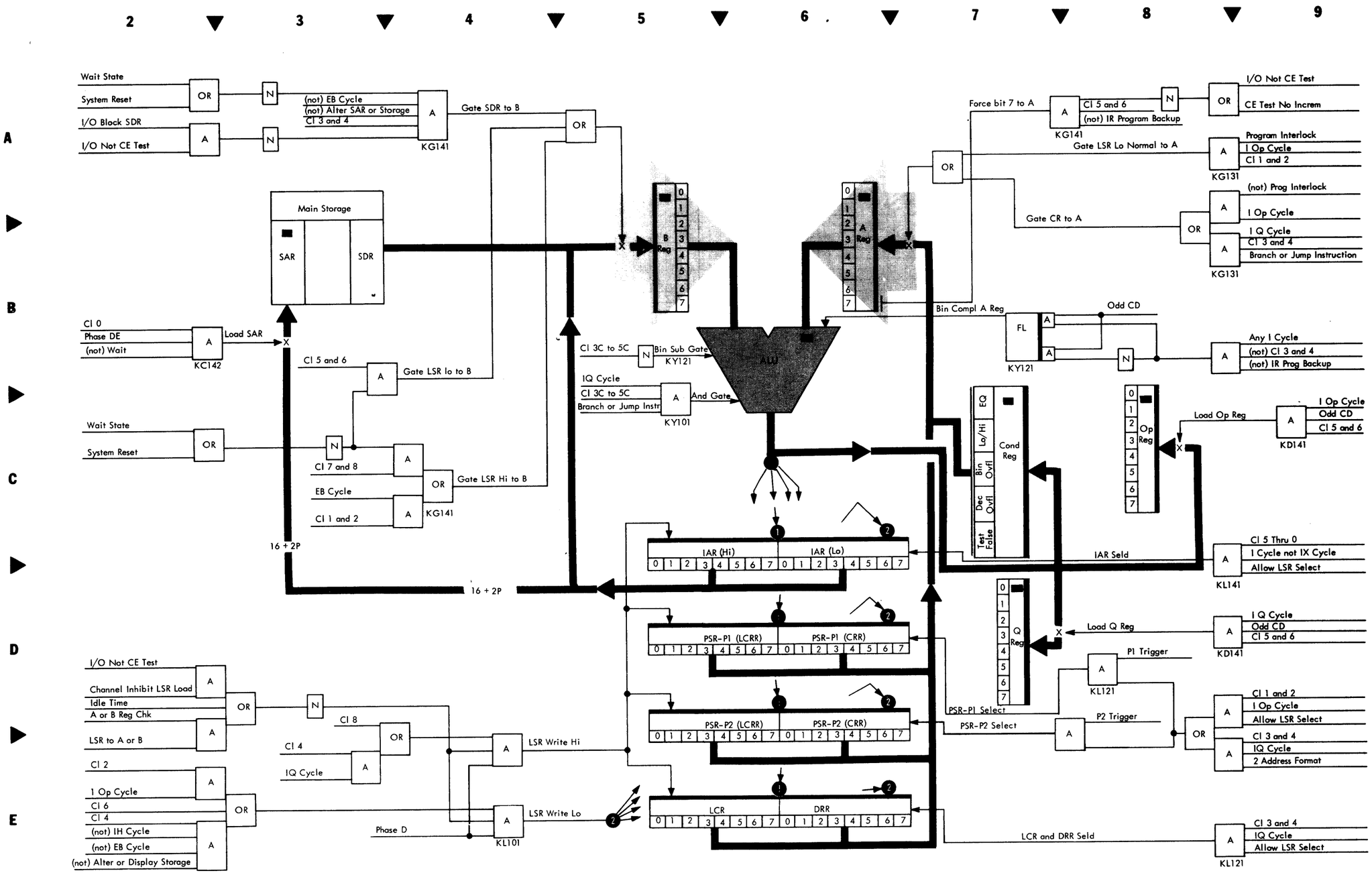


Diagram 5-012. I-Op and I-Q Cycles (PART 2 of 3)

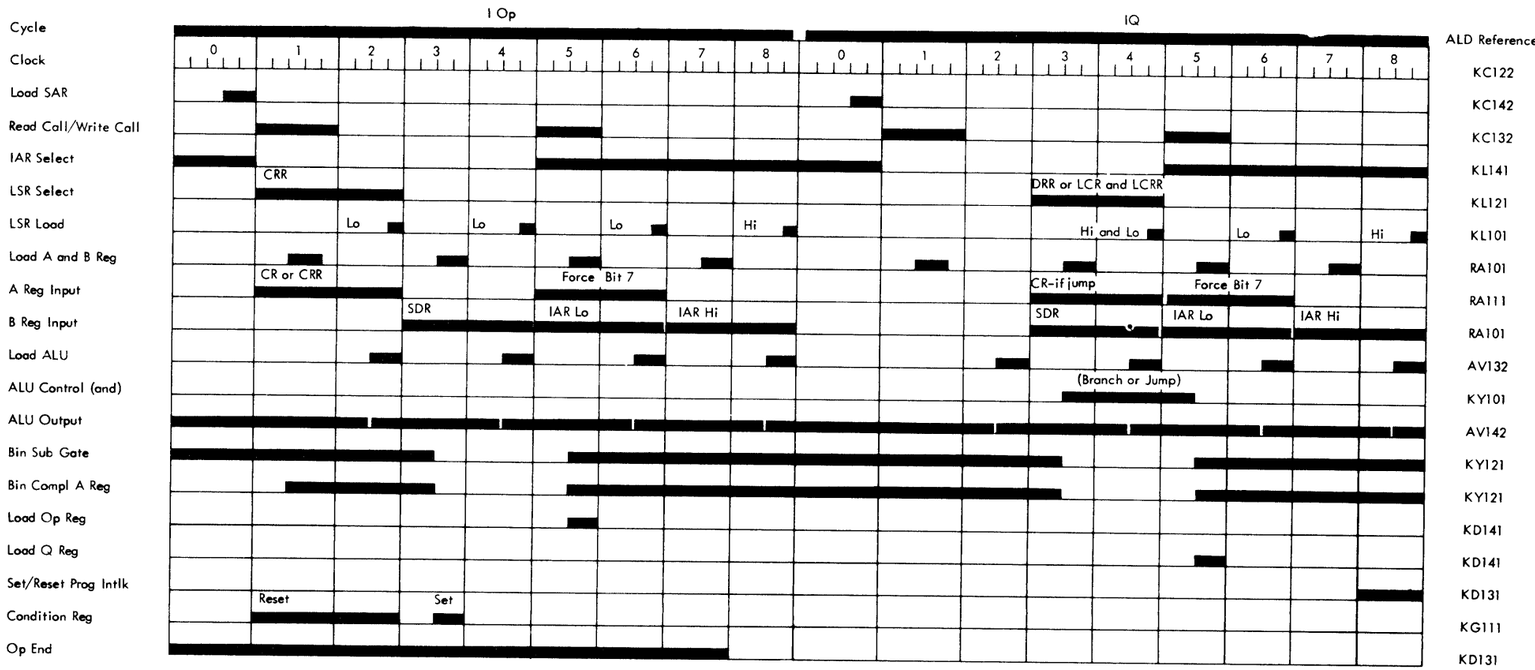


Diagram 5-014. I-Op and I-Q Cycles (PART 3 of 3)

2 3 4 5 6 7 8 9

Objectives:

- Execute command instruction, unless program interlocked
- Increment or decrement Instruction Address Register

A

Diag. 5-010 B — I-R CYCLE

clock 0 — Address storage

B

Refer to Diagram 5-010 Point A to determine which type of cycle to take after I-Q cycle

Activate 'IAR seld' — KL141

Activate 'load SAR' — KC142

C

clock 3&4 — Add to address in IAR for Jump instruction with condition satisfied

Data read out to SDR

Activate 'gate SDR to B' — KG141

D

Jump instruction with condition satisfied (Diagram 5-022 9-A)

No

Yes

Activate 'gate LSR lo normal to A' — KG131

E

1 — 3

1 — 3

Activate 'bin comp A reg' and 'bin sub gate' — KY121 KY121

Activate 'IAR seld' — KL141

2

Activate 'LSR write low' — KL101 — ALU output latched — AV211

clock 5&6 — Increment or decrement low order of instruction address

Activate 'IAR seld' — KL141

Activate 'gate LSR lo to B' — KG141

Advance instruction and Q reg blank

'Prog intlk' — KD131 Yes

No

uncondi-tional program level adv

Yes

No

Activate 'misc bit 7 to A' — KG141

Activate 'IR program backup' — KD151

Activate 'bin comp A reg' — KY121

Activate 'misc bit 6 to A' — KG141

Activate 'bin sub gate' — KY121

Activate 'LSR write low' — KL101 — ALU output latched — AV211

clock 7&8 — Increment or decrement high order of instruction address

Activate 'IAR seld' — KL141

Activate 'gate LSR hi to B' — KG141

5 — 4

5 — 4

END OF OPERATION

Activate 'bin sub gate' — KY121

'Prog intlk' — KD131 Yes

No

unconditional program level adv

Yes

No

Activate 'bin comp A reg' — KY121

Turn on 'Op end' trigger — KD131

Activate 'LSR write high' — KL101 — ALU Output latched — AV211

Cycle	IR	ALD Reference
Clock	0 1 2 3 4 5 6 7 8	KC122
Load SAR		KC142
Read Call/Write Call		KC132
IAR Select		KL141
LSR Load	*Lo Lo Hi	KL101
Load A and B Reg		RA101
A Reg input	IAR Force bit 7	RA111
B Reg input	SDR IAR Lo IAR Hi	RA101
Load ALU		AV132
ALU Output		AV142
bin Compl A Reg		KY121
bin Sub Gate		KY121
Op End		KD131

* Jump Instruction only

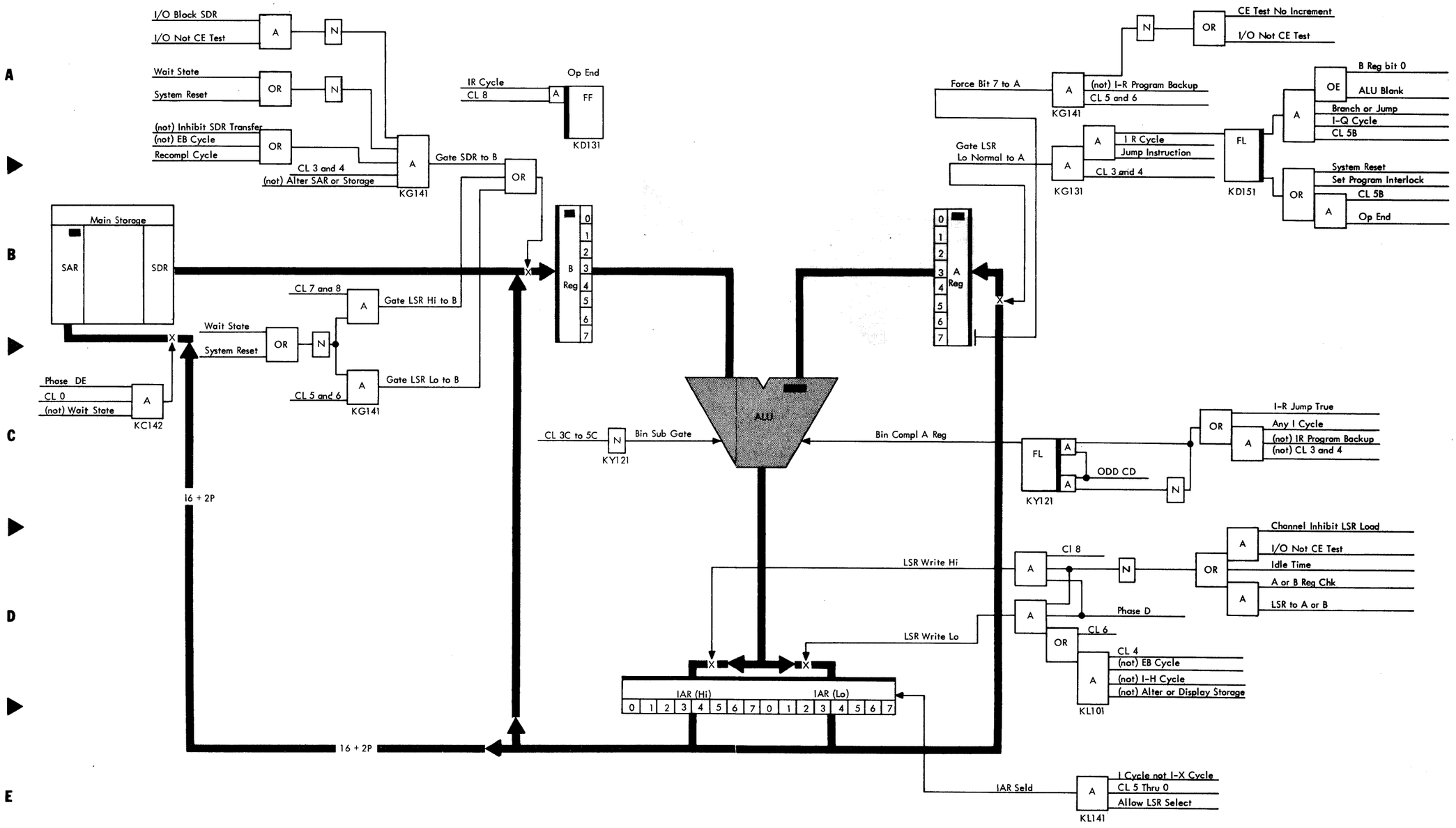


Diagram 5-022. I-R Cycle (PART 2 of 2)

Objectives:

- Load B Address Register except during load address instruction
- Load selected Index Register for load address instruction
- Load A Address Register for second address
- Load Adress Recall Register for branch or decimal instructions

I-H OR I-L CYCLE

C Diag 5-010

Refer to Diagram 5-010 point A to determine which type of cycle to take after I-Q cycle

5

Address storage

Clock 0

KL141 Activate 'IAR seld'

KC142 Activate 'load SAR'

Clock 3 & 4 Load register. High order position in I-H cycles, low order position in I-L cycles

1

I-H1 or I-L1 cycle

Yes / No

Load address inst

Yes / No

Branch or decimal inst

Yes / No

KL121 Activate 'sel AAR'

KL141 Activate 'ARR seld'

KL121 Activate 'sel BAR'

KL141 Activate 'XR1 Seld' or 'XR2 Seld'

XR1 - Q bit 7
XR2 - Q bit 6

KG141 Activate 'gate SDR to B'

2

1

I-H cycle

No / Yes

KL101 Activate 'LSR write low'

KL101 Activate 'LSR write high'

Clock 5 & 6 Modify low order of instruction address

3

KL141 Activate 'IAR seld'

KG141 Activate 'gate LSR lo to B'

KG141 Activate 'misc bit 7 to A'

KY121 Activate 'bin comp A reg' and 'bin sub gate'

AV211 ALU output latched

KL101 Activate 'LSR write low'

4

I-H1 cycle

No / Yes

Take I-L2 cycle

Take I-L1 cycle

3

4

Clock 7 & 8 Modify high order of instruction address

5

See Note 1 for format. Branch, test I/O and branch, or load address operations end after I-L1 cycle. Otherwise proceed to specific operation flow charts after completing I cycles

KL141 Activate 'IAR seld'

KG141 Activate 'gate LSR hi to B'

KY121 Activate 'bin comp A reg' and 'bin sub gate'

Branch or test I/O and branch instruction

No / Yes

Load address instruction

Yes / No

I-L cycle

No / Yes

KD131 Turn on 'op end' trigger

KL101 Activate 'LSR write high'

I-H cycle

Yes / No

I-L1 cycle

Yes / No

Op bits (0 and 1) or (2 and 3)

single address instruction

No / Yes

Op bit 2 or op bit 3

No / Yes

Take I-H2 cycle

Take I-X2 cycle

D Diag 5-042

6

END OF OPERATION

Branch instruction

Yes / No

Branch condition satisfied

Yes / No

KD151 Activate 'LSR intchg pulse' (Diag 4-073)

Load address instruction

No / Yes

Tested during I-Q cycle. Activates Br-Jump true FL. (Diagram 4-073) KD151

END OF I CYCLES

Note 1: Format for single address instruction is; I-H1 and I-L1 cycles or I-X1 cycle. Second address requires; I-H2 and I-L2 cycles or I-X2 cycle

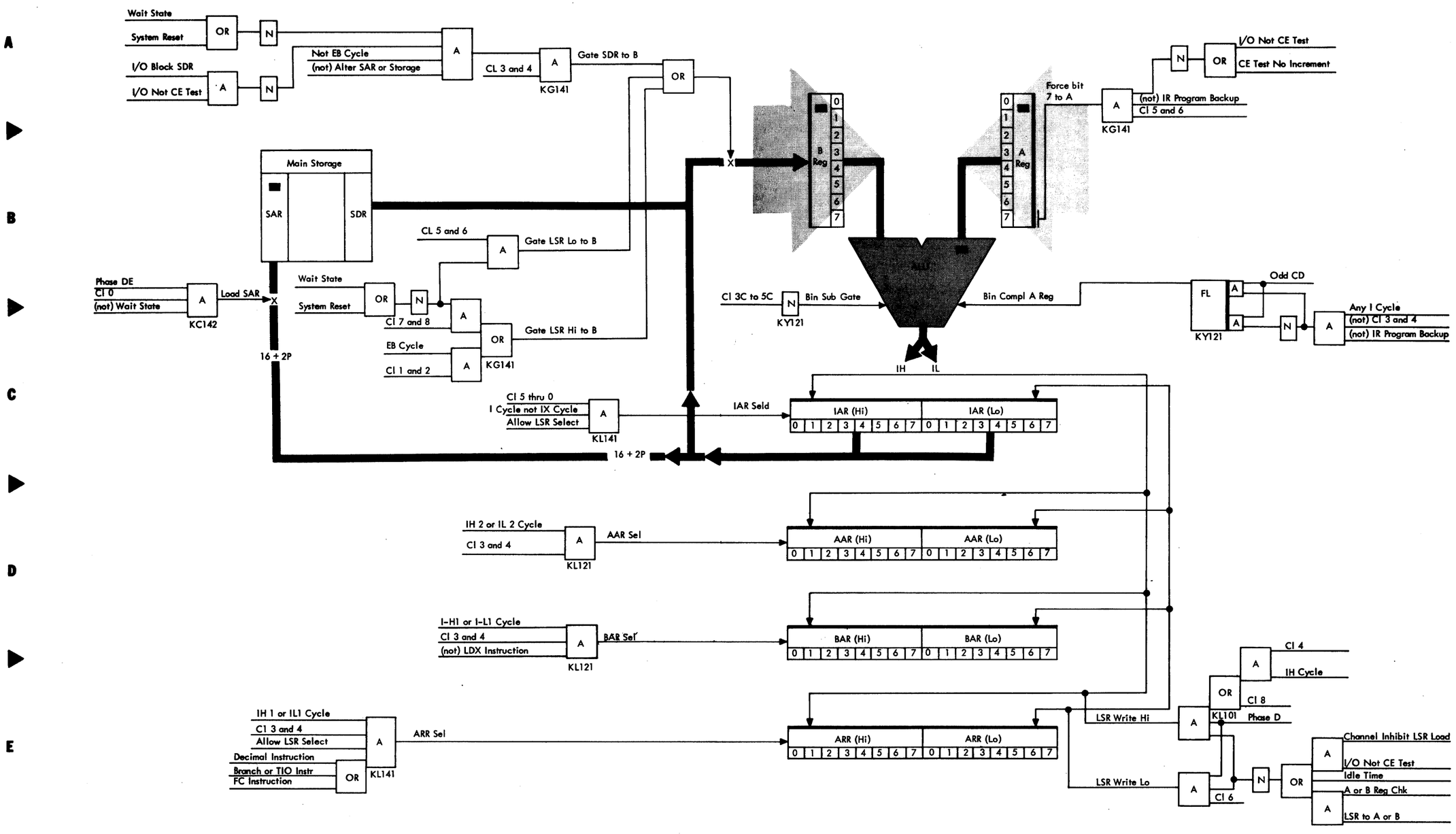
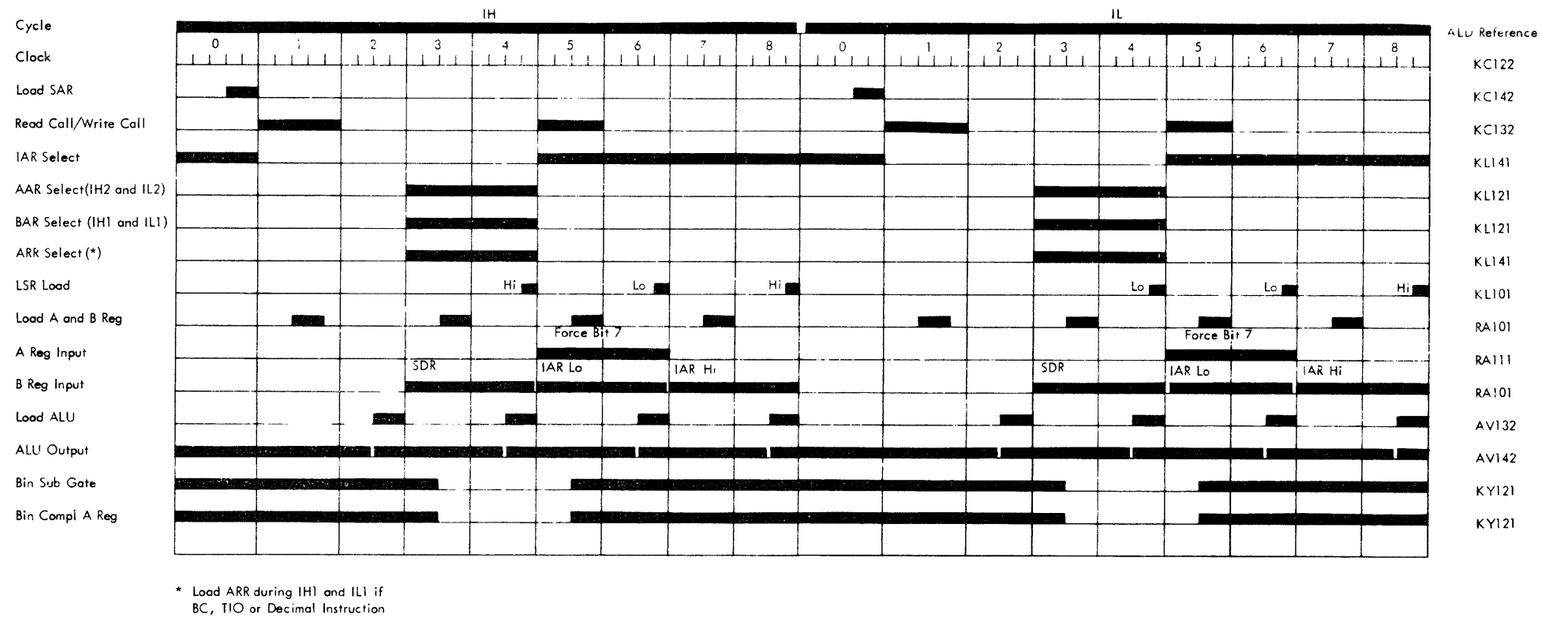


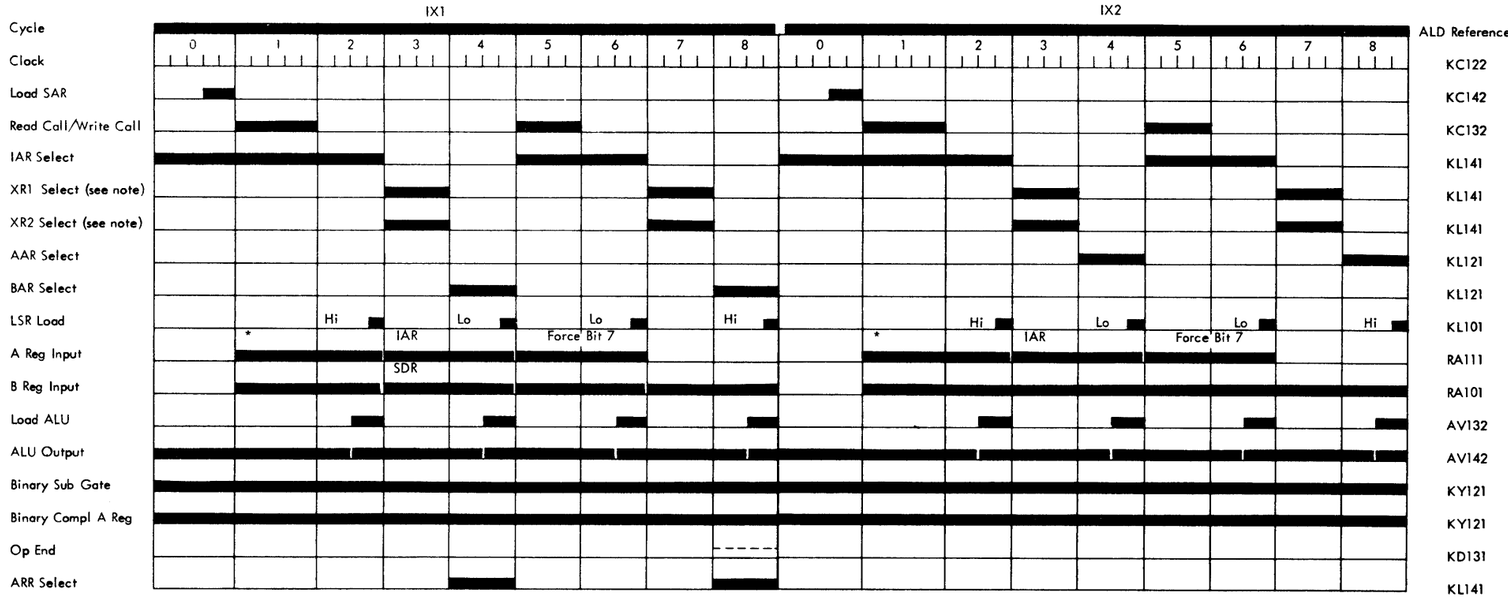
Diagram 5-032. I-H or I-L Cycles (PART 2 of 3)



* Load ARR during IH1 and IL1 if BC, TIO or Decimal Instruction

2 3 4 5 6 7 8 9

A B C D E



* Force bit 7 if IAR Lo contains all 1's (Predicts a carry from IAR-Lo)

NOTE: The contents of Op Register bits 0 thru 3 determine which Index Register is used.

Instruction Format	Op Bits 0 1 2 3	B Address Register	A Address Register
2 Address	0 0 0 0	2 bytes from Storage Unchanged	2 bytes from Storage Unchanged
	0 0 0 1		1 byte from Storage Added to Address from XR1
	0 0 1 0		1 byte from Storage Added to Address from XR2
	0 1 0 0	1 byte from Storage Added to Address from XR1	2 bytes from Storage Unchanged
	0 1 0 1		1 byte from Storage Added to Address from XR1
	0 1 1 0		1 byte from Storage Added to Address from XR2
	1 0 0 0	1 byte from Storage Added to Address from XR2	2 bytes from Storage Unchanged
	1 0 0 1		1 byte from Storage Added to Address from XR1
	1 0 1 0		1 byte from Storage Added to Address from XR2

Instruction Format	Op Bits 0 1 2 3	B Address Register
1 Address (non-branch)	0 0 1 1	2 bytes from Storage Unchanged
	0 1 1 1	1 byte from Storage Added to Address from XR1
	1 0 1 1	1 byte from Storage Added to Address from XR2
1 Address (Branch)	1 1 0 0	2 bytes from Storage Unchanged
	1 1 0 1	1 byte from Storage Added to Address from XR1
	1 1 1 0	1 byte from Storage Added to Address from XR2
Command	1 1 1 1	———

Diagram 5-040. I-X Cycles (PART 1 of 3)

Objectives:
- Add address to contents of Index Register
- Load B Address Register unless load address instruction
- Load selected index register if load address instruction
- Load A Register for second address
- Load Address Recall Register for Branch or Decimal operations

I-X CYCLE

D Diag 5-010

Clock 0: Address storage
- Activate 'IAR seld' KL141
- Activate 'load SAR' KC142

Refer to diagram 5-010 point A to determine which type of cycle to take after I-Q cycle

Clock 1 & 2: Increment high order of instruction address
- Activate 'IAR seld' KL141
- Activate 'gate LSR hi to B' KG141
  - Low order of IAR will carry to high when incremented
- MA122 LSR low F-F
  - No
  - Yes: Activate 'misc bit 7 to A' KG141
- Activate 'bin comp A reg' and 'bin sub gate' KY121
- Activate 'LSR write high' KL101

Clock 3 & 4: Load low order of selected register

(1) (2) (3) (4)

2 → I-X1 cycle
- No: single address instruction
  - No: Activate 'XR1 seld' or 'XR2 seld' KL141; Activate 'gate LSR lo normal to A' KG131; Activate 'gate SDR to B' KG141; Activate 'bin comp A req' and 'bin sub gate' KY121
  - Yes: XR1 for Op bit 1. XR2 for Op bit 0; XR1 for Op bit 3. XR2 for op bit 2
- Yes: Activate 'XR1 seld' or 'XR2 Seld' KL141; XR1 for Op bit 1 (not) bit 0 or Op bit 3 (not) bit 2 . XR2 for Op bit 0 (not) 1 or Op bit 2 (not) 3

Clock 4: Deactivate 'XR1 seld' or 'XR2 seld' KL141

Load address instruction
- No: I-X1 cycle
  - No
  - Yes: Activate 'XR1 seld' or 'XR2 seld' KL141; Activate 'sel BAR' KL121
- Yes

XR1 - Q bit 7
XR2 - Q bit 6

Branch or decimal instruction
- No
- Yes: Activate 'ARR seld' KL141; Activate 'sel AAR' KL121

Activate 'LSR write low' KL101

1 → 2

Clock 5 & 6: Increment low order of instruction address
- Activate 'IAR seld' KL141
- Activate 'gate LSR lo to B' KG141
- Activate 'misc bit 7 to A' KG141
- Activate 'bin comp A req' and 'bin sub gate' KY121
- Activate 'LSR write low' KL101

If computation resulted in a carry, 'temp carry' gives 'arith carry out' for clock 7 computation

Clock 7 & 8: Load high order of selected register
- Activate 'XR1 seld' or 'XR2 seld' KL141
- Activate 'gate LSR hi to B' KG141
- Activate 'bin comp A reg' and 'bin sub gate' KY121
- Clock 8: Deactivate 'XR1 seld' or 'XR2 seld' KL141
- Activate 'sel BAR,' 'ARR seld,' 'sel AAR,' 'XR1 seld,' or 'XR2 seld' KL121 KL141 KL121 KL141 KL141

Select same index register selected at clock 3

Select same register selected at clock 4

See Note 1 for format. Branch, test I/O and branch, or load address operations end after I-X1 cycle. Otherwise proceed to specific operation flow charts after completing I-cycles

Branch or test I/O and branch instruction
- No
- Yes: Load address instruction
  - Yes
  - No
- Turn on 'Op end' trigger KD131

3

3 → Activate 'LSR write high' KL101

I-X1 cycle
- No
- Yes: Single address instruction
  - Yes
  - No: Op bit 2 or Op bit 3
    - Yes: Take I-X2 cycle → 4
    - No: Take I-H2 cycle → C (Diag 5-030)

Op bits (0 and 1) or (2 and 3)

Branch instruction
- No: Load address instruction
  - No
  - Yes
- Yes: Branch condition satisfied
  - No
  - Yes: Activate 'LSR intchg pulse' KD151

END OF OPERATION

END OF I CYCLES

Tested during I-Q cycle. Activates Br-Jump true FL. (Diagram 4-073) KD151

Note 1: Format for single address instruction is; I-H1 and I-L1 cycles or I-X1 cycle. Second address requires; I-H2 and I-L2 cycles or I-X2 cycle.

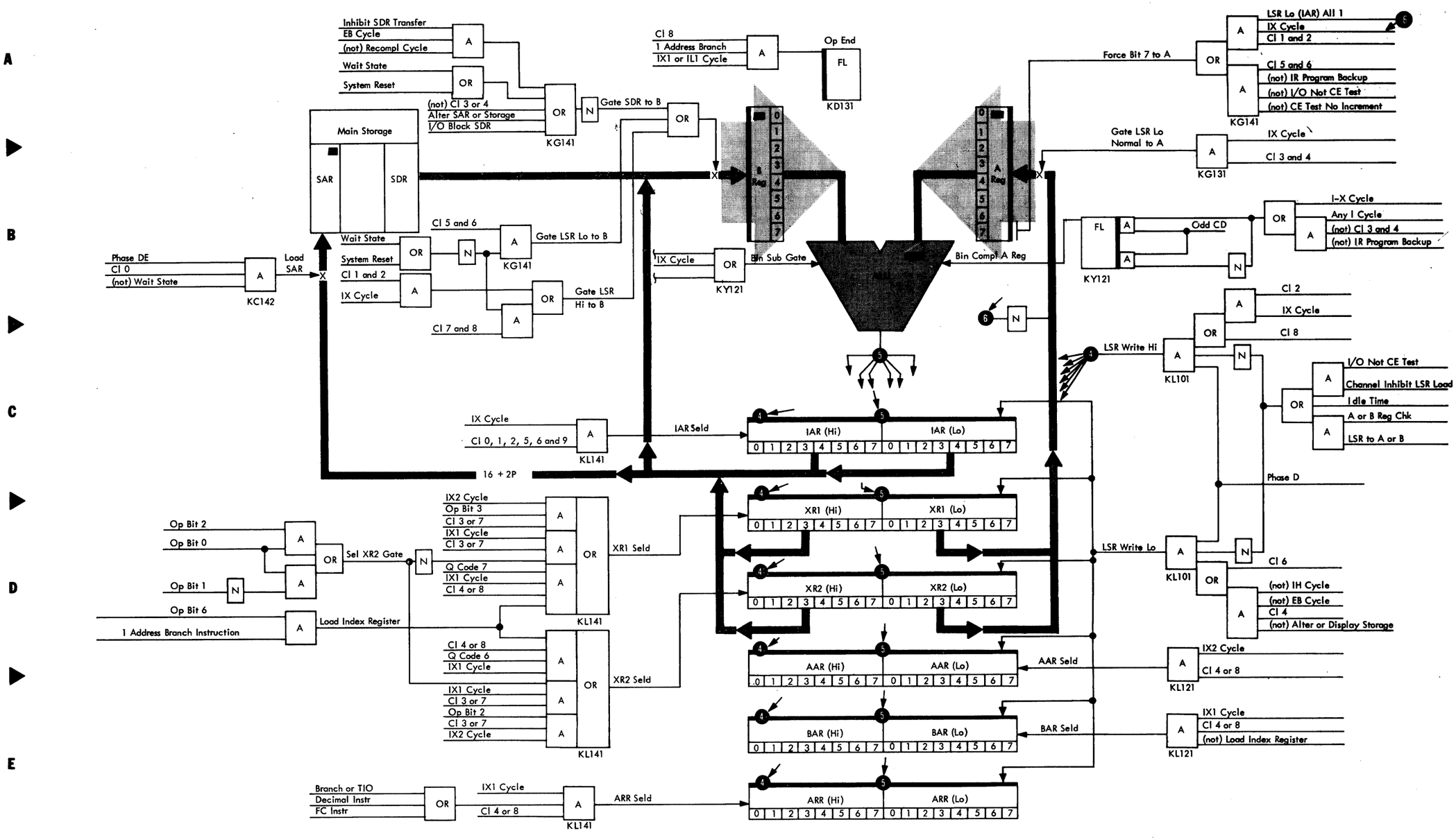


Diagram 5-044. I-X Cycles (PART 3 of 3)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

Objectives:

A

bits 0 1 2 3 4 5 6 7
Set Bits On Masked Op Code X X 1 1 1 0 1 0

- If a bit is present in the Q code, turn on the corresponding bit in the storage location specified by the B Address Register
- Do not change bits which correspond with bits not present in the Q code

bits 0 1 2 3 4 5 6 7
Set Bits Off Masked Op Code X X 1 1 1 0 1 1

▶

- If a bit is present in the Q code, turn off the corresponding bit in the storage location specified by the B Address Register
- Do not change bits which correspond with bits not present in the Q code

bits 0 1 2 3 4 5 6 7
Test Bits On Masked Op Code X X 1 1 1 0 0 0

B

- If a bit is present in the Q code, test to see if the corresponding bit in the storage location specified by the B Address Register is on
- Ignore bits which correspond with bits not present in the Q code.

▶

- Turn on 'test false' latch if selected bits are not all on

bits 0 1 2 3 4 5 6 7
Test Bits Off Masked Op Code X X 1 1 1 0 0 1

- If a bit is present in the Q code, test to see if the corresponding bit in the storage location specified by the B Address Register is off

C

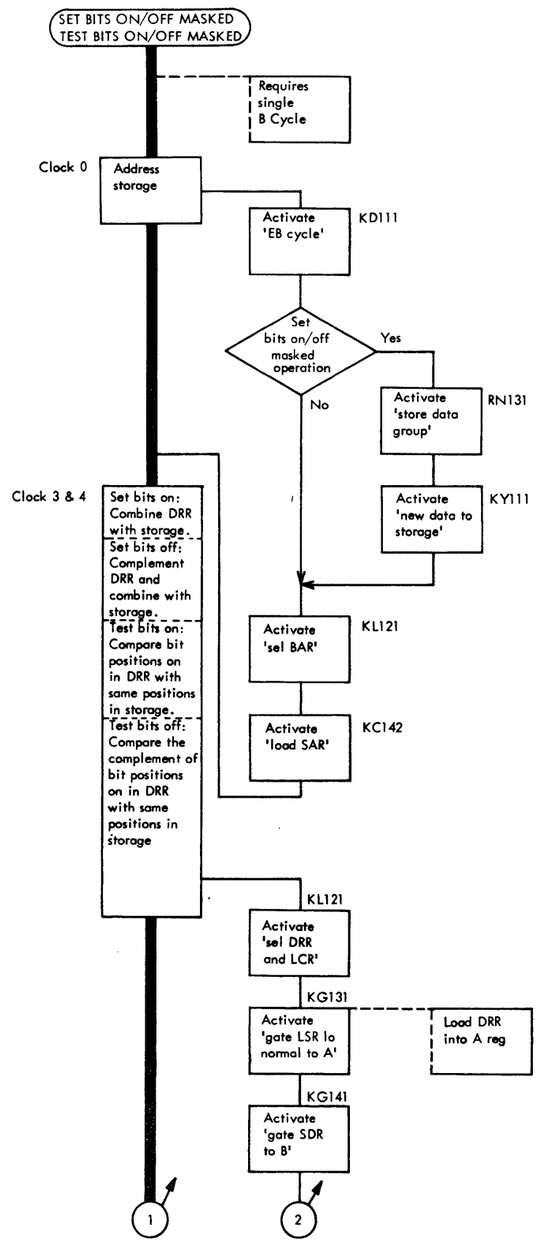
- Ignore bits which correspond with bits not present in the Q code
- Turn on 'test false' latch if selected bits are not all off

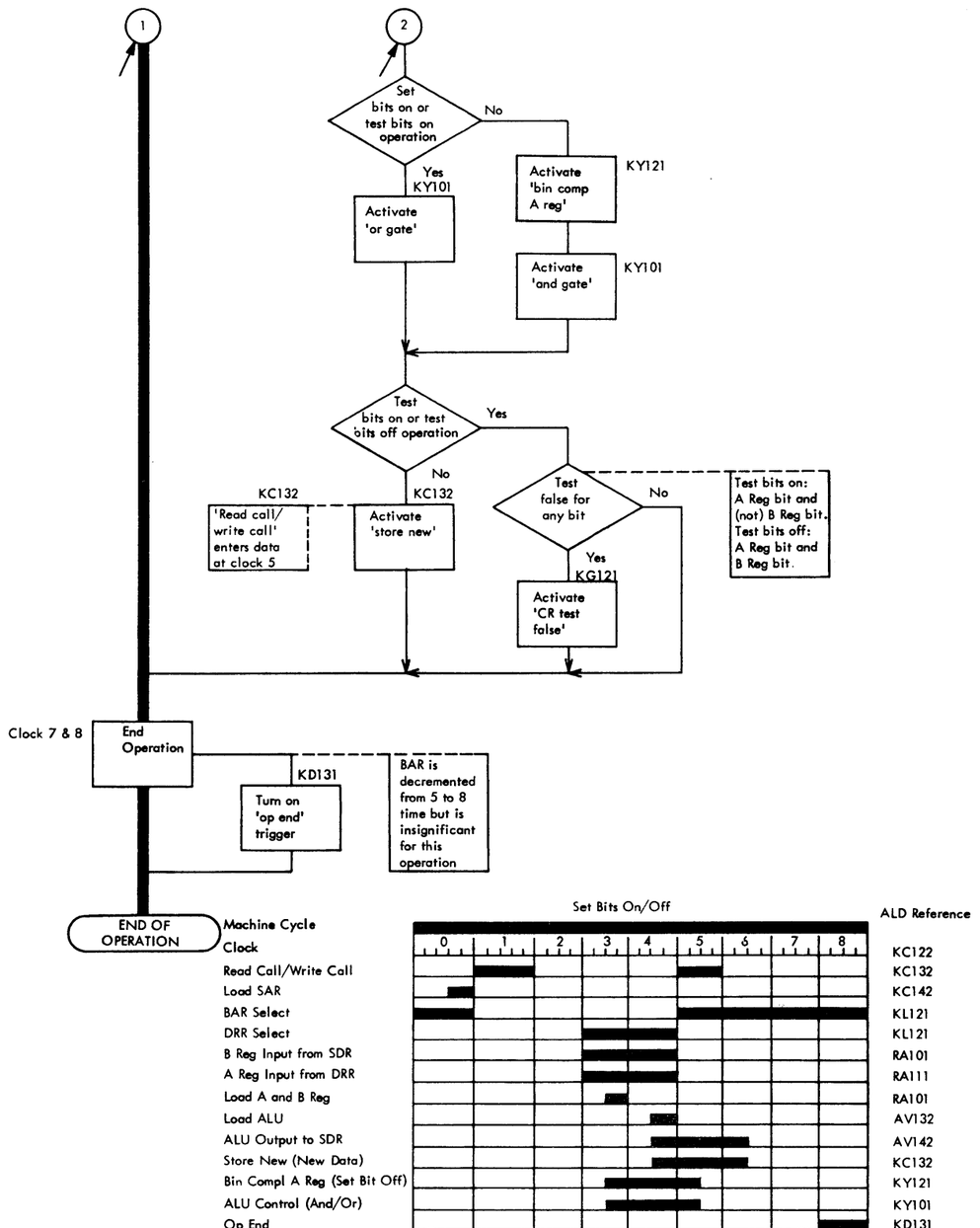
▶

D

▶

E





A

B

C

D

E

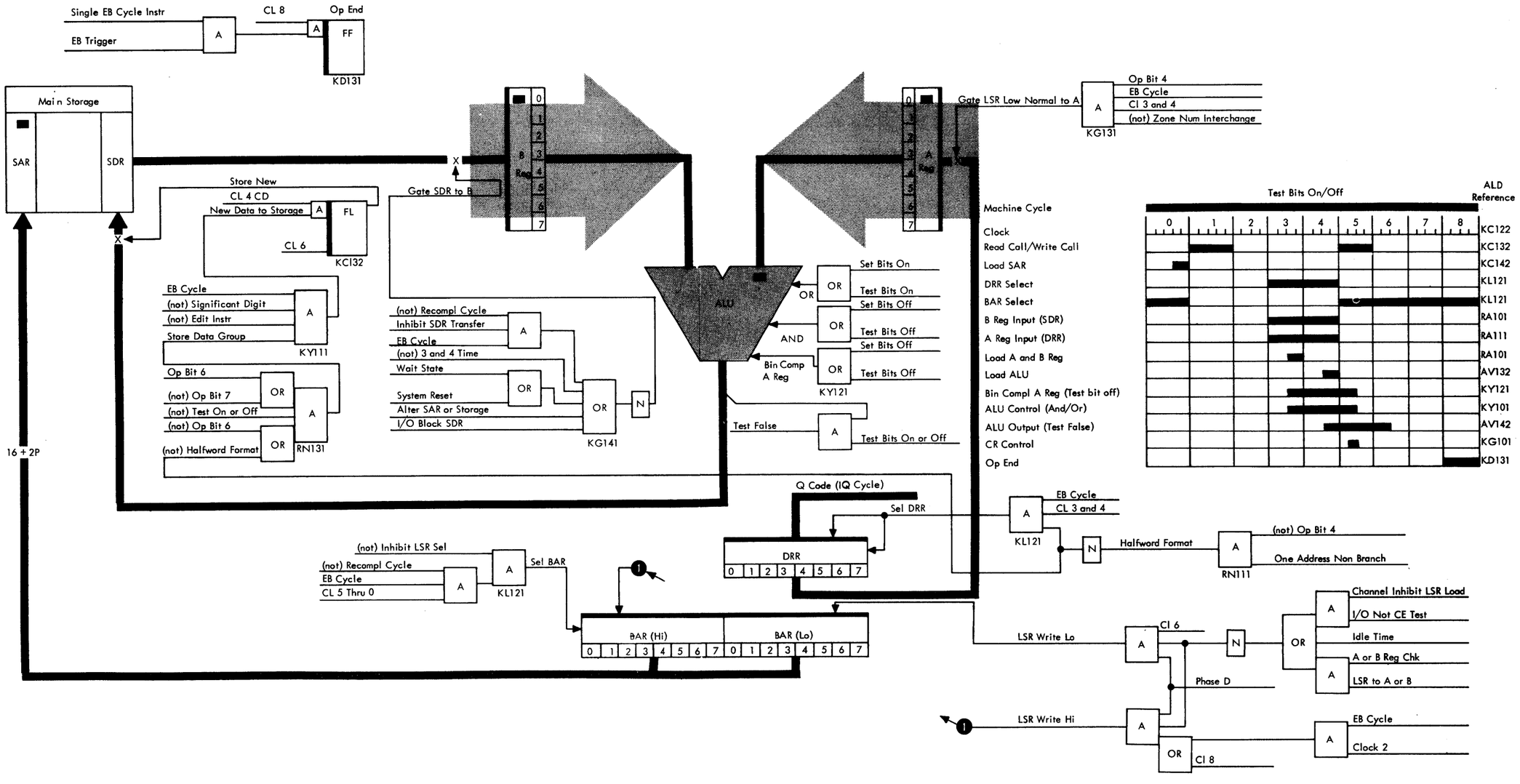


Diagram 5-052. Set Bits On/Off Masked and Test Bits On/Off Masked (PART 2 of 2)

2 3 4 5 6 7 8 9

A

Objectives:

bits - 0 1 2 3 4 5 6 7

Store Register Op Code X X 1 1 0 1 0 0

- Store the registers which are selected by the Q code into the location specified by the BAR

bits - 0 1 2 3 4 5 6 7

Load Register Op Code X X 1 1 0 1 0 1

- Load the registers which are selected by the Q code with data from the location specified by the BAR

bits - 0 1 2 3 4 5 6 7

Add to Register Op Code X X 1 1 0 1 1 0

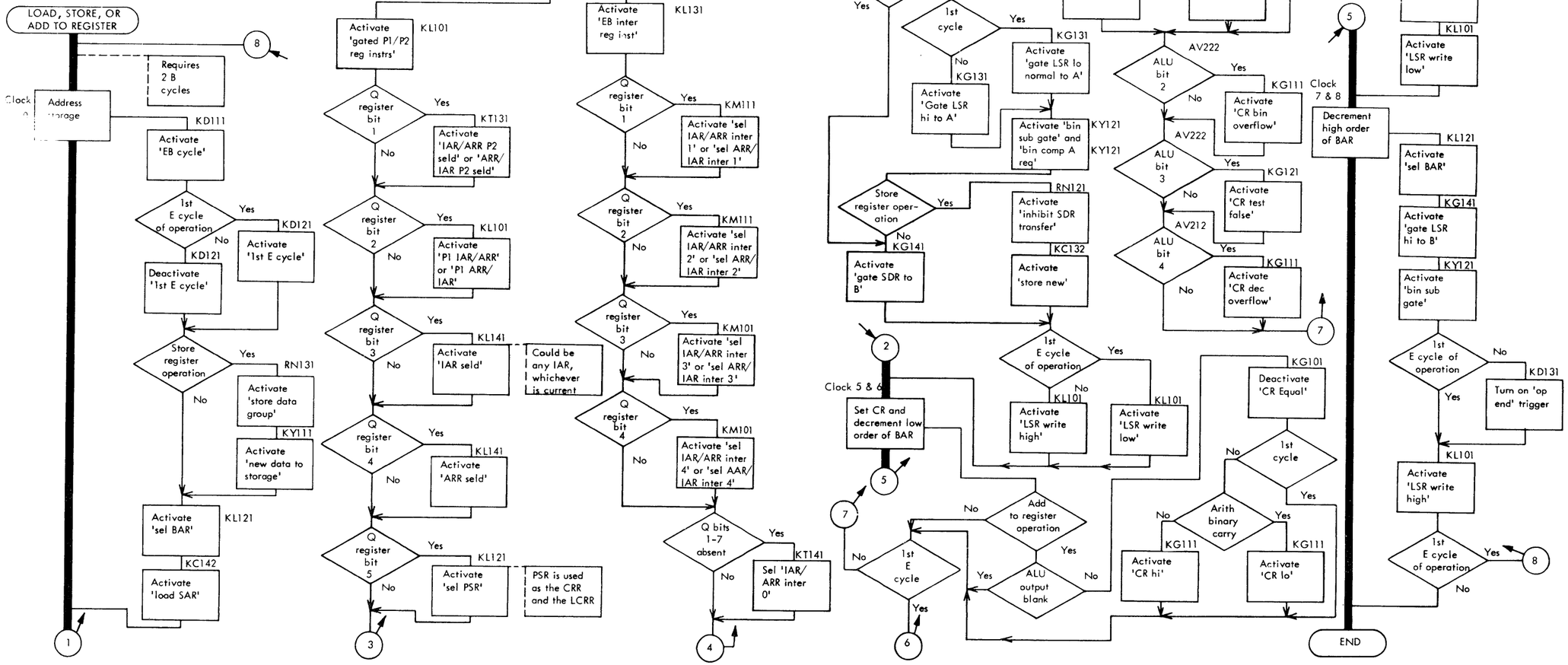
- Add the data from the location specified by the BAR to the contents of the registers which are selected by the Q code
- Load the results into the selected registers

B

C

D

E



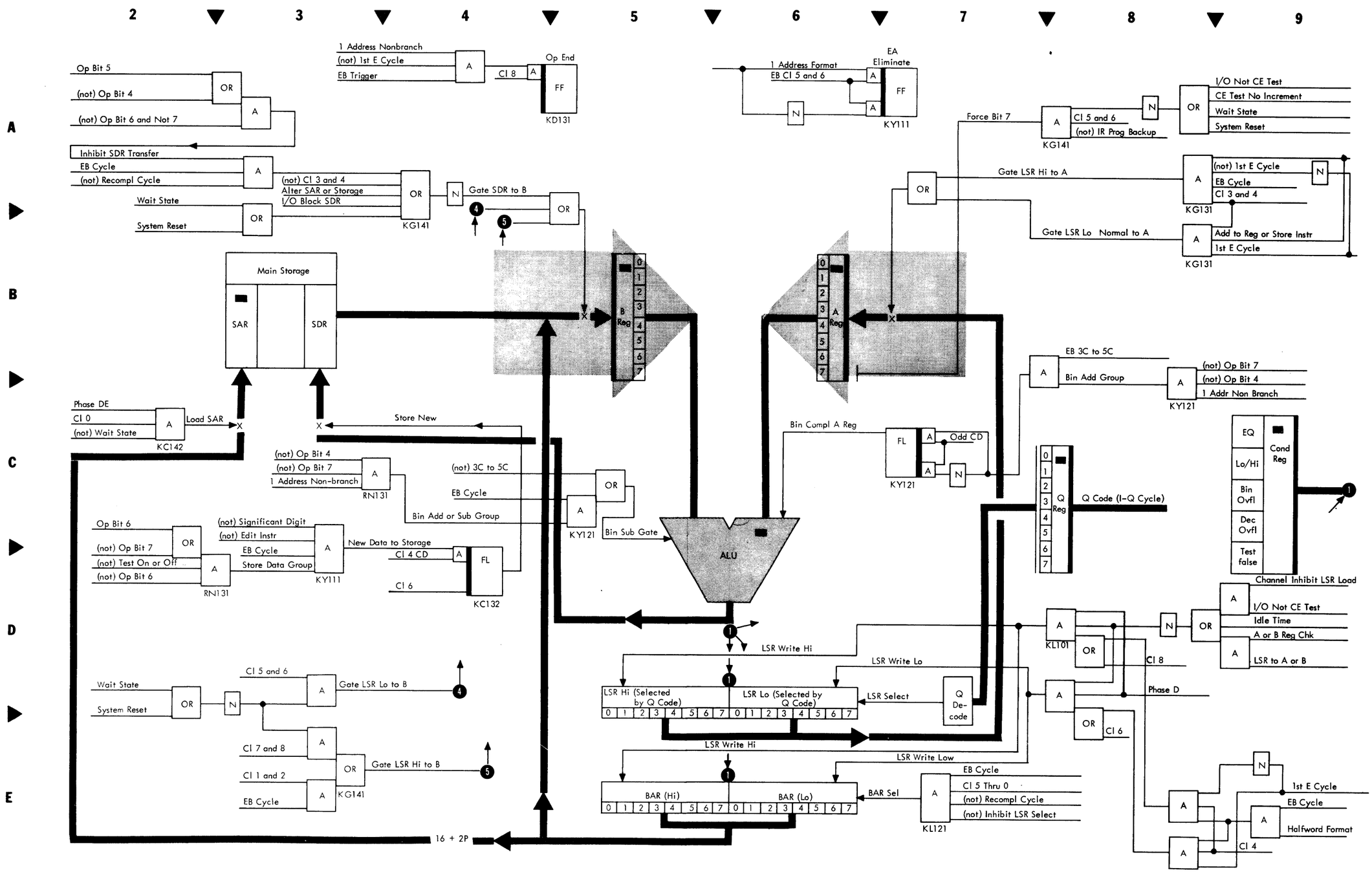
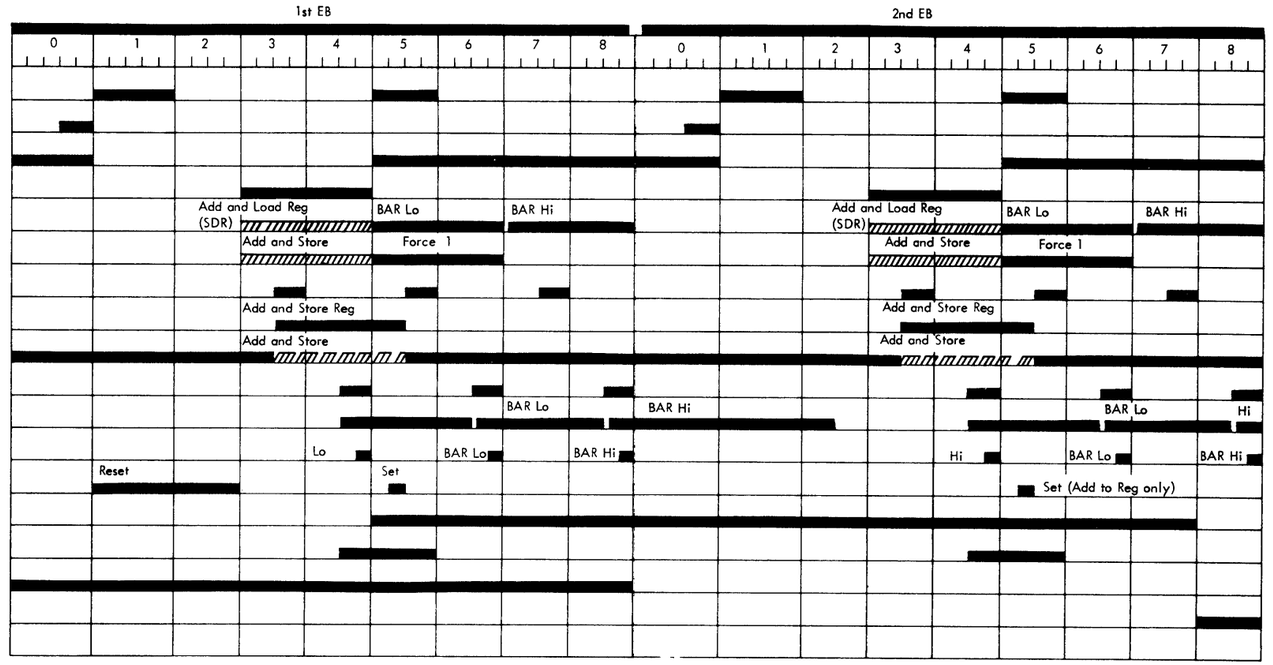


Diagram 5-062. Store, Load, or Add to Register (PART 2 of 3)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9



ALD Reference
KC122
KC132
KC142
KL121
KL121
RA101
RA111
RA101
KY121
KY101
AV132
AV142
KL101
KG111
KY111
KC132
KD111
KD131

LSR Selection		
Q Code bits	With Q bit 0	With No Q bit 0
1	Interrupt 1 IAR	P2-IAR
2	Interrupt 2 IAR	P1-IAR
3	Interrupt 3 IAR	IAR
4	Interrupt 4 IAR	ARR
5	———	PSR
6	———	XR2
7	———	XR1
No other bits	Interrupt 0 IAR	———

Condition Register						
Operation	Equal	Low	High	Binary Overflow	Test False	Decimal Overflow
Load PSR	If ALU bit 7	If ALU bit 6, not 7	If ALU not bit 6 or 7	If ALU bit 2	If ALU bit 3	If ALU bit 4
Add to Register	If Result is zero	If Result is not zero and a high order carry	If Result is not zero and no high order carry	If Result is too large for Register (no high order carry)	———	———

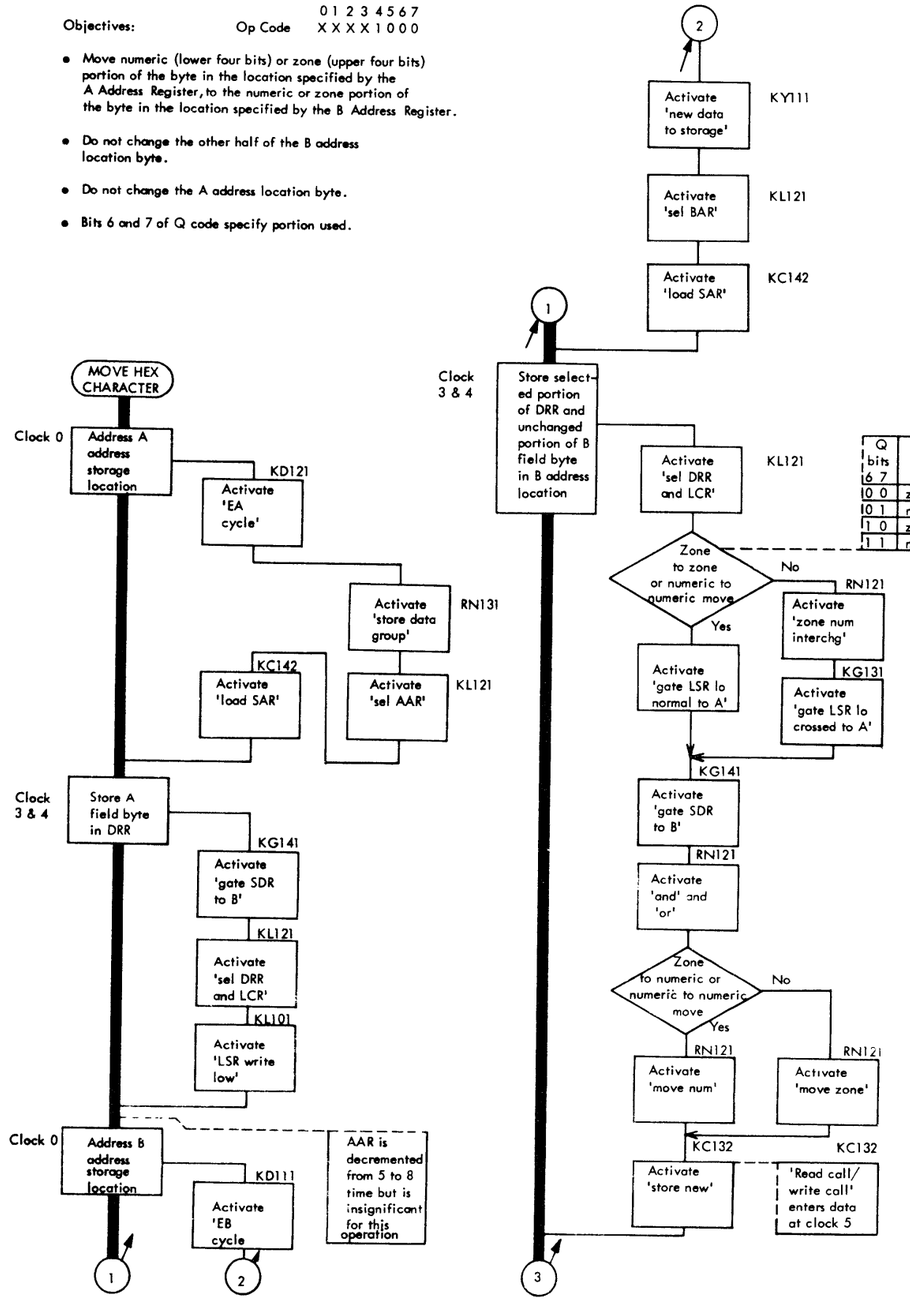
A ▶ B ▶ C ▶ D ▶ E

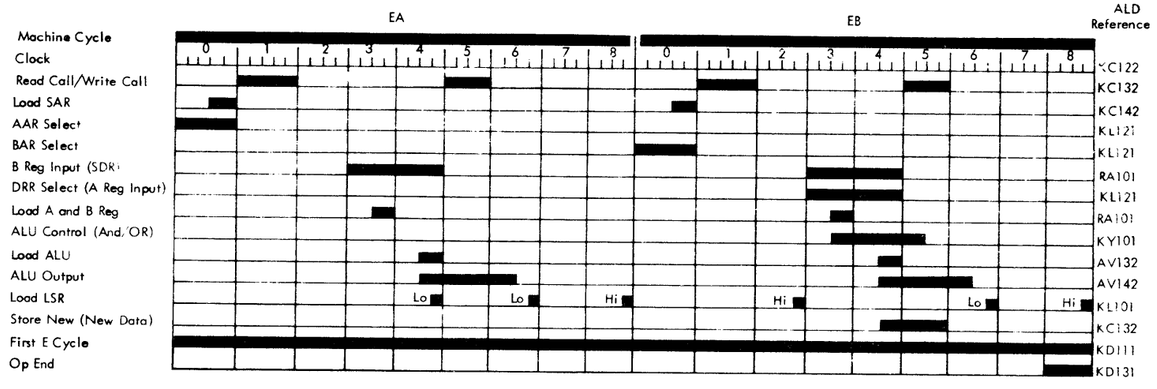
Diagram 5-064. Store, Load, or Add to Register (PART 3 of 3)

2 3 4 5 6 7 8 9

Objectives: Op Code 0 1 2 3 4 5 6 7 / X X X X 1 0 0 0

- Move numeric (lower four bits) or zone (upper four bits) portion of the byte in the location specified by the A Address Register, to the numeric or zone portion of the byte in the location specified by the B Address Register.
- Do not change the other half of the B address location byte.
- Do not change the A address location byte.
- Bits 6 and 7 of Q code specify portion used.





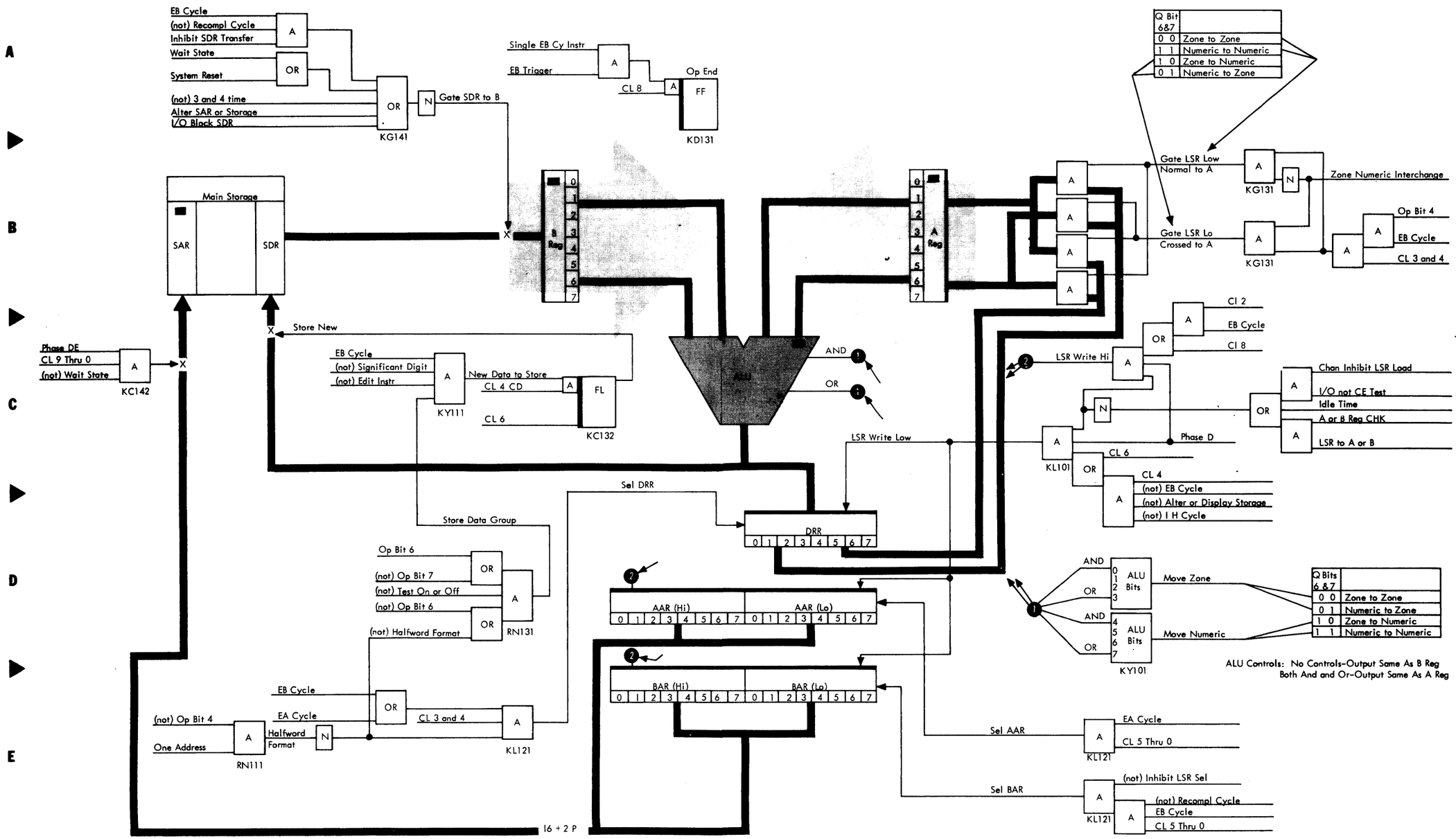
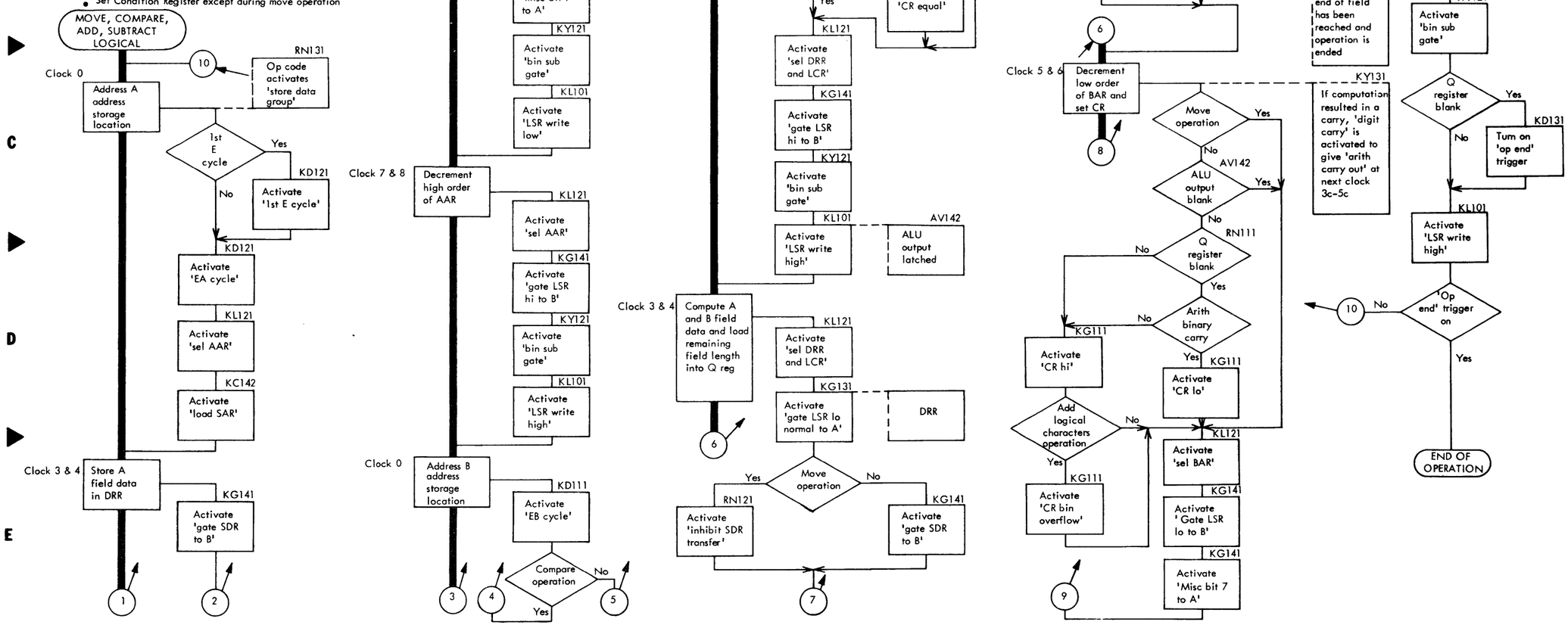


Diagram 5-072. Move Hex Character (PART 2 of 2)

Objectives:

1. Move Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 0 0
   - Move the contents of the A field to the B field
2. Compare Logical Chars. — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 0 1
   - Compare the A field data with the B field data
3. Add Logical Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 1 0
   - Binary add the A field data to the B field data and store results in B field location
4. Subtract Logical Characters — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 1 1 1 1
   - Binary subtract the A field data from the B field data and store results in B field location
5. All Operations
   - A and B fields are same length
   - Length of field is Q code plus 1
   - Set Condition Register except during move operation



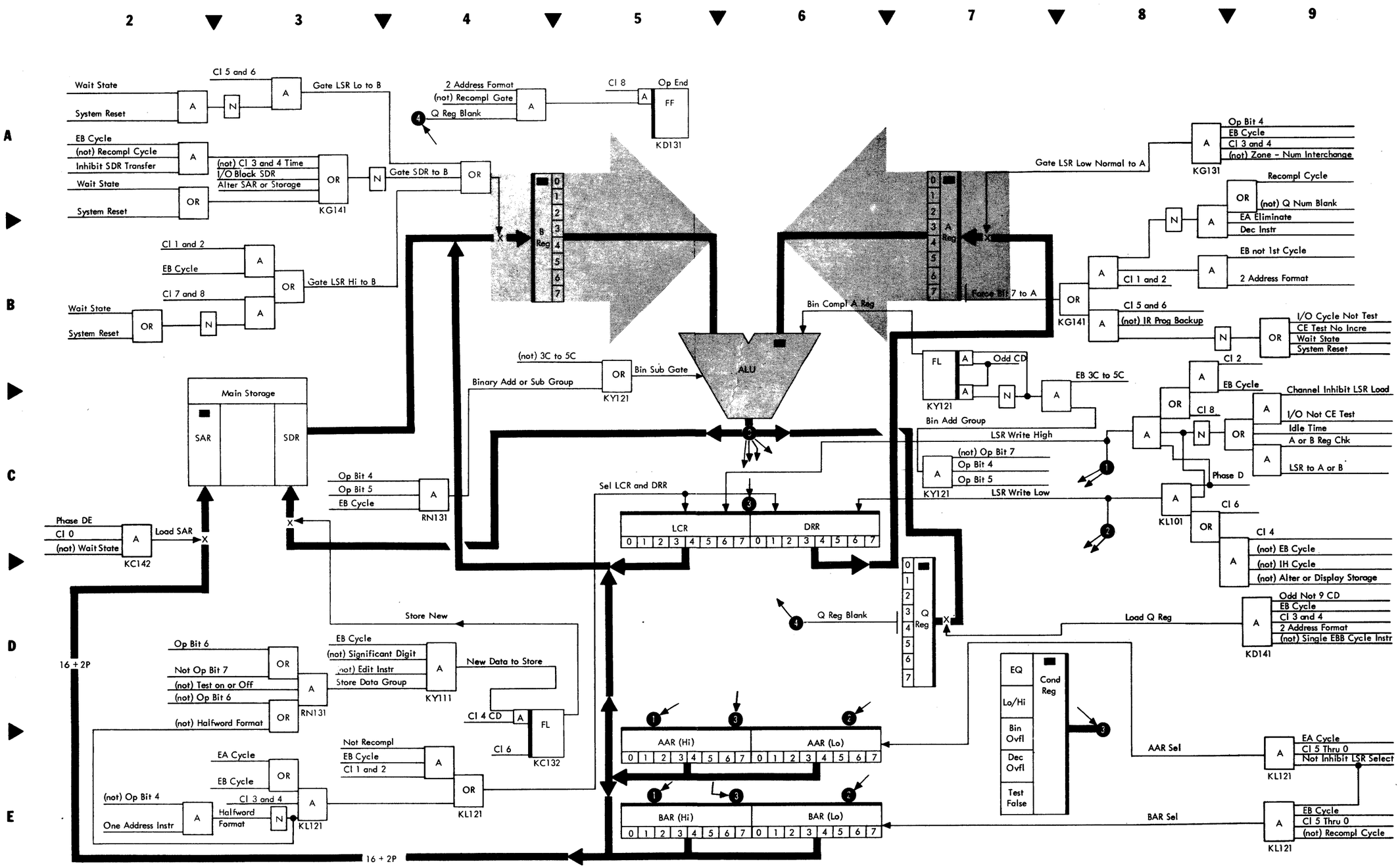
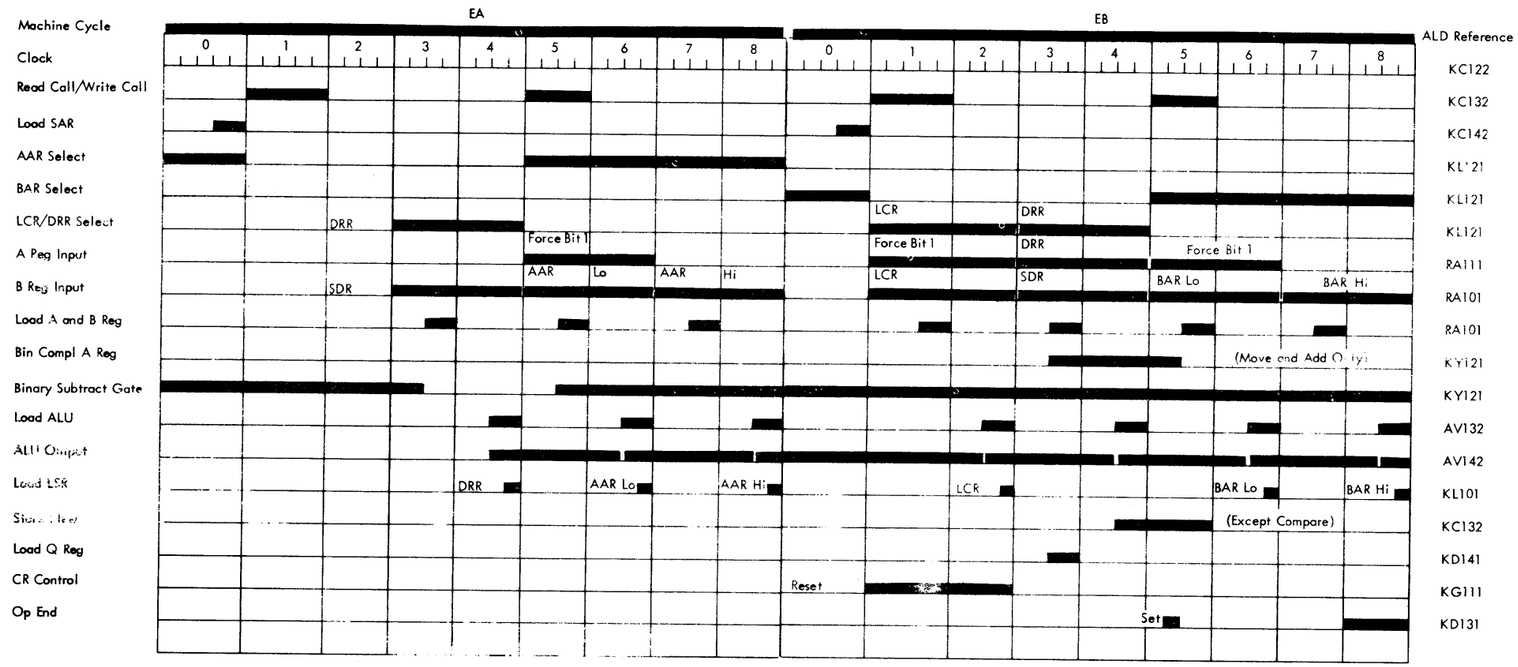


Diagram 5-082. Move Characters or Compare, Add, or Subtract Logical Characters (PART 2 of 3)



Condition Register				
Operation	Equal	Low	High	Binary Overflow
Move				
Add	If Result is zero	If Result not zero and a high order carry	If Result not zero and no high order carry	Result too large for field (no high order carry)
Subtract	If A field equals B field	If B field is lower than A field	If B field is higher than A field	
Compare	If A field equals B field	If B field is lower than A field	If B field is higher than A field	

A B C D E

(not) Recompl Cycle
Inhibit SDR Transfer
EB Cycle
Wait State
System Reset
(not)3 and 4
Alter SAR or Storage
I/O Block SDR
A
OR
OR
N
Gate SDR to B
KG141

Single EB Instr
EB Trigger
A
CL 8
A
FF
Op End
KD131

Main Storage
SAR
SDR
X
B Reg 0 1 2 3 4 5 6 7

ALU Blank
Bin Add or Sub No Move EB
Cl 5B
A
CR Equal
FL
KG101

CR Equal
N
Low
A
CR Low
High
A
CR High

Gate LSR Lo Normal to A
A
KG131
Op Bit 4
EB Cycle
Cl 3 and 4
(not) Zone - Num Interchange

A Reg 0 1 2 3 4 5 6 7
X

ALU
Bin Sub
OR
KY121
(not) 3C to 5C
Bin Add or Sub Group
A
Op Bit 4
Op Bit 5

Phase DE
Cl 0
(not) Wait State
A
Load SAR
X
KC142

EB Cycle
A
Bin Add or Sub No Move EB
Op End Gate
A

Op Bit 4 & 5
Op Bit 7
A
Bin Add or Sub Not Move

First E Cycle
Cl 1 and 2
A
KG101
Reset CR Lo

CR Lo/Hi
Cl 5 B
A
FL
OR
KG111

Edit Instr
EB Cycle
A
N
KG101

Arith Carry Out

Q Code
(IQ Cycle)

Sel DRR

DRR
0 1 2 3 4 5 6 7

Cl 1 and 2
Load CR Instr
First E Cycle
A
Reset CR
KG101

(not) Recompl Cycle
EB Cycle
Cl 5 thru 0
A
Sel BAR

BAR (Hi) 0 1 2 3 4 5 6 7
BAR (Lo) 0 1 2 3 4 5 6 7

(not) Op Bit 4
One Address Non-Branch
A
Halfword Format
N
EB Cycle
Cl 3 and 4
A
KL121

16 + 2P

	Bits 0 1 2 3 4 5 6 7	ALD Reference
	CLI Op Code X X 1 1 1 0 1	
Machine Cycle (EB)		KC122
Clock	0 1 2 3 4 5 6 7 8	KC132
Read Call/Write Call		KC142
Load SAR		KL121
BAR Select		KL121
DRR Select		RA101
B Reg Input (SDR)		RA111
A Reg Input (DRR)		RA101
Load A and B Reg		KY121
ALU Control (Bin Sub)		AV132
Load ALU		AV142
ALU Output (to CR)		KG111
CR Reset		KG111
CR Set		KD131
Op End		

Diagram 5-090. Compare Logical Immediate (PART 1 of 3)

2 3 4 5 6 7 8 9

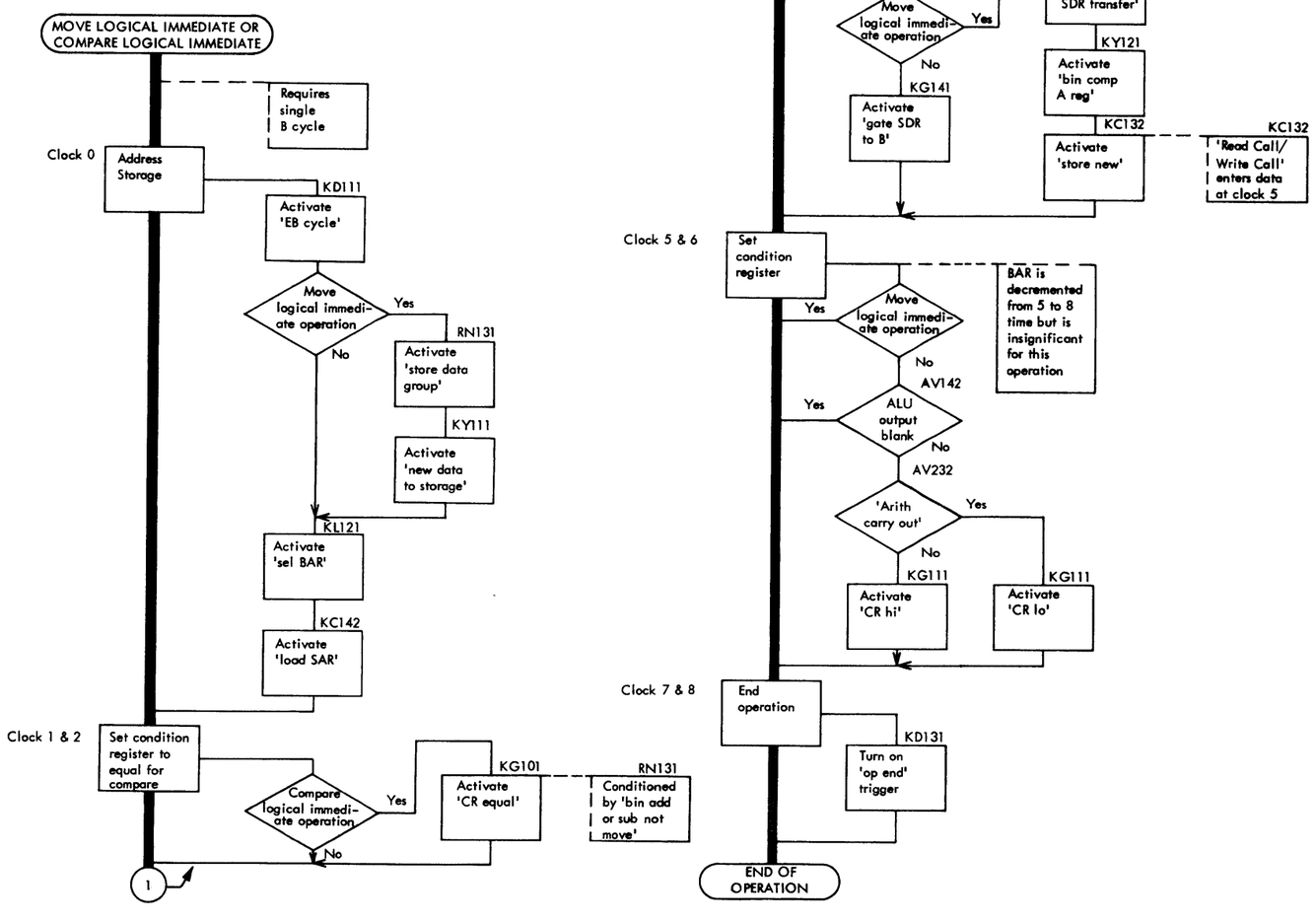
Objectives

		bits 0 1 2 3 4 5 6 7
Move Logical Immediate	Op Code	X X 1 1 1 1 0 0

- Store the Q code, which is located in the Data Recall Register, in the location specified by the B Address Register

		bits 0 1 2 3 4 5 6 7
Compare Logical Immediate	Op Code	X X 1 1 1 1 0 1

- Compare the Q code, which is located in the Data Recall Register, with the data in the location specified by the B Address Register
- Record the result of the comparison in the Condition Register



A

B

C

D

E

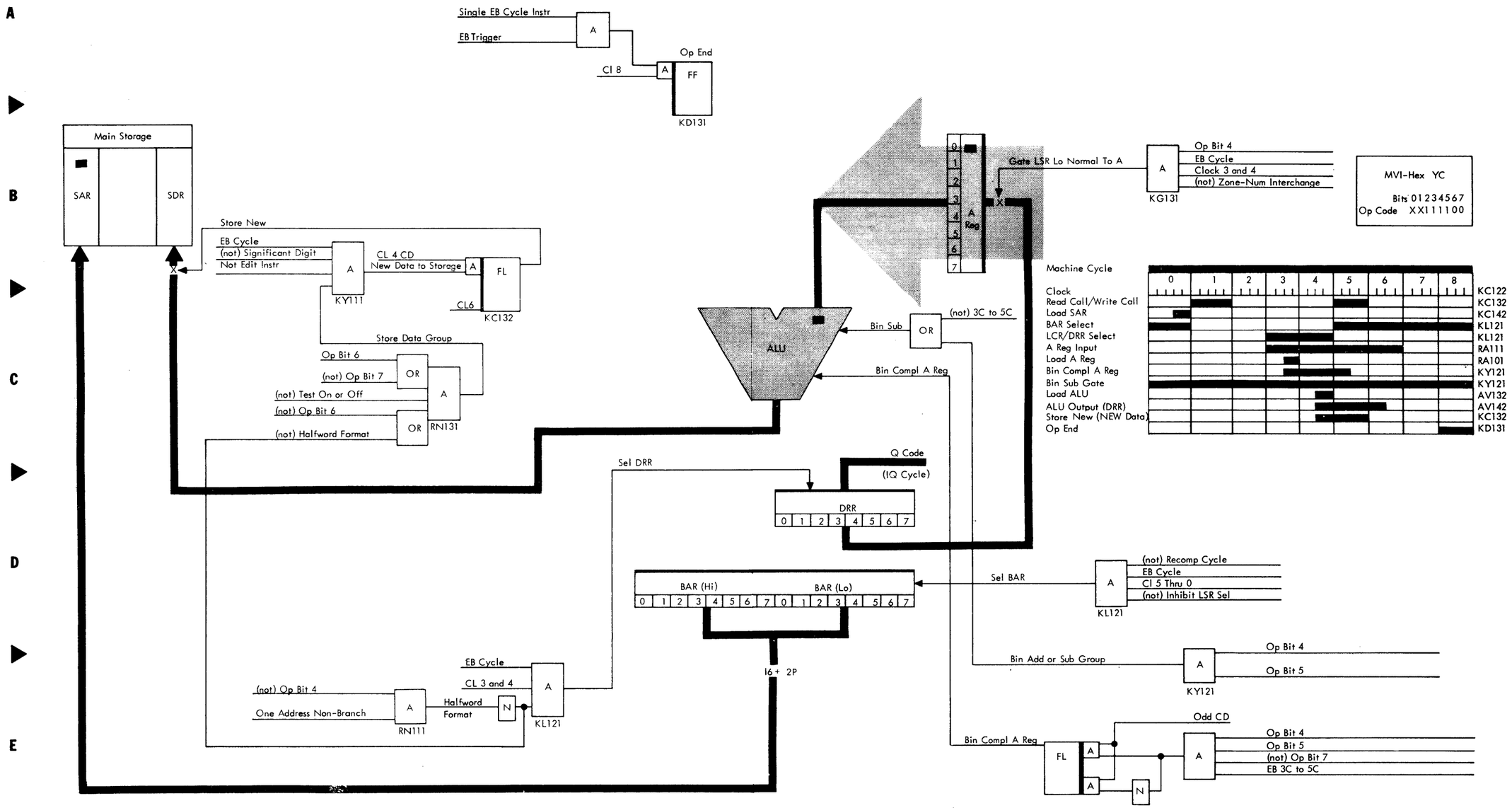


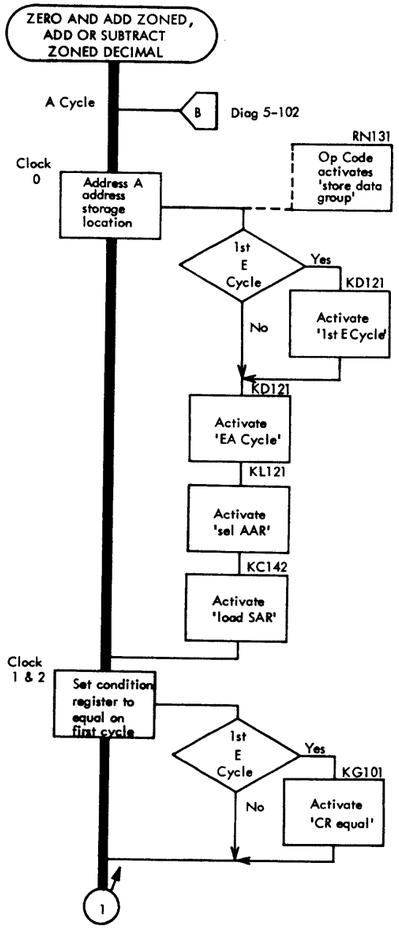
Diagram 5-094. Move Logical Immediate (PART 3 of 3)

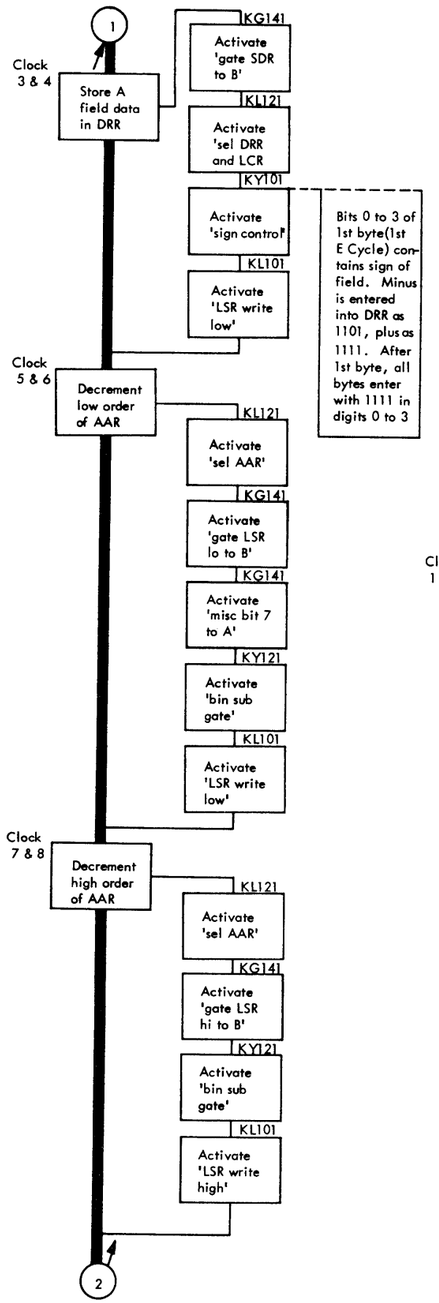
Objectives:

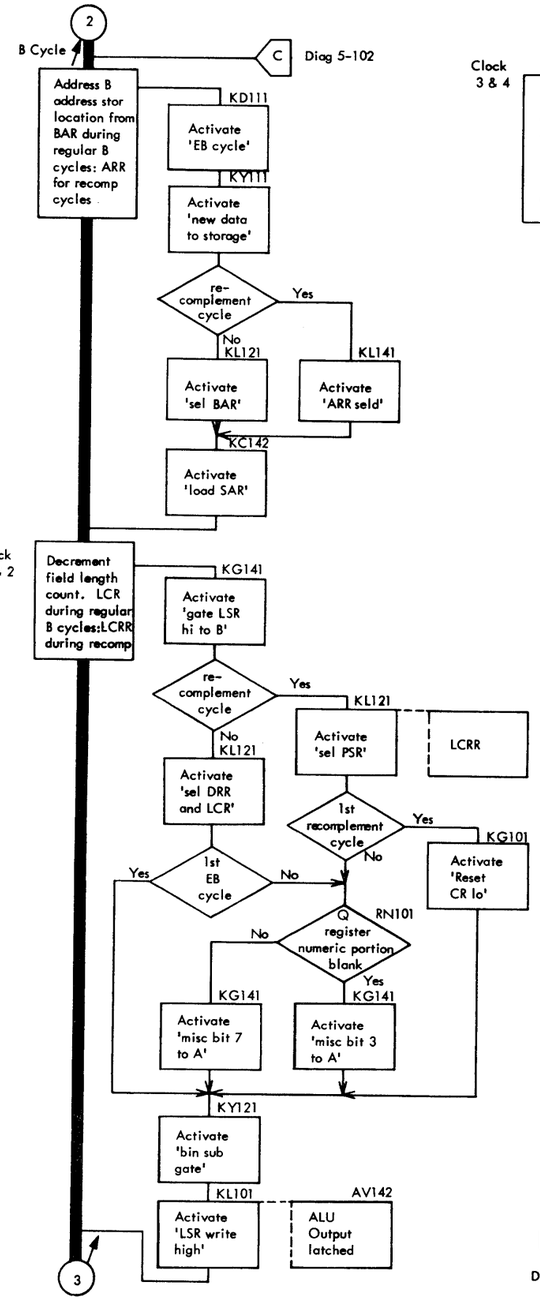
1. Zero and Add Zoned — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 0 1 0 0
   - Decimally add A field data to zeros and place results in B field location

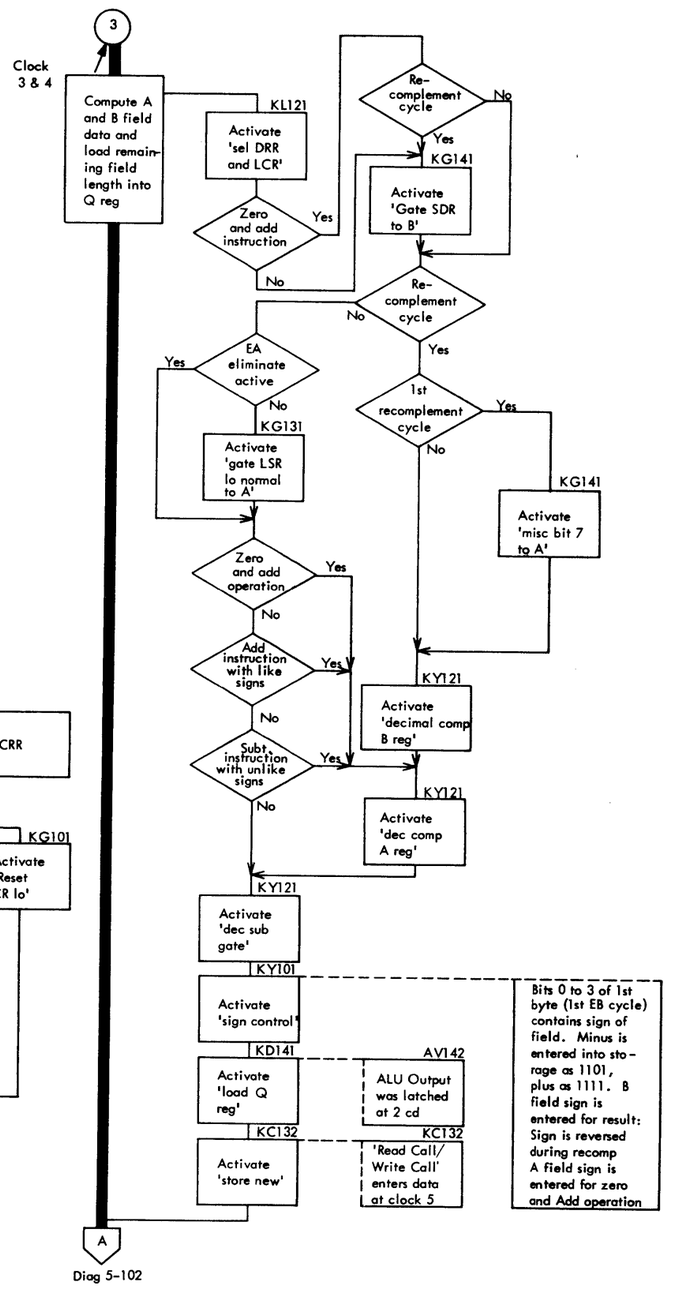
2. Add Zoned Decimal / Subtract Zoned Decimal — Op Code bits 0 1 2 3 4 5 6 7 = X X X X 0 1 1 0 / X X X X 0 1 1 1
   - Decimally add A field data to B field or subtract A field data from B field
   - Instruction and signs of fields determine add or subtract function

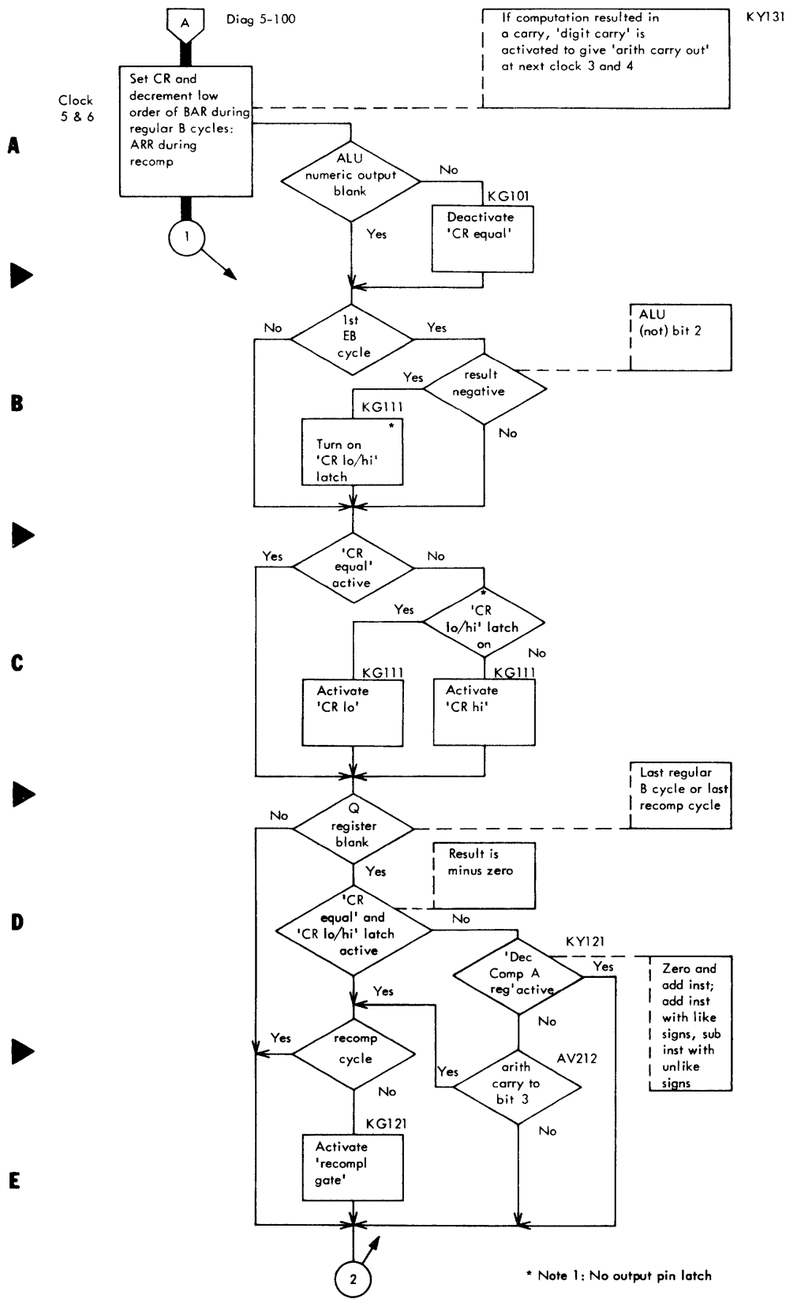
3. All Operations
   - Length of A field is numeric portion of Q code + 1
   - B field is longer than A field by amount in zone portion of Q code

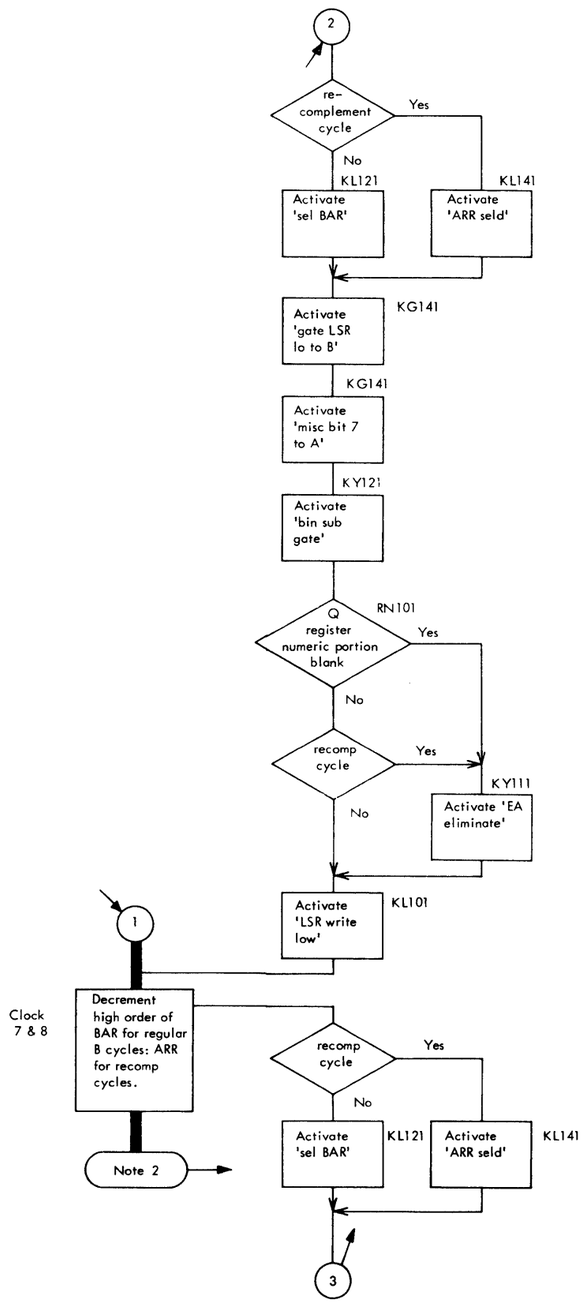


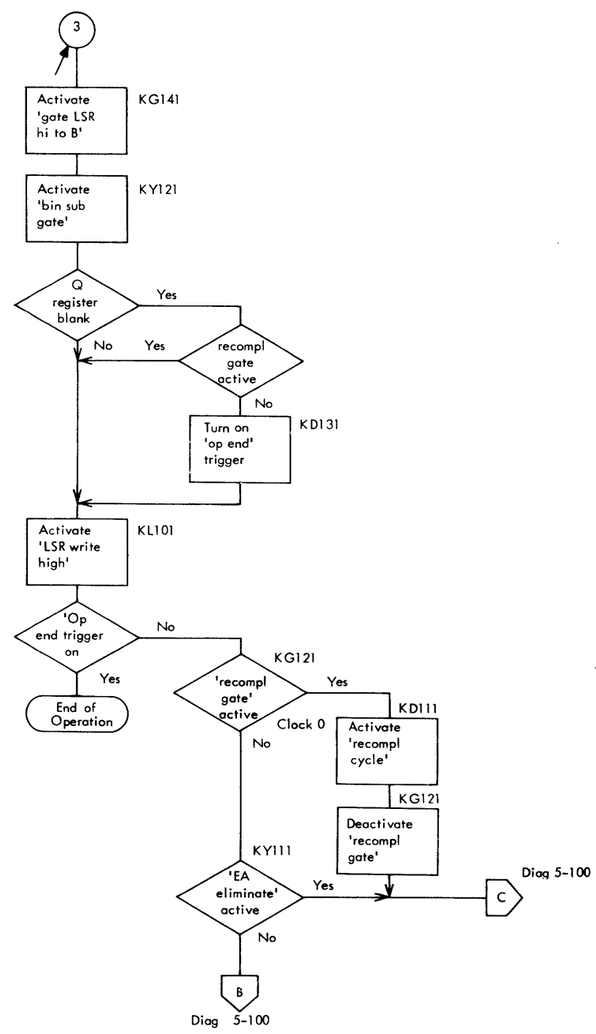






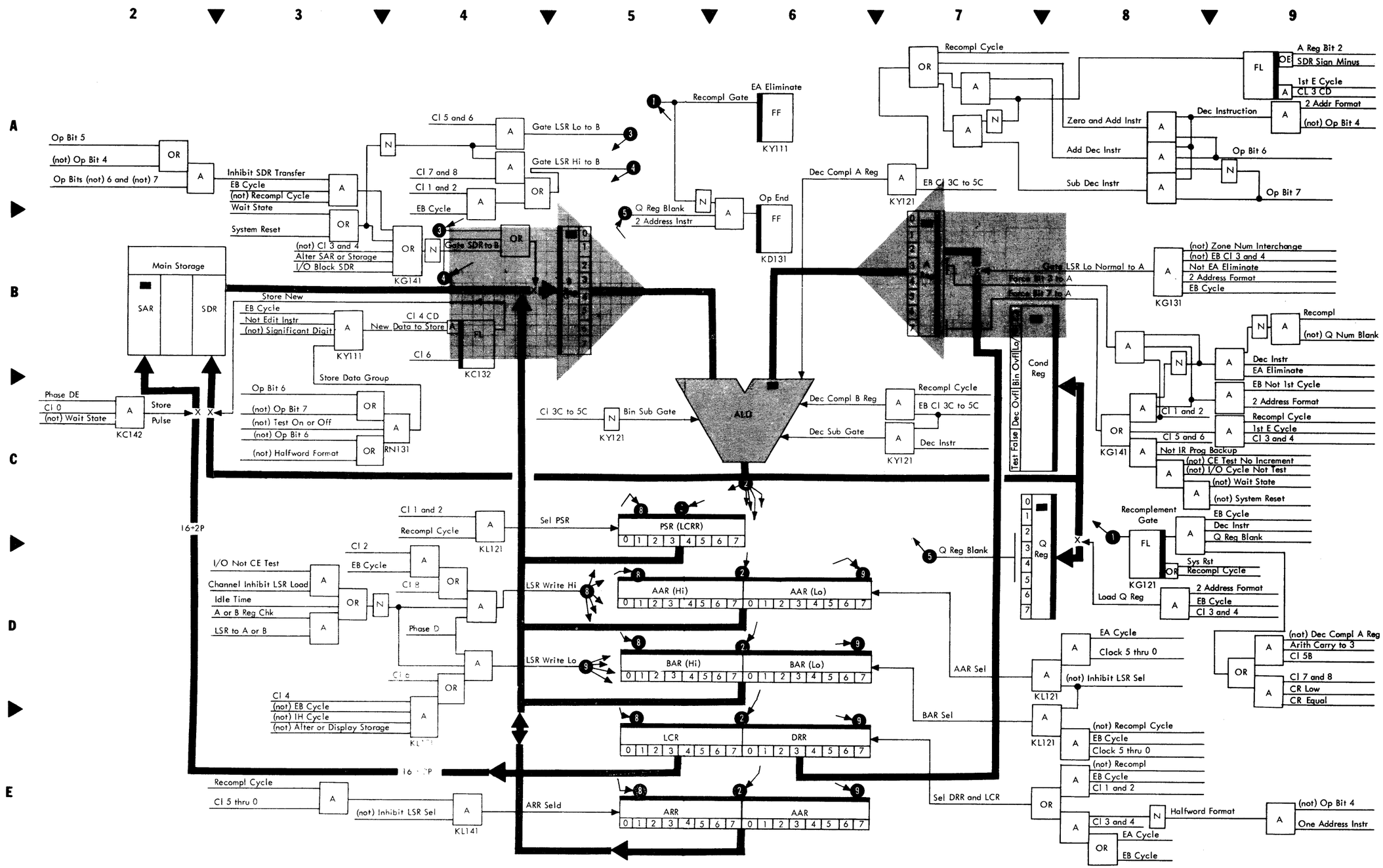


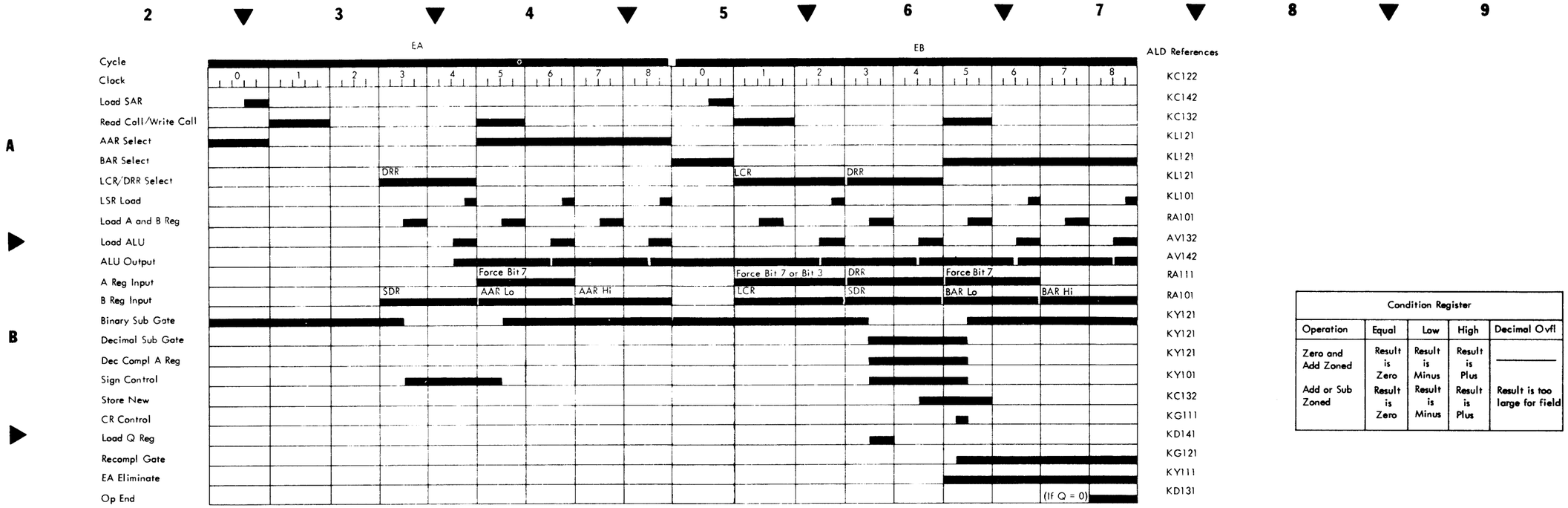




Note 2: Operation repeats A and B cycles until end of A field (Q register numeric portion blank). 'EA eliminate' then allows B cycles until end of B field (Q register blank). Operation ends unless result is in complement form. To recomplement, the low order of the B field is established by the ARR and the length of the field is established by the LCRR. 'EA eliminate' then allows B cycles until end of field (Q register blank). Operation ends.

Diagram 5-102. Zero and Add Zoned and Add or Subtract Zoned Decimal (PART 2 of 4)


2
3
4
5
6
7
8
9
A
B
C
D
E
Op Bit 5
(not) Op Bit 4
Op Bits (not) 6 and (not) 7
OR
A
Inhibit SDR Transfer
EB Cycle
(not) Recompl Cycle
Wait State
System Reset
(not) Cl 3 and 4
Alter SAR or Storage
I/O Block SDR
KG141
N
Cl 5 and 6
Gate LSR Lo to B
Gate LSR Hi to B
Cl 7 and 8
Cl 1 and 2
EB Cycle
Gate SDR to B
Recompl Gate
EA Eliminate
FF
KY111
Q Reg Blank
2 Address Instr
Op End
KD131
Recompl Cycle
Dec Compl A Reg
EB Cl 3C to 5C
KY121
Zero and Add Instr
Add Dec Instr
Sub Dec Instr
Dec Instruction
Op Bit 6
Op Bit 7
FL
A Reg Bit 2
SDR Sign Minus
1st E Cycle
CL 3 CD
2 Addr Format
(not) Op Bit 4
Main Storage
SAR
SDR
Store New
EB Cycle
Not Edit Instr
(not) Significant Digit
New Data to Store
Cl 4 CD
Cl 6
KC132
KY111
Store Data Group
Op Bit 6
(not) Op Bit 7
(not) Test On or Off
(not) Op Bit 6
(not) Halfword Format
RN131
Phase DE
Cl 0
(not) Wait State
Store
Pulse
KC142
Cl 3C to 5C
Bin Sub Gate
KY121
ALU
Dec Compl B Reg
Recompl Cycle
EB Cl 3C to 5C
Dec Sub Gate
Dec Instr
KY121
Gate LSR Lo Normal to A
Force Bit 3 to A
Force Bit 7 to A
(not) Zone Num Interchange
(not) EB Cl 3 and 4
Not EA Eliminate
2 Address Format
EB Cycle
KG131
Test False
Dec Ovfl
Bin Ovfl
Lo
Cond Reg
Recompl
(not) Q Num Blank
Dec Instr
EA Eliminate
EB Not 1st Cycle
2 Address Format
Recompl Cycle
1st E Cycle
Cl 3 and 4
Cl 1 and 2
Cl 5 and 6
Not IR Prog Backup
(not) CE Test No Increment
(not) I/O Cycle Not Test
(not) Wait State
(not) System Reset
KG141
Recomplement Gate
EB Cycle
Dec Instr
Q Reg Blank
Sys Rst
Recompl Cycle
KG121
Load Q Reg
2 Address Format
EB Cycle
Cl 3 and 4
16+2P
Cl 1 and 2
Recompl Cycle
KL121
Sel PSR
PSR (LCRR)
0 1 2 3 4 5 6 7
Cl 2
EB Cycle
Cl 8
I/O Not CE Test
Channel Inhibit LSR Load
Idle Time
A or B Reg Chk
LSR to A or B
LSR Write Hi
AAR (Hi)
AAR (Lo)
Phase D
Cl 6
Cl 4
(not) EB Cycle
(not) IH Cycle
(not) Alter or Display Storage
LSR Write Lo
BAR (Hi)
BAR (Lo)
LCR
DRR
Q Reg
Q Reg Blank
AAR Sel
BAR Sel
Sel DRR and LCR
EA Cycle
Clock 5 thru 0
(not) Inhibit LSR Sel
(not) Recompl Cycle
EB Cycle
Clock 5 thru 0
(not) Recompl
EB Cycle
Cl 1 and 2
Cl 3 and 4
EA Cycle
EB Cycle
Halfword Format
(not) Op Bit 4
One Address Instr
(not) Dec Compl A Reg
Arith Carry to 3
Cl 5B
Cl 7 and 8
CR Low
CR Equal
Recompl Cycle
Cl 5 thru 0
(not) Inhibit LSR Sel
KL141
ARR Seld
ARR
AAR



Condition Register				
Operation	Equal	Low	High	Decimal Ovfl
Zero and Add Zoned	Result is Zero	Result is Minus	Result is Plus	———
Add or Sub Zoned	Result is Zero	Result is Minus	Result is Plus	Result is too large for field

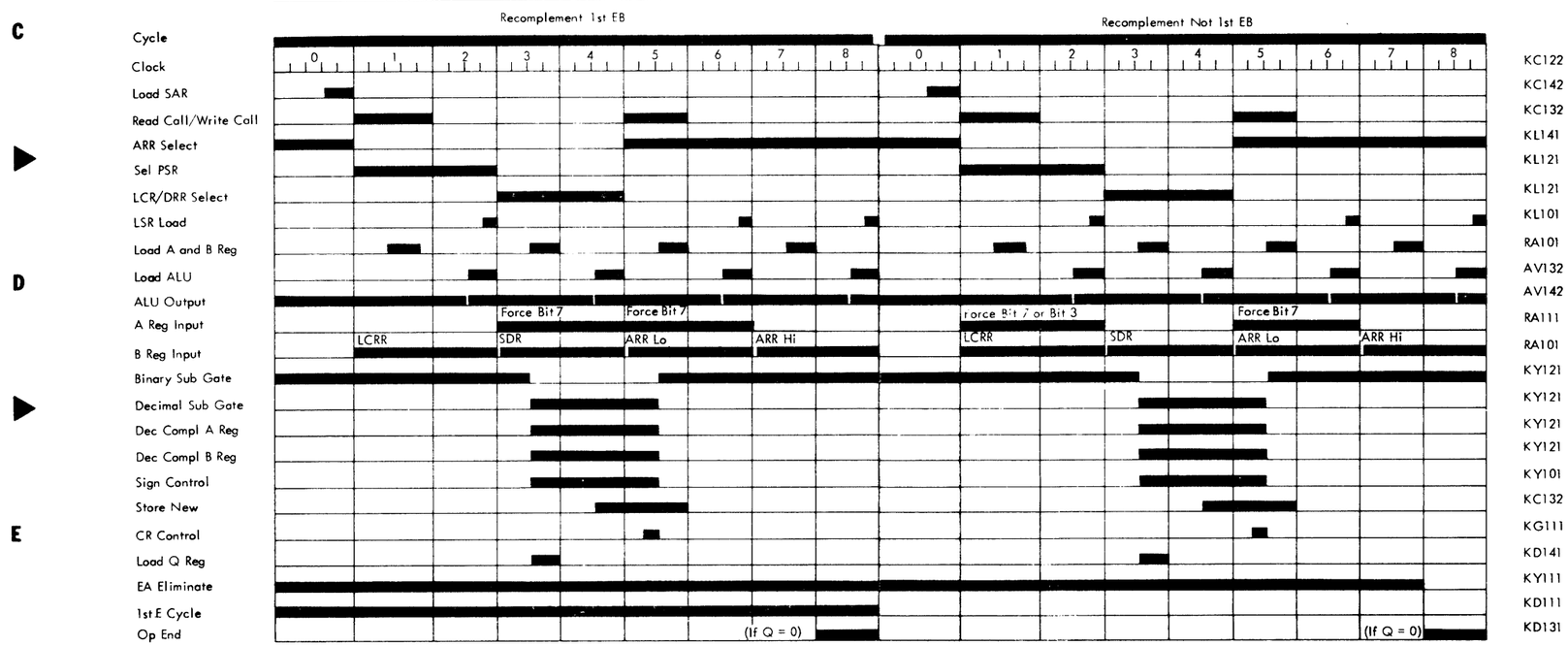


Diagram 5-106. Zero and Add Zoned and Add or Subtract Zoned Decimal (PART 4 of 4)

Objectives:

bits 0 1 2 3 4 5 6 7

Edit Op Code X X X X 1 0 1 0

- Replace hex 2/0 in B field with A field data
- Skip other characters in B field leaving them as they were
- Length of B field is Q code + 1
- A field sign stored in condition register

EXAMPLE:

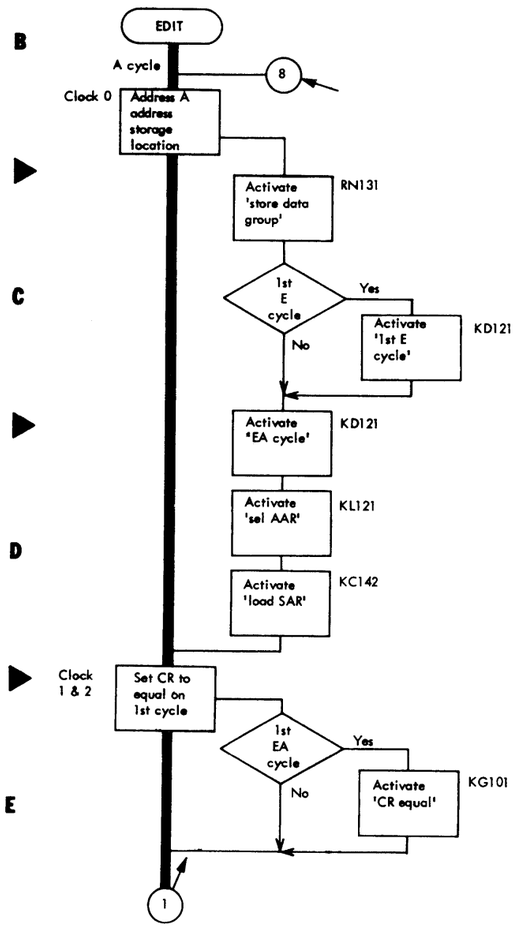
Q code = 9

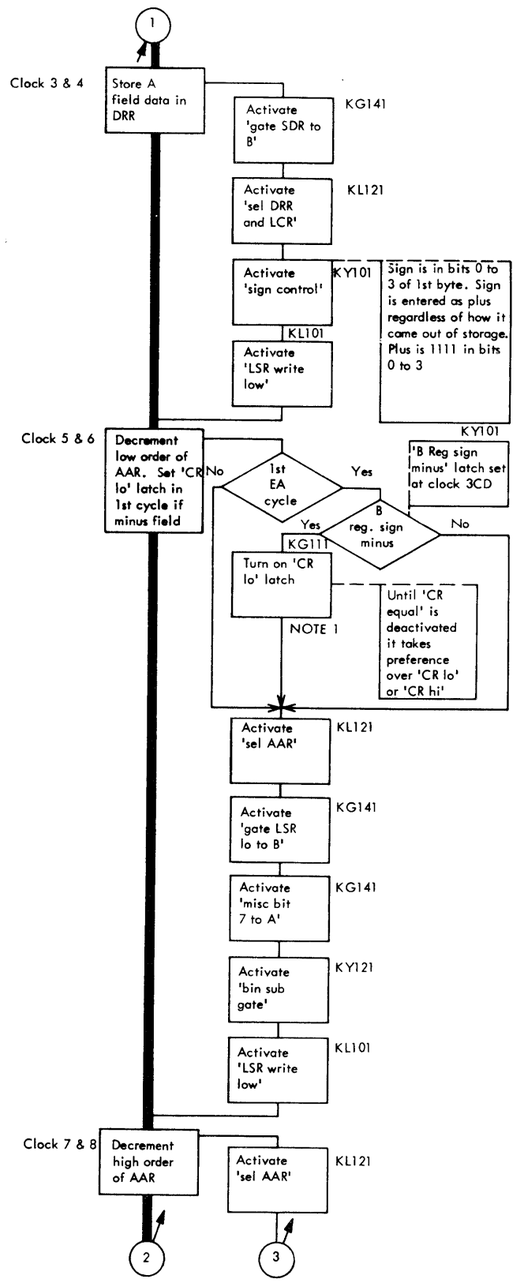
B field before edit X,XXX.XX

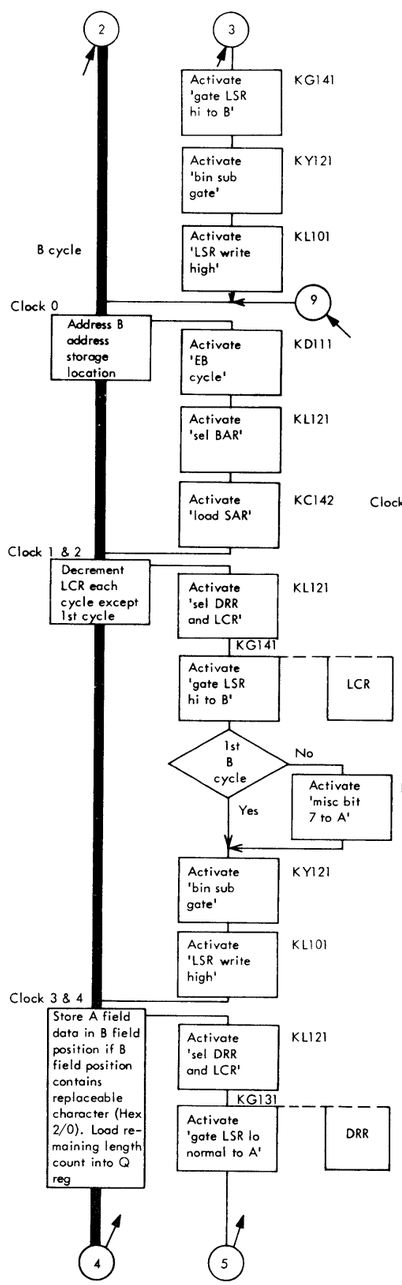
A field 090715 — blank

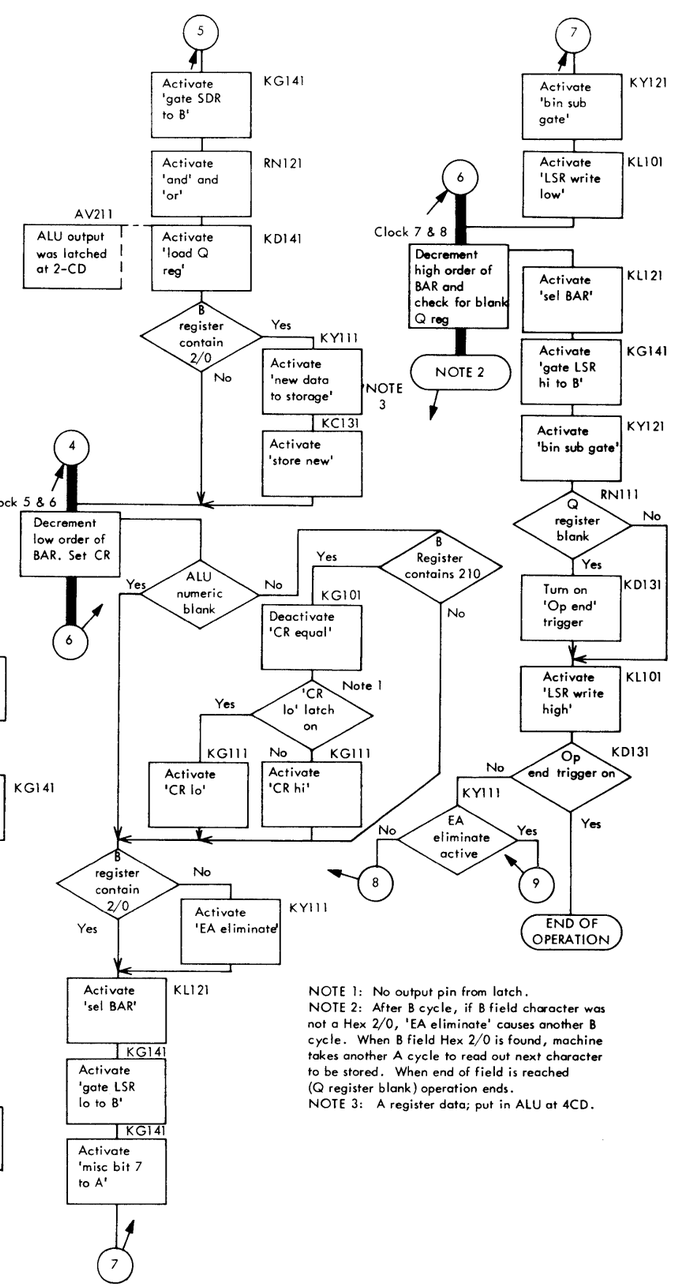
B field after edit 0,907.15

X=Replaceable Character (2/0)









NOTE 1: No output pin from latch.

NOTE 2: After B cycle, if B field character was not a Hex 2/0, 'EA eliminate' causes another B cycle. When B field Hex 2/0 is found, machine takes another A cycle to read out next character to be stored. When end of field is reached (Q register blank) operation ends.

NOTE 3: A register data; put in ALU at 4CD.

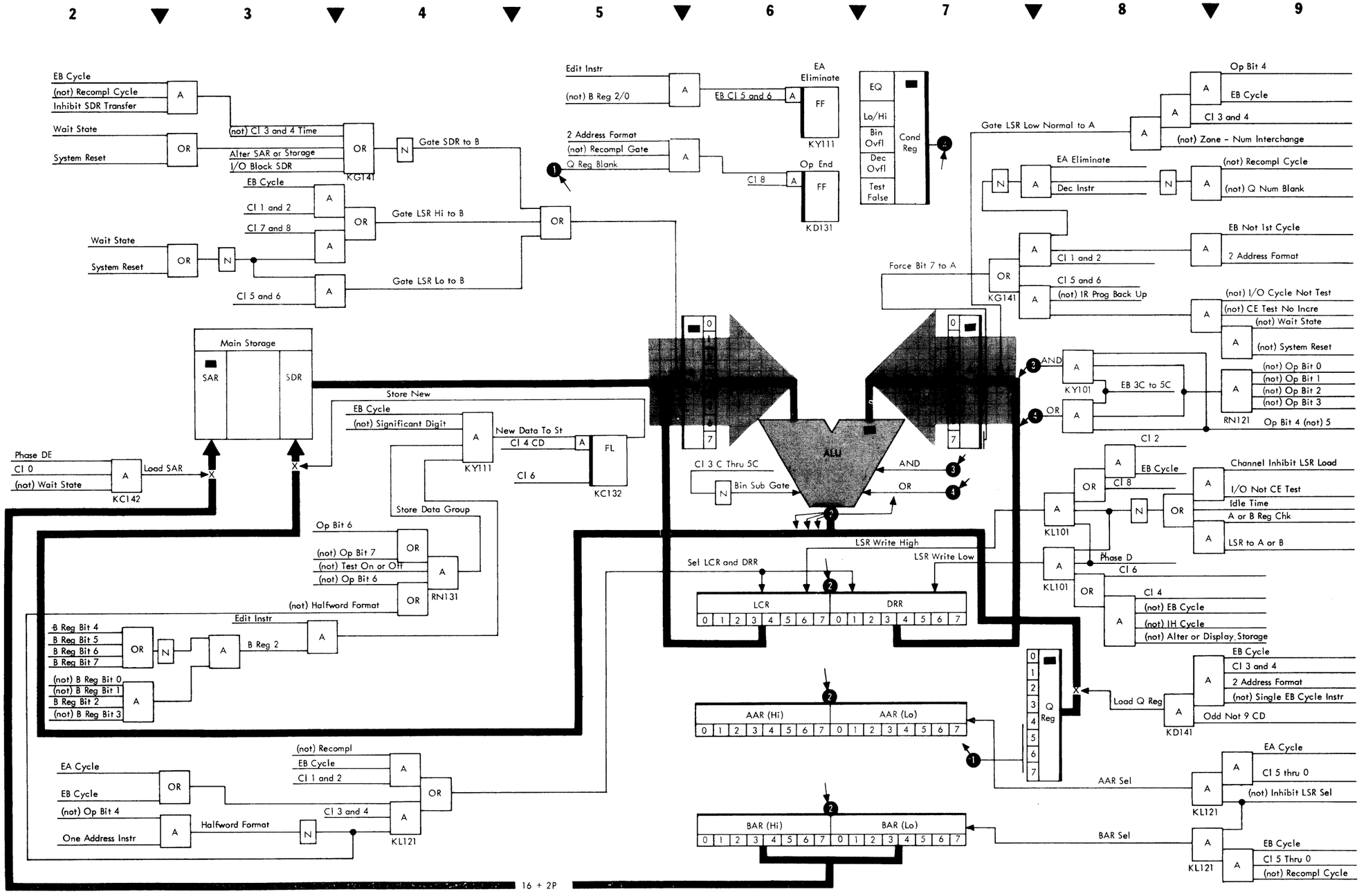
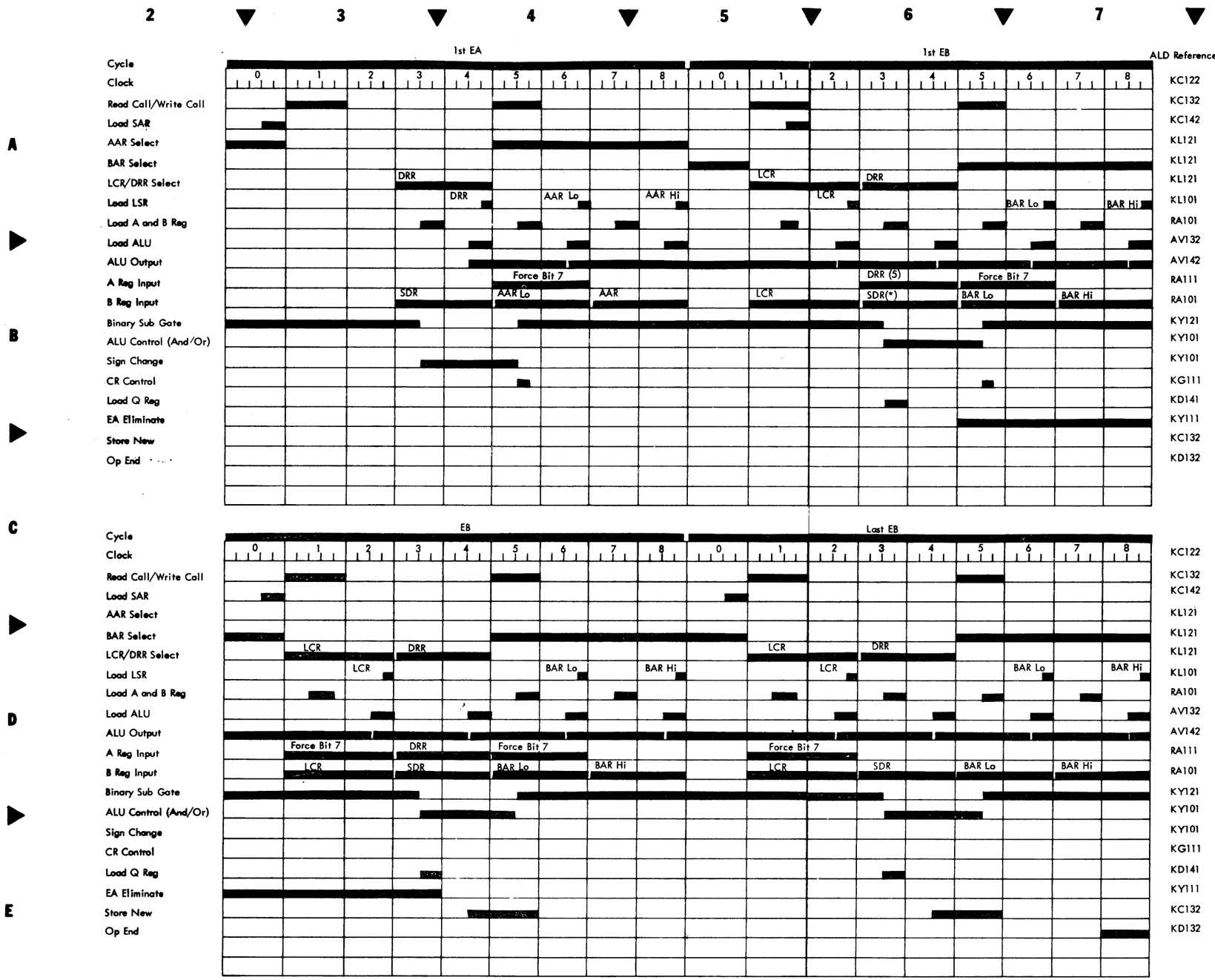


Diagram 5-112. Edit (PART 2 of 3)



Cycle	A	B	B	B	A	B	A	B	B	A	B	A	B	A	B	B
B Register	5	*	bl	X	1	X	7	·	X	0	X	9	X	0	,	X
A Register		5	5	5		1		7	7		0		9		0	0
Data Recall Register	5	5	5	5	1	1	7	7	7	0	0	9	9	0	0	0
Regenerate	5	*	bl		1		7	·		0		9		0	,	
New Data				5		1			7		0		9			0
Length Count	9	9	8	7	7	6	6	5	4	4	3	3	2	2	1	0

X = Replaceable Character

A Field	090715
B Field before edit	X,XXX.XX *
B Field after edit	0,907.15 * blank

Note: Since the A and B registers are loaded each odd CD clock time, the figures shown apply only to clock 3 and 4 time when the main storage data is being analyzed.

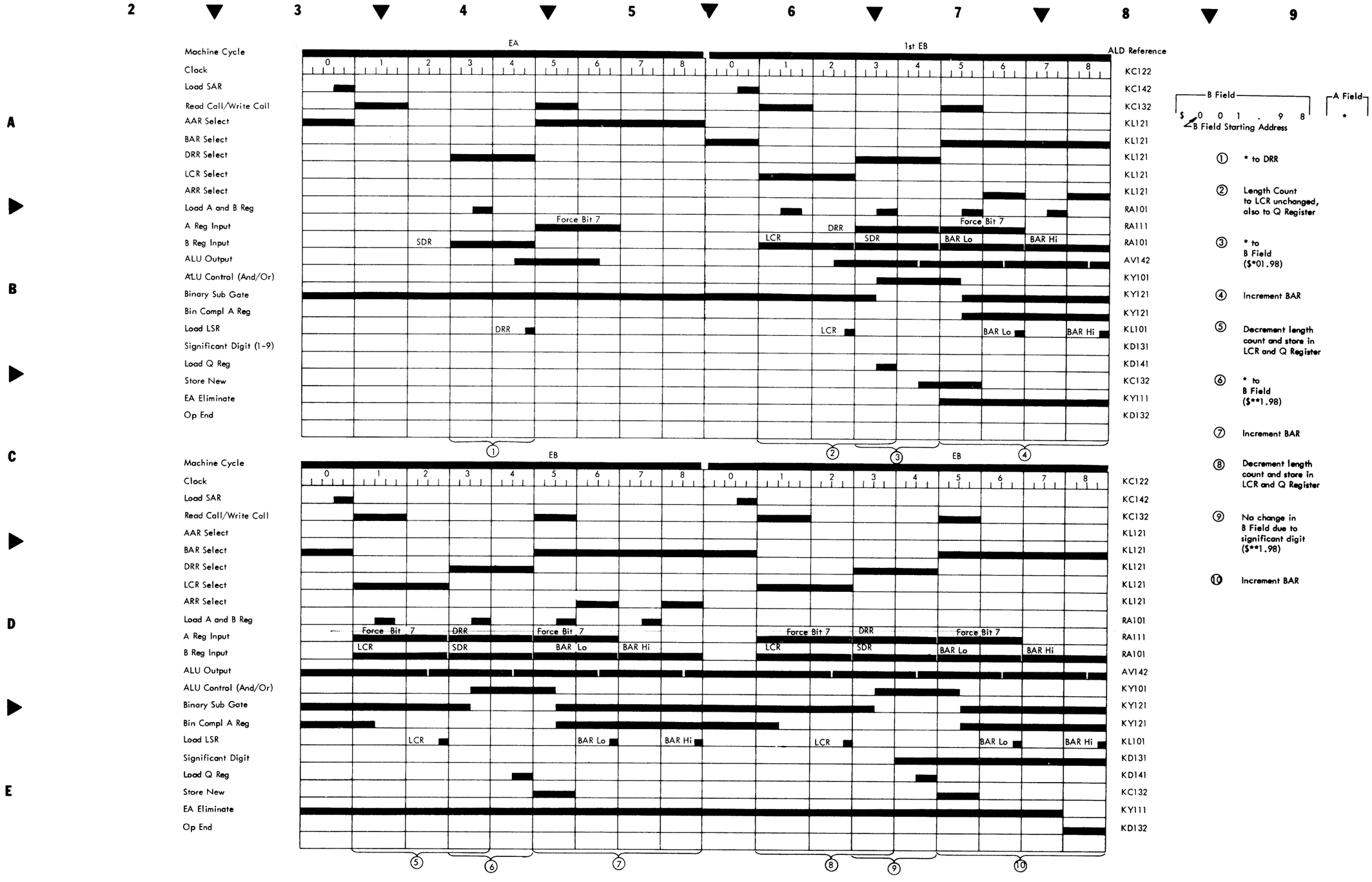


Diagram 5-120. Insert and Test Character (PART 1 of 3)

2 3 4 5 6 7 8 9

A B C D E

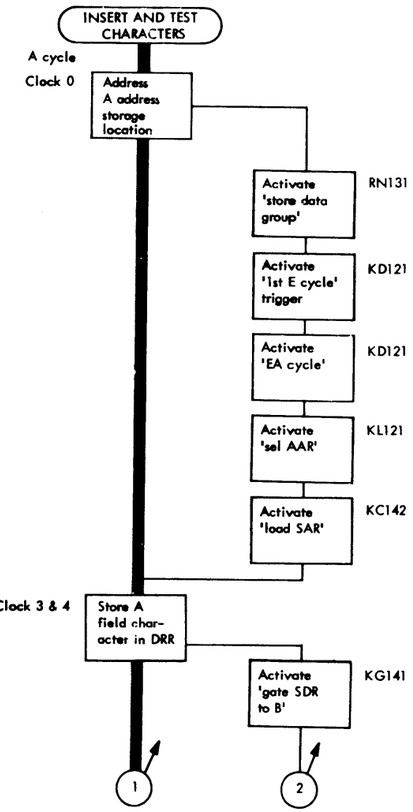
Objectives:

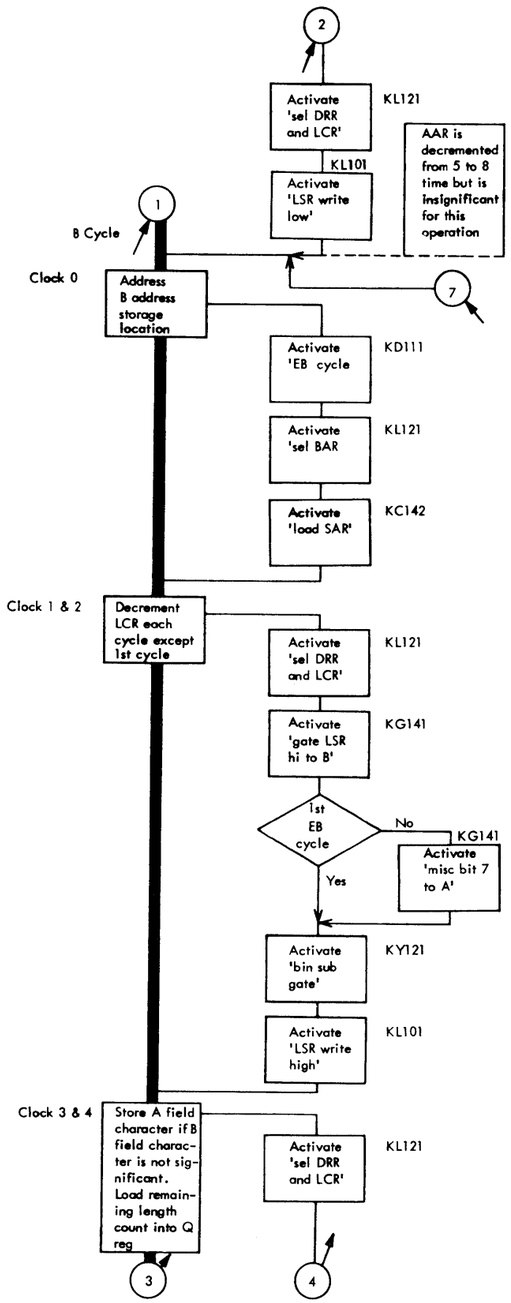
	bits 0 1 2 3 4 5 6 7
Insert and Test Character — Op Code	X X X X 1 0 1 1

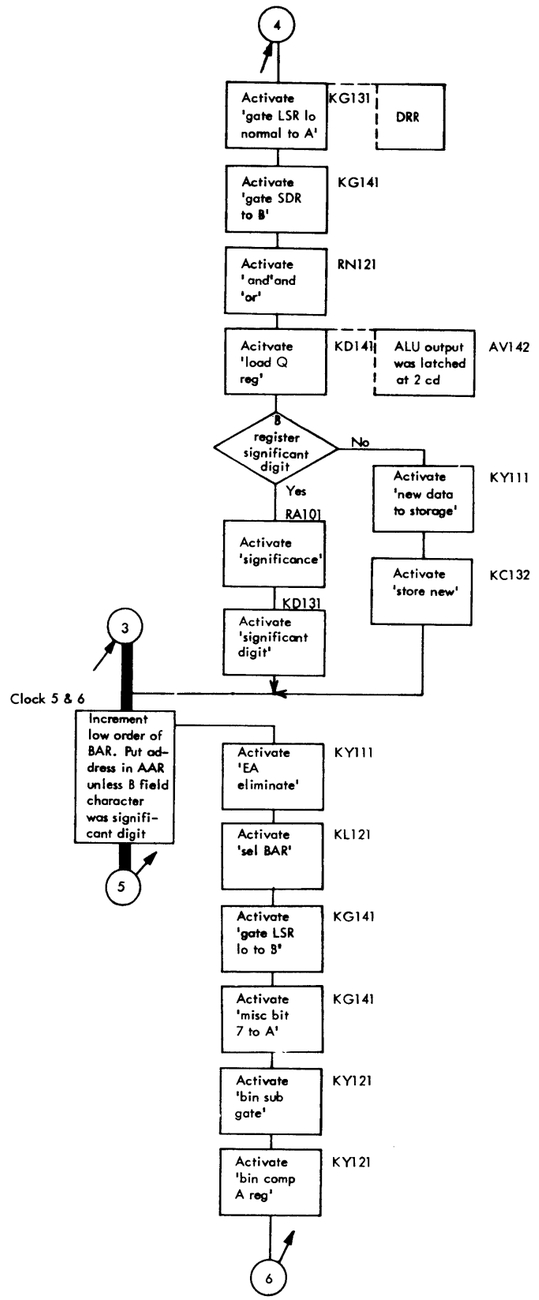
- Replace all characters to left of first significant digit in B field with A field character
- Only numeric characters 1 to 9 are considered significant digits
- Length of B field is Q code + 1
- A field is only 1 character in length

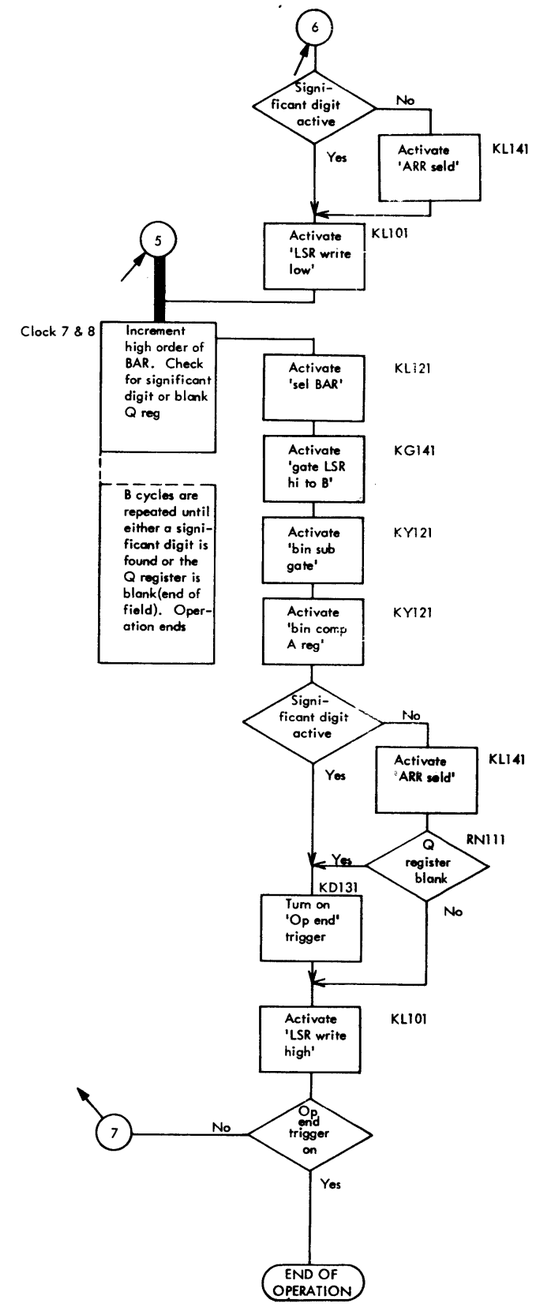
EXAMPLE:

Edited field before operation 0,907.15
A field character *
Edited field after operation **907.15 (blank)
B field starting address









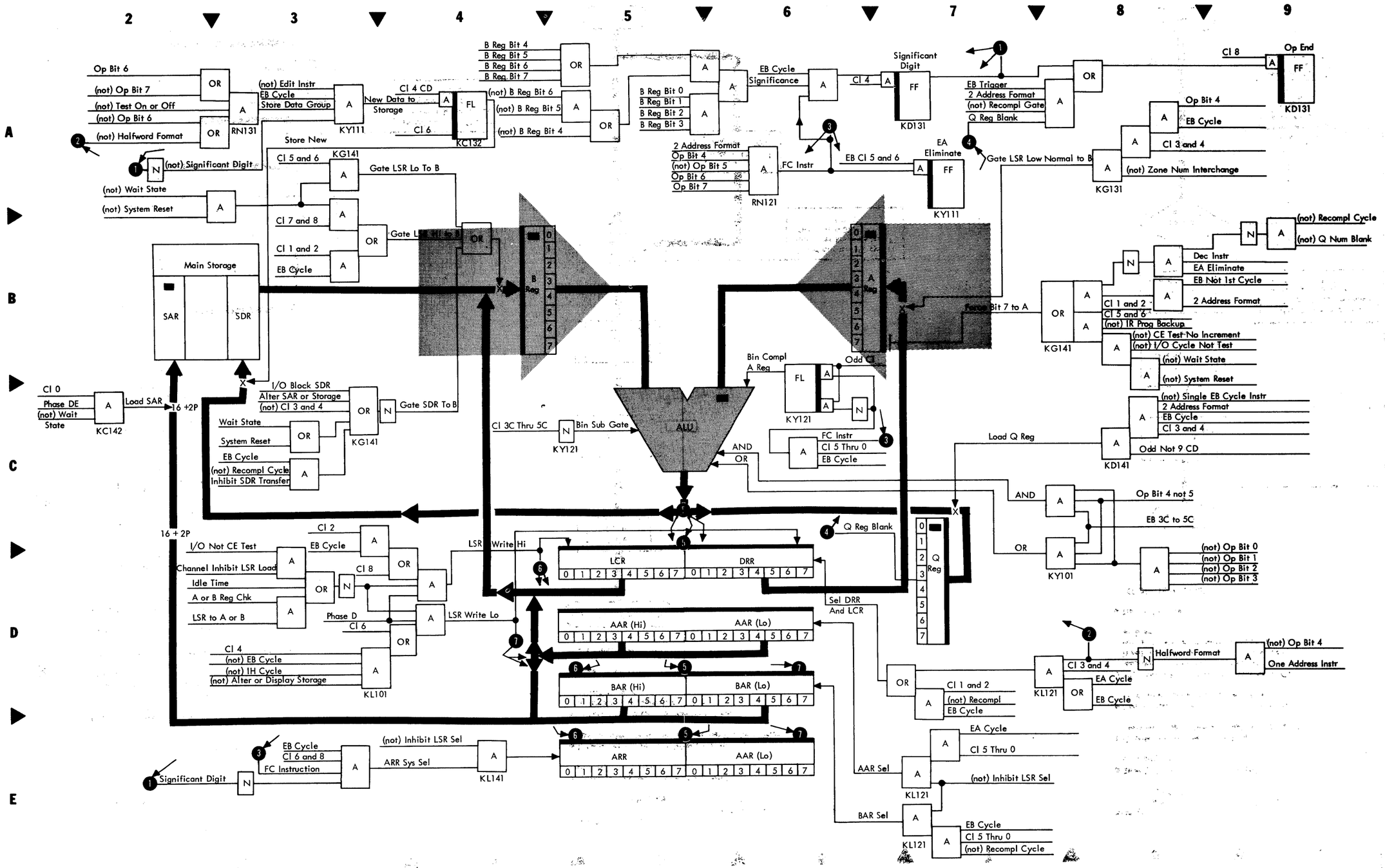


Diagram 5-124. Insert and Test Characters (PART 3 of 3)

Diagram 5-130. Branch On Condition

Branch on Condition

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	X	X	0	0	0	0

- Condition register is tested for condition specified in Q code
- Branch to address is placed in ARR
- Bit 6 of Q code is used to specify if the branch is performed on condition true or condition false
- IAR/ARR interchange if tested condition is satisfied
- Take I-H and I-L or I-X cycle

SEE DIAGRAM 5-030 (I-H, I-L)
5-042 (I-X)

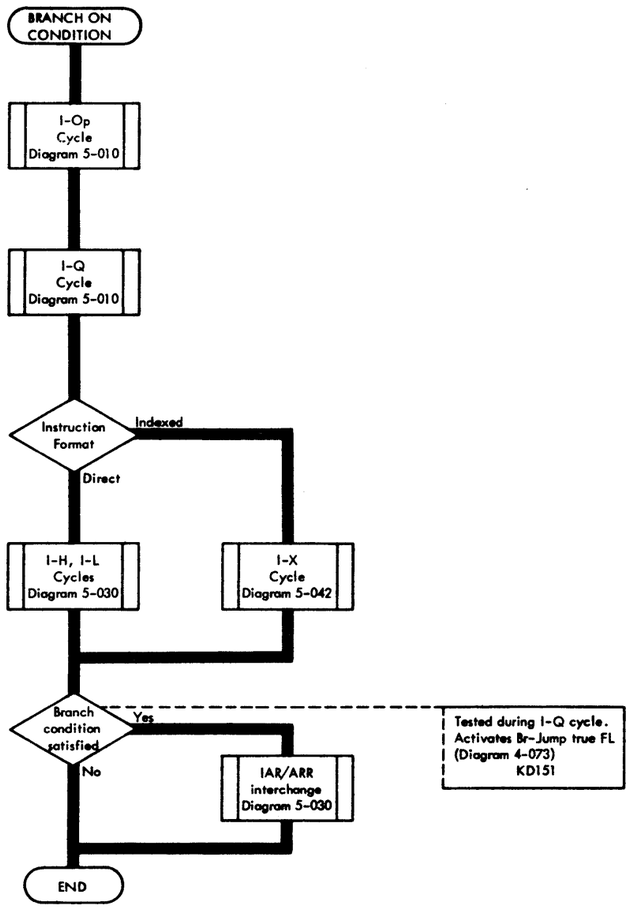


Diagram 5-140. Jump On Condition

Jump On Condition

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	1	0

- Condition register is tested for condition specified in Q code
- If tested condition is satisfied, control code is added to IAR for next sequential instruction
- Q code bit 0 is used to specify if jump is performed on condition true or condition false
- Take I-R cycle

SEE DIAGRAM 5-020

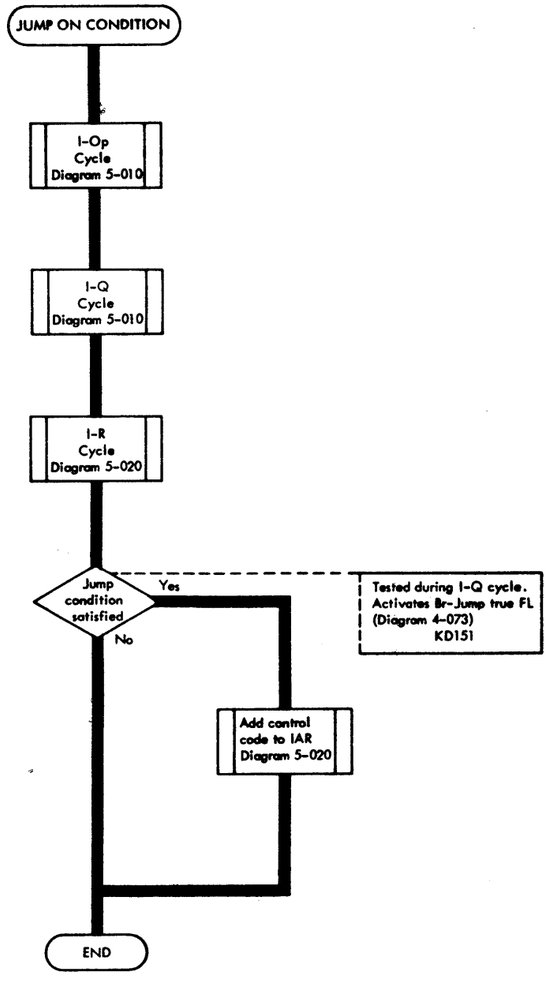


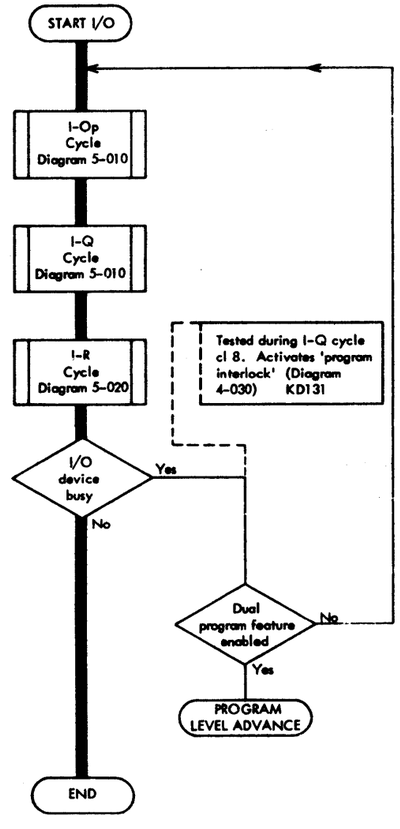
Diagram 5-150. Start I/O (12/69) 5-130 5-140 5-150

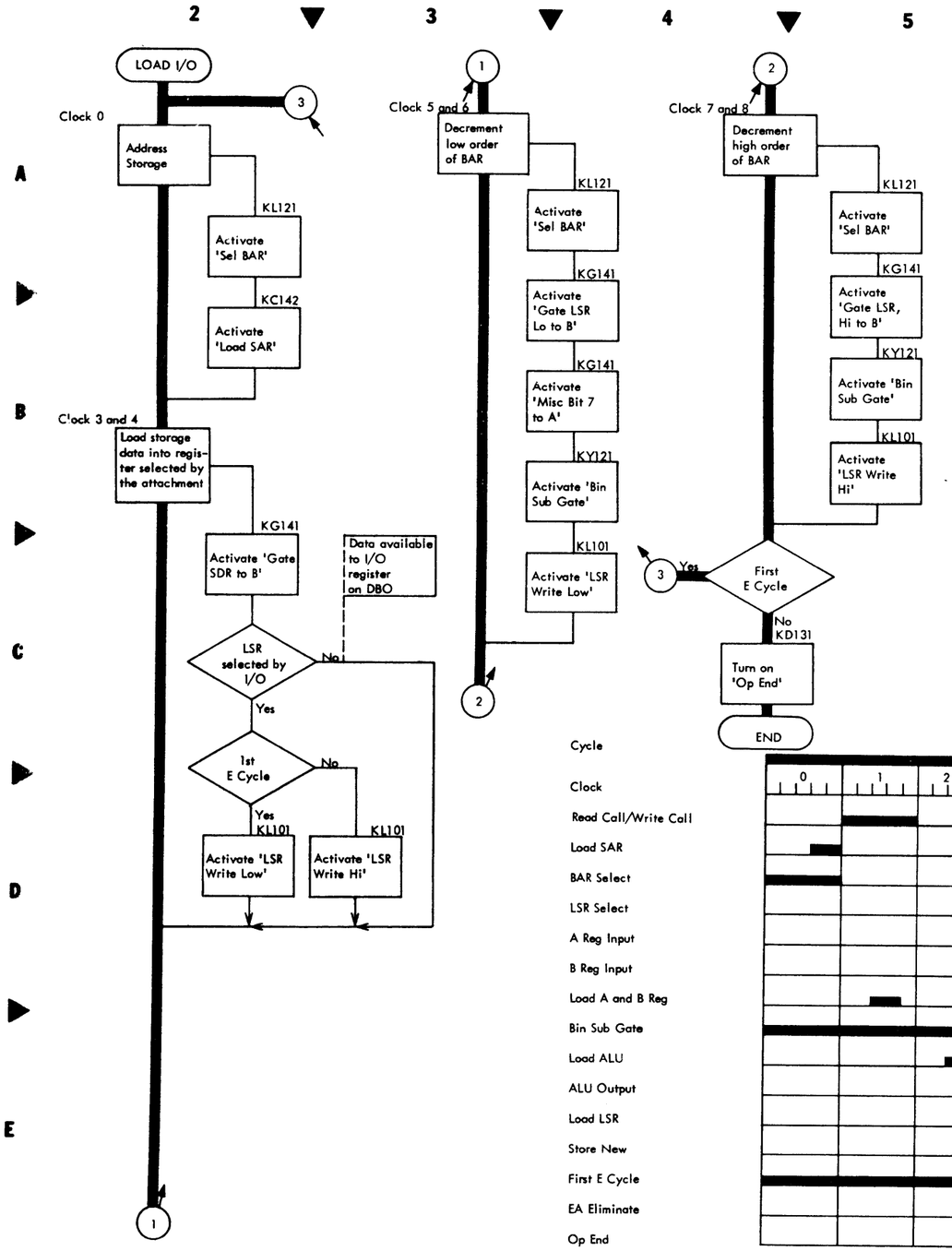
Start I/O

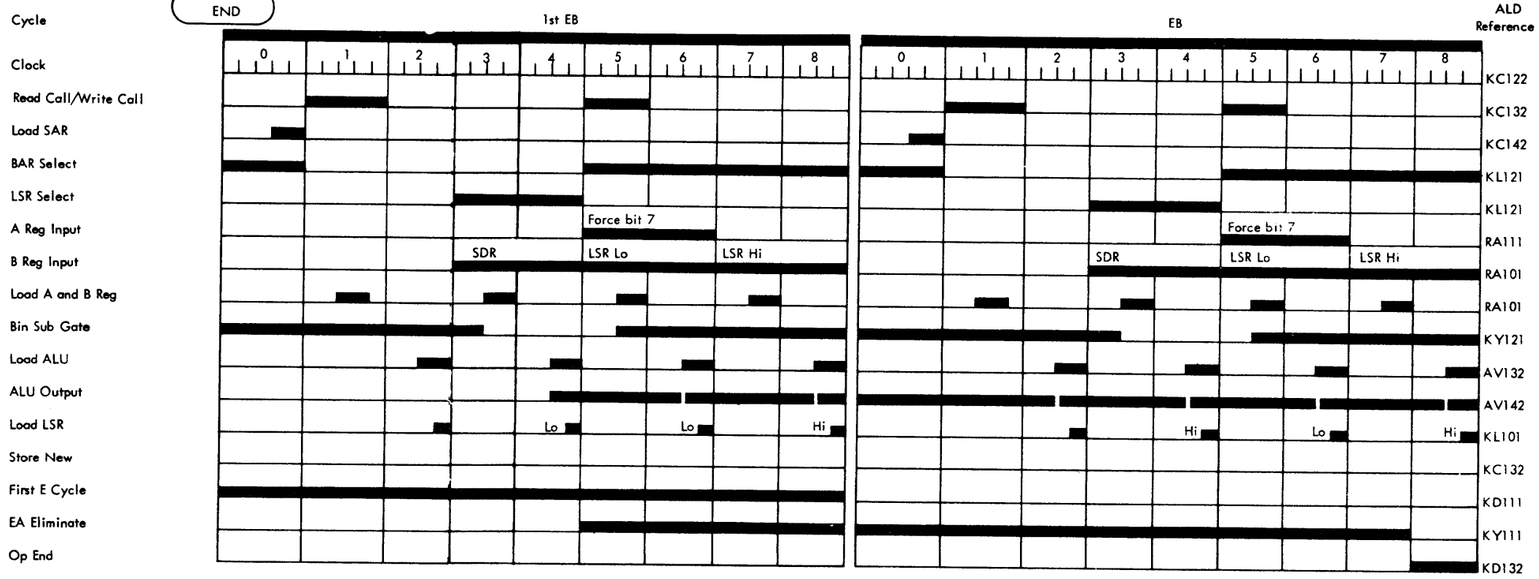
Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	1	1

- Start I/O device or enable/disable dual programming feature
- Q code contains device address and function to be performed (read, punch, etc)
- Control code contains additional instruction for device (space, stacker select, etc)
- I/O device busy causes; (1) program to loop on SIO instruction if dual programming is not installed, or (2) program level advance if dual programming is installed and enabled
- Take I-R Cycle

SEE DIAGRAM 5-020




2
3
4
5
6
7
8
9
A
B
C
D
E
LOAD I/O
Clock 0
Address Storage
KL121
Activate 'Sel BAR'
KC142
Activate 'Load SAR'
Clock 3 and 4
Load storage data into register selected by the attachment
KG141
Activate 'Gate SDR to B'
LSR selected by I/O
No
Yes
Data available to I/O register on DBO
1st E Cycle
No
Yes
KL101
Activate 'LSR Write Low'
KL101
Activate 'LSR Write Hi'
1
Clock 5 and 6
Decrement low order of BAR
KL121
Activate 'Sel BAR'
KG141
Activate 'Gate LSR Lo to B'
KG141
Activate 'Misc Bit 7 to A'
KY121
Activate 'Bin Sub Gate'
KL101
Activate 'LSR Write Low'
2
Clock 7 and 8
Decrement high order of BAR
KL121
Activate 'Sel BAR'
KG141
Activate 'Gate LSR, Hi to B'
KY121
Activate 'Bin Sub Gate'
KL101
Activate 'LSR Write Hi'
3
Yes
First E Cycle
No
KD131
Turn on 'Op End'
END


Cycle
Clock
Read Call/Write Call
Load SAR
BAR Select
LSR Select
A Reg Input
B Reg Input
Load A and B Reg
Bin Sub Gate
Load ALU
ALU Output
Load LSR
Store New
First E Cycle
EA Eliminate
Op End
1st EB
EB
0
1
2
3
4
5
6
7
8
Force bit 7
SDR
LSR Lo
LSR Hi
Lo
Hi
ALD Reference
KC122
KC132
KC142
KL121
KL121
RA111
RA101
RA101
KY121
AV132
AV142
KL101
KC132
KD111
KY111
KD132

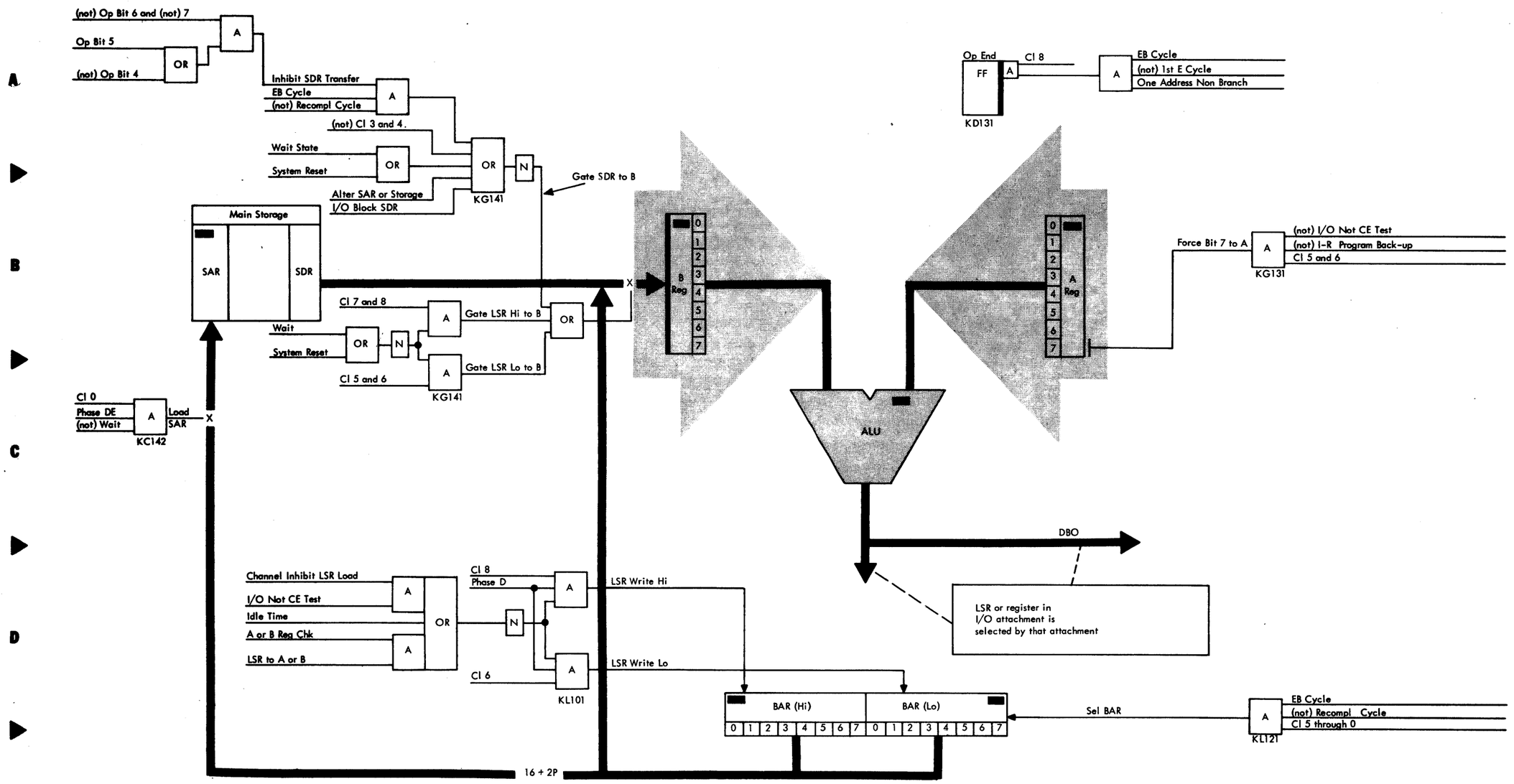
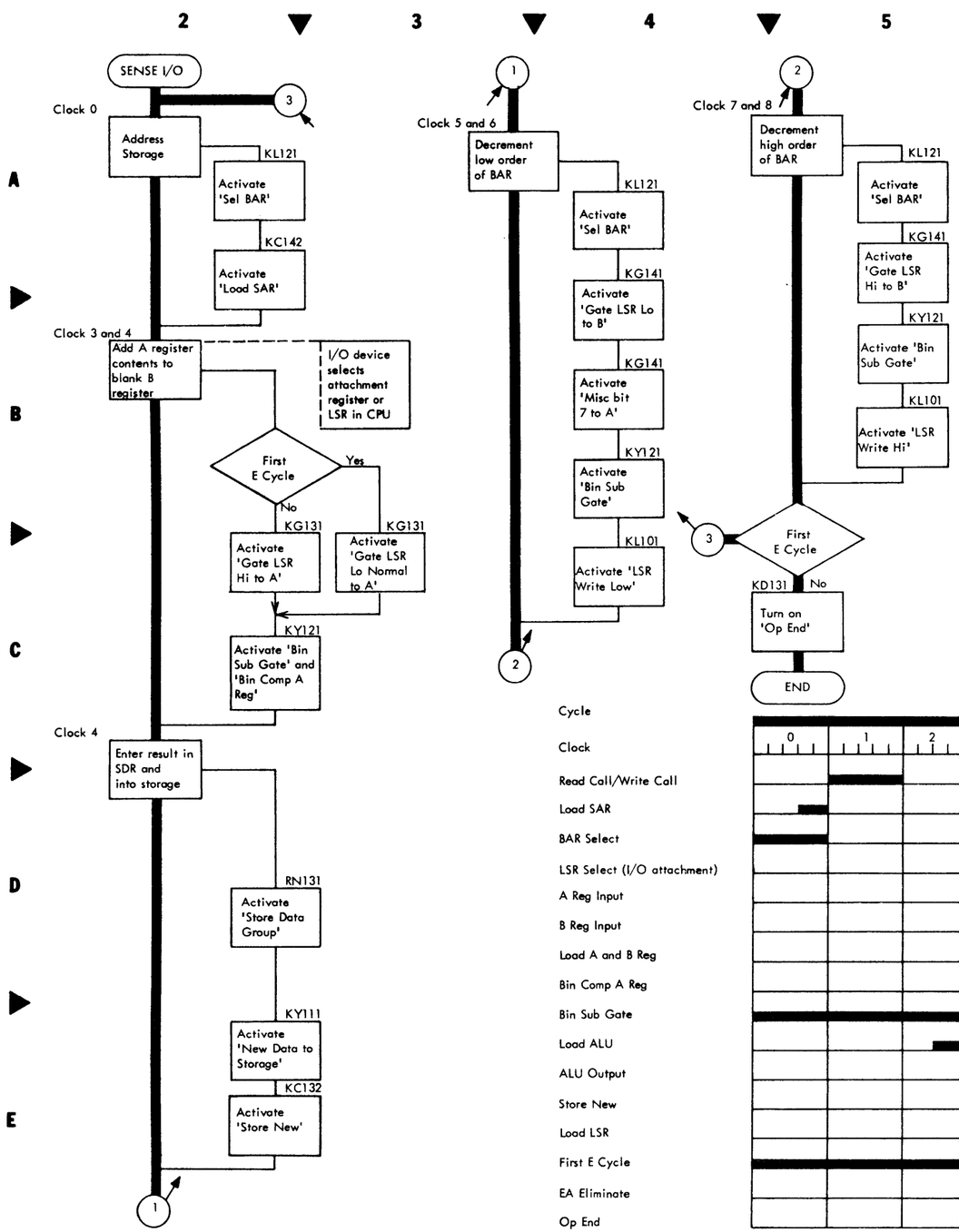


Diagram 5-162. Load I/O (Part 2 of 2)

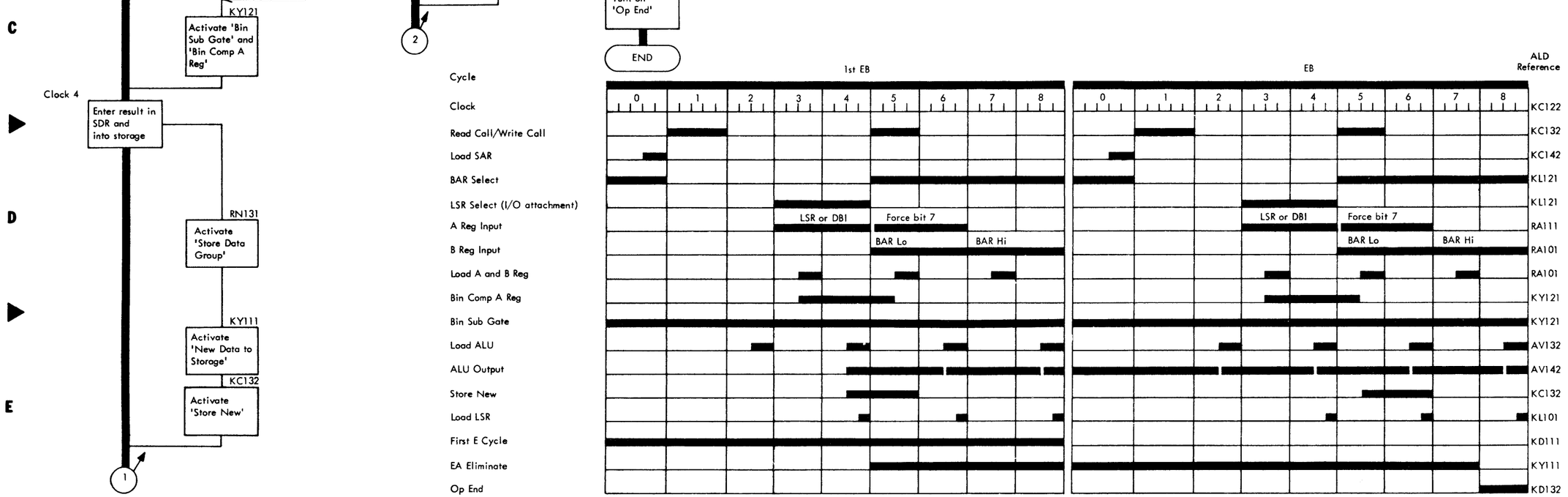


Sense I/O

Bits	0	1	2	3	4	5	6	7
Op Code	0	0	X	X	0	0	0	0

Objective:

- Move two bytes from register selected by I/O attachment to storage



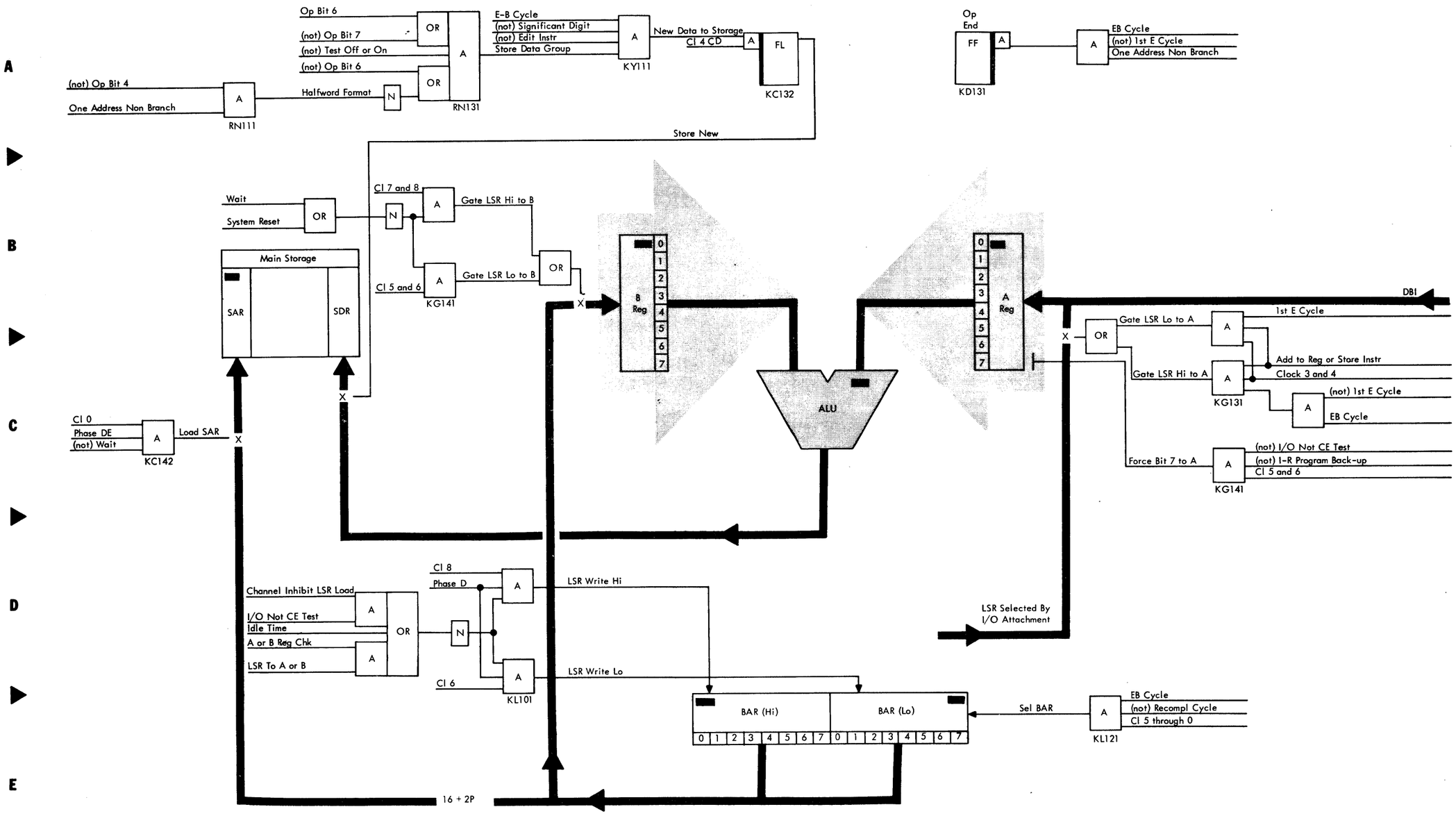


Diagram 5-172. Sense I/O (Part 2 of 2)

2 3 4 5 6 7 8 9

A

B

C

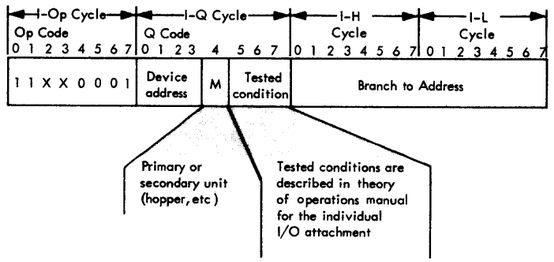
D

E

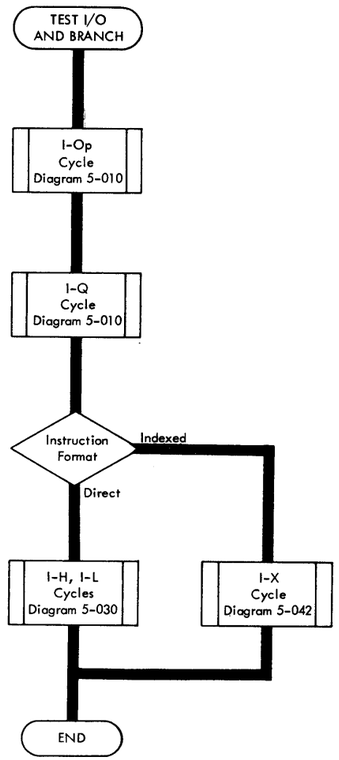
Test I/O and Branch

- Test for I/O condition specified in Q code N field
- Branch to address is loaded into ARR
- IAR/ARR interchange occurs if tested condition is satisfied
- Take I-H and I-L or I-X cycle

SEE DIAGRAM 5-030 (I-H, I-L)
5-042 (I-X)



Line Activated by Any Device	Significance
'I/O Condition B' only	Correct address, valid N code, condition for branching not met--proceed with next sequential instruction
'I/O Condition A' only	Correct address, valid N code, condition for branching met--branch to new address
Both lines	Incorrect parity--causes processor check and DBO parity check
Neither line	Invalid address or N code --causes processor check and invalid device address



Load Address

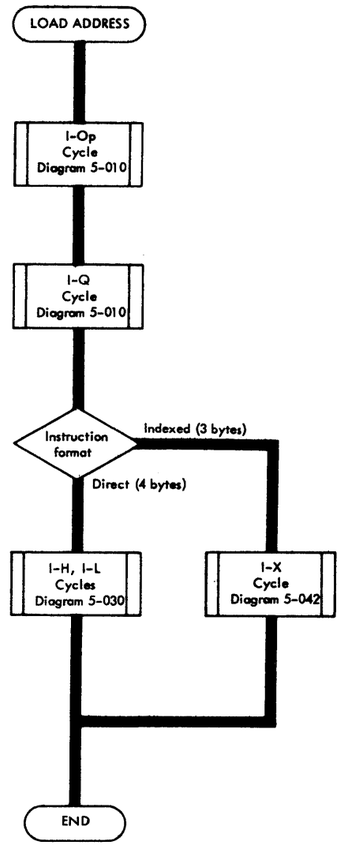
Bits	0	1	2	3	4	5	6	7
Op Code	1	1	X	X	0	0	1	0

- Load one or two bytes from storage into one of the two index registers
- If instruction format is four bytes, load two byte address into index register selected by Q code bits 6 and 7
- If instruction format is three bytes, add last instruction byte to index register selected by Op Code bits 2 and 3. Then load result into index register selected by Q code bits 6 and 7
- Take I-H and I-L cycles (four byte format)

SEE DIAGRAM 5-030

- Take I-X cycle (three byte format)

SEE DIAGRAM 5-042



2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A

Advance Program Level

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	0	1

Basic Machine

- Test for I/O condition specified in Q code N field
- Loop on APL instruction until condition tested for no longer exists
- Q code N field of all zeros causes automatic advance to next sequential instruction.

▶

- Take I-R cycle SEE DIAGRAM 5-020

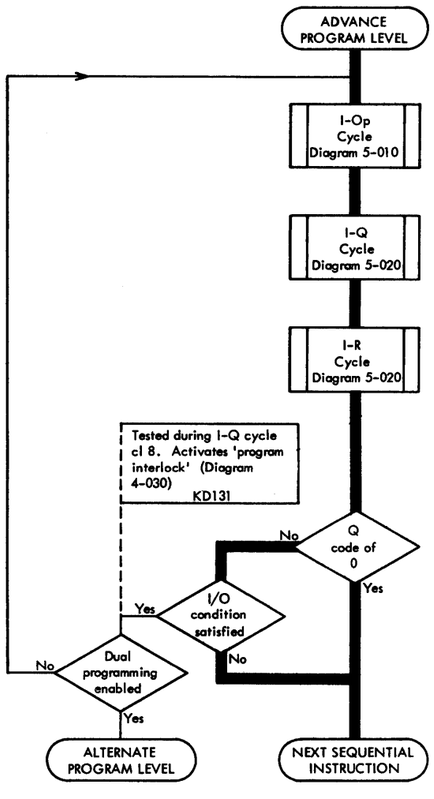
Dual Program Feature Enabled

- Test for I/O condition specified in Q code N field

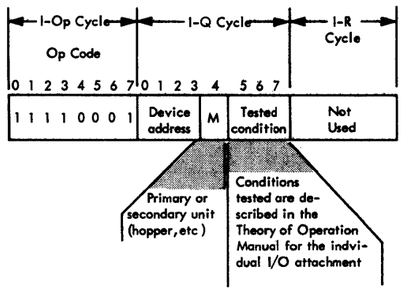
B

- Program level advance if condition is satisfied
- Program status register (PSR) contains recall information for returning to original program
- Take I-R cycle SEE DIAGRAM 5-020

▶



C ▶ D ▶ E



Line Activated by Any Device	Significance
'I/O Condition B' only	Correct address, valid N code, device not busy and doesn't need attention --instruction accepted
'I/O Condition A' only	Correct address, valid N code, device busy or needs attention--instruction rejected
Both lines	Incorrect parity--causes processor check and DBO parity check
Neither line	Invalid address or N code --causes processor check and invalid device address

Diagram 5-200. Advance Program Level

Halt Program Level

Bits	0	1	2	3	4	5	6	7
Op Code	1	1	1	1	0	0	0	0

Basic Machine

- Prevents execution of next sequential instruction
- Loops on instruction until system start key is pressed
- Instruction bytes two and three are displayed on console

Dual Program Feature Enabled

- Prevents execution of next sequential instruction
- Branches to alternate program level if DPF is enabled
- Program returns to original level if appropriate halt reset key is pressed
- Take I-R cycle SEE DIAGRAM 5-020

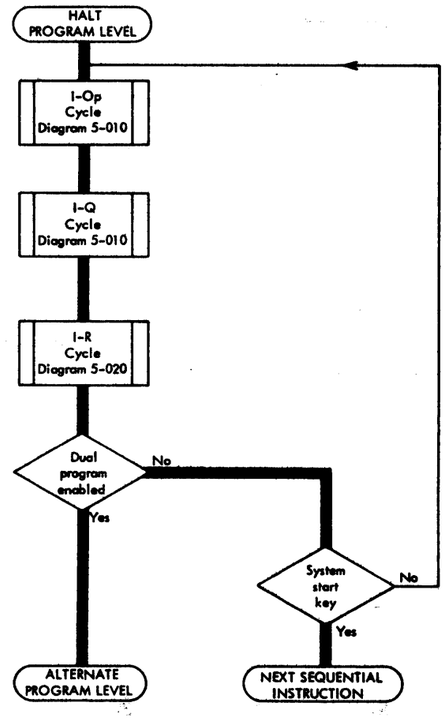
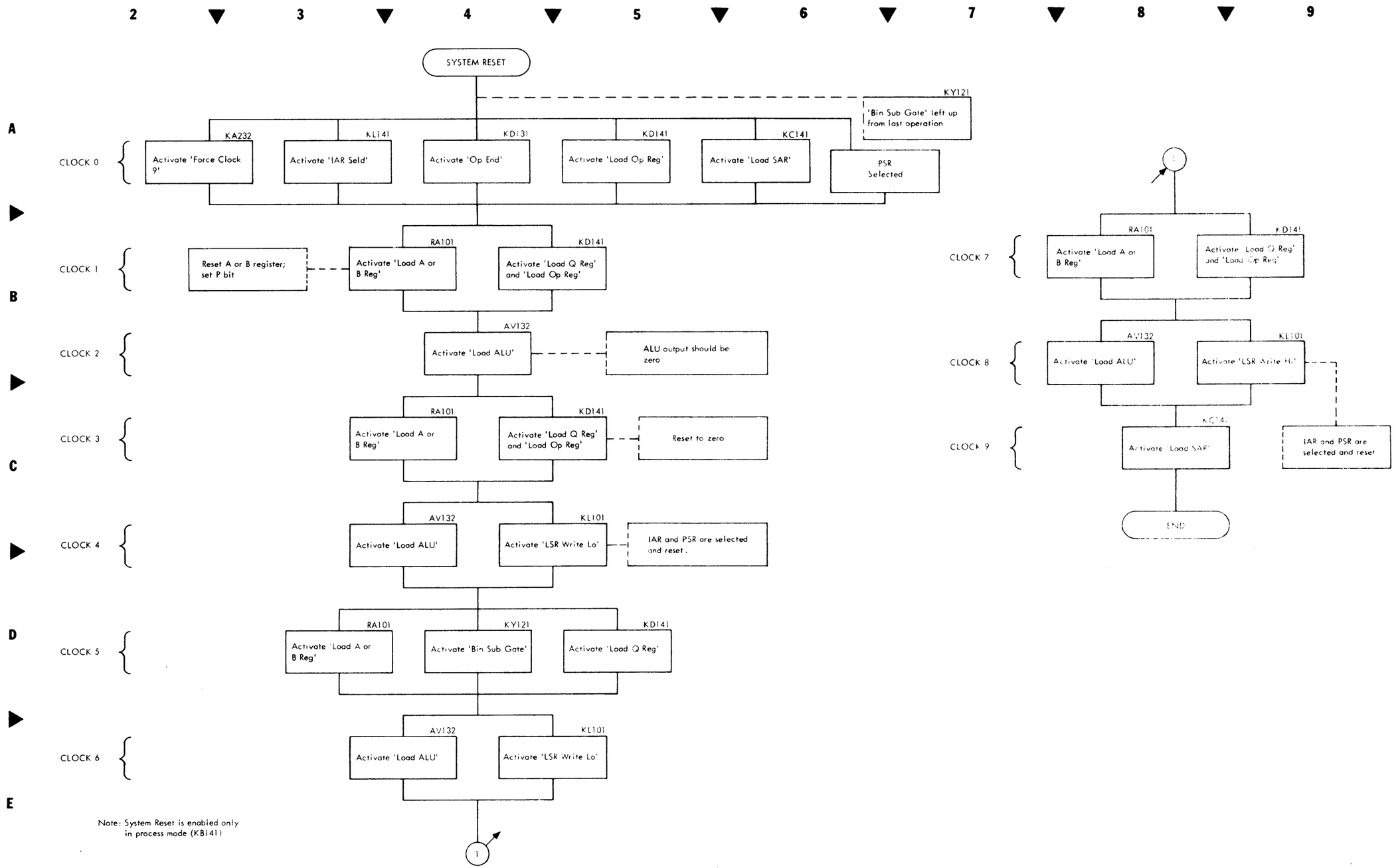
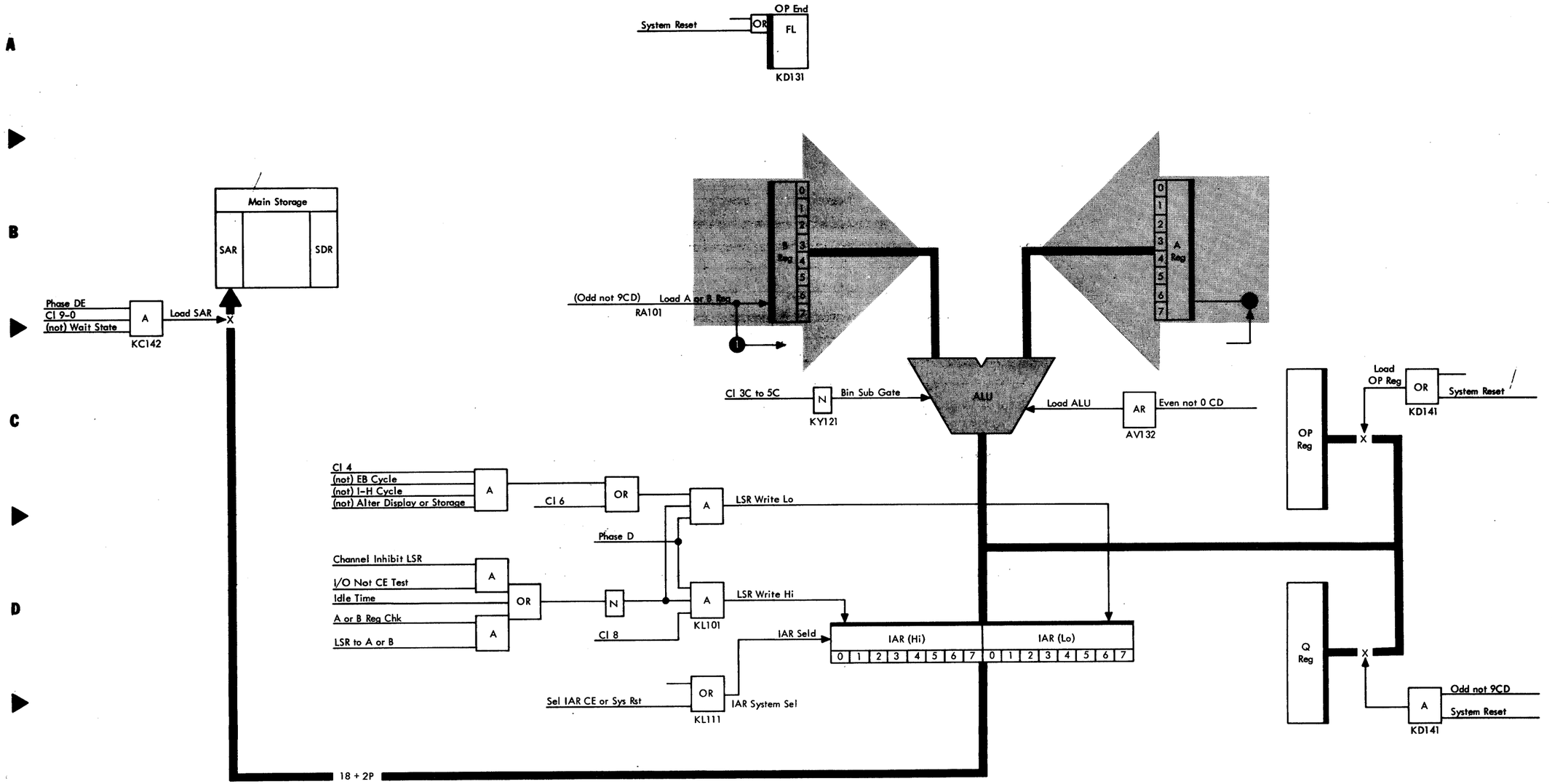


Diagram 5-210. Halt Program Level

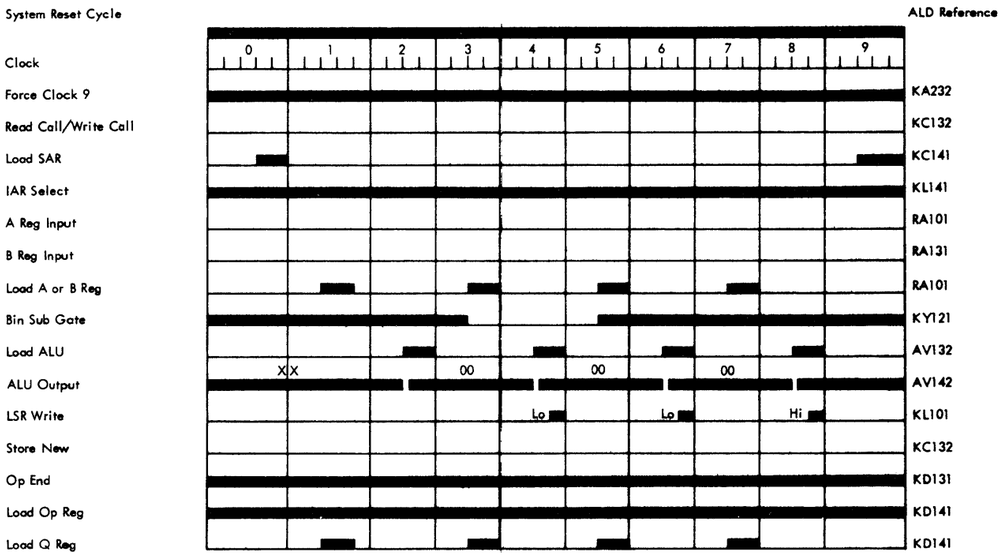


Note: System Reset is enabled only in process mode (KB141)



Note: 1. Refer to Diagram 4-020 for clock circuits
2. Refer to Diagram 4-030 for cycle controls

Diagram 5-222. System Reset (Part 2 of 3)



Note: Parity checking is disabled during System Reset

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

Initial Program Load (IPL)

Objectives

5410

- Program Load Key initiates system reset cycle
- Clock starts and continues to run
- System reset cycle causes:

  (1) DBO 7 (MFCU)
  DBO 5 (File

  (2) All zeros written into IAR and MRDAR (MFCU) or DFDR (File)

- 'I/O Condition B' resets IPL latch at end of data transfer and activates process run. First I-Op cycle addresses storage position 0000 (IAR set to all zero)

5424

- DBO bit 7 to MFCU
- Reset MRDAR to 0000
- Set execute primary latch in MFCU
- Set execute read in MFCU
- Set execute feed in MFCU

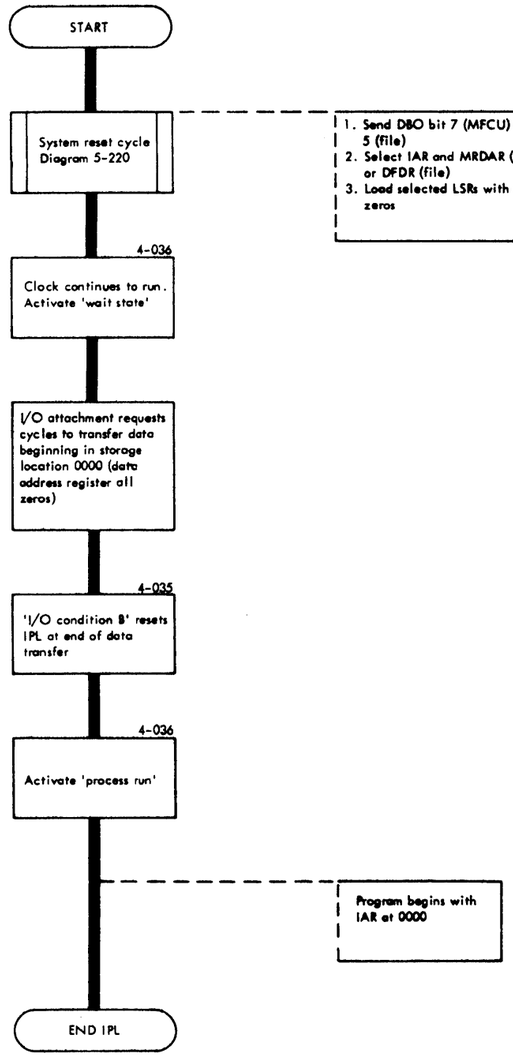


Diagram 5-225. Initial Program Load (IPL)

2 3 4 5 6 7 8 9

A

B

C

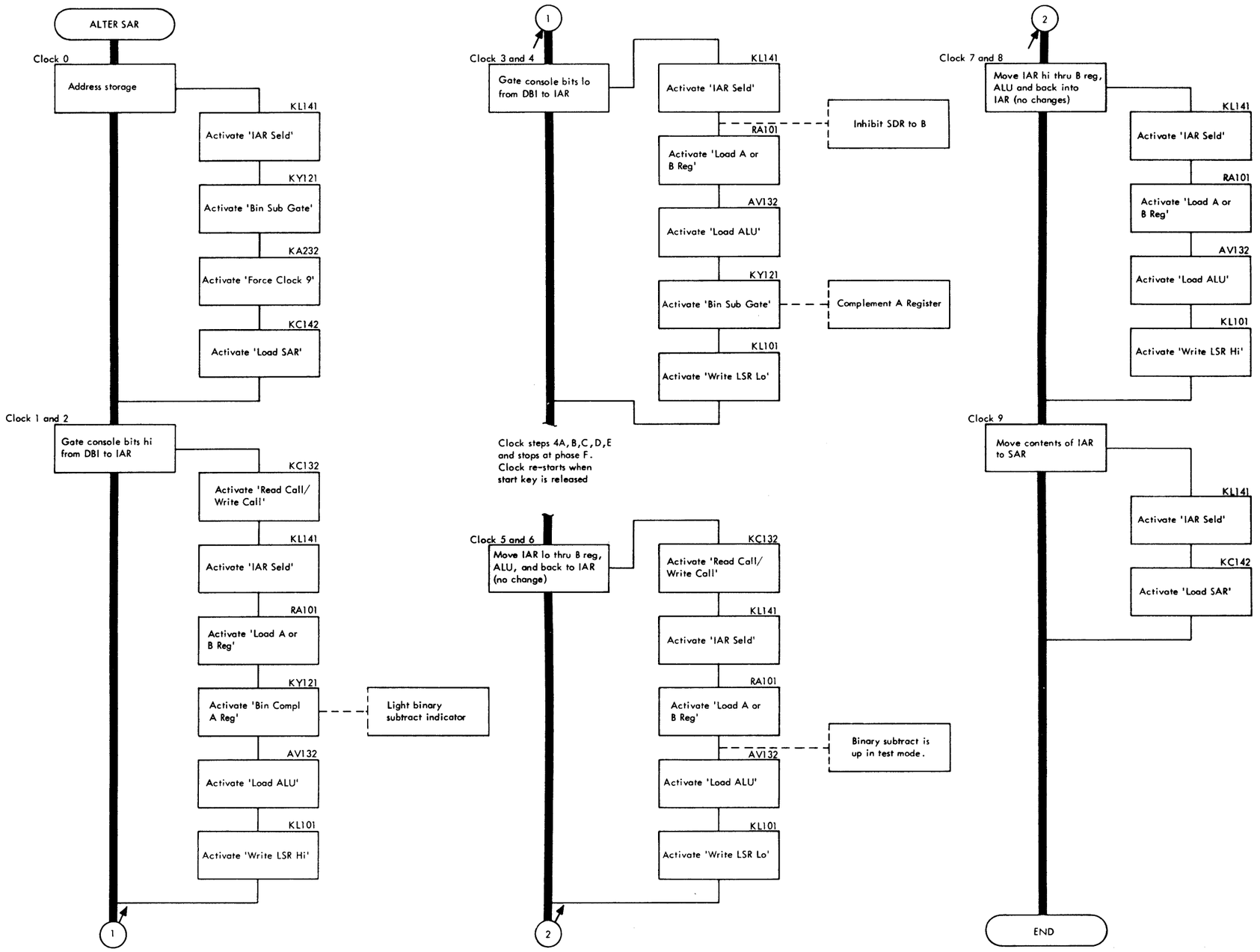
D

E

Alter SAR

Objectives:

- Load contents of four console Address/Data switches into the Instruction Address Register (IAR) by way of Data Bus In, A register and ALU
- Load SAR from the IAR at clock 9 time
- When start key is pressed, the clock runs 0 thru 4. When start key is released, clock runs from 5 thru 9.



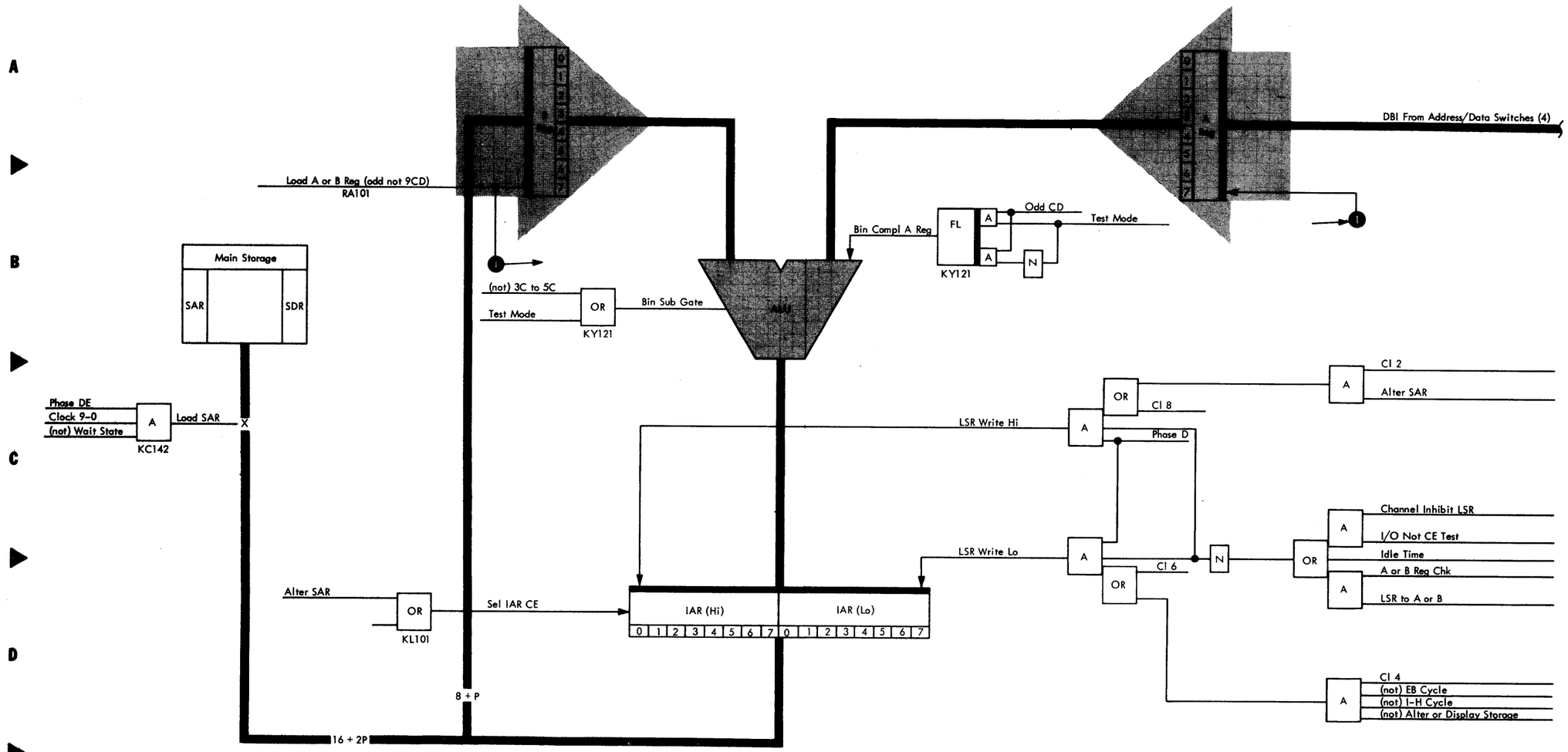


Diagram 5-232. Alter SAR (Part 2 of 3)

2 3 4 5 6 7 8 9

A

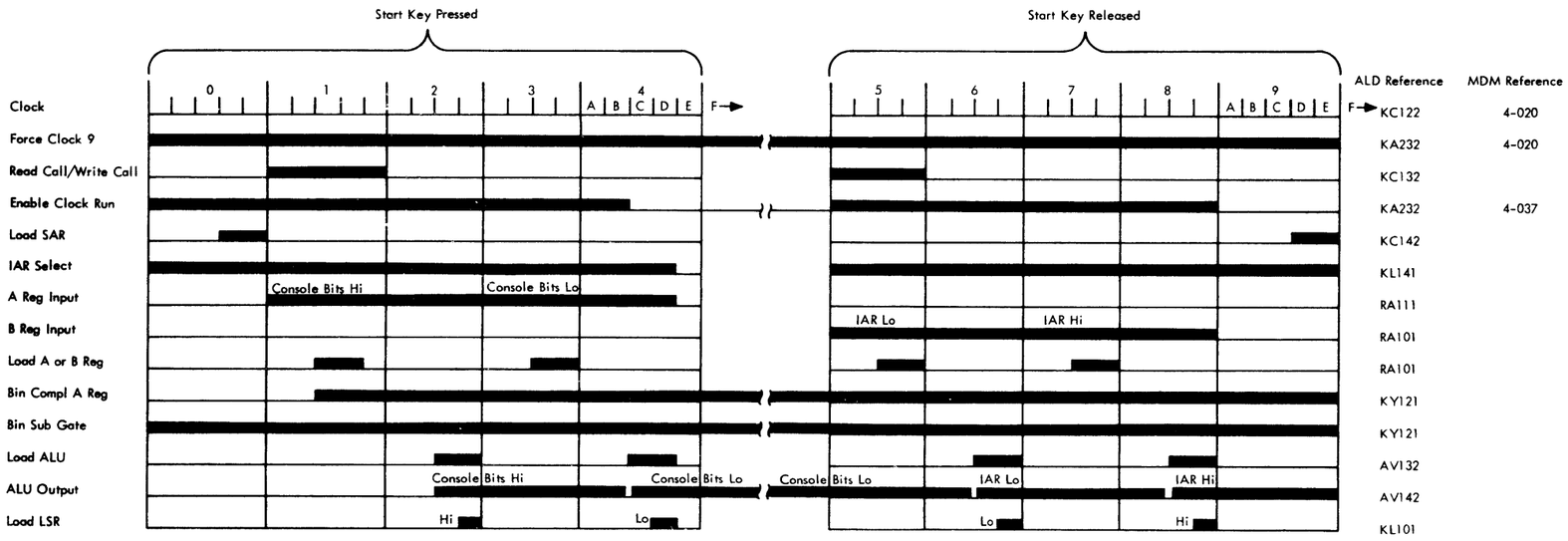
B

C

D

E

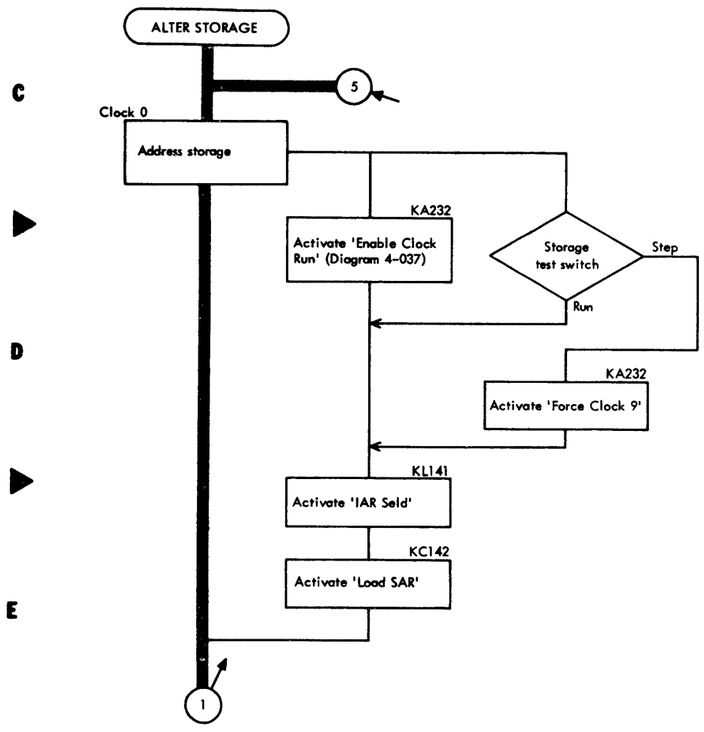
ALTER SAR

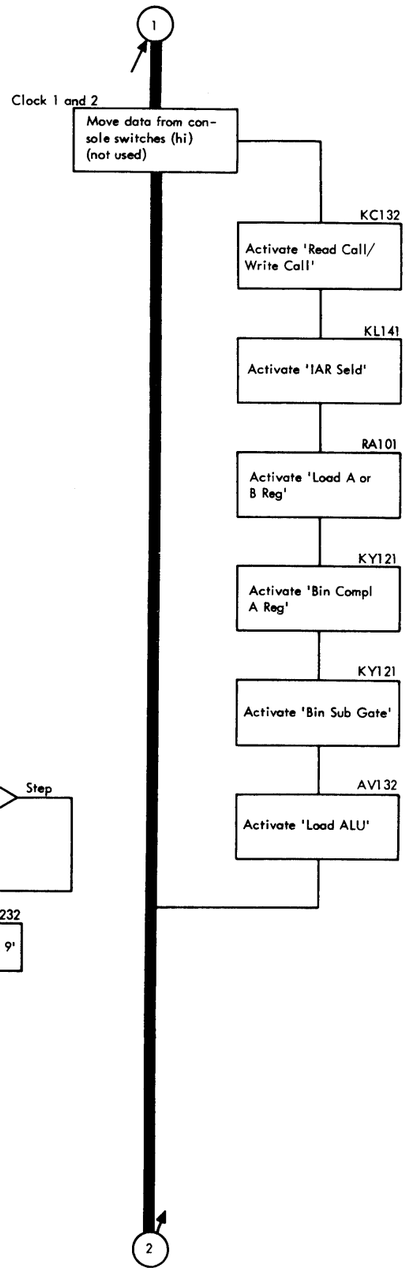


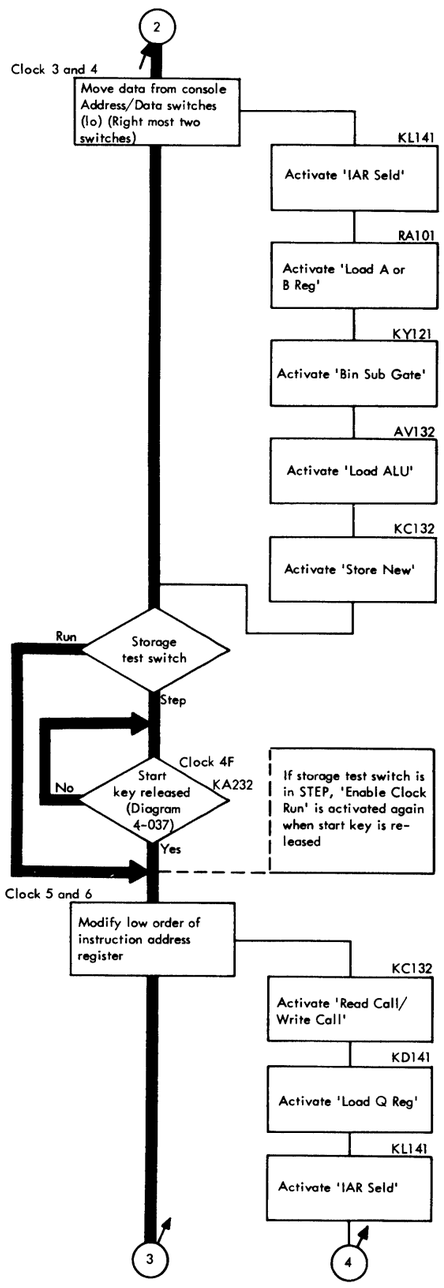
Alter Storage

Objectives:

- Transfer data from right most two console Address/Data switches (one byte) into Q reg and storage location designated by SAR
- With storage test switch in STEP; pressing start key advances clock through 4 time. Releasing start key advances clock through 9 time
- With storage test switch in RUN; clock re-cycles, skipping 9 time, until switch is returned to STEP
- Address Increment switch ON causes IAR to be incremented each CPU cycle
- Address Increment switch OFF causes console data to be transfered into same storage location each cycle







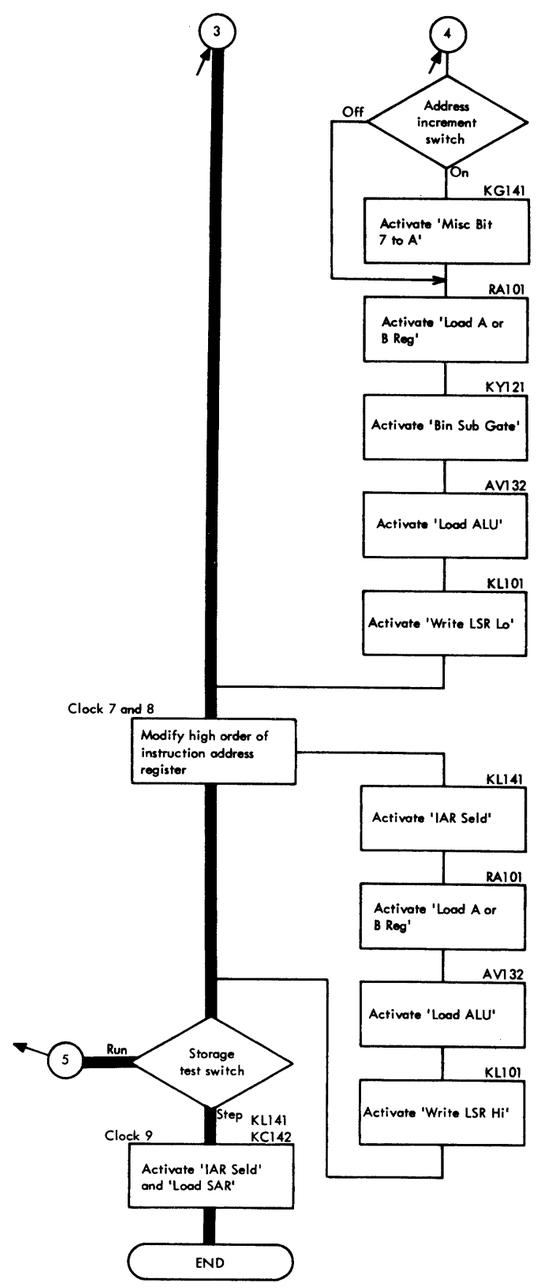
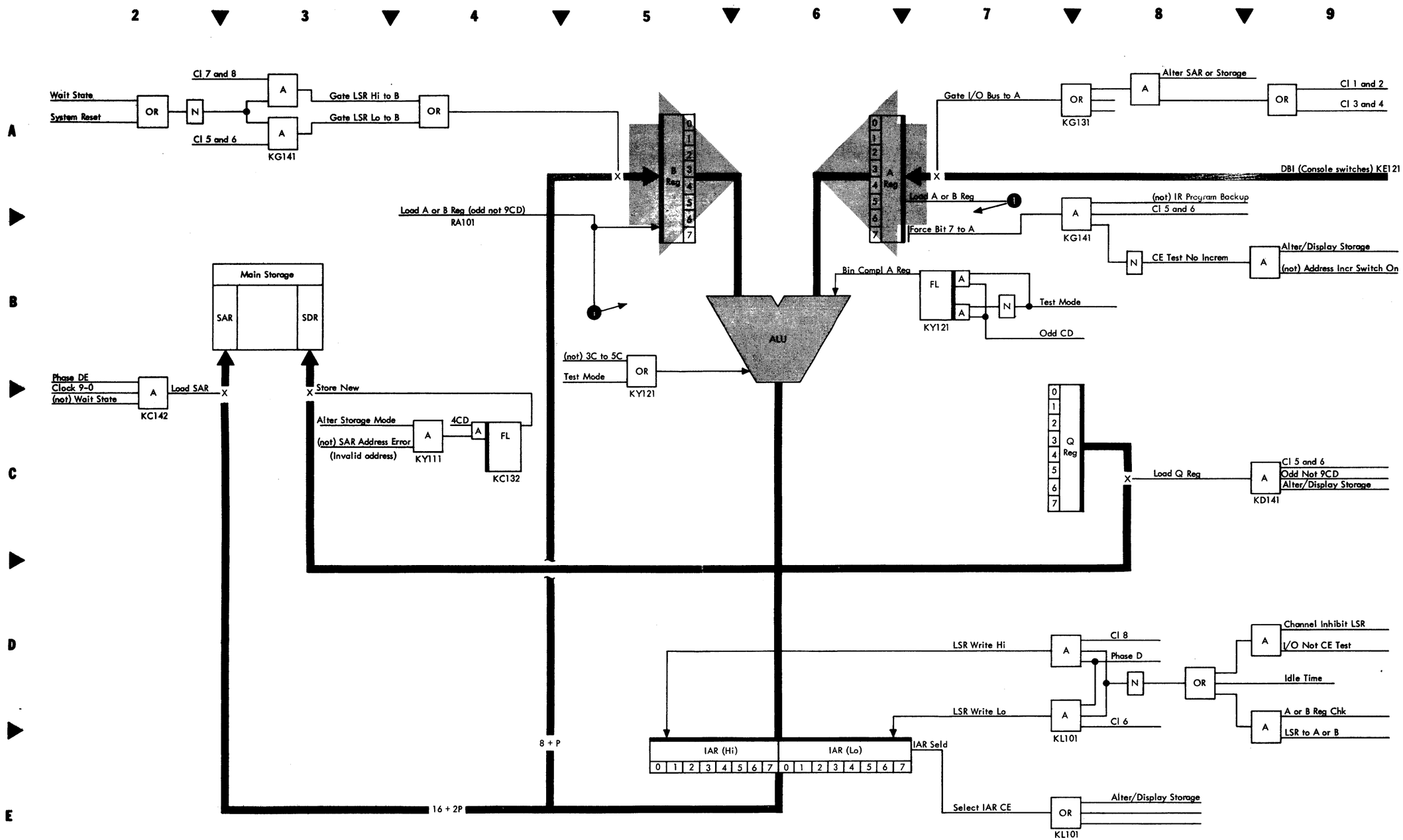
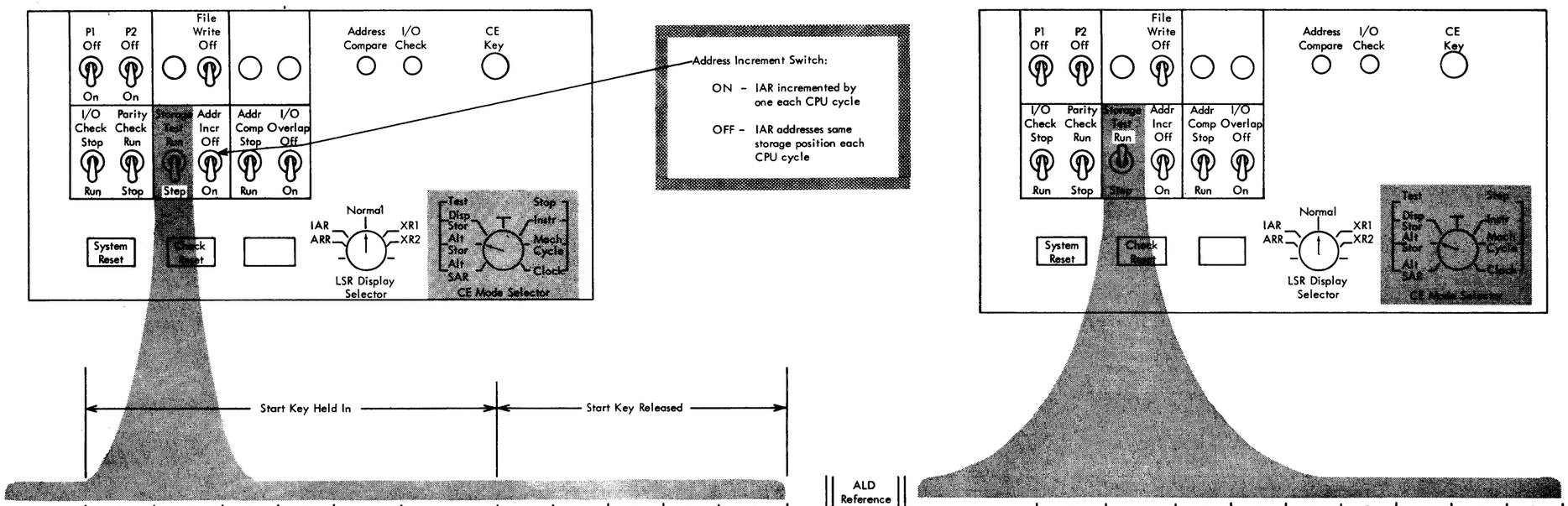


Diagram 5-240. Alter Storage (Part 1 of 3)


2
3
4
5
6
7
8
9
A
B
C
D
E
Wait State
System Reset
OR
N
Cl 7 and 8
Cl 5 and 6
A
KG141
Gate LSR Hi to B
Gate LSR Lo to B
OR
Load A or B Reg (odd not 9CD)
RA101
B Reg
A Reg
Gate I/O Bus to A
OR
KG131
A
Alter SAR or Storage
OR
Cl 1 and 2
Cl 3 and 4
DBI (Console switches) KE121
Load A or B Reg
Force Bit 7 to A
A
KG141
(not) IR Program Backup
Cl 5 and 6
N
CE Test No Increm
A
Alter/Display Storage
(not) Address Incr Switch On
Bin Compl A Reg
FL
A
A
N
Test Mode
Odd CD
KY121
ALU
Main Storage
SAR
SDR
(not) 3C to 5C
Test Mode
OR
KY121
Phase DE
Clock 9-0
(not) Wait State
A
KC142
Load SAR
X
Store New
Alter Storage Mode
(not) SAR Address Error
(Invalid address)
A
KY111
4CD
A
FL
KC132
Q Reg
Load Q Reg
A
Cl 5 and 6
Odd Not 9CD
Alter/Display Storage
KD141
8 + P
16 + 2P
IAR (Hi)
IAR (Lo)
IAR Seld
LSR Write Hi
LSR Write Lo
A
A
KL101
Cl 8
Phase D
Cl 6
N
OR
A
Channel Inhibit LSR
I/O Not CE Test
Idle Time
A
A or B Reg Chk
LSR to A or B
Select IAR CE
OR
KL101
Alter/Display Storage

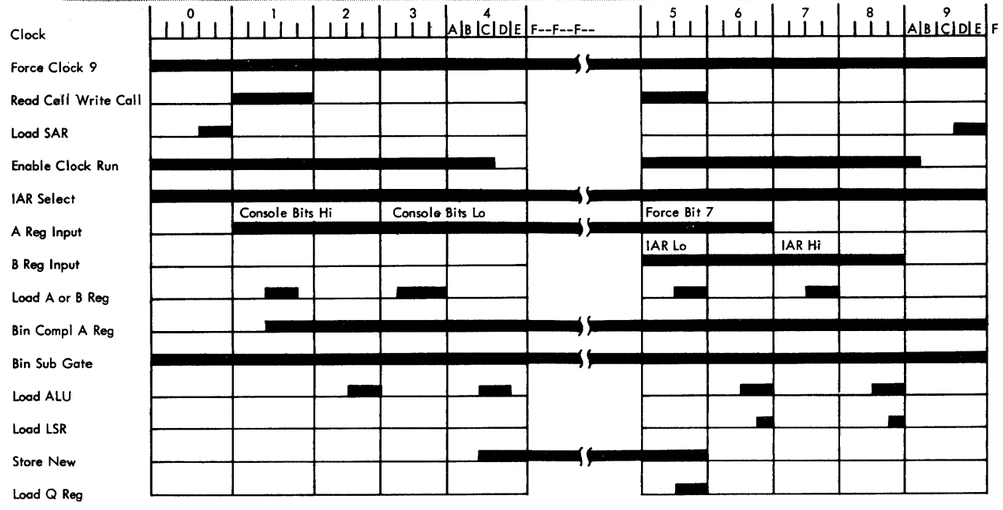
2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A ▶ B ▶



C ▶

D ▶ E



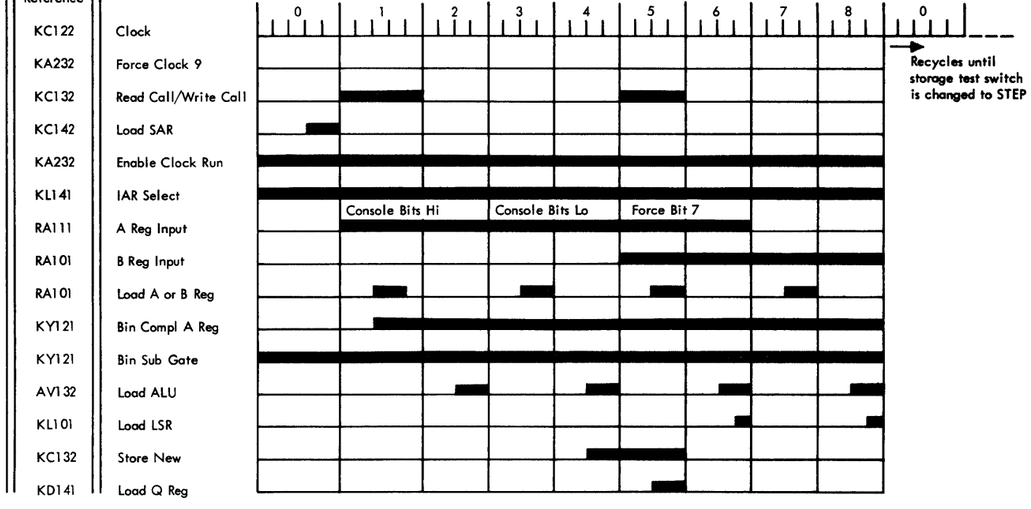


Diagram 5-244. Alter Storage (Part 3 of 3)

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A

B

C

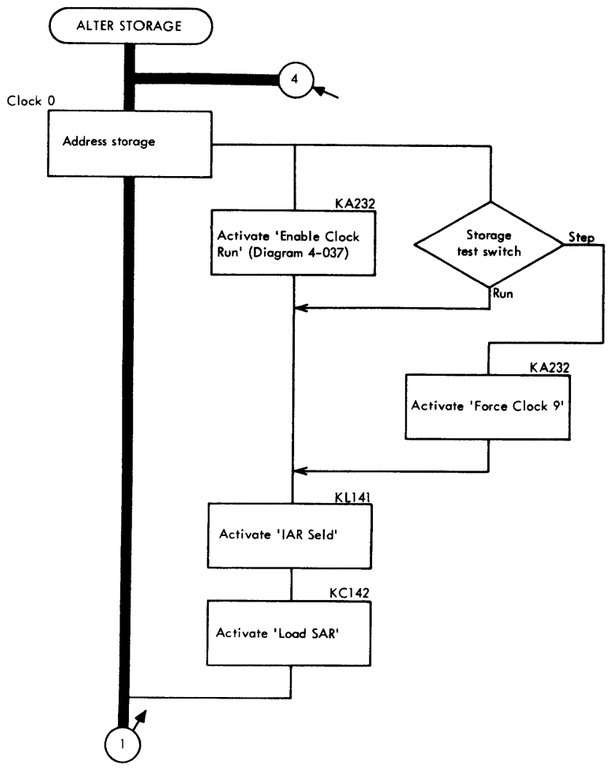
D

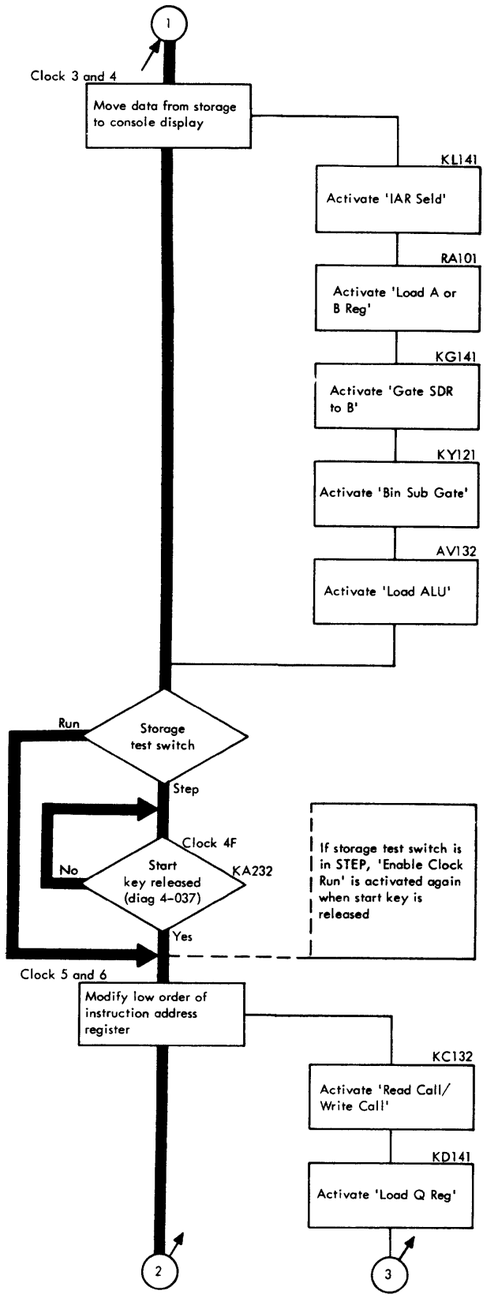
E

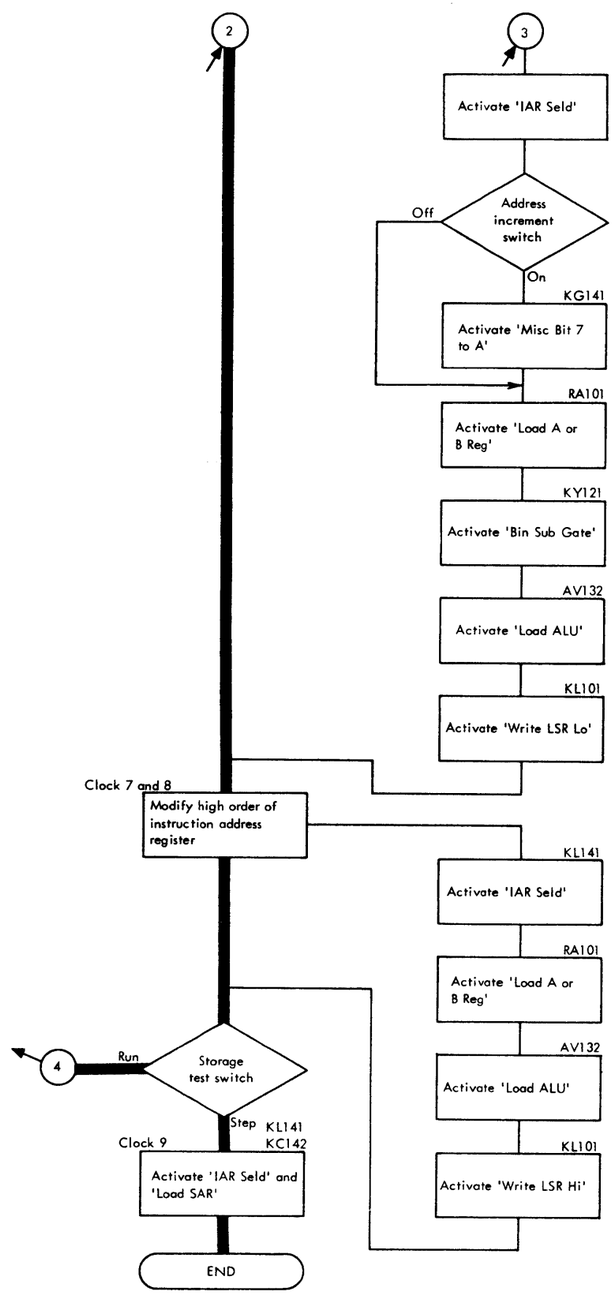
Display Storage

Objectives

- Transfer data from storage position addressed by SAR into Q register and display in console lights when drum switch is in position 5
- With storage test switch in STEP; pressing start key advances clock through 4 time. Releasing start key advances clock through 9 time
- With storage test switch in RUN; clock re-cycles, skipping 9 time, until switch is returned to STEP
- Address Increment switch ON causes IAR to be incremented each CPU cycle
- Address Increment switch OFF causes console data to be transfered into same storage location each cycle







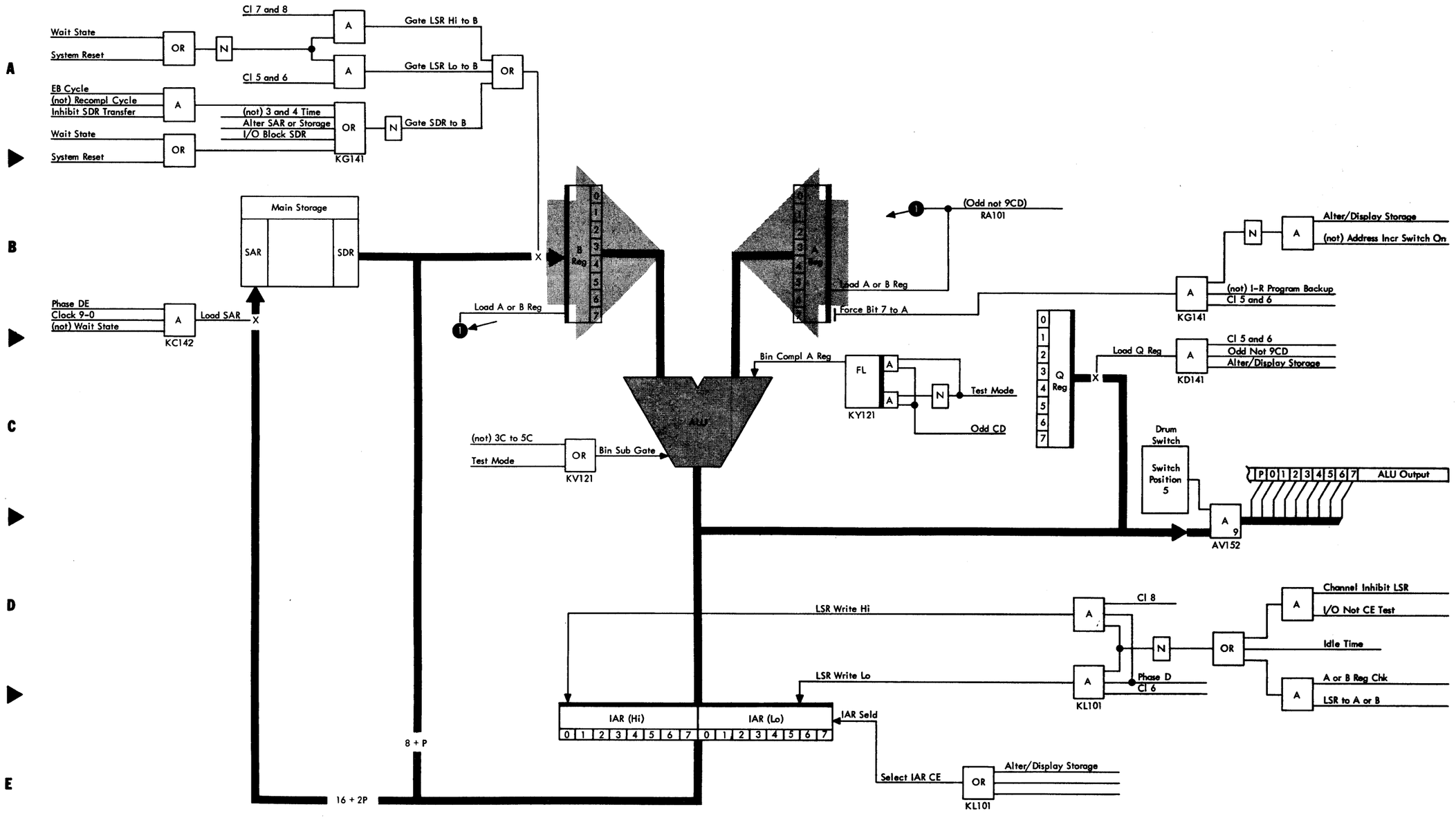
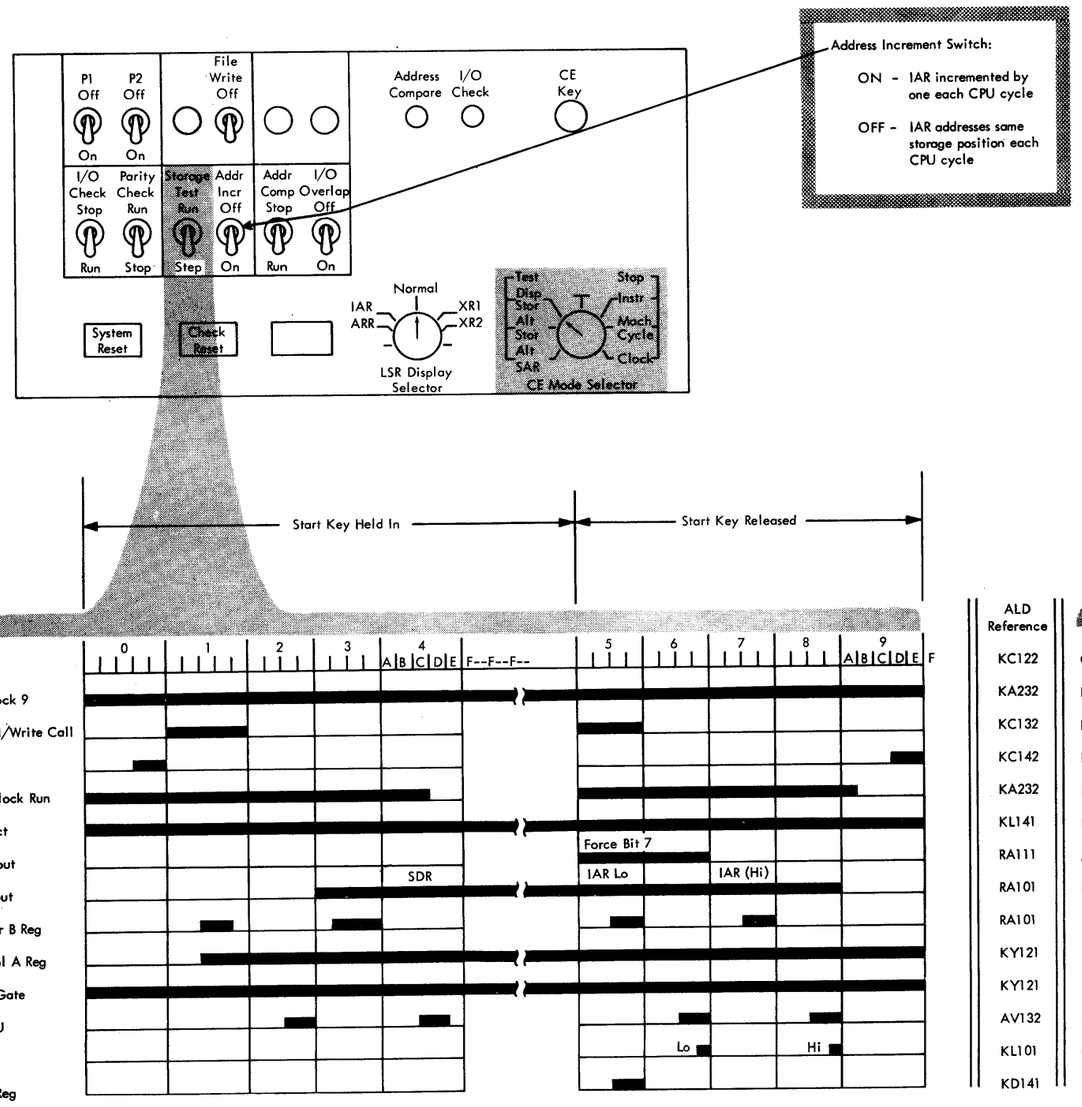


Diagram 5-252. Display Storage (Part 2 of 3)

2 3 4 5 6 7 8 9

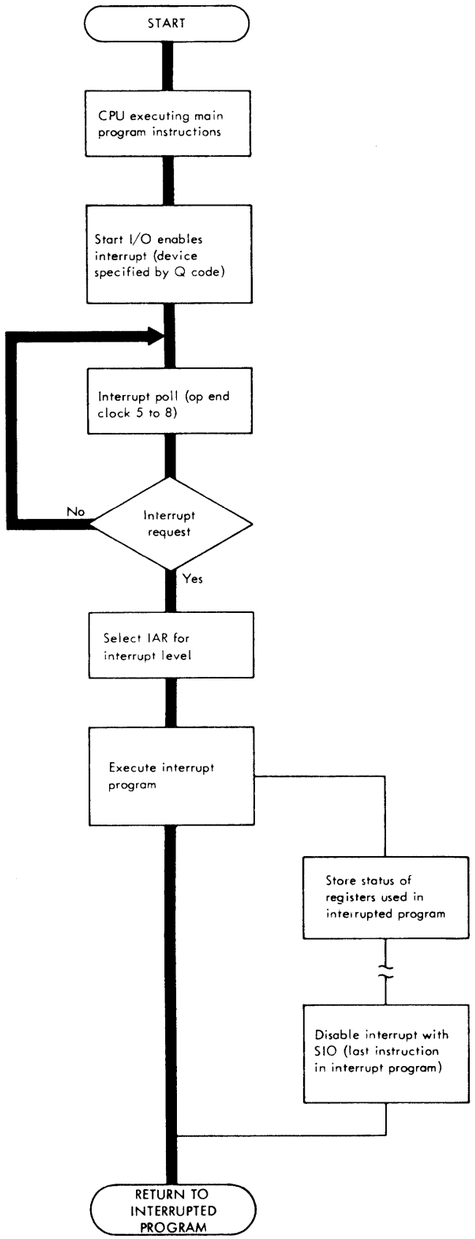
A B C D E

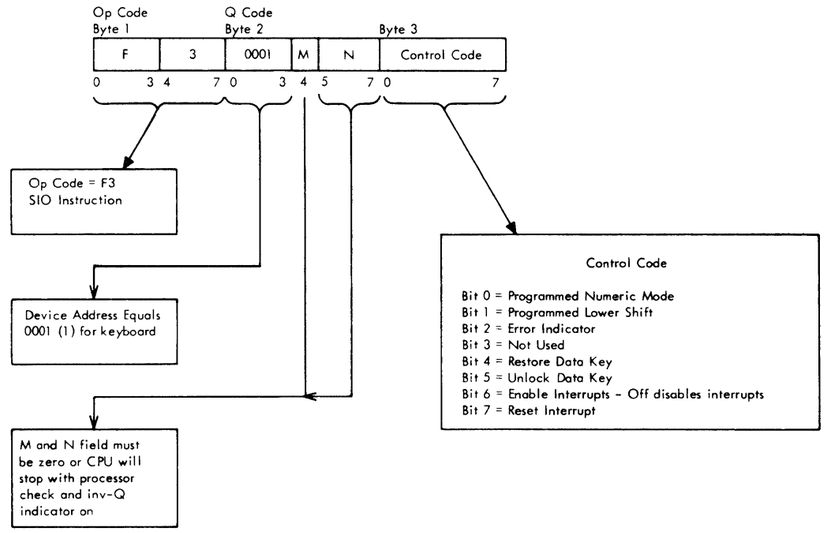


Interrupt

Objectives:

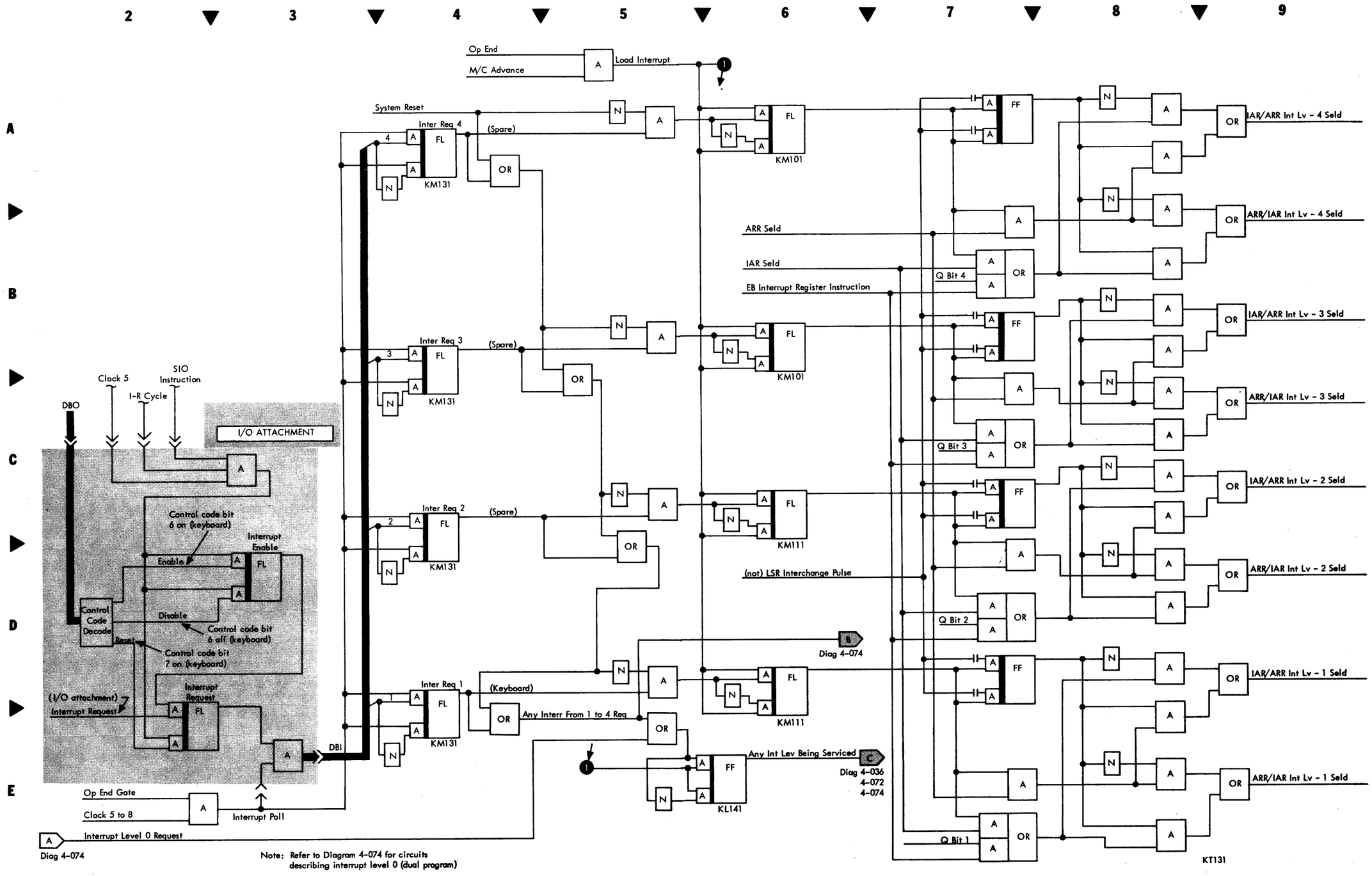
- Interrupt enable is turned on in I/O attachment by control code of SIO instruction
- I/O attachment sends interrupt request to CPU
- Interrupt occurs only after current instruction is finished
- Interrupts main program with separate program
- Highest interrupt device takes precedence over lower level devices
- Interrupt program ends with another SIO to disable interrupt





SIO Instruction Format for 5475 Keyboard (interrupt level 1)

Diagram 5-260. Interrupt (Part 1 of 2)


2
3
4
5
6
7
8
9
A
B
C
D
E
Op End
M/C Advance
Load Interrupt
System Reset
Inter Req 4
(Spare)
KM131
KM101
ARR Seld
IAR Seld
EB Interrupt Register Instruction
Q Bit 4
Q Bit 3
Q Bit 2
Q Bit 1
IAR/ARR Int Lv - 4 Seld
ARR/IAR Int Lv - 4 Seld
IAR/ARR Int Lv - 3 Seld
ARR/IAR Int Lv - 3 Seld
IAR/ARR Int Lv - 2 Seld
ARR/IAR Int Lv - 2 Seld
IAR/ARR Int Lv - 1 Seld
ARR/IAR Int Lv - 1 Seld
KT131
Inter Req 3
Inter Req 2
Inter Req 1
KM111
(not) LSR Interchange Pulse
Diag 4-074
(Keyboard)
Any Interr From 1 to 4 Req
Any Int Lev Being Serviced
Diag 4-036
4-072
4-074
KL141
DBO
Clock 5
I-R Cycle
SIO Instruction
I/O ATTACHMENT
Control code bit 6 on (keyboard)
Interrupt Enable
Enable
Control Code Decode
Disable
Control code bit 6 off (keyboard)
Reset
Control code bit 7 on (keyboard)
Interrupt Request
(I/O attachment) Interrupt Request
DBI
Op End Gate
Clock 5 to 8
Interrupt Poll
Interrupt Level 0 Request
Diag 4-074
Note: Refer to Diagram 4-074 for circuits describing interrupt level 0 (dual program)

2 3 4 5 6 7 8 9

A B C D E

POWER ON SEQUENCE

Turn on mainline CB

Activate power control circuits and energize convenience outlets.

Start with power available at input of mainline CB.

Energize +24 Vdc control power supply (TP2 = +24 Vdc)
1. Energize K1 (115 Vac convenience outlet power available).
2. Energize K2.

If the lamp test switch is pressed, only the thermal and power check indicators light.

Turn on power on/off switch.

Energize K3
1. Apply power to use meter power pack.
2. Apply power to logic and memory supply.
3. Apply power to gate and power supply fans.

Logic and memory supply energizes regulators.
1. Bias voltage (20 Vdc ± 10%) supplied to -4 Vdc, +6 Vdc, and -30 Vdc regulators.
2. Bulk voltages supplied to each regulator (terminals E1 and E2 of each regulator)
   - 10.2 Vdc to -4 Vdc supply (± 10%)
   - 12.4 Vdc to +6 Vdc supply (± 10%)
   - 46 Vdc to -30 Vdc supply (± 10%)

? BSCA feature installed — Yes

No — Apply 26 Vac to BSCA -12 Vdc supply
1. Energize K30 (sense BSCA -12V)
2. TP9 = 0 Vdc

-4 Vdc regulator output available
1. Energize K5 (senses -4V output)
2. Transfer K5-2 (TP2 = 0 Vdc)
3. Transfer K5-1 (starts +6 Vdc regulator)

Note: If -4V logic supply #2 and -4V logic supply #3 are installed, K17-1 and K19-1 are wired in series with K5-1; if -4V logic supply #2 is installed, K17-1 and K5-1 are in series.

? -4 Vdc logic supply #2 installed — Yes

No — ? -4 Vdc logic supply #3 installed — Yes

Energize K17 when -4V output is available.
1. TP3 = 0 Vdc
2. K17 is in series with K5-1.

Energize K19 when -4V output is available
1. TP4 = 0 Vdc
2. K19-1 is in series with K5-1 and K17-1.

No

(1)

(1)

Start voltage is applied to E12 of the +6V regulator.

+6 Vdc regulator output available
1. Energize K6 (senses +6V output)
2. TP5 = 0 Vdc (K6-2 contacts)
3. Activate -4V UV ax circuit (K6-3 contacts)
4. Energize time delay relay K7 (K6-1 contacts)
5. K7 energizes after 1 to 3 seconds delay.
6. Start -30 Vdc regulator (K7-1 contacts - - E12 terminal)

-30 Vdc regulator output available
1. Energize K8 (sense -30V output)
2. TP6 = 0 Vdc (K8-2 contacts)
3. Energize K9 (Energized by K8-1 contacts)
4. K9 supplies AC power to I/O device power supplies and lamp supplies. Clock 9 is forced on.
   (220/235 Vac supplied to I/O for 50 HZ
   208/230 Vac supplied to I/O for 60 HZ)

+24 Vdc 5424 supply and +60 Vdc 5203 supply outputs available.
1. Energize K10 and K11.
2. K10-1 and K11-1 hold K3 energized until both +24 Vdc 5424 supply and +60 Vdc 5203 supply are powered down during a normal power off sequence.
3. TP7 = 0 Vdc (K10-2 contacts)
4. TP8 = 0 Vdc (K11-2 contacts)

Energize K12
1. Turn off power check light (K12-1 contacts)
2. Remove power on reset and turn off clock 9 (K12-2 contacts)

END OF POWER ON SEQUENCE.
SYSTEM READY FOR PROCESSING

POWER OFF SEQUENCE

Turn off power on/off switch.

Apply +24 Vdc to -4V undervoltage ax circuit to prevent abnormal power down sequence (section C of on/off switch)

De-energize K7 to turn off -30 Vdc supply. (De-energize K9 at same time as K7:)
1. K1-1 removes start -30V.
2. Turn off -30V regulator (20 Vdc bias and 46 Vdc bulk voltages are present at -30V input until K3 de-energizes).

De-energize K8 to sense when -30 Vdc supply output is not available.

De-energize K12
1. K12-1 contacts turn on the power check light.
2. K12-2 contacts activate the power on reset relay line to CPU.
3. K12-3 contacts are used in the power on sequence.

Transfer K9 contacts to remove input power to 5424 24 Vdc and to 5203 60 Vdc supplies

Note: K9 de-energizes slower than K7

De-energize K10 (sense MFCU 24V) and K11 (sense 5203 60V)

De-energize K3 to remove bulk and bias voltages to -4 Vdc, +6 Vdc, and -30 Vdc regulators.

De-energize K5 (-4V sense) after -4 Vdc output is no longer available. (TP2 = +24 Vdc - - Turn off power check light.)

De-energize K6 (+6V sense) after +6 Vdc output is no longer available.

? -4 Vdc logic supply #2 installed — Yes

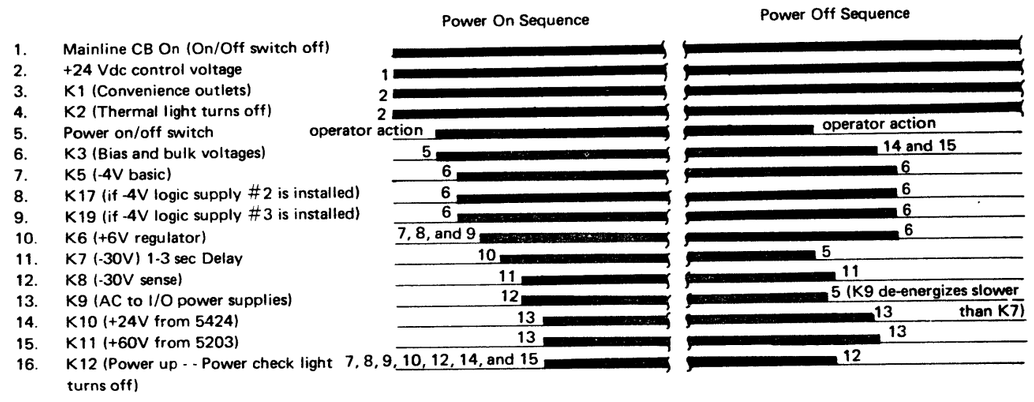
No — De-energize K17 -4 Vdc logic supply #2 sense after -4 Vdc is no longer available.

? -4 Vdc logic supply #3 installed — Yes

No — De-energize K19 (#3 feature -4 Vdc sense) after -4 Vdc is no longer available.

END OF NORMAL POWER OFF SEQUENCE

Note: K1 and K2 remain energized as long as +24V sequence control voltage is available.



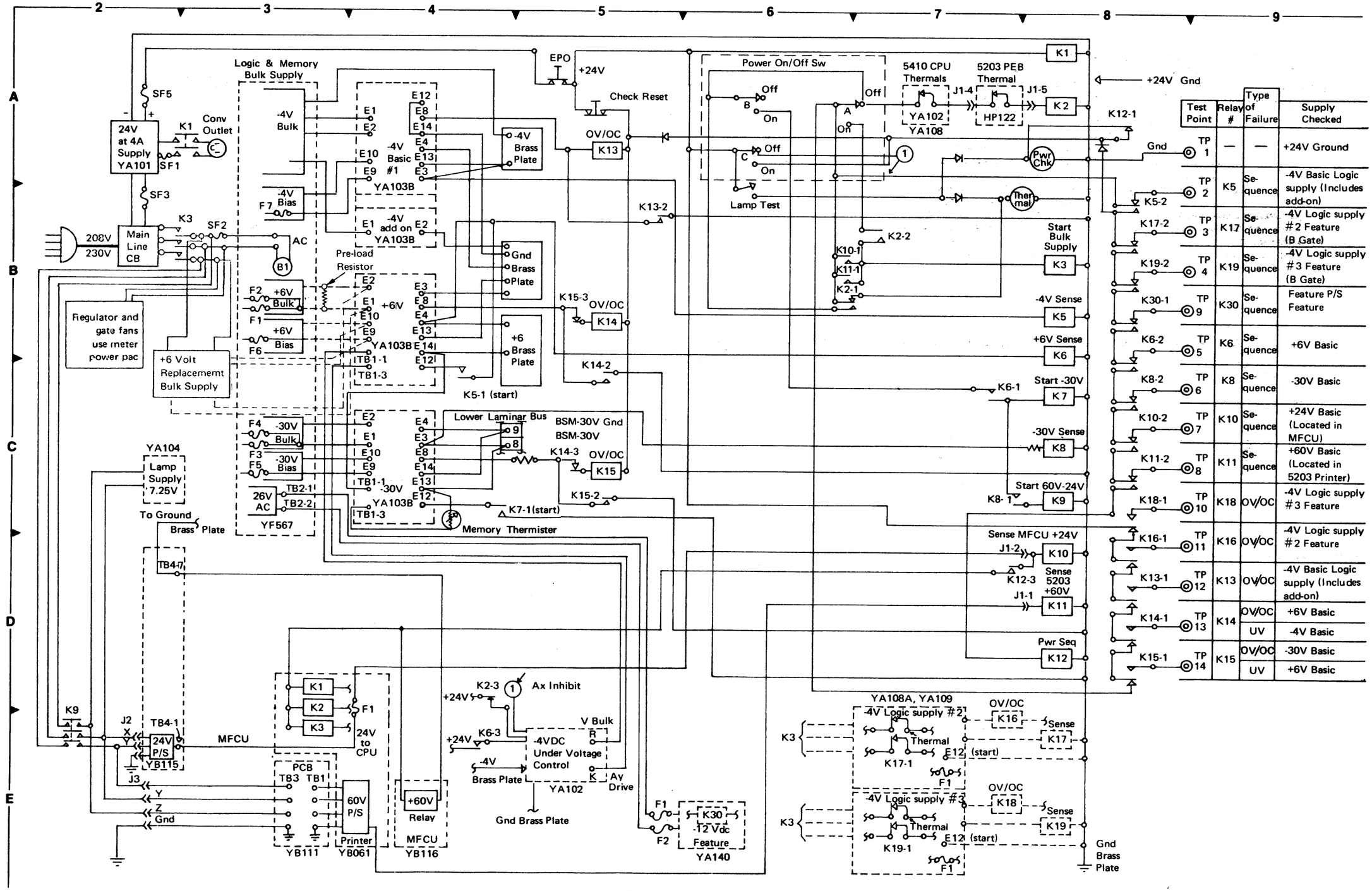


Diagram 6-010. Power Control Sequencing Diagram (Early)

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Revised April 5, 1971
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POWER ON SEQUENCE

Turn on mainline CB

Activate power control circuits and energize convenience outlets.

Start with power available at input of mainline CB.

Energize +24 Vdc control power supply (TP2 = +24 Vdc)
1. Energize K1 (115 Vac convenience outlet power available).
2. Energize K2.

If the lamp test switch is pressed, only the thermal and power check indicators light.

Turn on power on/off switch.

Energize K3
1. Apply power to logic and memory supply.
2. Apply power to gate and power supply fans.

Logic and memory supply energizes regulators.
1. Bias voltage (20 Vdc ± 10%) supplied to -4 Vdc, +6 Vdc, and -30 Vdc regulators.
2. Bulk voltages supplied to each regulator (terminals E1 and E2 of each regulator)
   - 10.2 Vdc to -4 Vdc supply (± 10%)
   - 12.4 Vdc to +6 Vdc supply (± 10%)
   - 46 Vdc to -30 Vdc supply (± 10%)

BSCA feature installed? Yes / No

Apply 26 Vac to BSCA -12 Vdc supply.
1. Energize K30 (sense BSCA -12V)
2. TP9 = 0 Vdc

-4 Vdc regulator output available
1. Energize K5 (senses -4V output)
2. Transfer K5-1 (TP2 = 0 Vdc)
3. Transfer K5-2 (starts +6 Vdc regulator

Note: If -4V logic supply #2 Feature and -4V logic supply #3 Feature are installed, K17-1 and K19-1 are wired in series with K5-2; if -4V logic supply #2 is installed, K17-1 and K5-2 are in series.

-4 Vdc logic supply #2 Feature installed? Yes / No

Energize K17 when -4V output is available.
1. TP3 = 0 Vdc
2. K17 is in series with K5-2

-4 Vdc logic supply #3 Feature installed? Yes / No

Energize K19 when -4V output is available
1. TP4 = 0 Vdc
2. K19-1 is in series with K5-2 and K17-1.

(1)

Start voltage is applied to E12 of the +6V regulator.

+6 Vdc regulator output available
1. Energize K6 (senses +6V output)
2. TP5 = 0 Vdc (K6-4 contacts)
3. Activate -4V UV ax circuit (K6-3 contacts)
4. Energize time delay circuit (K6-1 contacts)
5. Start -30 Vdc regulator (E12 to ground when T3 and T4 conduct)

-30 Vdc regulator output available
1. Energize K8 (sense -30V output)
2. TP6 = 0 Vdc (K8-2 contacts)
3. Energize K9, K9A, K9B (Energized by K8-1 contacts)
4. K9 supplies AC power to I/O device power supplies (220/235 Vac supplied to I/O for 50 HZ 208/230 Vac supplied to I/O for 60 HZ)
5. K9A supplies 115 Vac to printer keyboard feature.
6. K9B supplies 7.25 Vac to the system lamps (clock 9 is forced on) and 41 Vac is supplied to the use meter power pac.

+24 Vdc 5424 supply and +60 Vdc 5203 supply outputs available.
1. Energize K10 and K11.
2. K10-1 and K11-1 hold K3 energized until both +24 Vdc 5424 supply and +60 Vdc 5203 supply are powered down during a normal power off sequence.
3. TP7 = 0 Vdc (K10-2 contacts)
4. TP8 = 0 Vdc (K11-2 contacts)

Energize K12
1. Turn off power check light (K12-2 contacts)
2. Remove power on reset and turn off clock 9 (K12-4 contacts)

END OF POWER ON SEQUENCE. SYSTEM READY FOR PROCESSING

POWER OFF SEQUENCE

Turn off power on/off switch.

Apply +24 Vdc to -4V undervoltage ax circuit to prevent abnormal power down sequence (section C of on/off switch)

De-energize time delay circuit to turn off -30 Vdc supply. (De-energize K9 at same time as time delay circuit.)
1. T3, T4 removes start -30V.
2. Turn off -30V regulator (20 Vdc bias and 46 Vdc bulk voltages are present at -30V input until K3 de-energizes).

De-energize K8 to sense when -30 Vdc supply output is not available.

De-energize K12
1. K12-2 contacts turn on the power check light.
2. K12-4 contacts activate the power on reset relay line to CPU.
3. K12-1 contacts are used in the power on sequence.

Transfer K9, K9A, K9B contacts to remove input power to 5424 24 Vdc and to 5203 60 Vdc supplies

Note: K9 de-energizes slower than the time delay circuit.

De-energize K10 (sense MFCU 24V) and K11 (sense 5203 60V)

De-energize K3 to remove bulk and bias voltages to -4 Vdc, +6 Vdc, and -30 Vdc regulators.

De-energize K5 (-4V sense) after -4 Vdc output is no longer available. (TP2 = +24 Vdc - - Turn off power check light.)

De-energize K6 (+6V sense) after +6 Vdc output is no longer available.

-4 Vdc logic supply #2 Feature installed? Yes / No

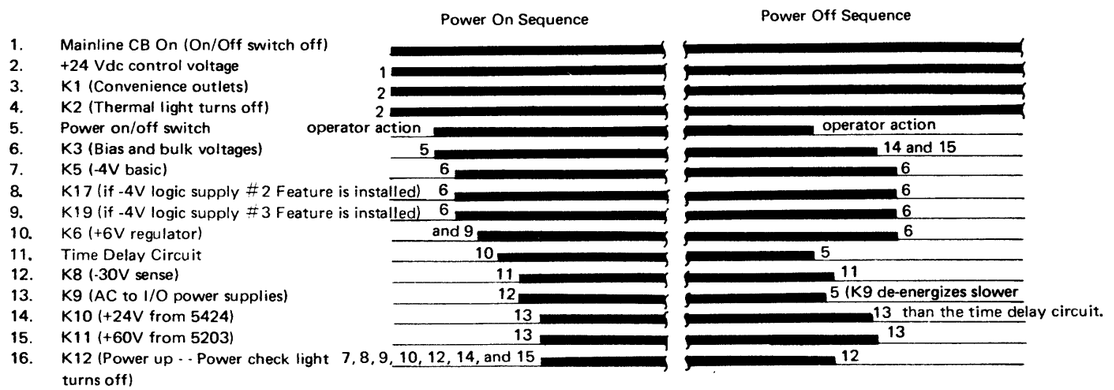
De-energize K17 -4 Vdc logic supply #2 sense after -4 Vdc is no longer available.

-4 Vdc logic supply #3 Feature installed? Yes / No

De-energize K19 (#3 feature -4 Vdc sense) after -4 Vdc is no longer available.

Note: K1 and K2 remain energized as long as +24V sequence control voltage is available.

END OF NORMAL POWER OFF SEQUENCE



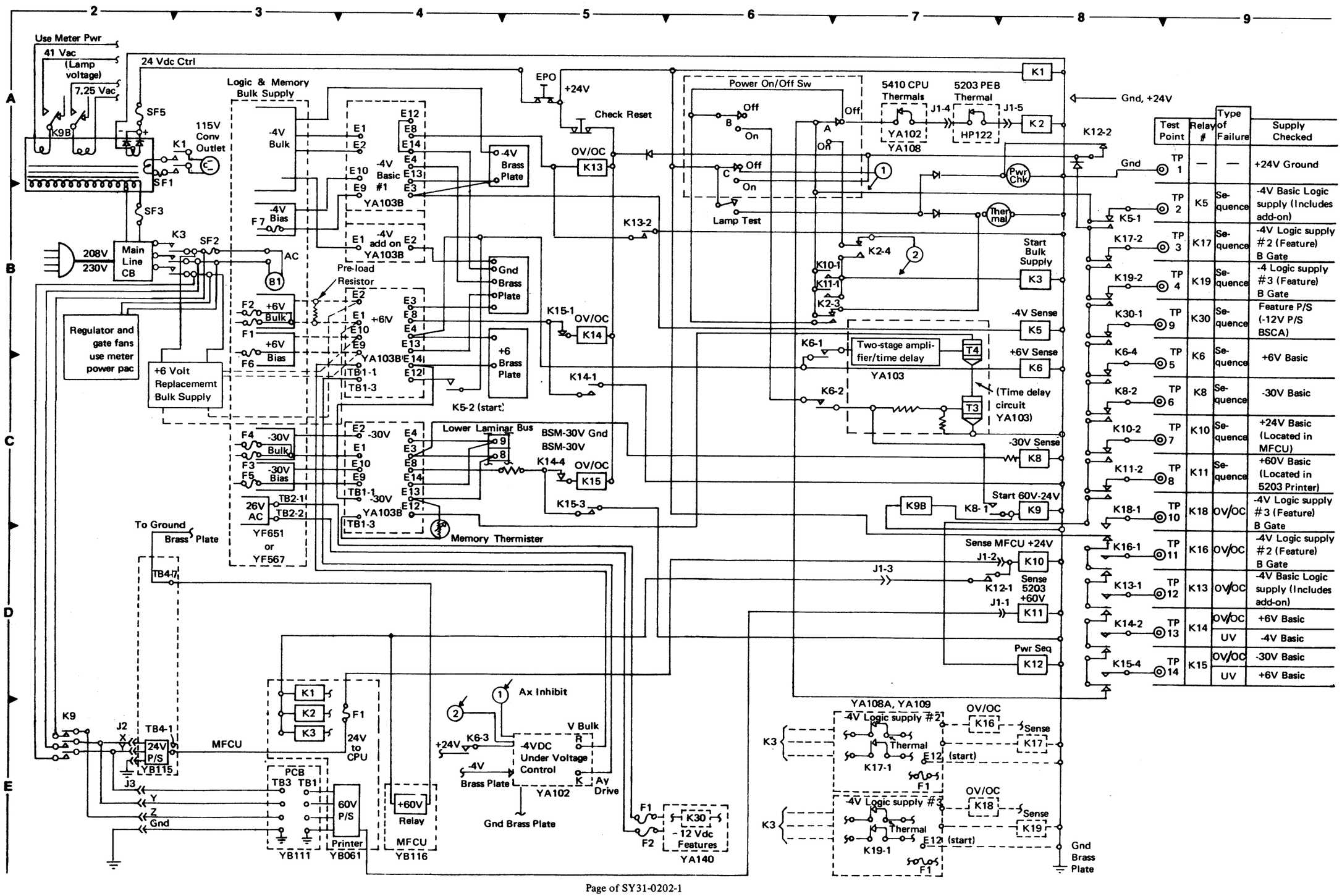


Diagram 6-020. Power Control Sequencing Diagram (Redesign)

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