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IBM Maintenance Library

5410 Processing Unit Maintenance Manual

SY31-0244-2

Preface

This manual, SY31-0244, contains maintenance information for the IBM 5410 Processing Unit. It should be used in conjunction with the maintenance manuals for the System/3 input/output devices to fully maintain the system.

The *IBM 5410 Processing Unit Theory of Operation*, SY31-0207, gives the instructional material.

The black circle shown here ● symbolizes the latest FE Supplement added to this manual.

TNL No. SN31-0307 dated December 1, 1971 has been added to this manual on Microfiche.

Summary of Amendments

This TNL adds 48K and 64K information. It also adds information on the +6V expansion power supply.

Fourth Edition (January 1971)

This is a major revision of, and obsoletes SY31-0244-1.

Some illustrations in this manual have a code number in the lower corner. This is a processing control number and is not related to the subject matter.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest FE Publication System Sequence Listing for revisions or contact the local IBM branch office.

A Reader's Comments Form is at the back of this publication. If the form is gone, address your comments to IBM Corporation, Publications, Department 245, Rochester, Minnesota 55901.

A	Ampere
AAR	Operand 2 Address Register
ac	Alternating Current
Addr	Address
adj	Adjust
ALD	Automated Logic Diagram
ALU	Arithmetic and Logic Unit
APL	Advance Program Level
Arith	Arithmetic
ARR	Address Recall Register
ASCII	American Standard Code for Information Interchange
Asynchronous	Without regular time relationships; unexpected or unpredictable with respect to the execution of a program instruction.
BAR	Operand 1 Address Register
BCD	Binary Coded Decimal
Bit	Binary digit; smallest unit of information
BM	Bill of Material
BSCA	Binary Synchronous Communications Adapter
BSM	Basic Storage Module
Byte	Eight bits of information plus parity bit
CB	Circuit Breaker
CE	Customer Engineer
Channel	A hardware device that connects the CPU and main storage with the I/O control units
cm	Centimeter
Cond	Condition
CPU	Processing Unit
CRR	Condition Recall Register
Ctrl	Control
DAR	Data Address Register
DBI	Data Bus In
DBO	Data Bus Out
DFCR	Data File Control Address Register
DFDR	Data File Data Address Register
Disp	Display
DRR	Data Recall Register
EBCDIC	Extended Binary Coded Decimal Interchange Code
EC	Engineering Change
ECA	Engineering Change Announcement
FBM	Field Bill of Material
FE	Field Engineering
FEALD	Field Engineering Automated Logic Diagram
hex	Hexadecimal
Hi	High
IAR	Instruction Address Register
Instr	Instruction
Interrupt	An asynchronous occurrence which causes the central processor to cease its normal execution of instructions and branch out to a new instruction stream. Interrupts are caused by several different and unrelated situations.
I/O	Input/Output
IPL	Initial Program Load
K	Kilo, Thousand
LCR	Length Count Register
LCRR	Length Count Recall Register
LIO	Load Input/Output
Lo	Low
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LSR	Local Store Register
MAP	Maintenance Analysis Procedures
MES	Miscellaneous Equipment Specification
MFCU	Multi-Function Card Unit
MLC	Machine Level Control
Mnem	Mnemonic
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MRDAR	MFCU Read Data Address Register
MST	Monolithic System Technology
mV	Millivolt
ns	Nanosecond
OC	Overcurrent
Op	Operation; Operand
OV	Overvoltage
P	Parity
PAIR	Product Analysis Incident Reprot
PCB	Printer Control Board
PEB	Printer Electronic Board
PG	Parity Generation
POT	Potentiometer
P/S	
PSR	Program Status Register
PSS	Print Subscan
PTR	Printer
Rd	Read
REA	Request for Engineering Action
Reg	Register
RPQ	Request Price Quotation
SAR	Storage Address Register
SIO	Start Input/Output
SLD	Solid Logic Dense
SLT	Solid Logic Technology
SMS	Standard Modular System
SS	Single Shot
Sync	Synchronize
Sys	System
S/Z	Sense-Inhibit
TIO	Test Input/Output and Branch
TP	Test Point
UV	Under voltage
V	Volts
Vac	Volts Alternating Current
Vdc	Volts Direct Current
wr	write
XR	Index Register
XRD	X-Read
XWR	X-Write
YRD	Y-Read
YWR	Y-Write
Z	Inhibit
=	Equals
>	Greater than
<	Less Than

PERSONAL SAFETY

Be sure to read and follow the safety suggestions in Form 229-1264, a pocket-sized card issued to all IBM Customer Engineers.

Remember:

- Loose clothing can become entangled in moving parts of the machine.
- Drive belts, because of their internal cable construction, can cause serious injury. DO NOT crank a machine by pulling on the drive belts.
- Heat sinks are at an electrical potential. DO NOT short heat sinks to each other or to the machine side frame.
- Always unplug machine power and wait ONE FULL MINUTE before attempting repairs or adjustments in the power supply area.
- Voltages developed in the resonant circuit of regulating power supplies are apt to be much greater than the line voltages.
- Follow the specific safety precautions that accompany many of the adjustment procedures in this manual.

Be aware that the 5424 motor and/or clutches can operate unexpectedly. Conditions that could cause this are:

- Program commands.
- Loss of a dc voltage to a machine, gate, board or chassis, card, or pin.
- Removing or inserting a card or cable.
- Probing and accidentally shorting a pin.

EQUIPMENT SAFETY

Electrical

Always replace blown fuses with fuses of the same type and rating. Using fuses of a different type or higher rating could result in component damage.

Remove power from the machine before replacing MST cards, magnets, or solenoids. Failure to do this could result in damage to a card being replaced or to other cards in the net.

Mechanical

Do not operate the machine under power with units disassembled, removed, or maladjusted. Keep tools, etc. clear of the mechanism when the machine is operating under power.

Caution
Do not use IBM cleaning fluid on plastic parts.

REFERENCE DATA

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This section contains charts, listings, and diagrams giving general information for diagnosing system failures.

Refer to the *IBM Field Engineering Maintenance Diagrams, 5410 Central Processing Unit*, Form SY31-0202 (FEMD) for flowcharts, simplified diagrams, timing charts, etc. The FEMD is to be used for instructional and for recall purposes.

For diagnostic techniques, refer to the maintenance analysis procedures (MAP) chart user's guide. The MAP charts help CEs to isolate machine troubles without the use of an oscilloscope. Figure 1-1 shows the format of the 96-column card used with the System/3., Figures 1-2 Fr. A16 through 1-8 Fr. B08 show the instruction sets and the instruction format used in this system. Figures 1-9 Fr. B08 through 1-17 Fr. B16 show the sense bytes of the 5410. Figures 1-18 Fr. B17 through 1-30 Fr. C09 show other diagnostic aids for troubleshooting the 5410 CPU.

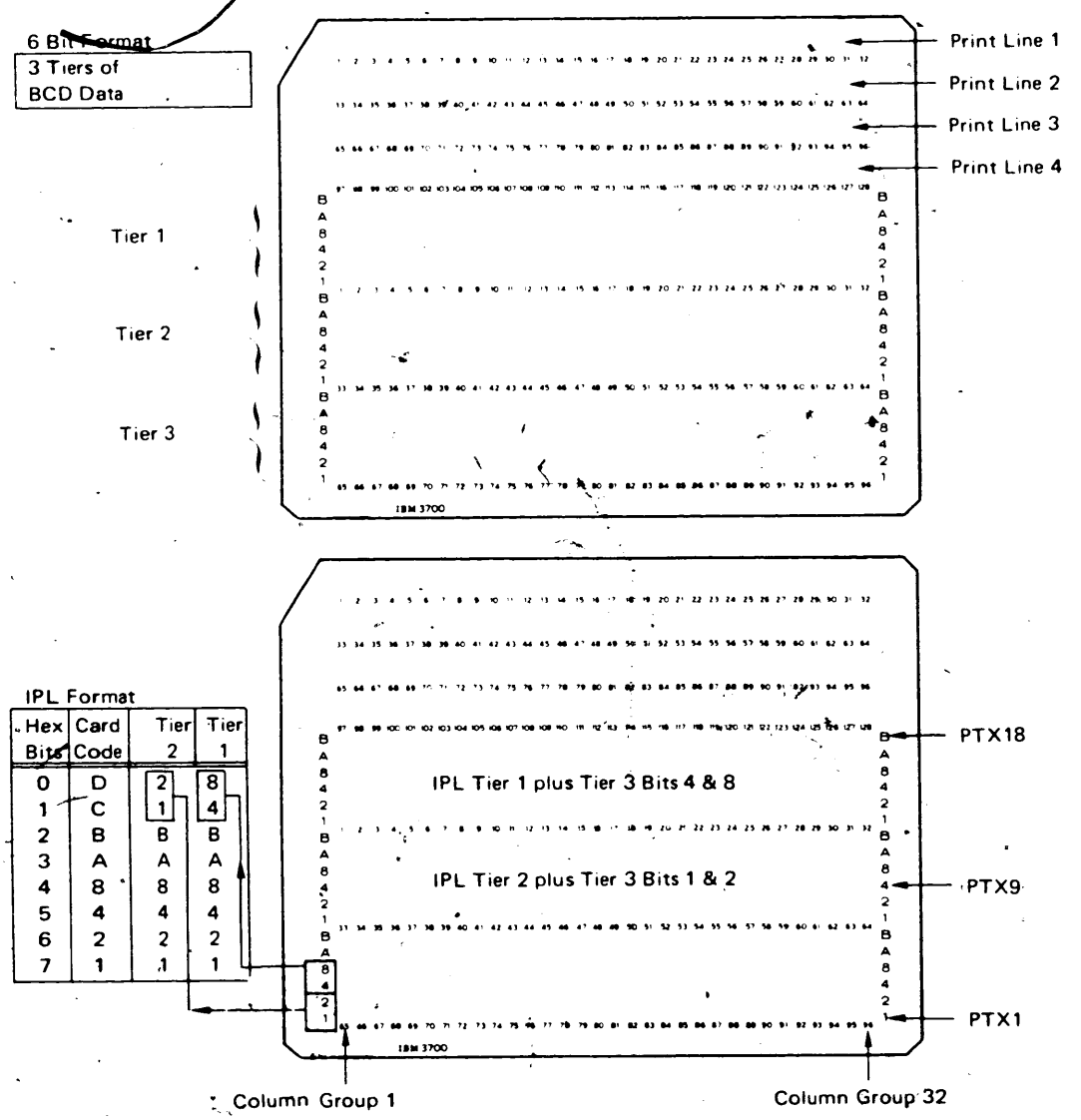


Figure 1-1. 96-Column Card Format

	Mnem	Op	Q	Operands				Comments
Two Address Instruction	ZAZ	4	L_1L_2					Zero and add zoned
	AZ	6	L_1L_2					Add zoned decimal
	SZ	7	L_1L_2					Subtract zoned decimal
	MVX	8						Move hex characters
	ED	A	L_1					Edit
	ITC	B	L_1					Insert and test characters
	MVC	C	L					Move characters
	CLC	D	L					Compare logical characters
	ALC	E	L					Add logical characters
	SLC	F	L					Subtract logical characters
		0		Op1	Op2			Op1 direct, Op2 direct
		1		Op1	Op2			Op1 direct, Op2 indexed by XR1
		2		Op1	Op2			Op1 direct, Op2 indexed by XR2
		4		Op1	Op2			Op1 indexed by XR1, Op2 direct
		5		Op1	Op2			Op1 indexed by XR1, Op2 indexed by XR1
		6		Op1	Op2			Op1 indexed by XR1, Op2 indexed by XR2
		8		Op1	Op2			Op1 indexed by XR2, Op2 direct
		9		Op1	Op2			Op1 indexed by XR2, Op2 indexed by XR1
		A		Op1	Op2			Op1 indexed by XR2, Op2 indexed by XR2
One Address Instruction (Non-Branch)	SNS	0	DA M N					Sense I/O
	LIO	1	DA M N					Load I/O
	ST	4	Reg					Store register
	L	5	Reg					Load register
	A	6	Reg					Add to register
	TBN	8	Mask					Test bits on
	TBF	9	Mask					Test bits off
	SBN	A	Mask					Set bits on
	SBF	B	Mask					Set bits off
	MVI	C	I_2					Move logical immediate
	CLI	D	I_2					Compare logical immediate
		3		Op1 Addr				Op1 direct
		7		Op1				Op1 indexed by XR1
		B		Op1				Op1 indexed by XR2
One Address Instruction (Branch)	BC	0	Cond					Branch on condition
	TIO	1	DA M N					Test I/O and branch
	LA	2	Bit 6-XR2 Bit 7-XR1					Load address
		C		Op1 Addr				Op1 direct
		D		Op1				Op1 indexed by XR1
		E		Op1				Op1 indexed by XR2
Command Instruction	HPL	F0	Tens	Unit				Halt program level
	APL	F1	DA M N	N U				Advance program level
	JC	F2	Cond	Number of bytes to jump				Jump on condition
	SIO	F3	DA M N	Control				Start I/O

Figure 1-2. Instructions

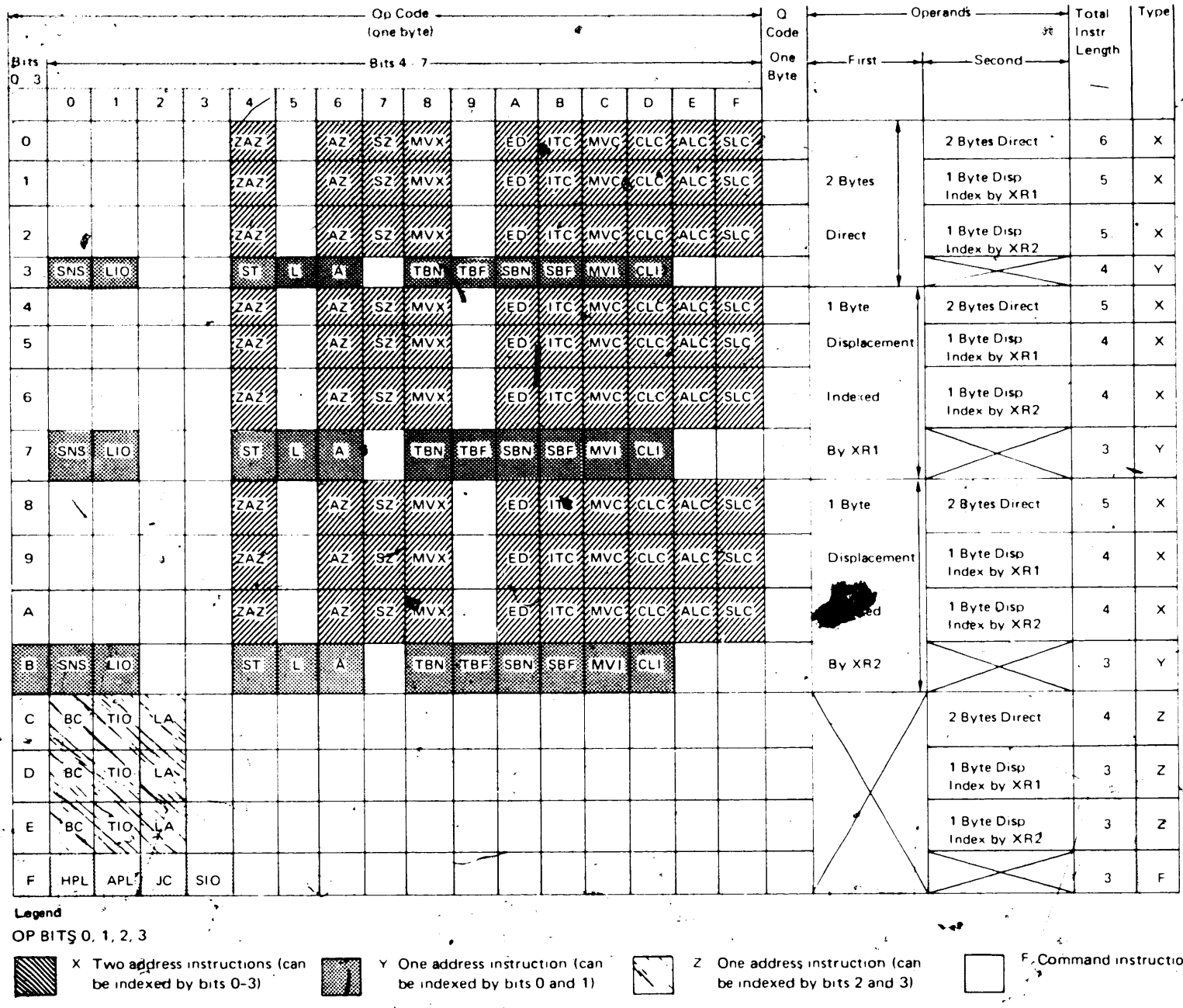


Figure 1-3. Instruction Codes and Addressing Schemes

CPU CYCLE PATTERNS

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
04	ZAZ	x	x			x	x		x	x	x	x
06	AZ	x	x			x	x		x	x	x	x
07	SZ	x	x			x	x		x	x	x	x
08	MVX	x	x			x	x		x	x	x	x
0A	ED	x	x			x	x		x	x	x	x
0B	ITC	x	x			x	x		x	x	x	x
0C	MVC	x	x			x	x		x	x	x	x
0D	CLC	x	x			x	x		x	x	x	x
0E	ALC	x	x			x	x		x	x	x	x
0F	SLC	x	x			x	x		x	x	x	x
14	ZAZ	x	x			x	x	x			x	x
16	AZ	x	x			x	x	x			x	x
17	SZ	x	x			x	x	x			x	x
18	MVX	x	x			x	x	x			x	x
1A	ED	x	x			x	x	x			x	x
1B	ITC	x	x			x	x	x			x	x
1C	MVC	x	x			x	x	x			x	x
1D	CLC	x	x			x	x	x			x	x
1E	ALC	x	x			x	x	x			x	x
1F	SLC	x	x			x	x	x			x	x
24	ZAZ	x	x			x	x	x			x	x
26	AZ	x	x			x	x	x			x	x
27	SZ	x	x			x	x	x			x	x
28	MVX	x	x			x	x	x			x	x
2A	ED	x	x			x	x	x			x	x
2B	ITC	x	x			x	x	x			x	x
2C	MVC	x	x			x	x	x			x	x
2D	CLC	x	x			x	x	x			x	x
2E	ALC	x	x			x	x	x			x	x
2F	SLC	x	x			x	x	x			x	x
30	SNS	x	x			x	x					x
31	LIO	x	x			x	x					x
34	ST	x	x			x	x					x
35	L	x	x			x	x					x
36	A	x	x			x	x					x
38	TBN	x	x			x	x					x
39	TBF	x	x			x	x					x
3A	SBN	x	x			x	x					x
3B	SBF	x	x			x	x					x
3C	MVI	x	x			x	x					x
3D	CLI	x	x			x	x					x
44	ZAZ	x	x		x				x	x	x	x
46	AZ	x	x		x				x	x	x	x
47	SZ	x	x		x				x	x	x	x
48	MVX	x	x		x				x	x	x	x
4A	ED	x	x		x				x	x	x	x
4B	ITC	x	x		x				x	x	x	x
4C	MVC	x	x		x				x	x	x	x
4D	CLC	x	x		x				x	x	x	x
4E	ALC	x	x		x				x	x	x	x
4F	SLC	x	x		x				x	x	x	x
54	ZAZ	x	x		x			x			x	x
56	AZ	x	x		x			x			x	x
57	SZ	x	x		x			x			x	x
58	MVX	x	x		x			x			x	x
5A	ED	x	x		x			x			x	x
5B	ITC	x	x		x			x			x	x
5C	MVC	x	x		x			x			x	x
5D	CLC	x	x		x			x			x	x
5E	ALC	x	x		x			x			x	x
5F	SLC	x	x		x			x			x	x
64	ZAZ	x	x		x			x			x	x
66	AZ	x	x		x			x			x	x
67	SZ	x	x		x			x			x	x
68	MVX	x	x		x			x			x	x
6A	ED	x	x		x			x			x	x
6B	ITC	x	x		x			x			x	x
6C	MVC	x	x		x			x			x	x
6D	CLC	x	x		x			x			x	x
6E	ALC	x	x		x			x			x	x
6F	SLC	x	x		x			x			x	x

Op	Mnem	Op	Q	R	X_1	H_1	L_1	X_2	H_2	L_2	A	B
70	SNS	x	x		x							x
71	LIO	x	x		x							x
74	ST	x	x		x							x
75	L	x	x		x							x
76	A	x	x		x							x
78	TBN	x	x		x							x
79	TBF	x	x		x							x
7A	SBN	x	x		x							x
7B	SBF	x	x		x							x
7C	MVI	x	x		x							x
7D	CLI	x	x		x							x
84	ZAZ	x	x		x				x	x	x	x
86	AZ	x	x		x				x	x	x	x
87	SZ	x	x		x				x	x	x	x
88	MVX	x	x		x				x	x	x	x
8A	ED	x	x		x				x	x	x	x
8B	ITC	x	x		x				x	x	x	x
8C	MVC	x	x		x				x	x	x	x
8D	CLC	x	x		x				x	x	x	x
8E	ALC	x	x		x				x	x	x	x
8F	SLC	x	x		x				x	x	x	x
94	ZAZ	x	x		x			x			x	x
96	AZ	x	x		x			x			x	x
97	SZ	x	x		x			x			x	x
98	MVX	x	x		x			x			x	x
9A	ED	x	x		x			x			x	x
9B	ITC	x	x		x			x			x	x
9C	MVC	x	x		x			x			x	x
9D	CLC	x	x		x			x			x	x
9E	ALC	x	x		x			x			x	x
9F	SLC	x	x		x			x			x	x
A4	ZAZ	x	x		x			x			x	x
A6	AZ	x	x		x			x			x	x
A7	SZ	x	x		x			x			x	x
A8	MVX	x	x		x			x			x	x
AA	ED	x	x		x			x			x	x
AB	ITC	x	x		x			x			x	x
AC	MVC	x	x		x			x			x	x
AD	CLC	x	x		x			x			x	x
AE	ALC	x	x		x			x			x	x
AF	SLC	x	x		x			x			x	x
B0	SNS	x	x		x							x
B1	LIO	x	x		x							x
B4	ST	x	x		x							x
B5	L	x	x		x							x
B6	A	x	x		x							x
B8	TBM	x	x		x							x
B9	TBF	x	x		x							x
BA	SBN	x	x		x							x
BB	SBF	x	x		x							x
BC	MVI	x	x		x							x
BD	CLI	x	x		x							x
C0	BC	x	x			x	x					
C1	TIO	x	x			x	x					
C2	LA	x	x			x	x					
D0	BC	x	x		x							
D1	TIO	x	x		x							
D2	LA	x	x		x							
E0	BC	x	x		x							
E1	TIO	x	x		x							
E2	LA	x	x		x							
F0	HPL	x	x	x								
F1	APL	x	x	x								
F2	JC	x	x	x								
F3	SIO	x	x	x								

Figure 1-4. CPU Instruction and Machine Cycles

CONTINUED ON
FRAME B01

TEST I/O AND BRANCH (TIO)

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16		
C1						Direct addressing — Operand 1 = 2 bytes
D1						Indexed by XR-1 — Operand 1 = 1 byte
E1						Indexed by XR-2 — Operand 1 = 1 byte
5424 MFCU	1111					Device address MFCU (F)
		0				Primary
		1				Secondary
			000			Feed not ready or error
			001			Read feed busy (condition 1)
			010			Punch data busy (condition 2)
			011			Condition 1 or 2
			100			Print data busy (condition 4)
			101			Condition 1 or 4
			110			Condition 2 or 4
			111			Condition 1, 2 or 4
				xxxx	xxxx	Branch to address if condition met. Op codes D1 and E1 are indexed.
5203 Printer	1110					Device address printer (E)
		0				Left carriage
		1				Right carriage
			000			Not ready
			001			Invalid
			010			Print buffer busy
			011			Invalid
			100			Carriage busy
			101			Invalid
			110			Printer busy
			111			Invalid
				xxxx	xxxx	Branch to address if condition met. Op codes D1 and E1 are indexed.
5471 and 5475	0001					Device address keyboard (1)
						Test I/O is invalid and will result in invalid Q byte processor check.
5444 Disk	1010					Device address disk drive 1 (A)
	1011					Device address disk drive 2 (B)
		0				Removable disk
		1				Fixed disk
			000			Not ready or error
			010			Busy - Data transfer in process
			100			Scan found
			*			*Condition may vary depending on disk drive selected. Refer to status byte.
				xxxx	xxxx	Branch to address if condition is met.
DPF	0000					Device address DPF (0)
		0				Must be zero
			0xx			Program level 1
			1xx			Program level 2
			x00			Cancel program level
			x01			Load program level from MFCU.
			x10			Load from console I/O
			*	xxxx	xxxx	Branch to address if condition is met. Op codes D1 and E1 are indexed.

Tests setting of DPF switch

* Note: All other N codes are invalid.

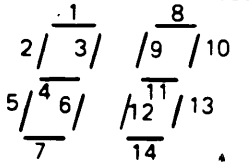
Figure 1-5. (Part 1 of 2) Test I/O and Branch (TIO) Instruction

Op Code	Q Code			Control Code	
	DA	M	N		
0 7	8 11	12	13 15	16	
C1					Direct Addressing – Operand 1 = 2 bytes
D1					Indexed by XR-1 – Operand 1 = 1 byte
E1					Indexed by SR-2 – Operand 1 = 1 byte
BSCA	0011				Device address SIOC (3)
		0			Must be zero
			000		Test for SIOC not ready
			010		Test for SIOC busy Note: All other N codes invalid.
				xxxx xxxx	Branch to address if condition is met. D1 and E1 are indexed.
	1000				Device address BSCA (8)
		0			Must be zero
			000		Not ready / Unit check
			001		Op end interrupt
			010		Busy
			011		ITB interrupt
			100		Interrupt pending
			101		Invalid
			110		New data
			111		Invalid
				xxxx xxxx	Branch to address if condition is met. D1 and E1 are indexed.
1442	0101				Device address 1442 (5)
		0			Must be zero
			000		Test for 1442 not ready
			010		Test for 1442 busy Note: All other N codes invalid.
				xxxx xxxx	Branch to address if condition is met. D1 and E1 are indexed.

Figure 1-5. (Part 2 of 2) Test I/O and Branch (TIO) Instruction

LOAD I/O (LIO) INSTRUCTION

Op Code	Q Code			Operand 1	
	DA	M	N		
0 7	8 11	12	13 15	16	
31					Direct addressing — Operand 1 = 2 bytes
71					Indexed by XR-1 — Operand 1 = 1 byte
B1					Indexed by XR-2 — Operand 1 = 1 byte
5203 Printer	1110				Device address line printer (E)
		0			M-bit is not used — a zero is preferred.
			000		Load form length. One byte for each carriage.
			100		Select line printer image address register
			110		Select line printer data address register
					Note: All other N codes invalid.
5424 MFCU	1111				Device address MFCU (F)
		0			Normal mode
		1			Diagnostic mode
			100		MFCU print address register
			101		MFCU read address register
			110		MFCU punch address register
					Note: All other N codes invalid
5444 Disk	1010				Device address disk drive 1 (A)
					Device address disk drive 2 (B)
		0			M-bit not used
			011		Diagnostic CE
			100		DFDR
			110		DFCR
					Note: All other N codes invalid.
5475 Keyboard	0001				Device address keyboard (1)
		0	000		M and N must be zero.



Data at operand Address-1									Data at operand 1 Address								
0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	
								Prog 1 ID									Prog 2 ID
1	2	3	4	5	6	7			8	9	10	11	12	13	14		
Indicator 1									Indicator 2								

Figure 1-6. (Part 1 of 2) Load I/O (LIO) Instruction

Op Code	Q Code			Operand 1	
0 7	DA 8 11	M 12	N 13 15	16	
31					Direct addressing—Operand 1 = 2 bytes
71					Indexed by XR-1—Operand 1 = 1 byte
B1					Indexed by XR-2—Operand 1 = 1 byte
SIOC	0011				Device address SIOC (3)
		0			Must be zero
			001		Load I/O function register
			010		Load SIOC length count register
			100		Load SIOC data address register
			101		Load data transfer register
					Note: All other N codes invalid.
5471 Printer Key-board	0001				Device address printer keyboard (1)
		1			Select printer must be a 1, 0 is invalid.
			000		Load EBCDIC character to be printed (N code must be zero.)
					Storage address can be one byte or two bytes (direct addressed, or indexed). The character to be printed is loaded from the first operand address - 1. All other N codes invalid.
BSCA	1000				Device address BSCA (8)
		0			Must be zero
			001		Stop address register
			010		Transition address register
			100		Current address register
			110		Current address register (not subject to busy)
					Note: All other N codes invalid.
1442	0101				Device address 1442 (5)
		0			Must be zero
			000		Load punch LCR
			100		Load 1442 DAR
					Note: All other N codes invalid.

Figure 1-6. (Part 2 of 2) Load I/O (LIO) Instruction

START I/O (SIO) INSTRUCTION

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
	1110					Device address printer (E)
		0				Left carriage is used (single feed carriage)
		1				Right carriage is used
			000			Space only
			001			Invalid
			010			Print followed by spacing
			011			Invalid
			100			Skip only
			101			Invalid
5203 Printer			110			Print followed by skip
			111			Invalid
				0000	0000	No space — A number greater than 3 is not permitted and will result in a space zero operation.
				0000	0001	One space
				0000	0010	Double space
				0000	0011	Triple space
				0000	0001	Skip to line 1 — A number greater than /00F0 may result in a carriage runaway. 112 lines are the maximum length of a form (8 lines per inch).
				0000	0010	Skip to line 2
				0110	1111	Skip to line 110
				0111	0000	Skip to line 112
	1111					Device Address MFCU (F)
		0				Primary card path is used
		1				Secondary card path is used
			000			Feed
			001			Read
			010			Punch feed
			011			Punch read
			100			Print feed
			101			Print read
			110			Punch print feed
5424 MFCU			111			Punch print read
				0		Printbuffer 1 is used
				1		Printbuffer 2 is used
				1		8 bit IPL read
				1		Print 4 lines
				x		Reserved
					x	Reserved
					000	No selection
					100	Select stacker 4
					101	Select stacker 1
					110	Select stacker 2
					111	Select stacker 3
	0001	0	0000			Device Address Keyboard, M and N must be zero
				1		Program numeric shift
				1		Program lower shift
				1		Turn error indicator on
5475 Keyboard					1	Restore key
					1	Unlock keyboard
					0	Disable interrupt
					1	Enable interrupt
					1	Turn off interrupt request

Figure 1-7. (Part 1 of 3) Start I/O (SIO) Instruction

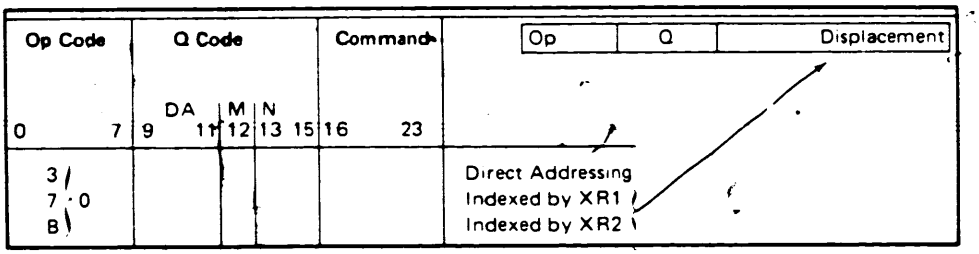
Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
5444 Disk	1010					Device address disk drive 1 (A)
	1011					Device address disk drive 2 (B)
		0				Removable disk
		1				Fixed disk
			000	0000	0000	Control - Seek
			001	0000	0000	Read - Data
			001	0000	0001	Read - Identifier
			001	0000	0010	Read - Diagnostic
			001	0000	0011	Read - Verify
			010	0000	0000	Write - Data
			010	0000	0001	Write - Identifier
			011	0000	0000	Scan - Equal
			011	0000	0001	Scan - Low or equal
			011	0000	0010	Scan - High or equal
						Notes: • Bits 16-21 are not used by the attachment. • All other N codes invalid.
SIOC	0011					Device address SIOC (3)
		0				M-bit is not used — zero is preferred.
			000	0000	0001	Reset interrupt request
			000	0000	0010	Enable interrupt ability
			000	0000	0100	Reset interrupt ability
			000	0000	1000	Remove SIOC from busy state
			000	0001	0000	Set interrupt request
						These control codes may also be used with N codes 001 or 010 below.
			001	0000	0000	Read I/O device
			010	0000	0000	Write I/O device
			011			I/O Control 1
				1		I/O Select 8
				1		I/O Select 7
				1		I/O Select 6
				1		I/O Select 5
					1	I/O Select 4
					1	I/O Select 3
					1	I/O Select 2
					1	I/O Select 1
			100			I/O Control 2
				1		I/O Select 14
				1		I/O Select 13
				1		I/O Select 12
				1		I/O Select 11
					1	I/O Select 10
					1	I/O Select 9
					1	I/O Unit 2 Select
					1	I/O Unit 1 Select
						All other N codes invalid.
DPF	0000	0	000			Device address - DPF - M and N must be zero
				0000	0	Not used
					1	Enable dual programming mode
					0	Disable dual programming mode
					1	Enable interrupt level 0 (system control panel interrupt) key
					0	Disable interrupt level 0
					1	Reset interrupt request 0
						All other N codes invalid.
1442	0101					Device address - 1442 RPQ (5)
		0				Must be zero
			000			Feed
			001			Read translate mode
			010			Punch and feed
			011			Read C1 mode
			100			Punch - No feed
				xxxx	x001	Note: All other N codes invalid. Select stacker 2. x indicates "don't care" bits. Any control code combination other than 001 is is invalid and will result in the card going to stacker 1.

Figure 1-7. (Part 2 of 3) Start I/O (SIO) Instruction

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
	1000					Device address BSCA (8)
		0				Must be zero
			000			Control
			001			Receive
			010			Transmit and receive
			011			Receive initial
			100			Auto call
			101			Invalid
			110			Loop test
			111			Invalid
BSCA				1xxx	x	If a 1, bits 1, 2, 3, and 4 of control code are effective.
				0xxx	x	If a 0, bits 1, 2, 3, and 4 of control code are disregarded.
				1		Enable BSCA
				0		Disable BSCA
				1		Enable test mode
				0		Disable test mode
				1		Enable step mode
				0		Disable step mode
					x	Spare (no effect)
					1	Start two second timeout
					0	Cancel two second timeout
					1	Enable interrupt
					0	Disable interrupt
					1	Reset interrupt request
					0	No action
						Note: The control code is effective with every "N" code function except that the start two second timeout must be used only with the control function ("N" = 000).
	0001					Device address - printer keyboard - (1)
		0				Select keyboard
			000			Must be zero — All other N codes invalid
				00xx	0xxx	Must be zero. Zero indicates unused position.
				1		Turn on request pending indicator
				0		Turn off request pending indicator
				1		Turn on proceed indicator
				0		Turn off proceed indicator
5471 Printer Key-board					1	Enable request key interrupts
					0	Disable request key interrupts
					1	Enable data key interrupts
					0	Disable data key interrupts
					1	Reset request or data key interrupts
		1				Select printer
			000			Must be zero — All other N codes invalid
				1		Start print
				0		Don't print
				1		Start carrier return (and index)
				0		Don't carrier return
				1		Force a printer feedback switch response
				1		Force a printer long function switch response
					0	Not used - Must be zero
					1	Enable printer interrupt
					0	Disable printer interrupt
					1	Degate printer magnets
					1	Reset printer interrupt

Figure 1-7. (Part 3 of 3) Start I/O (SIO) Instruction

SENSE INSTRUCTION FORMATS



Note: For explanation of Sense Bytes (2), check individual I/O sections.

(N code 0 is keyboard sense.)

Figure 1-8. Sense I/O (SNS) Instruction Format

5410 CPU SENSE

Op Code	Q Code DA	M	N	Operand 1		
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	0000			Device address CPU (0)		
		0		Must be zero		
				Low Core Address	High Core Address	
			000	Byte 2 (EB2)	Byte 1 (EB1)	
				0 1 2 3 Address switch 1	0 1 2 3 Address switch 3	
			*	4 5 6 7 Address switch 2	4 5 6 7 Address switch 4	
				xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid

Figure 1-9. 5410 Sense Bytes

5203 PRINTER SENSE

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1110				Device address printer (E)	
		0			Must be zero	
					Low Core Address	**High Core Address**
			000		Byte 2 (EB2) 0 1 2 3 } Left carriage 4 line location 5 6 7	Byte 1 (EB1) 0 1 2 3 } Right carriage 4 line location 5 6 7
			001		0 1 2 3 } Binary amount to 4 be added or sub- 5 tracted to the line 6 printer data address 7 register (LPDAR)	0 1 2 3 } Not printing - contains 4 character in chain counter 5 equal to character at 6 print position 1. 7 Printing - contains character in chain counter indicating character at position being addressed.
			010		0 Left or right carriage emitter 1 Execute print latch 2 Chain emitter SS 3 PSS 1 4 Print time 5 CE sense bit latched 6 HMR unit at extreme left (M1) 7 Home gate	0 Hammer shift clutch 1 Print start SS - emitter pulse 2 Left or right carriage clutch 3 Print cycle 1 4 Print cycle 2 5 Print cycle 3 6 Hammer set latch 7 Hammer bar right
			011		0 Carriage sync check 1 Carriage space check 2 Forms jam check 3 Incrementer failure check 4 CE sense bit latched 5 Hammer echo check 6 Any hammer on check 7 No op	0 Chain sync check 1 Incrementer sync check 2 Hammer unit thermal check 3 } Not used 4 } 5 48 character chain installed 6 Unprintable character 7 CE sense bit
			100		0 1 2 3 } LPIAR - Hi 4 5 6 7	0 1 2 3 } LPIAR - Lo 4 5 6 7
			101		Invalid	
			110		0 1 2 3 } LPDAR - Hi 4 5 6 7	0 1 2 3 } LPDAR - Lo 4 5 6 7
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destinations)	

Figure 1-10. 5203 Printer Sense Bytes

5424 MFCU SENSE

Op Code 0 7	Q Code DA 8 11	M 12	N 13 15	Operand 1 16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1111			Device address for MFCU (F)		
		0		Must be zero		
					Low Core Address	**High Core Address**
			000		Byte 2 (EB2)	Byte 1 (EB1)
					0 Punch CB	0 Hopper 1 or 2 magnet
					1 Punch strobe	1 Hopper cell covered
					2 Punch magnet one	2 Gear count 1, 3, 5, 7, 9, 11
					3 Ind 1 Byte 2 bit 3 (spare)	3 Read cell one exposed
					4 Print time	4 Read cell 18 exposed
					5 Print fire CB	5 Allow read
					6 Print magnet 1 (A1) 9(A2)	6 Hopper CB
					7 Ind 1 Byte 2 Bit 7 (spare)	7 Ind 1 Byte 1 Bit 7 (spare)
			001		0 Corner kick magnet	0 Punch registration roll 1 or 2
					1 Print stepper clutch magnet	1 Prepunch cell covered
					2 Post-print cell covered	2 Punch gate magnet
					3 Print inject CB	3 Punch eject roll magnet
					4 Print kick CB	4 Punch stepper roll magnet
					5 Print stepped CB	5 Corner cell covered
					6 Print allow, punch execute	6 Punch stepper CB
					7 Ind 2 Byte 2 Bit 7 (spare)	7 Ind 2 Byte 1 Bit 7 (spare)
			011		0 Print buffer 1 busy	0 Read check
					1 Print buffer 2 busy	1 Punch check
					2 Card in wait 1	2 Punch invalid
					3 Card in wait 2	3 Print data check
					4 Reserved	4 Print clutch check
					5 Hopper cycle not complete	5 Hopper check
					6 Card in transport counter bit 2	6 Feed check
					7 Card in transport counter bit 1	7 No-op
			010		Invalid	Stores register contents at operand address 1 and operand address 1 minus one.
			100		MFCU print address register	
			101		MFCU read address register	
			110		MFCU punch address register	
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destination)	

Figure 1-11. 5424 MFCU Sense Bytes

B10

5444 FILE SENSE

Op Code	Q Code			Operand 1		
0 7	DA 8 11	M 12	N 13 15	16		
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte Indexed by XR-2		
	1010				Device address disk drive 1 (A)	
	1011				Device address disk drive 2 (B)	
		0			Removable disk	
		1			Fixed disk	
					Low Core Address	**High Core Address**
					Byte 2 (EB2)	Byte 1 (EB1)
			000		Invalid	
			001		Invalid	
			010		0 No-op	0 Scan equal hit
					1 Invervention required	1 Cylinder zero
					2 Missing address marker	2 End of cylinder
					3 Equipment check	3 Seek busy
					4 Data check	4 100 cylinder
					5 No record found	5 Overrun
					6 Track condition check	6 Reserved
					7 Seek check	7 Disk drive 2 sel
			011		0 Unsafe	0 Reserved
					1 TAP line A	1 Jumperable CE bit
					2 TAP line B	2 Jumperable CE bit
					3 TAP line C	3 Not bit ring inhibit
					4 Index	4 Standard write trigger
					5 Head settling	5 Condition priority request
					6 Jumperable CE bit	6 Bit ring 0
					7 Reserved	7 Not CC reg position 17
			100		DFDR	
			101		Invalid	
			110		DFCR	
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destination)	

Figure 1-12. 5444 File Sense Bytes

5475 KEYBOARD SENSE

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes	Direct addressing	Byte 1 = Operand 1 address
70				Operand 1 = 1 byte	Indexed by XR-1	Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte	Indexed by XR-2	
	0001				Device address for keyboard (1)	
		0			Must be zero	

		Low Core Address	High Core Address
001		Byte 2 (EB2)	Byte 1 (EB1)
		0 Data character keyed (EBCDIC)	0 Print switch on
		1	1 Spare
		2	2 Lower shift key
		3	3 Invalid character detected
		4	4 Spare
		5	5 Multipunch interrupt
		6	6 Spare
		7	7 Data key interrupt
010		0 Program 1 key	0 Auto skip/auto dup on
		1 Program 2 key	1 Record erase actuated
		2 Program load switch actuated	2
		3 Release key	3 Program switch on
		4 Field erase key	4 Skip key
		5 Error reset key	5 Dup key
		6 Read key	6 Auto rec rel sw
		7 Right adjust key	7 Functional key interrupt
011		0 Not available	0 Keyboard enable
		1	1 Any function key
		2	2 Bail forward contacts
		3	3 Unlock keyboard signal
		4	4 Bail forward trig
		5	5 Toggle switch latch
		6	6 Any data key
		7	7 CE sense switch
*	xxxx xxxx	Operand address (sense bytes destination)	
		Note: Signal jumpered to A-B2 M2P03	

* Note: All other N codes are invalid.

Figure 1-13. 5475 Keyboard Sense Bytes

SIOC SENSE

Op Code	Q Code			Operand 1			
	DA	M	N				
0 7	8 11	12	13 15	16			
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address -1	
B0				Operand 1 = 1 byte Indexed by XR-2			
	0011				Device address SIOC (3)		
		0			Must be zero		
						Low Core Address	High Core Address
					Byte 2 (EB2)		Byte 1 (EB1)
			000		Invalid		
			001		0	Write mode set service response	Diag mode
					1	Reset service response after 6 msec	Spare
					2	Transfer line 2 EOT	Latch trans line 4
					3	Transfer line 1 EOT	Latch trans line 3
					4	Odd parity	Latch trans line 1
					5	Decrement DAR	Trans line 3 reset disc latch
					6	Latch I/O 1 select	Reset disc latch after 6 msec
					7	Slave (trans line 6 & 7 latch)	Trans line 5 reset disc latch
			010		0	Spare	0
					1	End request	1
					2	Interrupt pending	2
					3	I/O attention	3
					4	Data trans reg parity check	4
					5	No-op latch	5
					6	LCR overflow	6
					7	I/O ready	7
							Length count register
			011		0	I/O ID bit 8	I/O trans line 8
					1	I/O ID bit 4	I/O trans line 7
					2	I/O ID bit 2	I/O trans line 6
					3	I/O ID bit 1	I/O trans line 5
					4	I/O device attached	I/O trans line 4
					5	I/O transfer line 11	I/O trans line 3
					6	I/O transfer line 10	I/O trans line 2
					7	I/O transfer line 9	I/O trans line 1
			100		0		0
						DAR high	DAR low
					7		7
			101		0	SIOC request latch	0
					1	Service request	1
					2	Service response	2
					3	Interrupt enable	3
					4	I/O disconnect	4
					5	Write cell	5
					6	Read cell	6
					7	I/O selected	7
							Data transfer reg
			110		Invalid		
			111		Invalid		
				xxxx xxxx	Operand address (sense bytes destinations)		

Figure 1-14. SIOC Sense Bytes

5471 CONSOLE I/O SENSE

Op Code 0 7	Q Code DA 8 11	M 12	N 13 15	Operand 1 16		
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1
80				Operand 1 = 1 byte Indexed by XR-2		
	0001				Device address 5471 (1)	
		0			Selects keyboard	
		1			Selects printer	
					Low Core Address	**High Core Address**
			001		Byte 2 (EB2)	Byte 1 (EB1)
					0 Spare	0 Req key int pending
					1 Spare	1 End or cancel int pending
					2 B	2 Cancel key
					3 A	3 End key
					4 8 Card code	4 Return or data key interrupt pending
					5 4	5 Return key
					6 2	6 Keyboard translator check
					7 1	7 Keyboard data check
			011		0 Keyboard mode switch	0 Request key enabled
					1 P	1 Data key enabled
					2 B	2 Strobe switch
					3 A Keyboard	3 Strobe switch sampled
					4 8 code	4 Request-end-cancel key
					5 4	5 Request-end-cancel key sampled
					6 2	6 Keyboard shifting
					7 1	7 Reserved
					Printer (M bit 1)	
			001		0 Enable printer	0 Printer interrupt pending
					1 5.24 msec	1 Reserved
					2 2.68 sec	2 Unprintable character
					3 Cycle FL	3 Printer busy
					4 Reserved	4 End of line
					5 Feedback too late	5 End of form
					6 Extra cycle	6 Print translator check
					7 Cycle too long	7 Printer malfunction
			011		0 Shift mode switch	0 Lower shift required
					1 No print	1 Upper shift required
					2 T2	2 Reserved
					3 T1	3 Feedback switch
					4 R5	4 Feedback switch sampled
					5 R2A	5 Long function switch
					6 R2	6 Long function switch sampled
					7 R1	7 CE SNS bit (active for MST down level at A-B2N2U06)
			*	xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid.

Figure 1-15. 5471 Console I/O Sense Bytes

BSCA SENSE

Op Code 0 7	Q Code DA 8 11	M 12	N 13 15	Operand 1 16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1000				Device address BSCA (8)	
		0			Must be zero	
					Low Core Address	**High Core Address**
					Byte 2 (EB2)	Byte 1 (EB1)
			000		0 Reserved	0 Reserved
					1 Bit time counter 4	1 Reserved
					2 Bit time counter 2	2 Reserved
					3 Bit time counter 1	3 Reserved
					4 Reserved	4 Block cycle steal request (ITB, BCC or VRC check)
					5 Transmit trigger	5 LSR/shift reg parity check
					6 Receive trigger	6 I/O cycle steal overrun
					7 CE SNS bit	7 DBI parity check
			001		Stop address register	
			010		Transition address register	
			011		0 Timeout	0 Reserved
					1 CRC/LRC/VRC	1 Reserved
					2 Adapter check on transmit	2 Reserved
					3 Adapter check on receive	3 Reserved
					4 Invalid ASCII character	4 Reserved
					5 Abortive disconnect	5 Reserved
					6 Disconnect timeout	6 Data set ready
					7 Reserved	7 Data line occupied
			100		Current address register	
			101		Invalid	
			110		0 1 2 3 4 5 6 7 — CRC high (zeros for ASCII)	0 1 2 3 4 5 6 7 — CRC low (LRC for ASCII)
			111		Invalid	
				xxxx xxxx	Operand address (sense byte destination)	

Figure 1-16. BSCA Sense Bytes

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte Indexed by XR-2		
	0101				Device address 1442 (5)	
		0			Must be zero	
					Low Core Address	**High Core Address**
			011		Byte 2 (EB2)	Byte 1 (EB1)
					0 Not assigned	0 Read compare
					1 Not assigned	1 Last card indicator
					2 Not assigned	2 Punch check
					3 Read station jam	3 Data overrun
					4 Hopper misfeed	4 I/O attention
					5 Feed clutch	5 No-op latch
					6 Punch station jam	6 Feed check
					7 Transport jam	7 Invalid card code
			001		0 Not assigned	0 All cells on
					1 Not assigned	1 Read cells 7, 8, 9
					2 Not assigned	2 Read cells 4, 5, 6
					3 Punch incremental drive CB A	3 Read cells 1, 2, 3
					4 Punch CB 2	4 Read cells 12, 11, 0
					5 Punch CB 1	5 Read emitter
					6 Punch incremental drive CB B	6 Feed CB 2, 3, 4
					7 CE diagnostic bit 1	7 Feed CB 1
			010		0 Punch echo 9	0 Punch echo 1
					1 Punch echo 8	1 Punch echo 0
					2 Punch echo 7	2 Punch echo 11
					3 Punch echo 6	3 Punch echo 12
					4 Punch echo 5	4 Punch echo valid
					5 Punch echo 4	5 Not assigned
					6 Punch echo 3	6 Punch cell dark
					7 Punch echo 2	7 CE diagnostic bit 2
			100		Store 1442 DAR	
			*	xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes are invalid.

Figure 1-17. 1442 Sense Bytes

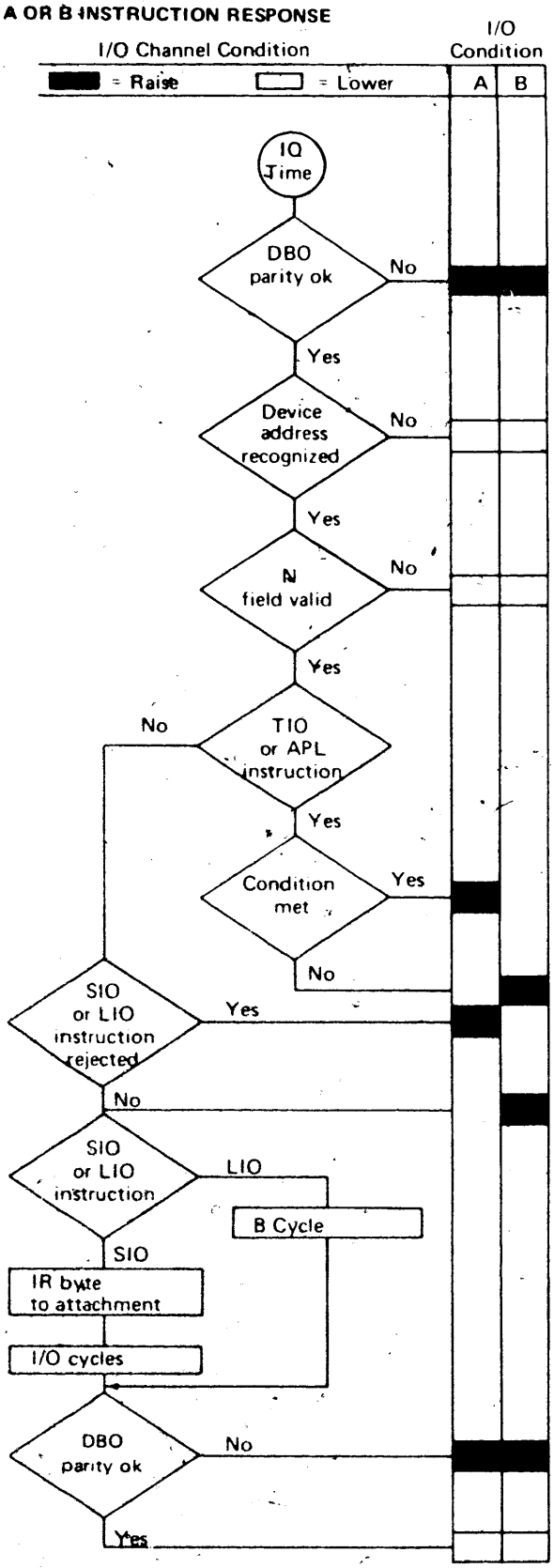


Figure 1-18. I/O Channel Condition A or B Instruction Response

CONDITION REGISTER SETTINGS

Binary Value	8	4	2	1	8	4	2	1
Bits	0	1	2	3	4	5	6	7
Meaning			*BO	Test False	**DO	HI	LO	EQ
DECIMAL								
ADD Decimal			–	–	overflow	> zero	< zero	zero
SUB Decimal			–	–	overflow	> zero	< zero	zero
ZERO & ADD			–	–		> zero	< zero	zero
LOGICAL								
ADD Logical			overflow	–	–	Carry	No Carry	zero
SUB Logical			–	–	–	1>2	1<2	zero
COMPARE			–	–	–	1>2	1<2	EQ
CLI						1>I	1<I	I = I
EDIT (second operand)			–	–	–	> zero	< zero	zero
Test Bits ON			–	Note 1	–	–	–	–
Test Bits OFF			–	Note 2	–	–	–	–
BRANCH ON CONDITION	X		–	Note 3	–	–	–	–

When ONE, branch if any of the tested bits are ON.
When ZERO, branch when all the tested bits are OFF.

*BO = Binary overflow
**DO = Decimal overflow

Notes:
1. Selected bits are not all one.
2. Selected bits are not all zero.
3. Turn off if tested.

Figure 1-19. Condition Register Settings

CONTINUED ON FRAME C01

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0 0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

Figure 1-20. Hexadecimal and Decimal Conversion

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

Figure 1-21. Hexadecimal Addition

C01

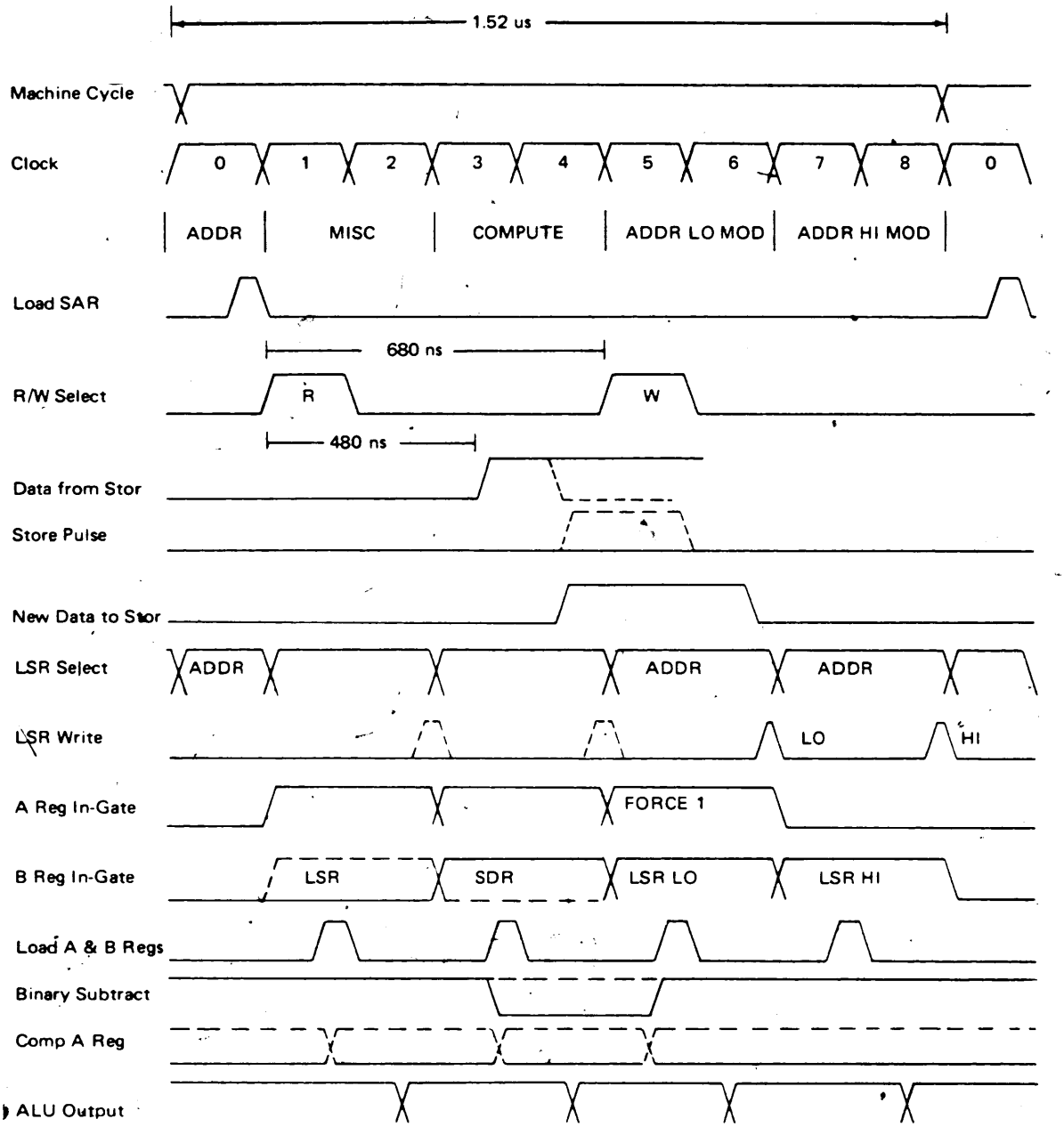


Figure 1-22. CPU Basic Timing

BASE SYSTEM

HIGH	LOW	LSR Acronym
Program level 1 instruction address register		P1-IAR
Program level 1 address recall register		P1-ARR
Operand 2 address register		AAR
Spare		
Program level 1 index register 1		P1-XR1
Length count recall register	Condition recall register	P1-PSR
Operand 1 address register		BAR
MFCU print data address register		MPTAR
Program level 1 index register 2		P1-XR2
Line printer data address register		LPDAR
Line printer image address register		LPIAR
MFCU punch data address register		MPCAR
MFCU read address register		MRDAR
Length count registers	Data recall register	LCR DRR
Interrupt level 1 instruction address register		IAR-1
Interrupt level 1 address recall register		ARR-1

FEATURE 1

HIGH	LOW	LSR Acronym
Program level 2, instruction address register		P2-IAR
Program level 2, address recall register		P2-ARR
Bi-sync comm adapter address register		BSCAR
Serial I/O channel address register		SIAR
Program level 2 status register		P2-PSR
Interrupt level 4, instruction address register		IAR-4
Interrupt level 4, address recall register		ARR-4
Disk file control address register		DFCR
Program level 2 index register 2		P2-XR2
Spare		Spare
Interrupt level 2, instruction address register		IAR-2
Interrupt level 2, address recall register		ARR-2
Disk file data address register		DFDR
Program level 2, index register 1		P2-XR1
Interrupt level 0, instruction address register		IAR-0
Interrupt level 0, address recall register		ARR-0

Figure 1-23. Local Storage Registers

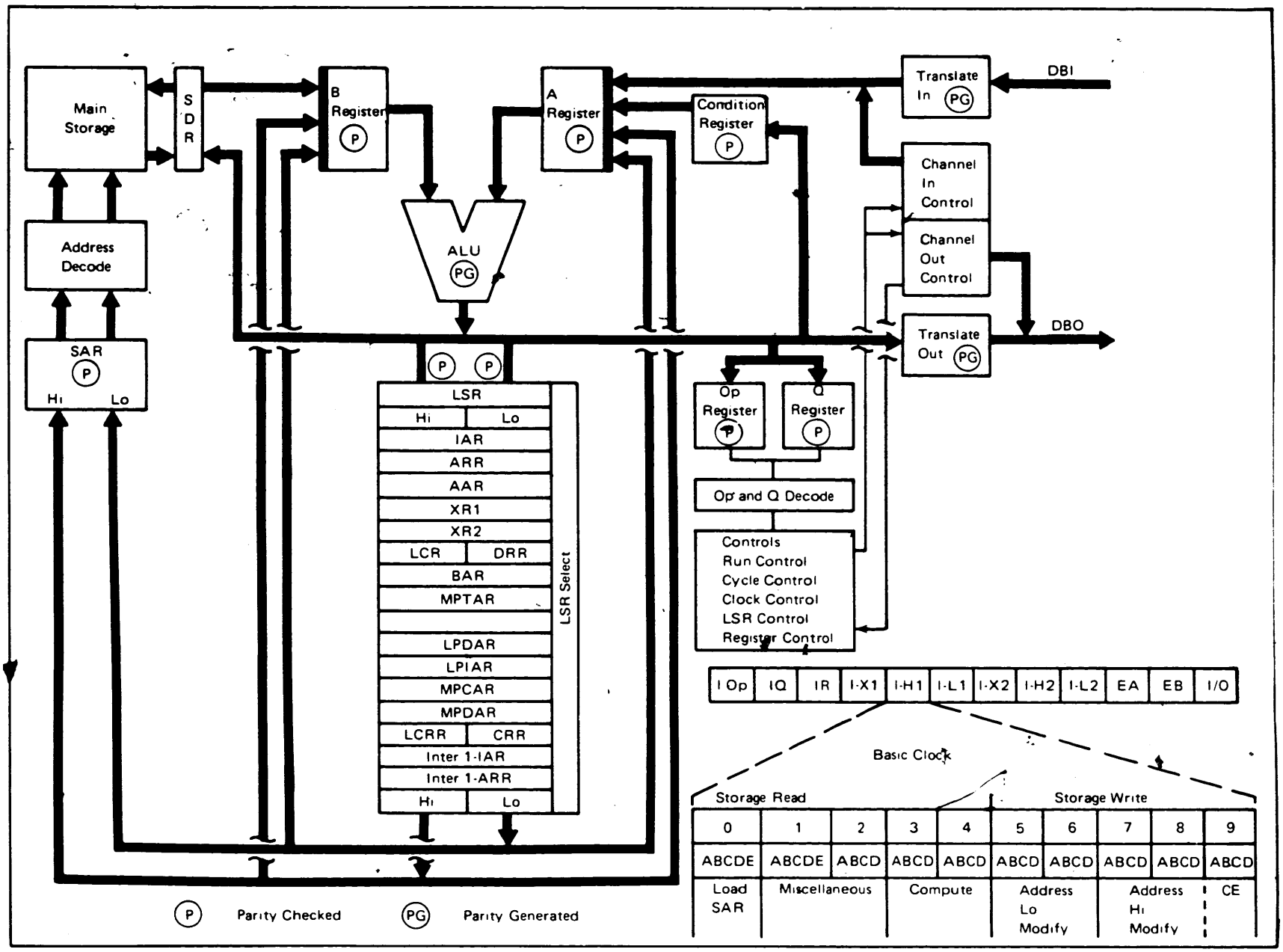
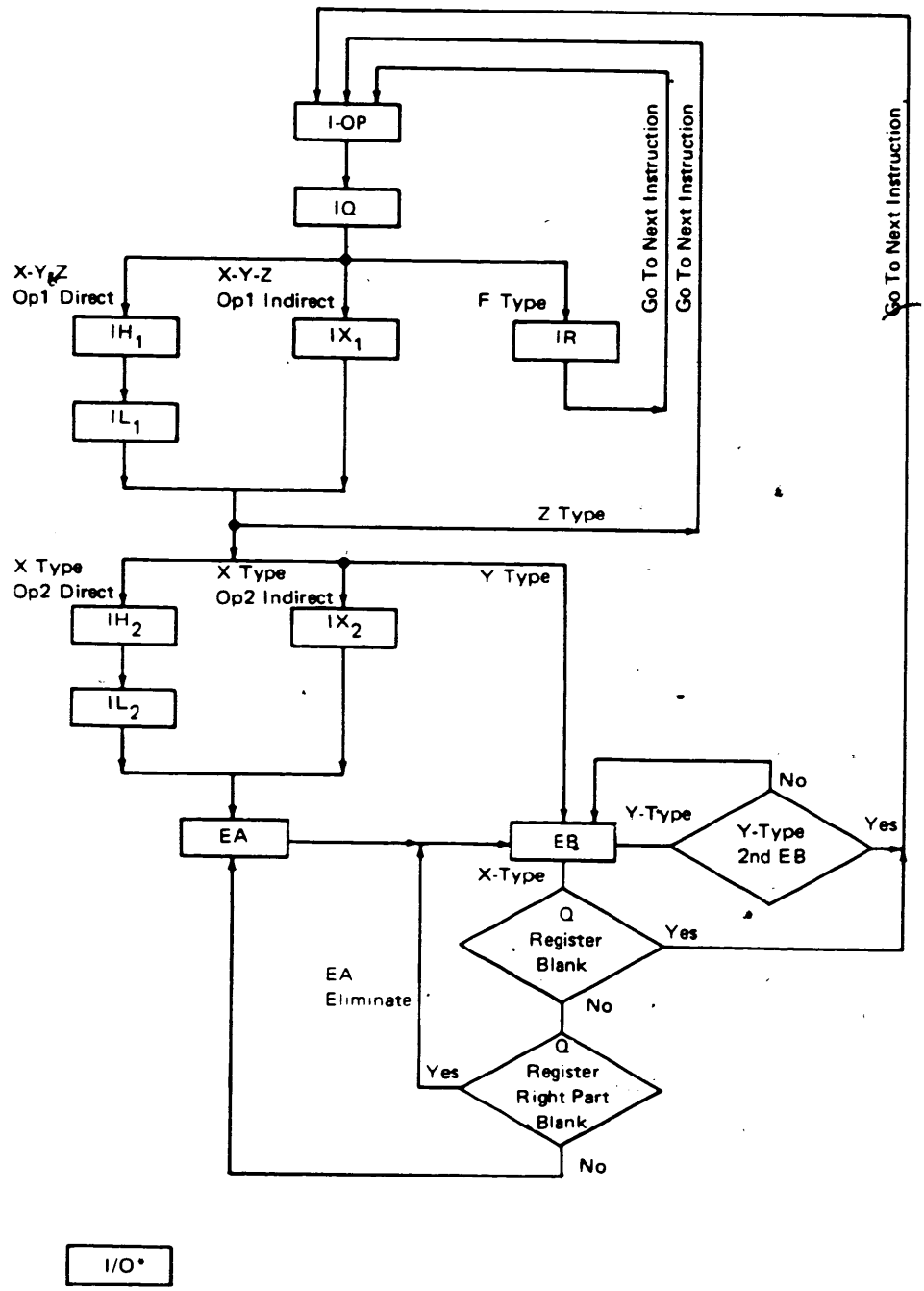


Figure 1-24. CPU Data Flow

C04



* Can be performed between any of the 11 above cycles.

Figure 1-25. CPU Cycle Pattern

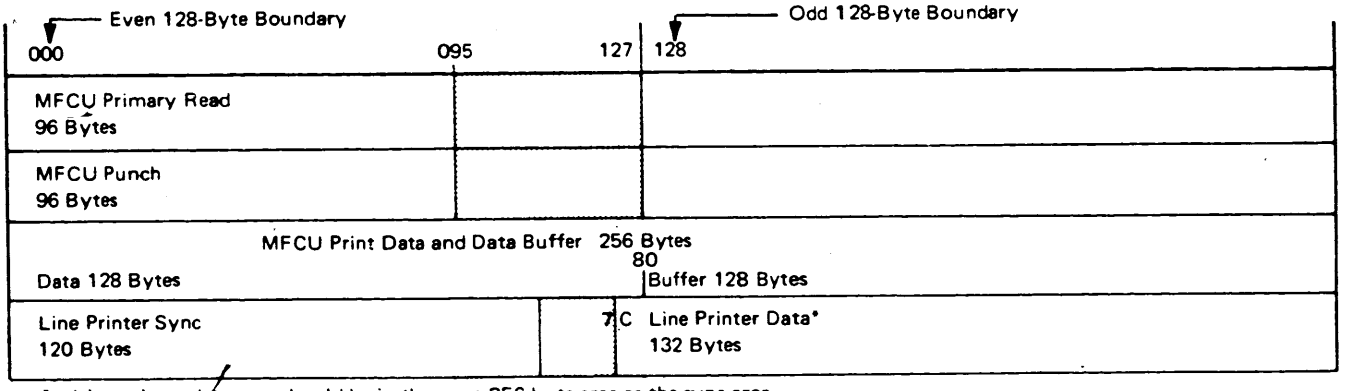
C05

Bit Position	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	6	7	0	1	2	3	4	5	6	7
Function	Zone				Digit				Zone				Digit				Zone				Digit				Zone		Digit		Sign*				Digit			
																													Low-Order Byte							

• Sign Configurations:		
Binary	Hexadecimal	Function
1010	A	Alternate Plus
1011	B	ASCII-8 Minus
1100	C	Alternate Plus
1101	D	Standard Minus
1110	E	Alternate Plus
1111	F	Standard Plus

Figure 1-26. Decimal Data Storage and Sign Control

A. Fixed Length Areas



* Line printer data area should be in the same 256 byte area as the sync area.

Indicates parts of I/O areas not used by the I/O devices.

IMAGE DATA
Line Printer must be XX00 and YY7C

Figure 1-27. I/O Storage Requirements

C06

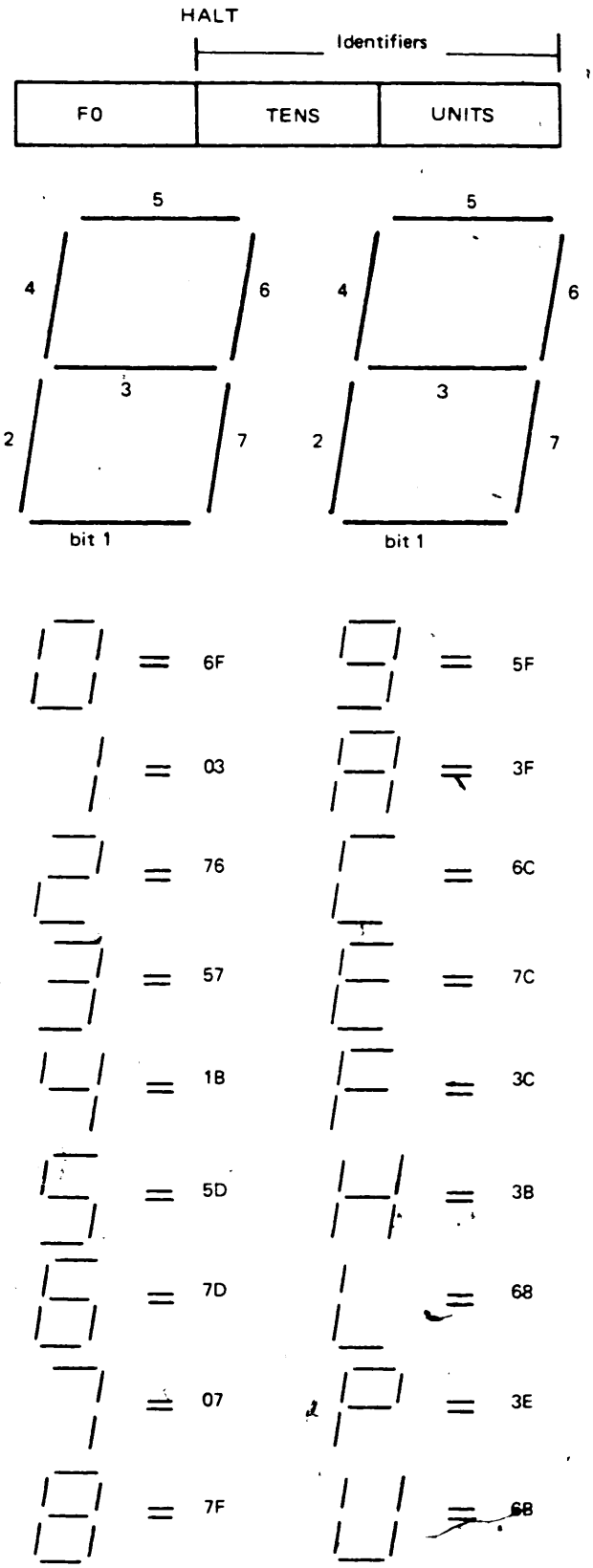


Figure 1-28. Halt Indicators

C07

LOGIC PAGE PREFIXES

Prefix-FEALD	Circuits
AI	Card socket listing
AV	ALU
CR	Use meter control
FG	MFCU box
GC	Printer keyboard controls
GK	Keyboard service
KA	25 MHz oscillator
KB	Display and check
KC	Clock controls
KD	Cycle controls
KE	Channel in
KG	Register controls
KL	Base LSR controls
KM	Interrupt 1 to 4
KY	ALU controls
MA	Base LSR and SAR low
MC	Data bus out—bank 2
MD	In phase terminated TLD's
MO	Socket listing
MM	Main storage
PA	CE mode and toggle switches
PB	Drum indicators
PC	Display selector drum
RA	A and B registers
RN	Op and Q registers
WA	Cable page
WB	Channel 1 out exit lines
WS	CPU to storage lines
YB	Printer box
YB	Voltage service
A1	Socket listing
FB	MFCU controls
FC	DBO and command control (MFCU)
FD	DBI and MFCU data registers
FE	Power drivers
WM	MFCU box
WP	Channel and attachment interface (printer)
WN	Channel and attachment interface (MFCU)
FP	Printer controls

Figure 1-29. FEALD Page Prefixes

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
000	00	DC		4	1	00000000	
001	01	DCBA 1		A @	A 3	00000001	
002	02	DCBA 2		B @	B 3	00000010	
003	03	DCBA 21		C @	C 3	00000011	
004	04	DCBA 4	ZAZ	D @	D 3	00000100	
005	05	DCBA 4 1		E @	E 3	00000101	
006	06	DCBA 42	AZ	F @	F 3	00000110	
007	07	DCBA 421	SZ	G @	G 3	00000111	
008	08	DCBA8	MVX	H @	H 3	00001000	
009	09	DCBA8 1		I @	I 3	00001001	
010	0A	CBA8 2	ED	¢ 4	¢ 1	00001010	
011	0B	CBA8 21	ITC	. 4	. 1	00001011	
012	0C	CBA84	MVC	< 4	< 1	00001100	
013	0D	CBA84 1	CLC	(4	(1	00001101	
014	0E	CBA842	ALC	+ 4	+ 1	00001110	
015	0F	CBA8421	SLC	I 4	I 1	00001111	
016	10	C A8 2		& 4	& 1	00010000	
017	11	DCB 1		J @	J 3	00010001	
018	12	DCB 2		K @	K 3	00010010	
019	13	DCB 21		L @	L 3	00010011	
020	14	DCB 4	ZAZ	M @	M 3	00010100	
021	15	DCB 4 1		N @	N 3	00010101	
022	16	DCB 42	AZ	O @	O 3	00010110	
023	17	DCB 421	SZ	P @	P 3	00010111	
024	18	DCB 8	MVX	Q @	Q 3	00011000	
025	19	DCB 8 1		R @	R 3	00011001	
026	1A	CB 8 2	ED	! 4	! 1	00011010	
027	1B	CB 8 21	ITC	$ 4	$ 1	00011011	
028	1C	CB 84	MVC	* 4	* 1	00011100	
029	1D	CB 84 1	CLC	) 4	) 1	00011101	
030	1E	CB 842	ALC	; 4	; 1	00011110	
031	1F	CB 8421	SLC	¬ 4	¬ 1	00011111	
032	20	CB		- 4	- 1	00100000	
033	21	C A 1		/ 4	/ 1	00100001	
034	22	DC A 2		S @	S 3	00100010	
035	23	DC A 21		T @	T 3	00100011	
036	24	DC A 4	ZAZ	U @	U 3	00100100	
037	25	DC A 4 1		V @	V 3	00100101	
038	26	DC A 42	AZ	W @	W 3	00100110	
039	27	DC A 421	SZ	X @	X 3	00100111	
040	28	DC A8	MVX	Y @	Y 3	00101000	
041	29	DC A8 1		Z @	Z 3	00101001	
042	2A	DCBA	ED	} @	} 3	00101010	
043	2B	C A8 21	ITC	. 4	. 1	00101011	
044	2C	C A84	MVC	% 4	% 1	00101100	
045	2D	C A84 1	CLC	_ 4	_ 1	00101101	
046	2E	C A842	ALC	> 4	> 1	00101110	
047	2F	C A8421	SLC	? 4	? 1	00101111	
048	30	DC A	SNS	0 @	0 3	00110000	
049	31	DC 1	LIO	1 @	1 3	00110001	
050	32	DC 2		2 @	2 3	00110010	
051	33	DC 21		3 @	3 3	00110011	
052	34	DC 4	ST	4 @	4 3	00110100	
053	35	DC 4 1	L	5 @	5 3	00110101	
054	36	DC 42	A	6 @	6 3	00110110	
055	37	DC 421		7 @	7 3	00110111	
056	38	DC 8	TBN	8 @	8 3	00111000	
057	39	DC 8 1	TBF	9 @	9 3	00111001	
058	3A	C 8 2	SBN	: 4	: 1	00111010	
059	3B	C 8 21	SBF	# 4	# 1	00111011	
060	3C	C 84	MVI	@ 4	@ 1	00111100	
061	3D	C 84 1	CLI	' 4	' 1	00111101	
062	3E	C 842		= 4	= 1	00111110	
063	3F	C 8421		" 4	" 1	00111111	
064	40	None				01000000	Space
065	41	D BA 1		A 8	A 2	01000001	
066	42	D BA 2		B 8	B 2	01000010	
067	43	D BA 21		C 8	C 2	01000011	
068	44	D BA 4	ZAZ	D 8	D 2	01000100	
069	45	D BA 4 1		E 8	E 2	01000101	
070	46	D BA 42	AZ	F 8	F 2	01000110	
071	47	D BA 421	SZ	G 8	G 2	01000111	
072	48	D BA8	MVX	H 8	H 2	01001000	
073	49	D BA8 1		I 8	I 2	01001001	
074	4A	BA8 2	ED	¢	¢	01001010	¢
075	4B	BA8 21	ITC	.	.	01001011	.
076	4C	BA84	MVC	<	<	01001100	<
077	4D	BA84 1	CLC	(	(	01001101	(
078	4E	BA842	ALC	+	+	01001110	+
079	4F	BA8421	SLC	I	I	01001111	I
080	50	A8 2		&	&	01010000	&
081	51	D B 1		J 8	J 2	01010001	
082	52	D B 2		K 8	K 2	01010010	
083	53	D B 21		L 8	L 2	01010011	
084	54	D B 4	ZAZ	M 8	M 2	01010100	
085	55	D B 4 1		N 8	N 2	01010101	
086	56	D B 42	AZ	O 8	O 2	01010110	
087	57	D B 421	SZ	P 8	P 2	01010111	
088	58	D B 8	MVX	Q 8	Q 2	01011000	
089	59	D B 8 1		R 8	R 2	01011001	
090	5A	B 8 2	ED	!	!	01011010	!
091	5B	B 8 21	ITC	$	$	01011011	$
092	5C	B 84	MVC	*	*	01011100	*
093	5D	B 84 1	CLC	)	)	01011101	)
094	5E	B 842	ALC	;	;	01011110	;
095	5F	B 8421	SLC	¬	¬	01011111	¬

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

Figure 1-30. (Part 1 of 3) Code Conversion Chart

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
096	60	B		-	-	01100000	-
097	61	A 1		/	/	01100001	/
098	62	D A 2		S 8	S 2	01100010	
099	63	D A 21		T 8	T 2	01100011	
100	64	D A 4	ZAZ	U 8	U 2	01100100	
101	65	D A 4 1		V 8	V 2	01100101	
102	66	D A 42	AZ	W 8	W 2	01100110	
103	67	D A 421	SZ	X 8	X 2	01100111	
104	68	D A8	MVX	Y 8	Y 2	01101000	
105	69	D A8 1		Z 8	Z 2	01101001	
106	6A	D BA8 2	ED	} 8	} 2	01101010	
107	6B	A8 21	ITC	.	.	01101011	.
108	6C	A84	MVC	%	%	01101100	%
109	6D	A84 1	CLC	_	_	01101101	
110	6E	A842	ALC	>	>	01101110	>
111	6F	A8421	SLC	?	?	01101111	?
112	70	D A	SNS	0 8	0 2	01110000	
113	71	D 1	LIO	1 8	1 2	01110001	
114	72	D 2		2 8	2 2	01110010	
115	73	D 21		3 8	3 2	01110011	
116	74	D 4	ST	4 8	4 2	01110100	
117	75	D 4 1	L	5 8	5 2	01110101	
118	76	D 42	A	6 8	6 2	01110110	
119	77	D 421		7 8	7 2	01110111	
120	78	D 8	TBN	8 8	8 2	01111000	
121	79	D 8 1	TBF	9 8	9 2	01111001	
122	7A	8 2	SBN			01111010	
123	7B	8 21	SBF	#	#	01111011	#
124	7C	84	MVI	@	@	01111100	@
125	7D	84 1	CLI	'	'	01111101	'
126	7E	842				01111110	=
127	7F	8421		"	"	01111111	"
128	80	DC		@	3	10000000	
129	81	CBA 1		A 4	A 1	10000001	
130	82	CBA 2		B 4	B 1	10000010	
131	83	CBA 21		C 4	C 1	10000011	
132	84	CBA 4	ZAZ	D 4	D 1	10000100	
133	85	CBA 4 1		E 4	E 1	10000101	
134	86	CBA 42	AZ	F 4	F 1	10000110	
135	87	CBA 421	SZ	G 4	G 1	10000111	
136	88	CBA8	MVX	H 4	H 1	10001000	
137	89	CBA8 1		I 4	I 1	10001001	
138	8A	DCBA8 2	ED	c @	c 3	10001010	
139	8B	DCBA8 21	ITC	. @	. 3	10001011	
140	8C	DCBA84	MVC	< @	< 3	10001100	
141	8D	DCBA84 1	CLC	(@	(3	10001101	
142	8E	DCBA842	ALC	+ @	+ 3	10001110	
143	8F	DCBA8421	SLC	I @	I 3	10001111	
144	90	CBA		} 4	} 1	10010000	
145	91	CB 1		J 4	J 1	10010001	
146	92	CB 2		K 4	K 1	10010010	
147	93	CB 21		L 4	L 1	10010011	
148	94	CB 4	ZAZ	M 4	M 1	10010100	
149	95	CB 4 1		N 4	N 1	10010101	
150	96	CB 42	AZ	O 4	O 1	10010110	
151	97	CB 421	SZ	P 4	P 1	10010111	
152	98	CB 8	MVX	Q 4	Q 1	10011000	
153	99	CB 8 1		I 4	I 1	10011001	
154	9A	DCB 8 2	ED	! @	! 3	10011010	
155	9B	DCB 8 21	ITC	$ @	$ 3	10011011	
156	9C	DCB 84	MVC	* @	* 3	10011100	
157	9D	DCB 84 1	CLC	) @	) 3	10011101	
158	9E	DCB 842	ALC	; @	; 3	10011110	
159	9F	DCB 8421	SLC	@	3	10011111	
160	A0	DCB		- @	- 3	10100000	
161	A1	DC A 1		/ @	/ 3	10100001	
162	A2	C A 2		S 4	S 1	10100010	
163	A3	C A 21		T 4	T 1	10100011	
164	A4	C A 4	ZAZ	U 4	U 1	10100100	
165	A5	C A 4 1		V 4	V 1	10100101	
166	A6	C A 42	AZ	W 4	W 1	10100110	
167	A7	C A 421	SZ	X 4	X 1	10100111	
168	A8	C A8	MVX	Y 4	Y 1	10101000	
169	A9	C A8 1		Z 4	Z 1	10101001	
170	AA	DC A8 2	ED	& @	& 3	10101010	
171	AB	DC A8 21	ITC	. @	. 3	10101011	
172	AC	DC A84	MVC	% @	% 3	10101100	
173	AD	DC A84 1	CLC	@	3	10101101	
174	AE	DC A842	ALC	> @	> 3	10101110	
175	AF	DC A8421	SLC	? @	? 3	10101111	
176	B0	C A	SNS	0 4	0 1	10110000	
177	B1	C 1	LIO	1 4	1 1	10110001	
178	B2	C 2		2 4	2 1	10110010	
179	B3	C 21		3 4	3 1	10110011	
180	B4	C 4	ST	4 4	4 1	10110100	
181	B5	C 4 1	L	5 4	5 1	10110101	
182	B6	C 42	A	6 4	6 1	10110110	
183	B7	C 421		7 4	7 1	10110111	
184	B8	C 8	TBN	8 4	8 1	10111000	
185	B9	C 8 1	TBF	9 4	9 1	10111001	
186	BA	DC 8 2	SBN	@	3	10111010	
187	BB	DC 8 21	SBF	# @	# 3	10111011	
188	BC	DC 84	MVI	@ @	@ 3	10111100	
189	BD	DC 84 1	CLI	' @	' 3	10111101	
190	BE	DC 842		= @	= 3	10111110	
191	BF	DC 8421		" @	" 3	10111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

Figure 1-30. (Part 2 of 3) Code Conversion Chart

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
192	C0	D	BC	8	2	11000000	
193	C1	BA 1	TIO	A	A	11000001	A
194	C2	BA 2	LA	B	B	11000010	B
195	C3	BA 21		C	C	11000011	C
196	C4	BA 4		D	D	11000100	D
197	C5	BA 4 1		E	E	11000101	E
198	C6	BA 42		F	F	11000110	F
199	C7	BA 421		G	G	11000111	G
200	C8	BA8		H	H	11001000	H
201	C9	BA8 1		I	I	11001001	I
202	CA	D BA8 2		Ç 8	Ç 2	11001010	
203	CB	D BA8 21		8	2	11001011	
204	CC	D BA84		< 8	< 2	11001100	
205	CD	D BA84 1		(8	(2	11001101	
206	CE	D BA842		+ 8	+ 2	11001110	
207	CF	D BA8421		! 8	! 2	11001111	
208	D0	BA	BC	}	}	11010000	}
209	D1	B 1	TIO	J	J	11010001	J
210	D2	B 2	LA	K	K	11010010	K
211	D3	B 21		L	L	11010011	L
212	D4	B 4		M	M	11010100	M
213	D5	B 4 1		N	N	11010101	N
214	D6	B 42		O	O	11010110	O
215	D7	B 421		P	P	11010111	P
216	D8	B 8		Q	Q	11011000	Q
217	D9	B 8 1		R	R	11011001	R
218	DA	D B 8 2		! 8	! 2	11011010	
219	DB	D B 8 21		$ 8	$ 2	11011011	
220	DC	D B 84		* 8	* 2	11011100	
221	DD	D B 84 1		) 8	) 2	11011101	
222	DE	D B 842		; 8	; 2	11011110	
223	DF	D B 8421		¬ 8	¬ 2	11011111	

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
224	E0	D B	BC	8	2	11100000	
225	E1	D A 1	TIO	/ 8	/ 2	11100001	
226	E2	A 2	LA	S	S	11100010	S
227	E3	A 21		T	T	11100011	T
228	E4	A 4		U	U	11100100	U
229	E5	A 4 1		V	V	11100101	V
230	E6	A 42		W	W	11100110	W
231	E7	A 421		X	X	11100111	X
232	E8	A8		Y	Y	11101000	Y
233	E9	A8 1		Z	Z	11101001	Z
234	EA	D A8 2		& 8	& 2	11101010	
235	EB	D A8 21		, 8	, 2	11101011	
236	EC	D A84		% 8	% 2	11101100	
237	ED	D A84 1		_ 8	_ 2	11101101	
238	EE	D A842		> 8	> 2	11101110	
239	EF	D A8421		? 8	? 2	11101111	
240	F0	A	HPL	0	0	11110000	0
241	F1	1	APL	1	1	11110001	1
242	F2	2	JC	2	2	11110010	2
243	F3	21	SIO	3	3	11110011	3
244	F4	4		4	4	11110100	4
245	F5	4 1		5	5	11110101	5
246	F6	42		6	6	11110110	6
247	F7	421		7	7	11110111	7
248	F8	8		8	8	11111000	8
249	F9	8 1		9	9	11111001	9
250	FA	D 8 2		8	2	11111010	
251	FB	D 8 21		# 8	# 2	11111011	
252	FC	D 84		@ 8	@ 2	11111100	
253	FD	D 84 1		' 8	' 2	11111101	
254	FE	D 842		= 8	= 2	11111110	
255	FF	D 8421		" 8	" 2	11111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

*Tier 3 character addition table

Tier 3 card bits required by tier 1 character \ Tier 3 card bits required by tier 2 character		1	2	3 (1+2 bits)
		1	2	3 (1+2 bits)
4		5 (4+1 bits)	6 (4+2 bits)	7 (4+2+1 bits)
8		9 (8+1 bits)	: (8+2 bits)	# (8+2+1 bits)
@ (4+8 bits)		' (8+4+1 bits)	= (8+4+2 bits)	" (8+4+2+1 bits)

Figure 1-30. (Part 3 of 3) Code Conversion Chart

CONSOLE AND MAINTENANCE FACILITIES

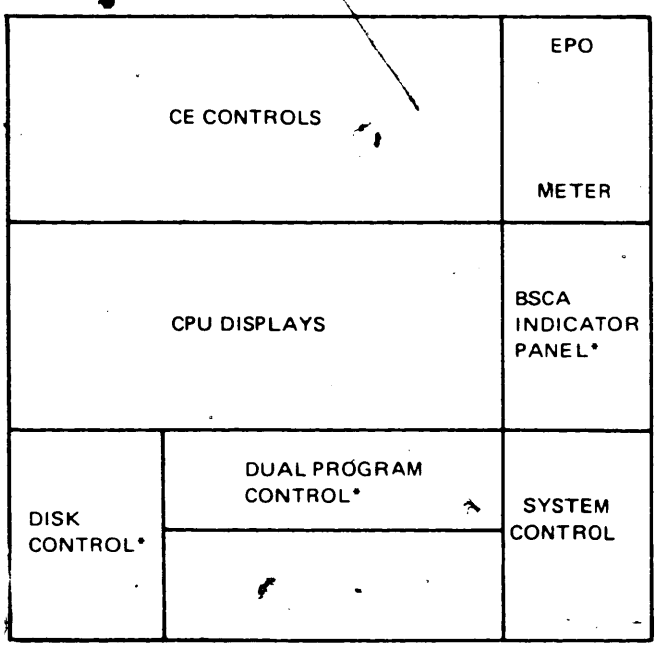
C12

Section 1. Basic Unit

2.1 SYSTEM CONTROL PANEL

System controls are divided into three sections: operator controls, customer engineering (CE) controls, and console display. The operator section contains controls for normal programmed system operation. The CE controls serve as diagnostic aids in locating hardware and programming malfunctions. The console display shows the operator and the CE the contents of the various registers in the CPU and the status of the major CPU controls.

Manual branching can be performed through the console switches, but first the CPU must be ready to start a new operation. The system control panel (Figure 2-1) contains the switches and lights required to operate and control the system.



* See Section 2. "Features"

Figure 2-1. System Control Panel

2.1.1 Operator Controls

2.1.1.1 Emergency Power-Off Switch (EPO)

Pulling this switch (Figure 2-2) turns off all power beyond the power-entry terminal on every unit that is part of the system or any unit connected to the system. The switch latches out and when it is in this position, the power on/off switch is ineffective.

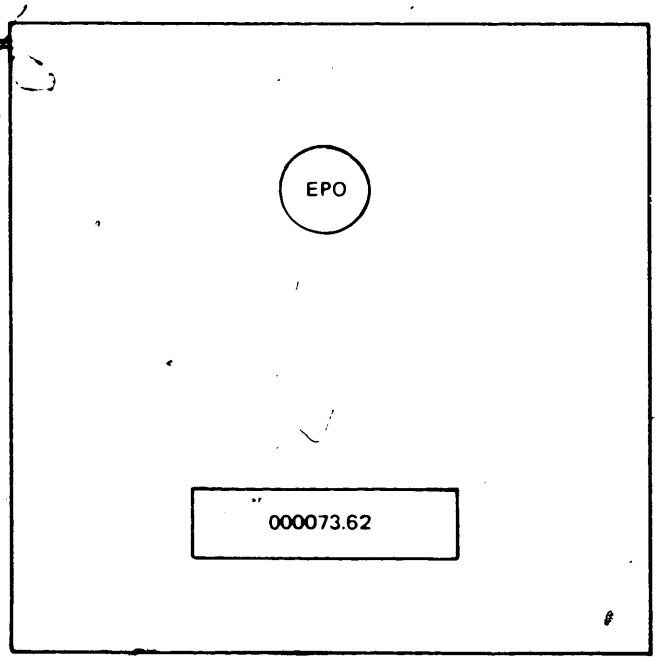


Figure 2-2. Emergency Power-Off Pull Switch

2.1.1.2 Usage Meter

The customer usage meter records system operating time. Recorded time starts when you press the start key or the load key and ends when the job is completed.

However, when operating in one of the step modes, the meter runs for 400 us. each time the start key is pressed.

Time is not recorded if one of the following conditions exists:

- Manual or programmed halt stops processing unit. (However, time is recorded when I/O operations are being performed during a programmed halt.)
- A processor check occurs.
- Power is lost.
- The CE key switch is turned off for system servicing.

2.1.1.3 Message Display Unit

This two-position message display unit (Figure 2-3) keeps a running display of the halt identifier portion of a halt instruction.

2.1.1.4 Processor Check Light

This light (Figure 2-3) is turned on when:

- An invalid op code, an invalid address, or a parity error is detected in the CPU.
- The device address (including the M field) and the N field of an I/O instruction is not recognized.
- The I/O device recognizes a parity error on data bus out at the I/O attachment.
- The immediate I/O error stop is on and an I/O error occurs.

This light is turned off when a system reset occurs or when the CE check-reset key is activated.

The processor stops on any of the above errors, and I/O data may be lost. The console display (2.1.3) shows the error. Following a processor check, use the program load procedure for a normal restart.

2.1.1.5 I/O Attention Light

The I/O attention light (Figure 2-3 Fr. C15 comes on when an addressed I/O device requires normal operator intervention. Normal operator intervention includes:

- Printer--Forms out, cover interlock.
- MFCU--Hopper empty, stacker full, chip box full, cover interlock.

The light goes off when the operator has intervened and returned the device to the ready state. I/O attention does not stop normal CPU processing. However, start I/O or load I/O instructions are not accepted.

2.1.1.6 Power On/Off Switch

This switch (Figure 2-3 Fr. C15 initiates the power on/off sequence of the system. As part of the power on/off sequence, a system reset is performed so that no I/O operations take place until they are specifically directed. The contents of main storage are not guaranteed after power on/off sequence.

Note: A power check occurs if the power on/off switch is turned on before a normal system power off sequence is completed.

2.1.1.7 Program Load Key

This key (Figure 2-3 Fr. C15 is used for initial program loading. As part of the program load sequence, a system reset is performed. Pressing the program load key allows the first record from the I/O device (normally the MFCU primary hopper) to be read and stored in main storage, beginning at location 0000. When the key is released, the CPU executes the instruction sequence starting at location 0000.

The console I/O attention light comes on when the program load key is activated if the I/O device is in a not ready state. To complete the program load function, the device must be readied.

2.1.1.8 Stop Key/Light

Pressing this key (Figure 2-3 Fr. C15 stops the processor at the end of the operation being performed. I/O transfers are completed without losing information. The stop light comes on to indicate processor stop. The processor may be restarted without loss of information by pressing the start key.

2.1.1.9 Start Key

Pressing the start key (Figure 2-3) takes the processor out of its stopped state, turns off the stop light, and allows the processor to continue. In the CE mode of operation the start key is also used to start the processor clock and then sequentially advance it.

2.1.1.10 Power Check Light

This light comes on when a machine power supply malfunctions or when a thermal condition exists. This light also comes on during a power up sequence and remains on until the sequence is completed.

For additional information refer to section 5.8. Fr C03, 1-2

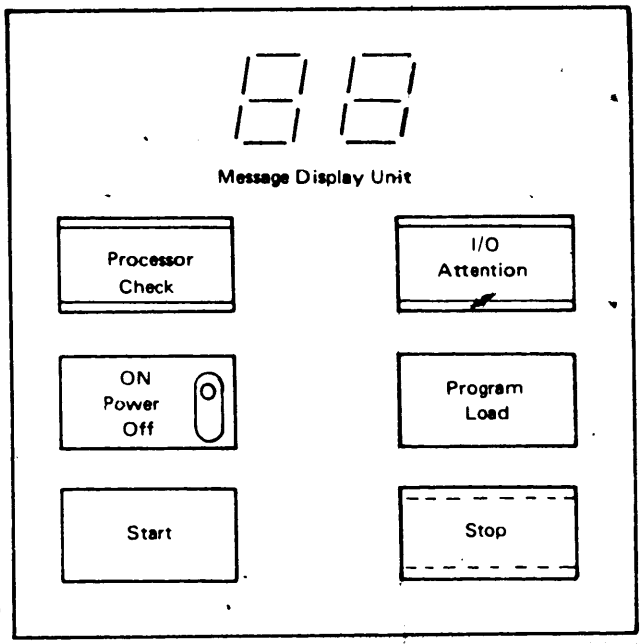


Figure 2-3. System Controls

2.1.1.11 Thermal Light

The thermal light and the power check light (Figure 2-4) Fr. C16 come on when overheating occurs in the CPU mainframe. Turning off the power On/Off switch turns off the power check light. The thermal light remains on until the thermal condition is removed. Then the normal power on sequence can be performed.

2.1.1.12 Lamp Switch

This switch turns on all system lights so that you can check for burned out lights.

2.1.2 CE Controls

2.1.2.1 Address/Data Switches

These four switches (Figure 2-4) Fr. C16 set up addresses or data. An address (16 bits) is loaded into the storage address register (SAR).

Data can now be entered into main storage—8 bits when operating in test mode or 16 bits via a program.

Once a program level has been halted, the halt must be reset before an instruction can be properly executed in a specific program level. The halt can be reset by pressing the system reset key or the start key. (On machines with the dual program feature, press the halt reset key to reset the halt condition.)

2.1.2.2 CE Key Switch

This switch (Figure 2-5), Fr. C17 when in the CE position, stops the usage meter from recording processor time while the CE services the equipment.

If this switch is turned off while the CPU is running, a processor check can occur.

C15

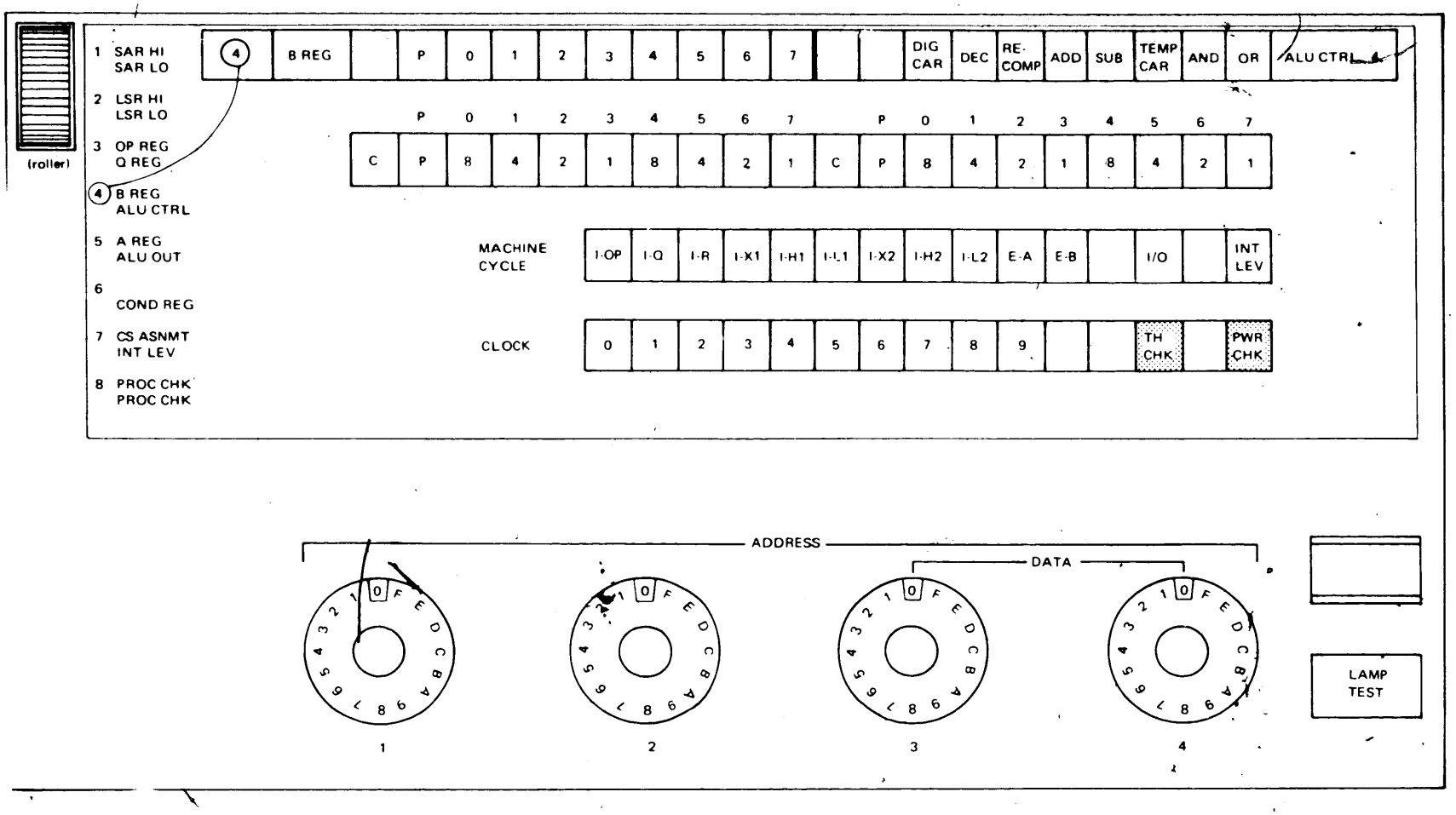


Figure 2-4. CPU Displays

C16

2.1.2.3 CE Mode Selector

This rotary switch selects one of three processor operating modes: the normal process mode, the step mode, or the test mode. Process is the mode for normal programmed system operation.

In the step mode, the rotary switch setting controls the manner in which the processor executes the stored program. There are three positions in the step mode.

Note: If this switch is changed while the system is running, a processor check can occur.

Instruction Step: In the instruction step, each start key depression and release causes one complete instruction to be executed. The I-phase is performed while the key is pressed and the E-phase, if any, when the key is released.

Note: Any SIO instruction which causes the clock to run as described under *Clock Step* also causes the next sequential instruction to be executed without start key operation.

Machine Cycle Step: In the machine cycle step, each start key depression and release advances the instruction through one machine cycle. Pressing this key causes data in storage to be accessed, modified as required, and the results displayed in the arithmetic logical unit (ALU) indicators of the console display. Upon release of the key, depending on the operation being performed, either the old data or the new result is written back into storage.

Clock Step: In the clock step, pressing the start key causes the clock to advance through and odd-numbered clock. Releasing the key causes the clock to advance through an even-numbered one.

The integrity of I/O data transfers is preserved by allowing the clock to run from the I-phase end of every executable start I/O instruction to the time the device is finished transferring data. The start key is not functional while this I/O transfer is taking place.

In systems without dual program feature, the halt identifier lights do not turn on in any step mode.

There are also three positions of the switch under test mode: alter SAR, alter storage, and display storage.

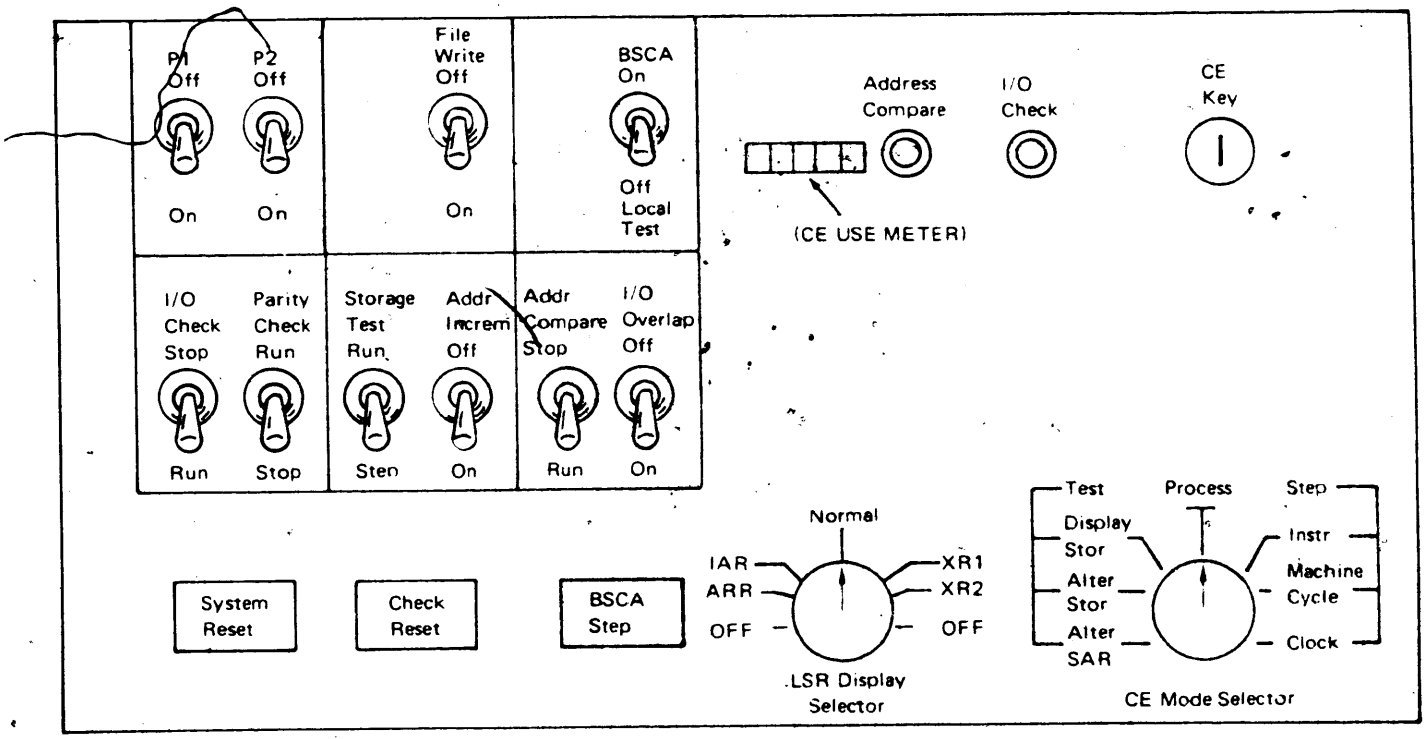


Figure 2-5. CE Control Panel

In the alter SAR position, the address set up in the address/data switches is transferred into SAR by the start key and the current IAR–instruction address register (P1, P2, or interrupt level). If the start key is held down, alter SAR has the ability of displaying in the A register the data that has been set in the data switches.

In the alter storage position, pressing the start key transfers data (previously set up in the rightmost two address/data switches) into the A register. Releasing the key causes this data to be placed in the storage location specified by SAR and into the Q register.

In the display storage position, pressing the start key transfers the contents of the storage location specified by SAR into the B register. When the key is released, these contents are rewritten into storage and transferred into the Q register.

2.1.2.4 LSR Display Selector

This rotary switch selects the local store register (LSR) to be displayed in position 2 of the display switch. The LSR's that can be displayed are instruction address register (IAR), address recall register (ARR), index register 1 (XR1), and index register 2 (XR2). The selected LSR is displayed whenever the CPU is not in CPU or I/O cycles. When this switch is in the normal position, as it should be when the system is in operation, the CPU controls the selection and display of LSRs.

Refer to section 2.5 for the procedure to display other LSRs.

2.1.2.5 System Reset Key

When this pushbutton is pressed, it resets all I/O and CPU registers, controls, and status registers, including the program status register (PSR). System reset also resets the current IAR (P1 or P2 IAR) and the MFCU read address register to zero. System reset is operable only when the CE mode selector is set to the process mode.

2.1.2.6 Check Reset Key

This pushbutton resets the processor and I/O check conditions. Check reset removes the current error conditions and allows the processor to resume its operation after the start key is pressed. It also resets the system power-check function and allows a 'power on' retry.

2.1.2.7 Storage Test Switch

This two position switch allows storage to be altered or displayed according to the position selected. In the step position, a storage location is accessed with each depression of the start key. In the run position, when the start key is pressed, core storage is exercised by accessing either the same location repetitively or all of core sequentially.

2.1.2.8 Address Increment Switch

This switch allows address incrementing when in the CE test modes of alter or display storage. With the switch on, the contents of SAR are incremented by 1 after each storage access. When the switch is off, SAR is not incremented.

2.1.2.9 Address Compare Switch

This switch allows a compare of the address/data switch setting and the register display when the register display is turned to SAR. When the address compare switch is in the run position, the address switch setting is compared to SAR through the register display, but no processor stop is initiated when a match occurs. The matched signal is provided as a sync point.

When the switch is in the stop position, a match of the address switches and the register display causes a processor stop at the completion of the storage read-write cycle. The processor is restarted by pressing the start key. I/O data transfers take place without loss of information. The contents of the SAR do not necessarily match the setting of the address switches when the processor stops.

2.1.2.10 I/O Overlap Switch

This switch modifies control of the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch turned to the normal position of on, I/O operations are executed in an overlap mode. When the switch is turned off, I/O operation is completed before the next sequential instruction is executed.

2.1.2.11 I/O Check Switch

This switch, when set to stop, forces the processor to an immediate stop on an I/O error. The console display is frozen to indicate the processor status at the time the error stop occurred. For normal operation, this switch is set to run.

CONTINUED ON FRAME D01

To restart after an I/O error, press check reset and then the start key.

2.1.2.12 Parity Switch

This switch, normally set to stop, forces the processor to an immediate stop whenever a parity error is detected. The restart procedure after a parity stop is to press check reset and then the start key. With the parity switch set to run, only the errors I/O LSR, INV ADR, INV OP, CHAN DBO, and INV Q will stop the processor; for all other errors, the processor will continue to run.

2.1.2.13 Address Compare Light

This light comes on when the address set in the address/data switches matches the SAR. For this to occur, the register display must be positioned to SAR. The system will not stop when the data matches unless the address compare switch is on.

2.1.2.14 I/O Check Light

This light is turned on when certain I/O errors (i.e., read check, punch check, hammer check) are detected by an addressed I/O device. It is turned off with a system reset, the check reset key, or at the discretion of the I/O device.

2.1.2.15 P1 and P2 Toggles

These two switches enable the CE to control selection of program level 1 or 2 to manually select the dual program mode of operation.

With P1 on and P2 off, the system operates in program level 1.

With P2 on and P1 off, the system operates in program level 2.

With both P1 and P2 off, the system is automatically enabled for the dual program mode of operation, with program level 1 being considered as the primary level.

For normal system operation, both P1 and P2 must be ON.

Note: An interrupt level 0 request is not accepted if either (but not both) P1 or P2 is turned off.

2.1.2.16 File (Disk) Write Switch

When this toggle switch is off, write operations cannot be performed on disk storage.

2.1.2.17 BSCA Local Test Switch

This toggle switch sets the high speed data-set into local test mode and causes data to be wrapped around through the data-set with a start I/O loop test instruction.

2

2.1.3 Console Display

The console displays are separated into two groups: a register display unit and a controls display section.

2.1.3.1 Register Display Unit

The register display unit (Figure 2-4 Fr. C16 consists of a row of twenty lights and eight legend strips mounted on an eight-position, roller-type, switch. At any one time, only one of the eight strips is visible through a cutout in the console above the row of lights. The legend strip and the corresponding register(s) displayed by the row of lights are selected by the eight-position switch.

2.1.3.2 Controls Display Section

1. Machine Cycles—Twelve indicator lamps represent the twelve mutually exclusive machine cycles. They identify the processor cycle just completed in all modes except the CE clock step mode, in which case, they indicate the cycle in progress.
2. Clock—Ten indicator lamps represent clocks 0 through 9 which can be stepped through in the CE clock step mode. In the normal process mode, a machine cycle consists of clocks 0 through 8 inclusive. Clock 9 is used with the CE step and test modes.
3. Interrupt—A single lamp indicator is used to monitor whether any interrupt level is being serviced.

DOI

2.2 ENVIRONMENTAL RECORDING

Errors detected during an RPG object program run will be stored in the communications area starting at core location /0180/. Forty-two bytes have been reserved for this, broken into two sections of 10 and 32 bytes. The 6-byte section is used to record 5203 hammer echo checks. Each of the 6 bytes will contain the filing print position. (Refer to Table 3 in the 5203 map charts.) In case more than six errors have occured, only the last six will be shown. The 32-byte section is made up of eight 4-byte sections showing the last eight errors to occur. Each 4-byte section will contain the Q, R, and 2 sense bytes of data about the failing instruction. These 42 bytes of information along with the date will be punched out into a card during a system installation run. This card will be merged with the system initialization program deck and will be the card just preceding the end card. This data will be the error data accumulated since the last system initialization run.

Refer to error recording analysis program (ERAP) documentation for specific details.

The card format for the data punched out is as follows:

Column 1	'W'
Columns 2-65	Error history table in hexadecimal. Eight sections of four bytes each containing the 'Q', 'R', and two sense bytes.
Columns 66-77	Six bytes of 5203 hammer echo check data.
Columns 78-93	Reserved
Columns 94-96	Date (coded)

2.3 MACHINE CHECKS

2.3.1 Processor Checks

If any of the following processor checks are detected, the system comes to an immediate stop and I/O data transfers are terminated:

1. *Invalid Address:* Indicates storage address register is addressing a location outside available core size.

2. *Operation Check:* Indicates that operation register contains an unassigned operation code.

3. *Parity Check:* Indicates that incorrect parity has been detected at one or more of the data or addressing check points in the CPU. (I/O data transfers are subject to these checks.) Restart: Initial program load procedure. Point of restart is a program/operator function.

4. *Invalid Q Code:* Indicates that no I/O device recognized the I/O instruction because either the device addressed is not attached (or not assigned) or because the N field of the Q code for that I/O instruction is invalid. Restart: As in parity check.

2.3.2 Unit Check

Unit check handling of testable indicates is controlled by programs. Restart procedures are conveyed to the operator by programmed halt operations, halt identifiers displayed on the console, and recovery/restart procedure listings.

2.4 PROCESS ERROR INDICATIONS

Processor checks are displayed and indicate the following:

1. *I/O LSR*–Selection of an LSR by an I/O device was not performed properly.
2. *LSR F1*–Parity is incorrect on the output of the LSR Feature 1.
3. *LSR F2*–Parity is incorrect on the output of the LSR Feature 2.
4. *LSR HI*–Parity is incorrect on the output of the LSR high.
5. *LSR LO*–Parity is incorrect on the output of the LSR low.
6. *SAR HI*–Parity is incorrect in the storage address register high.
7. *SAR LO*–Parity is incorrect in the storage address register low.
8. *INV ADDR*–The SAR contains an invalid address.
9. *SDR*–Parity in the storage data register is incorrect.
10. *CAR*–The carry out of the ALU is incorrect.
11. *DBI*–Parity is incorrect in the data bus in register.
12. *A/B*–Parity is incorrect in the A register or the B register.
13. *ALU*–Parity is incorrect in the ALU register.
14. *CPU DBO*–Parity is incorrect on the CPU end of the data bus out to the I/O devices.
15. *OP/Q*–Parity is incorrect in the op register or the Q register.
16. *INV OP*–Invalid op code in the op register.
17. *CHAN DBO*–Parity is incorrect on the I/O device end of the data bus out from the CPU.
18. *INV Q*–An invalid Q byte is present in an I/O instruction.

To determine which check comes first, compare the check lights to the clock time. Providing the proper clock is used, the leftmost check light that matches the clock time is the one that caused the processor check. Refer to Figure 2-6 for position 8 or the rotary register display unit.

	EVEN FOR LSR											ODD				
EVEN	NOT 0			CLOCK 1		1	4 or 6	EVEN NOT 0	ODD 1357	EVEN NOT 0	ODD NOT 9	NOT 789	8			
I/O LSR	LSR F1	LSR F2	LSR HI	SAR HI	SAR LO	INV ADR	SDR	CAR	DBI	A/B	ALU	CPU DBO	OP/Q	INV OP	CHAN DBO	INV Q

Figure 2-6. Register Display Unit-Position 8

2.5 LSR DISPLAY

To display LSR's other than IAR, ARR, XR1, and XR2, the following procedure should be used:

1. Turn the LSR display rotary switch off.

2. Turn the register display switch to position 2.

3. Tie up the desired LSR (Figure 2-7) to -0.75 volts (Figure 2-8)Fr. D05

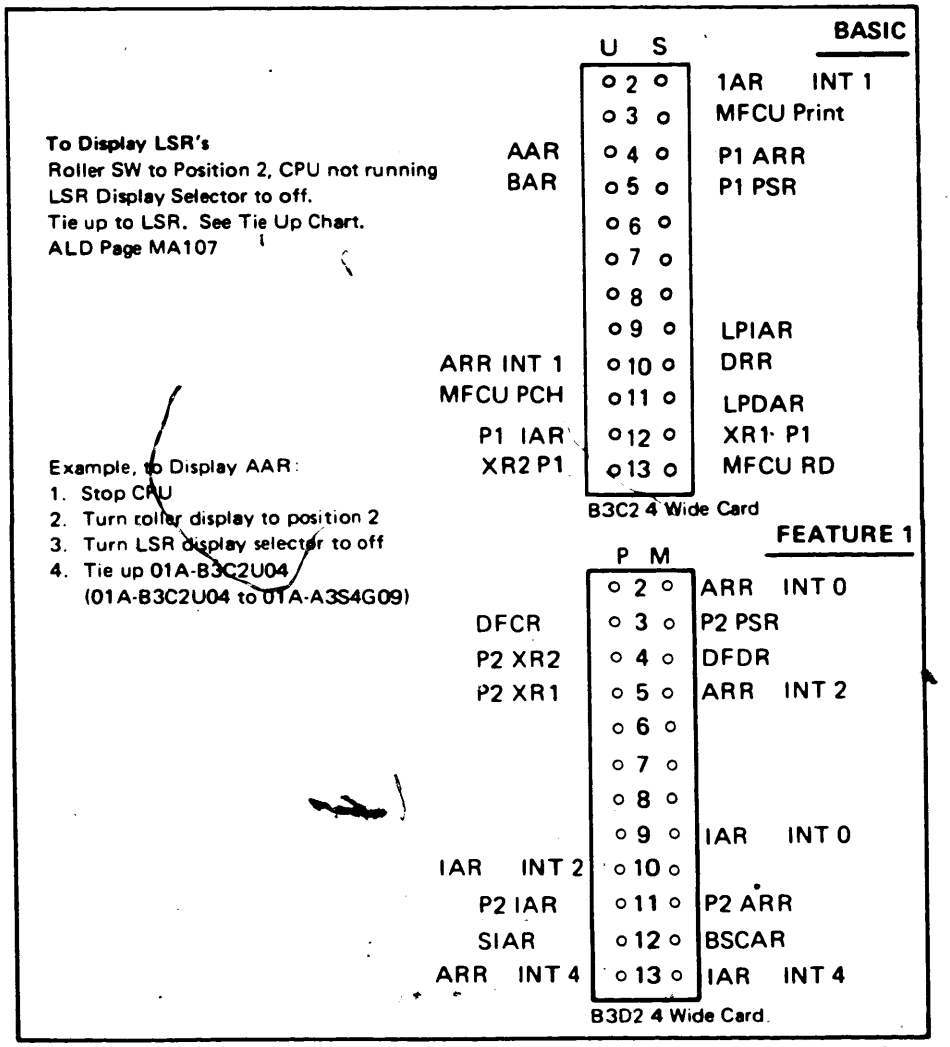
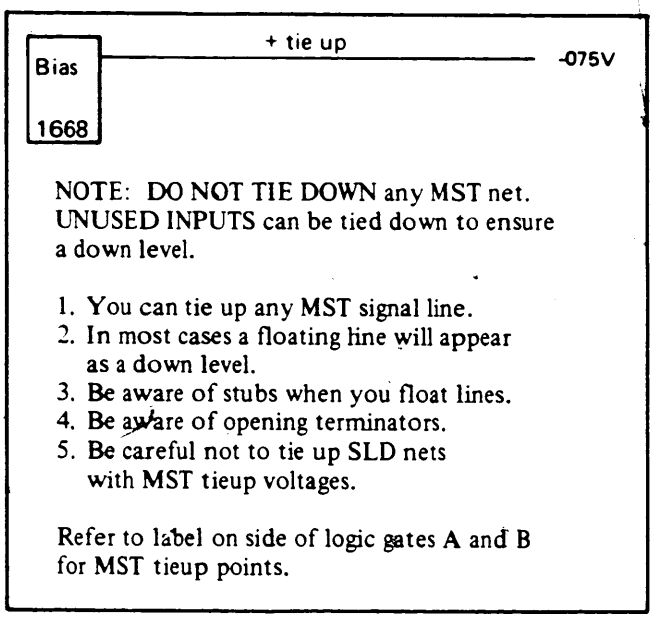


Figure 2-7. LSR Display

D04



NOTE: DO NOT TIE DOWN any MST net. UNUSED INPUTS can be tied down to ensure a down level.

1. You can tie up any MST signal line.
2. In most cases a floating line will appear as a down level.
3. Be aware of stubs when you float lines.
4. Be aware of opening terminators.
5. Be careful not to tie up SLD nets with MST tieup voltages.

Refer to label on side of logic gates A and B for MST tieup points.

Figure 2-8. MST Tie Up Data

2.6 VOLTAGE LEVELS

Figure 2-9 gives acceptable voltage levels for monolithic system technology (MST) -1 and solid logic dense (SLD) 700 technology.

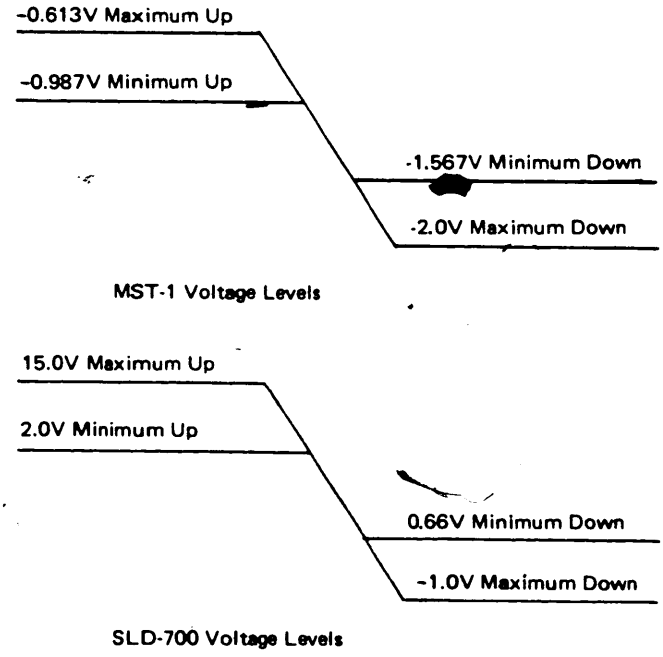


Figure 2-9. Voltage Levels

2.7 ERROR RECOVERY PROCEDURES

Figures 2-10Fr. D06 and 2-11Fr. D08 give procedures for recovering errors in the Printer and the MFCU. They list the condition re quiring operator intervention, a brief description of the problem, and the operator recovery procedure.

ERROR RECOVERY PROCEDURE UNIT PRINTER								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Incrementer Failure Check (PTR Ck Lite)	3	2	3	Off	P6	Incrementer failure check caused by the incrementing hammer unit failing to move. P6, P8 are hardware limited to set only the first bit in error.	1) Press printer start key. 2) Press CPU start key.* Note: This results in printing the remaining information on the line with no loss of data.	Re-execute the last printer SIO instruction.
Sync Check (PTR Ck Lite)	1 2	1 1	0 1	Off	P5	A maximum of two printed lines may be in error. Error is hardware limited to first error. 1) Chain sync check caused by loss of attachment sync with the chain. 2) Incrementer sync check caused by loss of attachment sync with the incrementing hammer unit or failing roller clutch.	1) Press printer start key. 2) Press CPU start key to continue without recovering errors.	Continue processing. Since the data printed in error is no longer available, no recovery of of that data is possible.
Print Check (PTR Ck Lite)	4 5	2 2	5 6	Off	P8	A maximum of one character may be in error. P6, P8 are hardware limited to set only the first bit in error. 1) Hammer echo check caused by improper hammer driver response during print time. 2) Any hammer on check caused by a hammer turning on when not in print time.	1) If the carriage has moved from the last line of printing and that line is incomplete, manually reposition the forms to the last line of printing using the carriage restore key and the carriage space key. If no manual intervention is made and the last line is not complete, the remainder of that line is printed in the stopped location. 2) Press printer start key. 3) Press CPU start key* to continue without recovering error.	Re-execute the last printer SIO instruction. Since the character printed in error is no longer available, no recovery of that character is possible.
Thermal Check (PTR Ck Lite)	6	1	2	Off	P7	Thermal check caused by overheating in the print hammer unit area.	1) Press printer start key. 2) Press CPU start key.*	Continue processing.
Forms Jam (PTR Ck Lite)	9	2	2	Off	P3	Forms jam in the print line.	1) Clear the forms jam. 2) Manually reposition next good form to line 1 using the carriage restore key. Note: Printing continues on the new form. Any missing printed information is recovered only by an IPL procedure. 3) Press printer start key. 4) Press CPU start key.*	1) Store carriage line counter with an SNS instruction before executing the P3 halt. 2) After start key is pressed the program issues an SIO skip to the proper line and continues printing.

* If the dual program feature is installed, press the halt reset key.

Figure 2-10. (Part 1 of 2) Error Recovery Procedures (Printer)

ERROR RECOVERY PROCEDURE UNIT PRINTER								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Carriage Check (PTR Ck Lite)	7 8	2 2	0 1	Off	 P1	Error is hardware limited to first error. 1) Carriage sync check caused by loss of attachment sync with the forms or carriage runaway detection. 2) Carriage space check caused by skipping or spacing farther than the instruction called for.	1) Manually reposition forms to the last line of printing using the carriage restore key and and the carriage space key. Note: If this is followed, no print or carriage information is lost. 2) Press printer start key. 3) Press CPU start key.*	Re-execute the carriage control portion of the last SIO instruction.
Unprintable Character	10	1	6	Off	PC	There was one or more unprintable characters in the last line printed.	1) Press printer start key. 2) Press CPU start key.*	Continue processing.
Chain Check	11	1	5	Off	 PE PF	The chain is not compatible with the image in core. 48 character set chain is mounted. UCS chain is mounted.	A) If incorrect chain: 1) Install correct chain 2) Press printer start key 3) Press CPU start key.* B) If incorrect image: 1) Re-IPL using correct image for chain.	A) Continue processing. B) IPL
Forms Check (Forms Lite)	12	-	-	On	Off	Less than 14 inches of forms remain.	When end of forms and line 1 is sensed, the FORMS light will come on. No additional lines can be printed. At this point it is necessary to: 1) Replace forms. 2) Press printer Start key.	Condition is not program identifiable. Continue processing.
Interlock Check (Interlock Lite)	12	-	-	On	Off	1) Cover interlock is open. 2) Chute interlock is open.	1) Correct interlock condition: a) Close the cover. b) Close the chute. 2) Press printer start key.	Condition is not program identifiable. Continue processing.

* If the dual program feature is installed, press the halt reset key.

Figure 2-10. (Part 2 of 2) Error Recovery Procedures (Printer)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Feed Check	1	1	6	Off	F0 or F1	Feed check indicates one or more cards are mispositioned or jammed in the feed path.	1. Open MFCU top covers. 2. Check halt ID for F0 or F1 and perform step a or b. a. If F0, remove card from primary (upper) wait station and place card under cards in the primary hopper. b. If F1, remove card from secondary (lower) wait station and place card under cards in the secondary hopper. 3. Press CPU start key.* The display in the message display unit will change from F0 to F1 to two numbers. 4. Remove remaining cards from MFCU transport. Begin at hopper and work toward print station. Keep the cards face down and in correct sequence by placing card nearest the hopper, on top. *Note:* If MFCU indicator 7, 8, 10, or 12 is on, replace the card that is between the punch station and the corner station with a blank card if a blank card was used; use a prepunched card if a prepunched card was used. 5. Check message display unit. The left digit indicates the number of cards that must be placed back in the secondary hopper (if halt ID is F0) or primary hopper (if halt ID is F1). If the number of cards you now have in your hand *equals* this displayed number, go to step 7.	The program determines the number of cards that should be in the machine by determining how many busy conditions have not been cleared within the program and adding one for each feed in use. All commands not complete are reissued. The restart procedure involves dummy operations to reposition the cards as they should have been at the time of the feed check. The program then reissues commands to complete the operations.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 1 of 6) Error Recovery Procedures (MFCU)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Attn Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Feed Check (cont.)							6. If the number of cards removed is less than the left displayed number, remove enough cards from the stacker indicated by the right displayed digit. Then place these cards on the bottom of the deck face down. 7. Place cards in secondary hopper (halt ID was F0) or primary hopper halt ID was F1).* 8. Raise cards in primary hopper and press NPRO key. Then raise cards in secondary hopper and press NPRO key. This action turns off error indicators on the MFCU panel. 9. Close MFCU top covers. 10. Press MFCU start key. 11. Press CPU start key.*	
Combinations of Errors	1					Halt Identifier: The halt identifier displayed is one of those described elsewhere.	The action taken by the operator is described under the particular halt indicator displayed.	The restart for combination of errors takes place in the following sequence and follows the procedure for the error indicated: 1. Feed Check 2. Print Data Check 3. Print Clutch Check 4. Punch Invalid 5. Punch Check 6. Read Check or Hopper Check
Error During Restart						If the same error is repeated during restart, the same halt identifier previously displayed is displayed again. If a new error occurs, the identifier associated with it is displayed subject to priorities listed in combinations of errors.	The operator runs out the MFCU and retrieve cards from the stacker or hopper, as necessary, to repeat the operator recovery action.	The program restart procedure is repeated.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 2 of 6) Error Recovery Procedures (MFCU)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Punch Check	2	1	1	Off	F4	Punch check means that extra or missing punches are in the card in the stacker indicated by the second halt. Second Halt 01 Stacker 1 02 Stacker 2 03 Stacker 3 04 Stacker 4	1. Observe the back-lit panel on the MFCU to determine which hopper fed the last card. 2. Check to determine if blank cards or prepunched cards are being punched. If blank cards are used, remove the last card in the indicated stacker and do Action 7. If prepunched cards are used, proceed with Actions 3–8. (If in doubt, assume prepunched cards are being used.) 3. Press CPU start key* to obtain stacker for error card. 4. Mark the last card in the indicated stacker. 5. Press stop on the MFCU. 6. NPRO the feed from which the last card was fed. Place in that hopper a blank card, followed by the card run out, followed by the remaining cards in that hopper. 7. Press start on the MFCU. 8. Press CPU start key.* 9. Upon completion of the job or removal of the cards from the stacker, do the following: a. Manually punch the information from the marked card into the card immediately following it, checking for extra punches which may have resulted from the punch check. b. Discard the marked card and replace the remaining card at its proper place in the deck. c. Mark the card and make a note to the programmer to check the card.	The restart procedure is reissue the last command except that if read was specified, the read portion of the command will not be re-executed. This way, a blank card is fed in from the correct hopper, the information is punched, printing is done if specified, and the card is stacked in the proper stacker. Since processing may have taken place in the read buffer, the read portion is not re-executed.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 3 of 6) Error Recovery Procedures (MFCU)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Punch Invalid	2	1	2	Off	F5	A character which is not one of 64 valid characters has been specified to the MFCU punch. The character less the C & D punches was punched. Punch checking was not performed on the remainder of the card. The error card is in the stacker indicated by the second halt. **Second Halt** 01 Stacker 1 02 Stacker 2 03 Stacker 3 04 Stacker 4	1. Press CPU start key* to obtain stacker for error card. 2. Mark the last card in the indicated stacker as being invalid. 3. To continue job, press CPU start key or correct program or data and re-IPL.	If continuation of the job is desired, the program may proceed as indicated. The operation is not re-executed.
Print Check	2	1	3	Off	F6	Data Check: caused by an error in the synchronization between the attachment and the print wheels.	To continue job, press CPU start key.*	The program will proceed as indicated. The operation is not re-executed.
	2	1	4	Off	FC or F6	Clutch Check: caused by an error in the synchronization between the attachment and the print stepper clutch.		
Print Data Check Full Function Error Recovery Procedure	2	1	3	Off	FA **Second Halt** 01 02 03 04 **Third Halt** F0 **Fourth Halt** 01 02 03 04	Caused by an error in the synchronication between the attachment and the print wheels. Stacker 1 Stacker 2 Stacker 3 Stacker 4 Stacker 1 Stacker 2 Stacker 3 Stacker 4	For a full function error recovery procedure, proceed as follows: 1. Press MFCU stop key. 2. Press CPU start key* to display stacker containing error card. 3. Remove card from stacker indicated by second halt display. Call this card one. 4. Press CPU start key.* 5. If I/O attention lights, go to step 7. 6. If halt indicator F0 lights, press CPU start key* to obtain stacker for the second card. Fourth Halt: a. If both cards are from the same stacker, place the second card removed under the first card. b. If a different stacker is indicated, place the second card on top of the first card.	When the print data check is detected, determine how many print buffers were not released. Display the stacker containing the latest card and halt. After pressing start key, display a halt if two buffers were busy. Then print-feed one or two cards and halt at F0. Then return to normal processing.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 4 of 6) Error Recovery Procedures (MFCU)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Full Function Error Recovery Procedure (cont.)							7. NPRO the primary feed. 8. Place the cards run-out on top of a number of blank cards equal to the number of cards removed in steps 1-6. If the primary feed was not being used, add one extra card. 9. Press MFCU start key. 10. After halt indicator F0 lights, NPRO the primary feed if it was not in use. Remove one or two cards from stacker as previously shown by halt indicator and manually correct any printing errors on cards removed in steps 1-8. 11. Place corrected cards in correct stacker. 12. Press CPU start key.*	
Read Check	3	1	0	Off	F3	Caused by: 1. Off punched card. 2. Damaged card. 3. MFCU feed problem. 4. Cards in hopper backwards or upside down.	1. Observe the back-lit panel on the MFCU to determine from which hopper the last card was fed. 2. Press stop on the MFCU. 3. NPRO the feed from which the last card was fed and replace the card run out in that hopper followed by the remaining cards in the hopper. 4. Press start on the MFCU. 5. Press CPU start key.*	The restart procedure repeats reading of the card which caused the read check. The hopper information is retrieved from the last command. A read check does not affect execution of the punch, print, or stacker select portion of the command. Therefore, that portion of the command is not re-issued.
Hopper Check	3	2	3	Off	F2	A card was not picked from the hopper.	1. Observe the back-lit panel on the MFCU to determine the hopper from which the last feed was attempted. 2. Straighten or, if necessary, reproduce the damaged card(s) in the hopper from which the feed was attempted. 3. Press start on the MFCU. 4. Press CPU start key.*	The restart procedure attempts to feed the card from the hopper, in which the hopper check occurred, into the wait station. If a read was specified in the last command, the card will be read. The hopper check does not affect execution of the punch, print, or stacker select portion of the command. Therefore, that portion of the command is not re-issued.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 5 of 6) Error Recovery Procedures (MFCU)

ERROR RECOVERY PROCEDURE UNIT MFCU								
Condition Requiring I/O Attention	PRIOR	STATUS BYTE	STATUS BIT	I/O Att Lite	HALT ID	DESCRIPTION	OPERATOR RECOVERY PROCEDURE	PROGRAM ACTION
Not Ready	4	–	–	On	Off	Caused by: 1. Hopper empty. 2. Stacker full. 3. Chip box full or out of machine. 4. Covers open. 5. Operator pressed stop key. *Note:* No halt identifier is displayed. The I/O attention light on the console is on.	1. Locate the cause of the not ready condition by checking the lights on the MFCU for: chip box full, covers open, or stacker full. If these lights are not on, check the back-lit panel on the MFCU to determine which hopper attempted the last feed. Then check that hopper for hopper empty condition. 2. Correct the condition causing the not ready. 3. Press CPU start key.*	None. The program loops on the SIO instruction until the MFCU is ready. Then SIO instruction is executed and the program continues.

*If the dual program feature is installed, press the halt reset key.

Figure 2-11. (Part 6 of 6) Error Recovery Procedures (MFCU)

2

D13

2.8 MFCU FEED CHECKS

Figure 2-12 Fr. D15 shows the possible MFCU feed checks and the cause of each one for troubleshooting.

D14

	During Which Operation Check Is Given				
	Every Operation	Punch Operation	Non-Punch Operation	Print Operation	Non-Print Operation
Hopper Check	x				
Feed Check 1	x				
Feed Check 2	x				
Feed Check 3					
Feed Check 4	x				
Feed Check 5	x				
Feed Check 6			x		
Feed Check 7		x			
Feed Check 8		x			
Feed Check 9			x		
Feed Check 10		x			
Feed Check 11			x		
Feed Check 12		x			
Feed Check 13	x				
Feed Check 14					x
Feed Check 15				x	
Feed Check 16					x
Feed Check 17				x	
Feed Check 18					
Feed Check 19	Stacker				
Feed Check 20	Gear emitter check or fire CB check				

Figure 2-12. MFCU Feed Checks

Given		Under Which Solar Cell Condition Check Is Given					
ration	Non-Print Operation	Covered Late	Uncovered Late	Uncovered Early	Never Dark	Dark Without Feed Cycle	
					Hopper Cell		Card never covered cell.
		Hopper Cell					Card covered cell late.
		Read Cells					Card late getting to read station.
						Read Cells	Card jammed in read station.
			Read Cells				Card too long in read station.
						Prepunch	Card left wait station without punch registration pressure roll.
		Prepunch					Card late to prepunch cell.
		Prepunch					Card late to prepunch cell in punch operation.
				Prepunch			Card out of registration in punch operation.
			Prepunch				Card too long in punch station.
			Prepunch				Card out of registration in punch operation.
		Corner					Card late to corner non-punch operation.
		Corner					Card late to corner punch operation.
				Corner			Card left corner without kicker.
	x		Corner				Card left corner late non-print operation.
			Corner				Card left corner late print operation.
	x	Postprint					Card too long in print station.
		Postprint					Card early or late leaving print station.
			Postprint				Card too slow to stacker transport.
				Jam			
3 check							

2.9 SPECIAL TOOLS

The following special tools used in troubleshooting System/3 are either included in the System/3 shipping group or are available from the branch office. See the *Integrated Maintenance Package User's Guide* (part 2589902) for detailed descriptions of the tools.

2.9.1 CE Diagnostic Probe

The CE diagnostic probe (Figure 2-13Fr. D18 part 817971) acts as a free-running oscilloscope which replaces scope usage for most System/3 service calls. The probe can measure SLT 100/700 and MST-1 signal levels. The probe also has two MST-1 gates for gated operation. Consult the *Integrated Maintenance Package User's Guide* (part 2589902) for specific levels that trigger the probe. An assembled view of the probe is given in Figure 2-13, insert A.Fr. D18The lamps (part 454612) and probe tips (part 453163), shown in the disassembled view of the probe (Figure 2-13, insert B)Fr. D18 are field replaceable.

Note: The probe may give a wrong indication because of electrical noise. For example, electrical noise can be caused by:

- The probe power cord close to the CPU memory magnetic field.
- The switching of flourescent lights.
- Electric drills.
- Electrostatic discharge.

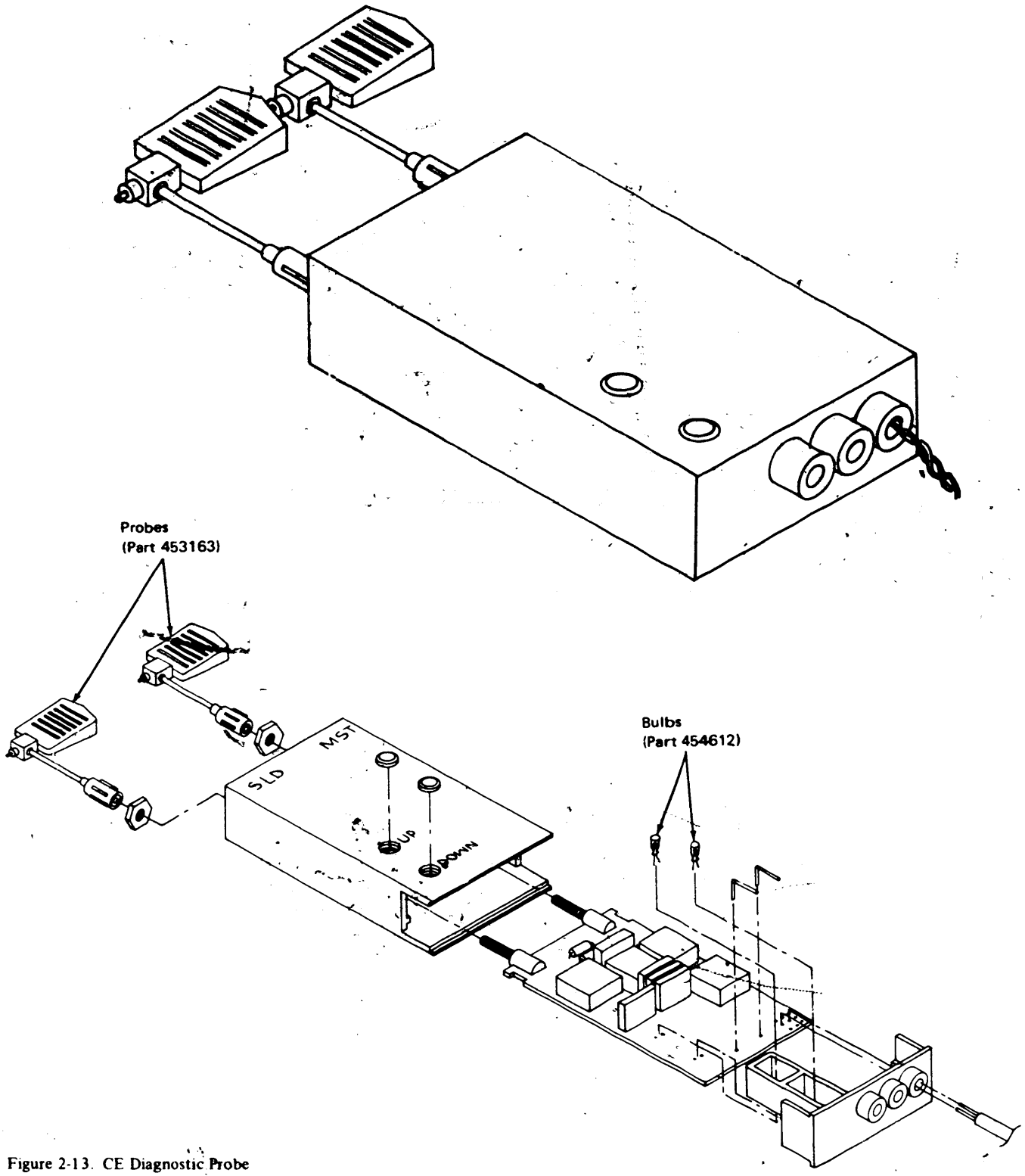


Figure 2-13. CE Diagnostic Probe

CONTINUED ON
FRAME E01

2.9.2 Jumper Wires

Six jumper wires (Figure 2-14) are included in each 5410 shipping group; two 6" wires (part 829117), two 12" wires (part 2588263) and two 18" wires (part 829118). These jumpers are provided for use with the MAP charts and diagnostic programs.

2.9.3 Single Pin Extenders

The single pin extender (Figure 2-15, part 2594238) is used to extend board pins when using the CE meter to measure voltage levels. The use of these pins elminates shorting to adjacent pins when using the meter leads.

2.9.4 MST-1 Card Extender

The MST-1 card extenders (Figure 2-16) allow the CE to extend a card above the tops of adjacent cards on a board. This makes the module pins on the back of the card more accessible for probing with a scope of the diagnostic probe. These card extenders are stocked at the branch office.

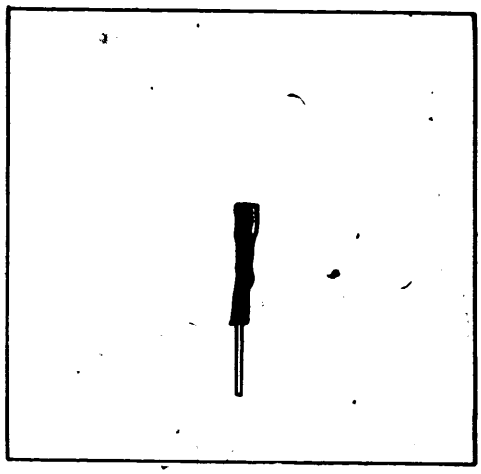


Figure 2-15. Single Pin Extenders

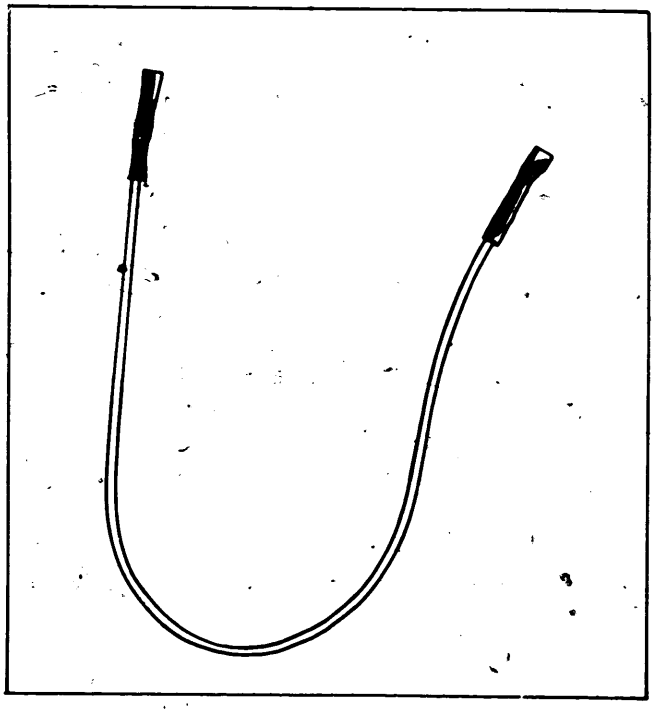


Figure 2-14. Jumper Wires

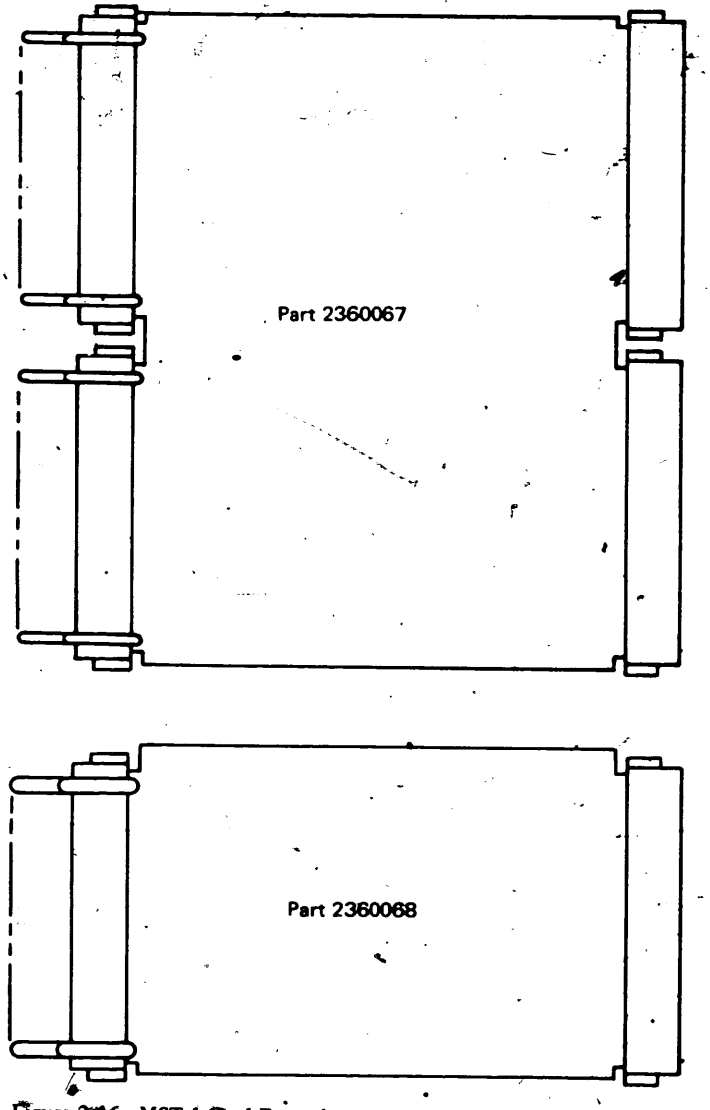


Figure 2-16. MST-1 Card Extender

2.10 DUAL PROGRAM CONTROL PANEL

The dual program controls (Figure 2-17) consist of:

2.10.1.1 Message Display Units

A message display unit is provided for each program level. These units operate in the same manner as the message display unit in the system controls.

2.10.1.2 Process Lights

These lights indicate which program level is functioning at any time. If an interrupt is being serviced, this indicator shows which index registers and program status register are in use.

2.10.1.3 Halt Reset Keys

These keys are used to take a program level out of the programmed halt state. Pressing either of these keys clears the corresponding message display unit and allows the corresponding program to continue its normal operation.

2.10.1.4 Interrupt Key/Light

Pressing this key when it is illuminated causes the program in operation at that time to halt its normal operation and enter the interrupt-handling subroutine for interrupt level 0. Normal programmed operation will be resumed after the interrupt routine signals completion of interrupt servicing with a start I/O instruction to reset interrupt request 0.

The interrupt key is lighted only when the system is in dual programming mode and interrupt level 0 is enabled. Selection of whether the system is to be used in the dedicated or the dual programming mode is accomplished via the start I/O instruction. The start I/O instruction is also used to enable or disable the use of interrupt level 0.

2.10.1.5 Dual Program Control Switch

This rotary switch is normally used in conjunction with the console interrupt key. The status of this switch is sampled by the test-I/O-and-branch instruction.

2.11 FILE CONTROL PANEL

The file controls (Figure 2-18) consist of:

2.11.1.1 Program Load Selector Switch

This switch is used to select the unit from which program loading is to be done. The fixed disk and removable disk positions refer to drive 1 only.

2.11.1.2 Start/Stop Switches

These switches (one per drive) turn the disk drive power on or off when system power is on. With the switch in the off position, the removable disk can be replaced.

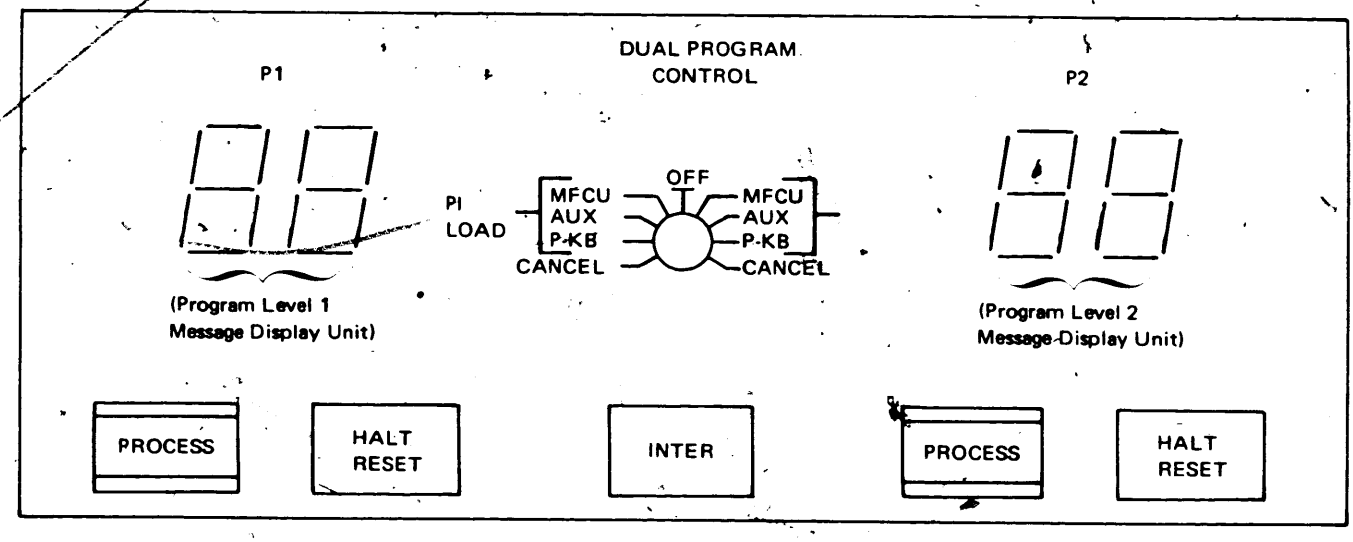


Figure 2-17. Dual Programming Control Panel

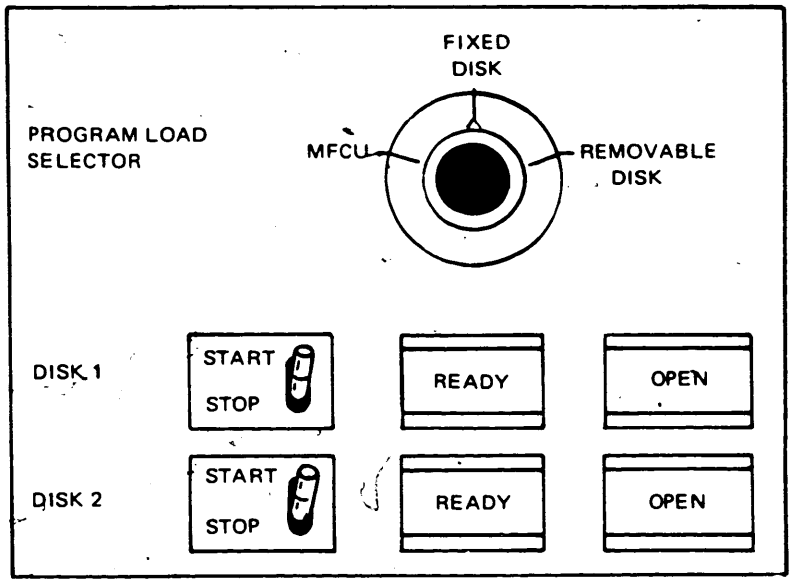


Figure 2-18. Disk Control Panel

2.11.1.3 Ready Lights

These lights (one for each drive) light when the disk drive is ready for use. If operation of the drive is attempted before this light turns on, the I/O attention light on the control panel will light.

2.11.1.4 Open Lights

These lights (one for each drive) indicate that the associated drive drawer can be opened for changing the removable disk. This light turns on when the start/stop switch is turned to the stop position, the read/write head has been retracted, and the disk has come to a stop.

2.12 BSCA INDICATOR PANEL

The BSCA Indicator panel (Figure 2-19, Fr. E04 consists of:

2.12.1.1 BSCA Attention Light

The following table shows the conditions indicated by this light.

Instruction	Condition Indicated
Any receive or transmit and receive or (on non-switched and multipoint networks only) receive initial.	Data set is not ready.
Auto call or receive initial on switched network.	Auto call unit power is off or data line in being used.
Any SIO except control SIO.	Either (1) the BSCA is disabled or (2) the external test switch is on and BSCA is not in test mode.
None.	Data set is not ready.

2.12.1.2 Unit Check Light

This light turns on when any bit in status byte 2 is on. Also, when an SNS transition or SNS stop register instruction is executed, it is possible for an LSR, S register, or DBI register parity check to occur, resulting in a unit check condition with the unit check light on. Under such a condition, the status byte 2 bits may all be zero.

The unit check indicator signifies that the BSCA program should enter an error recovery procedure.

2.12.1.3 Data Terminal Ready Light

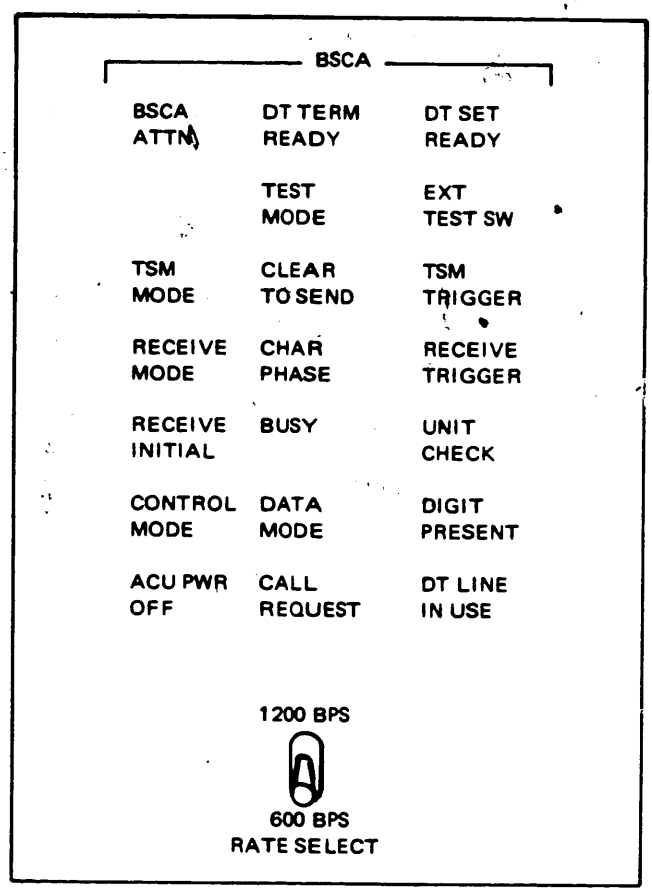
This light indicates that the BSCA is enabled and that the data terminal is ready for use.

2.12.1.4 Data Set Ready Light

The DT SET READY light indicates that the data set ready line from the data set is on and that the data set is ready for use.

2.12.1.5 Clear To Send Light

This light indicates that the clear to send line from the data set is on and that the adapter may now transmit.



Note: Rate select switch is for machines used outside the United States.

Figure 2-19. BSCA Control Panel

2.12.1.6 Receive Trigger Light

This light indicates the status of the receive trigger. The light is on when the trigger is at a binary 0 state.

2.12.1.7 Transmit Trigger Light

The TSM TRIGGER light indicates the status of the transmit trigger. The light is on when the trigger is at a binary 0 state.

2.12.1.8 Receive Mode Light

This light indicates that the adapter has been instructed to perform a receive operation.

2.12.1.9 Transmit Mode Light

The TSM MODE light indicates that the adapter has been instructed to perform a transmit operation.

2.12.1.10 Receive Initial Light

This light is turned on by an SIO receive initial instruction. It is turned off at the end of the receive initial operation.

2.12.1.11 Busy Light

This light indicates that the communication adapter is executing a receive initial, transmit and receive, auto call, receive or loop test instruction.

2.12.1.12 Character Phase Light

The CHAR PHASE light indicates that the adapter has established character synchronism with the transmitting station. The light is turned off at the end of receive operations and whenever character synchronism is lost.

2.12.1.13 Data Mode Light

This light is turned on by the decoding of an SOH or STX during a transmit or a receive operation. It is turned off at the end of the transmit or receive operation.

2.12.1.14 Control Mode Light

This indicator is used only on systems that have the station select feature installed. The light is turned on by an EOT sequence during a transmit, receive, or receive initial monitor operation when the station select feature is installed. It is turned off by the decoding of an SOH or STX.

2.12.1.15 Digit Present Light

This light indicates that a digit has been obtained from storage for the auto call unit when the auto call feature has been installed.

2.12.1.16 Auto Call Unit Power Off Light

The ACU PWR OFF light indicates that the auto call unit (special feature) power is off.

2.12.1.17 Call Request Light

On systems with the auto call feature installed, this light indicates that the communication adapter has received an SIO auto call instruction and is performing an auto call operation.

2.12.1.18 Data Line In Use Light

On systems with the auto call unit installed, the DT LINE IN USE light indicates that the data line occupied line from the auto call unit is on.

2.12.1.19 Test Mode Light

This light indicates that the program has placed the adapter in a test mode of operation.

2.12.1.20 External Test Switch Light

The EXT TEST SW light indicates that the switch at the data set end of the medium speed data set cable is in the test position. For high speed data sets, this indicator is active when the local test switch on the CE panel is in the on position.

2.12.1.21 Rate Select Switch

This switch, which is present only on systems installed outside the U.S.A. that have the rate selection feature as well, controls the rate of transmission and reception of data.

2.12.1.22 BSCA Step Key

The BSCA STEP key, which is effective only when the communication adapter is in step mode, causes the communication adapter to advance one bit-time for each key depression.

2.12.1.23 Local Test Switch

This toggle switch sets the high speed data set into local test mode and causes data to be wrapped around through the data set with a start I/O loop test instruction in test mode.

PREVENTIVE

MAINTENANCE

E06

Chapter 3. Preventive Maintenance

Section 1. Basic Unit

3.1 SCHEDULED MAINTENANCE

Perform the following maintenance every three months:

1. Check filters visually and replace as necessary.
2. Check cooling fans for proper operation.

Caution
Do not use IBM cleaning fluid on plastic parts.

3.2 I/O DEVICE MAINTENANCE

Scheduled maintenance for I/O devices is included in the maintenance manual for each device.

CONTINUED ON

FRAME A10

CARD 1-2