IBM

Series/1

SY34-0059-2

IBM Series/1
Communication Features
Theory Diagrams

Third Edition (June 1980)

This is a major revision of, and obsoletes, SY34-0059-1 and Technical Newsletter SN34-0603. Significant changes in this edition include incorporation of Chapter 4, "Feature–Programmable Multi-Line Communication." Technical changes to the text and illustrations are indicated by a vertical line to the left of the changes.

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Preface

This manual describes the Series/1 communication features.

This manual is designed to be used in the classroom as an aid in teaching personnel that are to be involved in the maintenance of the Series/1 communication features. This manual may also be used in the field as a recall document.

Pin numbers, voltage levels, and timing conditions used in this manual are not to be used in troubleshooting procedures. Use the engineering MLD pages for exact information.

The subject matter is presented in four chapters and four appendixes.

- Chapter 1 describes the asynchronous communication control (ACC) feature.
- Chapter 2 describes the binary synchronous communication control (BSC) feature.
- Chapter 3 describes the synchronous data link control (SDLC) feature.
- Chapter 4 describes the programmable multi-line communication feature.
- Appendix A contains a chart that lists the control and data characters for EBCDIC, ASCII, Eight-Bit Data Interchange Code, and Paper Tape Transmission Code.
- Appendix B shows schematic diagrams of various cables that are used to connect the communication features to modems and terminals.
- Appendix C contains timing diagrams.
- Appendix D contains a list of accronyms.

Related Publications

IBM Series/1 Model 3 4953 Processor and Processor Features Description, GA34-0022 or

IBM Series/1 Model 5 4955 Processor and Processor Features Description, GA34-0021

IBM Series/1 Communication Features Description, GA34-0028

Additional Series/1 information can be found in publications listed in IBM Series/1 Graphic Bibliography, GA34-0055.

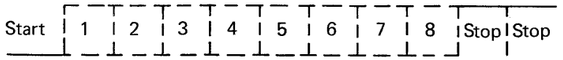
Contents

Chapter 1. Asynchronous Communication

The Asynchronous Communications Control (ACC) features allow the transfer of serial data to a remote processor or terminal using the start/stop method of character synchronization. In the start/stop method of synchronization, the transmission line is held in a marking condition until a character is to be sent. All characters begin with a start bit; the start bit is always a "space". Upon seeing a spacing condition on the line, the receiver starts the receive clock and bit ring. The bit ring counts the number of bits required by the transmission code being used. Some codes use seven data bits and some codes use eight data bits. The data bits are always followed by at least one stop bit. Stop bits are always "marks". The transmission code being used determines the number of stop bits.

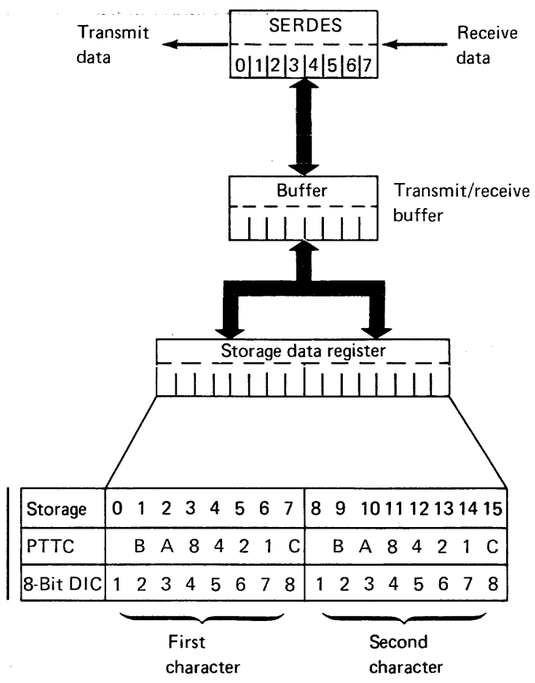
The Asynchronous Communications Control features can use either PTTC (Paper Tape and Transmission Code) or Eight Bit Data Interchange Code. PTTC codes use seven data bits and one stop bit; Eight Bit Data Interchange Code uses eight data bits and two stop bits.

PTTC code



8-Bit Data Interchange Code

The asynchronous communications attachments provide the ability for the program to select the transmission code to be used. The following example shows the relationship between the bits in storage and the bits in PTTC code and Eight Bit Data Interchange Code. The codes are shown in Appendix A.



The attachments also provide for programmable bit rates. The bit-rate is selected by storing a hexadecimal constant into a register in the attachment.

Data Flow

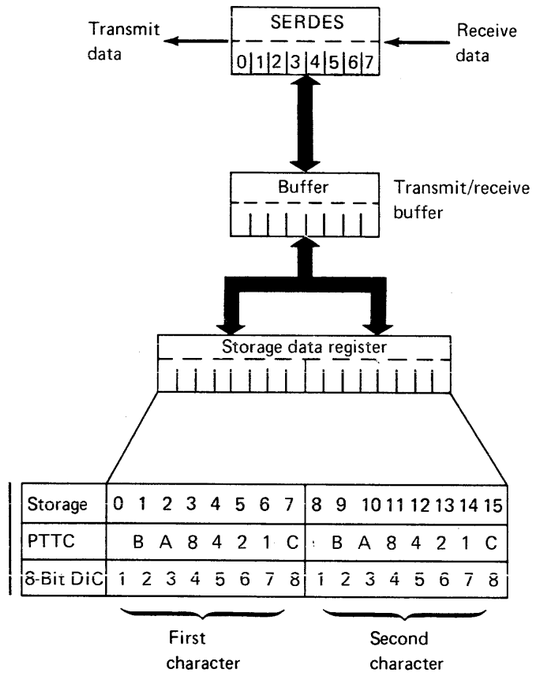
Each character occupies one byte in storage. Transfers to and from storage are two bytes at a time, except that the first and/or last transfers may move only one byte if specified by the data address or byte count.

Transmit

Transmission data is fetched from storage two bytes at a time (except as noted previously). The high order byte holds the first character to be sent and the low order byte holds the next character. After a character has been transferred into the SERDES (serializer/deserializer), it is transmitted over the line, high order bit first.

Receive

The first bit received is transferred into the high order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on until a character is assembled. Two characters are assembled in the attachment before data is transferred to storage (except as noted previously). When two characters are to be transferred to storage, the first character received is loaded into the higher order byte of the storage data register and the next characted is loaded into the low order byte before the data is transferred to storage. Data is written into storage without any code translation.



ACC transmit and receive data flow

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ACC Feature Configurations

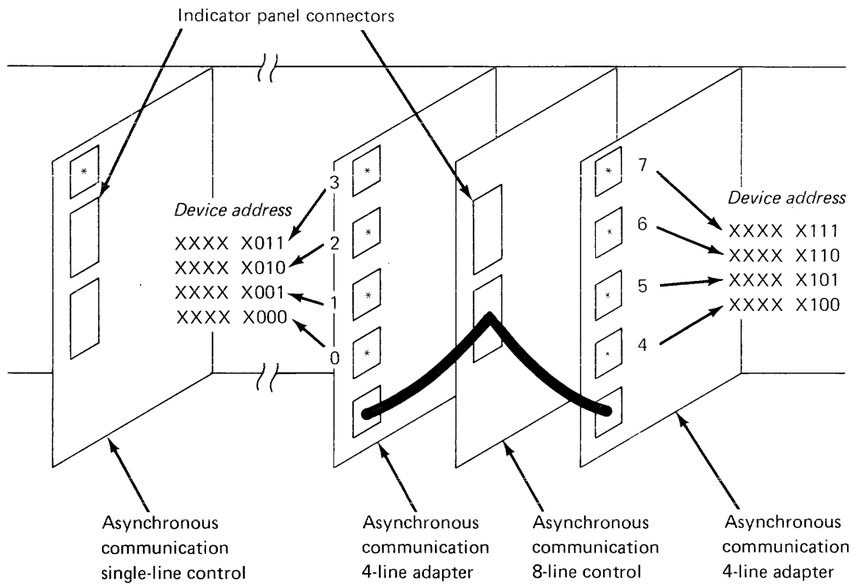
The Asynchronous Communication Control features are available in single-line multiple-line configurations. The multiple-line configuration provides up to eight lines. The single-line ACC feature contains one card. The multiple-line configuration contains either two or three features cards—two cards for one to four lines, three cards for five to eight lines.

Note: Throughout the remainder of this chapter, the term *attachment* is used as a general term to refer to either of the following:

- The Asynchronous Communications Single-Line Control feature
- The Asynchronous Communications 8-Line Control feature

When referring specifically to the single-line control feature, the term *single-line attachment* is used. When referring specifically to the 8-line control feature, the term *multiple-line attachment* is used.

Each line operates in a half-duplex mode. If desired, each line can be connected to a full-duplex modem to avoid modem turn-around times. If a line is connected to a full-duplex modem, the attachment still operates in half-duplex mode.



*Modem interface connectors

Note: XXXX = basic device address

Functional Units

Single-Line Feature

Ⓐ I/O (input/output) Channel Attachment Logic

This portion of the attachment performs the handshaking functions that are necessary for communication between the attachment and the processor I/O channel.

Ⓑ Microcontroller

The microcontroller manages everything that the attachment does. It contains a Read Only Storage (ROS) and circuitry that decodes the commands from the processor and automatically steps the attachment through every operation.

Ⓒ Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and sense conditions of the modem and communications line.

Ⓓ Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

Ⓔ SERDES (Serializer/Deserializer)

This is the portion of the attachment that converts the data from parallel form to serial form (transmit operations) and from serial form to parallel form (receive operation).

Ⓕ Bit-Rate Constant Register

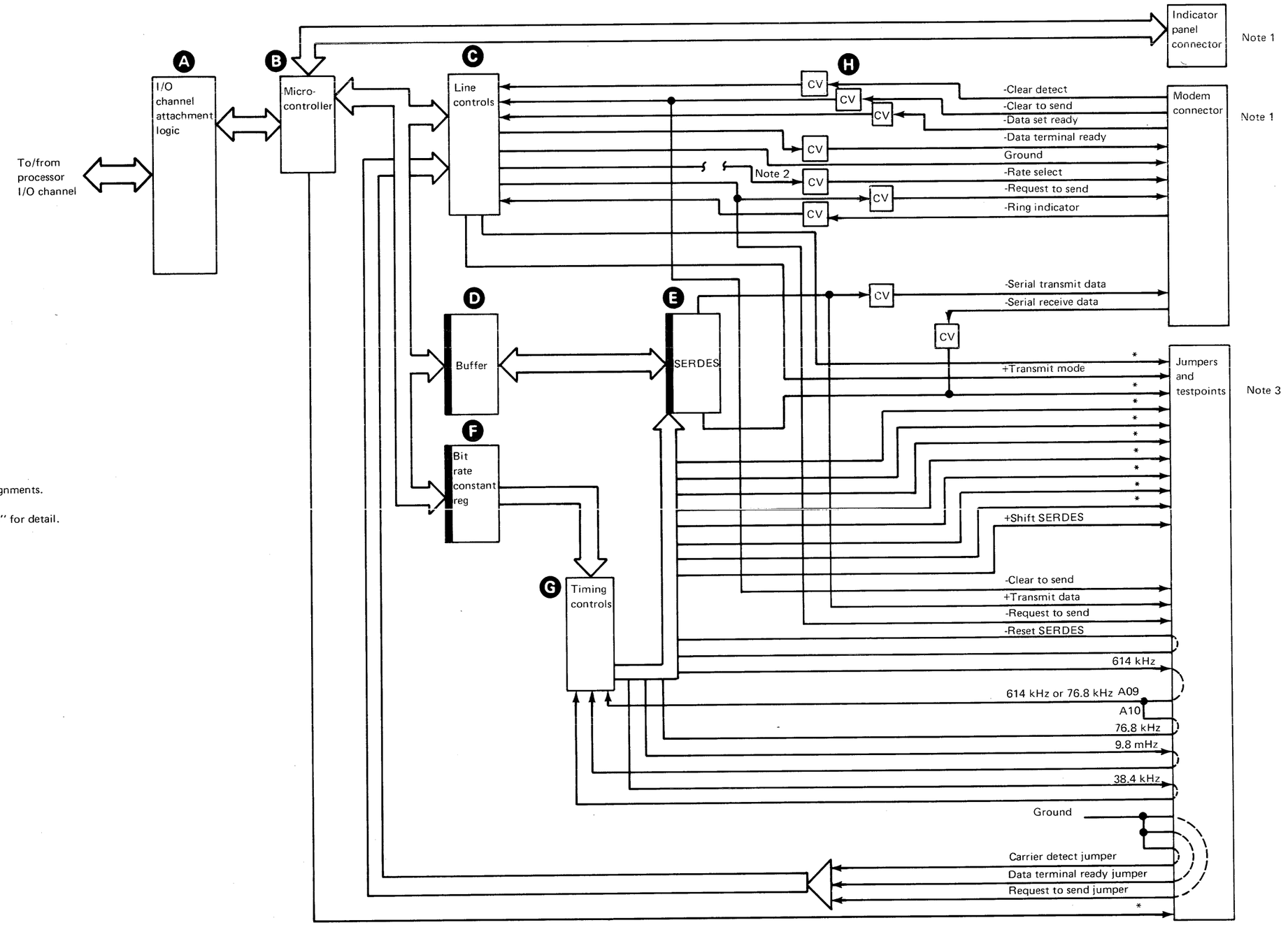
During a Set Control operation, this register is loaded with a hexadecimal constant supplied by the program. The attachment uses this constant to determine the duration of bits and characters to be transmitted and to maintain synchronism of bits within a character while receiving.

Ⓖ Timing Controls

This circuitry provides the timing necessary for the proper shifting of bits through the SERDES; and the transferring of characters between the SERDES and the buffer; and between the buffer and the microcontroller.

Ⓗ Converters (CV)

The converters change the signals going to the modem to signals that are compatible with the modem. They also change signals coming from the modem into signals that are acceptable to the attachment.



Notes:

1. See MLD page SC100 for pin assignments.
2. This lead is not controlled.
3. Refer to "Jumpering Information" for detail.

* Manufacturing test points

Multiple-Line Feature

Ⓐ I/O Channel Attachment Logic

This portion of the attachment performs the handshaking functions that are necessary for communication between the attachment and the processor I/O channel.

Ⓑ Microcontroller

The microcontroller manages everything that the attachment does. It contains a Read Only Storage (ROS), and circuitry that decodes the commands from the processor and automatically steps the attachment through every operation.

Ⓒ Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and communications line.

Ⓓ Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

Ⓔ SERDES (Serializer/Deserializer)

This is the portion of the attachment that converts the data from parallel form to serial form (transmit operations) and from serial form to parallel form (receive operation).

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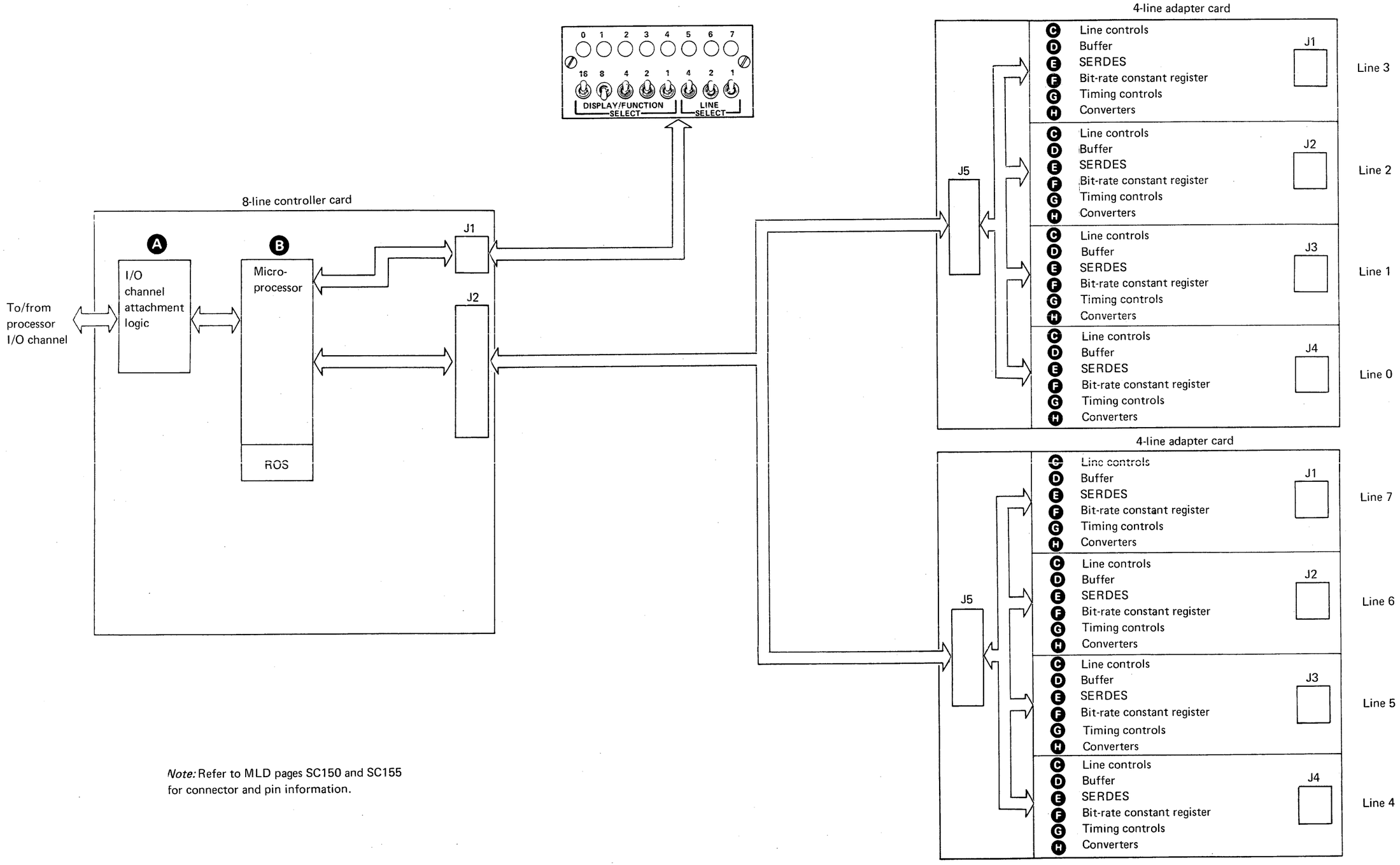


Note: Refer to MLD pages SC150 and SC155 for connector and pin information.

Line Control

Because each remote station might require different line control characters, the asynchronous attachments provide programmable line control characters. These characters are transferred to the attachment by using the device control block (DCB). The DCB that transfers the control characters to the attachment is different from other DCBs. It is identified by bits 11–15 of the control word being set to 01101 (Paper Tape Transmission Code) or 11101 (Eight-Bit Data Interchange Code).

Control Characters

Transmit operations using Paper Tape Transmission Code are terminated when the byte count goes to 0, with the exception of errors or an end-of-block (EOB) data character. On a receive operation, the attachment compares received characters with the programmed line control characters. All recognized control characters that cause a change of direction also cause the attachment to terminate the receive operation that is in progress. This is done with either a normal device-end interrupt request, a DCB command chaining operation, or an exception interrupt request with interrupt status byte bit 0 or 2 equal to 1. All received control characters, except upshift and downshift in Paper Tape Transmission Code, are placed in storage.

PTTC—Receive Mode

The program must initiate a set control operation, specifying (loading) the control characters in the DCB as follows:

Word	DCB (device control block)	
0	/0X0D	
1	Bit rate constant	/16 (EOA)
2	/3D (EOB)	/76 (Ⓨ)
3	/40 (Ⓝ)	/1F Ⓒ, (EOT)
4	/1C (Upshift)	/7C (Downshift)
5	Chain address—must be even	
6	Not used	
7	Not used	
	0	15

COD1/EOA. When the first end-of-address (EOA) Ⓓ character is received, the attachment begins longitudinal redundancy check (LRC) character accumulation, starting with the next character received. The EOA character is placed into storage. Any characters received between the first EOA and the COD 5 Ⓒ character that have the same bit configuration as the EOA are treated as data.

COD2/EOB. When the end-of-block (EOB) Ⓑ character is received, the attachment compares the next character received (which is the LRC character) with the LRC character accumulated by the attachment. If the LRC characters compare, the attachment ends the operation with a normal device end interrupt or begins a DCB chaining operation if chaining was specified (except when an incorrect length record is detected—see "Interrupt Status Byte" later in this chapter). If the LRC characters do not compare, or if a stop-bit error or vertical redundancy check (VRC) error is detected, the attachment ends the operation with an exception interrupt and sets interrupt status byte (ISB) bit 0 on.

Note: The attachment cannot distinguish between terminals that use record checking and those that do not use record checking; therefore, the EOB must not be received when record checking is not used.

COD3 and COD4. The set control DCB should be loaded (by the program) with the positive acknowledgement character COD 3 Ⓨ and the negative acknowledgement character COD4 Ⓝ so that these acknowledgements can be recognized from the remote terminals.

If the attachment is in receive mode, any COD3 or COD4 character received between an EOA and an EOT is treated as data.

If the attachment is in receive response mode (receive response mode is used after a transmit operation to receive the acknowledgement from the receiving station that it has received the data from the transmit station), the attachment recognizes a COD3 or COD4, places it in main storage, and presents a device end interrupt (except when an incorrect length record is detected—see "Interrupt Status Byte" later in this chapter. The program must then examine the character in storage to determine the appropriate action.

COD5/EOT. When the end-of-transmission (EOT) Ⓒ character is received, the attachment ends the operation with a device end interrupt or begins a DCB chaining operation if chaining was specified (except when an incorrect length record is detected—see "Interrupt Status Byte" in this chapter).

COD6/Upshift. When the upshift character (hexadecimal 1C) is received, the attachment places subsequent characters into storage with the high-order bit of each byte on, until a downshift (COD7) character is received or the attachment is reset. The upshift character is not placed in storage.

COD7/Downshift. When the downshift character (hexadecimal 7C) is received, the attachment places subsequent characters into storage with the high-order bit of each byte off, until an upshift (COD6) character is received or the attachment is reset. The downshift character is not placed in storage. All receive operations begin in lowercase.

PTTC Code—Transmit Mode

In transmit mode, all normal ending conditions are controlled by the byte count.

COD 1/EOA. When the end-of-address (EOA) character is transmitted, the attachment begins longitudinal redundancy check (LRC) character accumulation starting with the next character transmitted. Any characters with the same bit configuration as the EOA, occurring between the first EOA and the COD5 character, are treated as data.

COD 2/EOB. When the end-of-block character is transmitted, the attachment recognizes this and follows it with the LRC. If the byte count is 0 when the EOB is transmitted, the attachment presents a device end interrupt or begins a DCB chaining operation if chaining is specified. If the byte count is not 0 the attachment terminates the operation with an exception interrupt and sets interrupt status byte (ISB) bit 0 on and bit 4 on in cycle-steal status word 1.

Note: The attachment cannot distinguish between terminals that use record checking and those that do not use record checking; therefore, the EOB must not be transmitted when record checking is not used.

COD3 and COD4. Any COD3 or COD4 character coming from storage is transmitted as data.

COD5/EOT. Following the transmission of an EOT, the attachment is again able to recognize the EOA character as a control character.

COD6/Upshift and COD7/Downshift. For transmitted data, the shift bit (representing a change from upshift to downshift or downshift to upshift) causes the attachment to generate the appropriate shift character to be inserted into the data stream before the data character is sent.

Note: The attachment does not recognize shift characters from storage; it does not update the shift mode unless the shift bit with the shift character indicates a change. If the bit changes the current case, two shift characters are transmitted.

Eight-Bit Data Interchange Code—Receive Mode

In receive mode, the attachment recognizes any of the seven characters defined in the DCB (as shown below) and treats them as COD characters. When any of the defined characters are received, the attachment presents a device end interrupt request or begins a DCB command chaining operation (except when an incorrect length record is detected—see "Interrupt Status Byte" later in this chapter). All received control characters are placed in storage.

Note: The programmer must ensure that all COD characters are defined in the set control DCB. If they are not defined, hex 00 is treated as a COD character (by default) and terminates the receive operation.

Eight-Bit Data Interchange Code—Transmit Mode

In transmit mode there is no control character comparison. All ending conditions must be controlled by byte count. A device-end interrupt request occurs in transmit mode when the byte count is reduced to 0.

Word		
0	/001D	
1	Bit-rate constant	COD 1
2	COD 2	COD 3
3	COD 4	COD 5
4	COD 6	COD 7
5	Chain address—must be even	
6	Not used	
7	Not used	

Line Error Checking

The attachment performs error checks on received data in Paper Tape Transmission Code mode only. The type of terminal being communicated with and the code being used determine the type of checking used. The attachment performs longitudinal and vertical redundancy checks on the received data, which has odd parity. LRC is performed when the attachment recognizes an EOB character; therefore, do not transmit an EOB if LRC is not being used. The LRC is generated without regard to parity and is the modulo 2 sum of all bits transmitted.

If parity checking is required for Eight-Bit Data Interchange Code, the checking must be done by the program, because no VRC or LRC checking is done in Eight-Bit Data Interchange Code.

The attachment also checks each received character for the correct stop bits—one stop bit for Paper Tape Transmission Code, two stop bits for Eight-Bit Data Interchange Code.

Time-Outs

The attachment has two programmable timers (timer 1 and timer 2). Each timer is controlled by a 16-bit word in the DCB. Both timer values are reduced independently at a rate of 3.33 milliseconds per count. The maximum time that either timer can count is 218.4 seconds. The timers use a count (hex FFFF to 0001) supplied by the program. When the count reaches 0000, the attachment begins or terminates an operation. The timers are used with various operations defined in the control word of the DCB as shown below.

Timer 1

- Receive time-out (see "Receive with Time-Out" under "Operations" later in this chapter)
- Generate answer-tone or break
- Transmit delay
  - Slows down turnaround time (pre-transmit delay)
  - Allows last character to exit modem before dropping 'request to send' (post-transmit delay)
- 'Carrier detect' time-out

Timer 2

- Program delay
- Halt I/O
- 'Clear to send' time-out
- 'Data set ready' time-out
- Ring indicator time-out
- DTR disable delay

For detailed information about the use of the timers with particular operations, see "Device Control Block (DCB)" later in this chapter.

Commands

The Operate I/O instruction points to the IDCB, which contains one of the following commands:

- Prepare
- Device Reset
- Halt I/O
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1
- Start Diagnostic 2
- Start Control

It is the programmer's responsibility to ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

The programmer should exercise care in modifying the DCB words prior to an interrupt request that signifies the end of the operation. The attachment might not have fetched all of the DCB, because it is slower than the Series/1 processor's instruction speeds.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The immediate data field contains the level and I-bit. The single-line attachment is always able to accept and execute a Prepare command, even if it is busy or has an interrupt request pending from a previous command. On a multiple-line attachment, the device returns condition code 1 to this command if it has an interrupt pending, and the I-bit in the IDCB equals 0. The IDCB for the Prepare command has the following format.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*

60

00–FF for multiple-line attachments

00–7F for single-line attachments

Immediate data field		
0's	Level	I
16 ... *26*	*27* ... *30*	*31*

Level. This four-bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27 through 30 indicates priority levels of 0 through 3.

Example:

Bits 27–30	Level
0000	0
0001	1
0010	2
0011	3

A Prepare command issued to any device on a multiple-line attachment gives *all* of the devices in the attachment the same priority interrupt level. The I-bit information applies only to the specific device addressed.

I-Bit. This bit determines whether the device is allowed to present interrupt requests. An I-bit value of 1 permits requests; a value of 0 prevents requests.

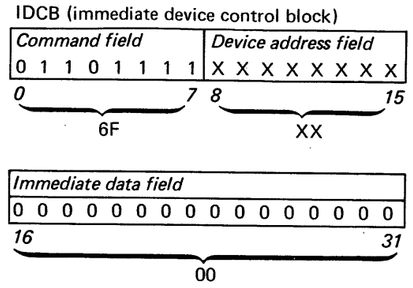
The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset during a system reset or a power-on reset, or is changed by the successful execution of another Prepare command issued to the attachment. The Prepare command causes an interrupt request to be presented if one was pending on the device and the I-bit equals 1.

The Prepare command causes this request only if the attachment is not prepared (I-bit equals 0) and has a request pending upon receipt of a Prepare command with the I-bit equal to 1.

The Prepare command always causes an attachment to respond with either satisfactory (Operate I/O CC7) or device busy (multiple-line controller only, CC1).

Device Reset

The Device Reset command resets the addressed device and clears any pending interrupt requests (except controller end). The Prepare command information, residual address, DTR line, controller-end interrupt, or set control operation's DCB is not affected (see "Status After Resets" later in this chapter). The IDCB for the Device Reset command has the following format:



A Device Reset command issued to the attachment causes the attachment to become "busy" while the reset functions are carried out. The differences between the single-line attachment and the multiple-line attachment are:

- The length of time the attachment is busy performing the reset function
- The method used to report the conclusion to the program

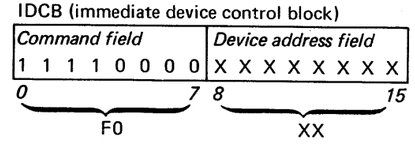
For example, if a Start command follows a Device Reset too closely, a 'busy after reset' (CC2) is reported on a single-line attachment. The program must reissue the command until a 'satisfactory' (CC7) is reported.

On a multiple-line attachment, a 'controller busy' (CC6) is reported when a Start follows Device Reset too closely. When the reset is completed, a 'controller end' interrupt (CC0) is presented by the base address of the multiple-line controller (line 0), at which time the program should reissue the Start I/O command.

Note: Under certain conditions, it is possible that more than one 'controller end' interrupt request is presented. If no busy condition is found upon examining the 'controller busy' queue, disregard the request.

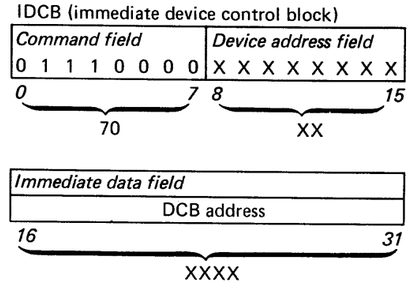
Halt I/O

The Halt I/O command halts all I/O activity on the I/O interface. Any pending interrupt requests, including controller end (CC0), are cleared. The I-bits and priority level do not change, and this instruction performs the same function as a system reset.



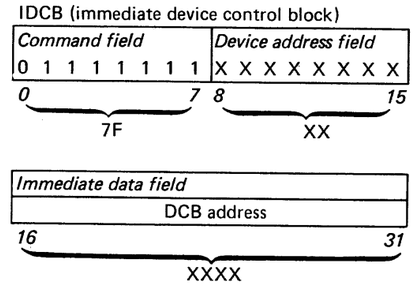
Start

The Start command initiates a cycle-steal operation in the addressed device. The format of the IDCB for the Start I/O command is:



Start Cycle Steal Status

The Start Cycle Steal Status command initiates a cycle-steal operation in the addressed device for the purpose of collecting status information about the previous cycle-steal operation. The format of the IDCB for this command follows.



This command does not allow a chaining operation. The byte count in the DCB (word 6) must be equal to 6 and the data address (word 7) must be on a word boundary (bit 15 off) or an exception interrupt request (CC=2) occurs with DCB specification bit (bit 3) equal to 1 in the interrupt status byte.

See "Cycle-Steal Status Words" later in this chapter for a description of the information transferred to storage by this command.

Read ID

The Read ID command puts the attachment's identification (ID) word into the immediate data field position of the IDCB. The ID word contains physical information about the attachment that is used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming. The format of the IDCB for this command is:

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 0	X X X X X X X X
0 7	*8* *15*
20	XX

Immediate data field
Identification word
16 *31*

Single-line ACC	100E	(single-line)
Two-line ACC	210E	(multiple-lines)
Four-line ACC	220E	
Six-line ACC	230E	
Eight-line ACC	200E	

Note: If the controller card has jumpers installed for addresses that are not present, the controller responds to commands as though the 4-line adapter card was present; therefore, the ID of the controller should match the number of attachment lines present to prevent errors. For example, an ID of 200E defines a multiple-line controller with two 4-line attachments (8 lines). If there is only one 4-line attachment present (4 lines), the ID is 220E.

Diagnostic Commands

Diagnostic commands are used by diagnostic programs to check for correct operation of the attachment. The results of these commands are sensitive to the engineering-change (EC) level of the attachment.

Start Diagnostic 1

The IDCB for this command is shown below:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 1	X X X X X X X X
0 7	*8* *15*
7D	XX

Immediate data field
DCB address
16 *31*
XXXX

Start Diagnostic 2

The IDCB for this command is shown below:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 0	X X X X X X X X
0 7	*8* *15*
7E	XX

Immediate data field
DCB address
16 *31*
XXXX

Start Control

The Start Control command is reserved for use by IBM engineering.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 0	X X X X X X X X
0 7	*8* *15*
7C	XX

Immediate data field
DCB address
16 *31*

Issuing this command to a multiple-line ACCA controller can cause the attachment to become inoperable. If this happens, the attachment can only be restored to operation by turning power off, and then on again.

Device Control Block (DCB)

The DCB is an eight-word area in main storage that describes the specific parameters of the operation. Its location in storage is assigned by the program. The DCB address transferred to the attachment through the IDCB points to word 0. The address of the DCB must be even. If the DCB address is odd, the attachment sets interrupt status byte bit 1 equal to 1 (Delayed Command Reject) and terminates the operation with an exception interrupt request. The DCB is fetched by the attachment, using a cycle-steal address key of 000 after issuing a Start, Start Cycle Steal Status, Start Control, or Start Diagnostic command. The format of the DCBs for a Start Cycle Steal Status commands follow:

Word	DCB (device control block)
0	Control word
1	Not used
2	Timer 1
3	Timer 2
4	Not used
5	Chain address
6	Byte count
7	Data address

0 15

Format of the DCB for a Start command

Word	DCB (device control block)	
0	*Control word* 0 0 1 0 0	*Addr key* X X X 0 0 0 0 0 0 0 0
1	Not used	
2	Not used	
3	Not used	
4	Not used	
5	Not used	
6	Byte count—must be 0006	
7	Data address	

0 15

Format of the DCB for a Start Cycle Steal Status command

Word	DCB (device control block)	
0	/000D or /001D	
1	Bit-rate constant	COD1
2	COD2	COD3
3	COD4	COD5
4	COD6	COD7
5	Chain address—must be even	
6	Not used	
7	Not used	

0 15

Format of the DCB for a Set Control command

Control Word 0

The control word is located in word 0 of the DCB. This word delineates the cycle-steal operation. The format of the control word for the Start command follows.

Bit 0—Chaining Flag. If this bit equals 1, the attachment fetches the next DCB in the chain after completing the current DCB operation.

Bit 1. This bit is not used and must equal 0.

Bit 2—Input Flag. This bit indicates the direction of data transfer. If bit 2 equals 1, data is transferred from the attachment to the processor; if bit 2 equals 0, data is transferred from the processor to the attachment.

Bits 3 and 4. These bits are not used and must equal 0.

Bits 5 Through 7—Cycle-Steal Address Key. This is a three-bit key presented by the attachment during data transfers. It is used by the processor to determine if the attachment can access certain areas of storage.

Bits 8 and 9. These bits are not used and must equal 0.

Bits 10–15—Operation. The attachment decodes these bits to determine which of the following operations is to be performed:

10	11	12	13	14	15	
0	0	0	0	0	0	Transmit
0	0	0	0	0	1	Transmit end
0	0	0	0	1	0	Transmit allow break
0	0	0	0	1	1	Transmit end allow break
0	0	0	1	0	0	Receive
0	0	0	1	0	1	Receive with time-out
1	0	0	1	0	0	Receive response
1	0	0	1	0	1	Receive response with time-out
0	0	0	1	1	0	Ring enable
0	0	0	1	1	1	Ring enable with time-out
0	0	1	0	0	0	DTR enable
0	0	1	0	0	1	DTR enable with time-out
0	0	1	0	1	0	DTR enable with answer-tone
0	0	1	0	1	1	DTR enable with answer-tone and time-out
0	0	1	1	0	0	DTR disable
0	0	1	1	0	1	Set control Paper Tape Transmission Code
0	1	1	1	0	1	Set control eight-bit data interchange
0	0	1	1	1	0	Program delay
0	0	1	1	1	1	Reset

Operations

The following paragraphs describe the operations specified by bits 10–15 of the DCB control word. Before issuing a transmit-type command, the programmer should ensure that the program has issued Prepare (I-bit equal to 1), Set Control, and Enable commands to ensure that the attachment is ready and configured to execute all commands.

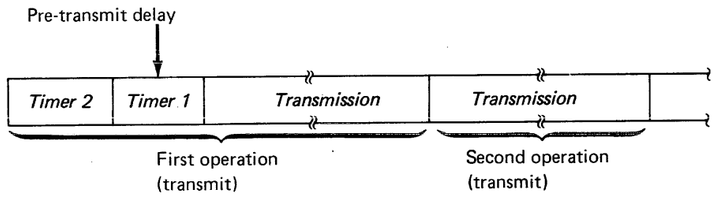
Transmit. This operation is used when another transmit type of operation is to follow immediately.

The attachment begins this operation by sending 'request to send' (RTS) to the modem and starting timer 2. The attachment then waits for 'clear to send' (CTS) from the modem. When the attachment gets 'clear to send,' it resets timer 2, starts timer 1, and waits for timer 1 to time-out. When timer 1 times out, the attachment begins fetching data from storage and transmitting the data to the remote station. The delay provided by timer 1, in this case, is called "pre-transmit delay"; its purpose is to allow the receiving station enough time to prepare to receive data and to allow time for the modem and communication lines to stabilize.

Timer 2 should be set to a value high enough to allow turnaround on a half-duplex teleprocessing link. If timer 2 is not correctly defined by the program, an exception interrupt request (CC2) occurs. With interrupt status byte bit 0 equal to 1, status word 1 of the attachment reports a modem interface error (bit 9 equals 1) indicating that RTS was active and that CTS was not returned by the modem within the time limits of timer 2.

The attachment presents a device-end interrupt request or begins a DCB command chaining operation when the byte count goes to 0. The attachment stays in transmit mode and leaves its RTS active at the end of this operation. This allows continuity from one transmit type of operation to another without sending another RTS and waiting for CTS.

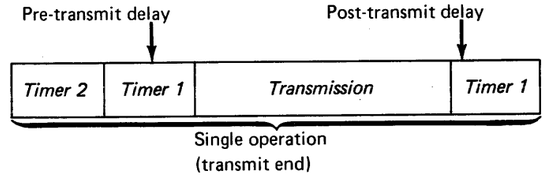
When chaining a series or transmit-type operations, timers 1 and 2 are used in the first operation only.

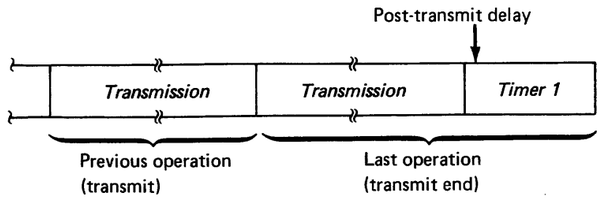


Note: Timer 1 should be set for a pre-transmit delay of approximately 9 milliseconds when the receiving station is a program-controlled device and is directly connected or connected through a full-duplex modem. Timers 1 and 2 should always be specified to prevent excessive turnaround times and noise.

Transmit End. This operation is used to transmit the last block of data in a chain of transmit-type operations or when only one block is being transmitted.

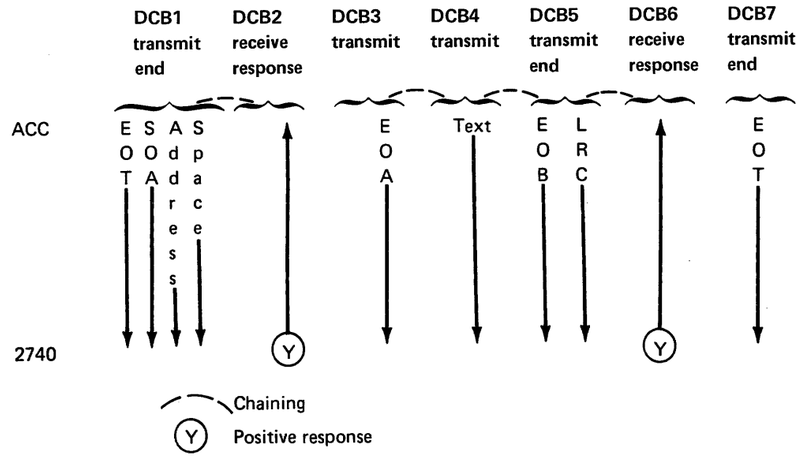
This operation is the same as the transmit operation, except that the attachment exits transmit mode and starts timer 1 after the last character is sent to the modem. When timer 1 times out, the attachment resets its RTS (if RTS is *not* wired "on"). This delay allows the last character to leave the modem before the attachment resets its 'request to send.' The timer 1 delay at the end of this operation is called "post-transmit delay." Note that timer 1 is used twice in this operation (pre-transmit and post-transmit delays) if this operation is not part of two or more transmit-type operations.





Transmit Allow Break. This operation is the same as the transmit operation, except that it allows the receiving station to stop the transmission. To do this, the receiving station "breaks" the line by driving its transmit line to a "space" condition for at least 150 milliseconds. If the attachment detects this condition, it presents an exception interrupt request with bit 0 equal to 1 in the interrupt status byte. Status word 1 bit 6 is equal to 1 to indicate a break.

Transmit End Allow Break. This operation is the same as the transmit-end operation, except that this operation allows the receiving station to stop the transmission. To do this, the receiving station "breaks" the line for at least 150 milliseconds. If the attachment detects this condition, it resets transmit mode and RTS, and presents an exception interrupt request with bit 0 equal to 1 in the interrupt status byte. The attachment does not reset RTS if it is wired "on."



An example of using ACC operations

Receive. This operation allows the attachment to begin placing data into storage when the attachment begins receiving valid data. If the 'carrier detect' jumper is installed, 'carrier detect' from the modem must be active before the attachment can begin transferring data to storage.

If while receiving, the attachment detects a VRC or stop-bit error, it places hex 00 into storage instead of the incorrect character. If the communications indicator panel is connected to the attachment and the DISPLAY/FUNCTION SELECT switches are set to 11110, the attachment places the character into storage "as is."

In PTTC mode, the attachment checks every character it receives to see if the character is a COD2, COD3, COD4, or COD5 character. In Eight-Bit Data Interchange Code, the attachment checks all COD characters. The attachment presents a device-end interrupt request or begins a DCB command chaining operation when it recognizes a COD character and the byte count goes to 0.

If the byte count goes to 0 before a COD is received, this is a long record. If a COD is received before the byte count goes to 0, this is a short record. Either condition terminates the operation with an exception interrupt request.

Before beginning this operation, transmit mode must be off and DSR must be on. The following chart shows the ending conditions for receive operations.

Note: Chaining is not allowed between two receive operations.

Input conditions				Receive termination		
Error condition (See Note)	Chain flag	Byte count=0	COD received	CC	ISB/IIB	Comment
No	No	No	Yes	2	A0	
No	No	Yes	No	2	20	
No	No	Yes	Yes	3	00	
No	Yes	No	Yes	2	A0	No chain
No	Yes	Yes	No	–	–	Chain to next DCB
No	Yes	Yes	Yes	–	–	Chain to next DCB
Yes	No	No	Yes	2	A0	
Yes	No	Yes	No	2	A0	
Yes	No	Yes	Yes	2	80	
Yes	Yes	No	Yes	2	A0	No chain
Yes	Yes	Yes	No	2	A0	No chain
Yes	Yes	Yes	Yes	2	80	No chain

Note: LRC and VRC errors can occur only in PTTC mode. LRC, VRC, and stop-bit error exception interrupts occur at the completion of the operation for the present DCB.

Receive With Time-Out. This operation is the same as the receive operation, except that the attachment uses timer 1 to limit the time it will wait for the first character. It also limits the time between characters. Failure to receive a character within this time results in an exception interrupt request with bit 0 equal to 1 in the interrupt status byte and status word 1 bit 1 equal to 1. If the 'carrier detect' jumper is installed, the attachment allows the time specified by timer 1 for 'carrier detect' to become active. If 'carrier detect' does not become active within the specified time, the attachment presents an exception interrupt request and posts modem interface error (bit 9) in cycle-steal-status word 1. Timer 1 is restarted after each character is received and also after 'data carrier detect' is detected.

Receive Response. This operation is used with Paper Tape Transmission Code when LRC checking is being used. It is used to receive the positive or negative response to a transmit operation.

This operation is the same as the receive operation, except that when the attachment is in receive response operation, it always recognizes the COD3 and COD4 characters. These are the low-order byte of word 2 and the high-order byte of word 3 in the set control operation's DCB. For a detailed description of the COD3 and COD4 characters, refer to "PTTC—Receive Mode" earlier in this chapter.

Receive Response With Time-Out. This operation is the same as the receive response operation, except that the attachment uses timer 1 to limit the time that the attachment waits to receive the response. 'Carrier detect' and character time-out are identical to the receive with time-out operation.

Ring Enable. This operation is used in switched-line applications. It allows the attachment to recognize that it is being called by another station. The attachment cannot accept another operation until either a call is received or the device is reset. When the attachment detects a "ring," it presents a device-end interrupt request or begins a DCB command chaining operation. This operation should logically chain to a 'DTR enable' type of command. Status word 2, bit 4 (ring indicator), is set upon detection of a ring signal. The 'ring enable' operation does not "enable" the adapter; it only notifies the program that a "ring" was detected. Logically, the program should either chain to or issue a DTR enable-type DCB operation to establish a connection with the switched-line modem.

Ring Enable With Time-Out. This operation is the same as the ring enable operation except that the attachment uses timer 2 to limit the time it will wait for a "ring." If timer 2 times out, the attachment presents an exception interrupt request with interrupt status byte bit 0 equal to 1 and status word 1, bit 1 (time-out), equal to 1.

DTR Enable. This operation causes the attachment to activate the 'data terminal ready' (DTR) line. DTR must be active for any transmit or receive operation to take place. When the attachment receives 'data set ready' (DSR) from the modem, it presents a device-end interrupt request or begins a DCB command chaining operation. The attachment also presents an interrupt request or begins a DCB command chaining operation if DSR is already active.

Note: DTR is normally wired on for leased lines and must not be wired for switched lines.

DTR Enable With Time-Out. This operation is the same as the DTR enable operation except that the attachment uses timer 2 to limit the time that it will wait for DSR to be returned from the modem. If timer 2 times out before DSR becomes active, the attachment presents an exception interrupt request, sets interrupt status byte bit 0 equal to 1, and sets status word 1 bit 9 (modem interface error) equal to 1.

DTR Enable With Answer-tone. This operation is the same as the DTR enable operation, except that the attachment places an answer-tone on the transmit line when DSR becomes active. The duraction of the answer-tone is determined by timer 1. The attachment presents a device-end interrupt request or begins a DCB command chaining operation when the timer 1 time-out occurs. Timer 1 should be set for approximately 3 seconds for this operation. The exact setting depends on the modem being used. Consult the manual about the modem to determine the correct length of the answer-tone.

This operation can be used to generate a break condition to a terminal. This command is valid when connected to a full-duplex type data set or when directly connected to a terminal with a break feature installed.

DTR Enable With Answer-tone and Time-Out. This operation combines the functions of the DTR enable with answer-tone and DTR enable with time-out operations.

DTR Disable. This operation causes the attachment to deactivate the DTR line to the modem. The modem then disconnects itself from a switched network. The attachment starts timer 2 at the same time that it deactivates DTR. When the time-out occurs, the attachment presents a device-end interrupt request or begins a DCB command chaining operation. Timer 2 should be set for at least 5 seconds to ensure that DSR has been deactivated. This operation should not be used in a leased-line application. For a leased-line operation, the DTR jumper should be installed on the attachment and one 'DTR enable' instruction should be issued at IPL time. If the enable instruction fails, a problem exists in the leased line data set (powered off).

Set Control PTTC. This operation performs four functions:

- It places the attachment in Paper Tape Transmission Code mode.
- It loads the bit-rate constant from word 1 of the DCB into the attachment's clock register.
- It loads the line-control characters from the DCB into registers in the attachment for use in transmit and receive operations. This enables the program to specify the bit pattern of all the line control characters. See "Line Control" earlier in this chapter for the location of the line control characters in the DCB.
- It sets the attachment for seven-bit code with a one-stop-bit operation.

The attachment presents a device-end interrupt request or begins a DCB command chaining operation at the end of this operation. The control information in the attachment remains unchanged until another set control operation is performed, or until a power-on reset occurs.

CAUTION: All seven COD characters must be defined or a hex 00 is decoded as a turnaround character.

Set Control Eight-Bit Data Interchange. This operation is the same as the set control operation that uses Paper Tape Transmission Code except that this operation places the attachment in eight-bit data interchange mode. It sets up eight-bit code and two stop bits.

CAUTION: All seven COD characters must be defined or a hex 00 is decoded as a turnaround character.

Program Delay. This operation allows the program to use timer 2. The attachment loads the value specified in DCB word 3 into timer 2 and starts the timer. When the time-out occurs, the attachment presents a device-end interrupt request or begins a DCB command chaining operation.

DCB Command Reset. This operation resets an individually addressed device. The prepare command information, the information supplied by the set control operation, and DTR are not reset by this operation. A device-end interrupt request occurs or a DCB command chaining operation begins when the reset is complete. Note that this DCB causes the device to be busy and should not be confused with an IDCB reset.

Bit-Rate Constant

An eight-bit hexadecimal number is used to control the bit rate within a range.

The single-line attachment runs at speeds from 37.5 to 1,200 bps (low range) with the low-speed jumper installed on the feature card. It runs at speeds from 300 to 9,600 bps (high range) with the high-speed jumper installed.

In a multiple-line attachment, the low-speed and high-speed jumpers are located on the Asynchronous Communications 4-Line Adapter cards. There is only one set of jumpers on each 4-line adapter card; therefore, if the high-speed jumper is installed on a 4-line adapter card, all lines associated with that card must run at speeds between 300 and 2,400 bps.

The bit-rate constant is supplied to the attachment by the program. The constant is taken from the high-order byte of DCB word 1 and stored in the attachment during a set control operation.

The bit-rate constant for low-range operation is determined by the following formula:

$$\text{Constant} = \frac{9600}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

Example: Determine the bit-rate constant for 150 bps.

$$\frac{9600}{150} - 1 = 63 \text{ (decimal)} = 3F \text{ (hexadecimal)}$$

The hexadecimal constant supplied by the program in conjunction with the set control operation is 3F.

The bit-rate constant for high-range operation is determined by the following formula:

$$\text{Constant} = \frac{76800}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

Example: Determine the bit rate constant for 1,200 bps (with high-speed jumper installed).

$$\frac{76800}{1200} - 1 = 63 \text{ (decimal} = 3F \text{ (hexadecimal)}$$

The hexadecimal constant supplied by the program in conjunction with the set control operation is 3F.

Note: The high-speed jumper should be installed when operating at speeds over 300 bps.

There are some bit rates in the ranges mentioned previously that are incompatible with the attachment. The difference between the bit rate of the attachment and the bit rate of the attached terminal must not exceed 1.5 percent. To determine the difference (in percent), use one of the following methods. An example follows method 2.

Method 1—For attachments that have the low-speed jumper installed.

Step 1. Divide the terminal's bit rate into 9,600 and round the answer to the nearest whole number.

Step 1. Multiply the above answer by 0.000104166. This gives the attachment's bit time.

Step 3. Determine the terminal's bit time by taking the reciprocal of the terminal's bit rate.

Step 4. Divide the smaller of the bit times by the larger of the bit times. Subtract the answer from 1. Multiply this answer by 100. This gives the percentage of difference between the bit rate of the terminal and the actual bit rate of the attachment for a given constant.

Method 2—For attachments that have the high-speed jumpers installed. Compute the difference in the same manner as method 1, making the following substitutions:

Step 1. Substitute the number 76,800 for 9,600.

Step 2. Substitute the number 0.0000130208 for 0.000104166.

Example: Determine the difference between the bit rate of the attachment and the bit rate of a terminal that operates at 134.5 bps.

Step 1 $\frac{9600}{134.5} = 71.37 = 71$

Step 2 0.000104166
X 71
0.007395786 = attachment's bit-time

Step 3 $\frac{1}{134.5} = 0.007434944$ = terminal's bit-time

Step 4 $(1 - \frac{0.007395786}{0.007434944})\ 100 = 0.53\%$

Therefore, a terminal with a bit rate of 134.5 bps is compatible with the attachment.

Timer 1

Timer 1 is used by the program to control the following:

- Receive time-out
- Generate answer-tone or break
- Transmit delay
  - Slows down turnaround time (pre-transmit delay)
  - Allows last character to exit modem before dropping RTS (post-transmit delay)
  - 'Carrier detect' time out

For detailed information about the use of timer 1 with specific operation, see "Device Control Block (DCB)" in this chapter.

Timer 2

Timer 2 is used the program to control the following:

- Program delay
- Halt I/O
- 'Clear to send' time-out
- 'Data set ready' time-out
- Ring indicator time-out
- DTR disable delay

For detailed information about the use of timer 2 with specific operation, see "Device Control Block (DCB) in this chapter.

Chain Address

The chain address word (DCB word 5) contains the storage address of the next DCB when chaining is indicated. The address of the chain-to DCB must be even. If it is odd, the attachment sets interrupt status byte bit 3 equal to 1 and terminates the operation with an exception interrupt request. DCB word 5 must always have an even address (chaining bit may or may not be set).

Byte Count

The byte count is a 16-bit word (DCB word 6) that contains an unsigned integer representing the count for this data transfer. The count is always specified in bytes.

Data Address

This word (DCB word 7) contains the storage address of the first data transfer for the operation being performed.

Interrupt Status Byte

When the attachment presents an interrupt request to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by the condition codes. The attachment presents the interrupt status byte to the processor as bits 0 through 7 of the interrupts ID word.

The bits and their meanings follow.

0	1	2	3	4	5	6	7
Device dependent status available	Delayed command reject	Incorrect length record	DCB specification check	Storage data check	Invalid storage address	Protect check	Interface data check

Bit 0—Device-Dependent Status Available. If this bit equals 1, additional status is available by using the Start Cycle Steal Status command (described later in this chapter). This bit may be set equal to 1 in conjunction with bit 2 (incorrect length record).

Bit 1—Delayed Command Reject. This bit is set equal to 1 for either of the following conditions:

- The IDCB contains an odd DCB address.
- The IDCB contains an invalid function/modifier.

Bit 2—Incorrect Length Record. This bit is reported only during receive operations. If interrupt status byte bit 0 equals 0 and bit 2 equals 1, the byte count has gone to 0 and the attachment has not received a change of direction (COD) character. If interrupt status byte bits 0 and 2 both equal 1, the attachment received a COD character and the byte count was not 0.

Bit 3—DCB Specification Check. This bit equals 1 under any of the following conditions:

- The DCB contains an odd chaining address (DCB word 5).
- The byte count (DCB word 6) contains a value other than 6 for a Start Cycle Steal Status command.
- The data address (DCB word 7) contains an odd address for a Start Cycle Steal Status command.
- The byte count for a transmit or receive operation is 0.
- Bit 2 of the DCB control word (word 0) is not set appropriately for the operation.
- The single-line attachment diagnostic DCB has the I/O bit set to 0 in the control word (odd data address).

Bit 4—Storage Data Check. This bit equals 1 during cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained incorrect parity. The parity in main storage is not corrected. The attachment terminates the operation.

Bit 5—Invalid Storage Address. This bit equals 1 if the storage address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation.

Bit 6—Protect Check. This bit equals 1 if the attachment attempted to access a storage location without the correct cycle-steal address key. The attachment terminates the operation.

Bit 7—Interface Data Check. This bit equals 1 if a parity error was detected on an interface during a cycle-steal data transfer. The condition can be detected by the processor I/O channel or the attachment. In either case, the operation is terminated and an exception interrupt requested is presented to the processor.

Cycle-Steal Status Words

Three words of status information are available by using the Start Cycle Steal Status command. This information is available regardless of the setting of interrupt status byte bit 0.

Three words (six bytes) of status information are transferred into main storage, starting at the data address contained in DCB word 7. Status words 1 and 2 are the only words required for analysis of attachment or terminal link errors.

Cycle steal status words

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word 0	Residual address															
Word 1	Overrun	Time out	Block check error	DCB reject	EOB, count not zero	VRC error	Break detect	Stop-bit error	———	Modem interface error	———	———	———	———	———	———
Word 2	Data terminal ready	Data set ready	Request to send	Clear to send	Ring indicator	Receive mode	Zeros									

Word 0

Word 0 contains the main storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or DCB address. The value of the residual address must be examined to determine if it is a data address or a DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Word 1

Bit 0—Overrun. During a receive operation, this bit equals 1 if the attachment is not able to transfer data to storage before the storage data register is needed for new data.

During a transmit operation, this bit equals 1 if the attachment is unable to fetch new data from storage in time to keep a steady stream of data going out on the line. Examine the bit rate being sent to the attachment and correct it with a new set-control DCB.

Bit 1—Time-Out. This bit equals 1 if:

- During a receive with time-out or a receive response with time-out operation, no data is received within the limits established by timer 1.
- During a ring enable with time-out operation, 'ring indicator' is not received from the modem within the limits of timer 2.

Increase timer 1 value during a ring enable with time-out. If a ring signal was not received within the limits of timer 2, increase the value of timer 2 and retry.

Bit 2—Block Check Error. The LRC character received does not compare with the LRC character accumulated by the attachment (Paper Tape Transmission Code mode only). Transmit a negative acknowledgement and retry.

Bit 3—DCB Reject. This bit equals 1 under either of the following conditions:

- A transmit-type operation is attempted when the attachment is in receive mode.
- A receive-type operation is attempted when the attachment is in transmit mode.

Examine receive mode bit 5 in status word 2, issue a device reset, and retry.

Bit 4—EOB and Count Not Zero. In transmit mode, an EOB was transmitted and the byte count was not 0 (Paper Tape Transmission Code mode only). Examine the transmit data for an EOB; remove the EOB and retry.

Bit 5—VRC Error. The parity of a received Paper Tape Transmission Code character was incorrect. The error interrupt request is presented at the end of the message.

A special character (hex 00) is placed in main storage when any incorrect data is detected. If the communications indicator panel is installed and the DISPLAY/FUNCTION SELECT switches are set to 11110, the received character is placed in storage without any modifications to the character. The interrupt request does not occur until a COD is detected, or the byte count is reduced to 0 and the chain bit equals 0.

Transmit a negative acknowledgement and retry.

Bit 6—Break Detected. During a transmit allow break or transmit end allow operation, a "break" condition was detected. The attachment resets transmit mode and 'request to send' (if RTS is not wired "on"). Programmers can write a program that can issue either a Receive command or continue transmitting.

Bit 7—Stop-Bit Error. A character was received with a stop bit missing. The interrupt request does not occur until the count is reduced to 0 or a COD character is received. This error is reported if the operator presses the "break" key on a terminal and the adapter is in receive mode.

The incorrect character is replaced in main storage with a special character (hex 00). If the communications indicator panel is installed and the DISPLAY/FUNCTION SELECT switches are set to 11110, the received character is placed in storage without any modifications to the character. The interrupt request does not occur until a COD is detected, or until the byte count is reduced to 0 and the chain bit equals 0.

The programmer should transmit a negative acknowledgement and retry.

Bit 8. This bit always equals 0.

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Bit 9—Modem Interface Error. Conditions that cause this error are:

- DSR is not received from the modem within the predetermined time after an enable-with-timer operation begins.
- DTR or DSR is inactive at the beginning of a transmit or a receive operation or goes inactive during a transmit or receive operation.
- CTS is active for more than 1 second while RTS is inactive at the beginning of a transmit operation.
- RTS or CTS is lost during a transmit operation.
- 'Carrier detect' becomes inactive during a receive operation, or 'carrier detect' does not become active within the time specified by timer 1 at the beginning of a receive with time-out operation. The conditions are applicable only when the 'carrier detect' jumper is installed.

Note: If a modem interface error is reported, the programmer should examine status word 2 and retry. If DTR equals 1, the attachment expects DSR to equal 1; if RTS equals 1, the attachment expects CTS to equal 1.

Bits 10–15. These are not used and must equal 0.

Note: More than one error may be reported in status word 1. An example is a block check error with a VRC error.

Word 2

Bit 0—Data Terminal Ready. This is an outbound signal from the attachment to the modem indicating readiness to communicate.

Bit 1—Data Set Ready. This bit is an inbound signal to the attachment from the modem indicating that power is on and the modem is ready to communicate.

Bit 2—Request to Send. This is an outbound signal from the attachment to the modem when transmit mode is active. Expect a CTS (bit 3) returned from the modem.

Some full-duplex modems always signal CTS as a power-on indication; in this case, the RTS jumper on the attachment should be installed.

Bit 3—Clear to Send. This is an inbound signal to the attachment from the modem in response to an RTS (bit 2) signal.

Bit 4—Ring Indicator. This is an inbound signal to the attachment from the modem signalling that the phone is ringing. The attachment only senses this signal during any ring-enable command.

Bit 5—Receive Mode. This bit equals 1 when the attachment is in receive mode. This bit equals 0 when the attachment is in transmit mode. Examine this bit if status word 1 bit 3 (DCB reject) is reported.

Bits 6–15. Not used.

Jumpering Information

The following options can be selected by installing jumper wires on the feature cards.

Asynchronous Communications Single-line Control Feature

Ⓐ Request to Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full—duplex modem. This option should always be selected when using a modem which always keeps 'clear to send' active.

Ⓑ Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

Ⓒ Speed Range Jumpers

These jumpers are mutually exclusive; that is, one or the other must be selected, but not both.

Low Range

With this jumper installed, speeds between 37.5 bps and and 1,200 bps can be selected by programming. However, it is recommended that the high range jumper be used for speeds above 300 bps.

High Range

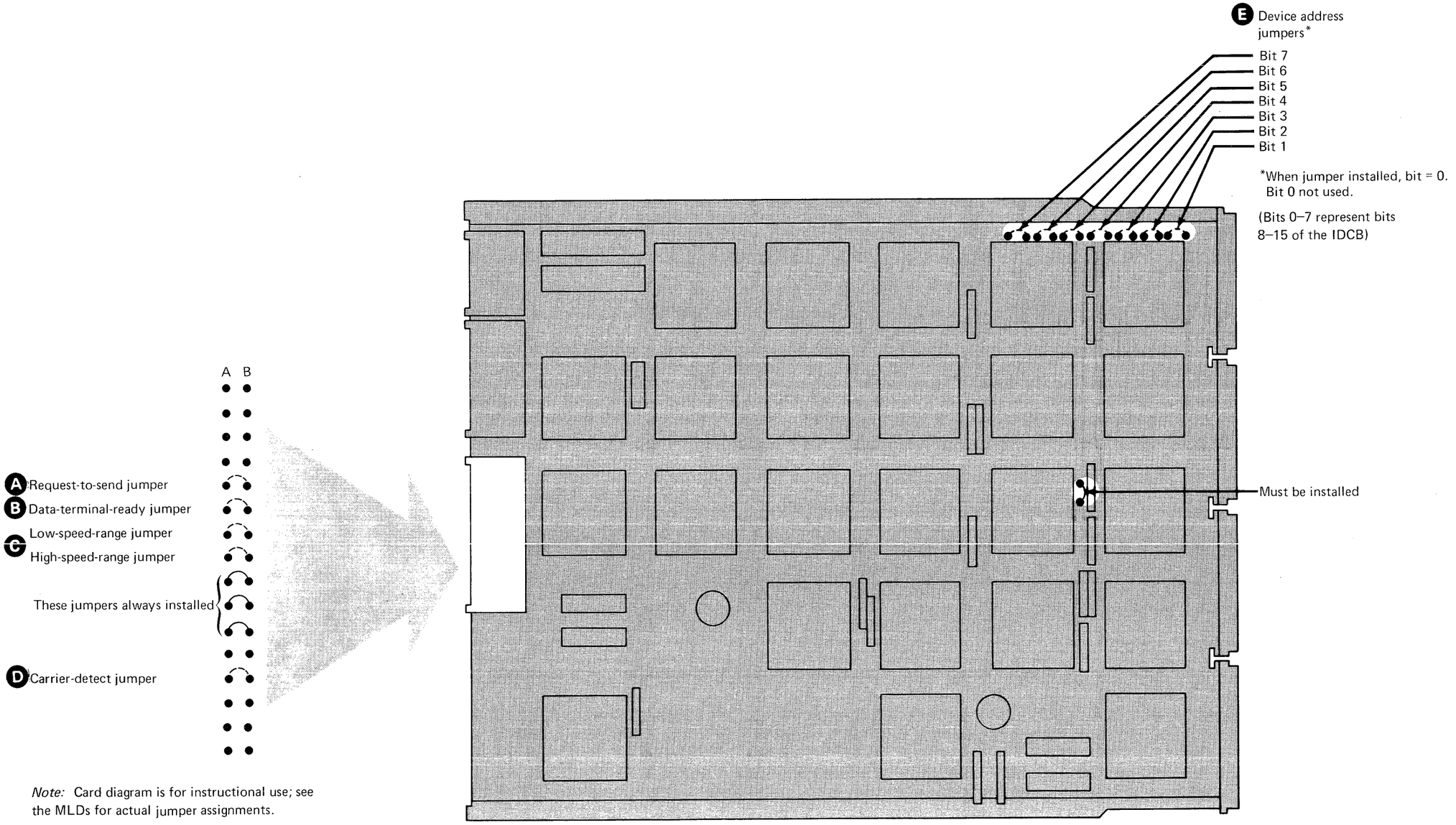
This jumper all the program to select the rates between 300 bps and 9,600 bps.

Ⓓ Carrier Detect

Some modems offer the ability to check the quality of the received signal. When the signal is of acceptable quality, the modem generates the signal 'carrier detect'. If the received signal starts to deteriorate, the modem notifies the attachment by deactivating 'carrier detect'. If the 'carrier detect' jumper is installed on the attachment card, the attachment waits for 'carrier detect' at the beginning of a receive type of operation. If 'carrier detect' does not become active within the specified time (timer 1) or if it becomes inactive during the receive operation, the attachment presents an exception interrupt and signals "modem interface error" to the processor.

Ⓔ Device Address

These jumpers select the address of the attachment on the Series/1 I/O interface.



Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

Asynchronous communications single-line control feature

Asynchronous Communications 4-Line Adapter Feature

Ⓐ Request to Send

There are four RTS jumpers on the card—one for each line. The jumpers perform the same functions as described for single-line attachments.

ⒷData Terminal Ready

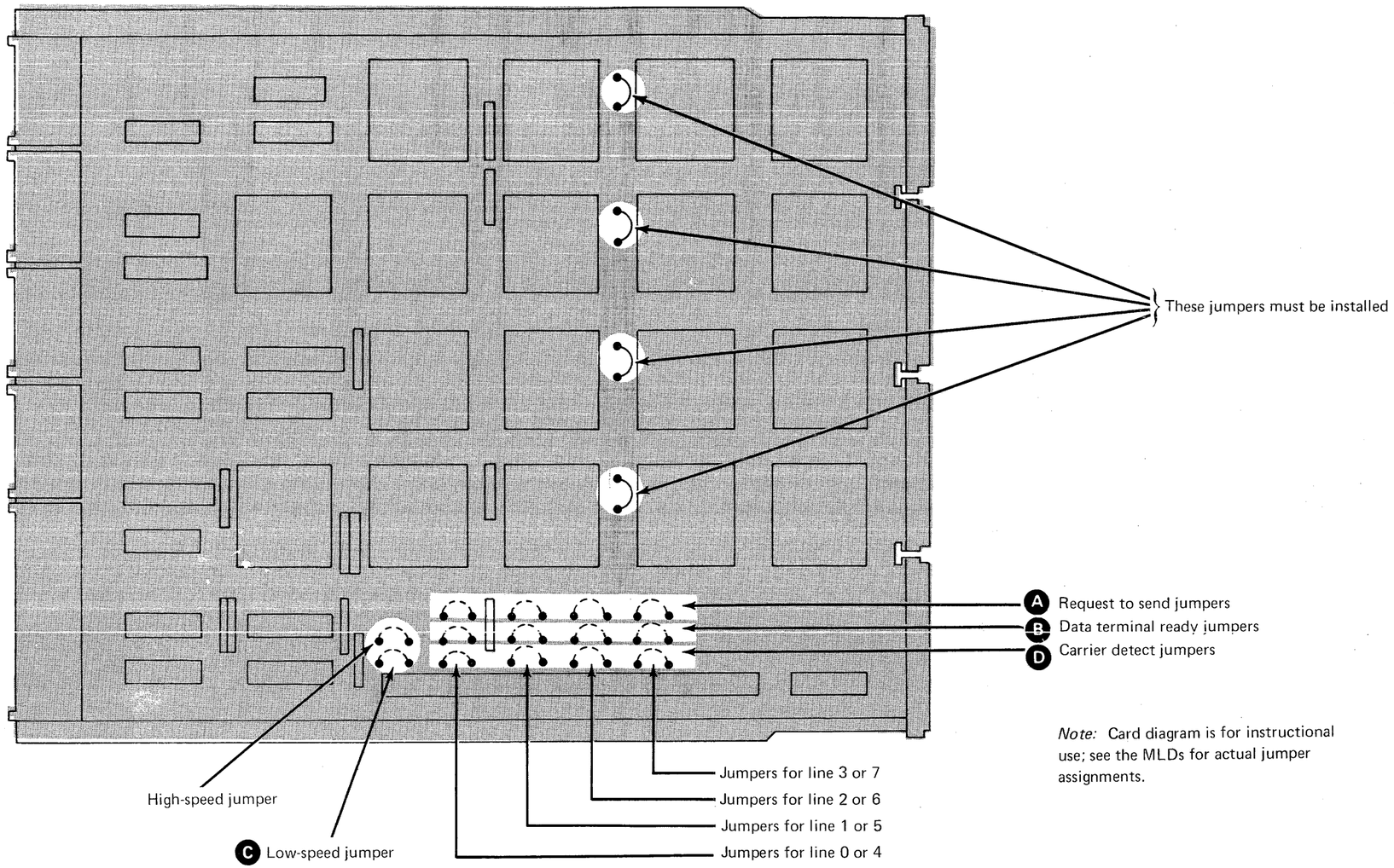
There are four DTR jumpers on the card—one for each line. The jumpers perform the same functions as described for single-line attachments.

Ⓒ Speed Range Jumpers

There is only one set (1 low range and 1 high range) of jumpers for the entire card. Therefore, all four lines on the card must run within the same range. The function of these jumpers is the same as previously described for the single-line attachment, except that the maximum bit rate in high range is 2,400 bps.

Ⓓ Carrier Detect

There are four carrier detect jumpers on the card—one for each line. The jumpers perform the same functions as described for single-line attachments.



Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

Asynchronous communications 4-line adapter feature

Asynchronous Communications 8-Line Control Feature

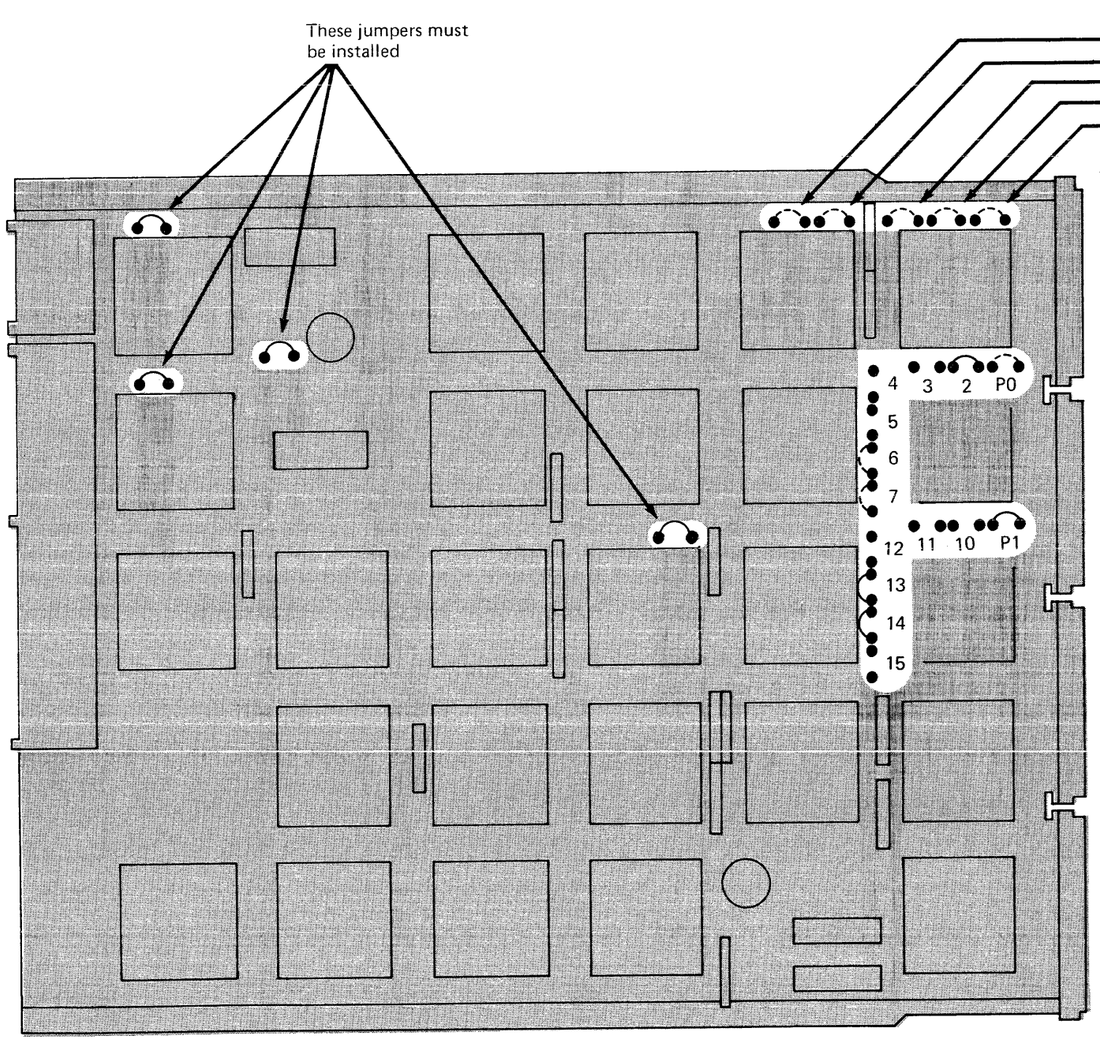
Ⓐ Device Address

These jumpers select the address of line 0 on the Series/1 I/O interface.

Ⓔ ID Jumpers

These jumpers determine the information that the attachment will pass to the processor during the Read ID instruction. The jumpers should be as follows:

Bit 2	On
Bits 3–5	Off
Bits 6 & 7	These are determined by the number of lines installed. 2 lines—bit 6 off, bit 7 on 4 lines—bit 6 on, bit 7 off 6 lines—bit 6 on, bit 7 on 8 lines—bit 6 off, bit 7 off
Bit P0	Jumpered as required to maintain odd parity in the high order byte of the ID word
Bits 10, 11, P1	Off
Bits 12–14	On



Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

Asynchronous communications 8-line control feature

Status After Resets

There are several methods of resetting some or all of the circuits in the attachment. The resets and their effects are shown in the following chart:

	DTR with jumper	DTR w/o jumper	RTS with jumper	RTS w/o jumper	Interrupt level	I-bit	Set control	Pending interrupts	Residual address	DCB
Power on reset	on	off	on	off	off	off	off	off	off	off
System reset	on	--	on	off	--	off	--	off	--	--
Halt I/O	on	--	on	off	--	--	--	off	--	--
Device reset	on	--	on	off	--	--	--	off*	--	--
DCB command reset	on	--	on	off	--	--	--	--	--	--
Indicator panel reset	--	off	--	--	--	--	--	--	--	--

*Will not reset controller end interrupt or controller busy condition.

-- = not reset

Multiple-Line Attachment Operation

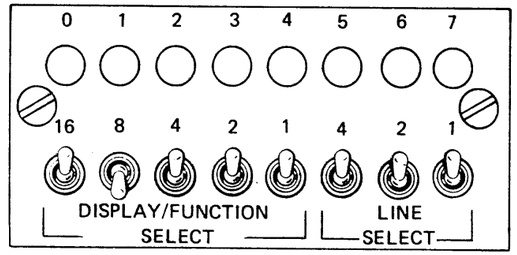
The asynchronous multiple-line attachment controller is designed to provide control circuitry for one or two asynchronous 4-line adapter features. The asynchronous multiple-line attachment contains hardware and a microprocessor to service the 4-line adapters. The basic difference between the multiple-line attachment and the single-line attachment is that the multiple-line attachment can present a controller busy (CC6) to the program followed by a controller-end interrupt request (CC0) when the multiple-line attachment controller hardware is no longer busy.

There is only one controller-end interrupt request when multiple controller busy operate I/O condition codes are presented; consequently, the program should queue the controller busy condition codes and clear (post) the controller-end interrupt condition code to all controller-busy codes received.

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine troubleshooting.

The indicator panel displays various conditions and registers in the attachment. In addition, the DTR line(s) to the modem(s) can be reset from the indicator panel. One setting of the DISPLAY/FUNCTION SELECT switches (11110) causes any incorrect data that is received to be placed in storage "as is."



LINE SELECT Switches

The three LINE-SELECT switches are used only with multiple-line attachments. They are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the LINE-SELECT switches.

These switches are ignored when the indicator panel is used with a single-line attachment.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed on the panel.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of the DCB control word
00001	0–7	Lamps 0–3 identify the subroutine. Lamps 4–7 show bits 12–15 of the DCB control word and identify the operation being performed.
		4–7 Operation
		0000 Transmit
		0001 Transmit end
		0010 Transmit allow break
		0011 Transmit end allow break
		0100 Receive or receive response
		0101 Receive or receive response—with time-out
		0110 Ring enable
		0111 Ring enable with time-out
		1000 DTR enable
		1001 DTR enable with time-out
		1010 DTR enable with answertone
		1011 DTR enable with answertone and time-out
		1100 DTR disable
		1101 Set control
		1110 Program delay
		1111 Reset
00010	0–7	Bit-rate constant
00011	0–7	COD1/EOA
00100	0–7	COD2/EOB
00101	0–7	COD3
00110	0–7	COD4
00111	0–7	COD5
01000	0–7	COD6/upshift
01001	0–7	COD7/downshift
01010	0–7	Bits 0–7 of the chain address
01011	0–7	Bits 8–15 of the chain address
01100	0–7	Bits 0–7 of the byte count
01101	0–7	Bits 8–15 of the byte count

(Part 1 of 2). Indicator panel information—ACC feature

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
01110	0–7	Bits 0–7 of the data address
01111	0–7	Bits 8–15 of the data address
10000	0–7	Bits 0–7 of timer 2
10001	0–7	Bits 8–15 of timer 2
10010	0–7	Bits 0–7 of timer 1
10011	0–7	Bits 8–15 of timer 1
10110	0	Overrun
	1	Time-out
	2	Block check error
	3	DCB reject
	4	EOB, count not 0
	5	VRC error
	6	Break detected
	7	Stop-bit error
10111	0–3	Bits 8–11 of the DCB control word
	4	Modem interface error
	5	DTR jumper installed
	6	RTS jumper installed
	7	Carrier detect jumper installed
11001	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Transmit line is in a "space" condition
	6	Receive line is in a "space" condition
	7	Carrier detect
11010	0	Used by diagnostic microprograms
	1	Receive mode
	2	Used by diagnostic microprograms
	3	Used by diagnostic microprograms
	4	8-Bit Data Interchange Code
	5	Transmit mode
	6	Used by diagnostic microprograms
	7	Not used
11011	0–7	This contains the last character sent or received (transmit/receive buffer). On receive operations, actual data appears; on transmit operations, data appears shifted one position to the left and bit 7 is turned on.
11100	0–7	Lamp test—all lamps should "blink"
11101	0–7	The interrupt status byte
11110		The lamps have no meaning. On a receive operaton, this switch setting causes any bad data that is received to be placed into storage. Normally, the attachment puts hex 00 in storage in place of any received bad data. This switch setting applies to all lines on a multi-line attachment, regardless of the setting of the LINE SELECT switches.
11111	0–7	The information displayed is the same as in switch setting 11001; however, this switch setting resets DTR if it is not jumpered "on."

(Part 2 of 2). Indicator panel information—ACC feature

Chapter 2. Binary Synchronous Communication

The Binary Synchronous Communication (BSC) features transmit and receive data as a stream of binary digits (zero bits and one bits). Character synchronization is maintained through the use of a specific bit pattern called the "sync pattern". At the beginning of a transmission and periodically during the transmission, the transmitting station inserts sync patterns into the stream of binary digits.

The bit rate of a BSC attachment is established by the modem's transmit and receive clocks. If the modem does not supply clocking, internal (business machine) clocking must be used. Internal clocking provides bit rates of 1200 bps (bits per second) and 600 bps.

The Binary Synchronous Communications Attachment (BSCA) can use either Extended Binary-Coded Decimal Interchange Code (EBCDIC) or American Standard Code for Information Interchange (ASCII) code. Selection of codes is controlled by the program. If the program does not specify ASCII code, the attachment automatically selects EBCDIC code. EBCDIC and ASCII codes are shown in Appendix A.

Data Flow

Each character occupies one byte in storage. Transfers to and from storage are two bytes at a time, except that the first and/or last transfers may move only one byte if specified by the data address or byte count.

Transmit

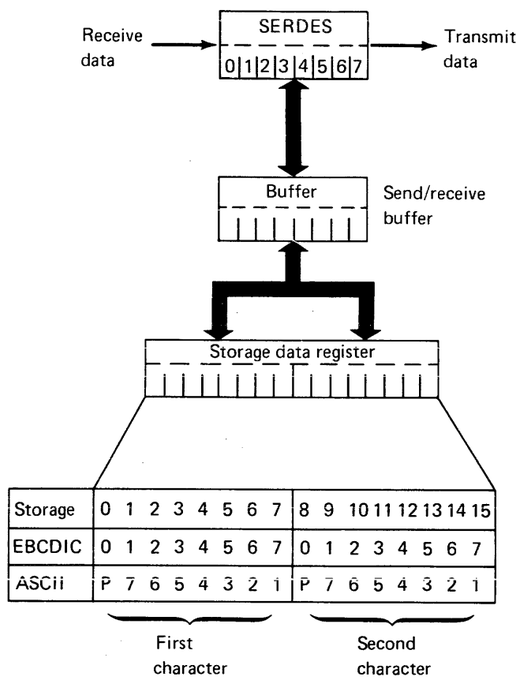
Transmission data is fetched from storage two characters at a time (except as noted previously). The high order byte holds the first character to be sent and the low order byte holds the next character. After a character has been transferred into the SERDES (serializer/deserializer), it is transmitted over the line, low order bit first.

ASCII characters in storage are eight bits in length--seven data bits plus one parity bit. This parity bit should not be confused with the parity bit in storage. The ASCII parity bit is bit 0 in a byte of storage.

The attachment does not check the ASCII parity during transmit operations, therefore, the program must maintain odd parity in storage bits 0–7 when using ASCII code.

Receive

The first bit received is transferred into the low order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on until a character is assembled. Two characters are assembled in the attachment before data is transferred to storage (except as noted previously). When two characters are to be transferred to storage, the first character received is loaded into the high order byte of the storage data register and the next character is loaded in the low order byte before the data is transferred to storage. Data is written into storage without any code translation.



BSC transmit and receive data flow

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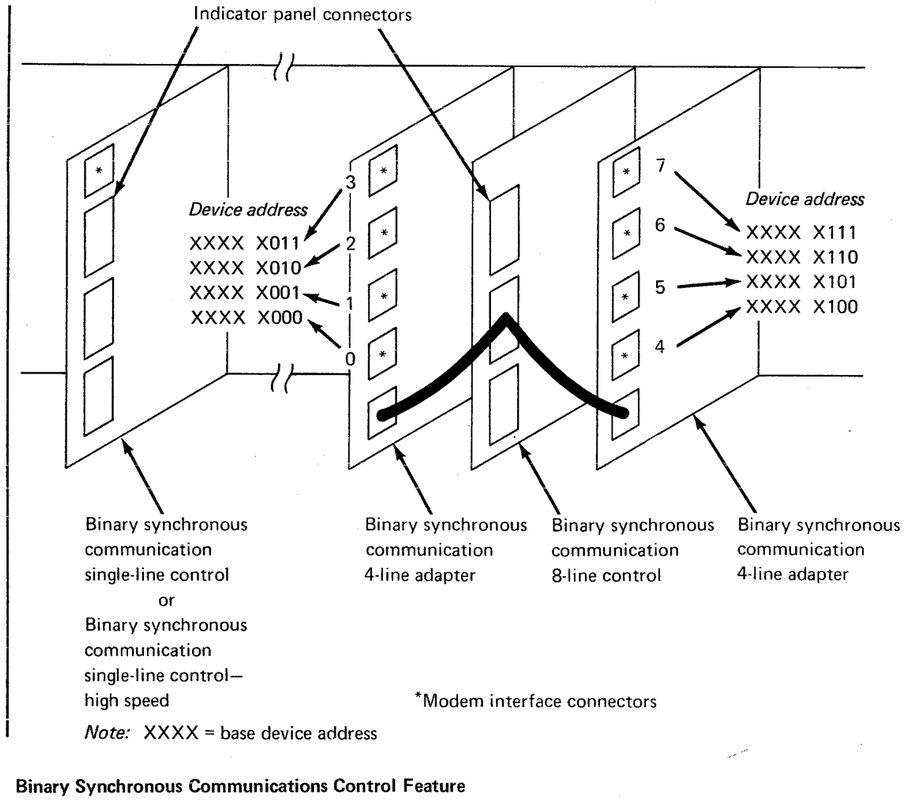
BSC Feature Configurations

The Binary Synchronous Communication Control features are available in single-line and multiple-line configurations. The multiple-line configuration provides up to eight lines. The single-line configurations are contained on one card. The multiple-line configuration contains either two or three feature cards—two cards for one to four lines, three cards for five to eight lines.

Note: Throughout the remainder of this chapter, the term *attachment* is used as a general term to refer to any of the following:

- The Binary Synchronous Communications Single-Line Control feature.
- The Binary Synchronous Communications Single-Line Control/High Speed feature.
- The Binary Synchronous Communications 8-Line Control feature and one or two Binary Synchronous Communications 4-Line Adapter features.

When referring specifically to either single-line feature, the term *single-line attachment* is used. When referring specifically to either the 8-line control feature or the 4-line adapter, the term *multiple-line attachment* is used.

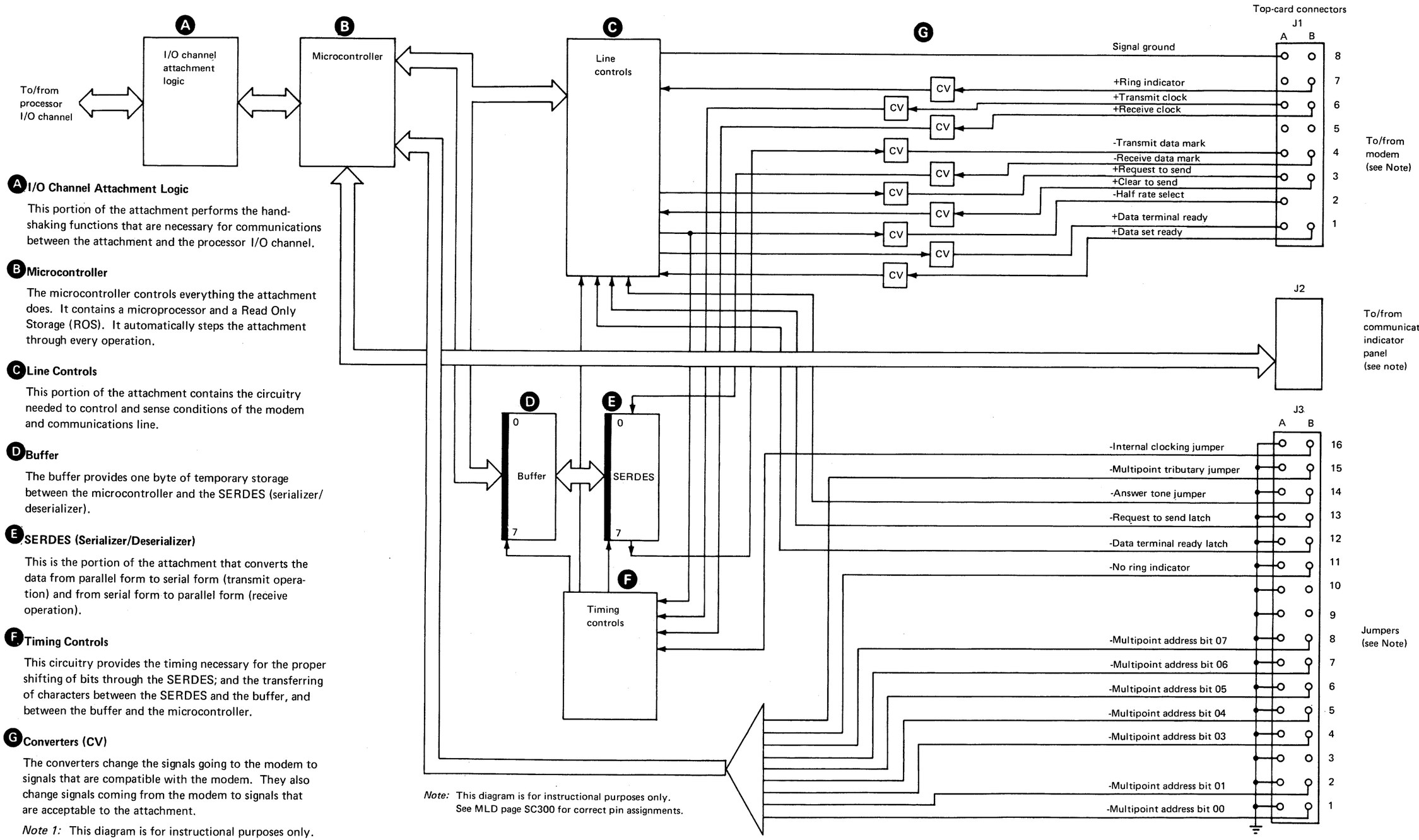


Note: XXXX = base device address

Binary Synchronous Communications Control Feature

Functional Units

Single Line BSCA—9,600 bps



A I/O Channel Attachment Logic

This portion of the attachment performs the hand-shaking functions that are necessary for communications between the attachment and the processor I/O channel.

B Microcontroller

The microcontroller controls everything the attachment does. It contains a microprocessor and a Read Only Storage (ROS). It automatically steps the attachment through every operation.

C Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and communications line.

D Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

E SERDES (Serializer/Deserializer)

This is the portion of the attachment that converts the data from parallel form to serial form (transmit operation) and from serial form to parallel form (receive operation).

F Timing Controls

This circuitry provides the timing necessary for the proper shifting of bits through the SERDES; and the transferring of characters between the SERDES and the buffer, and between the buffer and the microcontroller.

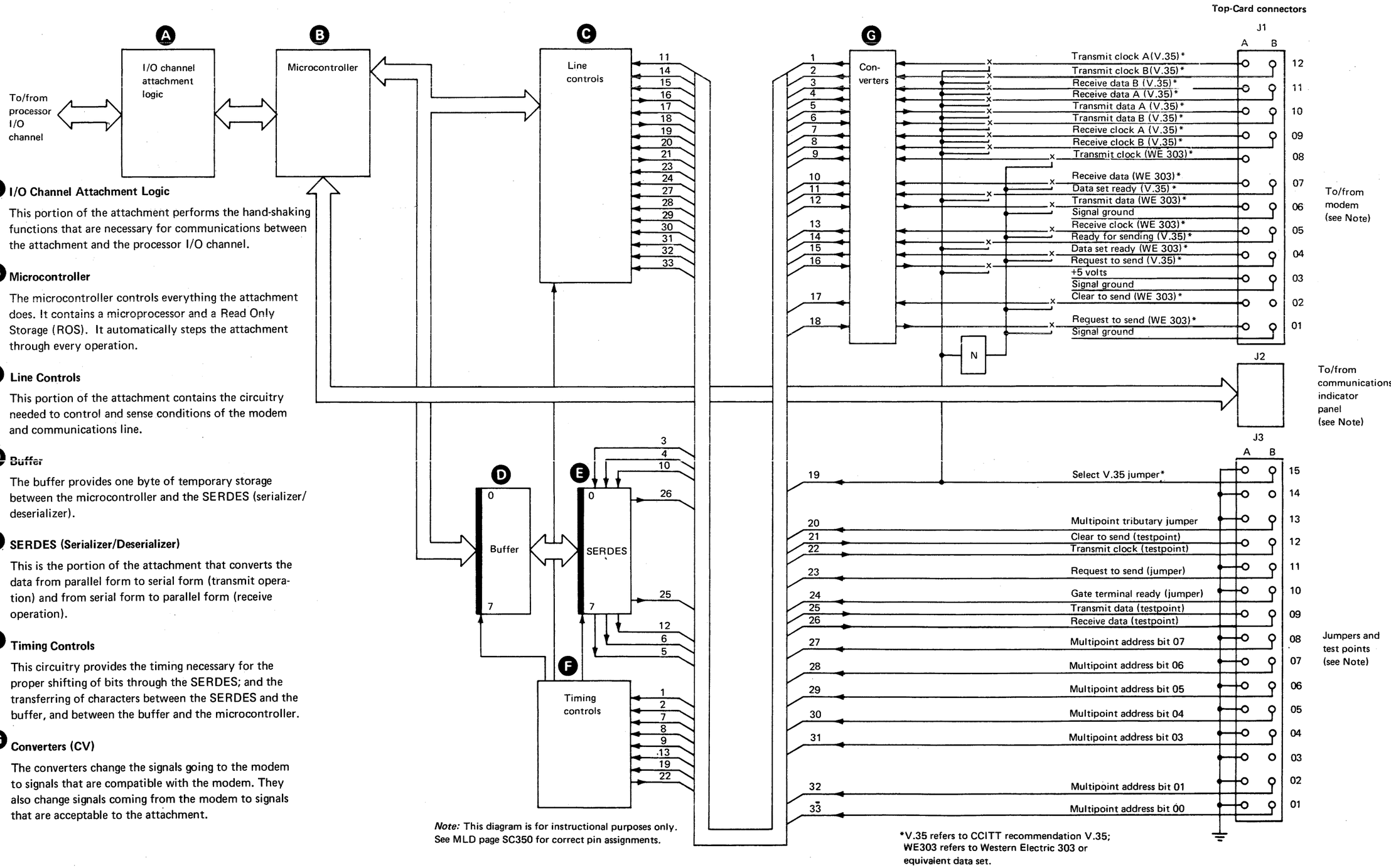
G Converters (CV)

The converters change the signals going to the modem to signals that are compatible with the modem. They also change signals coming from the modem to signals that are acceptable to the attachment.

Note 1: This diagram is for instructional purposes only. See MLD page SC300 for correct pin assignments.

Note: This diagram is for instructional purposes only. See MLD page SC300 for correct pin assignments.

Single-Line BSCA—56,000 bps



Note: This diagram is for instructional purposes only. See MLD page SC350 for correct pin assignments.

*V.35 refers to CCITT recommendation V.35; WE303 refers to Western Electric 303 or equivalent data set.

A I/O Channel Attachment Logic

This portion of the attachment performs the hand-shaking functions that are necessary for communications between the attachment and the processor I/O channel.

B Microcontroller

The microcontroller controls everything the attachment does. It contains a microprocessor and a Read Only Storage (ROS). It automatically steps the attachment through every operation.

C Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and communications line.

D Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

E SERDES (Serializer/Deserializer)

This is the portion of the attachment that converts the data from parallel form to serial form (transmit operation) and from serial form to parallel form (receive operation).

F Timing Controls

This circuitry provides the timing necessary for the proper shifting of bits through the SERDES; and the transferring of characters between the SERDES and the buffer, and between the buffer and the microcontroller.

G Converters (CV)

The converters change the signals going to the modem to signals that are compatible with the modem. They also change signals coming from the modem to signals that are acceptable to the attachment.

Multiple-Line BSCA

Ⓐ I/O Channel Attachment Logic

This portion of the attachment performs the handshaking functions that are necessary for communications between the attachment and the processor I/O channel.

Ⓑ Microcontroller

The microcontroller controls everything the attachment does. It contains a Read Only Storage (ROS), and circuitry that decodes the commands from the processor and automatically steps the attachment through every operation.

Ⓒ Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and communications line.

Ⓓ Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

Ⓔ SERDES (Serializer/Deserializer)

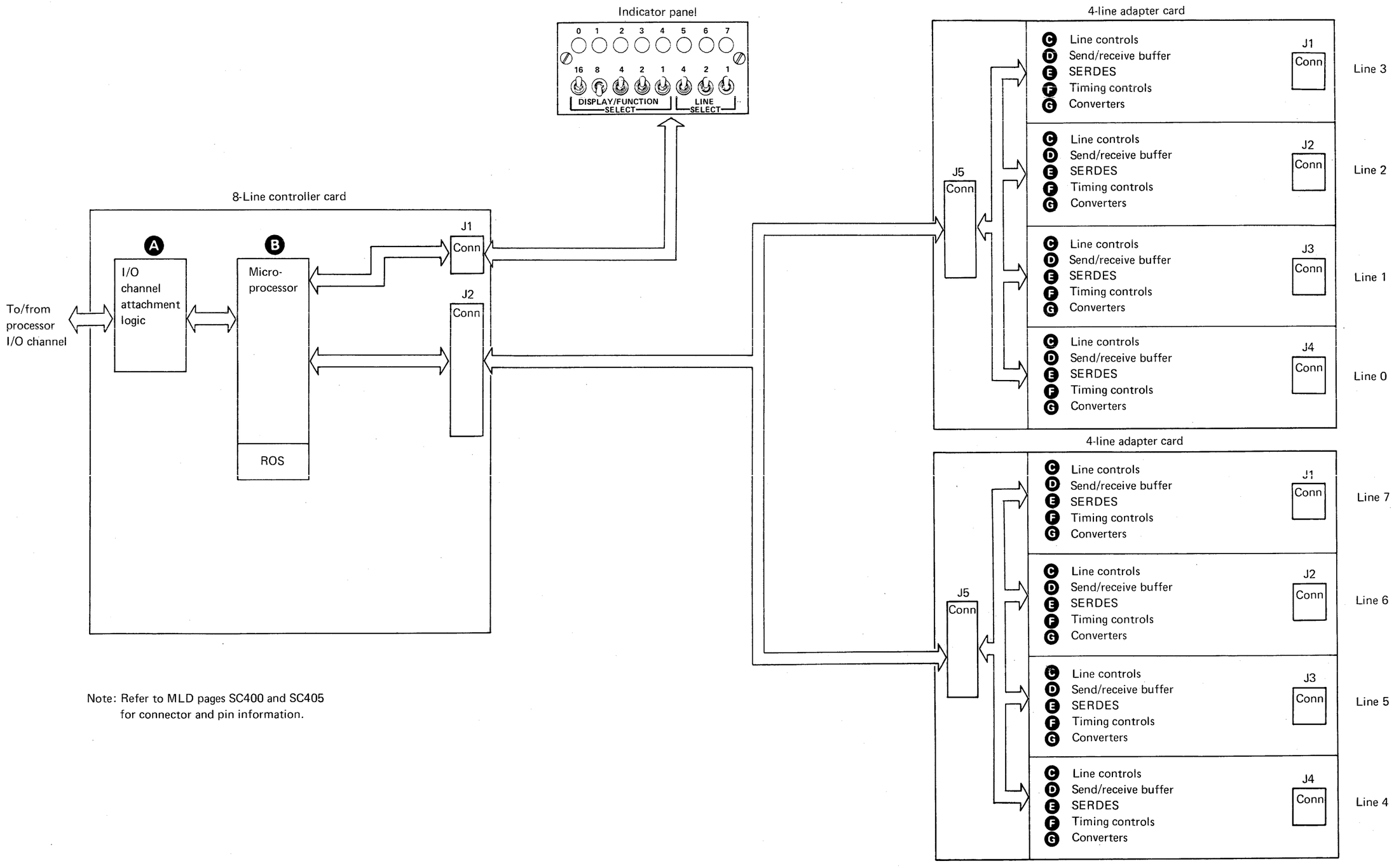
This is the portion of the attachment that converts the data from parallel form to serial form (transmit operation) and from serial form to parallel form (receive operation).

Ⓕ Timing Controls

This circuitry provides the timing necessary for the proper shifting of bits through the SERDES; and the transferring of characters between the SERDES and the buffer, and between the buffer and the microcontroller.

Ⓖ Converters

The converters change the signals going to the modem to signals that are compatible with the modem. They also change signals coming from the modem to signals that are acceptable to the attachment.



Note: Refer to MLD pages SC400 and SC405 for connector and pin information.

Operating Modes

The attachment has several operating modes that are selected by control characters.

Text

Text mode is selected when the first start-of-heading (SOH) or start-of-text (STX) control character is decoded. Subsequent SOH and STX characters are treated as data characters. During text mode, the attachment processes header or text characters and accumulates a block check character (BCC). Synchronization (SYN) characters and the first SOH or STX characters decoded are not included in the BCC accumulation. Text mode is terminated after an end-of-text (ETX) or end-of-transmission-block (ETB) character is decoded by the attachment.

Transparent Text

Transparent text mode is selected when a data-link-escape (DLE) STX sequence is decoded during a transmit or receive operation. While in this mode, any kind of binary data can be transmitted or received. The following changes from text mode occur:

- The attachment recognizes individual control characters or control sequences, (such as ETB, STX, and enquiry (ENQ)), only as data, with no other associated function.
- All inserted SYN characters are preceded automatically by a DLE character (DLE-SYN).
- A second DLE is attached automatically to every data DLE to distinguish it as a DLE control character, rather than data. This second DLE and the inserted DLE-SYNs are automatically deleted upon reception and do not enter main storage.

To exit transparent text mode, one of the following ending sequences are required:

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

These sequences must be transmitted by using the exit transparent operation (See "Device Control Block (DCB)" later in this chapter). In transparent text mode, the transmitting attachment automatically inserts a second DLE between the first DLE and the ETX, ETB, ENQ, or ITB. The receiving station discards the first DLE. The inserted DLE and the ETX, ETB, ENQ, or ITB are considered as two data characters and placed in storage. The exit transparent operation prevents the attachment from inserting a second DLE. The receiving station recognizes the ending sequences as ending sequences, not data. Because the DLEs in these ending sequences are true DLEs and are not placed in storage at the receiver, they should not be included in the byte count for the receiving station.

Only DLE-ITB leaves the attachment in text mode; all the others cause a COD.

During transparent text mode, a BCC is accumulated as in normal text mode. The only DLE characters included in the BCC are the data DLEs.

Control Mode

In a multipoint configuration, when the attachment receives a valid EOT sequence, it enters control mode. While in control mode, the attachment monitors for its station address. If the attachment does not enter selected mode and detects an address sequence other than its own, character synchronization is reset.

The multiple-line attachment must be in receive mode to recognize the EOT character. Due to its IPL capability, the single-line attachment will monitor the line for an EOT character while it is in control mode (that is, no command pending). An EOT character following the leading SYN-SYN sequence places the single-line attachment in control mode.

Selected Mode

The attachment enters selected mode when it decodes its station address twice (contiguously) after establishing byte synchronization. If a receive operation has been initiated, the message sequence, starting with the second station address character, is transferred to storage.

Note: The attachment's station-address (used in multipoint configuration only) is determined by discrete jumpers on the feature card. Control characters may not be used as an address. The bit-2 position in storage (station address) cannot be wired. In EBCDIC, this is bit 2; in ASCII, this is bit 6. The program, may use these bits to differentiate between a polling and a selecting sequence.

Multipoint address bit 0 must not be wired "on" when using ASCII.

Passive Mode

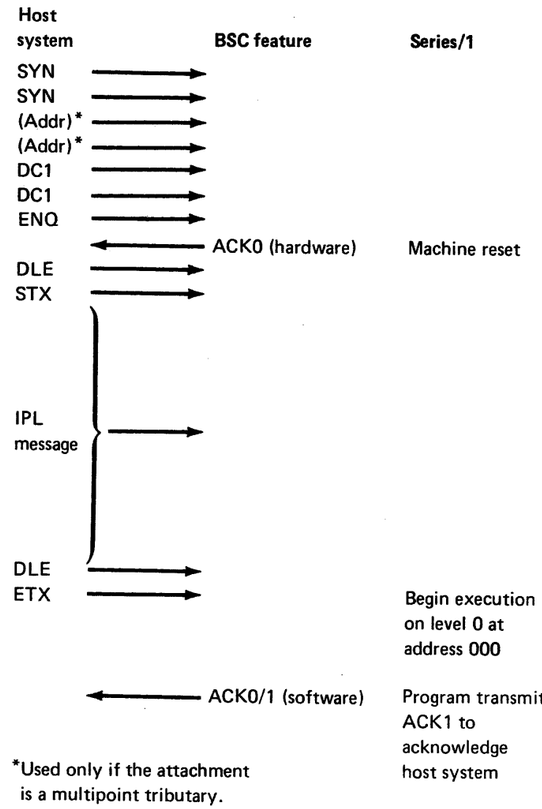
The attachment in a multipoint network is in passive mode when it is not in selected or in control mode. Passive mode is entered when the attachment is powered on. The attachment enters other modes, depending upon the characters received on the line as previously described.

IPL Mode

Initial program load (IPL) by a host system may be accomplished through a *single-line* attachment using EBCDIC characters only. A jumper (for bit 0 of the multipoint address) must be installed on the feature card to allow the attachment to IPL the processor.

If an IPL sequence (DC1-DC1-ENQ) is received, the attachment hardware responds with an EBCDIC acknowledgment (ACK0) after a 50-millisecond delay.

If the attachment is a multipoint tributary station, its address must be included in the IPL sequence, as shown in the following example. (It must also have been placed in control mode as described earlier).



*Used only if the attachment is a multipoint tributary.

The host must then transmit DLE-STX (to enter transparent text mode) followed by the IPL program. This sequence (DLE-STX) is not checked by the attachment for validity and is not placed into storage. The attachment enters transparent text mode and places all following data into storage beginning at location 0000.

Upon receiving a DLE-ETX followed by a valid BCC, the attachment presents a device-end interrupt request, on level 0, with the device address in register 7. The IPLed program must handle this interrupt request. The program must also transmit a positive acknowledgement back to the host system.

If the IPL operation is unsuccessful, the attachment holds the processor in IPL mode (Load light will be on) and monitors the line for a retry of the IPL operation. A general logic flow for a switched-line IPL sequence follows.

Notes:

1. For an unattended processor to be IPLed on a switched network, the modem must be capable of automatically answering calls. If the line has not been enabled ('data terminal ready' made active) and the allow-IPL jumper and the switched-line jumpers are installed, the attachment activate 'data terminal ready' and presents an attention interrupt request to the processor upon detecting the ring signal. If a command is not given by the processor or if the attention interrupt is not accepted by the processor, the attachment monitors the line for approximately 13 seconds looking for an IPL sequence. (Any command given by the processor during this period is accepted.) The line will be disconnected (DTR deactivated) if no IPL sequence is detected within this time period. If the line was enabled prior to this sequence, the DTR line will stay active.
2. On a leased line, the attachment cannot receive an IPL unless DTR is wired "on."
3. There are some modems that do not supply clocking and cannot run at speeds higher than 600 bps. These modems require the use of the internal clocking feature of the BSC attachments. Internal clocking automatically supplies clocking at 1,200 bps. The 600-bps rate of internal clocking can only be selected by a program already in storage; therefore, the system cannot be IPLed by the BSC attachments when such a modem is used.
4. The maximum number of bytes that can be loaded by the host IPL program using the BSC attachment is 65,535; however, the quality of the transmission line must be considered when transmitting 65,535 bytes.

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Transmission Codes

The BSC attachments allow data communication using EBCDIC or ASCII line codes. ASCII can be specified by the program after the IPL. The attachment establishes EBCDIC if:

- No code is specified
- A power-on reset occurs
- A system reset occurs

Note: The EBCDIC and ASCII character assignments are shown in Appendix A.

Control Characters

Note: For detailed information about BSC line control, refer to *General Information Binary Synchronous Communications*, GA27-3004.

Name	Mnemonic	EBCDIC	ASCII
Start of heading	SOH	SOH	SOH
Start of text	STX	STX	STX
End of transmission block (Note 1)	ETB	ETB	ETB
End of text (Note) 1)	ETX	ETX	ETX
End of transmission (Note 1)	EOT	EOT	EOT
Enquiry (Note 1)	ENQ	ENQ	ENQ
Negative acknowledge (Note 1)	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Immediate block character	ITB	IUS	US
Initial program load (Note 2)	IPL	DC1 DC1 ENQ	
Even acknowledge (Note 1)	ACK0	DLE(70)	DLE0
Odd acknowledge	ACK1	DLE/	DLE1
Wait before transmit-positive acknowledge (Note 1)	WACK	DLE,	DLE;
Mandatory disconnect (Note 1)	DISC	DLE EOT	DLE EOT
Reverse interrupt (Note 1)	RVI	DLE@	DLE<
Temporary text delay	TTD	STX ENQ	STX ENQ
Transparent start of text (Note 3)	XSTX	DLE STX	
Transparent intermediate block (Note 3)	XITB	DLE IUS	
Transparent end of text (Note 3)	XETX	DLE ETX	
Transparent end of transmission block (Note 3)	XETB	DLE ETB	
Transparent synchronous idle (Note 3)	XSYN	DLE SYN	
Transparent block cancel (Note 3)	XENQ	DLE ENQ	
Transparent TTD (Note 3)	XTTD	DLE STX DLE ENQ	
Data DLE in transparent mode (Note 3)	XDLE	DLE DLE	

Notes:

1. These control characters and sequences cause a change-of-direction (COD) interrupt request after the required action has been completed.
2. Not applicable in ASCII format.
3. Transparent mode not available in ASCII.

BSC-feature control characters

The functions of the control characters follow:

Mnemonic	Function
SOH or STX	Resets control mode and sets the adapter to text mode. BCC accumulation starts with the first character after the first SOH or STX character is transmitted/received.
ETB or ETX	Reset text mode with BCC comparison.
EOT	End of transmission.
ENQ	Reset text mode without BCC transmission and comparison.
NAK	Negative response to a request for a reply, or to a block of heading or a block of text in error.
SYN	Transmitted automatically by the adapter to establish and maintain synchronization.
DLE	Alert the adapter to test the next character for a defined control sequence in transparent text mode. In nontransparent text mode, DLE is treated as data.
ITB	Included in the BCC; it causes the BCC to be sent.
IPL	Control characters to initiate an IPL sequence.
ACK0	Indicates affirmative acknowledgement of even blocks.
ACK1	Indicates affirmative acknowledgement of odd blocks.
WACK	Indicates a temporary not-ready-to-continue (or not-ready-to-receive) condition.
DISC	Used only on switched communication facilities to initiate a disconnect.
RVI	Reverses direction of data transfer.
TTD	Alerts the receiving station of a temporary text delay
XSTX	Turns off control mode and set the adapter to transparent text mode.
XITB	Same as ITB, but turns off transparent text mode.

XETX/XETB	Same as ETB or ETX, but turns off transparent mode.
XSYN	Transmitted automatically by the adapter to establish and maintain synchronization in transparent text mode.
XENQ	Turn off transparent text mode and cancel the current block of data.
XTTD	Alerts the receiving station to a temporary text delay in transparent text mode.
XDLE	In transparent text mode, the transmitter adds a second DLE after each data DLE. At the receiver, the first DLE is removed and does not enter storage or the BCC.

Line Error Checking

Two different types of checking are employed, depending on the code selected. Cyclic redundancy check (CRC) is used with EBCDIC and longitudinal redundancy and vertical redundancy checking (LRC/VRC) is used with ASCII.

Error correction is accomplished by retransmitting the data block that was in error.

Synchronization and Timing

The attachment receives strobe pulses from the modem; these pulses establish and maintain bit synchronization. If the modem does not supply a pulse, the internal clocking feature must be wired "on" to supply synchronization. Whichever form of bit synchronization is used, a specific series of characters precedes each transmission in order to establish character synchronization.

Transmit Synchronization

The attachment automatically begins transmission with a leading pad character (hex 55) followed by the initial synchronizing pattern of two SYN characters. If internal clocking is being used, the attachment transmits two leading pad characters.

To maintain synchronization, the attachment inserts a synchronization pattern of SYN-SYN at one-second intervals (approximately). In transparent text mode this synchronization pattern is DLE-SYN. These characters are also inserted as time-fill characters when the attachment is not transmitting such as when it is fetching a new device control block (DCB) during a chaining operation.

SYN Insertion. SYN characters or transparent SYN characters are inserted automatically during transmission or between chaining. This is done to maintain synchronization.

SYN Deletion. SYN characters or transparent SYN characters are deleted and not placed in storage.

Trailing Pad Characters. The attachment automatically transmits a trailing pad character (hex FF) after every COD character or after the BCC if the change of direction calls for BCC. This ensures that the last character sent (COD or BCC) goes online in its entirety. A pad of hexadecimal FF also provides the second character of the NAK and EOT control character sequences. The attachment does not begin an interrupt request or chaining operation until the entire pad character is transmitted.

SYN and pad characters (leading and trailing) are provided by the attachment and are not stored in main storage.

Receive Synchronization

Character phase synchronization is established when two consecutive SYN characters followed by any non-SYN character are received and decoded. Character phase is maintained because the transmit station periodically inserts a synchronization pattern into the data stream.

SYN and pad characters are deleted by the attachment and are not stored in main storage.

Time-Outs

There are three types of time-outs possible with BSC operations: data set ready (DSR), receive, and program.

Data Set Ready Time-Out

When performing an enable terminal operation, bit 12 of DCB word 0 can be used to cause the attachment to wait a predetermined time (13 seconds for single-line and 3 seconds for multi-line) for DSR to be returned by the modem. If DSR is not returned within this time period of DTR being activated, the attachment terminates the operation and presents an exception interrupt request.

Receive Time-Out

The receive time-out is nominally three seconds and causes the attachment to present an exception interrupt (CC2) under the following conditions:

- Character phase is not established within three seconds after the attachment accepts a receive data operation. This is under program control and is effective only if bit 12 is set on in word 0 of the current DCB.
- A continuous synchronization pattern, or transparent synchronous idle (in transparent mode) is received for three seconds while in character phase.
- While receiving data, no synchronization pattern or transparent synchronization idle is received within three seconds.

Program Time-Out

A two-second time-out is available for use by the program. It is initiated by any Start command with bit 12 equal to 1 in word 0 of the associated DCB. After two seconds, the attachment presents a device-end interrupt request (CC3).

Turnaround Considerations

When operating with modem eliminators, approximately 10 milliseconds (plus any associated program delays) should be allowed from the termination of a write operation to the start of a read operation.

Commands

The Operate Input/Output instruction points to the immediate DCB (IDCB), which contains one of the following commands:

- Prepare
- Halt I/O
- Device Reset
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1
- Start Diagnostic 2
- Start Control

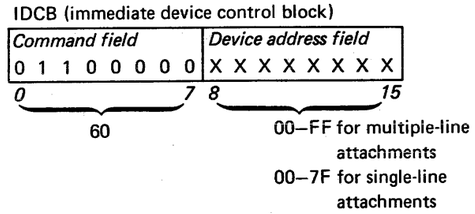
It is the programmer's responsibility to ensure that the program always tests the operate I/O condition codes following an Operate I/O instruction.

The programmer should exercise care in modifying the DCB words prior to an interrupt request that signifies the end of an operation. The attachment may not have entirely fetched all of the DCB (due to the relatively slow speed of the attachment in relation to Series/1 processor instruction speeds).

Note: See Appendix D for an example of an adapter initialization program.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The immediate data field of the IDCB contains the level and I-bit information. The single-line attachment is always able to accept and execute a Prepare command, even if it is busy or has an interrupt request pending from a previous command. On a multiple-line attachment, the device returns a condition code of 1 to this command if it has an interrupt request pending. The IDCB for the Prepare command has the following format:



Level. This four-bit field specifies the priority interrupt level assigned to the device.

Example:

Bits 27–30	Level
0000	0
0001	1
0010	2
0011	3

A Prepare command issued to any device on a multiple-line attachment gives *all* of the devices in the attachment the same priority interrupt level. The I-bit information, however, applies only to the device addressed.

I-Bit. This bit determines whether the device is allowed to present interrupt requests. An I-bit value of 1 means that the device can request an interrupt; a value of 0 means that the device cannot interrupt.

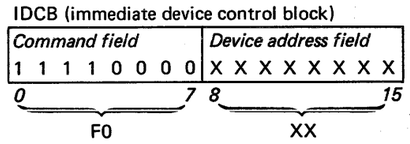
The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset by a power-on reset. The prepare information can be changed by the successful execution of another Prepare command.

The Prepare command may allow an interrupt request to occur if the attachment is not prepared and has an interrupt request pending upon receipt of a Prepare with the I-bit equal to 1.

The Prepare command always causes an attachment to respond with satisfactory (Operate I/O CC7) or device busy (on multiple-line controller only; CC1).

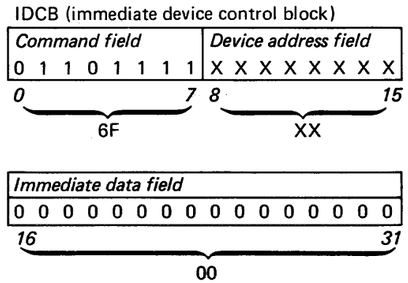
Halt I/O

The Halt I/O command halts all I/O activity on the I/O channel. Any pending interrupt requests, including controller end (CC0) are cleared; the I-bits and priority level do not change. This instruction performs the same function as a system reset.



Device Reset

The Device Reset command resets the addressed device and clears any pending interrupt requests (except controller end). The Prepare information and the residual address do not change. This command does not reset the DTR line to the modem or clear a 'controller end' interrupt request.



A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are carried out. There are differences between the single-line attachment and the multiple-line attachment are:

- The length of time the attachment is busy performing the reset function
- The method used to report the conclusion to the program

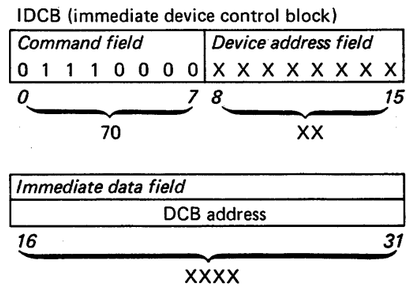
For example, if a Start command follows a Device Reset too closely, a 'busy after reset' (CC2) is reported on a single-line attachment. The program must reissue the command until a 'satisfactory' (CC7) is reported.

On a multiple-line attachment, a 'controller busy' (CC6) is reported when Start follows Device Reset too closely. When the reset is completed, a 'controller end' interrupt (CC0) is presented by the base address of the multiple-line controller (line 0).

Note: Under certain conditions, it is possible that more than one 'controller end' interrupt request is presented. If no busy condition is found upon examining the 'controller busy' queue, disregard the interrupt request.

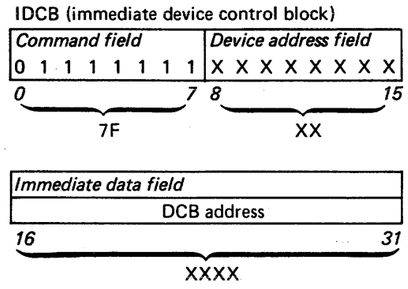
Start

The Start command initiates a cycle-steal operation for the addressed device. The format of the IDCB for the Start command is:



Start Cycle Steal Status

The Start Cycle Steal Status causes the device to initiate a cycle-steal operation for the purpose of collecting status information about the previous cycle-steal operation. The format of the IDCB for this command follows:



The byte count in the DCB (word 6) must be equal to 6 and the data address (word 7) must be on a word boundary (bit 15 off) or an exception interrupt request (CC2) will occur with DCB specification check bit (bit 3) equal to 1 in the interrupt status byte.

See "Cycle Steal Status Words" in this chapter for a description of the information transferred to storage by this command.

Read ID

The Read ID command puts the attachment's identification (ID) word into the immediate data field of the IDCB. The ID word contains physical information about the attachment that can be used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming.

IDCB (immediate device control block)

Command field	*Device address field*
0 0 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
20	XX

Immediate data field
ID word
16 ... *31*

Single-line BSC	1006
Two-line BSC	2106
Four-line BSC	2206
Six-line BSC	2306
Eight-line BSC	2006

Note: If the control-feature card has jumpers installed for addresses not present, the controller responds to commands as if the hardware is present. Consequently, the ID of the controller should match the number of attachment lines present to prevent errors. For example, an ID of 2006 defines a multiple-line controller with two 4-line attachments (all eight lines in use). If there is one 4-line attachment present, the ID is 2206 (or 2106 if only two of the four lines are in use).

Start Diagnostic

The Start Diagnostic commands are used by diagnostic programs to check for correct operation of the attachments.

Start Diagnostic 1

The format of the IDCB for this command is:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 1	X X X X X X X X
0 ... *7*	*8* ... *15*
7D	XX

Immediate data field
DCB address
16 ... *31*
XXXX

In the DCB control word, bit 2 must equal 1 bits 5 through 7 can equal either 0 or 1, and all other bits must equal 0. The byte count must be 0008 (for single-line) or 000E (for multiple-line), and the data address must be even. If any of these conditions are not met, the attachment presents an exception interrupt request and reports DCB specification check in the interrupt status byte.

This command causes the following two tests to occur in the attachment:

- A checksum test
- A register test

In the first test, the attachment calculates a checksum for each of the read-only storage (ROS) modules in the attachment. Single-line attachments have two modules; multiple-line attachments have three. The ROS modules have a check sum built into them when they are made. The attachment transfers these four check sums to storage, beginning at the address specified in DCB word 7.

Data word 0	=	Built in check sum—ROS 1
Data word 1	=	Calculated check sum (inverted)—ROS 1
Data word 2	=	Built in check sum—ROS 2
Data word 3	=	Calculated check sum (inverted)—ROS 2
Data word 4*	=	Built in check sum—ROS 3
Data word 5*	=	Calculated check sum (inverted)—ROS 3
Data word 6*	=	AA55 (results of buffer test in addressed device)

* Multiple-line attachments only

The second test checks all registers in the attachment. If the test is successful, the attachment presents a device-end interrupt request. If an error is detected, the attachment will "hang" and will not present a device-end interrupt request or an exception interrupt request.

Start Diagnostic 2

The IDCB for the Start Diagnostic 2 command has the following format:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7E	XX

Immediate data field
DCB address
16 ... *31*
XXXX

In the DCB control word, bit 2 must equal 1, bits 5–7 can equal either 0 or 1 and all other bits must equal 0. The byte count must be 0002 (for both single-line and multiple-line attachments), and the data address must be even. If any of these conditions are not met, the attachment presents an exception interrupt request and reports DCB specification check in the interrupt status byte.

The attachment activates DTR and request to send (RTS) and checks for DSR and clear to send (CTS) to be returned through the modem cable and wrap connector. The attachment then checks the serializer/deserializer (SERDES) by wrapping a data character through the cable and wrap connector. The results of this test are then placed into the high-order byte of the storage data register. The bits in this byte are:

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request to send
3	Clear to send
4	Clocks found*
5	Buffer service latch failed to set
6	Transmit mode latch (should equal 1)
7	Data wrap failed

* Bit 4 will be on if both transmit and receive clocks are activated due to internal clocking being wired on. The correct results of this test are F2XX or FAXX, depending on whether internal clocking is being used.

The attachment places hex FF into the low-order byte of the storage data register and then attempts to transfer only the high-order byte to storage. Only the high-order byte of the word in storage addressed by DCB word 7 should be changed. The program should load a value other than hex FF into the low-order byte of storage so that it can determine if the "byte mode" transfer worked. If the "byte mode" generated an error, the low-order byte in storage will contain hex FF.

Start Control

The Start Control command is reserved for use by IBM engineering.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7C	XX

Immediate data field
DCB address
16 ... *31*

Issuing this command to a multiple-line attachment can cause the attachment to become inoperable. If this happens, the attachment can only be restored to operation by turning power off, and then on again.

Device Control Block (DCB)

The DCB is an eight-word area in main storage that describes the specific parameters of the operation. Its location in storage is assigned by the program. The data is loaded and changed by the program. The address of the DCB must be even. If the DCB address is odd, the attachment sets interrupt status byte bit 1 equal to 1 (delayed command reject) and terminates the operation with an exception interrupt request (CC2).

It is fetched by the attachment, using a cycle-steal address key of 000, after successful execution of a Start I/O, Start Cycle Steal Status, Start Control, or Start Diagnostic command. The DCB address transferred to the attachment through the IDCB points to word 0 of the DCB.

DCB (device control block)

Word	
0	Control word
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address
6	Byte count
7	Data address

0 15

Control Word 0

Control word 0 prescribes the operation to be performed. The format of the control word follows.

Bit 0—Chaining Flag. If this bit equals 1, the attachment fetches the next DCB in the chain at the end of the current DCB operation.

Programming note. Chaining should not be used to receive continuous blocks of data in the high-speed attachment (greater than 9,600 bps), or the multiple-line attachment. Overrun errors may occur if receive operations are chained in these attachments.

Bit 1. This bit is not used and must be set to 0.

Bit 2—Input Flag. If bit 2 equals 1, data is transferred from the attachment to the processor; if bit 2 equals 0, data is transferred from the processor to the attachment.

On a Start command, this bit equal to 1 specifies a receive operation.

The receive operation allows the attachment to start transferring data to main storage after character synchronization is established.

The attachment presents a normal device-end interrupt request or begins a DCB command chaining operation when a COD character is received and the byte count is reduced to 0.

The attachment presents an exception interrupt request and interrupt status byte bit 1 equals 1 if DSR equals 0 when the operation begins.

Bit 12 of DCB word 0 may be used with this operation to limit the time the attachment allows for establishing character synchronization to 3 seconds. Failure to establish character synchronization within this time results in an exception interrupt request with interrupt status byte bit 0 equal to 1.

Bits 3 and 4. These bits are not used and must equal 0.

Bits 5 Through 7—Cycle-Steal Address Key. This is a three-bit key presented to the processor by the attachment during cycle-steal data transfers. It is used by the processor to determine if the attachment is authorized to access certain blocks of main storage.

Bit 8—Half-Rate. The attachment uses this bit only during the enable terminal operation. If bit 8 equals 1, the modem (if it is equipped to recognize half-rate) runs at one-half of its normal bit rate. If internal clocking is being used, this bit selects the 600-bps rate. If the state of the rate-select line is to change, the attachment automatically waits 13 seconds before checking for DSR. This allows the modem enough time to equalize.

Note: If this bit equals 1 and the attachment generates an answer-tone, it resets the bit rate to its previous speed. Another enable terminal operation is required to set half-rate again.

Bit 9—ASCII Mode. If this bit equals 1, the attachment uses ASCII; if the bit equals 0, the attachment uses EBCDIC.

Bit 10—Enable Terminal. This bit is used to activate DTR to the modem. A device-end interrupt request occurs 50 milliseconds after DSR is returned by the modem. If DSR is already active, the request occurs immediately.

Bit 12 may be used in conjunction with this operation to limit the time that the attachment will wait for DSR to become active. If bit 12 equals 1, failure to get DSR within 3 seconds results in DTR being reset and an exception interrupt request with interrupt status byte bit 0 equal to 1.

On a medium-speed, single-line attachment wired to IPL the Series/1 processor in s switched network, a ring indication from the modem also sets DTR equal to 1. For manual call or manual answer sequence, bit 10 must be used to set DTR equal to 1 prior to entering data mode.

On a leased line, DTR is normally wired "on".

Bit 11—Disable Terminal. This bit causes the attachment to deactivate DTR in order to disconnect the modem from a switched network. The attachment presents a device-end interrupt request or begins a chaining operation 2 seconds after DSR goes off. If DSR is not deactivated within 3 seconds, the attachment presents an exception interrupt request with interrupt status byte bit 0 equal to 1.

Bit 12—Start Timer. This bit can be used with an enable terminal operation or with a receive operation to provide a 3-second time-out. When used alone, bit 12 causes the attachment to start timing a 2-second period, after which the attachment presents a device-end interrupt request.

Bit 13—Transmit Operation. This operation starts a 3-second timer and turns on RTS. When the modem returns CTS, the attachment establishes synchronization (described under "Synchronization and Timing" earlier in this chapter). The attachment then starts fetching data from main storage and transmitting the data.

The attachment presents a normal device-end interrupt request or begins a DCB command chaining operation when a line turnaround character (COD) is transmitted and the byte count goes to 0.

The attachment presents an exception interrupt request and interrupt status byte bit 0 equals 1 if DSR equals 0 when the operation begins.

Failure to receive CTS from the modem within the 3-second time-out period or CTS being active for 3 seconds without RTS being active results in an exception interrupt request with bit 0 equal to 1 in the interrupt status byte.

The attachment resets transmit mode and RTS after transmitting the pad character following a COD character. If block checking is used, the attachment resets transmit mode and RTS after transmitting the pad character following the BCC.

Note: RTS can be permanently wired on when desired. CTS must not be permanently returned by the modem unless RTS is wired on.

Bit 14—Exit Transparent. Because the BSC attachment does not recognize control characters when transmitting in transparent text mode, there must be a method of transmitting control sequences so that they can be recognized as such. This is accomplished by the exit transparent operation.

The exit transparent operation requires its own DCB and a byte count of 2. Unexpected results may occur if the byte count is greater than 2.

This operation should only be used to transmit the control sequences shown below following a block of transparent text.

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

Bit 15. This bit is not used and should equal 0.

Chain Address

The Chain Address word contains the storage address of the next DCB and is used when chaining is indicated. The chain address must be even. If it is odd, the attachment sets interrupt status byte bit 3 equal to 1 and terminates the operation.

Byte Count

The Byte Count word contains the number of bytes to be transferred to or from storage.

Data Address

The Data Address is the address in main storage where data transfer is to start.

Interrupt Status Byte

When the attachment presents an interrupt request to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by condition codes. The interrupt status byte is meaningful only when interrupt condition code 2 or 6 is reported. The processor detects the interrupt status byte in bits 0 through 7 of the interrupt ID word.

The bits of the interrupt status byte and their meanings follow.

Bit 0—Device-Dependent Status Available. If this bit equals 1, additional status is available by using the Start Cycle Steal Status command (a discussion of this status follows in this chapter). This bit may be equal to 1 in conjunction with bit 2 (incorrect length record).

Bit 1—Delayed Command Reject. This bit equals 1 under the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The IDCB contains an odd DCB address.
- The command field of the IDCB specified a Write command (010X XXXX).

Bit 2—Incorrect Length Record. This error can occur during both transmit and receive operations. It is caused by either of the following conditions:

- The byte count has been decremented to 0, the attachment has not detected a COD character, and the chaining flag is off.
- The attachment has detected a COD character and the byte count has not been decremented to 0.

In this case, interrupt status byte bit 0 also equals 1. A Start Cycle Steal Status command can be used to determine the location of the COD in storage (residual address).

Bit 3—DCB Specification Check. Any of the following conditions causes this error:

- Word 5 of the DCB (chain address) contains an odd address.
- Word 6 of the DCB (byte count) contains a count other than 6 for a Start Cycle Steal Status command.
- Word 7 of the DCB (data address) contains an odd address for a Start Cycle Steal Status command.
- A byte count of 0 is specified in the DCB for either a transmit or receive operation.
- Bit 2 of the DCB control word equals 0 for a Start Cycle Steal Status command.
- Bit 3 of the DCB control word equals 1.

Bit 4—Storage Data Check. This bit equals 1 during cycle-steal output operations only. It indicates that the main storage location accessed during the current output cycle contains incorrect parity. The attachment terminates the operation with an exceptioninterrupt request.

Bit 5—Invalid Storage Address. This bit equals 1 if the address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation with an exceptioninterrupt request.

Bit 6—Protect Check. This bit equals 1 if the attachment attempts to access a storage location without the correct cycle-steal address key.

Bit 7—Interface Data Check. This bit equals 1 if a parity error has detected an interface cycle-steal data transfer. The condition can be detected by the channel or the attachment. In either case, the attachment terminates the operation with an exception-interrupt request.

Cycle-Steal Status Words

Three words of status information are available by using the Start Cycle Steal Status command.

The format of the DCB for this command is the same as for a normal cycle-steal data transfer. The chaining bit is not checked by the attachment, but it should equal 0. The byte count must be 6. Six bytes of information are transferred to main storage starting at the data address contained in DCB word 7.

Word 0

Word 0 contains the main storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or a DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Word 1

Word 1 has the following format.

Bit 0—Overrun. During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to main storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line.

Bit 1—Time-Out. This bit equals 1 if:

- DSR is not received from the modem within 3 seconds after an enable terminal operation begins (if bit 12 of DCB word 0 equals 1).
- Character phase is not established within 3 seconds of acceptance of a receive operation (if bit 12 of DCB word 0 equals 1).
- A continuous synchronization pattern is received for 3 seconds.
- While receiving data, no synchronization pattern is received for a period of 3 seconds.

Bit 2—Modem Interface Error. Conditions that cause this error are:

- DTR or DSR equals 0 at the beginning of a transmit or a receive operation.
- CTS equals 1 for more than 1 second while RTS equals 0 at the beginning of a transmit operation.
- DTR or DSR is lost during a transmit or a receive operation.
- RTS or CTS is lost during a transmit operation.
- CTS is not returned by the modem within 3 seconds after the attachment activates RTS.

Bit 3—Block Check Error. The BCC received over the data link does not compare with the BCC accumulated in the attachment. In ASCII mode, an LRC or VRC error is indicated by this bit.

Note: This error may also occur during heavy channel activity.

Bit 4—Multipoint Transmit Error. This bit indicates that the attachment is a tributary on a multipoint network and a transmit operation was attempted before the controlling station selected this station.

Bit 5—Answer-tone Jumper Installed. This bit indicates that the attachment is wired to provide an answer-tone when it senses that the 'ring indicator' line from the modem is active.

Bit 6—Multipoint Tributary Jumper Installed. This bit indicates that the attachment is a tributary station in a multipoint network.

Bit 7—Internal Clock Jumper Installed. This bit indicates that the internal clock jumper is installed in the attachment. The attachment provides clocking for 1,200 bps (600 bps if half-rate has been specified in the control word of the DCB).

Bits 8–15—Multipoint Address. These bits indicate that this is the multipoint address for which the attachment is wired.

Bit 8 equals multipoint address bit 0; bit 15 equals multipoint address bit 7.

Note: On single-line attachments, bit 8 (multipoint address bit 0) allows the attachment to IPL the processor when this bit equals 1, regardless of whether or not the attachment is a multipoint tributary. Bit 0 must not be wired on when using ASCII.

Word 2

Word 2 contains status information regarding certain key lines of the device and indicates that the following modem lines or conditions are active.

Bit 0—Data Terminal Ready. This bit is an outbound signal from the attachment to the modem indicating that the attachment is ready to communicate.

Bit 1—Data Set Ready. This bit is an inbound signal to the attachment from the modem indicating that power is on and the modem is ready for line operations.

Bit 2—Request to Send. This bit is an outbound signal from the attachment to the modem requesting that the modem prepare for data transmission.

Bit 3—Clear to Send. This bit is an inbound signal to the attachment from the modem indicating that the link is ready to transmit data.

Bit 4—Ring Indicator. This bit is an inbound signal to the attachment indicating that the modem detects a ring condition on the line; this is reported to the program as an attention interrupt request.

Bit 5—Half-Rate Selected. This bit is an outbound signal to the modem indicating that it should operate at half normal speed (modem must be equipped with this option); the signal is also called 'data signal rate selector.'

Bit 6—Transmit Mode Latch. This bit indicates that the attachment is transmitting data.

Bit 7. This bit is not used and should equal 0.

Bits 8 Through 15 (Indicator Panel Switch Setting). These bits indicate the current setting of the communications indicator panel DISPLAY/FUNCTION SELECT switches (if installed); bits equal 0 if communications panel is not installed.

Jumpering Information

The following options can be selected by installing jumper wires on the feature cards.

Binary Synchronous Communications Single-Line Control (Medium-Speed)

A Internal Clocking

With this jumper installed, the attachment provides clocking at 1,200 bps or 600 bps (selectable by programming).

B Answertone

With this jumper installed, the attachment provides a three second answertone after the modem activates 'data set ready' in response to the attachment activating 'data terminal ready'. This jumper should not be installed if the modem provides an answertone.

C Request to Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full-duplex modem. This option must be selected when using a modem which always keeps 'clear to send' active.

D Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

E No Ring Indication

This jumper must be installed if the modem does not provide a ring indication.

F Multipoint Tributary

This jumper is installed if the attachment is to be used as a multipoint tributary. It causes the attachment to look for its multipoint address on the receive data line after receiving an initial character synchronization sequence.

G Multipoint Address Jumpers

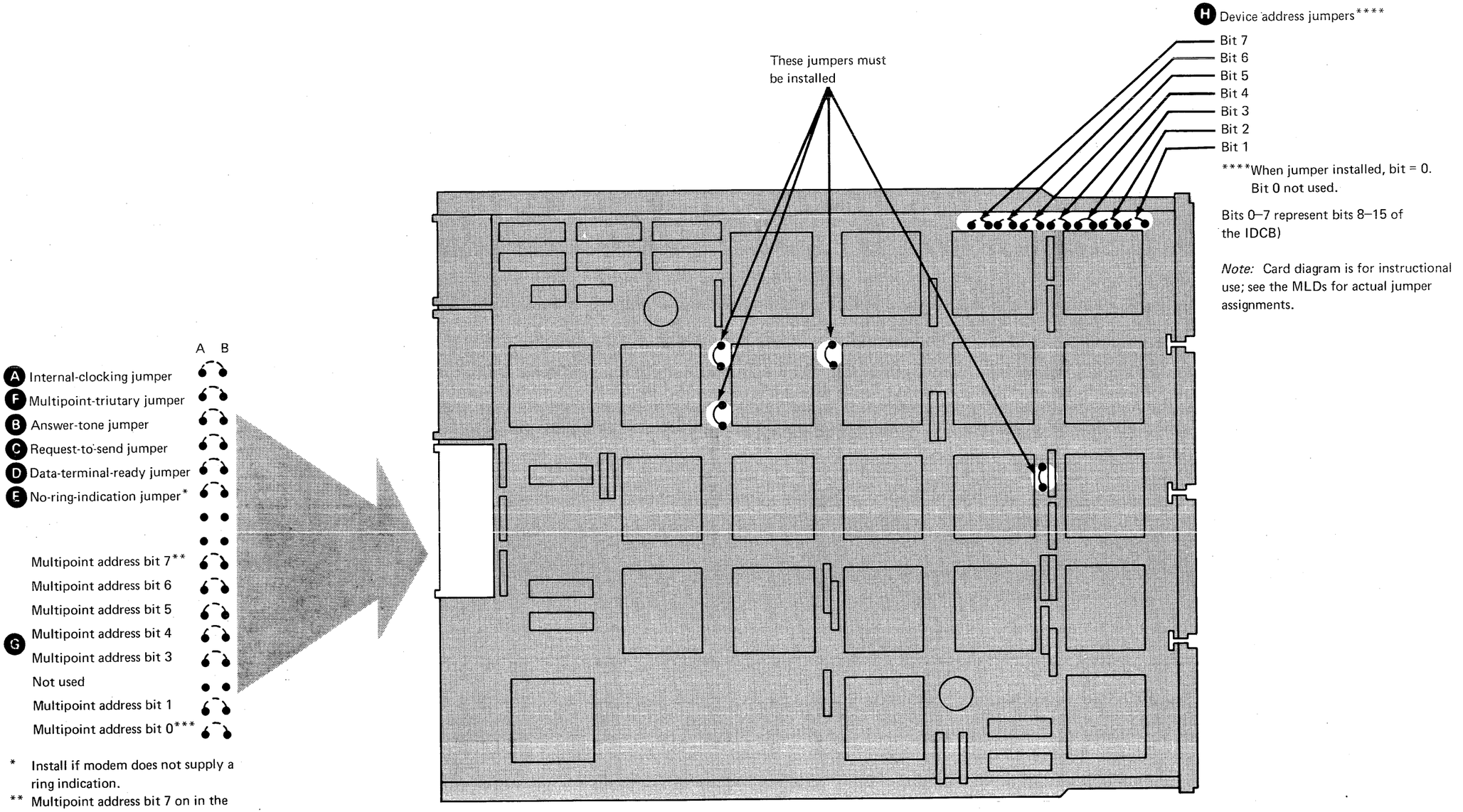
These jumpers establish the multipoint address to which the attachment is to respond.

If bit 0 is jumpered "on", the attachment is allowed to respond to a host initiated IPL sequence regardless of whether or not the multipoint tributary jumper is installed. Bit 0 must *not* be jumpered "on" when using ASCII code.

For switched-line operation, bit 7 must be jumpered "on", and the multipoint tributary jumper must not be installed.

H Device Address

These jumpers select the address of the attachment on the Series/1 I/O interface.



****When jumper installed, bit = 0. Bit 0 not used.

Bits 0–7 represent bits 8–15 of the IDCB)

Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

* Install if modem does not supply a ring indication.

** Multipoint address bit 7 on in the absence of the multipoint tributary jumper indicates switched-line operation.

***If this jumper is installed, the attachment is allowed to receive a host-initiated IPL.

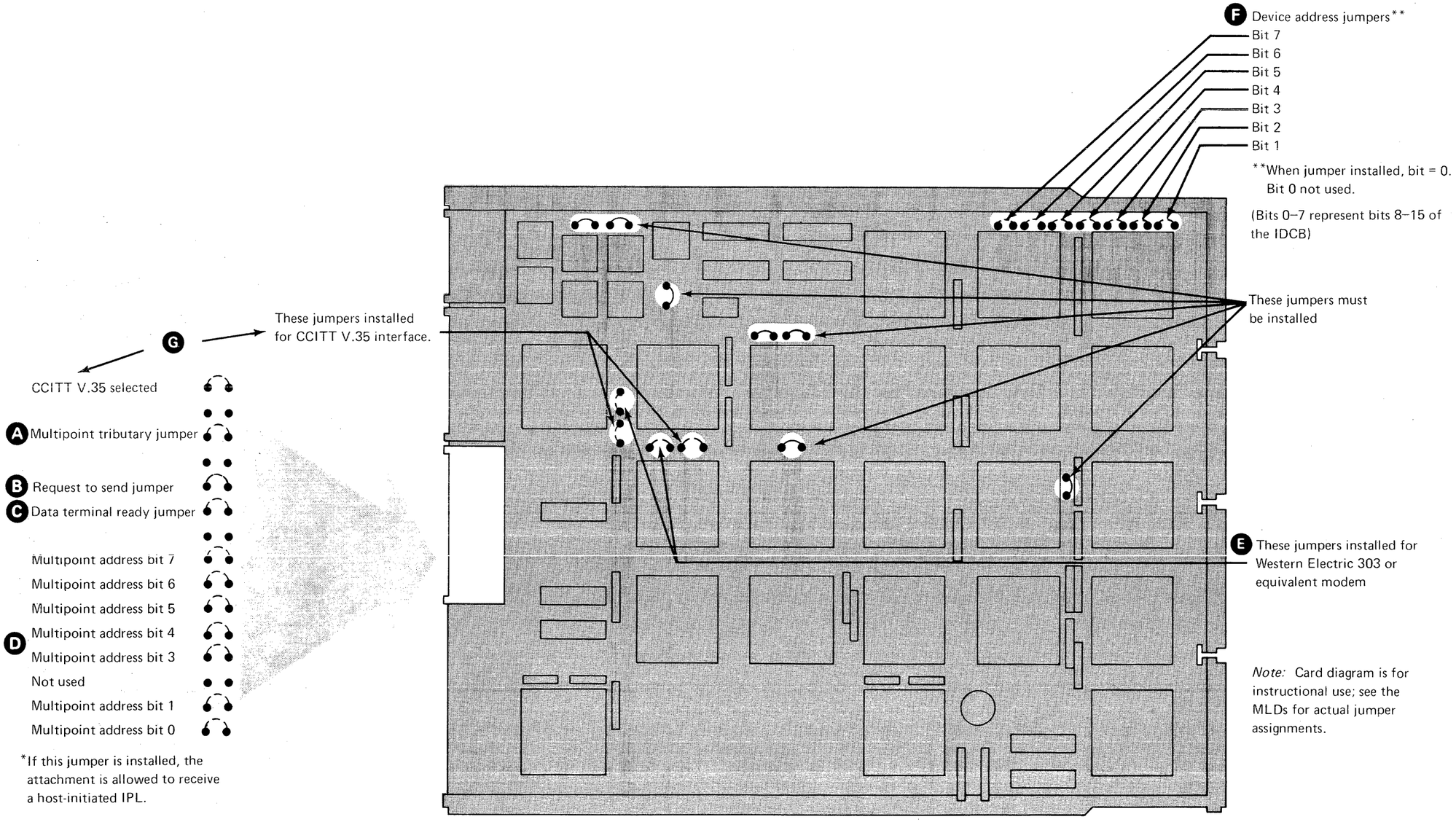
Binary synchronous communications single-line control (medium-speed)

Binary Synchronous Communications Single-Line Control (High-Speed)

The high speed attachment has the following jumpers which perform functions identical to those described for the medium-speed, single-line attachment:

- Multipoint tributary
- Request to send
- Data terminal ready
- Multipoint address
- Device address

In addition to the above options, the attachment has jumpers to select either an interface compatible with a Western Electric 303 data set (or equivalent) or an interface compatible with the Consultative Committee on International Telephone and Telegraph (CCITT) recommendation V.35.



Binary synchronous communications single-line control (high-speed)

Binary Synchronous Communications 4-Line Adapter

There are four complete sets of jumpers on each card—one set for each line.

A Internal Clocking

With this jumper installed, the attachment provides clocking at 1,200 bps or 600 bps (selectable by programming).

B Answertone

With this jumper installed, the attachment provides a three second answertone after the modem activates 'data set ready' in response to the attachment activating 'data terminal ready'. This jumper should not be installed if the modem provides an answertone.

C Request To Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full-duplex modem. This option should always be selected when using a modem which always keeps 'clear to send' active.

D Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation.

E No Ring Indication

This jumper must be installed if the modem does not provide a ring indication.

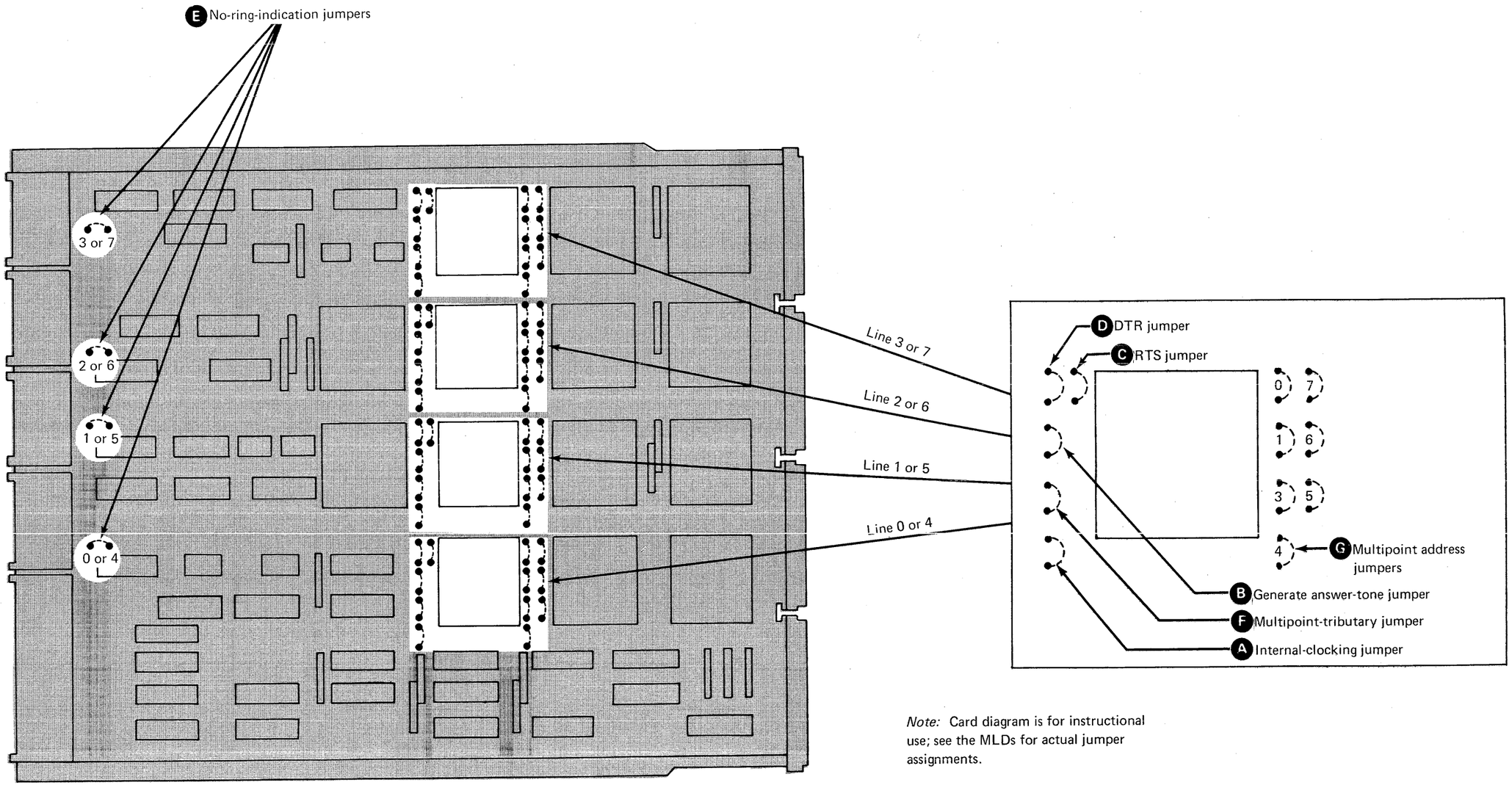
F Multipoint Tributary

This jumper is installed if the attachment is to be used as a multipoint tributary. It causes the attachment to look for its multipoint address on the receive data line after receiving an initial character synchronization sequence.

G Multipoint Address Jumpers

These jumpers establish the multipoint address to which the attachment is to respond. Bit 0 must *not* be jumpered "on" when using ASCII code.

For switched-line operation, bit 7 must be jumpered "on", and the multipoint tributary jumper must not be installed.



Binary synchronous communications 4-line adapter

Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

Binary Synchronous 8-Line Controller

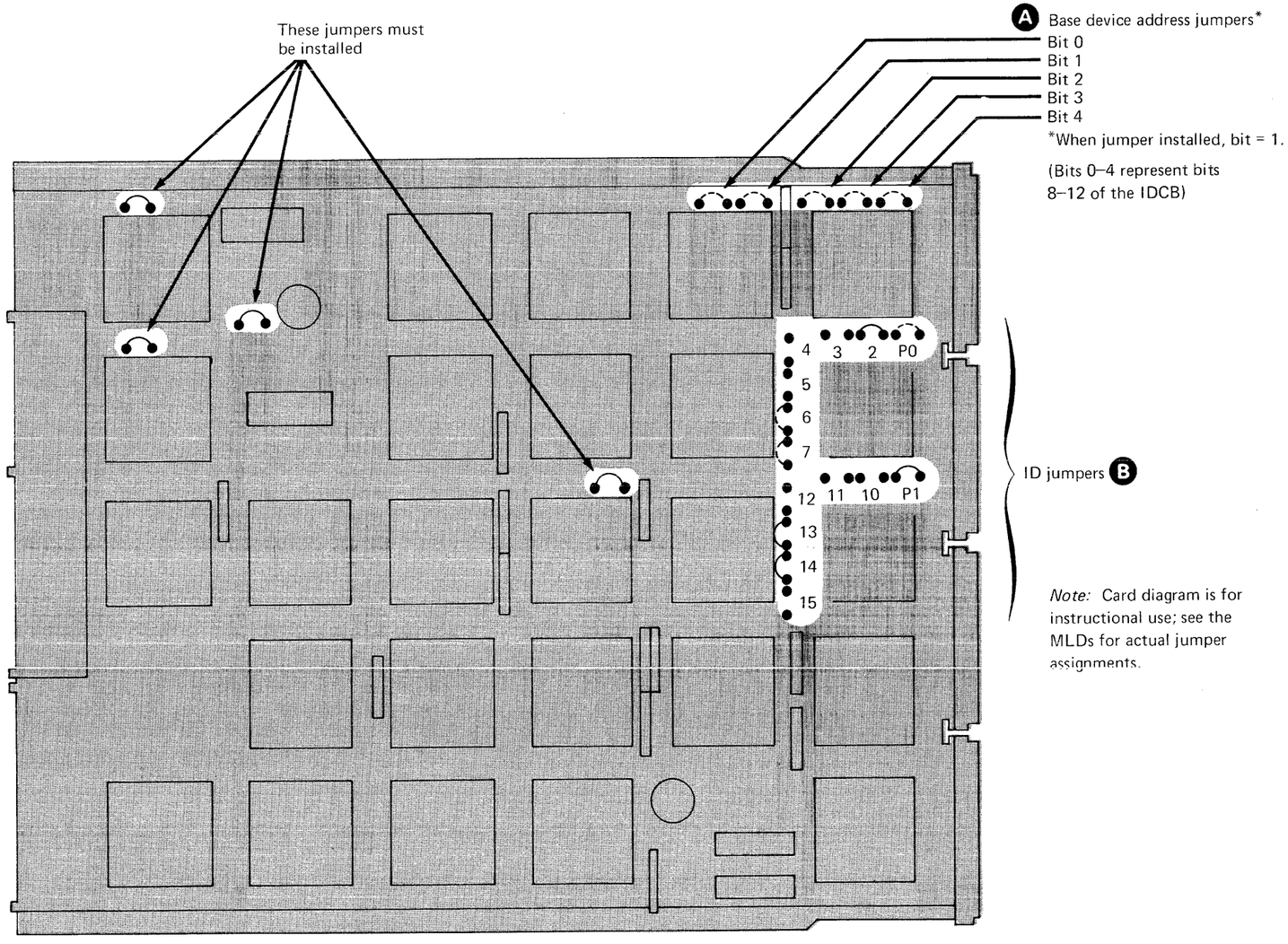
Device Address

These jumpers select the address of line 0 on the Series/1 I/O interface.

ID Jumpers

These jumpers determine the information that the attachment will pass to the processor during the *Read ID* instruction. The jumpers should be as follows:

Bit 2	On
Bits 3–5	Off
Bits 6 & 7	These are determined by the number of lines installed. 2 lines—bit 6 off, bit 7 on 4 lines—bit 6 on, bit 7 off 6 lines—bit 6 on, bit 7 on 8 lines—bit 6 off, bit 7 off
Bit P0	Jumpered as required to maintain odd parity in the high order byte of the ID word.
Bits 13, 14, P1	On
Bits 10–12, 15	Off



Binary synchronous 8-line controller

Status After Reset

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	Action
Power-on reset	All attachment components are reset to the off condition.
System reset/ Device reset	All attachment components (except DTR latches and the cycle-steal residual address) are reset to the off condition. The controller-end interrupt request is not affected by a device reset.

Note: For a System Reset, Device Reset, or Halt I/O command, the information displayed by indicator panel switch settings 0-C is not reset.

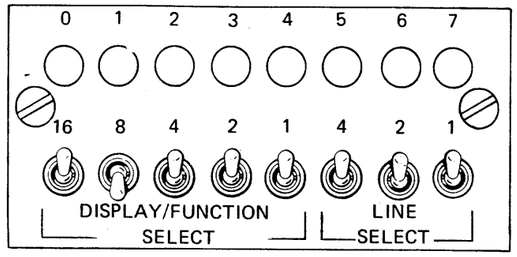
Multiple-Line Attachment Operation

The BSC multiple-line attachment controller is designed to service one or two binary synchronous communication 4-line adapter features. The BSC multiple-line attachment contains hardware and a microprocessor to service the 4-line adapter. The basic difference between the multiple-line attachment and the single-line attachment (other than speed limitations) is that the multiple-line attachment presents a controller busy operate I/O condition code to the program, followed by a controller-end interrupt request when its hardware is no longer busy.

The programmer should be aware that when multiple controller busy operate I/O condition codes are presented, there may be one controller-end interrupt request. The programmer should queue the controller busy Operate I/O condition codes and clear (post) the controller-end interrupt condition code to all the controller busy codes received.

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine troubleshooting.



LINE SELECT Switches

The three LINE-SELECT switches are used only with multiple-line attachments. They are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the LINE-SELECT switches. The LINE-SELECT switches are ignored when the indicator panel is used with a single-line attachment.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed on the panel. The following are lists of switch settings and the information that is displayed on the panel.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of DCB word 0 (control word)
00001	0–7	Low-order byte of DCB word 0 (control word)
00010	0–7	High-order byte of DCB word 5 (chain address)
00011	0–7	Low-order byte of DCB word 5 (chain address)
00100	0–7	High-order byte of DCB word 6 (byte count)
00101	0–7	Low-order byte of DCB word 6 (byte count)
00110	0–7	High-order byte of DCB word 7 (data address)
00111	0–7	Low-order byte of DCB word 7 (data address)
01000	0–7)	High-order byte of the storage data register
01001	0–7)	Low-order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High-order byte of cycle-steal status word 1
01101	0–7	High-order byte of the CRC
01110	0–7	Low-order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half-rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data (on = space)
	5	Receive data (on = space)
	6	Transmit mode
	7	Receive mode

(Part 1 of 2). Indicator panel information—single-line BSC features

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
10001	5	Answer-tone jumper installed
	6	Multipoint tributary jumper installed
	7	Internal clocking jumper installed
10100	0–7	Multipoint address
10110	0	COD
	1	BCC
	2	Text Mode
	3	Transparent mode
	4	DLE 1
	5	Character phase
	6	SYN 2
	7	SYN 1
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
	4	ASCII mode
11000	0	Second DC1
	1	First DC1 IPL sequence
	2	Address 2 (MP address received)
	3	Address 1 (MP address received)
11010	5	ITB sent or received
	6	EOT/NAK sent or received
11011	3	EOT sent or received
11100	0–7	Lamp test; all lamps should be on
11111	0–7	Same as switch setting 10000; resets DTR.

Note: Switch settings and lamp indications other than those shown require detailed knowledge of the microcode to understand.

(Part 2 of 2). Indicator panel information—single-line BSC features

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of DCB word 0 (control word)
00001	0–7	Low-order byte of DCB word 0 (control word)
00010	0–7	High-order byte of DCB word 5 (chain address)
00011	0–7	Low-order byte of DCB word 5 (chain address)
00100	0–7	High-order byte of DCB word 6 (byte count)
00101	0–7	Low-order byte of DCB word 6 (byte count)
00110	0–7	High-order byte of DCB word 7 (data address)
00111	0–7	Low-order byte of DCB word 7 (data address)
01000	0–7)	High-order byte of the storage data register
01001	0–7)	Low-order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High-order byte of cycle-steal status word 1
01101	0–7	High-order byte of the CRC
01110	0–7	Low-order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half-rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data
	5	Receive data
	6	Transmit mode
	7	Receive mode

(Part 1 of 2). Indicator panel information—multiple-line BSC features

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
10001	4	Interrupt pending
	5	Answer-tone jumper installed
	6	Multipoint tributary jumper installed
	7	Internal clocking jumper installed
10100	0–7	Multipoint address
10101	0	Enable timer bit
	1–7	Timer value in 50-milliseccond increments
10110	0	COD sent or received
	1	BCC sent or received
	2	Text Mode
	3	Transparent mode
	4	DLE sent or received
	5	Character phase
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
11000	2	Address 2 (MP address received)
	3	Address 1 (MP address received)
11001	1	ITB sent or received
	2	EOT/NAK sent or received
	7	EOT sent or received
11100	0–7	Lamp test; all lamps should be on
11101	0–7	First character after character phase in receive
11110	0–7	Contains last COD character sent or received
11111		Resets DTR if it is not jumpered "on"

Note: Switch settings and lamp indications other than those shown require detailed knowledge of the microcode to understand.

(Part 2 of 2). Indicator panel information—multiple-line BSC features

Chapter 3. Synchronous Data Link Control

The Synchronous Data Link Control (SDLC) Single-Line Control feature is an option which controls transfer of serial data to and from a remote terminal or host system via a modem and communications line facility. In this chapter, this feature is referred to as the *attachment*. The SDLC attachment can be used for connecting a Series/1 processor to telecommunication equipment or other processors having compatible adapters.

- Data transmission uses synchronous data link procedures
- Any eight-bit data codes may be used
- It is available as a single-line, medium-speed, half-duplex attachment *only*
- Bit rates can be up to 9,600 bps
- It may be used as either a primary or secondary station
- Internal clocking is available
- Non-return-to-zero inverted (NRZI) coding is used with internal clocking
- Non-return-to-zero (NRZ) coding or NRZI coding may be used with external clocking (supplied by the modem)
- Answertone generation can be provided by installing a jumper on the attachment card
- The attachment does not support station-address-field extensions or control-field extensions.

Data transmission is serial-by-bit, using the synchronous data link control (SDLC) method of character and bit transmission. A general discussion of the SDLC procedures may be found in "IBM Synchronous Data Link Control—General Information", GA27-3093.

The attachment can communicate with host systems or terminals using EBCDIC (Extended Binary-Coded Decimal Interchange Code) or ASCII (American Standard Code for Information Interchange) or any other eight-bit data codes. SDLC uses a specific set of line control characters, but because transparency is inherent in SDLC, the data characters can be any eight-bit code that the sending and receiving stations agree upon.

The SDLC attachment is a single-line half-duplex device that can operate on a switched or non-switched line at rates up to 9,600 bps (using external clocking).

Internal (business machine) clocking can be connected during installation if the modem does not supply clocking. The characters are transmitted and received using NZRI coding if internal clocking is used. When clocking is provided by the modem, either NRZ or NRZI coding may be selected by the software. Internal clocking provides the strobe pulses used to strobe bits between the modem and the adapter. In receive mode, it also establishes and maintains bit synchronization through an advance or retard of the data strobe. Transmission rates of 600 or 1,200 bps are available through the internal clocking feature.

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Data Flow

Each character occupies a byte position in storage. Transfers to and from storage are two bytes at a time, except that the first and/or last transfers may move only one byte if specified by the data address or byte count.

Transmit

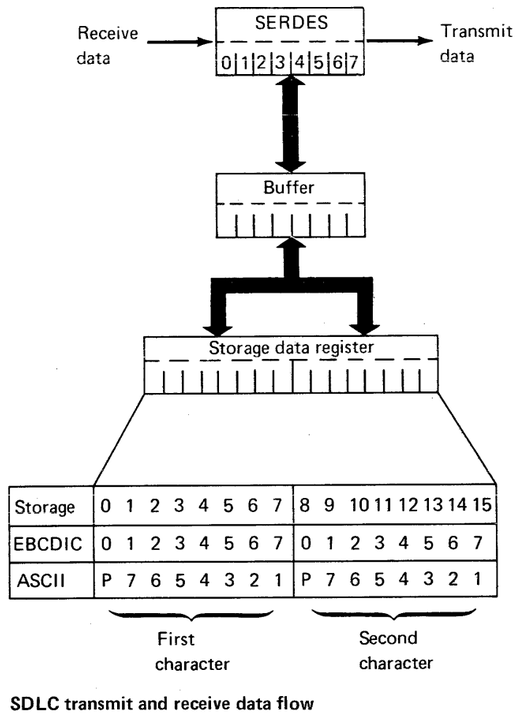
Transmission data is fetched from storage two characters at a time. The high order byte holds the first character to be sent and the low order byte holds the next character. After a character has been transferred into SERDES, it is transmitted over the line serially, low order bit first.

Note: If the data address in DCB word 7 is odd, only one character is fetched from storage on the first data transfer.

Receive

The first bit received is transferred into the low order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on, until a character is assembled. The first character received is loaded into the high order byte of the storage register and the next character is loaded in the low order byte. The attachment provides buffering for four bytes of data. This allows the attachment to recognize an ending flag without putting the FCS (Frame Check Sequence) into storage. Data is written into main storage without any code translation.

Note: If the data address (DCB word 7) is odd, only one character is sent to storage on the first data transfer.



SDLC transmit and receive data flow

SDLC Feature Configuration

The SDLC attachment is contained on a single card which can be installed in any I/O card slot in the processor enclosure or in the input/output expansion unit. The attachment is available only in a single-line, half-duplex configuration. Connections to the modem and the indicator panel are made by top-card connectors.

Functional Units

I/O Channel Attachment Logic

This portion of the attachment performs the handshaking functions that are necessary for communications between the attachment and the processor I/O channel.

Microcontroller

The microcontroller controls everything the attachment does. It contains a microprocessor and a Read Only Storage (ROS). It automatically steps the attachment through every operation.

Line Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and cmmunications line.

Buffer

The buffer provides one byte of temporary storage between the microcontroller and the SERDES (serializer/deserializer).

SERDES (Serializer/Deserializer)

This is the portion of the attachment that converts the data from parallel form to serial form (transmit operation) and from serial form to parallel form (receive operation).

SERDES Control

The SERDES Control includes a bit counter, a ones counter, and circuits for inserting and deleting zeros in the bit stream. It also handles conversion from NRZ to NRZI on transmit operations and from NRZI to NRZ on receive operations.

The bit counter keeps track of when the SERDES is either empty or full and tells the SERDES when to transfer data to or from the buffer.

The ones counter counts the number of consecutive ones transmitted or received. It also detects flags, abort conditions, idle conditions, and when a zero should be inserted or deleted.

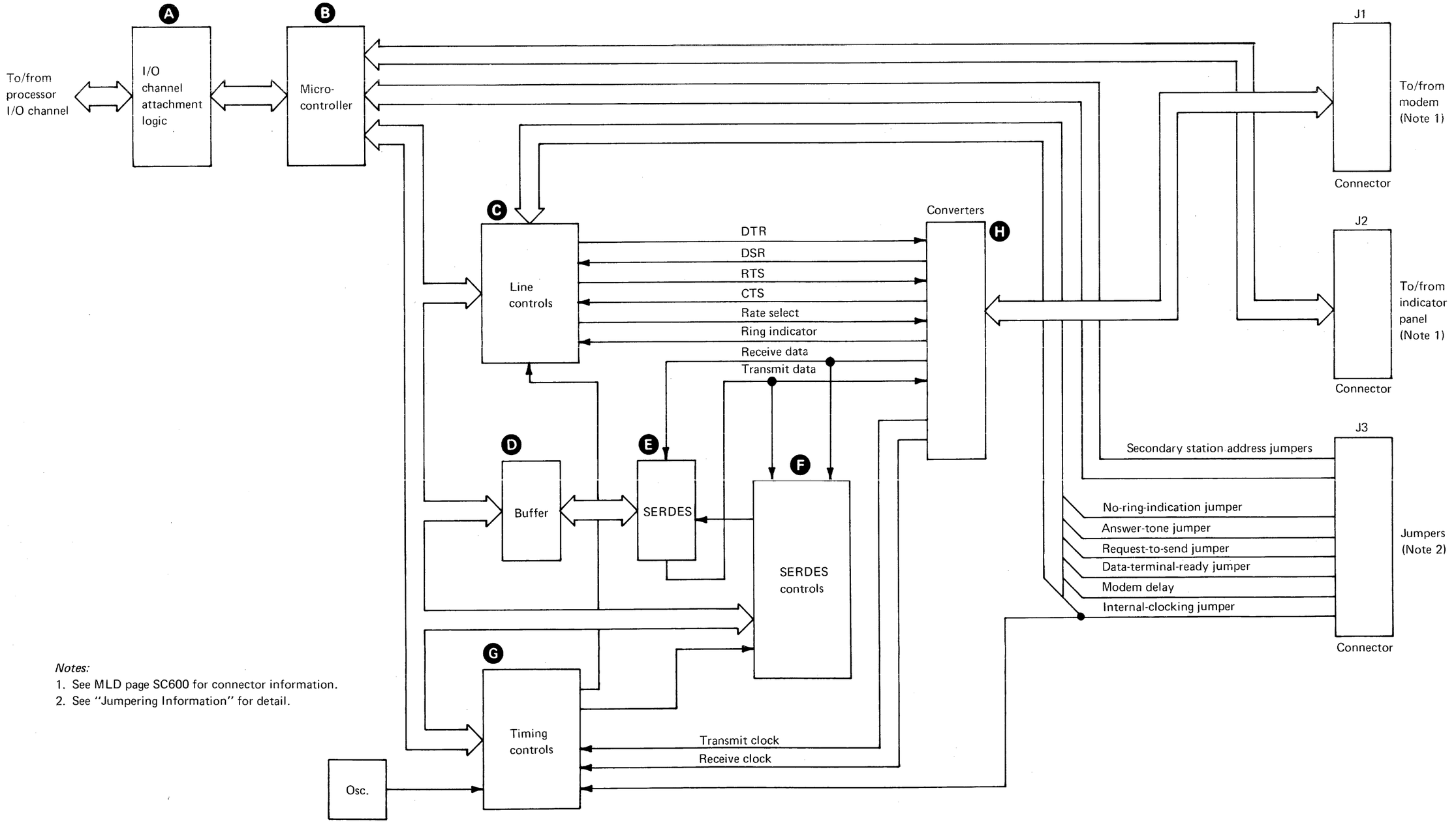
The zero insertion/deletion circuit either inserts zeros (transmit) or deletes zeros (receive) on signal from the ones counter.

Timing Controls

This portion of the attachment supplies timing to the line controls and SERDES controls.

Converters

The converters change the signals going to the modem to signals that are compatible with the modem. They also change signals coming from the modem to signals that are compatible with the modem.



Notes:

1. See MLD page SC600 for connector information.
2. See "Jumpering Information" for detail.

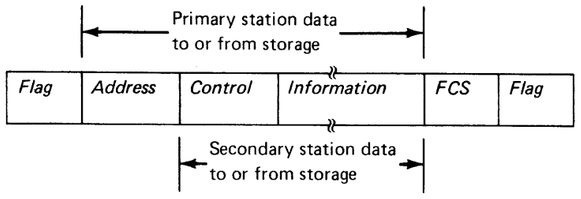
Operating Modes

Monitor Mode

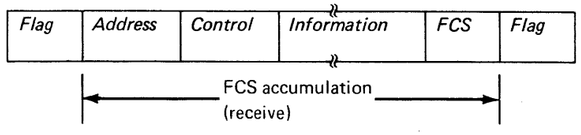
The attachment is placed in monitor mode by a Receive command. While in this mode, the attachment is constantly monitoring the line, looking for a flag character. If the attachment is operating as a primary station it immediately goes into receive mode upon recognizing a flag character. If the attachment is operating as a secondary station, it checks the address following the flag. If the address is its own (or the broadcast address), the attachment goes into receive mode. If the address is not the address of the attachment, the attachment remains in monitor mode.

Receive Mode

If the attachment is operating as a primary station, data is transferred to main storage beginning with the A-field. When the attachment is operating as a secondary station in receive mode, data is transferred to main storage beginning with the C-field. If the attachment is operating as a secondary station, the attachment automatically checks the received address to determine if the frame is intended for this station. If the frame is intended for this station, the attachment transfers the data to storage (beginning with the C-field).

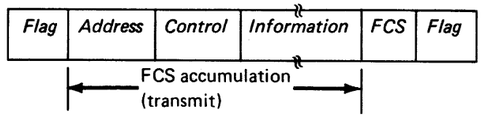


The accumulation of frame-check sequences starts with the address and includes the frame-check sequence received.



Transmit Mode

This mode is established when a Transmit command has been issued by the program. Frame-check sequence accumulation begins with the first character to be transmitted after the beginning flag character and continues until the byte count, device control block (DCB) word 6, is decremented to 0.



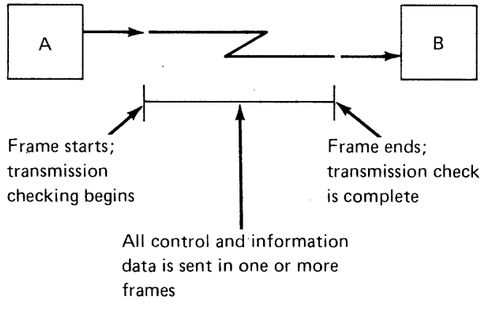
The frame-check sequence is then automatically transmitted, followed by a flag character. If the attachment is operating as a primary station, the address of the receiver comes from storage. If the attachment is operating as a secondary station, the hardware provides the A-field of the frame.

Transmission Codes

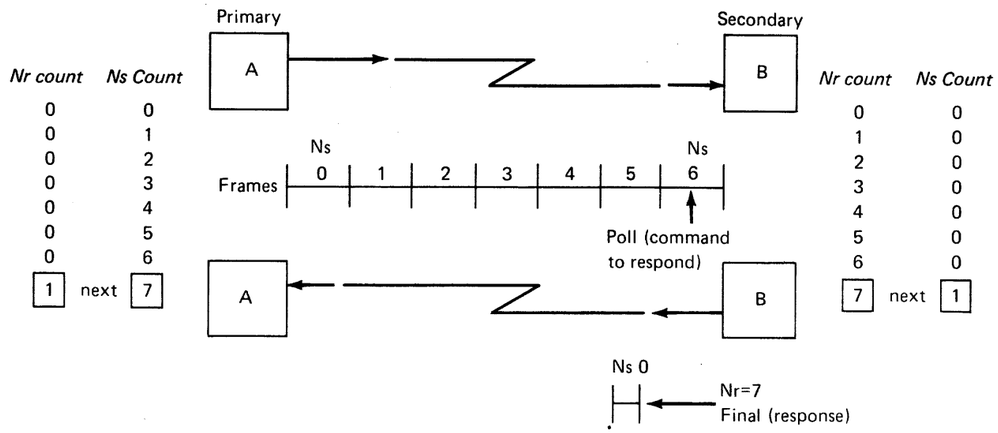
The SDLC attachment allows data communication using any eight-bit data code including EBCDIC or ASCII. The EBCDIC and ASCII character assignments are shown in Appendix A.

Control Characters

Two levels of information grouping are in SDLC procedures. The basic level, called a *frame*, is checked by the attachment for transmission errors. The frame is the vehicle for every command, every response, and all information that is transmitted using SDLC procedures.



The higher level of grouping, a frame sequence, is checked by the program for missing or duplicated frames. At a station that transmits sequenced frames, the program counts and numbers each sequenced frame; this count is called Ns. At a station receiving sequenced frames, the program counts each error-free sequenced frame that it receives; this count is called Nr.



If B responds with Nr =:

7 (as above, all frames check OK)
6 (frame 6 discarded because of error)
5 (error on frame 5; 5 and 6 discarded)
4 (error on frame 4; 4–6 discarded)
3 (error on frame 3; 3–6 discarded)
2 (error on frame 2; 2–6 discarded)
1 (error on frame 1; 1–6 discarded)
0 (error on frame 0; no frames accepted)

A may send, on request, Ns frames:

7, 0, 1, 2, 3, 4, 5 (continue)
7, 0, 1, 2, 3, 4 (retransmit and continue)
7, 0, 1, 2, 3 (retransmit and continue)
7, 0, 1, 2 (retransmit and continue)
7, 0, 1 (retransmit and continue)
7, 0 (retransmit and continue)
7 (retransmit and continue)
(retransmit)

Note: Shaded frames are retransmitted.

The program advances the Nr count when a frame is checked and found to be error-free. Nr then becomes the count of the next-expected frame and should agree with the next incoming Ns count. If the incoming Ns does not agree with Nr, the frame is out of sequence and the count Nr does not advance. Out-of-sequence frames may be rejected or saved, at the option of the program. The receiving station does accept the incoming Nr count (confirmation) if the out-of-sequence frame is otherwise error-free.

The counting capacity for Nr or Ns is 8, using the digits 0 through 7. These counts can "wrap around;" that is, 7 is followed by 0. Up to seven frames may be sent before the receiver reports its Nr count to the transmitter because some or all of the frames may need repeating. The reported Nr count is the sequence number of the next frame that the receiving station expects to receive; therefore, if the count is not the same at a checkpoint as the transmitter's next sequence number, some of the frames already sent must be repeated.

The Nr and Ns counts of both stations are initialized to 0 at the discretion of the primary station. At other times, the counts advance as sequenced frames are sent and received.

Frame Format

All active communication regulated by SDLC procedures have a format called a frame. Each frame is enclosed in flags.

Starting from the beginning flag as a reference point, eight consecutive binary bits are dedicated to the address (A) of the secondary station. The next eight consecutive bits comprise the control (C) information, which can be a command or response. At least 16 more bits are transmitted after the C-field before the ending flag is sent. These 16 bits, the frame-check sequence (FCS), contain the transmission checking information; therefore, the internal structure of any valid frame must consist of at least 32 consecutive binary bits.

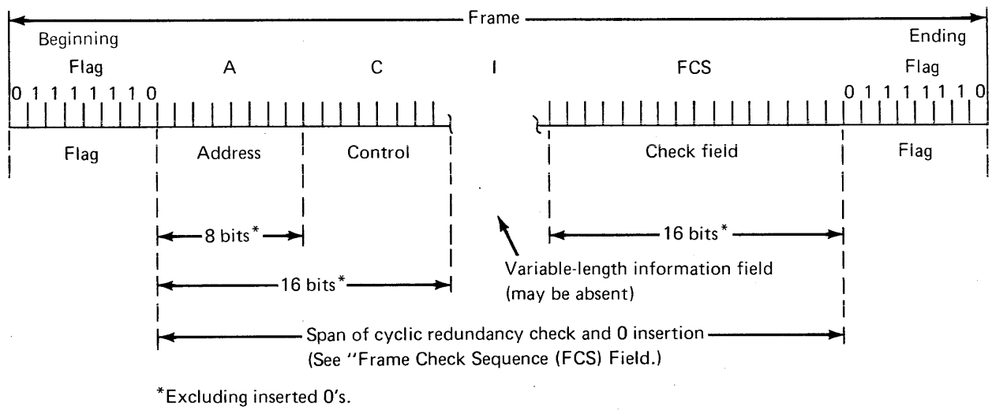
Any information (I) field is sent following the C-field and preceding the frame-check sequence field. The I-field is not restricted in format or content. In a frame with an I-field, the maximum length is not restricted by procedures.

The transmission check at the receiver is complete when the ending flag is recognized. The receiving attachment separates the I-field from frame-check sequence information when the ending flag is received, and does not put the frame-check sequence into storage.

Flag

Two flags, the beginning flag and the ending flag, enclose the SDLC frame. The beginning flag serves as a reference for the position of the A- and C-fields and initiates transmission error checking; the ending flag terminates the check for transmission errors. Both beginning and ending flags have the binary configuration 01111110. The bit orientation of SDLC allows the flag to be recognized at any time.

A flag may be followed by a frame or by another flag.



*Excluding inserted 0's.

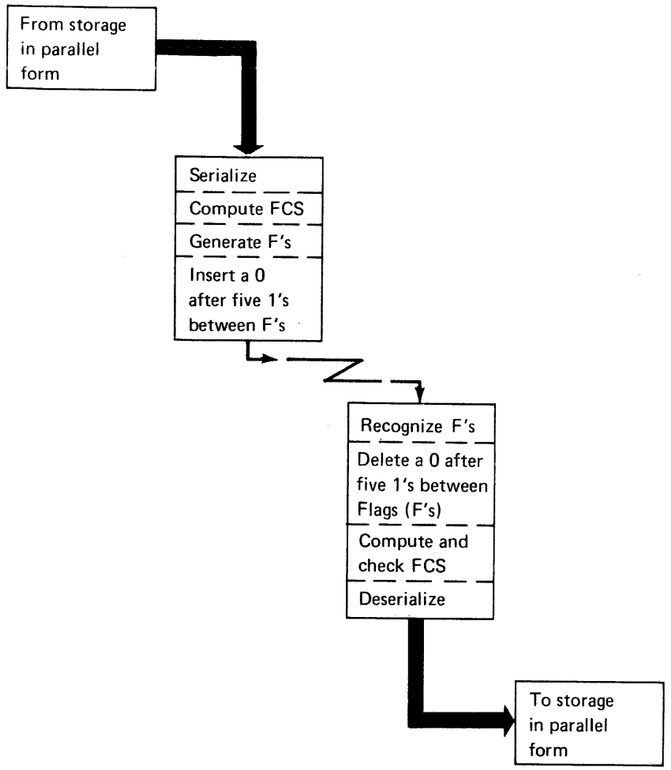
Frame Format

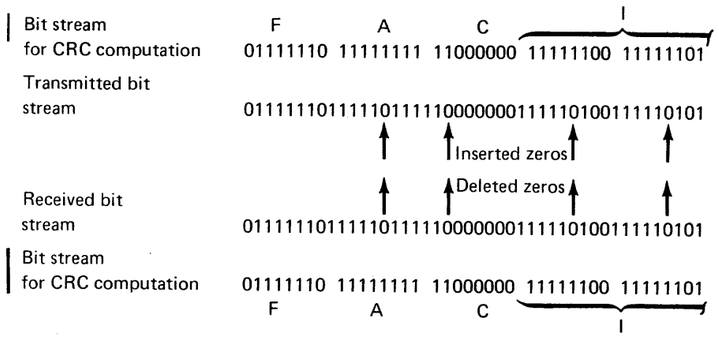
Zero Insertion

A frame can be identified because it begins with a flag and contains only non-flag bit patterns. (The frame ends at the next flag.) This characteristic does not restrict the contents of a frame, because SDLC procedures require that a binary 0 be inserted by the transmitted station after any succession of five contiguous 1's within the frame. No pattern of 01111110 (flag) is ever transmitted by chance. After testing for flag recognition, the receiver removes a 0 that follows a received succession of five contiguous 1's. The attachment automatically provides zero insertion and deletion. Inserted and removed 0's are not included in the transmission error check. (A one that follows five ones is not removed.)

Note: When NRZI transmission recording is used, zero insertion eliminates the remaining possibility of prolonged transitionless periods in the active state

NRZI transmission allows the transmit data line to change states when a logical zero is transmitted.





Data Link Control Functions and Zero Insertion/Deletion

Idle Stations

A series of contiguous flags may be transmitted by a station to maintain bit synchronization and to maintain the data link in an active state. A series of flags may also be used to hold the authority to transmit and to avoid time-outs at the linked station(s).

Note: The use of NRZI transmission recording and zero insertion is restricted to the active state of the data link; neither one operates in the idle state

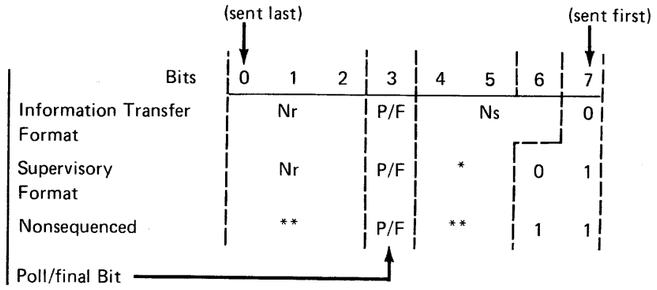
Address Field

The primary station manages a data link by issuing commands to the secondary stations that recognize their address in the A-field of a received frame.

A primary station can address all secondaries by sending an *all 1's* address (hex FF). A secondary station may receive a common address or its individual address; however, when a secondary station sends any response, only its individual address is used.

Control Field and the Poll/Final (P/F) Bit

The C-field contains, within its eight binary digits, the capability to encode the commands and responses required to control a data link. The C-field has three formats, as shown here:



*Codes for supervisory commands/responses
**Codes for nonsequenced commands/responses

Each C-field contains the format identifier and poll/final bits. The codes for the C-field commands and responses are shown here:

Format (See Note)	Sent last → Binary configuration → Sent first			Acronym	Command	Response	I-field prohibited	Resets Nr and Ns	Confirms frames through Nr-1	Defining characteristics
NS	000	P/F	0011	UI	X	X				Command or response that requires unnumbered information
	000	F	0111	RIM		X	X			Initialization needed; expect SIM
	000	P	0111	SIM	X		X	X		Set initialization mode; the using system prescribes the procedures
	100	P	0011	SNRM	X		X	X		Set normal response mode; transmit on command
	000	F	1111	DM		X	X			This station is offline
	010	P	0011	DISC	X		X			Do not transmit or receive information
	011	F	0011	NSA		X	X			Acknowledge NS commands
	100	F	0111	FRMR		X				Invalid frame received; must receive SNRM, DISC, or SIM
	101	P/F	1111	XID	X	X				System identification in I-field
	001	P/F	0011	NSP	X		X			Response optional if no P-bit
	111	P/F	0011	TEST	X	X				Check pattern in I-field
S	Nr	P/F	0001	RR	X	X	X		X	Ready to receive
	Nr	P/F	0101	RNR	X	X	X		X	Not ready to receive
	Nr	P/F	1001	REJ	X	X	X		X	Transmit or retransmit, starting with frame Nr
I	Nr	P/F	Ns 0	I	X	X			X	Sequenced I-frame

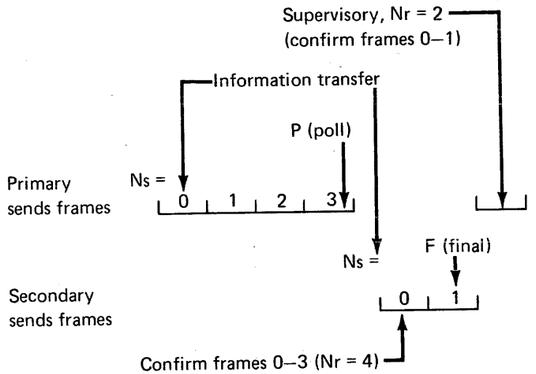
Note: NS = nonsequenced, S = supervisory, I = information.

The poll/final (P/F) bit is the send-receive control. A poll bit is sent to a secondary station to authorize transmission; a final bit is returned by the secondary station in response to the poll bit. (Do not confuse the final bit with the F (flag) frame delimiter pattern.) Normally, only one poll bit is outstanding (unanswered by a final bit) on a data link.

Information Transfer Format

A C-field in the information transfer format is a part of each sequenced frame that is transmitted over a data link. It contains the poll-final bit and the Nr and Ns counts.

Stations transmitting information-transfer frames request configuration by sending the Ns count; they confirm by sending the Nr count.



Supervisory Format

The supervisory format is an adjunct to the information transfer format. Frames containing a C-field of the supervisory format convey ready or busy conditions and may be used to report sequence errors (thus requesting retransmission). Such frames may be interspersed with frames having a C-field of the information transfer format. Whether or not a primary station has information data to transmit, it may use a frame having a C-field of the supervisory format to poll a secondary station. A secondary station may use the supervisory format to respond to a request for confirmation. Frames with a supervisory format C-field are not counted in the Nr or Ns counts.

Nonsequenced Format

Command and response frames having a C-field of this format are used for data link management. Data link management includes activating and initializing secondary stations, controlling the response mode of secondary station, and reporting of procedural errors (not recoverable by retransmission). Information data may also be transmitted, using a frame with a C-field of the nonsequenced format. Frames with a nonsequenced format C-field are not counted in the Nr or Ns counts.

Information Field

SDLC procedure are desinged as a vehicle for data contained in the I-field. The I-field contains data that is moved, by using the data link, from place to place in the system. The I-field is unrestricted in format and content; its contents are not apparent to the components of data link control.

An I-field is normally included with every frame having a C-field of the information-transfer format. These information-transfer frames are the only ones that are sequenced.

There are provisions for an I-field in frames with a nonsequenced format C-field, but these are unprotected by sequence checking.

Frame Check Sequence Field

The frame-check sequence field (also called block check character (BCC) contains 16 binary digits. It follows the I-field (if there is one; the C-field if not) and immediately precedes the ending flag. These 16 digits result from a mathematical computation on the digital value of all binary bits within the frame (excluding inserted 0's). The purpose is to validate transmission accuracy.

The transmitting SDLC attachment performs the computation and sends the resulting frame-check sequence value. The receiving SDLC attachment performs a similar computation and checks its results; it discards a frame that is found to be incorrect and does not advance its Nr count.

Synchronization

The basic SDLC attachment receives timing pulses from the modem. This establishes and maintains bit synchronization. When the attachment starts to transmit, the attachment automatically transmits a flag character. This establishes frame and byte synchronization.

Some modems, to operate properly, may require NRZI-recorded data and/or pad characters. Bits 9 and 12 of the DCB control word can be used to satisfy particular modem requirements.

If internal clocking is used, the attachment operates in NRZI mode and automatically sends two pad characters (hex 00) prior to sending the beginning flag. This causes 16 bit transitions to take place before the flag character is sent.

Timers

The attachment has two programmable timers. Each timer can count up to 27 seconds, in 106-millisecond increments. Bits 0 through 7 of DCB word 1 control one timer; bits 8 through 15 control the second timer.

Timer 1

Timer 1 can be used in a variety of ways:

- Idle detect timer—If a receive operation is specified, the attachment runs timer 1 for the duration specified by bits 0 through 7 of DCB word 1. When this time times out, the attachment begins checking the line for an idle condition. If an idle condition is detected, the attachment presents an exception-interrupt request.

  If a flag character is detected while timer 1 is running, the attachment immediately begins checking for an idle condition and stops timer 1. If an idle condition is detected from the time that timer 1 stops until the receive operation ends, the attachment presents an exception-interrupt request.

  If the program assigns a value of 0 to timer 1, the attachment does not check for an idle condition.

  Note: An idle condition is 15 contiguous ones on the line.

- 'Data set ready' time-out—During an enable terminal operation, this time-out occurs if 'data set read' (DSR) is not returned by the modem within the specified time. If the condition of the rate select line will be changed during the enable terminal operation, this timer must be set to a value that will allow the modem enough time to equalize. Consult the manual for the modem being used to determine equalizaiton time.
- 'Disable data terminal ready' time-out—During a disable terminal operation, a time-out occurs if DSR is not deactivated within the specified time.
- 'Clear to send' time-out—During a transmit operation, a modem interface error occurs if 'clear to send' (CTS) is not returned by the modem within the specified time.
- Program delay—When the operation is not an enable terminal, disable terminal, receive, or transmit operation, timer 1 can be used by the program for timing puposes.

Timer 2

Timer 2 is used in two ways:

- Nonproductive receive time-out. This time-out is used only during receive operations. Its purpose is to limit the total nonproductive receiving time for a total receive operation. A total receive operation can be a single receive operation or a chain of receive operations initiated by a single Operate I/O instruction. When chaining receive operations, the value for timer 2 is taken from each DCB in the chain. The timer runs anytime that the attachment is not receiving flags or frames. When timer 2 times out, the attachment presents an exception interrupt request.
- Hold-line-active timer. When timer 2 is used in conjunction with a transmit operation with bit 15 on in the DCB control word, the attachment transmits flag characters for the duration of the time specified by bits 8 through 15 of DCB word 1, or until another transmit operation begins.

Note: When the timers are set to 0, no time-out occurs.

Commands

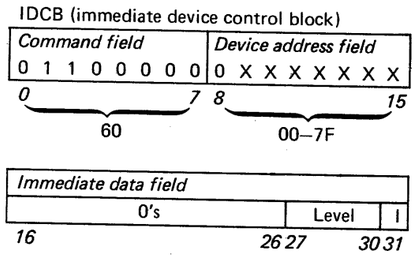
The Operate I/O instruction points to the immediate DCB (IDCB), which contains one of the following commands:

- Prepare
- Halt I/O
- Device Reset
- Start
- Start Cycle Steal Status
- Read ID
- Start Diagnostic 1
- Start Diagnostic 2

It is the programmer's responsibility to ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The data word contains the level and I-bit. The device is always able to accept and execute a Prepare command, even if it is busy or has an interrupt request pending from a previous command. The IDCB for the Prepare command has the following format:



Level This four-bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27–30 indicates priority levels of 0–3.

Example:

Bits 27–30	Level
0000	0
0001	1
0010	2
0011	3

I-Bit. This bit determines whether the device is allowed to present interrupt requests. An I-bit value of 1 means that the device can request to interrupt; a value of 0 means that the device cannot interrupt.

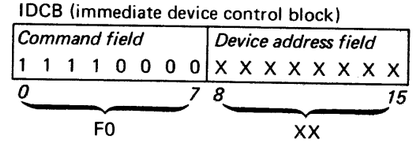
The attachment stores the level data and presents it to the processor each time the attachment presents an interrupt request. The prepare information (level and I-bit) is reset by a system reset or a power-on reset.

The Prepare command causes an interrupt request only when the attachment is not prepared (I-bit equal to 0) and has an interrupt request pending upon receipt of a Prepare with the I-bit equal to 1.

The Prepare command always causes an attachment to respond with satisfactory (CC7).

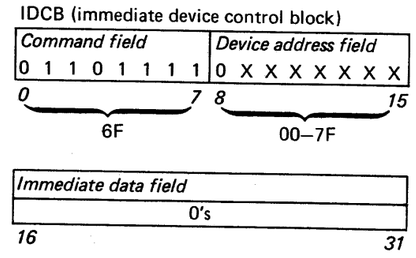
Halt I/O

This command halts all I/O activity on the I/O channel. The reset functions in the attachment are the same as those carried out for a Device Reset.



Device Reset

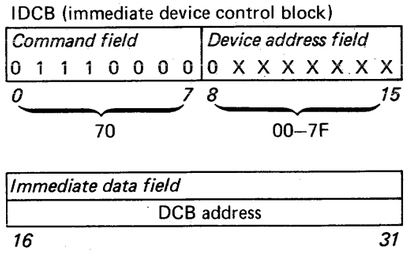
The Device Reset command resets the addressed device. Any pending interrupt requests are cleared. The prepared level, I-bit, residual address, and 'data terminal ready' (DTR) are not reset by this command. The Device Reset command has the following format:



A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are carried out. The amount of time that the attachment is busy is a function of the microcode program. The attachment presents a busy after reset (CC2) if an Operate I/O follows a Device Reset too closely.

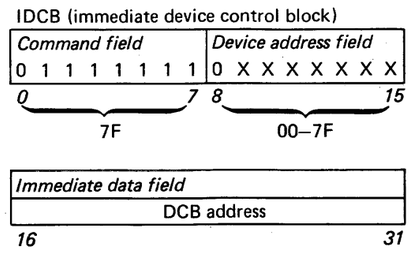
Start

The Start command transfers the address of a DCB to the attachment. When the Start command is accepted, the attachment fetches the DCB from the main storage address specified in the immediate data field of the IDCB and begins executing the operation.



Start Cycle Steal Status

The Start Cycle Steal Status command causes the attachment to transfer status information (about the previous cycle-steal operation to the processor. The attachment provides four words of cycle-steal status information. The byte count specified in word 7 of the DCB must be 8.



The data address (word 7) must be on a word boundary (bit 15 equal 0) or an exception interrupt request (CC2) will occur with DCB specification check bit (bit 3) equal to 1 in the interrupt status byte.

See "Cycle-Steal Status Words" (later in this chapter) for a description of the status information.

Read ID

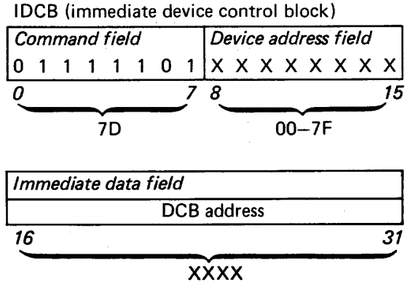
The Read ID command transfers the attachment's identification (ID) word from the attachment to the immediate data field of the IDCB. The ID word of the SDLC attachment is shown below as it appears in the immediate data field of the IDCB:

Diagnostic Commands

The Diagnostic Commands are used by diagnostic programs to check for corrrect operation of the attachment.

Start Diagnostic 1

The format of the IDCB for this command is:



The byte count for this operation must be 12 (hex 000C) and the data address must be even; otherwise, a DCB specification check will occur. The DCB control word should be hex 2000.

The Start Diagnostic 1 causes the following four tests to be performed in the attachment.

1. Register test—Upon recognition of the Start Diagnostic 1 command and before fetching the DCB, all registers accessible to the microcontroller are tested. If the test finds an error, the attachment will "hang" and proceed no further. If the test does not find an error, the attachment will fetch the DCB and proceed with test 2.
2. Check sum test—The read-only-storage (ROS) modules in the attachment have a check sum built into them when they are made. This test reads each location in ROS and calculates a check sum for each module. It then transfers the built-in and calculated check sums to storage as follows:

   Data word 0 = Built-in check sum ROS module 1

   Data word 1 = Calculated check sum ROS module 1 (inverted)

   Data word 2 = Built-in check sum ROS module 2

   Data word 3 = Calculated check sum ROS module 2 (inverted)
3. Function test—This test checks various circuits and latches in the attachment. The results are then placed in data word 4 in storage. The bits in data word 4 have the following significance:

Bit	Meaning
0	DTR active
1	DSR active
2	Not used
3	Not used
4	NRZ transmit tested successfully*
5	Not used
6	NRZI transmit tested successfully
7	Not used
8	Flag latch tested successfully
9	Abort latch tested successfully
10	Idle latch tested successfully
11	Buffer service latch tested successfully
12	Overrun latch tested successfully
13	Zero bit insert tested successfully
14	Transmit clock active
15	Receive clock active

*NRZ is not tested if the internal clock jumper is installed.

The following table shows the correct contents of data word 4 for various configurations:

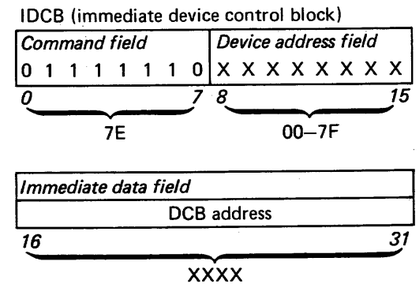
	With internal clocking	Without internal clocking*
Leased-line or switched-line with modem enable	C2FF	CAFC CAFD CAFE CAFF
Switched-line with modem disabled	82FF	8AFC 8AFD 8AFE 8AFF

*State of bits 14 and 15 depends on state of modem clocks.

4. Byte transfer test—The attachment loads the value in the DISPLAY/FUNCTION SELECT switches of the communication indicator panel into both bytes of the attachment's storage data register. If an indicator panel is not connected to the attachment, the value is 0. The attachment then attempts to transer only the high-order byte of the storage data register to data word 5 in storage. The low-order bytes of data word 5 in storage should remain unchanged. The program should make data word 5 equal to FFFF before issuing the Start Diagnostic 1 command to verify the correct byte transfer.

Start Diagnostic 2

The Start Diagnostic 2 command is used by diagnostic programs to perform the same tests as the Start Diagnostic 1 command, with the addition of a data wrap test during test 3 (see "Start Diagnostic 1"). The format of the IDCB for this command is:



The byte count for this operation must be 12 (hex 000C) and the data address must be even; otherwise a DCB specificaiton check will be transmitted. The DCB control word should be hex 2000. For this command to operate properly, the atttachment must be disconnected from the modem and a wrap connector must be plugged into the modem end of the cable that goes from the attachment to the modem.

The bits in data word 4 have the following significance for the Start Diagnostic 2 command:

Bit	Meaning
0	DTR active
1	DSR active
2	RTS active
3	CTS active
4	NRZ transmit tested successfully*
5	NRZ receive tested successfully*
6	NRZI transmit tested successfully
7	NRZI receive tested successfully
8	Flag latch tested successfully
9	Abort latch tested successfully
10	Idle latch tested successfully
11	Buffer service latch tested successfully
12	Overrun latch tested successfully
13	Zero bit insert tested successfully
14	Transmit clock active
15	Receive clock active

*NRZ is not tested if the internal clock jumper is installed.

If the attachment supplies internal clocking, data word 4 should equal F3FF. If the modem supplies clocking, data word 4 should equal FFFC.

Device Control Block (DCB)

The DCB is an eight-word area in main storage that describes the specific parameters of the operation. Its location in storage is assigned by the program. The data in its words is loaded and changed by the program. It is fetched by the attachment, using a cycle-steal address key of 0 after successful execution of a Start I/O, Start Cycle Steal Status, Start Diagnostic 1, or Start Diagnostic 2 command.

The DCB address transferred to the attachment through the IDCB points to word 0 of the DCB and must be even. If the DCB address is odd, the attachment sets interrupt status byte bit 1 (delayed command reject) to 1 and terminates the operation with an exception interrupt request (CC2). Words 1 through 5 are ignored during a Start Cycle Steal Status, Start Diagnostic 1, or Start Diagnostic 2 command. The format of the DCB is shown below.

DCB (device control block)

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (0's)	
3	Not used (0's)	
4	Status address	
5	Chain address	
6	Byte count	
7	Data address	
	0	15

Control Word 0

Control word 0 delineates the cycle-steal operation. The format of the control word follows.

Bit 0—Chaining Flag. If this bit equals 1, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit equals 0 and the operation is successfully completed, the attachment presents a normal ending interrupt request.

Bit 1. This bit is not used and must equal 0.

Bit 2—Input Flag. This bit indicates the direction of data transfer relative to main storage. If bit 2 equals 1, data is transferred from the attachment to the processor; if bit 2 equals 0, data is transferred from the processor to the attachment. On a Start command, a receive operation is specified by this bit begin equal to 1. This bit must equal 1 for a Start Cycle Steal Status, Start Diagnostic 1, or Start Diagnotic 2 command.

Receive operation —This operation allows the attachment to begin transferring received data to the processor after synchronization is established.

The ending conditions for a receive operation are dependent on several factors:

- The setting of the chaining flag (bit 0)
- The setting of the SE bit (bit 4)
- The condition of the poll-final bit in the current frame
- Whether any errors occurred in the frame

There are two general type of errors: *suppressible* and *nonsuppressible*. Nonsuppressible errors always cause an exception interrupt request (CC2). All errors except the following four are nonsuppressible.

- Overrun
- Aborted frame
- Incorrect length record
- Block check error

The action taken when a suppressible error occurs depends on the setting of the SE bit. If the SE bit equals 0, the attachment presents an exception interrupt (CC2) and posts the cause of the error in the interrupt status byte or cycle-steal status words. If the SE bit equals 1, the attachment posts the error in the residual status block and either presents a device end interrupt request (CC3) with interrupt information byte bit 0 equal to 1, or chains to the next DCB.

Bits 0 through 7 of DCB word 1 can be used in conjunction with the receive operation to specify a time after which the attachment will begin checking the line for an idle condition. If an idle condition is detected, the attachment sets bit 5 equal to 1 in cycle-steal status word 2 and bit 0 equal to 1 in the interrupt status byte, and presents an exception interrupt request.

Bits 8 through 15 of DCB word 1 can be used in conjunction with the receive operation to specify the nonproductive receive time-out period.

Bit 3. This bit is not used and must equal 0.

Bit 4—Suppress Exception. This bit is used with receive operations only. When this bit equals 1, the attachment does not present an exception interrupt request upon detecting incorrect-length records, aborted frames, overruns, or block check errors. Instead, the attachment stores two words of information into the residual status block at the end of the operation, beginning at the address specified in the status address (DCB word 4). The first word contains the residual byte count. The second word contains the residual status flags. See the description of the status address (DCB word 4) for a description of the residual status block.

Bits 5 Through 7—Cycle-Steal Address Key. This is a three-bit key presented to the processor by the attachment during data transfers so that the processor can ascertain whether the attachment is authorized to access certain blocks of main storage.

Bit 8—Half-Rate. The attachment only recognizes this bit during the enable terminal operation—and then only if DSR is already equal to 1. This bit causes the modem to operate at one-half of its normal bit rate (if the modem is equipped to do so). If internal clocking is being used, this bit selects the 600-bps bit rate. If changing bit rates, timer 1 (bits 0 through 7 of DCB word 1) should be set to allow enough time for the modem to equalize when using modem clocking. The attachment will not change rates if timer 1 equals 0, regardless of whether internal clocking or modem clocking is being used.

Bit 9—NRZI Recording. This bit causes the attachment to use and recognize NRZI recording. When the internal clocking feature is used, NRZI is automatic and this bit is ignored.

Bit 10—Enable Terminal Operation. This bit causes the attachment to activate the DTR line. A device-end interrupt request occurs or a chaining operation begins 50 milliseconds after the modem activates DSR.

Timer 1 may be used in conjunction with this operation to limit the time the attachment waits for DSR to become active. If DSR does not become active within the specified time, the attachment resets DTR and presents an exception interrupt request with bit 0 equal to 1 in the interrupt status byte and bit 4 equal to 1 in status word 2.

For manual answer or manual call sequences, this bit must be used to turn DTR on prior to entering data mode. On leased lines, DTR can be wired on.

Programming Note: When the modem presents a ring indication, the attachment presents an attention interrupt request (CC4) and waits 50 milliseconds for the program to perform an enable terminal operation. If after this time the program has not enabled DTR, the attachment presents another attention interrupt request (provided that the ring indication is still active).

Bit 11—Disable Terminal Operation. This bit causes the attachment to deactivate the DTR line and disconnect from a switched network. Timer 1 can be used in conjunction with this operation to limit the time that the attachment allows for DSR to become deactivated. If DSR does not deactive within the specified time, an exception interrupt request occurs with bit 0 equal to 1 in the ISB and bit 4 equal to 1 in status word 2. A device-end interrupt request occurs or a chaining operation begins 200 milliseconds after the attachment detects that the DSR line has been deactivated.

Bit 12—Pad. This bit is used only with a transmit operation. If this bit equals 1, the attachment automatically transmits two pad characters prior to transmitting the first flag character of the first frame. For NRZ, the pad character is a hexadecimal 55; for NRZI, the pad character is a hexadecimal 00.

Bit 13—Secondary or Primary. This bit determines whether the attachment will operate as a primary or a secondary station. If bit 13 equals 1, the station is a primary station; if bit 13 equals 0, the station is a secondary station. On a receive operation, the attachment examines the address portion of a received frame only if the attachment is being used as a secondary station. On a transmit operation, the attachment generates its own address only when it is operating as a secondary station.

Bit 14—Transmit Operation. The attachment begins this operation by activating 'request to send' (RTS), and then waiting for CTS to become active. Upon receiving CTS, the attachment transmits the beginning flag character and starts transmitting the data. When the byte count is reduced to 0, the attachment automatically transmits the frame-check sequence and the ending flag character. One DCB causes one frame to be transmitted.

If bit 0 (the chaining flag) equals 1, the attachment fetches the next DCB and starts the next frame. If bit 15 (hold line active) equals 0 and the attachment is unable to fetch the chained-to DCB in time to cause the next frame to immediately follow the preceding frame, the attachment deactivates transmit mode and the transmission line goes into an idle condition. The next DCB is then treated as a normal transmit operation. Bit 15 can be used to eliminate the possibility of the line idling between frames.

If bit 0 and bit 15 equal 0 and the modem delay jumper is installed, the attachment automatically transmits trailing pad characters (hex FF) for 2 milliseconds after the ending flag character. The attachment then exits transmit mode and resets RTS.

Bit 15—Hold Line Active. This bit is used in conjunction with bit 14 (transmit operation). If bit 15 equals 1 when the byte count goes to 0, the attachment stays in transmit mode and transmits flag characters until another operation begins or until the time specified in timer 2 passes. If the program sets timer 2 to 0, the line is not held active.

	Conditions			Results				
	Chn bit	SE bit	P/F bit	Int CC	IIB bit 0	Chain occurs	Post resid-ual status	EOC bit *
No errors	0	0	0	3	0	no	no	n/a
	0	0	1	3	0	no	no	n/a
	0	1	0	3	0	no	yes	1
	0	1	1	3	0	no	yes	1
	1	0	0	n/a	n/a	yes	no	n/a
	1	0	1	2	**	no	no	n/a
	i	i	0	n/a	n/a	yes	yes	0
	1	1	1	3	0	no	yes	1
Suppressible errors	0	0	0	2	**	no	no	n/a
	0	0	1	2	**	no	no	n/1
	0	1	0	3	1	no	yes	1
	0	1	1	3	1	no	yes	1
	1	0	0	2	**	no	no	n/a
	1	0	1	2	**	no	no	n/a
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	1	no	yes	1

*See "Status Address" for a description of this bit.

**When condition code 2 is reported, the IIB is called the ISB and bit 0 has a different meaning. See "Interrupt Status Byte" for a description of ISB bits.

Status Address

The Status Address word is used in conjunction with bit 4 suppress exception (SE) of the control word. Bit 4 of the control word and the status address are used only on receive operations. The address this word contains is the main storage address of the residual status block. If bit 4 of the control word equals 1 and the attachment detects any of the conditions that set residual status flags, an exception-interrupt request does not occur. Instead, the attachment automatically stores two words of information into the residual status block and monitors the line, looking for an ending flag character. When the ending flag is detected, the attachment presents a normal device-end interrupt request or begins a chaining operation. The first word stored in the residual status block is the residual byte count; the second word contains the residual status flags.

Residual Status Flags

The second word of the residual status block contains the residual status flags. The bits have the following meanings.

Bit—End of Chain. This bit indicates that no further chaining will take place. This is usually a result of the attachment receiving a frame in which the poll-final bit equals 1. This bit also equals 1 if the SE bit equals 1 and the chaining flag equals 0.

Bits 1 through 7. These bits are not used and must equal 0.

Bit 8—Overrun. This condition occurs during a receive operation if the attachment is unable to transfer the contents of the storage data register to the processor before it is time to load another word of data into the storage data register.

Bit 9—Abort. This condition occurs during a receive operation if the attachment detects an abort condition. An abort condition is eight contiguous 1-bits received after the beginning of a frame.

Bit 10—Long Frame. This bit indicates that the bytes count has been reduced to zero and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame; however, any data received after the byte count reaches 0 is lost.

Bit 11—Block Check Error. The frame check sequence received is incorrect.

Bits 12 through 14. These bits are not used and must equal 0.

Bit 15—No Exception. This bit indicates either of two conditions. The first condition is that the frame is the correct length and error free. The second condition is that the attachment received an error free but short frame. To determine which condition caused this bit to be set, examine the residual byte count. If the residual byte count is not 0, a short frame was received.

Chain Address

The Chain Address word contains the storage address of the next DCB and is used when chaining is indicated (bit 0 of control word equals 1). The chain address must be even. If the address is odd, the attachment sets interrupt status byte bit 3 equal to 1 and terminates the operation.

Byte Count

This 16-bit byte-count word contains the number of bytes to be transferred during the operation specified in the current DCB control word.

Data Address

This is the address in main storage where data transfer starts.

Interrupt Information Byte

When the attachment presents an interrupt request to the processor, the interrupt information byte is used to record information that cannot be indicated to the program by the condition codes. If interrupt information bytes bit 0 equals 1 when condition code 3 is reported, the SE bit was equal to 1 for the previous receive operation and a suppressible error was suppressed. When interrupt condition code 2 or 6 is reported, the interrupt information bytes has a fixed format called the interrupt status byte.

Interrupt Status Byte

The processor detects the interrupt status byte in bits 0 through 7 of the interrupt ID word. The format of the interrupt status byte follows.

Bit 0—Device Dependent Status Available. If this bit equals 1, additional status is available through the Start Cycle Steal Status command. A discussion of this status follows in this chapter.

Bit 1—Delayed Command Reject. This bit equals 1 under the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The immediate data field of the IDCB contains an odd DCB address.

Bit 2—Incorrect Record Length This error is reported only during receive operations and only when bit 4 of the IDCB control word equals 0. Incorrect record length indicates that the attachment detected a mismatch between the byte count and the frame length or that the poll-final bit was on in the frame just received (when chaining).

A Start Cycle Steal Status command may be issued to obtain the residual byte count and the address of the last attempted data transfer.

Bit 3—DCB Specification Check. This bit equals 1 if one of the following conditions occurs:

- The DCB contains an odd address in the chaining address (word 5).
- The byte count field (DCB word 6) contains a value other than 8—applies only to Start Cycle Steal Status commands.
- The data address (DCB word 7) contains an odd address—applies only to Start Cycle Steal Status, Start Diagnostic 1 or Start Diagnostic 2 commands.
- The status address (DCB word 4) contains an odd address—applies only to receive operations when the SE bit equals 1.
- The byte count (DCB word 6) equals 0 for either a transmit operation or a receive operation.
- Bit 2 of the DCB control word is not equal to 1 for a Start Cycle Steal Status, Start Diagnostic 1, or Start Diagnostic 2 command.
- More than one operation is specified in the control word (word 0) of the DCB.
- Bit 3 of DCB word 0 equals 1.
- Bit 1 of DCB word 0 equals 1.
- The byte count field (DCB word 6) contains a value other than 12 (applies only to Start Diagnostic 1 or Start Diagnostic 2 commands).

Bit 4—Storage Data Check. This bit equals 1 during cycle-steal output (storage to attachment) operations only. It indicates that the storage location accessed during the current output cycle contains incorrect parity. The parity in main storage is not corrected. The attachment terminates the operation.

Bit 5—Invalid Storage Address. This bit equals 1 if an address presented by the attachment during a cycle steal to or from storage exceeds the storage size of the system. The attachment terminates the operation.

Bit 6—Protect Check. This bit equals 1 if the attachment attempts to store data into a storage location without the correct cycle-steal address key.

Bit 7—Interface Data Check. This bit equals 1 if a parity error is detected on the interface during a cycle-steal data transfer. The condition may be detected by the channel or the attachment. In either case, the operation is terminated and an exception interrupt request is presented to the processor.

Cycle-Steal Status Words

When a cycle-steal data transfer is terminated by an exception condition, bit 0 of the interrupt status byte may be equal to 1. If interrupt status byte bit 0 equals 1, further information regarding the cause of the exception condition may be obtained by executing a Start Cycle Steal Status command.

The format of the DCB for this command is the same as for a normal cycle-steal data transfer. The attachment ignores bits 0, 4, and 8 through 15 of the control word, and DCB words 1 through 5. The byte count must be 8, and the data address must be an even address. Four words are transferred into main storage, starting at the data address contained in DCB word 7.

Word 0

Word 0 contains the main storage address of the last attempted cycle-steal transfer. This residual address may be a data address, DCB address, or status address. The illustration below shows which type of address the residual address can be for various error conditions. Where more than one possibility is shown, the program must decide which type of address cycle-steal status word 0 contains.

Error condition	Residual address		
	DCB address	Status address	Data address
Delayed command reject	N/A	N/A	N/A
Incorrect-length record		*	X
DCB specification check	*		
Storage data check	X		X
Invalid storage address	X	X	X
Protect check	X	X	X
Interface data check	X	X	X
Overrun		X	X
Time-out	X		X
Modem interface error	X		X
Block check error	X		X
Abort		X	X
Idle or inactivity detected	X		X
Nonproductive receive	X		X

* Long frame.

** The address is that of the DCB word in error.

Residual address table

Word 1

Word 1 contains the residual byte count. This is the byte count remaining when an operation ends.

Word 2

With an exception interrupt request (CC2) and an interrupt status byte of hex 80, issuance of a Start Cycle Steal Status command is recommended to further define an error. This section describes the required error analysis and recommended action.

Status words 2 and 3 are the only words required for attachment or interface error analysis. Word 2 has the following format.

Bit 0—Overrun. During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to main storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line. Channel activity is being stressed by servicing many I/O attachments. Verify this condition does not exist and retry. If the problem persists, it is probably caused by hardware.

Bit 1—Abort. During a receive operation, this bit equals 1 if the attachment receives eight consecutive 1-bits (no 0-bits insertion) within a normal frame. This indicates that the transmitting station decided to terminate the frame prematurely. This condition is recoverable by the program. If the condition occurs frequently, contact the remote location to determine if the program is aborting frames.

Bit 2—Long Frame. The byte count decremented to 0 and no ending flag was received. If using the SE bit, adjust buffer size and bytes count to accommodate more data. If not using SE bit, contact the remote location and determine the exact byte count necessary.

Bit 3—Block Check Error. In receive operation only, the attachment sets this bit equal to 1 if the frame check sequence received by the attachment is incorrect. The probable cause is a line error. The program may request retransmission for recovery.

Note: This error may also occur during heavy channel activity.

Bit 4—Time-Out. The attachment sets this bit equal to 1 if a DSR time-out or a Disable DTR time-out occurs. This is an attachment to modem handshaking problem during an enable or disable command. Increase value of timer 1 to allow DSR to become either active or inactive (depending on operation requested).

Bit 5—Idle Detected. This error occurs if the attachment detects an idle condition after timer 1 times out during a receive operation or disable command. The attachment expected to receive a frame and the line went idle. Increase timer 1 value or notify remote location that turnaround is too slow.

Bit 6—Nonproductive Receive Time-Out. This bit indicates that a nonproductive receive time-out occurred. The remote station is not transmitting frame soon enough after being polled within the limits specified in timer 2. The condition may occur at a line break or on a long frame.

If it occurs frequently, contact remote station to resolve problem.

Bit 7—Modem Interface Error. The attachment sets this bit equal to 1 under the following conditions:

- DSR is not active when either a transmit or receive operation is initiated.
- DTR, DSR, RTS, or CTS is lost during a transmit operation.
- DTR or DSR is lost during a receive operation.
- On a transmit operation, timer 1 times out before CTS is activated by the modem.

Examine status word 3 bits 0 through 3 for an error condition. Adjust timer value, if necessary and retry.

Bits 8 Through 12. These bits are not used and will be equal to 0.

Bit 13—Business Machine Clock. This bit indicates that the internal clocking jumper is installed.

Bit 14—Generate Answer-tone Jumper Installed. This bit indicates that the answer-tone jumper is installed in the attachment. The attachment provides a 3-second answer-tone when a ring is detected.

Bit 15—Modem Delay Jumper Installed. Some modems require that RTS remain active for a time after the attachment transmits the ending flag. When this jumper is installed, the attachment maintains RTS in the active condition and transmits trailing pad characters for 2-milliseconds after sending the ending flag.

Word 3

With an exception interrupt request (CC2) and an interrupt status byte of hex 80, issuance of a Start Cycle Steal Status command is recommended to further define the error. This section describes the required error analysis and recommended action.

Status words 2 and 3 are the only words required for attachment or interface error analysis. Word 3 contains status information regarding certain attachment and modem lines. After a modem error, word 3 indicates the status of the lines at the time of the error. If a modem error did not occur, word 3 indicates the status at the time the Start Cycle Steal Status command was executed. If a modem interface error is reported, status word 2 can be examined to determine the cause.

Bit 0—Data Terminal Ready. This is an outbound signal from the attachment to the modem signifying that the remote station is ready to communicate. It expects 'data set ready' (bit 1) from the modem. DTR is set by the 'DTR enable' type DCBs.

Bit 1—Data Set Ready. This is either an inbound signal to the attachment from the modem in response to DTR (bit 0) or an indication of power on from a leased-line modem. If the DSR always equals 1, then install the DTR jumper on the attachment.

Bit 2—Request to Send. This is an outbound signal from the attachment to the modem requesting that the modem prepare for data transmission. It expects a CTS (bit 3) return from the modem. Some full-duplex modems always signal CTS as a power-on indication. In this case, the RTS jumper on the attachment should be installed.

Bit 3—Clear to Send. This is an inbound signal to the attachment from the modem indicating the communication modem is ready to transmit data.

Bit 4—Ring Indicator. This is an inbound signal to the attachment indicating the modem has detected a ring condition on the line.

Bit 5—Half-Rate Selected. This is an outbound signal from the attachment to the modem requesting the modem to operate at half its normal bit rate. If internal clocking is used, this line causes the attachment to provide clocking at 600 bps.

Bit 6—Transmit Mode Latch. This does not interface to the modem. It indicates that the attachment hardware is set up to transmit.

Bit 7. This bit is not used and must equal 0.

Bit 8 Through 15. This is the low-order byte, and contains the secondary station address.

Status After Reset

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	Action
Power-on reset	All attachment components are reset to equal 0.
System reset	All attachment components (except DTR, half-rate, and the residual address) are reset to equal 0.
Halt I/O command	All attachment components (except DTR, prepared level, I-bit, half-rate, residual address, residual byte count, and residual DCB information) are reset to 0 by this command.
Device Reset command	This command resets the same component as the Halt I/O command.

Jumpering Information

The following options can be selected by installing jumper wires on the feature card.

(A) Internal Clocking

With this jumper installed, the attachment provides clocking at 1,200 bps or 600 bps (selectable by programming).

(B) Answertone

With this jumper installed, the atacchment provides a three second answertone after the modem activates 'data set ready' in response to the attachment activating 'data terminal ready'. This jumper should not be installed if the modem provides an answertone.

(C) Request to Send

If this jumper is installed, the attachment maintains 'request to send' in an active condition. This eliminates modem "turn-around" when using a full-duplex modem. This option must always be selected when using a modem which always keeps 'clear to send' active.

(D) Data Terminal Ready

If this jumper is installed, the attachment maintains 'data terminal ready' in an active condition. This option must not be selected for switched-line operation; it must be selected when using a modem which always keeps 'data set ready' active.

(E) Modem Delay

There are some modems which may lose the last character at the end of a transmit operation. If this jumper is installed, the attachment will keep the transmit data line in a marking condition for two milliseconds after sending the last character from being lost.

(F) Secondary Station Address

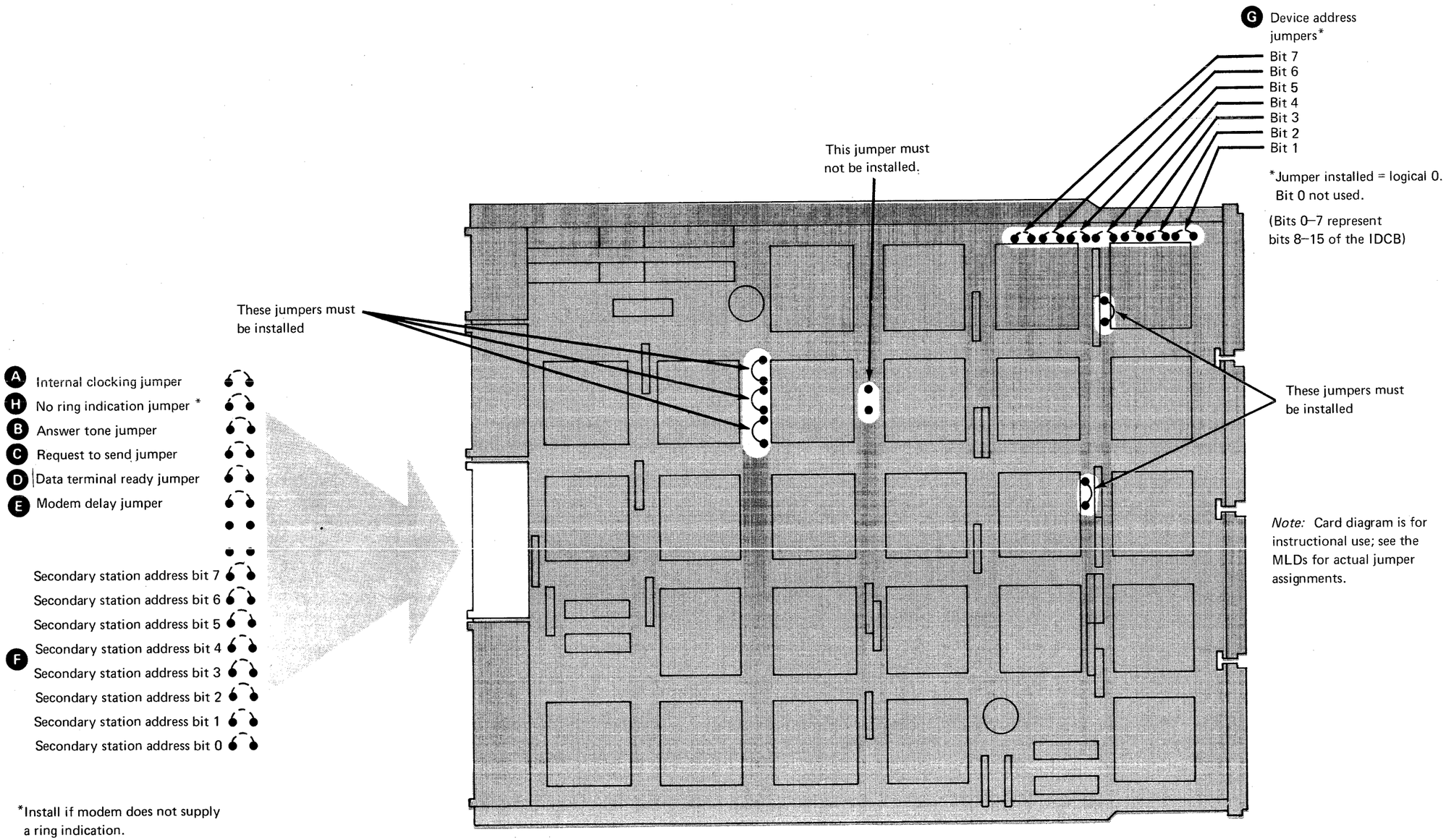
If the attachment is to be used as a secondary station, the station address is assigned by installing jumpers corresponding to bits of the address.

(G) Device Address

These jumpers select the address of the attachment on the Series/1 I/O interface.

(H) No Ring Indication

This jumper must be installed if the user has selected a modem that does not supply a ring indication to the attachment.



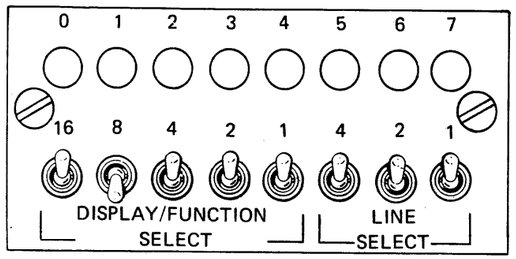
*Install if modem does not supply a ring indication.

Note: Card diagram is for instructional use; see the MLDs for actual jumper assignments.

Synchronous data link control single-line control feature

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine trouble shooting. Various conditions and registers in the attachment can be displayed. In addition, the DTR line to the modem can be reset from this panel.



LINE SELECT Switches

The three LINE-SELECT switches are used only with multiple-line communication devices. The SDLC attachment does not use these switches.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed in the indicator panel. The following is a list of switch settings and the information that is displayed in the indicator panel.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of DCB word 0 (control word)
00001	0–7	Low-order byte of DCB word 0 (control word)
00010	0–7	High-order byte of DCB word 5 (chain address)
00011	0–7	Low-order byte of DCB word 5 (chain address)
00100	0–7	High-order byte of DCB word 6 (byte count)
00101	0–7	Low-order byte of DCB word 6 (byte count)
00110	0–7	High-order byte of DCB word 7 (data address)
00111	0–7	Low-order byte of DCB word 7 (data address)
01000	0–7	Low-order byte of word 1 of the Residual Status Block
01001	0–7	Interrupt status byte (ISB)
01010	0–7	High-order byte cycle steal status word 2
01011	0–7	High-order byte of DCB word 4 (status address)
01100	0–7	Low-order byte of DCB word 4 (status address)
01101	0–7	SDLC control 0 Flag detected 1 Buffer service request 2 Idle detect 3 Abort detect 4 Overrun 5 Business machine clock selected 6 Attachment generated answer-tone 7 Modem delay selected
01110	0–7	Secondary station address
10100	0–7	Low-order byte of DCB word 1 (timer 2)
10101	0–7	High-order byte of DCB word 1 (timer 1)
11100	0–7	Lamp test
11101	0–7	Modem status 0 Data terminal ready 1 Data set ready 2 Request to send 3 Clear to send 4 Ring indicator 5 Half-rate select 6 Transmit mode 7 Receive mode
11110*		Enable for DTR reset
11111*		Reset DTR

* To reset DTR, the switches must first be set to 11110; then to 11111. This prevents resetting DTR unintentionally.

Indicator panel information—SDLC feature

Chapter 4. Feature—Programmable Multi-Line Communication

The programmable multi-line attachment controller is designed to provide control circuitry for one or two programmable 4-line adapter features. The programmable multi-line attachment contains hardware and a microprocessor to service the 4-line adapters.

Each line of the multi-line communication feature is programmable. This chapter describes this feature, which controls the serial transfer of data to and from remote terminals or host systems. The following communication characteristics apply:

- Data transmission is serial-by-bit, using either asynchronous (start-stop) or synchronous methods of character transmission.
- The feature can communicate with different terminals/systems using ASCII or any transmission code with 5, 6, 7, or 8 bits per character.
- Line control characters are defined by the program.
- The bit rate can range from 37.5 to 1,200 bps, or from 300 to 19,200 bps. Aggregate throughput is 64,000 bps (based on a 12-bit character).
- There is multipoint control; that is, the program can recognize secondary station addresses in a multipoint network.
- The feature provides answer-tone generation and break character recognition.
- Internal and external (modem) clocking capability (asynchronous only).
- Block check character reception for one or two characters is provided.
- Parity generation and checking can be specified as odd, even, or no parity.
- The stop bit length can be either 1 or 2 characters.
- Synchronous operation can have either 1 or 2 synchronization characters.
- Up to seven different change-of-direction (COD) characters can be recognized.
- Echoplex capability.
- Current loop (20 milliampere) capability or EIA RS232C or CCITT V.24 Interface.
- Expanded mode provides for the following attachment operations:
  - Continuous Receive
  - Continuous echoplex
  - Attention interrupt
  - With the following character recognition/detection
    - Two character change-of-direction (COD)
    - Two character longitudinal-redundancy-check (LRC)
    - Extended change-of-direction with block check capability.

Configurations

The programmable communication control feature has a multi-line configuration and provides control for up to eight lines. This configuration contains either two or three feature cards—two cards for one to four lines, and three cards for five to eight lines.

Note: Throughout the remainder of this chapter, the term "attachment" is used as a general term to refer to the Feature—Programmable 8-Line Communications Control and one or two Feature—Programmable 4-Line Communication Adapters.

Each line operates in a half-duplex mode (unless expanded mode is selected) and can be connected to a full-duplex modem to avoid excessive modem turnaround. If a line is connected to a full-duplex modem, the attachment still operates in half-duplex mode and the 'request to send' jumper on the feature card should be installed.

Multi-line Logic Diagram

Ⓐ I/O Channel Attachment Logic

This portion of the attachment performs the handshaking functions that are necessary for communication between the attachment and the processor I/O channel.

Ⓑ Microcontroller

The microcontroller manages everything that the attachment does. It contains a Read Only Storage (ROS) and circuitry that decodes the commands from the processor and automatically steps the attachment through every operation.

Ⓒ Modem Controls

This portion of the attachment contains the circuitry needed to control and sense conditions of the modem and communication line.

Ⓓ Line Control Logic

This logic is duplicated for each of the lines. The logic portions of the adapter card perform all of the hardware function associated with serializing and deserializing data, character formatting, bit synchronization, error detection. The buffer provides one byte of temporary storage between the microcontroller and the serializer/deserializer.

Ⓔ Bit-Rate Constant Register

During a set mode or set control operation, this register is loaded with a hexadecimal constant supplied by the program. The attachment uses this constant to determine the duration of bits and characters to be transmitted and to maintain sychronism of bits within a character while receiving.

Ⓕ Controller Interface Circuits

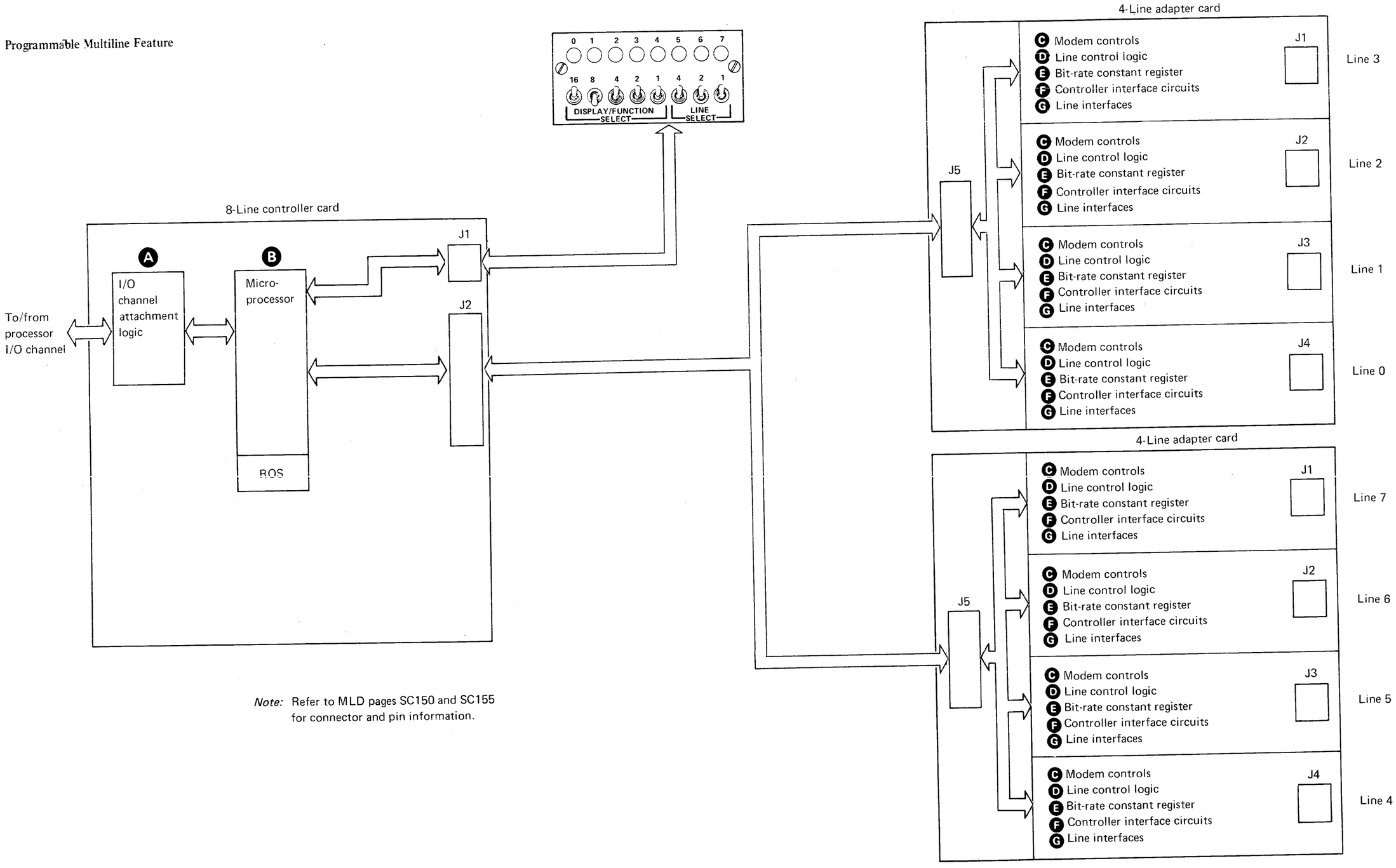
These circuits direct data to or from the individual line control circuits and bit rate generators of the adapter card. The appropriate gates and strobes to accomplish data transfer are generated by decoding specific commands from the controller card by the 9-bit I/O Address Bus Out. The particular line being addressed is determined by one of the line select signals from the controller. Data from the controller card arrives via the 8-bit Controller Data Bus Out; data is returned to the controller card by the 8-bit Data Bus In. The circuits include a priority encoder that presents transmit and receive service-request status to the controller. The prioritization algorithm presents any pending receive service request before a transmit service request and, within each classification, defines line 0 as the highest priority, line 7 as the lowest priority.

The circuits also include a 3.3 ms program-controlled timer. Physical interface to the controller is via a 20 X 2 Berg top card connector and cable.

Ⓖ Line Interfaces

The interfaces change the signals going to the modem to signals that are compatable with the modem. They also change signals coming from the modem into signals that are acceptable to the attachment.

If a line is jumpered for current loop, Data Terminal Ready (DTR) must be jumpered to Data Set Ready (DSR) and Request To Send (RTS) must be jumpered to Clear To Send (CTS). The current interface can be configured to supply current to the loop or be isolated from the Series/1 power supply.



Note: Refer to MLD pages SC150 and SC155 for connector and pin information.

Transmission Codes

In asynchronous operation, the attachment supports transmission codes with 5, 6, 7, or 8 bits per character plus parity and one or two stop bits. The adapter always adds a start bit. The attachment operates either with no parity bit or with an additional bit for even or odd parity checking.

In synchronous operation, the attachment supports any transmission code with 5, 6, 7, or 8 bits per character plus parity and one or two synchronization characters. (When two synchronization characters are used, they may be the same character or different characters.) The attachment operates either with no parity bit or with an additional bit for even or odd parity checking.

Any code that meets the preceeding requirements may be used at the programmer's discretion.

Control Characters

Each remote terminal may require different line control characters, each line of the adapter provides programmable line control characters. For example, a program could specify the same change-of-direction (COD) character in each of the seven COD positions in a set-control or set-mode device control block (DCB), which would allow 255 possible character configurations or 256 possible character configurations that could be received in an eight-bit code using the receive transparent command. The attachment recognizes up to seven different change-of-direction (COD) characters. These control characters are specified in the DCB in either the set-mode or set-control format.

Reception of any of the seven COD characters causes the attachment to terminate the current receive operation in one of the following conditions:

- Device-end interrupt request
- Exception interrupt request
- Chained operation

Note: The programmer must ensure that all COD characters (COD1 to COD7) are defined in the set-control/set-mode DCB.

These COD characters are transferred to the attachment by the DCB. The DCB format follows:

Word		
0	Control word	
1	Bit-rate constant	COD 1
2	COD 2	COD 3
3	COD 4	COD 5
4	COD 6	COD 7
5	Chain address—must be even	
6	Byte count*	
7	Data address	
	0	7 8 15

*Used for synchronous operation

Receive/Transmit Mode

In normal receive mode, when the set control or set mode operations have been used to initialize the adapter, the following conditions are in effect:

- Seven change-of-direction (COD) characters are operable. Two of the CODs can be conditioned, by command, to receive a single-character block check character.
- The receive and echoplex functions of the attachment are directly controlled by the Series/1 program using the defined start command operations. In this operating mode, the attachment receives data *only* when a DCB receive or DCB transmit with pre-receive operations are being processed.

In normal receive mode, the attachment recognizes any one of the seven characters defined in the DCB and treats them as COD characters. When any one of the defined characters is received, the attachment presents a device-end interrupt request or begins a DCB command chaining operation except when an incorrect length record is detected. All received control characters are placed in storage.

In expanded mode (note that more information about expanded mode is described under "Data Reception" later in this chapter), the two character change-of-direction causes the adapter to interpret the change-of-direction table in conjunction with a delineating character to determine an ending sequence. The user-specified delineating character is the first character received and the second character will be any of the seven programmable characters in the change-of-direction table. If two delineating characters are received consecutively followed by a character in the change-of-direction table, reception continues until a single delineating character followed by a COD is detected. Typically, the delineating character would be a DLE or ESC character.

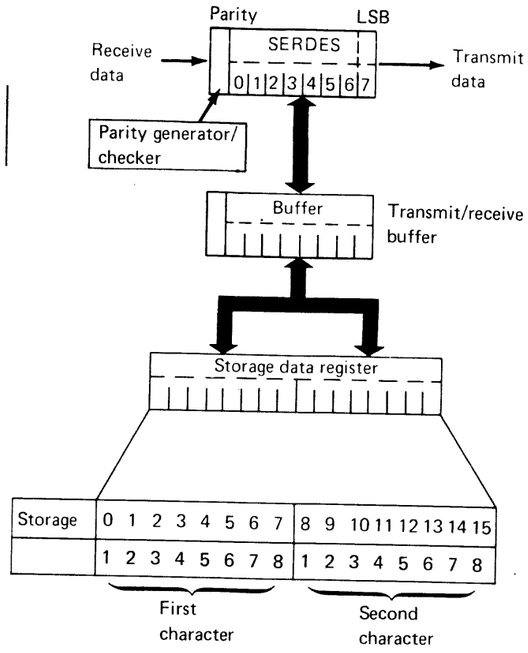
In transmit mode, there is no control character comparison. All ending conditions must be controlled by byte count. When the byte count is reduced to 0, a device-end interrupt request or chaining occurs.

Data Flow

Valid data is placed in storage as it is received. If parity checking is requested, the data is checked for odd or even parity, and then the parity bit is removed from the data character. Data that is received with incorrect parity is placed in storage as hex 00. The data may be placed in storage exactly as it is received by placing the DISPLAY/FUNCTION SELECT switches on the communication indicator panel (if installed) to 11110. This applies to any and all lines.

In expanded mode, the inhibit zero insertion affects the adapter error procedure when a bad parity character is received (assumes parity check enabled). Normal adapter operation is to replace the bad parity character with a binary zero character. When this mode is enabled, the adapter will not "zero" the character but will provide the character as it was received (incorrect data parity) with the parity bit removed.

Data is transmitted as it comes from storage; therefore, data must be organized in the exact bit configuration required by the code being used and in the sequence in which it is to be transmitted. Illustrated below is the attachment's storage data register and the bits in storage.



Note: The programmable attachment transmits by sending out the low-order bit of the byte first. The received characters are stored in the same manner; that is, the first bit received is the low-order bit of the byte. If the character is less than 8 bits, it must be right justified. If the data address (DCB word 7) is odd, only one character is moved in or out of storage on the first data transfer.

Line Error Checking

The attachment checks for line errors through programmed parity checking. The DCB in set-mode format specifies even, odd, or no parity. If even or odd parity is specified, the parity bit is generated by the adapter in transmit mode and checked by the adapter in receive mode.

Note: If the set-control DCB is executed, no parity is specified.

Asynchronous operation requires one or two stop bits (as defined in the set-mode/set control DCB) be transmitted with each character. The attachment checks each received character for only one stop bit.

Timers

The *attachment* has two programmable timers (timer 1 and timer 2). Each timer is controlled by a 16-bit word in the DCB. Both timer values are reduced independently at a rate of 3.33 milliseconds per count. The maximum time that either timer can count is 218.2 seconds. The timers use a count (hex FFFF to 0000) supplied by the program. When the count reaches 0000, the attachment begins or terminates an operation. The timers are used with various operations defined in the control word of the DCB; these operations are listed below.

Timer 1

- Receive time-out (see "Receive with Time-Out" under "Operations" later in this chapter)
- Generate answer-tone or break
- Transmit delay
  - Slows down turnaround (pre-transmit delay)
  - Allows last character to exit modem before deactivating 'request to send' (post-transmit delay)
- 'Carrier detect' time-out

Timer 2

- Program delay
- 'Clear to send' time-out
- 'Data set ready' time-out
- 'Ring indicator' time-out
- 'Data terminal ready' disable delay

For detailed information about the use of the timers with particular operations, see "Device Control Block (DCB)" later in this chapter.

Commands

The program initiates all communication operations by issuing an Operate I/O instruction.

The Operate I/O instruction points to the immediate device control block (IDCB), which contains one of the following commands:

- Prepare
- Device Reset
- Write Data
- Halt I/O
- Read ID
- Start
- Start Cycle Steal Status
- Start Diagnostic 1
- Start Diagnostic 2
- Start Control

It is the programmer's responsibility to ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

The programmer should exercise care in modifying the DCB words prior to an interrupt request that signifies the end of the operation. The attachment might not have fetched all of the DCB because it is slower than the Series/1 processor.

On this attachment, the base device address must have the following:

- The device addresses must be sequential.
- The first device address must have bits 13, 14, and 15 equal to 0.

See the illustration below.

	Device addresses							
Line	*Base device address**					*Line address*		
0	X	X	X	X	X	0	0	0
1	X	X	X	X	X	0	0	1
2	X	X	X	X	X	0	1	0
3	X	X	X	X	X	0	1	1
4	X	X	X	X	X	1	0	0
5	X	X	X	X	X	1	0	1
6	X	X	X	X	X	1	1	0
7	X	X	X	X	X	1	1	1
bit→	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*

*Base device address (indicated by X's) is set by jumpers on the controller card.

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The data word contains the priority level and I-bit. The IDCB for the Prepare command has the following format.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 0 0 0 0 0	X X X X X X X X
0 *7*	*8* *15*
60	00–FF

Immediate data field		
0's	Level	I
16 *26*	*27* *30*	*31*

Level. This four-bit field specifies the priority interrupt level assigned to the device. Bits 27 through 30 indicate priority levels.

Example:

Bits 27–30	**Level**
0000	0
0001	1
0010	2
0011	3

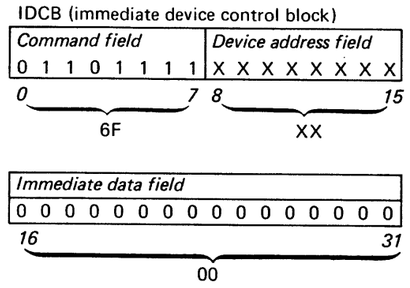
A Prepare command issued to any device on this attachment gives all of the devices in the attachment the same priority interrupt level. The I-bit information applies only to the specific device addressed.

I-Bit. This bit determines whether the device is allowed to present interrupt requests. An I-bit value of 1 allows requests; a value of 0 prevents requests.

The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset during a system reset or a power-on reset, or is changed by the successful execution of another Prepare command issued to the attachment. The Prepare command causes an interrupt request to be presented if one was pending on the device and the I-bit now equals 1. On a multi-line attachment, the device returns an operate I/O condition code 1 to this command if it has an interrupt request pending, and the I-bit in the IDCB equals 0.

Device Reset

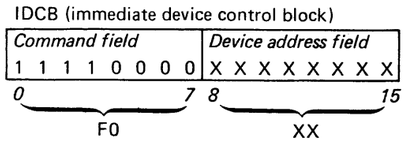
The Device Reset command resets the addressed device and clears any pending interrupt requests (except controller end). The following are not affected: the line control characters, bit rate constant, and number of data bits specified by the DCB; the DTR line; and the controller-end interrupt. (See "Status After Resets" later in this chapter.) The IDCB for the Device Reset command has the following format:



A Device Reset command issued to the attachment causes the attachment to become "busy" while the reset functions are being performed. A 'controller busy' (CC6) is reported if a Start command follows a Device Reset or another Start command too closely. When the attachment is capable of accepting another command, a controller-end interrupt request (CC0) is presented by the base address of the multi-line attachment (line 0) at which time the program should reissue the Start command.

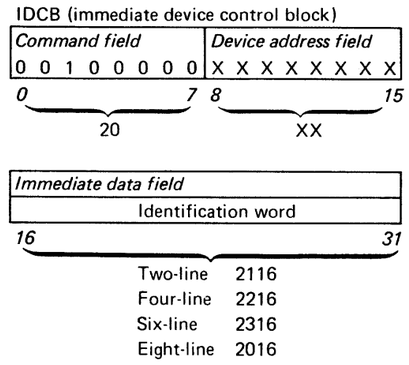
Halt I/O

The Halt I/O command halts all I/O activity on the I/O channel. Any pending interrupt requests, including controller end (CC0), are cleared. Except for the fact that the I-bits and priority level do not change, this instruction performs the same function as a system reset. The format of the IDCB for this command follows:



Read ID

The Read ID command puts the attachment's identification (ID) word into the IDCB's immediate data field. The ID word contains physical information about the attachment that can be used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming. The format of the IDCB for this command follows:

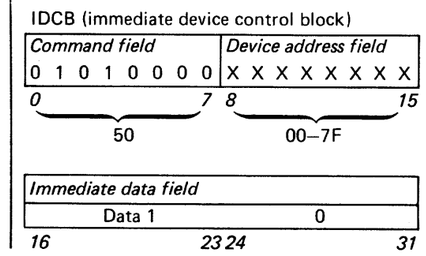


Note: If the controller card has jumpers installed for addresses that are not valid, the controller responds to commands as though the 4-line adapter card was present; therefore, the ID of the controller should match the number of attachment lines present to prevent errors. For example, an ID of 2016 or 2316 defines a controller with two 4-line attachments. If there is only one 4-line attachment present, the ID is 2216 or 2116.

Write Data

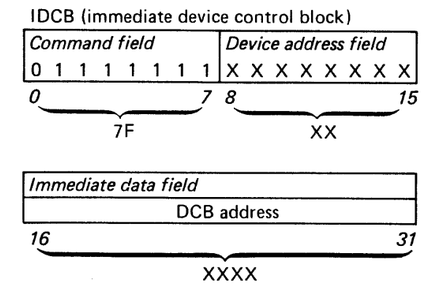
This command is provided as a way to handle character-by-character operation in the expanded operating mode to provide programmed echoplex. DTR, DSR, RTS, CTS must be active when this command is issued. This command is similar to a "Transmit End" Start command except there is no DCB associated with this command. Data is transferred to the attachment in the IDCB. Chaining, pre- and post-transmit delays, and modem control operations are not supported. The addressed device will be "Device Busy" until a Device End or Exception Interrupt is presented notifying the program it is capable of accepting more data.

The Write Data IDCB has the following format:



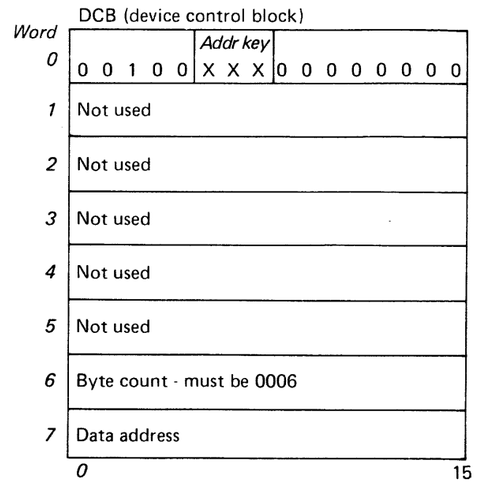
Start Cycle Steal Status

The Start Cycle Steal Status command initiates a cycle-steal operation in the addressed device to retrieve status information about the previous cycle-steal operation. The format of the IDCB for this command follows:



This command does not allow a chaining operation. The byte count in word 6 must be equal to 6 and the data address (word 7) must be on a word boundary (bit 15 equals 0) or an exception interrupt (CC2) occurs with DCB bit 3 (specification check) in the interrupt status byte equal to 1.

See "Cycle Steal Status Words" later in this chapter for a description of the information transferred to storage by this command.



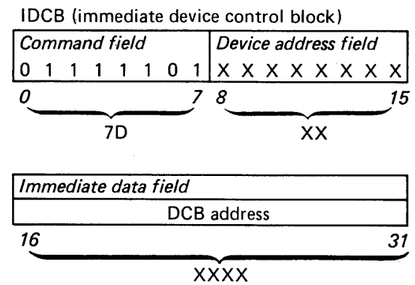
Format of the DCB for a Start Cycle Steal Status command

Diagnostic Commands

The Diagnostic Commands commands are used by diagnostic programs to check for correct operation of the attachment.

Start Diagnostic 1

The format of the IDCB for this command follows:



When a Start Diagnostic 1 command is issued to the attachment, the following sequence of operations takes place:

1. The DCB is fetched.
2. A test of the attachment registers is executed. When one or more registers identifies an error, the attachment enters a wait state and no interrupt request is presented.
3. A read-only-storage (ROS) check sum is calculated and the results are stored at the data address specified in the DCB.

Note: When the attachment recognizes Start Diagnostic 1, it dedicates itself to executing that command and no operations should be pending at other addresses controlled by this attachment.

DCB (device control block)

Word	
0	Control word
1	Not used
2	Timer 1
3	Timer 2
4	Not used
5	Chain address
6	Byte count
7	Data address

0 15

Format of the DCB for a Start command

Descriptions of the Start Diagnostic 1 DCB words follow:

Word 0

Bits 0 and 1. These bits must equal 0.

Bit 2. This bit must equal 1.

Bits 3 and 4. These bits must equal 0.

Bits 5–7. These bits are the storage protect key.

Bits 8–15. These bits should equal 0 to preclude future code obsolescence.

Words 1 through 5

These words are not used.

Word 6—Byte Count

This word must contain a count of 12 (hexadecimal C). Otherwise, the attachment terminates the operation with an exception-interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

Word 7—Data Address

This word must contain an even address. Otherwise, the attachment terminates the operation with an exception-interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

This word specifies the starting address for the attachment to cycle steal the following words into storage:

- Word 1—Stored check sum of ROS 1
- Word 2—Calculated check sum of ROS 1 (inverted)
- Word 3—Stored check sum of ROS 2
- Word 4—Calculated check sum of ROS 2 (inverted)
- Word 5—Stored check sum of ROS 3
- Word 6—Calculated check sum of ROS 3 (inverted)

Start Diagnostic 2

The Start Diagnostic 2 command can be issued to any device without disturbing the normal function of other devices.

The IDCB for this command is shown below:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 0	X X X X X X X X
0 — *7*	*8* — *15*
7E	00–7F

Immediate data field
DCB address
16 — *31*
XXXX

When a Start Diagnostic 2 command is issued to the attachment, various operations as defined in the DCB are executed. These operations are terminated with a device-end interrupt request after the attachment cycle steals the Start Diagnostic 2 words into storage. The operations and words are described below.

This command provides both external and internal wrap capability. The external wrap requires an external wrap connector; the internal wrap does not affect the transmit or receive lines.

Note: Before a Start Diagnostic 2 command can be issued, a Set Mode or Set Control command must be issued; otherwise, results are be unpredictable. If external clocking is available, it may be used with this command. Internal clocks not exceeding 300 bps may be used for diagnostic purposes in synchronous mode. DTR and RTS are reset following the completion of this command (if not jumpered on).

DCB (device control block)

Word																
0	0	0	1	0	0	*Addr key* X	X	X	0	0	0	0	0	0	0	0
1	Not used															
2	Not used															
3	Not used															
4	Not used															
5	Not used															
6	Byte count - must be 0006															
7	Data address															

0 15

Format of the DCB for a Start Cycle Steal Status command

Control Word 0

The bit descriptions for this word are given below.

Bits 0 and 1. These bits must equal 0.

Bit 2. This bit must equal 1.

Bits 3 and 4. These bits must equal 0.

Bits 5–7. These bits are the storage protect key.

Bit 8. If the '-data-terminal-ready' (DTR) jumper is not installed and this bit equals 1, DTR is deactivated for the length of the command.

Bit 9. If the 'request-to-send' (RTS) jumper is not installed and this bit equals 1, the RTS is deactivated for the length of the command.

Bit 10. The adapter activates echoplex when this bit equals 1. The echoplex latch is reset after Start Diagnostic 2 is executed.

Bit 11. This bit is not used and must equal 0.

Bit 12. The attachment places a "space" condition on the transmit line when this bit equals 1. If odd parity is selected, bit 12 (parity error) of diagnostic word 1 equals 1. If asynchronous mode is selected, bit 9 (break detect) and bit 10 (framing error) of the returned diagnostic data word equal 1. Diagnostic data word 0 is 0000 for 5-, 6-, 7-, and 8-bit character lengths.

Bit 13. This bit is not used and must equal 0.

Bit 14. An internal wrap test is performed when this bit equals 1. The 'transmit data' line to the modem remains at a mark level and no data is transmitted off the card. The 'receive data' line is not examined and does not affect the test.

Bit 15. This bit is not used and must equal 0.

Words 1 Through 5

These words are not used.

Word 6—Byte Count

This word must contain a count of 6. Otherwise, the attachment terminates the operation with an exception-interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

Word 7—Data Address

This word must contain an even address. Otherwise, the attachment terminates the operation with an exception-interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

This word specifies the starting address for the attachment to cycle steal the diagnostic data words into storage.

Diagnostic Data Words

The diagnostic data words are used in conjunction with the maintenance package.

Word 0

This word is defined by the character length of the selected transmission code as shown in the chart that follows.

Character length (bits)	Word 0 description	
	Start Diagnostic 2 DCB word 0, bit 12, equals 0	Start Diagnostic 2 DCB word 0, bit 12, equals 1
5	150A	0000
6	152A	0000
7	552A	0000
8	55AA	0000

Word 1

The bit descriptions for this word are given below.

Bit 0—Data Terminal Ready. This bit equals 1 if 'data terminal ready' (DTR) jumper is installed or if bit 8 of the DCB control word 0 equals 0. DTR is reset following the command execution.

Bit 1—Data Set Ready. This bit is set as follows:

- Equal to 1 if external wrap connector is used
- Equal to 1 if a leased-line modem is used and powered on.
- Equal to 1 if the IBM Current Interface Cable is installed and the current interface is wired
- Equal to 0 or 1 if a switched-line modem is used
- Equal to 0 if no cable is installed
- Equal to 0 if bit 8 of DCB control word 0 equals 1

Bit 2—Request To Send. This bit equals 1 if the 'request-to-send' (RTS) jumper is installed or if bit 9 of DCB control word 0 equals 0.

Bit 3—Clear To Send. This bit equals 0 or 1 for the same conditions as bit 1 (data set ready), as described previously.

Bit 4—External Clocks. This bit equals 1 if the bit-rate constant in the DCB for the Set Control or Set Mode command equals 00.

Bit 5—Carrier Detect. This bit equals 1 if the 'carrier detect' jumper is installed or the external wrap connector is used and control word 0 bit 9 equals 0. This bit can equal 0 or 1 if connected to a modem.

Bit 6—Echoplex. This bit equals 1 if bit 10 of control word 0 equals 1.

Bit 7—Receive Data Lead. This bit can equal 0 or 1.

Bit 8—Ring. This bit equals 0.

Bit 9—Sync/Break Detect. This bit equals 1 for all operations in synchronous mode and those in which bit 12 of DCB control word 0 equals 1 in asynchronous mode.

Bit 10—Framing Error. This bit equals 1 if bit 12 of DCB control word 0 equals 1 in asynchronous mode.

Bit 11—Overrun. This bit equals 0.

Bit 12—Parity Error. This bit equals 1 if bit 12 of DCB control word 0 equals 1 and odd parity is specified in set mode.

Bit 13—Transmit Empty. This bit equals 1.

Bit 14—Receive Ready. This bit equals 1.

Bit 15—Transmit Ready. This bit equals 1.

Word 2

This word is used to test the attachment's ability to cycle steal bytes of data into storage. Bits 0 through 7 are the bit rate constant and the only data byte to be placed in storage. If this byte transfer fails, hex FF is placed in bits 8 through 15; if the transfer is successful, bits 8 through 15 are unchanged.

Note: Before executing a Start Diagnostic 2 command, bits 8 through 15 of word 2 in storage should be equal too a value other than hex FF so that the program can determine if the byte transfer failed. After Start Diagnostic 2 is completed, DTR is reset unless it is wired "on."

Start Control

The Start Control command is used for the following operations:

- Write controller storage
- Read controller storage
- Start trace
- Trace dump
- Set expanded mode

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	1	1	1	0	0	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
7C								XX							

Immediate data field
DCB address
16 *31*

Issuing this command to the controller can cause the attachment to become inoperable, if certain conditions/parameters are not adhered to. If this happens, the attachment can only be restored to operation by turning power off, and then on again.

The data address (DCB word 7) must always be even. Otherwise, the attachment terminates the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

Write Controller Storage. The DCB format for this operation follows.

Word	DCB (device control block)
0	Control word—0X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address—not used
6	Byte count—must be 432 (hex 1B0)
7	Data address—must be even

This operation begins if DCB word 0 bit 2 equals 0 and the byte count is 432. Starting at the address specified in DCB word 7, the attachment cycle steals 432 bytes of data from processor storage into storage associated with the attachment. A device-end interrupt request is presented when the cycle stealing is completed. The 432 bytes of data transferred is used by IBM Engineering to make functional changes in the attachment.

If DCB word 0 bit 2 equals 0 and the byte count is not 432, the attachment terminates the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

Read Controller Storage. The DCB format for this operation follows.

Word	DCB (device control block)
0	Control word—2X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address—not used
6	Byte count—must be 1024 (hex 0400)
7	Data address—must be even

This operation begins if DCB word 0 bit 2 equals 1 and the byte count is 1024. Starting at the address specified in DCB word 7, the attachment cycle steals 1024 bytes of data from the attachment into storage. A device-end interrupt request is presented when the cycle stealing is completed.

If DCB word 0 bit 2 equals 1 and the byte count is not 1024, the attachment terminates the operation with an exception interrupt request and the DCB specification check bit in the interrupt status byte equals 1.

Start Trace. The DCB format for this operation follows.

Word	DCB (device control block)
0	Control word—0000
1	Not used
2	Bit-dependent
3	Not used
4	Not used
5	Chain address—not used
6	Byte count—must be 0
7	Data address—not used

This operation begins if DCB word 0 bit 2 equals 0 and the byte count is 0. An array is generated in attachment storage to provide the following information about the last seven DCBs issued to a single address (only one address can be traced at a time):

- The DCB control words
- The DCB addresses
- The interrupt status byte and interrupt condition codes
- The cycle-steal status word 1s information

Note: The field containing the interrupt status byte and interrupt condition code for the last DCB is followed by 0000; the field containing status word 1 for the last DCB is followed by 0000.

Data shifts through this array and is traced for predefined error conditions. These conditions are defined in DCB word 2 by having one or several bits equal to 1. The bits and their meanings follow:

Bit	Meaning
0	Overrun
1	Time-out
2	Log all status-word-1 errors (all other bits must be off)
3	DCB reject
4	Not used
5	Parity error
6	Break detected
7	Stop-bit error
8	Not used
9	Modem-interface error
10–11	Not used
12	Error during pre-receive/adapter buffer full
13–14	Not used
15	Adapter buffer not empty

After an error condition is detected, the trace operation stops and information about the last seven DCBs is available to the operator when the trace dump operation is performed. The trace operation also stops when DCB word 2 equals 0 or when any interrupt status byte except A0 or 80 is presented.

Trace Dump. The DCB format for this operation follows.

Word	DCB (device control block)
0	Control word—2X00
1	Not used
2	Not used
3	Not used
4	Not used
5	Chain address—must be even
6	Byte count—must be 64 (hex 0040)
7	Data address—must be even

This operation begins if DCB word 0 equals 2X00 and the byte count is 64. Data for error analysis is dumped from an array in storage to the data address specified in DCB word 7 and is made available to the operator through an output device.

This data is the following information about the last seven DCBs issued to a single address:

- The DCB control words
- The DCB addresses
- The interrupt status byte and interrupt condition codes
- The status word 1 information

This data also includes status words 0 and 2 for the last DCB if the trace operation stops due to an error detected.

Note: The field containing the interrupt status byte and interrupt condition codes for the last DCB is followed by FFFF; the field containing status word 1 for the last DCB is followed by FFFF.

The interrupt status byte and interrupt condition codes are presented in the following format:

Interrupt status byte	Reset indicator	Condition code

The condition codes and their meanings follow:

Condition code	Meaning
00	No interrupt returned
02	Exception interrupt returned
03	Device-end interrupt returned
F0	Operation terminated by reset
F2	Exception interrupt returned followed by reset
F3	Device-end interrupt returned followed by reset

The trace dump storage array appears in storage as follows:

Control word 0	DCB 5 6 7 0 1 2 3 4	byte 01
DCB address	DCB 5 6 7 0 1 2 3 4	
ISB/CC	DCB 5 6 7 0 1 2 3 4	
Status word 1	DCB 5 6 7 0 1 2 3 4	byte 64

Trace dump storage array

The trace dump printout is as follows:

	DCB5	DCB6	DCB7	DCB0	DCB1	DCB2	DCB3	DCB4
Control word 0			2004	SW0				
DCB address			XXXX	SW2				
ISB/CC			8002	FFFF				
Status word 1			8000	FFFF				

DCBs without errors — Failing DCB — DCBs without errors

- SW0 – Status word 0 for failing DCB
- SW2 – Status word 2 for failing DCB
- FFFF – Indicates that trace has stopped on preset error condition (*Note:* 0000 indicates that trace is still running)

Set Expanded Mode. To enable and disable the expanded operating mode the "Start Control" command is used.

The IDCB has the following format:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
7C	XX

Immediate data field
DCB address
16 ... 31

DCB Format

Word	0	0 0 0 1
	1	Not used
	2	Trace option
	3	X field Y field
	4	Not used
	5	Not used
	6	Must be zero
	7	Not used

X-field = Delineating Character used in Two Character Change of Direction Mode. Bit 10 of the Y field must be on to activate the mode.

Y-field = Bit 08 = not used; must be 0
Bit 09 = two character LRC mode
Bit 10 = two character change of direction mode
Bit 11 = inhibit zero insert mode
Bit 12 = 4 CODs with LRC mode
Bit 13 = continuous echoplex mode
Bit 14 = attention interrupt mode
Bit 15 = continuous receive mode

Note: See "Operations" for a description of the modes listed in the Y field.

These modes are stored in a bit significant manner, a "0" disables the mode and a "1" enables the mode.

These extensions are applicable on a per line basis within the Feature-Programmable Multi-line adapter. The various adapter modes of operation can be used together, however, certain combinations of modes such as continuous echoplex without continuous receive or attention interrupt without continuous receive are illogical.

(Device Reset, System Reset, Halt I/O will reset the expanded mode of operation.)

Start

The Start command initiates a cycle-steal operation in the addressed device. The format of the IDCB for the Start command follows:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
70	XX

Immediate data field
DCB address
16 ... *31*
XXXX

Device Control Block (DCB)

Cycle-steal commands require a DCB. The DCB is an eight-word area in storage that describes the specific parameters of the cycle-steal operation. Its storage address is assigned by the program and must be even. When this address is transferred to the attachment, it points to word 0. If the DCB address is odd, the attachment sets interrupt status byte bit 1 (delayed command reject) equal to 1 and terminates the operation with an exception interrupt request. The general format for a DCB Start command follows.

DCB (device control block)

Word	
0	Control word
1	Not used
2	Timer 1
3	Program-controlled interrupt/timer 2
4	Not used
5	Chain address—must be even
6	Byte count
7	Data address

The formats for the individual start commands (Start, Start Cycle Steal Status, Start Diagnostic, and Start Control) are described under "Commands," earlier in this chapter.

The general format for a DCB specifying asynchronous set-mode or set-control operation follows:

DCB (device control block)

Word		
0	Control word	
1	Bit-rate constant	Line-control character
2	Line-control character	Line-control character
3	Line-control character	Line-control character
4	Line-control character	Line-control character
5	Chain address	
6	Byte count	
7	Data address	

0 7 8 15

The general format for a DCB specifying synchronous set-mode operation (synchronous mode only) follows:

DCB (device control block)

Word		
0	Control word	
1	00	Line-control character
2	Line-control character	Line-control character
3	Line-control character	Line-control character
4	Line control character	Line-control character
5	Chain address	
6	Quantity of synchronization characters	
7	Address of synchronization characters	

0 7 8 15

A description of the eight DCB words follows.

Word 0—Control Word

This 16-bit word prescribes the operation to be performed.

Bit 0—Chaining Flag. If this bit equals 1, the attachment fetches the next DCB in the chain after completing the current DCB operation if there are no exception interrupt conditions.

Bit 1—Program-Controlled Interrupt (PCI) Request. If this bit equals 1, the attachment presents a PCI request at the completion of the DCB fetch and places DCB word 3 bits 8 through 15 in the interrupt information byte. Data transfers associated with the DCB can begin if the PCI request is pending. If the PCI request is pending when the attachment encounters the next interrupt-causing condition, the PCI condition is discarded by the device and is replaced with the new interrupt condition. This bit is recognized only during transmit and receive operations. If it equals 1 in any other type of operation, bit 3 of the interrupt status byte (DCB specification check) is set equal to 1 and the operation terminates with an exception interrupt request.

Bit 2—Input Flag. This bit indicates to the attachment the direction of data transfer. It equals 1 when data is transferred from the attachment to the processor; it equals 0 when data is transferred from the processor to the attachment.

Bits 3 and 4. These bits are not used and must equal 0; otherwise, bit 3 of the interrupt status byte (DCB specification bit) is set equal to 1 and the operation terminates with an exception interrupt request.

Bits 5 Through 7—Cycle-Steal Address Key. This key is presented by the attachment during data transfers. It is used to ascertain storage access authorization.

Bits 8 through 15. When bit 8 equals 1, the operation specified in bits 9 through 15 of the DCB control word is performed in set mode. The attachment decodes bits 9 through 15 to determine which of the following operations is to be performed.

Bits 8	9	10	11	12	13	14	15	Operation
0	0	0	0	0	0	0	0	Transmit
0	0	0	0	0	0	0	1	Transmit end
0	0	0	1	0	0	0	1	Transmit end with pre-receive
0	0	0	0	0	0	1	0	Transmit allow break
0	0	0	0	0	0	1	1	Transmit end allow break
0	0	0	1	0	0	1	1	Transmit end allow break with pre-receive
0	0	0	0	0	1	0	0	Receive
0	0	0	0	0	1	0	1	Receive with time-out
0	0	0	1	0	1	0	0	Receive with block check character
0	0	0	1	0	1	0	1	Receive with time-out and block check character
0	0	1	0	0	1	0	0	Receive with echoplex
0	0	1	0	0	1	0	1	Receive time-out and echoplex
0	0	1	1	0	1	0	0	Receive with echoplex and block check character
0	0	1	1	0	1	0	1	Receive with echoplex, time-out, and block check character
0	1	0	0	0	1	0	0	Receive transparent
0	1	0	0	0	1	0	1	Receive transparent with time-out
0	1	1	0	0	1	0	0	Receive transparent with echoplex
0	1	1	0	0	1	0	1	Receive transparent with echoplex and time-out
0	1	1	1	0	1	0	0	Read adapter buffer
0	0	0	0	0	1	1	0	Ring monitor
0	0	0	0	0	1	1	1	Ring monitor with time-out
0	0	0	0	1	0	0	0	DTR enable
0	0	0	0	1	0	0	1	DTR enable with time-out
0	0	0	0	1	0	1	0	DTR enable with answer-tone
0	0	0	0	1	0	1	1	DTR enable with time-out and answer-tone
0	0	0	0	1	1	0	0	DTR disable
0	0	0	1	1	1	0	1	Set control
0	0	0	0	1	1	1	0	Program delay
0	0	0	0	1	1	1	1	Reset
0	0	0	0	1	1	0	1	DCB specification check
1	X	X	X	X	X	X	X	Set mode

Data Transmission

Transmit.

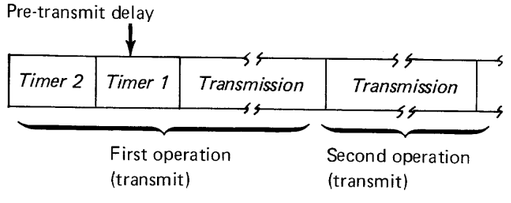
The transmit operation is used when another transmit-type operation follows immediately.

The attachment begins this operation by sending 'request to send' (RTS) to the modem and starting timer 2. The attachment then waits for 'clear to send' (CTS) from the modem. When the attachment receives 'clear to send,' it resets timer 2, starts timer 1, and waits for timer 1 to time out. When timer 1 times out, the attachment begins cycle stealing data from storage and transmitting the data to the remote station. The delay provided by timer 1, in this case, is called "pre-transmit delay"; its purpose is to allow the receiving station enough time to set up to receive data and to allow time for the modem and communication lines to stabilize.

Timer 2 should be set to a value high enough to allow turnaround on a half-duplex teleprocessing link. If timer 2 is not correctly defined by the program, an exception-interrupt request (CC2) occurs. If the interrupt status byte bit 0 equals 1, status word 1 of the attachment has a modem interface error (bit 9 equals 1) indicating that RTS was active and that CTS was not returned by the modem within the time limits of timer 2.

The attachment presents a device-end interrupt request or begins a DCB command chaining operation when the byte count goes to 0. The attachment stays in transmit mode and leaves RTS active at the end of this operation. This allows continuity from one transmit-type operation to another without sending another RTS and waiting for CTS.

When chaining a series of transmit-type operations, timer 2 is used only in the first operation; timer 1 provides a pre-transmit delay in the first operation only.

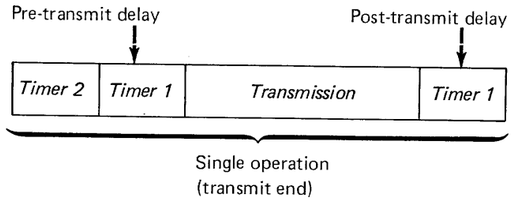


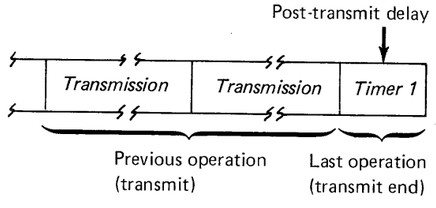
Timer 1 should be set for a pre-transmit delay of approximately 9 milliseconds when the receiving station is a program-controlled device and is directly connected or is connected through a full-duplex modem. Timers 1 and 2 should always be activated to prevent excessive turnaround and noise.

Note: Line control characters are not examined. In synchronous operation, leading pad characters and synchronization characters are not inserted by the attachment except in two situations. When data is not placed into the data stream as quickly as the attachment expects it, the attachment may insert synchronization characters into the data stream as follows:

- Between characters within a block of data
- Between blocks of data within the data stream when the blocks result from chained transmit operations

Transmit End. This operation is used to transmit the last block of data in a chain of transmit-type operations or when only one block is being transmitted. An example of the use of this operation is shown below.





This operation is the same as the transmit operation, except that the attachment exits transmit mode and starts timer 1 after the last character is sent to the modem. When timer 1 times out, the attachment resets its RTS (if RTS is *not* wired on). This delay allows the last character to leave the modem before the attachment resets 'request to send.' The timer-1 delay at the end of this operation is called "post-transmit delay." Note that timer 1 is used twice in this operation (pre-transmit and post-transmit delays) if this operation is not part of two or more transmit-type operations.

Transmit End With Pre-receive. This operation is the same as the transmit-end operation, except that there is no post-transmit delay and, when pre-receive time starts, incoming data is saved during the chaining process. Pre-receive time starts after the last character has been transmitted and a post-transmit delay is not used. Data can be received immediately; however, this operation must be chained to a receive-type command or an exception interrupt will occur. Interrupt status byte bit 3 (DCB specification check) is set equal to 1. To ensure data integrity during line turnaround, a direct connection or a four-wire interface must be used.

Transmit Allow Break. This operation is the same as the transmit operation, except that it allows the receiving station to stop the transmission. To do this, the receiving station "breaks" the line by driving its transmit line to a "space" condition for at least 150 milliseconds plus two character times. If the attachment detects this condition, it presents an exception interrupt request with bit 0 of the interrupt status byte equal to 1 and transmit mode is reset. Status word 1 bit 6 equals 1 to indicate the break.

Transmit End Allow Break. This operation is the same as the transmit-end operation, except that this operation allows the receiving station to stop the transmission. To do this, the receiving station "breaks" the line for at least 150 milliseconds plus two character times. If the attachment detects this condition, it resets transmit mode and RTS and presents an exception interrupt request with bit 0 of the interrupt status byte equal to 1. The attachment does not reset RTS if the jumper is installed.

Transmit End Allow Break With Pre-Receive. This operation is the same as the transmit-end with pre-receive operation and transmit-end-allow-break operation combined. The same restrictions stated under "Transmit End With Pre-Receive" apply to this command.

Data Reception

Normal receive mode (selected by using the set control or set mode operations) provides the following:

- ACCA compatibility
- Half-duplex operation
- 7 change-of-direction (COD) characters, 1 block check character, and 2 of the CODs can be conditioned by command to receive a single block check character
- Command-driven reception, with echoplex capabilities.

In the normal receive mode, the attachment receives data *only* when a DCB receive or DCB transmit with pre-receive operation is being processed. When no receive DCB or transmit DCB is being processed, the attachment assumes that no data is present to be received. This assumption is correct when dealing with a half-duplex device. When a device operates in full-duplex mode, data can be present almost anytime.

Expanded Mode

To expand the attachment capabilities, additional operations are defined using the Set Expand Mode command. (See "Set Expanded Mode" in the commands section of this chapter.)

Expanded mode provides the following operations:

- Continuous receive mode
- Attention interrupt mode
- Continuous echoplex mode
- Extended character recognition/ detection consisting of the following:
  - Two character change-of-direction
  - Inhibit zero insert mode
  - Two character block check mode
  - 4 CODs with LRC mode

Continuous Receive Mode. In the normal receive mode, the adapter receives data *only* when a DCB Receive or DCB transmit with pre-receive command is being processed by the adapter. When no receive DCB is in process or a transmit DCB is being processed, the attachment assumes that no data is present to be received. This assumption is correct when dealing with a half-duplex device. When a device operates in full-duplex mode, however, data can be present at almost anytime due to operator action or device operation. To handle this situation, a new mode of operation has been defined: continuous receive mode.

1. If a receive DCB is in process, the character will be handled in normal fashion; that is, it is compared with the (COD) character table and the receive either continued or terminated based on normal operation.
2. If no DCB is active or a non-receive DCB is active, the adapter stores the character within the adapter's 15 byte buffer (one character per byte) and awaits the processing of the next DCB receive. The adapter continues to buffer these characters on a first-in-first-out (FIFO) basis. When the next receive DCB is processed by the adapter, the buffer contents are processed as part of the operation just as if the buffer data was being received from the line. It will be transparent to the program whether the data from the receive came from the buffer or the actual line. If the adapter receives more characters than it can hold in the line buffer, the next DCB will terminate with a unique error condition of first-in-first-out (FIFO) full (status word 1, bit 12).

Note that the COD (change-of-direction) processing is simply an alert condition for lines operating in asynchronous mode (TTY); that is, the reception of the COD character does not necessarily mean a true end-of-message condition, but could simply be a special character within a message. In synchronous mode operations, after a COD has been received,' the attachment resets synchronization and begins the resynchronization process again. Set Mode Set Control, or DCB Reset commands clear the adapter of any stored input data. DTR, DSR, and DCD must be active before entering this mode of operation.

Attention Interrupt Mode. Attention interrupt mode is an operating mode used only in conjunction with continuous receive mode. When activated in the adapter, attention interrupt mode causes received characters to be processed by the adapter concurrent with other adapter operations. In this mode, when a character is received and a Read DCB is not in process, it is presented to the Series/1 using an attention interrupt with the received character in the IIB (interrupt information byte). The following special situations are dependent on the Attention Interrupt Mode: Attention interrupts will only be presented if a Transmit Type command or no command is active.

1. If a transmit allow break command is active and a character is received which is in the COD table, the adapter will terminate the Transmit Allow Break command (after processing the current transmit character) and present interrupt status with the residual address of the last character transmitted available to the system. Note if a COD character is received prior to the transmit allow break command, and is interrupt pending in the channel the transmit command will not be stopped.
2. If an error occurs, an attention with exception (CC=6) will be presented with an ISB equal to 80; and no further attention interrupts are presented until a read adapter buffer operation followed by a read cycle steal status is processed by the adapter. Attention interrupts resume if the first-in-first-out (FIFO) buffer is empty (Bit 15 of status word 1) following a Start Cycle Steal Status command. If a transmit-type command is terminated by the error, a Start Cycle Steal Status command should be issued, then a Read Adapter Buffer command followed by another Start Cycle Steal Status command. The first Start Cycle Steal Status command is used to obtain the residual address of the transmitted data. The read Adapter buffer operation is used to clear out all previously held data and the second Start Cycle Steal Status command will reenable attention interrupts. If the adapters buffer is not empty, and bit 15 of status word 1 is on, another read adapter buffer operation is required followed by a Start Cycle Steal Status command.

Continous Echoplex Mode. Continuous echoplex provides the capability to use the echoplex function with continuous receive in a half-duplex operation between the adapter and the Series/1. During read with echoplex operation, characters received from the terminal are automatically transmitted back to the terminal for display. When continuous receive mode is in operation and continuous echoplex is specified, any characters received without a pending read operation are saved and echoed to the terminal. During a transmit operation any characters received will *not* be held in the line buffer and *not* echoed to the terminal. Continuous echoplex is intended for situations where the device requires echoplex but no CPU logic is needed to process the data characters for echo.

Expanded Character Recognition/Detection

Two Character Change-of-Direction Mode. Two character change-of-direction causes the adapter to interpret the change-of-direction table in conjunction with a delineating character to determine an ending sequence. The user-specified delineating character is the first character received and the second character will be any of the seven programmable characters in the change-of-direction table. If two delineating characters are received consecutively followed by a character in the change-of-direction table, reception continues until a single delineating character followed by a COD is detected. Typically, the delineating character would be a DLE or ESC character.

Inhibit Zero Insert Mode. Inhibit zero insert mode, when enabled, causes the attachment to place a received character with incorrect parity into storage as it was received. If inhibit zero insert mode is not enabled, the attachment places 0's into storage when characters are received with incorrect parity.

Two Character Block Check Mode. Two character block check causes the adapter to process the Read with block check command such that two block check (LRC) characters following a COD are placed into the user's buffer within Series/1 storage. Similar to the conventional mode of LRC reception (single character) no check is made of the data received as a block check.

Four CODs with LRC Mode. 4 CODs with LRC causes the adapter to receive one additional character following COD recognition utilizing four specifiable COD characters. When a Receive with Block Check command is issued and COD 4, 5, 6, or 7 is received and interpreted from the change-of-direction table, one additional character is placed in Series/1 storage following the COD character.

Normal Receive.

This operation allows the attachment to begin cycle stealing data into storage when the attachment begins receiving valid data (the correct start bit or synchronization characters must be recognized). If the 'carrier detect' jumper is not installed, 'carrier detect' from the modem must be active before the attachment can begin transferring data to storage. When any of the defined characters are received, the attachment presents an interrupt request, as shown in the chart:

Receive Termination Chart

Input conditions				Receive termination		
Error condition*	Chain flag	Byte count = 0	COD received	CC	ISB/IIB	Comment
No	No	No	Yes	2	A0	
No	No	Yes	No	2	20	
No	No	Yes	Yes	3	00	
No	Yes	No	Yes	2	A0	No chain
No	Yes	Yes	No	–	–	Chain to next DCB
No	Yes	Yes	Yes	–	–	Chain to next DCB
Yes	No	No	Yes	2	A0	
Yes	No	Yes	No	2	A0	
Yes	No	Yes	Yes	2	80	
Yes	Yes	No	Yes	2	A0	No chain
Yes	Yes	Yes	No	2	A0	No chain
Yes	Yes	Yes	Yes	2	80	No chain

* Parity error exception interrupt occurs at the completion of the operation for the present DCB. All other exception interrupts are presented upon detection.

If the attachment detects a parity error while receiving data, it places hex 00 into storage instead of the incorrect character and continues receiving data until the ending condition occurs (COD received). The attachment then presents an exception interrupt request. If the indicator panel is connected to the attachment and the DISPLAY/FUNCTION SELECT switches are set to 11110, the attachment places the incorrect character into storage and continues receiving data.

A device-end interrupt request is presented when a COD character is recognized. After character synchronization is established, all characters, including any synchronization characters, are placed into storage.

When the attachment recognizes any receive operation, and the timer is not used, and the 'carrier detect' jumper is not installed, the attachment waits for an indefinite length of time for 'carrier detect' to become active before beginning the receive operation.

When the attachment recognizes any receive operation, and the timer is used, and the 'carrier detect' jumper is not installed, the attachment waits for the length of time specified in timer 1 for 'carrier detect' to become active before beginning the receive operation. If 'carrier detect' does not become active within the specified time, the attachment terminates the operation with an exception interrupt request and word 1 bit 9 (modem interface error) in the start cycle-steal status operation's DCB equals 1.

When the 'carrier detect' jumper is installed, a 'carrier detect' signal is returned to the attachment and the signal from the modem is not checked.

When DCB word 0 bit 0 (chaining flag) equals 0, the byte count reaches 0, and no COD is received:

- An exception interrupt request is presented
- Interrupt status byte bit 2 (incorrect length record) equals 1

Receive With Time-Out. This operation is the same as the receive operation, except that the attachment uses timer 1 to limit the time it will wait for the first character. It also limits the time that the attachment waits between characters. Failure to receive a character within this time results in an exception interrupt request with interrupt status byte bit 0 equal to 1 and status word 1 bit 1 (time-out) equal to 1. If the 'carrier detect' jumper is not installed, the attachment waits the length of time specified by timer 1 for 'carrier detect' to become active. If 'carrier detect' does not become active within the specified time, the attachment presents an exception interrupt request and posts modem interface error (bit 9) in cycle steal status word 1.

Receive With Block Check Character. This operation is the same as the receive operation except that the attachment waits for one character after detecting either the COD6 or COD7 character specified in the DCB format of a Set Control or Set Mode command. The block check character is not generated or checked by the adapter but is placed in storage. Parity, if set, is checked on the block check character.

Receive With Time-Out and Block Check Character. This operation is the same as the receive-with-block-check-character operation except that timer 1 is used to limit the time that the attachment waits for 'carrier detect' to become active, to receive the first character, or between characters. If the attachment does not receive a character or a block check character after a COD6 or COD7 character, an exception interrupt request is presented with interrupt status byte bit 0 equal to 1.

Receive With Echoplex. This operation is the same as the receive operation except that all data transmitted from the sending station is returned to the sending station on the sending station's receive line. A full-duplex interface is required.

Receive With Time-Out and Echoplex. This operation is the same as the receive-with-echoplex operation except that timer 1 is used to limit the time that the attachment waits to receive a character, the time between characters, and the time waiting for 'carrier detect' to become active. If the attachment does not receive a character or 'carrier detect' within the specified time, an exception interrupt request is presented with interrupt status byte bit 0 equal to 1.

Receive With Block Check Character and Echoplex. This operation is the same as the receive-with-block-check-character operation except that data is immediately transmitted back to the sending station.

Receive With Echoplex, Time-Out, and Block Check Character. This operation is the same as the receive-with-time-out-and-block-check-character operation except that data is immediately transmitted back to the sending station.

Receive Transparent. This operation is the same as receive, except that the COD characters are not recognized and this operation terminates when the byte count reaches 0.

Receive Transparent With Time-Out. This operation is the same as the receive-transparent operation except that timer 1 limits one of the following:

- The time that the attachment waits for 'carrier detect' to become active or to receive a character
- The time between characters when more than one character is being received

Receive Transparent With Echoplex. This operation is the same as the receive-transparent operation except that all data transmitted from the sending station returns to the sending station on the sending station's receive line.

Receive Transparent With Echoplex and Time-Out. This operation is the same as the receive-transparent-with-echoplex operation except that timer 1 limits one of the following:

- The time that the attachment waits for 'carrier detect' to become active or to receive a character
- The time between characters when more than one character is being received

Notes:

1. When 'carrier detect' jumper is not installed and the attachment recognizes any receive operation without timer, the attachment, before going into receive mode, waits for an indefinite period of time for 'carrier detect' signal from the modem to become active.
2. When 'carrier detect' jumper is not installed and the attachment recognizes any receive with time-out command, before going into receive mode, the attachment waits for the 'carrier detect' signal from the modem to become active within the period of time specified in timer 1. (DCB word 2). If at the end of timer 1 value, the 'carrier detect' signal from the modem has not become active then the attachment terminates the operation with an exception interrupt and modem interface error bit (bit 9) set in cycle steal status word two.

3. When the 'carrier detect' jumper is installed, 'carrier detect' is permanently returned to the attachment and the signal from the modem is not checked.

Read Adapter Buffer. This operation is used with the expanded mode commands. When executed, any data saved in the adapter buffer will be cycle-stolen into Series/1 storage. This command must be issued if an interrupt condition code of 6 is presented or if bit 15 of word 1 of the Start Cycle Steal Status command is active. The first byte placed into storage represents a byte count of the characters received error free but not reported by way of "CC4". Following the byte count are the receive characters. Up to 16 (hexadecimal 10) bytes may be placed into storage.

Line Control

Ring Monitor. This operation allows the attachment to monitor the 'ring indicator' line from the modem. Unless this is a chained operation, the attachment presents a device-end interrupt request to the processor when 'ring indicator' is active for more than 100 milliseconds.

Ring Monitor With Time-Out. This operation is the same as the ring-monitor operation except that timer 2 limits the length of time that the attachment waits for a ring condition. If a time-out occurs, an exception interrupt request is presented, interrupt status byte bit 0 equals 1, and bit 1 (time-out) is set in cycle steal status word 1.

DTR Enable. This operation sends 'data terminal ready' to the modem; the modem responds by activating 'data set ready.' Unless this is a chained operation, the attachment presents an interrupt request to the processor when 'data set ready' becomes active.

To ensure the validity of 'data set ready,' the minimum execution time of this operation is 100 milliseconds.

Note: 'Data terminal ready' is normally wired on for leased lines.

DTR Enable With Time-Out. This operation is the same as the DTR-enable operation except that timer 2 limits the length of time the attachment waits for 'data set ready.' If a time-out occurs before the DSR becomes active DTR is disabled, an exception interrupt request is presented to the processor, the interrupt status byte bit 0 equals 1, and bit 9 (modem interface error) is set in cycle steal status word 1. To ensure the validity of 'data set ready,' the minimum execution time of this operation is 100 milliseconds.

DTR Enable With Answer-tone. This operation is the same as the DTR-enable operation except that an answer-tone or space is placed on the transmission line for the period specified in timer 1 when 'data set ready' is activated. After the time-out occurs, an interrupt request is presented to the processor or chaining begins. To ensure the validity of 'data set ready,' the minimum execution time of this operation is 100 milliseconds. Timer 1 should be set to approximately 3 seconds (refer to the modem manual for an exact setting).

DTR Enable With Answer-tone and Time-Out. This operation is the same as the DTR-enable-with-answer-tone operation except that timer 2 limits the length of time the attachment waits for 'data set ready.' If a time-out occurs before the DSR becomes active, DTR is disabled, an exception interrupt request is presented to the processor, interrupt status byte bit 0 equals 1, and status word 1, bit 9 (modem interface error) is set in cycle steal status word 1. To ensure the validity of 'data set ready,' the minimum execution time of this operation is 100 milliseconds.

DTR Disable. This operation is used in a switched network to deactivate 'data terminal ready' and disconnect the attachment from the network. Timer 2, which should be set for at least 1 second, starts when 'data terminal ready' is deactivated. Unless this is a chained operation, the attachment presents a device-end interrupt request to the processor when a time-out occurs. If 'data terminal ready' or 'data set ready' is not deactivated within the time specified by timer 2, an exception interrupt is presented to the processor, interrupt status byte bit 0 equals 1 and cycle steal status word 1 bit 9 equals 1. 'Data terminal ready' cannot be deactivated if the jumper is installed.

Set Control. This operation provides compatibility with the Asynchronous Communications (ACC) features, and it places the attachment in asynchronous mode and COD characters are defined in the DCB for a Set Control command. The data length is eight bits, there is no parity specified, and there are two stop bits. The above conditions are effective until a new 'set control' or 'set-mode' is activated, or a power-on reset occurs.

Note: The attachment's mode of operation is designated by either 'set control' or 'set mode operation.'

Program Delay. This operation starts timer 2. Unless this is a chained operation, the attachment presents a device-end interrupt request to the processor when a time-out occurs.

Reset. This operation resets all information in an addressed device except Prepare command information, 'data terminal ready,' set control information, or set mode information. Unless this is a chained operation, a device-end interrupt request is presented to the processor when all of the designated information is reset.

Set Mode. This operation places the attachment in either asynchronous or synchronous operation. The format of bits 8 through 15 for both modes are shown here:

Bit	Value	Meaning	
8	1	Set mode	
9	0	Asynchronous operation	
	1	Synchronous operation	
10, 11	00	5 bits per character	
	01	6 bits per character	
	10	7 bits per character	
	11	8 bits per character	
		Asynchronous	**Synchronous**
12, 13	00	Invalid	SYN-SYN is recognized/ generated
	01	One stop bit	Invalid
	10	Reserved	SYN is recognized/ generated
	11	Two stop bits	Invalid
14	0	Odd parity	
	1	Even parity	
15	0	No parity	
	1	Parity	

Note: Any invalid configuration causes an exception interrupt request with ISB bit 3 (DCB specification check) equal to 1.

In asynchronous mode, external clocks must be provided when DCB word 1 bits 0 through 7 (bit-rate constant) equal 00.

In synchronous mode, external clocks must be provided and DCB word 1 bits 0 through 7 (bit-rate constant) must equal 00. The number of synchronization characters specified by bits 12 and 13 must equal the byte count in the DCB of a set-mode (synchronous) operation and must reside at an even-byte boundary; otherwise, a DCB specified check is presented to the processor. The location of the synchronization characters must be specified by DCB word 7 (data address). If two synchronization characters are used, they can be different characters.

Bit Rate

Any line on the adapter can be programmed for data transmission at a rate between 37.5 and 19,200 bps. (See limitations below.) If the rate is between 37.5 and 1200 bps, install the low-range jumper; if the rate is between 300 and 19,200 bps, install the high-range jumper. Specify the exact bit rate (bit-rate constant) in the program. The constant is the high-order byte of DCB word 1 and is stored in the attachment during a set control/set mode operation.

The programmable eight-line controller is limited to the following:

- A maximum aggregate throughput rate of 64,000 bps (at 12 bits per character), 56,000 if doing a trace operation
- A maximum of one four-line adapter if the bit rate of 19,200 bps is selected for any line synchronous operation
- When continuous receive mode is selected with buffered full-duplex devices, the bit rate used to determine controller loading should be twice the stated bit rate of the line.

Example:

Determine the bit-rate constant for 150 bps.

$$\text{Constant} = \frac{9600}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

$$\frac{9600}{150} - 1 = 63 \text{ (decimal)} = 3F \text{ (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the set control/set mode operation would be 3F.

The bit-rate constant for high-range operation is determined by the following formula:

$$\text{Constant} = \frac{76800}{\text{bps}} - 1$$

Round off to the nearest whole number and convert to hexadecimal.

Example:

Determine the bit-rate constant for 1,200 bps (with high-speed jumper installed).

$$\frac{76800}{1200} - 1 = 63 \text{ (decimal)} = 3F \text{ (hexadecimal)}$$

Therefore, the hex constant supplied by the program in conjunction with the set control/set mode operation would be 3F.

There are some bit rates in the ranges shown previously that are incompatible with the attachment. The difference between the bit rate of the attachment and the bit rate of the attached terminal must not exceed 1.5 percent. To determine the difference (in percent) use one of the following methods. An example follows method 2.

Method 1 For attachments that have the low-speed jumper installed.

Step 1. Divide the terminal's bit rate into 9,600 and round the answer to the nearest whole number.

Step 2. Multiply the above answer by 0.000104166. This gives the attachment's bit time.

Step 3. Determine the terminal's bit time by taking the reciprocal of the terminal's bit rate.

Step 4. Divide the smaller of the bit times by the larger of the bit times. Subtract the answer from 1. Multiply this answer by 100. This gives the percentage of difference between the bit rate of the terminal and the actual bit rate of the attachment for a given constant.

Method 2 For attachments that have the high-speed jumper installed. Compute the difference in the same manner as method 1, making the following substitutions:

Step 1. Substitute the number 76,800 for 9,600.

Step 2. Substitute the number 0.0000130208 for 0.000104166.

Example:

Determine the difference between the bit rate of the attachment and the bit rate of a terminal that operates at 134.5 bps.

Step 1 $\frac{9600}{134.5} = 71.37 = 71$

Step 2
$$\begin{array}{r} 0.000104166 \\ \times \quad\quad 71 \\ \hline 0.007395786 \end{array} = \text{attachment's bit-time}$$

Step 3 $\frac{1}{134.5} = 0.007434944 = \text{terminal's bit-time}$

Step 4 $\left(1 - \frac{0.007395786}{0.007434944}\right) 100 = 0.53\%$

The aggregate throughput rate can be determined by performing the following calculation:

$$\left| \sum_{x=0}^{7} \left[\frac{12B_x}{C_x} \right] \right| \text{ or the summation of}$$

$$\left| \left[\frac{12 \cdot B_0}{C_0}\right] + \left[\frac{12 \cdot B_1}{C_1}\right] + \left[\frac{12 \cdot B_2}{C_2}\right] + \left[\frac{12 \cdot B_3}{C_3}\right] + \left[\frac{12 \cdot B_4}{C_4}\right] + \left[\frac{12 \cdot B_5}{C_5}\right] + \left[\frac{12 \cdot B_6}{C_6}\right] + \left[\frac{12 \cdot B_7}{C_7}\right] \right|$$

Where:
B=bit rate (see note)
C=character length of line x (character length is equal to the sum of all bits in the character: start, data, parity, and stop)

For example, in a configuration, five lines with the following characteristics are desired:

- Two asynchronous lines at 9600 bps, each having a start bit, five data bits, one parity bit, and one stop bit
- Two asynchronous lines at 2400 bps, each having a start bit, eight data bits, no parity, and two stop bits
- One synchronous line at 9600 bps, having eight data bits and one parity bit

$$\left[\frac{12\ (9600)}{8}\right] + \left[\frac{12\ (9600)}{8}\right] + \left[\frac{12\ (2400)}{11}\right] + \left[\frac{12\ (2400)}{11}\right] + \left[\frac{12\ (9600)}{9}\right] = 46{,}836$$

Because 46,836 bps is less than 64,000 bps, the above configuration is valid.

Note: The *actual* bit rate multiplied by 2 should be used for buffered terminals using continuous receive mode.

Chain Address

The chain address word (DCB word 5) contains the storage address of the next DCB when chaining is indicated. The address must be even; otherwise, the attachment sets interrupt status byte bit 3 equal to 1 and terminates the operation with an exception interrupt request.

Byte Count

The 16-bit byte-count word (DCB word 6) contains an unsigned integer that is the byte count for this data transfer.

Data Address

The data address word (DCB word 7) contains the storage address of the first data transfer for the operation being performed.

Interrupt Status Byte

When the attachment presents an exception interrupt request (along with an interrupt condition code of 2 or 6) to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by the condition codes. The attachment presents the interrupt status byte to the processor as bits 0 through 7 of the interrupt ID word.

The bits and their meanings follow.

Bit 0—Device-Dependent Status Available. If this bit equals 1, additional status is available by using the Start Cycle Steal Status command (described later in this chapter). This bit may be set equal to 1 in conjunction with bit 2 (incorrect length record).

Bit 1—Delayed Command Reject. This bit is set to 1 for any of the following conditions:

- The IDCB contains an odd DCB address.
- The IDCB contains an invalid function modifier.
- The IDCB is for a command that performs a write operation.

Bit 2—Incorrect Length Record. This bit can be reported during all receive operations except the receive-transparent operation. If ISB bit 0 equals 0 and bit 2 equals 1, the byte count has gone to 0 and the attachment has not received a change of direction (COD) character. If ISB bits 0 and 2 both equal 1, the attachment received a COD character and the byte count was not 0.

Bit 3—DCB Specification Check. This bit equals 1 under any of the following conditions:

- The DCB contains an odd chaining address (DCB word 5).
- The byte count (DCB word 6) contains a value other than 6 for a Start Cycle Steal Status command.
- The data address (DCB word 7) contains an odd address for the following: a Start Cycle Steal Status, Start Control, or Start Diagnostic command (the chaining bit must equal 0 for these commands).
- The byte count for a transmit or receive operation is 0.
- Bit 2 of the DCB control word (word 0) is not set appropriately for the operation.
- The byte count of a Start Diagnostic 1 command is not equal to 12.
- The byte count of a Start Diagnostic 2 command is not equal to 6.
- Bit 2 of the control word for a Start Control command equals 1 and the byte count is not equal to hex 0400 or hex 0040.
- Bit 2 of the control word for a Start Control command equals 0 and the byte count is not equal to hex 01B0 or hex 0000.
- The PCI bit is on for other than transmit- or receive-type operations.

Bit 4—Storage Data Check. This bit equals 1 during cycle-steal output operations only. It indicates that the storage location accessed during the current output cycle contained incorrect parity. The parity in main storage is not corrected. The attachment terminates the operation.

Bit 5—Invalid Storage Address. This bit equals 1 if the storage address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation.

Bit 6—Protect Check. This bit equals 1 if the attachment attempted to access a storage location without the correct cycle-steal address key. The attachment terminates the operation.

Bit 7—Interface Data Check. This bit equals 1 if a parity error was detected on the Series/1 interface during a cycle-steal data transfer. The condition can be detected by the processor I/O channel or the attachment. In either case, the operation is terminated and an exception interrupt request is presented to the processor.

0	1	2	3	4	5	6	7
Device-dependent status available	Delayed command reject	Incorrect-length record	DCB specification check	Storage data check	Invalid storage address	Protect check	Interface data check

Interrupt Information Byte (IIB)

When the attachment presents an interrupt, the IIB is used to record additional information. If the condition code equals 3 (CC3) the IIB=0000. If the condition code equals 4 (CC4) and expanded mode is being used, the IIB equals the character received.

Cycle-Steal Status Words

Three words of status information are available by using the Start Cycle Steal Status command. This information is available regardless of the setting of ISB bit 0.

Three words (six bytes) of status information are transferred into main storage starting at the data address contained in DCB word 7. Status words 1 and 2 are the only words required for analysis of attachment or terminal link errors.

DCB (device control block)

Word			
0	*Ctrl word* 0 0 1 0 0	*Addr key* X X X	0 0 0 0 0 0 0 0
1	Not used		
2	Not used		
3	Not used		
4	Not used		
5	Not used		
6	Byte count—must be 0006		
7	Data address—must be even		

Word 0

Word 0 contains the main storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or DCB address. The value of the residual address must be examined to determine if it is a data address or a DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Word 1

Bit 0—Overrun. During a receive operation, this bit equals 1 if the attachment is not able to transfer data to storage before the storage data register is needed for new data.

Bit 1—Time-Out. This bit equals 1 if:

- During a receive-with-time-out operation, no data is received within the limits established by timer 1.
- During a ring-enable-with-time-out operation, 'ring indicator' is not received from the modem within the limits of timer 2.

For error recovery, increase the timer 2 value during a ring enable with time-out. If a ring signal was not received within the limits of timer 2, increase the value of timer 2 and retry.

Bit 2. This bit is not used.

Bit 3—DCB Reject. This bit equals 1 under either of the following conditions:

- A transmit-type operation is attempted when the attachment is in receive mode.
- A receive-type operation is attempted when the attachment is in transmit mode.

Bit 4. This bit is not used.

Bit 5—VRC Error. The parity of a received character was incorrect. The exception interrupt request is presented at the end of the message.

A special character (hex 00) is placed in main storage when any incorrect data is detected. If communications indicator panel is installed and the DISPLAY/FUNCTION SELECT switches are set to 11110, the received character is placed in storage without any modifications to the character. For expanded mode, inhibit zero insertion affects the adapter error procedure when a bad parity character is received (assumes parity check enabled). Normal adapter operation is to replace the bad parity character with a binary 0 character. When this mode is enabled, the adapter does not "zero" the character, but provides the character as it was received (incorrect data parity). The interrupt request does not occur until a COD is detected, or the byte count is reduced to 0 and the chain bit equals 0.

For error recovery, the program should transmit a negative acknowledgement and retry.

Bit 6—Break. During a transmit-allow-break, transmit-end-allow-break or transmit-end-allow-break-with-pre-receive operation, a "break" condition was detected. The attachment terminates the operation and resets transmit mode and 'request to send' (if RTS is not wired "on"). For error recovery, the program can then issue either a receive command or continue transmitting. During continuous receive mode, 'break detect' will not be presented.

Bit 7—Stop-Bit Error. A character was received with a stop bit missing. The exception interrupt request occurs as soon as the error is detected.

For error recovery, the program should transmit a negative acknowledgement and retry.

Bit 8. This bit is not used.

Bit 9—Modem Interface Error. Conditions that cause this error are:

- DSR is not activated from the modem within the predetermined time after a DTR enable with time-out operation begins.
- CTS is not activated from the modem within the time specified by timer 2 during any transmit or DTR enable with answer-tone operation.
- DTR or DSR are not active at the beginning of a transmit or a receive operation.
- CTS is active for more than 1 second while RTS is inactive at the beginning of a transmit operation. (If CTS is permanently returned, RTS must be wired on.)
- DTR or DSR is lost during a transmit or receive operation.
- RTS or CTS is lost during a transmit or answer-tone operation.
- 'Carrier detect' becomes inactive during a receive operation if the 'carrier detect' jumper is not installed.
- 'Carrier detect' is not received during a receive with time-out operation if the 'carrier detect' jumper is not installed.

If a modem interface error is reported, for error recovery, the programmer should examine status word 2 and retry. If DTR equals 1, the attachment expects DSR to equal 1; if RTS equals 1, the attachment expects CTS to equal 1.

Cycle-steal status words

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Word 0	Residual address															
Word 1	Overrun	Time-out	Not used	DCB reject	Not used	VRC error	Break	Stop-bit error	Not used	Modem interface error			Note 1			Note 2
Word 2	Data terminal ready	Data set ready	Request to send	Clear to send	External clocks	Carrier detect	Echo plex	Receive data	Indicator panel switch settings							

Notes:

1. Error during pre-receive/adapter buffer full.
2. Adapter buffer not empty.

Bits 10 and 11. These bits are not used.

Bit 12—Error During Pre-Receive, Adapter Buffer Full. This bit equals 1 when an error is detected during an operation with pre-receive. This bit equals 1 if operating in expanded mode with continuous receive and the adapter buffer is full.

Bits 13 Through 14. These bits are not used and must be 0.

Bit 15. This bit reflects the status of the adapter buffer. If this bit equals 1, a read adapter buffer operation followed by another Start Cycle Steal Status command must be issued to reset any error conditions and enable attention interrupts.

Note: More than one error may be reported in status word 1. An example is a VRC error with an overrun, time-out, modem interface error, or error during pre-receive.

Word 2

Bit 0—Data Terminal Ready. This bit is a signal from the attachment to the modem that indicates whether DTR was active at the time the Start Cycle Steal Status command was issued. It expects a DSR (bit 1) response from the modem.

DTR is set by the 'DTR enable' type DCBs.

Bit 1—Data Set Ready. This bit is a signal to the attachment from the modem. It is either in response to DTR (bit 0) or is a power-on indication from a leased-line modem.

If DSR is always equal to 1, install the DTR jumper on the attachment.

Bit 2—Request to Send. This bit is an outbound signal from the attachment to the modem when the attachment wishes to transmit. Expect a CTS (bit 3) returned from the modem.

Some full-duplex modems always signal CTS as a power-on indication; in this case, the RTS jumper on the attachment must be installed.

Bit 3—Clear to Send. This bit is an inbound signal to the attachment from the modem in response to RTS (bit 2) signal.

Bit 4—External Clocks. This bit equals 1 if the bit-rate constant in the DCB for a set mode/set control operation equals 00, indicating modem clocking is being used.

Bit 5—Carrier Detect. This bit equals 0 or 1 when the attachment is connected to a modem and the 'carrier detect' jumper is installed.

Bit 6—Echoplex. This bit equals 1 if the attachment is in echoplex mode.

Bit 7—Receive Data Lead. This bit may equal 0 or 1.

Bits 8–15. These bits designate the communications indicator panel DISPLAY/FUNCTION SELECT switch settings.

Status After Resets

There are several methods of resetting some or all of the circuits in the attachment. The resets and their effects are shown in the chart:

	Power-on reset	System reset	Halt I/O	Device reset	DCB command reset	Indicator panel reset
DTR with jumper	On	On	On	On	On	On
DTR without jumper	Off	--	--	--	--	Off
RTS with jumper	On	On	On	On	On	On
RTS without jumper	Off	Off	Off	Off	Off	Off
Interrupt level	Off	Off	--	--	--	--
I-bit	Off	Off	--	--	--	--
Set control	*	--	--	--	--	--
Pending interrupts	Off	Off	Off	Off	--	--
Residual address	**	--	--	--	--	--
Echoplex	Off	Off	Off	Off	Off	--
Trace	Off	***	***	***	--	--
Expanded mode	Off	Off	Off	Off	--	--

*Defaults to 8 data bits, 2 stop bits, no parity, internal clock.

**Reset to 0000.

***Does not disable the trace; logs the reset, if enabled.

--Does not change.

Error Recovery

Operate I/O Condition Codes

This attachment may present a variety of operate I/O condition codes. The codes for each type of Operate I/O command with a recommended program recovery or abort procedure are given following the programmable multi-line operate I/O condition-codes chart.

There will be only one controller-end interrupt request when multiple controller busy operate I/O condition codes are presented; consequently, the program should queue the controller busy condition codes and clear (post) the controller-end interrupt condition code to all controller-busy codes received.

Note: Under certain conditions, it is possible that more than one controller-end interrupt request is presented. If no busy condition is found upon examining the "controller busy" queue, disregard the interrupt request.

Programmable multi-line Operate I/O condition codes

CC	Even	Carry	Overflow	Meaning
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Busy after reset
3	0	1	1	Command reject
4	1	0	0	Intervention required
5	1	0	1	Interface data check
6	1	1	0	Controller busy (see Note)
7	1	1	1	Satisfactory

Note: Reported when the controller is busy servicing a previous Operate I/O instruction; a subsequent controller-end interrupt request will occur (interrupt condition code 0).

The following table shows recommended error-recovery or abort procedures for operate I/O error conditions:

Operate I/O command	Controller busy for next Operate I/O	Operate I/O CC	Recommended action
Read ID	No	0	Abort; device not attached
		1,2,4,6	Abort; hardware error
		3	Abort; examine IDCB function
		5	Retry; abort if problem persists
		7	Satisfactory
Prepare	No	0	Abort; device not attached
		1	Examine bit 15 (I-bit of the IDCB); if bit 15 equals 1, abort; if bit 15 equals 0, correct program
		2,4,6	Abort
		3	Abort; examine IDCB function
		5	Retry; abort if problem persists
		7	Satisfactory
Halt I/O	No	0,1,2,3,4,5,6	Abort
		7	Satisfactory
Device Reset	Yes	0	Abort; device not attached
		1,2,4,6	Abort
		3	Examine IDCB function; if OK, abort
		5	Retry; if trouble persists, abort
		7	Satisfactory
Write Data	Yes	0	Abort; device not attached
		1	Retry after device end if the device is busy or device reset, retry. If trouble persists, abort.
		2	Abort
		3	Examine IDCB, if correct, abort
		4	Abort
		5	Retry; if trouble persists, abort
		6	Retry after controller end interrupt
		7	Satisfactory
Start Start Cycle Steal Status, Start Diagnostics 1 & 2, Start Control	Yes	0	Device not attached; abort
		1	Retry after device end if device is busy or device reset then retry; if problem persists, abort
		2	Abort
		3	Examine function in IDCB; if correct, abort
		4	Abort
		5	Retry; if trouble persists, abort
		6	Retry after controller-end interrupt
		7	Satisfactory

Interrupt Condition Codes

Interrupt requests can only occur for the feature—programmable multi-line attachment following the acceptance of the following commands:

- Prepare (This command is not an interrupting command. An interrupt request can occur when the device is unprepared and an interrupt request is pending. This command is issued with the I-bit equal to 1.)
- Write Data
- Start
- Start Cycle Steal Status
- Start Diagnostic 1
- Start Diagnostic 2
- Start Control

The only interrupt codes presented by the attachment are 0, 1, 2, 3, 4, and 6. If an interrupt condition code 2 or 6 is reported, the program should examine the ISB and issue a Start Cycle Steal Status command (if the ISB bit 0 is active)

Programmable multi-line interrupt condition codes

CC	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end (see Note)
1	0	0	1	PCI
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention
5	1	0	1	Attention and PCI
6	1	1	0	Attention and exception
7	1	1	1	Attention and device end

Note: The controller presents the device address of line 0.

The following chart shows the recommended actions for various combinations of condition codes and interrupt status byte values. (The interrupt status byte bit meanings are included for your convenience.)

Interrupt status byte Bit	Name
0	Device-dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage check
5	Invalid storage address
6	Protection check
7	Interface data check

Interrupt CC	ISB (hex)	Recommended action
0	–	Retry Operate I/O commands queued with controller busy operate I/O condition code.
2	A0	Normal ending operation to a receive DCB if a COD was detected prior to reducing the byte count to 0. Perform a Start Cycle Steal Status command to obtain residual address.
2	80	Issue a Start Cycle Steal Status command; examine bits to determine further action.
2	40	Examine IDCB for invalid function modifier or odd DCB address; correct error condition; retry.
2	20	Occurs during a receive operation and indicates that the byte count reduced to 0 and no COD character was detected. Increase the receive data buffer size and byte count and retry.
2	10	Indicates that the DCB being executed had one or more of the following errors: an odd chaining address (word 5); a Start Cycle Steal Status DCB had a byte count other than 6 or an odd address; a transmit or receive DCB had a byte count of 0; the I/O bit of the DCB control word is incorrect; a diagnostic type DCB had incorrect byte count or odd data address; a Start Control command to an attachment with the I/O bit in the control word set to 1 did not have a byte count of hex 400 or hex 040, or, if the I/O bit equals 0, had an odd data address. Correct the error and retry.
2	08	Storage data check; retry operation; if error persists, abort.
2	04	Invalid storage address; correct program and retry.
2	02	Protect check; verify the protect key and retry. This error can only occur on a Series/1 processor that has the storage protection feature.
2	01	Interface data check; retry once; if the error persists, abort.
4	XX	Attention interrupt, used in expanded mode with ISB/IIB equal to the character received.
6	80	Attention with exception, always indicates that the expanded mode of operation (attention interrupt) detected an error on receive. This interrupt does not terminate any outstanding I/O commands.

Jumpers

Below is a description of the jumpers that can be installed on the four-line adapter cards.

Request to Send

There are four RTS jumpers on the card—one for each line. If this jumper is installed, the attachment maintains RTS in an active condition. This eliminates modem turnaround when using a full-duplex interface. This option must be selected when using a modem that always keeps CTS active.

Data Terminal Ready

There are four DTR jumpers on the card—one for each line. If this jumper is installed, the attachment maintains DTR in an active condition. To enable disconnecting from a switched network this option should not be selected for switched-line operation.

Bit Rate Jumpers

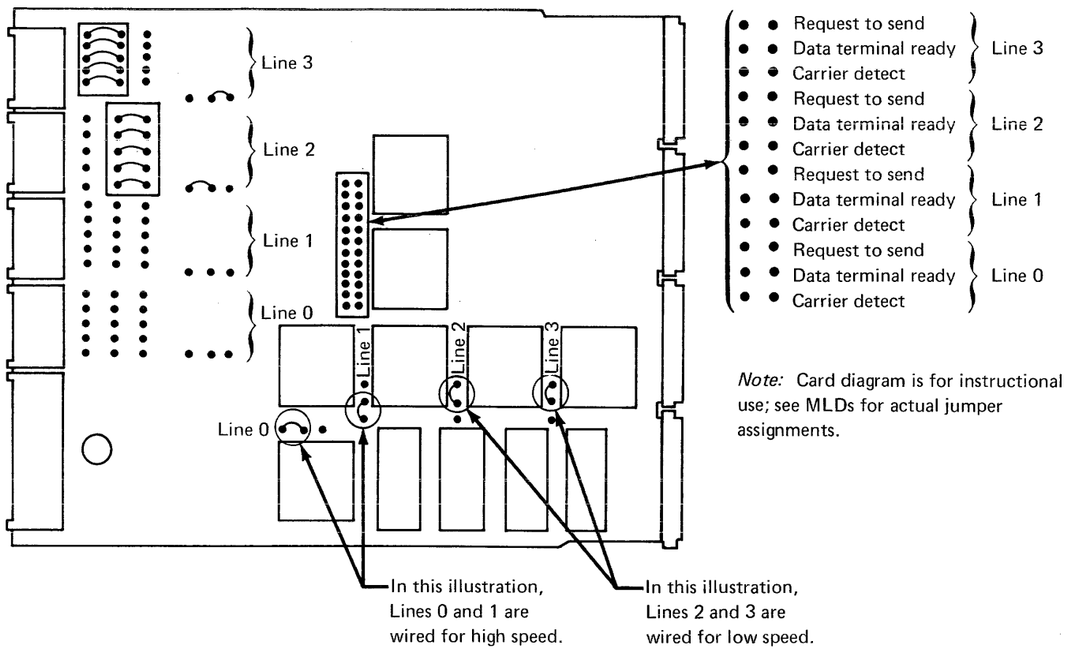
There are four sets (one low-range and one high-range) of jumpers for the card: one for each line. These jumpers are mutually exclusive; that is, one or the other must be selected for each line, but not both.

With the low-range jumper installed, speeds between 37.5 and 1,200 bps can be selected by programming; with the high-speed jumper installed, speeds between 300 and 19,200 bps can be selected by programming.

In this illustration:

Line 3 is wired for TTY current loop interface (all 6 jumpers must be installed).

Line 2 is wired for EIA RS232-C interface (all 6 jumpers must be installed).



Note: Card diagram is for instructional use; see MLDs for actual jumper assignments.

Carrier Detect

There are four carrier detect jumpers on the card—one for each line. Some modems offer the ability to check the quality of the received signal. When the signal is of acceptable quality, the modem generates 'carrier detect.' If the received signal starts to deteriorate, the modem notifies the attachment by deactivating 'carrier detect.'

'Carrier detect' is a function of the remote site when RTS and CTS are active. A loss of 'carrier detect' may be caused by the local modem, open lines, the remote modem, or the remote station not being in transmit mode.

If the 'carrier detect' jumper is not installed on the attachment card, the attachment waits for 'carrier detect' at the beginning of a receive type of operation. If 'carrier detect' does not become active within the time specified by timer 1, or if it becomes inactive during the receive operation, the attachment presents an exception interrupt request to the processor and activates 'modem interface error.' 'Carrier detect' also informs the user that the remote station has RTS active.

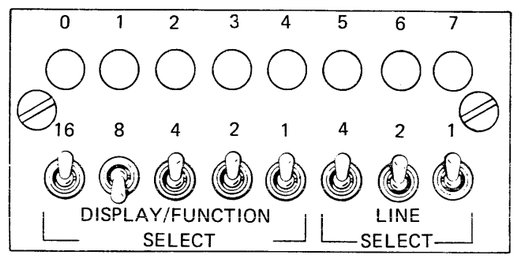
Line Interface Circuits

There are two types of line-interface-circuit jumpers: an EIA RS-232C/CCITTV24 interface and a 20 milliamp current loop interface. These jumpers are mutually exclusive; that is, one or the other must be selected for each line, but not both.

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine troubleshooting.

The communications indicator panel displays various conditions and registers in the attachment. In addition, the DTR line(s) to the modem(s) can be reset from the indicator panel. One setting of the DISPLAY/FUNCTION SELECT switches causes any incorrect data that is received to be placed in storage "as is."



LINE SELECT Switches

The three LINE SWITCHES switches are used to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the LINE SELECT switches.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION select switches determine what information is displayed on the panel. Following is a list of switch settings and the information that is displayed on the panel.

DISPLAY/ FUNCTION SELECT	Lamps	Information
00000	0–7	High-order byte of the DCB control word
00001	0–7	Low-order byte of the DCB control word
00010	0–7	Bit-rate constant
00011	0–7	Line-control character 1
00100	0–7	Line-control character 2
00101	0–7	Line-control character 3
00110	0–7	Line-control character 4
00111	0–7	Line-control character 5
01000	0–7	Line-control character 6
01001	0–7	Line-control character 7
01010	0–7	Bits 0–7 of the chain address
01011	0–7	Bits 8–15 of the chain address
01100	0–7	Bits 0–7 of the byte count
01101	0–7	Bits 8– 15 of the byte count
01110	0–7	Bits 0–7 of the data address
01111	0–7	Bits 8–15 of the data address
10000	0–7	Bits 0–7 of timer 2
10001	0–7	Bits 8–15 of timer 2
10010	0–7	Bits 0–7 of timer 1
10011	0–7	Bits 8–15 of timer 1
10100	0–4	Base device addresses
	5	Interrupt condition code (LSR even)
	6	Interrupt condition code (LSR carry)
	7	Interrupt condition code (LSR overflow)
10101	0–7	Engineering use
10110	0	Overrun
	1	Time-out
	2	Not used
	3	DCB reject
	4	Not used
	5	Parity error—VCR
	6	Break detected
	7	Stop-bit error
10111	0	Engineering use
	1	Modem-interface error
	2–3	Engineering use
	4	Error during pre-receive
	5–6	Engineering use
	7	Adapter buffer not empty
11000	0–7	Engineering use
11001	0	Data terminal ready
	1	Data set ready
	2	Request to send
	3	Clear to send
	4	External clocks
	5	Carrier detect
	6	Echoplex
	7	Receive line (on=mark)
11010	0–7	Engineering use
11011	0–7	Set mode or set control (bits 8–15 in the control word)
11100	0–7	Lamp test
11101	0–7	Interrupt status byte
11110	0–7	Place data into storage "as is"
11111	0	Data terminal ready
	1	Data set ready
	2	Request to send
	3	Clear to send
	4	External clocks
	5	Carrier detect
	6	Echoplex
	7	Receive

Programmable 8-Line Communication Control Feature

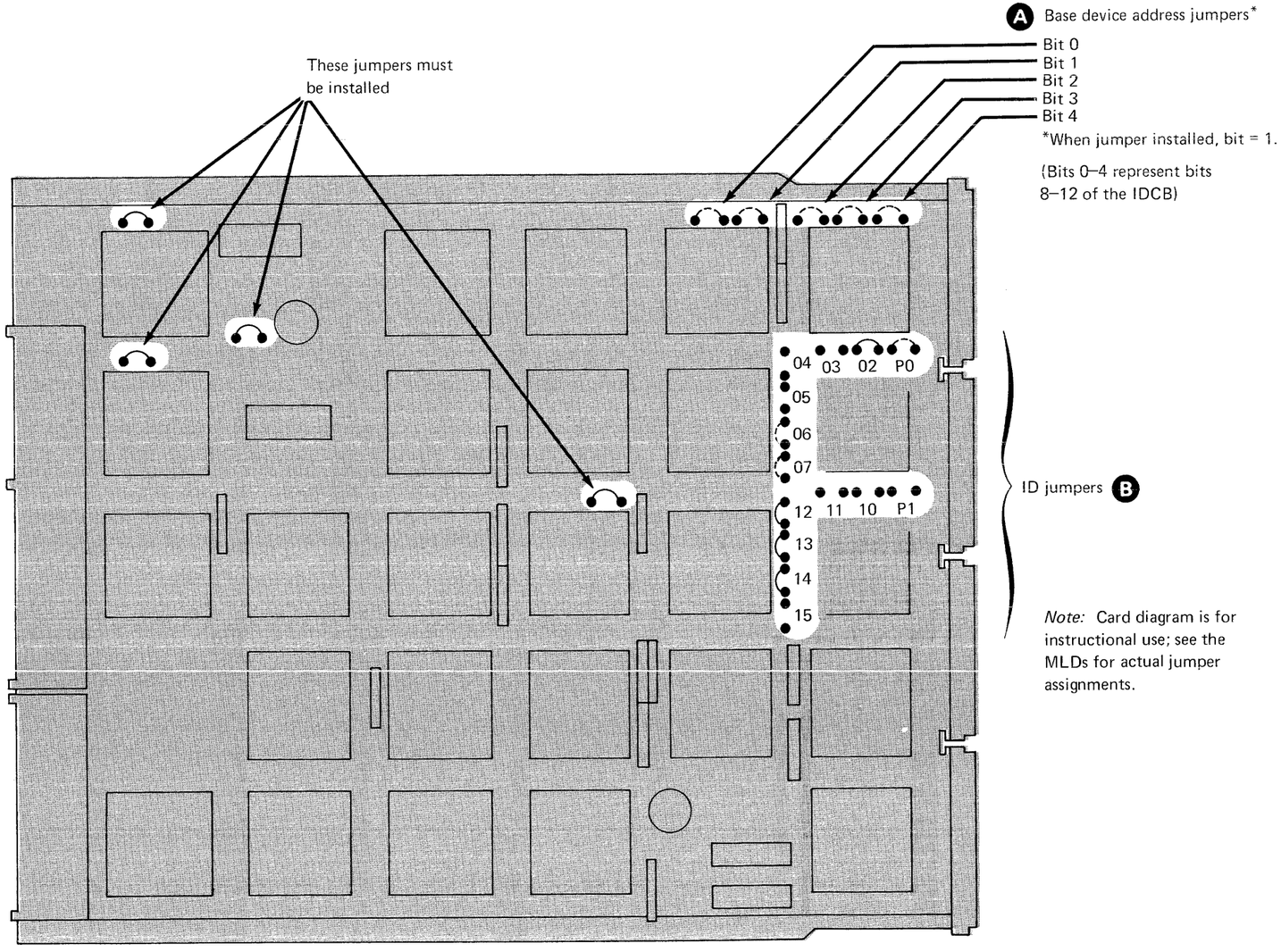
Ⓐ Device Address

These jumpers select the base address of line 0 on the Series/1 I/O interface.

Ⓑ ID Jumpers

These jumpers determine the information that the attachment will pass to the processor during the *Read ID* instruction. The jumpers should be as follows:

Bit 2	On
Bits 3, 4, 5	Off
Bits 6 & 7	These are determined by the number of lines installed. 2 lines—bit 6 off, bit 7 on 4 lines—bit 6 on, bit 7 off 6 lines—bit 6 on, bit 7 on 8 lines—bit 6 off, bit 7 off
Bit P0	Jumpered as required to maintain odd parity in the high order byte of the ID word
Bits 10, P1	Off
Bit 11	On
Bit 12	Off
Bits 13,14	On
Bits 15	Off



Asynchronous communications 8-line control feature

Chapter 5. Synchronous Communication Single Line Control

Introduction

The synchronous communication single line control attachment provides one International Telegraph and Telephone Consultative Committee (CCITT) X.21 interface to allow the interchange of data between the Series/1 processor and a remote terminal using the synchronous mode of data transmission. The terminal must comply with the electrical and functional requirements of CCITT recommendation X.21. Interconnection between the Series/1 and the remote terminal may be made using public or private leased data networks. In addition, terminals may be locally connected at distances up to 1220 meters (4000 feet).

This attachment supports synchronous data link control/high level data link control (SDLC/HDLC) or binary synchronous communication (BSC) protocol and, when operating with SDLC/HDLC protocol, may be operated in duplex mode. Duplex mode allows data to be concurrently transmitted and received between the Series/1 and the terminal. The communicating bit rate is normally controlled by clocking signals supplied by the DCE (Data Circuit Terminating Equipment), the exception being when using the local connect option, which provides clocking by the attachment. The attachment provides clocking for data rates of 9600 or 48000 bits per second (bps) when the local connect option is used.

For further information about the X.21 interface, refer to *IBM Implementation of X.21 Interface - General Information Manual*, GA27-3287.

> **Note:** The local connect option allows the connection of remote terminals without DCE's, using the RS-422A interface, at distances up to 1220 meters (4000 feet).

The attachment also provides one CCITT V.35 interface and supports both the SDLC/HDLC and BSC protocols with a maximum rate of 56000 bps.

> **Note:** Sustained throughput at 48000 and 56000 bps when using BSC protocol is considerable less than the clocking rate. Refer to the portion of this chapter on BSC protocol.

When using the local connect options, there are two basic connection methods:

- **Local 1 Attachment:** Internal clocking is occurs at a data rate of 9600 bps with the remote device capable of deriving the clocking information from the data stream. This mode of operation allows the remote terminal to be connected to a distance of 1220 meters (4000 feet) using an EIA RS-422A interface. Only the SDLC/HDLC half-duplex protocol is supported by this method of clocking. When operating in local 1 mode, the attachment transmits and receives in NRZI mode (bits 9 and 12 of the control word are ignored on transmit and bit 9 is ignored on receive). Leading pads are transmitted automatically at the beginning of each frame sequence.
- **Local 2 Attachment:** An internal attachment generated clocking signal at a data rate of 48000 bps is provided to an EIA RS-422A interface. This allows the remote device to use the clock as if a DCE were present. With this method of operation, the remote terminal must be connected at a distance of not greater than 305 meters (1000 feet). Both the SDLC/HDLC (half duplex & duplex) and BSC (half duplex) protocols are supported in this mode.

Control of up to 10 remote stations may be achieved by attaching them in a multi-drop configuration, stub length not exceeding 15 meters (45 feet). Both the SDLC/HDLC and BSC protocols are supported in this configuration.

> **Note:** For cable information, refer to the maintenance logic diagrams (MLD).

Refer to the Figure 5-1 flowchart for a graphic representation of installation considerations and available options.

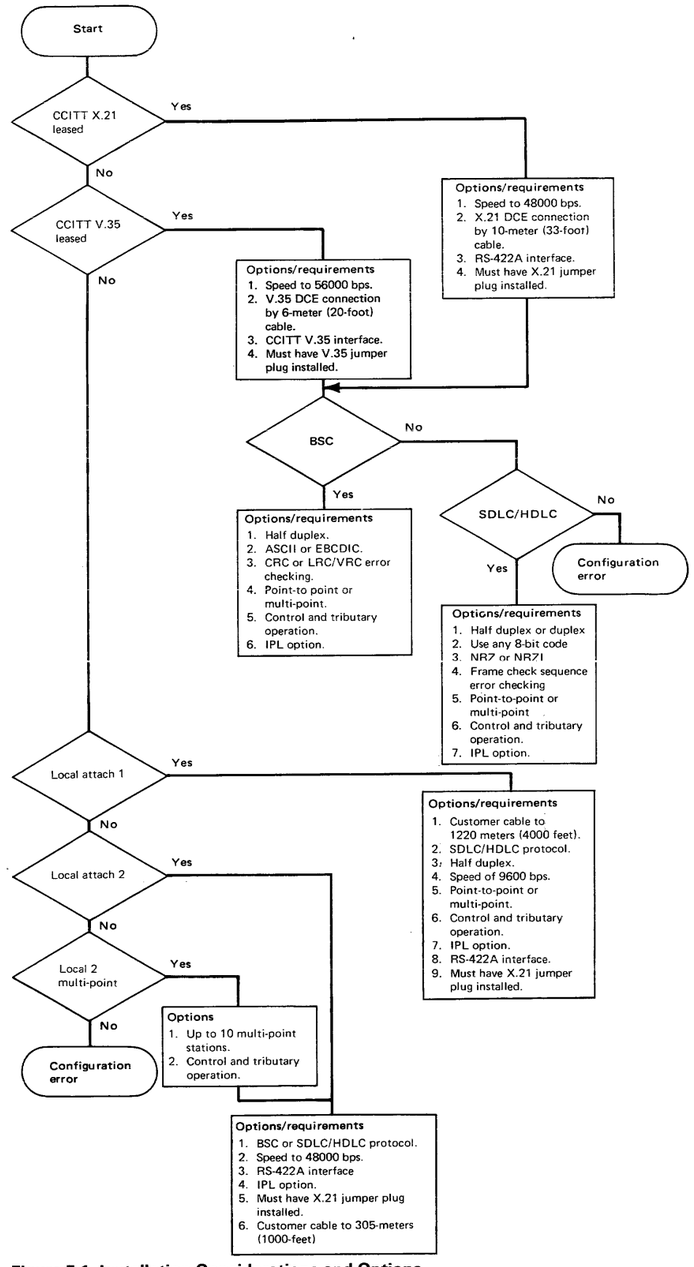


Figure 5-1. Installation Considerations and Options

Data Flow

Data transmission and reception protocol may be either SDLC/HDLC or BSC. Two characters at a time are fetched from storage during transmission. Bits 0-7 hold the first character transmitted and bits 8-15 hold the next. However, if the first character is located at an odd data address or the last character is located at an even data address, only one data character is fetched and transmitted.

On receive, the first bit received is placed in the least-significant bit, the second bit placed in the next higher bit position, and so on, until a character is assembled. The first character received is placed in bits 0-7 and the second character is placed into bits 8-15. Again, however, if the first character has an odd data address or the last character has an even data address, only one character is assembled and placed into processor storage.

Refer to Figure 5-2 for an example of data flow for both transmit and receive operations.

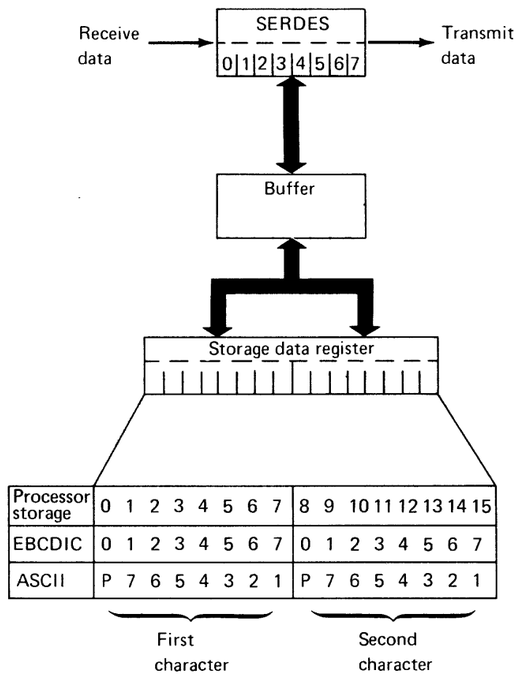


Figure 5-2. Data Flow

Device Addressing

The attachment has provisions for responding to Operate I/O commands for two unique device addresses. The addresses are contiguous, beginning with an even address. Jumper positions are provided on the attachment card for the assignment of the base device address (always even).

	Half duplex		Duplex	
Command	**Dev 0**	**Dev 1**	**Dev 0**	**Dev 1**
Start	X		X	
Enable*	X		X	
Disable*	X		X	
Transmit*	X		X	
Receive*	X			X
Timer*	X		X	X
Start Control**	X		X	
Start Modification**	X		X	
Start Cycle Steal Status**	X	X	X	X
Start Diag 1	X	X	X	X
Start Diag 2**	X		X	
Read ID	X	X	X	X
Halt I/O	X	X	X	X
Device Reset	X	X	X	X
Prepare	X	X	X	X

Note: Any command directed to device 0 or device 1 other than the ones indicated above will cause an exception interrupt.

* DCB specification check reported.
**Delayed command reject reported.

Note: This attachment always uses two device addresses.

When in half-duplex mode, device 0 is the even address. The device commands, addresses, and mode of operation are shown in the following table:

Device Commands

- Prepare
- Start Diagnostic 1
- Start Diagnostic 2
- Read ID
- Halt I/O
- Device Reset
- Start Control
- Start Modification

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The data word (bits 16-31) contains the level and I-bit. The device is always able to accept and execute a Prepare command, even if it is busy or has an interrupt request pending from a previous command. The IDCB for the Prepare command has the following format:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 0 0 0 0 0	X X X X X X X X
0 ... *7*	*8* ... *15*
60	00–FF

Immediate data field		
0's	Level	I
16 ... *26*	*27* ... *30*	*31*

Level - bits 27-30: This four-bit field specifies the priority interrupt level assigned to the device. The binary value of bits 27-30 indicates priority levels of 0-3.

Bits 27-30	Level
0000	0
0001	1
0010	2
0011	3

I-Bit - bit 31: This bit determines if the device is allowed to present interrupt requests. An I-bit set to 1 means that the device can request an interrupt; a 0 means that the device cannot interrupt.

The attachment stores the level data and presents it to the processor each time the attachment presents an interrupt request. The prepare information (level and I-bit) is reset by a system reset or a power-on reset.

The Prepare command causes an interrupt request only when the attachment is not prepared (I-bit set to 0) and has an interrupt pending upon receipt of a Prepare command with the I-bit set to 1.

The Prepare command always causes an attachment to respond with a condition code 7 (satisfactory).

Start Diagnostic 1

The IDCB for the Start Diagnostic 1 command is as follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 0 1	X X X X X X X X
0 ... *7*	*8* ... *15*
7D	00–FF

Immediate data field
DCB address
16 ... *31*

Start Diagnostic 1 causes two types of tests to occur in the attachment, with the results placed in processor storage beginning at the address specified in word 7 (data address) of the DCB. The byte count for this operation must be equal to 11 and the data address must be even; otherwise, an exception interrupt is presented with bit 3 (DCB specification check) set in the interrupt status byte.

A DCB specification check will occur if the control word of the DCB has any bit on other than bit 2, 5, 6, or 7.

The format of the DCB is as follows:

Word	*0 1 2 3 4 5 6 7 8* ... *15*
0	0 0 1 0 0 K E Y | 0's
1	Not used
2	Not used
3	Not used
4	Not used
5	Not used
6	Byte count (must be hex B)
7	Data address (even)

The diagnostic first performs an attachment storage test, which consists of writing/reading 1's and 0's through all the storage locations. If the test is successful, a hex FF is written into data word 5, high-order byte. If the test fails, a hex 00 is written into data word 5, bits 0-7.

> **Note:** During initial power-on sequencing, the random access storage patch (RAMPATCH) area is tested. The RAMPATCH area is not tested by the diagnostic command.

Next, a checksum is computed for the two ROS modules used by the attachment. The result is presented along with a checksum written into the modules at the time the modules were fabricated. The results are then placed in data words 1, 2, 3, and 4, which contain the following:

Data word 1	Stored checksum ROS 1
Data word 2	Computed checksum ROS 1 (complemented)
Data word 3	Stored checksum ROS 2
Data word 4	Computed checksum ROS 2 (complemented)
Data word 5	Bits 0-7 (FF good storage test)
	Bits 0-7 (00 storage test failure)
	Bits 8-15 (Secondary station/MP tributary address)
Data word 6	Bits 0-7 Bit 0 Not used Bit 1 BSC jumper Bit 2 Not used Bit 3 Local attach 2 jumper Bit 4 Local attach 1 jumper Bit 5 Allow IPL jumper Bit 6 V.35 jumper Bit 7 Not used
	Bits 8-15 refer to following text

The attachment reports the secondary station/multi-point tributary address jumpers in data word 5, bits 8-15. The attachment also reports the configuration jumpers in data word 6, bits 0-7. Bits 8-15 of the data storage register are set to a hex AA to test the byte mode of data transfer to storage. If byte mode fails a hex AA appears in data word 6, bits 8-15; otherwise, the value in data word 6, bits 8-15, is dependent on the processor storage initialization.

Start Diagnostic 2

The IDCB for the Start Diagnostic 2 command is as follows:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 1 1 1 0	X X X X X X X X
0 — *7*	*8* — *15*
7E	00—FF

Immediate data field
DCB address
16 — *31*

The Start Diagnostic 2 command causes a wrap test to occur in the attachment, with the results placed in processor storage, beginning at the address specified in word 7 (data address) of the DCB. The byte count for this operation must be equal to 2 and the data address must be even; otherwise, an exception interrupt is presented with bit 3 (DCB specification check) set in the ISB.

A DCB specification check occurs if the control word of the DCB has any bit on other than bit 2, 5, 6, 7, or 15. The DCB for the Start Diagnostic 2 command is as follows:

Word	*0 1 2 3 4 5 6 7 8* — *15*
0	0 0 1 0 0 K E Y 0's X
1	Not used
2	Not used
3	Not used
4	Not used
5	Not used
6	Byte count (must be 2)
7	Data address (must be even)

DCB word 0, bit 15, indicates the following:

- Bit 15 = 1, signal timing provided
- Bit 15 = 0, signal timing not provided

Note: Signal timing provided indicates that DCE (X.21 or V.35) is attached and is supplying the signal timing during the wrap test.

With the X.21 jumper in place, the attachment is tested in the X.21 mode in the following sequence:

1. Test 1 tests the control and transmit lines. The attachment sets bits 0-3 in data word 1 to 1's if the test is successful.
2. Test 2 checks the signal timing if bit 15 of DCB word 0 is set to a 1. If the test is successful, bit 4 of data word 1 is set to a 1. If bit 15 of DCB word 0 is set to 0, the attachment tests for a clocking signal and, if detected, bits 4 and 5 (signal timing and byte timing) in data word 1 are set to a 1's.
3. Test 3 causes the attachment to perform a BSC wrap test. If the test is successful, the attachment sets bit 6 in data word 1 to a 1.
4. Test 4 causes the attachment to perform an SDLC wrap test. If the test is successful, the attachment sets bit 7 in data word 1 to a 1.
5. Test 5 causes the attachment to "read" the switches on the indicator panel and report the hexadecimal value in bits 8-15 of data word 1. If the indicator panel is not attached, the attachment reports a hex 00 in bits 8-15 of data word 1.

Note: Data word 1 has the following bit definitions for X.21:

Bit	Definition
0	Transmit
1	Receive
2	Indicate
3	Control
4	Signal timing
5	Byte timing
6	BSC wrap
7	SDLC wrap
8-15	Indicator panel switch setting

With the V.35 jumper plug in place, the attachment is tested in the V.35 mode.

Note: All tests, with the exception of Test 1 function in the same manner as for the preceding X.21 tests. Test 2 is not performed in V.35 mode.

Test 1 checks 'the request to send' (RTS) and 'clear to send' (CTS) lines. If the test is successful, the attachment sets the associated bit (see following bit definitions) to a 1 in data word 1.

Data word 1 has the following bit definitions for V.35:

Bit	Definition
0	DSR
1	CTS
2	RTS
3	Not used (0's)
4	Not used (0's)
5	Not used (0's)
6	BSC wrap
7	SDLC wrap
8-15	Indicator panel switch setting

Read ID

The Read ID command transfers the attachment's identification word from the device to the data word position of the IDCB.

The attachment's ID is 5042. The IDCB for the Read ID command is:

IDCB (immediate device control block)

Command field	*Device address*
0 0 1 0 0 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
20	00—FF

Immediate data field
Identification word
16 — *31*

Halt I/O

This command halts all I/O activity on the data channel and sets the interface to DTE ready and resets the residual byte count to 0.

IDCB (immediate device control block)

Command field	*Device address*
1 1 1 1 0 0 0 0	X X X X X X X X
0 — *7*	*8* — *15*
F0	00—FF

Immediate data field
0's
16 — *31*

Device Reset

The Device Reset command resets the addressed device. Pending interrupt requests (except controller end) are cleared. The prepare level, I-bit, residual address, and interface state are not reset by this command. The Device Reset command has the following format:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 0 1 1 1 1	X X X X X X X X
0 — *7*	*8* — *15*
6F	00—FF

Immediate data field
0's
16 — *31*

A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are carried out. The amount of time that the attachment is busy is a function of the microcode program. The attachment presents a busy after reset (CC2) if an Operate I/O immediately follows a Device Reset.

Start Control

The Start Control command is used to setup operating conditions. The IDCB for the Start Control command is:

IDCB (immediate device control block)

Command field	*Device address*
0 1 1 1 0 0 0 1	X X X X X X X X
0 — *7*	*8* — *15*
71	00—FF

Immediate data field
DCB address
16 — *31*

The format for the Start Control (set mode) DCB is as follows:

DCB (device control block)

Word	*0* — *5*	*7*	*8* — *15*
0	X 0 0 0 0	K E Y	0 0 0 0 0 0 0 0
1	0 0 0 0 0	0 0 0	0 0 0 X X X 0 0
2	Not used		
3	Not used		
4	Not used		
5	Chaining address		
6	Not used		
7	Not used		
	0		*15*

Word 0

Bit 0 - Chaining: This bit is set to 1 if chaining is in effect.

Bits 1-4: These bits are not used and must be set to 0.

Bits 5-7 -Key: These bits represent a 3-bit key that the attachment presents to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid key causes an exception-interrupt request (condition code 2), with bit 6 set to 1 (protect check) in the ISB.

Bits 8-15: These bits are not used and must be set to 0.

Word 1

Bits 0-10: These bits are not used and must be 0's.

Bit 11 - PCI: When this bit is a 1, it indicates that PCI is supported.

Bit 12 - Mode: When this bit is a 1, the attachment is in duplex mode of operation. When this bit is a 0, the attachment is in half duplex mode of operation.

Note: When this bit is a 1, only SDLC/HDLC mode is supported.

Bit 13 - Installation Test: When this bit is a 1, the attachment performs internal tests (used for installation measurements).

Bit 14: This bit is not used and must be 0.

Bit 15: This bit is not used and must be 0.

Words 2-4

These words are not used and must be set to 0.

Word 5

This word contains the address of the next DCB in a chaining operation.

Words 6-7

These words are not used and must be set to 0.

Start Modification

The Start Modification command is used by engineering to modify the attachment micro-code. This command initiates a cycle-steal operation for device 0. If issued to device 1, a delayed command reject is reported (information status byte, bit 1 is set on). The IDCB for this command is as follows:

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 0 0 1 0	X X X X X X X X
0 — *7*	*8* — *15*
72	00—FF

Immediate data field
DCB address
16 — *31*

The DCB for the Start Modification command is described as follows:

1. Words 0, and 2-5 of the DCB are not used, therefore chaining of DCBs is not supported.
2. Word 1 of the DCB contains the address of the attachment storage location where the micro-code patch is to begin.
3. Word 6 of the DCB contains the byte count of the number of bytes to be allocated in the attachment for the micro-code patch.
4. Word 7 of the DCB contains the processor storage address where the micro-code patch begins.

Synchronous Data Link Control (SDLC/HDLC)

The synchronous data link control (SDLC/HDLC) capability allows transfer of serial data to and from a remote terminal or host system via a DCE and communications line facility. The SDLC/HDLC function can be used for connecting a Series/1 processor to telecommunication equipment or other processors having compatible adapters.

Note: The attachment views both the SDLC and HDLC protocols in the same manner.

- Data transmission uses SDLC/HDLC control procedures
- Any eight-bit data code may be used
- Bit rates can be up to 56000 bps using V.35 interface.
- It may be used as either a primary or secondary station
- Internal clocking is available for local 1 mode operation
- Non-return-to-zero inverted (NRZI) coding is used with internal clocking (local attach 1)
- Non-return-to-zero (NRZ) coding or NRZI coding may be used with clocking supplied by the DCE or local attach 2.

Data transmission is serial-by-bit, using the synchronous data link control (SDLC) method of character and bit transmission. A general discussion of the SDLC/HDLC procedures may be found in *IBM Synchronous Data Link Control — General Information* , GA27-3093.

The attachment can communicate with host systems using Extended Binary-Coded Decimal Interchange Code (EBCDIC) or any other eight-bit data code. The SDLC/HDLC uses a specific set of line control characters, but because transparency is inherent in SDLC/HDLC, the data characters can be any eight-bit code that is mutually acceptable to the sending and receiving stations.

The SDLC/HDLC communication can operate on a leased line at rates up to 56000 bps using V.35 interface.

When internal (business machine) clocking is used (local attach 1), the characters are transmitted and received using NRZI coding. When clocking is provided by the DCE, either NRZ or NRZI coding may be selected by the software. Internal clocking provides the strobe pulses used to strobe bits between the DCE and the adapter. In receive mode, it also establishes and maintains bit synchronization through an advance or retard of the data strobe. A transmission rate of 9600 bps is available through the internal clocking feature.

Operating Modes

Monitor Mode

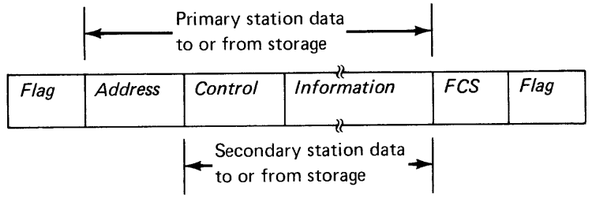
The attachment is placed in monitor mode by a receive operation. While in this mode, the attachment is constantly monitoring the line, looking for a flag character. If the attachment is operating as a secondary station, it checks the address following the flag. If the address is its own (or the broadcast address), the attachment goes into receive mode. If the address is not the address of the attachment, the attachment remains in monitor mode.

IPL Mode

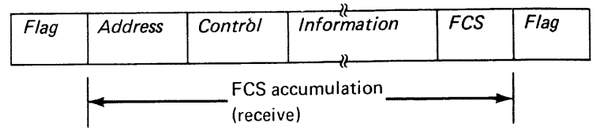
The attachment is placed in IPL mode. While in this mode, when the attachment is not busy, it monitors for an IPL sequence. If an IPL sequence is received, the attachment processes it and presents a device end interrupt. If an error occurs during the IPL sequence, the attachment holds the IPL line to the processor active, and again monitors for the IPL sequence.

Receive Mode

If the attachment is operating as a primary station, data is transferred to main storage beginning with the A-field (address field). When the attachment is operating as a secondary station in receive mode, data is transferred to processor storage beginning with the C-field (control field). If the attachment is operating as a secondary station, the attachment automatically checks the received address to determine if the frame is intended for this station. If the frame is intended for this station, the attachment transfers the data to storage (beginning with the C-field).

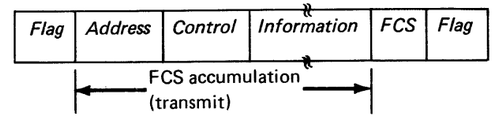


The accumulation of frame-check sequences starts with the address and includes the frame-check sequence (FCS) received.



Transmit Mode

This mode is established when a transmit operation has been issued by the program. Frame-check sequence accumulation begins with the first character to be transmitted after the beginning flag character and continues until the byte count, device control block (DCB) word 6, is decremented to 0.



The frame-check sequence is then automatically transmitted, followed by a flag character. If the attachment is operating as a primary station, the address of the receiver comes from storage. If the attachment is operating as a secondary station, the hardware provides the A-field of the frame.

Initial Program Load (IPL)

SDLC/HDLC IPL

When the attachment is not busy processing a software command, it monitors the 'receive data' line for an IPL sequence. The IPL sequence proceeds as follows:

1. The IPL'ing system sends a Set Initialization Mode (SIM) command that causes the Series/1 processor to begin an IPL sequence. The bit configuration of the control byte for the SIM command is hex 17. All of the commands and responses in this sequence are common to both SDLC and HDLC protocols.
2. The attachment responds with an unumbered acknowledgement (UA, hex 73), if the allow IPL jumper is installed. The attachment resets the Series/1 and prepares the system to receive the IPL data. If the attachment is not jumpered for allow IPL, a disconnected mode (DM, hex 53) response is issued.
3. The IPL'ing system transmits one frame of data of up to 64000 bytes. The first byte of data in the information field (I-field) is placed in the Series/1 processor storage at location 0.
4. If the received frame check sequence (FCS) is valid, the Series/1 transmits a receive not ready (RNR, hex 35) with an Nr count equal to 1 to acknowledge receipt of the information frame (IPL load). An interrupt is then presented to the processor on level 0 with the attachment device address in register 7 (the attachment is automatically prepared to level 0 with the I-bit set on). Program execution then starts at location 0.
5. Should a data error be detected, the attachment holds the IPL line to the processor active, does not respond, and monitors for a retry (new SIM command). The IPL'ing system must start the sequence anew and not simply retransmit the I-frame.

Notes:

a. The attachment monitors for the IPL sequence only when not busy; therefore, if a receive operation is pending and a SIM command is received, it is passed to the software the same as a normal frame.

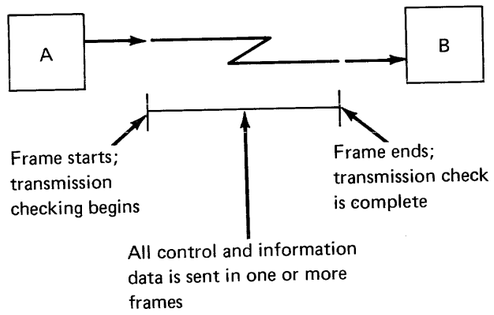
b. While the I-frame containing the IPL load may be up to 64000 bytes long, it is not recommended that an IPL load of this length be used. The 16-bit FCS loses some of its inherent checking capability when the frame length is greater than 4K bytes. Also, the possibility of receiving a line "hit" and bad data, even though it is determined to be invalid by the FCS, is also a function of the length of the I-frame.

Transmission Codes

The SDLC/HDLC function allows data communication using any eight-bit data code, including EBCDIC. The EBCDIC character assignments are shown in Appendix A.

Control Characters

Two levels of information grouping are used in SDLC/HDLC procedures. The basic level, called a frame, is checked by the attachment for transmission errors. The frame is the vehicle for all commands, responses, and information transmitted using SDLC/HDLC procedures.

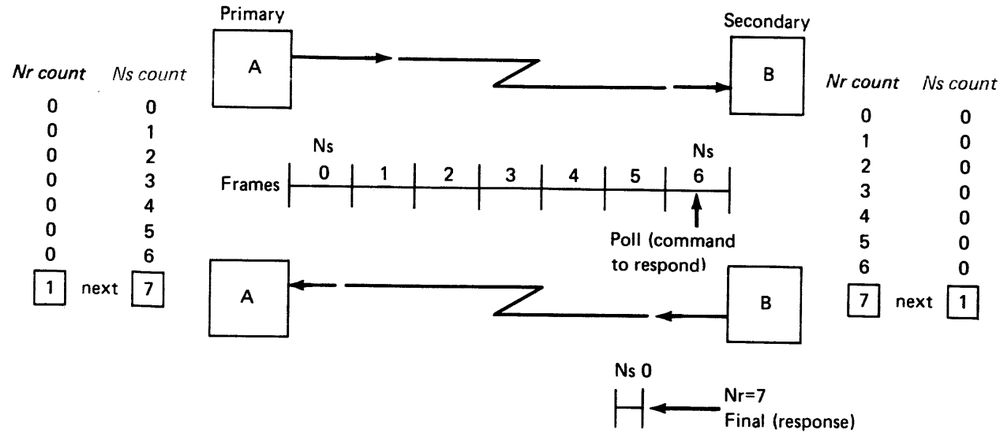


In the higher level of grouping, a frame sequence is checked by the program for missing or duplicated frames. At a station that transmits sequenced frames, the program counts and numbers each sequenced frame; this count is called Ns. At a station receiving sequenced frames, the program counts each error-free sequenced frame that it receives; this count is called Nr.

The program advances the Nr count when a frame is checked and found to be error-free. Nr then becomes the count of the next-expected frame and should agree with the next incoming Ns count. If the incoming Ns does not agree with Nr, the frame is out of sequence and the Nr count does not advance. Out-of-sequence frames may be rejected or saved, at the option of the program. The receiving station accepts the incoming Nr count (confirmation) if the out-of-sequence frame is otherwise error-free.

The counting capacity for Nr or Ns is 8, using the digits 0 through 7. These counts can "wrap around"; (7 is followed by 0). Up to seven frames may be sent before the receiver reports its Nr count to the transmitter because some or all of the frames may need repeating. The reported Nr count is the sequence number of the next frame that the receiving station expects to receive; therefore, if the count is not the same at a checkpoint as the transmitter's next sequence number, some of the frames already sent must be repeated.

The Nr and Ns counts of both stations are initialized to 0 at the discretion of the primary station. At all other times, the counts advance as sequenced frames are sent and received.



If B responds with Nr =:

7 (as above, all frames check OK)
6 (frame 6 discarded because of error)
5 (error on frame 5; 5 and 6 discarded)
4 (error on frame 4; 4–6 discarded)
3 (error on frame 3; 3–6 discarded)
2 (error on frame 2; 2–6 discarded)
1 (error on frame 1; 1–6 discarded)
0 (error on frame 0; no frames accepted)

Then A may send, on request, Ns frames:

7, 0, 1, 2, 3, 4, 5 (continue)
6, 7, 0, 1, 2, 3, 4 (retransmit and continue)
5, 6, 7, 0, 1, 2, 3 (retransmit and continue)
4, 5, 6, 7, 0, 1, 2 (retransmit and continue)
3, 4, 5, 6, 7, 0, 1 (retransmit and continue)
2, 3, 4, 5, 6, 7, 0 (retransmit and continue)
1, 2, 3, 4, 5, 6, 7 (retransmit and continue)
0, 1, 2, 3, 4, 5, 6 (retransmit)

Note: Shaded frames are retransmitted.

Frame Format

All active communication regulated by SDLC/HDLC procedures have a format called a frame, with each frame enclosed in flags.

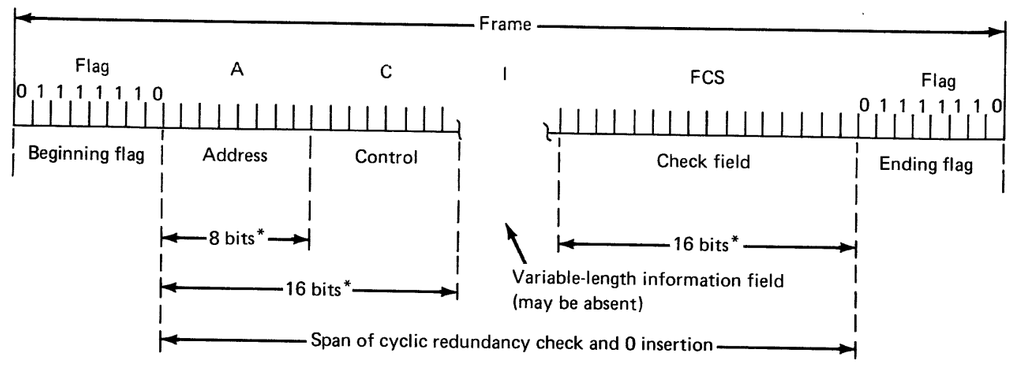
Starting from the beginning flag as a reference point, eight consecutive binary bits are dedicated to the address (A) of the secondary station. The next eight consecutive bits comprise the control (C) information, which can be a command or response. At least 16 more bits are transmitted after the C-field before the ending flag is sent. These 16 bits, the frame-check sequence (FCS), contain the transmission checking information; therefore, the internal structure of any valid frame must consist of at least 32 consecutive binary bits. Any information (I) field is sent following the C-field and preceding the frame-check sequence field. The I-field is not restricted in format or content. In a frame with an I-field, the maximum length is not restricted by procedures.

The transmission check at the receiver is complete when the ending flag is recognized. The receiving attachment separates the I-field from the frame-check sequence information when the ending flag is received, and does not put the frame-check sequence into storage.

Flag

Two flags, the beginning flag and the ending flag, enclose the SDLC/HDLC frame. The beginning flag serves as a reference for the positions of the A- and C-fields, and initiates transmission error checking; the ending flag terminates the check for transmission errors. Both beginning and ending flags have the binary configuration 01111110. The bit orientation of SDLC/HDLC allows the flag to be recognized at any time.

A flag may be followed by a frame or by another flag.



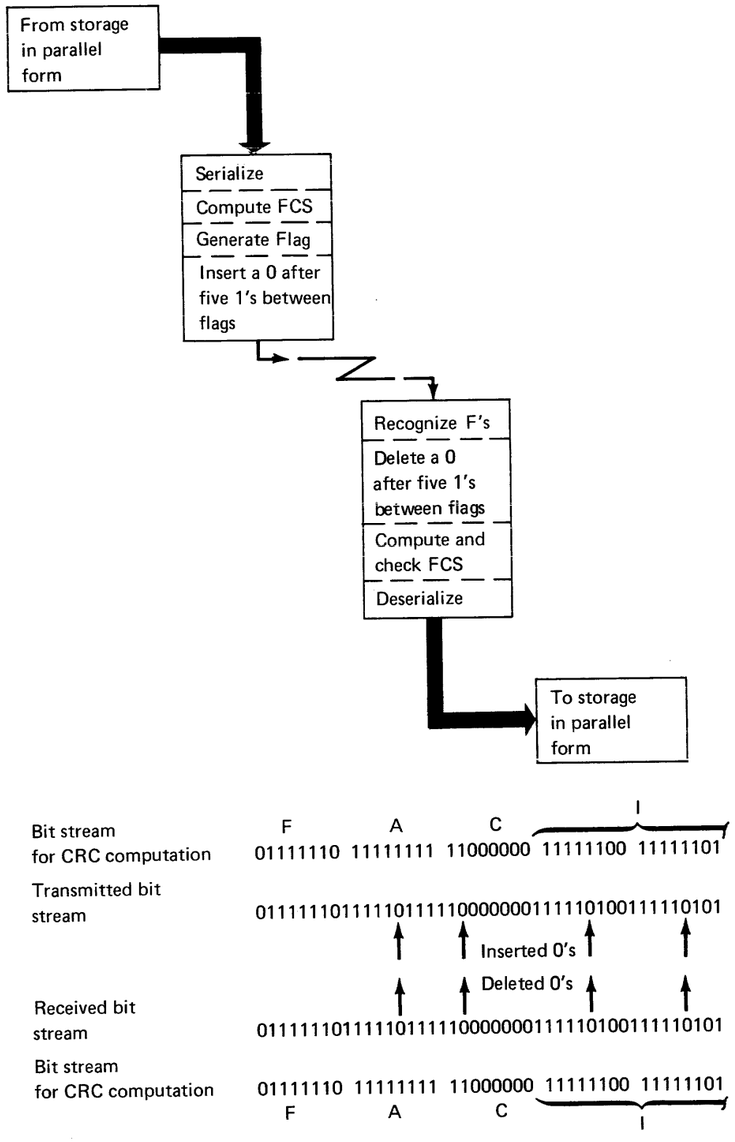
*Excluding inserted 0's.

Frame Format

0-Insertion

A frame can be identified because it begins with a flag and contains only non-flag bit patterns (The frame ends at the next flag). This characteristic does not restrict the contents of a frame, because SDLC/HDLC procedures require that a binary 0 be inserted by the transmitting station after any succession of five contiguous 1's within the frame. No pattern of 01111110 (flag) is ever transmitted by chance. After testing for flag recognition, the receiver removes a 0 that follows a received succession of five contiguous 1's. The attachment automatically provides 0-insertion and deletion. Inserted and removed 0's are not included in the transmission error check. (A 1 that follows five 1's is not removed.)

Note: When NRZI transmission recording is used, 0-insertion eliminates the remaining possibility of prolonged non-transition periods in the active state. NRZI transmission allows the transmit data line to change states when a logical 0 is transmitted.



Data Link Control Functions and 0 Insertion/Deletion

Idle Stations

A series of contiguous flags may be transmitted by a station to maintain bit synchronization and to maintain the data link in an active state. A series of flags may also be used to hold the authority to transmit and to avoid time-outs at the linked station(s).

Note: The use of NRZI transmission recording and 0-insertion is restricted to the active state of the data link; neither one operates in the idle state.

Address Field

The primary station manages a data link by issuing commands to the secondary stations that recognize their addresses in the A-field of a received frame.

A primary station can address all secondaries by sending an all 1's address (hex FF). A secondary station may receive a common address or its individual address; however, when a secondary station sends any response, only its individual address is used.

Control Field and Poll/Final (P/F) Bit

The C-field contains, within its eight binary digits, the capability to encode the commands and responses required to control a data link. The C-field has the following three formats:

	Sent last →							Sent first →
Bits	0	1	2	3	4	5	6	7
Information transfer format		Nr		P/F		Ns		0
Supervisory format		Nr		P/F	*		0	1
Nonsequenced format		**		P/F	**		1	1
Poll/final bit				▲				

*Codes for supervisory commands/responses
**Codes for nonsequenced commands/responses

Each C-field contains the format identifier and poll/final bits. The codes for the C-field commands and responses are as follows:

Format (See Note)	Sent last → Binary configuration → Sent first			Acronym	Command	Response	I-field prohibited	Resets Nr and Ns	Confirms frames through Nr-1	Defining characteristics
NS	000	P/F	0011	UI	X	X				Command or response that requires unnumbered information
	000	F	0111	RIM		X	X			Initialization needed; expect SIM
	000	P	0111	SIM	X		X	X		Set initialization mode; the using system prescribes the procedures
	100	P	0011	SNRM	X		X	X		Set normal response mode; transmit on command
	000	F	1111	DM		X	X			This station is offline
	010	P	0011	DISC	X		X			Do not transmit or receive information
	011	F	0011	NSA		X	X			Acknowledge NS commands
	100	F	0111	FRMR		X				Invalid frame received; must receive SNRM, DISC, or SIM
	101	P/F	1111	XID	X	X				System identification in I-field
	001	P/F	0011	NSP	X		X			Response optional if no P-bit
	111	P/F	0011	TEST	X	X				Check pattern in I-field
S	Nr	P/F	0001	RR	X	X	X		X	Ready to receive
	Nr	P/F	0101	RNR	X	X	X		X	Not ready to receive
	Nr	P/F	1001	REJ	X	X	X		X	Transmit or retransmit, starting with frame Nr
I	Nr	P/F	Ns 0	I	X	X			X	Sequenced I-frame

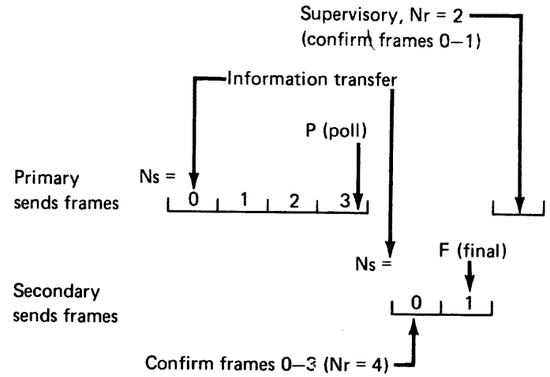
Note: NS = nonsequenced, S = supervisory, I = information.

The poll/final (P/F) bit is the send-receive control. A poll bit is sent to the secondary station to authorize transmission; a final bit is returned by the secondary station in response to the poll bit. **Do not confuse the final bit with the F-frame (flag) delimiter pattern.** Normally, only one poll bit is outstanding (unanswered by a final bit) on a data link.

Information Transfer Format

A C-field in the information transfer format is a part of each sequenced frame that is transmitted over a data link. It contains the poll-final bit and the Nr and Ns counts.

Stations transmitting information-transfer frames request configuration by sending the Ns count; they confirm by sending the Nr count.



Supervisory Format

The supervisory format is used with the information transfer format. Frames containing a C-field of the supervisory format convey ready or busy conditions and may be used to report sequence errors (thus requesting retransmission). Such frames may be interspersed with frames having a C-field of the information transfer format. Whether or not a primary station has information data to transmit, it may use a frame having a C-field of the supervisory format to poll a secondary station. A secondary station may use the supervisory format to respond to a request for confirmation. Frames with a supervisory format C-field are not counted in the Nr or Ns counts.

Nonsequenced Format

Command and response frames having a C-field in nonsequenced format are used for data link management. Data link management includes activating and initializing secondary stations, controlling the response mode of a secondary station, and reporting of procedural errors (not recoverable by retransmission). Information data may also be transmitted, using a frame with a C-field of the nonsequenced format. Frames with a nonsequenced format C-field are not counted in the Nr or Ns counts.

Information Field (I-Field)

SDLC/HDLC procedure is designated as a vehicle for data contained in the I-field. The I-field contains data that is moved, by using the data link, from place to place in the system. The I-field is unrestricted in format and content and its contents are not apparent to the components of data link control.

An I-field is normally included with every frame having a C-field in the information-transfer format. These information-transfer frames are the only ones that are sequenced.

There are provisions for an I-field in frames with a nonsequenced format C-field, but these are unprotected by sequence checking.

Frame Check Sequence Field

The frame-check sequence field, also called the block check character (BCC), contains 16 binary digits. It follows the I-field (if there is one; the C-field if not) and immediately precedes the ending flag. These 16 digits result from a mathematical computation on the digital value of all binary bits within the frame (excluding inserted 0's). The purpose is to validate transmission accuracy.

The transmitting SDLC/HDLC attachment performs the computation and sends the resulting frame-check sequence value. The receiving SDLC/HDLC attachment performs a similar computation and checks its results; it discards a frame that is found to be incorrect and does not advance its Nr count.

Synchronization

The basic SDLC/HDLC attachment receives timing pulses from the modem/DCE. This establishes and maintains bit synchronization. When the attachment starts to transmit, the attachment automatically transmits a flag character to establish frame and byte synchronization.

Some DCEs, to operate properly, may require NRZI-recorded data and/or pad characters. Bits 9 and 12 of the DCB control word can be used to satisfy particular DCE requirements.

If internal clocking (local 1 attach mode) is used, the attachment operates in NRZI mode and automatically sends two pad characters (hex 00) prior to sending the beginning flag. This causes 16 bit transitions to precede the flag character.

SDLC/HDLC Timers

The attachment has two programmable timers. Each timer can count up to 27 seconds, in 106-millisecond increments. Bits 0 through 7 of DCB word 1 control timer 1 and bits 8 through 15 control timer 2.

Timer 1

Timer 1 can be used in a variety of ways:

- *Idle detect timer.* If a receive operation is specified, the attachment runs timer 1 for the duration specified by bits 0 through 7 of DCB word 1. When this time runs out, the attachment begins checking the line for an idle condition. If an idle condition is detected, the attachment presents an exception-interrupt request.

  If a flag character is detected while timer 1 is running, the attachment immediately begins checking for an idle condition and stops timer 1. If an idle condition is detected from the time that timer 1 stops until the receive operation ends, the attachment presents an exception-interrupt request.

  If the program assigns a value of 0 to timer 1, the attachment does not check for an idle condition.

  Note: An idle condition is 15 contiguous 1's on the line.

- *DCE ready time-out.* During an enable terminal operation, this time-out occurs if DCE ready is not returned by the DCE within the specified time.
- *Disable data terminal ready time-out.* During a disable terminal operation, a time-out occurs if DCE ready is not deactivated within the specified time.
- *Clear to send time-out.* During a transmit operation, a DCE interface error occurs if clear to send (CTS) is not returned by the DCE within the specified time.

  Note: This CTS time-out is valid only in V.35 mode of operation.

- *Program delay.* When the operation is not an enable terminal, disable terminal, receive, or transmit operation, timer 1 can be used by the program for timing purposes.

Timer 2

Timer 2 is used in the following ways:

- *Nonproductive receive time-out.* This time-out is used only during receive operations. Its purpose is to limit the total nonproductive receiving time for a total receive operation. A total receive operation can be a single receive operation or a chain of receive operations initiated by a single Operate I/O instruction. When chaining receive operations, the value for timer 2 is taken from each DCB in the chain. The timer runs anytime the attachment is not receiving flags or frames. When timer 2 times out, the attachment presents an exception interrupt request.
- *Hold-line-active timer.* When timer 2 is used in conjunction with a transmit operation, with bit 15 on in the DCB control word, the attachment transmits flag characters for the duration of the time specified by bits 8 through 15 of DCB word 1, or until another transmit operation begins.

  Note: When the timers are set to 0's, no time-out occurs.

SDLC/HDLC Commands

- Start
- Start Cycle Steal Status

It is the programmer's responsibility to ensure that the program always tests the Operate I/O condition codes following an Operate I/O Instruction.

Start

The Start command transfers the address of a DCB to the attachment. When the Start command is accepted, the attachment fetches the DCB from the processor storage address specified in the immediate data field of the IDCB and begins executing the operation.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 0 0 0 0	0 X X X X X X X
0 — *7*	*8* — *15*
70	00—FF

Immediate data field
DCB address
16 — *31*

SDLC/HDLC Device Control Block (DCB)

The DCB is an eight-word area in processor storage that describes the specific parameters of the cycle-stealing operation. Its location in storage is assigned by the program. The data is loaded and changed by the program. The DCB is fetched by the attachment, using a cycle-steal address key of 000 after successful execution of a Start command.

The DCB address transferred to the attachment by the IDCB points to word 0. The table is in ascending storage address order, with the lowest storage address at the top of the table.

Note: The address of the DCB in processor storage must be even. If the address is odd, the attachment presents an exception interrupt (CC2), with bit 1 (delayed command reject) set in the interrupt status byte (ISB), and terminates the cycle-steal operation.

The format of the SDLC/HDLC DCB is as follows:

DCB (device control block)

Word		
0	Control word	
1	Timer 1	Timer 2
2	Not used (0's)	
3	DCB ID	Not used (0's)
4	Status address	
5	Chaining address	
6	Byte count	
7	Data address	
	0 — *15*	

Word 0 - Control Word

Bit 0 - Chaining Flag (CHN): If this bit is a 1, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit is a 0 and the operation is successfully completed, the attachment presents a device end interrupt.

Bit 1 - Program-Controlled Interrupt (PCI): This bit causes the device to present a PCI at the completion of the DCB fetch. The data transfer, associated with the DCB, may commence even though the PCI may be pending in the attachment. When this bit is set to 1, bits 0-7 of DCB word 3 are placed in the interrupt information byte (IIB) upon interrupt presentation.

This bit is recognized during any transmit or receive operation only. A DCB specification check (bit 3 of the interrupt status byte) is presented if attempted on any other command.

In order to use the PCI, a Start Control command DCB must have been previously issued with bit 11 set on in word 1. If a Set Mode command was not issued with this bit on, the attachment reports an exception interrupt (CC2) with bit 3 (DCB specification check) set in the interrupt status byte.

Bit 2 - Input Flag (IF): When the input flag bit is a 1, it allows the attachment to cycle-steal data into processor storage once byte synchronization is established. A receive operation is specified when this bit is a 1.

For a receive operation, a device end interrupt is given if no chaining is specified and no errors occurred. A device end interrupt is presented if the no-exception (NE) bit (residual status block word 1, bit 15) is set in all residual status blocks associated with the current frame sequence. A permissive device end interrupt (interrupt condition code 3 and IIB bit 0 set) is given if a residual status block has had the no-exception bit off for any frame received in the current frame sequence. If bit 12 of the control word is off on a receive operation and the poll/final (P/F) bit is detected as set, chaining is terminated and the chained-to-DCB is not fetched. Therefore, the use of chaining from a receive operation to any operation other than a receive should be avoided.

If no chaining was specified and no P/F bit was detected as set, the attachment anticipates another receive command by staying in receive mode and monitoring the 'receive data' line.

This operation allows the attachment to detect the following frame if only one flag was present between frames. The attachment cycle-steals the data into processor storage when a Receive command is issued or reports overrun if that condition exists.

An error interrupt is present when:

- The X.21 DTE/DCE interface is not ready for data transfers (bit 0, device-dependent status available, of the interrupt status byte is set).
- The V.35 DSR interface line is off (bit 0, device-dependent status available, of the interrupt status byte is set).
- The byte count in the DCB was specified as 0 (bit 3, DCB specification check, of the interrupt status byte is set).

Bits 0-7 of word 1 of the DCB can be used with the input flag bit to specify the idle detect time-out period.

Bits 8-15 of word 1 of the DCB can be used with the input flag bit to specify the nonproductive receive time-out period.

> **Note:** The input flag bit must be set to a 1 whenever data is to be cycle-stolen into the processor storage. Therefore, it must also be set to a 1 when either a Start Diagnostic or a Start Cycle Steal Status command is initiated in order to prevent a DCB specification check error interrupt from being presented.

There are two general types of errors: suppressible and nonsuppressible. Nonsuppressible errors always cause an exception interrupt request (CC2). The following errors are suppressible:

- Overrun
- Aborted frame
- Incorrect-length record
- Frame check sequence (FCS)

The action taken when a suppressible error occurs depends on the setting of the SE bit, which must be a 1 for receive mode. If the SE bit is a 1, the attachment posts the error in the residual status block and either presents a device end interrupt request (CC3) with interrupt information byte bit 0 set to 1, or chains to the next DCB.

Bit 3: This bit is not used and must be a 0.

Bit 4 - Suppress Exception (SE): This bit must be set to a 1 when a Receive command is specified. If not, an exception interrupt (CC2) is presented with bit 3 (DCB specification check) set in the interrupt status byte. The SE bit allows the attachment to suppress errors that could cause the next frame to be missed. The attachment stores the residual status block beginning at the status address specified in the DCB, when a suppressible error occurs (including short frame), or when the byte count equals 0 upon detection of the ending flag. For a frame whose length in bytes is equal to the byte count specified in the DCB, or for a short frame, the NE bit (residual status block word 1, bit 15) is be set on. In this case, the residual byte count in residual byte word 0 must be examined to determine the number of bytes received.

> **Note:** This attachment does not support SDLC/HDLC receive operations with the SE bit off. This is an exception to the SDLC description (refer to Chapter 4 of this document); however, it has no impact on existing SDLC/HDLC software.

The attachment handles the SE bit as shown in the following table:

Conditions	Results							
	Chn bit	SE bit	P/F bit	Int CC	IIB bit 0 *	Chain	Post resid. status	EOC bit **
No errors	0	1	0	3	0	no	yes	1
	0	1	1	3	0	no	yes	1
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	0	no	yes	1
	1	1	1	***	n/a	yes	yes	0
Suppressible errors	0	1	0	3	1	no	yes	1
	0	1	1	3	1	no	yes	1
	1	1	0	n/a	n/a	yes	yes	0
	1	1	1	3	1	no	yes	1
	1	1	1	***	n/a	yes	yes	0

* When condition code 2 is reported, the IIB is called the ISB and bit 0 has a different meaning. Refer to "Interrupt Status Byte" in this chapter for a description of the ISB bits.

** Refer to status address (DCB word 4) for a description of this bit.

***If the Pad/Control bit (bit 12 of the control word) is on during a receive operation, no interrupt (CC3) occurs, instead, chaining takes place.

As an example of SE bit usage, if a block check error occurs and the error can not be suppressed, an exception interrupt must be given with the BCC error reported via the cycle-steal status operation. This could cause the next frame to be missed if there is only one flag between frames. By using the SE bit, the attachment cycle-steals the residual status block into storage (which indicates that a BCC error occurred for that frame) while continuing to check the received data.

> **Note:** The SE bit is recognized only by the attachment in conjunction with a receive operation and is disregarded otherwise.

Bits 5 Through 7 - Cycle-Steal Address Key (KEY): This is a three-bit key presented to the processor by the attachment during data transfers so that the processor can ascertain whether the attachment is authorized to access certain blocks of processor storage.

Bit 8: This bit is not used and must be set to 0.

Bit 9 - NRZI Coding (NRZI): This bit causes the data to be transmitted according to NRZI encoding. When the internal clocking feature (local 1) is used, NRZI encoding is automatic and this bit is disregarded.

Bit 10 - Enable Terminal (ENB): This bit is used to set the X.21 interface to DTE ready. An interrupt or chain operation (if so specified by bit 0 of the control word) occurs after DCE ready state (1) is detected. This bit may be used with bits 0 through 7 of word 1 of the DCB to limit the time that the adapter waits for DCE ready to become active (27 seconds, maximum). Failure to get DCE ready within this time results in an exception interrupt with bit 0 (device-dependent status available) set in the interrupt status byte, and bit 4 (time-out) set in cycle steal status word 2. If timer 1 of the DCB is specified as 0, the attachment does not interrupt until 'DCE ready' is returned.

If the V.35 jumper plug is installed, the attachment checks for 'data set ready' (DSR).

Bit 11 - Disable Terminal (DSB): This bit causes the DTE (in X.21 mode) to assume DTE controlled not ready. An interrupt or chain operation (if so specified by bit 0 of the control word) begins immediately after the controlled not ready state is set.

This bit, if set on, causes an immediate device end interrupt if the V.35 jumper plug is installed.

This bit may be used in conjunction with bits 0 through 7 of word 1 of the DCB to limit the time the attachment waits for DCE ready to come active.

Failure to obtain DCE ready within the time limit setup results in an exception interrupt with bit 0 (device dependent status available) set in the interrupt status byte and bit 4 (time-out) set in cycle-steal status word 2. If timer 1 of the DCB is specified as 0, no time-out occurs.

Bit 12 - Pad/Control: If bit 14 of the control word is set to a 1 (transmit mode), bit 12 causes two pad characters (hex 55 or hex 00 if in NRZI mode) to be transmitted preceding the first flag of a frame sequence. If bit 2 of the control word is set to a 1 (receive mode), bit 12 prevents the attachment from breaking a chain operation (no interrupt) when the poll/final (P/F) bit is set to a 1.

Bit 13 - Secondary/Primary (S/P): This bit determines if the attachment operates as a secondary or a primary station. This bit is set to 1 for a primary station and to 0 for a secondary station. During a receive operation, the attachment examines the address portion of a received frame only if the attachment is being used as a secondary station. On a transmit operation, the attachment generates its own address only when it is operating as a secondary station.

Bit 14 - Transmit Operation (XMIT):

X.21 Leased

This operation causes the attachment to check that the DCE is ready (CCITT state 1). If the DCE is returning 'ready,' the attachment activates the control lead for at least 24 bit times prior to establishing synchronization, and cycle-steals data from processor storage. The data associated with the current DCB is transmitted as one frame.

An exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the interrupt status byte, and bit 7 (DCE interface error) set in the cycle-steal status word 2, if the DCE is not ready.

If a byte count of 0 is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the interrupt status byte.

A device end interrupt is presented when the byte count goes to 0 and the chaining flag is off. The C-line is deactivated for half duplex, but remains active for duplex operation.

V.35 Leased

This operation starts a timer (refer to bits 0-7 of word 1 of the DCB) and sends a 'request to send' (RTS) to the DCE. As soon as 'clear to send' (CTS) is returned from the DCE, the attachment establishes synchronization and cycle-steals data from processor storage.

An exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the interrupt status byte and bit 7 (DCE interface error) set in cycle-steal status word 2 if the 'data set ready' (DSR) line from the DCE is off. Failure to receive 'clear to send' (CTS) from the DCE within the time-out period results in an exception interrupt with bit 0 (device-dependent status available) set in the interrupt status byte and bit 7 (DCE interface error) set in cycle-steal status word 2.

Transmit mode is reset and 'request to send' (RTS) is dropped after the ending flag is transmitted. This occurs only if the chaining flag is off and hold line active (bit 15 set) is not specified.

A device end interrupt is presented when the byte count goes to 0 and the chaining flag is off.

If a byte count of 0 is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the interrupt status byte.

Hold Line Active (HLA): This bit is used in conjunction with bit 14 (transmit operation). If bit 15 is a 1 when the byte count goes to 0, the attachment stays in transmit mode and transmits flag characters until another operation begins or until the time specified in timer 2 elapses.

> **Note:** A value of 0 set into timer 2 causes the attachment to either hold the line active for 0-time or an indefinite time. The controlling parameter is if the attachment is operating in duplex; in this case, an indefinite HLA occurs.

Word 1 - Timers: This 16-bit word is used to specify time-out periods. The amount of time may be specified in increments of 106 milliseconds, with a maximum time-out period of 27 seconds.

Bits 0-7 Timer 1: In conjunction with receive (bit 2 of the control word set to 1), these bits are used to specify the idle detect time-out period. If chaining of receive DCB's is to take place, the timeout period must be specified in each DCB in order for the attachment to detect an idle condition after the first frame has been received. If the timeout period is selected as zero, the idle detect timer does not run, and therefore is not checked.

> **Note:** The idle detect time-out period is a specified period of time after which the receive line is checked for an idle condition (15 contiguous 1-bits).

In conjunction with enable terminal, these bits are used to specify the DCE ready time-out period. A timer value of zero causes the attachment to wait indefinately for the DCE to go ready. In V.35 mode, the attachment waits as above for data set ready to come active.

When the enable terminal, disable terminal, input flag, and transmit bits of the control word of the DCB are set to 0, timer 1 can be used by software as a timer. If the timeout period is selected as 0, or when the timeout period expires, a device end interrupt is presented, or a chaining operation continues (if specified).

In V.35 mode, timer 1 is used in conjunction with transmit to specify the clear-to-send time-out period.

Note: The clear-to-send time-out period is that period of time that the attachment allows for the return of clear-to-send on a transmit operation using the V.35 interface (DCE interface error, cycle-steal status word 2, bit 7, is set to a 1).

In conjunction with disable terminal, timer 1 is used to specify the time the attachment allows for the DCE to become ready. The interface is then set to DCE controlled not ready.

Bits 8-15 - Timer 2: In conjunction with receive (bit 2 of the control word set to 1), timer 2 is used to specify the non-productive receive time-out period. If chaining of receive DCB's is to take place, the time-out period must be specified in all of the DCB's in the chain. If the time-out period is specified as 0, the non-productive receive timer does not run, and therefore is not checked.

Note: The non-productive receive time-out period is that period of time after which the current receive operation is terminated if the signal on the line is unintelligible (no frames or flags).

In conjunction with hold line active, timer 2 is used to specify the amount of time that the line is held active. In half-duplex mode of operation, when the time-out period is selected as 0, the line is not held active. In full-duplex mode of operation, when the time-out period is selected as 0, the line is held active indefinately.

Word 2: This word is not used.

Word 3 - DCB ID: When PCI is specified, bits 0-7 of this word contain the DCB identifier.

Word 4 - Status Address: The status address word is used in conjunction with bit 4, suppress exception (SE), of the control word. Bit 4 of the control word and the status address are used only on receive operations. The address this word contains is the processor storage address of the residual status block. If bit 4 of the control word is a 1 and the attachment detects any of the conditions that set residual status flags, an exception-interrupt request does not occur. Instead, the attachment automatically stores two words of information into the residual status block and monitors the line, looking for an ending flag character. When the ending flag is detected, the attachment presents a normal device-end interrupt request or begins a chaining operation. The first word stored in the residual status block is the residual byte count; the second word contains the residual status flags.

Residual Status Flags: The second word of the residual status block contains the residual status flags. These bits have the following meanings:

Bit 0 - End Of Chain	This bit is associated with the permissive device end interrupt, that is, EOC will be set on when a frame having the P/F bit on is received and bit 12 of the control word is off. EOC is also on if chaining is not specified in the current DCB.
Bits 1 Through 7	These bits are not used and must be 0's.
Bit 8 - Overrun	This condition occurs during a receive operation.
Bit 9 - Abort	This condition occurs during a receive operation.
Bit 10 - Long Frame	This bit indicates that the byte count has been reduced to 0 and the current frame has not ended. The attachment continues to monitor the receive line until the end of the frame; however, any data received after the byte count reaches 0 is lost.
Bit 11 - Error	The frame check sequence received is incorrect.
Bits 12-14	These bits are not used and must be 0's.
Bit 15 - No Exception	This bit indicates either of two conditions. The first condition is that the frame is the correct length and error free; the second condition is that the attachment received an error free but short frame. To determine which condition caused this bit to be set, examine the residual byte count. If the residual byte count is not 0, a short frame was received.

Word 5 - Chaining Address: The chaining address word contains the storage address of the next DCB, and is used when chaining is indicated (bit 0 of the control word is a 1). The chain address must be even. If the address is odd, the attachment sets interrupt status byte bit 3 to a 1 and terminates the operation.

Word 6 - Byte Count: This 16-bit byte-count word contains the number of bytes to be transferred during the operation specified in the current DCB control word.

Word 7 - Data Address: This is the address in processor storage where data transfer starts.

Start Cycle Steal Status

The Start Cycle Steal Status command causes the attachment to transfer status information (about the previous cycle-steal operation) to the processor. The attachment provides four words of cycle-steal status information. The byte count specified in word 6 of the DCB must be 8.

IDCB (immediate device control block)

Command field	*Device address field*
0 1 1 1 1 1 1 1	0 X X X X X X X
0 — *7*	*8* — *15*
7F	00–FF

Immediate data field
DCB address
16 — *31*

The data address (word 7) must be on a word boundary (bit 15 set to 0) or an exception interrupt request (CC2) occurs with DCB specification check bit (bit 3) set to 1 in the interrupt status byte.

Refer to "Cycle-Steal Status Words" later in this chapter for a description of the status information.

This command initiates a cycle-steal operation to the addressed device to collect status information relative to the previous cycle-steal operation (not start cycle steal status). The word transferred from the data word position of the IDCB is the 16-bit logical storage address of the DCB.

When a cycle-steal data transfer is terminated by an exception condition (interrupt condition code 2), bit 0 of the interrupt status byte may be set on. If bit 0 is on, further device information regarding the cause of the exception condition may be found by executing a start cycle steal status (SCSS) command. This command may also be issued at any time to obtain information regarding logic card jumpers and DCE line status. The byte count for this operation must be 8 or 12 for SDLC/HDLC and the data address must be even.

The format of the start cycle-steal status DCB is as follows:

Word	*0 1 2 3 4 5 6 7 8*		*15*
0	0 0 1 0 0	K E Y	0's
1	Not used (0's)		
2	Not used (0's)		
3	Not used (0's)		
4	Not used (0's)		
5	Not used (0's)		
6	Byte count		
7	Data address (even)		

Cycle-Steal Status Words

Word 0: Word 0 contains the processor storage address of the last attempted cycle-steal transfer. This residual address may be a data address, DCB address, or status address. The following table shows the type of address that the residual address can be for various error conditions. Where more than one possibility is shown, the program must decide which type of address cycle-steal status word 0 contains.

Error condition	Residual address		
	DCB address	Status address	Data address
Delayed command reject	N/A	N/A	N/A
DCB specification check	X		
Storage data check	X		X
Invalid storage address	X	X	X
Protect check	X	X	X
Interface data check	X	X	X
Overrun		X	X
Time-out	X		X
Modem interface error	X		X
Block check error	X		X
Abort		X	X
Idle or inactivity detected	X		X
Nonproductive receive	X		X

Word 1: Word 1 contains the residual byte count. This is the byte count remaining when an operation ends.

Word 2: With an exception interrupt request (CC2) and an interrupt status byte of hex 80, issuing a Start Cycle Steal Status command is recommended to further define an error. This section describes the required error analysis and recommended action.

Bit 0 - Overrun: During a receive operation, overrun occurs if the receive buffer (attachment hardware) is not read within 16 bit times since it was last read (excluding 0-bit deletion).

During a transmit operation, the transmit buffer was not reloaded within 16 bit times since it was last filed (excluding 0-bit insertion).

Bit 1 - Abort: While receiving a frame, seven consecutive 1-bits (no 0-bit insertion) were received after at least one byte of data had already been cycle-stolen into storage. If no bytes of data have been stored, the abort condition is ignored and the attachment continues to monitor the receive line for a flag or an idle condition.

Bit 2 - Long Frame: This bit indicates that the byte count has been decremented to 0 and the current frame being received has not ended.

Bit 3 - Block Check Error (BCC or FCS) The frame check sequence (block check character; 16-bits) computed from the received data does not equal hex F0B8.

Bit 4 - Time-Out: This bit is set on to indicate that one of the time-outs has occurred. Only one time-out may occur for any operation.

Refer to "word 5" for an indication of the DTE and DCE lines that were active when the time-out occurred.

In V.35 mode, DSR was not returned by the DCE after an enable operation.

Bit 5 - Idle Detect: This condition occurs during a receive operation after the idle detect time-out period has exhausted and 15 consecutive 1-bits (no 0-bit insertion) have been detected.

> **Note:** The attachment does not look for an idle condition if the idle detect time-out period was specified as 0.

Bit 6 - Nonproductive Receive: This bit is set on if the attachment has been receiving bits that do not result in flags or frames, for a period longer than that specified in bits 8-15 (timer 2) of word 1 of the DCB.

> **Note:** The attachment does not look for a nonproductive receive condition if the nonproductive receive time-out period was specified as 0.

Bit 7 - DCE Interface Error: In X.21 leased-line mode, the DCE went to DCE not ready during a transmit or receive operation.

In V.35 mode 'clear to send' (CTS) was not returned from the DCE after setting 'request to send' (RTS).

Bits 8-12: These bits are not used and must be 0's.

Bit 13 - Local Attach 1: This bit indicates that the local attach 1 jumper is installed in the cable. The attachment provides clocking at 9600 bps in SDLC/HDLC mode only. The clocking signal is not provided to the remote terminal.

Bits 14-15: These bits are not used and must be 0's.

Word 3

Bit 0 - Data Terminal Ready (DTR): This bit is a 1 if DTR is active.

Bit 1 - Data Set Ready (DSR): This bit is a 1 if DSR is active.

Bit 2 - Request To Send (RTS): This bit is a 1 if RTS is active.

Bit 3 - Clear To Send (CTS): This bit is a 1 if CTS is active.

> **Note:** Bits 0-3 have no meaning on an X.21 network. Therefore, for software compatibility, these bits have the following meaning:

Bit		0	1	2	3
SCSS following	Enable normal	on	on	off	off
	Enable error	on	off	off	off
	Disable normal	off	off	off	off
	Disable error	off	off	off	off
	Transmit normal	on	on	on	on
	Transmit error	on	on	off	off
	Receive normal	on	on	off	off
	Receive error	on	off	off	off

Bits 4-5: These bits are not used and must be 0's.

Bit 6 - Transmit Mode: This bit, when a 1, indicates the attachment is in transmit mode.

Bit 7: This bit is not used and must be a 0.

Bits 8-15 - Secondary Station Address: These bits represent the address of the secondary station.

Word 4

Bits 0-9: These bits are not used and must be 0's.

Bit 10 - V.35: When this bit is a 1, it indicates that the attachment is jumpered for V.35 operation.

Bit 11: This bit is not used and must be 0.

Bit 12 - Local Attach 2: When this bit is a 1, it indicates that the attachment is jumpered for local attach 2. The attachment provides clocking at 48000 bps in either SDLC/HDLC or BSC mode. The clocking information is available to the remote terminal via a customer supplied cable.

Bit 13: This bit is not used and must be a 0.

Bit 14 - IPL: When this bit is a 1, it indicates that the allow IPL jumper is installed.

Bit 15 - BSC: When this bit is a 1, it indicates that the bisynchronous mode jumper is installed.

Word 5

Bits 0-7: These bits are not used and must be 0's.

Bit 8 - Transmit: This bit represents the state of the X.21 interface 'transmit' line.

Bit 9 - Receive: This bit represents the state of the X.21 interface 'receive' line.

Bit 10 - Indicate: This bit represents the state of the X.21 interface 'indicate' line.

Bit 11 - Control: This bit represents the state of the X.21 interface 'control' line.

Bits 12-15: These bits are not used and must be 0's.

> **Note:** Local 1 and local 2, when both jumpered, indicates the attachment is operating as a local 2 multi-point master. If a station address is also jumpered on the attachment, the attachment is operating as a local 2 multi-point slave.

Binary Synchronous Communication (BSC)

The binary synchronous communications (BSC) protocol is supported by the attachment to assist in future migration of the user to SDLC/HDLC protocol.

The binary synchronous communication (BSC) capability allows transfer of serial data to and from a remote terminal or host system via a DCE and leased communication line facility. The BSC function can be used for connecting a Series/1 processor to telecommunication equipment or other processors having compatible adapters. The BSC capability supports:

- Data transmission rates up to 56000 bps

  Note: Due to post and pre-processing delays in the attachment, the sustained data throughput when running at data transmission speeds of 48000 and 56000 bps is considerably less than the clocking rate. Depending on message size, the maximum throughput at 48000 and 56000 bps transmission speeds is 15000 bps.
- Supports EBCDIC or ASCII code.
- May be used as multipoint master or multi-point control or station on leased-line.
- Line error checking is provided for both EBCDIC and ASCII modes of transmission

At the beginning of a transmission and periodically during the transmission, the transmitting station inserts sync patterns (SYNs) into the stream of binary digits.

Binary synchronous communications can use either Extended Binary-Coded Decimal Interchange Code (EBCDIC) or American Standard Code for Information Interchange (ASCII) transmission codes. Selection of codes is controlled by the program. If the program does not specify ASCII code, the attachment automatically selects EBCDIC code.

For information on the BSC mode of operation, refer to *General Information - Binary Synchronous Operation*, GA27-3004.

Operating Modes

The attachment has several operating modes that are selected by control characters:

- Text
- Transparent text
- Control
- Selected
- Passive
- IPL
- Transmit
- Receive

Text Mode

Text mode is selected when the first start-of-heading (SOH) or start-of-text (STX) control character is decoded. Subsequent SOH and STX characters are treated as data characters. During text mode, the attachment processes header or text characters and accumulates a block check character (BCC). Synchronization (SYN) characters and the first SOH or STX characters decoded are not included in the BCC accumulation. Text mode is terminated after an end-of-text (ETX) or end-of-transmission-block (ETB) character is decoded by the attachment.

Transparent Text Mode

Transparent text mode is selected when a 'data-link-escape' (DLE) STX sequence is decoded during a transmit or receive operation. While in this mode, any kind of binary data can be transmitted or received. The following changes from text mode occur:

- The attachment recognizes individual control characters or control sequences, such as ETB, STX, and enquiry (ENQ), only as data, with no other associated function.
- All inserted SYN characters are preceded automatically by a DLE character (DLE-SYN).
- A second DLE is attached automatically to every data DLE to distinguish it as a DLE control character, rather than data. This second DLE and the inserted DLE-SYNs are deleted automatically upon reception and do not enter processor storage.

To exit transparent text mode, one of the following ending sequences is required:

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

These sequences must be transmitted by using the exit transparent operation. Refer to "Device Control Block (DCB)" later in this chapter. In transparent text mode, the transmitting attachment automatically inserts a second DLE between the first DLE and the ETX, ETB, ENQ, or ITB. The receiving station discards the first DLE. The inserted DLE and the ETX, ETB, ENQ, or ITB are considered as two data characters and placed in storage. The exit transparent operation prevents the attachment from inserting a second DLE. The receiving station recognizes the ending sequences as ending sequences, not data. Because the DLEs in these ending sequences are true DLEs and are not placed in storage at the receiver, they should not be included in the byte count for the receiving station.

Only DLE-ITB leaves the attachment in text mode; all others cause a change of direction (COD).

During transparent text mode, a BCC is accumulated as in normal text mode. The only DLE characters included in the BCC are the data DLEs.

Control Mode

In a multi-point configuration, when the attachment receives a valid EOT sequence, it enters control mode. While in control mode, the attachment monitors for its station address. If the attachment does not enter selected mode and detects an address sequence other than its own, character synchronization is reset.

Selected Mode

The attachment enters selected mode when it decodes its own station address twice (contiguously) after establishing byte synchronization. If a receive operation has been initiated, the message sequence, starting with the second station address character, is transferred to storage.

Notes:

1. The attachment's station-address (used in multi-point configuration only) is determined by discrete jumpers on the feature card.
2. BSC control characters may not be used as an address.
3. EBCDIC bit 2 or the ASCII bit 6 of the station address is not used by the hardware.
4. The program may use these bits to differentiate between a polling and a selecting sequence.
5. Multi-point address bit 0 must not be jumpered on when using ASCII.

Passive Mode

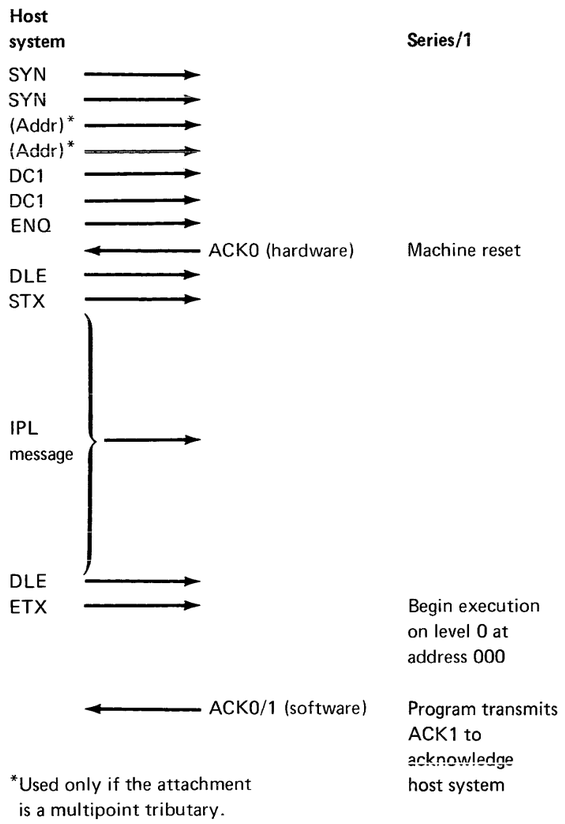
The attachment in a multi-point network is in passive mode when it is not in selected or in control mode. Passive mode is entered when the attachment is powered on. The attachment enters other modes, depending upon the characters received on the line as previously described.

IPL Mode

Initial program load (IPL) by a host system may be accomplished through the attachment using EBCDIC characters only. A jumper must be installed on the feature card to allow the attachment to IPL the processor.

If an IPL sequence (DC1-DC1-ENQ) is received, the attachment hardware responds with an EBCDIC acknowledgment (ACK0) after a 50-millisecond delay.

If the attachment is a multi-point tributary station, its address must be included in the IPL sequence, as shown in the following example. (It must also have been placed in control mode as described earlier.)



*Used only if the attachment is a multipoint tributary.

The host must then transmit DLE-STX (to enter transparent text mode) followed by the IPL program. This sequence (DLE-STX) is not checked by the attachment for validity and is not placed into storage. The attachment enters transparent text mode and places all following data into storage beginning at location 0000.

Upon receiving a DLE-ETX followed by a valid BCC, the attachment presents a device-end interrupt request, on level 0, with the device address in register 7. The IPLed program must handle this interrupt request. The program must also transmit a positive acknowlegement back to the host system.

If the IPL operation is unsuccessful, the attachment holds the processor in IPL mode (the Load light is on) and monitors the line for a retry of the IPL operation.

Note: The maximum number of bytes that can be loaded by the host IPL program using the BSC mode is 65,535; however, the quality of the transmission line must be considered when transmitting 65,535 bytes.

Transmit Mode

Transmission data is fetched from storage two characters at a time (except as noted previously). The high-order byte holds the first character to be sent and the low-order byte holds the next character. After a character has been transferred into the SERDES (serializer/deserializer), it is transmitted over the line, low order bit first.

ASCII characters in storage are eight bits in length; seven data bits plus one parity bit. This parity bit should not be confused with the parity bit in storage. The ASCII parity bit is bit 0 in a byte of storage.

The attachment does not check the ASCII parity during transmit operations; therefore, the program must maintain odd parity in storage when transmitting the data.

Programming Consideration: The BSC protocol as implemented has the restriction that the data block size on transmit and receive operations must not exceed 2000 bytes when the data rate is over 19200 bps.

Note: Link data transmission speeds over 19200 bps result in a through-put of approximately 15000 bps.

Receive Mode

The first bit received is transferred into the low-order bit position of a byte. The second bit received is transferred into the next higher bit position, and so on until a character is assembled. When two characters are to be transferred to storage, the first character received is loaded into the high-order byte of the storage data register and the next character is loaded into the low-order byte before the data is transferred to storage. Data is written into storage without any code translation.

Transmission Codes

The BSC mode allows data communication using EBCDIC or ASCII line codes. ASCII can be specified by the program after the IPL. The attachment establishes EBCDIC if:

- No code is specified
- A power-on reset occurs
- A system reset occurs

Control Characters

Note: For detailed information about BSC line control, refer to *General Information-Binary Synchronous Communications*, GA27-3004.

Name	Abbr	EBCDIC	ASCII
Start of heading	SOH	SOH	SOH
Start of text	STX	STX	STX
End of transmission block (Note 1)	ETB	ETB	ETB
End of text (Note 1)	ETX	ETX	ETX
End of transmission (Note 1)	EOT	EOT	EOT
Enquiry (Note 1)	ENQ	ENQ	ENQ
Negative acknowledge (Note 1)	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Immediate block character	ITB	IUS	US
Initial program load (Notes 2 and 3)	IPL	DC1 DC1 ENQ	
Even acknowledge (Note 1)	ACK0	DLE(70)	DLE 0
Odd acknolwedge	ACK1	DLE/	DLE 1
Wait before transmit-positive acknolwedge (Note 1)	WACK	DLE ,	DLE ;
Mandatory disconnect Note 1)	DISC	DLE EOT	DLE EOT
Reverse interrupt (Note 1)	RVI	DLE @	DLE <
Temporary text delay	TTD	STX ENQ	STX ENQ
Transparent start of text (Note 4)	XSTX	DLE STX	
Transparent intermediate block block (Note 4)	XITB	DLE IUS	
Transparent end of text (Note 4)	XETX	DLE ETX	
Transparent end of transmission block (Note 4)	XETB	DLE ETB	
Transparent synchronous idle (Note 4)	XSYN	DLE SYN	
Transparent block cancel (Note 4)	XENQ	DLE ENQ	
Transparent TTD (Note 4)	XTTD	DLE STX DLE ENQ	
Data DLE in transparent mode (Note 4)	SDLE	DLE DLE	

Notes:

1. These control characters and sequences cause a change-of-direction (COD) interrupt request after the required action has been completed.
2. Not applicable in ASCII format.
3. In general use as IPL sequence.
4. Transparent mode is not available in ASCII.

The functions of the control characters are as follows:

Mnemonic	*Function*
ACK0	Indicates affirmative acknowlegement of even blocks.
ACK1	Indicates affirmative acknowlegement of odd blocks.
DISC	Used only on switched communication facilities to initiate a disconnect.
DLE	Alert the attachment to test the next character for a defined control sequence in transparent text mode. In text mode, DLE is treated as data.
ENQ	Resets text mode without BCC transmission and comparison.
EOT	End of transmission.
ETB or ETX	Resets text mode with BCC comparison.
IPL	Control characters to initiate an IPL sequence.
ITB	Included in the BCC; it causes the BCC to be sent.
NAK	Negative response to a request for a reply, or to a block of heading or a block of text in error.
RVI	Reverses direction of data transfer.
SOH or STX	Resets control mode and sets the attachment to text mode. BCC accumulation starts with the first character after the first SOH or STX character is transmitted/received.
SYN	Transmitted automatically by the attachment to establish and maintain synchronization.
TTD	Alerts the receiving station of a temporary text delay.
WACK	Indicates a temporary not-ready-to-continue (or not-ready-to-receive) condition.
XDLE	In transparent text mode, the transmitter adds a second DLE after each data DLE. At the receiver, the first DLE is removed and does not enter storage or the BCC.
XENQ	Turns off transparent text mode and cancels the current block of data.
XETX/XETB	Same as ETB or ETX, but turns off transparent text mode.
XITB	Same as ITB, but turns off transparent text mode.
XSTX	Turns off control mode and sets the attachment to transparent text mode.
XSYN	Transmitted automatically by the attachment to establish and maintain synchronization in transparent text mode.
XTTD	Alerts the receiving station to a temporary text delay in transparent text mode.

Line Error Checking

Two different types of checking are employed, depending on the code selected. Cyclic redundancy check (CRC) is used with EBCDIC and longitudinal redundancy and vertical redundancy checking (LRC/VRC) is used with ASCII.

Error correction is accomplished by retransmitting the data block that was in error.

Synchronization And Timing

The attachment receives strobe pulses from the DCE; these pulses establish and maintain bit synchronization. A specific series of characters precedes each transmission in order to establish character synchronization.

Transmit Synchronization

The attachment automatically begins transmission with a leading pad character (hex 55) followed by the initial synchronizing pattern of two SYN characters. If internal clocking is being used, the attachment transmits two leading pad characters.

SYN Insertion: To maintain synchronization, the attachment inserts a synchronization pattern of SYN-SYN at one-second intervals (approximately). In transparent text mode, this synchronization pattern is DLE-SYN. These characters are also inserted as time-fill characters when the attachment is not transmitting such as when it is fetching a new device control block (DCB) during a chaining operation.

SYN Deletion: SYN characters or transparent SYN characters are deleted and not placed in storage.

Trailing Pad Characters: The attachment automatically transmits a trailing pad character (hex FF) after every COD character or after the BCC if the change of direction calls for BCC. This ensures that the last character sent (COD or BCC) goes online in its entirety. A pad of hexadecimal FF also provides the second character of the NAK and EOT control character sequences. The attachment does not begin an interrupt request or chaining operation until the entire pad character is transmitted.

SYN and pad characters (leading and trailing) are provided by the attachment and are not stored into processor storage.

Receive Synchronization

Character phase synchronization is established when two consecutive SYN characters followed by any non-SYN character are received and decoded. Character phase is maintained because the transmit station periodically inserts a synchronization pattern into the data stream.

SYN and pad characters are deleted by the attachment and are not stored in processor storage.

Time-Outs

The following is a list of the possible time-outs while in the BSC mode of operation:

- *Character synchronization time-out.* The period of time the attachment waits for character phase to be established after initiating a receive operation.
- *Continuous synchronization time-out.* A continuous synchronization pattern or transparent synchronization idle (in transparent mode) is received while in character phase.
- *Synchronization loss time-out.* While receiving data, no synchronization pattern or transparent synchronization idle is received.
- *DCE not ready time-out.* Bit 12 of the control word is used to limit the time (maximum of 3 seconds) the attachment will wait for DCE ready to become active.
- *Programmable time-out.* Used by the software for timing purposes when the operation specified in the DCB is not transmit, receive, enable, or disable terminal. A 2-second time-out is active.
- *Clear-To-Send (CTS) time-out.* The period of time the attachment allows for the return of CTS on a transmit operation. Using the V.35 interface, DCE interface error, cycle-steal status word 1, bit 2, is on.

BSC Commands

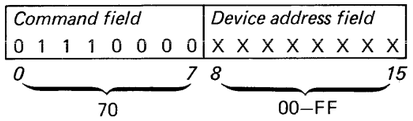
- Start
- Start Cycle Steal Status

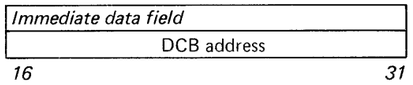
It is the programmer's responsibility to ensure that the program always tests the Operate I/O condition codes following an Operate I/O instruction.

Start

The Start command initiates a cycle-steal operation for the addressed device. The format of the IDCB for the Start command is:

IDCB (immediate device control block)





BSC Device Control Block (DCB)

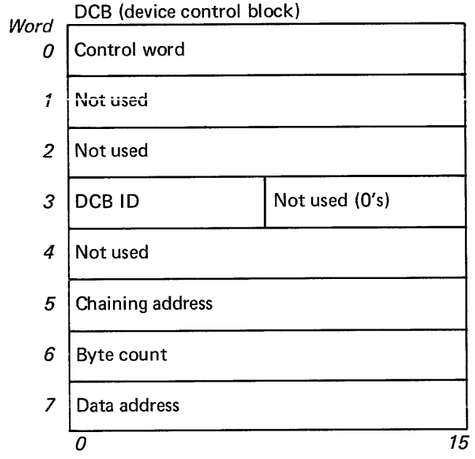
The DCB is an eight-word area in processor storage that describes the specific parameters of the cycle-stealing operation. Its location in storage is assigned by the program. The data in its words is loaded and changed by the program. It is fetched by the attachment, using a cycle-steal address key of 000 after successful execution of a Start command.

The DCB address transferred to the attachment via the IDCB points to word 0. The table is in an ascending storage address order with the lowest storage address at the top of the table.

> **Note:** The address of the DCB in processor storage must be even. If the address is odd, the attachment presents an exception interrupt (CC2), with bit 1 (delayed command reject) set in the interrupt status byte, and terminates the cycle-steal operation.

The format of the BSC DCB is as follows:

DCB (device control block)



Word 0 - Control Word: Control word 0 defines the operation to be performed. The format of the control word is as follows:

Bit 0 - Chaining Flag: If this bit is a 1, the next DCB in the chain is fetched after the successful completion of the current DCB operation. If this bit is a 0 and the operation is successfully completed, the attachment presents a device end interrupt.

Bit 1 - Program Controlled Interrupt (PCI): This bit causes the attachment to present a PCI at the completion of the DCB fetch. The data transfer associated with the DCB may commence even though the PCI may be pending in the attachment. When this bit is set to a 1, bits 0-7 of DCB word 3 are placed in the IIB upon interrupt presentation.

This bit is recognized only during a transmit or receive operation. A DCB specification check (bit 3 of the interrupt status byte) is presented if this bit is set on any other command.

In order to use the PCI, a set mode DCB must have previously been issued with bit 11 set on in word 1. If the set mode was not issued, this bit is not examined by the attachment.

Bit 2 - Input Flag: If this bit is a 1, it allows the attachment to cycle-steal data into processor storage once byte synchronization is established. A device end interrupt is presented when a change of direction (COD) is received.

If the byte count in the DCB was specified as 0, an exception interrupt is presented with bit 3 (DCB specification check) set in the interrupt status byte (ISB).

This bit may be used with bit 12 to limit the time that the attachment allows to establish character phasing. Failure to establish character phase within 3 seconds results in an exception interrupt with bit 0 (device dependent status available) set in the interrupt status byte and bit 1 (time-out) set in cycle-steal status word 1.

If the attachment is jumpered to operate with the V.35 interface, an exception interrupt occurs with bit 0 (device-dependent status available) set in the interrupt status byte and bit 2 (DCE interface error) set in cycle-steal status word 1, if the 'data set ready' line from the DCE is off.

Bit 3: This bit is not used and must be set to 0.

Bit 4: This bit is not used and must be set to 0.

Bits 5-7 - Cycle-Steal Address Key: These bits represent a three-bit key to be presented by the attachment during data transfers.

Bit 8: This bit is not used and must be set to 0.

Bit 9 - Set ASCII Mode: This bit sets up the attachment to allow communications using ASCII code. If this bit is a 0, it causes the attachment to recognize EBCDIC code.

Bit 10 - Enable Terminal: This bit sets the X.21 interface to DTE ready. An interrupt or chaining operation (if so specified by bit 0 of the control word) occurs after DCE ready (CCITT state 1) is detected. Bit 12 of the control word (start timer) may be used to limit (to 3 seconds) the time that the attachment waits for DCE ready to become active. Failure to receive DCE ready within this time results in an exception interrupt with bit 0 (device dependent status available) set in the interrupt status byte and bit 1 (time-out) set in cycle-steal status word 1. If the start timer bit is off, an enable with no time-out occurs.

If the V.35 jumper plug is installed, the attachment checks for 'data set ready'. Subsequent action taken is as described above for X.21 mode.

Bit 11 - Disable Terminal: This bit, when set with the attachment in X.21 mode, causes the DTE to assume DTE controlled not ready. An interrupt or chaining operation (if so specified by bit 0 of the control word) begins immediately after the controlled not ready state is set.

If the V.35 jumper plug is installed, the attachment causes an immediate device end interrupt.

This bit may be used with bit 12 of word 0 of the DCB to limit the time the adapter waits for DCE ready to become active. The time-out period is 3 seconds.

Failure to receive DCE ready within this time results in an exception interrupt being presented with bit 0 (device dependent status available) set in the interrupt status byte and bit 4 (time-out) set in cycle-steal status word 2.

Bit 12 - Start Timer: This bit is used with bits 2, 10 or 11 to provide a 3-second timeout. In the absence of bits 2, 10, and 11 of the control word, this bit provides a timer for software. In this case, a 2-second timeout occurs. The attachment presents a device end interrupt at the completion of this period.

Bit 13 - Transmit:

X.21 Leased

This operation causes the attachment to check that the DCE does not indicate DCE not ready. If DCE not ready is *not* active, the attachment activates the control lead for at least 24 bit times before establishing synchronization and cycle-steals data from processor storage.

If DCE not ready is active, an exception interrupt occurs immediately, with bit 0 (device-dependent status available) set in the interrupt status byte and bit 2 (DCE interface error) set in cycle-steal status word 1.

When the byte count goes to 0 and a change-of-direction (COD) character is detected, a device end interrupt is presented.

If the byte count goes to 0, the chaining bit is off, and no COD is sent, an exception interrupt is presented with bit 2 (ILR) set in the interrupt status byte (ISB).

If a COD character is detected prior to the byte count going to 0, an exception interrupt is presented with bits 0 and 2 (short record) set in the interrupt status byte (ISB).

If a byte count of 0 is specified in the DCB, an exception interrupt is presented with bit 3 (DCB specification check) set in the interrupt status byte (ISB).

Note: At data rates over 19200 bps, an ITB character is not supported unless it occurs on a DCB boundary. For example, the ITB character must be the last byte in the data buffer associated with a transmit DCB.

V.35 Leased

This operation starts a 3-second timer and turns on 'request to send' to the DCE. As soon as 'clear to send' is returned from the DCE, the attachment establishes synchronization and cycle-steals data from processor storage.

An exception interrupt occurs immediately, with bit 0 (device-dependent status available) set on in the interrupt status byte and bit 2 (DCE interface error) set in cycle-steal status word 1, if the data set ready line from the DCE is off.

Failure to receive 'clear to send' from the DCE within the 3-second time-out period results in an exception interrupt with bit 0 (device-dependent status available) set in the interrupt status byte and bit 2 (DCE interface error) set in cycle-steal status word 1.

Transmit mode is reset and 'request to send' to the DCE is dropped after the pad character is sent following a change-of-direction (COD) control character or a block control character (BCC), if required.

Bit 14 - Exit Transparent: This bit allows transmission of control sequences while in transparent text mode. It should be set on in the final DCB used for a transmit transparent text operation. The attachment does not transmit a delimiting DLE, nor does it accumulate the single DLE in the BCC. Bit 14 should only be used in a DCB following a block of transparent text.

When this bit is specified, the byte count must be equal to 2 or a DCB specification check (interrupt status byte, bit 3) is reported.

Bit 15: This bit is not used and must be 0.

Word 1: This word is not used and must be set to 0's.

Word 2: This word is not used and must be set to 0's.

Word 3 - DCB ID: When PCI is specified, bits 0-7 of this word contain the DCB identifier.

Word 4: This word is not used and must be set to 0's.

Word 5 - Chaining Address: The chaining address word contains the storage address of the next DCB and is used when chaining is indicated. The chaining address must be even. If it is odd, the attachment sets interrupt status byte bit 3 to a 1 and terminates the operation.

Word 6 - Byte Count: The byte count word contains the number of bytes to be transferred to or from storage.

The byte count in the DCB (word 6) must be equal to 6 or 10, and the data address (word 7) must be on a word boundary (bit 15 off) or an exception interrupt request (CC2) occurs with DCB specification check bit (bit 3) set to a 1 in the interrupt status byte. The BSC protocol as implemented has the restriction that the data block size on transmit and receive operations must not exceed 2000 bytes when the data rate is over 19200 bps.

Word 7 - Data Address: The data address is the address in processor storage where data transfer is to start.

Start Cycle Steal Status

The Start Cycle Steal Status command causes the device to initiate a cycle-steal operation to collect status information about the previous cycle-steal operation. The format of the IDCB for this command is as follows:

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	1	1	1	1	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
7F								00—FF							

Immediate data field
DCB address
16 *31*

The byte count in the DCB (word 6) must be equal to 6 or 10, and the data address (word 7) must be on a word boundary (bit 15 off) or an exception interrupt request (CC2) occurs with DCB specification check bit (bit 3) set to a 1 in the interrupt status byte.

Cycle-Steal Status Words

Five words of status information are available by using the Start Cycle Steal Status (SCSS) command.

Word 0: Word 0 contains the processor storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Word 1: Word 1 has the following format:

Bit 0 - Overrun: During a receive operation, overrun occurs if the receive buffer (attachment hardware) is not read by the attachment within 16 bit times since it was last read.

During a transmit operation, overrun occurs if the transmit buffer is not reloaded within 16 bit times since it was last filled.

Bit 1 - Time-Out: This bit is a 1 if any of the following conditions exist:

- In X.21 mode, DCE ready is not received from the DCE within 3 seconds after an enable terminal operation begins.

- In V.35 mode, DSR is not received from the DCE within 3 seconds after an enable terminal operation begins (if bit 12 of DCB word 0 is a 1).
- Character phase is not established within 3 seconds of acceptance of a receive operation (if bit 12 of DCB word 0 is a 1).
- A continuous synchronization pattern is received for 3 seconds.
- While receiving data, no synchronization pattern is received for a period of 3 seconds.

Bit 2 - DCE Interface Error: This bit is set to a 1 if any of the following conditions exist:

- The DCE went to DCE not ready during a transmit or receive operation.
- In V.35 mode, CTS was not returned from the DCE after setting RTS.

Bit 3 - Block Check Error: This bit is set to 1 if the block check character (BCC) received over the data link does not compare with the BCC accumulated. In ASCII mode, an LRC or VRC error is indicated.

Data transfer to processor storage ceases upon detection of an ASCII VRC (even parity) error, or in EBCDIC, following a BCC error after an ITB character.

> **Note:** A 1-second delay occurs before presentation of the error interrupt. This is to reduce the probability of the transmit station still passing data should the receive station reply with an immediate negative acknowlegement.

Bit 4 - Multi-Point Transmit Error: This bit is set to 1 if a transmit operation was attempted before being selected when the attachment is a tributary on a multi-point network.

Bit 5: This bit is not used and must be set to 0.

Bit 6 - Multi-point Tributary: This bit is set to 1 if the attachment is a multi-point tributary terminal.

Bit 7 - Improper Configuration: If this bit is set to 1, the attachment is configured improperly.

Bits 8-15 - Multi-point Address: The address for which the attachment is jumpered is presented in this byte. The BSC station address (used in multi-point configuration only) is determined by discrete jumpers on the attachment card. Control characters may not be used as an address. The EBCDIC 2-bit or the ASCII 6-bit of the station address is not used by the hardware. For example, the BSC recognizes either BB or SS as a valid EBCDIC address sequence. The program, however, may use these bits to differentiate between a polling and a selection sequence.

> **Note:** The attachment uses the multi-point address jumpers to indicate multi-point tributary. For example, any jumper set on in the multi-point address field causes the attachment to react as a multi-point tributary. Therefore, hex 00 is an invalid multi-point address.

Word 2

Bit 0 - Data Terminal Ready (DTR): This bit is a 1 if DTR is active.

Bit 1 - Data Set Ready (DSR): This bit is a 1 if DSR is active.

Bit 2 - Request To Send (RTS): This bit is a 1 if RTS is active.

Bit 3 - Clear To Send (CTS): This bit is a 1 if CTS is active.

> **Note:** Bits 0-3 have no meaning on an X.21 network. Therefore, for software compatability, these bits have the following meaning:

Bit		0	1	2	3
SCSS following	Enable normal	on	on	off	off
	Enable error	on	off	off	off
	Disable normal	off	off	off	off
	Disable error	off	off	off	off
	Transmit normal	on	on	on	on
	Transmit error	on	on	on	off
	Receive normal	on	on	off	off
	Receive error	on	off	off	off

Bits 4-5: These bits are not used and must be 0's.

Bit 6 - Transmit Mode: If this bit is a 1, it indicates that the attachment is in transmit mode.

Bit 7: This bit is not used and must be 0.

Bits 8-15: These bits indicate the current setting of the communications indicator panel DISPLAY/FUNCTION SELECT switches (if installed); the bits are 0's if the communications indicator panel is not installed.

Word 3

Bits 0-9: These bits are not used and must be 0's.

Bit 10 - V.35: If this bit is a 1, it indicates that the attachment is jumpered for V.35 operation.

Bit 11: This bit is not used and must be 0.

Bit 12 - Local Attach 2: If this bit is a 1, it indicates that the attachment is jumpered for local attach 2. The attachment provides clocking at 48000 bps in either SDLC/HDLC or BSC mode. The clocking information is available to the remote terminal via a customer supplied cable.

Bit 13: This bit is not used and must be 0.

Bit 14 - IPL: If this bit is a 1, it indicates that the allow IPL jumper is installed.

Bit 15 - BSC: If this bit is a 1, it indicates that the bisynchronous mode jumper is installed.

Word 4

Bits 0-7: These bits reflect the X.21 interface state.

Bit 8 - Transmit: This bit reflects the state of the X.21 interface 'transmit' line.

Bit 9 - Receive: This bit reflects the state of the X.21 interface 'receive' line.

Bit 10 - Indicate: This bit reflects the state of the X.21 interface 'indicate' line.

Bit 11 - Control: This bit reflects the state of the X.21 interface 'control' line.

Bits 12-15: These bits are not used and must be 0's.

Status

Interrupt Information Byte (IIB)

When the attachment presents an interrupt request to the processor, the interrupt information byte is used to record information that cannot be indicated to the program by the condition codes. If the interrupt information byte bit 0 is a 1 when condition code 3 is reported, the SE bit was equal to 1 for the previous receive operation and a suppressible error was suppressed. When interrupt condition code 2 is reported, the interrupt information byte has a fixed format called the interrupt status byte.

Interrupt Status Byte (ISB)

When the attachment presents an interrupt request to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by condition codes. The interrupt status byte is meaningful only when interrupt condition code 2 is reported. The processor detects the interrupt status byte in bits 0-7 of the interrupt ID word.

Definitions of the interrupt status byte bits are as follows:

Bit 0 - Device-Dependent Status Available: If this bit is a 1, additional status is available by using the Start Cycle Steal Status command. This bit may be a 1 in conjunction with bit 2 (incorrect-length record).

Bit 1 - Delayed Command Reject: This bit is a 1 for the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The IDCB contains an odd DCB address.
- A command was issued to the wrong device.

Bit 2 - Incorrect-Length Record: This error can occur during both transmit and receive operations. It is caused by either of the following conditions:

- The byte count has been decremented to 0, the attachment has not detected a COD character, and the chaining flag is off.
- The attachment has detected a COD character and the byte count has not been decremented to 0.

In this case, interrupt status byte bit 0 is also a 1. A Start Cycle Steal Status command can be used to determine the location of the COD in storage (residual address).

Bit 3 - DCB Specification Check: This bit is set to a 1 if any of the following conditions exist when the DCB is examined:

- There is an odd byte chaining address with the chain bit set to a 1 in the control word.
- There is an odd byte data address for a Start Cycle Steal Status command.
- There is an odd byte data address for a Start Diagnostic command.
- The byte count is not hexidecimal 11 for a Start Diagnostic 1 command.
- The byte count is not 2 for a Start Diagnostic 2 command.
- The byte count is 0 for a receive operation.
- The byte count is 0 for a transmit operation.
- The input flag I/F bit of the control word was not on for a Start Diagnostic or a Start Cycle Steal Status command.
- More than one of the following operations was specified in the control word at the same time: receive, transmit, disable terminal, and enable terminal.
- A Start command was issued to the wrong device.
- The BSC byte count does not equal 6 or 10 for a Start Cycle Steal Status command.
- A DCB other than a transmit or receive with the PCI bit on in the control word was issued.
- A set mode DCB specifying duplex when the BSC jumper is on was issued.
- A set mode DCB specifying installation test (bit 13 on in word 1 of the DCB) was turned on while any other bit in word 1 of the DCB is on.
- A Start Diagnostic 1 command occurred with any bit on in the control word other than bit 2 or bits 5-7. A Start Diagnostic 2 command occurred with any bit on in the control word other than 2, 5, 6, 7, or 15.
- An exit transparent command was issued with the byte count not equal to 2.
- The SDLC byte count does not equal 8 or 12 hexidecimal for a Start Cycle-Steal Status command.

Bit 4 - Storage Data Check: This bit is set to 1 during cycle-steal output operations only to indicate that the processor storage location accessed during the current cycle contains incorrect parity. The attachment terminates the operation with an exception interrupt request.

Bit 5 - Invalid Storage Address: This bit is set to 1 if the address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment terminates the operation with an exception interrupt request.

Bit 6 - Protect Check: This bit is set to 1 if the attachment attempts to access a storage location without the correct cycle-steal key.

Bit 7 - Interface Data Check: This bit is set to 1 if a parity error was detected on an interface cycle-steal data transfer. The condition may be detected by the channel or the attachment. In either case, the attachment terminates the operation with an exception interrupt request.

Status After Resets

Power-On Reset: Resets the attachment and sets the DTE interface to DTE ready. The control parameters are reset to no PCI and half duplex.

System Reset: Functions the same as power-on-reset with the exception that no attachment storage test is performed.

Halt I/O and Device Reset: Functions the same as the power-on-reset, with the exception that the prepare level and I-bit, residual address and control parameters are not reset. Device reset does not reset the X.21 state.

Reset function	Reset used			
Reset prepare level	Power on reset	System reset		
Reset I bit	Power on reset	System reset		
Reset X21 interface (DTE ready)	Power on reset	System reset		Halt I/O
Reset all DCB information displayed by communication indicator panel	Power on reset			
Reset residual address	Power on reset			
Reset residual byte count	Power on reset	System reset	Device reset	Halt I/O

Note: The residual address is the address of word 7 (+1) of the DCB under the following conditions:

- Receive time-out prior to character phase.
- DCE error prior to character phase.
- DCE error on initiation of a transmit or receive operation.
- Multi-point transmit error.
- Following an Enable or Disable command.

The following table shows the function for each of the resets:

Condition Codes

Condition codes are reported to the processor by the attachment and/or the channel during the execution of every Operate I/O instruction and upon acceptance of every interrupt. Condition codes are recorded in the even, carry, and overflow indicators.

Condition codes reported during an Operate I/O instruction are as follows:

CC value	Even	Carry	Overflow	Reported by	Meaning
0	0	0	0	Channel	Device not attached
1	0	0	1	Device	Busy
2	0	1	0	Device	Busy after reset
3	0	1	1	Device	Command reject
4	1	0	0	Device	Intervention req'd*
5	1	0	1	Chan/Dev	Interface data check
6	1	1	0	Device	Controller busy
7	1	1	1	Device	Satisfactory

*Not reported by the attachment.

Condition codes reported during interrupt acceptance are as follows:

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end
1	0	0	1	PCI
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention*
5	1	0	1	Attention and PCI*
6	1	1	0	Attention and exception*
7	1	1	1	Attention and device end*

*Not reported by the attachment.

Jumperable Options

The following attachment options can be enabled by installation of a card jumper:

> **Note:** Refer to the maintenance logic diagrams (MLD) for jumper locations and attachment feature card layout.

Allow IPL: This jumper causes the attachment to monitor for a BSC or SDLC/HDLC IPL sequence. The DTE interface is set to DTE ready.

Bi-Sync Mode: This jumper sets the attachment to BSC mode. Absence of this jumper indicates SDLC/HDLC mode to the attachment.

Local Attach 1: This jumper is installed in the local attach 1 cable. The attachment provides clocking in the SDLC/HDLC mode at a speed of 9600 bps.

> **Note:** The X.21 plug must be installed.

Local Attach 2: This jumper is installed in the local attach 2 cable. The attachment provides clocking at a speed of 48000 bps.

> **Note:** The X.21 plug must be installed.

Secondary Station Address/Multi-Point Address: These jumpers are used to assign the secondary station address in SDLC/HDLC mode, or to assign the multi-point address in BSC mode.

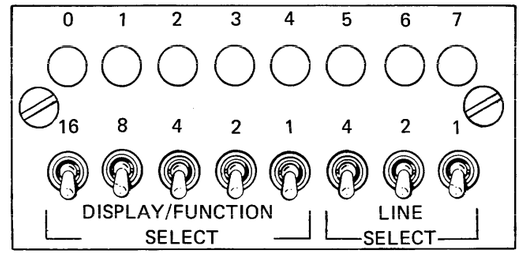
> **Note:** In BSC mode the attachment is a multi-point tributary if the multi-point address is not 0. Therefore, 0 is not a valid multi-point address.

Signal to Protective Ground: If this jumper is installed, it connects protective ground to signal ground. This jumper is installed to meet local code requirements when attaching to X.21 DCE.

X.21 Jumper: If this jumper plug is installed, the attachment operates with the X.21 interface.

V.35 Jumper: If this jumper plug is installed, the attachment operates with the V.35 interface.

Communications Indicator Panel



LINE SELECT Switches

Line select switches 2 and 4 must be set to 0 (down) for valid indications. Line select switch 1 is used to select either device 0 or device 1.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed on the panel. The following is a list of switch settings and the information that is displayed on the panel:

Switch setting						
16	8	4	2	1	Indicator	Display
0	0	0	0	0	0-7	Bits 0-7 of control word
0	0	0	0	1	0-7	Bits 8-15 of control word
0	0	0	1	0	0-7	Timer 1
0	0	0	1	1	0-7	Timer 2
0	0	1	0	0	0-7	Bits 0-7 of PCI ID
0	0	1	0	1	0-7	Bits 0-7 of status address
0	0	1	1	0	0-7	Bits 8-15 of status address
0	0	1	1	1	0-7	Bits 0-7 of chain address
0	1	0	0	0	0-7	Bits 8-15 of chain address
0	1	0	0	1	0-7	Bits 0-7 of byte count
0	1	0	1	0	0-7	Bits 8-15 of byte count
0	1	0	1	1	0-7	Bits 0-7 of data address
0	1	1	0	0	0-7	Bits 8-15 of data address
0	1	1	0	1	0-7	Bits 0-7 of CSSW-0
0	1	1	1	0	0-7	Bits 8-15 of CSSW-0
0	1	1	1	1	0-7	Bits 0-7 of CSSW-1
1	0	0	0	0	0-7	Bits 8-15 of CSSW-1
1	0	0	0	1	0-7	Bits 0-7 of CSSW-2
1	0	0	1	0	0-7	Bits 8-15 of CSSW-2
1	0	0	1	1	0-7	Bits 0-7 of CSSW-3
1	0	1	0	0	0-7	Bits 8-15 of CSSW-3
1	0	1	0	1	0-7	Bits 0-7 of CSSW-4
1	0	1	1	0	0-7	Bits 8-15 of CSSW-4
1	0	1	1	1	0-7	Bits 0-7 of CSSW-5 (SDLC)
1	1	0	0	0	0-7	Bits 8-15 of CSSW-5 (SDLC)
1	1	0	0	1	0-7	Bits 0-7 X.21 interface state
1	1	0	1	0	0-1	Device 0/device 1 busy flags
					2-4	Not used
					5-7	Interrupt condition code
1	1	0	1	1	0-7	Secondary or MP address
1	1	1	0	0	0-7	Lamp test
1	1	1	0	1	0-7	Interrupt status byte
1	1	1	1	0	0-3	X.21 interface status (TRIC)
					4-7	V.35 interface status (DTR/DSR/RTS/CTS)
1	1	1	1	1	0-2	Not used
					3-7	Set mode DCB word 1 bits 11-15

Error Recovery

Error recovery for the Synchronous Communications Single Line Control is as follows:

1. Inspect the Operate I/O condition code and use the following chart:

Command	Operate I/O CC	Recommended action
Read ID		
Prepare	0	Terminate (device not attached).
	1,2,4,6	Terminate (hardware error).
	3	Examine the IDCB function modifier; terminate if the IDCB is correct.
	5	Retry three times; terminate if the problem persists.
	7	Satisfactory
Halt I/O	0,1,2,3,4,5	Terminate (equipment error).
	7	Satisfactory
Device Reset	0	Terminate (device not attached).
	1,2,4,5,6	Examine the IDCB function modifier; terminate if the IDCB is correct.
	7	Satisfactory
Start, Start Cycle-Steal Status, Start Diag 1, Start Diag 2, Start Mod, Start Control	0	Terminate (device not attached).
	1	Retry after device end if the device is busy or device reset, retry; if trouble persists, terminate.
	2	Terminate
	3	Examine the IDCB function modifier; terminate if the IDCB is correct.
	4	Terminate
	5	Retry three times; terminate if the problem persists.
	6	Retry after controller end interrupt
	7	Satisfactory

2. Inspect the interrupt condition code.

- If the interrupt condition code is 3, terminate.
- If the interrupt condition code is 2, use the following chart.

Interrupt status byte (hex)	Recommended action
A0	Normal ending operation to the receive DCB if a COD was detected prior to decrementing the byte count to 0. Perform a Start Cycle Steal Status to obtain residual address and insure status word 1 is 0. Not reported in SDLC/HDLC data transfer mode.
80	Issue a Start Cycle Steal Status command; examine bits for determination of further action.
40	Examine IDCB for valid function modifier or odd DCB address; correct error condition and retry.
20	Occurs during a receive operation and indicates that the byte count decremented to 0 and no COD character was detected. Increases the receive data buffer size and byte count and retry. Not reported in SDLC/HDLC data transfer mode.
10	Indicates the attachment has detected an invalid situation in the DCB.
08	Storage data check; retry operation; if error persists, abort.
04	Invalid storage address; correct program and retry.
02	Protect check; verify the protect key and retry. This error can only occur on processors with storage protect feature.
01	Interface data check; retry the operation 3 times; abort if error persists.

Appendix A. Reference Information

Transmission Codes

Decimal	Hex	Binary	EBCDIC	ASCII (See Note)	Eight-bit data interchange	PTTC/EBCD	PTTC/ Correspondence
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		uppercase	uppercase
29	1D	1101	IGS	GS	8		≥
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space		@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	"	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	forms feed		
49	31	0001		1	forms feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5	,		
54	36	0110	UC	6			
55	37	0011 0111	EOT	7		Ⓢ (SOA), comma	b
56	38	1000		8			
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	*Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		Ⓝ ,-	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	'
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	|	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	^		idle	idle
95	5F	1111	¬				
96	60	0110 0000	-		ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	j	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	_	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000		p		h	/
113	71	0001		q	shift out		
114	72	0010		r	N (even parity)		
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		

Decimal	Hex	Binary	EBCDIC	ASCII (See Note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ Correspondence
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	
119	77	0111		w			
120	78	1000		x			
121	79	1001		y			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@	|		lowercase	lowercase
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	"	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±, [
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@
133	85	0101	e		! (odd parity)		
134	86	0110	f				
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),"	(
151	97	0111	p				
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	uppercase	uppercase
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H

Decimal	Hex	Binary	EBCDIC	ASCII (See Note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ Correspondence
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), !	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ ,–	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	"
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	⅃		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	⅂				
207	CF	1111				P	A
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100	⅁				
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					

Decimal	Hex	Binary	EBCDIC	ASCII (See Note)	Eight-bit data interchange	PTTC/EBCD	PTTC/ Correspondence
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		
246	F6	0110	6			Ⓨ , ¬	—
247	F7	0111	7				
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⇐ (even parity)	horiz tab	tab
251	FB	1011			⇐ (odd parity)		
252	FC	1100			? (even parity)	lowercase	lowercase
253	FD	1101			? (odd parity)		
254	FE	1110					
255	FF	1111			delete / rub out	delete	

*When used with the BSCA, the software must maintain parity in bits 0–7 of each byte.

Line Control Characters

2740 Line-control characters (EBCD)			
Char	Hex	Alternate designation	Meaning
Ⓑ	BD/3D	EOB	End of block
Ⓒ	9F/1F	EOT	End of transmission
Ⓓ	96/16	EOA	End of address
Ⓝ	C0/40	No	Negative response
Ⓢ	B7/37	SOA	Start of address; used only in addressing
Ⓨ	F6/76	Yes	Positive response
US	1C/9C		Upshift
DS	7C/FC		Downshift

2741 Line-control characters (Correspondence)			
Char	Hex	Alternate designation	Meaning
Ⓒ	9F/1F	EOT	End of transmission
Ⓓ	16/96	EOA	End of address
US	1C/9C		Upshift
DS	7C/FC		Downshift

Line-control characters (8-bit DIC)		
Char	Hex	Meaning
WRU	A1	Who are you? WRU or Dial requests identification (ID)
XON	89	Transmitter on
XOFF	C9	Transmitter off
EOT	21	End of transmission

Line-control characters (ASCII)		
Char	Hex	Meaning
STX	02	Start of text
ETB	17	End of transmission block
ETX	03	End of text
EOT	04	End of transmission
CR	0D	Carriage return
LF	0A	Line feed

Condition Codes

Operate I/O Condition Codes				
CC Value	**Even**	**Carry**	**Overflow**	**Meaning**
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Busy after reset (see Note 2)
3	0	1	1	Command reject
4	1	0	0	Intervention required (see Note 1)
5	1	0	1	Interface data check
6	1	1	0	Controller busy (see Note 3)
7	1	1	1	Satisfactory

Notes:

1. Not reported by any communication attachment.
2. Not reported by multiple-line BSC attachments.
3. Not reported by any single-line communication attachment. Reported on multiple-line attachments when the controller is busy servicing a previous Operate I/O instruction; a subsequent *Controller End* interrupt will occur (interrupt condition code zero).

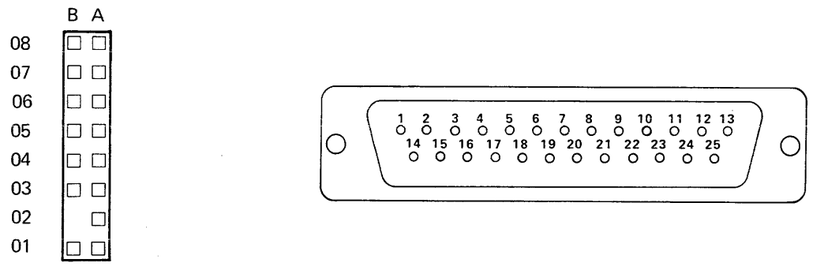
Interrupt Condition Codes				
CC Value	**Even**	**Carry**	**Overflow**	**Meaning**
0	0	0	0	Controller end (see Note 1)
1	0	0	1	PCI (see Note 3)
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention (see Note 2)
5	1	0	1	Attention and PCI (see Note 3)
6	1	1	0	Attention and exception (see Note 2)
7	1	1	1	Attention and device end (see Note 2)

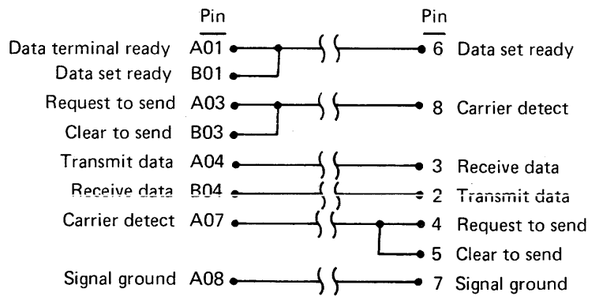
Notes:

1. Not reported by the SDLC attachment.
2. The ACC attachments do not report these condition codes. On BSC and SDLC attachments "attention" indicates that the 'ring indicator' line from the modem is active.
3. Not reported by any of the communications attachments.

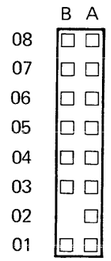
Appendix B. Cable Information

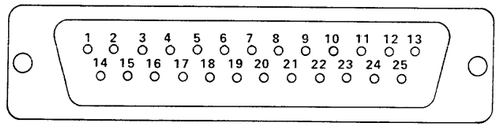
Asynchronous Local Attachment Communications Cable

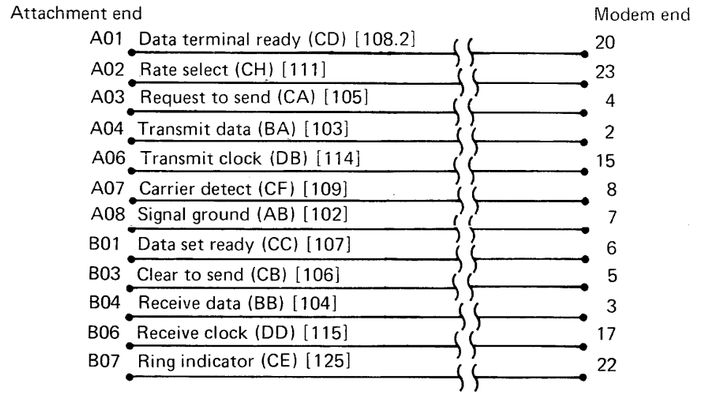




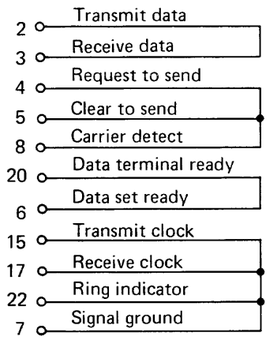
EIA Data Set Cable





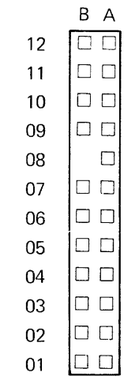


(EIA circuit designation)
[CCITT circuit number]

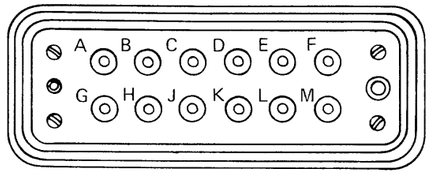


Wrap connector

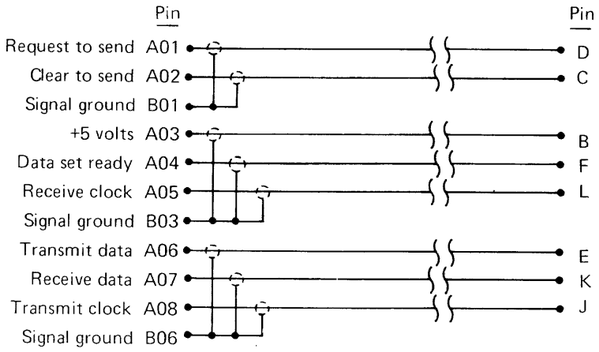
Binary Synchronous Communications/High Speed Cable (WE-Type 303)



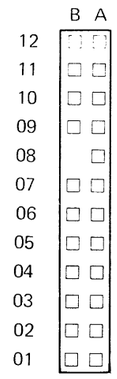
Attachment-end connector (end view)



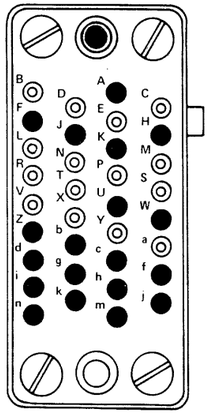
Modem-end connector (end view)



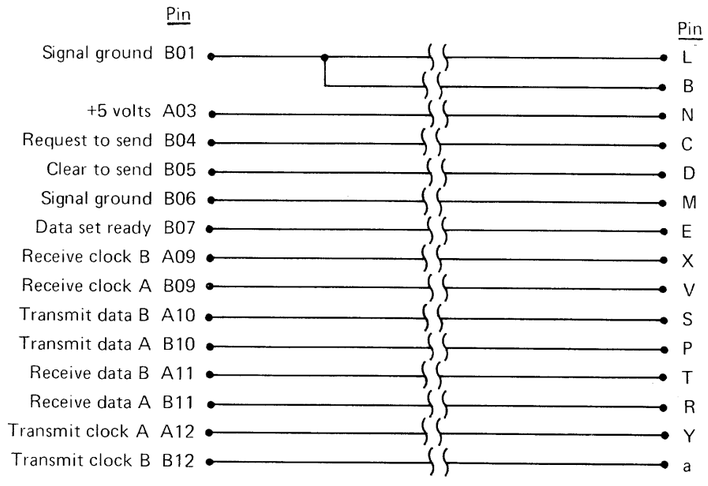
Binary Synchronous Communications V .35/High Speed DDN Cable



Attachment-end connector (end view)

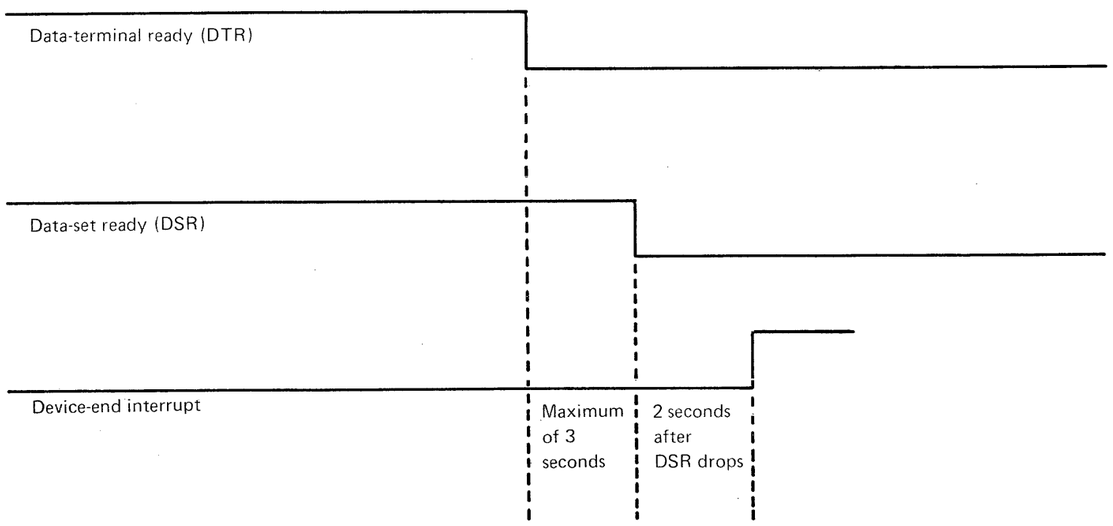


Modem-end connector (end view)

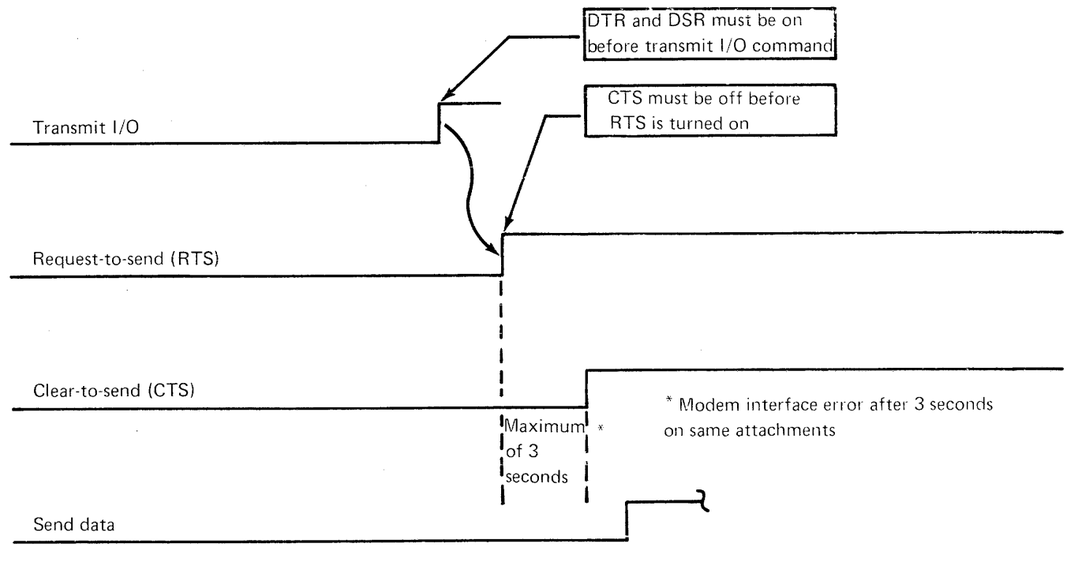


Appendix C. Timing Charts

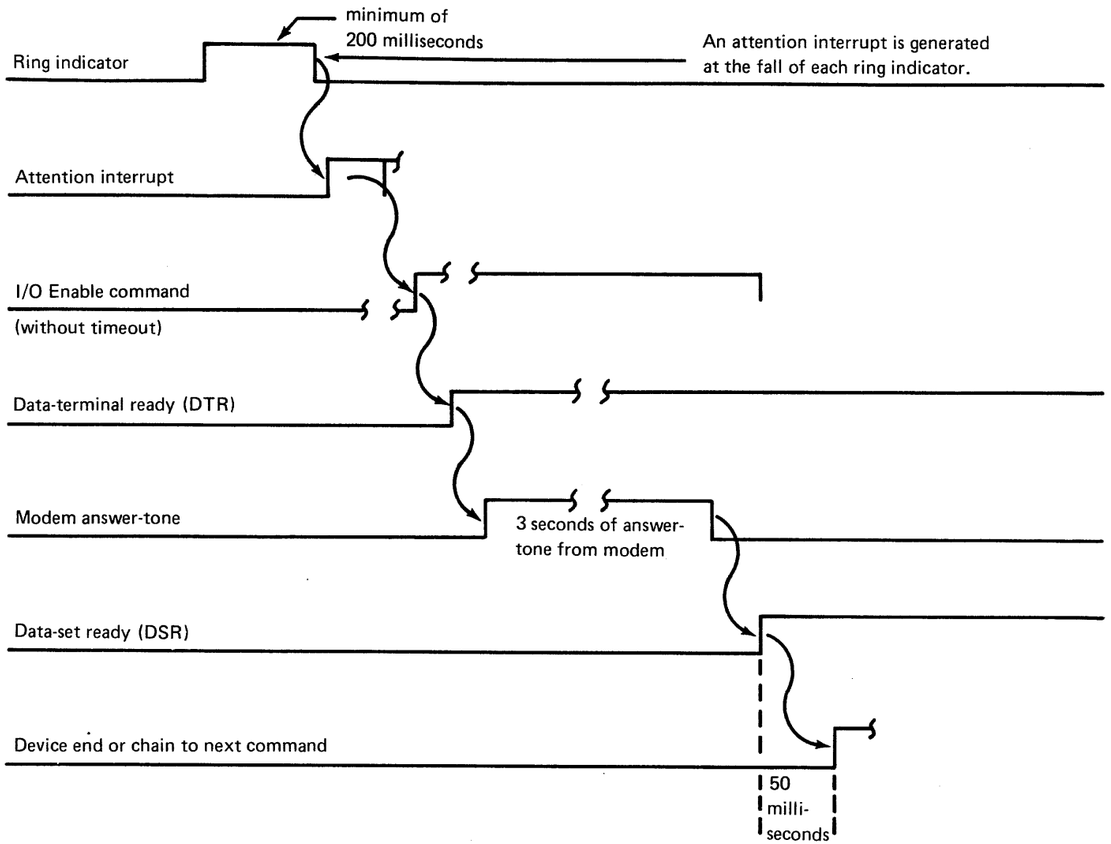
Switch-line disconnect



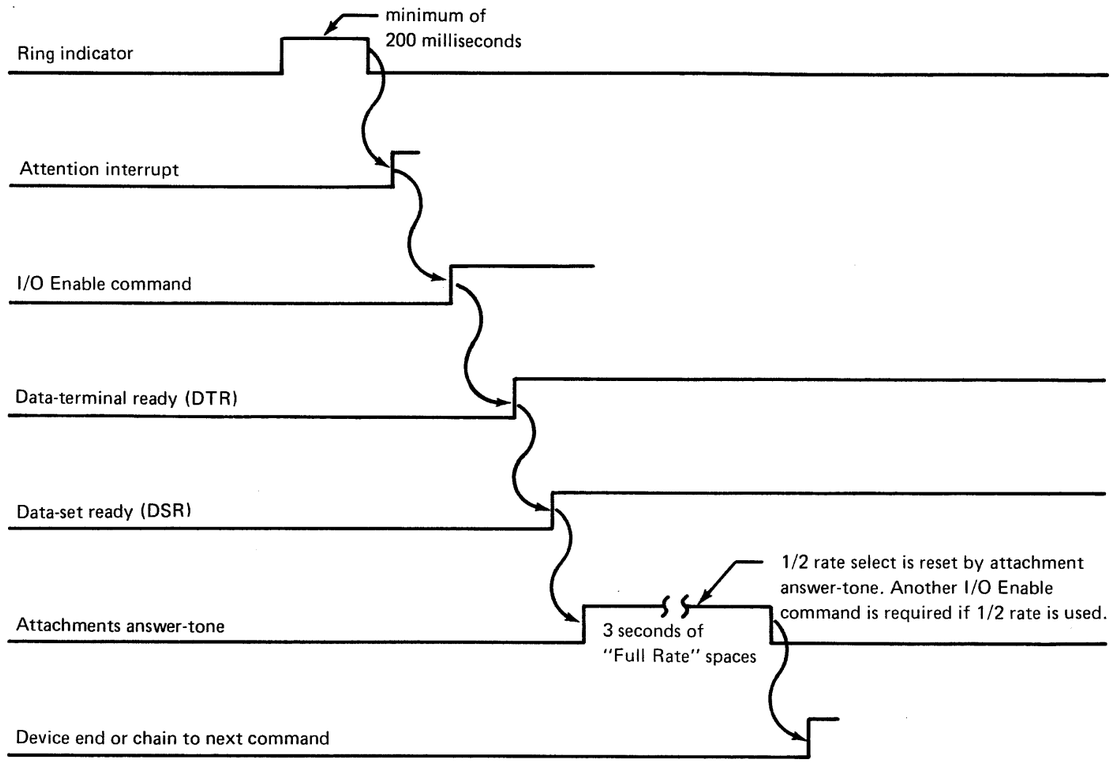
Transmit operation



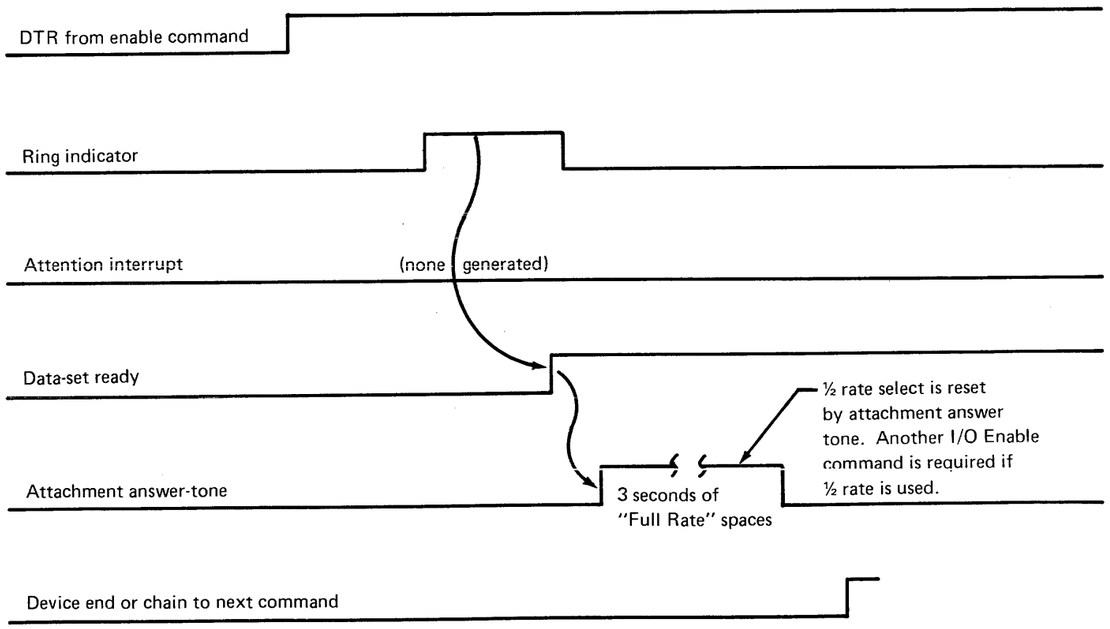
Connect data set to line with modem answer-tone



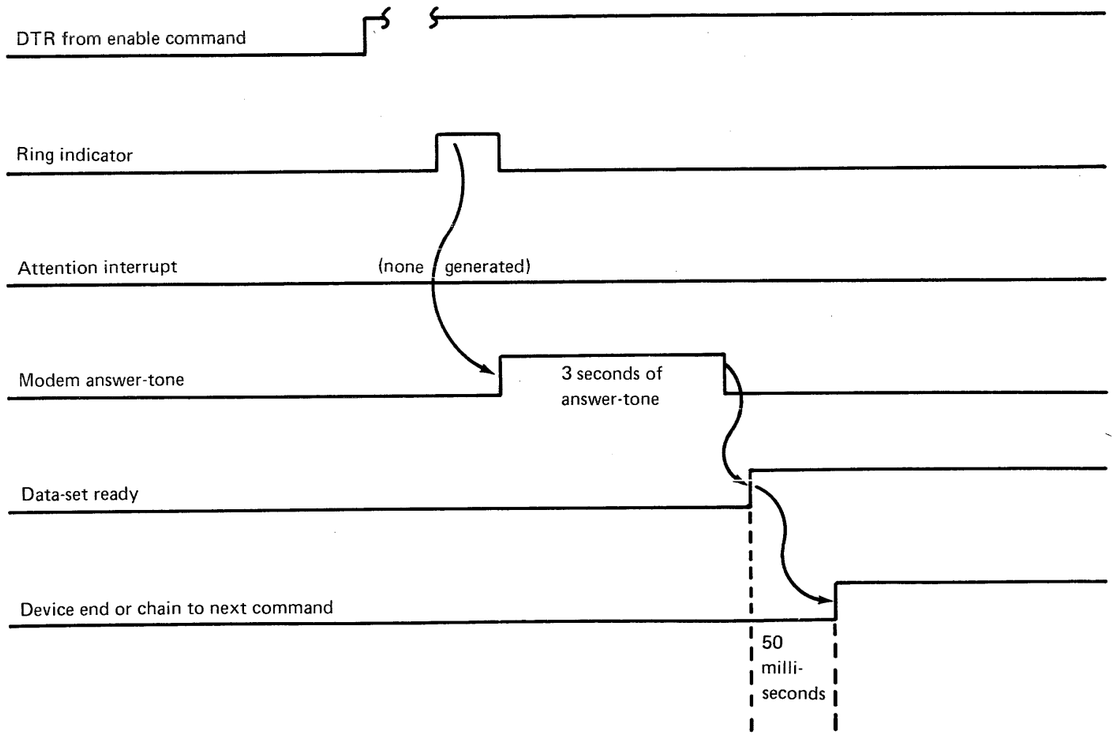
Connect data set to line with attachment jumpered for answer-tone generation



Data terminal ready (DTR) with attachments jumpered for answer-tone generation



Data terminal ready (DTR) with modem answer-tone



Appendix D. List of Acronyms

ACC	Asynchronous communication control
ACK	acknowledge character
ASCII	American Standard Code for Information Interchange
BCC	Block check character
bps	bits per second
BSC	Binary synchronous communications
BSCA	Binary synchronous communications attachment
CCITT	Consultative Committee on International Telephone and Telegraph
CC	condition code
COD	change of direction
CRC	cyclic redundancy check
CTS	clear to send
CV	converters
DCB	device control block
DLE	data link escape character
DSR	data set ready
DTR	data terminal ready
EBCDIC	extended binary coded decimal interchange code
ENQ	enquiry character
EOA	end of address
EOB	end of block
EOC	end of chain
EOT	end of transmission
ETB	end of transmission block character
ETX	end of text character
FCS	frame check sequence
HLA	hold line active
I	interrupt
I-bit	interrupt-bit
I/O	input/output
ID	identification
IDCB	immediate device control block
IIB	interrupt information byte
IPL	initial program load
ISB	interrupt status byte
ITB	end of intermediate transmission block
LCC	line control character
LRC	longitudinal redundancy check
MP	multipoint
NAK	negative acknowledge character
NE	no exception
NRZ	non-return-to-zero
NRZI	non-return-to-zero inverted
PTTC	perforated tape transmission code
ROS	read only storage
RTS	request to send
SDLC	synchronous data link control
SE	suppress exception
SERDES	serializer/deserializer
SOH	start of heading character
STX	start of text character
SYN	synchronous idle character
VRC	vertical redundancy check

Index

IBM / Technical Newsletter

This Newsletter No. SN34-0794
Date February 12, 1982
Base Publication No. SY34-0059-2
System S1-09
Previous Newsletters SN34-0723

IBM Series/1
Communication Features
Theory diagrams

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

5-1 through 5-8
5-19 through 5-26

A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

This technical newsletter adds change pages to Chapter 5 of the base document to provide corrections to the previous document.

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Communication Features
Theory Diagrams

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v, vi
5-1 through 5-26 (added)
X-1 through X-4

Summary of Amendments

This technical newsletter adds Chapter 5, Synchronous Communications Single Line Control, to the base publication.

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