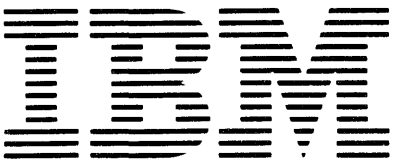
IBM

8100 Information System

Direct Access Storage Devices Description

GA23-0053



8100 Information System

Direct Access Storage Devices Description

GA23-0053-2
File No. 8100-07

Third Edition (April 1984)

This revision obsoletes GA23-0053-1.

This publication is for planning purposes and may be subject to minor changes. The functions and capabilities it describes reflect the information previously available in the *IBM 8130 Processor Description*, GA27-3196, and in the *IBM 8140 Processor Description*, GA27-2880.

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Preface

This manual describes the physical characteristics and specific implementation of the 8100 disk and diskette storage facilities. It is intended primarily to help a programming audience understand (1) how, for some operations, programming can control the way the hardware operates and (2) the significance of hardware status information that is accessible to programming. The manual is divided into three chapters, as follows:

Chapter 1 introduces the 8100 system units.

Chapter 2 describes the hardware components of the 8100 disk storage facility. The chapter describes the components, functional elements, and registers of the disk direct access storage device (DASD), and the commands implemented by the disk adapter. Examples of typical data transfer operations show the relationship between the programmed input/output (PIO) commands implemented by the disk adapter and the way data is transferred by use of channel I/O (CHIO) operations.

Chapter 3 describes the hardware components of the 8100 diskette storage facility. The chapter describes the physical characteristics and functional elements of the diskette storage facility. Like the previous chapter, it provides examples of typical data transfer operations for the diskette adapter.

Using 8100 System Description Publications

The following publications are companions to this one:

- *IBM 8100 Information System Principles of Operation,* GA23-0031
- *IBM 8130 Processor Description*, GA27-3196
- *IBM 8140 Processor Description*, GA27-2880
- *IBM 8150 Processor Description*, GA27-0122
- *IBM 8101/8102 Storage and Input/Output Unit Description*, GA27-2882
- *IBM 8130/8140 Processor Operator's Guide*, GA27-3197
- *IBM 8150 Processor Operator's Guide*, GA23-0123
- *IBM 8140 Processor Expanded Function Operator Panel Feature Description*, GA27-2879

The following figure shows the topics each publication includes.

8100 Offline Hardware Utilites Guide GA23-0152
System Verification Diskette

8130/8140 Operator's Guide GA27-3197
Operating Procedures Problem Determination

8150 Operator's Guide GA23-0123
Operating Procedures Problem Determination

Processor Description GA27-3196 (8130) GA27-2880 (8140) GA23-0122 (8150)
General Description Specific Implementation System Control Facility

8100 Communications, Loop, and Display/Printer Attachment Description GA27-2883
Part 1: Overview Part 2: Communications Description Part 3: Loop Description Part 4: Display/Printer Attachment Description

8100 Direct Access Storage Devices Description GA23-0053
Disk Storage Diskette Storage

8101/8102 Storage and Input/Output Unit Description GA27-2882
General Description System Control Facility Summary

8809 Magnetic Tape Unit Description GA26-1659
General Description Tape Unit

8140 Processor Expanded Function Operator Panel Feature Description GA27-2879
Operating Procedures Hardware Description

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Summary of Changes

Third Edition (April 1984)

The following changes were made to this edition:

- The term *DASD* is used to refer specifically to a single direct-access storage device, which includes a disk or diskette, an access mechanism, and a disk or diskette adapter.
- Chapter 2 has been updated to include references to the 8102 Models A15 and A17 with an enhanced disk DASD.
- Miscellaneous corrections and clarifications have been made throughout this manual.

Second Edition (March 1982)

The following changes were made to this edition:

- The term "processor storage" has been changed to "main storage" to match the other 8100 description manuals.
- The word "processor" has been changed to "processing and control element (PCE)" when referring to the processing unit within the 8100 system. The word "processor" was not changed when referring to the 8130 and 8140 processor.
- All chapters have been updated to include references to the 8140 Model C.
- Appendix C, "Sample 8100 Assembler Language Code to Generate CRC", has been added.
- Miscellaneous corrections and clarifications have been made throughout this manual.

Chapter 1. Introduction

The IBM 8100 Information System is a communication-oriented stand-alone system capable of being attached to a host System/370 or 4300, or to other 8100 systems. The 8100 processors and operating systems provide a flexible base for a wide variety of products.

Direct access storage devices are contained in the following 8100 Information System units:

8130 Processor
8140 Processor
8101 Storage and I/O Unit
8102 Storage and I/O Unit

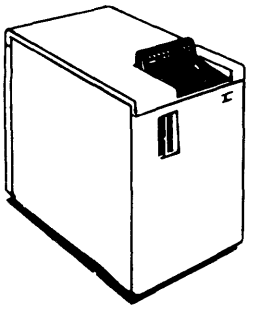
Storage capacity varies with each 8100 unit model. See Figure 1-1.

Disks are permanently sealed in an enclosure, which protects them from external contaminants; the user cannot remove them. Diskettes are inserted into the diskette drive when needed, but are stored outside the 8100 unit when not in use. An optional diskette lock, provided on 8140B and C Processors and also available on some other models, restricts access to the diskette drive.

8130/8140 Processor A Models

Disk Storage 23MB to 64MB

2D Diskette Drive



Communication Port Attachment
Loop Attachment
Display and Printer Attachment (8130B only)

8140 Processor B Models

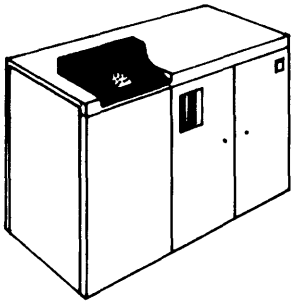
Disk Storage 58MB to 123MB

2D Diskette Drive

8140 Processor C Models

Disk Storage 123MB

2D Diskette Drive



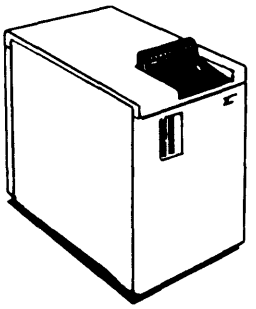
Communication Port Attachment
Display and Printer Attachment
Loop Attachment

8101 Storage and Input/Output Unit

Disk Storage 29MB to 128MB

With optional 2D Diskette, the disk storage is from 29MB to 64MB.

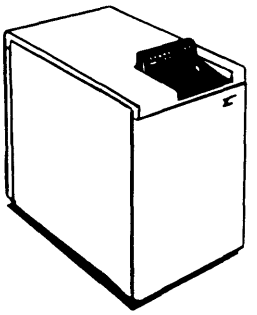
Note: *Disk storage is available only on 8101 Models A11, A13, A23, A25*



Communication Port Attachment
Display and Printer Attachment
Loop Attachment
Storage and I/O Unit Switch Feature

8102 Storage and Input/Output Unit

Disk Storage 129MB to 259MB



Display and Printer Attachment
Magnetic Tape Attachment
Storage and I/O Unit Switch Feature

Figure 1-1. 8100 Information System Units

Chapter 2. 8100 Disk Storage Facility

The 8100 disk storage facility, incorporated in 8130 and 8140 Processors and in 8101 and 8102 Storage and I/O Units, provides high-speed, large-capacity disk storage for data-base, data-communication, or general use.

The disk storage facility consists of one or more direct access storage devices (DASDs). Each disk DASD is composed of a disk, which stores data; fixed or movable magnetic heads, which transfer data to or from the disk; and a disk adapter, which links the disk to the 8100 unit and provides the logic that controls the device.

The storage capacities of 8100 unit models differ according to the number and type of DASDs the models contain. (The 8102 contains a disk DASD with greater capacity and enhanced error-correction capability.) The storage capacities of all 8100 unit models are listed in Appendix A.

Disk DASD Components and Functional Elements

This section describes the physical characteristics of the disk DASD and the elements that enable it to store and transfer data. Refer to Appendix C for physical-format specifications and for access times.

Disk Surfaces

The disk consists of a stack of up to six magnetic-coated platters, each providing two disk surfaces, permanently mounted on a motor-driven spindle. Up to 11 disk surfaces, numbered from 0 to 10, are available for storing data; one surface is reserved for servo coding. Each surface is divided into several hundred circular tracks. Tracks from different surfaces but with the same radius are grouped into cylinders. Cylinders and tracks are numbered starting from zero, with zero closest to the center. Each track is divided into 33 equal sectors, numbered from 0 to 32; any data record stored on a disk can be identified by its cylinder, track, and sector numbers.

Sector Fields

Each sector is divided into three fields: one identification (ID) field and two data fields. The ID field consists of one flag byte, three address bytes, and two cyclic redundancy check (CRC) bytes.

The *flag byte* defines the status of the sector and whether an alternate sector has been assigned. This byte contains the following bits:

Bit	Description
0	Defective field 1 (factory defect in 8102)
1	Defective field 0 (field defect in 8102)
2	Write protect field 1
3	Write protect field 0
4	Sector displaced
5	Sector reassigned
6	Sector defective
7	Alternate sector

The *address bytes* contain the sector, head, and cylinder numbers that identify a particular sector. The following table shows the bit meanings for the address bytes:

Sector Number

Bit	Decimal Value
0	0
1	32
2	16
3	8
4	4
5	2
6	1
7	0

Head Number

Bit	Decimal Value
0	0
1	(Designates a fixed head when equal to 1)
2	8
3	4
4	2
5	1

Cylinder Number

Bit	Decimal Value
6	0 (512 for 8102 only)
7	256
0	128
1	64
2	32
3	16
4	8
5	4
6	2
7	1

The *cyclic redundancy check (CRC) bytes* are error detection code bytes used to check the accuracy of data as it is read from the disk. They are described in more detail under "Disk Adapter Error Detection and Reporting."

Each data field contains 256 data bytes, used to store data, and two CRC bytes (four Error Correction Code—ECC—bytes in the 8102), which function similarly to the ID field CRC bytes described above.

Each data field can be transferred separately, or multiple fields can be transferred when record-length requirements exceed 256 bytes. The maximum number of data fields that can be read or written during a multiple field operation is 64, or the equivalent of one track. Figure 2-1 depicts the disk and its surface format.

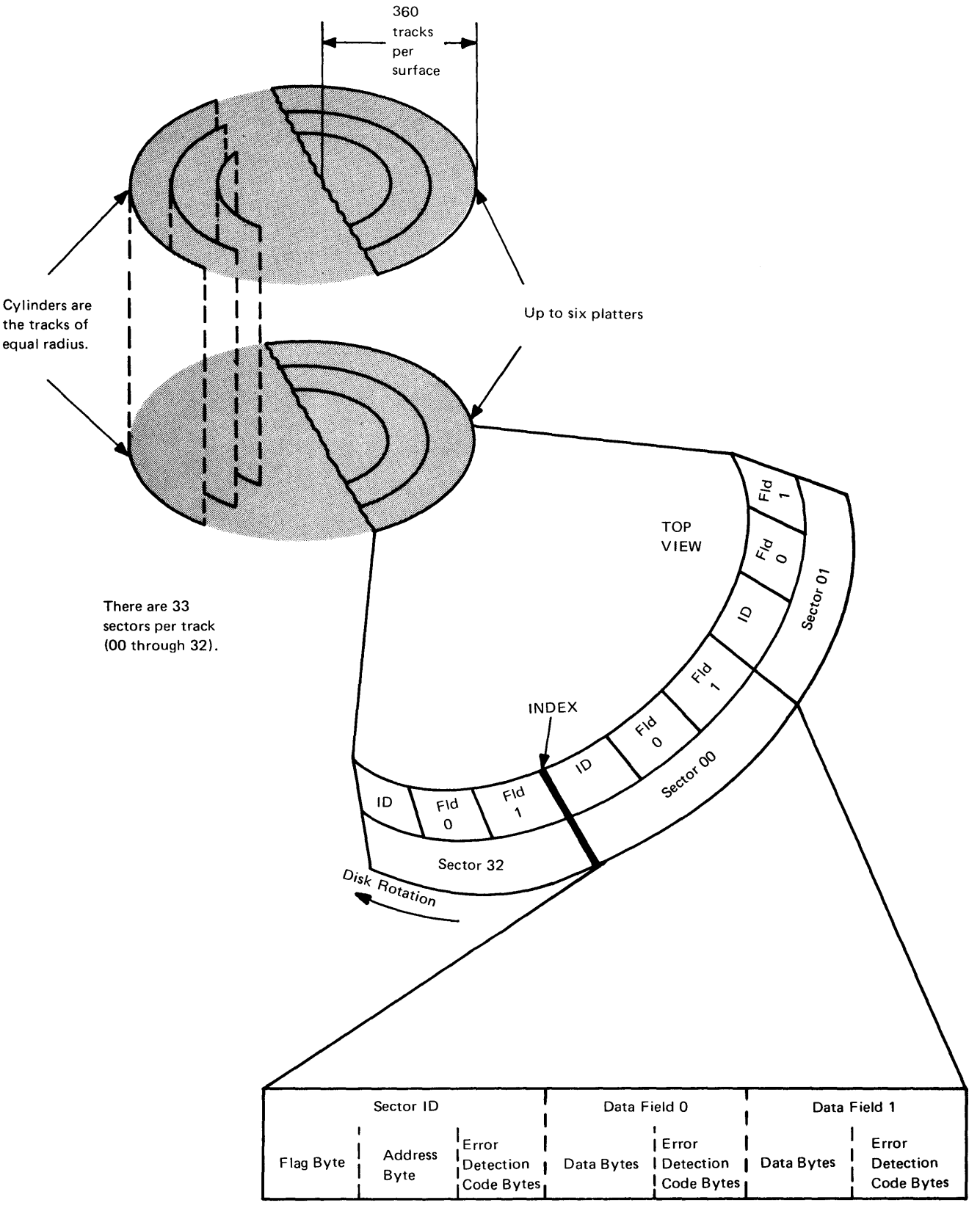


Figure 2-1. Disk Format

Sector Positions

On each disk surface, sectors are usually positioned in sequential order. The only sectors that may appear out of sequence are Sector 32 (which precedes the index) and any sector that has been reassigned or displaced because of defects. Defective sectors are reassigned as follows:

At the factory, the first defective sector on a track is reassigned as Sector 32; data and the original ID of the defective sector are displaced one sector, as are all subsequent sectors to the end of the track (Figure 2-2). The next defective sector on the same track is reassigned to Track 64 (in the 8102, either to the closest spare sector within 10 cylinders or to Track 64).

During normal operation, any defective sector is reassigned to Track 64 (in the 8102, either to the closest spare sector within 10 cylinders or to Track 64).

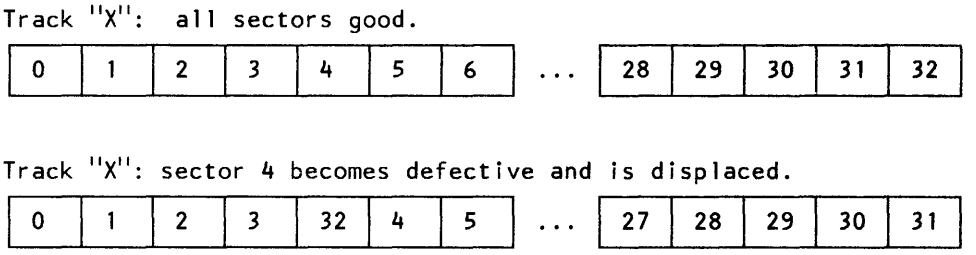


Figure 1. Sector Displacement

Magnetic Heads

Over each disk surface are suspended one or more magnetic heads for transferring data. The heads may be either fixed or movable.

A *movable-head configuration* uses one head per disk surface. A pivoting arm suspends the head over the surface, enabling it to move to any track. The head can access any data record on a surface, but there is a brief delay in data transfer whenever the head moves to a different track.

In a *fixed-head configuration*, eight heads are suspended over one disk surface. The heads are permanently positioned over their respective data tracks and can access only those eight tracks. When transferring data, fixed heads read each track on a surface in succession; they can transfer 131,072 successive bytes of data to or from their tracks without the delay of access motion.

8130, 8140, and 8101 Spiral Format

On each successive disk surface, Sectors 0–31 are skewed one quarter turn. This places Sector 0 of each surface over Sector 8 of the previous surface and arranges the tracks into a spiral twisting around the disk. (See Figure 2-3 for a depiction of the spiral format.)

The spiral format synchronizes the movement of the disk with the access delay of the heads. Switching to the next higher head in a cylinder takes up a 5-millisecond (ms) "head select" delay, during which the disk rotates one quarter turn. The spiral format prevents the first eight sectors on the next surface from rotating past the next active head. The first sector rotates into position only after the head becomes active, so the head can resume data transfer immediately. Figure 2-4 lists each sector number with its physical position on the disk surface.

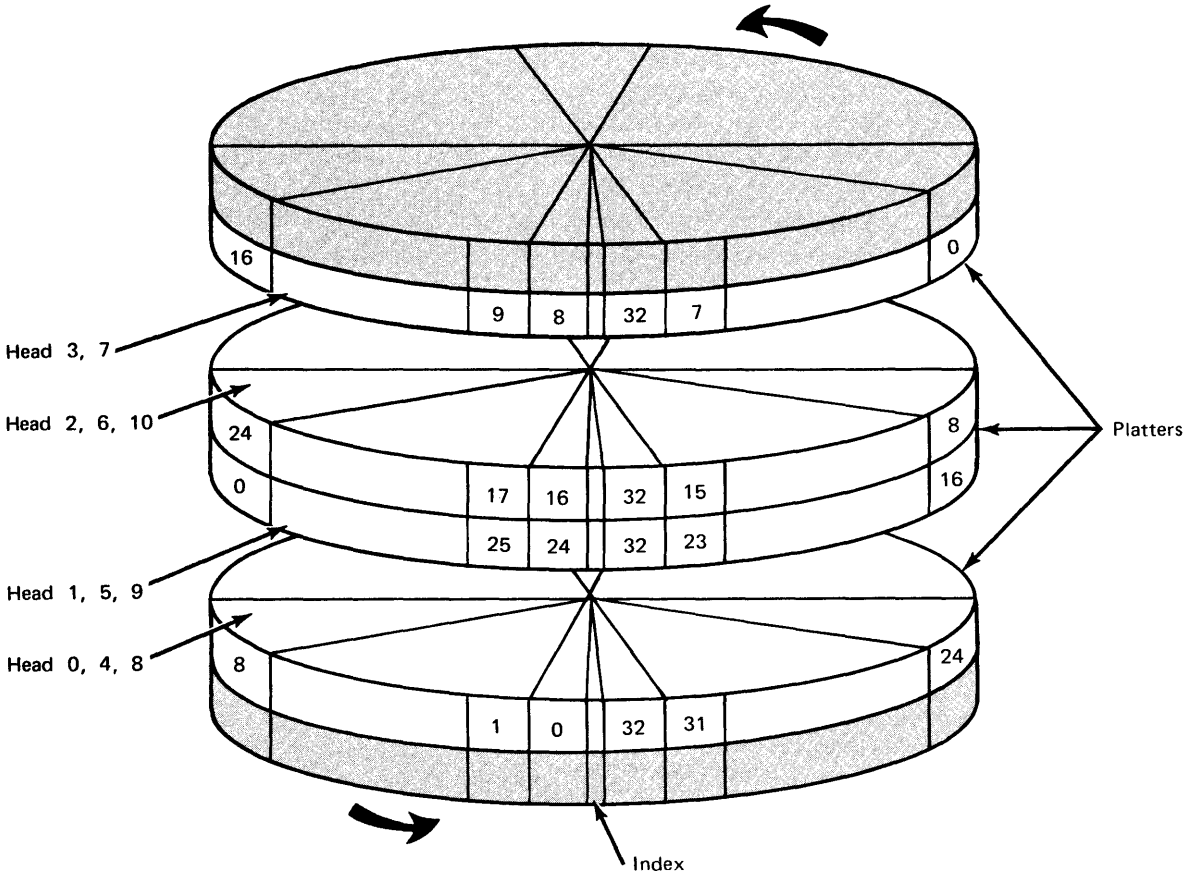


Figure 2-3. Spiral Format

	Heads 0, 4, 8		Heads 1, 5, 9		Heads 2, 6, 10		Heads 3, 7		
Physical Sector Number (Position)	**ID on Disk**	**LSN**	**ID on Disk**	**LSN**	**ID on Disk**	**LSN**	**ID on Disk**	**LSN**	
									<---Index
0	**00**	0	**30**	24	**20**	16	**10**	8	
1	**02**	1	**32**	25	**22**	17	**12**	9	
2	**04**	2	**34**	26	**24**	18	**14**	10	
3	**06**	3	**36**	27	**26**	19	**16**	11	
4	**08**	4	**38**	28	**28**	20	**18**	12	
5	**0A**	5	**3A**	29	**2A**	21	**1A**	13	
6	**0C**	6	**3C**	30	**2C**	22	**1C**	14	
7	**0E**	7	**3E**	31	**2E**	23	**1E**	15	
8	**10**	8	**00**	0	**30**	24	**20**	16	
9	**12**	9	**02**	1	**32**	25	**22**	17	
10	**14**	10	**04**	2	**34**	26	**24**	18	
11	**16**	11	**06**	3	**36**	27	**26**	19	
12	**18**	12	**08**	4	**38**	28	**28**	20	
13	**1A**	13	**0A**	5	**3A**	29	**2A**	21	
14	**1C**	14	**0C**	6	**3C**	30	**2C**	22	
15	**1E**	15	**0E**	7	**3E**	31	**2E**	23	
16	**20**	16	**10**	8	**00**	0	**30**	24	
17	**22**	17	**12**	9	**02**	1	**32**	25	
18	**24**	18	**14**	10	**04**	2	**34**	26	
19	**26**	19	**16**	11	**06**	3	**36**	27	
20	**28**	20	**18**	12	**08**	4	**38**	28	
21	**2A**	21	**1A**	13	**0A**	5	**3A**	29	
22	**2C**	22	**1C**	14	**0C**	6	**3C**	30	
23	**2E**	23	**1E**	15	**0E**	7	**3E**	31	
24	**30**	24	**20**	16	**10**	8	**00**	0	
25	**32**	25	**22**	17	**12**	9	**02**	1	
26	**34**	26	**24**	18	**14**	10	**04**	2	
27	**36**	27	**26**	19	**16**	11	**06**	3	
28	**38**	28	**28**	20	**18**	12	**08**	4	
29	**3A**	29	**2A**	21	**1A**	13	**0A**	5	
30	**3C**	30	**2C**	22	**1C**	14	**0C**	6	
31	**3E**	31	**2E**	23	**1E**	15	**0E**	7	
32	**40**	32	**40**	32	**40**	32	**40**	32	
									<---Index

LSN = Logical Sector Numbering
Sector 32 ("X40") is the alternate sector and precedes the index code, unless logically displaced or reassigned.
When fixed heads are used, movable head 0 is not present.

Figure 2-4. Sector Numbering

Adapter

The disk adapter includes the following elements:

- The Function Control Block (FCB) processor, which decodes commands, fetches control information from main storage, and initiates seek, file status, and sense operations to the disk.
- The data handler, which controls the movement of stored data between the disk and main storage.
- Data buffers, which hold data being transferred between the disk and main storage. There are two 256-byte buffers, labeled A and B.
- Adapter registers, which control and keep track of the disk adapter's data transfer operations. The disk adapter control registers control data transfer operations; the disk adapter status registers record the operational status of the disk adapter and identify error conditions detected by the disk adapter.

Operations

The disk adapter uses these elements to transfer data in two types of operations:

- Channel I/O (CHIO) operations, or the transfer of data between main storage and the disk, initiated by control logic and controlled by channel logic. (CHIO operations are described in greater detail under the heading "Disk Channel I/O [CHIO] Operations.")
- Disk Programmed I/O (PIO) operations, or the transfer of data between main storage and the disk, controlled by I/O instructions. (PIO operations are described in greater detail under the heading "Programmed I/O [PIO] Operations.")

During these data transfer operations, the adapter logic receives control signals from the channel and returns the appropriate responses.

If the transfer is a CHIO operation, the adapter uses buffers A and B to hold the data between the disk and main storage. It controls the buffers with bit 0 of its data handler extended status register. When this bit is set to 1, data buffer A transfers data between itself and main storage, and data buffer B transfers data between itself and the disk; when the bit is reset to 0, the buffers are conditioned oppositely. After a buffer is loaded, the disk adapter inverts the state of the bit, enabling the buffer to transfer its data out in the opposite direction. For multifield transfers, the disk adapter repeatedly inverts the state of the bit, enabling one buffer to start loading data in while the other transfers data out. (See Figure 2-5.)

When an I/O operation has been completed, or when an error condition has been detected by the disk adapter and recorded in its status registers, the disk adapter notifies the program by presenting I/O interrupt requests to the processing and control element (PCE).

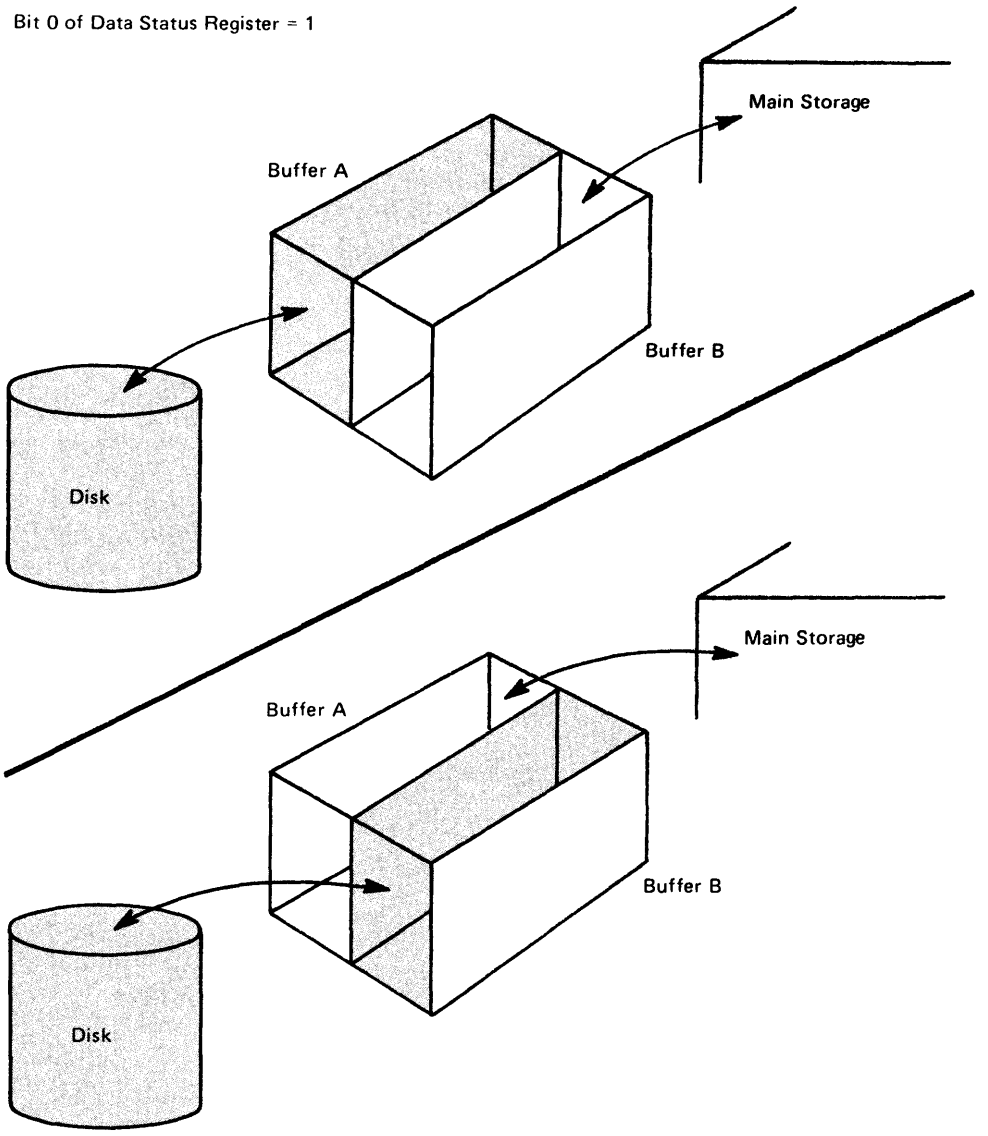


Figure 2-5. Disk Adapter Data Buffers

Disk Adapter Error Detection and Reporting

When data is written to the disk, the disk adapter automatically generates an error detection code for each ID or data field. When each field is subsequently read, the disk adapter compares the field's error detection code with a newly generated code. If the code bytes do not match, the disk adapter reports the error by presenting an I/O interrupt request to the PCE and setting the appropriate bits in one of its registers (BSTAT); the software and hardware can then attempt to recover from the failing operation.

The disk adapter checks the parity of all internal data transfers, and if incorrect parity is detected on data within the adapter, the disk adapter sets the appropriate bits in four of its registers (BSTAT, data status register, FCB processor register, and seek register).

The disk adapter also checks the parity of all commands and data that are received from the program. If incorrect parity is detected, the disk adapter sets the appropriate status bits and suppresses the response for the data or the command, forcing an I/O time-out check. The I/O time-out condition results in a system check interruption in the PCE, with the I/O operation being terminated when the Halt signal is activated by the PCE's channel logic. Again, the data status register, the FCB processor register, and the seek register contain additional information concerning the cause of the error.

Appendix C lists all adapter-detected errors with the register settings used to report them.

Disk Adapter Control Registers

The disk adapter uses the following seven control registers and the physical sector counter to control data transfer operations:

- Burst register
- Control CHCV register
- Data transfer CHCV register
- Residual count register
- Next function register
- Seek register
- Skip factor register

  and

- Physical sector counter

The following sections describe each disk adapter control register and the physical sector counter.

Burst Register

The burst register is a three-bit register whose value represents the maximum number of halfword transfers that can occur during one CHIO burst. One CHIO operation consists of one or more CHIO bursts during which data is transferred between the adapter and main storage. Some CHIO bursts may include *fewer* halfwords than the maximum defined by the burst register value.

Listed below are the burst register values which represent specific lengths of CHIO burst transfers:

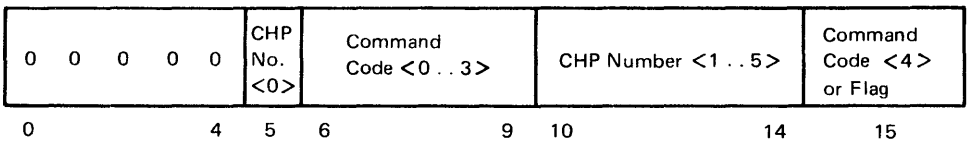
Burst Value (in binary)	**Burst Length (in halfwords)**
000	1 (2 bytes)
001	2 (4 bytes)
010	4 (8 bytes)
011	8 (16 bytes)
100	16 (32 bytes)
101	32 (64 bytes)
110	64 (128 bytes)
111	128 (256 bytes)

The burst register is set to binary 111 by the Reset Disk Adapter command (hex 02) and by system reset.

Programming Note: The contents of the burst register are loaded using bits 13–15 of the CHIO Load Burst Register operation, are read using the Read Burst Skip Factor and Spiral command (hex 21), and are returned in bits 13–15 of the data returned to the program.

Control CHCV Register

Channel Control Vector Format



The control CHCV register contains bits 3–5 and bits 10–14 of the CHCV used by the disk adapter to access control and data transfer operations from main storage. Bits 0–2 and 15 are used only for diagnostic purposes. The disk adapter generates bits 6–9, which are presented to the channel when the CHIO operation is initiated.

Programming Note: Bits 3 and 4 are reserved in the CHCV and must be set to 0 to prevent system check interruptions when the CHCV is sent to the PCE's channel logic.

This register is loaded during execution of the Initiate CHIO command (hex 08) by the Write Control CHCV Register (hex 24) and with the Load New Control

CHCV operation. The contents of this register cannot be read directly; the Diagnostic Read Control CHCV Register commands (hex 3B, 3D, and 3F) access its contents besides forcing other CHCV bits active during their execution.

Data Transfer CHCV Register

The data transfer CHCV register contains bits 3–5 and 10–14 of the CHCV used during disk data transfer operations to or from main storage. Bits 0–2 and 15 are not implemented. The disk adapter generates bits 6–9, which are presented to the channel when the CHIO operation is indicated.

Programming Note: Bits 3 and 4 are reserved in the CHCV and must be set to zero. If a CHCV is sent to the PCE's channel logic with 1's in bit 3 or 4, a system check interruption results and the CHIO operation is terminated.

This register is loaded during execution of the Write Data CHCV Register command (hex 26) and during execution of the Load New Data Transfer CHCV control operation. The contents of this register cannot be read directly; the Diagnostic Read Data CHCV Register commands (hex 31, 33, 35, and 37) access its contents besides forcing other CHCV bits active during their execution.

Residual Count Register

The residual count register is a 6-bit register designating the number of data fields remaining to be transferred by a CHIO data transfer operation. The register contains a value one less than the number of fields to be transferred. The register may contain hex values within the range 00 to 3F (0 to 63 decimal).

During a CHIO operation, the contents of the residual count register are decremented by the disk adapter as each field is transferred. At the normal completion of a CHIO data transfer operation, the residual count register has been decremented to zero. However, if an error condition has terminated a CHIO data transfer operation, the register contains the number of data fields remaining to be transferred.

Programming Note: The contents of the residual count register are loaded from bits 10–15 of the CHIO Load Skip Factor/Field Count operation, are read using the Read Residual Count Register command (hex 05), and are returned in bits 10–15 of the data returned to the program.

Next Function Register (NFR)

The NFR is a halfword register containing the current or next CHIO operation to be performed by the disk adapter. As CHIO control and data transfer operations are accessed from main storage, they are placed in the NFR. The NFR contains only the next operation to be performed when a moving head seek operation is being executed and the adapter has prefetched the next operation. Prefetching CHIO operations is described under "CHIO Control Operations."

Programming Note: The contents of the NFR can be loaded under program control by issuing the Write NFR command (hex 22), and can be accessed by issuing the Read NFR command (hex 39).

Seek Register

The seek register is a halfword register whose bits are grouped into fields identifying the location of the access mechanism and the current head selection value.

Bit	Description
0	**Recalibrate.** This bit is set when the Recalibrate operation is executed by the disk adapter. The Recalibrate operation returns the access mechanism to home position and sets the head selection value to head 1.
1–5 (8130, 8140, and 8101 only)	**Head Selection Value.** The head selection field identifies the current head selection value. In fixed-head configurations, bit 1 *set* indicates a fixed head; bit 1 *reset* indicates a moving head.
1 (8102 only)	**Reserved.** This bit is always zero.
2–5 (8102 only)	**Head Selection Value.** The head selection field identifies the current head selection value.
6 (8130, 8140, 8101 only)	**Reserved.** This bit is always zero.
7–15 (8130, 8140, 8101 only)	**Cylinder Selection Value.** The cylinder selection field identifies the current location of the access mechanism.
6–15 (8102 only)	**Cylinder Selection Value.** (Described above.)

Programming Note: The contents of the seek register can be loaded using the Seek or Recalibrate operations, or by issuing the Load Seek Register from NFR command (hex 2A). The head selection field is loaded from bits 2 to 6 of the operation register. The contents of the seek register can be read by issuing the Read Seek Register command (hex 29).

Skip Factor Register

The skip factor register is a 2-bit register that defines the sequence in which data fields are transferred from the disk surface during multifield transfers. The contents of the skip factor register are encoded as follows:

Bit Value	Skip Factor Description
00	**No Skip.** Access each data field sequentially from the disk.
01	**Skip One Field.** Access every other physical field location from the disk.
10	**Skip Three Fields.** Access every fourth physical field location from the disk.
11	**Skip Seven Fields.** Access every eighth physical field location from the disk.

Figure 2-6 shows the data field transfer sequence of physical data field locations for each skip factor value, beginning with sector 0 field 0. The figure shows the field transfer sequence for a full track, or 64 fields. When fewer than 64 fields are to be transferred, the sequence shown in Figure 2-6 is valid, but the starting sector value determines where in this sequence the data transfer operation begins and ends.

Programming Note: The contents of the skip factor register are loaded from bits 8 and 9 of the Load Skip Factor/Field Count operation. They are accessed by issuing the Read Burst, Skip Factor, and Spiral command (hex 21), and are returned in bits 8, 9 of the data returned to the program.

Skip Factor 00		Skip Factor 01		Skip Factor 10		Skip Factor 11	
0-0	16-0	0-0	0-1	0-0	1-0	0-0	2-0
0-1	16-1	1-0	1-1	2-0	3-0	4-0	6-0
1-0	17-0	2-0	2-1	4-0	5-0	8-0	10-0
1-1	17-1	3-0	3-1	6-0	7-0	12-0	14-0
2-0	18-0	4-0	4-1	8-0	9-0	16-0	18-0
2-1	18-1	5-0	5-1	10-0	11-0	20-0	22-0
3-0	19-0	6-0	6-1	12-0	13-0	24-0	26-0
3-1	19-1	7-0	7-1	14-0	15-0	28-0	30-0
4-0	20-0	8-0	8-1	16-0	17-0	0-1	2-1
4-1	20-1	9-0	9-1	18-0	19-0	4-1	6-1
5-0	21-0	10-0	10-1	20-0	21-0	8-1	10-1
5-1	21-1	11-0	11-1	22-0	23-0	12-1	14-1
6-0	22-0	12-0	12-1	24-0	25-0	16-1	18-1
6-1	22-1	13-0	13-1	26-0	27-0	20-1	22-1
7-0	23-0	14-0	14-1	28-0	29-0	24-1	26-1
7-1	23-1	15-0	15-1	30-0	31-0	28-1	30-1
8-0	24-0	16-0	16-1	0-1	1-1	1-0	3-0
8-1	24-1	17-0	17-1	2-1	3-1	5-0	7-0
9-0	25-0	18-0	18-1	4-1	5-1	9-0	11-1
9-1	25-1	19-0	19-1	6-1	7-1	13-0	15-0
10-0	26-0	20-0	20-1	8-1	9-1	17-0	19-0
10-1	26-1	21-0	21-1	10-1	11-1	21-0	23-0
11-0	27-0	22-0	22-1	12-1	13-1	25-0	27-0
11-1	27-1	23-0	23-1	14-1	15-1	29-0	31-0
12-0	28-0	24-0	24-1	16-1	17-1	1-1	3-1
12-1	28-1	25-0	25-1	18-1	19-1	5-1	7-1
13-0	29-0	26-0	26-1	20-1	21-1	9-1	11-1
13-1	29-1	27-0	27-1	22-1	23-1	13-1	15-1
14-0	30-0	28-0	28-1	24-1	25-1	17-1	19-1
14-1	30-1	29-0	29-1	26-1	27-1	21-1	23-1
15-0	31-0	30-0	30-1	28-1	29-1	25-1	27-1
15-1	31-1	31-0	31-1	30-1	31-1	29-1	31-1

Figure 2-6. Multifield Transfers with Skip Factor Values

Physical Sector Counter (PSC)

The physical sector counter (PSC) contains the number of the next physical sector available. The PSC is set to zero by the index signal and is incremented for each sector area on the disk surface. The PSC is used by the disk adapter to control data transfer operations, and cannot be accessed or modified through programming.

Disk Adapter Status Registers

The disk adapter uses the following four status registers to record the operational status of the disk adapter and to identify error conditions detected by the disk adapter.

- Disk basic status register (Disk BSTAT)
- Data handler extended status register

- FCB processor status register
- Seek status register

The bits in these registers can be reset by activating the Reset interface line or by decoding a Reset Adapter PIO command.

Disk BSTAT

The following sections list and describe the bits in each disk adapter status register.

The disk BSTAT is a 2-byte register.

Bit	Description
0	**FCB Processor Error.** This bit is set when a parity error is detected in the disk adapter control logic.
1	**Data Handler Error.** This bit is set when a data buffer parity check or a hardware failure is detected in the disk adapter control logic.
2	**Check Error.** This bit is set during disk read operations when the error detection code read from the disk does not match the error detection code generated by the disk adapter. When this bit is set, either bit 3 (ID error) or bit 4 (data field error) is set to identify the field containing the error.
3	**ID Error.** This bit is set under one of the following conditions: • A CRC error is detected while the ID field is being read. • The PSC indicates that the correct sector has been reached for a read or write operation, but one of the cylinder, head, or sector bytes does not compare with the value in the seek or NFR. • The "defective" bit in the ID flag byte is set, and a Read-Normal operation or any data-field read or write operation is in progress.
4	**Data Field Error.** This bit is set during a read operation if a CRC/ECC error is detected on a data field; it is set during a write operation when the "write protect" bit is set for the selected data field in the sector ID field flag byte.
5	**Sector Not Found.** This bit is set when a second index signal is detected by the disk adapter and the selected sector ID has not yet been located. This bit is also set if a displaced ID is met or if no byte sync field is detected in the ID.
6	**MCK-Halted CHIO Data Transfer.** This bit is set to indicate that the disk adapter received the Halt signal from the channel during a CHIO burst transfer of data. This bit is not set during CHIO control operation transfers. The Halt signal also sets BSTAT bit 13 (disk equipment check).

Bit	Description
7	**File Write Gate Error.** This bit is set when the Write Gate Return signal does not match the internal signal that activates the Write signal from the adapter to the file. When activating or deactivating the Write signal, the adapter waits 890 ns for the Write Gate Return signal before declaring an error.
8*	**Program-Controlled Interrupt (PCI).** This bit is set when the PCI operation is performed by the disk adapter. This bit can also be set through programming; however, BSTAT bit 15 is not automatically set in this case.
9*	**Device Error.** This bit is set whenever the disk adapter detects an error condition. When this bit is set, BSTAT bit 11 (busy) is reset by the disk adapter and BSTAT bit 15 is set to present an I/O interrupt request to the PCE. When this bit is reset through programming, bits 10 and 11 of the seek status register are reset, as are BSTAT bits 0–7 and FCB processor status register bits 8–15 if they contain a value in the range hex 38–3F.
10	**File Interrupt Disabled.** This bit is set only by a Set Basic Status command. When set, the bit causes the adapter to ignore any file interrupts. It is reset by a Reset Adapter or Reset Basic Status command.
11	**Busy.** This bit is set during execution of the Initiate CHIO command (hex 08) to indicate that a CHIO operation is in progress. This bit is reset by one of the following conditions: • The CHIO operation is completed normally with an End operation or a Terminate operation being performed by the disk adapter. • BSTAT bit 9 (disk adapter error) is set by an error condition other than a control operation time-out. • The disk adapter is reset. This bit cannot be set or reset using the Set or Reset BSTAT under Mask commands (hex 04 or 06).
12	**Channel Request Frozen.** When this bit is set, the disk adapter is unable to activate the Channel Request signal to initiate a CHIO burst transfer. This bit is only set and reset through programming.
13*	**Equipment Check.** This bit is set under one of the following conditions: • A Halt signal is received from the channel during PIO or CHIO operations. • A tag signal sequence error or a command error occurs, setting seek status register bit 8 or 9. • An out-of-parity command or out-of-parity write data is received. When this bit is reset through programming, seek status register bits 8 and 9 are also reset.

Bit	Description
14	**Requests Enabled.** This bit, when set, permits the disk adapter to initiate CHIO burst transfers and to present interrupt requests to the PCE. When this bit is reset, these functions are inhibited. This bit is only set through programming.
15	**Interrupt.** This bit is set when the disk adapter is attempting to present an I/O interrupt request to the PCE. If bit 14 (requests enabled) is reset, the interrupt request is held in the disk adapter until bit 15 is reset or bit 14 is again set.

*When this bit is set, BSTAT bit 15 (interrupt) is also set.

Programming Notes:

1. BSTAT bits 0–7 cannot be changed using the Set or Reset Disk BSTAT under Mask commands (hex 04 or 06). These bits can only be reset by resetting BSTAT bit 9 with the Reset BSTAT under Mask command (hex 04).

2. BSTAT bit 11 cannot be reset using the Reset BSTAT under Mask command (hex 04).

3. The Reset Disk Adapter command (hex 02) resets the disk BSTAT to zeros.

4. The contents of the disk BSTAT can be read by issuing the Read Disk BSTAT command (hex 07) and are returned to the program as a halfword operand.

Data Handler Extended Status Register

The data handler extended status register is a 2-byte register.

Bit	Description
0	**Buffer A to Disk.** This bit is controlled by the disk adapter. It indicates which of the 256-byte buffers is being used to transfer data to or from main storage. When this bit is set, buffer A is used to transfer data to or from the disk and buffer B is used to transfer data to or from main storage. When this bit is reset, buffer A is used to transfer data to or from main storage and buffer B is used to transfer data to or from the disk.
1	**Disk Speed Good.** This bit is set to indicate that the disk speed is correct. This bit is reset by the disk adapter when a speed error condition is detected.

Bit	Description
2–7	**ID Flags.** Each time an ID field is read from the disk, the contents of the flag byte, bits 2–7, are set into the data status register by the disk adapter. The flag bits correspond directly with the status register bits into which they are loaded. The flag bits are as follows: 2 Write protected field 1. 3 Write protected field 0. 4 Sector displaced. 5 Sector reassigned. 6 Sector defective. 7 Alternate sector.
8	**Reserved.** Always zero.
9	**Reserved.** Always zero.
10–15	**Residual Field Count.** Bits 10–15 reflect the contents of residual count register bits 10–15. When data transfer operations are ended without errors, these bits contain a hex zero value. If a data transfer operation is terminated with an error, the residual count register contains the number of data fields that remain to be transferred minus 1. This value is returned as the residual (bits 10–15) of the data handler extended status register.

Programming Note: The contents of the data handler extended status register can be read by issuing the Read Residual Count command (hex 05). Read-only access is provided for the contents of this register; the data handler extended status register cannot be written through programming. This register is reset to zeros by the Reset Disk Adapter command (hex 02). Bits 2–7 are not reset; they reflect the contents of the last flag byte read.

FCB Processor Status Register

The FCB processor status register is a 1-byte register. Its first two bits are reserved and are always set to "0, 0" ("1, 1" in the 8102). The other six bits identify error conditions detected by the disk adapter. This publication does not describe these bits in greater detail, because they are provided for maintenance use only.

Programming Note: Read-only access is provided for the contents of the FCB processor status register by issuing the Read FCB Processor Status Register command (hex 0B). When this command is executed by the disk adapter, byte 0 of the data returned to the program contains bits 0–7 of the disk BSTAT register and byte 1 contains the contents of the FCB processor status register.

Seek Status Register

The seek status register is a 1-byte register whose contents may be used for failure analysis or for error-recovery operations. Its bits are numbered from 8 to 15.

Bit	Description
8	**Tag Sequence Error.** This bit is set when an incorrect signal sequence is received by the disk adapter. When this bit is set, disk BSTAT bit 13 (equipment check) is also set. It is reset when BSTAT bit 13 (equipment check) is reset.
9	**Command Error.** This bit is set under the following conditions: • During a PIO operation directed to the disk adapter, an invalid command was received. • During a PIO operation directed to the disk adapter, a command with incorrect parity was received. • The disk adapter received a command that is not permitted while BSTAT bit 11 (busy) is set. These PIO commands are hex 08, 0B, 22, 24, 26, 2A, 2D, and 2E. When this bit is set, BSTAT bits 13 (disk equipment check) and 15 (disk interrupt request) are also set. It is reset when BSTAT bit 13 (disk equipment check) is reset.
10	**Card 1 Error.** This bit is set when the disk adapter detects incorrect parity on a PIO command or detects a byte of PIO write data that was received with incorrect parity. When this bit is set, BSTAT bit 9 (device error) and bit 15 (interrupt) are also set. It is reset when BSTAT bit 9 (device error) is reset.
11	**FCB Time-Out.** This bit is set when a minimum of 6.5 seconds (8 seconds for the 8102) have elapsed between channel requests to access control or data transfer operations. This condition can be caused through programming if BSTAT bit 12 (channel request frozen) or BSTAT bit 14 (requests enabled) is reset for this time period. When this bit is set, BSTAT bits 9 (device error) and 15 (interrupt) are also set. It is reset when BSTAT bit 9 (device error) is reset.
12	**Cable Continuity.** This bit is set as long as the cable path through the adapter is intact. This bit is only reset when the cable path through the adapter is interrupted; it cannot be set or reset through programming, or reset with system reset.
13–15	**Seek Activity Bits.** These bits indicate whether any of the following seek activities are in progress. • Moving Head Seek (MHS) • Fixed Head Select (FHS—8130, 8140, and 8101 only) • Head Shift (HDS—8102 only) • Recalibrate (RECAL)

These seek activities are designated by the following settings:

Bits 13, 14, and 15 Set To:	Description
000	No seek activities in progress.
001	A RECAL was begun and has not been completed.
010 (8130, 8140, and 8101 only)	An FHS operation was begun and has not been completed. No MHS or RECAL is in progress.
010 (8102 only)	An HDS operation was begun and has not been completed. No other seek activity is in progress.
100	An MHS operation was begun and has not been completed. No other seek activity is in progress.
101 (8130, 8140, and 8101 only)	An MHS operation was begun, followed by an FHS. The FHS has been completed, but the MHS has not.
110 (8130, 8140, and 8101 only)	An MHS operation was begun, followed by an FHS. Neither has been completed.
111 (8130, 8140, and 8101 only)	An MHS operation was begun, followed by an FHS. The MHS has been completed, but the FHS has not. No data transfer will begin until the FHS has been completed.

Programming Note: Read-only access is provided for the contents of the seek status register by using the Read Seek Status Register command (hex 0D). Byte 0 of the data returned to the program contains byte 0 of the disk BSTAT. Byte 1 contains bits 8–15 of the seek status register.

Data Transfer Operations

The following sections describe the PIO address assignments for the disk adapter, its priority level assignments, the PIO commands implemented by the disk adapter, and the CHIO operations implemented by the disk adapter. The last section in this chapter is a set of examples of data transfer operations performed by the disk adapter. These examples include the PIO operations needed to prepare the disk adapter for the CHIO operations that follow. The commands and CHIO operations are shown in the sequence in which they are executed by the disk adapter.

Disk Adapter PIO Address Assignments

The disk adapter PIO addresses depend upon the system component that contains the disk adapter. Address assignments for the disk adapters in each system component are listed in the following publications:

- *8101/8102 Storage and Input/Output Units Description*, GA27-2882
- *8130 Processor Description*, GA27-3196
- *8140 Processor Description*, GA27-2880

Ask your IBM representative for additional information on configuring an 8100 system and placing a system order.

I/O Interrupts

The disk adapter presents an I/O interrupt request to the PCE when BSTAT bits 14 and 15 are set. This interrupt request receives the appropriate priority level from the SSCF to which the adapter is attached.

Several adapters may be attached to one SSCF. The SSCF defines the priority level of each adapter by assigning it to a location in an interrupt translation array (ITA). An adapter's location in the ITA corresponds to the second hex digit of the adapter's PIO address. For example, the disk adapter with a PIO address of 91 is assigned to ITA location 1.

ITA also provides a means of assigning a unique identification to the interrupt request presented by the disk adapter, called the *sublevel assignment*. Both the priority level assignment and the sublevel assignment are defined in the ITA location to which the disk adapter is assigned, as illustrated in Figure 2-7.

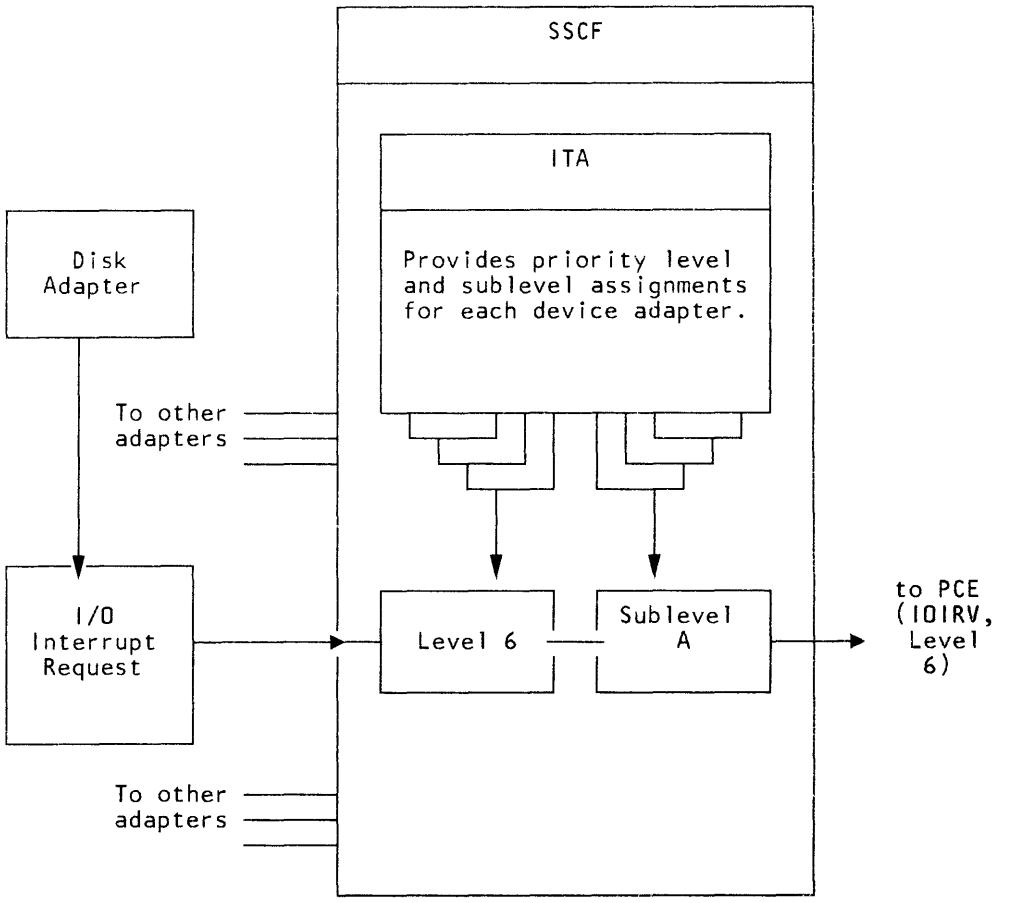


Figure 2-7. Priority and Sublevel Assignment in the ITA

For a detailed description of assigning priority levels and sublevels and of the ITA, refer to *IBM 8130 Processor Description*, GA27-3196, *IBM 8140 Processor Description*, GA27-2880, and *8101/8102 Storage and Input/Output Units Description*, GA27-2882.

Programmed I/O (PIO) Operations

Programs initiate PIO operations by executing I/O instructions to direct a command and one byte or one halfword of data to the disk storage facility. The channel and the disk adapter exchange control signals that ensure that the data and the control information are presented in the correct sequence. The PIO command determines whether data is transferred to or from the disk storage facility. The specific PIO commands implemented by the disk storage facility are described under "Disk PIO Commands." Specific I/O instructions and general programmed I/O operations are described in detail in the *8100 Information System Principles of Operation*, GA23-0031.

The disk adapter decodes and executes programmed I/O (PIO) commands as they are received from a program. These PIO commands are generally used to inspect or modify the contents of a status register, since they only transfer a halfword or a byte of data during their execution. PIO operations are also used to prepare the disk adapter for subsequent CHIO operations. The PIO command "Initiate CHIO" defines the beginning of a CHIO operation.

The following sections list and describe the disk PIO commands and the diagnostic error-recovery commands.

Disk PIO Commands

Code (in Hex)	Command Description
02	**Reset Disk Adapter.** This command resets all disk adapter status registers to hex 0 with the following exceptions: • Residual count register bits 2–7 reflect the contents of the last flag byte read by the disk adapter. These bits cannot be reset through programming. • Seek status register bit 12 (cable continuity) cannot be reset through programming. • The burst register is set to binary 111 (256-byte bursts). CHIO operations in progress when this command is executed are terminated by the disk adapter. After execution of this command, the disk adapter is disabled from presenting I/O interrupt requests to the PCE and from initiating CHIO operations. **Warning: Do not issue this command while the adapter is writing data to the file, because partial writes will result.**
04	**Reset Basic Status under Mask.** This command resets basic status register (BSTAT) bits that are selected by the mask operand. The mask bits correspond directly to the BSTAT bits. A mask bit with the value 1 resets the associated BSTAT bit; a mask bit with the value 0 does not affect the associated BSTAT bit. Only BSTAT bits 8–10 and 12–15 can be reset using this command. BSTAT bits 0–7 and bit 11 (busy) cannot be changed using this command.
05	**Read Residual Count.** This command causes the disk adapter to return the contents of the data status register to the program. Bits 0 – 15 of the data status register correspond directly to bits 0 – 15 of the data returned to the program. Bits 8, 9 are always returned as zeros.
06	**Set Basic Status under Mask.** This command transfers a mask operand to the disk adapter. The mask operand corresponds directly to bits 8 – 15 of the disk BSTAT. Active mask bits cause the corresponding BSTAT bits to be set, except for bits 0–7 and bit 11 (busy); these bits cannot be set using this command. When mask bits are set to zero, the corresponding BSTAT bit is not changed.

Code (in Hex)	Command Description
07	**Read Disk Basic Status.** This command causes the disk adapter to return the contents of the disk BSTAT to the program. This command is executed by the disk adapter regardless of whether a CHIO operation is in progress.
08*	**Initiate.** This command causes the disk adapter to set BSTAT bit 11 (busy) and to begin a CHIO operation after execution of this command. The program must define a channel control vector (CHCV) in the data operand that is sent to the disk adapter with this command. The CHCV sent by the program is loaded into bits 3–5 and 10–14 of the adapter CHCV register during the execution of this command. The disk adapter generates the remainder of the CHCV that is presented to the channel when the CHIO operation is initiated. **Programming Note:** Bits 3 and 4 of the CHCV are reserved and must contain zeros. If a CHCV is sent to the PCE's channel logic with 1's in either bit 3 or bit 4, a system check interrupt request is presented to the PCE and the CHIO operation is terminated. This command causes the disk adapter to fetch the first control operation from the function control block (FCB) in main storage. FCBs are described in this chapter under "Disk Channel I/O Operations." The control operations implemented by the disk adapter are described later under "CHIO Control Operations."
0A	**Terminate CHIO.** This command causes the disk adapter to terminate the CHIO operation in progress. The disk adapter presents an interrupt request to the PCE by setting BSTAT bit 15 (interrupt request) when the CHIO operation has been terminated. Termination of the current CHIO operation can be delayed by the disk adapter under the following circumstances: 1. When a multisector transfer is in progress, the CHIO operation is not terminated until all sectors have been transferred. 2. If a moving head seek operation was begun and a fixed head selection was begun before the moving head seek was completed, the CHIO operation is not terminated until the fixed head selection is completed. The disk adapter does not wait for completion of the moving head seek operation before setting BSTAT bit 15. 3. If a moving head seek is in progress, a fixed head selection has been completed, and a data transfer operation has been accessed, the data transfer operation is completed before the CHIO operation is terminated and BSTAT bit 15 is set by the disk adapter.

Code (in Hex)	Command Description
0B*	**Read FCB Status Register.** This command causes the disk adapter to return BSTAT byte 0 in bits 0–7 of the data returned to the program. Bits 8 and 9 of the returned data are set Bits 8 and 9 of the returned data are set to 1, 1 (0, 0 in 8102 only). Bits 10–15 contain the diagnostic error code currently in the FCB status register. If the disk adapter is performing CHIO operations (that is, if BSTAT bit 11—busy—is set when this command is received) the disk adapter suppresses the response to the channel, forcing a system check interrupt request to be presented to the PCE through error interrupt request vector bit 1 (I/O time-out check). When the channel detects the time-out condition, it activates the Halt signal to terminate the current I/O operation. The CHIO operation in progress at the time this command was received is also terminated because of the Halt signal.
0C	**Reset Disk.** This command causes the Reset Error line to be activated to the disk. The Reset Error line is used by the disk to reset the Data Unsafe and Command Error sense bits and certain file interrupts.
0D	**Read Seek Status.** This command causes the disk adapter to return BSTAT byte 0 in bits 0–7 of the data returned to the program. Bits 8–15 of this data are returned from the seek status register.

*If these commands are received when the disk adapter is busy (disk BSTAT bit 11 set to 1), the disk adapter terminates the current operation with a command reject error. Command reject is described under "Disk Adapter Error Detection and Reporting."

The following commands are used only to perform diagnostic analysis of the disk adapter hardware and to help restore the state of the disk adapter through programming during an error-recovery procedure. These commands are not used during normal programmed operations with the disk adapter to control data transfer sequences to or from the disk or the disk adapter hardware.

Code (in Hex) — **Command Description**

21 — **Read Burst, Skip Factor, and Spiral Register.** This command causes the disk adapter to return the following halfword data operand to the program:

Bit	Setting
0–5	Set to zeros.
6, 7	Contain the spiral value.
8, 9	Contain the skip factor.
10–12	Set to zeros.
13–15	Contain the burst length.

22* — **Write NFR.** This command causes the halfword operand received from the program to be written into the operation register.

24 — **Write FCB CHCV.** This command causes the disk adapter to load the halfword operand received from the program into the control CHCV register.

26* — **Write Data CHCV Register.** This command causes the disk adapter to load the halfword data operand received from the program into the data CHCV register.

29 — **Read Seek Register.** This command causes the disk adapter to return the contents of the seek register to the program as a halfword operand in the following format:

Bit	Setting
0	Contains the recalibrate bit.
1–5	Contain the head selection.
6	Set to zero.
7–15	Contain the cylinder selection.

Code (in Hex)	Command Description
2A*	**Load Seek Register from NFR.** This command causes the disk adapter to load bits 2–6 and bits 7–15 from the NFR into the seek register. Seek register bit 0 (recalibrate) is set only if bits 0, 1 of the NFR are set to binary 01. No data operand is transferred from the program during execution of this command.
2D*	**Read First Value.** This command causes the disk adapter to return the contents of the first value register to the program in bits 0–7 of the data returned. The contents of the pulsing register are returned to the program as bits 8–15 of the data operand.
2E*	**Write First Value.** This command causes the disk adapter to load bits 0–7 of the data received from the program into the first value register.
31,33,35,37*	**Read Data CHCV.** These commands cause the disk adapter to return the contents of the data CHCV register to the program as follows:

Bit	Setting
0–2	Set to zeros.
3–5	Returned from the data CHCV register.
6	Set to zero.
7–9	Set to the following values, depending on the specific command code issued by the program:

Command	Value of Bits 7, 8, 9 (in Binary)
Hex 31	1 1 1
Hex 33	0 0 0
Hex 35	0 1 0
Hex 37	0 1 1

10–14	Contain the low-order 5 bits of the channel pointer (CHP) number from the data CHCV register.
15	Set to zero.

39	**Read NFR.** This command causes the disk adapter to return the contents of the NFR to the program as a halfword data operand. Bits 0–15 of the NFR correspond directly with bits 0–15 of the data returned to the program.

Code (in Hex)	Command Description
3B,3D,3F	**Read FCB CHCV.** These commands cause the disk adapter to return the contents of the control CHCV register to the program as follows:

Bit	Setting
0–2	Set to zeros.
3–5	Returned from the control CHCV register.
6, 7	Set to zeros.
8, 9	Set to the following values depending on the specific command issued by the program:

Command	Value of Bits 8, 9 (in Binary)
Hex 3B	0 0
Hex 3D	1 0
Hex 3F	1 1

10–14	Contain the low-order 5 bits of the channel pointer (CHP) number from the control CHCV register.
15	Set to zero.

* This command is not permitted while a CHIO operation is in progress with the disk adapter. Disk BSTAT bit 11 (busy) is set throughout a CHIO operation. If this command is received while BSTAT bit 11 is set, the disk adapter suppresses the response for the command to force a time-out condition to be detected by the channel. This condition results in a system check interrupt request for priority level 0 in the PCE.

Disk Channel I/O (CHIO) Operations

The 8100 disk storage facility uses CHIO operations to transfer data between main storage and the disk. A program uses PIO commands to prepare the disk adapter for a CHIO operation and to indicate when that CHIO operation is to be started. The disk adapter performs the data transfer operations asynchronous to program execution in the PCE. CHIO operations are described in this section and, in detail, in the *8100 Principles of Operation*.

The disk adapter implements a special set of data protocols, used only during CHIO operations, that define additional control functions and specify data transfer operations that are to be performed during one CHIO operation. These control and data transfer operations are defined in main storage in an area called a *function control block* (Figure 2-8).

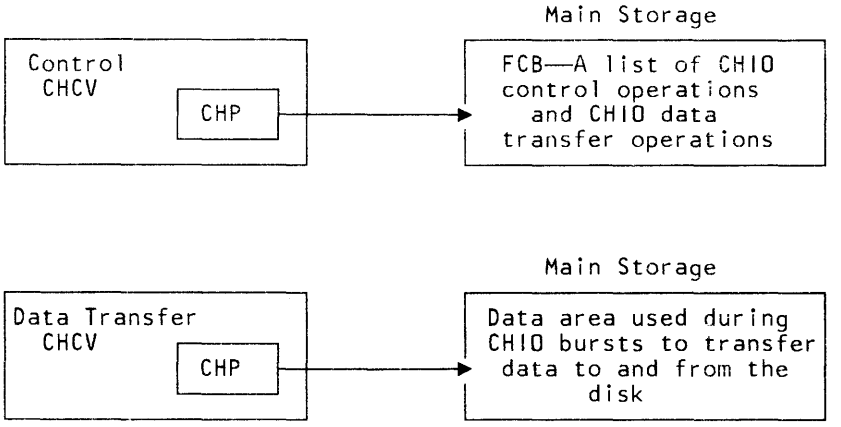


Figure 2-8. Function Control Block (FCB)

The function control block (FCB) is an area in main storage where a program has defined one or more control or data transfer operations to be accessed and performed by the disk adapter during a subsequent CHIO operation. The location of the FCB is identified in a channel pointer (CHP). This CHP is defined in the control CHCV that is sent to the disk adapter with the Initiate CHIO command (hex 08). The disk adapter uses the control CHCV to access control and data transfer operations; the data transfer CHCV is used only during CHIO bursts to transfer data to or from the disk.

FCBs can contain two types of operations: control operations and data transfer operations. Control operations position the access mechanism and load control information into certain registers in preparation for subsequent CHIO data transfer sequences. Data transfer operations cause data to be read from or written to the disk. Because these data transfer operations occur during a CHIO operation, the disk data is sent to, or received from, an area in main storage identified by the CHP in the data transfer CHCV.

Note: FCBs, in effect, form a program for the channel and thus are a branch instruction.

The FCB allows a program to specify a list of operations to be performed during a CHIO operation. One CHIO operation consists of one or more burst transfers between the disk adapter and main storage. When the Initiate CHIO command is completed and the control CHCV has been loaded into the control CHCV register, the disk adapter initiates the first channel request for a burst transfer. When the PCE grants that request, the disk adapter returns the control CHCV to the channel to identify that the first control operation is to be fetched from the FCB in main storage. When the first control operation is accessed, the first burst transfer is ended and the disk adapter performs the specified function. When the disk adapter has completed the first control operation, a channel request signal is activated for the next burst transfer. The next control operation is then accessed using the control CHCV. These bursts continue until the disk adapter accesses a data transfer operation. When the data transfer operation has been transferred to the disk adapter, the burst transfer is again complete. However, for this operation, data must be transferred between the disk and main storage.

The data transfer operation defines the direction in which the data is to be transferred. For this presentation, a read operation is assumed. The selected data is located on the disk and read into the available data buffer (A or B). When the selected data has been read, the disk adapter inverts the buffer control bit in data status register bit 9 (buffer A to disk) and activates the channel request signal to request another burst transfer. When the request is granted, the disk adapter sends the data CHCV to the channel, specifying the CHP that contains the address in main storage where the disk data is to be read. While this data is being transferred to main storage, the disk adapter can read the next data field into the other data buffer (if the residual count register specifies that more than one data field is to be transferred). The burst register determines the length of each burst transfer, and may contain a value that causes several burst transfers to occur while the data field is being transferred to main storage. Each burst transfer performed while the data field is being transferred is accompanied by the data CHCV. When the data field or fields have been transferred, the disk adapter requests another burst transfer to determine if the CHIO operation is to be ended with an End Operation code, or if another control or data transfer operation is to be performed. The control CHCV is always used to access control or data transfer operations. See Figure 2-9.

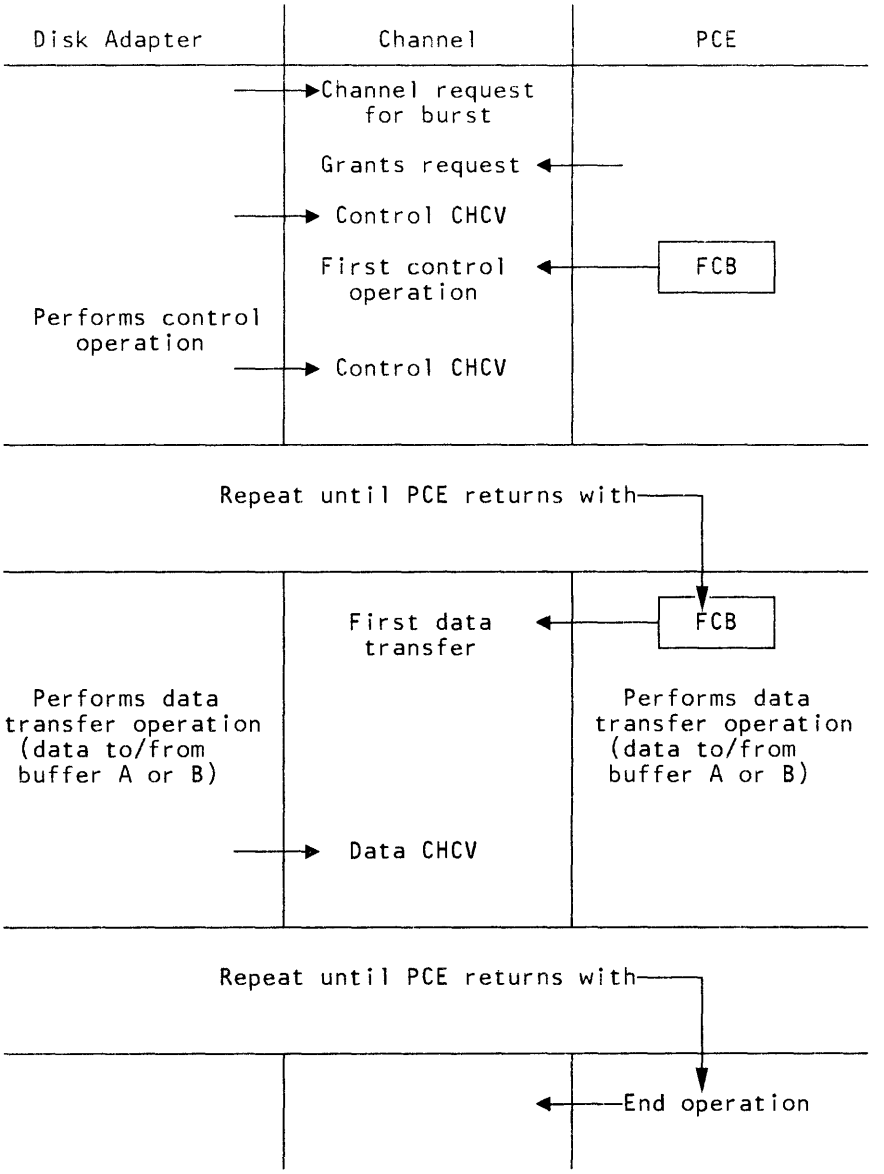


Figure 2-9. Example of a Channel I/O Operation

Programming Note: Each burst transfer is a complete CHIO operation to the PCE's channel logic. However, the program initiates a series of CHIO operations (or, in some cases, a single CHIO operation) with the disk adapter when it issues the Initiate CHIO command (hex 08). The disk adapter is busy (BSTAT bit 11, busy, is set to 1) from the time the Initiate CHIO command is executed until an error is detected, the End Operation control operation is received, or the Terminate CHIO command (hex 0A) is executed. The program then views the execution of a series of control and data transfer operations as a single CHIO operation.

Command Reject error is reported to the program if one of the following command codes is received by the disk adapter: *hex 08, 0B, 22, 24, 26, 2A, 2D, 2E.*

If a write operation is terminated by the Command Reject error, the CRC or ECC bytes for the field being written *may not be written on the disk*. Disk data or ID fields without correct ECC or CRC bytes cannot be read during normal programmed operations. If a write operation is prematurely terminated, the data must be correctly written on the disk before that field can be used.

CHIO control and data transfer operations are described in detail later in this chapter. Control operations are described separately from data transfer operations; each is preceded by a summary list that identifies the basic format and name assigned to each operation.

CHIO Request Priority

The disk adapter is assigned to the CR-lo priority chain in the SSCF to which it is attached. The channel request priority (CRP) value assigned to each SSCF is detailed in the 8130 and 8140 processor description manuals under "Channel I/O Operations."

CHIO Control Operations

This section describes each control operation implemented by the disk adapter. These control operations do not result in data transfers to or from the disk; rather, they are used to position the access mechanism and to set up the disk adapter for a subsequent data transfer operation. Only the codes described in this section are valid for use with the disk adapter; issuing control operations other than those described in this section will provide unpredictable results. Data transfer operations are described in the next section.

Code	Operation Description
Hex 0000 or 1000	**End Op.** Defines the end of an FCB. When this control operation is decoded by the disk adapter, the current CHIO operation is ended. BSTAT bit 11 (busy) is reset and BSTAT bit 15 (interrupt request) is set to present an interrupt request to the PCE if bit 14 (disk enabled) is also set. Both the hex 0000 and 1000 values cause the same actions by the disk adapter.
Hex 4200	**Recalibrate.** This code causes the disk adapter to recalibrate the access mechanism and to position it at Track 0. The selection of moving head 00001 is forced by the disk adapter. Seek register bit 0 (recalibrate) is set during execution of this operation. If the disk adapter detects an error during execution of this operation, a disk error condition exists, and the error is indicated as follows: • Seek status register bits 10–15 are set to hex 3A (disk error, data transfer inactive). • Disk BSTAT bit 9 (disk adapter error) and bit 15 (disk interrupt request) are set.

Code	Operation Description
Binary 10hhhhhccccccccc (8130, 8140, and 8101 only)	**Seek.** This code causes the disk adapter to perform a seek operation. (In this code, *h* designates head selection and *c* designates cylinder selection.) In the 8130, 8140, and 8101, the following head selection field settings determine the type of seek: **Binary 1hhhh** Fixed head select operation **Binary 0hhhh** Moving head seek operation These values are loaded into bits 2–15 of the seek register for subsequent ID field verification. After the disk adapter has decoded a moving head seek operation, loaded the seek register, and initiated the access operation, the next control operation is fetched by the disk adapter. The disk adapter decodes the next operation and executes it under the following conditions: • If a moving head seek is active and a fixed head is not selected by the next operation, the disk adapter can execute any operation except a second moving head seek, a recalibrate operation, a data transfer operation, or an end op. • If a moving head seek is active and a fixed head select operation has been executed since the moving head seek was initiated, a data transfer operation using the fixed head can be executed. The disk adapter cannot execute a recalibrate operation, an end op, or a second moving head seek.
Binary 10chhhhccccccccc (8102 only)	**Seek.** (Described above.) In the 8102, the code causes a moving head seek operation only.
Binary 11hhhhhccccccccc (8130, 8140, and 8101 only)	**Load Seek Register.** This code causes the disk adapter to load the new head and cylinder values into the seek register. (In this code, *h* designates head selection and *c* designates cylinder selection.) No access motion is initiated during this operation, and no head is selected by the disk adapter.

Code	Operation Description
Binary 11chhhhccccccccc (8102 only)	**Load Seek Register.** (Described above.)
Hex 0800	**No Op.** This code causes the disk adapter to access the next control operation from main storage. No operation is performed by the disk adapter when this operation is accessed. In addition to the defined value for the No Op function (hex 0800), 23 codes in bits 0–7 of the control operation are not implemented by the disk adapter. These codes result in the same action as the hex 0800 code when they are accessed by the disk adapter. The following 23 codes also do not result in disk adapter operations: *hex 0B, 0C–0F, 40, 41, 43, 44–47, 54–56, and 58–5F.* When these values are detected in bits 0–7 of the control operation, the disk adapter ignores the contents of bits 8–15 and decodes the operation as a No Op.
Hex 0900	**Program-Controlled Interrupt (PCI).** This code causes the disk adapter to set BSTAT bit 8 (PCI) and bit 15 (disk interrupt request). The current CHIO operation is not affected when the disk adapter presents an interrupt request to the PCE. The interrupt request is presented to the PCE when BSTAT bit 14 is also set; if BSTAT bit 14 (enabled) is not set, the interrupt request with the PCI status bit is held in the disk adapter until BSTAT bit 14 is again set.
Hex 0A0b	**Load Burst Register.** This code causes the disk adapter to load the burst value from bits 13–15 of the control operation into the burst register. (In this code, *b* designates the 3-bit burst value.) The burst value specifies the number of halfwords of data to be transferred during one CHIO transfer sequence. Burst values are listed with their corresponding burst lengths under "Burst Register."
Binary 00011000ssCCCCCC	**Load Skip Factor/Field Count.** This code causes the disk adapter to load bits 8, 9 from the control operation into the skip factor register, and to load bits 10–15 from the control operation into the residual count register. (In this code, *s* designates the skip factor and *C* designates the field count value.) Skip factor values (bits 8 and 9) are listed with their corresponding skip factors under "Skip Factor Register."

Code	Operation Description
	The field count values are specified in the range 0 to 63, where the specified value is 1 less than the actual number of data fields to be transferred during execution of the next data transfer operation. When one data field is to be transferred, a field count value of 0 is specified. A field value of 63 results in the transfer of 64 data fields.
Hex 5000 CHCV	**Load New Control CHCV.** This code causes the disk adapter to load the new CHCV value into the control CHCV register. The new CHCV to be loaded is defined in the main storage halfword location immediately following the control operation.
Hex 5100 CHCV	**Load New Data Transfer CHCV.** This code causes the disk adapter to load the new CHCV value into the data transfer CHCV register. The new CHCV to be loaded is defined in the main storage halfword location immediately following the control operation.
Hex 5200 ADDR	**Load New Address into Control CHP Bytes 2 and 3.** This code causes the disk adapter to load the received address value into bytes 2 and 3 of the CHP identified in the control CHCV register. The address value is specified in the halfword location immediately following the control operation. **Note:** The values hex 48–4F and 68–6F are reserved for maintenance.
Hex 5700 ADDR	**Load New Address into Data CHP Bytes 0, 1.** This code causes the disk adapter to load the received address value into bytes 0, 1 of the CHP identified in the data CHCV register. The address value is specified in the halfword location immediately following the control operation.

The values hex 48–4F and 68–6F are reserved for maintenance use.

CHIO Data Transfer Operations

Data transfer operations implemented by the disk storage control are two bytes long and contain information that describes the specific disk data to be transferred, the direction of data transfer, and the address of the sector at which the data transfer is to begin. Throughout the remainder of this description, data transfer operations are described in this format: nnXX.

Bit	Description
0–7 (nn)	Contain two hex characters that identify the data transfer operation.
8–15 (XX)	Contain the physical sector number and the data field with which the data transfer is to begin.
9–14	Contain the physical sector number.
15	Identifies whether the data transfer begins with data field 0 or data field 1. If bit 15 = 0, data field 0 is the first data field to be read or written in the selected sector; if bit 15 = 1, data field 1 is the first data field to be read or written in the selected sector.

The remainder of this section describes each data transfer operation implemented by the disk adapter. Only the operations described section are valid for use with the disk adapter; issuing data transfer operations other than those described in this section will give unpredictable results.

Note: In CHIO data transfer operations where a successful comparison is made between the selected sector value in the NFR and the sector value in the disk ID field, a successful comparison is also required between the head and cylinder values in the seek register and those in the disk ID field. If there is an unsuccessful comparison of the head or cylinder values, disk BSTAT bit 3 (ID error), BSTAT bit 9 (device error), and BSTAT bit 15 are set. An interrupt request is presented to the PCE if BSTAT 14 (request enabled) is also set.

Code (in Hex)	Operation Description
20XX	**Read ID–Normal.** This code causes the disk adapter to locate the specified sector using the physical sector counter (PSC). When the PSC value is equal to the selected sector, the 4-byte ID field is read, the flag field is checked, and, if the flag field does not indicate that the sector is displaced, the contents of the ID field are returned to main storage using the CHP in the data transfer CHCV. If flag bit 4 (sector displaced) is set in the ID field, the disk adapter automatically reads the ID field of the next sequential sector, compares its sector value with the selected sector value in the NFR, and transfers the ID field to main storage if the sector value compares. If a CRC error is detected on the ID field, the data will not be transferred until the adapter has attempted to recover the data. If the data cannot be recovered, no data will be transferred to main storage. BSTAT bits 2, 3, 9, and 15 are set to indicate that a read error occurred in an ID field. An interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.

Code (in Hex)	Operation Description
24XX	**Read ID—Compare.** This code causes the disk adapter to read each sector ID field on the track comparing the sector field value with the selected sector value in the NFR until either a compare is made (selected sector located) or the comparison has been unsuccessfully attempted for a complete revolution of the disk. When the selected sector is located, the 4-byte ID field is transferred to main storage using the CHP in the data transfer CHCV. If the selected sector cannot be located in a complete revolution of the disk, BSTAT bits 5, 9, and 15 are set to indicate that the sector could not be located. If BSTAT bit 14 is set, an interrupt request is presented to the PCE. If a CRC error is detected on the ID field, no data is transferred to main storage. BSTAT bits 2, 3, 9, and 15 are set to indicate that a read error occurred in an ID field. An interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.
21XX	**Read ID—Displaced.** This code causes the disk adapter to locate the selected sector using the value in the PSC. When the PSC value is equal to the selected sector, the 4-byte ID field is read from an area displaced 64 bytes into data field 0. The 4-byte ID field is transferred to main storage using the CHP in the data transfer CHCV. If flag bit 4 (sector displaced) is set, the disk adapter automatically reads the ID field of the next sector, compares its sector field value with the selected sector value in the NFR, and transfers the ID field to main storage if the sector values compare. If a CRC error is detected on the ID field, no data is transferred to main storage. Rather, BSTAT bits 2, 3, 9, and 15 are set to indicate that a read error occurred in an ID field. An interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.
23XX	**Read ID at PSC.** This code causes the disk adapter to locate the selected sector using the PSC value. No comparison is made with the selected sector value in the operation register. The 4-byte ID field is transferred to main storage using the CHP in the data transfer CHCV. If a CRC error is detected on the ID field, BSTAT bits 2, 3, 9, and 15 are set to identify that a read error was detected in an ID field. No data is transferred and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.

Code (in Hex)	Operation Description
26XX	**Read ID—Immediate.** This code causes the disk adapter to read the first sector ID field met after this code is received. The head and cylinder values in the ID field are compared with the head and cylinder values in the seek register; no comparison is performed on the sector byte in the ID field. A comparison of the seek register head and cylinder values with the values in the ID field permits the disk control to transfer the 4-byte ID field to main storage using the CHP in the data transfer CHCV. If a CRC error is detected on the ID field being read, the disk adapter automatically reads the next sector's ID field. If the head and cylinder values in the ID field do not compare with the values in the seek register, the next ID field is read. If no comparison can be made during one complete revolution of the disk, BSTAT bits 5, 9, and 15 are set to identify that the comparison of head and cylinder values did not occur. No data is transferred, and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.
28XX	**Write ID.** This code causes the disk adapter to access the 4-byte ID field data from main storage using the CHP in the data transfer CHCV. The PSC is used to locate the correct physical sector on the disk. The disk adapter then writes the new ID field using the flag, sector, head, and cylinder information received from main storage. **Programming Note:** Before this operation is initiated, the program must read the ID field for this sector so that the contents of the flag byte can be reproduced to preserve the integrity of the disk. After the ID field is written, the program must read the ID field and compare it with the ID written to ensure the integrity of the ID field. If execution of this command is abruptly terminated because of a Command Reject error or a disk equipment check error, the CRC bytes are not written on the disk at the end of the field. The program must correctly rewrite this field to prevent unrecoverable read errors during subsequent read operations.
29XX	**Write ID—Displaced.** This code causes the disk adapter to access the 4-byte ID field data from main storage using the CHP in the data transfer CHCV. When the PSC indicates the location of the selected sector, the disk control logic writes the next ID field in an area displaced 64 bytes into the zero sector. **Programming Note:** Refer to the programming note for the Write ID operation.

Code (in Hex)	Operation Description
30XX	**Read Data Field.** This code causes the disk adapter to locate the selected sector using the PSC and to read the ID field. If the flag byte does not indicate defective, reassigned, or displaced, the adapter compares the sector number with the value specified in this operation. If the sector number matches, the adapter compares the head/track with the seek register and then verifies the ID CRC. If no error occurs in the ID field and the disk adapter reads the data field selected in bit 15 of this operation into the available data buffer. When more than one field is to be read, as indicated by a field count value greater than 0 in the residual count register, the disk adapter inverts data status register bit 0 (buffer A to disk) to indicate which buffer is to be transferred to main storage and which buffer is to be loaded with disk data, and reads the next data field from the disk. The skip factor value determines the location of the next data field to be accessed from the disk. Regardless of whether another data field is to be read from the disk, when data status register bit 0 (buffer A to disk) is inverted, the disk adapter transfers the 256 bytes of disk data from buffer A or B to main storage using the CHP in the data transfer CHCV. The burst length value determines how many channel transfer sequences are required to transfer the data to main storage. When several data fields are to be read, the transfer of one data field from the buffer to main storage occurs at the same time as the next data field is being read from the disk. If the sector displaced flag is set in the ID field of the selected sector, the disk adapter automatically reads the ID field of the next sequential sector before comparing the selected sector value in the NFR with the sector byte in the ID field. If a CRC/ECC error is detected on the ID or on a data field, the operation is terminated with BSTAT bits set to indicate that a read error was detected either on the ID field or on a data field. The data field in error is not transferred to main storage, and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.
34XX	**Read Data Field—Compare.** This code causes the disk adapter to compare the sector byte in the ID field of each sector with the selected sector value in the NFR. When a comparison is made, the data field selected in bit 15 of this operation is read into the available data buffer. When the buffer is loaded, the disk adapter inverts data status register bit 0 (buffer A to disk) and transfers the 256 bytes of data to main storage using the CHP in the data transfer CHCV. If additional data fields are to be transferred, the disk adapter reads the next data field into the other buffer while the contents of buffer A or B are being transferred to main storage.

Code (in Hex)	Operation Description
	If no comparison is made on the selected sector value after a complete revolution of the disk, the operation is terminated with BSTAT bit 5 (sector not found) and bit 9 (disk adapter error) set, and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set. CRC errors detected on ID fields cause the disk adapter to read the next ID field for comparison. Noncorrectable ECC errors detected on a data field being accessed terminate the operation with BSTAT bits set to indicate that a read error was detected on the data field. No data is transferred, and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.
38XX	**Write Data Field.** This code causes the disk adapter to fetch 256 bytes of data from main storage using the CHP in the data transfer CHCV. When the data has been transferred to buffer A or B, the disk adapter inverts data status register bit 0 (buffer A to disk) to indicate that the contents of that buffer are to be written to the disk. When the PSC value indicates that the selected sector has been reached, the ID field of that sector is read. If the flag byte does not indicate defective, reassigned, or displaced, and the sector byte compares with the selected sector value, the data field selected in bit 15 of this operation is written using the data from the buffer loaded from main storage. If the flag byte indicates displaced, the disk adapter automatically reads the ID field from the next sequential sector on the disk for comparison with the selected sector value in the NFR. If the field count value in the residual count register indicates that more than one data field is to be written during this operation, the disk control accesses the next 256 bytes of data from main storage into the available data buffer while the first data field is being written on the disk. During the data transfer from main storage, the CHP in the data transfer CHCV is used by the disk adapter. The value in the burst length register determines the number of channel transfer sequences required to access each 256-byte data field to be written. If no comparison can be made between the sector byte read from the disk and the selected sector value in the NFR, BSTAT bit 5 (sector not found) and bit 9 (disk adapter error) are set, no data is written on the disk, and an interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set.

Code (in Hex)	Operation Description
	Programming Note: The Write Data Field operation does not verify the CRC/ECC bytes written with each data field. A Read-Back Check or Read-Back Check Compare operation may be used to verify that the CRC/ECC bytes match the data fields written on the disk. If each data field is verified before the source data from which the field was written is destroyed, is scratched, or otherwise becomes unavailable, temporary write error conditions can be detected and corrected. Failure either to use a Read-Back Check operation or to read the data field to verify that the CRC/ECC bytes match the data fields on the disk can result in a permanent read error when the record is next accessed. If execution of this command is abruptly terminated because of a Command Reject error or a disk equipment check error, the CRC/ECC bytes are not written on the disk at the end of the field. The program must correctly rewrite this field to prevent unrecoverable read errors during subsequent read operations.
3CXX	**Write Data Field—Compare.** This code causes the disk adapter to fetch 256 bytes of data from main storage and to set data status register bit 0 (buffer B to storage) to identify which data buffer is to be written to the disk. For this operation, the ID field of each sector is read, and the sector byte is compared with the selected sector value in the NFR. When the sector values compare and the flag field does not contain the defective or write protect bits for the selected field, the data in the buffer identified by data status register bit 0 (buffer A to disk) is written to the disk in the data field selected by bit 15 of the NFR. If the field count value in the residual count register indicates that more than one data field is to be written during this operation, the data transfer from main storage is overlapped with the writing of the first data field as described for the Write Data Field operation. If no comparison can be made between the ID field sector byte and the selected sector value during one complete revolution of the disk, BSTAT bit 5 (sector not found) is set with BSTAT bit 9 (device error), no data is written to the disk, and an interrupt request is presented to the PCE if BSTAT bit 14 (request enabled) is also set. **Programming Note:** The Write Data Field—Compare operation does not verify the CRC/ECC bytes written with each data field. A Read-Back Check or Read-Back Check Compare operation may be used to verify that the CRC/ECC bytes match the data fields that are written on the disk. If each data field is verified before the source data from which the field was written is destroyed, is scratched, or otherwise becomes unavailable, temporary write error conditions can be detected and corrected. Failure either to use a Read-Back Check operation or to read the data field to verify that the ECC bytes match the data fields on the disk can result in a permanent read error when the record is next accessed.

Code (in Hex)	Operation Description
	If execution of this command is abruptly terminated because of a Command Reject error or a disk equipment check error, the CRC/ECC bytes are not written on the disk at the end of the field. The program must correctly rewrite this field to prevent unrecoverable read errors during subsequent read operations.
60XX	**Read-Back Check.** This code causes the disk adapter to locate the selected sector using the value in the PSC and to read the ID field of that sector. The sector byte in the ID field is compared with the selected sector value in the NFR. When a comparison exists, and the flag byte does not indicate defective, reassigned, or displaced, the contents of the selected data field are read into the available data buffer. No data is transferred to main storage; the purpose of this operation is to verify integrity of the data in the field being read. More than one data field may be verified by defining a multi-field count value in the residual count register. If a CRC/ECC error is detected, BSTAT bits 2 and 4 are set with bits 9 and 15 to indicate that a CRC/ECC error was detected on the data field being read. An interrupt is presented to the PCE if BSTAT bit 14 is also set. **Programming Note:** Read-Back Check operations may be used to verify each data field written on the disk. Verifying each data field before its source data becomes unavailable allows temporary write error conditions to be detected and corrected. Failure to verify data fields written on the disk can result in permanent read errors the next time a data field containing a CRC/ECC error is accessed.
64XX	**Read-Back Check—Compare.** This code causes the disk adapter to compare the sector byte of each ID field on the track with the selected sector value in the NFR. When a comparison is made, the selected data field is read into the available buffer in the disk control, but no data is transferred to main storage. More than one data field can be verified using this operation by defining a field count value greater than hex 0 in the residual count register. If a CRC/ECC error is detected, BSTAT bits 2, 4, 9, and 15 are set to indicate that a CRC/ECC error was detected on the data field. An interrupt request is presented to the PCE if BSTAT bit 14 (enabled) is also set. If no comparison is made between the sector byte of the ID field and the selected sector value in the NFR after one complete revolution of the disk, BSTAT bit 5 (sector not found) is set with bits 9 and 15. An interrupt request is presented to the PCE if bit 14 (enabled) is also set.

Code (in Hex)	Operation Description
	Programming Note: Read-Back Check–Compare operations may be used to verify each data field written on the disk. Verifying each data field before its source data becomes unavailable allows temporary write error conditions to be detected and corrected. Failure to verify data fields written on the disk can result in permanent read errors the next time a data field containing a CRC/ECC error is accessed.
70XX (8130, 8140, and 8101)	**Read CRC.** This code transfers to main storage the CRC of the data field defined by bit 15.
70XX (8102)	**Get Syndrome.** This code transfers to main storage the contents of the ECC Syndrome register in the Data Handler.
	Programming Notes:
	1. When the ECC Syndrome register is read out, the most significant byte is destroyed. Therefore, if a Data Handler error occurs during transfer of the syndrome to main storage, the Get Syndrome FCB operation should not be retried. Instead, a Buffer Diagnostic operation should be used to get the syndrome from the buffer currently attached to main storage. (Data Handler Extended Status Register bit 0 indicates the correct buffer.)
	2. The second byte of the Get Syndrome operation code has no significance. Hex 7000 through hex 70FF will perform the Get Syndrome operation.
71XX	**Retrieve Field.** This code causes the disk adapter to use the PSC to locate the selected sector's physical location on the disk. When the PSC indicates that the selected sector has been located, the disk adapter reads the selected data field into the available buffer. No ID comparison is performed; a data field CRC/ECC error does not inhibit this read operation and is not reported to the PCE; however, the data returned to main storage is not guaranteed to be separated into bytes, and may be skewed from one to seven bits. This operation is to be used only as a last resort to recover data from a sector that has become defective since the data was written and verified.
	The 256 bytes of data are transferred to main storage using the CHP in the data transfer CHCV. Only one data field is transferred by this operation.

Code (in Hex)	Operation Description
78XX	**Format Sector.** This code causes the disk adapter to access 62 bytes of data from main storage using the CHP in the data transfer CHCV. This data is used to define the format of the sector to be written on the disk. When the data has been transferred into the available data buffer, data status register bit 0 (buffer A to disk) is inverted to indicate which 256-byte data buffer contains the data to be written. Using the PSC value to locate the selected physical sector, the disk adapter writes the entire sector format on the disk. From the 62 bytes provided by the program, the disk adapter writes 572 bytes of data on the disk. The program specifies one byte that is to be repeated 256 times for each data field by the disk adapter. The 62 bytes of data provided by the program are arranged in the following format:

Bytes	Value
14 leading sync area bytes	Hex 00.
1 byte sync character byte	Hex 01.
4 ID field bytes	Flag, sector, head, and cylinder values for this sector.
2 ID CRC bytes	Computed from ID field value.
16 sync area bytes (14 in 8102 only)	Hex 00.
1 byte sync byte	Hex 01.
1 data field 0 character byte	Any value. This character is repeated 256 times to define data field 0.
2 data field 0 CRC/ECC (4 in 8102 only)	Computed from data field 0 value.
16 sync area bytes (14 in 8102 only)	Hex 00.
1 byte sync byte	Hex 01.
1 data field 1 character byte	Any value. This character is repeated 256 times to define data field 1.
2 data field 1 CRC/ECC bytes (4 in 8102 only)	Computed from data field 1 value.
1 trailing character byte	Hex 00.

Code (in Hex)	Operation Description
	Programming Note: When the sector data is defined for the Format operation, the program must supply the CRC/ECC characters for ID and data fields. The CRC characters for the ID field are generated on the flag byte and the three address bytes. The CRC/ECC characters for the data fields are generated on the 256 data bytes. CRC characters are generated by dividing the data string by the generator polynomial $X^{16}+X^{12}+X^{5}+1$ and storing the remainder. ECC characters are generated by the same method using the polynomial $X^{32}+X^{28}+X^{21}+X^{12}+X^{5}+1$. For normal write operations, the disk adapter generates the CRC/ECC characters automatically and writes them at the end of the data or ID field. They are required to be computed only for the Format Sector operation. If execution of this command is abruptly terminated because of a Command Reject error or a disk equipment check condition, the complete sector is not written on the disk. The program must correctly rewrite the data to permit subsequent error-free use of the sector being formatted.

Examples of Disk Data Transfer Operations

This section presents two examples of data transfer operations (Figures 2-10 and 2-11). In the first example, the disk access seeks to the desired cylinder and then reads data fields 0 and 1 of the sector specified in the read data field operation. The second example uses the head selection and cylinder position specified in the first example. Two data fields are written in the sector specified in the write data field operation. These data fields are then checked for temporary write errors using the read-back check operation. The write operation example assumes that no other disk operations were performed and that the disk adapter was not reset after the read operation example.

The CHIO bursts to transfer control and data transfer operations are numbered in both examples; these numbers correspond to those assigned to the FCB operations shown at the top of each example. The CHCV used for each CHIO burst is identified as the data or the control CHCV to identify the type of data being transferred (again, the accessing of control and data transfer operations is only a short data burst to the PCE's channel logic).

An example of a read operation is shown in Figure 2-10; an example of a write operation, in Figure 2-11. These are not intended to be restrictive examples of disk data transfer operations; rather, they show one way that these operations can be performed.

Program/Main Storage	Disk Adapter	Disk Media

The program initializes two channel pointers (CHPs). One CHP contains the address of the area in main storage where the data is to be read; this CHP is the *data* CHP. The other CHP contains the beginning address of the function control block (FCB) that is to be defined in main storage; this CHP is the *control* CHP.

The program also must define the FCB in main storage. For this example, the FCB contains the following control and data transfer operations:

1. (hex 8606) Seek to cylinder 6 and select head 3.
2. (hex 5100CHCV) Load New Data Transfer CHCV
3. (hex 0A07) Load Burst Register (256-byte bursts)
4. (hex 1801) Load Skip Factor/Field Count (skip factor=0, field count=hex 01)
5. (hex 3000) Read Data Field (sector 0, field 0)
6. (hex 0000) End Operation

The program enables the disk adapter for CHIO operations and interrupt request presentation by issuing the Set BSTAT under Mask command with bit 14 active in the mask data.

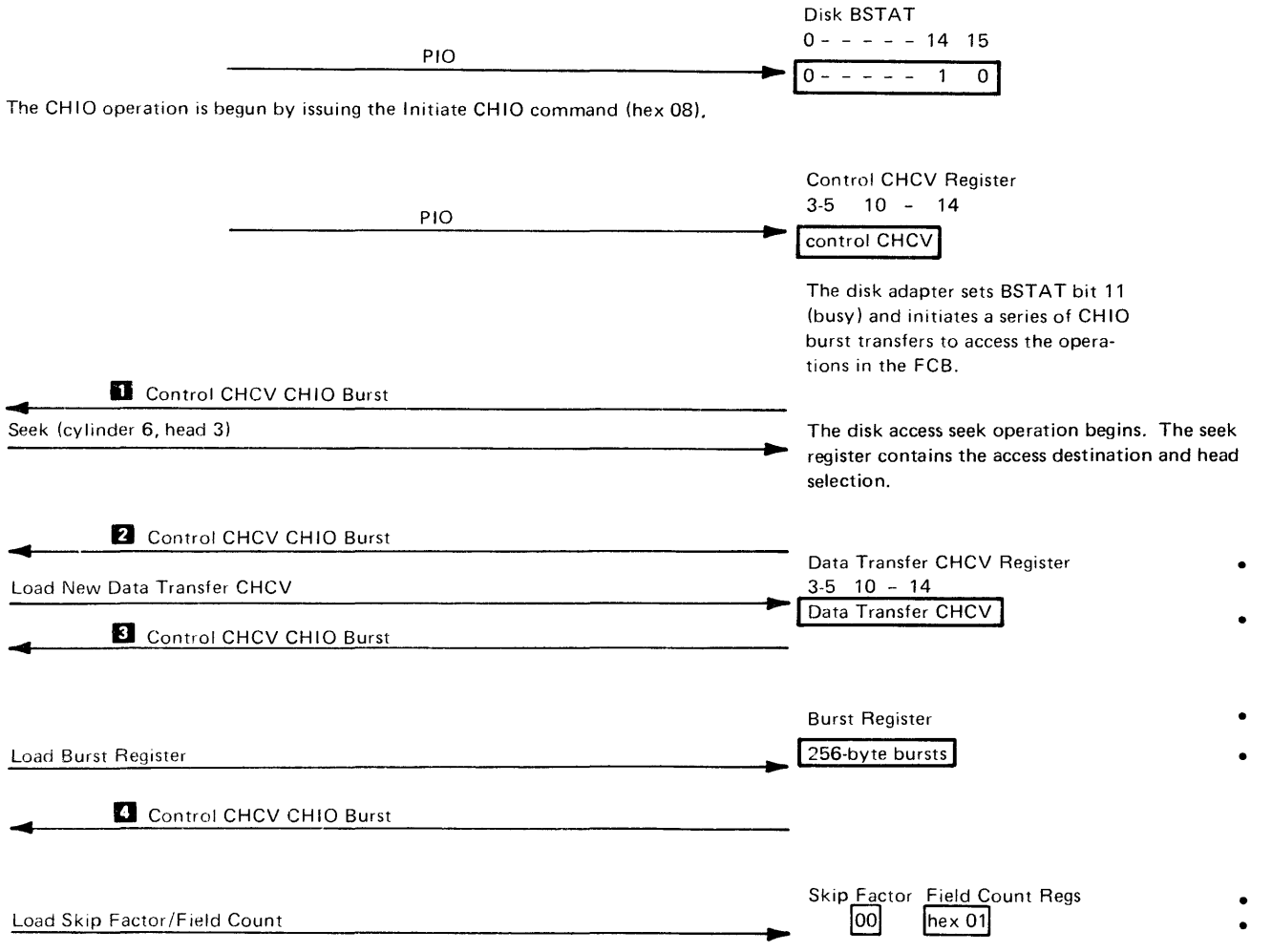


Figure 2-10 (Part 1 of 2). Disk Read Operation Example

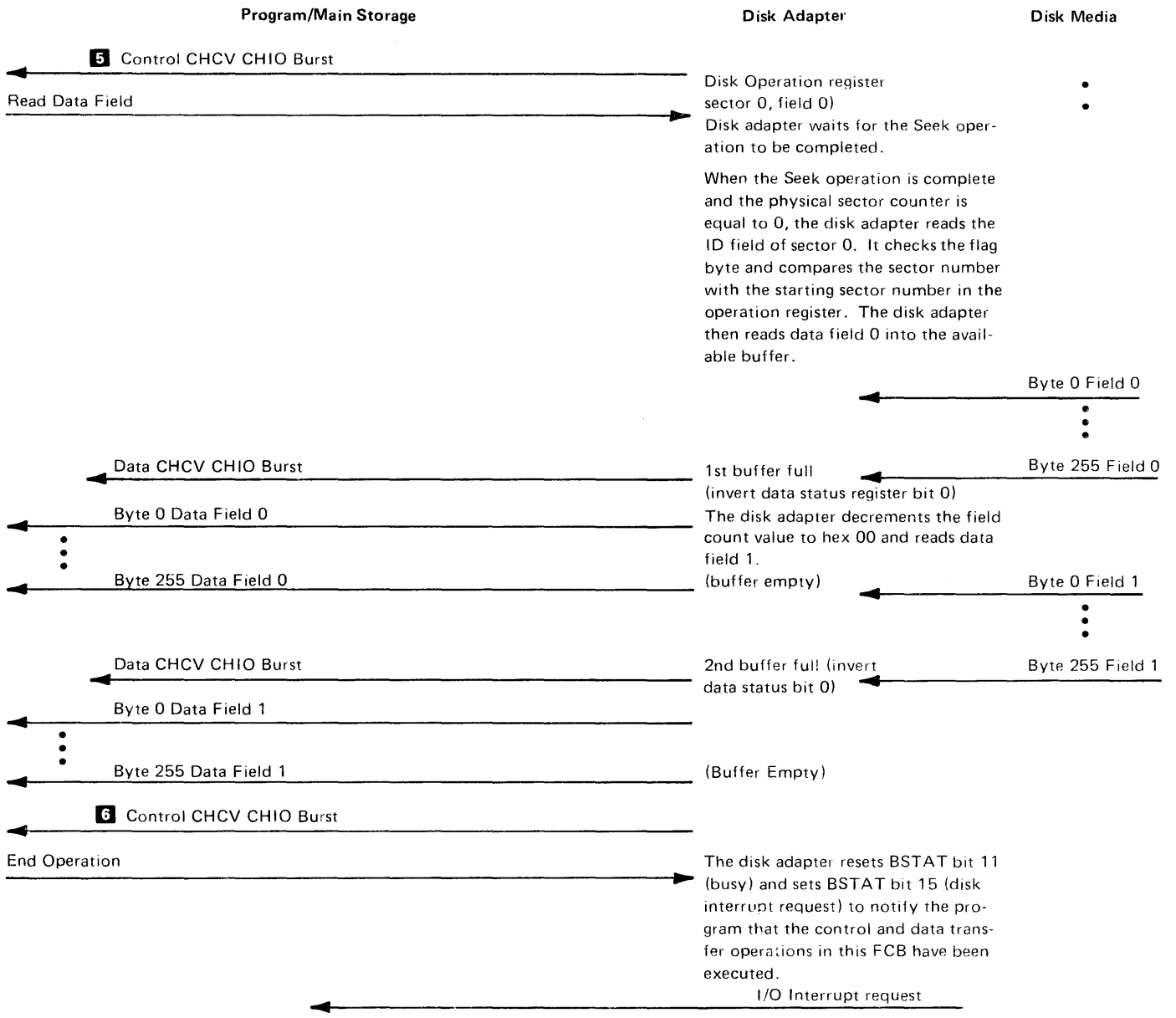


Figure 2-10 (Part 2 of 2). Disk Read Operation Example

Program/Main Storage

The program initializes two CHPs. The data CHP contains the main storage address of the data to be written. The *control* CHP contains the main storage address of the FCB to be used in this example.

The program must define the FCB in main storage. For this example, the FCB contains the following control and data transfer operations.

2 (hex 5100 CHCV) Load New Data Transfer CHCV
1 (hex 1801) Load Skip Factor/Field Count
3 (hex 3800) Write Data Field (sector 0, field 0)
4 (hex 1801) Load Skip Factor/Field Count
5 (hex 6000) Read Back Check (sector 0, field 0)
6 (hex 0000) End Operation

The program starts the CHIO operation by issuing the Initiate CHIO command (hex 08).

Disk Adapter **Disk Media**

The disk adapter is assumed to be enabled (BSTAT bit 14, disk enabled set to 1). The access mechanism position is the same as the read operation example in Figure 2-7 and the burst length has been set to 256-byte bursts.

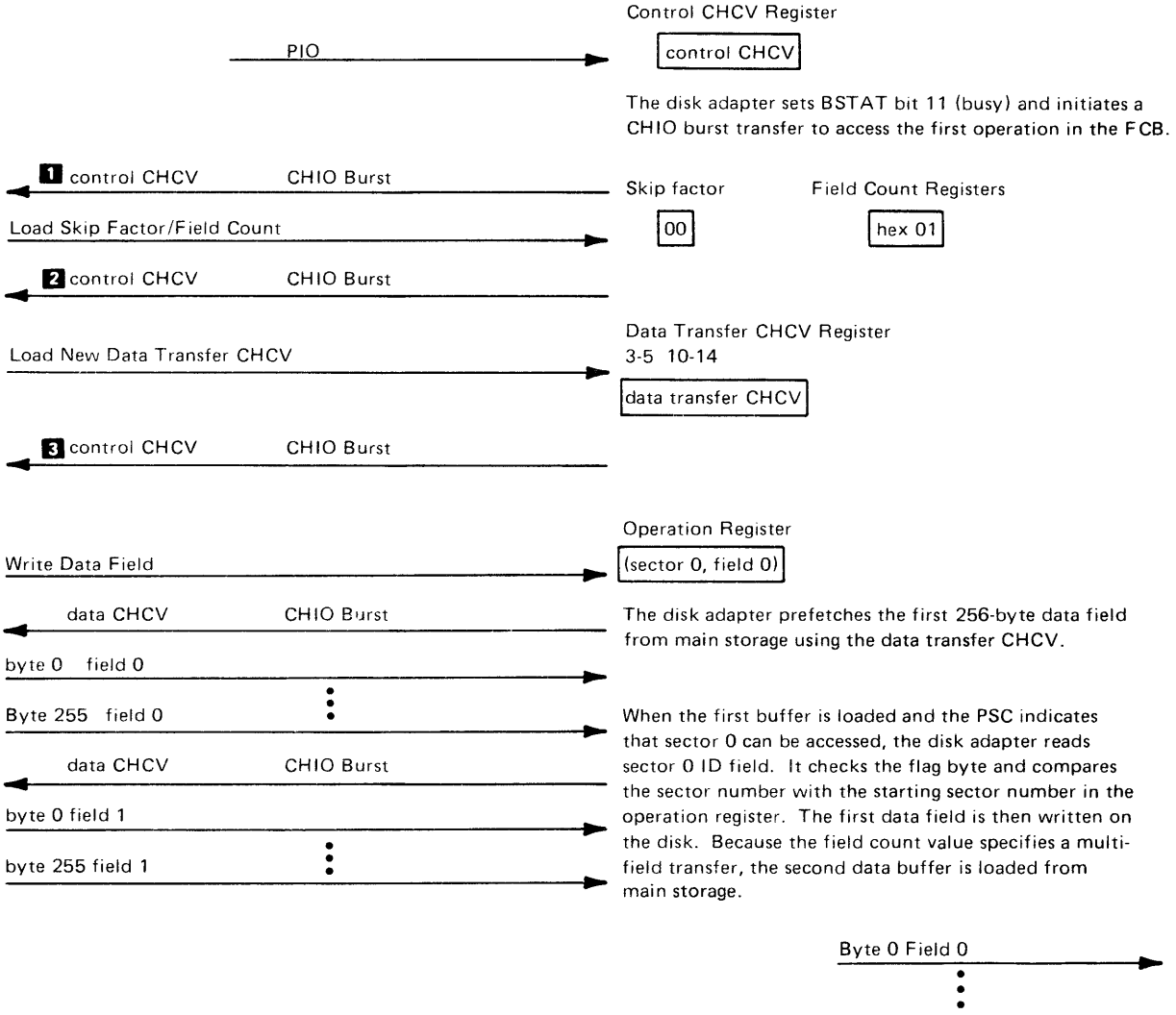


Figure 2-11 (Part 1 of 2). Disk Write Operation Example

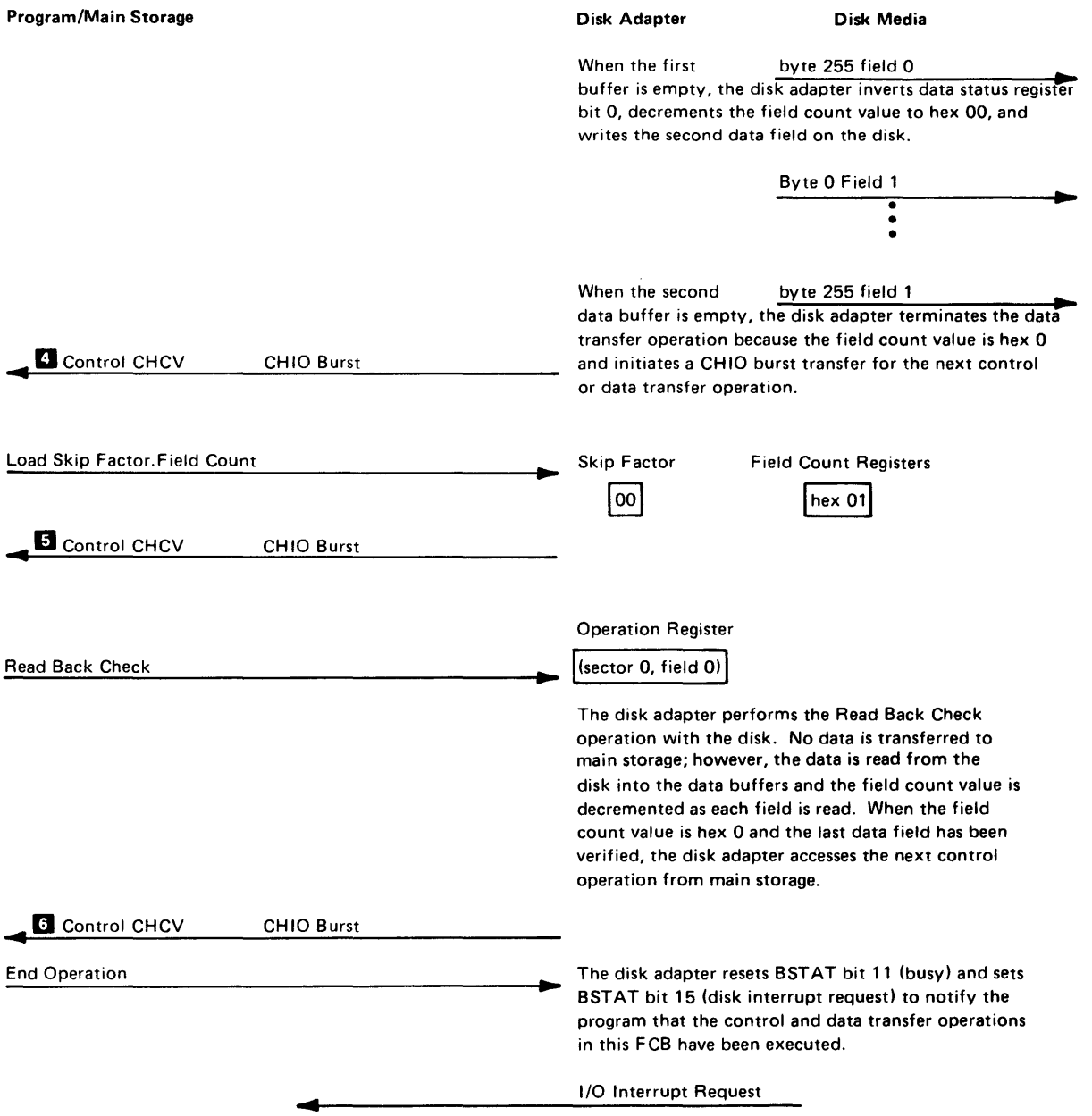


Figure 2-11 (Part 2 of 2). Disk Write Operation Example

Chapter 3. 8100 Diskette Storage Facility

The 8100 diskette storage facility incorporates a diskette 2D drive that provides a maximum of 1,212,416 bytes of removable diskette storage and that operates at a maximum data rate of 62,500 bytes per second. The facility can be used for:

- Logging
- Dumping
- Data exchange
- Initial program load

The diskette storage facility is included in the 8130, 8140, and 8150 processors; a second facility can optionally be featured in the 8101 Storage and I/O Unit Models A10, A11, A13, A20, A23. Each includes a separately programmable diskette adapter.

The diskette adapter provides the logic for programmed control of the diskette drive, data transfer operations, and status reporting for the diskette storage facility. The diskette adapter is described later under "Diskette Storage Functional Elements" and "Diskette Storage Functional Characteristics."

The physical characteristics of the diskette drive and the diskette media are described in the following section.

Diskette Storage Physical Characteristics

This section describes the physical characteristics of the diskette drive and the general format of the diskette media. Refer to Appendix C for the physical specifications of the diskette storage facility, and to the *IBM Diskette General Information Manual*, GA21-9182, for a more complete description of the diskette media.

Read/Write Heads (Loading/Unloading)

The diskette 2D drive provides two read/write heads to read surface 0 on diskette 1 and surfaces 0 and 1 on diskette 2 or 2D media. Loading and unloading the read/write heads are controlled by the diskette adapter. The diskette adapter automatically loads the read/write heads when a data transfer operation is begun with the heads unloaded. When no data transfer operations are performed and two index signals are detected by the diskette adapter, the read/write heads are automatically unloaded. The read/write heads are also automatically unloaded when any error condition is detected.

When required, loading the read/write heads adds an 80-ms delay to the data transfer operation that initiates their loading.

Diskette Format

Diskettes contain 77 tracks on each usable side; diskette 1 uses only one side, and diskette 2 or 2D uses two sides. All diskettes reserve cylinder 0, head 0 for labeling information. This track is always divided into 26 sectors, each containing 128 bytes of data recorded in single-density mode so that they can be read on all diskette drives. For diskette 2 and 2D media, cylinder 0, head 1 is also reserved

for labeling. In single-density mode, this track is formatted in 26 sectors, each containing 128 bytes of data. In double-density mode, each sector contains 256 bytes of data. This data is recorded in single-density mode for diskette 1 and in double-density mode for diskette 2D media.

Track Format

Data cylinders are numbered 0 to 76, with cylinder 0 being the outermost cylinder, and cylinder 76 the innermost. Cylinders 75 and 76 are reserved to provide alternate space. Appendix D lists the track and diskette capacities available on the 8100 diskette storage facility.

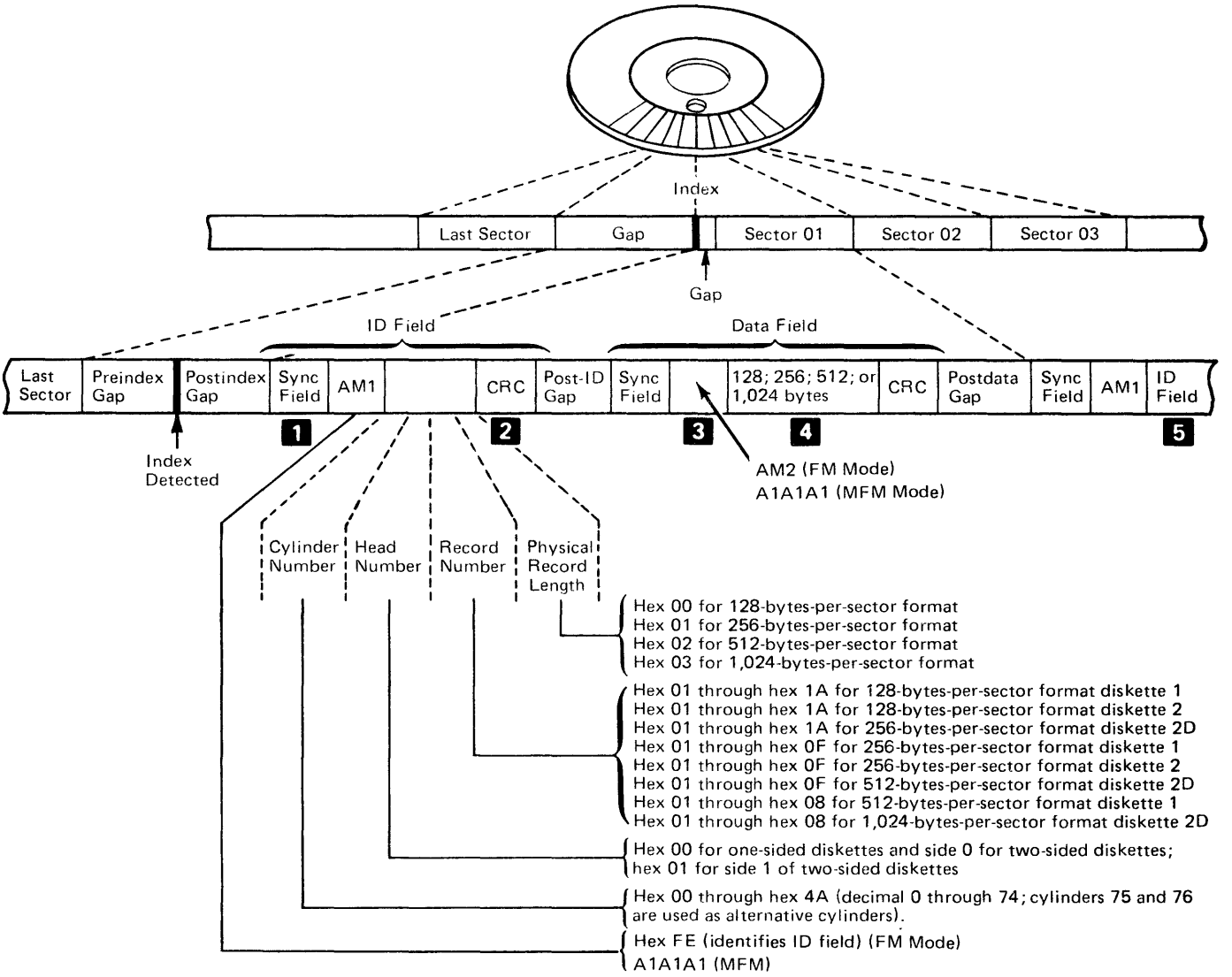
Sector Format

Each sector contains an identification (ID) field and a data field. The length of the data field determines the number of sectors that are contained on one track. Both the ID and the data fields are preceded by a "gap" field, a "synchronizing (sync)" field, and an "address marker" field. The specific length of these fields is determined by the recording mode for the diskette. These fields are shorter for single-density diskettes than for double-density diskettes, as described in the *IBM Diskette General Information Manual.*

With the exception of cylinder 0, all sectors on the diskette are initialized to the same recording mode and data field length. See Figure 3-1 for a description of a single sector.

ID Field: The sector ID field contains four bytes of information that can be accessed by a program using the Read ID or Read ID Next commands (hex 20 and 22, respectively). The sector ID information that is available to the program includes the following: cylinder number, head number, sector number, and physical sector length. The sync field and the address marker are not returned by the diskette adapter.

Data Field: The data field usually contains the data record associated with this sector. This field can also be used as a control field if the program implements the use of sector control fields. The address marker that precedes this field identifies whether it is a data field or a control field. Only the data or control information is available to the program; the sync field and the address marker are not returned to the program.



1 Binary zero sync bytes.

2 Cyclic redundancy check. The check bytes are generated during a write operation and are used during both write and read operations to verify that the data is correct.

3 Various systems have the ability to modify records or the locations of records. These modifications are as follows:

- Logically delete a record.
- Move a record from a defective sector to the next sequential sector.
- Move a record from a defective sector to an alternative sector.

These modifications are made by changing the contents of the address marker AM2 and the first character of the data field that immediately follows AM2. When the first character of the data field changes, the data field changes to a control field that designates what type of modification was made.

Note: ***The address marker AM2 usually contains a hex FB. When any of the three modifications is necessary, AM2 is changed to hex F8. F8 alerts the device to check the first character of the next field.***

4 The value of the first character of this field specifies the type of modification that has affected the record that previously occupied the sector. The characters used and their significance are:

- D, which means delete the record. During subsequent read operations, the device ignores the remaining contents of this sector.
- F, which means move the record to the next sequential sector. During subsequent read operations, the device ignores the remaining contents of this sector and searches for the record in the next sequential sector.
- . (period), which means move the record to a sector that has been allocated as an alternative sector. The address of the alternative sector is written in the error directory (sector 05 on side 0 of the index cylinder). During subsequent read operations, the device reads the period and searches for the sector address in the error directory (error map).

5 The ID field contains the sync field, address marker 1, the address and length of the record, and CRC bits. From this information, the system can identify and locate the record. If the cylinder is defective, all the ID fields on that cylinder are filled with binary ones.

Figure 3-1. Diskette Sector Format

Diskette Storage Functional Elements

The 8100 diskette storage facility consists of the physical diskette 2D drive and the diskette adapter. The diskette 2D drive includes the access mechanism used to locate the read/write heads relative to the surface of the diskette and is described earlier in this chapter under "Diskette Storage Physical Characteristics." The diskette adapter provides for the programmed control of the diskette access mechanism and the transfer of data and control information between the diskette storage and a program. This section contains an introduction to the diskette adapter and describes the elements of the diskette adapter that are accessible through programming or that control programmed operations.

Diskette Adapter

The diskette adapter implements both programmed I/O (PIO) operations and channel I/O (CHIO) operations. It includes status registers that record and control the operational status of the diskette storage facility. Several control registers are used to control data transfer operations between the diskette and main storage. The diskette adapter contains logic that receives control signals from the PCE's channel logic and that returns appropriate responses during PIO and CHIO operations. The diskette adapter includes two 128-byte data buffers. These buffers are used during CHIO data transfer operations between the diskette media and main storage. The diskette adapter also presents I/O interrupt requests to notify the program when an I/O operation has ended, or that an error condition has been detected and recorded in the diskette adapter's status registers.

Diskette Adapter Data Buffers

The diskette adapter contains two 128-byte data buffers that are only used during CHIO data transfer operations. PIO operations with the diskette adapter transfer only one byte of data to or from a register and do not require buffering. These data buffers are managed totally by the diskette adapter; no programmed control is needed for their use.

During read operations, these buffers are loaded before a CHIO burst transfer is requested by the diskette adapter. During Write operations, these buffers are loaded using CHIO burst transfers before the diskette adapter locates the record to be written on the diskette. The use of these buffers is described in detail later in this chapter under "Diskette CHIO Operations."

During data transfer operations, the full/empty status of these buffers is used by the diskette adapter to detect the Overrun/Underrun condition that identifies that the channel logic is not servicing diskette requests for CHIO burst transfers at a rate that is adequate for the rate at which the data is being read or written on the diskette.

Diskette Adapter Control Registers

This section describes the registers used by the diskette adapter to control data transfer operations. These registers are described in terms of the significance of their contents and how they are read or written through programming. The registers described in this section include the channel pointer (CHP) number register, the diskette control register, the drive control register, the record count register, and the record number register.

Channel Pointer (CHP) Number Register

This register is used during the initiation of a channel I/O (CHIO) burst transfer. As the diskette adapter generates the channel control vector (CHCV), the contents of the CHP number register identifies which of the 64 channel pointers is to be used during subsequent CHIO operations.

Bits 0, 1 of this register are reserved; bits 2–7 contain the CHP number in hex.

Programming Note: The contents of the CHP number register are loaded using the Load CHP Number Register command (hex 08). The contents of this register are read using the Read CHP Number Register (hex 01).

For a detailed explanation of CHP number registers, refer to the *8100 Principles of Operation*, GA23-0031.

Diskette Control Register

The contents of this register define the recording mode of the diskette media, the record length used on the diskette media, and the last operation performed by the diskette adapter.

The significance of the fields in the diskette control register is as follows:

Field	Description
Bit 0	Single density. This bit identifies the recording mode used by the diskette adapter. When set to 1, this bit places the diskette adapter in single-density recording mode. When set to 0, this bit places the diskette adapter into double-density recording mode. The Reset Diskette Adapter command (hex 02) and system reset set this bit to 1.
Bits 1,2	Data field length. These bits define the record length used by the diskette adapter. The record lengths are as follows:

Bit 1,2 Value	Record Length
00	128-byte records
01	256-byte records
10	512-byte records
11	1024-byte records

Field	Description
Bits 3–7	Diskette operation. This field contains a value that reflects the last operation being performed by the diskette adapter. The values in this field are set by the diskette adapter; read-only access for this field is provided through programming. The contents of this field are determined by the last operation executed by the diskette adapter and have the following meanings:

Value of Bits 34567	Previous Operation
00000	Idle (reset state)
00001	Read ID next
00010	Write track
00011	Reserved—not used.
00100	Load record number register and write record
00101	Load record number register and read record
00110	Load record number register and read back check
00111	Load record number register and read ID
01000	Select head 1, no seek
01001	Select head 0, no seek
01010	Seek, select head 1, cylinder range 00–41
01011	Seek, select head 0, cylinder range 00–41
01100	Seek, select head 1, cylinder range 42–59
01101	Seek, select head 0, cylinder range 42–59
01110	Seek, select head 1, cylinder range 60–76
01111	Seek, select head 0, cylinder range 60–76
10000 through 11110	Reserved for maintenance use.
11111	Read drive status register

Programming Note: The contents of the diskette control register are read during the execution of the Read Diskette Control Register command (hex 03). Bits 0–2 of this register are loaded during the execution of the Load Diskette Control Register command (hex 0A). Bits 3–7 of this register cannot be loaded through programming; they are set only by the diskette adapter.

Drive Control Register

This register identifies whether a diskette 1 is loaded in the diskette drive and which read/write is selected. Only two bits are used in this register; bits 0–3, 5, and 7 are reserved. The significance of bits 4 and 6 follows:

Bit	Description
4	Diskette 1. This bit is set to 1 by the diskette adapter when a diskette 1 is loaded in the diskette drive. This bit is 0 when a diskette 1 or 2D is loaded. This bit cannot be set or reset through programming.
6	Select Head 0. This bit controls which read/write head is used for diskette data transfer operations. When this bit is 1, head 0 is selected; when this bit is 0, head 1 is selected. **Programming Note:** This bit is loaded during execution of a Seek command or a Write Track command. Bit 4 of the Seek command code is loaded into this bit to set the desired head selection. During the PIO execution phase of the Write Track command, bit 0 of the PIO data operand is loaded into this bit to set the specified head selection for the Write Track operation.

Programming Note: The contents of this register can be read by issuing the Read Drive Control Register command (hex 09). Bits 0–3, 5, and 7 are returned as zeros; the contents of bits 4 and 6 are returned directly to the program.

The contents of this register cannot be loaded using a single load register command. Bit 4 is set by the diskette adapter hardware when a diskette is loaded into the diskette drive; bit 6 is set during the PIO execution of a Seek command or during a Write Track data transfer operation.

Record Count Register

This register is used by the diskette adapter during multirecord transfer operations and during seek operations that move the access mechanism. For multirecord transfers, this register is loaded with a value that is 1 less than the total number of records that are to be transferred. The diskette adapter decrements this value as each record is successfully transferred to or from main storage until the count value is zero. The record transfer is then terminated. If an error condition causes the multirecord transfer to be prematurely terminated, the record count register contains a value of 1 less than the number of records that remain to be transferred.

When a Seek command is received, bits 1–7 of the data operand sent during the PIO execution of the seek command are loaded into the record count register. This value is 1 less than the total number of tracks that are to be crossed during the seek operation. If an error is detected that prevents completion of the seek operation, the record count register contains a value equal to 1 less than the number of tracks that remain to be crossed.

Programming Note: The contents of bits 3–7 of this register can be read by issuing the Read Diskette Status Extension Register (hex 05). Bits 3–7 of this register are returned in bits 2–6 (record count/seek count field) of the byte operand returned to the program. Bit 0 of this register is reserved, and bits 1 and 2 of this register are not returned. The contents of this register can be loaded in two ways: During execution of the Load Record Count Register command (hex 18), bits 3–7 of this register are loaded from bits 3–7 of the byte operand received from the program; bits 0–2 are ignored by the diskette adapter. During execution of a Seek command that moves the access mechanism, bits 1–7 of this register are loaded from bits 1–7 of the byte operand received from the program. Bit 0 of the Seek command byte operand is used by the diskette adapter to determine the direction of the seek operation.

Record Number Register

The record number register is used during data transfer operations to identify the starting record number for that operation. This register is loaded during the PIO execution phase of a data transfer operation. The value loaded into bits 3–7 of the record number register is used by the diskette adapter as it searches the sector ID fields for the selected record number; bits 0–2 of this register are reserved. The Read ID Next and Write Track operations do not load this register, because the diskette adapter does not perform record number searches during their execution.

This register is also used by the diskette adapter during multirecord transfers to locate the next record number to be transferred. The starting record number is incremented by the diskette adapter when the first record is transferred. The diskette adapter then uses the new record number value to search for the next record on the diskette. As each record is transferred, the diskette adapter increments the record number register value by 1 until the record count is exhausted and the operation is completed.

Programming Note: The contents of this register cannot be read through programming. If an error condition terminates a multirecord transfer operation prematurely, the current record number value must be calculated by the program. The residual number of records to be transferred can be accessed by issuing the Read Diskette Status Extension command (hex 05). This value can then be used to calculate the current record number.

Diskette Adapter Status Registers

There are two diskette status registers: the diskette basic status register (BSTAT) and the diskette status extension register. These registers record and control the operational status of the diskette adapter and identify error conditions detected by the diskette adapter. The diskette BSTAT is a byte register; the diskette status extension register contains only two bits.

Diskette BSTAT Summary

Bit	Description
0,1	Error status codes 00 – No error 01 – CRC error 10 – Command reject 11 – Parity check
2,3,4	Operational status codes 000 – Operation complete 001 – Control complete 010 – Drive error 011 – Busy 100 – Overrun/Underrun 101 – Timeout 110 – Record not found 111 – Diskette not ready
5	Diskette equipment check
6	Diskette enabled
7	Diskette interrupt request

Diskette BSTAT Description

Bit **Description**

0,1 Error status codes. These codes identify error conditions detected by the diskette adapter. The significance of their values follows:

Value	Meaning
00	No Error. This code is set when an operation is completed without error.
01	Data CRC Error. This code identifies that the diskette adapter detected a CRC error during execution of a single or multirecord read record or read-back check operation. This error code is not set during record number searches or read ID field operations, to prevent the possibility of erroneously identifying duplicate record numbers. This code is also set if the wrong sector size is selected.

Value	Meaning
10	Command Reject. This code is set under the following two conditions: 1. When the diskette adapter receives an invalid PIO command, the Command Reject code is set and the following bits are set: a. BSTAT bit 5: Equipment Check. b. BSTAT bit 7: Diskette Interrupt Request. (In the 8130B and the 8150, bit 7 is not set if the invalid command has correct parity.) The response for the command is suppressed and a system check interrupt request is forced in the PCE by the I/O timeout condition. 2. When the diskette adapter is "busy" (BSTAT bits 2, 3, 4 are set to the Busy code, binary 011), only three PIO command codes can be executed by the diskette adapter: Reset Diskette Adapter (hex 02), Read Diskette Control Register (hex 03), and Read Diskette BSTAT (hex 07). The command reject code is set if any other PIO command codes are received when the diskette adapter is "busy."
11	Parity Check. This code identifies that the diskette adapter has detected a parity check condition. The contents of the diskette status extension register identify the type of parity check that was detected.

Programming Note: When either bit 0, bit 1, or both bits 0 and 1 are set, bit 7 (diskette interrupt request) is also set. The Reset Diskette Adapter command (hex 02) or the Reset BSTAT under Mask command (hex 04) with mask bits 0, 1 set must be issued to resume normal operation of the diskette adapter. Bits 0 and 1 of the diskette status extension register, if set, are also reset.

Bit	Description
2,3,4	Operational status codes. This field contain codes that are set by the diskette to identify conditions under which the last diskette operation ended. The significance of these codes follows:

Value	Meaning
000	Operation Complete. This code is set by the diskette adapter when the current operation is completed without error. Register-oriented PIO commands do not cause this code to be set by the diskette adapter; the completion of a data transfer command or of a seek command causes this code to be set. Loading a diskette into the drive causes this code to be set and an interrupt request to be presented to the PCE asynchronous to program execution. **Programming Note:** Some adapters may present a false ready interrupt. Any interrupt indicating a transition from not ready to ready should be confirmed 170 ms after the original interrupt before issuing a seek read or write operation. Failure to confirm this transition may cause unpredictable results.
001	Control Complete. This code is set by the diskette adapter only after completion of a read record operation during which a control record was read. If a multirecord operation was in progress, it has been terminated by reading the control record. In either case, the control record had been transferred to main storage. If a multirecord read operation was ended when the control record was read, the record count register contains a value that is 1 less than the number of records that remained to be transferred when the operation was ended. **Programming Note:** If a CRC error occurred while reading a control record, the Control Complete code may not be set. A Read Access Lines (hex 4) must be done to clear this condition and to permit subsequent data records to be read correctly.
010	Drive Error. This code is set by the diskette adapter when an incorrect write signal response is detected. The diskette adapter monitors the state of the diskette drive's write logic at all times; if the state of the write logic is incorrect, regardless of whether a write operation is in progress, the diskette adapter sets this code. If a write operation is attempted, no data will be written on the diskette.

Bit	Description	
	Value	**Meaning**
	011	Busy. This code is set by the diskette adapter during execution of all Seek commands and data transfer commands. This code defines the "busy state"of the diskette adapter. When the diskette adapter is busy, only three PIO commands can be executed by the diskette adapter: Reset Diskette Adapter (hex 02), Read Diskette Control Register (hex 03), and Read Diskette BSTAT (hex 07). If any other commands are received while the diskette adapter is busy, the diskette adapter sets the Command Reject code in BSTAT bits 0, 1 and terminates the operation in progress.
	100	Overrun/Underrun. This code is set during a read or write record in 256-byte-multisector, 512-byte, or 1024-byte record mode if the PIO operation to a buffer has not been completed by the time that buffer is needed. It will not be set in 128-byte single-sector record mode. It can be set on a write track operation regardless of the record size. It can also be set on a "Read Record" if the adapter does not detect the "Data AM." This state will terminate the operation and cause bit 7 to be set.
	101	Timeout. This code is set by the diskette adapter when execution of a data transfer command was begun and not completed in 26 revolutions of the diskette.
	110	Record Not Found. This code is set by the diskette adapter when a data transfer operation that requires a record number search is initiated and the selected record number cannot be located on the diskette. This condition can occur for single record and multirecord transfers. If a multirecord transfer is terminated by this condition, the record count register contains a value that is 1 less than the number of records that remain to be transferred. This value can be used to calculate the record number that cannot be located. **Note:** This code can be set if the diskette adapter detects a CRC error on the ID field of a sector. This code is set, rather than CRC Error, to prevent erroneous duplicate record number comparisons. This code is also set when an operation is attempted that requires reading an ID field if the incorrect mode (single or double density) is selected.

Bit	Description	
	Value	**Meaning**
	111	Diskette Not Ready. This code is set by the diskette adapter when no diskette is loaded in the drive. It can also be set if the diskette adapter detects a speed error with a diskette loaded. If a Seek command or any data transfer operation is initiated when this code is active, BSTAT bit 7 (diskette interrupt request) is set to notify the program that these operations cannot be performed at that time. **Programming Note:** This code can also be set when the access door is opened. If this door is opened to remove the diskette while diskette operations are in progress, the diskette adapter can be placed in an unexpected "hang" condition. The current operation will be terminated, and the diskette adapter MAY NOT present an interrupt request to the PCE to notify the program that this condition exists. This "hang" condition can be removed by issuing the Reset Diskette Adapter command (hex 02). This code may not actually reflect a not-ready condition. To determine whether a not-ready condition exists, do a Reset Adapter (hex 02) and then a Read Diskette Basic Status (hex 07). If the condition still exists, it is a true not-ready condition. Operator personnel should be instructed to remove the diskette media ONLY after receiving a message requesting that the diskette media be removed.

Programming Note: The contents of BSTAT bits 2, 3, 4 cannot be changed using the Set or Reset BSTAT under Mask command (hex 06 and 04, respectively). However, the error conditions represented by these bits will be reset by using Reset BSTAT under Mask (hex 04) with a mask of C1. Only the Reset Diskette Adapter command (hex 02) can reset these bits. If no diskette is loaded in the drive, the Diskette Not Ready code is immediately set by the diskette adapter.

5 Diskette Equipment Check. This bit is set to indicate that an operation with the diskette adapter was abnormally terminated for one of the following reasons:

- Invalid command received
- Command parity check detected
- Write data parity check detected
- CHCV or read data returned to the PCE's channel logic with incorrect parity.

Bit	Description
	Conditions that set this bit also result in a system check interrupt request being presented through the PCE's error interrupt request vector. **Programming Note:** This bit can be set through programming using the Set Diskette BSTAT under Mask command (hex 06). It can be reset using the Reset Diskette Adapter command (hex 02) or the Reset Diskette BSTAT under Mask command (hex 04).
6	Diskette Enabled. When active, this bit permits the diskette adapter to initiate CHIO burst transfer requests and to present I/O interrupt requests to the PCE. When reset, this bit prevents the diskette adapter from participating in CHIO data transfer operations or presenting I/O interrupt requests to the PCE. This bit is only set with the Set Diskette BSTAT under Mask command (hex 06) and reset with either the Reset Diskette Adapter command (hex 02) or the Reset Diskette BSTAT under Mask command (hex 04).
7	Diskette Interrupt Request. This bit is set when the diskette adapter is attempting to present an I/O interrupt request to the PCE. (The presentation of the interrupt request is controlled by the state of BSTAT bit 6, diskette enabled.) The diskette adapter sets this bit when one of the following conditions occurs: 1. Any condition that causes the Error Status field (BSTAT bits 0, 1) to be set to a nonzero value. 2. Any condition that causes the Operational Status field (BSTAT bits 2, 3, 4) to go from Busy (binary 011) to any other value. 3. A change in the Operational Status field value from Diskette Not Ready (binary 111) to any other value. 4. Attempting to execute a Seek command or a data transfer command when the Operational Status field is set to the Diskette Not Ready code. 5. Receiving the Halt signal when the diskette adapter is performing a PIO or a CHIO operation. (In this case, BSTAT bit 5, diskette equipment check, is also set to 1.) **Programming Note:**This bit can be set using the Set Diskette BSTAT under Mask command (hex 06). It is reset by system reset and during execution of the Reset Diskette Adapter command (hex 02) or the Reset BSTAT under Mask command (hex 04).

Diskette Status Extension Register Description

Bit	Description
0	External parity check. This bit is set by the diskette adapter when a parity check is detected on the PIO command byte, or when a parity check is detected on data received during any write operation. When this bit is set, the BSTAT Error Status field is set to binary 11 and BSTAT bit 7 is set.
1	Internal parity check. This bit is set by the diskette adapter when a parity check is detected on data being operated upon within the diskette adapter. When this bit is set, the diskette adapter also sets the BSTAT Error Status field to binary 11 and sets BSTAT bit 7 (diskette interrupt request).

Programming Note: These bits are reset by the Reset Diskette Adapter command (hex 02). No command is provided to reset these bits directly; however, when the Reset Diskette BSTAT under Mask command is issued with mask bits 0 and 1 active, the diskette status extension register bits, if 1, are reset to 0's. When these bits are set, the BSTAT Error Status field contains the binary value 11; when the diskette BSTAT contains this code, normal diskette operations cannot be resumed until these status bits are reset.

2–6	Record Count/Seek Count. These bits represent the number of sectors not transferred due to an error condition.
7	Always 0.

Diskette Functional Characteristics

This section describes the PIO address assignments defined for the diskette adapter, the assignment through programming of the priority level for which the diskette adapter presents I/O interrupt requests, the PIO commands implemented by the diskette adapter, and the CHIO operations implemented by the diskette adapter. The last section in this chapter contains a set of examples of data transfer operations performed by the diskette adapter. These examples include the PIO operations that prepare the diskette adapter for the CHIO operations that follow.

Programming Note: When a system reset or an I/O reset function has been executed, the program must wait a minimum of 350 ms before initiating any programmed operations with the diskette adapter. Failure to follow this procedure can result in unpredictable diskette adapter errors and hang conditions.

Diskette Adapter PIO Address Assignments

The diskette adapter's address assignment is determined by the system component in which it is contained. One diskette adapter is contained in the 8130, 8140 and 8150 processors. One more diskette adapter can be optionally featured in an 8101 Storage and I/O Unit; a maximum of two diskette drives can be included in the 8100 system configuration.

The diskette adapter contained in the 8130 or 8140 Processor is assigned the PIO address hex 87 and is attached to the SSCF usage 1 in the 8140. The optional second diskette adapter, when featured, is attached to the SSCF usage 3 in the 8101 and is assigned one of the following PIO addresses, depending on the 8101 in which it is contained:

8101*1	**8101*2**	**8101*3**	**8101*4**
hex 97	hex A7	hex B7	hex C7

8101*1 through 8101*4 are defined with a specify code at the time the 8100 system is ordered and identified by their unit ID labels. Refer to the *8101/8102 Storage and Input/Output Unit Description* manual for a complete description of the unit ID label.

Diskette Adapter I/O Interrupts

The diskette adapter presents I/O interrupt requests to the PCE when BSTAT bits 6 (diskette enabled) and 7 (diskette interrupt request) are set. This interrupt request signal is intercepted by the SSCF to which the diskette adapter is attached and is translated into an I/O interrupt request to the PCE for the priority level to which the diskette adapter is currently assigned.

Programmable Priority Level Assignment

The diskette adapter is assigned to present I/O interrupt requests for a specific priority level through programming. The SSCF to which the diskette adapter is attached contains an *interrupt translation array* (ITA) that provides a means to define the priority level assignment of each attached adapter. The diskette adapter is assigned to location 7 of the ITA because its PI address is hex X7. The ITA also provides a means to assign a unique identification to the interrupt request presented by the diskette adapter, termed the *sublevel assignment*. Both the priority level assignment and the sublevel assignment are defined in the ITA location to which the diskette is assigned, as illustrated in Figure 3-2.

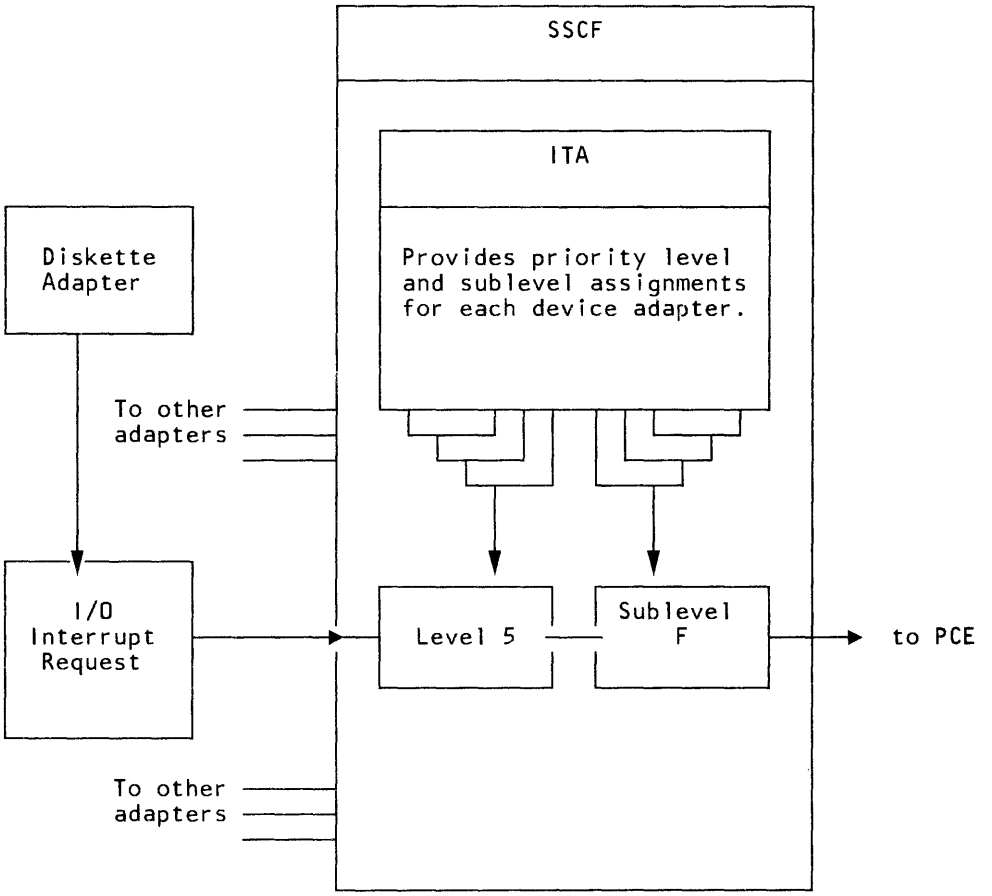


Figure 3-2. Priority and Sublevel Assignment in the ITA

Programmed operations should not be directed to the diskette adapter until the priority level and sublevel assignments have been defined in the ITA location with which the adapter is associated.

For a discussion of assigning priority levels and sublevels and for a detailed description of the ITA, refer to "Secondary System Control Facility (SSCF)" in the 8130 or 8140 Processor Description manual.

Diskette PIO Operations

Programs initiate PIO operations by executing byte-type I/O instructions to direct a command and a byte of data to the diskette storage facility. The channel and the diskette adapter exchange control signals to ensure that the data and the control information are presented in the correct sequence. The PIO command determines whether data is transferred to or from the diskette storage facility. The specific PIO commands implemented by the diskette adapter are described under "Diskette PIO Command Description."

Programming Note: The diskette adapter does not implement halfword data transfer operations; data is transferred one byte at a time. The Input/Output-Halfword (IOH) instruction should NOT be used during PIO operations with the diskette adapter.

Specific byte-type I/O instructions and general programmed I/O operations are described in detail in the *8100 Principles of Operation* manual.

The PIO command description is divided into three sections. The first group of commands described is used to reset the diskette adapter or to inspect or modify the contents of a specific register; these commands are described under "Register-Oriented Commands." The second group of commands is used to initiate the CHIO transfer of data between the diskette and main storage; these commands are described under "Data Transfer Commands." The commands in the last group are the eight versions of the Seek command implemented by the diskette adapter; they are described under "Seek Commands." Commands that are reserved for maintenance use are identified under "Diskette PIO Command Summary." The error resulting from sending an invalid command code to the diskette adapter is described at the end of this chapter under "Diskette Adapter Error Detection and Reporting." All PIO commands implemented by the diskette adapter are identified under "Diskette PIO Command Summary."

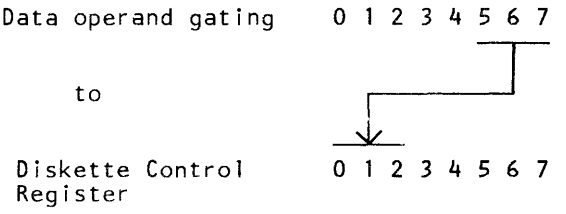
Programming Note: All data transfer commands and all Seek commands that move the read/write heads are performed when the diskette adapter is "busy" (BSTAT bits 2,3,4 are set to the Busy code — binary 011). Only three commands can be executed by the diskette adapter when the Busy code is set in BSTAT bits 2, 3, 4: Reset Diskette Adapter (hex 02), which aborts operation; Read Diskette Control Register (hex 03); and Read Diskette Basic Status Register (hex 07). If any other PIO commands are received when the diskette adapter is busy, the diskette adapter terminates the current operation, sets the Command Reject code in BSTAT bits 0, 1, and sets BSTAT bit 7 (diskette interrupt request) to notify the program that this error has been detected. Although Read Diskette BSTAT can be issued while the adapter is busy, doing so causes unpredictable results.

Register-Oriented Commands

Command (in Hex)	Description
01	Read CHP Number Register. This command causes the diskette adapter to return the current channel pointer number on the diskette CHCV register to the program. The format of the byte operand returned is: 0 1 2 3 4 5 6 7 0 0 CHP number in hex
02	Reset Diskette Adapter. This command causes the registers in the diskette adapter to be reset to the values described under "Diskette Reset State" in Appendix B. All CHIO data transfer operations are terminated; if a diskette write operation is in progress, it is terminated without writing the CRC bytes for the field being written. If an interrupt request is pending when this command is received, the interrupt request is reset.

Command (in Hex)	Description
	This command may move the R/W head, thus causing the position of the R/W head to be unknown. Do a Read ID to determine the position of the R/W head.
03	Read Diskette Control Register. This command causes the diskette adapter to return the contents of the diskette control register to the program. Bits 0–7 of this register are returned directly as a byte operand.
04	Reset Basic Status Register under Mask. This command resets BSTAT bits that are selected by the byte mask operand. The mask bits correspond directly to the BSTAT bits. A mask bit with the value 1 resets the associated BSTAT bit; a mask bit with the value 0 does not affect the associated BSTAT bit. **Programming Note**: This command does not affect the values of BSTAT bits 2, 3, and 4. The corresponding mask bits may be included, but these bits are not reset. However, the error condition represented by these bits will be reset by using this command with a mask of hex 01 or 10. When mask bits 0, 1 are active, the diskette status extension bits 0 and 1, if set, are set to 0. A RESET ADAPTER command (hex 02) may be necessary to reset BSTAT bits 2–4.
05	Read Diskette Status Extension Register. This command causes the diskette adapter to return the contents of the diskette status extension register in bits 0, 1 of the byte operand; bits 2–6 are termed the record count/seek count field and are returned from bits 3–7 of the record count register. Bit 7 is returned as zero.
06	Set Basic Status Register under Mask. This command sets bits in the BSTAT that are selected with a byte mask operand. The mask bits correspond directly with the BSTAT bits. A mask bit with the value 1 sets the associated BSTAT bit; a mask bit 0 does not affect the associated BSTAT bit. **Programming Note**: This command does not affect the values of BSTAT bits 2, 3, and 4. The corresponding mask bits may be included, but these bits cannot be set through programming.
07	Read Diskette Status Register. This command causes the diskette adapter to return the contents of the BSTAT to the program. Bits 0–7 of this register are returned directly as a byte operand.

Command (in Hex)	Description
08	Load CHP Number Register. This command causes the diskette adapter to load bits 2–7 of the data operand received from the program into bits 2–7 of the CHP number register. Bits 0 and 1 are reserved and must be set to zeros in the data operand. **Programming Note:** If bits 0 and 1 of the data operand are set to a value other than 00, the next CHIO burst transfer will cause a system check interruption. The current operation is abruptly terminated; BSTAT bits 5 (equipment check) and 7 (diskette interrupt request) are set to notify the program of this error.
09	Read Drive Control Register. This command causes the diskette adapter to return the contents of the drive control register to the program. Bits 4 and 6 of this register are returned as bits 4 and 6 of the byte operand; bits 0-3, 5, and 7 are returned as zeros.
0A	Load Diskette Control Register. This command causes the diskette adapter to load bit 5 of the received data operand into bit 0 of the diskette control register, and to load bits 6, 7 of the received data operand into bits 1, 2 of the diskette control register. Bits 0–4 of the data operand are unused and should contain zero.



Programming Note: Bit 5 of the data operand sets the diskette adapter's recording mode to single or double density and must be set to reflect the recording mode of the diskette. Failure to set bit 5 correctly results in false Record Not Found errors.

Bits 6 and 7 of the data operand set the record length used by the diskette adapter and must be set to reflect the record length of the diskette as defined in the Physical Record Length byte of the sector ID field. Failure to set the correct record length value results in false CRC errors during read record operations. If write record operations are attempted when the record length is set incorrectly, the next sector ID field may be overwritten, destroying the data organization of the diskette.

Command (in Hex)	Description
18	Load Record Count Register. This command causes the diskette adapter to load bits 3–7 of the data operand received from the program into bits 3–7 of the sector count register. Bits 0–2 are reserved and should be set to zeros. The value loaded into the record count register specified 1 less than the number of records that are to be read or written during the next CHIO data transfer operation. When the value in the record count register is greater than zero, the next data transfer command results in a multirecord transfer operation of up to the number of records on one track.

Data Transfer Commands

These PIO commands initiate channel I/O (CHIO) operations with the diskette adapter. The command code issued by the program identifies the data to be transferred in CHIO bursts after the PIO operation is completed. The byte PIO data operand is loaded into the record number register to identify the record number of the first ID field or data record that is to be transferred. Multiple records or ID fields can be transferred during the CHIO operation when the record count register contains a value greater than zero to identify the number of records or ID fields that are to be transferred. The read/write heads are loaded automatically if necessary, adding an 80-ms delay to the current operation. The description of the individual commands is preceded by an overview description of functions performed during execution of the data transfer commands. This overview is divided into the following topics: "PIO Execution," "Locating the Selected Record," "Multirecord Transfers," and "Multirecord Termination Conditions."

PIO Execution

The PIO execution consists of transferring the command code from the program to the diskette adapter during execution of an IO or an IOI instruction. Bits 3–7 of the data operand are loaded into the record number register to identify the location of the first ID field or data record that is to be transferred to or from main storage. The command code identifies whether an ID field or a data record is to be transferred. When the diskette adapter accepts the byte of data that is loaded into the record number register, PIO operation is completed.

Locating the Selected Record

For read operations, the diskette adapter locates and reads the selected ID field or record before initiating a CHIO burst transfer to main storage. For write operations, the diskette loads the first available 128-byte data buffer from main storage before locating the selected record on the diskette. For record lengths of 256 bytes or more, the diskette adapter loads the second 128-byte buffer while the selected record number is being located on the diskette.

To locate the selected record number, the diskette adapter reads the ID field for each sector on the diskette, comparing the record number read from the diskette with the contents of the record number register. With a record number match, the diskette continues to perform the specified data transfer to or from the diskette until the record count is zero.

Programming Note: The program must verify that the read/write heads are positioned over the correct cylinder and that the correct head is selected before a write record operation is begun. The diskette adapter does not perform any verification of the location of the read/write heads before writing the specified record on the diskette.

The diskette adapter reads each ID field on the diskette, searching for a record number comparison until the second Index signal is detected. The second Index signal notifies the diskette adapter that the entire track has been searched. If no record number comparison has occurred, the diskette adapter terminates the operation with an interrupt request to the PCE; the record not found (code 110 in BSTAT bits 2, 3, 4) is indicated in the diskette BSTAT (see "Diskette Adapter Status Registers"). When a write operation is terminated with the Record Not Found error code, the data that was prefetched into one or both of the data buffers is lost. That data must again be accessed by the diskette adapter during a subsequent write operation; the terminated operation cannot be restarted.

Record number searches are not performed for the Read ID Next and Write Track commands.

Transferring the Data

The diskette adapter transfers the specified data using CHIO bursts as the data is read from, or written to, the diskette.

For Load Record Number Register and Read ID and Read ID Next commands (hex 20 and 22), the diskette data transfer is completed when the selected record number or numbers have been located on the diskette. The diskette adapter then initiates a CHIO burst transfer to send the 4-byte ID field to main storage. The data transfer operation is completed when the ID field has been sent to main storage. The diskette adapter notifies the program of its completion by presenting an interrupt request to the PCE; the operation complete (BSTAT bits 2, 3, 4 — binary 000) indication is set in the diskette BSTAT.

For the Load Record Number Register and Read Record command (hex 30), the diskette adapter reads the first 128 bytes of diskette data into the available buffer and initiates a CHIO burst transfer to send that data to main storage. Two CHIO burst transfers are required to transfer the data in the first buffer; the diskette adapter implements a fixed burst length for CHIO bursts of 64 bytes per burst. While the data in the first buffer is being transferred to main storage, the diskette adapter continues to read diskette data into the second 128-byte data buffer if the record length is greater than 128 bytes. This overlapped transfer continues until the selected record has been transferred to main storage.

For the Load Record Number Register and Write Record command (hex 38) the diskette adapter has already loaded the first 128 bytes of data from main storage into the available data buffer before the selected record number was located on the diskette. Usually the second 128-byte data buffer has also been filled when the record length is greater than 128 bytes. The diskette adapter writes the data from the first data buffer onto the diskette. When the data from the first buffer has been written, and the record length is greater than 256 bytes, the diskette adapter initiates another CHIO transfer to load the empty buffer while the data from the full buffer is being written onto the diskette. If the record length is 128 bytes or 256 bytes, the operation is completed when the diskette adapter

completes writing the data in the buffers onto the diskette. At that time, the diskette adapter presents an interrupt request to the PCE to inform the program that the "operation complete" indication is set in the diskette BSTAT.

The Write Track command (hex 78) is described separately under "Write Track" later in this section because its execution sequence is different from that of the normal data transfer commands.

If a parity error is detected during data transfer over the channel, in the adapter's internal buffer, or in any of the adapter's internal paths, the operation is terminated, bit 5 is set in the BSTAT, and a system check is initiated.

Programming Note: All data transfer commands cause the diskette adapter to become "busy" during their execution (BSTAT bits 2, 3, 4 set to the Busy code — binary 011). No further commands may be directed to the diskette adapter until it is no longer "busy" if the current operation is to be completed normally. With the exception of the Reset Diskette Adapter (hex 02), the Read Diskette Control Register (hex 03), and the Read Diskette BSTAT (hex 07) commands, PIO commands received while the diskette adapter is busy cause the current operation to be prematurely terminated with the Command Reject code set in the Error Status field of the diskette BSTAT. Issuing the Read Diskette BSTAT command (hex 07) while the adapter is "busy" can cause unpredictable results.

Multirecord Transfers: All data transfer commands are capable of performing multiple record transfers of up to a full track, with the exception of the Write Track command, which is a full-track operation. Before a multirecord transfer can occur, the program must first load a value equal to 1 less than the number of records to be transferred into the record count register. The PIO command Load Record Count Register (hex 18) is used to do this.

When the diskette adapter receives one of the data transfer commands after a record count value greater than zero has been loaded, the diskette adapter transfers the first data record or ID field as if a single record transfer were specified. Then, instead of presenting an interrupt request to the PCE, the diskette adapter increments the record number by 1, decrements the record count value by 1, and initiates a search for the new record number on the diskette. When the ID field on the diskette contains a record number that compares with the new record number value, the selected field or record for that sector can be transferred to or from main storage. If the record numbers are sequential, up to a full track of contiguous records can be read or written in a single diskette revolution. If a skip factor was used to number the records on the diskette, the diskette adapter may have to search one or more ID fields before a record number comparison is located. In this case, if the record count value indicates that all records on that track are to be read, more than one revolution of the diskette may be required before all the desired data is read or written.

The diskette adapter continues its multirecord transfers as described in the preceding text, until the record count register contains zero, until an error condition is detected, or until a control record is read. At that time, the diskette adapter presents an interrupt request to the PCE to notify the program that the operation has been completed or terminated.

Programming Note: If a multirecord write is performed in 128 single-density mode, the adapter transfers an extra 128 bytes of data before terminating the operation. This can cause a storage check if storage protection is violated.

Multirecord Termination Conditions: This section presents an overview of the specific conditions that cause multirecord data transfers to be terminated. This section summarizes the conditions detected and describes their effect on the operation in progress. All diskette error conditions are listed in Appendix C.

Termination Condition	Description
Record Not Found	Both multirecord read and write operations are terminated when the diskette adapter cannot locate the next record number to be accessed. The diskette adapter presents an interrupt request to notify the program that the operation was terminated with the Record Not Found code in diskette BSTAT bits 2, 3, 4 — binary 110. **Note:** The Record Not Found code can result from detecting a CRC error in the ID field of the sector that contains the desired record number. The CRC error indication is not identified when it is detected during a record number search, because errors in the record number byte could cause erroneous duplicate record number comparisons. **Programming Note**: The low-order 5 bits (bits 3 through 7) of the record count register value are returned to the program during execution of the Read Diskette Status Extension Register Command (hex 05) as bits 2 through 6 of the byte operand. These bits give the number of records that remained to be transferred when the error occurred. Because the record number register cannot be read, the number of the last record accessed must be calculated.
CRC Error	When a CRC error is detected on a data field being read by the diskette adapter, the multirecord operation is terminated immediately; the data is transferred to main storage from the record in error, and the diskette adapter presents an interrupt request to the PCE to notify the program that the operation was terminated with the CRC Error code in BSTAT bits 0, 1 — binary 01. **Programming Note:** Refer to the Programming Note above under "Record Not Found."

Termination Condition	Description
Reading a Control Record in a String of Data Records	A multirecord read operation is terminated when the diskette adapter reads a control record. The control information is returned to the program, and the CHIO data transfer is ended; an interrupt request is presented to the PCE to notify the program that the operation was terminated with the Control Complete code in BSTAT bits 2, 3, 4 — binary 001. **Programming Note:** Refer to the Programming Note above under "Record Not Found."
Parity Check	When a parity check occurs, the operation being performed is terminated and a system check occurs. The contents of the diskette status extension register identify the type of parity check that was detected. The amount of data that is transferred is unpredictable.
Drive Error	When a drive error is detected, the operation is terminated and an I/O interrupt request is presented to the PCE. The diskette adapter sets a drive error when an incorrect write response is detected. The diskette adapter monitors the state of the diskette drive's write logic at all times; if the state of the write logic is incorrect, regardless of whether a write operation is in progress, the diskette adapter sets a drive error. If a write operation is attempted, data will not be written in the diskette. If a read operation is attempted, it may destroy existing data on the diskette.

Data Transfer Command Description

Command (in Hex)	Description
20	Load Record Number Register and Read ID. This command causes the diskette adapter to load the record number register with the starting record number using PIO execution, to search for the selected sector, and, when a comparison has been made with the record number on the diskette, to transfer the 4-byte ID field to main storage using a CHIO burst transfer. At the completion of this operation, the diskette adapter presents an interrupt request to the PCE to notify the program that completion status is available in the diskette BSTAT.

Command (in Hex)	Description
22	Read ID Next. Execution of this command is the same as that of the Load Record Number Register and Read ID command, except that the diskette adapter does not perform a record number search. The first ID field that can be read without error is transferred to main storage using a CHIO burst transfer. At the completion of this operation, the diskette adapter presents an interrupt request to the PCE to notify the program that completion status is available in the diskette BSTAT.
30	Load Record Number Register and Read Record. This command causes the diskette adapter to load the record number register with the starting record number using PIO execution, to search for the selected sector, and when a comparison has been made with the record number from the diskette, to transfer the data record to main storage using CHIO burst transfers. The length of the data record determines the number of 64-byte CHIO bursts required. At the completion of this operation, the diskette adapter presents an interrupt request to the PCE to notify the program that completion status is available in the diskette BSTAT. When a control record is read, rather than a data record, the control information is transferred to main storage before the operation is ended. In this case, however, the diskette adapter sets the Control Complete code in BSTAT bits, 2, 3, 4 — binary 001 to notify the program that the last record read was a control record. If a control record is read during a multirecord transfer, the operation is ended after the control field has been transferred to main storage. The status extension register contains the low-order bits of the record count register so the program can calculate the number of records that remain to be transferred. If a CRC error is detected when the data field is read, the diskette adapter terminates the operation; the data is transferred to main storage, and the CRC Error code is set in BSTAT bits 0, 1. The diskette adapter presents an interrupt request to the PCE to notify the program that the completion status is available in the diskette BSTAT. When a CRC error terminates a multirecord transfer operation, the status extension register contains the low-order 5 bits of the record count register value so that the program can calculate the number of records that remain to be transferred. However, the amount of data transferred into storage from the last record is unpredictable. If the record with the CRC error is a control record, Control Complete may not be set in BSTAT bits 2–4 .

Command (in Hex)	Description
	Programming Note: Execution of the Load Record Number Register and Read Record command can be abruptly terminated if the diskette adapter executes the Reset Diskette command (hex 02), or detects one of the following conditions: Overrun/Underrun Command Reject Drive Error If one of these conditions causes the read record operation to be prematurely terminated, the last record may not be completely transferred. The contents of the record count register and the value in the channel pointer used for this operation identify where the operation was terminated.
38	Load Record Number Register and Write Record. This command causes the diskette adapters to load the record number register with the starting record number using PIO execution, and then to load the first 128-byte data buffer from main storage using CHIO burst transfers. After the first data buffer is loaded, the record length field in the diskette control register identifies the record length that is to be written. If the record length is greater than 128 bytes per record, the diskette adapter loads the second 128-byte data buffer while it is searching for the selected record number on the diskette. The byte operand received from the program during the PIO execution phase of this operation determines whether a data record or a control record is to be written. When bit 0 of the data received from the program is 0, a data record is written by the diskette adapter. When bit 0 of the data received is 1, a control record is written by the diskette adapter. The remainder of the byte operand specifies the starting record number register. **Programming Note**: The write record command can be used to write multiple data records or multiple control records, but the two types of records cannot be mixed during execution of one write record command. If one control record is to be written in between several data records, a separate Write Record command must be issued to write the control record. The diskette adapter automatically writes the address marker corresponding to the specified record type that is to be written during this operation. As each record is written, the diskette adapter automatically writes the sync field and the address marker associated with the data to the control record. At the end of each record written, the diskette adapter also writes the two CRC characters that it has generated as the data or control information was written on the diskette. When the CRC bytes have been written, the write operation for that record is completed and the diskette adapter either searches for the next record number if a multirecord write operation is in progress, or presents an interrupt request to the PCE to notify the program that completion status is available in the diskette BSTAT. For a normal

Command (in Hex)	Description

completion, the Operation Complete code is set into BSTAT bits 2, 3,4, — binary 000; the Control Complete code is not set by this command regardless of whether data or control records were written.

Programming Notes:

1. Execution of this command can be abruptly terminated if the diskette adapter detects an Overrun/Underrun condition, a Command Reject condition, or a Drive Error condition, or executes the Reset Diskette Adapter command (hex 02). These conditions can cause the diskette adapter to terminate the write operation prematurely; the last record may not be completely transferred under these conditions. The contents of the record count register and the value in the CHP used for this operation identify where the operation was terminated. For these conditions, the CRC characters at the end of the data or control record are not written on the diskette. The program must rewrite the record with the missing CRC characters to prevent unrecoverable read errors during subsequent accesses of that record.

   When a multirecord write operation is prematurely terminated, the number of records that remain to be transferred can be determined by issuing the Read Diskette Status Extension Register command (hex 05). The contents of the record count register are returned in bits 2–6 of the byte operand. Because the record number register cannot be read, the current record number must be calculated using the contents of the record count register.

   The Reset Adapter command (hex 02) is described earlier in this section under "Reset Diskette Adapter." The Drive Error condition and the Overrun/Underrun condition are described in this chapter under "Diskette Basic Status Register."

2. Write record operations do not verify the CRC bytes written with each record.

   Either of two operations is recommended to verify the CRC bytes:

   a. Read-back check operations

   b. Read record operations

   Either of these commands can detect write-error conditions only if it is used before the source data is destroyed, scratched, or otherwise made unavailable. Failure to use either a Read Back Check command or a Read Record command to verify records written on the diskette can result in a permanent read error when the record is next accessed.

Command (in Hex)	Description
	3. On the 8130 and 8140 (all models) only: When executing a multirecord write in 128-byte single-density mode, the adapter transfers an extra 128 bytes of data from main storage to the adapter. This data is not written on the diskette, but may cause storage protection checks.
60	Load Record Number Register and Read Back Check. This command provides a means of verifying the integrity of the records written on the diskette by checking that the CRC bytes match the data in a record. When this command is issued by the program, the byte of data that identifies the starting sector number is transferred during the PIO execution phase of this command. The diskette adapter searches for the starting record number just as if this were a Load Record Number Register and Read Record operation. The major difference between this command and the read command is that this command does not transfer any data to main storage; this command only verifies the CRC bytes at the end of each record. The CRC bytes for multiple data or control records can be verified by loading the record count register with a value that is 1 less than the desired number of records to be verified before this command is issued. The Load Record Number Register and Read Back Check command does not differentiate between data and control records during its execution. Unlike the Read Record command, this command verifies the CRC bytes of the data records and control records without interruption when a multirecord operation is specified. When all specified records have been verified, the diskette adapter presents an interrupt request to the PCE to notify the program that completion status is available in the diskette BSTAT. This command only returns the Operation Complete code in BSTAT bits 2, 3, 4, — binary 000; it does not set Control Complete. If the CRC bytes read at the end of the current record do not match the CRC bytes generated by the diskette adapter as the record was read, the operation is terminated, the CRC Error code is set in BSTAT bits 0, 1 — binary 01, and an interrupt request is presented to the PCE to notify the program that the operation was terminated. If a multirecord operation was in progress when the error was detected, the record count register contains the number of records that remain to be verified. Issuing the Read Diskette Status Extension register command (hex 05) causes the contents of the record count register to be returned to the program. Because the record number register cannot be read, the failing record number must be calculated.

Command (in Hex)	Description
	Programming Note:
	Read-back check operations are recommended to verify CRC for each record written on the diskette.
	This command can detect and correct temporary write-error conditions only if it is used before the source data is destroyed, scratched, or otherwise made unavailable. Failure to verify records written on the diskette using this command can result in permanent read errors the next time a record containing a CRC error is accessed.
78	Write Track. This command provides a means to write an entire track, including all gaps, address markers, sync fields, data or control fields, and the CRC bytes for both the data/control fields and the ID fields. The description of this command is divided into three topics: "Write Track PIO Execution Phase," "Data Requirements for Write Track,"and "Write Track CHIO Execution Phase."
	Programming Note: Before this command is issued, the program must ensure that the read/write heads are positioned over the correct track. The diskette adapter does not verify the location of the access mechanism before writing the specified data on the diskette. The program is also responsible for ensuring that the data provided to the diskette adapter is correct; the diskette adapter does not check the format of data received from the program.
	Write Track PIO Execution Phase. When the program issues this command, a byte operand is transferred to the diskette adapter during the PIO execution phase of this command. Bit 0 of this operand specifies the head selection for the Write Track operation. Then bit 0 is 0, head 0 is selected for this operation; when bit 0 is 1, head 1 is selected for this operation. The remainder of this data operand is ignored by the diskette adapter. The diskette defines whether the track is written in single- or double-density recording mode, and it also defines the length of the data records in each sector.
	Data Requirements for Write Track. The diskette adapter requires that a data area in main storage be provided for executing the Write Track command. This data area is defined as follows:
	One 128-byte block of control information is required for each sector that is to be written during this operation. The record length field in the drive control register defines the length of the data records in the track and therefore determines the number of sectors to be written. These 128-byte blocks must be contiguous in main storage. The format of these 128-byte blocks is determined by the recording mode specified for the track. These blocks contain control information used by the diskette adapter to write each sector on the track. The information in the first block is repeated in all subsequent blocks since all sectors are

single-density recording mode is shown in Figure 3-3. The block data format for double-density recording mode is shown in Figure 3-4.

Three additional 128-byte blocks contain gap data. For single-density recording mode, these blocks contain 128 bytes of hex FF; for double-density, they contain 128 bytes of hex 4E.

Byte Address	Contents	Normal Data (Hex)	Byte Address	Contents	Normal Data (Hex)
00	Gap Data	FF	103	Gap Data	FF
↓	↓	↓	104	Gap Data	FF
69	Gap Data	FF	↓	↓	↓
70	Sync Byte 1	00	112	Gap Data	FF
71	Sync Byte 2	00	113	Gap Data	FF
72	Sync Byte 3	00	114	Sync Byte 1	00
73	Sync Byte 4	00	115	Sync Byte 2	00
74	Sync Byte 5	00	116	Sync Byte 3	00
75	Sync Byte 6	00	117	Sync Byte 4	00
76	AM1 Byte	FE	118	Sync Byte 5	00
77	Not Used	"XX"	119	Sync Byte 6	00
↓	↓	↓	120	AM2 Byte	FB, F8
96	Not Used	"XX"	121	Not Used	"XX"
97	Cylinder	00 to 4C	122	Not Used	"XX"
98	Head	00, 01	123	Not Used	"XX"
99	Record Number	01 to 1A	124	Data Byte	"XX"
100	Record Length	00, 01, 02	125	Data CRC1	"XX"
101	ID CRC1	"XX"	126	Data CRC2	"XX"
102	ID CRC2	"XX"	127	Gap Data	FF

Notes:

1. *The value for the ID field CRC bytes and the data field CRC bytes must be provided by the program in block locations 101, 102 and 125, 126 respectively. An algorithm that can be used to calculate the CRC byte values is available in Appendix C.*

   The data string for the ID field consists of the AM1 and the four ID bytes.

   The data string for the data or control record consists of the AM2 and the data byte specified in location 124, repeated the number of times equal to the record length.

2. *Byte location 120 specifies a data record with hex FB or a control record with hex F8.*

3. *Byte location 124 specifies the data byte that is repeated the number of times specified by the record length.*

Figure 3-3. Single-Density Write Track Control Information Format

Byte Address	Contents	Normal Data (Hex)	Byte Address	Contents	Normal Data (Hex)
00	Gap Data	4E	86	Gap Data	4E
↓	↓	↓	87	Gap Data	4E
63	Gap Data	4E	↓	↓	↓
64	Sync Byte 1	00	106	Gap Data	4E
65	Sync Byte 2	00	107	Gap Data	4E
↓	↓	↓	108	Sync Byte 1	00
74	Sync Byte 11	00	109	Sync Byte 2	00
75	Sync Byte 12	00	↓	↓	↓
76	AM1 Byte 1	A1	118	Sync Byte 11	00
77	AM1 Byte 2	A1	119	Sync Byte 12	00
78	AM1 Byte 3	A1	120	AM2 Byte 1	A1
79	AM1 Byte 4	FE	121	AM2 Byte 2	A1
80	Cylinder	00 to 4C	122	AM2 Byte 3	A1
81	Head	00, 01	123	AM2 Byte 4	FB, F8
82	Record Number	01 to 1A	124	Data Byte	"XX"
83	Record Length	01	125	Data CRC1	"XX"
84	ID CRC1	"XX"	126	Data CRC2	"XX"
85	ID CRC2	"XX"	127	Gap Data	4E

Notes:

1. *The value for the ID field CRC bytes and the data record CRC bytes must be provided by the program in byte locations 84, 85 and 125, 126, respectively. An algorithm that can be used to calculate the CRC byte values is available in Appendix C.*

   The data string for the ID field consists of the AM1 (four bytes) and the four ID bytes.

   The data string for the data or control record consists of the AM2 (four bytes) and the data byte specified in location 124, repeated the number of times equal to the record length.

2. *Byte location 123 specifies a data record with hex FB or a control record with hex F8.*

3. *Byte location 124 specifies the data byte that is repeated the number of times specified by the record length to fill the data or control field.*

Figure 3-4. Double-Density Write Track Control Information Format

Write Track CHIO Execution Phase. When the diskette adapter has selected the read/write head identified in the PIO operand sent by the program, the PIO execution phase is complete. The diskette adapter initiates a CHIO burst transfer to load the first 128-byte data buffer from the first block of control information. Both 128-byte data buffers are loaded before the write operation is begun. When the buffers are loaded, the next Index signal causes the diskette adapter to begin writing the track format data on the diskette. As each sector is written on the diskette, the diskette adapter reloads the empty buffer with the next 128-byte block of control information until all sectors have been written on the diskette. The diskette adapter then loads the buffers with the blocks of gap data on the diskette until the next Index signal is detected. The Write Track operation is ended when the Index signal is detected. The diskette adapter then presents an interrupt to the PCE to notify the program that the operation has been completed.

Programming Note: The Write Track command must be completed in one revolution of the diskette. When this command is issued, the system activity must permit the CHIO burst transfers required to transfer the 128-byte blocks of control information to the diskette adapter's data buffers without interrupting the write operation. If the write operation is interrupted because a data buffer is needed to continue writing, and that buffer has not yet been loaded, the write operation is terminated. The diskette adapter presents an interrupt request to the PCE to notify the program that the operation was terminated; the Overrun/Underrun code is set in the diskette BSTAT bits 2, 3, 4 — binary 100.

When a Write Track operation is terminated with an error condition, the track cannot be used until it is correctly written with a subsequent Write Track command.

Programming Note: A Read Verify should be performed to ensure that the format is correct. After performing a Write Track operation in 1,024 byte double-density mode, rewrite the data using a Load Record Number Register and Write Record command (hex 38).

Seek Commands

Eight Seek commands are implemented by the diskette adapter. Two of these commands do not cause access motion to occur; they cause head 0 or head 1 to be selected for the next operation.

Seek commands result *only* in movement of the read/write heads; the diskette adapter *does not* verify the resulting location of the read/write heads on the diskette surface. The program includes a byte of data with each Seek command that specifies how many tracks are to be crossed when the read/write heads are moved. The PIO execution phase of the Seek commands is completed when the byte operand is accepted by the diskette adapter. The seek operation is performed asynchronous to instruction execution. At the completion of the seek operation, an interrupt request is returned to the PCE to notify the program of the completion.

Programming Note: After a Seek command has been executed by the diskette adapter, the program *must issue* either the Read ID command (hex 20) or the Read ID Next command (hex 22) to verify that the read/write heads are correctly positioned. Failure to follow this procedure may result in unpredictable data operations and in the destruction of the data on that diskette.

One byte of data is sent to the diskette adapter with each of the Seek commands that cause the read/write heads to be moved; this byte of data identifies whether the access motion is to be *out* (towards cylinder 76) or *in* (towards cylinder 0), and also provides a value equal to 1 less than the number of cylinders that are to be crossed during the seek. The format of this data is as follows:

0 1 - - - - - 7

In/Out Number of cylinders to be crossed -1

bit 0 = 0 — seek *in* towards cylinder 0.
bit 0 = 1 — seek *out* towards cylinder 76.

This data operand is not required for Seek commands that only result in head selection (hex 80 and hex 88).

When the diskette adapter receives a Seek command and its 1-byte operand, the diskette adapter loads bits 1–7 of the data operand into the record count register. During the head movement, the diskette adapter is busy (BSTAT bits 2, 3, 4 set to the Busy code — binary 011). The value in the record count register is decremented by the diskette adapter each time a cylinder is crossed until the record count register contains zero. At that time, the seek operation is complete and the diskette adapter presents an I/O interrupt request to the PCE to indicate the completion of the operation. If a command other than hex 02, 03, or 07 is received while the seek operation is in progress, the seek is immediately terminated with BSTAT bits 0, 1 set to Command Reject.

Programming Note: The destination cylinder *must* be reflected in the Seek command code issued by the program. If the command code specifying the destination cylinder range is not matched with the actual destination cylinder, the diskette adapter may return false indications of *No Record Found* or *CRC Error* during execution of subsequent data transfer commands.

If a seek operation is prematurely terminated, the record count register contains a value that is 1 less than the number of track crossings that remained when the seek was terminated. Only the low-order 5 bits of this value can be accessed through programming using the Read Diskette Status Extension Register command (hex 05).

In summary, the Seek commands implemented by the diskette adapter are:

Command (in Hex)	**Description**
80	Select Head 1, No Seek
82	Seek, Select Head 1, cylinder range 00–41
84	Seek, Select Head 1, cylinder 42–59
86	Seek, Select Head 1, cylinder range 60–76
88	Select Head 0, No Seek
8A	Seek, Select Head 0, cylinder range 00–41
8C	Seek, Select Head 0, cylinder range 42–59
8E	Seek Select Head 0, cylinder range 60–76

Diskette Channel I/O (CHIO) Operations

The 8100 diskette storage facility uses channel I/O (CHIO) operations to transfer data between the diskette media and main storage. The diskette adapter implements PIO commands that load certain values to prepare the diskette adapter for a subsequent CHIO operation. The diskette adapter does not implement a unique Initiate CHIO command; rather, several dual-purpose PIO commands termed *data transfer commands* are implemented to load the starting record number register and then initiate a CHIO operation to transfer the specified ID field or data record to or from main storage. These commands are described in detail under "Data Transfer Commands" earlier in this chapter. General CHIO operations are described in detail in the *8100 Principles of Operations*; the specific implementation of the diskette adapter is described in this section.

CHIO Request Priority

The diskette adapter is assigned to the channel request-low (CR-lo) priority chain in the SSCF to which it is attached. The channel request priority (CRP) value assigned to each SSCF is detailed in the 8130 and 8140 processor description manuals under "Channel I/O Operations."

Diskette CHIO Operation Introduction

The diskette can perform CHIO operations from the reset after BSTAT bit 6 (diskette enabled) has been set to 1. No programmed setup is required; however, the diskette adapter will use channel pointer (CHP) 0, and it will only perform single-record transfers of 128-byte records in single-density recording mode. If a CHP other than 0 is to be used, or if multirecord transfers are desired, the program must prepare the diskette adapter for the CHIO operation by performing the example steps shown in Figure 3-5.

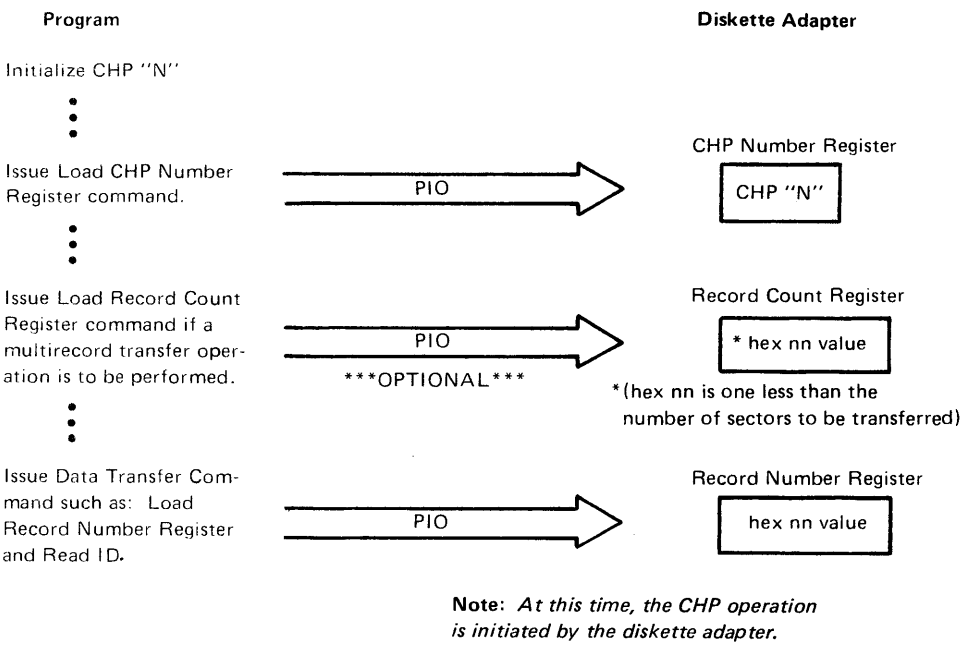


Figure 3-5. Example of CHIO Preparation

Initiating a CHIO Burst Transfer

When the diskette adapter has loaded the first 128-byte buffer for a read record operation, or when a write record operation has been received, it activates the Channel Request signal to request a CHIO burst transfer. *The CHIO burst transfer length for the diskette adapter is 64 bytes.* Several CHIO bursts may be required to transfer the data record being read or written, but each CHIO burst transfer is initiated as shown in Figure 3-6. One CHIO operation consists of at least two CHIO burst transfers for 128-byte records; for read ID operations, however, only 4 bytes are transferred during each CHIO burst.

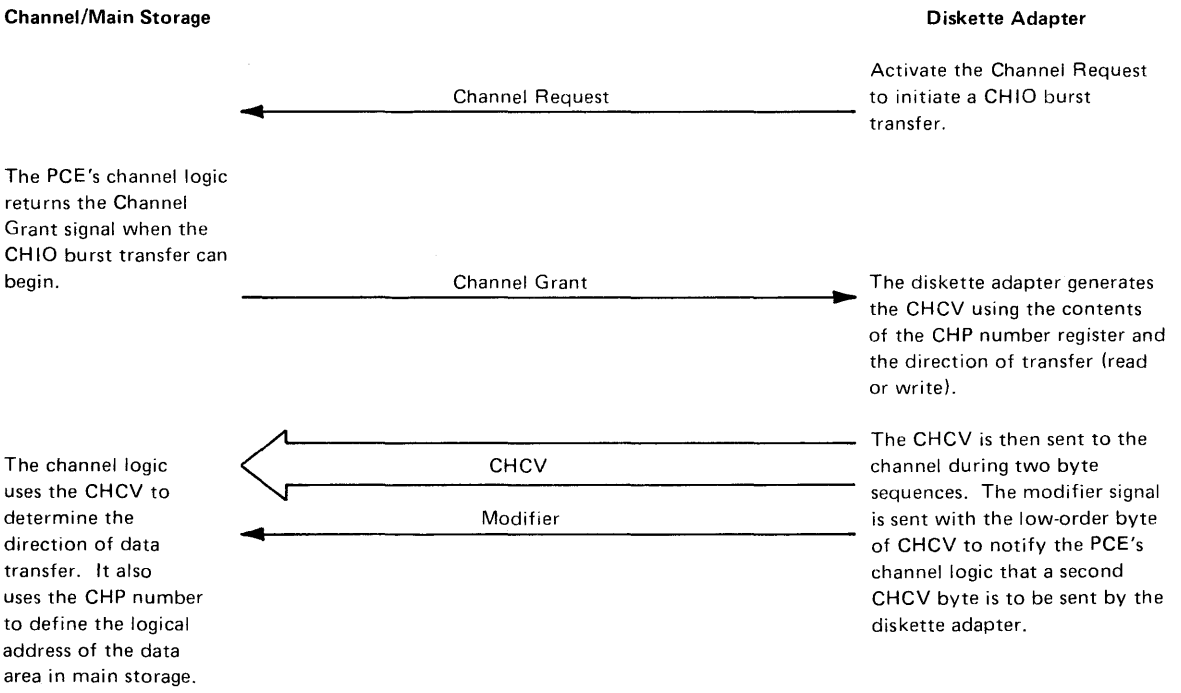
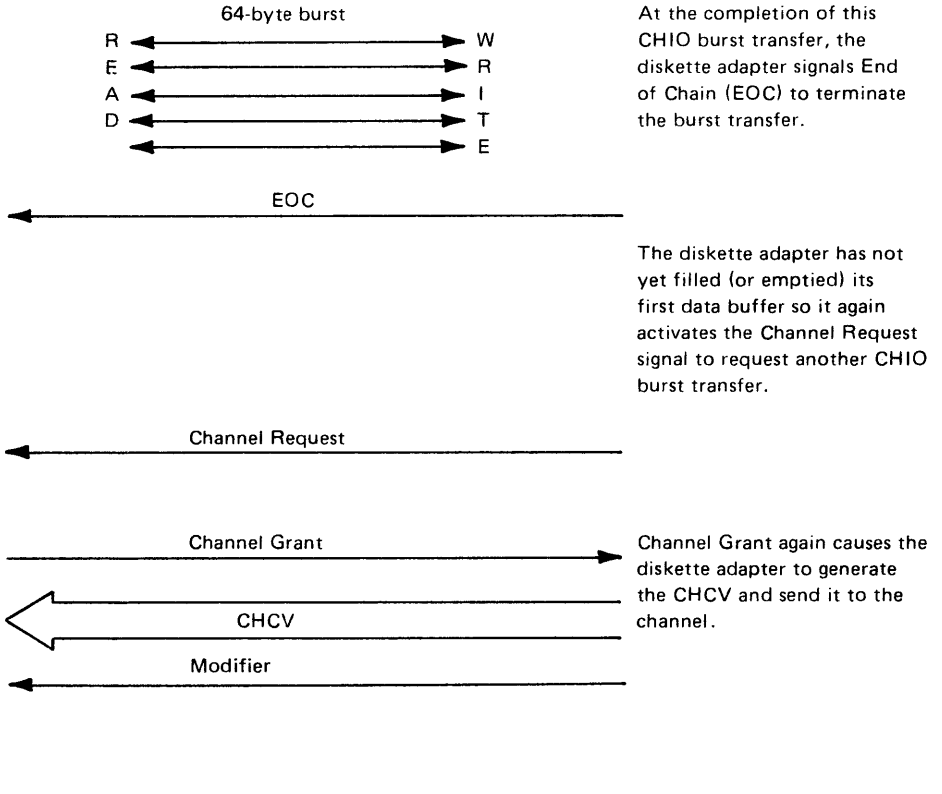


Figure 3-6 (Part 1 of 2). Initiating CHIO Burst Transfers

Channel/Main Storage **Diskette Adapter**

The first 64 bytes of data are now transferred between main storage and the diskette adapter's data buffers.



At the completion of this CHIO burst transfer, the diskette adapter signals End of Chain (EOC) to terminate the burst transfer.

The channel logic ends the CHIO burst by updating the address in the CHP to reflect the data transfer and stores the CHP in the PCE's register storage.

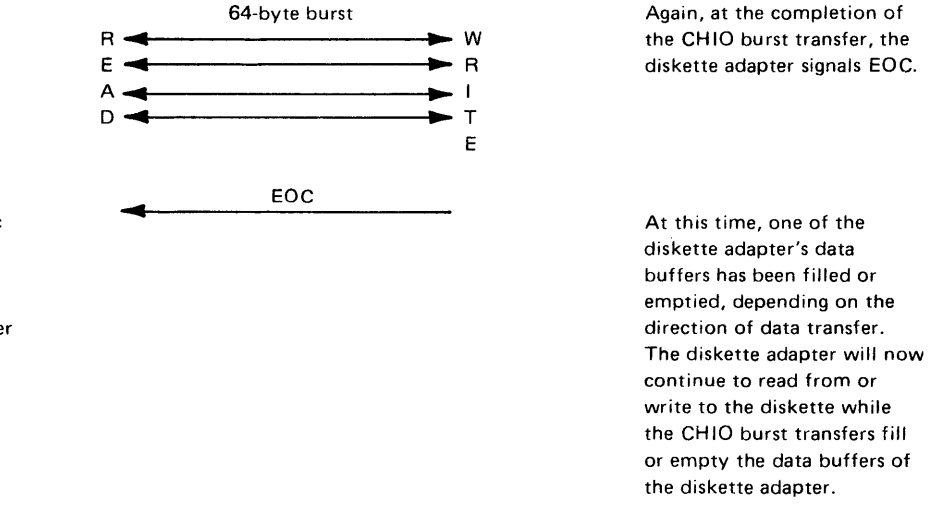
The diskette adapter has not yet filled (or emptied) its first data buffer so it again activates the Channel Request signal to request another CHIO burst transfer.

Again, Channel Grant is returned.

Channel Grant again causes the diskette adapter to generate the CHCV and send it to the channel.

The channel logic again accesses the CHP specified in the CHCV and establishes the direction of data transfer.

The next 64 bytes of data are transferred between main storage and the diskette adapter's data buffers.



Again, at the completion of the CHIO burst transfer, the diskette adapter signals EOC.

Again, the channel logic updates the value in the CHP to reflect the data transfer and stores the CHP in the PCE's register storage.

At this time, one of the diskette adapter's data buffers has been filled or emptied, depending on the direction of data transfer. The diskette adapter will now continue to read from or write to the diskette while the CHIO burst transfers fill or empty the data buffers of the diskette adapter.

Note: *The burst transfers shown in this figure are continued until the specified record or records have been transferred to or from main storage. For multirecord transfers, the diskette adapter continues the burst transfers shown in this figure, updating the record number register and decrementing the record count register as each record is transferred, until the specified number of records have been read or written.*

The program views the entire transfer as one CHIO operation; each burst transfer is a CHIO operation to the channel logic. When the burst transfer is completed, the channel is free to service another channel request from a different device.

Figure 3-6 (Part 2 of 2). Initiating CHIO Burst Transfers

Examples of Diskette Data Transfer Operations

This section presents two examples of typical data transfer operations: the first is a read record operation, and the second is a write record operation. Both examples describe a multirecord transfer. The CHIO burst transfers are not described in detail in these examples; rather, they are identified where they occur.

For both examples, four records labeled Rec 01 through Rec 04 are transferred; their record numbers are hex 01 through hex 04 for simplicity. The record length is 256 bytes, and the recording mode is double density. In these examples, the CHP number register is loaded during the setup of the diskette adapter; in reality, this may not be required. The program may choose to use the same CHP for all diskette operations and redefine the logical address in the CHP before data transfer operations are begun.

These examples do not show the positioning of the access mechanism, verification of the location of the read/write heads, or setting the record length and recording mode value in the diskette control register. The activity is assumed to have been done before the beginning of the example.

The example of a multirecord read operation is shown in Figure 3-7. Figure 3-8 shows a multirecord write operation. Neither example is intended to be a restrictive description of programmed techniques to accomplish these functions; they are both provided as samples that show the maximum amount of PIO setup for these functions.

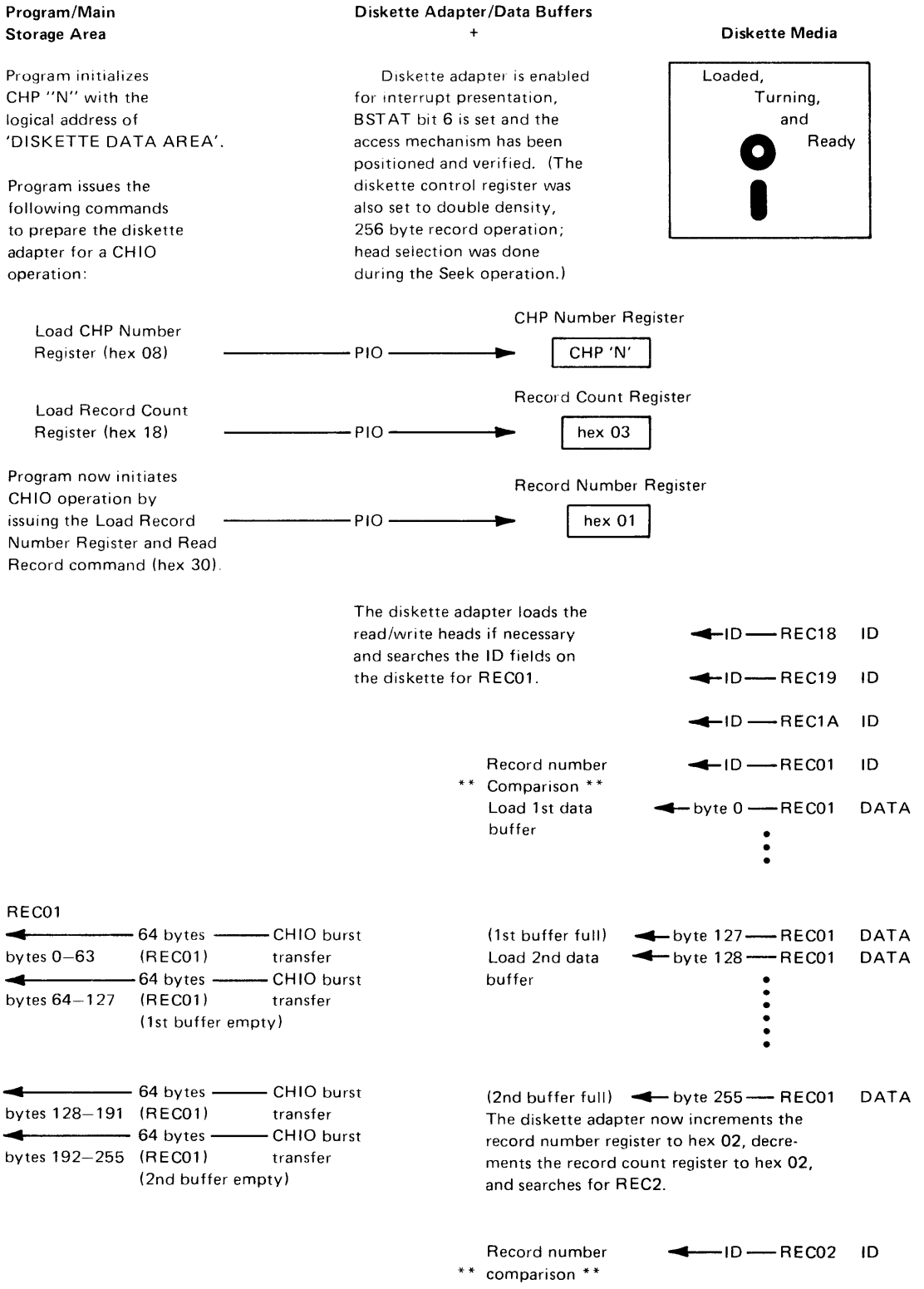


Figure 3-7 (Part 1 of 2). Sample Multirecord Read Operation

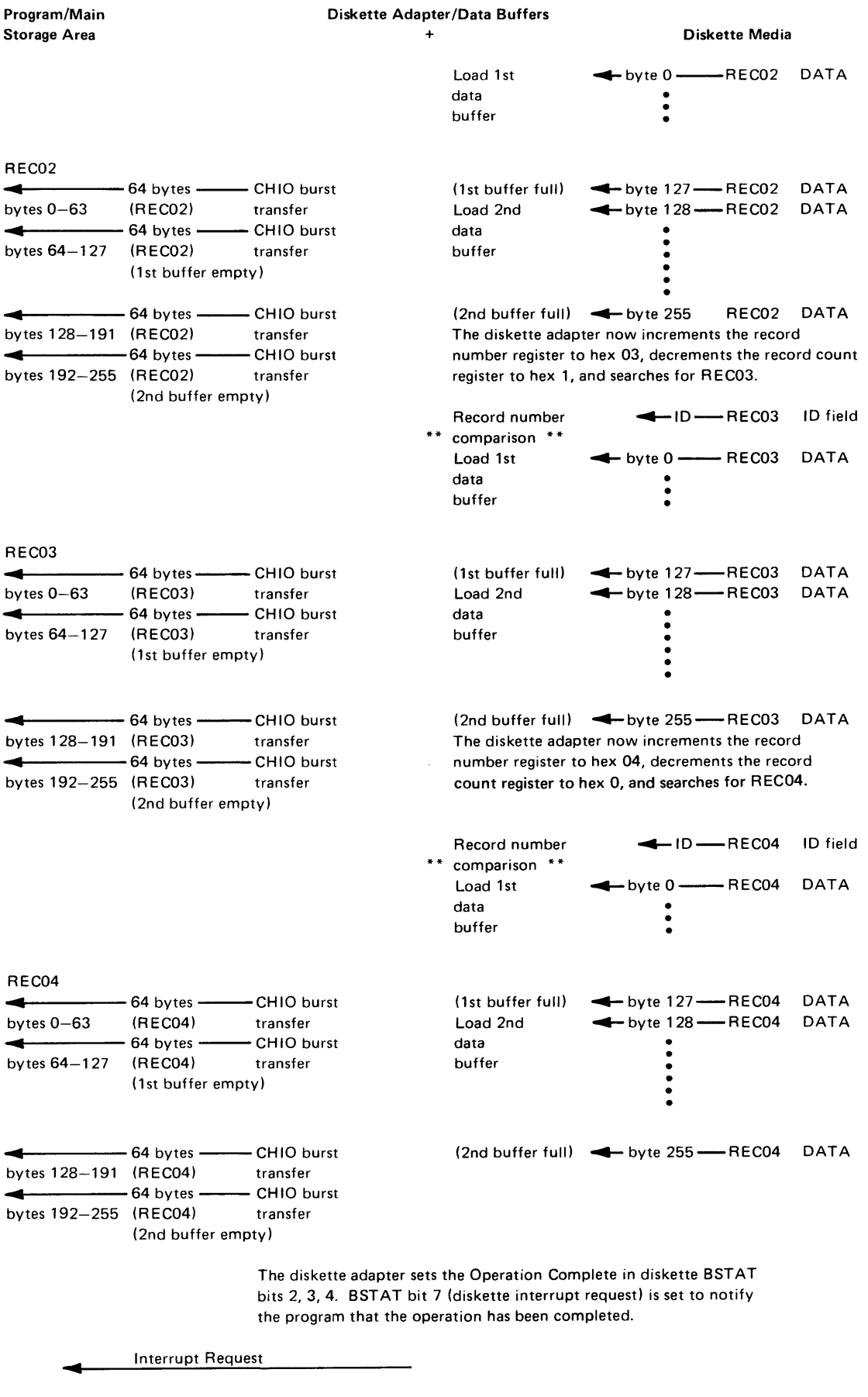


Figure 3-7 (Part 2 of 2). Sample Multirecord Read Operation

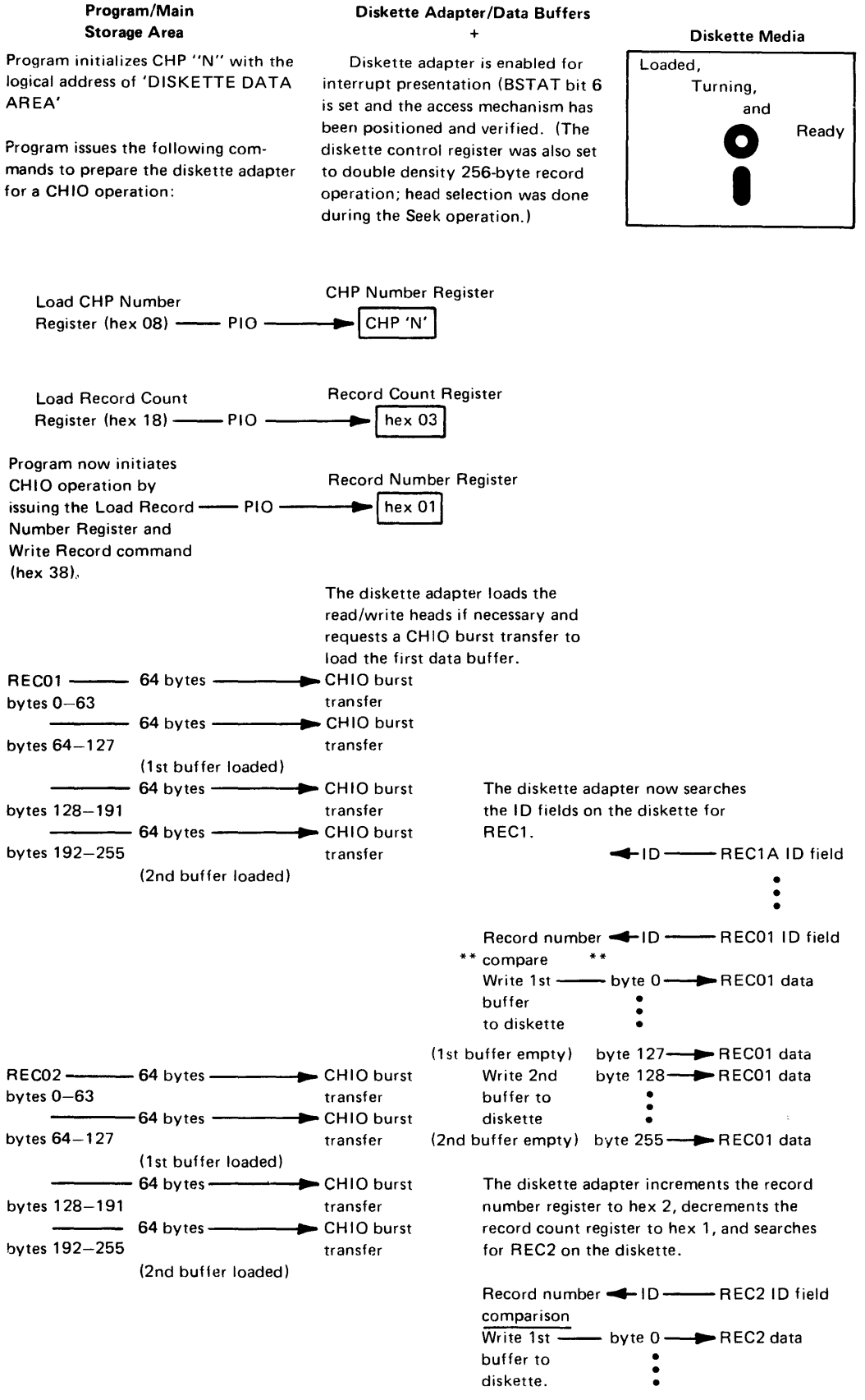


Figure 3-8 (Part 1 of 2). Sample Multirecord Write Operation

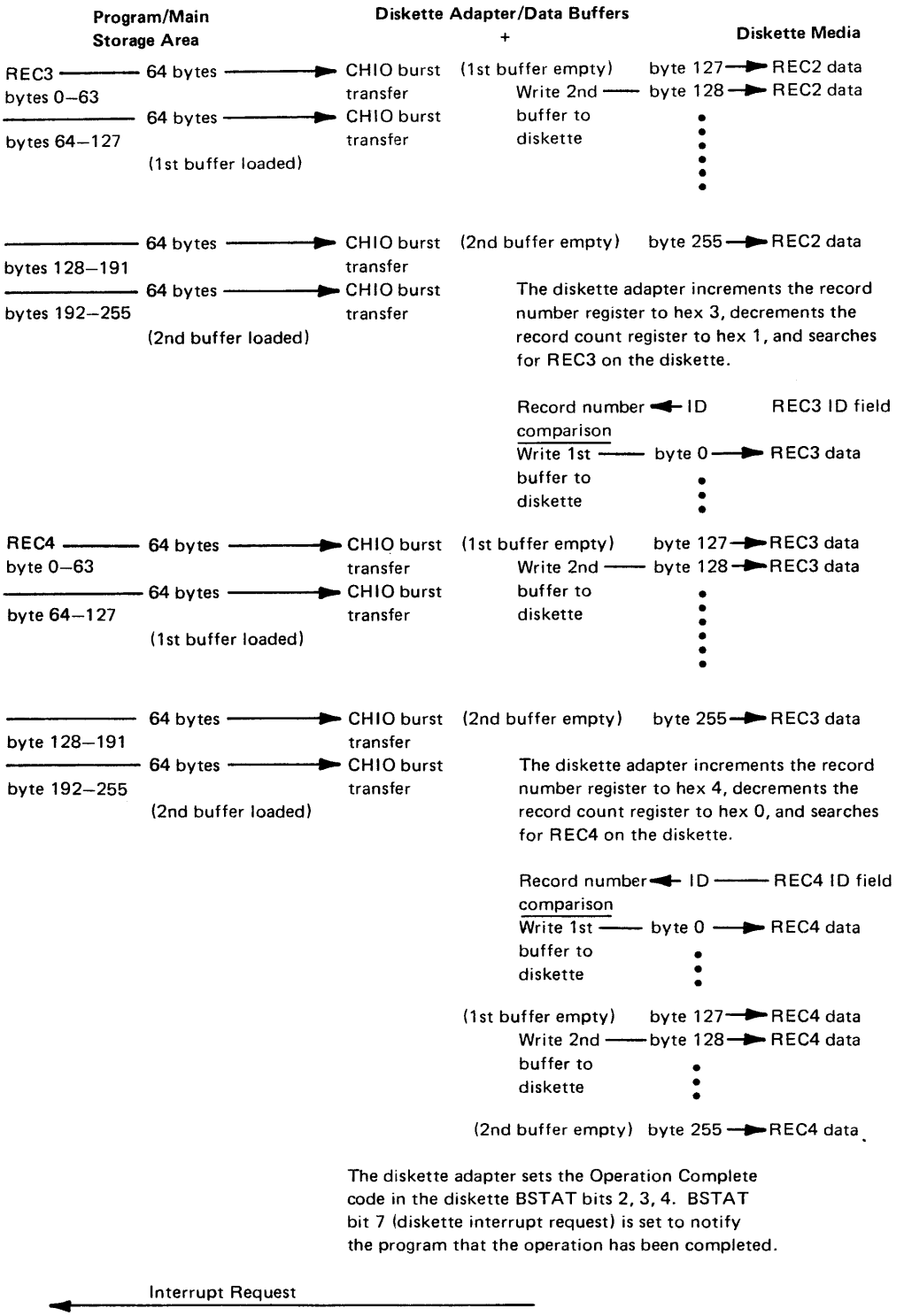


Figure 3-8 (Part 2 of 2). Sample Multirecord Write Operation

Diskette Adapter Error Detection and Reporting

This section summarizes the error-detection capabilities of the diskette adapter and describes how these errors are reported to the PCE and to the program.

As each record is read, the diskette adapter checks the bit configuration of the data read by generating a pair of CRC bytes that it compares against the CRC bytes read from the diskette at the end of record. If these CRC bytes are mismatched, the diskette adapter sets BSTAT bits 0, 1 to binary 01 (CRC error code) and presents an interrupt request to the PCE to notify the program that the error condition has been detected and that the data record that was transferred should be reread.

The diskette adapter also checks the parity of data that is transferred internally; if a parity check is detected on internal data transfers, the diskette adapter sets bit 1 (internal parity check) in the status extension register, sets BSTAT bits 0, 1 to binary 11 (parity check), and presents an interrupt to the PCE to notify the program that the operation should be retried.

The diskette adapter also checks the parity of all data and commands that are received from the program. If a parity check is detected, the diskette adapter sets bit 0 (external parity check) in the status extension register, sets BSTAT 0, 1 to binary 11 (Parity Check code), and presents an interrupt request to the PCE to notify the program that the data or command was out of parity. At the time the error is detected, the diskette adapter suppresses the response for the data or command, causing an I/O time-out condition. When the PCE's channel logic detects the I/O time-out condition, it sets bit 1 (I/O time-out check) in the PCE's error interrupt request vector to cause a system check interruption if the PCE is enabled for interrupt requests for priority level 0.

Appendix C summarizes the error conditions detected by the diskette adapter and the resulting status bits set in the diskette adapter's status registers.

Appendix A. Data Storage Capacities

Disk DASD Data Storage Capacities by Model

8130 Model	8140 Model	8101 Model	8102 Model	Capacity in Bytes	Head Configuration
A21	A31 A41 A51	A11		29,327,360	Movable
A22	A32 A42 A52			23,461,888	Movable and fixed
A23	A33 A43 A54	A13 A23		64,520,192	Movable
A24	A34 A44 A54			58,654,720	Movable and fixed
	B51 B61 B71			58,654,720	Movable and fixed
	B52 B62 B72			123,174,912	Movable and fixed
	C72 C82 C92			123,174,912	Movable and fixed
		A25		129,040,384	Movable
			A15	129,761,280	Movable
			A17	259,522,560	Movable

Diskette DASD Data Storage Capacities

Record Length	No. of Sectors	Track Capacity	Diskette Capacity
128 bytes (single density)	26	3,328	246,272 (diskette 1) 492,544 (diskette 2)
256 bytes (single density)	15	3,840	284,160 (diskette 1) 568,320 (diskette 2)
512 bytes (single density)	8	4,096	303,104 (diskette 1) 606,208 (diskette 2)
256 bytes (double density)	26	6,656	985,088 (diskette 2D)
512 bytes (double density)	15	7,680	1,136,640 (diskette 2D)
1024 bytes (double density)	8	8,192	1,212,416 (diskette 2D)

Appendix B. DASD Physical Specifications

Disk DASD Functional Specifications and Access Times

Disk Format

Data tracks per moving head	358 (720 in 8102 only)
Alternate sector tracks per moving head	1 (#64)
Diagnostic tracks per moving head	1 (#359 in 8130, 8140, and 8101; #721 in 8102)
Addressable sectors per track	32 (#0-#31)
Alternate sectors per track	1 (#32)
Flag bytes per ID field	1
Address bytes per ID field	3
Error detection code bytes per ID field	2 CRC bytes
Data bytes per data field	256
Error detection code bytes per data field	2 CRC bytes (4 ECC bytes in 8102 only)

Access Times

Head switching time (nominal)	8 sector times minus 40 microsec (8 sector times minus 150 microsec in 8102 only)
Moving head average access time (maximum)	27.0 ms
Moving head single track average access time (maximum)	9.0 ms
Disk rotation speed (nominal)	3,125 rpm
Data transfer rate (nominal-instantaneous)	1,031,000 bytes per second

Diskette DASD Physical Specifications

This section describes the disk drive physical specifications and the general format of the diskette media. Refer to the *IBM Diskette General Information Manual*, GA21-9182, for a more complete description of the diskette media.

Diskette DASD Functional Specifications and Access Times

Read/write heads	2 (opposed)
Access times:	
Average rotational delay	83 ms
Maximum rotational delay	166.7 ms
Average access time (38 cylinder seek)	225 ms
Maximum access time (77 cylinder seek)	420 ms
Single-track access time	40 ms
Automatic head load	80 ms
Data transfer rate:	
Single-density recording	31,250 bytes per second
Double-density recording	62,500 bytes per second
Disk rotational speed	360 rpm
Total Data tracks accessible	77 per side
Usable tracks	74 per side
Tracks reserved for labeling	1 (cylinder 0): single density, per sector format on head 0 for Diskette 1, 2, 2D; single density, 128 bytes per sector on head 1 for Diskette 2; double density, 256 bytes per sector on head 1 for Diskette 2D.
Tracks reserved for alternate track use	2 (tracks 75 and 76)
Sectors per track	26 15 8
Bytes per sector	128 256 512 (Diskettes 1 and 2) 256 512 1024 (Diskette 2D)

Note: Diskette access time can be calculated using the following formula: (5 ms × the number of tracks crossed) + 35 ms. The 35 ms is required for settling the read/write heads if they are loaded; if the read/write heads are not loaded, the 35-ms delay is replaced by an 80-ms delay to load the heads.

Appendix C. Error Status Summary

Disk Error Status Summary

Conditions for Setting Equipment Check (BSTAT 13) Bit

Condition	Adapter Basic Status									FCB Processor Status
	6	8	9	10	11	12	13	14	15	
Decode of invalid PIO	-	0	1	0	-	-	1	-	1	-
Address or PIO command received with bad parity	-	0	1	0	-	-	1	-	1	-
Bad parity on data received from PCE during PIO cycle	-	0	1	0	-	-	1	-	1	-
Bad parity on write data during FCB transfer CHIO	-	0	0	0	-	-	1	-	1	X'FE'
Bad parity on write data during data transfer CHIO	1	0	0	0	-	-	1	-	1	X'C7'*
Tag sequence error during adapter's I/O cycle	-	1	0	0	-	-	1	-	1	-
Set under mask PIO	-	0	0	0	-	-	1	-	1	-

* Multisector DATAOP in progress
**Single-sector DATAOP

Conditions for Setting Device Error (BSTAT 9) Bit

Condition	Adapter Basic Status										Seek Status			FCB Processor Status
	0	1	2	3	4	5	7	9	11	15	9	10	11	
PTY errors on internal PCE bus (PIO)	-	-	-	-	-	-	-	1	1	1	-	1	-	-
PTY error on internal PCE bus (data transfer) or on a DATAOP	1	-	-	-	-	-	-	1	0	1	0	0	0	F9
PTY errors internal to data handler	0	1	-	-	-	-	-	1	0	1	0	0	0	F9
ID CRC error	0	0	1	1	-	-	0	1	0	1	0	0	0	F9
Data field CRC error	0	0	1	0	1	-	-	1	0	1	0	0	0	F9
Record not found	0	0	0	0	0	1	0	1	0	1	0	0	0	F9
Adapter time-out	-	-	-	-	-	-	-	1	1	1	0	0	1	≤F7
FCB processor-detected errors	-	-	-	-	-	-	-	1	0	1	0	0	0	≥F8
Set under Mask PIO	-	-	-	-	-	-	-	1	0	1	-	-	-	-

Diskette Error Status Summary

Error Condition	Diskette BSTAT 0, 1	Diskette BSTAT 2, 3, 4	Diskette BSTAT 5	Diskette BSTAT 7	Status Extension 0	Status Extension 1	System Check
PIO address PC							Yes
Invalid command	10	000	1	1	0	0	Yes
Command PC	11	000	1	1	1	0	Yes
PIO write data PC	11	000	1	1	1	0	Yes
CHIO write data PC	11	000	0	1	1	0	No
Channel-detected PC (read data or CHCV transfer)	00	000	1	1	0	0	Yes
Internal PC-detected during:							
Read ID/Read Record	11	000	1	1	0	1	Yes
Write Record	11	000	0	1	0	1	No
CHIO Prefetch for Write	11	000	1	1	0	1	Yes
CRC error during read record operation	01	000/1	0	1	0	0	No
CRC error during read record CHIO transfer	01	000/1	1	1	0	0	Yes
Read-back check CRC error	01	000	0	1	0	0	No
Command reject during busy	10	000	0	1	0	0	No
Drive error	00	010	0	1	0	0	No
Drive error during CHIO transfer	00	010	1	1	0	0	Yes
Overrun/underrun	00	100	0	1	0	0	No
Time-out	00	101	0	1	0	0	No
Record not found	00	110	0	1	0	0	No
Data transfer or Seek command received while diskette not ready	00	111	0	1	0	0	No

Appendix D. Sample 8100 Assembler Language Code to Generate Cyclic Redundancy Check (CRC)

The following 8100 assembler language instructions will generate the CRC bytes required by the diskette for a Write Track command. The symbols used are defined as follows:

CRC	A halfword general register used to accumulate the CRC. It must be initialized to X'FFFF'.
HICRC	The high-order byte of CRC.
DATA	A byte general register that contains the byte to be added to the CRC.
HWR	A halfword general register used as a work register.
HIBR	The high-order byte of HWR.
LOBR	The low-order byte of HWR.

XR	HICRC, DATA	Exclusive-OR high-order CRC byte with data byte.
LRI	HIBR, 0	Clear high-order byte of work register.
LR	LOBR, HICRC	Move high-order byte of CRC to low-order byte of work register.
RLH	HWR, 4	Rotate work register 4 bits left.
XR	LOBR, HICRC	Exclusive-OR low-order byte of work register with high-order byte of CRC.
NRI	LOBR, X'F0'	Delete low-order four bits of work register.
XHR	CRC, HWR	Exclusive-OR CRC with work register.
RLH	HWR, 1	Rotate work register 1 bit left.
RLH	CRC, 8	Exchange bytes of CRC.
XHR	CRC, HWR	Exclusive-OR CRC with work register.

At the conclusion of this instruction sequence, the register CRC will contain the CRC value. This sequence must be repeated for every byte included in the CRC.

The bytes included in the CRC calculation are:

- For a sector ID:
  - The AM1 byte(s) (X'FE' for single density; X'A1A1A1FE' for double density)
  - The C, H, R, and N bytes of the sector ID (see table below). For additional information, see *IBM Diskette General Information Manual*, GA21-9182.
- For the data portion of the sector:
  - The AM2 byte(s) for the sector (X'F8' or X'FB' for single density; X'A1A1A1F8' or X'A1A1A1FB' for double density)
  - The data bytes of the sector.

Diskette Type	Physical Record Length (Bytes)	C Cylinder Number (Hex)	H Head Number (Hex)	R Record Number (Hex)	N
1	128	00–4A	00	01–1A	00
2	128	00–4A	00, 01	01–1A	00
1	256	00–4A	00	01–0F	01
2	256	00–4A	00, 01	01–0F	01
2D	256	00–4A	00, 01	01–1A	01
1	512	00–4A	00	01–08	02
2	512	00–4A	00, 01	01–08	02
2D	512	00–4A	00, 01	01–0F	02
2D	1,024	00–4A	00, 01	01–08	03

Glossary

This glossary includes terms and definitions from the *IBM Vocabulary for Data Processing, Telecommunications, and Office Systems,* GC20-1699.

Most entries in this glossary are defined as they apply to the 8100 Information System.

A

access control. The field of a translation-table entry that controls the types of storage accesses permitted during the fetching and execution of an instruction or during a channel I/O operation.

ACV. Address control vector.

adapter. Hardware that is generally required to transfer data and commands between the processor and an I/O device.

ADDR. Address.

address base. The field of an address control vector that designates the origin of a logical address space in the PCE address space. It is concatenated with a logical address during dynamic address relocation.

address control vector (ACV). The formatted information used to control dynamic address relocation and the activation of dynamic address translation.

address limit. The field of an address control vector that designates the maximum logical address in a logical address space. It is used to check the validity of a logical address during dynamic address relocation.

adjunct register. A 32-bit register used as storage for an address control vector (ACV); only the low-order 16 bit positions are available to the program.

adjunct register set. A set of eight adjunct registers located consecutively in the adjunct register group.

application mode. The mode of program execution that allows processing of all instructions, except those that are supervisor-privileged or I/O-privileged.

array. An arrangement of elements in one or more dimensions.

assembler. A computer program used to translate a symbolic language program into a machine language program by substituting absolute operation codes for symbolic operation codes and absolute or relocatable addresses for symbolic addresses.

asynchronous. Without regular time relationship; unexpected or unpredictable with respect to the execution of a program's instructions.

B

base address. Either the instruction address or the content of a general register from which a logical address is derived during instruction execution by combination with a displacement.

basic status register (BSTAT). A 1- or 2-byte register that contains control logic status information.

binary code. A code that makes use of exactly two distinct characters, usually 0 and 1.

binary digit. In binary notation, either of the characters 0 and 1. Synonymous with *bit.*

binary synchronous communication (BSC). Communication using binary synchronous transmission, that is, data transmission in which synchronization of characters is controlled by timing signals generated at the sending and receiving stations.

bit. Synonym for *binary digit.*

block. (1) A string of records, a string of words, or a character string formed for technical or logic reasons to be treated as an entity. (2) A set of things, such as words, characters, or digits, handled as a unit. (3) A collection of contiguous records recorded as a unit. Blocks are separated by interblock gaps, and each block may contain one or more records.

block address. The field in a translation table entry that contains the common high-order bits of the real addresses associated with a 2048-byte block of physical main storage.

BSC. Binary synchronous communication.

BSC/S-S communication control. The logic that allows system connection to a variety of devices that use start/stop or binary synchronous communication facilities.

BSTAT. Basic status register.

buffer. An area of storage that is temporarily reserved for use in performing an input/output operation, into which data is written or from which data is read.

burst. In data communication, a sequence of signals counted as one unit in accordance with some specific criterion or measure.

byte. (1) A binary character operated upon as a unit and usually shorter than a computer word. (2) The representation of a character. (3) A sequence of eight adjacent binary digits that are operated upon as a unit and that constitute the smallest addressable unit in the system.

byte operand. An 8-bit unit of data referenced as an operand of an instruction. See also *operand.*

C

C-bit. One of the four condition indicators.

CG. Channel grant.

CG-hi. Channel grant high.

CG-lo. Channel grant low.

CG-med. Channel grant medium.

channel. The facility that controls the transmission of information between the PCE or main storage and an I/O device.

channel control vector (CHCV). The formatted information that specifies the controlling parameters, such as the channel I/O command, used during a channel I/O operation.

channel grant (CG). A signal from the PCE granting the control logic permission to start a previously requested channel I/O operation. The signal can be one of three priorities, listed from lowest to highest: channel grant low (CG-lo), channel grant medium (CG-med), and channel grant high (CG-hi).

channel grant high (CG-hi). The first-priority channel-grant signal.

channel grant low (CG-lo). The third-priority channel-grant signal.

channel grant medium (CG-med). The second-priority channel-grant signal.

channel input/output (CHIO) burst operation. That portion of a channel operation during which the channel and an I/O device are logically connected for transferring information.

channel input/output (CHIO) operation. The transfer of data between main storage and an I/O device. The operation consists of one or more channel I/O burst operations. It is initiated by the control logic rather than the PCE, and is controlled by the PCE's channel logic. PCE instruction execution is temporarily suspended while a CHIO operation is in progress.

channel I/O command. The field of a channel control vector that directs a channel and an I/O device to perform a channel I/O burst operation.

channel mask. The 1-bit mask used to suspend channel I/O operations.

channel pointer (CHP). The principal register containing the logical address used during a channel I/O operation.

channel pointer number. The field of a channel control vector that designates the channel pointer to be used during a channel I/O operation.

channel request. A signal from the control logic indicating that the control is requesting permission to start a channel I/O operation.

channel request high (CR-hi). The first-priority channel-request signal.

channel request low (CR-lo). The third-priority channel-request signal.

channel request medium (CR-med). The second-priority channel-request signal.

channel request priority (CRP). Logic in the system control facility that establishes the priority of each adapter's request to initiate CHIO operations.

character. A letter, digit, or other symbol that is used as part of the organization, control, or representation of data.

CHCV. Channel control vector.

CHIO. Channel input/output (operation).

CHP. Channel pointer.

command. A character string from a source external to a system that represents a request for system action.

common mask. The 8-bit mask used to selectively enable or disable the dispatching of priority levels.

component. A functional part of an operating system.

condition. One of a set of specified values a data item can assume.

condition indicators. The four bits in a program status vector (PSV) that reflect the result of a previous arithmetic, logical, or I/O operation.

condition values. The values that are assigned to various combinations of the condition indicators and that may be used as mask values in conditional branching operations.

contiguous. Touching or joining at the edge or boundary, adjacent; for example, an unbroken consecutive series of storage locations.

control. The determination of the time and order in which the different parts of a data processing system and the devices that contain those parts perform the input, processing, storage, and output functions.

control block. A storage area used by a computer program to hold control information.

control logic. In the 8100 system, I/O hardware that can decode and perform commands addressed to it by I/O instructions.

counter. A device whose state represents a number and that, on receipt of an appropriate signal, causes the number represented to be increased by unity or by an arbitrary constant; the device is usually capable of bringing the number represented to a specified value, for example, zero.

CR-hi. Channel request high.

CR-lo. Channel request low.

CR-med. Channel request medium.

CRC. Cyclic redundancy check.

CRP. Channel request priority.

current priority level. The number of the active or controlling priority level. Contrast with *last priority level.*

cyclic redundancy check (CRC). A redundancy check in which the check key is generated by a cyclic algorithm.

cylinder. (1) In a disk pack, the set of all tracks with the same nominal distance from the axis about which the disk rotates. (2) The tracks of a disk storage device that can be accessed without repositioning the movable access mechanism.

D

DAT. Dynamic address translation.

data area. A storage area used by a program to hold information.

decrement. To decrease a number by a specified value; in information processing, usually to decrease the value of a counter or register.

device. A mechanical, electrical, or electronic contrivance with a specific purpose.

diagnostic. Pertaining to the detection and isolation of a malfunction or mistake.

disabled. (1)Pertaining to a state of a processing unit that prevents the occurrence of certain types of interruptions. Synonymous with *masked*. (2) Not selectable.

diskette. A thin, flexible magnetic disk and a semirigid protective jacket, in which the disk is permanently enclosed.

diskette drive. A device that rotates diskettes in a diskette storage device. The diskette drive reads and writes double-density information on both sides of an IBM diskette 2D or equivalent, and single-density information on one side of an IBM diskette 1 or equivalent.

diskette 1. See *IBM diskette 1*.

diskette 2D. See *IBM diskette 2D*.

Distributed Processing Control Executive (DPCX). A licensed program designed to control the IBM 8100 Information System. DPCX manages the 8100 system resources (devices, storage, and processing time) in such a way as to provide central control of a distributed processing system and application programming capability.

Distributed Processing Programming Executive (DPPX). A comprehensive collection of program products that make up an operating system for 8100 Information System hardware. DPPX includes the DPPX base and other program products that provide programming languages, application support, and System/370 network access.

Distributed Processing Programming Executive Base (DPPX/Base). A program product that schedules and supervises the execution of programs written for 8100 Information System processing. DPPX base provides I/O control, storage management, data management, execution scheduling, application development tools, and related services.

DPCX. Distributed Processing Control Executive.

DPPX. Distributed Processing Programming Executive.

dual program status vectors. The association of two program status vectors with each priority level, used to facilitate the definition of both an application program and a supervisory program on a single priority level.

dynamic address relocation. The mapping of logical storage addresses to relocated storage addresses.

dynamic address translation (DAT). The mapping of logical storage addresses to real storage addresses.

E

ECC. Error correction code.

EFP. Expanded function operator panel.

EIRV. Error interrupt request vector.

enabled. Pertaining to a state of the processing unit that allows the occurrence of certain types of interruptions.

end of chain (EOC). A signal sent by control logic during a channel I/O operation to indicate that the control is finished with the I/O bus.

EOC. End of chain.

error correction code (ECC). A code that indicates errors when its elements do not conform to specific rules of construction, and that can be used to correct certain of those errors.

error interrupt request vector (EIRV). The formatted information used to indicate an interrupt request generated by the PCE when a system-check condition is detected, and to identify the system-check condition.

execute. To perform an instruction or to run a computer program.

expanded function operator panel (EFP). A panel that permits the user to alter, display, and control various areas of the processor and storage.

F

facility. An operational capability, or the means for providing such a capability.

FCB. Function control block.

feature. A particular part of an IBM product that can be ordered separately by the customer.

FHS. Fixed head select (seek activity).

flag. (1) Any of various types of indicators used for identification; for example, a wordmark. (2) A character that signals the occurrence of some condition, such as the end of a word.

floating-point register. A 64-bit register used for floating-point operation.

floating-point register set. A set of four floating-point registers located consecutively in the floating-point register group.

floating-point status vector (FSV). The formatted information used to allocate floating-point registers, to control exception masking, to control precision, and to hold and indicate floating-point check and program-exception conditions related to floating-point operations.

framing bits. Non-information-carrying bits used to separate characters in a bit stream. Synonymous with *sync bits*.

FSV. Floating-point status vector.

function control block (FCB). In Subsystem Support Services, a control block that contains information such as a function's status, event control block, task I/O queue, and I/O queue.

H

H-bit. One of the four condition indicators.

halfword. A contiguous sequence of bits or characters that comprise half a computer word and can be addressed as a unit.

hardware. Physical equipment used in data processing, as opposed to programs, procedures, rules, and associated documentation. Contrast with *software*.

hex. Hexadecimal.

host computer. The primary or controlling computer in a multiple-computer installation.

I

IBM diskette 1. A flexible diskette that is the medium used to record single-density information on one physical side.

IBM diskette 2D. A flexible diskette that is the medium used to record double-density information on both physical sides.

increment. To increase a number by a specified value; in information processing, usually to increase the value of a counter or register.

index. A list of the contents of a file or of a document, together with keys or references for locating the contents.

inhibited. Pertaining to a state of a processing unit in which certain types of interruptions are not allowed to occur. See also *enabled* and *disabled*.

initial program load (IPL). (1) The initialization procedure that causes an operating system to commence operation. (2) The process by which a configuration image is loaded into storage at the beginning of a workday or after a system malfunction.

initialize. To set counters, switches, addresses, or contents of storage to zero or other starting values-at the beginning of, or at prescribed points in, the operation of a computer routine.

input. Pertaining to the process of transmitting data from peripheral equipment, or external storage, to internal storage, or pertaining to the data or states involved in that process.

input/output (I/O). (1) Pertaining to a device whose parts can be performing an input process and an output process at the same time. (2) Pertaining to either input or output, or both.

input/output interrupt request vector (IOIRV). The formatted information used to indicate an interrupt request generated by an I/O device.

instruction address. The logical address that is used to fetch an instruction.

interface. A shared boundary. An interface might be a hardware component to link two devices or it might be a portion of storage or registers accessed by two or more computer programs.

interrupt request. A request for processing on a particular priority level. It may be generated by the active program, the processing and control element, or an I/O device.

invert. To change a physical or logical state to its opposite.

I/O. Input/output.

I/O mode. The mode of program execution that allows processing of all instructions except those that are supervisor-privileged.

I/O-privileged instruction. An instruction that may be executed in I/O, supervisor, or master mode but not in application mode.

I/O tag. A signal that notifies the system and I/O control logic that a channel I/O operation or programmed I/O operation is beginning.

IOH. Input/output halfword (instruction).

IOIRV. Input/output interrupt request vector.

IPL. Initial program load.

ITA. Interrupt translation array.

K

KDO. Control direct out.

keylock feature. A processor feature that prevents unauthorized system access by means of a three-position, key-operated switch.

L

last priority level. The number of the most recent priority level that was active prior to dispatching the current program status vector. Contrast with *current priority level*.

level. The degree of subordination of an item in a hierarchic arrangement.

load. In programming, to enter data into storage or working registers.

logical address. The storage address that is either supplied to or by a program during the fetching and execution of an instruction or used as a channel pointer during a channel I/O operation. Contrast with *relocated address*.

logical address space. The set of logical addresses numbered sequentially from zero to one less than the address limit. See also *address limit*.

logical storage. The concept of storage space that may be regarded as addressable main storage by an application program in which logical addresses are mapped into real addresses through control blocks.

LSN. Logical sector numbering.

M

main storage. Program-addressable storage from which instructions and other data can be loaded directly.

master mask. A one-bit mask used to suspend the dispatching of a new priority level.

master mode. The mode of program execution that allows processing of all instructions and permits overriding store-protection and execution-protection access control.

MHS. Moving-head seek.

microsecond. One-millionth of a second.

millisecond. One-thousandth of a second.

mode. A method of operation; for example, the binary mode.

ms. Millisecond.

N

NFR. Next function register.

nominal (rated) speed. Maximum speed or data rate of a device or facility which makes no allowance for necessary delaying functions, such as checking data for accuracy.

O

OP. Operator panel.

operand. An entity to which an operation is applied.

operator panel (OP). A display control panel that enables the user to input information, display system status, control powering and IPL, and override normal IPL parameters, and, when the keylock feature is installed, restricts panel access.

operator panel display register. A register whose contents provide the value for the four-character hexadecimal display of the operator panel.

overwrite. To record into an area of storage so as to destroy the data that was previously stored there.

P

parity bit. A binary digit appended to a group of binary digits to make the sum of all the digits either always odd (odd parity) or always even (even parity).

PAV. Program activation vector.

PCE. Processing and control element.

PCE address space. The set of relocated addresses numbered sequentially from zero to the maximum available address.

PCI. Program-controlled interrupt (operation).

PEC. Program exception code.

PIO. Programmed I/O.

PIRV. Programmed interrupt request vector.

pointer. An identifier that indicates the location of an item of data.

primary PSV. One of two program status vectors (PSVs), associated with each priority level, normally used for the definition of a supervisory program.

primary register set. One of two principal register sets assigned to a program for use as general registers. See also *secondary register set.*

primary register set number. The field in a program status vector that designates the number of the primary register set.

primary system control facility (PSCF). System control facility circuitry associated with the processor.

principal register. A 32-bit register used as a general register, as storage for half of a program status vector, or for storage of a channel pointer.

principal register group. All principal registers available to the processor.

principal register set. A set of eight principal registers located consecutively in the principal register group.

priority level. In the 8100 system, a number that designates a relative precedence among interrupt requests so that processing on one level may be temporarily suspended when an interrupt request is generated for a level of higher priority. The numbers range from 0 to 7, 0 being the highest priority level.

processing and control element (PCE). The logical entity that is the controlling center of the system. It contains the sequencing and processing controls for instruction execution, interruption action, dynamic address transformation, and other control or processing functions.

processor. In a computer, a functional unit that interprets and executes functions. See also *processing and control element.*

program activation vector (PAV). The formatted information used to control which of two program status vectors is introduced when a new priority level is made active. See also *dual program status vectors.*

program exception. The condition recognized by the processor resulting from execution of a program, including the improper specification or use of instructions, operands, or control information.

program exception code (PEC). A four-bit code that identifies the cause of a program interruption.

program information code (PIC). A field in a program status vector that either contains the program exception code or indicates that a Call PSV instruction was executed.

program interruption. The suspension of a program's execution as the result of a program exception.

program mode (PM). The field in a program status vector that controls which instructions may be executed by the associated program. See also *application mode, I/O mode, master mode,* and *supervisor mode.*

program status vector (PSV). The formatted information used to control the order in which instructions are executed, to allocate general registers, and to hold and indicate the status of the PCE in relation to a particular program.

programmable storage. Storage that can be addressed by an application programmer.

programmed interrupt request vector (PIRV). The formatted information used to indicate an interrupt request generated by the executing program.

programmed I/O (PIO) address. The information specified as an operand of an I/O instruction that identifies the I/O device to be selected for a programmed I/O (PIO) operation.

programmed I/O (PIO) command. The information specified as an operand of an I/O instruction that directs an I/O device to perform a programmed I/o operation.

programmed I/O (PIO) operation. The transfer of data between the PCE and an I/O device as part of the execution of an I/O instruction. The I/O instruction designates the address of the I/O device, the command to be performed, and the register into or from which the data is transferred.

protocol. In Systems Network Architecture, the meanings of, and the sequencing rules for, requests and responses used for managing the network, transferring data, and synchronizing the states of network components.

PSCF. Primary system control facility.

PSV. Program status vector.

R

real address. The address of a physical main storage location.

redundancy check. A check that depends on extra characters attached to data for the detection of errors. See *cyclic redundancy check*.

register. A storage device having a specified storage capacity such as a bit, a byte, or a computer word, and usually intended for a special purpose.

relocated address. The address in the PCE's address space that is derived during dynamic address relocation by concatenating the high-order bits of the address base with the low-order bits of the logical address. Synonym for *real address* when dynamic address translation is not active.

reset. (1) To cause a counter to take the state corresponding to a specified initial number. Contrast with *set (1)*. (2) To put all or part of a data processing device back into a prescribed state. Contrast with *set (2)*.

RPM. Revolutions per minute.

S

S-S. Start-stop. See start-stop system.

SCF. System control facility.

secondary PSV. One of two program status vectors, associated with each priority level, normally used for the definition of an application program.

secondary register set. One of two principal register sets assigned to a program for use as general registers. See also *primary register set*.

secondary register set number. The field in a program status vector that designates the number of the secondary register set.

secondary system control facility (SSCF). System control facility circuitry associated with an I/O subsystem.

servo. Servomechanism.

servomechanism. (1) An automatic device that uses feedback to govern the physical position of an element. (2) A feedback control system in which at least one of the system signals represents mechanical motion.

set. (1) To cause a counter to take the state corresponding to a specified number. Contrast with *reset (1)*. (2) To put all or part of a data processing device into a specified state. Contrast with *reset (2)*.

SNA. Systems Network Architecture.

software. Programs, procedures, rules, and any associated documentation pertaining to the operation of a computer system. Contrast with *hardware*. See *start-stop system*.

SSCF. Secondary system control facility.

start-stop system. (TC97) A data transmission system in which each character is preceded by a start signal and is followed by a stop signal.

storage capacity. The amount of data that can be contained in a storage device, measured in binary digits, bytes, characters, words, or other units of data.

storage operand address range. A bit in the program status vector that controls the maximum number of bits (32 versus 16) used by the associated program to represent a logical address that is formed using the contents of a general register and that pertains to a storage operand reference.

supervisor mode. The mode of program execution that allows processing of all instructions.

supervisor-privileged instruction. An instruction that may be executed in supervisor or master mode but not in application or I/O mode.

sync. Synchronization. See *sync bits* and *framing bits*.

sync bits. Non-information-carrying bits used to separate characters in a bit stream. Synonymous with *framing bits*.

system control facility (SCF). A system component consisting of one primary system control facility and one or more secondary system control facilities.

Systems Network Architecture (SNA). The description of the logical structure, formats, protocols, and operational sequences for transmitting information units through and controlling the configuration and operation of networks.

U

underrun. Loss of data caused by the inability of a transmitting device or channel to provide data to the communications control logic at a rate fast enough for the attached data link or loop.

unrecoverable error. An error that makes recovery impossible without the use of recovery techniques external to the computer program or run (irrecoverable error).

V

V-bit. One of the four condition indicators.

vector. One or more related fields of information, in a specified format, associated with the control of the processor, channel, or floating-point facility.

verify. To determine whether a transcription of data or other operation has been accomplished accurately.

W

word operand. A 32-bit unit of data referenced as an operand of an instruction. See also *operand*.

Z

Z-bit. One of the four condition indicators.

8

8100 Information System. A collection of processors and devices that can be connected together to form a system for general use. These systems can be used stand-alone, connected to other 8100 Information Systems, or connected to a host processor.

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IBM 8100 Information System
Direct Access Storage Devices
Description

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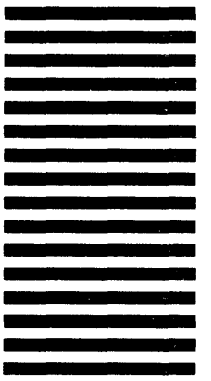

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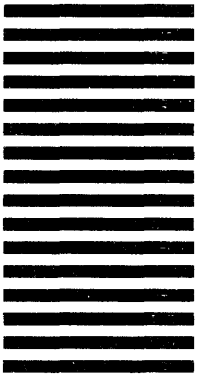

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