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Customer Engineering

Manual of Instruction

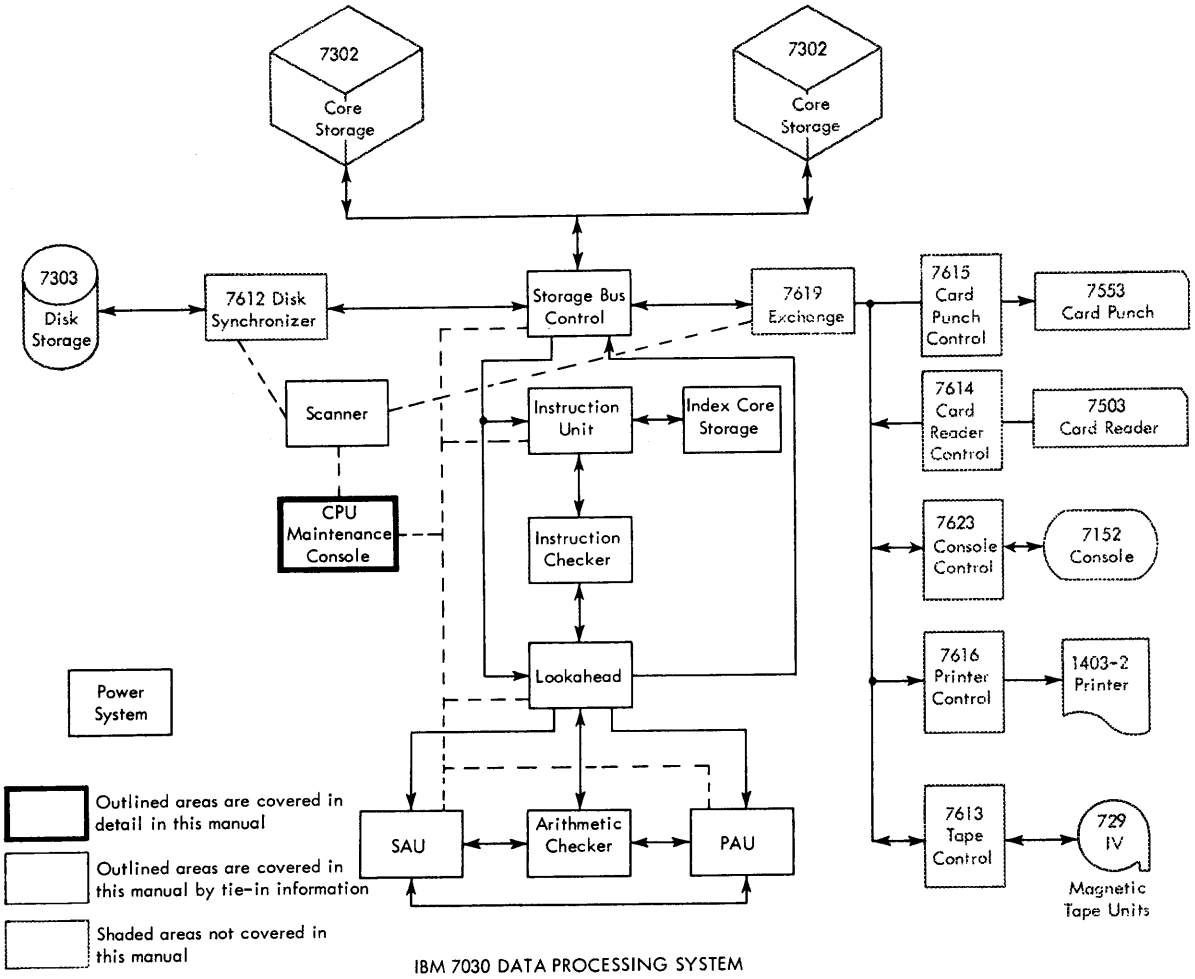
7101 Maintenance Console

PREFACE

This is the Customer Engineering Manual of Instruction on the IBM 7101 Central Processing Unit Maintenance Console for the 7030 System. The material is based on the information available on the commercial 7030 system as of December 15, 1960. Areas of the system are covered as shown in the frontispiece.

The manual contains:

1. Physical description and locations.
2. Theory of operation of switches, keys, and indicator circuits.
3. Description of switches.
4. Description of format rollers.
5. Discussion of power sequencing and marginal checking.
6. Description of error injection system and its use.
7. Reference diagrams on instruction formats, operation codes, powers of two, 7030 check bit organization, and error injection.



IBM 7030 DATA PROCESSING SYSTEM

CONTENTS

1 INTRODUCTION

THE 7101 Central Processing Unit Maintenance Console (Figure 1-1) enables detection of CPU malfunctions in minimum time. It provides visual indications for monitoring control lines and following data flow. Switches and keys on the console allow the operator to simulate automatic operation manually. These operations can be simulated at machine speeds or, in most cases, at a single step rate.

The maintenance console is located at one end of the CPU and contains circuits and components for the following:

1. Indicators and indicator drivers.
2. Manual control switches.
3. Marginal check controls.
4. Power interlocks, protection, and distribution.
5. Voltage monitoring.
6. Indicator scanning.

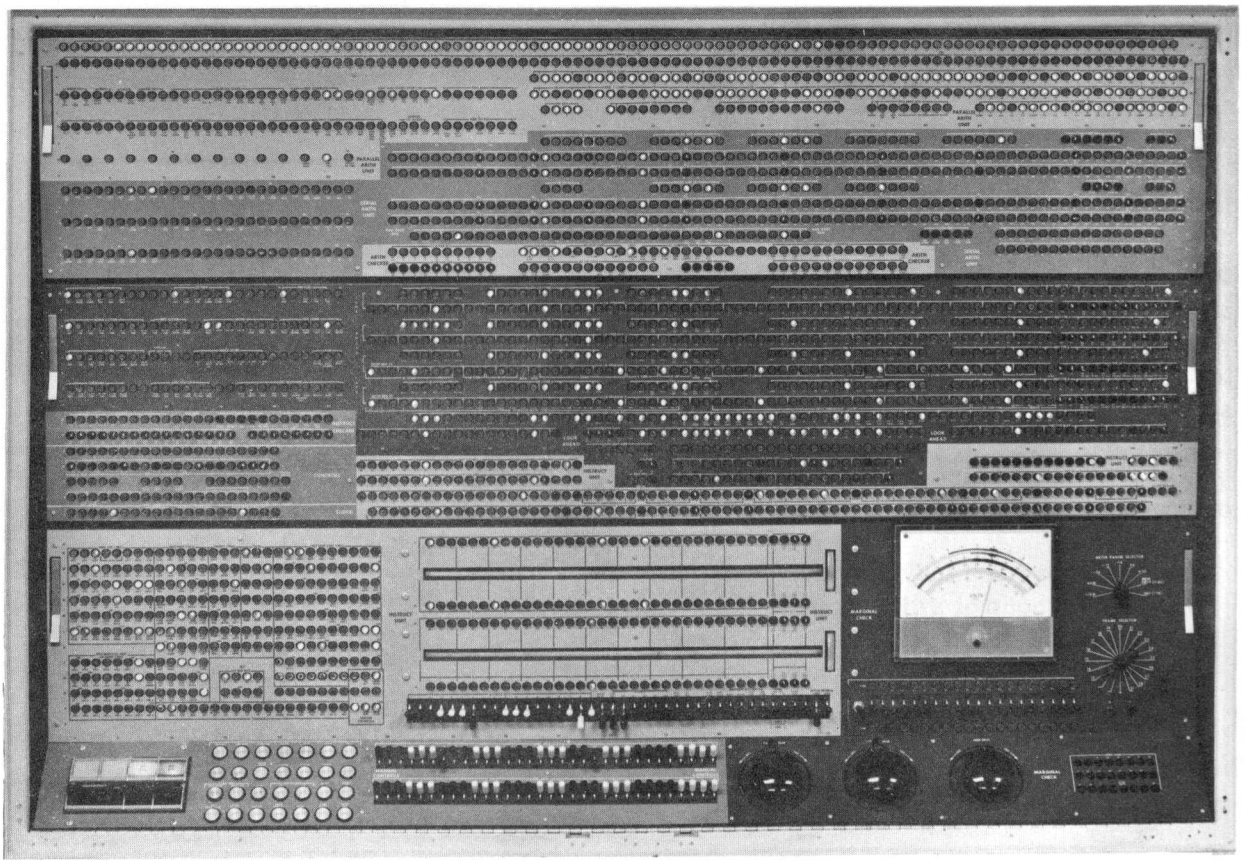


FIGURE 1-1A. 7030 CPU MAINTENANCE CONSOLE PANEL

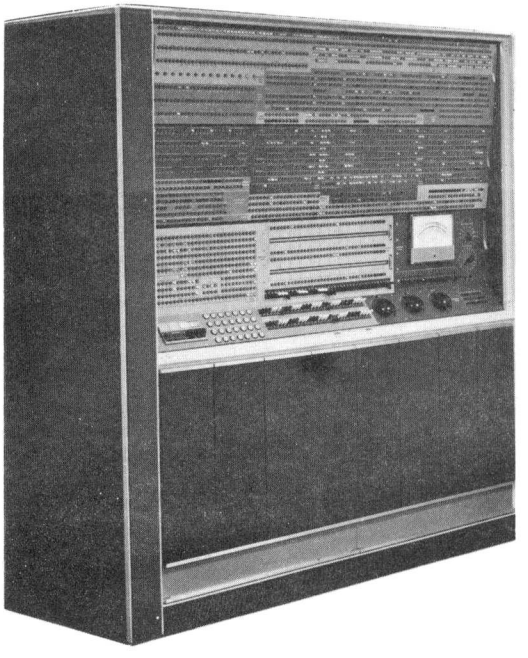


FIGURE 1-1B. 7030 CPU MAINTENANCE CONSOLE

2 PHYSICAL DESCRIPTION

THE CONSOLE FRAME (frame 31) is divided into two sections: upper (A) and lower (B). See Figure 2-1. Panel and gate locations in section A of the console are:

Panel 1: Top indicator panel.
Panel 2: Middle indicator panel.
Panel 3: Lower indicator, switch, and marginal check panel.
Gate 4: Circuit breaker and contactor sliding gate on end of frame.
Gate 5: Not used. Gate 4 takes up space designated for this gate.
Gate 6: Power supply on sliding gate on right end of frame.
Gate 7: Scanner logic gate on right end of frame behind power supply.

Gates in section B are the swinging type and are hinged at the top front. Space is provided for eight gates across the front of the frame. The tailgate, located on the left end of the frame, occupies the space designated for gate 1 (Figure 2-1) but it swings to the side rather than the front; therefore, it is numbered according to the Standard Modular System (SMS) used for the IBM computer frames. Gates in frame 31B are:

Gate 1: Unused. (See gate F following.)
Gate 2-8: Indicator Drivers. Identical except for a slight variation in gates 2 and 3 due to scanner circuit loading.
Gate F: Tailgate. Contains all signal lines to and from the console. (Uses space provided for gate 1.)

The three indicator panels are divided into horizontal rows and vertical columns. Rows are lettered A through Q on panels 1 and 2, and A through S on panel 3; columns are numbered 1 through 104 on panels 1 and 2, and 1 through 70 on panel 3.

2.1 PANEL 1

The following visual indicators are located on panel 1. See Figure 2.1-1.

PAU registers
PAU controls
SAU registers
SAU controls
Arithmetic checker

2.2 PANEL 2

The following visual indicators are located on panel 2. See Figure 2.2-1.

Lookahead registers
Lookahead controls
Instruction unit registers, except registers 1Y and 2Y
I checker
Clock

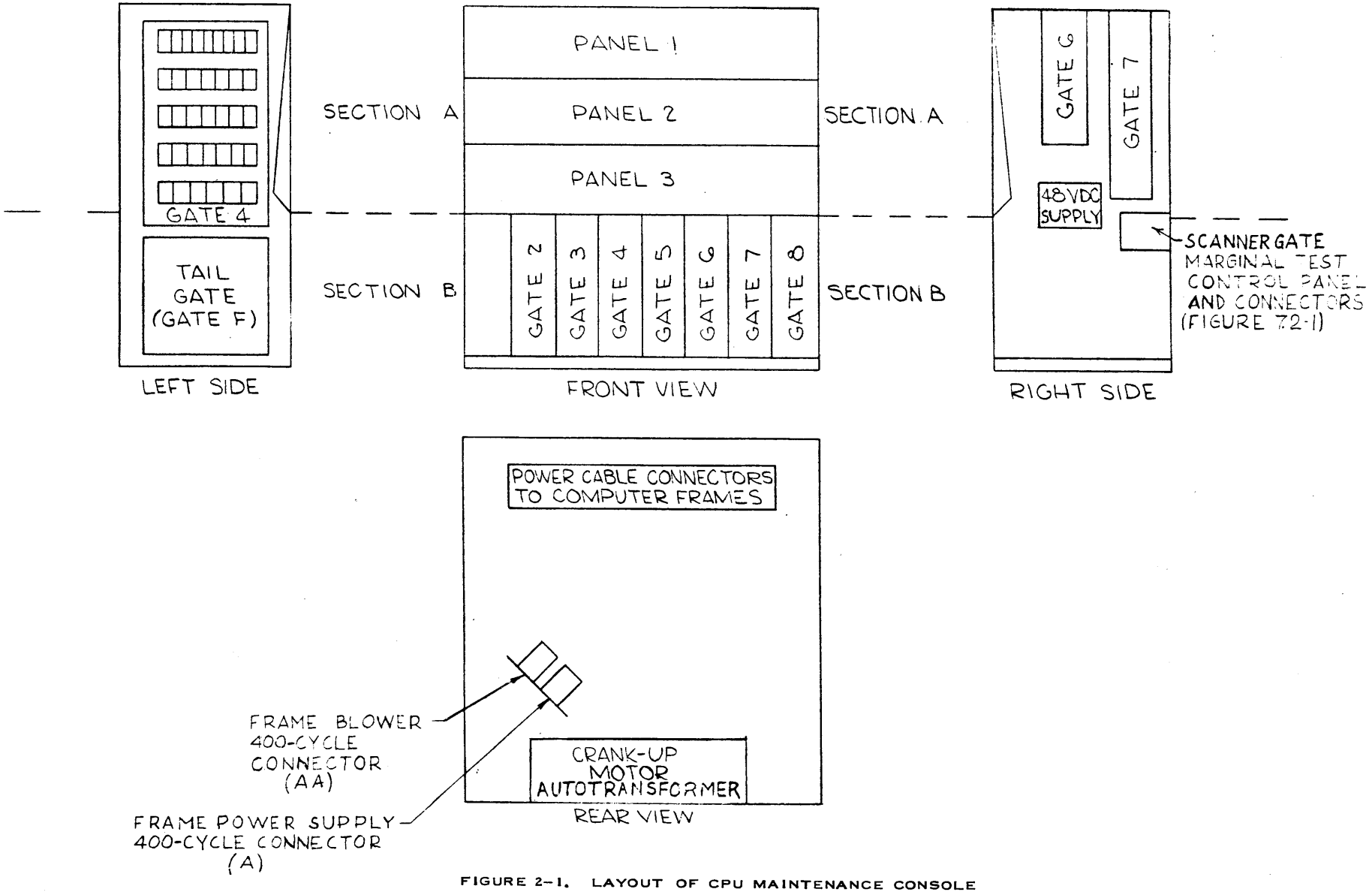


FIGURE 2-1. LAYOUT OF CPU MAINTENANCE CONSOLE

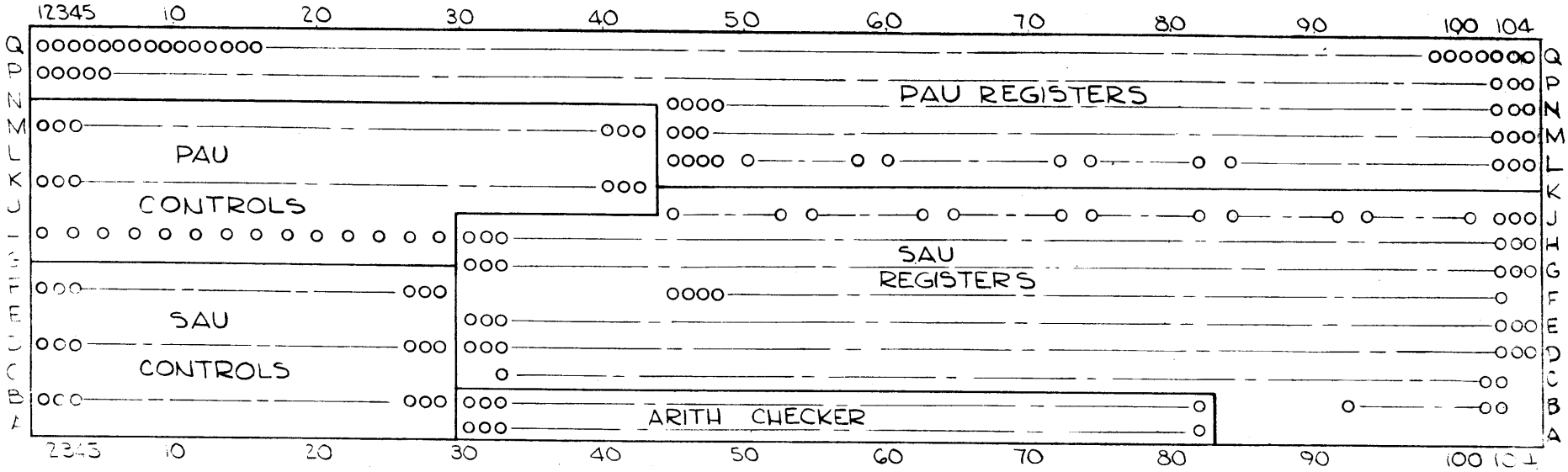


FIGURE 2.1-1. PANEL 1

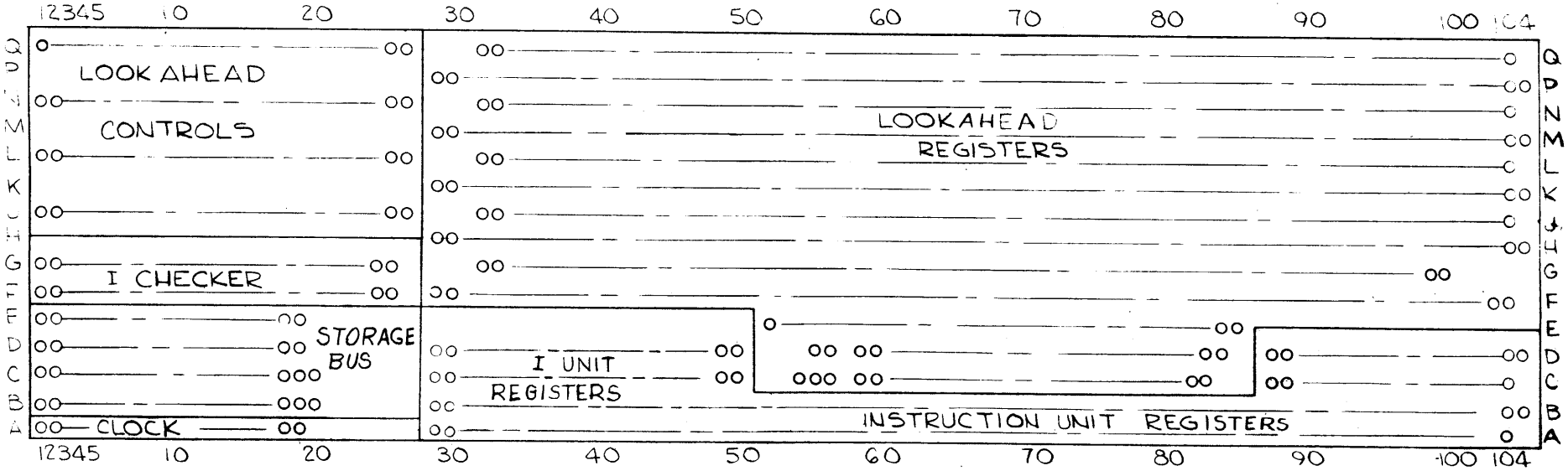


FIGURE 2.2-1. PANEL 2

2.3 PANEL 3

The following visual indicators and switches are located on panel 3 (Figure 2.3-1).

Registers 1Y and 2Y
Format charts
Unit controls for arithmetic modes
Manual controls
Marginal check controls
Voltmeter and voltage selection switches
Blown-fuse lights
Power control switches and lights

2.4 GATE CONTENTS

The scanner gate (31A7) contains 28 card sockets across the panel (columns 1-28), and 10 rows of sockets (rows A-K). The socket pins are designated by A through R according to the standard used throughout the system.

Indicator gates (31B2-31B8) contain 26 columns and 6 rows -- (columns 1-26 and rows A-F). See Figure 2.4-1. Fifty-six ZW__ cards are located on each gate, providing 492 indicator circuits. Input lines to the indicator drivers use edge connectors B01 through B17, C01, C02, D01, D02, E01, E02, F01, and F02. Output lines to the indicators are connected to the back panel pins by slide connectors.

The tailgate (gate F) contains 120 cable connector blocks (mostly open wire connectors) arranged in five columns (A-E), and 24 rows (1-24) (Figure 2.4-2). The coaxial connectors contain 16 pins, and the open wire connectors contain 32 pins. Each block in Figure 2.4-2 shows the source of each cable connected to tailgate F; indicated are the frame number, the tailgate designation and the position of the cable in the tailgate.

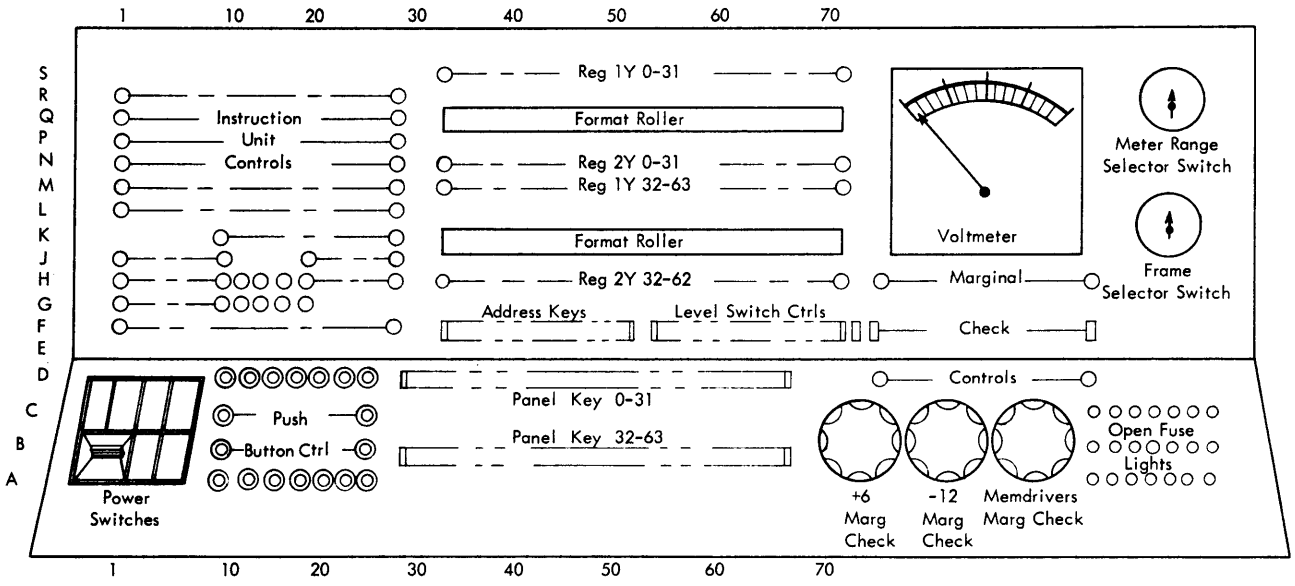


FIGURE 2.3-1. PANEL 3

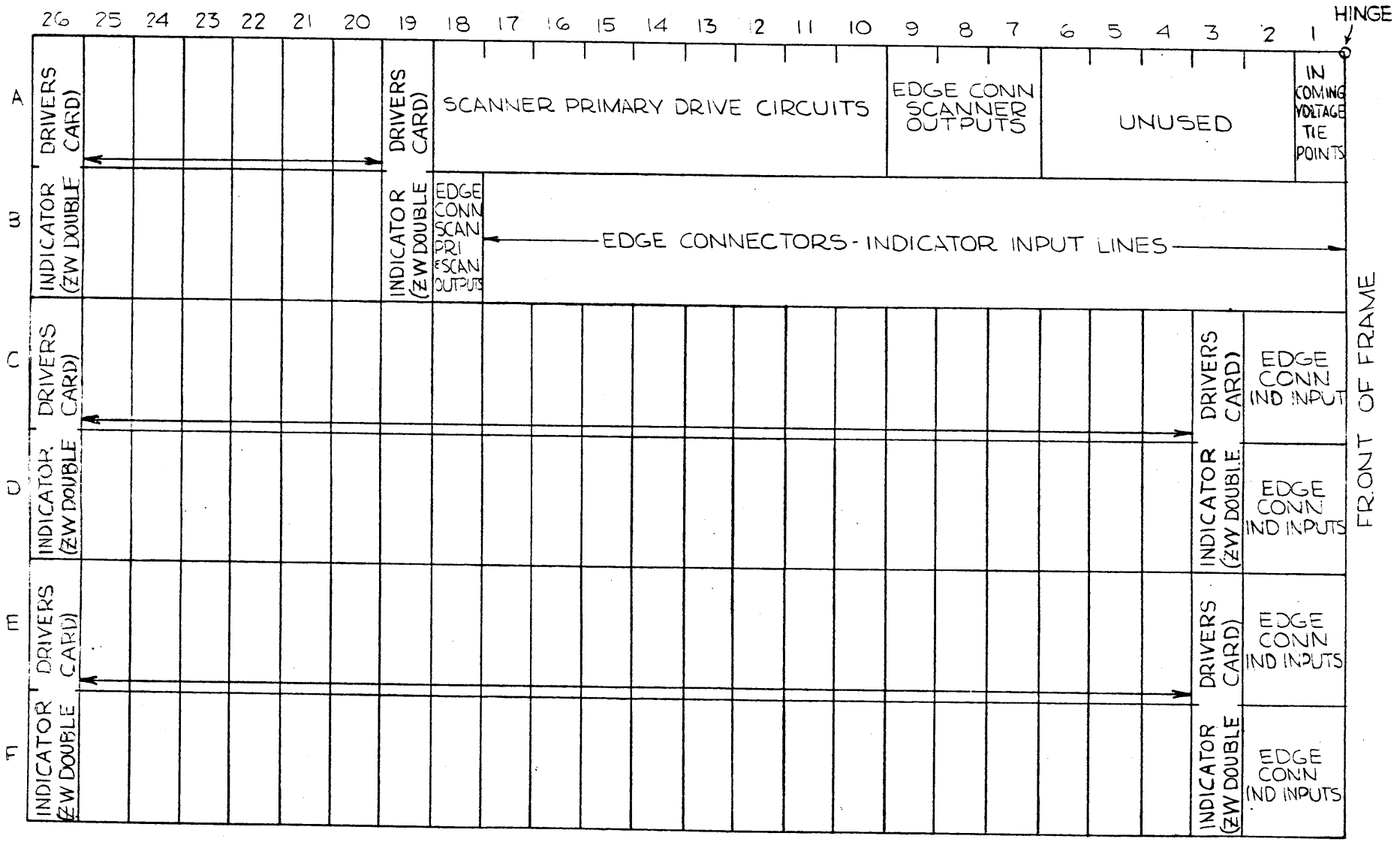


FIGURE 2.4-1. INDICATOR GATE (WIRING SIDE)

	A	B	C	D	E
1	01F	16F	12F	SPARE	SPARE
2	13E	10F	16F	SPARE	SPARE
3	19F	01F	12F	10F	SPARE
4	14E01B	14E01C	14E01D	16E01C	19E02D
5	14E02B	14E02C	14E02D	16E01B	18E01C
6	14F02B	14F02C	14F02D	15E01C	18E01C
7	13E01B	13E01C	13E01D	17E01C	11E01B
8	13F01B	13F01C	13E02B	17E01B	16E01D
9	15E01B	17E01B	16E01D	15E01B	16E01C
10	20E01C	20E02D	13E01D	18E01D	23E02B
11	20E01D	20E02C	19E02C	19E01D	23E02B
12	20E02B	20E01B	19E02B	19E02C	26E02B
13	20E01B	20E01C	19E02B	19E01C	22E02C
14	18E02D	18E01D	19E01C	19E01B	19E01B
15	23E01D	23E01D	24E02B	22E02D	18E03B
16	26E01B	26E01C	26E01B	26E01C	21E01B
17	27E01B	27E01B	27E01C	27E01D	22E02D
18	26E01B	28E01B	28E01C	28E01C	26E01D
19	28E01D	28E01D	22E02C	25E02D	25E02D
20	23E01B	23E01B	24E02C	21E01C	24E01C
21	23E01C	23E01C	21E01B	22E01D	22E01D
22	24E02B	24E01C	25E01C	25E01B	25E01D
23	24E02C	25E02B	25E02C	25E01D	SPARE
24	20E02B	20E02C	11E01B	12E01C	SPARE

FIGURE 2.4-2. CPU MAINTENANCE CONSOLE TAILGATE

3 MAINTENANCE CONSOLE LOGIC

IN ITS OPERATION with the CPU, the console uses only non-logic circuits, such as indicator drivers, lights, and switches. Logic circuits in the console (for rings and for gating) are used only to scan the indicators on the console panels and to gate out the status of these indicators. Switch outputs from the console go directly to the various frames where the terminating resistor cards are located. Indicator driver and scanner primary gating are integrated on a card. Seven drivers and gates are packaged on one double card (ZW__).

Figure 3-1 shows a typical indicator circuit. The load for the trigger output is at the input of the indicator driver. Because the load is at the input of the indicator driver, the indicator driver circuit is not affected by noise on the line. Noise at the trigger end of the line can be great enough to affect the speed of the circuit. Since other outputs from the trigger are used for CPU logic, the bypass capacitor and resistor are placed close to the trigger in the indicator line to suppress noise.

Indicator lamps are rated at 10 volts, 15ma. All indicator lines from the CPU are -P type. A level of -P (-6.6 volts) on the input line causes the transistor to conduct and turn on the lamp. About 15 ma flow through the lamp when the transistor conducts; about 6 ma flow through when the transistor is cut off.

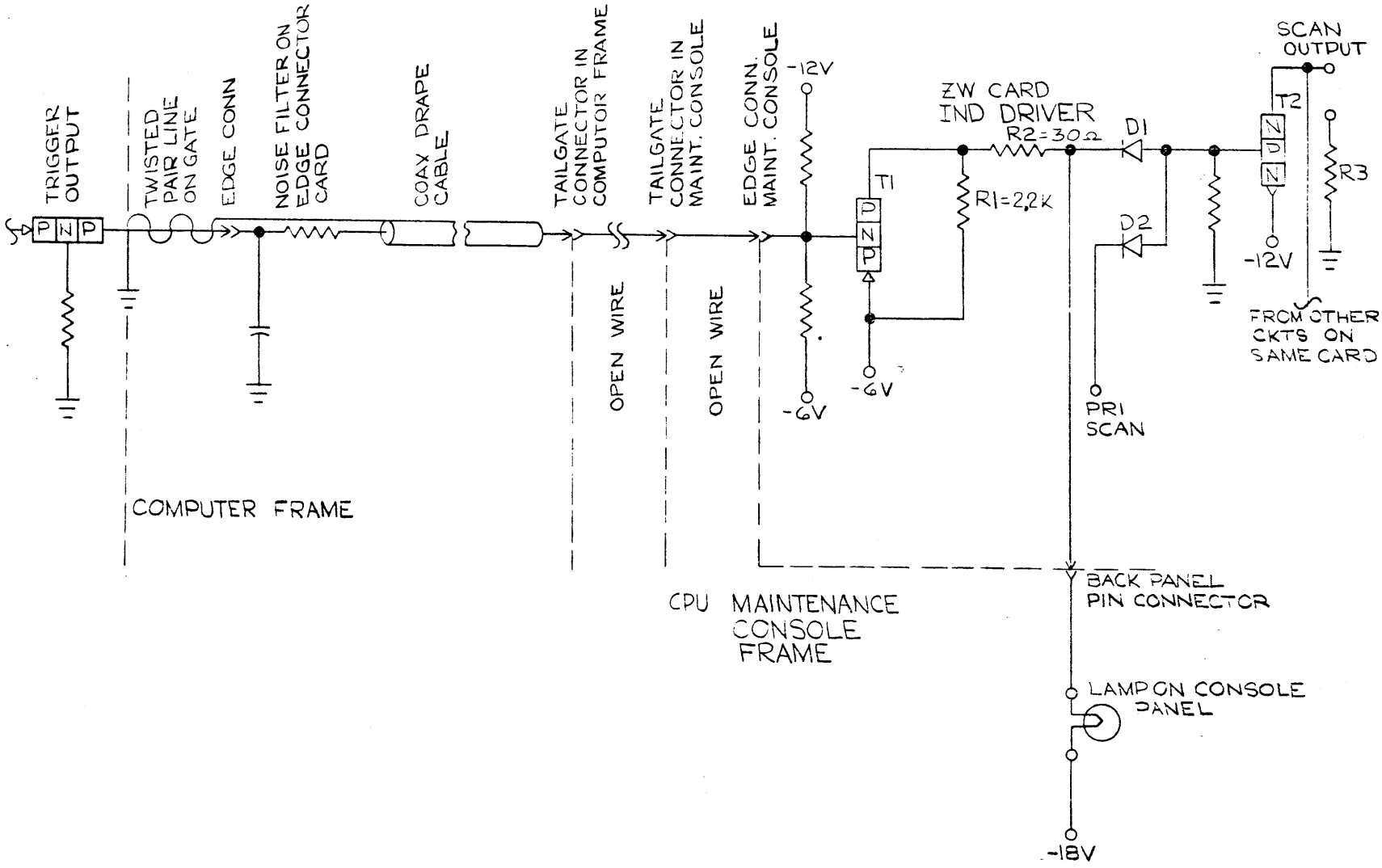


FIGURE 3-1. MINUS P TYPE INDICATOR CIRCUIT

4 MANUAL CONTROLS

THE CPU MAY BE CONTROLLED manually by the switches on console panel 3. Two types of switches are used: a telephone-type to produce a steady state logic level at the output of a resistor network card, and a pulse-type switch to produce a single pulse of short duration that initiates a series of computer operations. See CE Manual of Instruction, 7030 Instruction Unit, Volume I and Volume II, Form R23-9698, and R23-9699, for a more complete discussion, including sequence diagrams of the manual controls. The switches are used for panel keys, address keys, and as controls.

4.1 SWITCH TYPES

Telephone Type. These switches connect +30 volts to the input of a SLUD card (Figure 4.1-1). The output of the resistor network on this card is at a -N level with the switch open, and at a +N level with the switch closed.

Pulse Type. The pulse switch is a microswitch connected to a switching network which consists of a capacitor, resistor, core, and diode (Figure 4.1-2).

When the button is depressed, the first bounce of the contact charges the capacitor. The charging current of the capacitor flips the core, producing a pulse at the output. When the button is released, the capacitor is discharged; the core flips back to its original state, but the diode cuts out the reverse pulse.

The input voltage and component values of the circuit are selected to produce an output pulse of a fixed amplitude and duration when operating into a given impedance. Most of the pulse switches used in this console have the following characteristics:

Volts in: -12 volts
Volts out: 3 volts
Output impedance: 93 ohms
Pulse duration: 0.750 usec
Bias voltage on output: -0.8 volts

The pulse switch operates into a UQUD card (Figure 4.1-2). Effective impedance of the load network on this card is 93 ohms, which allows coaxial cable to be used between the switch and load card. The output of the load network is a -N level (about -0.8 volts). A voltage divider in the network drops the +3 volt pulse of the pulse switch to about 1.5 volts at the output of the UQUD card. This produces a +N level for the duration of the pulse.

Two pulse switches, ring step and ring reset, located on panel 3 at B14 and B16, have different characteristics from those just described, although the principle of operation is the same. The characteristics for these two switches are:

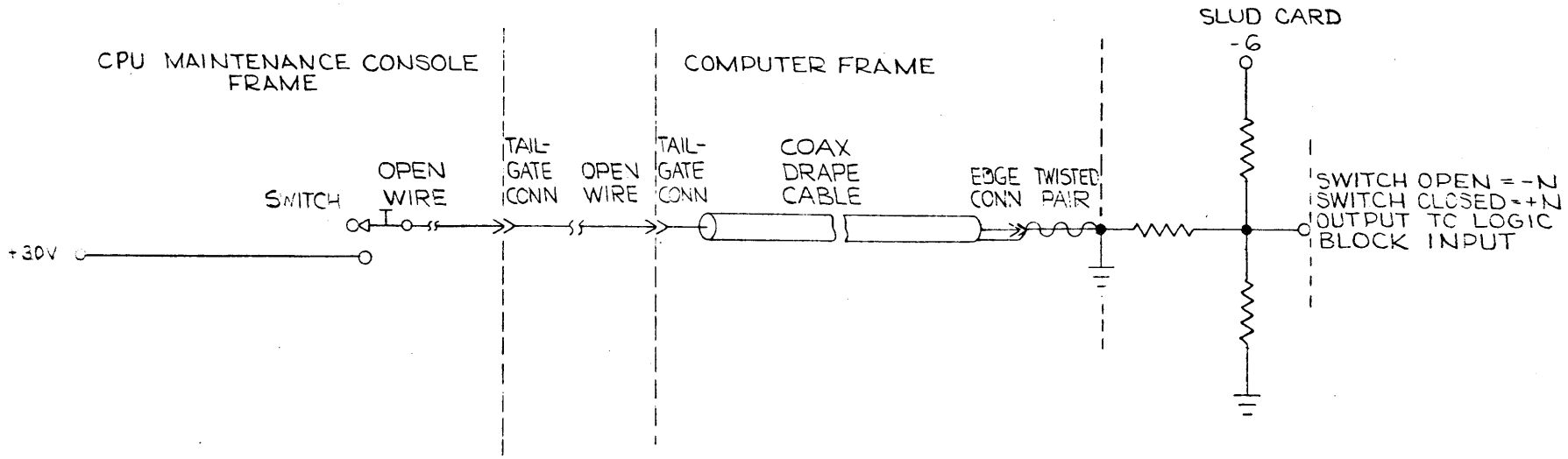


FIGURE 4.1-1. LEVEL SWITCH INPUT TO LOGIC

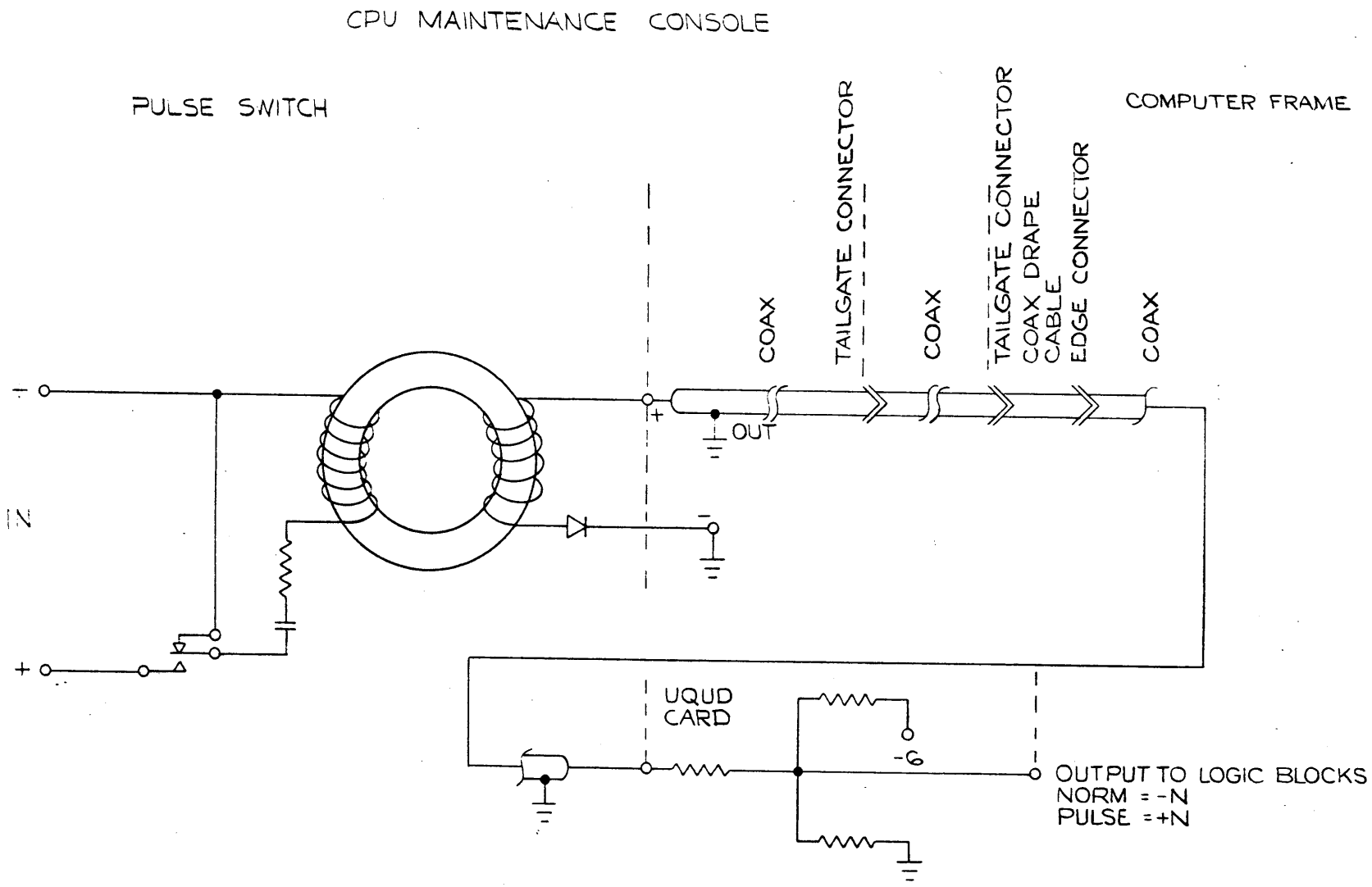


FIGURE 4.1-2. PULSE SWITCH INPUT TO CPU LOGIC

Volts in: -12 volts
Volts out: between -7 1/2 and -14 volts
Output impedance: 470 ohms
Pulse duration: between 2.5 and 5 usec
Bias voltage on output: +6 volts

Figure 4.1-3 shows how these two switches operate directly into the T level input of the CTDL (complementary transistor diode logic) block. The normal level for this circuit is +6 volts, and the shift is to about -6 volts for the duration of the pulse.

4.2 PANEL KEYS (D29-D60 and B29-B60)

The panel keys consist of 64 telephone-type switches wired as shown in Figure 4.2-1. Numbers following switch names show the locations of these switches on panel 3. The principle of operation is the same as described in Section 4.1. These switches indicate a zero when in the normal (straight out) position and a one when in the down position. The panel key set-up switches (F65 and F66) override panel switches in the zero position. See descriptions of panel key set-up 01 and 10 in Section 4.4.1.

Panel switches are used as the data input when storing into core storage, as an instruction source for enter instruction operations, and as a data source for storage address 4 when in the test mode. Various uses of these switches are discussed in Section 4. Outputs of the panel switches are gated to the storage out-bus by AND circuits located in a storage bus frame.

4.3 ADDRESS KEYS (F31-F48)

The address switches consist of 18 telephone-type switches used to enter the address into the CPU during manual display and store operations. The outputs of these switches are gated into register W by AND circuits located in the instruction unit frame. A zero is indicated by the normal position of the switch, and a one by the down position. The output from the SLUD card is +N for zero and -N for one (Figure 4.3-1). This reverse logic is accomplished by using the normally closed contacts of the switch instead of the normally open contacts.

4.4 CONTROL SWITCHES

4.4.1 Level Switches (F49-F68)

Level switches are telephone-type switches that place a DC level on a control line in the CPU.

Maintenance Mode (F49). When depressed, this switch supplies voltage to the pulse switches on the CPU maintenance console. It also enables the panel key gating controls in the storage bus control for manual operations, the program controlled references to storage address 04, and the error injection circuits. This switch disables the boundary compare circuits. Thus, when the system is not in the maintenance mode (switch in the normal position), the boundary compare circuits are operative but the pulse switches, panel key gating, and error injection circuits are inoperative.

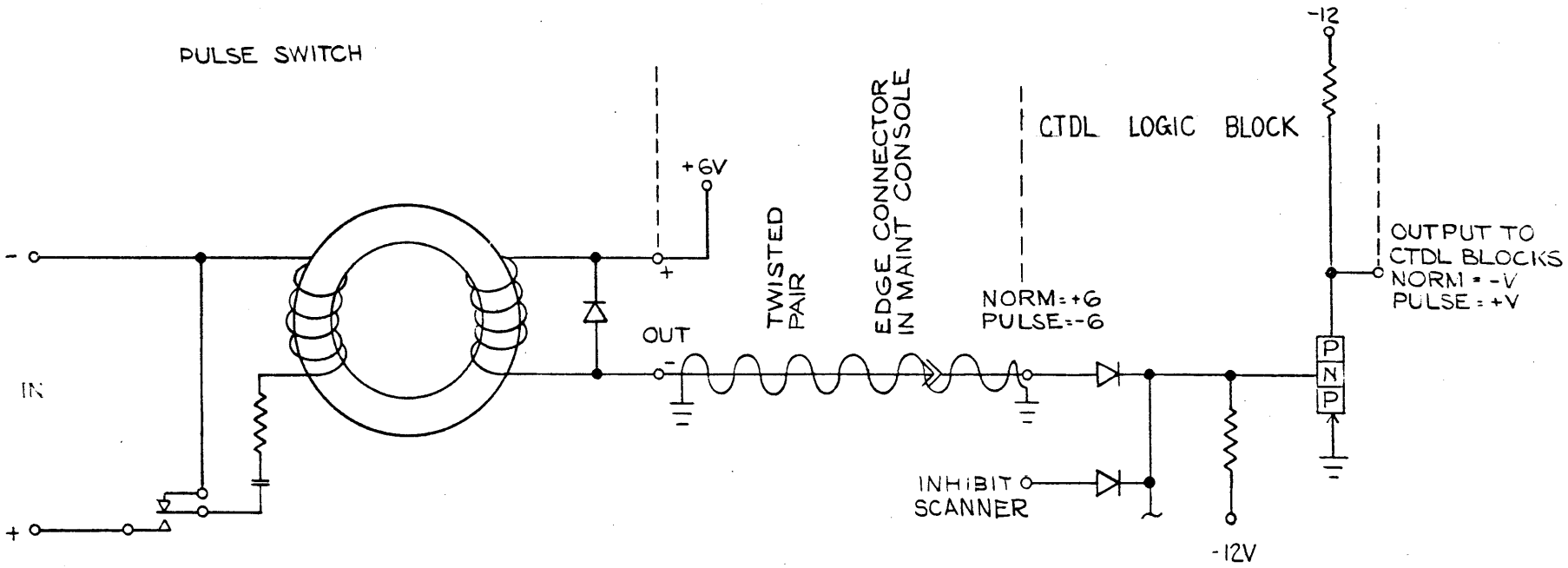


FIGURE 4. 1-3. PULSE SWITCH INPUT TO SCANNER LOGIC

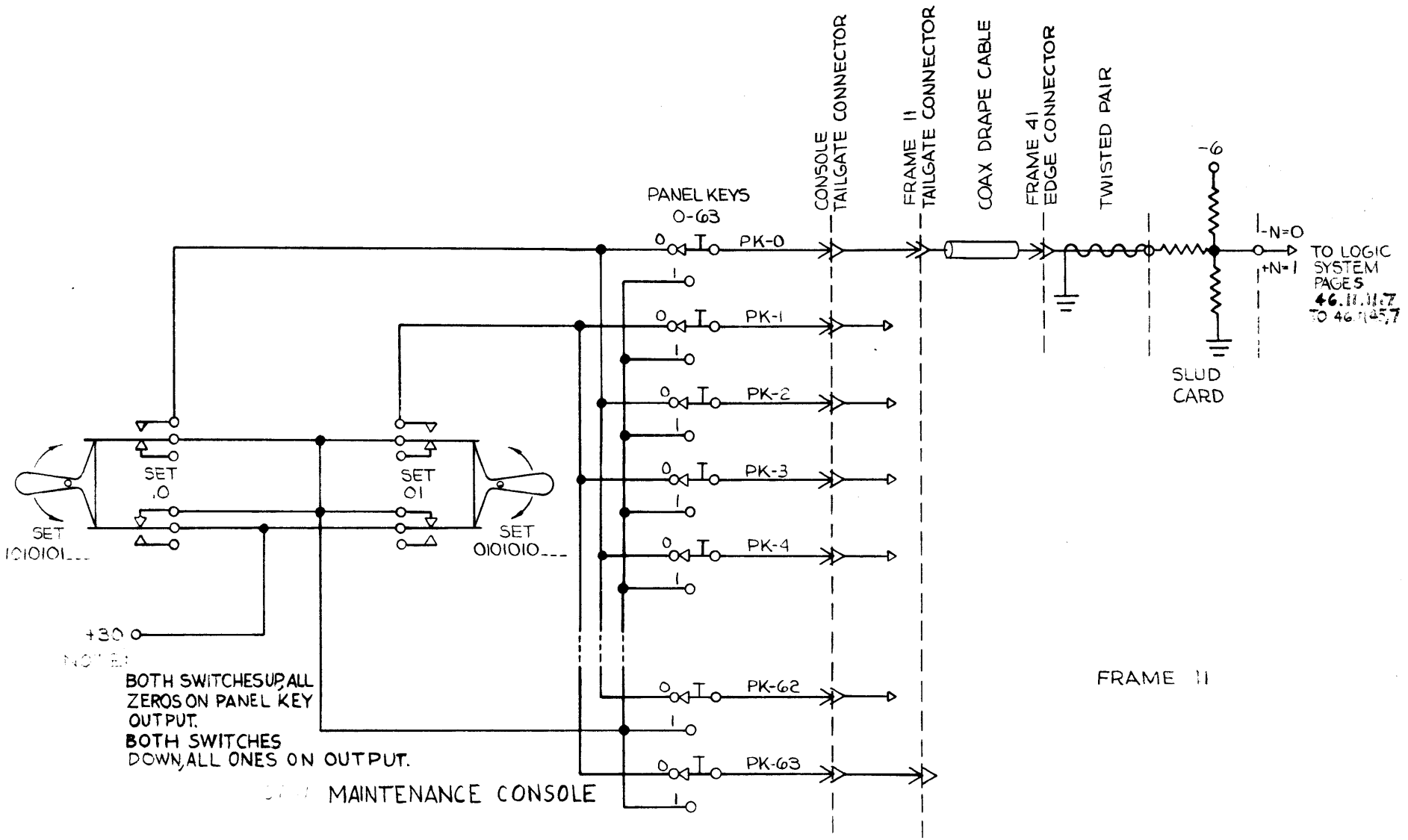


FIGURE 4.2-1. PANEL KEYS AND PATTERN SWITCHES

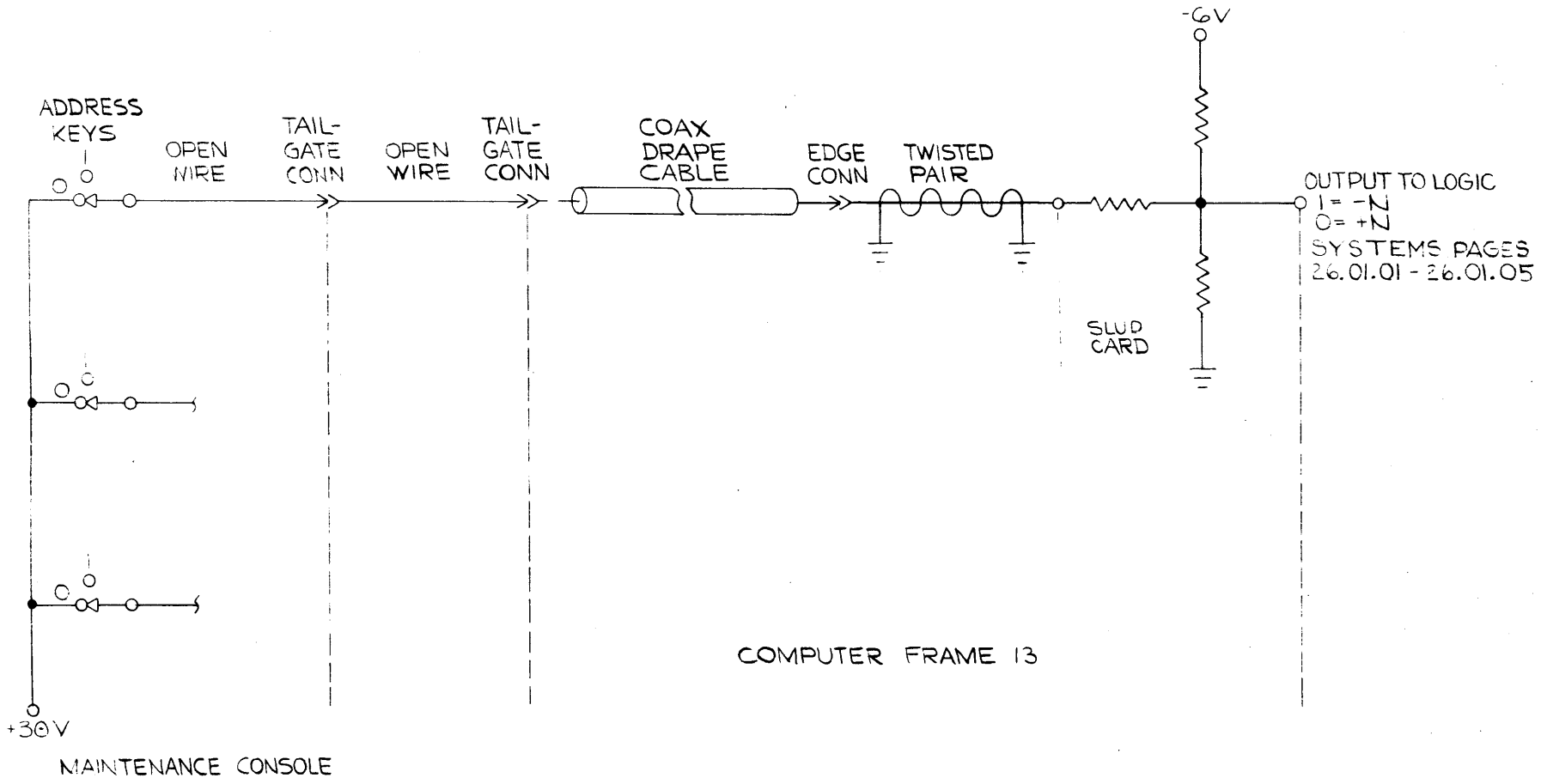


FIGURE 4.3-1. ADDRESS KEYS

Disable Time Clock Advance (F50). This switch suppresses time clock advance when in the down position.

Disable Interrupt (F51). This switch prevents all interrupts that normally result from action of the indicator register, including those from forced enable in execute instructions.

Disable Lookahead 1, 2, 3, and 4 (F52-F55). Each of these switches suppresses the operation of its respective level of lookahead.

Repeat Instruction (F56). This switch sets up a mode that enables the CPU to gate the contents of the panel keys into registers 1Y and 2Y alternately; it does not initiate any operation. With this switch down, depressing of the program start key causes the CPU to continually execute the contents of the panel keys instead of instructions from storage; depressing of single operation executes the instruction in the panel keys. One full-word or two half-word instructions may be used for this operation. Also, the left-half of a full-word instruction may be placed in panel keys 32-63 and the right half in panel keys 0-31 to simulate a word boundary cross-over instruction. If a branch instruction is attempted in the repeat instruction mode, the branch address should be between 64 and 2047; this will allow continuous panel key fetching.

Time Clock Test (F57). This switch allows the time clock to run as in normal operation while the CPU is stopped.

Multiple Operation (F58). This switch has the same effect as repeated depressions of the single operation switch. Single operations are repeated continually whenever this switch is in the down position and terminated when it is restored to the normal (up) position.

Inhibit Scan (F59). Depressing this switch prevents a scan of the CPU indicators when an error is detected. The system continues normal operation.

Error Stop (F60). When this switch is down, the computer stops if an error is detected. To continue operation, the error triggers must be reset and the clock started. Depress error trigger reset and start clock buttons. If the inhibit scan switch is normal, the scan operation is made before the CPU is stopped.

Operation of the inhibit scan and error stop switches is as follows:

Inhibit Scan	Error Stops	Action
ON	OFF	A detected error will have no effect on the clock.
ON	ON	A detected error will stop the clock. No scan will occur.
OFF	OFF	An error will stop the clock. A scan will occur and the clock will be restarted automatically after the error triggers are reset.
OFF	ON	An error will stop the clock. A scan will occur, but the clock will not restart. If it is desired to restart the clock, it must be done manually after manually resetting the error triggers.

Index Storage Test Read (F61). This switch sets up a condition that allows successive read cycles from the index storage. The information read out is checked by the I checker, and an error trigger is turned on when an error is detected. The test operation is initiated by the start index storage test key and is conditioned by maintenance mode.

Index Storage Test Write (F62). This switch sets up conditions that allow successive read and write cycles from index storage. Information that is read is checked for error. The test operation is initiated by the start index storage test switch and is conditioned by maintenance mode.

Index Storage Test Address Advance (F63). This switch causes the index storage address to be advanced by one during each cycle of the index storage test.

Index Storage Test Error Stop (F64). This switch terminates the index storage test operation when an error is detected. The test continues when the error trigger is reset and the start index storage test switch is depressed.

Panel Key Set-up 10 (F65). This switch causes alternate ones and zeros to appear on the output lines of the panel keys. Thus, starting with the panel key zero, the information is 1010....etc. This switch is effective only on the panel keys in the zero position.

Panel Key Set-up 01 (F66). This switch causes alternate zeros and ones to appear on the output lines of the panel keys. Thus, starting with the panel key zero, the information is 0101....etc. This switch is effective only on panel keys which are in the zero position. If both panel key set-up 01 and panel key set-up 10 switches are down, all ones appear on the output lines regardless of the information contained in the panel keys. If both switches are up, all zeros appear on the output lines regardless of the information contained in the panel keys. See Figure 4.2-1.

Both switches (01 and 10) have three set positions --up, down, normal. The following table shows the effect of the two switches:

Switch 01	Switch 10	Action
up	up	Zeros are read from all positions.
up	normal	No effect.
up	down	An OR of the panel keys and a 1010 pattern.
normal	up	No effect.
normal	normal	No effect.
normal	down	An OR of the panel keys and a 1010 pattern.
down	up	An OR of the panel keys and a 0101 pattern.
down	normal	An OR of the panel keys and a 0101 pattern.
down	down	Ones are read from all positions.

Scan Test (F67). This switch enables manual stepping and resetting of the arithmetic scanner circuitry when in maintenance mode. Specifically, it enables ring reset (B14) and ring step (B16).

Pulsed Mode - Computer Reset (F69). When this switch is turned on, it provides a computer reset approximately every millisecond. After the reset, the clock is started, an enter instruction operation is performed, and a program start is initiated.

Pulsed Mode - Master Reset (F70). This switch is used only in conjunction with the pulsed mode, computer reset switch. When both switches are on, a master reset occurs approximately every millisecond. After the reset, the clock is started, an enter instruction operation is performed, and a program start is initiated.

4.4.2 Pulse Switches

Pulse switches are used to eliminate the hazard of contact bounce on control lines that initiate high-speed operations. A list of all pulse switches on the CPU maintenance console follows.

Master Reset (D14). This switch provides a control reset and an error reset to all units of the CPU and to the storage bus.

Error Trigger Reset (D16). This switch provides an error reset to the bus error latches and the local error triggers throughout the CPU.

Computer Reset (D18). This switch provides a reset to the CPU and the lookahead request trigger in the storage bus. During this reset, clock pulses are not distributed to the CPU.

Start Clock (D20). This switch allows controlled clock pulses to be distributed to the CPU.

Stop Clock (D22). This switch stops distribution of the controlled clock pulses.

Program Start (D24). This switch allows the CPU to resume high-speed operation, by resetting the program halt trigger.

Program Halt (D26). This switch turns on the program halt trigger that suppresses lookahead loading, allowing the instruction unit to fill up and wait for lookahead. Normally, it is depressed in order to stop the program in arithmetic mode and allow manual intervention. Upon entry into arithmetic mode, the first arithmetic instruction will be executed, after which the CPU will stop in arithmetic mode in the normal program halt status.

AXXB Mode (C18). When the CPU clock is stopped, depressing this switch causes controlled pulses to be distributed at one-third their normal frequency. This mode is terminated upon depression of clock stop.

1 Pulse (C20). This switch produces a single controlled clock pulse either A or B, depending upon the status of the clock. The clock must be stopped before this control is effective.

2 Pulse (C22). This switch produces two controlled clock pulses, either A-B or B-A, depending upon the status of the clock. The clock must be stopped before this control is effective.

3 Pulse (C24). This switch produces three controlled clock pulses, either A-B-A or B-A-B, depending upon the status of the clock. The clock must be stopped for this control to be effective.

Ring Reset (B14). When the system is in the maintenance mode, and if scan test (F67) is enabled, this switch resets the scanner rings. (Further discussed in the CE Manual of Instruction, 7030 Scanner, Form R23-9711.)

Ring Step (B16). When the system is in the maintenance mode, and if scan test (F67) is enabled, this switch causes single-stepping of the scanner rings.

Scan (B18). This switch initiates a scan operation. To scan the CPU maintenance console indicators, first depress stop clock.

Error Injection On (B20). This switch turns on bit 58 in the upper-boundary register and enables error injection during test mode operations. (Refer to Section 8.)

Error Injection Off (B22). This switch turns off bit 58 in the upper-boundary register and disables error injection.

Single Operation (B26). Each depression of this switch allows one instruction to be executed. This is accomplished by allowing only one level of lookahead to be filled as a result of switch operation. Thus, the instruction unit remains full and the arithmetic units execute each instruction as it is loaded into lookahead from the instruction unit.

To step through an instruction and stop at its completion, the clock must first be stopped. The single operation button is then depressed, followed by depressions of 1-pulse, 2-pulse, or 3-pulse, as desired. At the completion of the instruction further pulsing has no effect.

To step through an instruction and continue pulsing into the program, program start is depressed after the clock is stopped. Now, the 1-pulse, 2-pulse and 3-pulse buttons are effective indefinitely. At any time upon depression of start clock, high-speed operation is resumed.

Initial Program Load (A14). The initial program load switches on the IBM 7152 Operator's Console, the exchange maintenance console, and the CPU maintenance console all produce the same results, as follows:

1. Execution of any program by the CPU is interrupted by terminating the instruction in execution at the time the switch is depressed. All storage locations and registers which were altered prior to the termination are not restored to a former or predetermined state.

2. The interruption system is temporarily disabled.

3. All input-output operations on the exchange are terminated.

4. All control words in the exchange are reset to zero.

5. The exchange is set to interpret the next channel signal in a special way.

6. The contents of the instruction counter buffer are transferred to the instruction counter register if the depression of IPC occurs in arithmetic mode.

Start Index Storage Test (A16). When the CPU is stopped, this switch initiates a series of index storage read or read-and-write cycles. The type of test performed is determined by the condition of the level switches associated with the index storage test (F61-F64). The test cycles are terminated by turning off the level switch at F61 or F62 or by a stop-on-error condition.

Display (A18). When the address keys (F31-F48) contain an external core storage address, this key causes the address to be taken to the storage bus addressing controls via register W and the instruction counter adder. In arithmetic mode, when the contents of the desired core storage address appear on the storage-out bus, the address is gated into register 1Y, through the I checker, and into register X. The previous contents of register X have entered register 2Y. Thus, register 1Y contains the original word from core storage with its ECC bits, while register X contains the corrected word (in the case of a single error) with the instruction unit parity. Index storage words are displayed in a similar manner, but internal storage addresses are not displayed since they have individual indicators on the console panel.

Consecutive Display (A20). In arithmetic mode, the action for consecutive display is the same as that for display, with two exceptions: (1) the address keys are not gated to register W; (instead, the contents of register W is increased by 1 and gated to the storage bus addressing controls or the index address bus), and (2) the contents of register X is gated into register 2Y before the new word is received.

If the display switch is depressed and then the consecutive display switch depressed, the contents of the storage address set in the address switches are displayed in register 2Y with instruction unit parity. The contents of the next sequential storage address are displayed in register 1Y with ECC bits and in register X with instruction unit parity.

Store (A22). The contents of the address switches are used as in the display operation to select the address at which the word will be stored. The contents of the panel switches (D29-D60 and B29-B60) are gated to the storage-out bus, into register 1Y, through the I checker, and into register X with instruction unit parity.

If the desired address where the word to be stored is in index storage, the contents of register X are sent to index storage. If the desired address is in external core storage, the contents of register X are gated through the I checker to a level of lookahead with ECC bits. From the lookahead level, the word is gated to the storage-in bus and stored in a normal manner. If the desired address is in internal storage, data flow is the same as for external storage, except that the word is gated from the lookahead level to the transfer-out bus and, with VFL parity, into the desired register.

Consecutive Store (A24). This operation is the same as store except that the address at which the word is stored is obtained by increasing the contents of register W and by 1.

Enter Instruction (A26). The contents of the panel switches are set into register 1Y with instruction unit parity. No other action is produced by this switch. The instruction may be executed by depressing the single operation start switch. One full-word or two half-word instructions may be entered with one depression of the switch. The left half of register 1Y is operated upon first.

If stepping through the instruction is desired, the clock must be stopped before depressing the single operation switch. The sequence of control operations should be:

1. Stop clock (D22).
2. Set instruction into panel switches (D29-D60 and B29-B60).
3. Enter instruction (A26).
4. Single operation (B26).
5. 1 pulse (C20), 2 pulse (C22), or 3 pulse (C24).

Repeated depressions of the desired switch will step through the instruction.

Multi-Op Key

When the Multi-Op key on the CPU maintenance console is held down, it causes instructions to single step at a rate of 10 instructions per second.

5 FORMAT ROLLERS

TWO FORMAT ROLLERS mounted behind horizontal slots in panel 3 show the bit format for each instruction displayed in registers 1Y and 2Y. See Figure 5-1. Information displayed in either register is compared with the instruction formats on the rollers to determine the exact operation in process. The formats also provide the bit configuration needed to manually key an instruction into a register so that the format of the instruction can be observed in the register. The arithmetic formats are repeated on both rollers.

One roller is located between the left (top) halves of register 1Y and 2Y; the other is located between the right (lower) halves of these registers. See Figure 2.3-1. These two rollers are located so that a display in any portion of the registers can be readily compared with the nearest roller. Instruction information displayed in either half of either register may be the left-half or right-half of a full word instruction or a half-word instruction.

Bit positions 24 through 27 of the information displayed in any half of a register are the key positions in determining the exact instruction. If the bit configuration displayed in these four positions is 1000 (the indicator in position 24 on and the other three indicators off) the information displayed is the left-half of a full-word instruction (Figure 5.2), and the display of the right-half of the instruction can be compared against the formats on the roller to determine the exact operation.

Color coding is used on the charts to assist in locating the type of instruction. The color in the block to the right of the format of the instruction indicates the portion or type of instruction preceding the colored block. Refer to Figure 5-1 for this coding.

If the bit configuration in positions 24 through 27 displayed in a register is not 1000, then the information displayed is either a half-word instruction, the right-half of a full-word instruction, or data that is not an instruction. See Figure 5-2. The exact type of operation (if it is an instruction) can be determined by comparing the displayed information with the format roller.

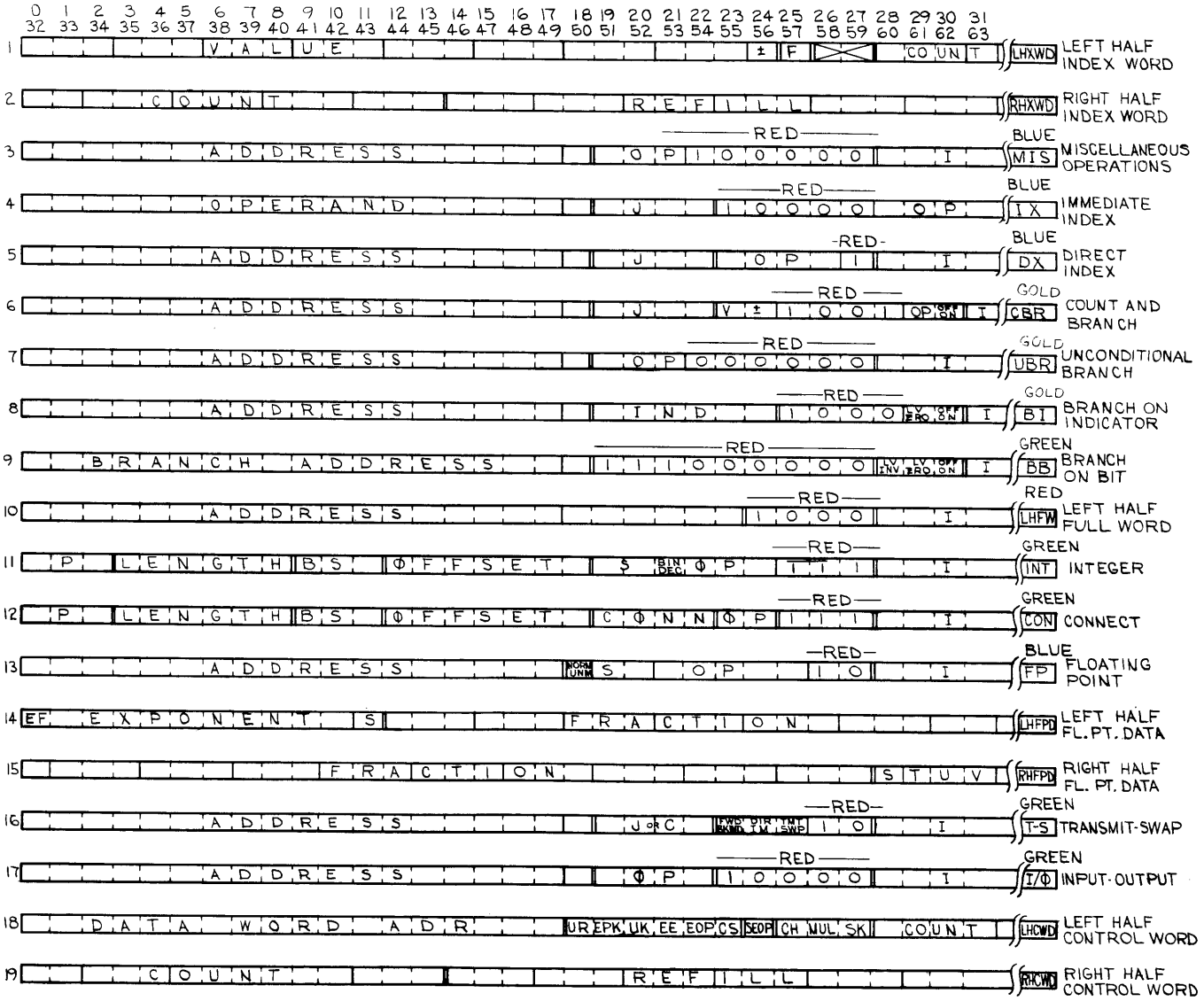


FIGURE 5-1. TYPICAL FORMAT ROLLER

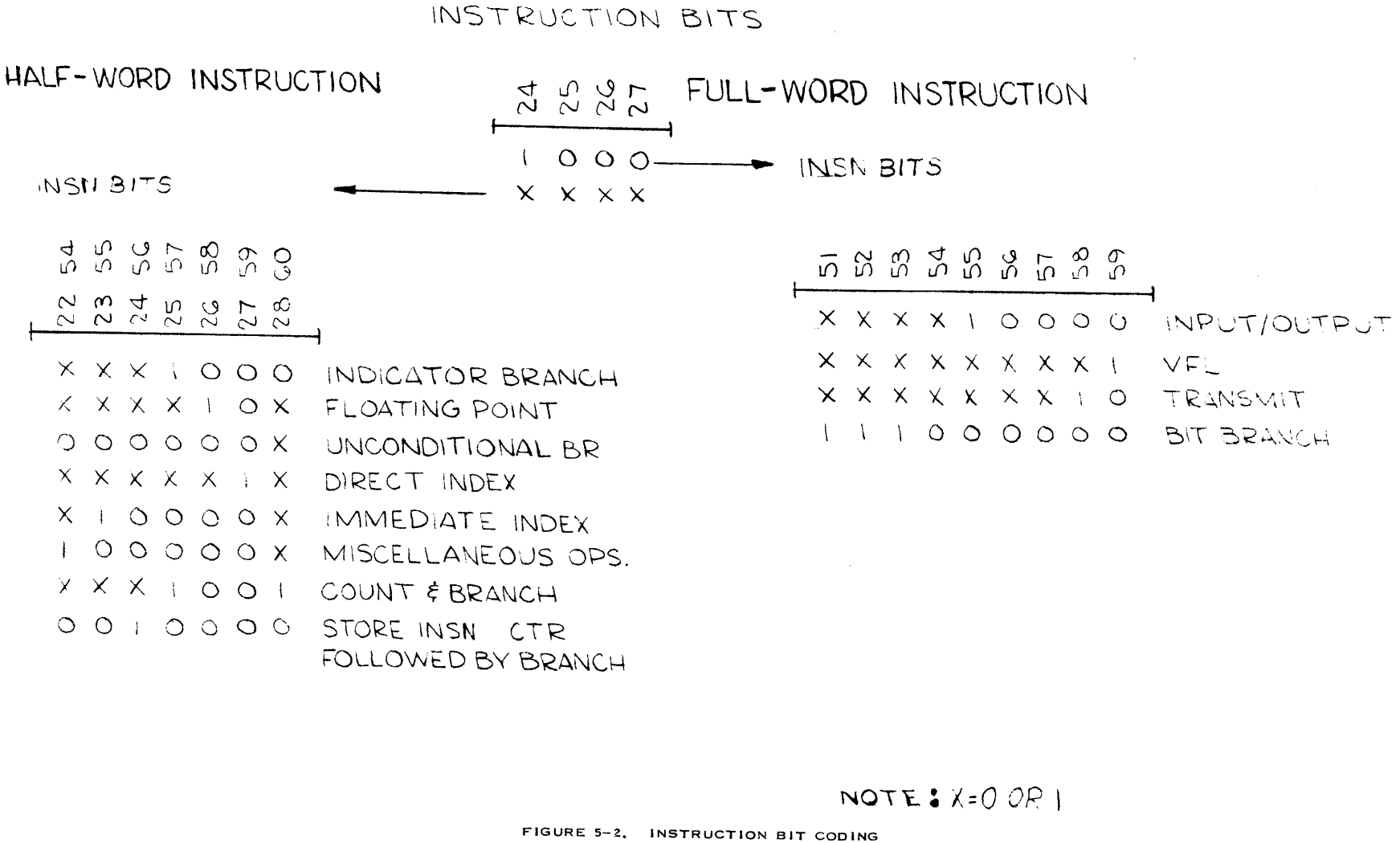


FIGURE 5-2. INSTRUCTION BIT CODING

6 COMPUTER SCANNER

THE SCANNER CIRCUITS in the CPU maintenance console operates under control of, and as part of the scanner control unit located in the exchange. The CPU maintenance console circuits consists of primary and secondary rings, and enough driving, gating, and control circuits to reduce the total indicator output to a series of 8-bit bytes which are sent to the exchange.

7 POWER CIRCUITS

THE CPU MAINTENANCE CONSOLE contains the controls, circuit breakers, contactors, and necessary equipment to supply 208 volt, 3 phase, 400 cycle ac power to all CPU frames for blowers and dc power supplies. The console also has facilities for power circuit protection of the CPU interlocking and sequencing power controls, and marginal checking.

7.1 POWER SEQUENCE AND CRANK-UP

The 208 volt, 400 cycle power is supplied to the maintenance console from the power distribution frame (PDF) by two separate cables. One cable is for the CPU blowers, and the other is for the dc power supplies in the maintenance console and all CPU frames. Figure 7.1-1 shows how power is distributed to the frames.

The ac-on switch on the maintenance console energizes contactors in the power distribution frame, and the PDF supplies power to the console for blowers and dc power. The ac-on switch brings up power only if the emergency off switches on all maintenance consoles and the power distribution frame are on, and certain circuit breakers in the PDF are on.

When ac power is supplied to the maintenance console, CPU frame blower sequencing is started immediately. These blowers operate on 400 cycles and cannot be energized at one time because of the surge of current which would be produced; therefore, the blowers are energized in four groups of five frames per group. There is a delay of five seconds between the energizing of each blower group. The blowers in the maintenance console gates operate on 60 cycles and are energized immediately by the ac-on contactors in the PDF.

The dc power will be cranked up when all of the following are on: the CPU frame blowers, all of the circuit breakers in the maintenance console, the circuit breakers in each CPU frame power supply, certain circuit breakers in the PDF, and the dc-on switches on the maintenance console and PDF. Power to the dc power supplies must be brought up slowly; therefore, the 3 phase, 400 cycle power is turned on by using a motor driven variable autotransformer. When the transformer has been driven to the full-voltage position, contactors are energized which short out the transformer and remove it from the circuit. All power supplies in the CPU (except the special voltage for index storage drivers), are cranked-up together. After the logic voltages are up, the autotransformer is driven back down; a contactor energizes the special index storage supply and it is cranked-up.

When dc is turned off by the dc-off switch or a blown fuse, the voltage to the special index storage supply is dropped first. Approximately four seconds later, power to the logic voltage supplies is dropped.

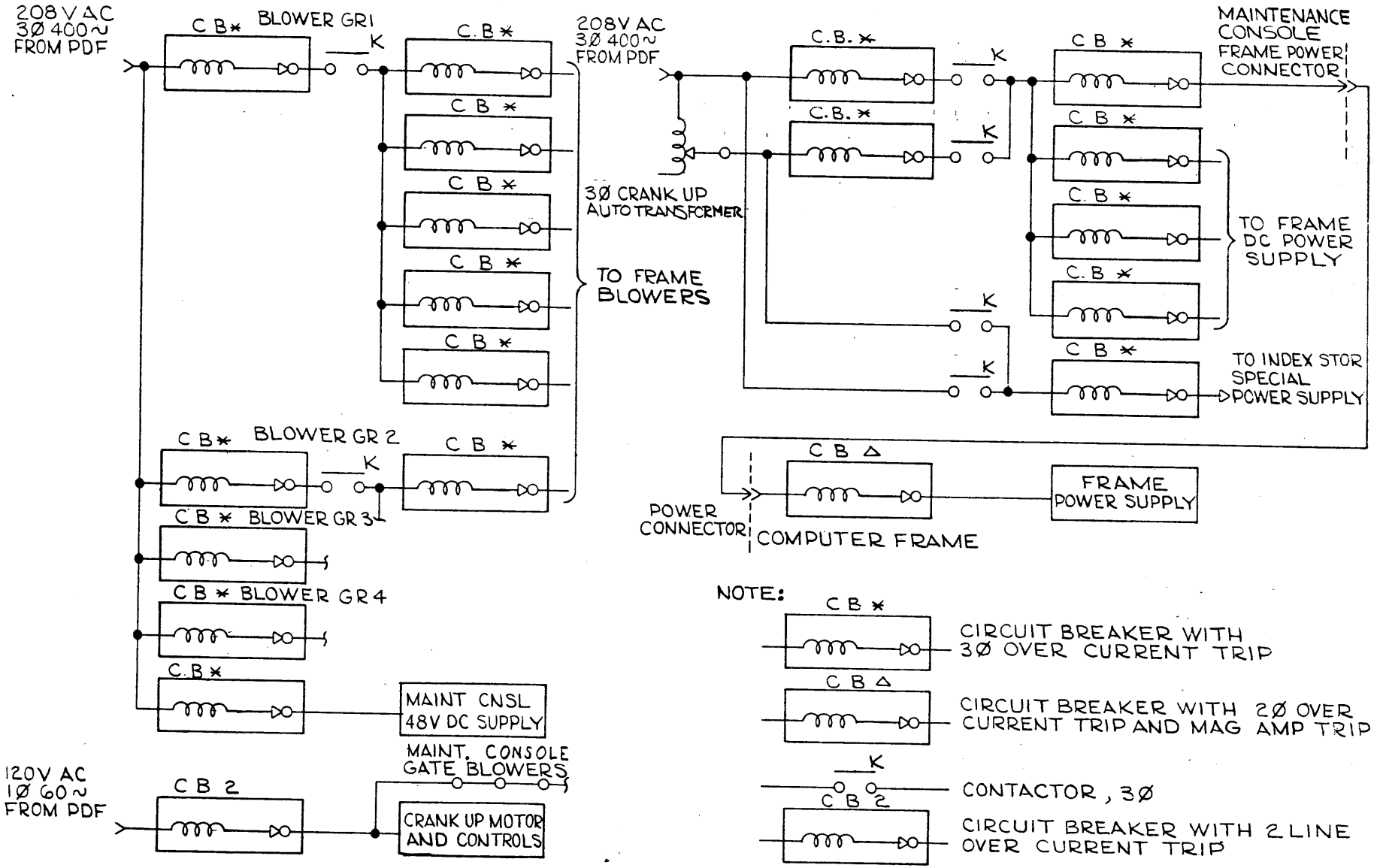


FIGURE 7.1-1. POWER DISTRIBUTION CPU MAINTENANCE CONSOLE

A blown fuse in any frame energizes the magnetic amplifier in the power supply. The magnetic amplifier trips the circuit breaker in that frame and drops power on the entire CPU. A blown fuse-light in the lower right hand corner of panel 3 indicates which frame contains the tripped circuit breaker. See Figure 2.3-1. These breakers may also be tripped by an overheated thermal contact in any gate or by an overload on the power supply.

7.2 MARGINAL CHECK

Provisions are made so that one or more frames can be marginal checked at a time. Voltages that are marginal checked are +6 volts and -12 volts. The controls for marginal checking are on the maintenance console and allow frame and voltage selection in any combination.

A buck-boost transformer is used to control the output voltages of the marginal check supplies. The input voltage for the marginal check supplies is connected to a reference voltage through the normally closed contacts of a relay. See Figure 7.2-1. The normally open contacts of the relay are connected to the movable contacts of a manually driven variable autotransformer. To shift the output dc voltage of the marginal check supply, the reference voltage of the buck-boost transformer must be changed. The center contacts of the variable autotransformer are placed at electrical zero, that is, at the same value as the reference voltage of the buck-boost transformer. Then the marginal check relay is energized.

The relay points are adjusted so that the normally open contact makes before the normally closed contact breaks, thus assuring a continuous voltage at the buck-boost transformer. The voltage from the variable autotransformer can be raised or lowered with a resulting increase or decrease in the dc output of the supply.

The marginal check relays are controlled by the marginal check switches on panel 3. See Figure 2.3-1. One switch is used for each frame. Raising a switch closes a contact which picks the +6 volt marginal relay in that frame. Putting the switch in the down position causes the -12 volt marginal relay in the same frame to be picked. A marginal check switch is operative only when its variable autotransformer is at electrical zero. The light over each variable autotransformer control is on unless the autotransformer is at electrical zero.

Energizing the marginal check switch does not necessarily mean that the relay is picked. Two indicators are associated with each switch; one indicator shows when the +6 volt relay is picked, and the other shows when the -12 volt relay is picked. Once the relays have been picked, they hold until the reset switch is depressed. The reset switch is effective only when the variable autotransformer associated with the picked relays is at electrical zero.

The tolerances of the various voltage outputs and the recommended swing of the marginal voltages are marked on the voltmeter dial. The voltmeter measures the voltage at the output of the power supply.

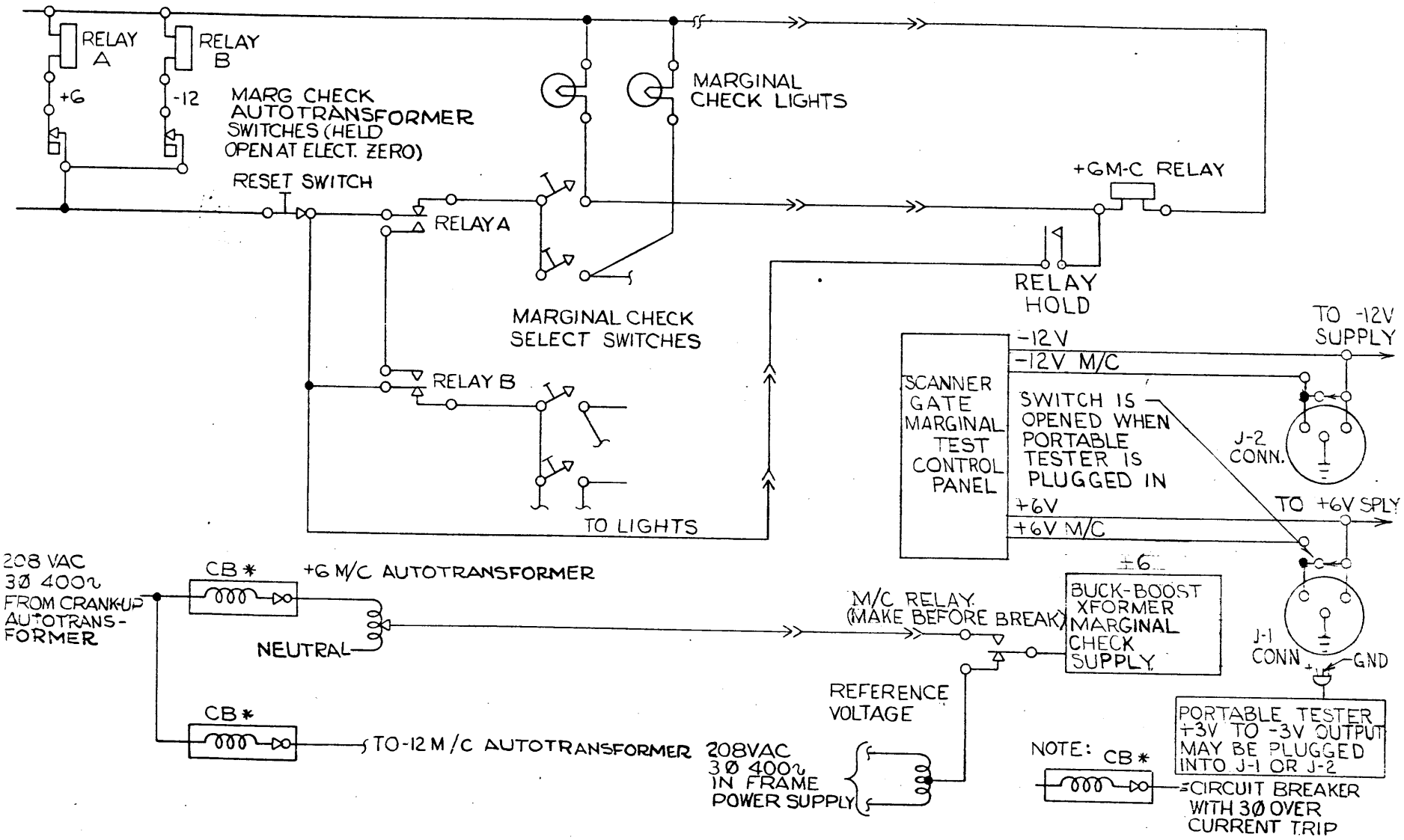


FIGURE 7.2-1. MARGINAL CHECK CONTROL

7.2.1 Scanner Gate Marginal Check

The scanner logic (on gate A7) can be marginal checked by means of a portable power supply. This supply is set to 0 volts and plugged into one of two connectors (one for +6 volts, the other for -12 volts) on the scanner marginal check control panel. See Figure 7.2-1. Separate switches for +6 and -12 volts allow the variable supply to be inserted in series with the normal supply voltages for these levels. The variable supply has a range of +3 volts to -3 volts through a 0 volt position which is employed when switching into, or out of marginal test mode. At the conclusion of a marginal test of the scanner controls, the +6 or -12 volt switch must be returned to its normal position to insure proper operation of the scanner.

CAUTION: Either switch must be returned to the normal position ONLY when the supply is set to the 0 volt position to avoid blowing the power supply fuse. After restoring the switch to the normal position, the variable power supply may be removed.

7.3 GROUNDING

The electronic grounds throughout the entire system (CPU, exchange, I-O, etc.) are common and insulated from the frame ground. The frames of all components of the system are connected together. The frame ground, an additional system bond, and generator neutral are tied together at the 400 cycle generator.

8 ERROR INJECTION AND ITS USE

ERROR INJECTION, the technique whereby data errors are deliberately created in the machine system, is the most effective method of testing check circuits under program control. Circuits are provided in the 7030 system to permit injection of errors for the testing of check circuits and the correction mechanism.

The error injection mode is active only when the system is in maintenance mode. The system is placed in maintenance mode by a manual toggle switch located on the maintenance console. Once the machine is in maintenance mode, error injection can be made active by depressing a pushbutton on the maintenance console or by program control. Either method turns on (1 bit) the error injection trigger, which is physically located at bit position 58 of the bounds register (address 3). The error injection trigger is turned off (0 bit) by a manual pushbutton on the maintenance console or by program control.

The error injection trigger, when on, (possible only in maintenance mode) enables control bits located in the bounds register (address 3) to designate the errors, if any, to be injected into the system. The specific abilities of the error injection control bits are as follows:

Bit Position	If "0"	If "1"
0	No action	Suppresses ECC and I parity error indications from the I checker
1	"	Invert: P3(12-15), P11(0-17), and C0
2	"	Invert: P4(16-23), P12(18-23), C1, and P12*
3	"	Invert: P5(24-31), P13(24-27), C2, and P13*
4	"	Invert: P6(32-39), P14(28-31), and C4
5	"	Invert: P7(40-47), P15(32-49), P16(46-49), and C8
6	"	Invert: P8(48-55), P17(50-55), C16, and P17*
7	"	Invert: P9(56-59), C32, and P9*
8	"	Invert: P10(60-63) and CT
58	No error injection	Permits bits 0-8 to become effective to control check bit inversion, thereby providing error injection.

* Parity on certain I unit execution instructions where only one field of X register is changed.

The program must cause a branch disable instruction to be executed prior to entering the error injection mode; in order to do this, the interrupt system must be disabled.

Address boundary comparison operations are suspended or suppressed while error injection is active. Programs should properly interpret any IJ, AD, DF, and DS indications resulting from a control bit pattern rather than an address remaining in the upper boundary register.

Exiting from the error injection mode can be accomplished only by setting bit 58 of the bounds register to zero. This can be done manually or under program control by

means of an instruction that will not be no-op'ed. Since all instructions carrying a parity error will be no-op'ed, an instruction that will not be no-op'ed must be provided in the error injection system.

A full word instruction carrying a parity inconsistency will always be no-op'ed. A full word containing two half-word instructions will have both instructions no-op'ed only if a parity discrepancy exists on both. If a parity discrepancy exists on only one of the half-word instructions, then only that half-word instruction will be no-op'ed; the other will be executed properly. Error injection can be turned off under program control by providing a half-word instruction (floating point store, etc.) that contains no parity discrepancy. Proper set-up of the error injecting control bits, of the operand in accumulator (or index register) and positioning of the instruction in the program and in memory are necessary prior to initiating error injection.

A program having an instruction sequence 1, 2, 3, 4, 5, ----n, in the 7030 computer usually finds that when 1 is being executed by the arithmetic unit, the lookahead unit may contain 2 and 3, and 4 and 5 may be in the I unit undergoing preparation. If instruction 1 is designated to turn on error injection (affecting the output of the I checker) it is apparent that instructions in lookahead ($4 \geq n \geq 0$) are immune to error injection, as may be a portion of the instructions in the I unit ($6 \geq n \geq 1$). This infers that a programmer has two basic approaches in utilizing error injection.

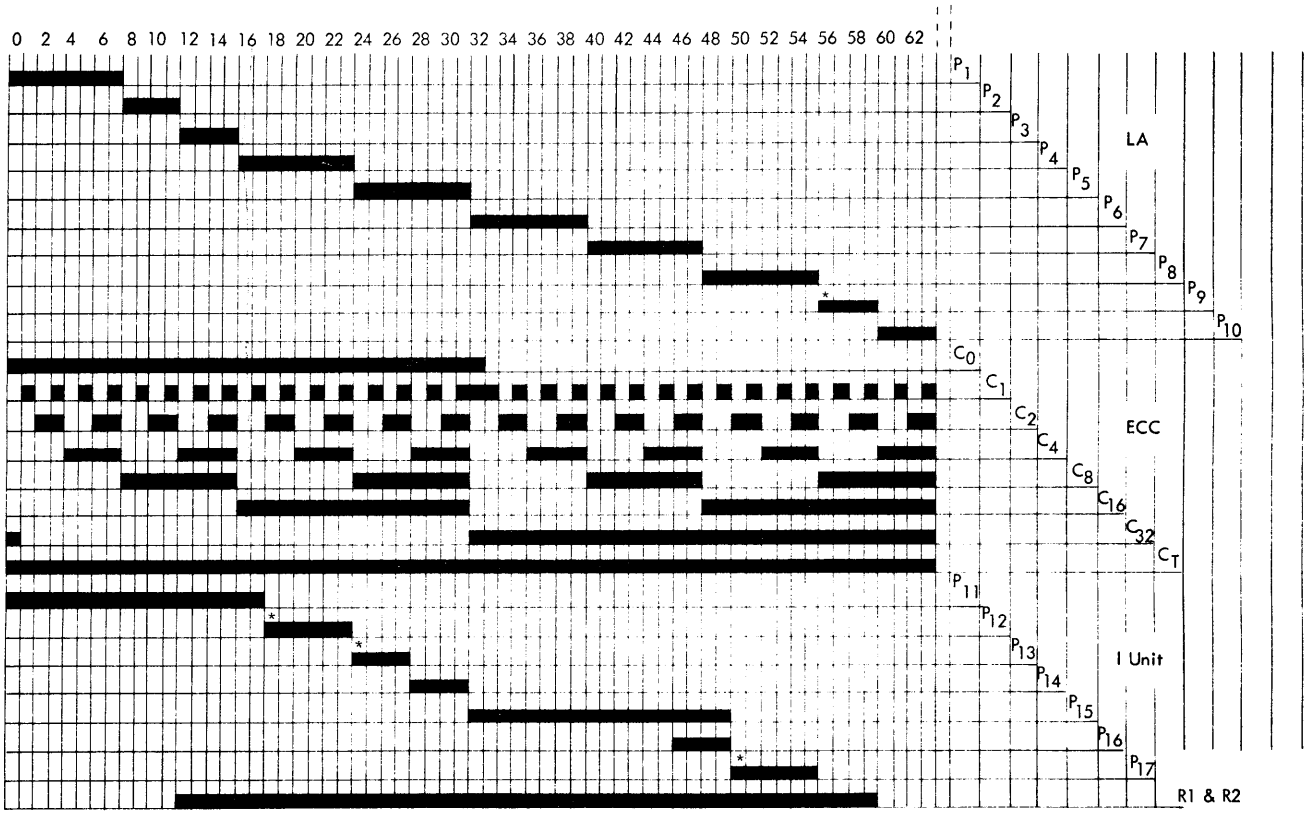
The first approach is that a programmer can buffer entry into error injection with 10 no-op instructions (5 full words) to insure that the first intended work instruction will be subject to error injection. In lieu of 10 no-op's, a programmer can use pseudo-store instruction plus a smaller buffering if error injection is initiated by a store to address 3, since the subsequent store cannot enter lookahead until previous store instructions have been cleared. (Exiting from error injection may require buffering for reasons similar to those already discussed.)

The second basic approach implies that a programmer can program the desired function in a very few instructions and insure that these instructions will be positioned in lookahead or the I unit so that they will not be affected by the error injection process, which could cause no-op'ing of these critical instructions. An effective technique for many cases involves creation of a data word containing parity or ECC inconsistencies and positioning of this word in external/internal or index memory for later use in conjunction with a program in normal operating mode. ECC bits can be made available to a program for analysis by writing tape in ECC mode and reading the tape in non-ECC mode.

One suggested approach entails the use of a single transmit backwards immediate instruction following an error inject initializing instruction. The transmit can safely be entered into the I unit and be prepared. The transmitting action can provide error words for later use and the last transmit function (or transmit to word 3) could or should cause a zero bit to be placed in position 58 of word 3, thereby deactivating error injection.

Extreme care should be exercised in programming the use of error injection. Full consideration should be given to the desired objective, check bits to be inverted, logical approach, and program provided. Error injection is the only mode of operation in which complete control of the system can be lost.

Refer to Figure 8-1 for the 7030 ECC and parity scheme and Figure 8-2 for Error Injection operation masks.



P1 (0-7)
P2 (8-11)
P3 (12-15)
P4 (16-23)
P5 (24-31)
P6 (32-39)
P7 (40-47)
P8 (48-55)
P9 (56-59)
P10 (60-63)
P11 (0-17)
P12 (18-23)
P12* (18-23) (x18)
P13 (24-27)
P13* (24-27) (x24)
P14 (28-31)
P15 (32-49)
P16 (46-49)
P17 (50-55)
P17* (50-55) (x50)
P9* (56-59) (x56)

* Parity on certain I unit execution instructions where only one field of X register is changed.

FIGURE 8-1. 7030 CHECK BIT ORGANIZATION CHART

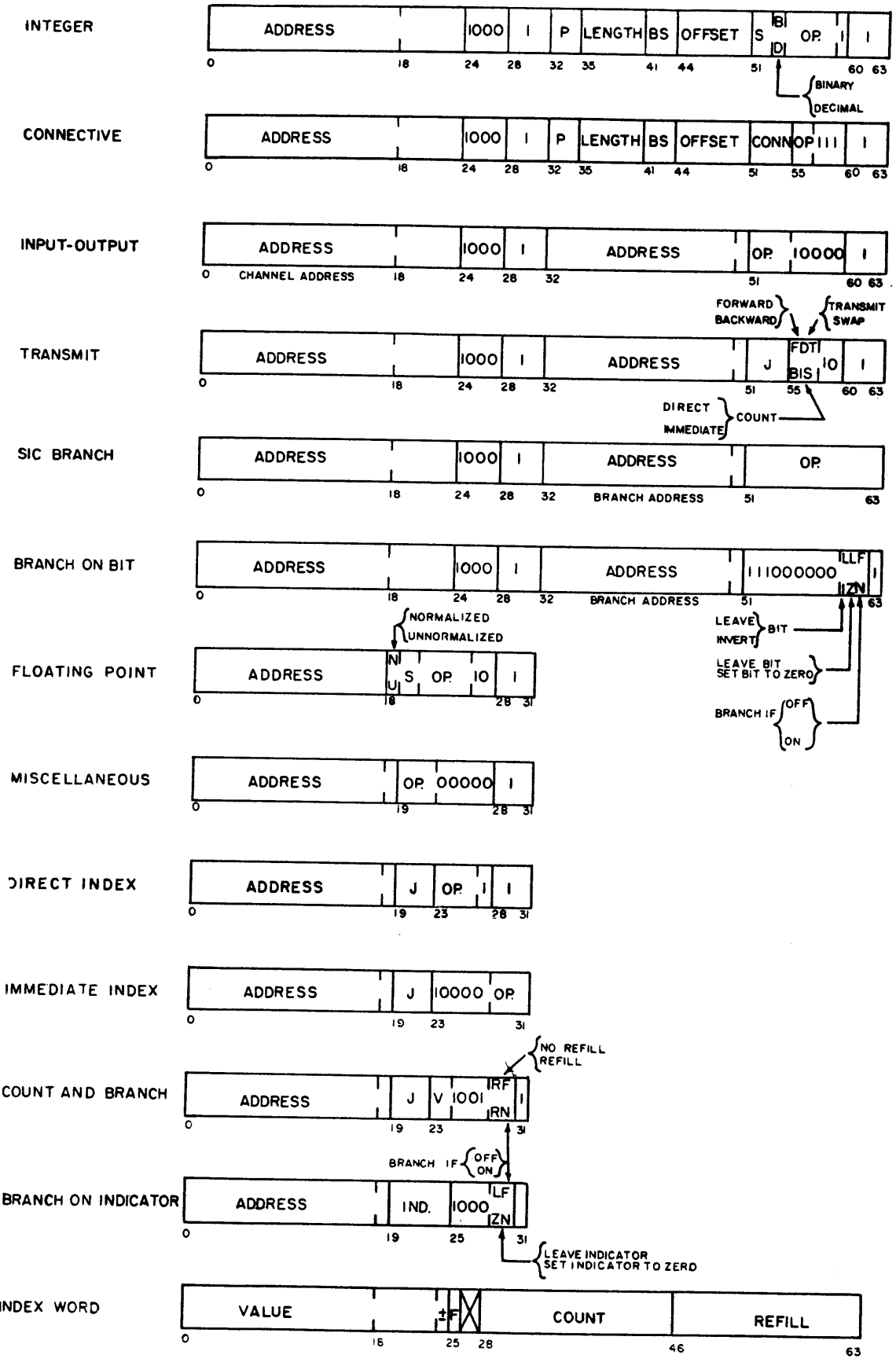
Bit To Be Chkd	No ECC or I-Par From Chkr	C0	C1	C2	C4	C8	C16	C32	CT	ECC Octal Code
0	1	1						1	1	603
1	1	1	1						1	701
2	1	1		1					1	641
3	1	1	1	1						740
4	1	1			1				1	621
5	1	1	1		1					720
6	1	1		1	1					660
7	1	1	1	1	1				1	761
8	1	1				1			1	611
9	1	1	1			1				710
10	1	1		1		1				650
11	1	1	1	1		1			1	751
12	1	1			1	1				630
13	1	1	1		1	1			1	731
14	1	1		1	1	1			1	671
15	1	1	1	1	1	1				770
16	1	1					1		1	605
17	1	1	1				1			704
18	1	1		1			1			644
19	1	1	1	1			1		1	745
20	1	1			1		1			624
21	1	1	1		1		1		1	725
22	1	1		1	1		1		1	665
23	1	1	1	1	1		1			764
24	1	1				1	1			614
25	1	1	1			1	1		1	715
26	1	1		1		1	1		1	655
27	1	1	1	1		1	1			754
28	1	1			1	1	1		1	635
29	1	1	1		1	1	1			734
30	1	1		1	1	1	1			674
31	1	1	1	1	1	1	1		1	775

Bit To Be Chkd	No ECC or I-Par From Chkr	C0	C1	C2	C4	C8	C16	C32	CT	ECC Octal Code
32	1	1	1					1		702
33	1		1					1	1	503
34	1			1				1	1	443
35	1		1	1				1		542
36	1				1			1	1	423
37	1		1		1			1		522
38	1			1	1			1		462
39	1		1	1	1			1	1	563
40	1					1		1	1	413
41	1		1			1		1		512
42	1			1		1		1		452
43	1		1	1		1		1	1	553
44	1				1	1		1		432
45	1		1		1	1		1	1	533
46	1			1	1	1		1	1	473
47	1		1	1	1	1		1		572
48	1						1	1	1	407
49	1		1				1	1		506
50	1			1			1	1		446
51	1		1	1			1	1	1	547
52	1				1		1	1		426
53	1		1		1		1	1	1	527
54	1			1	1		1	1	1	467
55	1		1	1	1		1	1		566
56	1					1	1	1		416
57	1		1			1	1	1	1	517
58	1			1		1	1	1	1	457
59	1		1	1		1	1	1		556
60	1				1	1	1	1	1	437
61	1		1		1	1	1	1		536
62	1			1	1	1	1	1		476
63	1		1	1	1	1	1	1	1	577

FIGURE 8-2. ERROR INJECTION OPERATION MASKS FOR SINGLE ERROR SIMULATION -- BITS 0 - 63

Appendix

A. Instruction Formats



B. List of Indicators

No.	Mnemonic	Mask	Class	Name
Equipment Check				
0	MK	1	P,H	Machine Check
1	IK	1	P,H	Instruction Check
2	IJ	1	P,S	Instruction Reject
3	EK	1	P,C	Exchange Control Check
Attention Request				
4	TS	1	P,C	Time Signal
5	CPUS	1	P,C	CPU Signal
Input-Output Reject				
6	EKJ	1	P,S	Exchange Check Reject
7	UNRJ	1	P,S	Unit Not Ready Reject
8	CBJ	1	P,S	Channel Busy Reject
Input-Output Status				
9	EPGK	1	P,C	Exchange Program Check
10	UK	1	P,C	Unit Check
11	EE	1	P,C	End Exception
12	EOP	1	P,C	End of Operation
13	CS	1	P,C	Channel Signal
14		1		Reserved
Instruction Exception				
15	OP	1	P,S	Operation Code Invalid
16	AD	1	P,S	Address Invalid
17	USA	1	P,S	Unended Sequence of Addresses
18	EXE	1	P,S	Execute Exception
19	DS	1	P,S	Data Store
20	DF	m	P,S*,C	Data Fetch
21	IF	m	P,S*,C	Instruction Fetch

*Class S when mask is one; otherwise Class C.

No.	Mnemonic	Mask	Class	Name
Result Exception				
22	LC	m	P,C	Lost Carry
23	PF	m	P,C	Partial Field
24	ZD	m	P,C	Zero Divisor
Result Exception - Floating Point				
25	IR	m	P,C	Imaginary Root
26	LS	m	P,C	Lost Significance
27	PSH	m	P,C	Preparatory Shift Greater than 48
28	XPFP	m	P,C	Exponent Flag Positive: Exp. $\geq 2^{10}$
29	XPO	m	P,C	Exponent Overflow: Exp. $\geq 2^{10}$
30	XPH	m	P,C	Exponent High: $2^{10} >$ Exp. $\geq 2^{9}$
31	XPL	m	P,C	Exponent Low: $2^{9} >$ Exp. $\geq 2^{6}$
32	XPU	m	P,C	Exponent Underflow: Exp. $\leq -2^{10}$
33	XPFN	m	P,C	Exponent Flag Negative: Exp. $\leq -2^{10}$
34	RU	m	P,C	Remainder Underflow

No.	Mnemonic	Mask	Class	Name
Flagging				
35	TF	m	T,C	Data Flag T } Reset by variable field length and floating point operations requiring data fetch.
36	UF	m	T,C	Data Flag U }
37	VF	m	T,C	Data Flag V }
38	XF	m	T,S*,C	Index Flag - Reset by index arithmetic operations

*Class S only during index branching when the mask is one and the system enabled; otherwise Class C.

No.	Mnemonic	Mask	Class	Name
Transit Operation				
39	BTR	m	P,C	Binary Transit
40	DTR	m	P,C	Decimal Transit
Program				
41-47	PG0-PG6	m	P,C	Program Indicators Zero through Six
48	XCZ	0	T,C	Index Count Zero } Reset by index arithmetic ops. other than comparisons
49	XVLZ	0	T,C	Index Value Less than Zero }
50	XVZ	0	T,C	Index Value Zero }
51	XVGZ	0	T,C	Index Value Greater than Zero }
52	XL	0	T,C	Index Low } Reset by index comparison operations.
53	XE	0	T,C	Index Equal }
54	XH	0	T,C	Index High }
Arithmetic Result				
55	MOP	0	T,C	To-Memory Op. Reset by variable field length or floating point op.
56	RLZ	0	T,C	Result Less than Zero } Reset by variable field length or floating point ops. except comparisons
57	RZ	0	T,C	Result Zero }
58	RGZ	0	T,C	Result Greater than Zero }
59	RN	0	T,C	Result Negative }
60	AL	0	T,C	Accum. Low } Reset by comparison operations
61	AE	0	T,C	Accum. Equal }
62	AH	0	T,C	Accum. High }
Mode				
63	NM	0	P,C	Noisy Mode

T Indicator temporary and is reset by later operations.

P Indicator permenent but may be turned off by interruption or during BI.

C The execution of the instruction during which the indicator is actuated is completed.

H The execution of the instruction during which the indicator is actuated is terminated.

S The execution of the instruction during which the indicator is actuated is suppressed, except during EX, EXIC, T, and SWAP.

C. Storage Assignment

Location		Name	Length	Bit Address
0		Zero	64	0-63
1	P,a	Interval timer	19	0-18
1	P,b	Elapsed time clock	36	28-63
2	P	Interruption address	18	0-17
3	P	Upper boundary	18	0-17
3	P	Lower boundary	18	32-49
3	P	Boundary control bit	1	57
4		Maintenance bits	64	0-63
5	b	Channel address	7	12-18
6		Other CPU	19	0-18
7		Left zeros count	7	17-23
7		All ones count	7	44-50
8		Left half of accumulator	64	0-63
9		Right half of accumulator	64	0-63
10		Accumulator sign	8	0-7
11	c	Indicators	64	0-63
12	d	Mask	64	0-63
13		Remainder	64	0-63
14		Factor	64	0-63
15		Transit	64	0-63
16-31		Index registers X0 through X15	64	0-63

P Permanently protected area of storage.

a Read-only except for STORE VALUE, STORE COUNT, STORE REFILL, and STORE ADDRESS.

b Read-only.

c Bit positions 0-19 are read-only.

d Bit positions 0-19 are always ones, and bit positions 48-63 are always zeros.

D. Alphabetical Listing of Operation Codes

+	Add
+MG	Add to magnitude
*	Multiply
*+	Add product
/	Divide
B	Branch
BB	Branch on bit
BD	Branch disabled
BE	Branch enabled
BEW	Branch enabled and wait
BI	Branch on indicator
BR	Branch relative
C	Connect
C+	Add to count
CB	Count and branch
CBR	Count, branch, and refill
CCW	Copy control word
CM	Connect to memory
CV	Convert
CT	Connect for test
CTL	Control
D+	Add double
D+MG	Add double to magnitude
D*	Multiply double
D/	Divide double
DCV	Convert double
DL	Load double
DLWF	Load double with flag
E+	Add to exponent
EX	Execute
EXIC	Execute indirect and count
F+	Add to fraction
K	Compare
KC	Compare count
KE	Compare if equal
KF	Compare field
KFE	Compare field if equal
KFR	Compare field for range
KMG	Compare magnitude
KMGR	Compare magnitude for range
KR	Compare for range
KV	Compare value

L	Load
LC	Load count
LCV	Load converted
LFT	Load factor
LOC	Locate
LR	Load refill
LTRCV	Load transit converted
LTRS	Load transit and set
LV	Load value
LVE	Load value effective
LVS	Load value with sum
LWF	Load with flag
LX	Load index
M+	Add to memory
M+MG	Add magnitude to memory
M+1	Add one to memory
NOP	No operation
R	Refill
R/	Reciprocal divide
RCZ	Refill on count zero
RD	Read
REL	Release
RNX	Rename
SC	Store count
SHF	Shift fraction
SIC	Store instruction counter if
SLO	Store low order
SR	Store refill
SRD	Store rounded
SRT	Store root
ST	Store
SV	Store value
SVA	Store value in address
SWAP	Swap
SX	Store index
T	Transmit
V+	Add to value
V+C	Add to value and count
V+CR	Add to value, count and refill
W	Write
Z	Store zero

E. Complete Operation and Modifier List

INTEGER ARITHMETIC OPERATIONS; Instruction bits 51-63

ssbxxxxx1 iiii	Mnemonic	Name	Page
Operations			
00000	+	Add	60
10000	+MG	Add to magnitude	60
00010	L	Load	61
10010	LWF	Load with flag	61
00100	M+	Add to memory	61
10100	M+MG	Add magnitude to memory	62
10101	M+1	Add one to memory	62
00110	ST	Store	63
10110	SRD	Store rounded	64
01000	K	Compare	65
11000	KF	Compare field	65
01001	KE	Compare if equal	65
11001	KFE	Compare field if equal	66
01010	KR	Compare for range	66
11010	KFR	Compare field for range	67
11110	LTRS	Load transit and set	67
01100	*	Multiply	68
00101	LFT	Load factor	69
11100	*+	Multiply and add	69
01110	/	Divide	70
Classes			
0		Binary	
1		Decimal	
Modifiers			
0		Signed	
1		Unsigned	
0		Same sign	
1		Negative sign	

RADIX CONVERSION OPERATIONS; Instruction bits 51-63

ssbxxxxx1iiii	Mnemonic	Name	Page
Operations			
00001	LCV	Load converted	72
10001	LTRCV	Load transit converted	73
01101	CV	Convert	73
11101	DCV	Convert double	74
Classes			
0		Binary	
1		Decimal	
Modifiers			
0		Signed	
1		Unsigned	
0		Same sign	
1		Negative sign	

CONNECTIVE OPERATIONS; Instruction bits 51-63

ccccxx111iiii	Mnemonic	Name	Page
Operations			
00	C	Connect	76
01	CM	Connect to memory	77
10	CT	Connect for test	77

FLOATING POINT OPERATIONS; Instruction bits 18-31

nssxxxxx10iiii	Mnemonic	Name	Page
Operations			
00000	+	Add	86
01000	+MG	Add to magnitude	88
00001	L	Load	88
01001	LWF	Load with flag	88
00010	M+	Add to memory	88
01010	M+MG	Add magnitude to memory	89
00011	ST	Store	90
00100	K	Compare	90
01100	KMG	Compare magnitude	91
00101	KR	Compare for range	91
01101	KMGR	Compare magnitude for range	92
00110	*	Multiply	92
00111	/	Divide	93
01111	R/	Reciprocal divide	94
11011	SRT	Store root	94
10000	D+	Add double	95
11000	D+MG	Add double to magnitude	96
10001	DL	Load double	96
11001	DLWF	Load double with flag	96
01011	SRD	Store rounded	96
10011	SLO	Store low order	97
10110	D*	Multiply double	97
10010	LFT	Load factor	98
01110	*+	Multiply and add	98
10111	D/	Divide double	99
10100	F+	Add to fraction	101
11100	SHF	Shift fraction	102
10101	E+	Add to exponent	102
11101	E+I	Add immediate to exponent	102
Classes			
0		Normalized	
1		Unnormalized	
Modifiers			
0		Same sign	
1		Absolute sign	
0		Same sign	
1		Negative sign	

DIRECT INDEX ARITHMETIC; Instruction bits 19-31

jjjjxxxx1iiii	Mnemonic	Name	Page
Operations			
0000	LX	Load index	23
0001	LV	Load value	23
0010	LC	Load count	24
0011	LR	Load refill	24
1000	SX	Store index	24
1001	SV	Store value	24
1010	SC	Store count	24
1011	SR	Store refill	24
0101	V+	Add to value	24
0110	V+C	Add to value and count	24
0111	V+CR	Add to value, count, and refill	24
0100	KV	Compare value	24
1100	KC	Compare count	24
1111	RNX	Rename	27
1101	LVE	Load value effective	28
1110	SVA	Store value in address	29

IMMEDIATE INDEX ARITHMETIC; Instruction bits 19-31

jjjj10000xxxx	Mnemonic	Name	Page
Operations			
0001	LVI	Load value immediate	25
0010	LCI	Load count immediate	25
0011	LRI	Load refill immediate	25
1001	LVNI	Load value negative immediate	25
0101	V+I	Add immediate to value	25
0110	V+IC	Add immediate to value and count	25
0111	V+ICR	Add immediate to value, count and refill	25
1101	V-I	Subtract immediate from value	25
1110	V-IC	Subtract immediate from value and count	25
1111	V-ICR	Subtract immediate from value, count and refill	25
0000	C+I	Add immediate to count	25
1000	C-I	Subtract immediate from count	25
0100	KVI	Compare value immediate	25
1100	KVNI	Compare value negative immediate	25
1010	KCI	Compare count immediate	25
1011	LVS	Load value with sum	28

UNCONDITIONAL BRANCHING; Instruction bits 19-31

xxx000000iiii	Mnemonic	Name	Page
Operations			
010	B	Branch	39
011	BR	Branch relative	40
000	BE	Branch enabled	40
001	BD	Branch disabled	40
100	BEW	Branch enabled and wait	40
110	NOP	No operation	40

INDICATOR BRANCHING; Instruction bits 25-31

1000xxi	Mnemonic	Name	Page
Operation	BI	Branch on indicator	40
Modifiers			
0		Leave indicator	
1		Set indicator to zero	
0		Branch if off	
1		Branch if on	

BIT BRANCHING; Instruction bits 51-63

111000000xxxi	Mnemonic	Name	Page
Operation	BB	Branch on bit	41
Modifiers			
0		Leave bit	
1		Invert bit	
0		Leave bit	
1		Set bit to zero	
0		Branch if off	
1		Branch if on	

INDEX BRANCHING; Instruction bits 19-31

jjjjxx1001xxi	Mnemonic	Name	Page
Operations			
0	CB	Count and branch	26,40
1	CBR	Count, branch and refill	26,41
Modifiers			
0		Branch if count non-zero	
1		Branch if count zero	
00		Leave value unchanged	
01		Add half to value	
10		Add one to value	
11		Subtract one from value	

STORE INSTRUCTION COUNTER IF; Instruction bits 24-31

1000iiii	Mnemonic	Name	Page
Operation	SIC	Store instruction counter if	41

INPUT-OUTPUT OPERATIONS; Instruction bits 51-63

xxxx10000iiii	Mnemonic	Name	Page
Operations			
0000	RD	Read	119
0001	W	Write	119
0010	CTL	Control	120
0011	LOC	Locate	120
1001	REL	Release	121
0100	RD(SEOP)	Read SEOP	121
0101	W(SEOP)	Write SEOP	121
0110	CTL(SEOP)	Control SEOP	121
0111	LOC(SEOP)	Locate SEOP	121
1101	REL(SEOP)	Release SEOP	121
1000	CCW	Copy control word	122

TRANSMIT OPERATIONS; Instruction bits 51-63

jjjjfdx10iiii	Mnemonic	Name	Page
Operations			
0	T	Transmit	30
1	SWAP	Swap	30
Modifiers			
0		Forward	
1		Backward	
0		Direct count	
1		Immediate count	

MISCELLANEOUS OPERATIONS; Instruction bits 19-31

xxx100000iiii	Mnemonic	Name	Page
Operations			
000	R	Refill	26
001	RCZ	Refill on count zero	26
010	EX	Execute	50
011	EXIC	Execute indirect and count	50
100	Z	Store zero	31

INDEXING MODES FOR VARIABLE FIELD LENGTH OPERATIONS; Instruction bits 32-34

ppp	Mnemonic	Name	Page
		Normal address modification	24
000		Direct addressing	
100	I(suffix)	Immediate addressing	
		Progressive indexing	21
001	V+	Add to value	
010	V+C	Add to value and count	
011	V+CR	Add to value, count and refill	
101	V-	Subtract from value	
110	V-C	Subtract from value and count	
111	V-CR	Subtract from value, count, and refill	

F. Powers of Two

2^n	n	2^n	n
2	1	8 589 934 592	33
4	2	17 179 869 184	34
8	3	34 359 738 368	35
16	4	68 719 476 736	36
32	5	137 438 953 472	37
64	6	274 877 906 944	38
128	7	549 755 813 888	39
256	8	1 099 511 627 776	40
512	9	2 199 023 255 552	41
1 024	10	4 398 046 511 104	42
2 048	11	8 796 093 022 208	43
4 096	12	17 592 186 044 416	44
8 192	13	35 184 372 088 832	45
16 384	14	70 368 744 177 664	46
32 768	15	140 737 488 355 328	47
65 536	16	281 474 976 710 656	48
131 072	17	562 949 953 421 312	49
262 144	18	1 125 899 906 842 624	50
524 288	19	2 251 799 813 685 248	51
1 048 576	20	4 503 599 627 370 496	52
2 097 152	21	9 007 199 254 740 992	53
4 194 304	22	18 014 398 509 481 984	54
8 388 608	23	36 028 797 018 963 968	55
16 777 216	24	72 057 594 037 927 936	56
33 554 432	25	144 115 188 075 855 872	57
67 108 864	26	288 230 376 151 711 744	58
134 217 728	27	576 460 752 303 423 488	59
268 435 456	28	1 152 921 504 606 846 976	60
536 870 912	29	2 305 843 009 213 693 952	61
1 073 741 824	30	4 611 686 018 427 387 904	62
2 147 483 648	31	9 223 372 036 854 775 808	63
4 294 967 296	32	18 446 744 073 709 551 616	64

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