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3880

Storage Control Models 21 and 23
Error Code Manual

3880 ECM	Seq HA0010	PN 6315684 1 of 2	881145 13 Jan 84	881216 15 Aug 84	A15621 01 Apr 85		

Preface

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Maintenance Manual Ordering Procedure (IBM Internal)

Individual pages of the 3880 Maintenance manual can be ordered from the Tucson plant by using the Wiring Diagram/Logic Page Request, Z150-0130 (U/M 015). In the logic page columns, enter the page identifier information: sequence number and side number **1**, part number **2**, and engineering change (EC) number **3**.

	1	**2**	**3**
3880 ECM	**Seq HA0010**	**PN 6315684 2 of 2**	**881145 13 Jan 84**

Groups of pages can be ordered by including a description (section, volume) and the machine serial number.

Related Publications

A list of related publications can be found in the Maintenance Support Manual, REF section.

3880 ECM	**Seq HA0010**	**PN 6315684 2 of 2**	**881145 13 Jan 84**	**881216 15 Aug 84**	**A15621 01 Apr 85**		

Introduction

Contents of This Section

Description by Section

The 3880 Error Code Manual (ECM) is divided into sections identified by tabs.

The following is a description of the tab labels and the section content.

INTRO INTRODUCTION

The Introduction section defines the organization of the manual and the content of the manual sections.

The introduction section also explains how to use this manual and gives power off procedures.

ECI ERROR CODE INDEX

The Error Code Index section contains a list of all known error codes and references to other sections in the ECM that contain information to help correct each error.

The eight sections below contain error-associated information such as:

- Error Condition Diagrams
- Circuit Descriptions
- Diagnostic Procedures
- FRUs associated with the error

CTL-I CONTROL INTERFACE

MNT-C MAINTENANCE CONNECTION

DBFR DATA BUFFER

CTRL CONTROL

CHL-I CHANNEL INTERFACE

DD DISKETTE DRIVE

PORT PORT

STOR SUBSYSTEM STORAGE

The sections below contain a description of the diagnostics.

DC INT DIAGNOSTIC CODE INTRODUCTION

DC HC DIAGNOSTIC CODE HARD CORE

DC 5000 DIAGNOSTIC CODE 5000

DC 6000 DIAGNOSTIC CODE 6000

DC 7000 DIAGNOSTIC CODE 7000

How to Use This Manual

1. Collect all available error symptom information.
2. Look in the ECI section for the error code.
3. Go to the page referred to by the ECI to continue the repair procedure. The front of each error code section contains a functional diagram and a circuit description.

   Each error code will have:

   - A description of the error
   - The card with the error indicator
   - A list of FRUs that can cause the error
   - Diagnostics that can be run and looped to trap the error

   To check nets or to scope in the failing area, use:

   - List of cards that can cause the error
   - Functional diagram for data flow
   - Circuit description for theory
   - Logic Reference Manual (LRM) for pin locations
   - To check the continuity of a net use the XREF pages in the LRM.
4. Use the DC sections of this manual for information on the diagnostic routines.

   Use the OPER section in the Maintenance Support Manual (MSM) to assist in locating high-level circuit diagrams and descriptions of machine functions.

   Use the LGND section in the Maintenance Information Manual (MIM) for a description of the symbology used. Use the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

How to Convert Card Location to LRM Page

The first character of the LRM page number represents the gate and board location, as indicated in the following charts.

01A Gate Board Locations

A1 = A	B1 = E
A2 = B	B2 = F
A3 = C	B3 = G
A4 = D	B4 = H

01B Gate Board Locations

A1 = J	B1 = L
A2 = K	B2 = M

The next two characters of the LRM page number represent the card location. The last two characters are (usually) zeros.

Example: For card location 01A B3 F2

1. Use chart for 01A gate
2. B3 Translates to G the first letter of the LRM page → G
3. The card location is the second and third letters of the LRM page. → GF2
4. Add two 00s → GF200
5. Therefore, LRM page GF200 represents the card at location 01A-B3F2.

   If the card has more information (circuits) than can be shown on one LRM page the second page for this card would be labeled GF210.

Description and Use of This Manual INTRO 10

Power Off Procedure to Remove or Replace Logic Cards

CAUTION
The Power Check indicator (operator panel) must be off. See the instructions on resetting the Power Check indicator on this page.

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01A-B1 Board (Maintenance Board)

CAUTION
This action also removes power from both storage directors and the subsystem storage. Ensure that both storage directors can be taken offline.

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1. Press the Device Power Sequencing switch (power switch panel) to the disabled position.
2. Turn the Power Select switch (power switch panel) to the Local position.
3. Press the Subsystem Power switch (operator panel) to the Off position.

01A-A3, A4, B3, B4 Boards (Storage Directors 1 and 2)

Warning: To prevent damage to the power supply, always use the DC Power System switch (power switch panel) to remove dc power from both storage directors.

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. . . . . .

. . . . . .

1. Press the Device Power Sequencing switch (power switch panel) to the disabled position.
2. Turn the Power Select switch (power switch panel) to the Local position.
3. Press the DC Power System switch (power switch panel) to the Off position.

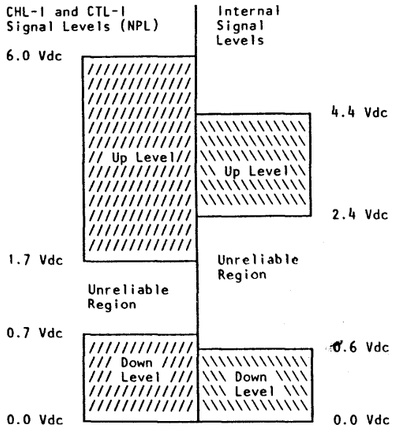
01A-A3, A4, B3, B4 Board (Storage Director 1 or Storage Director 2 Only)

1. Press the Device Power Sequencing switch (power switch panel) to the disabled position.
2. Turn the Power Select switch (power switch panel) to the Local position.
3. Turn the Storage Director Power SD1 or SD2 switch (power switch panel) to the Off position.

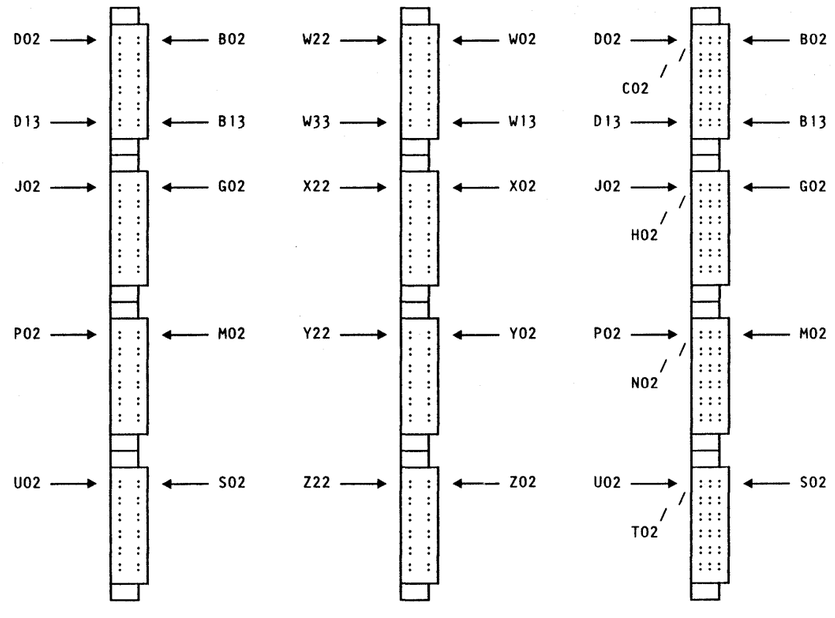
01B-A1, A2 Boards (Subsystem Storage)

1. Press the Device Power Sequencing switch (power switch panel) to the disabled position.
2. Turn the Power Select switch (power switch panel) to the Local position.
3. Press the Subsystem Storage Power switch (power switch panel) to the Off position.

Voltage Information



CARD CONTACT ASSIGNMENT



Resetting the Subsystem Power Check Indicator (Operator Panel)

Note: The following procedure assumes both storage directors and subsystem storage are offline. On the 3880 models with Subsystem Storage the Power Check Indicator may be set by either a PS-1 power failure or a PS-2 power failure.

1. Press the Device Power Sequencing switch (power switch panel) to the disable position.
2. Press the Subsystem Power switch (operator panel) to the Off position.
3. Reset any tripped circuit breakers or circuit protectors.
4. Turn the Power Select switch (power switch panel) to the Local position.
5. Press the DC Power System switch (power switch panel) to the On position.
6. Press the Subsystem Storage Power switch (power switch panel) to the On position.

Scoping Information

Use an oscilloscope (X 10 probe) to measure the DIF/VTL levels. Do not use a volt-ohmmeter.

Use the INDEX and OPER sections in the Maintenance Support Manual (MSM) to assist in locating high-level circuit diagrams and descriptions of machine functions.

Use the LGND section in the Maintenance Information Manual (MIM) for a description of the symbology used in the MIM circuit diagrams. Use the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Error Condition Index

Contents of This Section

Contents ECI 1

Error Condition Codes

Error condition codes are divided into four distinct classes.

- Symptom codes
- Isolation codes
- Power codes
- Initial microcode load (IML) codes

Symptom Codes

Symptom codes are generated when an error condition is detected while the functional microcode is running. The symptom codes are in sense bytes 22 and 23.

Isolation Codes

Isolation codes are generated by the diagnostic microcode when an error condition is detected while the diagnostic microcode is running, these codes are six digits. Isolation codes pertaining to the maintenance board are usually four digits.

Power Codes

Power codes are generated by the power sensing circuits when an error is detected in the power system.

IML codes

IML codes are generated by the IML microcode when an error condition is detected during the IML process.

The error condition index contains all known error condition codes, except power codes. Power codes are all contained within the maintenance device (MD), with cross-references to the PWR section in the Maintenance Information Manual (MIM).

How To Use This Index

1. Find the error condition code in the left-hand column **1**.
2. Go to the page indicated in the right-hand column **2** to find additional information associated with that error condition.

1 Error Condition Code — **2** ECM Page

Special Codes

If only one storage director is failing, a -1 is placed after the two-digit IML code. If both storage directors are failing, a -2 is placed after the IML code.

An x in a code means that character can be anything from 0 through F.

Diagnostics

The diagnostics error codes are in the DC sections of this manual. The diagnostics are listed in the index by routine, and test, the error stops are not shown in the index. To find information on the error stops, go to the routine and test.

Error Condition Codes ECI 2

Notes:

1. A 3880 storage director has stopped during an IML due to a wrong bit set in the channel interface (CIF) card address switches. See the INST section in the Maintenance Information Manual (MIM) for the correct address settings.

2. This code indicates that a selective reset occurred while a device was selected. Normally, this code is preceded by a check-1 error that is stored in the alternate storage director.

3. This code is not an error. It indicates that a trace/save operation was performed. See the MD section in the Maintenance Support Manual (MSM) for a description of the save command.

4. All 5xxx to 7xxx codes are described in sequence in the DC section of this manual.

5. These codes are not errors. They indicate the state of the IML process when a clock stop error occurs.

6. A IML F5 indicates that an IML is successfully completed.

7. A IML F2 indicates that an invalid patch area is used on the diskette.

Error Code Index

Error Code Index

Control Interface

Contents of This Section

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
32	10	1	C01
38	10	1	C01
3D	10	1	C01
A5	10	1	C01
A7	10	1	C01
A8	10	1	C01
AA	10	1	C01
B4	10	1	C01
B5	15	1	C03
BA	15	1	C03
C3	15	1	C03
C5	15	1	C03
2004	20	1	C05
2008	20	1	C05
2018	20	1	C05
2020	20	1	C05
2080	20	1	C05
20F0	20	1	C05
2540	20	1	C05
2801	20	1	C05
2802	25	1	C05
2810	25	1	C07
2820	25	1	C07
292A	25	1	C07

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

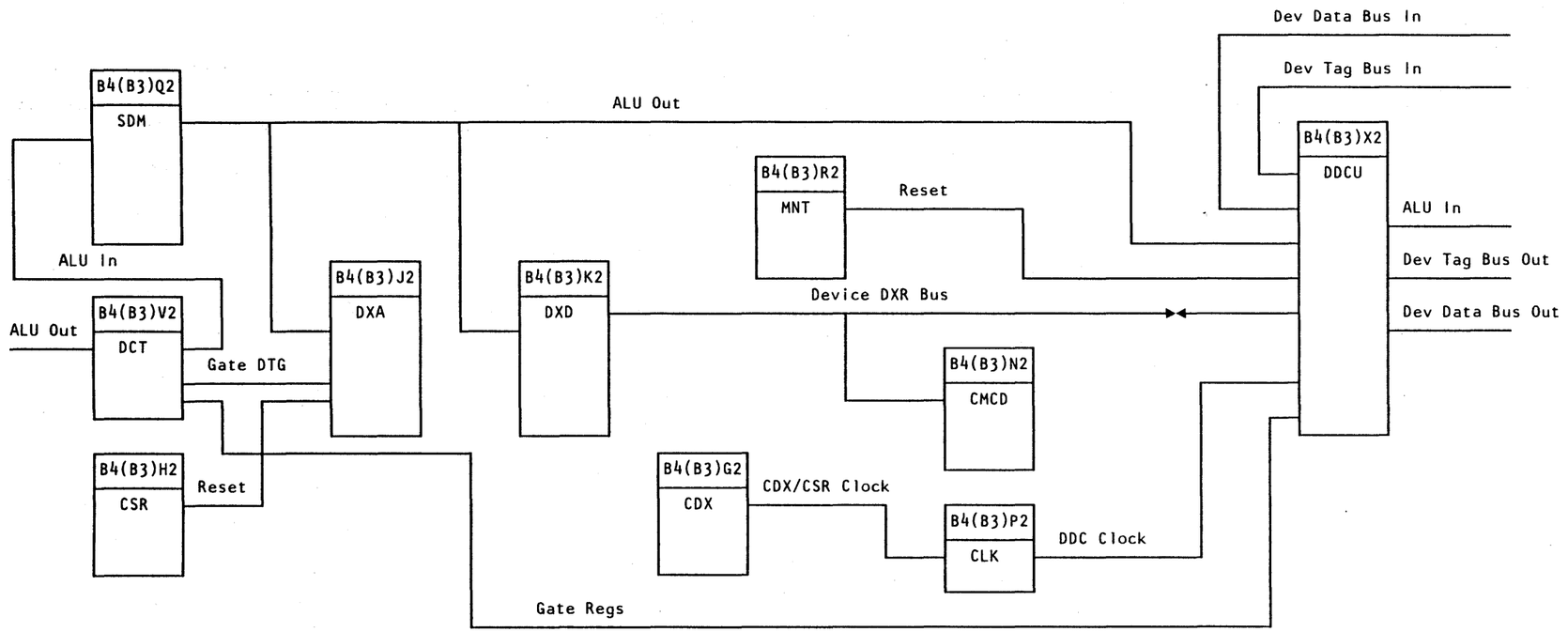
See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Error Code Diagram Model 21

Data sent to a device flows through the control interface area. Data between the device and the device DXR bus (to the DXD and CMCD cards) flows through the DDC card. This data flow is controlled by the SDM card in conjunction with the Device Tag/ Ctrl Bus In lines and the DDC card.

Note: See the OPER section of the MSM for a detailed description of this area



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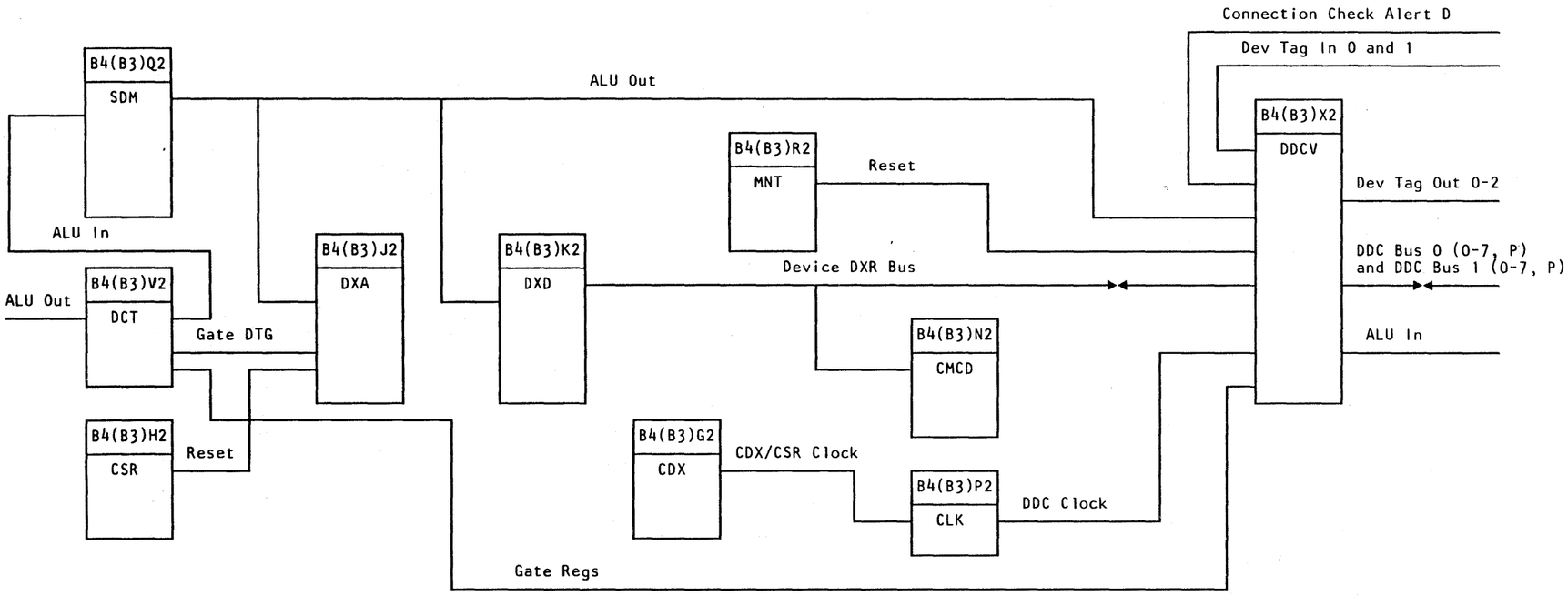
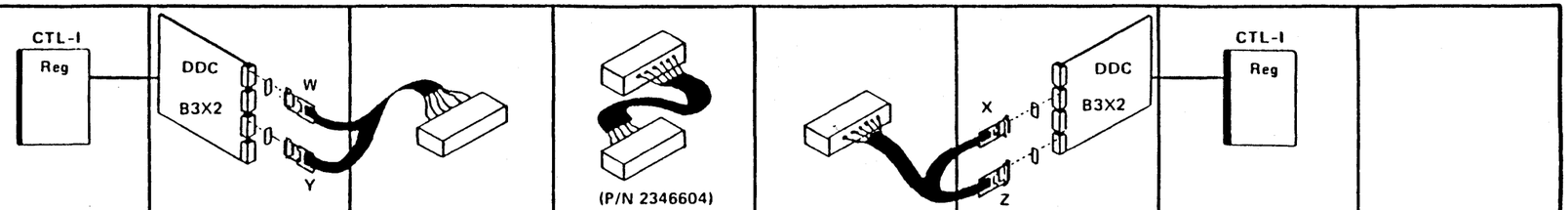
Error Code Diagram Model 23

Data sent to a device flows through the control interface area. Data between the device and the device DXR bus (to the DXD and CMCD cards) flows through the DDC card. This data flow is controlled by the SDM card in conjunction with the Device Tag/ Ctrl Bus In lines and the DDC card.

Note: See the OPER section of the MSM for a detailed description of this area

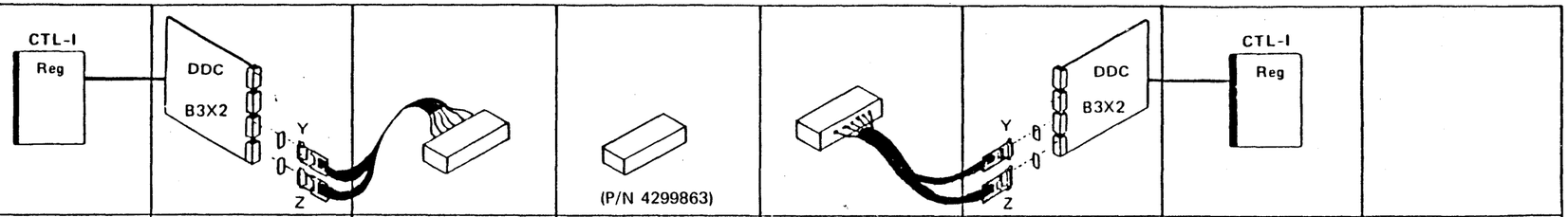


Control Interface Wrap Connection Model 21



Outbound Line Name	DDC Register	Leaves DDC Top-Card Connectors	Leaves CTL-I Tailgate Connector		Wraparound Cable	Enters CTL-I Tailgate Connector		Enters DDC Top-Card Connectors	DDC Register	Inbound Line Name
+DDC Bus Out Bit 0	DBO-0	W24	01T-A1(A2)A	D04	→	01T-A1(A2)A	J04	X24	DBI-0	+DDC Bus In Bit 0
+DDC Bus Out Bit 1	DBO-1	W25		B05	→		G05	X25	DBI-1	+DDC Bus In Bit 1
+DDC Bus Out Bit 2	DBO-2	W26		D06	→		J06	X26	DBI-2	+DDC Bus In Bit 2
+DDC Bus Out Bit 3	DBO-3	W28		B08	→		G08	X28	DBI-3	+DDC Bus In Bit 3
+DDC Bus Out Bit 4	DBO-4	W29		D09	→		J09	X29	DBI-4	+DDC Bus In Bit 4
+DDC Bus Out Bit 5	DBO-5	W30		B10	→		G10	X30	DBI-5	+DDC Bus In Bit 5
+DDC Bus Out Bit 6	DBO-6	W31		D11	→		J11	X31	DBI-6	+DDC Bus In Bit 6
+DDC Bus Out Bit 7	DBO-7	W32		B12	→		G12	X32	DBI-7	+DDC Bus In Bit 7
+DDC Bus Out Bit P	DBO-P	W23		B03	→		G03	X23	DBI-P	+DDC Bus In Bit P
+Tag Out Bus Bit 0	DTO-0	Y23	01T-A1(A2)B	B03	→	01T-A1(A2)B	G03	Z23	DTI-0	+Select Active
+Tag Out Bus Bit 4	DTO-4	Y25		B05	→		J04	Z24	DTI-1	+Tag Valid
+Tag Out Bus Bit 5	DTO-5	Y24		D04	→		G05	Z25	DTI-4	+Normal End
+Tag Out Bus Bit 6	DTO-6	Y28		B08	→		J06	Z26	DTI-2	+Check End
+Tag Out Bus Bit 7	DTO-7	Y26		D06	→		J13	X33		+Sync In
+Tag Out Bus Bit P	DTO-P	Y29		D09	→					
+Tag Gate	DTG-1	Y30		B10	→		G08	Z28	DTI-7	+Error Alert (In)
+Sync Out		W33		D13	→		J09	Z29	DTI-6	+Index
+Response	DTG-2	Y32		B12	→					
+Recycle		Y33		D13	→		G12	Z32	DTI-3	+CE Alert
+Select Hold	DTG-0	Y31		D11	→					

Control Interface Wrap Connection Model 23



Outbound Line Name	DDC Register	Leaves DDC Top-Card Connectors	Leaves CTL-I Tailgate Connector 01T-A1(A2)B	CTL-I Wrap Tool (Bidirectional)	Enters CTL-I Tailgate Connector 01T-A1(A2)B	Enters DDC Top-Card Connectors	DDC Register	Inbound Line Name
−DDC Bus 0 Bit 0	DBOH-0	Y08	B07	→	G04	Z05	DBL-0	−DDC Bus 1 Bit 0
+DDC Bus 0 Bit 0	DBOH-0	Y28	B08	→	G05	Z25	DBL-0	+DDC Bus 1 Bit 0
−DDC Bus 0 Bit 1	DBOH-1	Y09	D08	→	J07	Z06	DBL-1	−DDC Bus 1 Bit 1
+DDC Bus 0 Bit 1	DBOH-1	Y29	D09	→	J06	Z26	DBL-1	+DDC Bus 1 Bit 1
−DDC Bus 0 Bit 2	DBOH-2	Y10	B09	→	G11	Z07	DBL-2	−DDC Bus 1 Bit 2
+DDC Bus 0 Bit 2	DBOH-2	Y30	B10	→	G06	Z27	DBL-2	+DDC Bus 1 Bit 2
−DDC Bus 0 Bit 3	DBOH-3	Y11	D10	→	G07	Z08	DBL-3	−DDC Bus 1 Bit 3
+DDC Bus 0 Bit 3	DBOH-3	Y31	D11	→	G08	Z28	DBL-3	+DDC Bus 1 Bit 3
−DDC Bus 0 Bit 4	DBOH-4	Y12	B13	→	J08	Z09	DBL-4	−DDC Bus 1 Bit 4
+DDC Bus 0 Bit 4	DBOH-4	Y32	B12	→	J09	Z29	DBL-4	+DDC Bus 1 Bit 4
−DDC Bus 0 Bit 5	DBOH-5	Y13	D12	→	G09	Z10	DBL-5	−DDC Bus 1 Bit 5
+DDC Bus 0 Bit 5	DBOH-5	Y33	D13	→	G10	Z30	DBL-5	+DDC Bus 1 Bit 5
−DDC Bus 0 Bit 6	DBOH-6	Z02	J03	→	J10	Z11	DBL-6	−DDC Bus 1 Bit 6
+DDC Bus 0 Bit 6	DBOH-6	Z22	J02	→	J11	Z31	DBL-6	+DDC Bus 1 Bit 6
−DDC Bus 0 Bit 7	DBOH-7	Z03	G02	→	G13	Z12	DBL-7	−DDC Bus 1 Bit 7
+DDC Bus 0 Bit 7	DBOH-7	Z23	G03	→	G12	Z32	DBL-7	+DDC Bus 1 Bit 7
−DDC Bus 0 Bit P	DBOH-P	Z04	J05	→	J12	Z13	DBL-P	−DDC Bus 1 Bit P
+DDC Bus 0 Bit P	DBOH-P	Z24	J04	→	J13	Z33	DBL-P	+DDC Bus 1 Bit P
−Tag Out Bit 0	DTO-0	Y02	D03	→	D07	Y05	DTI-0	−Tag In Bit 1
+Tag Out Bit 0	DTO-0	Y22	D02	→	D06	Y25	DTI-0	+Tag In Bit 1
−Tag Out Bit 1	DTO-1	Y03	B02	→	B04	Y06	DTI-1	−Tag In Bit 0
+Tag Out Bit 1	DTO-1	Y23	B03	→	B05	Y26	DTI-1	+Tag In Bit 0
−Tag Out Bit 2	DTO-2	Y04	D05	→	B11	Y07	DTI-3	−Connection Ck AL
+Tag Out Bit 2	DTO-2	Y24	D04	→	B06	Y27	DTI-3	+Connection Chk AL

IML 32

DDC Clock Check: Is generated when bits 3 and 4 of the transfer error status (XES) register are active after a machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)P2 40%
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML 38

Data Overrun/DDC Bus In PC/DDC Card Chk/DDC Sync In Chk: Is caused by either bit 0, 2, 4, or 5 of the transfer error status (XES) register failing to reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 70%
01A-B4(B3)J2 20%
01A-B4(B3)V2
01A-B4(B3)R2
01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

IML 3D

DCT Card Check: Is generated when bit 1 of the check register is active after a machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)V2
01A-B4(B3)D2
01A-B4(B3)J2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML A5

Fail To Latch First Sync In: Is generated when bit 6 of the transfer control status (XCS) register fails to activate and deactivate at the correct time during an IML operation.

Bit 6 is activated by the Diagnostic Sync In and Run Device lines activating. When the microprocessor senses that bit 6 is active, it deactivates the run device line, which then deactivates bit 6.

If bit 6 is not as expected when tested, the IML operation is ended and IML A5 is generated.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)R2 50%
01A-B4(B3)J2 20%
01A-B4(B3)X2
01A-B4(B3)K2
01A-B4(B3)N2
01A-B4(B3)M2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML A7

DDC End of Transfer Not Set/Reset: Is caused by bit 2 of the transfer control status (XCS) register failing to activate or deactivate at the proper time.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)R2 50%
01A-B4(B3)J2 20%
01A-B4(B3)X2 10%
01A-B4(B3)V2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML A8

DDC Card Check After a Buffer to DBO Transfer: Is caused by XES register bit 4 staying on after a data transfer operation.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2
01A-B4(B3)H2
01A-B4(B3)N2
01A-B4(B3)V2
01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)G2
01A-B4(B3)P2
01A-B4(B3)Q2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

IML AA

First Sync In Missing (DBI Reg to ADT Buffer): Is generated when XCS bit 6 is not active after a data transfer operation between the device bus in and the automatic data transfer control (ADT) buffer.

Card detecting the error:

01A-B4(B3)XX

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)J2 40%
01A-B4(B3)M2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML B4

DCT Card Check: Indicates that a device counter (DCT) card check occurred during a device buffer in bus to buffer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)V2
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML B5

DDC Card Check: Indicates that a director-to-controller (DDC) card check occurred during a device bus in (DBI) buffer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML BA

DCT Card Check Not Set or Reset: Indicates that bit 1 of the check register cannot be set or reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)V2
01A-B4(B3)J2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

IML C3

Data Overrun Check or DDC Card Check Not Set or Reset: Is generated when one of the following occurs:

- Bit 0 of the transfer error status (XES) register fails to set when the buffer is empty and one more byte is fetched from the buffer during a manual read operation.
- Bit 0 of the transfer error status (XES) register fails to set when the buffer is full and one more byte is transferred to the buffer during a write operation.
- A check reset fails to reset transfer error status (XES) bit 0.
- Bit 0 of the transfer error status (XES) register either fails to set or reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2
01A-B4(B3)R2
01A-B4(B3)J2
01A-B4(B3)V2
01A-B4(B3)F2
01A-B4(B3)D2

Diagnostic Check

Refer to Diagnostic Check 1 on page CTL-I 30.

IML C5

Sync In Check: Is generated when bit 5 of the transfer error status (XES) register fails to activate after a diagnostic sync in or fails to deactivate after a check 2 error reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 30%
01A-B4(B3)P2 20%
01A-B4(B3)J2 10%
01A-B4(B3)R2 10%
01A-B4(B3)V2
01A-B4(B3)N2
01A-B4(B3)M2

Diagnostic Check

Refer to Diagnostic Check 1 on page CTL-I 30.

SC 2004

Sync In Check: Is caused by a solid or unexpected sync in signal from the device.

The sync in check causes a hardware detected error during normal customer operation. The code is displayed in environmental recording, editing, and printing (EREP) or interpreted by the maintenance device (MD) as a sync in check error.

Card detecting the error:

01A-B4(B3)X2

FRU List

01A-B4(B3)X2 30%
01A-B4(B3)P2 20%
01A-B4(B3)R2 10%
01A-B4(B3)V2
01A-B4(B3)J2
Attached Device

Diagnostic Check

Refer to Diagnostic Check 1 on page CTL-I 30.

SC 2008

DDC Card Check: Is caused by:

- Incorrect parity detected in the device tag gate, device tag out, or the device bus out registers on the director-to-device controller (DDC) card
- The Take Data and Data Taken lines not activating and deactivating once for each data transfer cycle
- A clock check detected

Card detecting the error:

01A-B4(B3)X2

FRU List

01A-B4(B3)X2 70%
01A-B4(B3)K2
01A-B4(B3)V2
01A-B4(B3)G2
01A-B4(B3)P2
01A-B4(B3)J2
01A-B4(B3)R2
01A-B4(B3)Q2
01A-B4(B3)H2
Attached Device

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 2018

DDC Clock Check: Indicates that a clock check was detected on the director-to-device controller (DDC) card. The clock check circuits check for extra or missing pulses on the DDC clock lines. The -Clock Check Two line sets bit 3 (clock check 2) and bit 4 (DDC card check) of the XES register. Bit 4 indicates that the DDC card detected the error.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)P2 40%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 2020

DDC BUS In Parity Check: Is active when incorrect parity is detected on the device bus in lines. Bit 2 of the transfer error status (XES) register is active.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 80%
01A-B4(B3)P2 10%
01A-B4(B3)V2 10%
01A-B4(B3)R2
Attached Device

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 2080

Data Overrun Check: Is active when errors are detected on the data transfer bus lines; this can be caused by a read/write failure or control storage overrun. Checks are made to ensure the read/write circuits are ready to accept a byte of data from the DDC card when the Take Data line is active. A check is made to ensure that a byte of data is present on the DXR bus in lines at the time the device bus out register is loaded.

Bit 0 of the XES register is set by the data overrun check.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 70%
01A-B4(B3)V2 10%
01A-B4(B3)P2 10%
01A-B4(B3)N2
01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)G2
Attached Device

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 20F0

Device Overrun: Indicates that the channel was degated and the subsystem storage was performing a write operation to the device. Subsystem storage could not load data into the ADT buffer as rapidly as the device required data. This can be caused by a hang of the Port controls or the ADT.

Bit 0 of the XES register is set by the data overrun check.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 70%
01A-B4(B3)V2 10%
01A-B4(B3)P2 10%
01A-B4(B3)N2
01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)G2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 2540

DCT Card Check: Is active when a parity error is detected in any of the device counter (DCT) card registers and activates bit 1 in the check register on the automatic data transfer (ADT) card.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)V2 80%
01A-B4(B3)J2 10%
01A-B4(B3)X2
01A-B4(B3)K2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30.

SC 2801

The 3880 functional microcode detected an unexpected end. The device ended data transfer early.

Card detecting the error:

NONE

FRU List

01A-B4(B3)X2 60%
01A-B4(B3)V2 20%
01A-B4(B3)P2 10%
01A-B4(B3)K2 10%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 2 on page CTL-I 30.

Symptom Codes

SC 2802

The 3880 functional microcode detected that the device selection was lost during a control interface operation with error alert up.

Note: These error codes are further defined by sense byte 20. See SENSE section in the Maintenance Support Manual (MSM) for a further description of sense byte 20.

Card detecting the error:

NONE

FRU List

01A-B4(B3)X2 70% Attached device
01A-B4(B3)V2 10%
01A-B4(B3)P2 10%

Diagnostic Check

Refer to Diagnostic Check 2 on page CTL-I 30.

SC 2810

Tag Sequence Error: Occurs when the device detects a tag out sequence error.

Card detecting the error:

01A-B4(B3)X2

FRU List

01A-B4(B3)X2 80%
Attached Device

Diagnostic Check

Refer to Diagnostic Check 4 on page CTL-I 30.

SC 2820

Device Detected Bus Out Parity Error: Occurs when the device detects a tag out parity error. When in one-byte mode, the parity error is on the DDC Bus Out Bit 0 lines. When in two-byte mode, the parity error is on the DDC Bus Out 0 or 1 lines.

Card detecting the error:

01A-B4(B3)X2

FRU List

01A-B4(B3)X2 80%
Attached Device

Diagnostic Check

Refer to Diagnostic Check 2 on page CTL-I 30.

SC 292A

Fail To Latch First Sync In: Is generated when all of the following conditions are present:

- The read/write operation is complete.
- XCS register bit 2 is active.
- XCS register bit 6 is not active.

  The output of the first sync-in latch on the director-to-device controller (DDC) card activates bit 6 of the XCS register on the ADT cards. When the microprocessor senses that bit 6 is active, it can begin processing skip-defect and record-address information as the read/write operation continues.

  At the end of the read/write operation, XCS bit 2 (DDC end of transfer) is activated. If XCS bit 6 is not active, symptom code 292A is generated.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 50% Attached Device
01A-B4(B3)K2 20%

Diagnostic Check

Refer to Diagnostic Check 3 on page CTL-I 30

Diagnostic Check 1

Execute the following diagnostic and scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses. To find the nets use the LRM, Volume R70, and reference INTRO 10 in this manual for the LRM page.

- Bypass any IML error halt (see the MD section in the MSM).
- Select and load diagnostic routine 70.
- Select and loop function test '1A'.

Note: See the DC section in this manual for a description of routine 70 test '1A'.

Diagnostic Check 2

Execute the following diagnostic and scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses. To find the nets use the LRM, Volume R70, and reference INTRO 10 in this manual for the LRM page.

- Bypass any IML error halt (see the MD section in the MSM).
- Select and load diagnostic routine 71.
- Select and loop test '07'.

Note: See the DC section in this manual for a description of routine 71 test '07'.

Diagnostic Check 3

Execute the following diagnostic and scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses. To find the nets use the LRM, Volume R70, and reference INTRO 10 in this manual for the LRM page.

- Bypass any IML error halt (see the MD section in the MSM).
- Select and load diagnostic routine 70.
- Select and loop function test '15'.

Note: See the DC section in this manual for a description of routine 70 test '15'.

Diagnostic Check 4

1. Power off the failing storage director. Remove all cards shown in the FRU list and check all nets with a multimeter. Check and repair open or short circuits between nets, grounds, or voltage pins.
2. Place the failing storage director in an IML loop (see PDA section). Scope all nets on the cards indicated in the FRU list and check for incorrect levels or misshapen pulses. While looping the IML failure, check for differences between the input and output pins.
3. Execute the following diagnostic and scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses.

   Bypass any IML error halt (see the MD section in the MSM).

   Select and load diagnostic routine 71.

   Select and loop test '07'.

   Note: See the DC section in this manual for a description of routine 71 test '07'.

Diagnostic Checks CTL-I 30

Contents of This Section

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
00-1	10	1	C15
00-2	10	1	C15
01-1	10	1	C15
01-2	15	1	C17
02-1	15	1	C17
03-1	15	1	C17
04-1	15	1	C17
05-1	15	1	C17
06-1	15	1	C17
06-2	15	1	C17
0A	15	1	C17
10-1	20	1	D01
10-2	20	1	D01
11-1	20	1	D01
11-2	20	1	D01
12-1	15	1	C17
13-1	15	1	C17
14-1	15	1	C17
15-1	15	1	C17
16-1	15	1	C17
16-2	15	1	C17
40-1	20	1	D01
42-1	15	1	C17
43-1	15	1	C17
44-1	15	1	C17
45-1	15	1	C17
46-1	15	1	C17
46-2	15	1	C17
CE	20	1	D01
CF	20	1	D01
0100	25	1	D03
0200	25	1	D03
0300	25	1	D03
0301	25	1	D03
0302	25	1	D03
0303	25	1	D03
0304	25	1	D03
0305	25	1	D03
0306	25	1	D03
0307	25	1	D03

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
0400-1	30	1	D05
0400-2	30	1	D05
0401-1	30	1	D05
0401-2	30	1	D05
0402-1	30	1	D05
0402-2	30	1	D05
0403-1	30	1	D05
0403-2	30	1	D05
0404-1	30	1	D05
0404-2	30	1	D05
0405	30	1	D05
0406-1	30	1	D05
0406-2	30	1	D05
0500-1	30	1	D05
0500-2	30	1	D05
0501-1	30	1	D05
0501-2	30	1	D05
0502	35	1	D07
0503	35	1	D05
0507	35	1	D07
0600-1	35	1	D07
0600-2	35	1	D07
0601-1	35	1	D07
0601-2	35	1	D07
0602-1	35	1	D07
0602-2	35	1	D07
0603-1	35	1	D07
0603-2	35	1	D07
0604	35	1	D07
0605-1	35	1	D07
0605-2	35	1	D07
0606-1	35	1	D07
0606-2	35	1	D07
0700	40	1	D09
0701	40	1	D09
0702	40	1	D09
0703	40	1	D09
0704	40	1	D09
0705	40	1	D09
0706	40	1	D09
0800	45	1	D11
0801	45	1	D11
0802	45	1	D11

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
0803	45	1	D11
0804	45	1	D11
0805	45	1	D11
0805	45	1	D11
0806	45	1	D11
0900	45	1	D11
0901	45	1	D11
0902	45	1	D11
0903	45	1	D11
0904	45	1	D11
0905	45	1	D11
0906	45	1	D11
3000	50	1	D13
3001	50	1	D13
3003	50	1	D13
3011	50	1	D13
3012	50	1	D13
3013	50	1	D13
3014	50	1	D13
3015	50	1	D13
3016	50	1	D13
3102	55	1	D15
3210	55	1	D15
3280	55	1	D15
F011	50	1	D13
F012	50	1	D13
F013	50	1	D13
F014	50	1	D13
F015	50	1	D13
F016	50	1	D13

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

See the SENSE section in the MSM for a description of the check conditions.

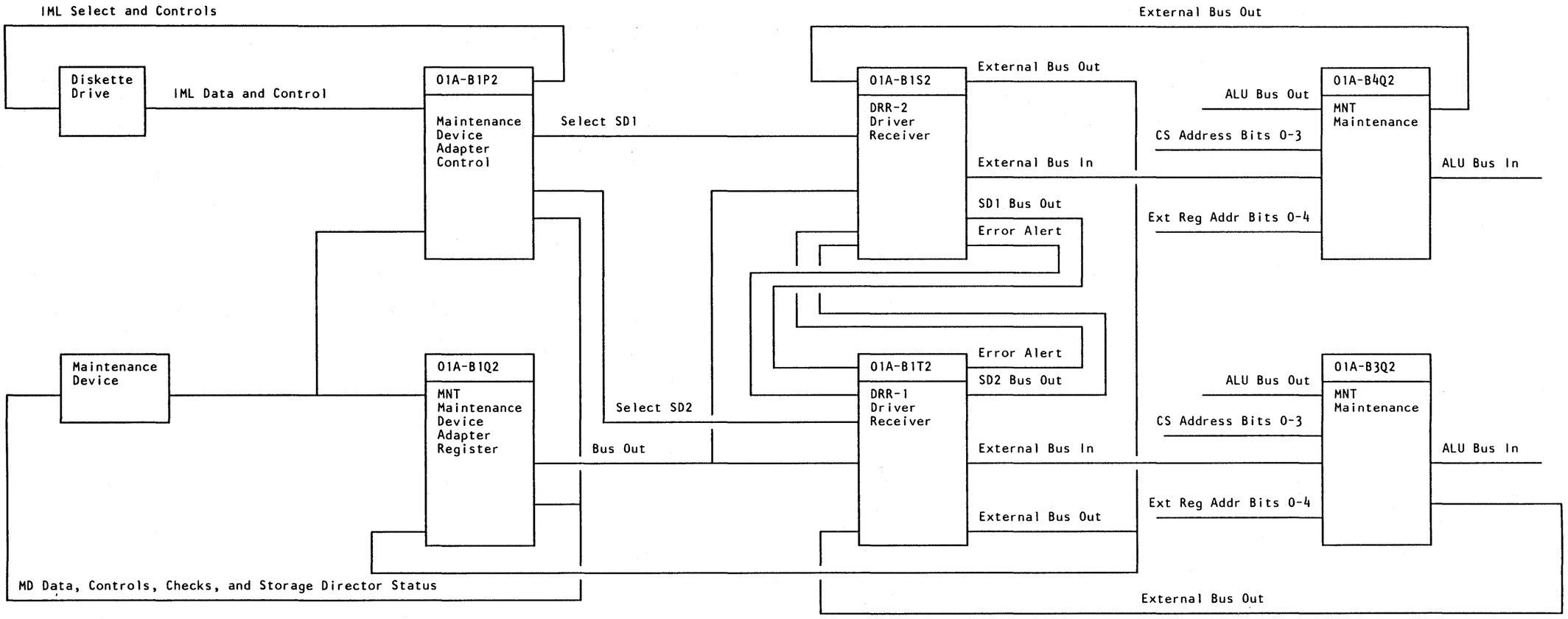
See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Error Code Diagram

IML read/write serialized data from the diskette flows through the maintenance board to the storage directors. The diagram on this page shows the cards involved in the data flow.

Note: For FRUs not shown on this diagram refer to the functional area of that FRU in the OPER section in the MSM.

For a description of the maintenance area see the OPER section.



3880 ECM							
	Seq HK0001	PN 6315688 2 of 13	881145 13 Jan 84	881216 15 Aug 84	A15621 01 Apr 85		

IML Error Codes

IML 00-1

IML Failed to Start (One SD Only): The external bus out (EBO) register is reset by a power on reset (POR) or the start of an IML operation. An IML code of 00-1 means:

- The read-only storage (ROS) did not select.
- The clocks did not start.
- The microprocessor did not start.
- The EBO register did not load.

An error in the 3880 channel interface hardware causes the 3880 controller to stop.

ROS Did Not Select

The ROS select signal from the device counter card starts the execution of the ROS tests. ROS select is bit 1 of the maintenance control/sense (MCS) register.

MCS bit 1 is activated by the +Start DXR Clock line from the maintenance card. The +Start DXR Clock line is activated by a POR or an IML command.

These failures cause the +ROS select signal to remain inactive.

- +Start DXR Clock signal is inactive
- +Reset line is active preventing the MCS register bit 1 to reset.
- +Power On Reset (SD1 or SD2) line not activating or staying active after a POR.

  Note: An IML command from the maintenance device should cause an IML even if the +Power On Reset (SD1 or SD2) line is open. However, the IML may not be successfully completed because some registers do not reset.

Clocks Did Not Start

The power on reset stops the clock ring on the clock card. After the power on reset operation is completed the clock ring starts and the clocks are gated to the dynamic refresh control, automatic data transfer, and the maintenance cards.

The +Start line from the maintenance card gates the clocks to the director to device controller, device counter, channel interface, channel data transfer, and storage director microprocessor cards.

The first start DXR latch (set just prior to the +Start DXR Clock line activating) sets the IML-to-cycle-share latch on the maintenance card. The latch output is wrapped back into the maintenance card and sets the start latch at T5 time.

Some of the failures that can prevent the clocks from starting are:

- The clock ring fails to start.
- The maintenance card clocks fail to start.
- The +Hold SDM line from the dynamic refresh control card stops the clocks on the storage director microprocessor card.

Microprocessor Did Not Start

Two control lines to the storage director microprocessor card can prevent the microprocessor from executing instructions. They are:

- - Reset
- - SDM Start Delayed

If either line is constantly active, it can cause this failure.

EBO Register Did Not Load

As each ROS test begins to execute, it loads a test number into the EBO register from the ALU bus out lines. One of the following conditions can cause the EBO register to load incorrectly:

- The microprocessor does not put the proper address on the external register address bus.
- The +Ld Ext Reg Clk D line to the maintenance card is open or held inactive.

The maintenance device adapter test detects most of the EBO register failures by checking the external bus out and bus in lines. These tests are run automatically as soon as the maintenance device is attached to the 3880. If the microprocessor is unable to load the EBO register the maintenance device cannot read the sense bytes from an inline diagnostic.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2
01A-B4(B3)P2
01A-B4(B3)U2
01A-B4(B3)V2
01A-B4(B3)N2
01A-B1P2
01A-B1Q2
01A-B1S2
01A-B1T2
01A-B4(B3)Q2
01A-B1E2,
01A-B4(B3)F2
CIFA 2X
CIFB 4X
01A-B4(B3)C2
SWITCH 101

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 00-2

IML 00-2: Occurs when open or shorted power-on reset lines prevent the start of an IML operation. A power-on reset starts the IML operation on both storage directors. If the power-on reset lines are open or shorted to a plus or minus level, the IML operation is not started.

Card detecting the error:

NONE

FRU List

01A-B1E2 90%
01A-B1C2
01A-B1P2

Diagnostic Check

- Scope the power-on reset lines (01A-B4(B3)Q2) by using the Power On switch on the operator panel.
- Power off the failing storage director and remove all cards associated with the power on reset lines. Check the nets associated with the power on reset lines for an open, a short between nets, or a short between a net pin and ground, or a voltage.

IML 01-1

IML 01-1: Occurs when one of several conditions prevents either storage director from selecting the diskette drive. They are:

1. The +Diskette Drive Request (SD1 or SD2) lines are grounded or shorted to a minus-level signal in the W top-card connector cable from the maintenance card.
2. The -Diskette Drive Request (A or B) lines are floating or shorted to a plus-level signal line in the board wiring to the maintenance device adapter control card.
3. The +Diskette Drive Selected (SD1 or SD2) or the +(SD1 or 2) Selected lines are grounded in the X top-card connector cable to the maintenance card.
4. The -Diskette Drive Select (SD1 or SD2) or the -Select (SD1 or SD2) lines are floating or shorted to a plus-level signal line in the board wiring from the maintenance device adapter control card.
5. The +Diskette Drive Busy (SD1 or SD2) lines are floating or shorted to a plus-level signal in the X top-card connector cable to the maintenance card.
6. The -Diskette Drive Busy (1 or 2) lines are grounded in the board wiring from the maintenance device adapter control card.
7. The +Mnt Clock T6 line is intermittently grounded in the board wiring from the clock card.

   Note: A +Mnt Clock T6 line that is constantly active causes a maintenance clock check (SC 3102).

Card detecting the error:

NONE

FRU List

01A-B1P2 40%
01A-B4(B3)R2 30%
01A-B1S2
01A-B1T2
01A-B1Q2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 01-2

IML 01-2: Occurs when one of several conditions prevents both storage directors from selecting the diskette drive.

Refer to IML code 01-1 for the conditions that can cause this failure.

Card detecting the error:

NONE

FRU List

01A-B1P2 70%
01A-B1Q2 30%

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 02-1, 12-1, or 42-1

Waiting for Index (One SD Only): These codes are generated if the +Diskette Drive Index line is inactive when the index on the diskette is sensed.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 40%	01A-B1T2
01A-B1P2 30%	01A-B4(B3)P2
01A-B1S2	File Control Card

Diagnostic Check

If the +Diskette Drive Index line 01A-B1S2(T2) is constantly active, check for the following:

- The +Diskette Drive Index line is shorted to ground or to a minus-level signal line in the W top-card connector cable to the maintenance card.
- The -File Index line is shorted to ground or to a minus-level signal line in the board wiring from the maintenance device adapter control card.

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 03-1, 13-1, or 43-1

Waiting for Index (One SD Only): These codes are generated if the +Diskette Drive Index line is inactive when the index on the diskette is sensed.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 30%	01A-B1Q2
01A-B4(B3)P2 30%	File Ctrl Cd
01A-B4(B3)Q2	01A-B1S2
01A-B1P2	01A-B1T2

Diagnostic Check

If the +Diskette Drive Index line 01A-B1S2(T2) is constantly inactive, check for the following:

- The +Diskette Drive Index line is floating or shorted to a plus-level signal line in the W top-card connector cable to the maintenance card.
- The -File Index line is floating or shorted to a plus-level signal line in the board wiring to the maintenance device adapter control card.

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 04-1, 05-1, 14-1, 15-1, 44-1, or 45-1

No Sync Or Clock Pulses (One SD): These IML codes are generated if the diskette drive index pulse is present and if the clock, sync, or data pulses are missing.

Diskette drive clock pulses occur every 4 microseconds and define the period when sync or data pulses can be present. When the storage director microprocessor card receives the index and clock pulses, it waits for the sync pulses. (The sync pulse is the first data pulse after the index pulse and identifies the start of a record.)

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 50%	01A-B1P2
01A-B4(B3)P2 10%	File Control Card
01A-B1S2	Diskette
01A-B1T2	

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IML 06-1, 16-1, or 46-1

Microcode Load Does Not Complete (One SD): Generated when a storage director fails to read data from the diskette drive.

The diskette drive receives index, clock, and sync pulses at the start of the IML operation, but cannot read a data record. A time-out occurs on the maintenance device adapter control card, stopping the IML operation.

Card detecting the error:

NONE

FRU List

A-B4(B3)R2 60%	01A-B4(B3)P2 10%
01A-B1S2 30% SD1 only	01A-B1P2
01A-B1T2 30% SD2 only	Diskette

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

Note: A solid failure can cause IML 04-1 or 05-1 when the IML operation is re-tried.

IML 06-2, 16-2, 46-2

Microcode Load Does Not Complete (Both SDs): Generated when a time-out occurs on the maintenance device adapter control card without the read-only storage (ROS) code detecting an invalid track ID, a data check, or an access error while the diskette is reading track zero.

Card detecting the error:

NONE

FRU List

01A-B1P2 30%
01A-B1Q2 30%
Diskette

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

Note: A solid time-out failure causes IML 01-20.

IML 0A

IML 0A: Is generated when the microprocessor branches improperly from the overlay loader area of control storage.

The instructions for the overlay loader area of control storage are data on the 3880 diskette. A parity error, when the data is being read from the diskette or written into control storage, causes other error codes.

Card detecting the error:

NONE

FRU List

Diskette 90%	01A-B4(B3)R2
01A-B4(B3)Q2	

Diagnostic Check

There is no diagnostic check for this error, replace the diskette.

IML Error Codes

IML 10-1 or 10-2

IML 10-1 and 10-2: Are generated when the overlay loader program senses a diskette drive busy signal during the diskette drive selection operation on both storage directors.

Card detecting the error:

NONE

FRU List 10-1:

01A-B1P2 60%
01A-B4(B3)R2 30%
01A-B1S2 SD1 only
01A-B1T2 SD2 only

FRU List 10-2:

01A-B1P2 90%

Diagnostic Check

- Scope the diskette drive busy lines 01A-B1P2.
- Power off the failing storage director and remove all cards shown in the FRU list. Check all nets for an open, a short between nets, or a short between a net pin and ground, or a voltage.

IML 11-1 or 11-2

IML 11-1 or 11-2: Is generated when the diskette drive select signal is lost between the read-only storage (ROS) controlled drive selection and the overlay loader program selection.

Card detecting the error:

NONE

FRU List 11-1

01A-B1P2 40%
01A-B4(B3)R2 30%
01A-B1Q2
01A-B4(B3) P2
01A-B1S2
01A-B1T2

FRU List 11-2

01A-B1P2 70%
01A-B1Q2 10%

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

Note: If the failure is solid and another IML operation is attempted, the error code will change to either 01-1 (see MNT-C-70) or 01-2 (see MNT-C-90). An intermittent failure can also cause these error codes.

IML 40-1

IML 40-1: Is caused by a mismatch on one storage director between a track identification on the 3880 diskette and the diskette load control switches on the maintenance (MNT) card.

The contents of the load control switches are loaded into bits 5 through 7 of the IML register. (See the INST section in the Maintenance Information Manual for a description of the 3880 diskette load control switches.) The microprocessor uses these bits to select the correct diskette track for the storage director at IML time.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 90%
Maintsw
Diskette

Diagnostic Check

Check the following problem areas for:

- Diskette load control switches that are improperly set on the MNT card
- A defective MNT card
- A defective 3880 diskette

IML CE

IML CE: Is caused by one of two conditions:

- The timer did not overflow as expected.
- The timer caused an interrupt when disabled.

Card detecting the error:

NONE

FRU List

01A-B4(B3)P2 60%
01A-B4(B3)V2 30%

Diagnostic Check

Perform these steps:

1. If the timer did not overflow, sync on the -Chan Check/Timer Interrupt 1 line 01A-B4(B3)P2 and check this line for a short to a minus level or ground.
2. If the timer produces an interrupt pulse when the +Enable Timer line is minus, check for an open line.

IML CF

IML CF: Occurs when the timer overflowed but the time was not within the 650.0 ms +30% to -20% tolerance.

Card detecting the error:

NONE

FRU List

01A-B4(B3)P2 60%
01A-B4(B3)V2 30%

Diagnostic Check

If the timer is out of tolerance, check the +Enable Timer line 01A-B4(B3)V2 for extra minus pulses after it is initially activated.

Note: The channel sequence control card should be replaced to ensure that an intermittent channel check is not occurring. Loop hardcore test 12. This test should detect a continuously active bit with an IML 9C error.

IC 0100, 0305, 0306

IC 0100, 0305, 0306: Are generated when the maintenance device (MD) receives incorrect data from the serializer deserializer (SERDES) card. The MD uses the -MD Shift, -MD Data In, and -MD Data Out lines to shift a pattern of eight bits through the maintenance device adapter control (MDAC) card SERDES and back to the MD where the data is compared.

After the shift test is completed successfully, the -MD Enable Interface line is activated. A control command is sent to the MDA. If there is no response, IC 0100 is also generated.

Possible causes of an IC 0100 error code are:

- Clock stopped
- System activity (frequent system resets)
- Microcode loop
- Contingent connecting (status pending)

Card detecting the error:

NONE

FRU List

PWR	01A-B1C2
01A-B1P2	MD
01A-B1Q2	MD INPUT
01A-B1E2	TO B1V4 CABLE
01A-B4(B3)N2	

Diagnostic Check

Perform the following steps:

1. Check that 01A-B1E2M07 is not grounded (YA105).
2. Observe the operator panel. If the conditions are not normal, correct or use this condition as a symptom for the repair action.
3. Determine if system activity caused the problem.
4. Display the check registers.
5. Check for clock stopped. If it is, try RSD,R (support option 5) and check for an IC 0100 error code.

IC 0200

IC 0200: Is generated when the MD receives an unexpected interrupt from the MDA while opening the MD port. Any one of the following conditions can cause an MDA interrupt:

- SERDES parity check/register select check
- EBO parity check
- EBI parity check
- Alert from a storage director

The Status Out line is activated by one of these checks and causes an MD interrupt.

Card detecting the error:

NONE

FRU List

01A-B1P2	01A-B1T2
01A-B1Q2	MD
01A-B1S2	MD INPUT TO B1V4 CABLE

Diagnostic Check

Refer to Diagnostic Check 2 on page MNT-C 60.

IC 0300, 0301, 0302, 0304, 0305, 0306, 0307

Isolation codes 0300, 0301, 0303, and 0304: Are generated when a failure occurs in the maintenance device adapter (MDA) test. This test:

1. Checks the hardware on the two maintenance device cards that are responsible for processing commands.
2. Checks that the status register bits are capable of being set and reset.

No storage director is selected during this test.

IC 0300

IC 0300: Occurs when the maintenance device (MD) sends a command to the MDA card and does not receive a response in the allotted time.

IC 0301

IC 0301: Indicates that the MD has received an interrupt from the MDA. An MDA interrupt is caused by the same conditions as IC 0200.

IC 0302

IC 0302: Occurs when the MD does not receive a response from the storage director in the allotted time while in the receive mode.

IC 0303

IC 0303: Occurs when an interrupt is received from the MDA while the MD is receiving data from the MDA. An interrupt is caused by the same conditions as IC 0200.

IC 0304

IC 0304: Occurs when data received from the MDA is not as expected, but no parity error is present.

IC 0307

IC 0307: The MD did not receive an interrupt from the MDA cards when the MDA check bits are forced on by a command to the MDA.

Card detecting the error:

NONE

FRU List IC 0300-0304, 0307

01A-B1P2	MD
01A-B1Q2	01A-B1S2
MDIPT	01A-B1T2

Diagnostic Check

Refer to Diagnostic Check 2 on page MNT-C 60.

IC 040x-n

These codes are generated when a failure occurs during the storage director test. An n in the error code indicates that a failure is detected in one storage director but the second storage director cannot be checked. The result is the field-replaceable unit (FRU) group contains all the cards that could fail for both storage directors.

Card detecting the error:

NONE

FRU List IC 040x-n

01A-B4(B3)R2	01A-B1Q2
01A-B1S2	01A-B1E2
01A-B1T2	01A-B1C2
01A-B1P2	01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0400-1 or 0400-2

IC 0400-1: Occurs when the maintenance device (MD) does not receive a response from the selected storage director during the allotted time.

IC 0400-2: Occurs when the MD does not receive a response from both storage directors during the allotted time when in the transmit mode.

IC 0401-1 or 0401-2

IC 0401-1: Occurs when an interrupt is received by the MD during a transmit mode to the selected storage director.

IC 0401-2: Occurs when the MD receives an interrupt during a transmit mode from both storage directors.

The interrupts are caused by:

- SERDES parity check/register select check
- EBO parity check
- EBI parity check
- Alert from a storage director

IC 0402-1 or 0402-2

IC 0402-1: Occurs when the MD does not receive a response from the selected storage director in the allotted time while in receive mode.

IC 0402-2: Occurs when the MD does not receive a response from both storage directors in the allotted time while in receive mode.

IC 0403-1 or 0403-2

IC 0403-1: Occurs when the MD receives an interrupt during a receive mode from a storage director.

IC 0403-2: Occurs when the MD receives an interrupt during a receive mode from both storage directors.

An interrupt is caused by the same conditions as IC codes 0401-1 and 0401-2.

IC 0404-1 or 0404-2

IC 0404-1: Occurs when incorrect data is received from a single storage director during the storage director select test.

IC 0404-2: Occurs when incorrect data is received from both storage directors during the storage director select test.

IC 0405

IC 0405: Occurs when a MDA hardware check is detected during the storage director select test. This failure is an OR of bits 1, 2, and 3 of the MDA check register. The bit failures are:

Bit 1, Shift counter check, or IML counter overflow check.

Bit 2, Clock check, multiple decode check, 5 microsecond delay counter check, multiple IML, or storage director select check.

Bit 3, Command register parity check.

IC 0406-1 or 0406-2

IC 0406-1: Occurs when the MD does not receive a response from the storage director (a timeout occurred).

IC 0406-2: Occurs when the MD does not receive a response from the storage director (a timeout occurred).

IC 0500-1 or 0500-2

IC 0500-1 or 0500-2: Occurs when the IML operation fails to start when a command is issued from the maintenance device or by a power on reset.

Card detecting the error:

NONE

FRU List IC 0500-1:

01A-B4(B3)R2	01A-B1S2 SD1 only
01A-B4(B3)P2	01A-B1T2 SD2 only
01A-B4(B3)V2	01A-B1E2
01A-B4(B3)Q2	01A-B1Q2
	01A-B1P2
	SWITCH 101

FRU List IC 0500-2:

01A-B1E2
01A-B1P2
01A-B1Q2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 0501-1

IC 0501-1: Occurs when a maintenance device (MD) initiated IML to a storage director fails to start, but an IML initiated by a power on reset is successful.

This isolation code indicates that the failing storage director cannot decode an MD generated IML command. A power on reset IML does not require a command decode.

Card detecting the error:

NONE

FRU List

01A-B1P2	01A-B1S2 SD1 only
01A-B1Q2	01A-B1T2 SD2 only
01A-B4(B3)R2	

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 0501-2

IC 0501-2: Occurs when the MD cannot initiate an IML to either storage director but both storage directors can initiate an IML by a power on reset.

Card detecting the error:

NONE

FRU List

01A-B1S2	01A-B1Q2
01A-B1T2	01A-B4(B3)R2
01A-B1P2	

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 0502

IC 0502: Occurs when the MD receives an interrupt from the maintenance device adapter (MDA) while initiating an IML.

An interrupt is caused by:

- SERDES parity check/register select check

Card detecting the error:

NONE

FRU List

01A-B1P2 01A-B4(B3)R2
01A-B1Q2 01A-B4(B3)P2
01A-B1S2 01A-B4(B3)Q2
01A-B1T2 01A-B4(B3)N2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 0503

IC 0503: Occurs when the MD receives an interrupt from a storage director while initiating an IML.

An interrupt is caused by:

- EBO parity check
- EBI parity check
- Alert from a storage director

Card detecting the error:

NONE

FRU List

01A-B1S2 SD1 only 01A-B1P2
01A-B1T2 SD2 only 01A-B4(B3)P2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 0507

IC 0507: Occurs when the IML operation intermittently fails to start.

Card detecting the error:

NONE

FRU List

01A-B1E2
01A-B1P2
01A-B1Q2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

IC 060x-n

IC 060x-n: Isolation codes are generated when a failure occurs in the maintenance connection test. An n in the error code indicates that a failure is detected in one storage director but the second storage director cannot be checked. The result is the field-replaceable unit (FRU) group containing all the cards that could fail for both storage directors. This test sends a command followed by two bytes of data (AA and 55) to the storage director. The storage director sends the data back to the maintenance device (MD), where the data is compared with the data sent to the storage director.

Card detecting the error:

NONE

FRU List IC 060x-n

01A-B4(B3)R2 01A-B1Q2
01A-B1S2 01A-B1E2
01A-B1T2 01A-B1C2
01A-B1P2 01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 4 on page MNT-C 60.

IC 0600-1 or 0600-2

IC 0600-1: Occurs when the MD does not receive a response in the allotted time while sending a command or data to a storage director.

IC 0600-2: Occurs when the MD does not receive a response in the allotted time while sending a command or data to either storage director.

IC 0601-1 or 0601-2

IC 0601-1: Occurs when the MD receives an interrupt during a transmit mode to a storage director.

IC 0601-2: Occurs when the MD receives an interrupt during a transmit mode to either storage director.

An interrupt is caused by the same conditions as IC 0200.

IC 0602-1 or 0602-2

IC 0602-1: Occurs when the MD does not receive a response in the allotted time from a storage director during a receive mode.

IC 0602-2: Occurs when the MD does not receive a response in the allotted time from either storage director during a receive mode.

IC 0603-1 or 0603-2

603-1: Occurs when the MD receives an interrupt while receiving data from a storage director.

IC 0603-2: Occurs when the MD receives an interrupt while receiving data from both storage directors.

An interrupt is caused by the same conditions as IC 0200.

IC 0604

IC 0604: Occurs when the data received from the maintenance device adapter (MDA) does not compare with data sent during the maintenance connection test.

IC 0605-1 or 0605-2

IC 0605-1: Occurs when the data received from a storage director does not compare with data sent.

IC 0605-2: Occurs when the data received from both storage directors does not compare with the data sent.

IC 0606-1 or 0606-2

IC 0606-1: Occurs when the MD does not receive a response from the storage director (a timeout occurred).

IC 0606-2: Occurs when the MD does not receive a response from the storage director (a timeout occurred).

Isolation Codes

IC 070x

IC 070x: Isolation codes are generated when one of the following tests isolates a failure to the channel interface:

- IML
- Maintenance connection test
- Storage director select test

IC 0700

IC 0700: Occurs when a failure is isolated on a single channel storage director.

Card detecting the error:

NONE

FRU List

CIFA
01A-B4(B3)P2
CIF address switches set incorrectly

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0701

IC 0701: Occurs when a failure is isolated on a two channel storage director.

Card detecting the error:

NONE

FRU List

CIFA,B	01A-B4(B3)G2
01A-B4(B3)F2	01A-B4(B3)C2
01A-B4(B3)P2	CIF address switches set incorrectly

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0702

IC 0702: Occurs when a failure is isolated to the channel A or B interface area on a four channel storage director.

Card detecting the error:

NONE

FRU List

CIFA,B	01A-B4(B3)D2
01A-A4(A3)P2	01A-A4(A3)N2
01A-B4(B3)E2	CIF address switches set incorrectly
01A-B4(B3)C2	

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0703

IC 0703: Occurs when a failure is isolated to the channel C or D area on a four channel storage director.

Card detecting the error:

NONE

FRU List

CIFC,D	01A-B4(B3)C2
01A-A4(A3)G2	01A-A4(A3)N2
01A-B4(B3)D2	01A-B4(B3)G2
01A-B4(B3)E2	CIF address switches set incorrectly

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0704

IC 0704: Indicates a failure during the support CE test. This test checks the address compare (ACR) logic in the maintenance interface.

The support CE test insures that the ACR sync and ACR stop function are operative. This test uses a sampling of addresses that exercise the address bits. The following sequence of events occur during the test:

1. A loop of nine addresses is set up.
2. The contents of the tested address locations are saved.
3. The nine addresses are loaded with branch instructions.
4. The instruction address register (IAR) is set to the starting address.
5. The ACR is set to the stopping address.
6. The ACR stop is set and the clock is started.
7. The MD waits until the instruction is complete. The MD then checks the maintenance device adapter (MDA) status register for address compare successful and the storage director check register to ensure that the clocks are stopped.
8. The MD resets the IAR and the ACR to the next two addresses and repeats the loop.

This sequence is repeated until all the addresses in the loop are tested.

Three of the loops are set and exercised during the support CE test. This test verifies that the bits in the ACR and IAR are valid. This test checks the capability of fetching and storing from the MD.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2	01A-B1Q2
01A-B1S2 (SD1) only	01A-B1P2
01A-B1T2 (SD2) only	

Diagnostic Check

Scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses.

IC 0705

IC 0705: Occurs when a failure is isolated to the channel E or F interface area on a eight channel storage director.

Card detecting the error:

NONE

FRU List

CIFE,F	01A-A4(A3)N2
01A-A4(A3)P2	CIF address switches set incorrectly
01A-B4(B3)D2	

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 0706

IC 0706: Occurs when a failure is isolated to the channel G or H area on a eight channel storage director.

Card detecting the error:

NONE

FRU List

CIFG,H	01A-A4(A3)N2
01A-A2(A1)G2	CIF address switches set incorrectly
01A-B4(B3)D2	

Diagnostic Check

Refer to Diagnostic Check 3 on page MNT-C 60.

IC 080x

These isolation codes are generated when a maintenance device (MD) invoked diagnostic is prevented from running.

Card detecting the error:

NONE

FRU List for 080x

01A-B4(B3)R2	01A-B1Q2
01A-B1S2	01A-B1E2
01A-B1T2	01A-B1C2
01A-B1P2	01A-B4(B3)P2

Diagnostic Check

No option is provided to loop the initialization of a diagnostic routine. Perform the following steps:

1. Select the MD support mode(s).
2. Select the failing storage director.
3. Select option 5.
4. Select the failing diagnostic.
5. Select run option 00 (no loop routine, halt on error).
6. Press the PF key on the MD to exit the diagnostic routine.

Execute the test each time a line is scoped.

Repeat steps 1 through 6 while scoping the nets on the cards shown in the FRU list. Check for incorrect levels or misshapen pulses.

IC 0800

IC 0800: Occurs when the response from the storage director, on initiation of a diagnostic routine, has exceeded the allotted time while in transmit mode.

IC 0801

IC 0801: Occurs when the MD detects an interrupt during initiation of a diagnostic routine when in a transmit mode.

The following check conditions cause interrupts:

- SERDES parity check/register select check
- EBO parity check
- EBI parity check
- Alert from a storage director

IC 0802

IC 0802: Occurs when the response from the storage director, on initiation of a diagnostic routine, exceeds the allotted time while in a receive mode.

IC 0803

IC 0803: Occurs when the MD detects an interrupt during initiation of a diagnostic routine when in a receive mode.

The check conditions causing interrupts is the same as for IC 0801.

IC 0804

IC 0804: Occurs when the data received from the maintenance device adapter (MDA) is incorrect.

IC 0805

IC 0805: Occurs when the data received from the storage director is incorrect.

IC 0806

IC 0806: Occurs when there is no response from the storage director when running a diagnostic routine.

IC 090x

These isolation codes are generated when a failure occurs while the maintenance device (MD) is in the support mode.

Card detecting the error:

NONE

FRU List for 090x

PWR	01A-B1E2
01A-B1P2	MD
01A-B1Q2	MD INPUT
01A-B4(B3)N2	SWITCH 103
01A-B1C2	

Diagnostic Check

Perform the following steps:

1. Select options 1 or 5 (start repair/machine checkout).
2. Scope the nets on the cards shown in the FRU list for incorrect levels or misshapen pulses.

IC 0900

IC 0900: Occurs when the response from the storage director exceeds the time allotted while in the transmit mode.

Note: This can be caused by the Loop Option being set on in the diagnostics and not in the MD option, or if the SD is powered down.

IC 0901

IC 0901: Occurs when the MD detects an interrupt while the storage director is in the transmit mode.

The check conditions causing interrupts are the same as for IC 0801.

IC 0902

IC 0902: Occurs when the response from a storage director exceeds the allotted time during the receive mode.

IC 0903

IC 0903: Occurs when the MD detects a storage director interrupt in the receive mode.

The check conditions causing interrupts are the same as for IC 0801.

IC 0904

IC 0904: Occurs when the data received from the maintenance device adapter (MDA) is not correct.

IC 0905

IC 0905: Occurs when the data received from a storage director is not correct.

IC 0906

IC 0906: Occurs when there is no response from the storage director when running a diagnostic routine.

SC 3000

An error alert is sent from the failing storage director to the operating storage director. When the operating storage director finds no bits active in the check registers of the failing storage director, SC 3000 is generated.

SC 3000 can be caused by one of the following:

- A short to ground in one of the error alert lines between the maintenance cards of the storage directors.
- The single check bit in the FRU or check register of the failing storage director is not activating.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4R2 50%	01A-B1Q2
01A-B3R2 30%	CIFA 2X
01A-B4(B3)P2 10%	CIFB 4X
01A-B1S2	01A-B4(B3)C2
01A-B1T2	01A-B4(B3)H2
01A-B1P2	01A-B4(B3)V2
	ADDRSW

Diagnostic Check

Remove the W top-card connector cable from the maintenance card 01A-B4(B3)R2 and scope the W28 pin, -Error Alert (Out). If the -Error Alert (Out) line is active at this pin, check the board wiring at the maintenance card for a short to ground or a minus-level signal line. If the -Error Alert (Out) line is not active at this pin, follow the wiring through the circuits shown on the LRM Card Reference Diagram.

Refer to Diagnostic Check 4 on page MNT-C 60.

SC 3001

The time-out error is a microcode detected error caused by a time-out in the storage director-to-storage director error data collection operation after an error alert.

SC 3001 code can be caused by one of the following:

- The failing storage director did not activate the -Command Valid (Out) line.
- The operating storage director did not activate the -Confirm (Out) line.

Card detecting the error:

NONE

FRU List

01A-B3R2 50%	CIFA 2X
01A-B4R2 20%	CIFB 4X
01A-B4(B3)P2 10%	01A-B4(B3)C2
01A-B1S2	
01A-B1T2	

Diagnostic Check

Refer to Diagnostic Check 5 on page MNT-C 60.

SC 3003

SC 3003: External bus in parity check is a hardware check sensed by the operating storage director while it is gathering failure data from the failing storage director.

Card detecting the error:

NONE

FRU List

01A-B4R2 30%	01A-B1T2 10%
01A-B3R2 30%	01A-B1Q2
01A-B1S2 10%	

Diagnostic Check

Refer to Diagnostic Check 5 on page MNT-C 60.

SC 3011 or F011

SC 3011 or F011: Is generated when the diskette drive select signal is lost between the read-only storage (ROS) controlled drive selection and the overlay loader program selection.

Card detecting the error:

NONE

FRU List

01A-B1P2 40%	01A-B1Q2
01A-B4(B3)R2 30%	01A-B4(B3) P2
01A-B1S2	
01A-B1T2	

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

SC 3012, 3013, F012, or F013

These codes are generated if the +Diskette Drive Index line is inactive when the index on the diskette is sensed.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 40%	01A-B1T2
01A-B1P2 30%	01A-B4(B3)P2
01A-B1S2	File Control Card

Diagnostic Check

If the +Diskette Drive Index line 01A-B1S2 is always active, check for the following:

1. The +Diskette Drive Index line is shorted to ground or to a minus-level signal line in the W top-card connector cable to the maintenance card.
2. The -File Index line 01A-B1P2 is shorted to ground or to a minus-level signal line in the board wiring from the maintenance device adapter control card.

Refer to Diagnostic Check 1 on page MNT-C 60.

SC 3014, 3015, F014, or F015

These symptom codes are generated if the diskette drive index pulse is present and if the clock, sync, or data pulses are missing. Diskette drive clock pulses occur every 4 microseconds and define the period when sync or data pulses can be present. When the storage director microprocessor card receives the index and clock pulses, it waits for the sync pulses. (The sync pulse is the first data pulse after the index pulse and identifies the start of a record.)

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 50%	01A-B1P2
01A-B4(B3)P2 10%	File Control Card
01A-B1S2	Diskette
01A-B1T2	

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

SC 3016, or F016

These symptom codes are generated when a storage director fails to read data from the diskette drive. The diskette drive receives index, clock, and sync pulses at the start of the IML operation, but cannot read a data record. A time-out occurs on the maintenance device adapter control card stopping the IML operation.

Card detecting the error:

NONE

FRU List

A-B4(B3)R2 60%	01A-B4(B3)P2
01A-B1S2 30%	01A-B1P2
01A-B1T2	Diskette

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

SC 3102

SC 3102: Is caused by a failure on the clock card or in the clock pulse distribution circuits that is detected on the maintenance card.

The clock check logic on the maintenance card checks the +Mnt Clock (T0-T7) lines to ensure the clock pulses maintain correct sequence and timing. This check cannot be caused by an inactive clock.

When the clock check logic senses a sequence or timing error, it activates bit 6 of check register 1 on the maintenance card.

Card detecting the error:

NONE

FRU List

01A-B4(B3)P2 50%
01A-B4(B3)R2 50%

Diagnostic Check

1. Run the loop check 1 clock stop error procedure. (See MD section of MSM.)
2. Refer to Diagnostic Check 7

SC3210

SC 3210: Occurs after an invalid sequence is detected. The invalid sequence check is a hardware check performed on the clock card. The check is sent to the maintenance card where it activates bit 3 of check register 2.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)R2 90%
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

SC 3280

SC 3280: Occurs when the external register address decode circuit selects more than one external register at the same time. The multiple decode check is sensed on the maintenance card by the multiple decode check logic. The line (on the maintenance card) from the multiple decode check logic activates bit 0 of check register 2.

Card detecting the error.

01A-B4(B3)R2

FRU List

01A-B4(B3)R2 90%
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 1 on page MNT-C 60.

Diagnostic Checks

Diagnostic Check 1

1. Select the MD support mode (S).
2. Select the failing storage director.
3. Select option 5 (manual control). See the MD section in the MSM for a further description of this option.
4. Select the loop IML option.
5. Check the circuits on the error condition diagram (MNT-C 5) for opens or shorts to ground.

Diagnostic Check 2

1. Select the MD support mode (S).
2. Select the failing storage director.
3. Select option 6 (maintenance connection test). See the MD section in the MSM for a further description of this option.
4. Select the MDA test.
5. Select the loop test and halt on error option.

If an error occurs, repeat steps 1 through 5 using the loop test and bypass error option.

Diagnostic Check 3

1. Select the MD support mode (S).
2. Select the failing storage director.
3. Select option 6 (maintenance connection test). See the MD section in the MSM for a further description of this option.
4. Select the storage director selection test.
5. Select the loop test and halt on error option.

If an error occurs, repeat steps 1 through 5 using the loop test and bypass error option.

Diagnostic Check 4

Enter the following selections into the MD:

1. Select option 6 (maintenance connection test). See the MD section in the MSM for a further description of this option.
2. Loop and halt on error option

If an error occurs, repeat Diagnostic Checks and the Maintenance Connection Test using the loop and bypass error option. Scope the nets on the error condition diagram (MNT-C 5) for incorrect levels and misshapen pulses.

Diagnostic Check 5

1. Select the MD support mode (S).
2. Select the failing storage director.
3. Select option 6 (maintenance test). See the MD section in the MSM for a description of this option.
4. Select the storage director to storage director test (option 4).
5. Select the loop test and halt on error option.

If an error occurs, repeat steps 1 through 5 using the loop test and bypass error option.

Diagnostic Check 6

Enter the following selections into the MD:

1. Select option 5 (manual control). See the MD section in the MSM for a further description of this option.
2. Loop option

Contents of This Section

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
25	10	1	E05
2E	10	1	E05
2F	10	1	E05
31	10	1	E05
33	10	1	E05
37	10	1	E05
3A	10	1	E05
3B	10	1	E05
3C	10	1	E05
51	15	1	E07
52	15	1	E07
53	15	1	E07
54	15	1	E07
5D	15	1	E07
6D	15	1	E07
6E	15	1	E07
6F	15	1	E07
71	15	1	E07
72	15	1	E07
73	15	1	E07
74	20	1	E09
75	20	1	E09
76	20	1	E09
77	20	1	E09
78	20	1	E09
79	20	1	E09
7A	20	1	E09
7B	20	1	E09
7C	20	1	E09
7D	20	1	E09
7E	20	1	E09
7F	20	1	E09
A3	25	1	E11
A4	25	1	E11
A9	25	1	E11
AB	25	1	E11
AC	25	1	E11
AD	25	1	E11
AE	25	1	E11
AF	25	1	E11
B1	25	1	E11
B6	25	1	E11
BD	25	1	E11
BE	25	1	E11
BF	30	2	A05
C1	30	2	A03
C2	30	2	A03
C4	30	2	A03
C8	30	2	A03
CD	30	2	A03
20xx	35	2	A07
2010	35	2	A07
2502	40	2	A09
2504	40	2	A09
2580	40	2	A09
28C2	40	2	A09
28C8	40	2	A09
28C9	45	2	A11
28CA	45	2	A11
28CB	45	2	A11
28CC	45	2	A11
2928	50	2	A13
2A00	50	2	A13
2A01	50	2	A13
2A02	50	2	A13
2A03	55	2	A15
2A04	55	2	A15
2A0A	55	2	A15
2A0B	55	2	A15
3D00	55	2	A15
F214	60	2	A17
F215	60	2	A17
F261	60	2	A17
F262	60	2	A17
F263	60	2	A17
F264	60	2	A17
F265	60	2	A17
F294	60	2	A17
F295	60	2	A17
F2E1	60	2	A17
F2E2	60	2	A17
F2E3	60	2	A17
F2E4	60	2	A17
F2E5	60	2	A17

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

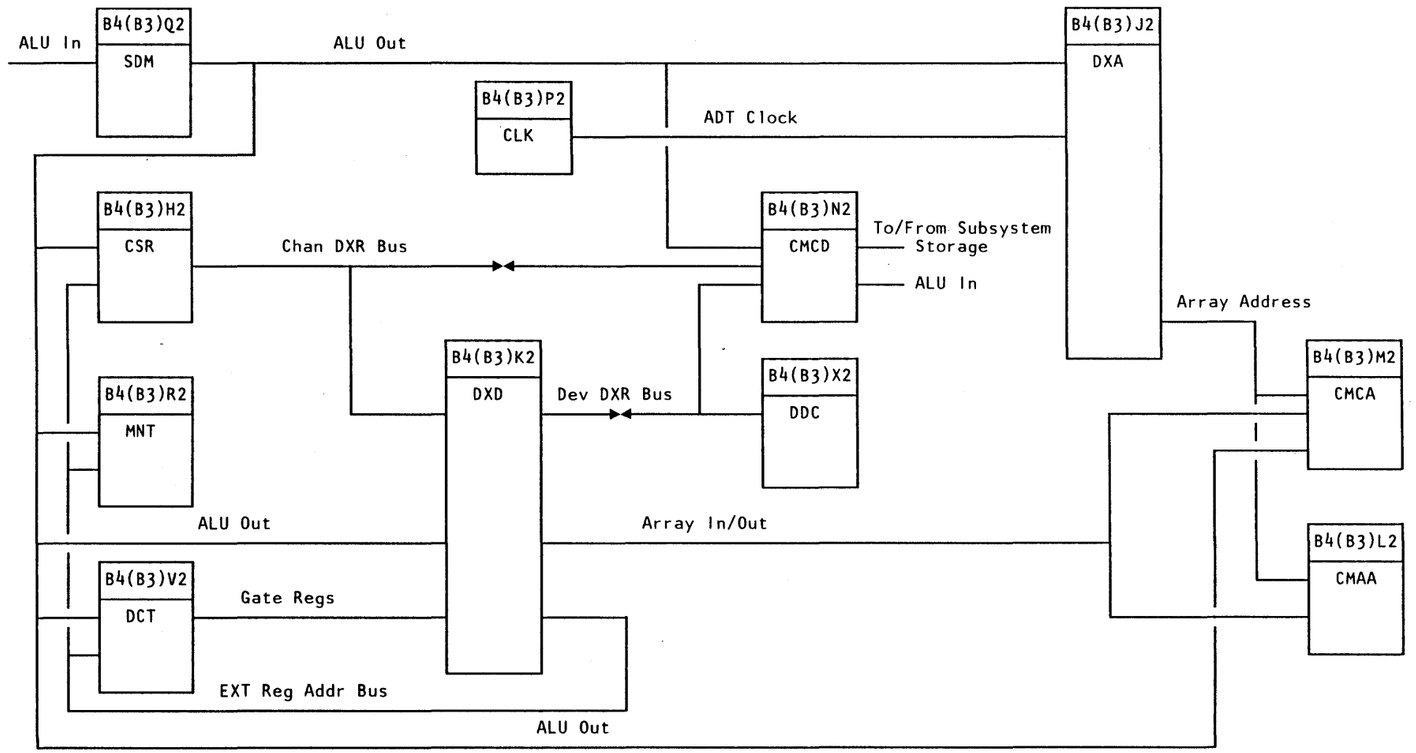
Error Code Diagram

This diagram shows the data transfer to and from the ADT buffer (CMCA card) and the device interface (DDC card), the channel interface (CSR card), the Microprocessor (SMD card), and the port adapter (CMCD card).

Data may be transferred from:

- Device to channel through the buffer
- Device to subsystem storage through the buffer or bypassing the buffer
- Device to subsystem storage and to the channel through the buffer
- Channel to device through the buffer
- Channel to subsystem storage through the buffer or bypassing the buffer
- Channel to subsystem storage and to the device through the buffer
- Buffer to subsystem storage
- Subsystem storage to buffer
- ALU to subsystem storage
- Subsystem storage to ALU
- ALU to buffer
- Buffer to ALU

Note: See the OPER section of the MSM for a detailed description of this area



IML 25

DXA Register Failure: Occurs when a machine reset fails to reset one of the external registers on the data transfer address (DXA) card, or a failure causes the external registers to change value after the reset occurs. The external registers on the DXA card are:

- Data transfer control
- Toggle FRU register
- Buffer ALU Pointer low
- Buffer ALU Pointer high
- Channel Buffer Pointer low
- Channel Buffer Pointer high
- Device Buffer Pointer low
- Device Buffer Pointer high

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2 50%
01A-B4(B3)K2 40%
01A-B4(B3)Q2
01A-B4(B3)H2
01A-B4(B3)R2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 2E

DDC End of Transfer or First Sync In: Indicates that the following register bits were not reset by machine reset.

- Bit 2 (DDC end of transfer) of the transfer error status (XES) register.
- Bit 6 (first sync in) of the transfer complete status (XCS) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)J2 30%
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 2F

CDX End of Transfer or Compare successful: Indicates that the following XCS register bits were not reset by machine reset:

- Bit 4 (CDX end of transfer)
- Bit 5 (compare successful)

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2 60%
01A-B4(B3)J2 30%

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 31

Channel Truncation: Indicates that bit 7 (channel truncation) of the XCS register is not reset by machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)G2
01A-B4(B3)J2
01A-B4(B3)H2
01A-B4(B3)P2
CIFA 2X
CIFB 4x
01A-B4(B3)F2
01A-A4(A3)G2
01A-B4(B3)E2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 33

DXD Clock/ External Register Address Check: Occurs when a machine reset fails to reset the following register bits:

- Bit 3 (clock check 2) of the transfer error status (XES) register
- Bit 6 (DXD card check) of the check (CHK) register

It also occurs when a clock check is detected on the data transfer data (DXD) card immediately after the machine is reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)N2
01A-B4(B3)P2
01A-B4(B3)Q2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 37

Clock Check Without Card Check: Indicates that a machine reset has failed to reset transfer error status (XES) register bit 3. The failure is caused by:

- A clock check is detected by the DXD, DDC, CDX, or the CSC cards, but the respective card check latch failed to set.
- The -Clock Check Two line drivers on the failing card failed.
- Bit 3 (clock check 2) of The XES register failed to reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)F2
01A-B4(B3)G2
01A-B4(B3)X2
CIFx
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

IML 3A

Channel Buffer Check: Occurs when a machine reset fails to reset bit 6 (channel buffer check) of the transfer error status (XES) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)G2
01A-B4(B3)J2
01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 3B

Device Buffer Check: Occurs when a machine reset fails to reset bit 7 (device buffer check) of the transfer error status (XES) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)X2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 3C

DXA Card Check: Indicates that bit 0 (DXA card check) of the check (CHK) register is not reset by machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 90%
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 51 or 54

Toggle Failure: Indicates a failure of the buffer ALU pointer (BAP), channel buffer pointer (CBP), or the device buffer pointer (DBP) register toggles.

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 52

DXA Card Check: Indicates that bit 0 (DXA card check) of the CHK register did not set or reset under microcode control.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2
01A-B4(B3)H2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 53

DXA Card Check: Indicates that bit 0 (DXA card check) of the CHK register is active during one of the following register tests:

- Data transfer control (DXC)
- Channel buffer pointer (CBP)
- Device buffer pointer (DBP)
- Buffer ALU pointer (BAP)

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 5D

Array Out Parity Check: Occurs when a machine reset fails to reset bit 4 (array out check) of the check (CHK) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 6D

Sense Register Check: Indicates that bit 5 (sense register check) of the check (CHK) register did not reset by machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)H2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 6E

DXD Card Check: Occurs when a machine reset fails to reset bit 6 (DXD card check) of the check (CHK) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML 6F

Check Register: Indicates that a machine reset failed to reset bit 7 of the check (CHK) register.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)N2 60%
01A-B4(B3)L2 20%
01A-B4(B3)M2 20%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 71

BAP Register Failure: Indicates a failure of the buffer ALU pointer register to increment or to wrap correctly.

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2
01A-B4(B3)K2
01A-B4(B3)L2
01A-B4(B3)M2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 72

DXD Clock/External Register Address Check: Indicates that the following register bits are active during a buffer read/write test:

- Bit 3 (clock check 2) of the transfer error status (XES) register
- Bit 6 (DXD card check) of the check (CHK) register

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)P2
01A-B4(B3)K2
01A-B4(B3)Q2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 73

DXA Card Check: Indicates that bit 0 (DXA card check) of the CHK register is active during a buffer read/write test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML 74

DXD Card Check: Occurs when bit 6 (DXD card check) of the CHK register is active after a buffer read/write test.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 75

Array Out Parity Check: Indicates that bit 4 (array out check) of the CHK register is active during a data fetch from the CMAA card.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)L2
01A-B4(B3)M2
01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 76

Array Out Parity Check: Indicates that bit 4 (array out check) of the CHK register is active during a data fetch from the CMCA card.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)M2
01A-B4(B3)L2
01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 77

Array Out Parity Check: Indicates that bit 4 (array out check) of the CHK register is active during a data fetch from the CMAA and CMCA card.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2
01A-B4(B3)L2
01A-B4(B3)M2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 78

Array Out Parity Check: Indicates that bit 4 (array out check) of the CHK register is not set by forcing incorrect parity on the Array Bus Out lines or is not reset by check reset.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 79

Array Out Parity Check: Indicates that a data miscompare occurs during a data fetch from the CMAA card.

Card detecting the error.

NONE

FRU List

01A-B4(B3)L2
01A-B4(B3)M2
01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7A

Array Out Parity Check: Indicates that a data miscompare occurs during a data fetch from the CMCA card.

Card detecting the error.

NONE

FRU List

01A-B4(B3)M2
01A-B4(B3)L2
01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7B

Array Out Parity Check: Indicates that a data miscompare occurs during a data fetch from the CMCA card.

Card detecting the error.

NONE

FRU List

01A-B4(B3)K2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7C

Array Out Parity Check: Indicates that bit 4 (array out check) of the CHK register is active during a buffer increment (BFI) or buffer increment (CFI) register fetch operation.

Card detecting the error.

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2
01A-B4(B3)L2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7D

Buffer Failure: Indicates that a data miscompare occurs during a buffer increment (BFI) register read/write test.

Card detecting the error.

NONE

FRU List

01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7E

Channel Buffer Pointer Failure: Indicates that a channel buffer pointer (CBP) register failure occurs during a buffer increment (CFI) buffer read/write test.

Card detecting the error.

NONE

FRU List

01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML 7F

Buffer Failure: Indicates that a data miscompare occurs during a buffer increment (CFI) to buffer read/write test.

Card detecting the error.

NONE

FRU List

01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 page DBFR 75.

IML A3

DXA Card Check: Indicates that bit 0 (DXA card check) of the CHK register is active during a buffer to device bus out (DB0) test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML A4

Buffer to Device Bus Out Miscompare: Indicates that a data miscompare occurred during a data transfer from the buffer to the device bus out (DB0) register.

Card detecting the error:

NONE

FRU List

01A-B4(B3)K2 50%
01A-B4(B3)J2
01A-B4(B3)X2
01A-B4(B3)Q2
01A-B4(B3)V2
01A-B4(B3)H2
01A-B4(B3)N2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML A9

DXD Card Check: Occurs when bit 6 (DXD card check) is active after a buffer to device bus out (DB0) register data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)X2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML AB

Device Bus In to Buffer Miscompare: Indicates that a data miscompare occurred during a data transfer from the device in (DBI) to the buffer.

Card detecting the error:

NONE

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)K2 40%
01A-B4(B3)V2
01A-B4(B3)N2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML AC

Device Buffer Check: Indicates that a device buffer check occurred during a (DBI) to buffer data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2 60%
01A-B4(B3)K2 40%
01A-B4(B3)V2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML AD

DXD Card Check: Occurs when bit 6 (DXD card check) of the CHK register is active after a device bus in (DBI) register to buffer data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)J2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML AE

CDX End of Transfer Failure: Indicates that bit 4 (CDX end of transfer) of the transfer complete status (XES) register failed to set or reset during a data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2
01A-B4(B3)G2
01A-B4(B3)J2
01A-B4(B3)F2
01A-B4(B3)V2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML AF

Indicates that a buffer pointer wrap failure occurred during a data transfer test.

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2 90%
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML B1

Device Buffer Check: Indicates that a device buffer check occurred during a buffer to (DBO) data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)X2
01A-B4(B3)H2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML B6

DXA Card Check: Indicates that bit 0 (DXA card check) of the CHK register is active during a buffer to device bus out (DB0) test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 90%

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML BD

Channel Buffer Check: Indicates that bit 6 (channel buffer check) of the XES register occurred during a buffer to channel buffer in (CBI) data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML BE

DXD Card check: Occurs when bit 6 (DXD card check) of the CHK register is active after the buffer to channel bus in (CBI) register data transfer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML BF

DXA Card check: Indicates that bit 0 (DXA card check) of the CHK register is active during a channel bus in (CBI) to buffer test.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 90%

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML C1

Device Buffer check: Indicates that bit 7 (device buffer check) of the XES register did not set or reset by check reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 40%
01A-B4(B3)J2 40%
01A-B4(B3)R2 20%

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML C2

Channel Buffer Check: Indicates that bit 6 (channel buffer check) of the XES register did not set or reset by check reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 40%
01A-B4(B3)J2 40%
01A-B4(B3)R2 20%

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

IML C4

DXD Card check: Occurs when bit 6 (DXD card check) of the CHK register remains inactive after forcing a data transfer (DXD) card check or bit 6 was active following a power on reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 40%
01A-B4(B3)J2 40%
01A-B4(B3)R2 10%
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML C8

Level 2 Interrupt Failure: Indicates that a level 2 interrupt does not occur when bit 2 of the XCS register is active during a data transfer test and the 3880 is enabled.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)X2
01A-B4(B3)J2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML CD

Channel Check 1: Indicates that a CDX card check did not set the Channel Check 1 line on the selected storage director.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)F2
01A-B4(B3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

IML Error Codes DBFR 30

SC 20xx

Transfer Error Sense Register: SC 20xx is generated when multiple check indications are latched in the XES register and represents a combination of symptom codes.

Determine which combination of bits are on, and go to those symptom codes (SC). The failing SCs are:

2001
2004
2008
2018
2020
2080

Card detecting the error:

01A-B4(B3)J2

FRU List FOR 20xx

01A-B4(B3)X2 50%
01A-B4(B3)J2 40%
01A-B4(B3)K2
01A-B4(B3)P2
01A-B4(B3)V2

See the ECI section in this manual for the location of these error codes.

SC 2010

Clock Check Without Card Check: Indicates that a clock check condition is detected by one of the following cards:

- Director-to-device controller (DDC)
- Data transfer address (DXA)
- Channel data transfer (CDX)
- Channel sequence control (CSC).

The card check latch line from the card that detected the check failed to set.

The clock check without card check failure sets bit 3 of the XES register located on the DXA card.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 50%
01A-B4(B3)H2
01A-B4(B3)G2
01A-B4(B3)V2
01A-B4(B3)X2
01A-B4(B3)F2
01A-B4(B3)K2
CIFx
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

SC 2210

DXR Bus In Parity Check: Indicates that incorrect parity was detected on an operation when either the channel or the device was degated and that data was being sent to the ADT from the CMCD card.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)N2 50%
01A-B4(B3)X2 10%
01A-B4(B3)H2 10%
01A-B4(B3)G2
01A-B4(B3)Q2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

SC 2501

ADT Buffer Check: Indicates that the port connection or the ADT buffer had a buffer check.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 50%
01A-B4(B3)L2 30%
01A-B4(B3)N2 20%

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

SC 2502

DXD Card Check: Indicates a failure of the DXD card due to one of the following conditions:

- Buffer state check
- Data in register (DIR) select check
- Data out register (DOR) select check
- Write enable compare check

BUFFER STATE CHECK

During automatic data transfer, the buffer is always in one of four states; empty, positive data, full, or negative data. The buffer state logic that determines the buffer state is duplicated to ensure correct operation. The check is performed at every T2 or T4 clock time.

DATA IN REGISTER SELECT CHECK

The data in register (DIR) holds data that is being written into the buffer during an array store cycle. The data is loaded from the following hardware registers during microprocessor store, channel automatic store, and device automatic store operations:

- Buffer in
- Buffer/channel 2
- Buffer/device 2

DATA OUT REGISTER SELECT CHECK

The data out register (DOR) holds data read from the buffer during an array fetch cycle. It is loaded from the Array Out Hi or Array Out Lo line.

The DOR select check is a check of the load lines and is performed at every T1 or T5 clock time.

WRITE ENABLE COMPARE CHECK

The write enable compare check is a check of the -Write Enable line form the data transfer address (DXA) card with a duplicate +Array Write line generated on the data transfer data (DXD) card by comparing the two signals at every T1 or T5 clock time.

The check condition is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)K2 90%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2504

Sense Register Check: Indicates that incorrect parity is detected across bits 2, 4, 5, 6, and 7 of the XCS register.

The XCS register is latched into the sense register at T6 clock time and the check is performed at the following T4 clock time.

The check is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 70%
01A-B4(B3)H2 20%
01A-B4(B3)G2
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

SC 2580

DXA Card Check: Indicates that one of the following check conditions is detected on the DXA card:

- Chip select check
- Array out gate check
- DOR select check
- Register parity check

CHIP SELECT CHECK

The chip select check ensures that only one Chip Select line is active during a buffer store or fetch operation. The check is performed at T1 or T5 clock time when the BAP, CBP, or DBP registers are gated to the current address register (CAR).

ARRAY OUT GATE CHECK

The array out gate check ensures that only one Array Out Gate line is active during a buffer store or fetch operation. The check is performed at T2 or T6 clock time when the BAP, CBP, or DBP registers are gated to the current address register (CAR).

DOR SELECT CHECK

The data output register select check verifies that the data out register (DOR) Input Hi and DOR Input Lo lines are active with the correct Chip Select lines. The check is performed at T1 or T5 clock time.

REGISTER PARITY CHECK

The register parity check indicates that incorrect parity is detected in one of the buffer address registers (BAP, CBP, or DBP).

The check condition is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 90%
01A-B4(B3)K2
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2581

Pad Count Check: Indicates that a pad count check happened during cache operations.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)N2 10%
01A-B4(B3)H2 10%
01A-B4(B3)G2 10%
01A-B4(B3)V2 10%
01A-B4(B3)X2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 28C2

Unexpected Level 2 Interrupt: Is a check 2 error detected by the microcode. When the check is detected, format 2, sense byte 20 is loaded with message 'C2'. This indicates that a level 2 interrupt occurred because of an unexpected hardware failure. A level 2 interrupt is caused by the following conditions:

- Select out trapped
- End Op from the attached device
- Device end of transfer

Card detecting the error:

NONE

FRU List

01A-B4(B3)X2 50%
01A-B4(B3)J2 30%
01A-B4(B3)R2 10%

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 28C8

DBP or PCR Not As Predicted: Is a check 2 error detected by the microcode. When this check is detected, format 2, sense byte 7 equals '2F' and sense byte 20 contains message 'C8'. This indicates that during a data transfer operation an incorrect number of bytes is transferred in or out of the buffer. The check is performed by comparing the value of the device buffer pointer (DBP) or the pad count (PCR) register to a predicted value at the end of the transfer. The predicted value is obtained by adding the total number of bytes to be transferred to the value of DBP at the start of the data transfer.

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2 60%
01A-B4(B3)K2 30%
01A-B4(B3)V2 10%
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 28C9

CBP Not As Predicted: Is a check 2 error detected by the microcode. When this check is detected, format 2, sense byte 7 equals '2F' and sense byte 20 contains message 'C9'. This indicates that during a data transfer operation an incorrect number of bytes is transferred in or out of the buffer. The check is performed by comparing the value of the channel buffer pointer (CBP) register to a predicted value at the end of the transfer. The predicted value is obtained by adding the total number of bytes to be transferred to the value of CBP at the start of the data transfer.

Card detecting the error:

NONE

FRU List

01A-B4(B3)J2 60%
01A-B4(B3)K2 30%
01A-B4(B3)G2
01A-B4(B3)H2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

SC 28CA

Channel Cyclic Redundancy Check: Indicates that a data field fetched from the buffer during a buffer-to-channel operation did not contain the same cyclic redundancy check byte that is generated when the data field is stored in the buffer during a device-to-buffer operation.

During a device-to-buffer data transfer a cyclic redundancy check byte is generated by the device cyclic redundancy (DRC) register for the data field being stored in the buffer. The check byte for the data field is then stored in the buffer with the data by the microprocessor using a processor operation.

When the data field is fetched from the buffer during a buffer-to-channel operation, a second cyclic redundancy check byte is generated by the channel cyclic redundancy (CRC) register. This check byte for the data fetched from the buffer is then compared with the check byte generated when the data field was stored in the buffer.

This is a check 2 error detected by the microcode. When it is detected, format 2 sense byte 7 equals '2F' and sense byte 20 contains the message 'CA', indicating the channel cyclic redundancy check.

Card detecting the error:

NONE

FRU List

01A-B4(B3)K2 60%
01A-B4(B3)X2 20%
01A-B4(B3)J2 10%
01A-B4(B3)G2
01A-B4(B3)L2
01A-B4(B3)M2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

SC 28CB

Device Cyclic Redundancy Check: Indicates that a data field fetched from the buffer during a buffer-to-device operation did not contain the same cyclic redundancy check byte that is generated when the data field is stored in the buffer during a channel-to-buffer operation.

During a channel-to-buffer data transfer a cyclic redundancy check byte is generated by the channel cyclic redundancy (CRC) register for the data field being stored in the buffer. The check byte for the data field is then stored in the buffer with the data by the microprocessor using a processor operation.

When the data field is fetched from the buffer during a buffer-to-device operation, a second cyclic redundancy check byte is generated by the device cyclic redundancy (DRC) register. This check byte for the data fetched from the buffer is then compared with the check byte generated when the data field was stored in the buffer.

This is a check 2 error detected by the microcode. When it is detected, format 2 sense byte 7 equals '2F' and sense byte 20 contains the message 'CB', indicating the device cyclic redundancy check.

Card detecting the error:

NONE

FRU List

01A-B4(B3)K2 70%
01A-B4(B3)H2 10%
01A-B4(B3)J2 10%
01A-B4(B3)G2 10%
01A-B4(B3)L2
01A-B4(B3)M2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

SC 28CC

Device Interrupt Process Timeout: Is a check 2 error detected by the microcode. When this check is detected, format 2, sense byte 7 equals '2F' and sense byte 20 contains message 'CC'. This check indicates a microcode timer overflow due to a hang condition during a device interface process operation.

Card detecting the error:

NONE

FRU List

01A-B4(B3)K2 60%
01A-B4(B3)X2 20%
01A-B4(B3)J2 10%
MLX4 In MIM

Diagnostic Check

Refer to Diagnostic Check 2 on page DBFR 75.

SC 2928

Check 2 Without a Check 2 Error Condition: Is generated when bit 0 (check 2) of the transfer complete status (XCS) register is active, but the check conditions that set this bit are off. See the SENSE section in the Maintenance Support Manual for a description of the check conditions that set, bit 0 or the XCS register.

The channel sequence control (CSC) and director-to-device controller (DDC) cards set bit 0 of the XCS register by activating the -Check 2 line.

- The CSC card activates the -Check 2 line when a channel bus out deskew register parity check is detected.
- The DDC card activates -Check 2 line when the +Connection Check Alert is active from the attached device.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)J2 90%	01A-B4(B3)F2
01A-B4(B3)X2 10%	CIFx
01A-A1R2 SD1	01A-B4(B3)H2
01A-A1S2 SD2	01A-B4(B3)G2
01A-B4(B3)N2	01A-B4(B3)K2
	Attached device

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2A00

DXD Clock/External Register Address Check: Occurs when one of the following check conditions is detected on the DXD card:

- Multiple or sequential clock check
- Load external register clock check
- External register address parity check
- Multiple decode check

Multiple or Sequential Clock Check

The multiple or sequential clock check indicates an extra or missing clock pulse.

Load External Register Clock Check

The load external register clock check ensures the correct operation of the +Ld Ext Reg Clk B line from the storage director microprocessor (SDM) card that validates the data on the ALU Bus Out lines. The check is generated when the +Ld Ext Reg Clk B line is active and the +Ext Reg Select line is inactive or if the +Ext Reg Select line is active and the +Ld Ext Reg Clk B line is inactive, at T0 clock time.

External register address parity check

The external register address parity check indicates that invalid parity is detected on the DXD card across the External Register Address Bus and Ext Reg Select lines generated by the SDM card.

Multiple Decode Check

The multiple decode check indicates an external register decode failure on the DXD card.

The check condition is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)K2

FRU List

01A-B4(B3)P2 40%	01A-B4(B3)K2 20%
01A-B4(B3)Q2 20%	01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2A01 or SC 2A02

Channel Buffer Check: Indicates a failure during data transfer between the channel and the buffer because of one of the following:

- Buffer channel register 1 (BC1) parity check
- Buffer overrun
- Data transfer data (DXD) card is not active

BC1 – Parity Check

BC1 is a temporary storage register that holds data being transferred between the buffer and the channel interface hardware. BC1 is loaded at T0 or T4 clock time from the Channel DXR Bus lines when the transfer is from the channel to the buffer or from the data out register (DOR) if the transfer is from the buffer to the channel.

The check is performed at T2 or T4 clock time if the BC1 register is full.

Buffer Overrun

Buffer overrun is caused when an overrun condition is detected between the channel interface hardware and the buffer. This occurs when the +Take Data or Data Taken control line from the channel data transfer (CDX) card is active, and the -Need Data or Data Ready line from the data transfer data (DXD) card is not active.

DXD Card Inactive

The channel buffer check is divided into two symptom codes to indicate the direction of the data flow between the channel and the buffer at the time of the error. The direction is determined by channel transfer checks (CXC) register bits 1, 2, and 6.

- SC 2A01 - Channel Buffer Check

  SC 2A01 indicates the check is detected during a channel-to-buffer operation and that the data is sent to the buffer from the channel search (CSR) card during a write operation.

- SC 2A02 - Channel Buffer Check

  SC 2A02 indicates the check is detected during a buffer-to-channel operation and that the data is sent from the buffer to the channel search (CSR) card during a read operation.

  The check condition is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2 40%	01A-B4(B3)J2 10%
01A-B4(B3)K2 40%	01A-B4(B3)G2 10%
	01A-B4(B3)N2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2A03 or 2A04

Device Buffer Check: Indicates a device buffer check (bit 7 of the XES register) during a data transfer between the device interface hardware and the buffer because of one of the following:

- Buffer/device register 1 (BD1) parity check
- Buffer overrun

BD1 – Parity Check

BD1 is a temporary storage register that holds data being transferred between the buffer and the device interface hardware. BD1 is loaded at T0 or T4 clock time from the device DXR Bus lines when the transfer is from the device interface to the buffer or from the data out register (DOR) if the transfer is from the buffer to the device.

The check is performed at T2 or T6 clock time if the BD1 register is full.

Buffer Overrun

Buffer overrun is caused when an overrun condition is detected between the device interface hardware and the buffer. This occurs when the -Take Data or the -Data Taken lines are active, and the -Need Data/Data Ready line is not active.

The device buffer check is divided into two symptom codes to indicate the direction of the data flow between the device interface hardware and the buffer at the time of the error. The direction is determined by bit 6 of the device tag gate (GTD) register.

- SC 2A03 - Device Buffer Check

  SC 2A03 indicates the check is detected during a device-to-buffer operation and that the data is sent to the buffer from the director-to-device controller (DDC) card during a read operation.

- SC 2A04 - Device Buffer Check

  SC 2A04 indicates the check is detected during a buffer-to-device operation and that the data is sent to the DDC card from the buffer during a write operation.

  The check condition is reset by check reset or machine reset.

Card detecting the error:

01A-B4(B3)J2

FRU List 2A03

01A-B4(B3)X2 40%
01A-B4(B3)K2 40%
01A-B4(B3)J2 10%
01A-B4(B3)G2
01A-B4(B3)H2
01A-B4(B3)N2

FRU List 2A04

01A-B4(B3)K2 70%
01A-B4(B3)J2 10%
01A-B4(B3)X2 10%
01A-B4(B3)G2
01A-B4(B3)H2
01A-B4(B3)N2

Diagnostic Check

Refer to Diagnostic Check 1 on page DBFR 75.

SC 2A0A or 2A0B

Array Out Parity Check: Indicates that data with incorrect parity is fetched from the buffer.

During a buffer store operation the address and data parity bits are exclusive ORed and stored as the data parity. This is accomplished on the data transfer data (DXD) card where the parity bit of the current address register (CAR) is exclusively ORed with the parity bit of the data in register (DIR), which contains the data being stored into the buffer. This new parity bit is stored with the data byte.

During a buffer fetch operation, the data fetched from the buffer is gated to the data out register (DOR). The CAR and DOR parity bits are exclusive ORed on the DXD card. This provides address protection and data protection.

The check is performed at T1 or T5 clock time when the DOR register contains valid data.

The check is reset by check reset or machine reset.

- SC 2A0A – ARRAY OUT PARITY CHECK

  SC 2A0A indicates that the check is detected during a data fetch from the CMCA card.

- SC 2A0B – ARRAY OUT PARITY CHECK

  SC 2A0B indicates that the check is detected during a data fetch from the CMCA card.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)M2 50%
01A-B4(B3)K2 30%
01A-B4(B3)J2 10%
01A-B4(B3)L2

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

SC 3D00

Clock Check: Indicates that a clock check occurred with out a card check. The CSC, CDX, and the channel interface card check bits are off.

01A-B4(B3)K2

FRU List

01A-B4(B3)J2 60%
01A-B4(B3)K2 30%

Diagnostic Check

Refer to Diagnostic Check 3 on page DBFR 75.

SC F214 (Port 1) or F294 (Port 2)

Auxiliary SDM Adapter IR Summary Check: Is set because of the Auxiliary SDM Adapter IR Summary Check being active. (Bit 0 of the CSPRDIC register was active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)N2
01A-B4(B3)M2
01A-B4(B3) WLMN TCC
01A-B4(B3) YLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F215 (Port 1) or F295 (Port 2)

Communication Adapter IR Summary Check: Is set because of the Communication Adapter IR Check being active. (Bit 1 of the CSPRDIC register was active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 90%
01A-B4(B3)N2
01A-B4(B3) WLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F261 (Port 1) or F2E1 (Port 2)

Buffer/ASDM Array in Parity Check: Is set because of a parity error on the Array In bus going to the Buffer or the ASDM Control Storage. (Bit 3 of the CAAJCK register is active).

Card detecting the error:

01A-B4(B3)L2

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)M2
01A-B4(B3)K2
01A-B4(B3)H2
01A-B4(B3)X2
01A-B4(B3)J2

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F262 (Port 1) or F2E2 (Port 2)

Current Address Register Check: Is set because of a parity error on the Current Address Register (CAR) bus going to the buffer or the ASDM control storage (Bit 7 of the CAAJCK register is active).

Card detecting the error:

01A-B4(B3)L2

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)M2
01A-B4(B3)J2
01A-B4(B3) WLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F263 (Port 1) or F2E3 (Port 2)

ASDM Local Storage/External Register Address Parity Check: Is set because of an SDM external register (excluding IRG) being addressed by the ASDM. (Bit 1 of the CAAJCK register is active).

Card detecting the error:

01A-B4(B3)L2

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)M2
01A-B4(B3)YLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F264 (Port 1) or F2E4 (Port 2 ASDM)

Control Storage Address Parity Check: Is set because of a parity error on the ASDM control storage address bus. (Bit 6 of the CAAJCK register is active).

Card detecting the error:

01A-B4(B3)L2

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)M2
01A-B4(B3) YLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

SC F265 (Port 1) or F2E5 (Port 2)

ASDM Internal Check: Is set because of an error internal to the ASDM. (Bit 2 of the CAAJCK register is active).

Card detecting the error:

01A-B4(B3)L2

FRU List

01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Checks 4-9, page DBFR 75.

Diagnostic Check 1

1. Power off the failing storage director and remove all cards shown in the FRU list. Check all nets with a CE meter for an open, a short between nets, a short between a net pin and ground, or a voltage. See the MDM for the voltage pin list.
2. Bypass the IML error halt. Re-execute routine 70 with default parameters and determine the failing test. If an intermittent failure is suspected execute routine 70.
3. Execute an IML to the failing storage director, bypass the error halt, and loop the failing function test. Scope all nets on the ECD for incorrect levels or misshapen pulses.
4. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, call for assistance.

Diagnostic Check 2

1. Power off the failing storage director and remove all cards shown in the FRU list. Check all nets with a CE meter for an open, a short between nets, a short between a net pin and ground, or a voltage. See the MDM for the voltage pin list.
2. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, go to the next step.
3. Place the failing storage director in an IML loop. Scope all nets on the ECD for incorrect levels or misshapen pulses. While looping the IML failure, check for differences between the input and output pins.

Diagnostic Check 3

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Reset the failing storage director and ensure that the -Clock Check Two latched line is inactive. Power off the failing storage director and remove all cards shown in the FRU list. Check all nets with a CE meter for an open, a short between nets, a short between a net pin and ground, or a voltage. See the MDM for the voltage pin list.
2. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, go to the next step.
3. Bypass the IML error halt and loop routine 70. Scope all nets on the ECD for incorrect levels or misshapen pulses. While looping the IML failure, check for differences between the input and output pins.

Diagnostic Check 4

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routines 50-5C. If error occurs proceed as directed by the MD.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 5

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routines 57-5F.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 6

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routines 65-67.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 7

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routine 69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 8

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routines 68-69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 9

Warning: Make sure that subsystem storage is offline to all storage directors.

1. Attach the MD to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the ECD that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the ECD.
4. Run diagnostic routine 6A.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Control

Contents of This Section

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
0F	10	2	B07
20	10	2	B07
21	10	2	B07
22	10	2	B07
23	10	2	B07
24	10	2	B07
98	10	2	B07
99	10	2	B07
9A	10	2	B07
9B	10	2	B07
9C	10	2	B07
9D	10	2	B07
E0	10	2	B07
E1	10	2	B07
E2	15	2	B09
E3	15	2	B09
E4	15	2	B09
E8	15	2	B09
E9	15	2	B09
EA	15	2	B09
EB	15	2	B09
EC	15	2	B09
300F	20	2	B11
3104	20	2	B11
3108	20	2	B11
3110	20	2	B11
3120	20	2	B11
3140	25	2	B13
3180	25	2	B13
31A0	25	2	B13
3201	25	2	B13
3220	25	2	B13
3240	25	2	B13
3401	30	2	B15
3402	30	2	B15
3403	30	2	B15
3404	30	2	B15
3405	30	2	B15
3406	30	2	B15
3410	30	2	B15
3411	30	2	B15
3412	30	2	B15
3413	30	2	B15
3600	35	2	B17
3601	35	2	B17
3602	35	2	B17
3604	35	2	B17
3800	35	2	B17
3801	35	2	B17
3802	35	2	B17
3803	35	2	B17
3804	35	2	B17
3805	35	2	B17
380F	40	2	C01
3A01	45	2	C03
3A02	45	2	C03
3A03	45	2	C03
3A04	45	2	C03
3A05	45	2	C03
3A06	45	2	C03
3A07	45	2	C03
3A10	45	2	C03

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

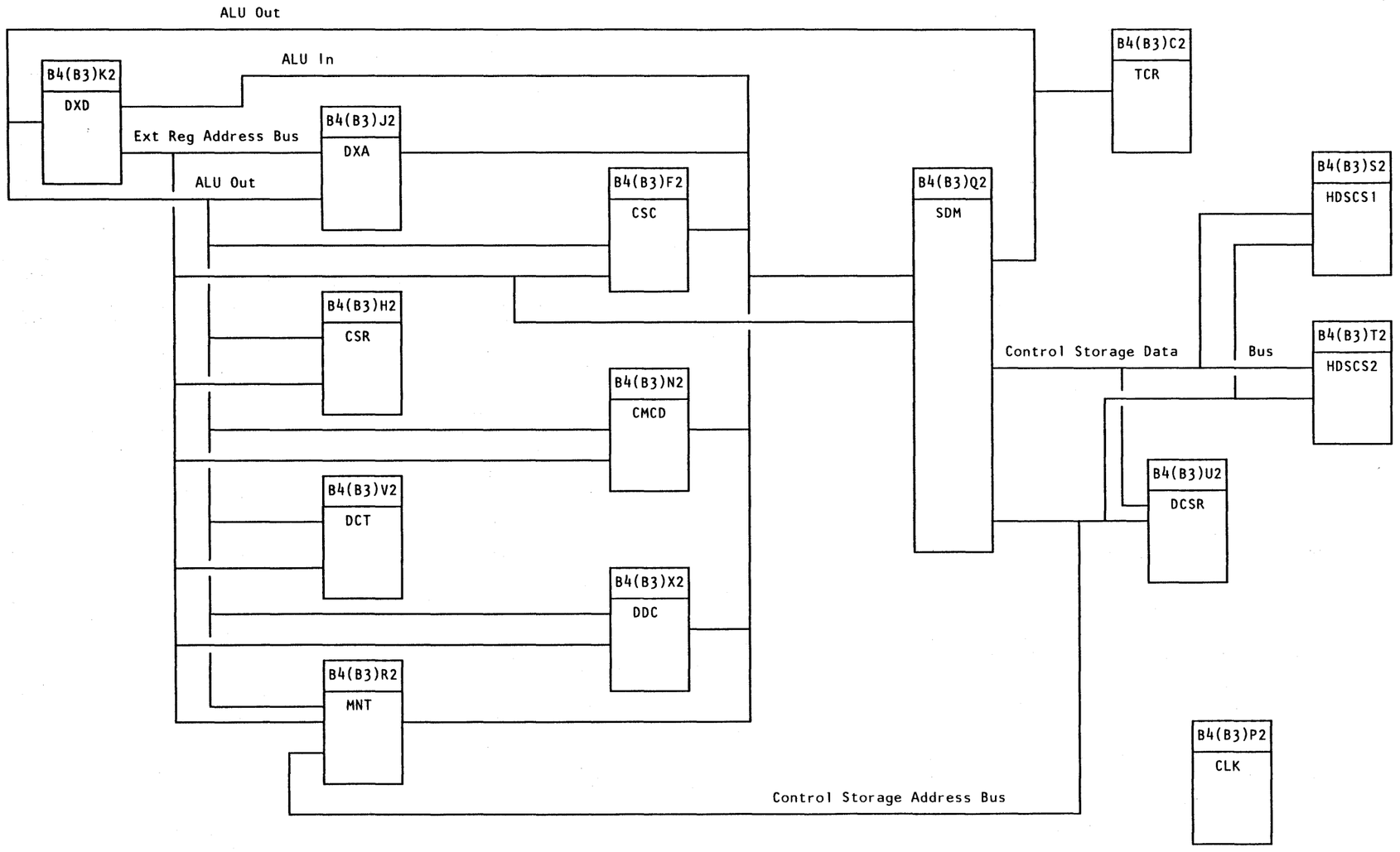
See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Error Code Diagram CTRL 5



Note: See Control Area Card Descriptions in the OPER section of the MSM for a detailed description of this area.

3880 ECM	Seq HO0001	PN 6315690 2 of 11	881145 13 Jan 84	881216 15 Aug 84	A15621 01 Apr 85		

IML Error Codes

IML 0F

IML ROS Selection Failure: Is caused by a failure on the maintenance device counter or storage director microprocessor cards. This failure results in the +ROS Select line remaining active after bit 1 of the maintenance/control sense register is turned off by the read-only storage (ROS) code. This failure results in a branch to a single instruction loop at ROS address X'010' with X'0F' in the external bus out register.

Card detecting the error:

01A-B4(B3)V2

FRU List

01A-B4(B3)R2 30%
01A-B4(B3)Q2 30%
01A-B4(B3)V2 30%

Diagnostic Check

Refer to Diagnostic Check 1 on page CTRL 50.

IML 20, 21, or 24,

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML 22

External Register Check: Is generated by the hardcore diagnostics when a failure occurs during the external register test. The test uses the device count low (DCL) register as the destination register to verify all external register operations.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2
01A-B4(B3)X2
01A-B4(B3)N2
01A-B4(B3)V2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 2 on page CTRL 50.

IML 23

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)P2
01A-B4(B3)S2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML 98, 99

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List IML 98

01A-B4(B3)S2 90%
01A-B4(B3)Q2

FRU List IML 99

01A-B4(B3)T2 90%
01A-B4(B3)Q2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML 9A

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List

01A-B4(B3)U2 90%
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML 9B

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML 9C

Interrupt Failure: Indicates that one of the following occurred:

- A failure to interrupt to a higher interrupt level from a lower interrupt level
- An interrupt level compare error on an interrupt
- A failure to interrupt to a lower interrupt level from a higher interrupt level

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2
01A-B4(B3)Q2
01A-B4(B3)V2
01A-B4(B3)J2
01A-B4(B3)K2
01A-B4(B3)M2
01A-B4(B3)C2
01A-B4(B3)F2
01A-B4(B3)P2
01A-B4(B3)E2

Diagnostic Check

Refer to Diagnostic Check 3 on page CTRL 50.

IML 9D

See DC HC00 in this manual for a cross reference chart of IML error codes to routine 70 tests.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page CTRL 50.

IML E0

Maintenance Interface Failure:

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2
01A-B4(B3)Q2
01A-B4(B3)F2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 8 on page CTRL 50.

IML E1

Control Store (0-4K) Read/Write Failure: Card detecting the error:

NONE

FRU List

01A-B4(B3)S2 90%
01A-B4(B3)Q2

Diagnostic Check

Refer to Diagnostic Check 8 on page CTRL 50.

IML E2

Control Store (0-4K) Read/Write Failure: Card detecting the error:

NONE

FRU List

01A-B4(B3)T2 90%
01A-B4(B3)Q2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 8 on page CTRL 50.

IML E3

Control Store (16-32K) Read/Write Failure:

Card detecting the error:

NONE

FRU List

01A-B4(B3)U2 90%
01A-B4(B3)Q2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 8 on page CTRL 50.

IML E4

SDM Fails to Restart After First DCS Cycle: Is the result of a failure to restart the SDM (Storage Director Microprocessor) clocks after the first dynamic control storage (DCS) cycle.

All DCS cycles require two machine cycles. In order to accomplish a DCS cycle, the SDM clocks are stopped for one cycle and then restarted.

Prior to the first DCS cycle, the external bus out (EBO) register is loaded with E4. If there is a failure that prevents the SDM clocks from restarting, a hang condition exists with IML E4 set in the EBO register.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)U2 50%
01A-B4(B3)R2 50%
01A-B4(B3)Q2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 6 on page CTRL 50.

IML E8

Microprocessor Error: Is a microprocessor error.

Card detecting the error:

NONE

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)P2
01A-B4(B3)U2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 8 on page CTRL 50.

IML E9

Common Register Failure: Indicates a register failure on the CMCD card.

Card detecting the error:

NONE

FRU List

01A-B4(B3)M2 70%
01A-B4(B3)L2 20%
01A-B4(B3)N2 10%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

IML EA

ADT/ASDM Buffer Card Failure: Indicates a register failure on the CMAA card.

Card detecting the error:

NONE

FRU List

01A-B4(B3)L2 90%
01A-B4(B3)M2
01A-B4(B3)J2
01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

IML EB

Common Register Failure: Indicates a register failure on the CMCA/CMCD card.

Card detecting the error:

NONE

FRU List

01A-B4(B3)M2 70%
01A-B4(B3)L2 20%
01A-B4(B3)N2 10%
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

IML EC

ASDM Failure: Indicates an ASDM failure on the CMAA card.

Card detecting the error:

NONE

FRU List

01A-B4(B3)L2 90%

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

SC 300F

SDM Internal Check: Occurs when incorrect parity is detected for any of the following reasons:

- A parity error in the IRG, MIRL, or MIRH registers
- A branch decision error
- A clock decoder error resulting from an invalid clock ring state

This check 1 error is latched in bit 2 of error register 3 and sets bit 4 of check register 1.

The check is reset by the -Reset line from the maintenance card.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)P2
01A-B4(B3)R2
01A-B4(B3)C2
CIFA 2X
CIFB 4X

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3104

Dynamic Control Storage Uncorrectable Data Check: Indicates that during a dynamic storage fetch cycle the data fetched had a double bit failure that could not be corrected. The dynamic control storage and refresh card (DCSR) has hardware error correction code (ECC) logic that performs single-bit error correction and double-bit error detection for all data fetched from dynamic storage.

During a dynamic storage store cycle six ECC check bits are automatically generated and stored with the 16 data bits received from the storage director microprocessor.

SC 3104 is a check 1 condition that stops the storage director clocks. The check is set in bit 5 of check register 1. This bit is reset by the Machine Reset, Power On Reset, System Reset or Selective Reset lines.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)U2 90% 01A-B4(B3)R2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3108

SDM Module Check: Is generated when bit 4 of check register 1 is on and bits 0 through 2 of check register 3 are off.

Bit 4 of check register 1 is the logical OR of bits 0 through 2 of check register 3. This check indicates that the check register 1, bit 4, latch failed or the OR circuit failed producing a -SDM Error Out. The check is reset by the Machine Reset command.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 60% 01A-B4(B3)R2
01A-B4(B3)P2 30%

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3110

SDM Card Check: Indicates that one of the following conditions was detected on the storage director microprocessor (SDM) Card.

- Control storage address parity check
- Invalid control storage data bus enable

The local storage address bus parity check is performed at -TC and +TB or +TC and -TB times. (These times correspond to the microprocessor T1 and T5 clock times.)

During an interrupt, the local storage address bus parity circuit also checks the interrupt address for correct parity.

The invalid control storage data bus enable check is the one, *and only one,* check, that ensures that only one control storage data bus select line is active at any one time. The enable lines checked are: Local Storage Enable, External Register Enable, ROS Enable, and Control Storage Select Enable. This error is reset by the -Reset line from the maintenance card, and is latched in bit 3 of check register 3.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)P2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3120

CSC ALU Out Check: Indicates that either the channel sequence control (CSC), the maintenance (MNT) card, or both, have detected invalid ALU bus out parity.

The checks ensure that data placed on the ALU bus out lines by the microprocessor is correct at the time that data on the bus is valid. This is a check 1 that stops the storage director clocks.

Incorrect parity on the ALU bus in lines generates incorrect parity on the ALU bus out lines whenever the Inhibit Bus In Check lines to the storage director microprocessor (SDM) card are inactive. The check condition is reset by the +Reset line from the MNT card.

The CSC card loads the contents of the ALU Bus Out lines into a series of latches when -Load Clock A line is active at T1 time. The check on these latches is made at T4 time.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 80% 01A-B4(B3)R2
01A-B4(B3)F2 10% 01A-B4(B3)N2
01A-B4(B3)P2 01A-B4(B3)H2
01A-B4(B3)C2 01A-B4(B3)E2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

SC 3140

External Register Address Parity Check: Is the result of a parity check performed by the maintenance (MNT) card on the External Register Address Bus. The external register address is generated on the storage director microprocessor (SDM) card and is valid when the External Register Select line is active. The check is performed at every T0 time and is latched in bit 1 of check register 1 on the MNT card. External register address parity check is a check 1 that stops the storage director clocks.

Incorrect parity on Control Store Data Out Bus during a microinstruction read operation can cause incorrect parity on the External Register Address Bus.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)N2
01A-B4(B3)R2
01A-B4(B3)F2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

SC 3180

MNT ALU Out Check: The MNT card performs the check directly on the ALU bus out lines at every T1 time. The parity check output latches error register 1, bit 0.

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)N2
01A-B4(B3)R2
01A-B4(B3)F2
01A-B4(B3)C2
01A-B4(B3)E2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

SC 31A0

CSC and MNT ALU Out Check: Indicates that both the CSC and MNT cards have detected invalid parity on the ALU bus out lines.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)N2
01A-B4(B3)R2
01A-B4(B3)V2
01A-B4(B3)F2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 5 on page CTRL 50.

SC 3201

Dynamic Control Storage Write Data Check: Indicates that a control storage data check is detected on the dynamic control storage and refresh card (DCSR) during a write cycle.

As a result of this check, there is a possibility that incorrect data is stored in the storage location being addressed.

A write data check is always treated as a solid failure. This data check cannot be reset by selective reset from the channel.

The DCSR card is checked for the write data check at 60 ns after the -Card Select line is active at T1 clock time.

This is a check 1 condition that stops the storage director clocks. The check is set into bit 7 of check register 2 and reset by the Machine Reset, Power On Reset, or System Reset lines.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 50%
01A-B4(B3)P2
01A-B4(B3)U2 40%
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3220

DCSR Card Check: Indicates that one of the following checks was detected by the dynamic control storage and refresh card:

- Refresh timer check
- Refresh address counter check
- A key bit check

Refresh Timer Check

To show that a refresh cycle is required, a refresh timer is located on the DCSR card. The timer is a 7-bit counter, which is incremented by the +Refresh Timer Clock line every T5 clock time. The refresh timer check indicates incorrect parity was detected in the refresh timer, which is checked after each increment.

Refresh Address Counter Check

During a refresh cycle, only a portion of the memory is refreshed. A counter is used to generate the block address for a portion of the memory to be refreshed. The refresh address check indicates incorrect parity in the parity address counter.

Key Bit Check

To provide address protection for data stored or fetched, a key bit is defined that acts as the 17th data bit in the generation of the six error correction code (ECC) check bits stored. The key bit is generated by exclusive ORing the CS Address Bit Parity line with CS Write Line. The key bit check indicates that when a data fetch is performed the key bit generated from the fetch address did not match the key bit stored.

The storage director clocks are stopped with a check 1 condition. The check is set in bit 2 of check register 2 and reset by the Machine Reset, Power On Reset, or Selective Reset lines.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)U2 90%
01A-B4(B3)P2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3240

Clock Card Check: Indicates that one of the following check conditions is detected:

- Clock Ring Check
- Hold Check
- Selection Check

Clock Ring Check

The clock ring check occurs when more than one of the non-overlapping gates on the clock ring are active at the same time.

Hold Check

The hold check occurs when a dynamic control storage cycle is initiated by the storage director microprocessor (DCS Select line is active), but the corresponding hold signal is not generated. The hold signal is internal to the clock card.

Selection Check

A selection check occurs on the DCSR card when more than one select signal is active at the same time. The select signals check are:

- Refresh Select
- DCS Select 0
- DCS Select 1
- DCS Select 2

An internal DCSR delay allows the leading edge of the -Refresh Select line to overlap the -DCSR Select line by 35 ns without a check condition.

The storage director clocks are stopped with a check 1 condition. The check is set in bit 1 of check register 2 and reset by the Power On Reset, Machine Reset, or Selective Reset lines.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)P2 90%
01A-B4(B3)Q2
01A-B4(B3)U2 10%
01A-B1E2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SCs 34xx and 3Axx

ALU Bus In Check: SCs 34xx and 3Axx indicate that the SDM card detected invalid parity on the ALU Bus In lines when the contents of an internal or external register was being gated to the ALU.

Because of the large number of cards involved in this check, FRU registers 2, 3, and 4 hold data to aid in analyzing the symptom code and reduces the number of cards. Bits 0 through 3 of FRU Register 2 and bit 3 of FRU Register 3 indicate the card that performed the register address decode. Bit 4 of the FRU Register 2 indicates whether an external or internal register was being gated to ALU. Bits 3 through 7 of FRU Register 4 contain the address of the external register being gated to ALU.

The check conditions are reset by +Reset from the MNT card.

SC 34xx

Selection Check: Symptom codes are generated when an ALU Bus In check is detected and more than one card decoded the external register address. This symptom code indicates that the cards with the decoders are the cause of the ALU In Check.

The 34xx symptom codes are:

SC 3401

Selection Check MNT and DDC cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)V2 50%
01A-B4(B3)R2 40%

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3402

Selection Check MNT and DXD cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)K2 50%
01A-B4(B3)R2 40%

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3403

Selection Check MNT and CSC cards:

Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)R2 50%
01A-B4(B3)F2 40%

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3404

Selection Check CSC and DDC cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)F2 50%
01A-B4(B3)X2 40%
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3405

Selection Check DDC and DXD cards:

Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)K2 50% 01A-B4(B3)V2
01A-B4(B3)X2 40% 01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3406

Selection Check DXD and CSC cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)K2 50% 01A-B4(B3)R2
01A-B4(B3)F2 40% 01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3410

Selection Check MNT and CMCD cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)N2 50%
01A-B4(B3)R2 40%

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3411

Selection Check DDC and CMCD cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)N2 50% 01A-B4(B3)R2
01A-B4(B3)X2 40%

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3412

Selection Check DXA and CMCD cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)N2 50% 01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3413

Selection Check CSC and CMCD cards: Card detecting the error:

01A-B4(B3)R2
01A-B4(B3)Q2

FRU List

01A-B4(B3)N2 50% 01A-B4(B3)R2
01A-B4(B3)F2 40% 01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3600, 3601, 3602, or 3604

Static Control Storage Address Check or ROS Select Check: Indicates that incorrect parity is detected on the control storage address bus lines during a static or dynamic control storage cycle or that an invalid ROS selection occurred.

The address check on the static control storage cards (SCS-1 and SCS-2 is performed across CS address bits 4 through 15 on all storage cycles. The address check on the dynamic control storage and refresh (DCSR) card is performed across bits 2 through 15 and the -CS Write line only during a dynamic storage cycle.

The storage director microprocessor (SDM) card samples the parity check signal with a polarity hold (PH) latch during each control storage (CS) cycle. The maintenance (MNT) card samples this latch after it has settled at T6 time.

This check condition is latched on the MNT card in bit 6 of check register 2. It is a check 1 error that stops the storage director clocks.

A read-only storage (ROS) check occurs when the +ROS Select line is active at any time other than during IML or selective reset. A ROS select check can also occur during the selection of static control storage 1 (SCS1) or SCS2. It is ORed with CS Address Check on the MNT card.

These checks are reset by -Reset from the MNT card.

SC 3600

SC 3600 is generated when check register 2 bit 6 = 1 and FRU register 3 bits 0 and 1 = 00. This indicates that SCS 1 (0-4K) was being addressed at the time the check occurred.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 70% 01A-B4(B3)P2
01A-B4(B3)S2 10% 01A-B4(B3)V2
01A-B4(B3)T2 10% 01A-B4(B3)C2
01A-B4(B3)U2 01A-B4(B3)F2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3601

SC 3601 is generated when check register 2 bit 6 = 1 and FRU register 3 bits 0 and 1 = 01. This indicates that HDSCS 1 (4-8K) was being addressed at the time the check occurred.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 70% 01A-B4(B3)R2
01A-B4(B3)T2 10% 01A-B4(B3)P2
01A-B4(B3)S2 10% 01A-B4(B3)V2
01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3602

SC 3602 is generated when check register 2 bit 6 = 1 and FRU register bits 0 and 1 = 1x. This indicates that SCS3 (8-12K) was being addressed at the time the check occurred.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 70% 01A-B4(B3)P2
01A-B4(B3)T2 10% 01A-B4(B3)V2
01A-B4(B3)S2 10% 01A-B4(B3)C2
01A-B4(B3)U2 01A-B4(B3)F2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3604

SC 3604 occurs when check register 2 bit 6 = 1 and FRU register 3 bit 2 = 1. This indicates that dynamic control storage (16-32K) is being addressed at the time the check occurred.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 70% 01A-B4(B3)R2
01A-B4(B3)U2 10% 01A-B4(B3)P2
01A-B4(B3)S2 10% 01A-B4(B3)V2
01A-B4(B3)T2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SCs 3800, 3801, 3802, 3803, 3804, or 3805

SCs 3800, 3801, 3802, 3803, 3804, and 3805 indicate that a control storage data check was detected on the storage director microprocessor (SDM) card during an instruction or data read cycle.

The check is performed during a control storage read operation at T2 time (this is an SDM internal T2 time). The check is reset by machine reset. Because the high density control storage (HDSCS) cards share a common bidirectional bus, the data in FRU registers 2 and 3 is analyzed to generate the specific symptom codes whenever a control storage (CS) data check is detected. Bit 7 in FRU register 2 is set whenever a read only storage (ROS) operation is performed. Bits 0 through 2 of FRU register 3 contain CS address bits 2, 3, and either 0 or 1. The contents of FRU register 3 are decoded in the following chart.

BIT 0 1 2	BIT SIGNIFICANCE
0 x 0	Static control storage 1
1 x 0	Static control storage 2
x x 1	Dynamic control storage

SC 3800

SC 3800 indicates that the check occurred during a control storage read operation from the (0-4K) HDSCS-1 or SCS-1 card (FRU register 2, bit 7 equals 0, and FRU register 3, bits 0 through 2 equal 000).

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)S2 90% 01A-B4(B3)F2
01A-B4(B3)Q2 CIFA 2X
01A-B4(B3)T2 CIFB 4X
01A-B4(B3)U2 01A-B4(B3)C2
01A-B4(B3)P2 01A-B4(B3)V2
01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3801

SC 3801 indicates that the check occurred during a control storage read operation from the (4-8K) HDSCS-1 card (FRU register 2, bit 7 equals 0, and 2 FRU register 3, bits 0 through 2 equal 010).

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)T2 90% 01A-B4(B3)R2
01A-B4(B3)S2 01A-B4(B3)F2
01A-B4(B3)Q2 CIFA,2X
01A-B4(B3)U2 CIFB 4X
01A-B4(B3)P2 01A-B4(B3)C2
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

Symptom Codes

SC 3802

SC 3802 indicates that a read operation was attempted from an invalid control store address.

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%
01A-B4(B3)R2
01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3803

SC 3803 indicates that the check occurred during a control storage read operation from the (12-16K) HDSCS-2 card (FRU register 2, bit 7 equals 0, and 2 FRU register 3, bits 0 through 2 equal 100).

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)T2 90%	01A-B4(B3)R2
01A-B4(B3)Q2	01A-B4(B3)F2
01A-B4(B3)S2	CIFA,2X
01A-B4(B3)U2	CIFB 4X
01A-B4(B3)P2	01A-B4(B3)C2
	01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3804

SC 3804 indicates that the check occurred during a control storage read operation from the (16-64K) dynamic control storage card, (FRU register 2 bit 7 equals 0 and FRU register 3 bit 2 = 1).

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)U2 90%	01A-B4(B3)F2
01A-B4(B3)Q2	CIFA 2X
01A-B4(B3)S2	CIFB 4X
01A-B4(B3)T2	01A-B4(B3)C2
01A-B4(B3)P2	01A-B4(B3)V2
01A-B4(B3)R2	01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 4 on page CTRL 50.

SC 3805

SC 3805 indicates that the check occurred during a read only storage (ROS) read operation. The ROS arrays are on the SDM card (FRU register 2 bit 7 equals 1).

Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%	01A-B4(B3)U2
01A-B4(B3)S2	01A-B4(B3)P2
01A-B4(B3)T2	01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 1 on page CTRL 50.

SC 380F

SC 380F occurs when a control storage (CS) data check is detected during a power on. The CS data check is caused by an active system or selective reset.

System Reset

System reset occurs when the operational out and suppress out lines are concurrently inactive, and an I/O device is online. This condition causes the operational in line to become inactive. It also resets all attached control units, devices and status lines.

Selective Reset

Selective reset occurs when the suppress out line is active and the operational out line is inactive.

This condition causes the operational in line to become inactive. It also causes the device and the status line to reset. The device end line is returned to the storage director after the reset. To be effective, the suppress out line must be active for 250 nanoseconds (ns) before operational out line is inactive. The suppress out must remain active for 250 ns after operational out becomes active. The operational out line must stay inactive until operational in line is inactive or for 6 microseconds.

SC 3Axx

ALU Bus In Check: Symptom codes are generated whenever a single card decodes the external register address and an ALU Bus In Check is detected. The external register address is used to determine which card the register is on. A unique symptom code is generated for each card that feeds the ALU. The 3Axx symptom codes are:

SC 3A01

SDM ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)Q2 90%	01A-B4(B3)H2
01A-B4(B3)N2	01A-B4(B3)P2
01A-B4(B3)X2	01A-B4(B3)V2
01A-B4(B3)F2	01A-B4(B3)C2
01A-B4(B3)R2	01A-B4(B3)S2
01A-B4(B3)J2	01A-B4(B3)T2
01A-B4(B3)K2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A02

DDC ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)X2 70%	01A-B4(B3)H2
01A-B4(B3)N2 10%	01A-B4(B3)P2
01A-B4(B3)F2 10%	01A-B4(B3)V2
01A-B4(B3)Q2	01A-B4(B3)C2
01A-B4(B3)R2	01A-B4(B3)S2
01A-B4(B3)J2	01A-B4(B3)T2
01A-B4(B3)K2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A03

CSR ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)H2 70%	01A-B4(B3)K2
01A-B4(B3)N2 10%	01A-B4(B3)P2
01A-B4(B3)X2 10%	01A-B4(B3)V2
01A-B4(B3)F2 10%	01A-B4(B3)C2
01A-B4(B3)Q2	01A-B4(B3)S2
01A-B4(B3)R2	01A-B4(B3)T2
01A-B4(B3)J2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A04

DXA or DXD ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)J2 40%	01A-B4(B3)H2
01A-B4(B3)K2 20%	01A-B4(B3)Q2
01A-B4(B3)X2	CIFx
01A-B4(B3)F2	01A-B4(B3)V2
01A-B4(B3)R2	01A-B4(B3)S2
01A-B4(B3)G2	01A-B4(B3)T2
01A-B4(B3)P2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A05

CSC ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)F2 70%	01A-B4(B3)H2
01A-B4(B3)N2 10%	01A-B4(B3)V2
01A-B4(B3)X2 10%	01A-B4(B3)C2
01A-B4(B3)Q2	01A-B4(B3)E2
01A-B4(B3)R2	01A-B4(B3)S2
01A-B4(B3)K2	01A-B4(B3)T2
01A-B4(B3)J2	01A-B4(B3)U2
CIFx	01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A06

MNT ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)R2 70%	01A-B4(B3)Q2
01A-B4(B3)N2 10%	01A-B4(B3)P2
01A-B4(B3)X2 10%	01A-B4(B3)V2
01A-B4(B3)F2 10%	01A-B4(B3)C2
01A-B4(B3)J2	01A-B4(B3)S2
01A-B4(B3)K2	01A-B4(B3)T2
01A-B4(B3)H2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A07

DCT ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)V2 70%	01A-B4(B3)K2
01A-B4(B3)N2 10%	01A-B4(B3)H2
01A-B4(B3)X2 10%	01A-B4(B3)C2
01A-B4(B3)F2 10%	01A-B4(B3)P2
01A-B4(B3)Q2	01A-B4(B3)S2
01A-B4(B3)R2	01A-B4(B3)T2
01A-B4(B3)J2	01A-B4(B3)U2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

SC 3A10

CMCD ALU Bus In Check: Card detecting the error:

01A-B4(B3)R2

FRU List

01A-B4(B3)N2 90%	01A-B4(B3)Q2
01A-B4(B3)X2	01A-B4(B3)R2

Diagnostic Check

Refer to Diagnostic Check 7 on page CTRL 50.

Symptom Codes CTRL 45

Diagnostic Checks

Diagnostic Check 1

1. Power off the failing storage director and check for an open circuit between the input and output pins of the +ROS Select and +Start DXR Clock lines.

2. Power off the failing storage director and remove all cards shown in the FRU list. Check all nets with a CE meter for an open, a short between nets, a short between a net pin and ground pin, or a voltage pin. See the MDM for voltage pin lists.

3. Select the MD support mode and loop on IML failure (see the MD section in the MSM). While the test is looping, check the nets on the cards indicated on the FRU list with an oscilloscope for incorrect levels or misshapen pulses.

Diagnostic Check 2

1. Power off the failing storage director and check for an open circuit between the input and output pins on the cards shown in the FRU list.

2. Remove the cards and check the pins on the cards shown in the FRU list for a short circuit to another circuit or a voltage pin. See the MDM for voltage pin lists.

3. Select the MD support mode and bypass the IML error halt (see the MD section in the MSM). Load diagnostic routine 70 and loop function test '0A'. Check the nets on the cards indicated in the FRU list with an oscilloscope for incorrect levels.

   Note: See the DC section of this manual for a description of routine 70, test '0A'.

Diagnostic Check 3

1. Power off the failing storage director and remove all cards shown in the FRU list. Check all nets with a CE meter for an open, a short between nets, a short between a net pin and ground pin, or a voltage pin. See the MDM for voltage pin lists.

2. Select the MD support mode and bypass the IML error halt (see the MD section in the MSM). Load diagnostic routine 70 and loop function test '07'. Check the nets on the cards indicated in the FRU list with an oscilloscope for incorrect levels.

   Note: See the DC section of this manual for a description of routine 70, test '07'.

Diagnostic Check 4

1. Select the MD symptom analysis option and enter the symptom code. Replace the cards and crossovers that have not previously been replaced.

2. Reset the failing storage director and verify that the nets on the cards indicated on the FRU list are inactive. Power off the failing storage director and check for an open circuit between the input and output pins of the cards indicated on the FRU list.

3. Power off the failing storage director. Remove all cards shown on the FRU list and check all nets with a CE meter. Check and repair an open or short circuit between nets, grounds, or voltage pins. See the MDM for voltage pin lists.

4. Select the MD support mode and loop on the check 1 clock stop error (see the MD section in the MSM). Check the nets shown on the FRU list with an oscilloscope for incorrect levels or misshapen pulses.

Diagnostic Check 5

1. Select the MD symptom analysis option and enter the symptom code. Replace the cards and crossovers listed by the MD that have not previously been replaced.

2. Power off the failing storage director. Check for an open circuit between the ALU bus out pins at the input to the maintenance (MNT) and channel sequence control (CSC) cards starting with the card that is detecting the check.

3. Power on, reset the failing storage director, and verify that the ALU bus out circuits (including the parity bit) are inactive. Also verify that the +Inhibit Bus In Check line to the storage director microprocessor (SDM) card is inactive.

4. Power off the failing storage director. Remove all cards shown on the FRU list and check all nets with a CE meter. Check and repair an open or short circuit between nets, grounds, or voltage pins.

5. Select the MD support mode and loop on check 1 clock stop error (see the MD section in the MSM). Check the circuits on the cards indicated on the FRU list with an oscilloscope for incorrect levels or misshapen pulses while the test is looping.

Diagnostic Check 6

1. Reset the failing storage director and ensure that all pins on the cards shown on the FRU list are inactive.

2. Power off the failing storage director. Remove all cards shown on the FRU list and check all nets with a CE meter. Check and repair an open or short circuit between nets, grounds, or voltage pins.

3. Select the MD support mode and loop on IML failure (see the MD section in the MSM). While the test is looping, check the nets shown on the cards indicated in the FRU list with an oscilloscope for incorrect levels or misshapen pulses.

   Note: See DC INTRO in this manual for a description of the read only storage (ROS) hardcore diagnostics.

Diagnostic Check 7

1. Select the MD symptom analysis option and enter this symptom code. Replace the cards and crossovers called out that have not been replaced.

2. Power off the failing storage director and check for an open circuit between the ALU Bus In 1, ALU Bus In 2, and External Register Address Bus input and output pins. Turn the power on, reset the failing storage director, and verify that the ALU Bus In 1, ALU Bus In 2, and external register address bus pins are inactive.

3. Power off the failing storage director and remove the cards shown in the FRU list. Check the circuits on the cards shown in the FRU list for an open or short circuit between nets, ground, or voltage pins.

4. Select the MD support mode and loop on check 1 clock stop error (see the MD section in the MSM). Check the nets shown on the cards indicated in the FRU list with an oscilloscope for incorrect levels or misshapen pulses while the test is looping.

Diagnostic Check 8

See DC RS00 in this manual for a description of the read-only storage (ROS) hard core diagnostics. Loop on the IML failure.

Channel Interface

Contents of This Section

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
26	20	2	C17
27	20	2	C17
28	20	2	C17
29	20	2	C17
2A	20	2	C17
2B	20	2	C17
2C	20	2	C17
2D	20	2	C17
34	20	2	C17
35	20	2	C17
36	20	2	C17
39	20	2	C17
3E	20	2	C17
3F	20	2	C17
5E	25	2	D01
5F	25	2	D01
61	25	2	D01
62	25	2	D01
63	25	2	D01
64	30	2	D03
65	30	2	D03
66	30	2	D03
67	30	2	D03
68	30	2	D03
69	30	2	D03
6A	30	2	D03
6B	30	2	D03
6C	30	2	D03
91	35	2	D05
92	35	2	D05
93	35	2	D05
94	35	2	D05
95	35	2	D05
96	35	2	D05
97	35	2	D05
C6	35	2	D05
C7	35	2	D05
C9	35	2	D05
CA	35	2	D05
CB	35	2	D05
CC	35	2	D05
D1	35	2	D05

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
0F00	40	2	D07
0F00-0	40	2	D07
0F00-2	40	2	D07
0F00-5	40	2	D07
0F01	40	2	D07
0F02	40	2	D07
0F03	40	2	D07
0F04	40	2	D07
0F05	40	2	D07
0F06	40	2	D07
0F07	40	2	D07
2040	45	2	D09
2520	45	2	D09
270x	45	2	D09
2708	45	2	D09
270B	45	2	D09
27Fx	45	2	D09
3B0x	50	2	D11
3B1x	50	2	D11
3B2x	55	2	D13
3B3x	55	2	D13
3C3x	55	2	D13
3C4x	60	2	D15
3C6x	60	2	D15
3D10	60	2	D15
3D20	60	2	D15
3D3x	65	2	D17
3D4x	65	2	D17
3D5x	65	2	D17
3Exy	65	2	D17
3F0x	65	2	D17
3F1x	65	2	D17
3F2x	70	2	E01
78xx	75	2	E03
FF01	80	2	E05
FF02	80	2	E05
FF03	80	2	E05
FF04	80	2	E05
FF05	80	2	E05
FF06	80	2	E05
FF07	85	2	E07
FF08	85	2	E07
FF09	85	2	E07
FF0A	85	2	E07

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

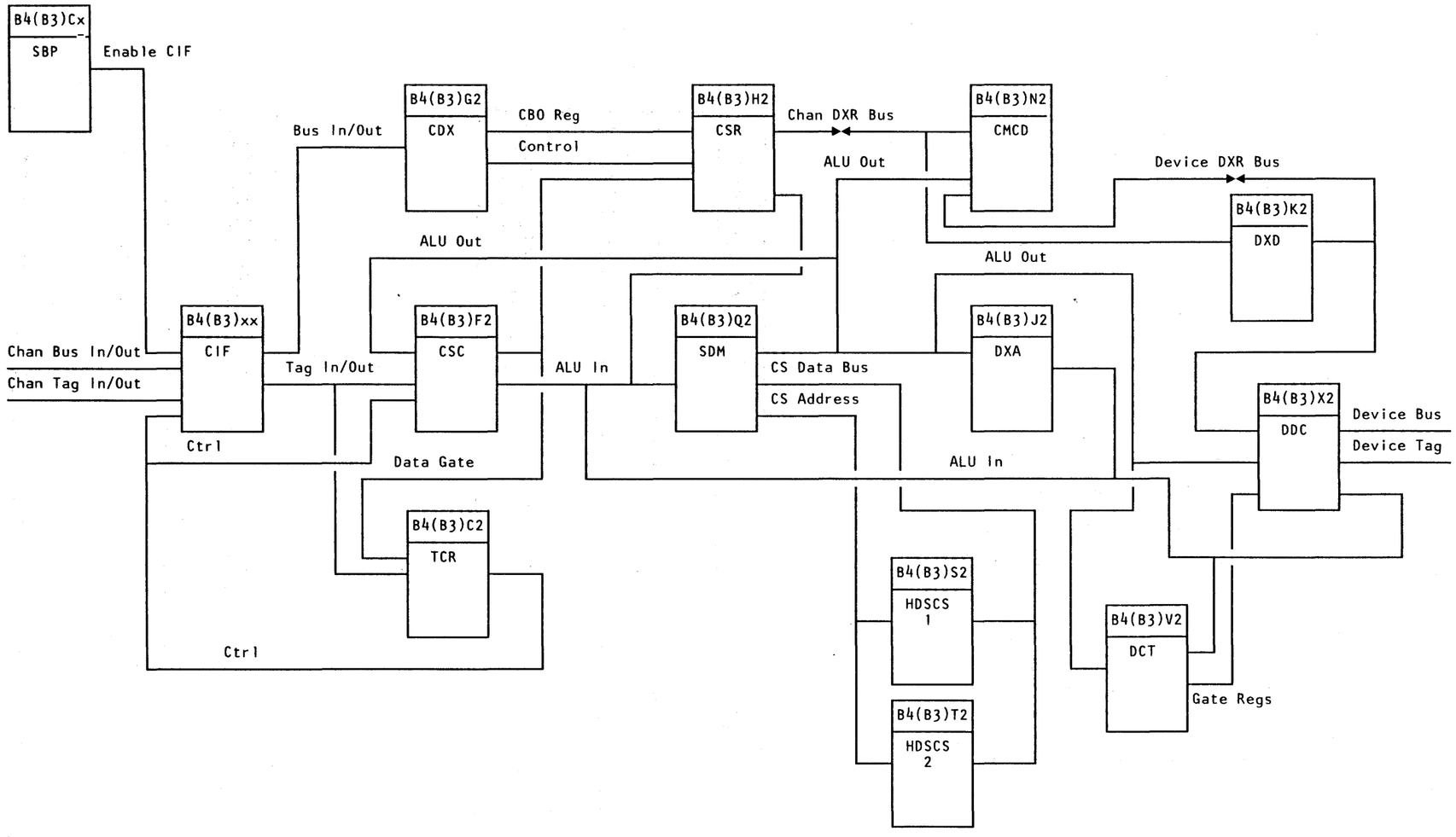
See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Note: If (TCA) appears in the error description the error and the FRU List also apply to the Two Channel Additional Feature.

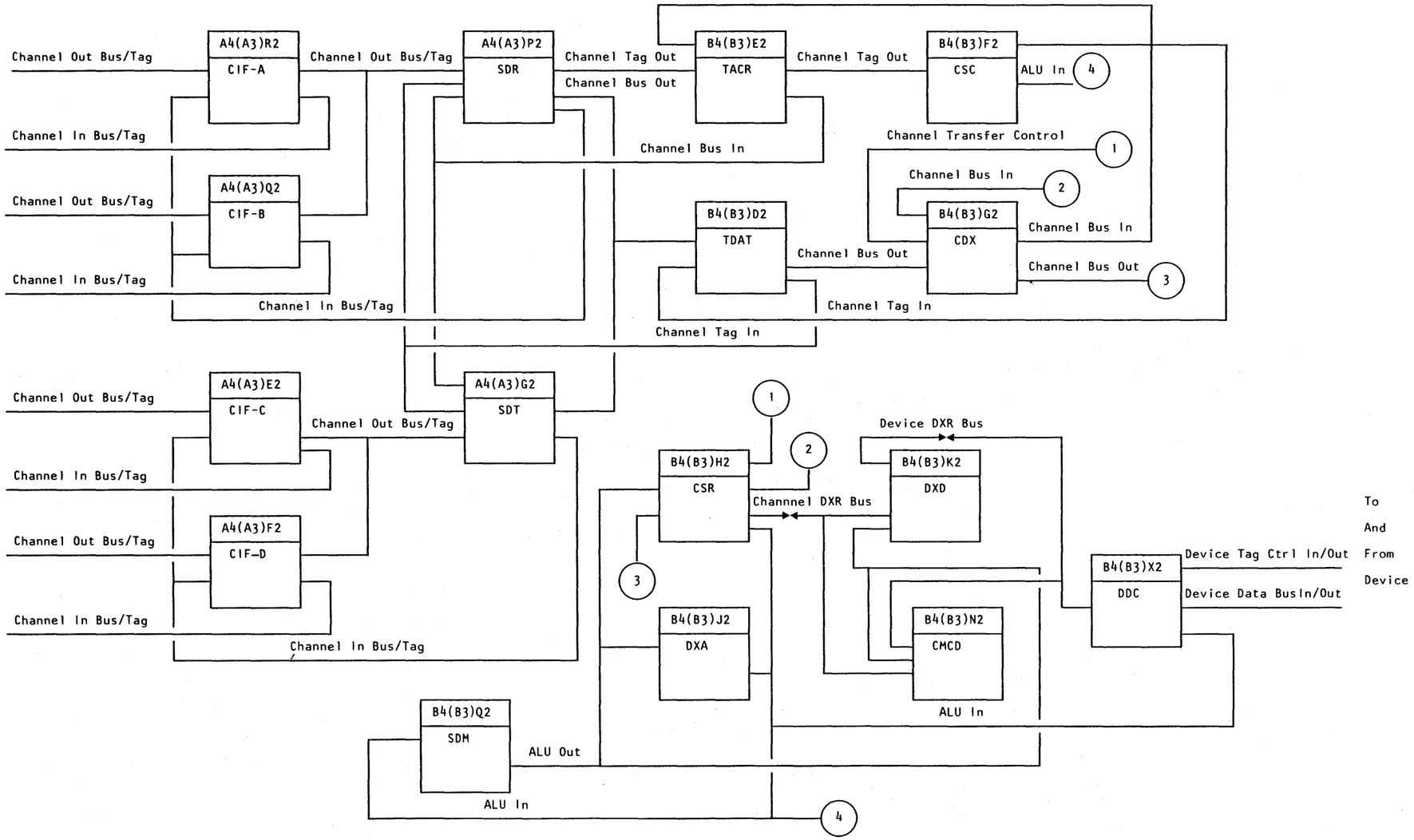
Numbers within parentheses indicate SD2.

Two Channel Switch-Pair



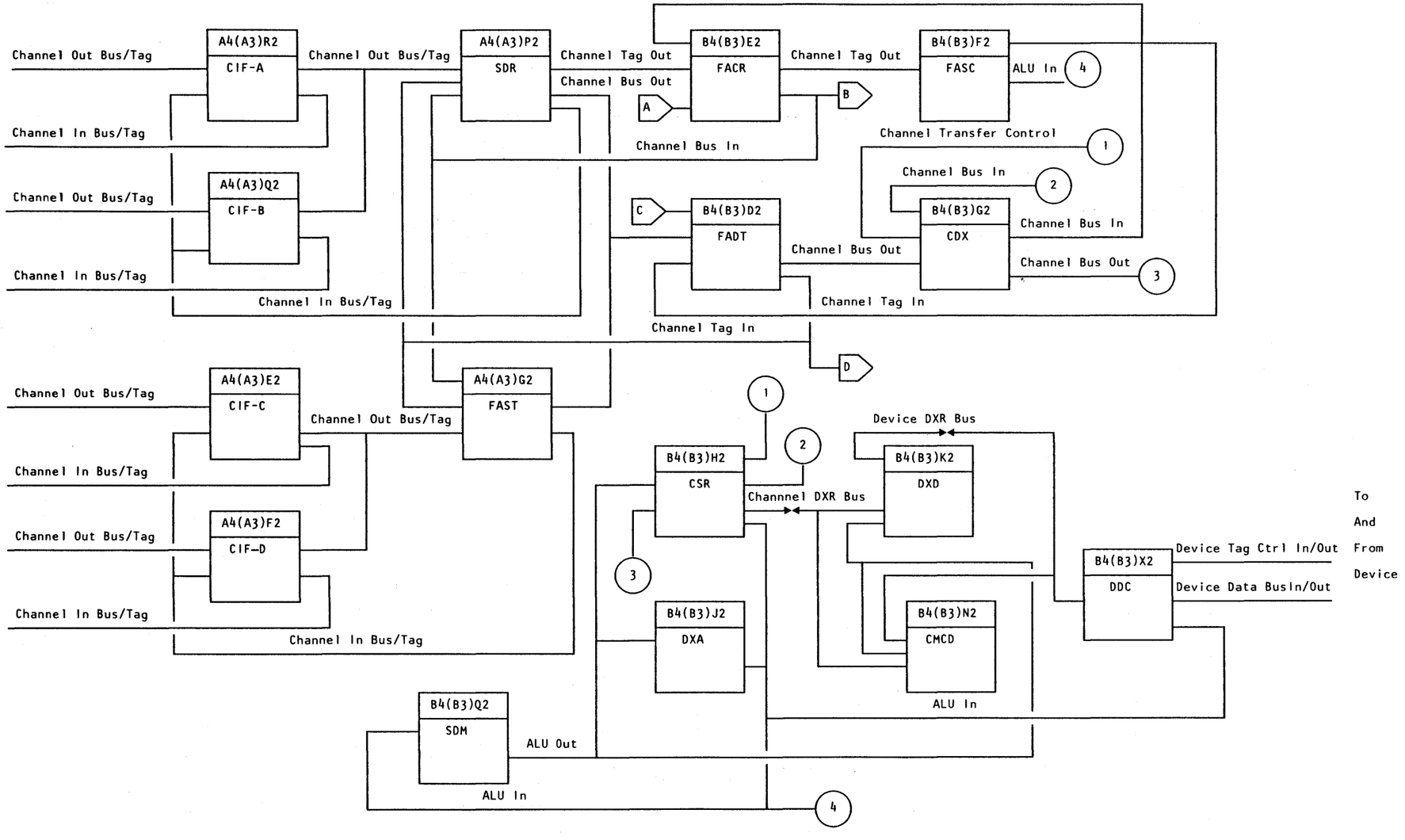
Note: See the OPER section of the MSM for a detailed description of this area

Two Channel Switch-Pair Additional



Note: See the OPER section of the MSM for a detailed description of this area

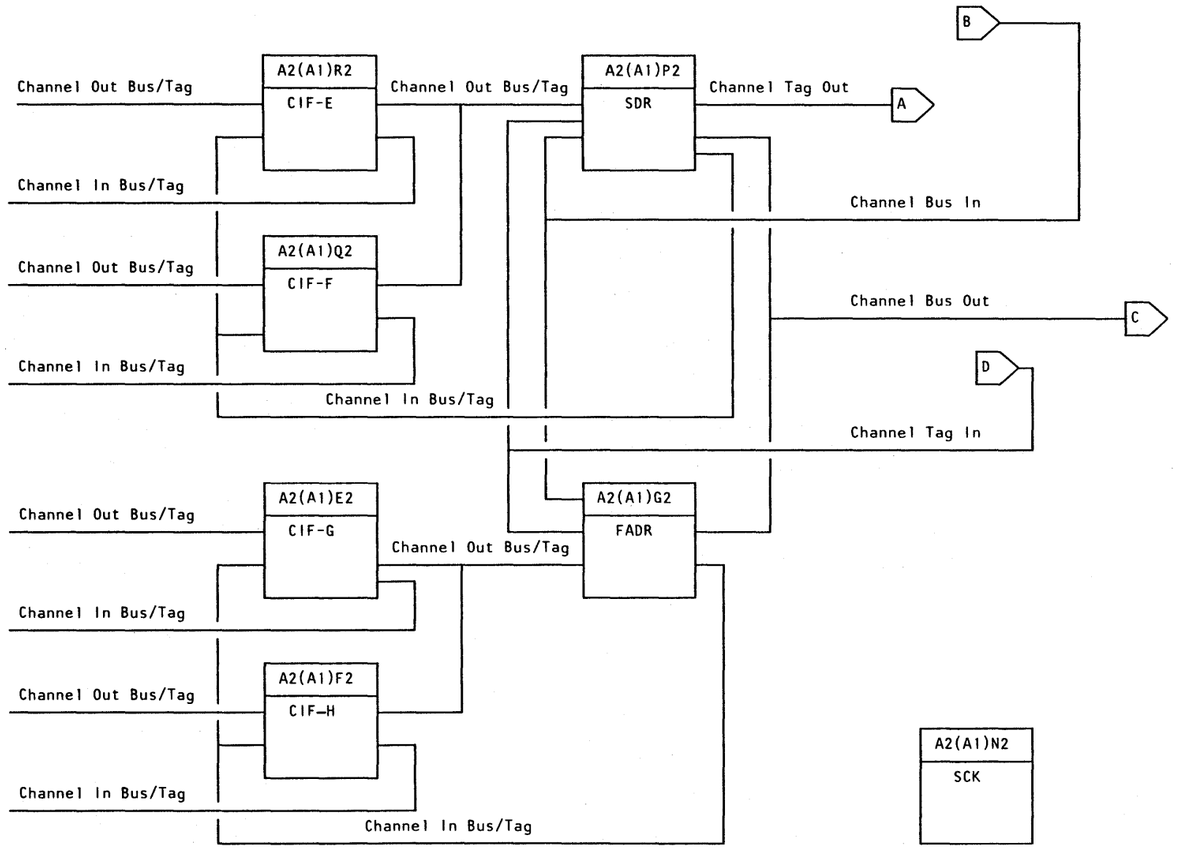
Four Channel Switch Additional



Note: See the OPER section of the MSM for a detailed description of this area

3880 ECM							
	Seq HQ0001	PN 6315691 4 of 20	881145 13 Jan 84	881216 15 Aug 84	A15621 01 Apr 85		

Four Channel Switch Additional (Continued)



IML 26, 27, 28, 29, 2A, 2B, 2C, or 2D

Failure to Reset an External Register (TCA): Error codes result when a machine reset fails to reset an external register.

Card detecting the error:

NONE

FRU List

IML 26 DXD FAILURE

MNT SWITCH
01A-B4(B3)H2 70%
01A-B4(B3)J2 20%
01A-B4(B3)K2
01A-B4(B3)N2
01A-B4(B3)R2
01A-B4(B3)V2
01A-B4(B3)X2

Diskette load switches on the MNT card

IML 27 DDC FAILURE

01A-B4(B3)X2 80%
01A-B4(B3)R2 10%
01A-B4(B3)V2

IML 28 DCT FAILURE

01A-B4(B3)V2 80%
01A-B4(B3)R2 10%
01A-B4(B3)K2
01A-B4(B3)P2

IML 29 CSR FAILURE

01A-B4(B3)H2
01A-B4(B3)R2
01A-B4(B3)G2
01A-B4(B3)K2
01A-B4(B3)Q2
01A-B4(B3)F2

IML 2A CDX FAILURE

01A-B4(B3)G2 60%
01A-B4(B3)R2 30%

IML 2B CSC FAILURE

01A-B4(B3)F2
CIFA 2X
CIFB 4X
01A-B4(B3)R2
01A-B4(B3)C2
01A-A4(A3)N2

IML 2C TCR FAILURE

01A-A4(A3)P2
01A-B4(B3)C2
01A-B4(B3)E2
01A-B4(B3)F2
01A-B4(B3)R2

IML 2D MNT FAILURE

01A-B4(B3)R2 90%

Diagnostic Check

Refer to Diagnostic Check 2 on page CHL-I 100.

IML 34

CDX Clock Check (TCA): Occurs when a machine reset fails to reset transfer error sense register, bit 3 (clock check 2), and channel interface check register, bit 2 (CDX card check). IML 34 indicates that the channel data transfer (CDX) card detected a clock check following the machine reset.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)G2
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 35

CSC Clock Check (TCA): Indicates that the -Clock Check Two line is active. The channel sequence control (CSC) card check and clock check 2 bits are on.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)G2
01A-B4(B3)F2
01A-B4(B3)P2
01A-B4(B3)Q2
01A-B4(B3)E2
CSC Switches

Diagnostic Check

Place the failing storage director in an IML loop (see the MD section of the MSM). Scope all the nets associated with the -Clock Check Two line and check for incorrect levels or misshapen pulses.

IML 36

CIF Clock Check (TCA): Indicates that an active channel interface (CIF) clock check bit is detected during an IML operation. The CIF card check and clock check 2 bits are on.

Card detecting the error:

01A-B4(B3)F2

FRU List

CIFA 2X
CIFB 4X
01A-B4(B3)P2

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 39

Channel Overrun (TCA): Occurs when a machine reset fails to reset transfer error status (XES) register, bit 1.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)G2
01A-B4(B3)J2

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 3E

CSR CARD CHECK: Occurs when a machine reset does not reset check register bit 2 (CSR card check 2).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2 70%
01A-B4(B3)J2

Diagnostic Check

Bypass the IML error halt. Select and load diagnostic 70 and select the following test:

- IML 3E – loop function test '0F'.

IML 3F

Channel Data Check (TCA): Occurs when a machine reset fails to reset check register bit 3 (channel data check).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2 70%
01A-B4(B3)J2 20%
01A-B4(B3)G2

Diagnostic Check

Refer to Diagnostic Check 2 on page CHL-I 100.

IML Error Codes

IML 5E

CIF Card Check (FCA): Indicates that an active CIF clock check bit is detected during an IML operation for channels E, F, G, H. This hardware-detected failure is the result of the -CIF Check Latched line which sets CRO register bit 5 (CIF Card Check).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-A4(A3)N2 CIFH
CIFE 01A-B4(B3)F2
CIFF
CIFG

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

IML 5F

Channel Clock Check (FCA): Indicates that an active channel clock check bit is detected during an IML operation for channels E, F, G, H. This hardware-detected failure is the result of the -Clock Check Latched line which sets CRO register bit 5 (Channel Clock Check E-H).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)F2 CIFG
01A-A4(A3)N2 CIFH
CIFE 01A-A4(A3)P2
CIFF 01A-A4(A3)D2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

IML 61

CHANNEL Bus In Parity Check (TCA): Indicates that an active channel bus in parity check (channel interface check register, bit 0) is detected during an initial microcode load procedure.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2
01A-B4(B3)G2

Diagnostic Check

Reset the failing storage director and ensure that the -Chan Bus In Parity Check line 01A-B4(B3)D2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

IML 62

CIF Card Check (TCA): Indicates that an active CIF card check (channel interface check register, bit 1) is detected during the hardcore tests.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2

Diagnostic Check

Reset the failing storage director and ensure that the -Cif Card Check line 01A-B4(B3)D2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

IML 63

CDX Card Check (TCA): Occurs when a machine reset does not reset channel interface checks (CRO) register, bit 2 (CDX card check).

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)G2 01A-B4(B3)F2
01A-B4(B3)H2

Diagnostic Check

Reset the failing storage director and ensure that the -CDX Card Check line 01A-B4(B3)G2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

IML 64

CSR Card Check Not Reset (TCA): Occurs if a machine reset fails to reset channel interface checks (CRO) register, bit 3 (CSR card check).

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)H2 01A-B4(B3)G2
01A-B4(B3)F2

Diagnostic Check

Reset the failing storage director and ensure that the -CSR Card Check 1 line 01A-B4(B3)H2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

IML 65

Channel Clock Check (FCA): Indicates that an active channel clock check bit is detected during and IML operation for channels A, B, C, D. This hardware-detected failure is the result of the - Clock Check Latched line which sets CRO register bit 5 (Channel Clock Check A-D).

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)P2
01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

IML 66

FACR/TACR Card Check: Indicates that the channel status 2 register, bit 3, is set during an IML operation.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)E2 90%
01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 67

CSC Card Check (TCA): Indicates that an active channel sequence control (CSC) card check bit (channel status 2 register, bit 4) is detected during hardcore tests.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2
CSC Switches

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 68

Channel Bus Out Parity Check: Indicates that an active channel bus out deskew register parity check (channel status 2, bit 5) occurred during an IML operation.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 2 on page CHL-I 100.

IML 69

TCR Card Check (TCA): Indicates that an active two-channel condition register (TCR) card check (channel status 2 register, bit 5) is detected during the hardcore tests.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)C2
01A-B4(B3)F2

Diagnostic Check

Reset the failing storage director and ensure that the -TCR Card Check line 01A-B4(B3)C2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

IML 6A

Channel Check 1 (TCA): Indicates that a channel check 1 (channel status register, bit 7) occurred during an IML operation.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

IML 6B

Halt I/O, System Reset, or Selective Reset: Indicates that a halt I/O, system reset or selective reset (channel status register bits 0, 1, or 2) is active during an IML operation.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 2 on page CHL-I 100.

IML 6C

Channel Clock Check (FCA): Indicates that an active channel clock check bit is detected during an IML operation for channels A, B, C, D. This hardware-detected failure is the result of the -Clock Check Latched line which sets CRO register bit 5 (Channel Clock Check A-D).

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)N2 CIFD
CIFA 01A-A4(A3)G2
CIFB 01A-B4(B3)D2
CIFC 01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

IML 91, 92, 93, 94, 95, or 96

Load Read Failure: Error codes result when an external register has either failed to load or cannot be read.

Card detecting the error:

NONE

FRU List

IML 91 DXA External Register Load/Read Failure

01A-B4(B3)J2
01A-B4(B3)P2

IML 92 DBO, DTG, or DTO Register Load/Read Failure

01A-B4(B3)X2 90%	01A-B4(B3)N2
01A-B4(B3)V2	01A-B4(B3)R2

IML 93 DCH, DCL, or MSC Register Load/Read Failure

01A-B4(B3)V2 90%	01A-B4(B3)K2
01A-B4(B3)J2	

IML 94 CBI, CCH, CCL, or CXC Register Load/Read Failure

01A-B4(B3)H2 90%
01A-B4(B3)G2

IML 95 CC1, CC2, or CC3 Register Load/Read Failure

CIFA 2X	01A-B4(B3)C2
CIFB 4X	01A-B4(B3)R2
01A-B4(B3)N2	01A-B4(B3)Q2
01A-B4(B3)F2	

IML 96 CR2, CR3, or CR6 Register Load/Read Failure

01A-B4(B3)C2 90%

Diagnostic Check

Bypass the error halt, select and load diagnostic routine 70, and loop function test 0F.

IML 97

CDX Card Check (TCA): Indicates that the SPC external registers on the channel data transfer (CDX) card caused a CDX card check after a load register operation.

Card detecting the error:

NONE

FRU List

01A-B4(B3)G2 90%
01A-B4(B3)H2

Diagnostic Check

Bypass the error halt, select and load diagnostic routine 70, and loop function test 0F.

IML C6

CSR Card Check, Buffer-to-CBI Miscompare (TCA): Is a failure to correctly transfer a byte of data from the automatic data transfer (ADT) buffer to the channel bus in (CBI) register using the ADT hardware.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)H2	01A-B4(B3)J2
01A-B4(B3)N2	01A-B4(B3)F2
01A-B4(B3)K2	01A-B4(B3)D2
01A-B4(B3)G2	

Diagnostic Check

Bypass the IML error halt. Select and load diagnostic 70 and loop function test '1B'.

IML C7

CSR Card Check 1 (TCA): Is generated whenever a CSR card check 1 is detected at the end of the buffer-to-CBI register test.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)H2 90%	01A-B4(B3)G2
01A-B4(B3)K2	

Diagnostic Check

Bypass the IML error halt (see the MD section in the MSM). Select and load diagnostic 70 and loop function test '1B'.

IML C9

Search Compare Failure (TCA): Occurs when the search compare hardware test fails to set and reset the compare successful latch (XES register, bit 5).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)H2 80%	01A-B4(B3)J2
01A-B4(B3)K2 10%	01A-B4(B3)V2
01A-B4(B3)G2	

Diagnostic Check

Bypass the IML error halt (see the MD section in the MSM). Select and load diagnostic 70 and loop test '1A'.

IML CA

CSC Card Check (TCA): Indicates that the hardcore tests are unable set on the channel check 1 bit (channel status register 2, bit 7) by forcing a CSC card check.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2	01A-B4(B3)R2
01A-B4(B3)G2	01A-B4(B3)D2
01A-B4(B3)H2	

Diagnostic Check

Select and load diagnostic 70 and select and load test '1C'.

IML CB

Interrupt Level 1 Not Set by Channel Check 1: Indicates that a channel check 1 has failed to set interrupt level 1 (interrupt level register, bit 1) during an IML operation.

Card detecting the error:

01A-xx(xx)xx

Diagnostic Check

Refer to Diagnostic Check 2 on page CHL-I 100.

IML CC

CDX Card Check (TCA): Occurs when CRO register, bit 2 (CDX card check) fails to set when CXC register bits 4 and 5 are set simultaneously or when a check reset fails to reset CRO register bit 2.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)G2	01A-B4(B3)R2
01A-B4(B3)F2	01A-B4(B3)H2

Diagnostic Check

Bypass the IML error halt (see the MD section in the MSM). Select and load diagnostic 70 and loop test '1D'.

IML D1

Active Bit On Channel Bus Out (TCA): Is generated when the contents of channel bus out contains one or more constantly active bits. The active bits are checked in two steps.

1. The contents of the channel bus out are gated into the channel bus out register and checked that bits 0 through 7 are active.
2. The parity bit is checked and if active, sets the channel search card check, which generates a D1 error.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)H2
01A-B4(B3)G2

Diagnostic Check

Reset the failing storage director and ensure that the -CSR Card Check 1 line 01A-B4(B3)H2 is inactive. Place the failing storage director in an IML loop. Scope all nets and check for incorrect levels or misshapen pulses.

SC 0F00

Sense byte 0, bits 0, 2, and 5 indicate a 3880 failure. If bit 0 (command reject) is on, see SC 0F00-0. If bit 2 (bus out parity check) is on see SC 0F00-2.

When any sense bit in sense bytes 0 through 6 is on, other than bit 0, 2, or 5 of sense byte 0, the failure is in the attached device. See the MSM SENSE section.

SC 0F00-0

Command Reject (TCA): Is set when:

- An invalid command is issued
- An invalid command sequence is detected
- A write command is issued with a file mask set
- A write command is issued with the Write Inhibit switch in the Read-Only position

The command reject error is indicated when sense byte 0, bit 0 equals 1.

Card detecting the error:

CIFx

FRU List

CIFx 70%	01A-B4(B3)K2
01A-B4(B3)H2	01A-B4(B3)X2
01A-B4(B3)J2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 0F00-2

Channel Bus Out Parity Check (TCA): When the hardware detects a parity error on the channel bus out lines, channel status 2 register, bit 5 is set. At command out time during a data transfer operation, the channel interface (CIF) card performs the parity check when the Chan Addr In line is active. The channel bus out parity check is indicated when sense byte 0, bit 2 equals 1.

The channel bus out parity check is caused by a failure in one of the following areas:

- Channel hardware
- Channel interface bus cables, terminators, or connectors
- Storage control cards or boards

Card detecting the error:

CIFx

FRU List

CIFx 70%	01A-B4(B3)F2
01A-B4(B3)D2	
01A-B4(B3)E2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 0F00-5

If sense byte 0, bit 5 (overrun) is on, see the ECD for either SC 2040 (channel overrun) or SC 2080 (data overrun).

Card detecting the error:

CIFx

FRU List

CSC Switches	01A-B4(B3)G2
CIFx 70%	01A-B4(B3)K2
01A-B4(B3)F2	01A-B4(B3)J2
01A-B4(B3)H2	

Address switches on the CSC card set incorrectly.

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100. When any sense bit in sense bytes 0 through 6 is on, other than bit 0, 2, or 5 of sense byte 0, the failure is in the attached device. See the MSM SENSE section.

SC 0F01

Command Reject (TCA): Occurs when the storage director receives an invalid command (that is, a read backward or similar command not contained in the service command set or a command pertaining to a feature that is not installed).

Card detecting the error:

CIFx

FRU List

System Software
Attached Devices
CIFx 50%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 0F02

Command Reject (TCA): Occurs when the storage director receives an incorrect sequence of commands (that is, a write command given without having previously specified the data block). For more information, see format 0, message 2 in the SENSE section of the MSM.

Card detecting the error:

CIFx

FRU List

System Software	01A-B4(B3)K2
Attached Device	01A-B4(B3)J2
CIFx 50%	01A-B4(B3)C2
01A-B4(B3)H2 10%	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 0F03

Command Reject (TCA): Occurs when the storage director receives a CCW count that is less than required. For more information, see format 0, message 3 in the SENSE section of the MSM.

SC 0F04

Command Reject (TCA): Occurs when the storage director detects a programming error in which invalid search argument are used. For more information, see format 0, message 4 in the SENSE section of the MSM.

SC 0F05

Command Reject (TCA): Occurs when the storage director receives a diagnostic command that violates bit 5 of the file mask. For more information, see format 0, message 5 in the SENSE section of the MSM.

SC 0F06

Command Reject (TCA): Occurs when the channel does not indicate command chaining when retry status is activated. For more information, see format 0, message 6 in the SENSE section of the MSM.

SC 0F07

Command Reject (TCA): Occurs when the storage director receives channel retry commands when retry status is activated. For more information, see format 0, message 7 in the SENSE section of the MSM.

Card detecting the error:

CIFx

FRU List 0F03-0F07

System Software
Attached Device
CIFx 50%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 2040

Channel Overrun (TCA): Is set when any of the following conditions occur:

- Out tag sequence check
- Data out or service out signal is not a minimum of 80 ns
- More out tag lines received than requested
- Out tag lines overlap more than 100 ns

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)G2 70%
01A-B4(B3)H2 10%
01A-B4(B3)K2
01A-B4(B3)N2
01A-B4(B3)J2
01A-B4(B3)F2
CIFx

Diagnostic Check

Refer to Diagnostic Check 3 on page CHL-I 100.

SC 2520

CSR CARD CHECK 2 (TCA): Indicates a hardware failure on the channel search (CSR) card. One of the following conditions causes the check to be set:

- Parity check in the channel count high or channel count low registers
- Circuit failure during a channel compare successful check

Channel Count High or Low Register Parity Check

The microcode loads the count high and count low registers with the number of bytes that are transferred to and from the channel.

During data transfer, the hardware decrements the count by one for each transfer. When the count equals zero and the channel has completed the control respond to the tag lines, CDX end of transfer (XCS register bit 4) is set.

Parity is checked for the initial byte count from the ALU bus and for each decrement under control of the +Check Byte Count Parity line.

Channel Compare Successful Check

The channel compare successful check is set when a compare is made of the duplicate compare hardware following the completion of an automatic search operation.

These two hardware comparators perform a byte-for-byte comparison of data in the channel bus out (CBO) and channel bus in (CBI) registers. At the completion of the search operation the output of both comparators are compared to ensure that they are equal.

The channel compare successful signal is sent to the automatic data transfer (ADT) cards, and to ensure the line is not open or shorted, the compare line is combined with two lines not associated with the CSR card.

From the three lines, a parity check bit is generated and checked by the ADT cards.

Card detecting the error:

01A-B4(B3)F2

01A-B4(B3)H2 80%
01A-B4(B3)G2 10%
01A-B4(B3)J2 10%
01A-B4(B3)V2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 270x, 2708, or 270B

Channel Data Check: Is active when a halt I/O check or a channel longitudinal redundancy check occurs. SC 2708 indicates a failure in channel A and 2709 indicates channel B.

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
2700	none
2708	A
2709	B
270A	C
270B	D
270C	E
270D	F
270E	G
270F	H

Card detecting the error:

01A-B4(B3)J2

FRU List SC 270x

01A-B4(B3)H2 60%
01A-B4(B3)G2 30%
01A-B4(B3)J2 10%
01A-B4(B3)F2

FRU List SC 2708-2709

01A-B4(B3)G2 30%
01A-B4(B3)H2 20%
CIFx 20%
01A-B4(B3)F2 10%
01A-B4(B3)J2
01A-A4(A3)P2
01A-A4(A3)G2
01A-B4(B3)D2
CIFz

FRU List SC 270B

01A-B4(B3)G2 30%
01A-B4(B3)H2 20%
CIFx 20%
01A-B4(B3)F2 10%
01A-B4(B3)J2
01A-A4(A3)G2
01A-A4(A3)P2
01A-B4(B3)D2
CIFz

Note: CIFz = The other half of a two channel pair. (A and B or C and D)

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 27Fx

Channel Bus Out Parity Check: When the hardware detects a parity error on the channel bus out lines, the channel status 2 register, bit 5 is set. At command out time during a data transfer operation, the channel interface (CIF) card performs the parity check when the +Chan Addr In (CSC) line is active. The channel bus out parity check is indicated when sense byte 0, bit 2 equals 1.

The channel bus out parity check is caused by a failure in one of the following areas:

- Channel hardware
- Channel interface bus cables, terminators, or connectors
- Storage control cards or boards

SC 27F0 indicates that neither CIF card is selected by the storage director at the time of the failure.

The least likely failing FRUs for SC 27F0 are the CIF cards and the cables between channels.

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
27F0	none
27F8	A
27F9	B
27FA	C
27FB	D
27FC	E
27FD	F
27FE	G
27FF	H

Card detecting the error:

01A-B4(B3)F2

FRU List SC 27Fx

CIFx 30%
01A-A4(A3)P2 20%
01A-B4(B3)D2 10%
01A-B4(B3)F2
01A-B4(B3)G2

FRU List SC 27F8-27F9

CIFx 60%
01A-A4(A3)P2 10%
01A-B4(B3)D2 10%
01A-B4(B3)F2
01A-B4(B3)G2
CIFz

FRU List SC 27FA-27FB

CIFx 60%
01A-A4(A3)G2 10%
01A-B4(B3)D2
01A-B4(B3)F2
01A-B4(B3)G2
CIFz

Note: CIFz = The other half of a two channel pair. (A and B or C and D)

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3B0x

Channel Bus In Parity Check: Occurs when the channel interface (CIF) card detects a parity error in the data sent from the storage director to the channel. Data is loaded into the channel bus in register of the selected CIF card, sent to the bus in deskew register, and gated to the channel.

The selected CIF card performs the parity check when the channel data transfer (CDX) card activates the +Set Bus In Deskew Reg (CDX) line. When the CIF card detects a parity error, it activates the -Chan Bus In Parity Check line. This in turn sets the channel bus in parity check, bit 0 in the channel interface check register.

SC 3B00 indicates that neither CIF card is selected by the storage director at the time of the failure.

The least likely failing FRUs for SC 3B00 are the CIF cards and the cables between channels.

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3B00	none
3B08	A
3B09	B
3B0A	C
3B0B	D
3B0C	E
3B0D	F
3B0E	G
3B0F	H

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3B0x

01A-B4(B3)H2 50%	01A-B4(B3)G2
CIFx 40%	01A-B4(B3)E2
01A-A4(A3)P2 10%	01A-A4(A3)G2
01A-B4(B3)F2	01A-B4(B3)D2

FRU List SC 3B0A-3B0B

01A-B4(B3)H2 50%	01A-B4(B3)G2
CIFx 40%	01A-B4(B3)E2
01A-A4(A3)G2	CIFz
01A-B4(B3)F2	01A-B4(B3)D2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3B1x

CIF Card Check (TCA): Occurs when channel bus register, bit 1 is set. This bit indicates to the channel sequence control (CSC) card that the channel interface (CIF) card has detected one of the following conditions:

- CIF clock check
- CIF propagate select out failure
- System reset failure
- Pending system reset failure
- Parity check of the channel bus-in lines (to drivers)
- Parity check of the channel bus-in lines from the channel data transfer (CDX) card
- Read or force switches (CSC) check condition active during data transfer

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3B10	none
3B18	A
3B19	B
3B1A	C
3B1B	D
3B1C	E
3B1D	F
3B1E	G
3B1F	H

Card detecting the error:

CIFx

FRU List SC 3B1x

CIFx 40%	01A-B4(B3)G2
01A-A4(A3)P2 30%	SBPx
01A-B4(B3)D2	01A-A4(A3)G2
01A-B4(B3)F2	01A-A4(A3)N2
	01A-B4(B3)E2

FRU List SC 3B18 - 3B19

CIFx 90%	01A-B4(B3)G2
01A-A4(A3)P2	SBPx
01A-B4(B3)D2	01A-A4(A3)G2
01A-B4(B3)F2	01A-A4(A3)N2
CIFz	01A-B4(B3)E2

FRU List SC 3B1A - 3B1B

CIFx 90%	01A-B4(B3)G2
01A-A4(A3)G2	SBPx
01A-B4(B3)D2	01A-A4(A3)P2
01A-B4(B3)F2	01A-A4(A3)N2
CIFz	01A-B4(B3)E2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

Note: CIFz = the other half of a two channel pair.

Symptom Codes

SC 3B2x

CDX Card Check: Occurs when the channel data transfer (CDX) card performs one of the following:

- Channel transfer control (CXC) register parity check
- Speed control timer and channel speed control (SPC) register parity check
- Pending counter parity check
- Load counter bus out (CBO) compare check
- CDX clock check

SC 3B20 indicates that neither CIF card is selected by the storage director at the time of the failure.

The least likely failing FRUs for SC 3B20 are the CIF cards and the cables between channels.

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3B20	none
3B28	A
3B29	B
3B2A	C
3B2B	D
3B2C	E
3B2D	F
3B2E	G
3B2F	H

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3B20

01A-B4(B3)G2 90%	01A-A4(A3)P2
01A-B4(B3)H2	01A-B4(B3)F2
01A-B4(B3)J2	01A-B4(B3)X2
	01A-B4(B3)R2

FRU List SC 3B28 - 3B2F

01A-B4(B3)G2 90%	01A-B4(B3)F2
01A-B4(B3)H2	01A-B4(B3)K2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3B3x

CSR Card Check 1: Occurs when the channel search (CSR) card detects a failure and activates the -CSR Card Check 1 line to the automatic data transfer card. This line is activated when the CSR card performs one of the following three parity checks.

- Channel bus in (CBI) register parity check
- Channel bus out (CBO) register parity check
- Channel transfer control (CXC) register parity check

CSR card check 1 also sets the channel check 1 latch on the channel sequence control (CSC) card. Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3B30	none
3B38	A
3B39	B
3B3A	C
3B3B	D
3B3C	E
3B3D	F
3B3E	G
3B3F	H

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3B3x

01A-B4(B3)H2 90%	01A-B4(B3)R2
01A-B4(B3)F2	01A-B4(B3)K2
01A-B4(B3)P2	

FRU List SC 3B38-3B39

ADDRSW	01A-B4(B3)E2
01A-B4(B3)H2 50%	01A-B4(B3)K2
CIFx 20%	01A-A4(A3)P2
01A-B4(B3)D2	CIFz
01A-B4(B3)G2	01A-B4(B3)C2
01A-B4(B3)F2	01A-B4(B3)P2

FRU List SC 3B3A-3B3B

ADDRSW	01A-B4(B3)F2
01A-B4(B3)H2 50%	01A-B4(B3)E2
CIFx 20%	01A-B4(B3)K2
01A-A4(A3)G2	01A-A4(A3)P2
01A-B4(B3)G2	CIFz
01A-B4(B3)D2	

Note: CIFz = the other half of a two channel pair.

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3C3x

FACR/TACR Card Check: Occurs when the hardware sets channel status 2 register, bit 3. The two/four channel additional condition register on the FACR/TACR card activates the FACR/TACR card check line to the channel sequence control card when a failure is detected in one of the following areas:

- Request-in logic
- Suppress-out logic
- Register 17 logic bit

The FACR/TACR card check is divided into nine symptom codes.

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3B30	none
3B38	A
3B39	B
3B3A	C
3B3B	D
3B3C	E
3B3D	F
3B3E	G
3B3F	H

Card detecting the error:

01A-B4(B3)E2

FRU List

01A-B4(B3)E2 90%	01A-B4(B3)P2
01A-B4(B3)F2	01A-B4(B3)Q2
CIFx	01A-B4(B3)R2

Note: CIFz = the other half of a two channel pair.

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3C4x

CSC Card Check: Occurs when the channel sequence (CCR) card detects one of the following:

- Channel selection check
- Register 16 check
- Channel control 1 register check
- CSC clock check
- CSC in tag check

Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3C40	none
3C48	A
3C49	B
3C4A	C
3C4B	D
3C4C	E
3C4D	F
3C4E	G
3C4F	H

Card detecting the error:

None

FRU List SC 3C4x

01A-B4(B3)F2 70%
01A-B4(B3)G2 30%
01A-B4(B3)E2
01A-B4(B3)P2

FRU List SC 3C48-3C4B

01A-B4(B3)F2 90%
CIFx
01A-A4(A3)P2 A/B
01A-A4(A3)G2 C/D
01A-B4(B3)D2
01A-B4(B3)E2
01A-A4(A3)P2 C/D
01A-A4(A3)G2 A/B
01A-B4(B3)G2
01A-B4(B3)P2
01A-B4(B3)Q2
CIFz

Note: CIFz = the other half of a two channel pair.

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3C6x

TCR Card Check: Occurs when the hardware sets channel status 2 register, bit 6.

The two-channel condition register (TCR) card activates the -TCR Card Check line to the channel sequence control card when a failure is detected in one of the following areas:

- Request in logic
- Request out logic
- Register 17 logic bit

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3C60

01A-B4(B3)C2 90%
01A-B4(B3)F2
01A-B4(B3)P2
01A-B4(B3)Q2
01A-B4(B3)R2

FRU List SC 3C68-3C6B

01A-B4(B3)C2 90%
01A-B4(B3)F2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3D10

CDX Clock Check: Indicates that one of the four clock lines (T0, T2, T4, T6) received by the CDX card from the clock card is out of sequence. The check detects missing or extra clock pulses.

This condition is a group of toggle latches that are set or reset by the four clock lines. When one or more of the clocks is out of sequence, the latches are not set or reset. This condition activates the -CDX Clock Check line to the automatic data transfer card.

The CDX clock check is degated by either of the following conditions:

- An inactive +CXC Reg (CSR) Bit 5 line from the channel search (CSR) card
- An active +Disable Run Chan line from the channel sequence control (CSC) card

The -CDX Clock Check line is dot ORed on the board with all other storage director clock checks. The check condition is reset by the +Reset line from the maintenance card.

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)G2 60%
01A-B4(B3)P2 40%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3D20

CSC Clock Check: Occurs if the -Clock Check Two line is active when a clock signal is determined to be missing or out of sequence. When the channel sequence control (CSC) card detects the clock check, it sets the CSC card check bit, channel status 2 (CS2) register, bit 4. This in turn sets transfer error status register, bit 3 (clock check 2) and CS2 register, bit 7 (channel check 1).

Card detecting the error:

01A-B4(B3)F2

FRU List

01A-B4(B3)F2 50%
01A-B4(B3)P2 30%
01A-B4(B3)Q2 10%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3D3x

CIF Clock Check: When the channel interface (CIF) card detects a clock failure, it activates the -CIF Clock Check line to the automatic data transfer card. This hardware detected clock failure sets channel interface check register, bit 1 (CIF clock check) and channel status 2 register, bit 1 (channel check 2). Use the Symptom Code Chart to find which CIF card was selected by the storage director at the time of the failure.

SYMPTOM CODE	CIF CARD
3D3x	none
3D38	A
3D39	B

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3D3x

CIFA 40% 01A-B4(B3)P2 10%
CIFB 40% 01A-A4(A3)N2 10%

FRU List SC 3D38-3D39

CIFx 80%
01A-B4(B3)P2 10%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3D4x

CIF Clock Check: When the four-channel additional sequence control (FASC) card detects a CIF card clock failure for channels A, B, C, D. The failing CIF or clock card activates the -Clock Check Latched line which sets CRO register bit 4 (channel clock check). The selected CIF card also activates the -CIF Card Check line which sets CRO register bit 1 (CIF card check).

Note: If channels E, F, G, or H are selected at the time of the failure, the symptom code is 3D40.

SYMPTOM CODE	CIF CARD
3D40	none
3D48	A
3D49	B
3D4A	C
3D4B	D

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3D4x

CIFx 50% 01A-B4(B3)D2
01A-A4(A3)N2 40% 01A-B4(B3)F2
01A-A4(A3)G2

FRU List SC 3D48-3D4B

01A-A4(A3)N2 60% 01A-B4(B3)D2
CIFx 30% 01A-B4(B3)F2
01A-A4(A3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3D5x

CIF Clock Check: When the four-channel additional sequence control (FASC) card detects a CIF card clock failure for channels E, F, G, H. The failing CIF or clock card activates the -Clock Check Latched line which sets CRO register bit 5 (channel clock check E-H). The selected CIF card also activates the -CIF Card Check line which sets CRO register bit 1 (CIF card check).

Note: If channels A, B, C, or D are selected at the time of the failure, the symptom code is 3D50.

SYMPTOM CODE	CIF CARD
3D50	none
3D5C	E
3D5D	F
3D5E	G
3D5F	H

Card detecting the error:

01A-B4(B3)F2

FRU List SC 3D5x

CIFx 50% 01A-B4(B3)D2
01A-A4(A3)N2 40% 01A-B4(B3)F2
01A-A4(A3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3Exy

Channel Multiple Failure (TCA): Indicates that a channel check 1 error has occurred and the symptom code generator has detected an SC 3Eyy in the channel status 2 registers. To get a 3Eyy symptom code, more than one on the following checks must be on:

- Channel sequence control (CSC) card check
- Channel bus out parity check (CIF)
- Two-channel condition register (TCR) card check
- Channel bus in parity check (CIF)
- Channel data transfer (CDX) card check
- Channel search (CSR) card check
- Channel clock check

yy BIT	CHANNEL CHECK	SYMPTOM CODE (See Note)
0	Chan bus in prty chk	3B0x
1	CIF card check	3B1x
2	CDX card check	3B2x
3	CSR card check	3B3x
4	Not used	–
5	CSC card check	3C4x
6	Not used	–
7	TCR card check	3C6x

Note: The x in the symptom code column indicates the channel selected at the time the error occurred. Replace the x with bits 4 through 7 of sense byte 14. If sense bytes are not available, use x=0.

Card detecting the error:

CIFx

FRU List SC 3E00

01A-B4(B3)F2 90% 01A-B4(B3)D2
01A-A4(A3)N2 01A-B4(B3)C2
CIFx

FRU List SC 3Exy

01A-B4(B3)G2 50% 01A-A4(A3)N2
01A-B4(B3)H2 40% 01A-B4(B3)P2
01A-B4(B3)F2 01A-B4(B3)E2
CIFx 01A-B4(B3)D2
01A-B4(B3)C2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3F00 Through SC 3F1x

Channel Time-Out failure (TCA): Occurs when the storage director takes more than 650 milliseconds to execute a channel operation. The time-out failure turns off maintenance control sense register bit 0 (enable timer) that resets the timer and turns off interrupt level register bits 1 and 6. The storage director continues to another interrupt level.

The channel time-out failure can cause symptom codes from 2F00 through 3F1F. The generated symptom code indicates approximately which portion of the operating system failed. (See the system documentation.)

If the failing storage director is attached to a 4341 system, 3880 time-out errors may occur when the operator initiates a system IML or reset.

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)F2 40% 01A-B4(B3)K2
CIFx 30% 01B-B4(A3)P2
01A-B4(B3)G2 10% 01A-B4(B3)U2
01A-A4(A3)P2 10% 01A-B4(B3)C2
01A-B4(B3)H2 SBPx
01A-B4(B3)V2
01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC 3F2x

Channel Time-Out Failure: The 3880 has timed out after 650 milliseconds while connected to the host channel. To determine the cause of the time-out, see the sense information for the failing storage director.

The low-order character in the symptom code defines the selected channel when the time-out occurred.

The channel time-out failure is divided into three symptom codes. These codes indicate the channel connected at the time of the failure.

SC 3F20

Indicates that neither channel is connected at the time of the failure.

SC 3F28

Indicates that channel A is connected at the time of the failure.

SC 3F29

Indicates that channel B is connected at the time of the failure.

(TCA)

SYMPTOM CODE	CIF CARD
3F20	none
3F28	A
3F29	B
3F2A	C
3F2B	D
3F2C	E
3F2D	F
3F2E	G
3F2F	H

To detect the failure, it may be necessary to disable the interval timer, which places the storage director in a hang condition.

Place the MD in support made and select option 0.

The hex information presented in sense byte 20 is the channel time-out message number corresponding to one of the following messages:

Message 01

The storage director has activated CU busy (status in and timed out) waiting for select out to deactivate. CU busy is active for one of the following reasons:

- With device status stacked in the storage director, a Start I/O was initiated to a different device
- With a contingent connection present in the storage director, a Start I/O was initiated to the wrong device
- While Command Retry was in progress, a Start I/O was initiated

Message 02

During a selection sequence (either control unit or channel initiated), the control unit has activated the OP In and Address In lines, and timed out waiting for the Command Out line to become active. The channel can also activate Halt I/O to stop the selection sequence and exit from this loop.

Message 03

The control unit is trying to present initial status, and timed out waiting for the channel to activate the Service Out line (status accepted). The channel can also activate the Command Out line (status stacked) or Halt I/O (abort) line to exit from this loop. Sense byte 19 contains the actual status presented to the channel.

Message 04

The control unit timed out, while waiting for the channel to deactivate the Command Out and/or Service Out lines before presenting status, or before or during manual data transfer (see note).

Message 05

The control unit microcode activates the Status In line to present status, and times out waiting for the channel to respond with the Service Out line (status accepted). The channel can activate the Command Out line (status stacked), or Halt I/O (abort) line to exit from this loop.

Message 06

The control unit microcode initiated a hardware sequence to present status to the channel by activating Hardware Ending Status Sequence (CS3 register, bit 3). The control unit timed out waiting for one of the following bits to be set.

1. Sequence Complete. This is set when a chain reselection is completed to the point where a new channel command word (CCW) is received on the Bus Out lines.
2. Sequence Terminated. This is set by one of the following:
   - Command Out (status stacked) in response to the Status In line.
   - Service Out with no Suppress Out line (status accepted, but no command chaining).
   - Halt I/O (interface disconnect, or abort)

Message 07

At the end of a (CCW) chain, the control unit microcode timed out waiting for the Service Out line to deactivate before deactivating the Op In line.

Message 08

During manual data transfer (see note), the control unit microcode activates the Service In line and timed out waiting for the Service Out line (data sent/received) to become active. The channel can activate Halt I/O (abort) or the Command Out lines to stop the data transfer sequence and exit from this loop.

Message 09

During manual data transfer (see note), while reading data to the channel, the control unit microcode timed out waiting for the Suppress Out line to deactivate. The channel may suppress data transfer temporarily by activating the Suppress Out line. A time out occurs if the Suppress Out line is active for more than 650 milliseconds.

Message FF

This entry is an undefined combination of sense bits. Ensure that all recommended FRUs are replaced, then call for diagnostic assistance.

Note: Manual data transfer is a method used to transfer data to or from the channel when the transfer is not time-dependent. (For example, during the transfer of a seek address, a file mask, or sense information).

Card detecting the error:

01A-B4(B3)J2

FRU List

01A-B4(B3)F2 40%
CIFx 30%
01A-B4(B3)G2 10%
01A-A4(A3)P2 10%
01A-B4(B3)H2
01A-B4(B3)V2
01A-B4(B3)X2
01A-B4(B3)K2
01B-B4(A3)P2
01A-B4(B3)U2
01A-B4(B3)C2
SBPx

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

Note: Time-outs on a 4341 system If the failing storage director is attached to a 4341 system, 3880 time-out errors may occur when the operator initiates a system IPL or reset.

ICs 78xx

Channel Failure (TCA): Codes are channel wrap isolation codes developed by the MD while running the channel wrap diagnostics. The 78xx codes are for machines with internal electronic wrap.

IC 7844

Indicates that only channel B failed during the channel wrap diagnostic.

IC 7848

Indicates that only channel A failed during the channel wrap diagnostic.

IC 784C

Indicates channel A and B are failing at least one of the channel wrap diagnostic routine 78 tests.

ISOLATION CODE	CHANNEL ERROR
7841	Channel D
7842	Channel C
7843	Channel C and D
7844	Channel B
7848	Channel A
784C	Channel A and B
7881	Channel H
7882	Channel G
7883	Channel G and H
7884	Channel F
7888	Channel E
788C	Channel E and F

FRU List IC 7841-7842

CIFx
SBPx
01A-A4(A3)G2
OP PNL SW
01A-B4(B3)F2

FRU List IC 7843

CIFx
CIFy
01A-A4(A3)G2
01A-B4(B3)F2
01A-B4(B3)P2
01A-A4(A3)N2
01A-B4(B3)E2

FRU List IC 7844-7848

CIFx
SBPx
01A-A4(A3)P2
01A-A4(A3)N2
OP PNL SW
01A-B4(B3)E2

FRU List IC 784C

01A-A4(A3)P2
CIFx
CIFy
01A-B4(B3)F2
01A-A4(A3)N2
01A-B4(B3)C2

FRU List IC 7881-7882

CIFx
SBPx
01A-A2(A1)G2
OP PNL SW
01A-B4(B3)F2
01A-B4(B3)E2

FRU List IC 7883

01A-A2(A1)G2
CIFx
CIFy
01A-B4(B3)F2
01A-A4(A3)N2

FRU List IC 7884,7888

CIFx
SBPx
01A-A4(A3)P2
OP PNL SW
01A-B4(B3)F2
01A-B4(B3)E2

FRU List IC 788C

01A-A4(A3)P2
CIFx
CIFy
01A-B4(B3)F2
01A-A4(A3)N2

Diagnostic Check

To find the cause of the 78xx error codes, the actual diagnostic error stop must be determined. Perform the following:

1. Place the MD in support mode.
2. Select the failing storage director.
3. Set the channel Enable/Disable switch to the enable position,and execute routine 78.
4. Perform an IML operation as directed by the MD.
5. Run all the tests within routine 78.
6. Select diagnostic run option B.

   The MD displays the routine, test, and error stop for the actual failure in the channel wrap diagnostic that produced the error codes.
7. Use the DC section of this manual as a reference to understand the exact failure. You may choose to re-enter support option B and to select routine 78 with parameters. To run the test that failed, specify sub-option 3, which is loop continue on error

SC FF01

Condition Code 3 (TCA): For the description of condition code 3 errors, see *IBM System/370 Principals of Operation,* GA22-7000, or *IBM 4300 Processor Principles of Operation,* GA22-7070.

Condition code 3 (select in received for initial selection) is caused when either the 3880 or the device is not operational. If the 3880 is suspected, ensure that the:

- Storage director is powered on
- Enable/Disable is in the Enable position
- Enable/Disable indicator is off

If the Enable/Disable indicator is on in response to a Start I/O command to the failing storage director, a permanent error occurred.

Card detecting the error:

NONE

FRU List

EN/DS SW.	01A-B4(B3)D2
ADDRESS SW	01A-B4(B3)E2
CIFx 40%	01A-A4(A3)P2
SBPx 10%	01A-A4(A3)G2
01A-B4(B3)F2	01A-B1E2
	01A-B4(B3)X2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF02

Channel Time-Out Failure (TCA): Occurs when the storage director takes more than 30.5 milliseconds to execute a channel operation. The time-out failure turns off maintenance control sense register, bit 0 (enable timer) that resets the timer and turns off interrupt level register, bits 1 and 6. The storage director continues to another interrupt level.

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-B4(B3)G2
01A-B4(B3)F2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF03

Control Unit Busy Mode (TCA): Indicates to the processing unit that channel control 1 register, bit 4 is active, causing the hardware in the channel interface logic to generate control unit busy.

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-A4(A3)P2
01A-B4(B3)F2 20%	01A-A4(A3)G2
01A-B4(B3)D2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF04

Interface Control Check (TCA): Occurs when a processing unit detects a failure. See the system documentation for failure descriptions.

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-A4(A3)N2
01A-B4(B3)F2	SBPx
01A-A4(A3)P2	01A-B4(B3)D2
01A-B4(B3)G2	01A-B4(B3)E2
01A-B4(B3)H2	01A-B4(B3)C2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF05

Bus In Parity Check (TCA): Is a processing unit detected parity error on the channel bus in lines.

Card detecting the error:

01A-B4(B3)F2

FRU List

CIFx 90%

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF06

Processor Detected Channel Control Check: Is developed by the MD to indicate to the 3880 that a machine malfunction is affecting the channel interface controls.

Error conditions that result from channel control checks can invalidate the channel command word (CCW). These conditions include:

- Invalid checking block code on a CCW
- Channel detected errors associated with data transfer that are not indicated as a channel data check (SC FF08)
- I/O interface errors detected by the channel that are not indicated as a interface control check (SC FF04)

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-A4(A3)P2
SBPx	
01A-B4(B3)F2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF07

System Check or Hang: Is developed by the MD to indicate a machine malfunction that causes either a system check or a hang condition when no check indication is available. When a machine malfunction is detected, the action taken depends upon the situation in which it occurs. A damage condition exists when the automatic hardware recovery mechanism is not successful or the recovery mechanism does not exist. System checks are reported as machine checks and cause the CPU to enter a check stop.

Card detecting the error:

NONE

FRU List

CIFx 70%	SBPx
01A-B4(B3)D2	01A-B4(B3)V2
01A-A4(A3)G2	01A-B4(B3)J2
01A-B4(B3)F2	01A-B4(B3)K2
01A-B4(B3)G2	01A-B4(B3)X2
01A-B4(B3)C2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF08

Channel Data Check (TCA): Is an error detected in the processor. This check indicates that an error was detected in the data transferred to or from main storage during an I/O operation, or that a parity error occurred on the bus in lines during an input operation.

The channel data check is caused by a failure in one of the following areas:

- The Channel
- Main Storage
- The path between main storage and the channel interface

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-B4(B3)F2
01A-B4(B3)H2	

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF09

SC FF09 is a processor detected error condition that indicates to the channel that the path to the addressed device is busy.

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-B4(B3)D2
SBPx	01A-A4(A3)P2
01A-B4(B3)F2	01A-A4(A3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

SC FF0A

Undefined Channel Error (TCA): Is an undefined CPU detected channel error reported by the 3880.

Card detecting the error:

NONE

FRU List

CIFx 70%	01A-B4(B3)D2
SBPx 10%	01A-A4(A3)P2
01A-B4(B3)F2 10%	01A-A4(A3)G2

Diagnostic Check

Refer to Diagnostic Check 1 on page CHL-I 100.

Diagnostic Check 1

Note: Install the select-out bypass jumpers/card before disturbing channel cables or any cards. (See the CARR section in the MIM).

The order in which the following checks are listed is chosen so the first one has the highest probability of resulting in the repair of the machine. Perform each step if it has not already been done.

After performing each step, determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, go to the next check.

1. Run the control interface (CTL-I) wrap diagnostics. Then run the channel interface (CHL-I) wrap diagnostics. If any cards, crossovers, or cables are listed by the MD, replace or swap them until the cause of the failure is isolated. If a failure other than this symptom code is detected, use the symptom analysis option (option 4) for a description and list of the field replaceable units (FRUs).

2. Power off the failing storage director and reseat all cables (including power cables) that attach to the board. Check all crossovers carefully on the failing storage director for bent or missing pins on the crossover connectors and the bottom and top card connectors.

3. Power off the failing storage director and check the cable paddle cards that plug into the rear of the channel serpent connector blocks to ensure that they are correctly seated. Do not unplug any paddles if the system is operational; simply push each one firmly into its socket.

4. Request an environmental recording, editing, and printing (EREP) printout for all processors attached to the non-failing storage director and examine all recent symptom codes that pertain to the failing storage director. If any format 3 symptom codes appear (sense byte 7 equals 3x) other than this symptom code, select the MD symptom analysis option (option 4) and enter them. Replace or swap any FRUs listed that have not previously been replaced or swapped.

5. Run the CHL-I wrap diagnostics again if an error was detected the first time they were run but the trouble has not yet been found. Loop the routine for the failing test and scope all nets associated with the FRU list, using the LRM, for incorrect levels or misshapen pulses.

6. Loop the complete CHL-I wrap diagnostic and scope all nets, using the LRM for incorrect levels or misshapen pulses.

7. Replace or swap any FRUs on the FRU list that have not already been replaced or swapped.

8. Power off the failing storage director and remove all cards shown on the FRU list. Using the LRM check all nets with a CE meter for an open, a short between nets, or a short between a net pin and ground, or a voltage. See the MDM for the voltage pin list.

Diagnostic Check 2

Reset the failing storage director and ensure that the +Channel Data Check line 01A-B4(B3)H2 is inactive.

Bypass the IML error halt (see the MD section in the MSM) and loop routine 70. While looping the IML failure, check all the nets associated with the FRU list for incorrect levels or misshapen pulses.

Note: Bypassing the IML error halt may cause a check 1 error when routine 70 is invoked. The check 1 bypass option can be used.

Remove all cards on the FRU list and using the LRM check all nets with a CE meter.

Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, call for assistance.

Diagnostic Check 3

Power off the failing storage director. Remove all of the cards shown on the FRU list. Use the LRM (Logic Reference Manual) and the MDM and check all of the nets used with a CE meter. Check for an open or short circuit between nets, grounds, or voltage pins. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise, call for assistance.

Control Interface

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89-2	20	3	A13
8C-1	20	3	A13
8C-2	20	3	A13
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3018	10	3	A09
3019	20	3	A13
301B	20	3	A13
301C	20	3	A13
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FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

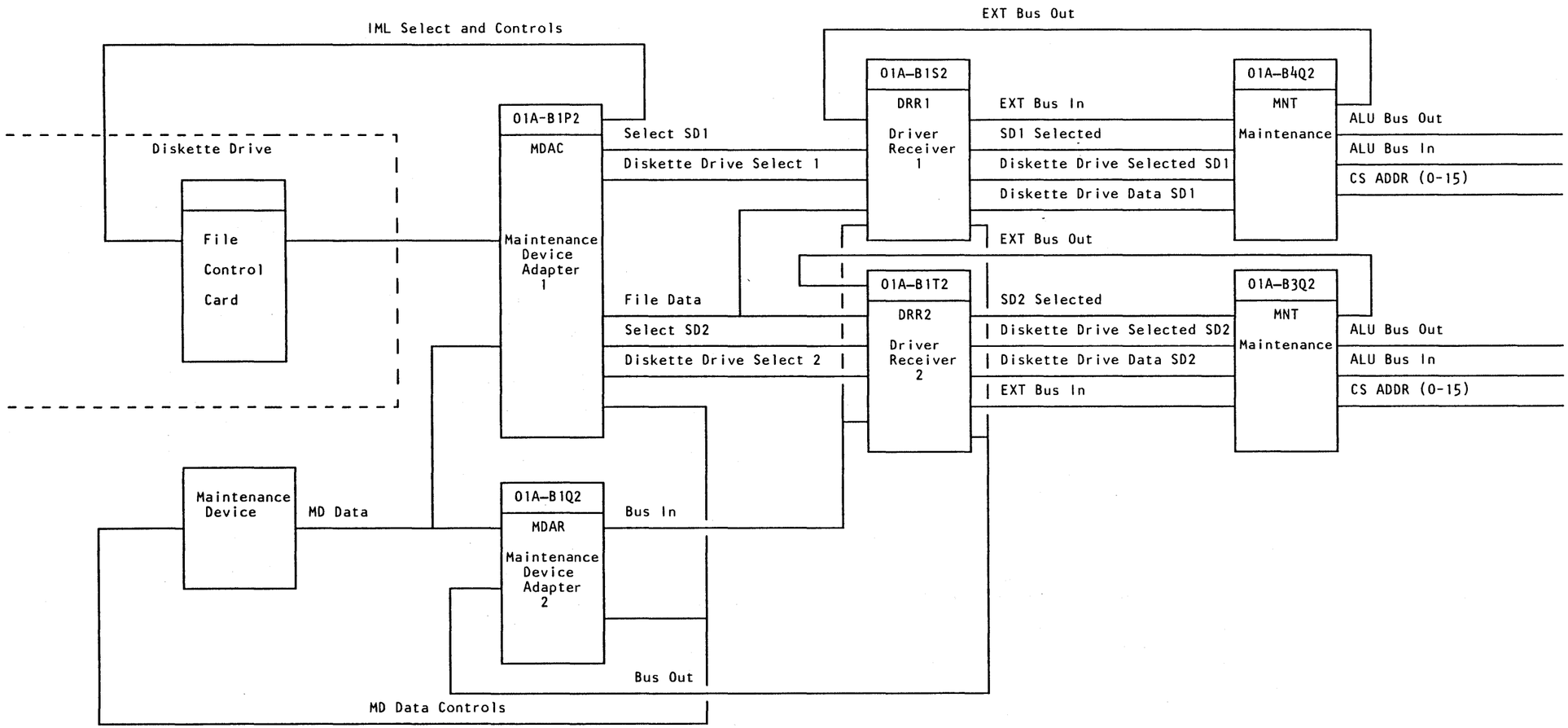
See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Error Code Diagram

IML data from the diskette flows through the maintenance board to the storage directors. The diagram on this page shows the cards involved in the data flow.

For information on the diskette drive see the OPER section in the MSM.



IML 02-2, 12-2, 42-2

Waiting For Index: Indicates that the +Diskette File line is continuously active.

Card detecting the error:

01A-B1P2

FRU List

File Control Card 70%
01A-B1P2 30%
Diskette Drive
01A-B1S2
01A-B1T2

Diagnostic Check

Refer to Diagnostic Check 1 on page DD 30.

IML 03-2, 13-2, 43-2

Waiting For Index: Indicates that the +Diskette File line is continuously inactive.

Card detecting the error:

01A-B1P2

FRU List

File Control Card 70%
01A-B1P2 30%
01A-B1Q2
01A-B1S2
01A-B1T2
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 2 on page DD 30.

IML 04-2, 05-2, 14-2, 15-2, 44-2, 45-2

No Sync or Clock Pulse: Codes are caused by one of the following problems:

- Diskette drive index pulse is present and the clock pulses are missing
- Diskette drive clock pulses are present and the sync pulse is missing

Diskette drive clock pulses occur every 4 microseconds and define the period that sync or data pulses can be present. When the storage director microprocessor card receives the index and clock pulses, it waits for the sync pulse. (The sync pulse is the first data pulse after the index pulse and identifies the start of a record.)

Card detecting the error:

01A-B1P2

FRU List

File Control Card 80%
01A-B1S2
Diskette Drive
01A-B1P2
01A-B1T2

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 07-1, 17-1, 47-1, SC 3017, F017

Wrong Track ID Read From Diskette: Codes are caused by the diskette drive reading the wrong track identification byte.

The read-only storage (ROS) IML selection code reads a diskette track ID into control storage. The byte from the diskette track does not match the ID byte in ROS even after the track ID is re-read 10 times.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 40%
01A-B4(B3)P2 30%
01A-B1S2
01A-B1T2
01A-B1P2
01A-B1Q2
01A-B4(B3)Q2
File Control card
Diskette

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 07-2, 17-2, 47-2

Wrong Track ID Read From Diskette: Codes occur when the diskette drive reads the wrong track identification byte.

Card detecting the error:

NONE

FRU List

File Control Card 50%
01A-B1P2 50%
01A-B1S2
01A-B1T2
01A-B1Q2
Diskette Drive
Diskette

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 08-1, 18-1, 48-1, SC 3018, F018

Diskette Drive Data Check: Codes are caused by extra or missing bits in an IML record.

Card detecting the error:

NONE

FRU List

Diskette
01A-B4(B3)R2 40%
01A-B4(B3)P2 30%
01A-B1S2 0%
01A-B1T2
01A-B1P2
File Control Card

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 09-1

Diskette Drive Access Error: Occurs when accessing to track zero, the diskette drive read head is moved eight tracks before a track ID byte is read. If the track read is track zero, the access operation is complete. If not, the access operation is repeated a maximum of 10 times. If track zero is not found, IML 09-1 is generated.

Card detecting the error:

NONE

FRU List

Diskette
01A-B4(B3)R2 50%
01A-B4(B3)P2
01A-B1S2
01A-B1T2
01A-B1P2
01A-B1Q2
File Control Card

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 19-1, 49-1

Diskette Drive Access Error: Codes occur when accessing tracks other than zero the microprocessor determines the direction and number of tracks the head must move. If the track is not found in 11 attempts:

- IML 19-1 is generated if the access operation was started from the overlay loader
- IML 49-1 is generated if the access operation was started from the common loader

Card detecting the error:

NONE

FRU List

Diskette	01A-B1T2
01A-B4(B3)R2 50%	01A-B1P2
01A-B4(B3)P2	01A-B1Q2
01A-B1S2	File Control Card

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 09-2, 19-2, 49-2, SC 3081, F081

IML Access Error: Codes are caused by a failure of the diskette drive access operation in an area that affects both storage directors.

Card detecting the error:

NONE

FRU List

01A-B1P2 50%	01A-B1S2
File Control Card 30%	01A-B1T2
01A-B1Q2 20%	Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

IML 1B

Diskette Record Not Found: Is caused by a request for a diskette track that is not in the track set for the 3880 configuration.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 1C

Diskette Record Not Found: Is caused by a double record on the last track of the diskette.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 1D

Diskette Record Not Found: Is caused by one of the following:

- Overlay mismatch
- Double record
- Incorrect first ID

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 1E, 1F, SC 301F, F01F

Diskette Record Not Found: Codes are caused by one of the following:

- Overlay mismatch
- Overlay not found
- Double record
- Mismatch between the first and second ID

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 4B

IML 4B is the result of an incorrect compacted start address error.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 4D

IML 4D is the result of a compacted track word count of 2462.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 4E

IML 4E is the result of decompaction error on the diskette.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

IML 80-1, 81-1, 84-1

Diskette Turns Too Slowly: Codes are caused by the diskette turning too slowly.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 50%	01A-B1P2
01A-B1S2	01A-B1Q2
01A-B1T2	File Control Card

Diagnostic Check

Refer to Diagnostic Check 5 on page DD 30.

IML 80-2, 81-2, 84-2

Diskette Turns Too Slowly: Codes are caused by the diskette turning too slowly.

Card detecting the error:

NONE

FRU List

Diskette Drive	01A-B1T2
	01A-B1P2
01A-B1S2	File Control Card

Diagnostic Check

Refer to Diagnostic Check 5 on page DD 30.

IML 88-1, 89-1, 8C-1

Diskette Turns Too Fast: Codes are caused by the diskette turning too fast.

Card detecting the error:

NONE

FRU List

Diskette	01A-B4(B3)R2
File Control Card 60%	01A-B1S2
01A-B1P2 30%	01A-B1T2

Diagnostic Check

Refer to Diagnostic Check 5 on page DD 30.

IML 88-2, 89-2, 8C-2

Diskette Turns Too Fast: Codes are caused by the diskette turning too fast.

Card detecting the error:

NONE

FRU List

Diskette Drive	01A-B1T2
	01A-B1P2
01A-B1S2	File Control Card

Diagnostic Check

Refer to Diagnostic Check 5 on page DD 30.

SC 3019, F019

Diskette Seek Error: Codes occur when a permanent seek error is detected during an IML operation.

Card detecting the error:

NONE

FRU List

01A-B4(B3)R2 50%	01A-B1P2
01A-B4(B3)P2	01A-B1Q2
01A-B1S2	File Control Card
01A-B1T2	
Diskette	

Diagnostic Check

Refer to Diagnostic Check 3 on page DD 30.

SC 301B, F01B

Track Request Out of Band: Codes are generated after an inline program is loaded and the track request is found to be higher than the track pointer limits of the band.

These codes can occur if the microcode has been patched, but the LRC has not been updated it include the patch.

Card detecting the error:

NONE

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

SC 301C, F01C

Double Overlay Crosses Track Boundary: Codes occur when an incorrect table of beginning overlay numbers is detected.

These codes can occur if the code has been patched, but the LRC has not been updated it include the patch.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

SC 301D, F01D

Overlay ID Mismatch: Codes are generated when an overlay ID does not match the ID specified by the routine locator.

When loading an inline program, the routine locator specifies the overlay ID, the track, and the record. When the ID is read after loading, the ID is not the same as the ID specified by the routine locator.

These codes can occur if the code has been patched, but the LRC has not been updated it include the patch.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

SC 301E, F01E

Double Load Verification: Codes occur when an error is detected during decompaction of the diskette data.

These codes can occur if the code has been patched, but the LRC has not been updated it include the patch.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

SC 3089, F089

Diskette Turns Too Fast: Codes occur when the diskette drive turns too fast during an IML operation.

Card detecting the error:

NONE

FRU List

Diskette Drive	01A-B1T2
	01A-B1P2
01A-B1S2	File Control Card

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

SC 3F70, FF70

Error in Functional Code Swap: Codes are generated when an error is found in the functional microcode.

If an inline program is going to be moved from Dynamic Control Storage (DCS) to Static Control Storage (SC) for high speed running, the microcode in the area of SC that is to be used, must be temporarily moved to DCS.

When this code is moved to DCS, the stored longitudinal redundancy check (LRC) is checked. If it does not compare, an error code is presented.

These codes can occur if the code has been patched, but the LRC has not been updated it include the patch.

Card detecting the error:

NONE

FRU List

Diskette 90%
Diskette Drive

Diagnostic Check

Refer to Diagnostic Check 4 on page DD 30.

Diagnostic Check 1

Note: Replace the diskette with a known good one before performing the diagnostic checks.

Prepare a scope loop as follows:

1. Prepare the MD for manual control operation as shown in the MD section of the MSM.
2. Select the failing storage director.
3. Execute the LOOP option.

See MD section for an explanation of the scope loop preparation.

Check the cable between B1V2 and the file control card. Check pin B13 (+Index Diskette) for a short to ground or to a minus-level signal line.

See the CARR section in the Maintenance Information Manual for diskette drive voltage checks.

Diagnostic Check 2

Note: Replace the diskette with a known good one before performing the diagnostic checks.

Prepare a scope loop as follows:

1. Prepare the MD for manual control operation as shown in the MD section of the MSM.
2. Select the failing storage director.
3. Execute the LOOP option.

See MD section for an explanation of the scope loop preparation.

Check the following:

- 01A-B1V2B13 for an open or a short to a plus-level signal line
- The line between 01A-B1P2P04 and 01A-B1V2B13 for an open or a short to a plus-level signal line

See the CARR section in the Maintenance Information Manual for diskette drive voltage checks.

If the problem persists, replace the maintenance board or the diskette drive.

Diagnostic Check 3

Note: Replace the diskette with a known good one before performing the diagnostic checks.

Prepare a scope loop as follows:

1. Prepare the MD for manual control operation as shown in the MD section of the MSM.
2. Select the failing storage director.
3. Execute the LOOP option.

See MD section for an explanation of the scope loop preparation.

Check the circuits on the error condition diagram for intermittent opens or shorts to ground or other active signal lines.

See the CARR section in the Maintenance Information Manual for diskette drive voltage checks.

Diagnostic Check 4

Note: Replace the diskette with a known good one before performing the diagnostic checks.

If another diskette at the same engineering change level is available to swap, try to recreate the error condition. If a diskette is not available call for diagnostic assistance.

Diagnostic Check 5

Note: Replace the diskette with a known good one before performing the diagnostic checks.

The microprocessor checks the speed of the diskette by timing the interval between index pulses. The nominal speed of the diskette is 166.66 ms per revolution (+3.98 ms, -4.66 ms). If the drive motor, belt, and pulley have not been changed, check them before continuing with this check.

Prepare a scope loop as follows:

1. Prepare the MD for manual control operation as shown in the MD section of the MSM.
2. Select the failing storage director.
3. Execute the LOOP option.

See MD section for an explanation of the scope loop preparation.

Use a scope to check the circuits on the error condition diagram for intermittent opens or shorts to ground or other active signal lines.

Note: Missing or extra index pulses can also cause these error codes.

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F181	15	3	B07
F182	15	3	B07
F183	15	3	B07
F186	15	3	B07
F187	15	3	B07
F1D0	15	3	B07
F201	15	3	B07
F202	15	3	B07
F203	20	3	B09
F204	20	3	B09
F205	20	3	B09
F206	20	3	B09
F207	20	3	B09
F208	20	3	B09
F209	20	3	B09
F20A	20	3	B09
F20B	20	3	B09
F20C	25	3	B11
F210	25	3	B11
F211	25	3	B11
F212	25	3	B11
F213	25	3	B11
F216	25	3	B11
F217	25	3	B11
F218	25	3	B11
F219	30	3	B13
F220	30	3	B13
F221	30	3	B13
F222	30	3	B13
F223	30	3	B13
F224	30	3	B13
F225	30	3	B13
F226	35	3	B15
F227	35	3	B15
F228	35	3	B15
F229	35	3	B15
F230	35	3	B15
F231	35	3	B15
F232	35	3	B15

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
F233	40	3	B17
F234	40	3	B17
F235	40	3	B17
F236	40	3	B17
F237	40	3	B17
F238	40	3	B17
F239	40	3	B17
F240	40	3	B17
F241	45	3	C01
F242	45	3	C01
F243	45	3	C01
F244	45	3	C01
F245	45	3	C01
F246	45	3	C01
F247	50	3	C03
F248	50	3	C03
F249	50	3	C03
F250	50	3	C03
F251	50	3	C03
F252	50	3	C03
F253	55	3	C05
F254	55	3	C05
F255	55	3	C05
F256	55	3	C05
F257	55	3	C05
F258	55	3	C05
F259	55	3	C05
F260	55	3	C05
F27F	55	3	C05
F281	15	3	B07
F282	15	3	B07
F283	20	3	B09
F284	20	3	B09
F285	20	3	B09
F286	20	3	B09
F287	20	3	B09
F288	20	3	B09
F289	20	3	B09
F28A	20	3	B09
F28B	20	3	B09
F28C	25	3	B11
F290	25	3	B11
F291	25	3	B11
F292	25	3	B11
F293	25	3	B11
F296	25	3	B11
F297	25	3	B11
F298	25	3	B11
F299	30	3	B13
F2A0	30	3	B13
F2A1	30	3	B13
F2A2	30	3	B13
F2A3	30	3	B13
F2A4	30	3	B13
F2A5	30	3	B13

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
F2A6	35	3	B15
F2A7	35	3	B15
F2A8	35	3	B15
F2A9	35	3	B15
F2B0	35	3	B15
F2B1	35	3	B15
F2B2	35	3	B15
F2B3	40	3	B17
F2B4	40	3	B17
F2B5	40	3	B17
F2B6	40	3	B17
F2B7	40	3	B17
F2B8	40	3	B17
F2B9	40	3	B17
F2C0	40	3	B17
F2C1	45	3	C01
F2C2	45	3	C01
F2C3	45	3	C01
F2C4	45	3	C01
F2C5	45	3	C01
F2C6	45	3	C01
F2C7	50	3	C03
F2C8	50	3	C03
F2C9	50	3	C03
F2D0	50	3	C03
F2D1	50	3	C03
F2D2	50	3	C03
F2D3	55	3	C05
F2D4	55	3	C05
F2D5	55	3	C05
F2D6	55	3	C05
F2D7	55	3	C05
F2D8	55	3	C05
F2D9	55	3	C05
F2E0	55	3	CC5
F2FF	55	3	C05

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

See the SENSE section in the MSM for a description of the check conditions.

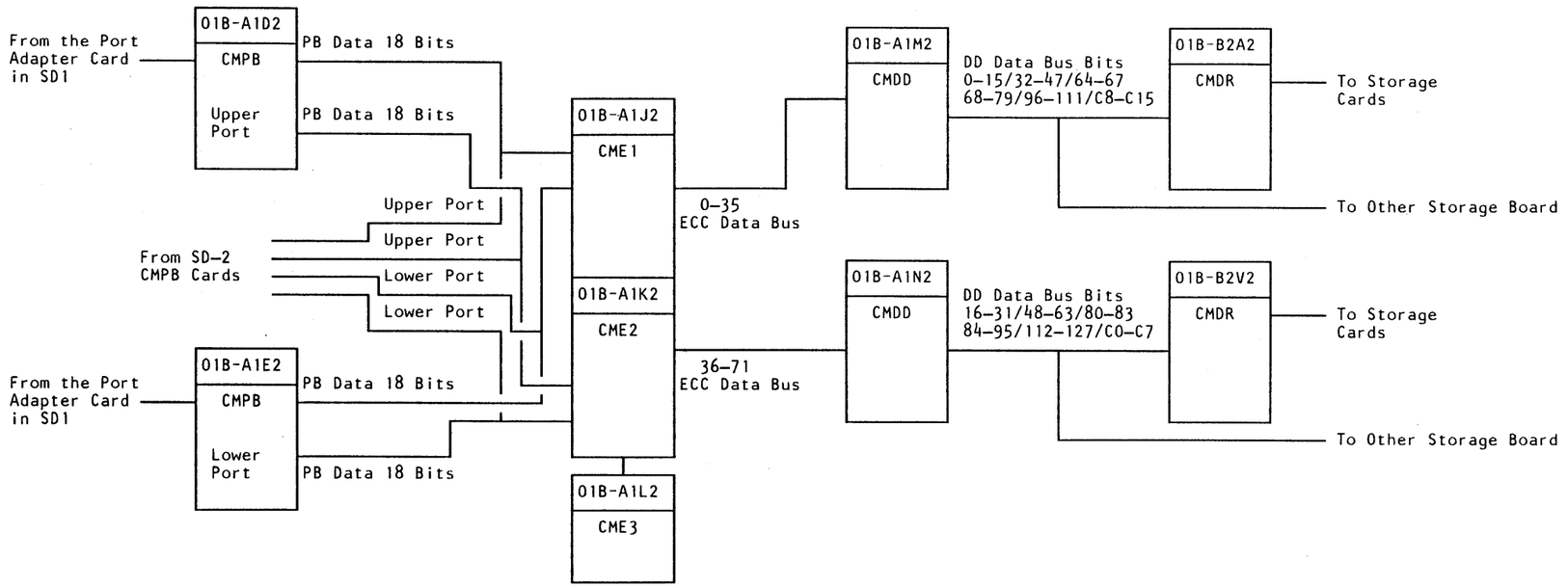
See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Port Data Path Error Code Diagram

Port Data Paths

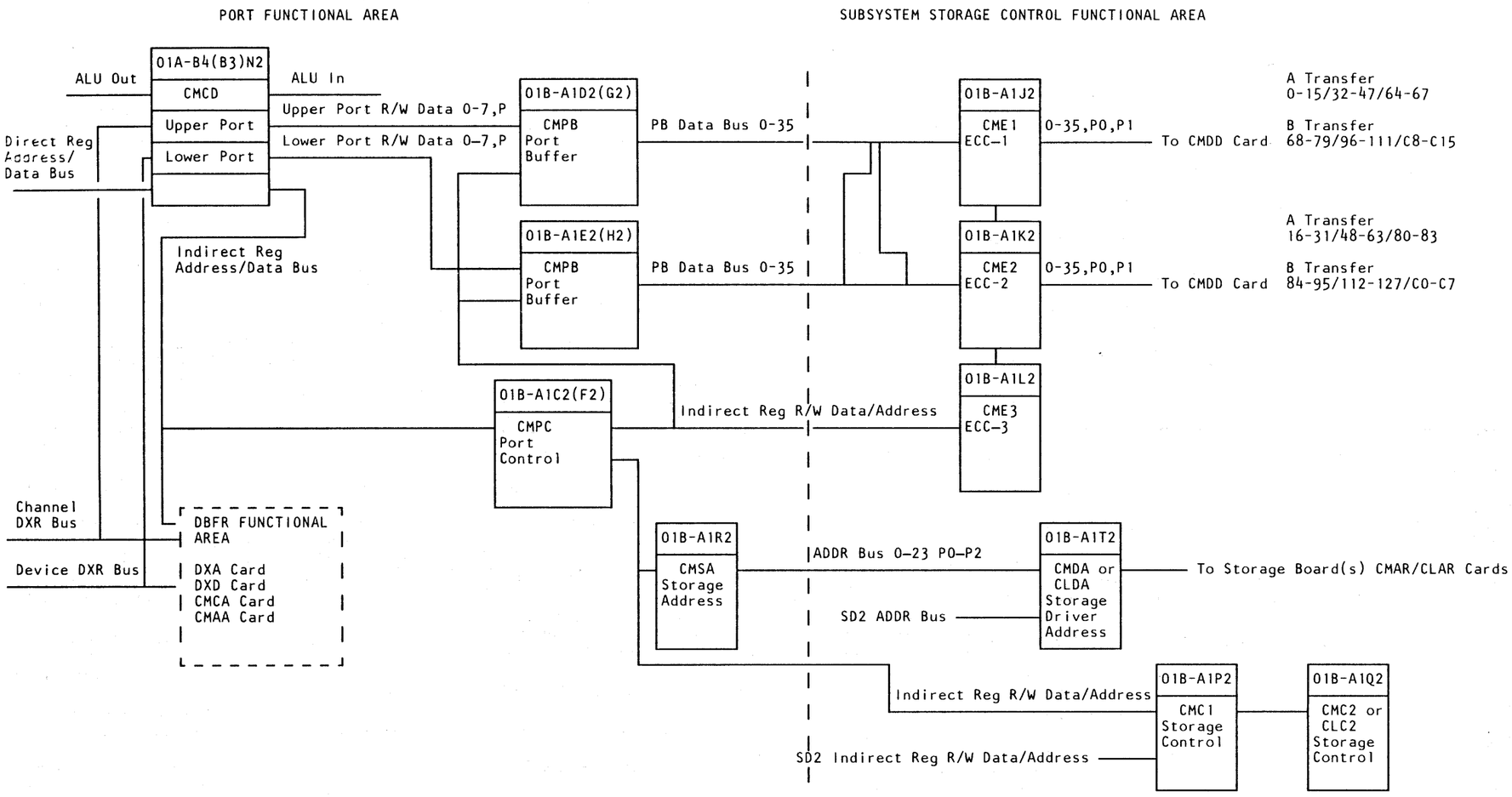
On a store operation, data enters the port buffer (CMPB card) one byte at a time. It is transferred to the ECC function (CME1-CME2) four bytes at a time (two bytes to CME1 and two bytes to CME2). Byte parity is ignored at the CME1 and CME2 cards and, at this point, the CME1, CME2, and CME3 cards generate two check bytes and two parity bits per A and B transfer. The 16 byte word and check bytes are then transferred to the Data Drivers (CMDD cards) 72 bits at a time, 36 bits to each CMDD card (two transfers). The data is then gated to the data redrivers (CMDR cards) and on to the storage cards (CMSH or CLP2/CLP4 cards). This occurs in one 400 nanosecond cycle that has two parts, an A transfer and a B transfer.

Note: Each CMAR/CLAR (Address Redrive card) addresses half of the storage cards in the board. CMAR/CLAR card K2 address the data bits associated with CMDR (Data Redrive card) A2. CMAR/CLAR card L2 addresses the data bits associated with CMDR card V2.



3880 ECM	Seq HT0001	PN 6315694 2 of 13	881145 13 Jan 84	881216 15 Aug 84	A15621 01 Apr 85		

Port Functional Area Error Code Diagram **PORT 10**



Note: See the OPER section of the MSM for a detailed description of this area

The CLC1, CLDA, and CLAR cards are used with expanded storage

SC F101 (SD1) or SC F181 (SD2)

Communication Check: Is set because bit 4 in the CSTAT3 register was active. This indicates a parity error on the IR address bus, or the data bus in or bus out of the communication buffer.

Card detecting the error:

01A-B3M2

FRU List

01A-B3M2 80%
01A-B4M2 10%
01A-B4N2
01A-B3N2
Cable: 01A-B4YM to 01A-B3YM
Cable: 01A-B4YL to 01A-B3YL

Note: If this error occurs on SD1, it can be caused by the communication card in SD2.

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F102 (SD1) or SC F182 (SD2)

SD Indicator Check: Is set because both SDs or neither SD indicator is active. (CSTAT4 bits 1 and 2 cause the CCOMACK register bit 7 to be set).

Card detecting the error:

01A-B3M2

FRU List

01A-B4(B3)M2 90%
Cable: 01A-B3ZE to 01B-A1B5 (SD2 only)
Cable: 01A-B4ZE to 01B-A1A5 (SD1 only)

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F103 (Port 1) or SC F183 (Port 2)

Test and Set Check: Is set because the Test and Set Obtained bit is active for both SDs. (Bit 0 of the CSACK register is active).

Card detecting the error:

01A-B4(B3)M2

FRU List

Port 1	Port 2
01B-A1P2	01B-A1P2 60%
01B-A1R2	01B-A1S2 20%
01B-A1S2	01B-A1R2 20%
01B-A1 WRST TCC	01B-A1 WRST TCC

Diagnostic Checks

Refer to Diagnostic Check 3 on page PORT 65.

SC F106 (Port 1) or SC F186 (Port 2)

Refresh Address Increment Check: Is set because of a parity error in the storage addressing during refresh. (Bit 6 of the CSARCK register is active).

Card detecting the error:

01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1T2	01B-A1T2 40%
01B-A1R2	01B-A1S2 30%
01B-A1S2	01B-A1R2 20%
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F107 (Port 1) or SC F187 (Port 2)

DA Refresh Address Check: Is set because of a parity error in the storage addressing during refresh. (Bit 7 of the CSARCK register is active).

Card detecting the error:

01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1T2	01B-A1T2 50%
01B-B2L2	01B-B2L2 20%
01B-B2K2	01B-B2K2 20%
01B-A1R2	01B-A1S2
01B-A1S2	01B-A1R2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F150 (Port 1) or SC F1D0 (Port 2)

Common Check: Is set because the common check generator was called and none of the expected bits in the CSCRACK register were active.

Card detecting the error:

01A-B4(B3)M2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 30%
01B-A1P2	01B-A1P2
01A-B4M2	01A-B3M2
Cable	Cable
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F201 (Port 1) or F281 (Port 2)

Address Error: Is set because of an indirect register address error.

Card detecting the error:

01A-B4(B3)N2, CMCD Card

FRU List

01A-B4(B3)M2 60%
01A-B4(B3)N2 30%
01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F202 (Port 1) or F282 (Port 2)

IR Control Error: Is set because of an indirect register control error.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 60%
01A-B4(B3)N2 30%
01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F203 (Port 1) or F283 (Port 2)

IR Data Bus Error: Is set because of an IR data bus error (CMCD to subsystem storage control board).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 70%
01A-B4M2	01A-B3M2 10%
01B-A1R2	01B-A1S2 10%
01A-B4N2	01A-B3N2
01B-A1P2	01B-A1P2
01B-A1E2	01B-A1H2
01B-A1D2	01B-A1G2
01A-B4L2	01A-B3L2
01A-A1L2	01A-A1L2
Cable	Cable
01A-B4M3 to	01A-B3M3 to
01B-A1A2	01B-A1B2
01A-B4 WLMN TCC	01A-B3 WLMN TCC

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F204 (Port 1) or F284 (Port 2)

IR Summary Check: Is set because of an IR error has modified the sense data.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4M2	01A-B3M2 80%
01B-A1C2	01B-A1F2 10%
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F205 (Port 1) or F285 (Port 2)

IR Data Bus Error: Is set because of an IR Data Bus error on a subsystem storage control board to CMCD card read.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01B-A1C2	01B-A1F2 20%
01B-A1L2	01B-A1L2
01B-A1P2	01B-A1P2
01B-A1E2	01B-A1H2
01B-A1D2	01B-A1G2
01A-B4M2	01A-B3M2 90%
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F206 (Port 1) or F286 (Port 2)

IR Summary Check: Is set because of an IR error has modified the sense data.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 70%
01A-B4M2	01A-B3M2 20%
01A-B4L2	01A-B3L2
01A-B4N2	01A-B3N2

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F207 (Port 1) or F287 (Port 2)

IR Bus Errors: Is set because of an IR bus error on a write to a CMCD indirect register.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 90%
01A-B4(B3)N2
01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F208 (Port 1) or F288 (Port 2)

IR Bus Error: Is set because of an IR bus error on a write to a CMAA register.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 90%
01A-B4(B3)N2
01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F209 (Port 1) or F289 (Port 2)

IR Bus Error: Is set because of an IR bus error on a write to a CMCA register.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 90%
01A-B4(B3)N2
01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F20A (Port 1) or F28A (Port 2)

IR Data Bus Error: Is set because of an address decode error or a control error on the IR Data bus. (Bits 2, 3, and 4 are active in the CSPRDIC register.)

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 50%
01A-B4M2	01A-B3M2 50%

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F20B (Port 1) or F28B (Port 2)

IR Control Check: Is set because of a control error on the IR bus when addressing the CMAA card. (Bits 2 and 4 are active in the CSPRDIC register.)

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 40%
01A-B4M2	01A-B3M2 30%
01B-A1C2	01B-A1F2 20%
01B-A1E2	01B-A1H2
01B-A1D2	01B-A1G2
01B-A1P2	01B-A1P2
01B-A1L2	01B-A1L2
01A-B4 YLMN TCC	01A-B3 YLMN TCC
Cable	Cable
01A-B4ZE to	01A-B3ZE to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F20C (Port 1) or F28C (Port 2)

IR Control Check: Is set because of an IR Data Bus control check. (Bits 1, 2, and 4 are active in the CSPRDIC register.)

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 70%
01A-B4M2	01A-B3M2 20%
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Checks 1 page PORT 65.

SC F210 (Port 1) or F290 (Port 2)

IR Bus Errors: Is set because of an IR bus error on a read from a CMAA register.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F211 (Port 1) or F291 (Port 2)

IR Bus Error: Is set because of an IR bus error on a read from a CMCA register.

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F212 (Port 1) or SC F292 (Port 2)

Multiple IR Summary Checks: Is set because of the Port Adapter IR Summary Check and the Read Clock Delayed Check being active. (Bit 2 of the CSPRDIC and bit 5 of the CPACK registers were active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4M2	01A-B3M2 40%
01A-B3M2	01A-B4M2 30%
01B-A1C2	01B-A1F2 20%
01A-B4N2	01A-B3N2
01B-A1D2	01B-A1G2
01B-A1E2	01B-A1H2
01B-A1R2	01B-A1S2
01A-B4L2	01A-B3L2
01B-A1P2	01B-A1P2
01B-A1L2	01B-A1L2
01A-B4 YLMN TCC	01A-B3 YLMN TCC
01B-A1 XCDE TCC	01B-A1 XFGH TCC
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F213 (Port 1) or SC F293 (Port 2)

Port Adapter IR Summary Check: Is set because the Port Adapter IR Summary Check is active. (Bit 2 of the CSPRDIC register was active and some bits of CPACK1 may be active.)

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 50%
01A-B4M2	01A-B3M2 30%
01A-B4N2	01A-B3N2 10%
01A-B4L2	01A-B3L2
01B-A1K2	01B-A1K2
01B-A1J2	01B-A1J2
01B-A1D2	01B-A1G2
01B-A1E2	01B-A1H2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01B-A1P2	01B-A1P2
01B-B4 WLMN TCC	01B-B3 WLMN TCC
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

SC F216 (Port 1) or SC F296 (Port 2)

Port Control IR Summary Check: Is set because the Port Control IR Summary Check is active. (Bit 3 of the CSPRDIC register was active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 60%
01B-A1P2	01B-A1P2 30%
01A-B4M2	01A-B3M2
01B-A1D2	01B-A1G2
01B-A1E2	01B-A1H2
01B-A1R2	01B-A1S2
01A-B4N2	01A-B3N2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F217 (Port 1) or SC F297 (Port 2)

Control Board IR Summary Check: Is set because of a read/write register clock error.

Card detecting the error:

01A-B4(B3)N2
01A-A1R2 - Port 1
01A-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 70%
01A-B4M2	01A-B3M2 30%
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F218 (Port 1) or F298 (Port 2)

Control Board IR Summary Check: Is set because of an IR error on CMPB/CME3 interface of the CMPC card.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 30%
01B-A1D2	01B-A1G2 30%
01B-A1E2	01B-A1H2 30%
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F219 (Port 1) or SC F299 (Port 2)

Control Board IR Summary Check: Is set because the Control Board IR Summary Check is active and the Storage Adapter and Storage Control IR Checks are active. (Bit 4 of the CSPRDIC register and bits 6 and 7 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01A-A1R2 - Port 1
01A-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 90%
01B-A1P2	01B-A1P2
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F220 (Port 1) or SC F2A0 (Port 2)

Control Board IR Summary Check and Upper Port Buffer IR Check: Is set because the Control Board IR Summary Check and the Upper Port Buffer IR Check are active. (Bit 4 of the CSPRDIC register and bit 2 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01A-A1R2 - Port 1
01A-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1L2	01B-A1G2 30%
01B-A1E2	01B-A1L2 30%
01B-A1D2	01B-A1H2 30%
01B-A1C2	01B-A1F2
01B-A1R2	01B-A1S2
01B-A1 WCDE TCC	01B-A1 WFGH TCC
01B-A1 XCDE TCC	01B-A1 XFGH TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F221 (Port 1) or SC F2A1 (Port 2)

Control Board IR Summary Check and Lower Port Buffer IR Check: Is set because the Control Board IR Summary Check and the Lower Port Buffer IR Check are active. (Bit 4 of the CSPRDIC register and bit 4 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1E2 40%	01B-A1H2 30%
01B-A1L2 30%	01B-A1L2 30%
01B-A1D2 20%	01B-A1G2 30%
01B-A1C2	01B-A1F2
01B-A1R2	01B-A1S2
01B-A1 XCDE TCC	01B-A1 XFGH TCC
01B-A1 WCDE TCC	01B-A1 WFGH TCC

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200

SC F222 (Port 1) or SC F2A2 (Port 2)

Control Board IR Summary Check and ECC IR Check: Is set because the Control Board IR Summary Check and the ECC IR Check are active. (Bit 4 of the CSPRDIC register and bit 5 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1L2	01B-A1L2 60%
01B-A1C2	01B-A1F2 10%
01B-A1D2	01B-A1G2 10%
01B-A1E2	01B-A1H2 10%
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F223 (Port 1) or SC F2A3 (Port 2)

Control Board IR Summary Check and Storage Adapter IR Check: Is set because the Control Board IR Summary Check and the Storage Adapter IR Check are Active. (Bit 4 of the CSPRDIC register and bit 6 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1P2	01B-A1P2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F224 (Port 1) or SC F2A4 (Port 2)

Control Board IR Summary Check and Storage Control IR Check: Is set because the Control Board IR Summary Check and the Storage Control IR Check are Active. (Bit 4 of the CSPRDIC register and bit 7 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 70%
01B-A1P2	01B-A1P2 20%
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F225 (Port 1) or SC F2A5 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active. (Bit 4 of the CSPRDIC register and bit 1 in the CSACK register were active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 10%
01A-B4M2	01A-B3M2 10%
01B-A1C2	01B-A1F2 10%
01A-B4L2	01A-B3L2
01B-A1P2	01B-A1P2
01B-A1E2	01B-A1H2
01B-A1D2	01B-A1G2
01B-A1L2	01B-A1L2
01A-B4 YLMN TCC	01A-B3 YLMN TCC
Cable: 01A-B4ZE to 01B-A1A5	Cable: 01A-B3ZE to 01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F226 (Port 1) or SC F2A6 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter, SD, and Upper Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0, 3, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1D2	01B-A1G2 10%
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F227 (Port 1) or SC F2A7 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter, SD, and Lower Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1, 3, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1E2	01B-A1H2 10%
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F228 (Port 1) or SC F2A8 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter, SD, and ECC IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 2, 3, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 90%
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F229 (Port 1) or SC F2A9 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter, SD, and Storage Control IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 3, 4, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1P2	01B-A1P2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F230 (Port 1) or SC F2B0 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Control, SD, and ECC IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 2, 4, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 90%
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F231 (Port 1) or SC F2B1 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Control, SD, and Lower Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1, 4, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1E2	01B-A1H2 10%
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F232 (Port 1) or SC F2B2 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Control, SD, and Upper Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0, 4, and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1D2	01B-A1G2 10%
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F233 (Port 1) or SC F2B3 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper and Lower Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0 and 1 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 40%
01B-A1D2	01B-A1G2 40%
01B-A1R2	01B-A1S2 20%

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F234 (Port 1) or SC F2B4 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper Port Buffer and ECC IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0 and 2 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1D2	01B-A1G2 10%
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F235 (Port 1) or SC F2B5 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper Port Buffer and Storage Adapter IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0 and 3 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1D2	01B-A1G2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F236 (Port 1) or SC F2B6 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper Port Buffer and Storage Control IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0 and 4 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01B-A1P2	01B-A1P2 30%
01B-A1D2	01B-A1G2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F237 (Port 1) or SC F2B7 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper Port Buffer and SD IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 0 and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 30%
01A-B4M2	01A-B3M2 30%
01B-A1C2	01B-A1F2 30%
01B-A1D2	01B-A1G2
01B-A1R2	01B-A1S2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F238 (Port 1) or SC F2B8 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Upper Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 0 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F239 (Port 1) or SC F2B9 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Lower Port Buffer and ECC IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1 and 2 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 80%
01B-A1E2	01B-A1H2 10%
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F240 (Port 1) or SC F2C0 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Lower Port Buffer and Storage Adapter IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1 and 3 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1E2	01B-A1H2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F241 (Port 1) or SC F2C1 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Lower Port Buffer and Storage Control IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1 and 4 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 70%
01B-A1P2	01B-A1P2 10%
01B-A1E2	01B-A1H2 10%
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F242 (Port 1) or SC F2C2 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Lower Port Buffer and SD IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 1 and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 30%
01A-B4M2	01A-B3M2 30%
01B-A1C2	01B-A1F2 30%
01B-A1E2	01B-A1H2
01B-A1R2	01B-A1S2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F243 (Port 1) or SC F2C3 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Lower Port Buffer IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 1 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F244 (Port 1) or SC F2C4 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with ECC and Storage Adapter IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 2 and 3 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 50%
01B-A1R2	01B-A1S2 40%
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F245 (Port 1) or SC F2C5 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with ECC and Storage Control IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 2 and 4 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 70%
01B-A1P2	01B-A1P2 20%
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F246 (Port 1) or SC F2C6 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with ECC and SD IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 2 and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 30%
01A-B4M2	01A-B3M2 30%
01B-A1C2	01B-A1F2 30%
01B-A1R2	01B-A1S2
01A-B4L2	01A-B3L2
01B-A1L2	01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F247 (Port 1) or SC F2C7 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with ECC IR Decoded also active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 2 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F248 (Port 1) or SC F2C8 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter and Storage Control IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 3 and 4 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1P2	01B-A1P2
01B-A1C2	01B-A1F2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F249 (Port 1) or SC F2C9 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter and SD IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 3 and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 80%
01A-B4M2	01A-B3M2 10%
01B-A1C2	01B-A1F2
01A-B4L2	01A-B3L2
01A-B4N2	01A-B3N2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F250 (Port 1) or SC F2D0 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Adapter IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 3 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01A-B4M2	01A-B3M2 90%
01B-A1R2	01B-A1S2
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F251 (Port 1) or SC F2D1 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Control and SD IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bits 4 and 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 40%
01A-B4N2	01A-B3N2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01B-A1C2	01B-A1F2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F252 (Port 1) or SC F2D2 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with Storage Control IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 4 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01A-B4M2	01A-B3M2 90%
01B-A1R2	01B-A1S2
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F253 (Port 1) or SC F2D3 (Port 2)

Control Board IR Summary Check and Address Decode Check: Is set because the Control Board IR Summary Check and the Address Decode Check are active with SD IR Decoded active. (Bit 4 of the CSPRDIC register, bit 1 in the CSACK register and bit 5 in the CMADEC register are active).

Card detecting the error:

01A-B4(B3)N2
01B-A1R2 - Port 1
01B-A1S2 - Port 2

FRU List

Port 1	Port 2
01B-A1P2	01B-A1P2 80%
01B-A1R2	01B-A1S2 20%

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F254 (Port 1) or SC F2D4 (Port 2)

Control Board IR Summary Check: Is set because the Control Board IR Summary Check is active with none of the other error bits active. (Bit 4 of the CSPRDIC register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 50%
01B-A1C2	01B-A1F2 40%
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F255 (Port 1) or SC F2D5 (Port 2)

SDM ALU Out Parity Check: Is set because of an SDM ALU Out Parity Check. (Bit 1 of the CPACK1 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)N2 90%
01A-B4(B3)M2
01A-B4(B3)Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F256 (Port 1) or SC F2D6 (Port 2)

External Register Address or Decode Check: Is set because of an External Address or Decode Check. (Bit 2 of the CPACK1 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)N2 90%
01A-B4(B3)M2
01A-B4(B3)Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F257 (Port 1) or SC F2D7 (Port 2)

External Register Selection Check: Is set because of an External Register Selection Check. (Bit 3 of the CPACK1 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)N2 90%
01A-B4(B3)Q2
01A-B4(B3)R2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F258 (Port 1) or SC F2D8 (Port 2)

ALU Out Control Check: Is set because of an ALU Out Control Check. (Bit 6 of the CPACK1 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)N2 90%
01A-B4(B3)M2
01A-B4(B3)Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F259 (Port 1) or SC F2D9 (Port 2)

Clock Check: Is set because of a Clock Check. (Bit 4 of the CPACK2 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)N2 90%
01A-B4(B3)M2
01A-B4(B3)P2

Diagnostic Checks

Refer to Diagnostic Check 2 on page PORT 65.

SC F260 (Port 1) or SC F2E0 (Port 2)

Range Select Check: Is set because the two decoders addressing the buffer are not equal. (Bit 7 of the CPACK2 register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

01A-B4(B3)M2 90%
01A-B4(B3)N2
01A-B4(B3) YLMN TCC

Diagnostic Checks

Refer to Diagnostic Check 1 on page PORT 65.

SC F27F (Port 1) or SC F2FF (Port 2)

Port Connection/Port Control Generator Check: Is set because either an unexpected combination of error indicators or no error indicators were set when the SC generator was called.

Card detecting the error:

None

FRU List

Port 1	Port 2
01A-B4L2	01A-B3L2 90%
01A-B4J2	01A-B3J2
01A-B4N2	01A-B3N2
01A-B4M2	01A-B3M2
01B-A1C2	01B-A1F2
01B-A1R2	01B-A1S2
01B-A1P2	01B-A1P2
01B-A1D2	01B-A1G2
01B-A1E2	01B-A1H2
01B-A1L2	01B-A1L2
01A-B4 WLMN TCC	01A-B3 WLMN TCC
01A-B4 YLMN TCC	01A-B3 YLMN TCC

Diagnostic Checks

None

Diagnostic Checks

Diagnostic Check 1

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 50-5C. If an error occurs proceed as directed by the MD.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 2

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 57-5F.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 3

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 65-67.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 4

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Loop diagnostic routine 69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 5

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 68-69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 6

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Loop diagnostic routine 6A.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

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F105	10	3	D07
F109	10	3	D07
F110	10	3	D07
F111	10	3	D07
F112	10	3	D07
F113	10	3	D07
F114	15	3	D09
F115	15	3	D09
F116	15	3	D09
F117	15	3	D09
F118	15	3	D09
F119	15	3	D09
F11A	15	3	D09
F11B	15	3	D09
F120	20	3	D11
F121	20	3	D11
F122	20	3	D11
F123	20	3	D11
F124	20	3	D11
F125	20	3	D11
F126	20	3	D11
F127	20	3	D11
F128	20	3	D11
F129	25	3	D13
F130	25	3	D13
F131	25	3	D13
F132	25	3	D13
F133	25	3	D13
F134	25	3	D13
F135	25	3	D13
F136	25	3	D13
F137	25	3	D13
F138	26	3	D15
F13A	26	3	D15
F13B	26	3	D15
F13C	26	3	D15
F13E	26	3	D15
F13F	26	3	D15
F140	26	3	D15
F142	26	3	D15
F143	26	3	D15
F14A	26	3	D15
F14C	26	3	D15
F14D	26	3	D15
F184	10	3	D07
F185	10	3	D07
F189	10	3	D07
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F191	10	3	D07
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F196	15	3	D09

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F199	15	3	D09
F19A	15	3	D09
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F1A0	20	3	D11
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F1A2	20	3	D11
F1A3	20	3	D11
F1A4	20	3	D11
F1A5	20	3	D11
F1A6	20	3	D11
F1A7	20	3	D11
F1A8	20	3	D11
F1A9	25	3	D13
F1B0	25	3	D13
F1B1	25	3	D13
F1B2	25	3	D13
F1B3	25	3	D13
F1B4	25	3	D13
F1B5	25	3	D13
F1B6	25	3	D13
F1B7	25	3	D13
F1B8	26	3	D15
F1BA	26	3	D15
F1BB	26	3	D15
F1BC	26	3	D15
F1BE	26	3	D15
F1BF	26	3	D15
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F1C2	26	3	D15
F1C3	26	3	D15
F1CA	26	3	D15
F1CC	26	3	D15
F1CD	26	3	D15
F301	26	3	D15
F302	26	3	D15
F303	26	3	D15
F307	30	3	D17
F308	30	3	D17
F309	30	3	D17
F30A	30	3	D17
F310	30	3	D17
F311	30	3	D17
F312	30	3	D17
F313	35	3	E01
F314	35	3	E01
F315	35	3	E01
F316	35	3	E01
F317	35	3	E01
F318	35	3	E01
F319	40	3	E03
F31A	40	3	E03
F31B	40	3	E03
F31C	40	3	E03
F31D	40	3	E03

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F31F	40	3	E03
F320	40	3	E03
F321	40	3	E03
F322	45	3	E05
F323	45	3	E05
F324	45	3	E05
F325	45	3	E05
F326	45	3	E05
F327	45	3	E05
F328	45	3	E05
F329	45	3	E05
F32A	50	3	E07
F32B	50	3	E07
F32C	50	3	E07
F32D	50	3	E07
F32E	50	3	E07
F32F	50	3	E07
F330	50	3	E07
F331	50	3	E07
F332	55	3	E09
F333	55	3	E09
F334	55	3	E09
F335	55	3	E09
F336	55	3	E09
F337	55	3	E09
F338	55	3	E09
F339	55	3	E09
F33A	60	3	E11
F33B	60	3	E11
F340	60	3	E11
F341	60	3	E11
F342	60	3	E11
F343	60	3	E11
F354	60	3	E11
F356	60	3	E11
F357	60	3	E11
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F35F	61	3	E13
F364	61	3	E13
F366	61	3	E13
F367	61	3	E13
F368	61	3	E13
F369	61	3	E13
F36A	61	3	E13
F36C	61	3	E13
F36D	62	4	A05
F36E	62	4	A05
F36F	62	4	A05
F381	26	3	D15
F382	26	3	D15
F383	26	3	D15
F38A	30	3	D17

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F401	62	4	A05
F402	62	4	A05
F403	65	4	A07
F404	65	4	A07
F405	65	4	A07
F406	65	4	A07
F407	65	4	A07
F408	65	4	A07
F409	65	4	A07
F40A	65	4	A07
F40B	65	4	A07
F40C	70	4	A09
F420	70	4	A09
F421	70	4	A09
F422	70	4	A09
F424	70	4	A09
F425	70	4	A09
F426	70	4	A09
F427	70	4	A09
F428	70	4	A09
F429	75	4	A11
F42A	75	4	A11
F42B	75	4	A11
F42C	75	4	A11
F42D	75	4	A11
F42E	75	4	A11
F42F	75	4	A11
F430	76	4	A13
F431	76	4	A13
F432	76	4	A13
F433	80	4	A15
F434	80	4	A15
F435	80	4	A15
F436	85	4	A17
F440	85	4	A17
F441	85	4	A17
F442	85	4	A17
F443	85	4	A17
F444	90	4	B01
F445	90	4	B01
F446	90	4	B01
F447	90	4	B01
F448	90	4	B01
F449	90	4	B01
F44A	90	4	B01
F44B	90	4	B01
F44C	95	4	B03
F460	95	4	B03
F461	95	4	B03
F462	95	4	B03
F464	95	4	B03
F465	95	4	B03
F466	95	4	B03
F467	95	4	B03
F468	95	4	B03

ERROR CODE	PAGE	MICRO FICHE CARD	MICRO FICHE FRAME
F469	100	4	B05
F46A	100	4	B05
F46B	100	4	B05
F46C	100	4	B05
F46D	100	4	B05
F46E	100	4	B05
F46F	100	4	B05
F470	101	4	B07
F471	101	4	B07
F472	101	4	B07
F473	105	4	B09
F474	105	4	B09
F475	105	4	B09
F476	105	4	B09
F480	62	4	A05
F481	62	4	A05
F482	62	4	A05
F483	65	4	A07
F484	65	4	A07
F485	65	4	A07
F486	65	4	A07
F487	65	4	A07
F488	65	4	A07
F489	65	4	A07
F48A	65	4	A07
F48B	65	4	A07
F48C	70	4	A09
F4A0	70	4	A09
F4A1	70	4	A09
F4A2	70	4	A09
F4A4	70	4	A09
F4A5	70	4	A09
F4A6	70	4	A09
F4A7	70	4	A09
F4A8	70	4	A09
F4A9	75	4	A11
F4AA	75	4	A11
F4AB	75	4	A11
F4AC	75	4	A11
F4AD	75	4	A11
F4AE	75	4	A11
F4AF	75	4	A11
F4B0	76	4	A13
F4B1	76	4	A13
F4B2	76	4	A13
F4B3	80	4	A15
F4B4	80	4	A15
F4B5	80	4	A15
F4B6	85	4	A17
F4C0	85	4	A17
F4C1	85	4	A17
F4C2	85	4	A17
F4C3	85	4	A17
F4C4	90	4	B01
F4C5	90	4	B01
F4C6	90	4	B01

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F4C7	90	4	B01
F4C8	90	4	B01
F4C9	90	4	B01
F4CA	90	4	B01
F4CB	90	4	B01
F4CC	95	4	B03
F4E0	95	4	B03
F4E1	95	4	B03
F4E2	95	4	B03
F4E4	95	4	B03
F4E5	95	4	B03
F4E6	95	4	B03
F4E7	95	4	B03
F4E8	95	4	B03
F4E9	100	4	B05
F4EA	100	4	B05
F4EB	100	4	B05
F4EC	100	4	B05
F4ED	100	4	B05
F4EE	100	4	B05
F4EF	100	4	B05
F4F0	101	4	B07
F4F1	101	4	B07
F4F2	101	4	B07
F4F3	105	4	B09
F4F4	105	4	B09
F4F5	105	4	B09
F4F6	105	4	B09
F4F7	110	4	B11
F500	110	4	B11
F501	110	4	B11
F502	110	4	B11
F503	110	4	B11
F504	110	4	B11
F505	110	4	B11
F506	110	4	B11
F507	110	4	B11
F508	115	4	B13
F509	115	4	B13
F50A	115	4	B13
F50B	115	4	B13
F50C	115	4	B13
F50D	115	4	B13
F50E	115	4	B13
F50F	115	4	B13
F511	115	4	B13
F512	115	4	B13
F513	115	4	B13
F514	120	4	B15
F515	120	4	B15
F516	120	4	B15
F517	120	4	B15
F518	120	4	B15
F51E	120	4	B15
F51F	110	4	B09
F520	120	4	B15

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F560	121	4	B17
F562	121	4	B17
F563	121	4	B17
F564	121	4	B17
F565	121	4	B17
F583	110	4	B11
F584	110	4	B11
F585	110	4	B11
F586	110	4	B11
F5A0	120	4	B15
F5A2	120	4	B15
F5A3	120	4	B15
F5A4	120	4	B15
F5A5	120	4	B15
F5E0	121	4	B17
F5E2	121	4	B17
F5E3	121	4	B17
F5E4	121	4	B17
F601	122	4	C01
F602	122	4	C01
F603	122	4	C01
F604	122	4	C01
F605	122	4	C01
F606	122	4	C01
F607	125	4	C03
F608	125	4	C03
F609	125	4	C03
F610	125	4	C03
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F613	125	4	C03
F614	125	4	C03
F615	125	4	C03
F616	130	4	C05
F701	130	4	C05
F702	130	4	C05
F703	130	4	C05
F704	130	4	C05
F781	130	4	C05
F800	130	4	C05
F801	130	4	C05
F802	130	4	C05
F803	130	4	C05
F804	130	4	C05
F805	135	4	C07
F880	130	4	C05
F881	130	4	C05
F882	130	4	C05
F883	130	4	C05
F884	130	4	C05
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F904	135	4	C07
F905	140	4	C09
F906	140	4	C09
F907	140	4	C09
F908	140	4	C09
F90A	140	4	C09
F90B	140	4	C09
F90C	141	4	C11
F90D	141	4	C11
F980	141	4	C11
F981	141	4	C11
F982	141	4	C11
F983	141	4	C11
F984	145	4	C13
F985	145	4	C13
F986	145	4	C13
F987	145	4	C13
F988	145	4	C13
F98A	145	4	C13
F98B	145	4	C13
F98C	146	4	C15
F98D	146	4	C15
F9A0	146	4	C15
F9A1	146	4	C15
F9A2	147	4	C17
F9A3	147	4	C17
F9A4	147	4	C17
F9A5	147	4	C17
F9A6	147	4	C17
F9A7	147	4	C17
F9A8	148	4	D01
F9AA	148	4	D01
F9AB	148	4	D01
F9AC	148	4	D01
F9AD	148	4	D01
F9C0	150	4	D03
F9C1	150	4	D03
F9C2	150	4	D03
F9C3	150	4	D03
F9C4	150	4	D03
F9C5	150	4	D03
F9C6	151	4	D05
F9C7	151	4	D05
F9C8	151	4	D05
F9CA	151	4	D05
F9CB	151	4	D05
F9CC	151	4	D05
F9CD	155	4	D07
F9E0	155	4	D07
F9E1	155	4	D07
F9E2	155	4	D07
F9E3	155	4	D07
F9E4	155	4	D07

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F9E7	156	4	D09
F9E8	156	4	D09
F9EA	156	4	D09
F9EB	156	4	D09
F9EC	156	4	D09
F9ED	156	4	D09
F9FF	160	4	D11
FA01	160	4	D11
FA02	160	4	D11
FA03	160	4	D11
FA04	160	4	D11
FA05	160	4	D11
FA06	160	4	D11
FA07	160	4	D11
FA08	160	4	D11
FA09	160	4	D11
FA0A	160	4	D11
FA0B	160	4	D11
FA0C	160	4	D11
FA0D	160	4	D11
FA11	160	4	D11
FA12	160	4	D11
FA13	160	4	D11
FA14	160	4	D11
FA15	160	4	D11
FA19	165	4	D13
FA1A	165	4	D13
FB02	165	4	D13
FB03	165	4	D13
FB04	165	4	D13
FB05	165	4	D13
FB06	165	4	D13
FB07	165	4	D13
FB08	160	4	D13
FB0A	160	4	D11
FB0B	165	4	D13
FB0C	160	4	D11
FB0D	165	4	D13
FC01	165	4	D13
FC02	165	4	D13
FD02	165	4	D13
FD03	165	4	D13
FD06	165	4	D13
FD10	165	4	D13
FD11	170	4	D15
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FD83	165	4	D13
FD86	165	4	D13
FD90	165	4	D13
FD91	170	4	D15
FEF0	170	4	D15
FEFF	170	4	D15

FRU List Probability of Fix

FRUs are listed for each error code in the order of probability of fixing the problem. Some FRUs have a percentage of probability listed. All FRUs with no percentage listed have an equal probability of fixing the problem.

References to Other Sections

See the DC sections in this manual for a description of the diagnostics.

See the ECI section for an index of error codes shown in this section.

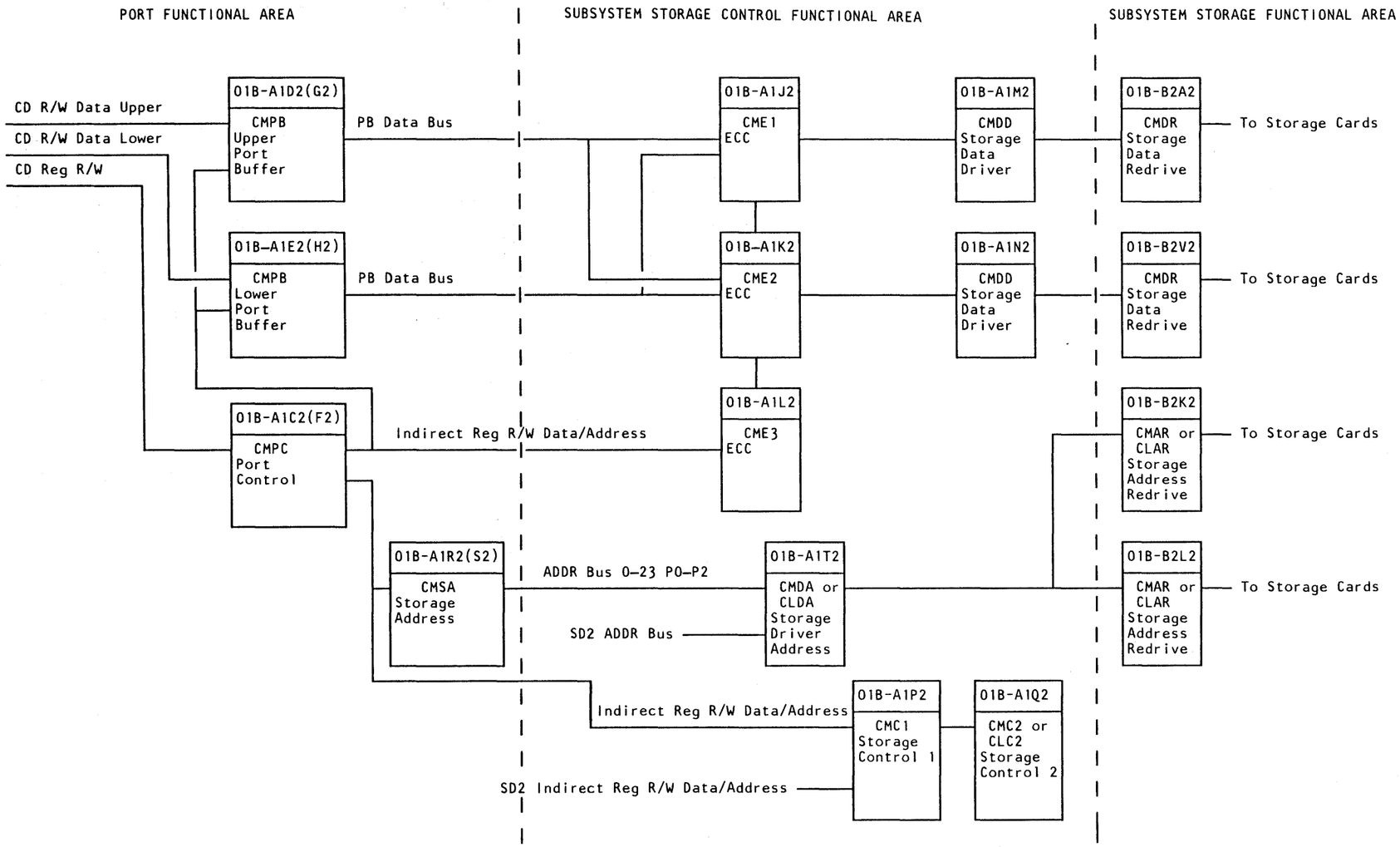
See the OPER section in the Maintenance Support Manual (MSM) to locate high-level circuit diagrams and descriptions of machine functions.

See the MD section in the MSM for a description of the bypass IML error halt routine.

See the SENSE section in the MSM for a description of the check conditions.

See the GLOS section in the MIM for a definition of technical terms and for explanations of abbreviations.

Storage Control Functional Data Path Description **STOR 4**



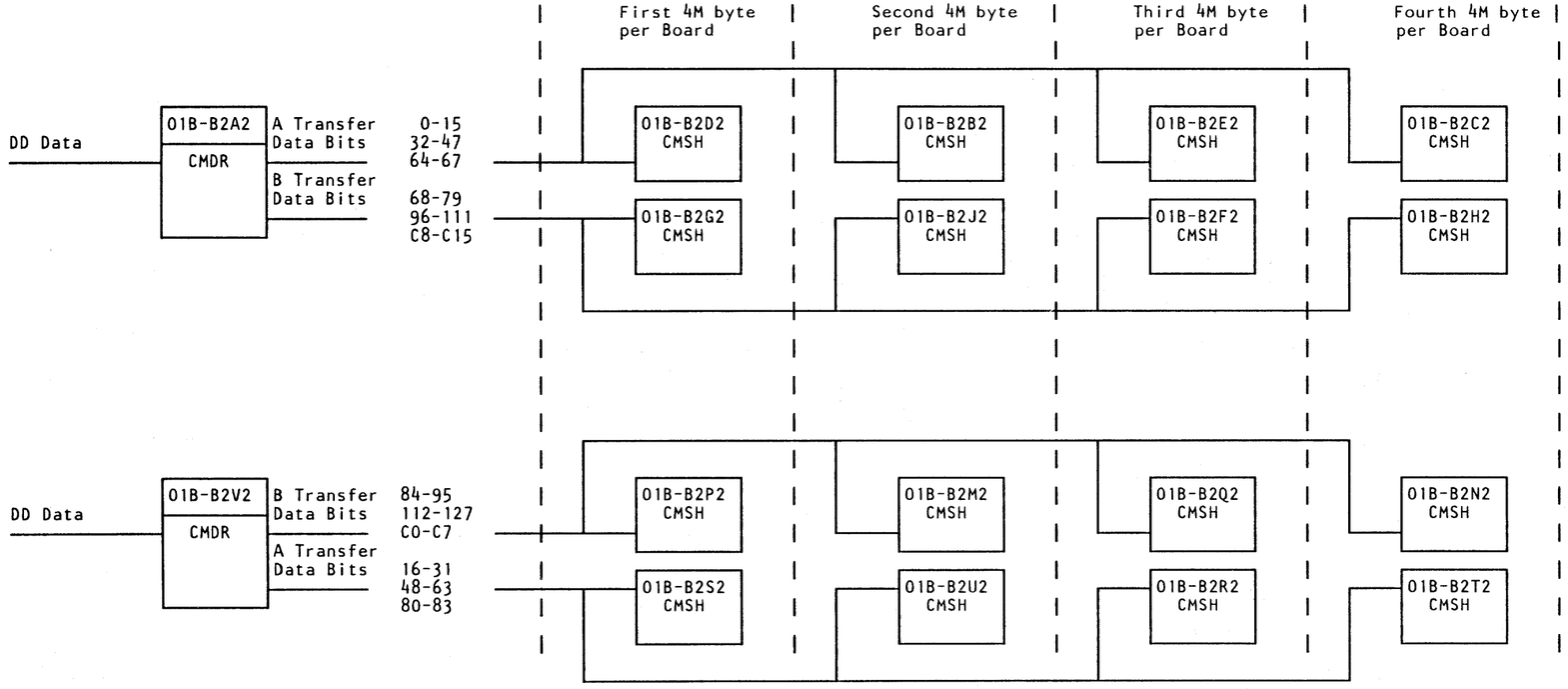
Note: See the OPER section of the MSM for a detailed description of this area

The CLDA, CLC2, and CLAR cards are used with expanded storage

Storage Description Without Expanded Storage

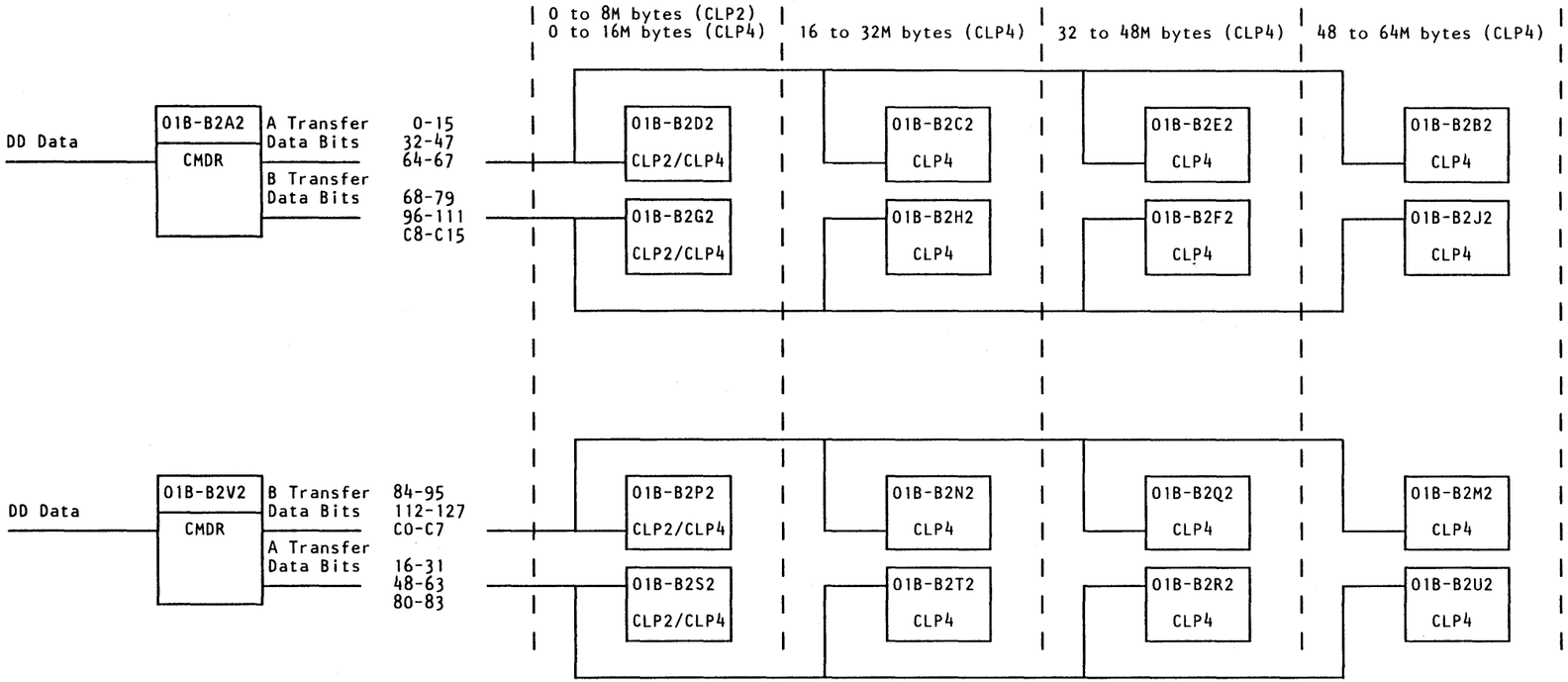
Storage Cards

Note: This diagram shows the cards in the first storage board (16 megabytes of storage). The first 16 megabytes of storage is located at 01B-B2, the second 16 megabytes (16-32) of storage is located at 01B-A2.

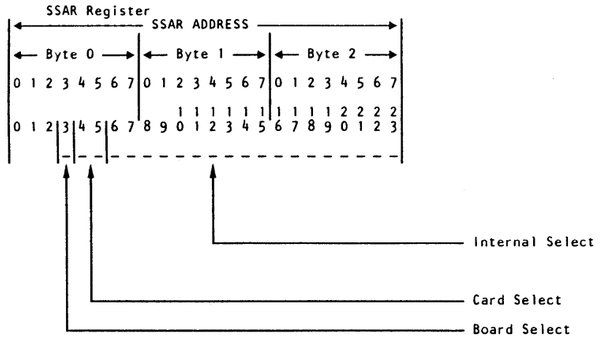


Storage Description With Expanded Storage

Storage Cards



Storage Card Addressing Without Expanded Storage



CARD SELECT BITS 4 AND 5	CMAR card K2		CMAR card L2	
	A Transfer	B Transfer	B Transfer	A Transfer
00 0-4M byte	CMSH card D2	CMSH card G2	CMSH card P2	CMSH card S2
01 4-8M byte	CMSH card B2	CMSH card J2	CMSH card M2	CMSH card U2
10 8-12M byte	CMSH card E2	CMSH card F2	CMSH card Q2	CMSH card R2
11 12-16M byte	CMSH card C2	CMSH card H2	CMSH card N2	CMSH card T2

SSAR Values To Storage Cards

SSAR VALUES FROM SENSE FROM	TO	STORAGE PARTITION	CARD
00 00 00	03 FF FF	0 - 4M byte	01B-B2 D2, G2, P2, S2
04 00 00	07 FF FF	4 - 8M byte	01B-B2 B2, J2, M2, U2
08 00 00	0B FF FF	8 - 12M byte	01B-B2 E2, F2, Q2, R2
0C 00 00	0F FF FF	12 - 16M byte	01B-B2 C2, H2, N2, T2
10 00 00	13 FF FF	16 - 20M byte	01B-A2 D2, G2, P2, S2
14 00 00	17 FF FF	20 - 24M byte	01B-A2 B2, J2, M2, U2
18 00 00	1B FF FF	24 - 28M byte	01B-A2 E2, F2, Q2, R2
1C 00 00	17 FF FF	28 - 32M byte	01B-A2 C2, H2, N2, T2
FF FF FF		Unknown	

Addressing

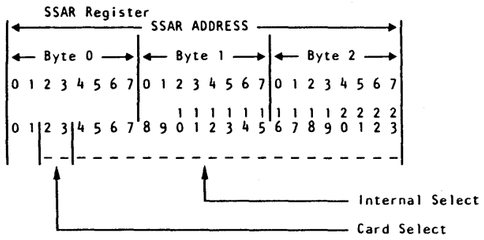
Data transfers to or from storage consist of up to 8 transfers with 16 bytes per transfer (128 bytes). The 8 transfers are controlled by the data gates generated from SSAR bits 21-23. Each 16 byte transfer consists of an A transfer and a B transfer. Each storage board has two address redriver (CMAR) cards, each CMAR card addresses half of the storage (CMSH) cards on the board. Each CMAR card address two storage cards on each 16 byte transfer.

Bits 0-15, 32-47, 64-67, are transferred on the A transfer to one of the CMDR cards, and bits 16-31, 48-63, and 80-83 to the other CMDR card. Bits 68-79, 96-111, C8-C15, are transferred on the B transfer to one of the CMDR cards, and bits 84-95, 112-127, and C0-C7 to the other. Each CMAR card addresses one CMSH card on the A transfer and one on the B transfer.

The Model 21 uses a 24 bit SSAR register to address storage, The bits are used as follows:

Bits 0-2	not used
Bit 3	1 = 32M byte board
	0 = 16M byte board
Bits 4,5	Card select
Bits 6-23	Internal Selection

Storage Card Addressing With Expanded Storage



CARD SELECT BITS 2 AND 3	CLAR card K2		CLAR card L2	
	A Transfer	B Transfer	B Transfer	A Transfer
00 0-8M byte with CLP2 0-16M byte with CLP4	CLP2/CLP4 card D2	CLP2/CLP4 card G2	CLP2/CLP4 card P2	CLP2/CLP4 card S2
01 16-32M byte	CLP4 card C2	CLP4 card H2	CLP4 card N2	CLP4 card T2
10 32-48M byte	CLP4 card E2	CLP4 card F2	CLP4 card Q2	CLP4 card R2
11 48-64M byte	CLP4 card B2	CLP4 card J2	CLP4 card M2	CLP4 card U2

SSAR Values To Storage Cards

SSAR VALUES FROM SENSE FROM	TO	STORAGE PARTITION	CARD
00 00 00	07 FF FE	0 - 8M byte	01B-B2 D2, G2, P2, S2
00 00 00	0F FF FF	0 - 16M byte	01B-B2 D2, G2, P2, S2
10 00 00	1F FF FF	16 - 32M byte	01B-B2 C2, H2, N2, T2
20 00 00	2F FF FF	32 - 48M byte	01B-B2 E2, F2, Q2, R2
30 00 00	3F FF FF	48 - 64M byte	01B-B2 B2, J2, M2, U2
FF FF FF		Unknown	

Addressing

Data transfers to or from storage consist of up to 8 transfers with 16 bytes per transfer (128 bytes). The 8 transfers are controlled by the data gates generated from SSAR bits 21-23. Each 16 byte transfer consists of an A transfer and a B transfer. Each storage board has two address redriver (CLAR) cards, each CLAR card addresses half of the storage (CLP4) cards on the board. Each CLAR card address two storage cards on each 16 byte transfer.

Bits 0-15, 32-47, 64-67, are transferred on the A transfer to one of the CMDR cards, and bits 16-31, 48-63, and 80-83 to the other CMDR card. Bits 68-79, 96-111, C8-C15, are transferred on the B transfer to one of the CMDR cards, and bits 84-95, 112-127, and C0-C7 to the other. Each CLAR card addresses one CLP4 card on the A transfer and one on the B transfer.

A 24 bit SSAR register is used to address storage. The bits are used as follows:

Bits 0,1 not used
Bits 2,3 Card select
Bits 4-23 Internal Selection

SC F104 (Port 1) or SC F184 (Port 2)

SC Clock Check: Is set because of a clock error on the CMC2 card. (Bit 0 of the CSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1Q2 90%
01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F105 (Port 1) or SC F185 (Port 2)

Port Select Check: Is set because more than one port was selected on a storage cycle. (Bit 1 of the CSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1Q2 90%
01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F109 (Port 1) or SC F189 (Port 2)

AR Card Refresh Address Check - K: Is set because a Refresh error is indicated on two storage boards. (Bits 4, 6, and 7 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 40%	01B-B2K2 40%
01B-A1Q2 30%	01B-A1Q2 30%
01B-A1P2 30%	01B-A1P2 30%
	01B-A2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F110 (Port 1) or SC F190 (Port 2)

AR Card Refresh Address Check - K: Is set because of a parity error in SSAR with Refresh active. The error was detected by the CMAR/CLAR card on storage board 1. (Bits 4 and 6 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 90%	01B-B2K2 90%
01B-A1Q2	01B-A2K2
01B-A1P2	01B-A1Q2
01B-B2D2	01B-A1P2
01B-B2C2	01B-B2D2
01B-B2E2	01B-B2C2
01B-B2B2	01B-B2E2
01B-B2G2	01B-B2B2
01B-B2H2	01B-B2G2
01B-B2F2	01B-B2H2
01B-B2J2	01B-B2F2
01B-A1T2	01B-B2J2
	01B-A1T2
Cable	Cable
01B-A1Y6	01B-A1Y6
to	to
01B-B2Y4	01B-B2Y4
Cable	Cable
01B-A1V2	01B-A1V2
to	to
01B-B2Z3	01B-B2Z3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F111 (Port 1) or SC F191 (Port 2)

AR Card Refresh Address Check - K: Is set because of a parity error in SSAR with Refresh active. The error was detected by the CMAR/CLAR card on storage board 2. (Bits 4 and 7 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 70%	01B-A2K2 90%
01B-A1Q2 30%	01B-B2K2
01B-A1P2	01B-A1Q2
01B-A1T2	01B-A1P2
01B-B2B2	01B-A2D2
01B-B2J2	01B-A2G2
01B-B2C2	01B-A2B2
01B-B2H2	01B-A2J2
	01B-A2E2
	01B-A2F2
	01B-A2C2
	01B-A2H2
	01B-A1T2
	Cable
	01B-A136
	to
	01B-A244
	Cable
	01B-A1V5
	to
	01B-A223

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F112 (Port 1) or SC F192 (Port 2)

AR Card Refresh Address Check - K: Is set because Refresh Address Check - K was active with neither storage board active. (Bit 4 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 50%	01B-B2K2 50%
01B-A1Q2 50%	01B-A1Q2 50%
01B-A1P2	01B-A2L2
	01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F113 (Port 1) or SC F193 (Port 2)

AR Card Refresh Address Check - L: Is set because Refresh is active on both storage boards. (Bits 5, 6, and 7 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 40%	01B-B2L2 40%
01B-A1Q2 30%	01B-A1Q2 30%
01B-A1P2 30%	01B-A1P2 30%
	01B-A2L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F114 (Port 1) or SC F194 (Port 2)

AR Card Refresh Address Check L: Is set because of a parity error in SSAR with Refresh active. The error was detected by the CMAR/CLAR card on storage board 1. (Bits 5 and 6 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 90%	01B-B2L2 90%
01B-A1Q2	01B-A2L2
01B-A1P2	01B-A1Q2
01B-B2P2	01B-A1P2
01B-B2N2	01B-B2P2
01B-B2Q2	01B-B2N2
01B-B2M2	01B-B2Q2
01B-B2S2	01B-B2M2
01B-B2T2	01B-B2S2
01B-B2R2	01B-B2T2
01B-B2U2	01B-B2R2
	01B-B2U2
Cable	Cable
01B-A1Y6	01B-A1Y6
to	to
01B-B2Y4	01B-B2Y4
Cable	Cable
01B-A1V2	01B-A1V2
to	to
01B-B2Z3	01B-B2Z3
	01B-A1Z6
	to
	01B-A2Y4
	Cable
	01B-A1V5
	to
	01B-A2Z3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F115 (Port 1) or SC F195 (Port 2)

AR Card Refresh Address Check - L: Is set because of a parity error in SSAR with Refresh active. The error was detected by the CMAR/CLAR card on storage board 2. (Bits 5 and 7 of the CSCRACK register are active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 70%	01B-A2L2 90%
01B-A1Q2 30%	01B-B2L2
01B-A1P2	01B-A1Q2
	01B-A1P2
	01B-A2P2
	01B-A2N2
	01B-A2Q2
	01B-A2M2
	01B-A2S2
	01B-A2T2
	01B-A2R2
	01B-A2U2
	Cable

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F116 (Port 1) or SC F196 (Port 2)

AR Card Refresh Address Check - L: Is set because Refresh was not active on either storage board during a refresh cycle. (Bit 5 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 50%
01B-A1Q2 50%
01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F117 (Port 1) or SC F197 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address checks BCHJ and DEFG with storage board 1 Refresh active. (Bits 0, 1, and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-A1Q2
01B-B2D2
01B-B2G2
01B-B2B2
01B-B2J2
01B-B2E2
01B-B2F2
01B-B2C2
01B-B2H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F118 (Port 1) or SC F198 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address checks BCHJ and DEFG with storage board 2 Refresh active. (Bits 0, 1, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A1Q2
01B-A2D2
01B-A2G2
01B-A2B2
01B-A2J2
01B-A2E2
01B-A2F2
01B-A2C2
01B-A2H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F119 (Port 1) or SC F199 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address checks MNTU and PQRS with storage board 1 Refresh active. (Bits 2, 3, and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-A1Q2
01B-B2P2
01B-B2S2
01B-B2M2
01B-B2U2
01B-B2Q2
01B-B2R2
01B-B2N2
01B-B2T2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F11A (Port 1) or SC F19A (Port 2)

Storage Card Refresh Address Check: Is set because storage card address checks MNTU and PQRS with storage board 2 Refresh active. (Bits 2, 3, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A1Q2
01B-A2P2
01B-A2S2
01B-A2M2
01B-A2U2
01B-A2Q2
01B-A2R2
01B-A2N2
01B-A2T2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F11B (Port 1) or SC F19B (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check BCHJ with storage boards 1 and 2 Refresh active. (Bits 0, 6, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 40%	01B-B2K2 40%
01B-A1Q2 30%	
01B-A1P2 30%	01B-A1Q2 30%
	01B-A1P2 30%
	01B-A2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F120 (Port 1) or SC F1A0 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check BCHJ with storage board 1 Refresh active. (Bits 0 and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2B2
01B-B2J2
01B-B2C2
01B-B2H2
01B-A2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F121 (Port 1) or SC F1A1 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check BCHJ with storage board 2 Refresh active. (Bits 0 and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2	01B-A2K2 90%
	01B-A2B2
	01B-A2J2
	01B-A2C2
	01B-A2H2
	01B-B2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F122 (Port 1) or SC F1A2 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check BCHJ was active with Refresh not active to any storage board. (Bit 0 of the CSCRACK register active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F123 (Port 1) or SC F1A3 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check DEFG with storage boards 1 and 2 Refresh active. (Bits 1, 6, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 40%	01B-B2K2 40%
01B-A1Q2 30%	01B-A1Q2 30%
01B-A1P2 30%	01B-A1P2 30%
	01B-A2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F124 (Port 1) or SC F1A4 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check DEFG with storage board 1 Refresh active. (Bits 1 and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2D2
01B-B2G2
01B-B2E2
01B-B2F2
01B-A2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F125 (Port 1) or SC F1A5 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check DEFG with storage board 2 Refresh active. (Bits 1 and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2	01B-A2K2 90%
	01B-A2D2
	01B-A2G2
	01B-A2E2
	01B-A2F2
	01B-B2K2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F126 (Port 1) or SC F1A6 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check DEFG is active with Refresh not active to any storage board. (Bit 1 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 40%	01B-B2L2 40%
01B-A1Q2 30%	01B-A1Q2 30%
01B-A1P2 30%	01B-A1P2 30%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F127 (Port 1) or SC F1A7 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check MNTU with storage boards 1 and 2 Refresh active. (Bits 2, 6, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 40%	01B-B2L2 40%
01B-A1Q2 30%	01B-A1Q2 30%
01B-A1P2 30%	01B-A1P2 30%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F128 (Port 1) or SC F1A8 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check MNTU with storage board 1 Refresh active. (Bits 2 and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2M2
01B-B2U2
01B-B2N2
01B-B2T2
01B-A2L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F129 (Port 1) or SC F1A9 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check MNTU with storage board 2 Refresh active. (Bits 2 and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2	01B-A2L2 90%
	01B-A2M2
	01B-A2U2
	01B-A2N2
	01B-A2T2
	01B-B2L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F130 (Port 1) or SC F1B0 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check MNTU is active with Refresh not active to any storage board. (Bit 2 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F131 (Port 1) or SC F1B1 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check PQRS with storage boards 1 and 2 Refresh active. (Bits 3, 6, and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 40%	01B-B2L2 40%
01B-A1Q2 30%	01B-A2L2 30%
01B-A1P2 30%	01B-A1Q2 20%
	01B-A1P2 20%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F132 (Port 1) or SC F1B2 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check PQRS with storage board 1 Refresh active. (Bits 3 and 6 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2P2
01B-B2S2
01B-B2Q2
01B-B2R2
01B-A2L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F133 (Port 1) or SC F1B3 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check PQRS with storage board 2 Refresh active. (Bits 3 and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2	01B-A2L2 90%
	01B-A2P2
	01B-A2S2
	01B-A2Q2
	01B-A2R2
	01B-B2L2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F134 (Port 1) or SC F1B4 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check PQRS is active with Refresh not active to any storage board. (Bit 3 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F135 (Port 1) or SC F1B5 (Port 2)

Storage Board Refresh Check: Is set because storage board 1 and storage board 2 Refresh were both active. (Bits 6 and 7 of the CSCRACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F136 (Port 1) or SC F1B6 (Port 2)

Storage Board Refresh Check: Is set because storage board 1 Refresh indicator is active with no refresh in progress. (Bit 6 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F137 (Port 1) or SC F1B7 (Port 2)

Storage Board Refresh Check: Is set because storage board 2 Refresh indicator is active with no refresh in progress. (Bit 7 of the CSCRACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F138, F13A, F13B (Port 1) or SC F1B8, F1BA, F1BB (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check BCHJ with storage board 1 Refresh active. (Bits 0 and 6 of the CSCRACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F138, F1B8

01B-B2K2

FRU List F13A, F1BA

01B-B2K2 90%
01B-B2C2
01B-B2H2

FRU List F13B, F1BB

01B-B2K2 90%
01B-B2C2
01B-B2H2
01B-B2B2
01B-B2J2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F13C, F13E, F13F (Port 1) or SC F1BC, F1BE, F1BF (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check DEFG with storage board 1 Refresh active. (Bits 1 and 6 of the CSCRACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F13C, F13E, F1BC, F1BE

01B-B2K2 90%
01B-B2D2
01B-B2G2

FRU List F13F, F1BF

01B-B2K2 90%
01B-B2D2
01B-B2G2
01B-B2E2
01B-B2F2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F140, F142, F143 (Port 1) or SC F1C0, F1C2, F1C3 (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check MNTU with storage board 1 Refresh active. (Bits 2 and 6 of the CSCRACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F140, F1C0

01B-B2L2

FRU List F142, F1C2

01B-B2L2 90%
01B-B2N2
01B-B2T2

FRU List F143, F1C3

01B-B2L2 90%
01B-B2N2
01B-B2T2
01B-B2M2
01B-B2U2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F14A, F14C, F14D (Port 1) or SC F1CA, F1CC, F1CD (Port 2)

Storage Card Refresh Address Check: Is set because storage card address check PQRS with storage board 1 Refresh active. (Bits 3 and 6 of the CSCRACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F14A, F14C, F1CA, F1CC

01B-B2L2 90%
01B-B2P2
01B-B2S2

FRU List F14D, F1CD

01B-B2L2 90%
01B-B2P2
01B-B2S2
01B-B2Q2
01B-B2R2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F301 (Port 1) or SC F381 (Port 2)

SSAR Increment Check: Is set because of a parity error while incrementing SSAR. (Bit 0 of the USADPCK/LSADPCK register was active).

Card detecting the error:

01B-A1R2 Port 1

01B-A1S2 Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F302 (Port 1) or SC F382 (Port 2)

SD - DA Data Address 0-23 Check: Is set because of a parity error on the CMSA to CMDA/CLDA address bus. (Bit 4 of the USADPCK/LSADPCK register was active).

Card detecting the error:

01B-A1R2 Port 1

01B-A1S2 Port 2

FRU List

Port 1	Port2
01B-A1R2	01B-A1S2 50%
01B-A1S2	01B-A1R2 40%
01B-A1T2	01B-A1T2
01B-A1 WRST TCC	01B-A1 WRST TCC
01B-A1 XRST TCC	01B-A1 XRST TCC
01B-A1 YRST TCC	01B-A1 YRST TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F303 (Port 1) or SC F383 (Port 2)

SD - Op Complete Check: Is set because Op complete was raised before inhibit op complete. (Bit 5 of the USADPCK/LSADPCK register was active).

Card detecting the error:

01B-A1R2 Port 1

01B-A1S2 Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 90%
01B-A1Q2	01B-A1Q2 10%

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F307

SD 1 DA Duplicate Card Select Decode Check: Is set because of a decode error on the CMDA/CLDA card. (Bit 2 of the USADPCK/LSADPCK was active).

Card detecting the error:

01B-A1R2
01B-A1S2

FRU List

01B-A1R2 40%
01B-A1S2 30%
01B-A1T2 30%

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F308

DA Data Address 6-15 Check: Is set because of a parity error on the CMDA/CLDA Card. (Bit 3 of the USADPCK/LSADPCK register was active).

Card detecting the error:

01B-A1R2 Port 1
01B-A1S2 Port 2

FRU List

Expanded Storage	Without Expanded Storage
01B-A1T2 70%	01B-A1T2 70%
01B-B2L2 10%	01B-B2L2 10%
01B-B2K2 10%	01B-B2K2 10%
01B-A1R2	01B-A2K2
01B-A1S2	01B-A2L2
	01B-A1R2
	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F309

AR Card Address Check - K and L: Is set because of a parity error on the CMDA/CLDA card. (Bits 4 and 5 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-A1T2 50%	01B-A1T2 50%
01B-B2L2 20%	01B-B2L2 20%
01B-B2K2 20%	01B-B2K2 20%
01B-A1Q2	01B-A2K2
01B-A1R2	01B-A2L2
01B-A1S2	01B-A1Q2
01B-A1P2	01B-A1R2
Cable:	01B-A1S2
01B-A1Y5	01B-A1P2
to	Cable:
01B-B2Y3	01B-A1Z5
Cable:	to
01B-A1Y6	01B-A2Y3
to	Cable:
01B-B2Y4	01B-A1Z6
Cable:	to
01B-A1V2	01B-A2Y4
to	Cable:
01B-B2Z3	01B-A1V5
	to
	01B-A2Z3

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F30A (SD 1) or SC F38A (SD2)

Storage Cycle Check: Is set because none or more than one storage cycle is active. (Bit 1 of the USADPCK/LSADPCK register was active).

Card detecting the error:

01B-A1R2

FRU List

Port 1	Port 2
01B-A1T2	01B-A1T2 40%
01B-A1R2	01B-A1S2 30%
01B-A1P2	01B-A1P2 10%
01B-A1S2	01B-A1R2 10%
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2
01B-A1 YRST TCC	01B-A1 YRST TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F310

AR Card Address Check K with Storage Partition unknown: Is set because of a parity error on a CMAR/CLAR Card. (Bit 4 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F311

AR Card Address Check K: Is set because of a parity error detected by the CMAR card on board 01B-B2. (Bit 4 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2K2 90%	01B-B2K2 90%
01B-A1P2	01B-A1P2
01B-B2B2	01B-B2B2
01B-B2C2	01B-B2C2
01B-B2D2	01B-B2D2
01B-B2E2	01B-B2E2
01B-B2F2	01B-B2F2
01B-B2G2	01B-B2G2
01B-B2H2	01B-B2H2
01B-B2J2	01B-B2J2
	01B-A2K2
	01B-A2B2
	01B-A2J2
	01B-A2C2
	01B-A2H2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F312

AR Card Address Check K: Is set because of a parity error detected by the CMAR card on board 01B-A2. (Bit 4 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

Card detecting the error:

01B-A2K2 90%
01B-A1P2
01B-A1Q2
01B-A2B2
01B-A2C2
01B-A2D2
01B-A2E2
01B-A2F2
01B-A2G2
01B-A2H2
01B-A2J2
01B-B2K2
01B-B2B2
01B-B2J2
01B-B2C2
01B-B2H2
01B-A1 WRST TCC
Cable:
01B-A1V5
to
01B-A2Z3

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F313

AR Card Address Check L with Storage Partition unknown: Is set because of a parity error detected by a CMAR card. (Bit 5 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F314

AR Card Address Check L: Is set because of a parity error detected by the CMAR card on board 01B-B2. (Bit 5 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2L2 90%	01B-B2L2 90%
01B-A1P2	01B-A1P2
01B-B2M2	01B-B2M2
01B-B2N2	01B-B2N2
01B-B2P2	01B-B2P2
01B-B2Q2	01B-B2Q2
01B-B2R2	01B-B2R2
01B-B2S2	01B-B2S2
01B-B2T2	01B-B2T2
01B-B2U2	01B-B2U2
	01B-A2L2
	01B-A2M2
	01B-A2U2
	01B-A2N2
	01B-A2T2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F315

AR Card Address Check L: Is set because of a parity error detected by the CMAR card on board 01B-A2. (Bit 5 of the USCACK/LSCACK register was active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A1P2
01B-A1Q2
01B-A2M2
01B-A2N2
01B-A2P2
01B-A2Q2
01B-A2R2
01B-A2S2
01B-A2T2
01B-A2U2
01B-B2L2
01B-B2M2
01B-B2U2
01B-B2N2
01B-B2T2
01B-A1 WRST TCC
Cable:
01B-A1V5
to
01B-A2Z3

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F316

Storage Card Address Check BCDE and FGHJ: Is set because of an address error from a CMAR-K card. (Bits 0 and 1 of the USCACK/LSCACK register were active with the storage partition unkown).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F317

Storage Card Address Check MNPQ and RSTU: Is set because of an address error from a CMAR-L card. (Bits 2 and 3 of the USCACK/LSCACK register were active with the storage partition unkown).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F318

Storage Card Address Check BCDE: Is set because of an address error - partition unknown. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F319

Storage Card Address Check D: Is set because of an address error in the 0-4M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2D2
01B-B2B2
01B-B2C2
01B-B2E2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31A

Storage Card Address Check B: Is set because of an address error in the 4-8M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2B2
01B-B2C2
01B-B2D2
01B-B2E2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31B

Storage Card Address Check E: Is set because of an address error in the 8-12M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2C2
01B-B2B2
01B-B2D2
01B-B2E2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31C

Storage Card Address Check C: Is set because of an address error in the 12-16M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2C2
01B-B2B2
01B-B2D2
01B-B2E2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31D

Storage Card Address Check D: Is set because of an address error in the 16-20M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2D2
01B-A2B2
01B-A2C2
01B-A2E2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31E

Storage Card Address Check B: Is set because of an address error in the 20-24M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2B2
01B-A2C2
01B-A2D2
01B-A2E2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F31F

Storage Card Address Check E: Is set because of an address error in the 24-28M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2E2
01B-A2B2
01B-A2C2
01B-A2D2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F320

Storage Card Address Check C: Is set because of an address error in the 28-32M byte range. (Bit 0 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2C2
01B-A2B2
01B-A2D2
01B-A2E2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F321

Storage Card Address Check FGHJ: Is set because of an address error - partition unknown. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	**Port 2**
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F322

Storage Card Address Check G: Is set because of an address error in the 0-4M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2G2
01B-B2F2
01B-B2H2
01B-B2J2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F323

Storage Card Address Check J: Is set because of an address error in the 4-8M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2J2
01B-B2F2
01B-B2G2
01B-B2H2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F324

Storage Card Address Check F: Is set because of an address error in the 8-12M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2F2
01B-B2G2
01B-B2H2
01B-B2J2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F325

Storage Card Address Check H: Is set because of an address error in the 12-16M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2H2
01B-B2F2
01B-B2G2
01B-B2J2
01B-A2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y5 to 01B-B2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F326

Storage Card Address Check G: Is set because of an address error in the 16-20M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2G2
01B-A2F2
01B-A2H2
01B-A2J2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F327

Storage Card Address Check J: Is set because of an address error in the 20-24M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2J2
01B-A2F2
01B-A2G2
01B-A2H2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F328

Storage Card Address Check F: Is set because of an address error in the 24-28M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2F2
01B-A2G2
01B-A2H2
01B-A2J2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F329

Storage Card Address Check H: Is set because of an address error in the 28-32M byte range. (Bit 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2, CMC1 Card

FRU List

01B-A2K2 90%
01B-A2H2
01B-A2F2
01B-A2G2
01B-A2J2
01B-B2K2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z5 to 01B-A2Y3

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32A

Storage Card Address Check MNPQ: Is set because of an address error. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32B

Storage Card Address Check P: Is set because of an address error in the 0-4M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2P2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32C

Storage Card Address Check M: Is set because of an address error in the 4-8M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2M2
01B-B2N2
01B-B2P2
01B-B2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32D

Storage Card Address Check Q: Is set because of an address error in the 8-12M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2Q2
01B-B2M2
01B-B2N2
01B-B2P2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32E

Storage Card Address Check N: Is set because of an address error in the 12-16M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2N2
01B-B2M2
01B-B2P2
01B-B2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F32F

Storage Card Address Check P: Is set because of an address error in the 16-20M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2P2
01B-A2M2
01B-A2N2
01B-A2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F330

Storage Card Address Check M: Is set because of an address error in the 20-24M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2M2
01B-A2N2
01B-A2P2
01B-A2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F331

Storage Card Address Check Q: Is set because of an address error in the 24-28M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2Q2
01B-A2M2
01B-A2N2
01B-A2P2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F332

Storage Card Address Check N: Is set because of an address error in the 28-32M byte range. (Bit 2 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2, CMC1 Card

FRU List

01B-A2L2 90%
01B-A2N2
01B-A2M2
01B-A2P2
01B-A2Q2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F333

Storage Card Address Check RSTU: Is set because of an address error. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	**Port 2**
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F334

Storage Card Address Check S: Is set because of an address error in the 0-4M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2S2
01B-B2R2
01B-B2T2
01B-B2U2
01B-A2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F335

Storage Card Address Check U: Is set because of an address error in the 4-8M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2U2
01B-B2R2
01B-B2S2
01B-B2T2
01B-A2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F336

Storage Card Address Check R: Is set because of an address error in the 8-12M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2R2
01B-B2S2
01B-B2T2
01B-B2U2
01B-A2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F337

Storage Card Address Check T: Is set because of an address error in the 12-16M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2T2
01B-B2R2
01B-B2S2
01B-B2U2
01B-A2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Y6 to 01B-B2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F338

Storage Card Address Check S: Is set because of an address error in the 16-20M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2S2
01B-A2R2
01B-A2T2
01B-A2U2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F339

Storage Card Address Check U: Is set because of an address error in the 20-24M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2U2
01B-A2R2
01B-A2S2
01B-A2T2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F33A

Storage Card Address Check R: Is set because of an address error in the 24-28M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2R2
01B-A2S2
01B-A2T2
01B-A2U2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F33B

Storage Card Address Check T: Is set because of an address error in the 28-32M byte range. (Bit 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2T2
01B-A2R2
01B-A2S2
01B-A2U2
01B-B2L2
01B-A1P2
01B-A1 WRST TCC
Cable: 01B-A1Z6 to 01B-A2Y4

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F340

AR Card Address Check K: Is set because of a parity error on the CMAR card on board 01B-B2. (Bits 0 and 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 90%
01B-B2D2
01B-B2G2
01B-B2B2
01B-B2J2
01B-B2E2
01B-B2F2
01B-B2C2
01B-B2H2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F341

AR Card Address Check K: Is set because of a parity error on the CMAR card on board 01B-A2. (Bits 0 and 1 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2K2 90%
01B-A2D2
01B-A2G2
01B-A2B2
01B-A2J2
01B-A2E2
01B-A2F2
01B-A2C2
01B-A2H2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F342

AR Card Address Check L: Is set because of a parity error on the CMAR card on board 01B-B2. (Bits 2 and 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 90%
01B-B2P2
01B-B2S2
01B-B2M2
01B-B2U2
01B-B2Q2
01B-B2R2
01B-B2N2
01B-B2T2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F343

AR Card Address Check L: Is set because of a parity error on the CMAR card on board 01B-A2. (Bits 2 and 3 of the USCACK/LSCACK register were active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2L2 90%
01B-A2P2
01B-A2S2
01B-A2M2
01B-A2U2
01B-A2Q2
01B-A2R2
01B-A2N2
01B-A2T2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F354 or F356

Storage Card Address Check D: Is set because of an address error in the 0-4M byte range. (Bit 0 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F354

01B-B2K2 70%
01B-B2D2 10%
01B-A1P2 10%

FRU List F356

01B-B2K2 70%
01B-B2D2 10%
01B-A1P2 10%
01B-B2B2
01B-B2C2
01B-B2E2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F357

Storage Card Address Check C: Is set because of an address error in the 16-32M byte range. (Bit 0 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 40%
01B-B2C2 30%
01B-A1P2 20%
01B-B2B2
01B-B2D2
01B-B2E2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F35A or F35C

Storage Card Address Check G: Is set because of an address error in the 0-16M byte range. (Bit 1 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F35A

01B-B2K2 40%
01B-B2G2 30%
01B-A1P2 20%

FRU List F35C

01B-B2K2 40%
01B-B2G2 30%
01B-A1P2 20%
01B-B2F2
01B-B2H2
01B-B2J2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F35D

Storage Card Address Check H: Is set because of an address error in the 16-32M byte range. (Bit 1 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 70%
01B-B2H2 10%
01B-A1P2 10%
01B-B2F2
01B-B2G2
01B-B2J2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F35E

Storage Card Address Check F: Is set because of an address error in the 16-32M byte range. (Bit 1 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 70%
01B-B2F2 10%
01B-A1P2 10%
01B-B2G2
01B-B2H2
01B-B2J2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F35F

Storage Card Address Check J: Is set because of an address error in the 16-32M byte range. (Bit 1 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2K2 70%
01B-B2J2 10%
01B-A1P2 10%
01B-B2F2 10%
01B-B2G2
01B-B2H2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F364 or F366

Storage Card Address Check P: Is set because of an address error in the 0-16M byte range. (Bit 2 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F364

01B-B2L2 70%
01B-B2P2 10%
01B-A1P2 10%

FRU List F366

01B-B2L2 70%
01B-B2P2 10%
01B-A1P2 10%
01B-B2M2
01B-B2N2
01B-B2Q2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F367

Storage Card Address Check N: Is set because of an address error in the 16-32M byte range. (Bit 2 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2N2 10%
01B-A1P2 10%
01B-B2M2
01B-B2P2
01B-B2Q2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F368

Storage Card Address Check Q: Is set because of an address error in the 16-32M byte range. (Bit 2 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2Q2 10%
01B-A1P2 10%
01B-B2M2
01B-B2N2
01B-B2P2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F369

Storage Card Address Check M: Is set because of an address error in the 16-32M byte range. (Bit 2 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2M2 10%
01B-A1P2 10%
01B-B2N2
01B-B2P2
01B-B2Q2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F36A or F36C

Storage Card Address Check S: Is set because of an address error in the 0-16M byte range. (Bit 3 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List F36A

01B-B2L2 70%
01B-B2S2 10%
01B-A1P2 10%

FRU List F36C

01B-B2L2 70%
01B-B2S2 10%
01B-A1P2 10%
01B-B2R2
01B-B2T2
01B-B2U2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F36D

Storage Card Address Check T: Is set because of an address error in the 16-32M byte range. (Bit 3 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2T2 10%
01B-A1P2 10%
01B-B2R2
01B-B2S2
01B-B2U2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F36E

Storage Card Address Check R: Is set because of an address error in the 16-32M byte range. (Bit 3 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2R2 10%
01B-A1P2 10%
01B-B2S2
01B-B2T2
01B-B2U2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F36F

Storage Card Address Check U: Is set because of an address error in the 16-32M byte range. (Bit 3 of the USCACK/LSCACK register were active). These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1P2

FRU List

01B-B2L2 70%
01B-B2U2 10%
01B-A1P2 10%
01B-B2R2
01B-B2S2
01B-B2T2

Diagnostic Checks

Refer to Diagnostic Check 4 on page STOR 200.

SC F400 (SD 1) or SC F480 (SD 2)

Upper Port Check: Is set because of an Upper Port Check indicator with none of the expected error indicators active on a store operation. (Bit 0 of the CSTAT1 register is active).

Card detecting the error:

01B-A1R2 Port 1
01B-A1S2 Port 2

FRU List

Port 1	**Port 2**
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 20%
01B-A1P2	01B-A1P2 10%
01B-A1L2	01B-A1L2
01B-A1D2	01B-A1G2
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-B1A5

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F401 (SD 1) or SC F481 (SD 2)

Upper Port SRC Check: Is set because of an Upper Port SRC Check indicator is active on a store operation. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	**Port 2**
01A-B4N2	01A-B3N2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F402 (SD 1) or SC F482 (SD 2)

Upper Port ECC - PB Data In Check 1: Is set because of a parity error on the Port Buffer Data In bus on a store. (Bit 6 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	**Port 2**
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F403 (SD 1) or SC F483 (SD 2)

Upper Port ECC PB Data In Check 2: Is set because of a parity error on the Port Buffer Data In bus on a store. (Bit 7 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F404 (SD 1) or SC F484 (SD 2)

Upper Port DXR PA Overrun/Underrun Check: Is set because of an overrun or an underrun between the port adapter and the DXR bus. (Bit 2 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 80%
01A-B4N2	01A-B3N2 10%
01A-B4M2	01A-B3M2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F405 (SD 1) or SC F485 (SD 2)

Upper Port DXR PA Parity Check: Is set because of a parity error on the buffer registers between the DXR Bus and the CMCD card. (Bit 0 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 90%
01A-B4M2	01A-B3M2
01A-B4K2	01A-B3K2
01A-B4H2	01A-B3H2
01A-B4X2	01A-B3X2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F406 (SD 1) or SC F486 (SD 2)

Upper Port PA PB Data In/Out Parity Check: Is set because of a parity error on the CMCD card on a store (Bit 6 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 80%
01B-A1R2	01B-A1S2 10%
01B-A1D2	01B-A1G2 10%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F407 (SD 1) or SC F487 (SD 2)

Upper Port Buffer Parity Check: Is set because of a parity error, on the upper port buffer, on a store operation.

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 60%
01A-B4N2	01A-B3N2 40%
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F408 (SD 1) or SC F488 (SD 2)

Upper Port PA PB Overrun Check: Is set because of an overrun on a port adapter to port buffer data transfer on a store. (Bit 5 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 50%
01B-A1R2	01B-A1S2 20%
01A-B4N2	01A-B3N2 20%
01A-B4M2	01A-B3M2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F409 (SD 1) or SC F489 (SD 2)

Upper Port Byte Counter Check: Is set because of a byte counter error on a store. (Bit 3 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F40A (SD 1) or SC F48A (SD 2)

Upper Port Byte Counter Shadow Check: Is set because of a byte counter shadow parity error on a store. (Bit 4 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F40B (SD 1) or SC F48B (SD 2)

Upper Port Byte Count Zero Check: Is set because of a byte count zero controls error on a store. (Bit 1 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1Q2 30%	01B-A1G2 90%
01B-A1D2 30%	01B-A1Q2 10%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F40C (SD 1) or SC F48C (SD 2)

Upper Port Buffer Overrun/Underrun: Is set because of a port buffer Overrun or Underrun on a store. (Bit 0 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 80%
01B-A1Q2	01B-A1Q2 10%
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F420 (SD 1) or SC F4A0 (SD 2)

Upper Port Check: Is set because of an upper Port check on a fetch with no other error bits on.

Card detecting the error:

01B-A1R2 Port 1
01B-A1S2 Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 20%
01B-A1P2	01B-A1P2 10%
01B-A1L2	01B-A1L2
01B-A1D2	01B-A1G2
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F421 (SD 1) or SC F4A1 (SD 2)

Upper Port PA - PB Overrun: Is set because of a PA PB Overrun on a fetch. (Bit 5 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 90%
01A-B4M2	01A-B3M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F422 (SD 1) or SC F4A2 (SD 2)

Upper Port PA - PB Data In Parity Check: Is set because of a PA PB parity error on a fetch. (Bit 5 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F424 (SD 1) or SC F4A4 (SD 2)

Upper Port Byte Counter Check: Is set because of a byte counter error on a fetch. (Bit 3 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F425 (SD 1) or SC F4A5 (SD 2)

Upper Port Byte Counter Shadow Check: Is set because of a byte counter shadow error on a fetch. (Bit 4 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F426 (SD 1) or SC F4A6 (SD 2)

Upper Port Byte Count Zero Check: Is set because of a byte count zero controls error on a fetch. (Bit 1 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F427 (SD 1) or SC F4A7 (SD 2)

Upper Port ECC - PA Data In Parity Check 1: Is set because of a ECC PA data in parity error on a fetch. (Bits 6 and 7 of the UPBCK register are active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

01B-A1J2 50%
01B-A1K2 50%
01B-A1L2
01B-A1Q2
01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F428 (SD 1) or SC F4A8 (SD 2)

Upper Port ECC - PB Data In Parity Check 1: Is set because of an ECC PB parity error on a fetch. (Bit 6 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 70%
01B-A1K2	01B-A1K2 10%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1H2
01B-A1G2	01B-A1D2
01B-A1E2	01B-A1E2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F429 (SD 1) or SC F4A9 (SD 2)

Upper Port ECC - PB Data In Parity Check 2: Is set because of an ECC - PB parity error on a fetch. (Bit 7 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 70%
01B-A1K2	01B-A1K2 10%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1H2
01B-A1G2	01B-A1D2
01B-A1E2	01B-A1E2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F42A (SD 1) or SC F4AA (SD 2)

Upper Port PA - PB Data In Parity Check: Is set because of a PA - PB parity error on a fetch. (Bit 6 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 90%
01A-B4N2	01A-B3N2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F42B (SD 1) or SC F4AB (SD 2)

Upper Port DXR - PA Parity Check: Is set because of a DXR - PA parity error on a fetch. (Bit 0 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 90%
01A-B4N2	01A-B3N2
01A-B4M2	01A-B3M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F42C (SD 1) or SC F4AC (SD 2)

Upper Port PB Overrun/Underrun Check: Is set because of a port buffer overrun/underrun error on a fetch. (Bit 0 of the UPBCK register is active).

Card detecting the error:

01B-A1D2 Port 1
01B-A1G2 Port 2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 90%
01A-B4N2	01A-B3N2
01B-A1Q2	01B-A1Q2
01B-A1R2	01B-A1S2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F42D (SD 1) or SC F4AD (SD 2)

Upper Port DXR - PA Overrun/Underrun Check: Is set because of a DXR - PA overrun/underrun error on a fetch. (Bit 2 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 90%
01A-B4N2	01A-B3N2
01A-B4M2	01A-B3M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F42E (SD 1) or SC F4AE (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from an unknown storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F42F (SD 1) or SC F4AF (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 0-3M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01B-A1J2
01B-B2D2	01B-B2D2
01B-B2G2	01B-B2G2
01B-B2P2	01B-B2P2
01B-B2S2	01B-B2S2
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F430 (SD 1) or SC F4B0 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 4-7M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2B2	01B-B2B2
01B-B2J2	01B-B2J2
01B-B2M2	01B-B2M2
01B-B2U2	01B-B2U2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F431 (SD 1) or SC F4B1 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 8-11M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2E2	01B-B2E2
01B-B2F2	01B-B2F2
01B-B2Q2	01B-B2Q2
01B-B2R2	01B-B2R2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F432 (SD 1) or SC F4B2 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 12-15M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2C2	01B-B2C2
01B-B2H2	01B-B2H2
01B-B2N2	01B-B2N2
01B-B2T2	01B-B2T2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

Symptom Codes

SC F433 (SD 1) or SC F4B3 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 16-19M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2D2	01B-A2D2
01B-A2G2	01B-A2G2
01B-A2P2	01B-A2P2
01B-A2S2	01B-A2S2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F434 (SD 1) or SC F4B4 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 20-23M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2B2	01B-A2B2
01B-A2J2	01B-A2J2
01B-A2M2	01B-A2M2
01B-A2U2	01B-A2U2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F435 (SD 1) or SC F4B5 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 24-27M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2E2	01B-A2E2
01B-A2F2	01B-A2F2
01B-A2Q2	01B-A2Q2
01B-A2R2	01B-A2R2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F436 (SD 1) or SC F4B6 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 28-31M byte storage partition. (Bit 1 of the UPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2C2	01B-A2C2
01B-A2H2	01B-A2H2
01B-A2N2	01B-A2N2
01B-A2T2	01B-A2T2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F440 (SD 1) or SC F4C0 (SD 2)

Lower Port Check: Is set because of lower port check is set with no supporting error bits.

Card detecting the error:

01B-A1R2 Port 1
01B-A1S2 Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 20%
01B-A1P2	01B-A1P2 10%
01B-A1L2	01B-A1L2
01B-A1E2	01B-A1H2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F441 (SD 1) or SC F4C1 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a store operation. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F442 (SD 1) or SC F4C2 (SD 2)

Lower Port ECC - PB Data In Parity Check 1: Is set because of a parity error on a store. (Bit 6 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F443 (SD 1) or SC F4C3 (SD 2)

Lower Port ECC - PB Data In Parity Check 2: Is set because of a parity latch error on a store. (Bit 7 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F444 (SD 1) or SC F4C4 (SD 2)

Lower Port DXR - PA Overrun/Underrun: Is set because of an overrun/underrun on a store. (Bit 2 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 80%
01A-B4N2	01A-B3N2 10%
01A-B4M2	01A-B3M2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F445 (SD 1) or SC F4C5 (SD 2)

Lower Port DXR - PA Parity Check: Is set because of a DXR - PA parity error on a store. (Bit 0 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 90%
01A-B4M2	01A-B3M2
01A-B4K2	01A-B3K2
01A-B4H2	01A-B3H2
01A-B4X2	01A-B3X2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F446 (SD 1) or SC F4C6 (SD 2)

Lower Port PA - PB Data In/Out Parity Check: Is set because of a PA - PB Data In/Out parity error on a store. (Bit 6 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 80%
01B-A1R2	01B-A1S2 10%
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F447 (SD 1) or SC F4C7 (SD 2)

Lower Port PA - PB Data In Parity Check: Is set because of a PA - PB Data In parity error on a store. (Bit 5 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 50%
01B-A1E2	01B-A1H2 40%
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F448 (SD 1) or SC F4C8 (SD 2)

Lower Port PA - PB Overrun Error: Is set because of a PA - PB Data overrun error on a store. (Bit 5 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 50%
01B-A1R2	01B-A1S2 20%
01A-B4N2	01A-B3N2 20%
01A-B4M2	01A-B3M2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F449 (SD 1) or SC F4C9 (SD 2)

Lower Port Byte Counter Error: Is set because of a Byte Counter error on a store. (Bit 3 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F44A (SD 1) or SC F4CA (SD 2)

Lower Port Byte Count Zero Error: Is set because of a Byte Count Shadow register error on a store. (Bit 4 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F44B (SD 1) or SC F4CB (SD 2)

Lower Port Byte Count Zero Error: Is set because of a Byte Count Zero control check on a store. (Bit 1 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1Q2	01B-A1Q2 70%
01B-A1E2	01B-A1H2 30%

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F44C (SD 1) or SC F4CC (SD 2)

Lower Port Buffer Overrun/Underrun: Is set because of a port buffer overrun/underrun on a store. (Bit 0 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 90%
01B-A1Q2	01B-A1Q2
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F460 (SD 1) or SC F4E0 (SD 2)

Lower Port Check: Is set because of a lower port check error with no supporting error indicators. (Bit 1 of the CSTAT1 register is active).

Card detecting the error:

01B-A1R2 Port 1
01B-A1S2 Port 2

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 60%
01A-B4N2	01A-B3N2 20%
01B-A1P2	01B-A1P2 10%
01B-A1L2	01B-A1L2
01B-A1E2	01B-A1H2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F461 (SD 1) or SC F4E1 (SD 2)

Lower Port PA - PB Overrun: Is set because of a PA - PB overrun error. (Bit 5 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 90%
01A-B4M2	01A-B3M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F462 (SD 1) or SC F4E2 (SD 2)

Lower Port PA - PB Data In Parity error: Is set because of a PA-PB Data In parity error. (Bit 5 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F464 (SD 1) or SC F4E4 (SD 2)

Lower Port Byte Counter Error: Is set because of a byte counter error on a fetch. (Bit 3 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F465 (SD 1) or SC F4E5 (SD 2)

Lower Port Byte Counter Shadow Check: Is set because of a byte counter shadow error on a fetch. (Bit 4 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F466 (SD 1) or SC F4E6 (SD 2)

Lower Port Byte Count Zero Check: Is set because of a byte count zero controls error on a fetch. (Bit 1 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F467 (SD 1) or SC F4E7 (SD 2)

Lower Port ECC - PA Data In Parity Check 1: Is set because of a ECC - PA data in parity error on a fetch. (Bits 6 and 7 of the LPBCK register are active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1J2	01B-A1J2 50%
01B-A1K2	01B-A1K2 50%
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2
01B-A1 ZJKL TCC	01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F468 (SD 1) or SC F4E8 (SD 2)

Lower Port ECC - PB Data In Parity Check 1: Is set because of an ECC - PB parity error on a fetch. (Bit 6 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 70%
01B-A1K2	01B-A1K2 10%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1D2
01B-A1D2	01B-A1G2
01B-A1G2	01B-A1E2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F469 (SD 1) or SC F4E9 (SD 2)

Lower Port ECC - PB Data In Parity Check 2: Is set because of an ECC - PB parity error on a fetch. (Bit 7 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 70%
01B-A1K2	01B-A1K2 10%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1D2
01B-A1D2	01B-A1G2
01B-A1G2	01B-A1E2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F46A (SD 1) or SC F4EA (SD 2)

Lower Port PA - PB Data In Parity Check: Is set because of a PA - PB parity error on a fetch. (Bit 6 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 90%
01A-B4N2	01A-B3N2
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F46B (SD 1) or SC F4EB (SD 2)

Lower Port DXR - PA Parity Check: Is set because of a DXR - PA parity error on a fetch. (Bit 0 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 90%
01A-B4M2	01A-B3M2
01A-B4K2	01A-B3K2
01A-B4H2	01A-B3H2
01A-B4X2	01A-B3X2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F46C (SD 1) or SC F4EC (SD 2)

Lower Port PB Overrun/Underrun Check: Is set because of a port buffer overrun/underrun error on a fetch. (Bit 0 of the LPBCK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 90%
01A-B4N2	01A-B3N2
01A-B1Q2	01A-B1Q2
01B-A1R2	01B-A1S2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F46D (SD 1) or SC F4ED (SD 2)

Lower Port DXR - PA Overrun/Underrun Check: Is set because of a DXR - PA overrun/underrun error on a fetch. (Bit 2 of the LPACK register is active).

Card detecting the error:

01B-A1E2 Port 1
01B-A1H2 Port 2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 90%
01A-B4N2	01A-B3N2
01A-B4M2	01A-B3M2

Diagnostic Checks

Refer to Diagnostic Check 1 on page STOR 200.

SC F46E (SD 1) or SC F4EE (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from an unknown storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F46F (SD 1) or SC F4EF (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 0-3M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2D2	01B-B2D2
01B-B2G2	01B-B2G2
01B-B2P2	01B-B2P2
01B-B2S2	01B-B2S2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F470 (SD 1) or SC F4F0 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 4-7M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2B2	01B-B2B2
01B-B2J2	01B-B2J2
01B-B2M2	01B-B2M2
01B-B2U2	01B-B2U2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F471 (SD 1) or SC F4F1 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 8-11M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2E2	01B-B2E2
01B-B2F2	01B-B2F2
01B-B2Q2	01B-B2Q2
01B-B2R2	01B-B2R2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F472 (SD 1) or SC F4F2 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 12-15M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2C2	01B-B2C2
01B-B2H2	01B-B2H2
01B-B2N2	01B-B2N2
01B-B2T2	01B-B2T2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F473 (SD 1) or SC F4F3 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 16-19M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2D2	01B-A2D2
01B-A2G2	01B-A2G2
01B-A2P2	01B-A2P2
01B-A2S2	01B-A2S2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F474 (SD 1) or SC F4F4 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 20-23M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2B2	01B-A2B2
01B-A2J2	01B-A2J2
01B-A2M2	01B-A2M2
01B-A2U2	01B-A2U2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F475 (SD 1) or SC F4F5 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 24-27M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2E2	01B-A2E2
01B-A2F2	01B-A2F2
01B-A2Q2	01B-A2Q2
01B-A2R2	01B-A2R2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F476 (SD 1) or SC F4F6 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 28-31M byte storage partition. (Bit 1 of the LPACK register is active).

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-A2C2	01B-A2C2
01B-A2H2	01B-A2H2
01B-A2N2	01B-A2N2
01B-A2T2	01B-A2T2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A2A2	01B-A2A2
01B-A2K2	01B-A2K2
01B-A2L2	01B-A2L2
01B-A2V2	01B-A2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F4F7 (SD 1) or SC F51F (SD 2)

Incorrect Sense Build: Is set because the microcode recognized an incorrect operation type during sense build.

FRU List

None

Diagnostic Check

None

SC F500

SD 1/SD 2 ECC Uncorrectable Error: Is set because of an ECC error indicator being on. (Bit 0 of the UECCCK/LECCCK Register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1Q2 90%
01B-A1L2 10%

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F501

SD 1/SD 2 ECC ROS-M Check: Is set because of an ECC ROM-M error indication on a store. (Bit 5 of the UECCCK/LECCCK Register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F502

SD 1/SD 2 Port Buffer - ECC Data In Check 1: Is set because of a PB - ECC Data In check (Clock error on the CME3 card). (Bits 1 and 2 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2 50%
01B-A1Q2 10%
01B-A1E2
01B-A1H2
01B-A1D2
01B-A1G2
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F503 (SD 1) or SC F583 (SD 2)

SD 1/SD 2 Upper Port and PB - ECC Data In Check 1: Is set because of an upper PB - ECC Data In check 1 (Bit 0 of the CSTAT1 register and bit 1 of the UECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 80%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1H2
01B-A1G2	01B-A1D2
01B-A1E2	01B-A1E2
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F504 (SD 1) or SC F584 (SD 2)

SD 1/SD 2 Lower Port and PB - ECC Data In Check 1: Is set because of a lower PB - ECC Data In check 1 (Bit 1 of the CSTAT1 register and bit 1 of the LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 80%
01B-A1J2	01B-A1J2 10%
01B-A1H2	01B-A1D2
01B-A1D2	01B-A1G2
01B-A1G2	01B-A1E2
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F505 (SD 1) or SC F585 (SD 2)

SD 1/SD 2 Upper Port and PB - ECC Data In Check 2: Is set because of an Upper PB - ECC Data In check 2 (Bit 0 of the CSTAT1 register and bit 2 of the UECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 80%
01B-A1K2	01B-A1K2 10%
01B-A1H2	01B-A1H2
01B-A1G2	01B-A1D2
01B-A1E2	01B-A1E2
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F506 (SD 1) or SC F586 (SD 2)

SD 1/SD 2 Lower Port and PB - ECC Data In Check 2: Is set because of a Lower PB - ECC Data In check 2 (Bit 1 of the CSTAT1 register and bit 2 of the LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 80%
01B-A1K2	01B-A1K2 10%
01B-A1H2	01B-A1D2
01B-A1D2	01B-A1G2
01B-A1G2	01B-A1E2
01B-A1L2	01B-A1L2
01B-A1Q2	01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F507

SD 1/SD 2 ECC Data In or ROS Check E1: Is set because of an ECC parity check. (Bit 3 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1J2 90%
01B-A1L2
01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F508

SD 1/SD 2 ECC Data In or ROS Check E2: Is set because of an ECC parity check. (Bit 4 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1K2 90%
01B-A1L2
01B-A1Q2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F509

SD 1/SD 2 E2/DD - Storage Data Out Parity Check: Is set because of an error in the board select circuits on the CMDA/CLDA card. (Bits 6 and 7 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1T2 80%
01B-A1L2 10%
01B-A1Q2
01B-A1K2
01B-A1J2
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50A

SD 1/SD 2 E1/DD - Storage Data Out Parity Check: Is set because of a parity error on data bits 0-35. (Bit 6 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1M2 50%
01B-B2A2 40%
01B-A1J2
01B-A1L2
01B-A1K2
01B-B2V2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50B

SD 1/SD 2 E2/DD - Storage Data Out Parity Check: Is set because of a parity error on data bits 36-71. (Bit 7 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1N2 50%
01B-B2V2 40%
01B-A1K2
01B-A1L2
01B-B2A2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50C

SD 1/SD 2 E1/DD - Storage Data Out Parity Check: Is set because of a parity indicator on a fetch. (Bit 6 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2 90%
01B-A1M2
01B-A1K2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50D

SD 1/SD 2 E2/DD - Storage Data Out Parity Check: Is set because of a parity indicator on a fetch. (Bit 7 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2 90%
01B-A1N2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50E

SD 1/SD 2 PB - ECC Data In Check 1: Is set because of an ECC parity indication. (Bit 1 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2 40%
01B-A1Q2 30%
01B-A1J2 20%
01B-A1K2
01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F50F

SD 1/SD 2 PB - ECC Data In Check 2: Is set because of an ECC parity indication. (Bit 2 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1Q2 40%
01B-A1L2 30%
01B-A1K2 20%
01B-A1J2 10%
01B-A1 ZJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F511

SD 1/SD 2 ECC ROS-M Check: Is set because of an ECC ROS-M check on a fetch. (Bit 5 of the UECCCK/LECCCK register is active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F512

SD 1/SD 2 ECC Data In/ROS Check E1 and ECC Data In/ROS Check 2: Is set because of a ROS module error. (Bits 3 and 4 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1L2 90%
01B-A1 WJKL TCC
01B-A1 XJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F513

SD 1/SD 2 ECC Data In/ROS Check E1: Is set because of a ROS parity error on a fetch. (Bit 3 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1J2 90%
01B-A1L2
01B-A1 WJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F514

SD 1/SD 2 ECC Data In/ROS Check E2: Is set because of a ROS parity error on a fetch. (Bit 4 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

01B-A1K2 90%
01B-A1L2
01B-A1 WJKL TCC

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F515

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is unknown. (Bit 0 of the UECCCK/LECCCK register are active).

Card detecting the error:

01B-A1L2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F516

Storage Control Board Power is Off: (Bit 5 of CSTAT4 is on)

SC F517

Storage Board 1 Power is Off: (Bit 6 of CSTAT4 is on)

SC F518

Storage Board 2 Power is Off: (Bit 7 of CSTAT4 is on)

Card detecting the error:

01B-A1L2

FRU List for SC F516, F517, F518

Port 1	Port 2
01A-B1J2	01A-B1J2 70%
01A-B4M2	01A-B3M2 20%
Cable:	Cable:
01A-B4ZE	01A-B3ZE
to	to
01B-A1A5	01B-A1B5
Cable:	Cable:
01A-B1V5	01A-B1V5
to	to
01B-A1V3	01B-A1V3

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F51E

SD 1/SD 2 Upper/Lower General Check: Is set because of a general check and no supporting indicators.

Card detecting the error:

None - Microcode detected

FRU List

Port 1	Port 2
01A-B4N2	01A-B3N2 60%
01B-A1L2	01B-A1L2 30%
01B-A1R2	01B-A1S2
01B-A1D2	01B-A1G2
01B-A1P2	01B-A1P2
01A-A1E2	01A-A1H2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F520, F522 (SD 1) or SC F5A0, F5A2 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 0-16M byte storage partition. (Bit 1 of the UPACK register is active). These error codes are only for machines with expanded storage.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2D2	01B-B2D2
01B-B2G2	01B-B2G2
01B-B2P2	01B-B2P2
01B-B2S2	01B-B2S2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F523, F524, F525 (SD 1) or SC F5A3, F5A4, F5A5 (SD 2)

Upper Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 16-32M byte storage partition. (Bit 1 of the UPACK register is active). These error codes are only for machines with expanded storage.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1D2	01B-A1G2 20%
01B-A1E2	01B-A1H2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01A-A1J2
01B-B2C2	01B-B2C2
01B-B2H2	01B-B2H2
01B-B2N2	01B-B2N2
01B-B2T2	01B-B2T2
01A-B4N2	01B-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1N2
01B-A1N2	01B-A1M2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

Symptom Codes

SC F560, F562 (SD 1) or SC F5E0, F5E2 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 0-16M byte storage partition. (Bit 1 of the LPACK register is active). These error codes are only for machines with expanded storage.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01B-A1J2
01B-B2D2	01B-B2D2
01A-B2G2	01A-B2G2
01B-B2P2	01B-B2P2
01B-B2S2	01B-B2S2
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1M2
01B-A1N2	01B-A1N2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F563, F564, F565 (SD 1) or SC F5E3, F5E4, F5E5 (SD 2)

Lower Port Storage Redundancy Check (SRC): Is set because of an SRC error on a fetch from 16-32M byte storage partition. (Bit 1 of the LPACK register is active). These error codes are only for machines with expanded storage.

Card detecting the error:

01A-B4(B3)N2

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 20%
01B-A1D2	01B-A1G2 20%
01B-A1G2	01B-A1E2 10%
01B-A1H2	01B-A1D2 10%
01B-A1T2	01B-A1T2
01B-A1K2	01B-A1K2
01B-A1J2	01B-A1J2
01B-B2C2	01B-B2C2
01A-B2H2	01A-B2H2
01B-B2N2	01B-B2N2
01B-B2T2	01B-B2T2
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2
01B-A1L2	01B-A1L2
01A-B3N2	01A-B4N2
01B-A1M2	01B-A1M2
01B-A1N2	01B-A1N2
01B-B2A2	01B-B2A2
01B-B2K2	01B-B2K2
01B-B2L2	01B-B2L2
01B-B2V2	01B-B2V2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2

Cable: 01B-B2Y4 to 01B-A1Y6
Cable: 01A-B4N5 to 01B-A1A4
Cable: 01A-B3N3 to 01B-A1B3
Cable: 01A-B3N5 to 01B-A1B4
Cable: 01B-B2Y3 to 01B-A1Y5
Cable: 01A-B4N3 to 01B-A1A3
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01A-B2Z5 to 01B-A1Y3
Cable: 01A-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01A-B2Z3 to 01B-A1V2
Cable: 01B-B2Z2 to 01B-A1Y1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F601

SD 1/SD 2 DR Clock Check 1: Is set because of a clock error on a store. The store was to the CMDR - A card on storage board 01B-A2 or B2. (Bit 2 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F602

SD 1/SD 2 DR Clock Check 1: Is set because of a clock error on a store. The store was to the CMDR - A card on storage board 01B-B2. (Bit 2 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2A2 70%	01B-B2A2 70%
01B-A1Q2 10%	01B-A1Q2 10%
01B-B2V2 10%	01B-B2V2 10%
01B-A1P2	01B-A1P2
	01B-A2A2

Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y2 to 01B-A1Y2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F603

SD 1/SD 2 DR Clock Check 1: Is set because of a clock error on a store. The store was to the CMDR - A card on storage board 01B-A2. (Bit 2 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2A2 80%
01B-A2V2 10%
01B-A1Q2 10%
01B-A1P2
01B-B2A2
Cable: 01B-A2Z2 to 01B-A1Z1

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F604

SD 1/SD 2 DR Clock Check 2: Is set because of a clock error on a store. The store was to the CMDR - V card on storage board 01B-A2 or B2. (Bit 3 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F605

SD 1/SD 2 DR Clock Check 2: Is set because of a clock error on a store. The store was to the CMDR - V card on storage board 01B-B2. (Bit 3 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2V2 70%	01B-B2V2 70%
01B-A1Q2 10%	01B-A1Q2 10%
01B-B2A2 10%	01B-B2A2 10%
01B-A1P2	01B-A1P2
	01B-A2A2

Cable: 01B-B2Y5 to 01B-A1Y4
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y2 to 01B-A1Y2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F606

SD 1/SD 2 DR Clock Check 2: Is set because of a clock error on a store. The store was to the CMDR - V card on storage board 01B-A2. (Bit 3 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2V2 70%
01B-A2A2 10%
01B-A1Q2
01B-A1P2
01B-B2V2
Cable: 01B-A2Z5 to 01B-A1Z3

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F607

SD 1/SD 2 DD - DR Data 0-35 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - A on board 01B-B2 or A2. (Bit 0 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F608

SD 1/SD 2 DD - DR Data 0-35 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - A on board 01B-B2. (Bit 0 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2A2 80%
01B-A1M2 10%
01B-B2V2
01B-A1L2
01B-A1P2
01B-B2L2
01B-B2K2
Cable: 01B-A1Y1 to 01B-B2Z2
Cable: 01B-A1Y2 to 01B-B2Y2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F609

SD 1/SD 2 DD - DR Data 0-35 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - A on board 01B-A2. (Bit 0 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2A2 90%
01B-A2V2
01B-A1L2
01B-A1P2
01B-A1M2
01B-B2A2
01B-A2K2
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-A1Z2 to 01B-A2Y2
Cable: 01B-A1Z1 to 01B-A2Z2
Cable: 01B-A1Z3 to 01B-A2Z5
Cable: 01B-A1Z4 to 01B-A2Y5

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F610

SD 1/SD 2 DD - DR Data 36-71 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - V on boards 01B-A2/B2. (Bit 1 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Port 1	Port 2
01B-A1C2	01B-A1F2 40%
01B-A1R2	01B-A1S2 30%
01A-B4M2	01A-B3M2 20%
01B-A1P2	01B-A1P2
01A-B4N2	01A-B3N2
01A-B4L2	01A-B3L2
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F611

SD 1/SD 2 DD - DR Data 36-71 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - V on board 01B-B2. (Bit 1 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-B2V2 90%
01B-A1N2
01B-B2A2
01B-A1L2
01B-A1P2
01B-B2L2
01B-B2K2
Cable: 01B-A1Y4 to 01B-B2Y5
Cable: 01B-A1Y3 to 01B-B2Z5

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F612

SD 1/SD 2 DD - DR Data 36-71 Parity Check: Is set because of a DD - DR data parity error on a store to CMDR - V on board 01B-A2. (Bit 1 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A2V2 90%
01B-A2A2
01B-A1L2
01B-A1P2
01B-B2V2
01B-A1N2
01B-A2L2
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-A1Z1 to 01B-A2Z2
Cable: 01B-A1Z2 to 01B-A2Y2
Cable: 01B-A1Z4 to 01B-A2Y5
Cable: 01B-A1Z3 to 01B-A2Z5

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F613

SD 1/SD 2 DR Clock Check 1: Is set because of a DR clock error on a fetch. (Bit 2 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2A2	01B-B2A2 90%
01B-B2V2	01B-B2V2
01B-A1P2	01B-A2A2
	01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F614

SD 1/SD 2 DR Clock Check 2: Is set because of a DR clock error on a fetch. (Bit 3 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-B2V2	01B-B2V2 90%
01B-A1P2	01B-A2V2
	01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F615

SD 1/SD 2 DD - DR (0-35) Data Check: Is set because of a DD - DR parity error on a fetch. (Bit 0 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-A1P2	01B-A1P2 60%
01B-B2A2	01B-B2A2 40%
	01B-A2A2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F616

SD 1/SD 2 DD - DR (36-71) Data Check: Is set because of a DD - DR parity error on a fetch. (Bit 1 of the USCCK/LSCCK register is active).

Card detecting the error:

01B-A1P2

FRU List

Expanded Storage	Without Expanded Storage
01B-A1P2	01B-A1P2 60%
01B-B2V2	01B-B2V2 40%
	01B-A2V2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F701 (SD 1) or SC F781 (SD 2)

Port Adapter-Control Cable Out: Is set because of a port adapter to subsystem storage control board cable not seated. (01A-B4(B3) to 01B-A1) (Bit 5 of the CSTAT3 register is active).

Card detecting the error:

01A-B3(B4)M2

FRU List

Port 1	Port 2
01A-B4M2	01A-B3M2 90%
Cable:	Cable:
01A-B4M3	01A-B3M3
to	to
01B-A1A2	01B-A1B2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4
Cable:	Cable:
01A-B4ZE	01A-B3ZE
Dto	to
01B-A1A5	01B-A1B5

Diagnostic Checks

Refer to SC F701 Cable Check or SC F781 Cable Check on page STOR 300.

SC F702

SD 1/SD 2 Communication Cable out: Is set because of the communications cable between SD 1 and SD 2 CMCA card is not seated. (Bit 6 of the CSTAT3 register is active).

Card detecting the error:

01A-B3(B4)M2

FRU List

01A-B3M2 50%
01A-B4M2 50%
Cable: 01B-B3YL to 01B-B4YL
Cable: 01B-B3YM to 01B-B4YM

Diagnostic Checks

Refer to SC F702 Cable Check on page STOR 305.

SC F703

SD 1/SD 2 Storage Board 1 Cable Out: Is set when a cable to storage board 1 is not seated. (01B-A1 to 01B-B2) (Bit 0 of the GSSCIN register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2 90%
Cable: 01B-A1Y1 to 01B-B2Z2
Cable: 01B-A1Y2 to 01B-B2Y2
Cable: 01B-A1Y3 to 01B-B2Z5
Cable: 01B-A1Y4 to 01B-B2Y5
Cable: 01B-A1Y5 to 01B-B2Y3
Cable: 01B-A1Y6 to 01B-B2Y4
Cable: 01B-A1V2 to 01B-B2Z3

Diagnostic Checks

Refer to SC F703 Cable Check on page STOR 305.

SC F704

SD 1/SD 2 Storage Board 2 Cable Out: Is set when a cable to storage board 2 is not seated. (01B-A1 to 01B-A2) (Bit 1 of the GSSCIN register is active).

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2 90%
Cable: 01B-A1Z1 to 01B-A2Z2
Cable: 01B-A1Z2 to 01B-A2Y2
Cable: 01B-A1Z3 to 01B-A2Z5
Cable: 01B-A1Z4 to 01B-A2Y5
Cable: 01B-A1Z5 to 01B-A2Y3
Cable: 01B-A1Z6 to 01B-A2Y4
Cable: 01B-A1V5 to 01B-A2Z3

Diagnostic Checks

Refer to SC F704 Cable Check on page STOR 305.

SC F800 (SD 1) or SC F880 (SD 2)

Invalid Storage Size: Is set because the GSSCIN register indicates an invalid storage size.

Card detecting the error:

01B-A1P2

FRU List

01B-A1P2

Diagnostic Checks

Refer to Diagnostic Check 2 on page STOR 200.

SC F801 (SD 1) or SC F881 (SD 2)

Microcode timeout - Test and Set: Is set because a hardware error occurred causing a microcode timeout waiting for Test and Set Obtained.

Card detecting the error:

None - Microcode detected

FRU List

Port 1	Port 2
01B-A1P2	01B-A1P2 80%
01B-A1R2	01B-A1S2 10%
01A-B4M2	01A-B3M2
01A-B3M2	01A-B4M2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F802 (SD 1) or SC F882 (SD 2)

Microcode timeout - Communications Failure: Is set because a communications hardware error occurred.

Card detecting the error:

None - Microcode detected

FRU List

01A-B3M2 50%
01A-B4M2 40%
01A-B4N2
01A-B3N2

Cable: 01B-B3YM to 01B-B4YM
Cable: 01B-B3YL to 01B-B4YL

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F803 (SD 1) or SC F883 (SD 2)

Microcode timeout: Is set because a timeout waiting for OP complete.

Card detecting the error:

None - Microcode detected

FRU List

Port 1	Port 2
01B-A1E2	01B-A1H2 40%
01B-A1D2	01B-A1G2 40%
01A-B4N2	01A-B3N2
01B-A1R2	01B-A1S2
01B-A1Q2	01B-A1Q2
01B-A1P2	01B-A1P2
01A-B4M2	01A-B3M2
01A-B3M2	01A-B4M2
Cable:	Cable:
01A-B4N3	01A-B3N3
to	to
01B-A1A3	01B-A1B3
Cable:	Cable:
01A-B4N5	01A-B3N5
to	to
01B-A1A4	01B-A1B4

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F804 (SD 1) or SC F884 (SD 2)

Microcode timeout - ASDM Operation: Is set because of an error in the ASDM operation.

Card detecting the error:

None - Microcode detected

FRU List

Port 1	Port 2
01A-B4L2	01A-B3L2

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F805 (SD 1) or SC F885 (SD 2)

Op Complete Check: Is set because op complete is active before the storage cycle starts.

Card detecting the error:

None - Microcode detected

FRU List

Port 1	Port 2
01B-A1R2	01B-A1S2 10%

Diagnostic Checks

Refer to Diagnostic Check 5 on page STOR 200.

SC F900

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 0-3M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-B2D2 20%
01B-B2G2 20%
01B-B2P2 20%
01B-B2S2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1M2
01B-A1N2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2B2
01B-B2C2
01B-B2E2
01B-B2F2
01B-B2H2
01B-B2J2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-B2R2
01B-B2T2
01B-B2U2
Cable: 01B-A1Y2 to 01B-B2Y2
Cable: 01B-A1Y1 to 01B-B2Z2
Cable: 01B-A1Y3 to 01B-B2Z5
Cable: 01B-A1Y4 to 01B-B2Y5
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-A1V2 to 01B-B2Z3

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F901

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 4-7M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-B2B2 20%
01B-B2J2 20%
01B-B2M2 20%
01B-B2U2 20%
Same as F900 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F902

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 8-11M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-B2E2 20%
01B-B2F2 20%
01B-B2Q2 20%
01B-B2R2 20%
Same as F900 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F903

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 12-15M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-B2C2 20%
01B-B2H2 20%
01B-B2N2 20%
01B-B2T2 20%
Same as F900 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F904

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 16-19M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-A2D2 20%
01B-A2G2 20%
01B-A2P2 20%
01B-A2S2 20%
01B-A1L2
01B-A2A2
01B-A2V2
01B-A1K2
01B-A1J2
01B-A1M2
01B-A1N2
01B-A1Q2
01B-A2K2
01B-A2L2
01B-A1P2
01B-A2B2
01B-A2C2
01B-A2E2
01B-A2F2
01B-A2H2
01B-A2J2
01B-A2M2
01B-A2N2
01B-A2Q2
01B-A2R2
01B-A2T2
01B-A2U2
Cable: 01B-A1Y2 to 01B-B2Y2
Cable: 01B-A1Y1 to 01B-B2Z2
Cable: 01B-A1Y3 to 01B-B2Z5
Cable: 01B-A1Y4 to 01B-B2Y5
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-A1V2 to 01B-B2Z3

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F905

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 20-23M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-A2B2 20%
01B-A2J2 20%
01B-A2M2 20%
01B-A2U2 20%
Same as F904 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F906

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 24-27M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-A2E2 20%
01B-A2F2 20%
01B-A2Q2 20%
01B-A2R2 20%
Same as F904 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F907

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 28-31M byte.

Card detecting the error:

01B-A1L2

FRU List

01B-A2C2 20%
01B-A2H2 20%
01B-A2N2 20%
01B-A2T2 20%
Same as F904 except the listed CMSH cards

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F908 or F90A

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 0-15M byte. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1L2

FRU List F908

01B-B2D2 20%
01B-B2G2 20%
01B-B2P2 20%
01B-B2S2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1M2
01B-A1N2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2B2
01B-B2C2
01B-B2E2
01B-B2F2
01B-B2H2
01B-B2J2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-B2R2
01B-B2T2
01B-B2U2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-B2Z3 to 01B-A1V2

FRU List F90A

01B-B2D2 20%
01B-B2G2 20%
01B-B2P2 20%
01B-B2S2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1N2
01B-A1M2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2B2
01B-B2C2
01B-B2E2
01B-B2F2
01B-B2H2
01B-B2J2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-B2R2
01B-B2T2
01B-B2U2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-B2Z3 to 01B-A1V2

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F90B

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 16-31M byte. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1L2

FRU List

01B-B2C2 20%
01B-B2H2 20%
01B-B2N2 20%
01B-B2T2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1N2
01B-A1M2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2B2
01B-B2D2
01B-B2E2
01B-B2F2
01B-B2G2
01B-B2J2
01B-B2M2
01B-B2P2
01B-B2Q2
01B-B2R2
01B-B2S2
01B-B2U2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-B2Z3 to 01B-A1V2

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F90C

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 32-48M byte. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1L2

FRU List

01B-B2E2 20%
01B-B2F2 20%
01B-B2Q2 20%
01B-B2R2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1N2
01B-A1M2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2B2
01B-B2C2
01B-B2D2
01B-B2G2
01B-B2H2
01B-B2J2
01B-B2M2
01B-B2N2
01B-B2P2
01B-B2S2
01B-B2T2
01B-B2U2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-B2Z3 to 01B-A1V2

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F90D

SD 1/SD 2 ECC Uncorrectable Data Error: Is set because of a triple bit data error on fetch. Storage partition is 48-64M byte. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1L2

FRU List

01B-B2B2 20%
01B-B2J2 20%
01B-B2M2 20%
01B-B2U2 20%
01B-A1L2
01B-B2A2
01B-B2V2
01B-A1K2
01B-A1J2
01B-A1N2
01B-A1M2
01B-A1Q2
01B-B2K2
01B-B2L2
01B-A1P2
01B-B2D2
01B-B2C2
01B-B2E2
01B-B2F2
01B-B2H2
01B-B2G2
01B-B2P2
01B-B2N2
01B-B2Q2
01B-B2R2
01B-B2T2
01B-B2S2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC
Cable: 01B-B2Z3 to 01B-A1V2

Diagnostic Checks

Refer to Diagnostic Check 6 on page STOR 200.

SC F980

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card D Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2D2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2C2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F981

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card B Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2B2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2C2
01B-B2D2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F982

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card E Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2E2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2C2
01B-B2D2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F983

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card C Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2C2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2D2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F984

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card D Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2D2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2B2
01B-A2C2
01B-A2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F985

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card B Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2B2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2C2
01B-A2D2
01B-A2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F986

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card E Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2E2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2B2
01B-A2C2
01B-A2D2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F987

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card C Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2C2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2B2
01B-A2D2
01B-A2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F988 or F98A

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card D Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2D2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2C2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F98B

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card C Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2C2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2D2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F98C

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card E Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2E2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2B2
01B-B2C2
01B-B2D2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F98D

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card B Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2B2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2C2
01B-B2D2
01B-B2E2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A0

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card G Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2G2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2H2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A1

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card J Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2J2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2G2
01B-B2H2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A2

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card F Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2F2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2G2
01B-B2H2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A3

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card H Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2H2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2G2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A4

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card G Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2G2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2F2
01B-A2H2
01B-A2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A5

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card J Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2J2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2F2
01B-A2G2
01B-A2H2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A6

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card F Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2F2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2G2
01B-A2H2
01B-A2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A7

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card H Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2H2 80%
01B-A2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-A2K2
01B-A1J2
01B-A1Q2
01B-A2F2
01B-A2G2
01B-A2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9A8 or F9AA

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card G Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2G2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2H2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9AB

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card H Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2H2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2G2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9AC

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card F Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2F2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2G2
01B-B2H2
01B-B2J2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9AD

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card J Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2J2 80%
01B-B2A2 10%
01B-A1L2
01B-A1M2
01B-A1K2
01B-B2K2
01B-A1J2
01B-A1Q2
01B-B2F2
01B-B2G2
01B-B2H2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C0

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card P Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2P2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C1

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card M Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2M2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2N2
01B-B2P2
01B-B2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C2

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card Q Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2Q2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2N2
01B-B2P2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C3

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card N Board 1.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2N2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2P2
01B-B2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C4

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card P Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2P2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2M2
01B-A2N2
01B-A2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C5

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card M Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2M2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2N2
01B-A2P2
01B-A2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C6

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card Q Board 2

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2Q2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2M2
01B-A2N2
01B-A2P2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C7

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card N Board 2

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2N2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2M2
01B-A2P2
01B-A2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9C8 or F9CA

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card P Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2P2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2N2
01B-B2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9CB

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card N Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2N2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2P2
01B-B2Q2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9CC

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card Q Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2Q2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2M2
01B-B2N2
01B-B2P2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9CD

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card M Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2M2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2N2
01B-B2P2
01B-B2Q2
Cable: 01B-B2Y2 to 01B-A1Y2
Cable: 01B-B2Z2 to 01B-A1Y1
Cable: 01B-B2Z5 to 01B-A1Y3
Cable: 01B-B2Y5 to 01B-A1Y4
Cable: 01B-B2Z3 to 01B-A1V2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E0

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card S Board 1

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2S2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2T2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E1

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card U Board 1

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2U2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2S2
01B-B2T2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E2

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card R Board 1

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2R2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2S2
01B-B2T2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E3

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card T Board 1

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2T2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2S2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E4

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card S Board 2

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2S2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2R2
01B-A2T2
01B-A2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E5

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card U Board 2

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2U2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2R2
01B-A2S2
01B-A2T2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E6

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card R Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2R2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2S2
01B-A2T2
01B-A2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E7

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card T Board 2.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-A2T2 80%
01B-A2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-A2L2
01B-A1J2
01B-A1Q2
01B-A2R2
01B-A2S2
01B-A2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9E8 or F9EA

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card S Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2S2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2T2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9EB

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card T Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2T2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2S2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9EC

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card R Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2R2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2S2
01B-B2T2
01B-B2U2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9ED

ECC Uncorrectable Error: Is set because of an ECC uncorrectable error on a fetch. Storage card U Board 1. These error codes are only for machines with expanded storage.

Card detecting the error:

01B-A1J2
01B-A1K2

FRU List

01B-B2U2 80%
01B-B2V2 10%
01B-A1L2
01B-A1N2
01B-A1K2
01B-B2L2
01B-A1J2
01B-A1Q2
01B-B2R2
01B-B2S2
01B-B2T2
01B-A1 WJKL TCC
01B-A1 XJKL TCC
01B-A1 YJKL TCC
01B-A1 ZJKL TCC

Diagnostic Check

Refer to Diagnostic Check 6 on page STOR 200.

SC F9FF

SD1/SD2 Availability Threshold Crossed: Is set because the available storage was reduced across the reporting boundary.

Check the EREP Detail Report for previous failures and enter Start Repair with the new symptom code.

If the problem is not resolved contact the next level of support.

SC FA01

SD1/SD2 Subsystem Storage Unusable: Is set because Subsystem Storage Unusable has been set because of a device error.

1. Check the console log and/or the EREP report for DASD equipment checks.
2. If sense byte 7 = '1X', go to the device maintenance library.
3. If sense byte 1 bit 6=1, check the device.

SC FA02 - SD1/SD2 Subsystem Storage Unusable

SC FA02 is set because of a Port failure.

1. Check the console log and/or the EREP report for sense byte 7 = 'F2'.
2. Enter start repair using the new FSC.
3. If the problem is not resolved contact your next level of support.

SC FA03, FA07, FA0B, FA17

SD1/SD2 Subsystem Storage Unusable: Is set because of a general error, or the subsystem storage unusable following an IML.

Diagnostic Check

1. Check the console log and or the EREP reports for previous subsystem storage equipment checks (Sense byte 7 = 'F2').
2. Enter 'Start Repair' using the new symptom code.
3. If the problem is not resolved, contact your next level of support.

SC FA04

SD1/SD2 Subsystem Storage Unusable: Is set because a Set Subsystem Mode command took the subsystem storage offline.

Diagnostic Check

Notify the operator/system programmer.

SC FA05

SD1/SD2 Subsystem Storage Unusable: Is set because subsystem storage is unusable due to a microcode malfunction.

Diagnostic Check

Check the console log and or EREP reports for the previous error, sense byte 7 = 'F1'. Save the sense data and contact your next level of support.

SC FA06, FA0D, FA13

SD1/SD2 General Storage Failure: Is set because subsystem storage is unusable due to a subsystem storage failure.

Diagnostic Check

Check the console log and or the EREP reports for sense byte 7 = 'F2'. Use the obtained symptom code to begin maintenance.

SC FA08, FB08

SD1/SD2 Subsystem Storage Unusable: Is set because a Diagnostic Mode switch has the subsystem storage offline.

Note: A FB08 error requires initialization.

FRU List

01B-A1P2 50%
S111 Mode Switch 20%
S112 Mode Switch 20%
Cable: S111 and S112 to 01B-A1V4

SC FA09

SD1/SD2 Subsystem Storage Unusable: Is set because of a device format error has the subsystem storage bound.

Diagnostic Check

1. Check the console log and or the EREP reports for DASD invalid track format or no record found error (Sense byte 7 = 'F7').
2. Enter Start repair using the new symptom code.
3. If the problem is not solved contact your next level of support.

SC FA0A, FB0A

SD1/SD2 Storage Director Equipment Checks: Is set because of a storage director equipment check.

Diagnostic Check

Check the console log and or the EREP reports for a storage director failure (sense byte 7 = '2x'). Use the obtained symptom code to begin maintenance.

SC FA0C, FB0C

SD1/SD2 Test and Set Failure: Is set because of a test and set failure.

Diagnostic Check

Check the console log and or the EREP reports for sense byte 7 = 'F2'. Use the obtained symptom code to begin maintenance.

SC FA11

SD1/SD2 Caching Reinitiated: Is set because subsystem storage is entering a limited caching state due to a failure.

Diagnostic Check

Check the console log and or the EREP reports for sense byte 7 = 'F2'. Use the obtained symptom code to begin maintenance.

SC FA12

SD1/SD2 Port Failure: Is set because subsystem storage is unusable due to a subsystem storage port failure.

Diagnostic Check

Check the console log and or the EREP reports for sense byte 7 = 'F2'. Use the obtained symptom code to begin maintenance.

SC FA14

SD1/SD2 Caching Status Mode: Is set because a caching status mode miscompare was detected.

Diagnostic Check

1. Check the console log and or the EREP reports for previous errors, sense byte 7 = X'F8', X'7x', or X'8x'.
2. Enter Start repair using the new symptom code. If sense byte 7 = X'7x' or X'8x' invoke the device checkout.
3. If the problem is not solved contact your next level of support.

SC FA15

SD1/SD2 Microcode Logic Error: Is set because subsystem storage is unusable due to a microcode logic error.

Diagnostic Check

Check the console log and or the EREP reports for a previous microcode error sense byte 7 = 'F1'. Save the sense information and contact your next level of support.

SC FA19

SD1/SD2 Caching Reinitialization: Is set because test and set appears locked by the other SD.

Diagnostic Check

1. Check the console log and or the EREP reports for sense byte 7 = X'F8'.
2. Enter Start repair using the new symptom code.
3. If the problem is not solved contact your next level of support.

SC FA1A

SD1/SD2 Storage Director Equipment Check: Is set because subsystem storage is unusable due to a storage director equipment check.

Diagnostic Check

Check the console log and or the EREP reports for a storage director failure sense byte 7 = '2x'.

SC FB02

SD1/SD2 Initialization Required: Is set because of a subsystem storage port error.

Diagnostic Check

1. Same as steps 1 and 2 on SC FA03
2. If sense byte 7 = 'F2' is not found, run the subsystem storage diagnostics.
3. If the problem is not solved contact your next level of support.

SC FB03

SD1/SD2 Initialization Required: Is set because of a subsystem storage general failure.

Diagnostic Check

Same as FB02.

SC FB04

SD1/SD2 Set Subsystem Storage Mode Command Received: Is set because a storage director received a Set Subsystem Storage Mode Command. Notify the operator.

Diagnostic Check

None

SC FB05

SD1/SD2 Initialization Required: Is set because of a microcode logic error.

Diagnostic Check

1. Check the console log and or the EREP reports for a previous microcode logic error (Sense byte 7 = 'F1').
2. Save the sense information and contact your next level of support.

SC FB06

SD1/SD2 Initialization Required: Is set because of a subsystem selective reset occurred while reset protected.

FRU List

01A-B4(B3)M2

SC FB07

SD1/SD2 Initialization Required: Is set because one SD received a message from the other SD to perform initialization.

Diagnostic Check

Same as FB02.

SC FB0B

Subsystem Storage Initialization Required: Subsystem Storage initialization is required because of an MD command or a machine power up.

SC FB0D

Subsystem Storage Initialization Required: Subsystem Storage initialization is required because a diagnostic force bit is active.

Diagnostic Check

Check the console log or EREP reports for prior system store check, sense byte 7=F2. It the error persists after an IPL execute subsystem storage diagnostics, if not, save the sense and schedule maintenance.

SC FC01

SD1/SD2 Invalid Track Format: Is set because the microcode recognized an invalid track format.

Diagnostic Check

Notify the system programmer, if the problem is not resolved contact your next level of support.

SC FC02

SD1/SD2 No Record Found: Is set because of a no record found condition.

Diagnostic Check

Same as FC01.

SC FD02 (SD 1) or SC FD82 (SD 2)

Communication Failure: Is set because of no response from the other storage director via the DPS array.

Diagnostic Check

1. Check the 3380 data path switches
2. Check the device interface cable
3. Run CTL-I wrap test to the device end on the CTL-I cable
4. If the problem is not resolved, contact your next level of support

SC FD03 (SD 1) or SC FD83 (SD 2)

Communication Failure: Is set because of a DPS array lock timeout.

Diagnostic Check

1. Check the 3380 data path switches
2. Check the device interface cable
3. Run CTL-I wrap test to the device end on the CTL-I cable
4. If the problem is not resolved, contact your next level of support

SC FD06 (SD 1) or SC FD86 (SD 2)

Communication Failure: Is set because of a controller not being available.

Diagnostic Check

1. Check the console log and or the EREP reports for previous DASD equipment checks (sense byte 7 = '7X' or '8x').
2. Invoke the device machine checkout procedure.
3. If the problem is not resolved, contact your next level of support.

SC FD10 (SD 1) or SC FD90 (SD 2)

Communication Timeout: Is set because the other storage director did not respond to a message sent by way of the communications buffer.

Card detecting the error:

None - Microcode detected

FRU List

01A-B3M2 50%
01A-B4M2 50%
Cable: 01B-B3YM to 01B-B4YM

Diagnostic Checks

Refer to Diagnostic Check 3 on page STOR 200

SC FD11 (SD 1) or SC FD91 (SD 2)

Communication Failure: Is set because of the diagnostic mode switch for the other port being set to diagnostic mode position.

Diagnostic Check

Check the subsystem storage mode switches.

SC FEF0

Caching Operation Terminated: Is set because the caching operation terminated.

Check the console log and or the EREP for a previous subsystem error.

Enter Start Repair using the new symptom code.

SC FEFF

SD1/SD2 Microcode Logic Error: Is set because the microcode recognized an invalid sequence.

Diagnostic Check

Save the sense information and contact your next level of support.

SC 000F

Soft Error Logging: Is set because sense data was logged for subsystem storage.

Check the console log and or the EREP for a previous subsystem error.

Enter Start Repair using the new symptom code.

Diagnostic Checks

Diagnostic Check 1

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 50-5C. If error occurs proceed as directed by the MD.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 2

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 57-5F.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 3

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 65-67.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 4

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Loop diagnostic routine 69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 5

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Run diagnostic routines 68-69.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

Diagnostic Check 6

Warning: Make sure that subsystem storage is offline to all storage directors.

If cards are to be removed or replaced in the B gate, subsystem storage must be offline and the attached devices run in direct mode or offline. Power to the subsystem storage can then be turned off.

1. Attach the maintenance device (MD) to the 3880 and select the Start Repair option. Perform the procedures as instructed by the MD.
2. Replace the cards shown on the FRU list that have not previously been replaced.
3. If the failure persists, check the voltages to the cards shown on the FRU list.
4. Loop diagnostic routine 6A.
5. Determine whether the repair has been accomplished. If it has, restore the machine to its normal condition and return it to the customer; otherwise call for assistance.

SC F701 Cable Check

To isolate the failure for FSC F701, probe the points in the following list. If point A is below +0.5 Vdc and point B is above +3.5 Vdc, replace the indicated FRU.

A	B	Failing FRU
01A-B4M2 D08	01A-B4N6 C04	01A-B4 Board
01A-B4N6 C04	01B-A1A5 B08	01A-B4ZE to 01B-A1A5 Cable
01B-A1A5 B08	01A-A1A4 B08	01B-A1 Board
01B-A1A3 B08	01A-A1A2 B08	01B-A1 Board

If the points above did not indicate a FRU, probe the following points and complete the following steps.

C	D
01B-A1A4 B08	01B-A1A3 B08

1. Power down SD1 and subsystem storage.
2. If point C was below +0.5 Vdc and point D was above +3.5 Vdc, disconnect the 01A-B4N5(Z) end of the cable that connects 01A-B4N5(Z) to 01B-A1A4.
   a. Check the cable for continuity from 01A-B4N5(Z) D08 to 01A-B4M2 D08.
      - If the circuit is open, replace the 01A-B4N5 to 01B-A1A4 cable.
      - If the circuit is not open, reseat the cable.
   b. Disconnect the 01A-B4N3(X) end of the 01A-B4N3(X) to 01B-A1A3 cable.
   c. Check the cable for continuity from 01A-B4N3(X) D08 to 01A-B4M2 D08.
      - If the circuit is open, replace the 01A-B4N3(X) to 01B-A1A3 cable.
      - If the circuit is not open, replace the 01A-B4N2 (CMCD) card.
3. If point D was below +0.5 Vdc disconnect the 01A-B4M3 end of the cable that connects 01A-B4M3 to 01B-A1A2.
   a. Check for continuity from 01A-B4M3 D08 on the cable to 01A-B4M2 D08.
      - If the circuit is open, replace the 01A-B4M3 to 01B-A1A2 cable.
      - If the circuit is not open, replace the 01A-B4M2 (CMCA) card.

SC F781 Cable Check

To isolate the failure for FSC F781, probe the points in the following list. If point A is below +0.5 Vdc and point B is above +3.5 Vdc, replace the indicated FRU.

A	B	Failing FRU
01A-B3M2 D08	01A-B3N6 C04	01A-B3 Board
01A-B3N6 C04	01B-A1B5 B08	01A-B3ZE to 01B-A1B5 Cable
01B-A1B5 B08	01A-A1B4 B08	01B-A1 Board
01B-A1B3 B08	01A-A1B2 B08	01B-A1 Board

If the points above did not indicate a FRU, probe the following points and complete the following steps.

C	D
01B-A1B4 B08	01B-A1B3 B08

1. Power down SD1 and subsystem storage.
2. If point C was below +0.5 Vdc and point D was above +3.5 Vdc, disconnect the 01A-B3N5(Z) end of the cable that connects 01A-B3N5(Z) to 01B-A1B4.
   a. Check the cable for continuity from 01A-B3N5(Z) D08 to 01A-B3M2 D08.
      - If the circuit is open, replace the 01A-B3N5(Z) to 01B-A1B4 cable.
      - If the circuit is not open, reseat the cable.
   b. Disconnect the 01A-B3N3(X) end of the 01A-B3N3(X) to 01B-A1B3 cable.
   c. Check the cable for continuity from 01A-B3N3(X) D08 to 01A-B3M2 D08.
      - If the circuit is open, replace the 01A-B3N3(X) to 01B-A1B3 cable.
      - If the circuit is not open, replace the 01A-B3N2 (CMCD) card.
3. If point D was below +0.5 Vdc disconnect the 01A-B3M3 end of the cable that connects 01A-B3M3 to 01B-A1B2.
   a. Check for continuity from 01A-B3M3 D08 on the cable to 01A-B3M2 D08.
      - If the circuit is open, replace the 01A-B3M3 to 01B-A1B2 cable.
      - If the circuit is not open, replace the 01A-B3M2 (CMCA) card.

Cable Checks

SC F702 Cable Check

To isolate the failure for FSC F702, probe the points in the following list. If point A is below +0.5 Vdc and point B is above +3.5 Vdc, replace the indicated FRU.

A	B	Failing FRU
01A-B4M2 D08	01A-B4G1 C13	01A-B4 Board
01A-B4G1 C13	01A-B3G1 C13	01A-B3YL to 01A-B4YL Cable
01A-B3G1 C13	01A-B3H1 D13	01A-B3M2 CMCA
01A-B3H1 D13	01A-B4H1 D13	01A-B3YL to 01A-B4YL Cable
01A-B4H1 D13	01A-B4K1 D13	01A-B4M2 CMCA
01A-B4K1 D13	01A-B3K1 D13	01A-B3YM to 01A-B4YM Cable

If all of the points are above +3.5 Vdc then the failing FRU is the 01A-B3M2 (CMCA) card.

SC F703 Cable Check

To isolate the failure for FSC F703, probe the points in the following list. If point A is below +0.5 Vdc and point B is above +3.5 Vdc, replace the indicated FRU.

A	B	Failing FRU
01B-A1C2 D08	01B-B2R6 A04	01B-B2 Board
01B-B2R6 A04	01B-A1J1 B13	01B-A1Y3 to 01B-B2Z5 Cable
01B-A1J1 B13	01B-A1M1 E13	01B-A1 Board
01B-A1M1 E13	01B-B2R1 A13	01B-A1Y4 to 01B-B2Y5 Cable
01B-B2R1 A13	01B-B2M1 E13	01B-B2 Board
01B-B2M1 E13	01B-A1U1 B13	01B-A1Y6 to 01B-B2Y4 Cable
01B-A1U1 B13	01B-A1R1 A13	01B-A1 Board
01B-A1R1 A13	01B-B2J1 B13	01B-A1Y5 to 01B-B2Y3 Cable
01B-B2J1 B13	01B-B2F1 A13	01B-B2 Board
01B-B2F1 A13	01B-A1F1 A13	01B-A1Y2 to 01B-B2Y2 Cable
01B-A1F1 A13	01B-A1B1 E13	01B-A1 Board
01B-A1B1 E13	01B-B2F6 A04	01B-A1Y1 to 01B-B2Z2 Cable
01B-B2F6 A04	01B-B2J6 B04	01B-B2 Board
01B-B2J6 B04	01B-A1V2 B08	01B-A1V2 to 01B-B2Z3 Cable

If all of points are above +3.5 Vdc, the failing FRU is the 01B-A1P2 (CMC1) card.

SC F704 Cable Check

To isolate the failure for FSC F704, probe the points in the following list. If point A is below +0.5 Vdc and point B is above +3.5 Vdc, replace the FRU indicated.

A	B	Failing FRU
01B-A1C2 D08	01B-A2R6 A04	01B-A2 Board
01B-A2R6 A04	01B-A1J6 B04	01B-A1Z3 to 01B-A2Z5 Cable
01B-A1J6 B04	01B-A1M6 E04	01B-A1 Board
01B-A1M6 E04	01B-A2R1 A13	01B-A1Z4 to 01B-A2Y5 Cable
01B-A2R1 A13	01B-A2M1 E13	01B-A2 Board
01B-A2M1 E13	01B-A1U6 B04	01B-A1Z6 to 01B-A2Y4 Cable
01B-A1U6 B04	01B-A1R6 A04	01B-A1 Board
01B-A1R6 A04	01B-A2J1 B13	01B-A1Z5 to 01B-A2Y3 Cable
01B-A2J1 B13	01B-A2F1 A13	01B-A2 Board
01B-A2F1 A13	01B-A1F6 A04	01B-A1Z2 to 01B-A2Y2 Cable
01B-A1F6 A04	01B-A1B6 E04	01B-A1 Board
01B-A1B6 E04	01B-A2F6 A04	01B-A1Z1 to 01B-A2Z2 Cable
01B-A2F6 A04	01B-A2J6 B04	01B-A2 Board
01B-A2J6 B04	01B-A1V5 B08	01B-A1V5 to 01B-A2Z3 Cable

If all of points are above +3.5 Vdc then the failing FRU is the 01B-A1P2 (CMC1) card.

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Introduction to Diagnostic Tests

Purpose of Diagnostic Descriptions

The diagnostic descriptions are provided to give a description of the activity of a diagnostic test, with the following intent:

- Provide information about the test parameters and error display.
- Provide an understanding of what the diagnostic was doing at the time an error exit is taken.

Each diagnostic description page contains the following information:

- A brief description of the diagnostic test
- The test parameters
- The error display meanings for that test
- The test error stops and meanings

Organization of the DC Sections

The following sections of the manual describe the diagnostic programs for the 3880 that execute within the storage director of the 3880.

The Introduction (INTRO) pages describe how the information is assembled, states the purposes of its various parts, and explains the conventions used within the text.

The Diagnostic Tests pages describe the objectives and the sequence of command executions for each of the routines and tests.

For pages DC RS00 through DC 7Exx, the page numbers correspond to the first test described on that page. The first two digits identify the routine; the last two digits identify the test. For example, page DC HC16 describes the IML Hardcore routine, Test 16; page DC 7804 describes routine 78, Test 04.

Some test routines have a test 00 page, for example DC 7800, which gives a more detailed description of the routine.

Only the routines above routine 50 can be individually selected for execution. These routines are executed from the maintenance device in maintenance mode or in support mode. Refer to the MD diagnostic operating procedures in the MD section of the maintenance support manual (MSM).

- The maintenance mode is the mode where the routines are automatically selected and executed at the appropriate time in the maintenance procedure.
- The support mode permits the CE to select and control the execution of a routine or test within a routine.

Organization of Tests

The 3880 diagnostics are executed automatically during an initial microcode load (IML), or from the maintenance device (MD), either automatically or under the direction of the CE.

A detailed description of the MD diagnostic operating procedures is located in the MD section of the Maintenance Support Manual (MSM).

The following is a list of all the diagnostic test groups:

- Read-only Storage (ROS) Hardcore Tests
- Initial Microcode Load (IML) Hardcore Tests
- Routines 50-6B - Subsystem Storage Tests
- Routine 70 - Function Tests
- Routine 71 - Unidirectional Control Interface (CTL-I) Wrap Diagnostic (Model 21)
- Routine 72 - Inline Display Utility
- Routine 75 - T3880B OLT Microcode Support
- Routine 77 - Bidirectional Control Interface (CTL-I) Wrap Diagnostic (Model 23)
- Routine 78 - Electronic Channel Wrap Diagnostic
- Routine 79 - External Channel Wrap Block Diagnostic
- Routine 7E - Auxiliary Storage Director Microprocessor Tests

Read-Only Storage (ROS) Hardcore Tests

The read-only storage (ROS) hardcore tests reside in the ROS of each storage director. The IML operation executes these tests prior to the execution of any other microcode. Any error detected by these tests is loaded into the external bus out register (EBO) for analysis by the maintenance device.

Initial Microcode Load (IML) Hardcore Tests

The IML hardcore tests reside on the functional diskette. These tests execute as a series of diagnostic overlays after track 0 on the functional diskette has been read, and prior to the functional microcode being loaded into control storage from the functional diskette. Any error detected by these diagnostics is loaded into the external bus out register (EBO) for analysis by the maintenance device.

Diagnostic Test Errors

Test errors are points in the diagnostic where an error exit is taken. Each diagnostic routine has an error description for that routine and test. The error descriptions are in the following format:

5E02F0: Store operation ended with a lower port check

The error description shows the routine, test, and error stop with a description of the error.

In the above example:

Routine 5E, test 02 was running, and had an error stop of F0. The error description is: a store operation ended with a lower port check.

Routine 50 - CMCA and CMCD Register Test

This routine checks the registers not checked by the hardcores on the CMCA and CMCD cards.

Routine 51 - CMCA Card Checkout Part 2

This routine continues to check out the CMCA card.

Routine 52 - Port Control Test

This routine checks the indirect register addressability and error detection associated with the CMPC card.

Routine 53 - Port Buffer Indirect Register Test

This routine checks the indirect register addressability associated with the CMPB card.

Routine 54 - Port Buffer Error Generation

This routine checks the error detection circuitry on the CMPB card.

Routine 55 - Port Buffer Data Path

This routine checks the port buffer array with a read write test loop.

Routine 56 - Port Data Path to Subsystem Storage

This routine checks the complete data path.

Routine 57 - Storage Address Indirect Registers

This routine checks the indirect registers located on the storage control board (CMSA, CMC1, CMC2, CME1 - CME3 cards).

Routine 58 - Storage Address Error Generation

This routine checks the error detection circuitry located on the CMSA card.

Routine 59 - Storage Address Data Path

This routine checks the storage address data path by writing to SSARS 1, 2, and 3.

Routine 5A - Storage Data Driver

This routine checks the CMDD card with different data combinations.

Routine 5B - Storage Control Error Generation

This routine checks the error detection circuitry on the CMC1 and CMC2 cards.

Routine 5C - ECC Data Path and Error Generation

This routine checks the data path and error detection circuitry on the CME1, CME2, and CME3 cards.

Routine 5D - Single-Bit Error Correction

This routine checks the single-bit error correction circuitry on the CME1, CME2, and CME3 cards.

Routine 5E - Double-Bit Error Correction

This routine checks the double-bit error correction circuitry on the CME1, CME2, and CME3 cards.

Routine 5F - Uncorrectable Error Detection

This routine checks the uncorrectable error circuitry on the CME1, CME2, and CME3 cards.

Routine 60 - Dual Transfers

This routine checks that data can be interleaved through the upper and lower ports.

Routine 61 - Shadow Byte Count Register

This routine checks the port buffer shadow byte count register for proper operation.

Routine 62 - Port buffer

This routine checks that data can be transferred between cache and channel and cache and device.

Routine 63 - Byte Count Zero Operation

This routine checks the upper and lower byte counters.

Routine 64 - Padding Function

This routine checks that the disable padding function on the channel is working correctly.

Routine 65 - Communication Diagnostic 1 (Model 21 Only)

This routine is the first part of the communication between storage directors checkout.

Routine 66 - Communication Diagnostic 2 (Model 21 Only)

This routine is the second part of the communication between storage directors checkout.

Routine 67 - Communication Diagnostic 3 (Model 21 Only)

This routine is the third part of the communication between storage directors checkout.

Routine 68 - Subsystem Storage Cards Data Test

This routine checks that all of the data bits can be set and reset correctly on the storage cards.

Routine 69 - Subsystem Storage Cards Address Test

This routine checks the address path from the SSARs to the Storage cards.

Routine 6A - Subsystem Storage Cards Error Mapping

This routine counts the number of bits in error for a partition per each card.

Routine 6B - CMCA and CMCD Register Test

This routine checks the registers not checked by the hardcores on the CMCA and CMCD cards. This is the first part of the CMCA and CMCD register test it is run before Routine 50.

Routine 70 - Function tests

Routine 70 provides the same testing as IML hardcore tests 01 through 20. Routine 70 also contains special control storage tests 21 through 29.

Routine 71 - Unidirectional Control Interface (CTL-I) Wrap

Diagnostic (Model 21)

This control interface wrap diagnostic provides extended testing of the Model 21 CTL-I hardware by wrapping the outbound lines to the the inbound lines using an external wrap cable.

Routine 72 - Inline Display Utility

The inline display utility is used by the MD to access data in control storage of a selected storage director concurrent with customer operation.

Routine 75 - T3880B OLT Microcode Support

The T3880B OLT microcode support routine provides the functional microcode to support the T3880B online test.

Routine 77 - Bidirectional Control Interface (CTL-I) Wrap

Diagnostic (Model 23)

This control interface wrap diagnostic provides extended testing of the Model 23 CTL-I hardware by wrapping the outbound lines to the the inbound lines using an external wrap cable.

Routine 78 - Electronic Channel Wrap Diagnostic

The electronic channel interface diagnostic provides extended testing of the channel and automatic data transfer hardware.

Routine 79 - External Channel Wrap Block Diagnostic

The external channel wrap block diagnostic provides extended testing of the external channel interface hardware by wrapping the inbound tag and bus lines to the outbound tag and bus lines.

Routine 7E - Auxiliary Storage Director Microprocessor Tests

Routine 7E provides the same testing as IML hardcore tests 21 through 50.

Hardware Areas Tested by the Diagnostics

The chart below shows the hardware areas tested by each of the diagnostic routines and tests.

HARDWARE AREA TESTED	ROS HARD-CORE TESTS	IML HARD-CORE TESTS	ROUTINES								
			70	71	72	75	5X 6X	77	78	79	7E
Channel Interface						X				X	
Channel, Except Interface		X	X						X	X	
Channel Data Transfer		X	X						X		
Automatic Data Transfer		X	X	X				X	X		
Device Data Transfer		X	X	X				X	X		
Control		X	X	X				X	X		
Control Interface				X				X	X		
Control Storage	X	X	X								
Microprocessor	X	X	X								
Device Interface				X				X			
Subsystem Storage							X				
Aux. Storage Director Microprocessor (ASDM)		X									X

Diagnostic Execution Procedures Using the Maintenance Device (MD)

Refer to the MD diagnostic operating procedures in the MD section of the maintenance support manual (MSM).

Diagnostic Execution Options

When running one of the selectable diagnostic routines (such as routines 50-6B, 70, 71, 78, 79, 7E) there are two additional types of execution criteria which may be specified, routine parameters and run options.

- Routine parameters are used as follows:

  For routines 50-6B to specify a test to loop within a routine and/or other test requirements.

  For routines 70, 71, 78, 79, and 7E to specify a test or range of tests to run.

  For routine 72 to select the data to be displayed.

- Run options are used as follows:

  To optionally specify looping of a test or routine.

  To optionally specify halting with an error display when an error is detected, or continuing following an error and displaying the error dynamically.

The routine parameters are specific to a routine and are described on the test 00 page specified for that routine.

Run options are not specific to a routine and are described on the next page.

Diagnostic Run Options

Two diagnostic run options can be optionally specified during the execution of a routine. These run options are:

- Continue on error, or bypass error halt

  The continue on error option bypasses a halt that normally occurs after an error exit is used by the routine. This option is used with the loop routine option when the CE wishes to place the routine in a scope loop. Following an error exit, the failing test or block of tests are restarted.

- Loop routine/test

  The loop routine option causes the routine to loop upon termination. If a test block is specified, then only those tests specified will be looped. If no test block is specified then the entire routine is looped.

Looping a Single Test

To loop a single test, specify the test to be looped in parameter byte 3. For example 000003 is used to loop test 03.

To loop a single test (for other than routines 50-6B), specify the test to be looped in parameter bytes 1 and 2. For example 030300 is used to loop test 03. The run option loop routine/test must be specified.

Looping a Block of Tests

To loop a block of tests (for other than routines 50-6B) specify the low (first) and high (last) test numbers in parameter bytes 1 and 2. For example 1A1C80 is used to loop tests 1A, 1B, and 1C. The loop routine option must also be specified.

Diagnostic Action Based on Run Options and Termination Mode

The table below shows the action used by the diagnostic based on the run options in effect and the type of termination mode used by the diagnostic.

RUN OPTION IN EFFECT		DIAGNOSTIC ACTION TAKEN BASED ON TERMINATION MODE			
LOOP ROUTINE	CONTINUE ON ERROR	END OF ROUTINE	NORMAL ERROR DISPLAY	DYNAMIC ERROR DISPLAY	DISPLAY WITH HALT
Off	Off	Halt or Wait	Halt or Wait	Continue	Halt or Wait
Off	On	Halt or Wait	Continue	Continue	Halt or Wait
On	Off	Restart Routine	Halt or Wait	Continue	Halt or Wait
On	On	Restart Routine	Continue	Continue	Halt or Wait

Diagnostic Error Displays

The following shows the format of the error displays that can be received from a diagnostic routine:

	FIRST ERROR DISPLAY	SECOND ERROR DISPLAY	THIRD ERROR DISPLAY	FOURTH OR LAST ERROR DISPLAY
Failing Test Number	E1	E5	E9	ED
Test Error Code	E2	E6	EA	EE
Expected Data or Address	E3	E7	EB	EF
Received Data or Address	E4	E8	EC	

The following is the display format on the maintenance device when running diagnostics under support option 7:

```
DIAGNOSTIC DETECTED
AN ERROR. IC=rrttcc
BYTES=E1E2E3E4E5E6E7
E8E9EAEBECEDEEEF
```

Where:

rr = routine

tt = test ID

cc = error code

Those six hex digits make up the isolation codes described under each routine on the following pages. The error display bytes (E1, E2, and so forth) are also described under each routine.

Normally only the first error display shown above appears (when running the halt on error run option). The second, third, and fourth error displays are used when the diagnostic is continued following an error display with halt. These are also used when multiple errors are detected (when the loop and continue on error run options are in effect).

The information in the fourth error display position above is variable. These bytes are over-layed with new information for each new error encountered after the fourth error.

The significance of the expected and received data or address values of each error display vary with the particular error.

Refer to the routine and test for a description of the isolation codes.

Diagnostic Control Display

8Cxx = Routine xx running

8Dxx = Dynamic display during execution of routine xx

CAxx = Routine xx ready for execution

E1xx = Error indicated for routine xx

Note: 8Dxx will be displayed only by diagnostics capable of running concurrently.

ROS Hardcore Diagnostics

ROS Hardcore

Description

The ROS Hardcore tests validate the following:

- Branch Direct, Branch and Link, and Branch on Condition instructions
- Branch on Internal instruction register bits
- Branch on External instruction register bits
- External register operations
- Internal register array (store)
- Internal register array (fetch)
- Maintenance interface card, exit on selective reset, and level 0 PSW initialization
- Control storage fetch and store operations.
- Control storage, static and dynamic (store portion)
- Control storage, static and dynamic (fetch portion) and ROS hardcore exit

Error Description

The contents of the external bus out (EBO) are as follows:

EBO = E0: Failure while testing maintenance card
EBO = E1: Failure while testing static CS card 1
EBO = E2: Failure while testing static CS card 2
EBO = E3: Failure while testing first location dynamic CS card
EBO = E4: Failure while testing static CS card 1
EBO = E8: Failure while testing microprocessor card

EBO Code to Hardcore Test Number Cross Reference Listing

The following table provides a list of the hardcore tests associated with each of the EBO codes which can be issued during an initial microcode load (IML). These are provided to give insight into what testing was being performed at the time an error is detected.

EBO Codes

EBO CODE	HARDWARE TEST NUMBER(s)
20	01,02,03,04,05,06
21-22	07,08,09
23	0A,0B
24	0C,0D
25-3F	0E
51-54	0F
61-6E	0E
71-7F	13,14,15
91-97	0F
98-9A	10,11
9C-9D	12
9E-9F	13,14
A1	14
A2	15
A3-AB	16,17,18,19,1A
AC	18,1A
AD	1A
AE	13,19
AF	14,15,1A
B1-B9	16,17,18,1A
BB	19
BC-BD	1B
C1-C5	1B,1C
C6-C7	1B
C8	1C
C9	1D
CA-CB	1E
CC-CD	1F
CE-CF	20
E0-E4	ROS
E8	ROS
E9,EA	21-36,37-3D,4B-50
EB	24,37-3D,4B-50
EC	4B-50

Using Routines 70 and 7E to Determine Point of Failure in Hardcore Tests

In most cases it is not possible to determine the exact point in the hardcore tests where an error is detected, since more than one test can issue the same EBO code. Routines 70 and 7E can be used to determine the exact point of failure in the hardcore tests. Routines 70 and 7E are a duplication of the hardcore tests and contain a unique error or isolation code for each error detected. Routine 70 is a duplication of the first part, and routine 7E is a duplication of the second part.

In order to run routine 70 or 7E, it is necessary to complete an IML. If IML fails to complete due to a hardcore detected error, refer to 'Bypass IML Error Halt' in the MD section of the MSM.

When IML is complete, run routine 70 with default parameters (to execute all linked series tests).

Hardcore to Routine 70 Test Cross Reference Listing

HARDCORE TEST NUMBER	ROUTINE 70 TEST NUMBER	TEST DESCRIPTION
01	01	Branch Direct
02	02	Branch and Link
03	03	Branch and Link Register
04	04	Branch on Condition
05	05	Jump on Internal Register Bit
06	06	Jump on External Register Bit
07	08	Internal to Internal Register
08	09	Internal Register Immediate
09	0A	External Register
0A	0B	Control Store Op 0
0B	0C	Control Store Op 1
0C	0D	Internal Register Array Fixed
0D	0E	Internal Register Array Variable
0E	--	External Register Reset
0F	0F	External Register Read/Write
10	10	Control Store Fixed
11	11	Control Store Variable
12	07	Interrupt Test
13	12	Automatic Data Transfer Buffer Test #1
14	13	Automatic Data Transfer Buffer Test #2
15	14	Automatic Data Transfer Buffer Test #3
16	15	Automatic Data Transfer Buffer to Device Bus Out
17	16	Device Bus In to Automatic Data Transfer
18	17	Automatic Data Transfer Pad/Drop Buffer
19	18	Automatic Data Transfer Padding Circuit
1A	19	Automatic Data Transfer Buffer Wrap
1B	1A	Automatic Data Transfer Buffer to Channel Bus In
1C	1B	Check 2 and Device Overrun
1D	1B	Search Compare Hardware
1E	1D	CSC Card Check
1F	1E	CDX Card Check
20	1F	Interval Timer

Hardcore to Routine 7E Test Cross Reference Listing (Model 21 Only)

HARDCORE TEST NUMBER	ROUTINE 7E TEST NUMBER	TEST DESCRIPTION
21	01	CPACK1, CPACK2 Reset Value Test
22	02	1B, 1B Shadow, '08' Register Test
23	03	1B Register Increment
24	04	CCOMAD1 Write/Read
25	05	Force Port Adapter IR Check 1
26	06	Force Port Adapter IR Check 2
27	07	Force Port Adapter IR Check 3
28	08	Force SDM ALU Out Parity Check
29	09	Force External Register Address or Decode Check
2A	0A	Force External Register Selection Check
2B	0B	Force Read Clock Delay Check
2C	0C	Force ALU Out Control Check
2D	0D	Force Clock Check
2E	0E	Force CD Duplicate IR Address Decode Check
2F	0F	Force Range Select Check
30	10	Force ADT/ASDM IR Check 1
31	11	Force ADT/ASDM IR check 2
32	12	Force ADT Buffer/ASDM CS In Parity
33	13	Force Duplicate IR Address Check
34	14	Force Car Check
35	15	CACTL Write/Read
36	16	CARD1, CARD2 Write/Read
37	17	ASDM Control Store Write/Read
38	18	ADT Buffer Write/Read
39	19	ASDM Control Store/ADT buffer Write/Read
3A	1A	ASDM Control Store/ADT Buffer Write/Read
3B	1B	ADT Buffer Write/Read
3C	1C	ASDM Control Store Wrap 1
3D	1D	ASDM Control Store Wrap 2
3E	1E	ASDM Branch Direct Command
3F	1F	ASDM Branch and Link Command
40	20	ASDM Command Branch and Link Register
41	21	ASDM Command Branch on Condition
42	22	ASDM Command Jump on Internal Register
43	23	ASDM Command Jump on External Register
44	24	ASDM Internal Register to Int Register
45	25	ASDM Int Register to Immediate Inst
46	26	ASDM External Register Instruction
47	27	ASDM Control Store Op 0
48	28	ASDM Control Store Op 1
49	29	ASDM Internal Register Array
4A	2A	ASDM Internal Register Array
4B	2B	ASDM External Register Write/Read
4C	2C	Force ASDM LSR/External Register Address Parity 1
4D	2D	Force ASDM LSR/External Register Address Parity 2
4E	2E	Force ASDM Internal Check
4F	2F	Force ASDM SC Address Parity
50	30	ASDM Level 6/7 Interrupt

Routine HC Test 01

Description

This test validates the operation of the microprocessor instruction Branch Direct.

The following are validated:

- Failure to branch (next instruction executed)
- Branch to address other than that intended
- Registers modified on branch

Error Description

EBO = 20: Branch Direct instruction failed

Routine HC Test 02

Description

This test validates the operation of the microprocessor instruction Branch and Link.

The following are validated:

- Branch is taken (next instruction not executed)
- IAR+1 saved in PR4
- All other registers not changed

Error Description

EBO = 20: Branch and Link instruction failed

Routine HC Test 03

Description

This test validates the operation of the microprocessor instruction Branch and Link Register.

The following are validated:

- Branch is taken to IR1
- IAR+1 saved in IR2
- All other registers not changed

Error Description

EBO = 20: Branch and Link Register instruction failed

Routine HC Test 04

Description

This test validates the operation of the microprocessor instruction Branch on Condition.

The following are validated:

- Branch is taken when appropriate
- Branch not taken when appropriate

Error Description

EBO = 20: Branch on Condition instruction failed

Routine HC Test 05

Description

This test validates the operation of the microprocessor instruction Jump on Internal Register Bit. The following are validated:

- Branch is taken when appropriate
- Branch not taken when appropriate

Error Description

EBO = 20: Jump on Internal Register Bit instruction failed

Routine HC Test 06

Description

This test validates the operation of the microprocessor instruction Jump on External Register Bit.

The following are validated:

- Branch is taken when appropriate
- Branch not taken when appropriate

Error Description

EBO = 20: Jump on External Register Bit instruction failed

Diagnostic Tests DC HC01

Routine HC Test 07

Description

This test validates the operation of the microprocessor Internal Register to Internal Register instruction.

The following are validated:

- Condition codes set properly following execution
- Accumulator (destination register) contains valid results

Error Description

EBO = 21: Internal Register to Internal Register instruction failed
EBO = 22: Condition codes set following instruction execution failed

Routine HC Test 08

Description

This test validates the operation of the microprocessor Internal Register Immediate instruction.

The following are validated:

- Condition codes set properly following execution
- Accumulator (destination register) contains valid results

Error Description

EBO = 21: Internal Register Immediate instruction failed
EBO = 22: Condition codes set following instruction execution failed

Routine HC Test 09

Description

This test validates the operation of the microprocessor External Register instruction.

The following are validated:

- Condition codes set properly following execution
- Accumulator (destination register) contains valid results

Error Description

EBO = 21: External Register instruction failed
EBO = 22: Condition codes set following instruction execution failed

Routine HC Test 0A

Description

This test validates the operation of the microprocessor instruction Control Store OP 0. The following are validated.

- Fetch from a known location (correct data loaded)
- Increments address only when it should
- Store does not take place during a fetch operation
- Registers not altered during operation

Error Description

EBO = 23: Microprocessor instruction Control Store OP 0 failed

Routine HC Test 0B

Description

This test validates the operation of the microprocessor instruction Control Store OP 1. The following are validated:

- Fetch from a known location (correct data loaded)
- Increments address only when it should
- Store does not take place during a fetch operation
- Registers not altered during operation

Error Description

EBO = 23: Microprocessor instruction Control Store OP 1 failed

Routine HC Test 0C

Description

This test validates the integrity of the microprocessor internal register array. The following are validated:

- Ability to store various data patterns in each location
- Ability to fetch data from the stored location
- Valid register selection

Error Description

EBO = 24: Microprocessor internal register array failed

Routine HC Test 0D

Description

This test validates the integrity of the microprocessor internal register array. The test stores a unique data pattern in each register location and validates the store only after every location has been stored into. The following are validated:

- Ability to store various data patterns in each location
- Ability to fetch data from the stored location
- Valid register selection

Error Description.

EBO = 24: Microprocessor internal register array failed

Routine HC Test 0E - External Register Reset Condition Test

Description

This test is used to validate the reset conditions of each of the external registers. Each external register is compared to an expected value.

Error Description

EBO = 25: DXC, TFR, BAL, BAH, CBL, CBH, DBL, or DBH register failure
EBO = 26: DRC register failure
EBO = 27: DTG or DBO register failure
EBO = 28: MCS or DCH register failure
EBO = 29: CXC or CBI register failure
EBO = 2A: CBO register failure
EBO = 2B: CS1, CS3, or CC1 register failure
EBO = 2C: CR2, CR3, or CR6 register failure
EBO = 2D: ILR register failure
EBO = 2E: XCS register bits 2 and 6 are on
EBO = 2F: XCS register bits 4 and 5 are on
EBO = 31: XCS register bit 7 is on
EBO = 32: XES register bit 4 is on
EBO = 33: DXC register bit 0 or CHK register bit 6 not correct
EBO = 34: CR0 register bit 6 is on
EBO = 35: CS2 register bit 4 is on
EBO = 36: CR0 register bit 1 is on
EBO = 37: Clock check without a card check
EBO = 38: XES register bits 0, 2, 4, or 5 are on
EBO = 39: XES register bit 1 is on
EBO = 3A: XES register bit 6 is on
EBO = 3C: CHK register bit 0 is on
EBO = 3D: CHK register bit 1 is on
EBO = 3E: CHK register bit 2 is on
EBO = 3F: CHK register bit 3 is on
EBO = 5D: CHK register bit 4 is on
EBO = 5E: CR0 register bit 1 is on
EBO = 5F: CR0 register bit 1 is off
EBO = 61: CR0 register bit 1 is on
EBO = 62: CR0 register bit 1 is on
EBO = 63: CR0 register bit 2 is on
EBO = 64: CR0 register bit 3 is on
EBO = 65: CR0 register bit 0 is on
EBO = 66: CS2 register bit 3 is on
EBO = 67: CS2 register bit 4 is on
EBO = 68: CS2 register bit 5 is on
EBO = 69: CS2 register bit 6 is on
EBO = 6A: CS2 register bit 7 is on
EBO = 6C: CR0 register bit 1 is on
EBO = 6D: CHK register bit 5 is on
EBO = 6E: CHK register bit 6 is on
EBO = 91: DXC register failure
EBO = 93: MCS register bit 2 is off
EBO = E9: CSPRDIC register bit other than bit 3 is on, CPACK1 or CPACK2 register is not zero, or CHK register bit 7 is on
EBO = EA: CAAJCK register is not zero

Routine HC Test 0F

Description

This test validates the integrity of the storage director external registers. The following are validated.

- Ability to store and fetch all possible data patterns in the read/write registers
- Ability to store all possible data patterns in the write only registers
- Ability to read a read-only register

Error Description

EBO = 51: TFR register bit 2 (bap switch) not in correct state
EBO = 52: CHK register bit 0 is not at the correct value
EBO = 53: CHK register bit 0 is on
EBO = 54: TFR register bit 2 (bap switch) not in correct state
EBO = 91: DXC register failure
EBO = 92: DBO or DTG register failure
EBO = 93: DCH, DCL, MCS, or RLL register failure
EBO = 94: CXC, CBI, CCH, or CCL register failure
EBO = 95: CC2, CC1, or CS3 register failure
EBO = 96: CR2, CR3, or CR6 register failure
EBO = 97: CR0 register bit 2 (CDX card check is on)
EBO = 0A: CHK register bit 2 (CSR card check 2) is on

Routine HC Test 10

Description

This test is used to validate the ability to store and fetch various data patterns to and from static and dynamic control storage. Each block (address range) of control storage is stored into before the fetch verification.

Error Description

EBO = 98: Miscompare in address range X'0B00' through X'0FFF'
EBO = 99: Miscompare in address range X'1000' through X'1FFF'
EBO = 9A: Miscompare in address range X'6000' through X'BFFF'
EBO = 9B: Miscompare in address range X'2000' through X'2FFF'
EBO = 9C: Miscompare in address range X'3000' through X'38FF'

Routine HC Test 11

Description

This test is used to validate the ability to store and fetch a unique data pattern into each static and dynamic control storage location. All addresses are stored into prior to fetch verification to test for any control storage access decode failures.

Error Description

EBO = 98: Miscompare in address range X'0B00' through X'1FFF'
EBO = 99: Miscompare in address range X'1000' through X'1FFF'
EBO = 9A: Miscompare in address range X'6000' through X'FFFF'
EBO = 9B: Miscompare in address range X'2000' through X'2FFF'
EBO = 9C: Miscompare in address range X'3000' through X'38FF'

Routine HC Test 12

Description

This test checks the operation of the microprocessor Interrupt Processing command. It tests:

- The ability to change interrupt levels from:
  - Level 3 to Level 2 to Level 1
  - Level 1 to Level 2, Level 2 to Level 3
  - Level 3 to Level 1
  - Level 1 to Level 3
- PSWs contain valid contents after an interrupt
- ILR/IRG registers contain valid contents after an interrupt

Error Description

EBO = 9C: ILR register not correct after an interrupt
EBO = 9D: PSWs or condition codes not correct

Routine HC Test 13

Description

This test validates the writing and reading of the ADT buffer using the BFR register. The test includes testing for pre-fetch failures and array out parity checks.

Error Description

EBO = 71: BAP register address not correct
EBO = 72: Clock check/DXD card check
EBO = 73: CHK register bit 0 (DXA card check) is on
EBO = 74: CHK register bit 6 (DXD card check) is on
EBO = 75: CHK register bit 4 (array out parity check) is on
EBO = 78: CHK register bit 4 (array out parity check) is off
EBO = 79: Data loaded from BFR does not equal test pattern

Routine HC Test 14

Description

This test validates the writing and reading of the ADT buffer using the BFI register. As the data is written and read from the ADT, the BAP (buffer ALU pointer) registers are validated.

Error Description

EBO = 71: BAP register address not correct
EBO = 72: Unexpected clock check or DXD card check
EBO = 73: CHK register bit 0 (DXA card check) is on
EBO = 74: CHK register bit 6 (DXD card check) is on
EBO = 7C: CHK register bit 4 (array out parity check) is on
EBO = 7D: Data loaded from BFI does not equal test pattern data
EBO = AF: BAP register did not wrap to the correct address

Diagnostic Tests DC HC10

Routine HC Test 15

Description

This test validates the writing and reading of the ADT buffer using the CFI register. As the data is written and read from the ADT, the CBP (channel buffer pointer) registers are validated.

Error Description

EBO = 72: CHK register bit 6 (DXD card check) is on
EBO = 73: CHK register bit 0 (DXA card check) is on
EBO = 74: CHK register bit 6 (DXD card check) is on
EBO = 7C: CHK register bit 4 (array out parity check) is on
EBO = 7E: CBP register address not correct
EBO = 7F: Data loaded from CFI does not equal test pattern
EBO = AF: CBP did not wrap to the correct address

Routine HC Test 16

Description

This test transfers data from the ADT Buffer to the DBO register on the DCC card using a two byte data transfer. This test validates the following:

- The integrity of the data transferred
- The decrement of the device count registers
- The device end-of-transfer indication
- The presence of any error check indicators during or following the data transfer
- The proper increment of the device buffer pointer (DBP) register.
- The DRC register
- Suspend DRC register operation

Error Description

EBO = A3: CHK register bit 0 (DXA card check) is on
EBO = A4: Data in the DBO register does not equal the data pattern
EBO = A5: XCS register bit 6 (first sync in latch) is not correct
EBO = A6: DCH and DCL registers do not equal the expected value
EBO = A7: XCS register bit 2 (device end of transfer) is not correct
EBO = A8: XES register bit 4 (DCI card check) is on
EBO = B1: XES register bit 7 (device buffer check) is on
EBO = B2: DRC register value is not as expected
EBO = B3: DBH and DBL registers value are not as expected

Routine HC Test 17

Description

This test transfers data from device bus in (DBI) register to the ADT buffer and validates the following:

- The integrity of the data transferred
- The decrement of the device count registers
- The device end-of-transfer indication
- The presence of any error check indicators during and following the data transfer
- The proper increment of the buffer pointer (DBP) register
- The DRC register
- Suspend DRC register operation

Error Description

EBO = A3: CHK register bit 0 (DXA card check) is on
EBO = A9: CHK register bit 6 (DXD card check) is on
EBO = AA: XCS register bit 6 (first sync in latch) is off
EBO = AB: Data in BFR register is not as expected
EBO = B1: XES register bit 7 (device buffer check) is on
EBO = B5: XES register bit 4 (DCC card check) is on
EBO = B7: DRC register value is not as expected

Routine HC Test 18

Description

This test is used to test the ADT pad/drop hardware circuits and validates the following:

- The data transmitted from or to the ADT buffer before, at, or following the pad/drop transition point
- Status and error indications at and following the pad/drop transition point
- Status and error indication following the completion of the data transfer operation

Error Description

EBO = A3: CHK register bit 0 (DXA card check) is on
EBO = A4: DBO register value is not as expected
EBO = A5: XCS registers bit 6 (first sync in latch) not correct
EBO = A7: XCS register bit 2 (device end of transfer) not as expected
EBO = A8: XES register bit 4 (DCC card check) is on
EBO = A9: CHK register bit 6 (DXD card check) is on
EBO = AB: BFR register value is not as expected
EBO = B1: XES register bit 7 (device buffer parity check) is on
EBO = B2: RLL/DRC register value is not as expected

Diagnostic Tests DC HC15

Routine HC Test 19

Description

This test is used to validate the state of the device tag out register during a transfer of data from the ADT buffer to device bus out (DBO) register. This test is not run on Model 21 (DCI) machines.

Error Description

EBO = BB: DTO register value is not as expected

Routine HC Test 1A

Description

This test validates the following:

- The successful increment of the DBH and DBL registers from X'0001' to X'03FF'
- The successful decrement of the DCH and DCL registers from X'0400' to X'0000'
- The wrap of the DBH and DBL registers from X'03FF' to X'0200'
- The device end of transfer bit when the DCH and DCL registers are decremented through X'0000'

Error Description

EBO = A6: DCH and DCL registers value are not as expected
EBO = AF: DBH and DBL registers value are not as expected
EBO = B4: CHK register bit 1 (DCT card check) is on
EBO = B5: XES register bit 4 (DCC card check) is on
EBO = B6: CHK register bit 6 (DXA card check) is on

Routine HC Test 1B

Description

This test is used to test a data transfer from the ADT buffer to the channel bus in (CBI) register. The following is tested:

- The transfer of data from the ADT buffer to the CBI register
- Status and error indications during and following the transfer

Error Description

EBO = AE: XCS register bit 4 (CDX end of transfer) is not correct
EBO = BC: TFR register bits 6 and 7 (BC1 full, BC2 empty) is not correct
EBO = BD: XES register bit 6 (channel buffer check) is on
EBO = C6: CBI register data is not equal to the expected data
EBO = C7: CR0 register bit 3 (CSR card check) is on

Diagnostic Tests DC HC19

Routine HC Test 1C

Description

This test validates the level 2 interrupt hardware and the hardware error checks.

Error Description

EBO = C1: XES register bit 7 (device buffer check) is not correct
EBO = C2: XES register bit 6 (channel buffer check) is not correct
EBO = C3: XES register bit 0 (device overrun) is not correct
EBO = C5: XES register bit 5 (sync in check) is not correct
EBO = C8: ILR register bit 2 (new level 2) is not correct

Routine HC Test 1D

Description

This test checks the search compare hardware circuits and validates the following:

- Compare-successful bit turns on during a one byte data transfer to the CBI register
- That the compare-successful bit can be reset

Error Description

EBO = C9: XCS register bit 5 (compare successful) not correct

Routine HC Test 1E

Description

This test validates the CSC card hardware check by testing that a channel check 1 condition will cause a level 1 interrupt. The channel check 1 condition is caused by turning on bit 0 in the CXC register, along with bit 2 in the CC1 register.

Error Description

EBO = CA: CS2 register bits 4 and 7 (CSC card check, channel check 1) are on
EBO = CB: ILR register bit 1 (new level 1) is off

Routine HC Test 1F

Description

This test validates the CDX card hardware check by testing that a channel check 1 condition will cause a level 1 interrupt. The channel check 1 condition is caused by turning on bits 4 and 5 at the same time in the CXC register.

Error Description

EBO = CC: CR0 register bit 2 (CDX card check) is not correct
EBO = CD: CS2 register bit 7 (channel check 1) is off

Routine HC Test 20

Description

This test validates the interval timer by checking that:

- The timer interrupt occurs within the specified tolerance (650 milliseconds, +30% -20%)
- The timer can be disabled after being enabled

Error Description

EBO = CE: ILR register bit 1 (new level 1) is not correct
EBO = CF: Timer interval is too small or too large

Diagnostic Tests DC HC1C

Routine HC Test 21

Description

This test checks the reset value of the CPACK1 and CPACK2 registers on the CMCD card.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 22

Description

This test checks the integrity of the following registers:

- X'1B'
- X'1B' shadow
- X'0F'
- SP OP hold X'1B' shadow
- SP OP restore X'1B'

This is done by testing the reset value of the following ASDM external registers on the CMAA card:

- CAAJCK
- CACTL
- CARD1
- CARD2

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 23

Description

This test checks that the X'1B' register address increments after a WRF instruction. Addresses X'83', X'86', X'A3', X'A6', and X'FF' are loaded to the X'1B' register and a WRF instruction is then executed. The X'1B' register is then read to ensure that the increment occurred. The X'1B' shadow register is also read to ensure that it also incremented.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 24

Description

This test checks the CCOMADI register by writing and reading the following data patterns: X'00', X'05', X'0B', and X'10'.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 25

Description

This test forces a port adapter IR check (CPACK 1 register bit 0) in the following two ways:

- Set CCOMADI register to X'19', and then read a register on this card. This simulates that both write and read gates are active.
- Set CCOMADI register to X'1C', and then read a register on this card. This simulates that no write or read gates are active.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 26

Description

This test forces a port adapter IR check (CPACK 1 register bit 0) in the following two ways:

- Set CCOMADI to X'1A', and write to an addressable register on this card. This simulates a parity check on the IR address bus.
- Set CCOMADI to X'1F', and write to an addressable register on this card. This simulates a decoder check on the IR address bus.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 27

Description

This test forces a port adapter IR check (CPACK1 register bit 0) in the following two ways:

- Set CCOMADI register to X'1E', and then write to an addressable register on this card. This simulates an address decoder check.
- Set CCOMADI register to X'1B', and then write to an addressable register on this card. This simulates a parity check.

The X'1B' register will also cause an IR data out parity check (CPACK1 register bit 4).

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 28

Description

This test forces an SDM ALU out parity check (CPACK1 register bit 1) and an RDF reg read parity check (CPACK1 register bit 7). The SDM parity check is forced by setting register CCOMADI to X'16' and writing an odd number of bits to an addressable register on this card. The RDF parity check is forced by reading the register that was written at the beginning of this test. The SDM ALU Out P-Check' will also cause a PA IR check and an IR data out P-Check.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 29

Description

This test forces an external register address or decode check (CPACK1 register bit 2) in the following two ways:

- Set CCOMADI register to X'17' and then write to register X'1B'.
- Set CCOMADI register to X'10' which will immediately force the error. This will also cause an ALU out control check (CPACK1 register bit 6).

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 2A

Description

This test forces an EXT reg selection check (CPACK1 register bit 3) by setting the CCOMADI register to X'0C' and then writing to an addressable register on a card other than the CMCD card.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 2B

Description

This test forces a read clock delay check (CPACK1 register bit 5) by setting the CCOMADI register to X'14' and then reading any addressable register.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 2C

Description

This test forces an ALU out control check (CPACK1 register bit 6) by setting the CCOMADI register to X'15'.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC2A

Routine HC Test 2D

Description

This test forces a clock check (CPACK2 register bit 4) by setting register CCOMADI to X'08'.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 2E

Description

This test forces a CD duplicate IR addr decode check (CPACK2 register bit 5) by setting the CCOMADI register to X'18' and writing to a register on this card.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 2F

Description

This test forces a range select check (CPACK2 register bit 7) in the following two ways:

- Set register CCOMADI to X'0D' and the ADT buffer address to X'1000'.
- Set register CCOMADI to X'0D' and the ASDM control store address to X'2000'.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 30

Description

This test forces a ADT/ASDM IR check (CAAJCK register bit 0) in the following two ways:

- Set the CCOMADI register to X'19', and then read a register on this card. This simulates both write and read gates active.
- Set the CCOMADI register to X'1C', and then read a register on this card. This simulates that no write or read gates are active.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 31

Description

This test forces a ADT/ASDM IR check (CAAJCK register bit 0) in the following two ways:

- Set the CCOMADI register to X'1A', and write to an addressable register on this card. This simulates multiple decodes of the CD address bus.
- Set the CCOMADI register to X'1B', and write to an addressable register on this card. This simulates a parity check on the register data bus.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 32

Description

This test forces an ADT buffer ASDM CS in parity check' (CAAJCK register bit 3) by setting register CCOMADI to X'05' and writing to the ADT buffer.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC30

Routine HC Test 33

Description

This test forces a duplicate IR address decode check (CAAJCK register bit 4) by setting the CCOMADI register to X'03' and writing to a register on the CMAA card.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 34

Description

This test forces a CAR check (CAAJCK bit 7) in the following two ways:

- Set the CCOMADI register to X'09' and write to ASDM control store.
- Set the CCOMADI register to X'07' and write to ASDM control store.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 35

Description

This test checks the ASDM write register (CACTL). The register is written with a floating data pattern of X'01' and then read and the value compared to an expected value. Registers CAAJCK, CPACK1, CPACK2, CHK, and XCS are checked to ensure that no errors occur after the write/read operations. Bit 0 is not checked in this test.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 36

Description

This test checks the ASDM write registers (CARD1 and CARD2). The registers are written with a floating data pattern of X'01' and then read and the value compared to an expected value. Registers CAAJCK, CPACK1, CPACK2, CHK, and XCS are checked to ensure that no errors occur during the write/read operations. Bit 0 is not checked in this test.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 37

Description

This test validates the function of the ASDM control storage. A data pattern is written to control storage. The data is then read and compared to an expected value. The ADT buffer is read to ensure that no data was written to the buffer when the pointer used (BAP) is set to X'2xxx' or X'3xxx'. The read from control storage uses BAP = X'2xxx' or X'3xxx' and the read from the ADT buffer uses CBP = X'0xxx'. After the write and read operation, the CBP/BAP registers are checked for correct wrap points.

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Routine HC Test 38

Description

This test validates the function of the ADT buffer. A data pattern is written to the ADT buffer. The data is then read and compared to an expected value. The ASDM control storage is read to ensure that no data was written to the control storage when the pointer used (BAP) is set to X'0xxx'. The read from control storage uses CBP = X'3xxx' and the read from the ADT buffer uses BAP = X'4xxx'. After the write and read operation, the CBP and BAP registers are checked for the correct wrap points.

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Routine HC Test 39

Description

This test checks that data is written to the ADT buffer and ASDM control storage at the same time the pointer (CDP) is set to X'5xxx'. The data is read from control storage using BAP = X'3xxx' and the read from the ADT buffer is done using CBP = X'5xxx'. After the write and read operation, the CBP and BAP registers are checked for the correct wrap points.

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Diagnostic Tests DC HC37

Diagnostic Tests DC HC3A

Routine HC Test 3A

Description

This test checks that no data is written to the ADT buffer or ASDM control storage when the pointer used (BAP) is set to '4XXX'. The data read from the buffer and ASDM control storage is compared to make sure the data in the buffer and ASDM control storage was not overwritten by the write operation. The read from control storage uses BAP = '3XXX' and the read from the buffer uses CBP = '6XXX'. After the write and read, the CBP and BAP registers are checked for the correct wrap points.

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Routine HC Test 3B

Description

This test writes/reads data to/from the ADT buffer. The data read is compared to an expected value. The ASDM control storage is read to ensure that no data was written to control storage when the pointer used (BAP) is set to '6XXX'. The read from the ADT buffer uses BAP = '6XXX' and the read from control storage uses CBP = '3XXX'. After the write and read, the CBP and BAP registers are checked for the correct wrap points.

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Routine HC Test 3C

Description

This test will check the ASDM control storage wrap points. Four bytes are written to each block starting at location X'2XFC'. The pointer should wrap after the fourth byte. The wrap points are:

X'23FF' - - X'2200'

X'2BFF' - - X'2A00'

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Diagnostic Tests DC HC3A

Routine HC Test 3D

Description

This test will check the ASDM control storage wrap points. Four bytes are written to each block starting at location X'3XFC'. The pointer should wrap after the fourth byte. The wrap points are:

X'33FF' - - X'3200'

X'3BFF' - - X'3A00'

EBO = E9: CMCD Card Failure
EBO = EA: CMAA Card Failure
EBO = EB: CMCA Card Failure
EBO = EC: ASDM Failure

Routine HC Test 3E

Description

This test validates the operation of the ASDM command Branch Direct. The following are validated:

1. Branch is taken (next instruction not executed)
2. All other registers are unaltered

EBO = E9: CMCD Card Failure
EBO = EC: ASDM Failure

Routine HC Test 3F

Description

This test validates the operation of the ASDM Command Branch and Link. The following are validated:

1. Branch is taken (next instruction not executed)
2. IAR+1 (return address) is saved in PR4
3. All other registers, except PR4, are unaltered

EBO = E9: CMCD Card Failure
EBO = EC: ASDM Failure

Routine HC Test 40

Description

This test validates the operation of the ASDM Command Branch and Link Register instruction. The following conditions are checked to ensure that:

- A branch is taken to the IR1 (PR6) register
- IAR+1 is saved in the IR2 (PR2) register
- All other registers, except PR6 and PR2, are not changed

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 41

Description

This test validates the operation of the ASDM Command Branch on Condition instruction. The following conditions are checked to ensure that:

- A branch is taken when appropriate
- A branch is not taken when appropriate

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 42

Description

This test validates the operation of the ASDM Command Jump on Internal Register Bit instruction. The following conditions are checked to ensure that:

- A branch is taken when appropriate
- A branch is not taken when appropriate

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC40

Routine HC Test 43

Description

This test validates the operation of the ASDM Command Jump on External Register Bit instruction. The following conditions are checked to ensure that:

- A branch is taken when appropriate
- A branch is not taken when appropriate

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 44

Description

This test validates the operation of the ASDM Internal Register to Internal Register instruciton. The following conditions are checked to ensure that:

- The condition codes are set properly following an instruction execution
- The destination register for the accumulator contains valid results

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 45

Description

This test validates the operation of the ASDM Internal Register Immediate instruction. The following conditions are checked to ensure that:

- The condition codes are set correctly following an instruction execution
- The destination register for the accumulator contains valid results

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 46

Description

This test validates the operation of the ASDM External Register instruction. The following conditions are checked to ensure that:

- The condition codes set properly following an instruction execution
- The destination register for the accumulator contains valid results

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 47

Description

This test validates the operation of the ASDM instruction, Control Store OP 0. The following conditions are checked to ensure:

- The ability to fetch data from a known location
- The ability to store data at a known location
- That the address increments only when appropriate
- That the registers not involved are not changed

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 48

Description

This test validates the operation of the ASDM instruction, Control Store OP 1. The following conditions are checked to ensure:

- The ability to fetch data from a known location
- The ability to store data at a known location
- That the address increments only when appropriate
- That the registers not involved are not changed

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC46

Routine HC Test 49

Description

This test validates the integrity of the ASDM internal register array. The following conditions are checked to ensure:

- The ability to store various data patterns in each register location
- The ability to fetch data from the stored data location
- Valid register selection

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 4A

Description

This test validates the integrity of the ASDM internal register array. All registers in all groups are loaded with a unique data value 'xy' (where x is the register ID and y is the group ID). The store operation is validated after every register of a group has been stored into. The following conditions are checked to ensure:

- The ability to store a unique data pattern in each register location
- The ability to fetch data from the stored data location
- Valid register selection

EBO = E9: CMCD card failure
EBO = EC: ASDM failure

Routine HC Test 4B

Description

This test checks the ASDM read and write registers. SDM writes the CARD1 and CARD2 registers with a data pattern. Control is then passed to the ASDM. The ASDM reads the CARD1 and CARD2 registers and compares them to an expected value. The ASDM then writes this value to the CAWR1 and CAWR2 registers, then reads the registers and compares the data with an expected value. SDM then reads the CAWR1 and CAWR2 registers and compares the data with an expected value.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC49

Routine HC Test 4C

Description

This test forces an ASDM LSR/EXT register address parity check (CAAJCK register bit 1) by setting register CCOMADI to X'0B'. The ASDM then reads one of its indirect registers.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 4D

Description

This test forces an ASDM LSR/EXT register address parity check (CAAJCK register, bit 1) by setting register CCOMADI to X'02'. The ASDM then accesses one of its indirect registers.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 4E

Description

This test forces an ASDM internal check (CAAJCK register, bit 2) by setting register CCOMADI to X'1B'. The ASDM then reads the CARD2 register.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 4F

Description

This test forces an ASDM CS address parity check (CAAJCK register, bit 6) by setting register CCOMADI to X'01', then having the ASDM read its control storage.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Routine HC Test 50

Description

This test checks the ability of ASDM to change interrupt levels. The first part of the test changes from interrupt level 6 to interrupt level 7. The second part of the test changes from interrupt level 7 to interrupt level 6.

EBO = E9: CMCD card failure
EBO = EA: CMAA card failure
EBO = EB: CMCA card failure
EBO = EC: ASDM failure

Diagnostic Tests DC HC4F

Routine 50 Test 01

Descriptive Name

Subsystem Storage Tests

Description

This test checks the addressing and data integrity of the upper port OP/CTL register (UOPCTL) by writing and reading data patterns to and from the register.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500101: CPACK 1 register did not reset
500102: CPACK2 register did not reset
500103: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not reset
500104: CSPRDIC shows an error has occurred after write into UOPCTL register
500105: CPACK 1 register not as expected after write into UOPCTL register
500107: CSPRDIC shows an error has occurred after read from UOPCTL register
50010C: Read of UOPCTL register did not agree with write

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 02

Description

This test checks the addressing and data integrity of the upper port control register (UCTL) by writing and reading data patterns to and from the register.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500201: CPACK 1 register did not reset
500202: CPACK2 register did not reset
500203: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not reset
500204: CSPRDIC shows an error has occurred after write into the UCTL register
500205: CPACK 1 register not as expected after write into UCTL register
500207: CSPRDIC shows an error has occurred after read from UCTL register
50020C: Read of UCTL register did not agree with write

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 03

Description

This test checks the addressing and data integrity of the lower port OP/CTL register (LOPCTL) by writing and reading data patterns to and from the register.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500301: CPACK 1 register did not reset
500302: CPACK2 register did not reset
500303: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not reset
500304: CSPRDIC shows an error after write into LOPCTL register
500305: CPACK 1 register not as expected after write into LOPCTL register
500307: CSPRDIC shows an error has occurred after read from LOPCTL register
500309: CPACK2 register not as expected after read from LOPCTL register
50030C: Read of LOPCTL register did not agree with write

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 04

Description

This test checks the addressing and data integrity of the lower port control register (LCTL) by writing and reading data patterns to and from the register.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500401: CPACK1 register did not reset
500402: CPACK2 register did not reset
500403: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not reset
500404: CSPRDIC shows an error has occurred after write into LCTL register
500405: CPACK1 register not as expected after write into LCTL register
500407: CSPRDIC shows an error has occurred after read from LCTL register
50040C: Read of LCTL register did not agree with write
50040D: Bit 2 on the bus is active from reading the LCTL register

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 05

Description

This test checks the port buffer test loop W/R (bit 0 of the UPBDI register). A store operation is performed with bit 0 of the UPBDI register on. This bit inhibits the incrementing of the SSARs and the decrementing of the byte counter shadow register. These registers are checked for proper operation. Test A5 will be called if there is an IR Bus error.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors
Bit 2 - Unused
Bit 3 - 1 Run tests 6 through 12 after test 5

Isolation Codes

500511: Byte count shadow register is not as expected
500512: Reset value of UPBDI register is not correct
500513: CSPRDIC register indicates an error (bits 2, 3, and 4)
500514: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500516: Data transfer complete bit did not get set after a transfer operation and a microcode delay
500517: CSTAT4 register bit 5 (storage control board power off) or bit 6 (storage board 1 power off) is on
500518: BCS register changed while UPBDI register bit 0 (port buffer test loop W/R) was on
500519: SSAR registers changed while UPBDI register bit 0 (port buffer test loop W/R) was on
50051A: CSTAT1 register bit 4 (upper port op complete) was on
50051B: CSTAT3 register bit 5 (port adapter/control cables out) is on
50051C: CSPRDIC register bits 0, 1, and 2 indicate an error after reading CSTAT3
50051D: CSPRDIC register bits 0, 1, and 2 indicate an error after reading CSTAT4
50051E: CSPRDIC register bits 0, 1, and 2 indicate an error after doing common check, SD, and U/L check reset
500530: CSPRDIC register bits 2, 3, and 4 indicate an error after reading CSTAT1
500531: CSPRDIC register bits 2, 3, and 4 indicate an error after writing UPBDI
500532: CSPRDIC register bits 2, 3, and 4 indicate an error after reading UPBDI
500533: CSPRDIC register bits 2, 3, and 4 indicate an error after writing SSAR2
500534: CSPRDIC register bits 2, 3, and 4 indicate an error after reading SSAR2

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 06

Description

This test checks the port buffer test loop W/R (bit 0 of the LPBDI register). A store operation is performed with bit 0 of the LPBDI register on. This inhibits the incrementing of the SSARs and the decrementing of the byte counter shadow register. These registers are checked for proper operation. Test A6 will be called if there is an IR Bus error.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500611: Byte count shadow register is not as expected
500612: Reset value of LPBDI register is not correct
500613: CSPRDIC register indicates an error (bits 2, 3, and 4)
500614: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
500616: Data transfer complete bit did not get set after a transfer operation and a microcode delay
500617: CSTAT4 register bit 5 (storage control board power off) or bit 6 (storage board 1 power off) is on
500618: BCS register changed while LPBDI register bit 0 (port buffer test loop W/R) was on
500619: SSAR registers changed while LPBDI register bit 0 (port buffer test loop W/R) was on
50061A: CSTAT1 register bit 4 (lower port op complete) was on
50061B: CSTAT3 register bit 5 (port adapter/control cables out) is on
50061C: CSPRDIC register bits 0, 1, and 2 indicate an error after reading CSTAT3
50061D: CSPRDIC register bits 0, 1, and 2 indicate an error after reading CSTAT4
50061E: CSPRDIC register bits 0, 1, and 2 indicate an error after doing common check, SD, and U/L check reset
500630: CSPRDIC register bits 2, 3, and 4 indicate an error after reading CSTAT1
500631: CSPRDIC register bits 2, 3, and 4 indicate an error after writing LPBDI
500632: CSPRDIC register bits 2, 3, and 4 indicate an error after reading LPBDI
500633: CSPRDIC register bits 2, 3, and 4 indicate an error after writing SSAR2
500634: CSPRDIC register bits 2, 3, and 4 indicate an error after reading SSAR2

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 07

This test forces an SRC check (bit 1 of UPACK register) by storing a word with a byte count of 14 with SRC and then fetching the same stored 16 byte word with a byte count of 12 with SRC.

This bit should not be on when fetched with a byte count of 14 with SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500702: Reset value of UPACK register is not correct
500703: CSPRDIC indicates an error
500704: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500705: UPBCK register indicates an error
500706: Data transfer complete bit did not set after a microcode delay
500708: UPACK register indicates an error
500709: SRC check (bit 1 of UPACK) did not set by forcing method
50070A: CSTAT1 register bit 0 (upper port check) did not set
50070B: UPBCK register did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 08

This test forces an SRC check (bit 1 of lower port adapter check register) by storing a word with a byte count of 14 with SRC and then fetching the same stored 16 byte word with a byte count of 12 with SRC.

This bit should not be on when fetched with a byte count of 14 with SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500802: Reset value of LPACK register is not correct
500803: CSPRDIC indicates an error
500804: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
500805: LPBCK register indicates an error
500806: Data transfer complete bit did not set after a microcode delay
500808: UPACK register indicates an error
500809: SRC check (bit 1 of LPACK) did not set by forcing method
50080A: CSTAT1 register bit 1 (lower port check) did not set
50080B: LPBCK register did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 09

This test forces a DXR/PA parity check (bit 0 of UPACK) by setting the COMMADI register to X'11' then executing a fetch data operation with at least one byte having an odd number of active data bits. A byte count of 14 is used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'09' Run only test 09

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500902: Reset value of UPACK register is not correct
500903: CSPRDIC indicates an error
500904: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500906: Data transfer complete bit did not set after a microcode delay
500909: DXR/PA parity check (bit 0 of UPACK) did not set by forcing method
50090A: CSTAT1 register bit 0 (upper port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0A

This test forces a DXR/PA parity check (bit 0 of LPACK) by setting the COMMADI register to X'11' then executing a fetch data operation with at least one byte having an odd number of active data bits. A byte count of 14 is used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0A' Run only test 0A

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500A02: Reset value of LPACK register is not correct
500A03: CSPRDIC indicates an error
500A04: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
500A06: Data transfer complete bit did not set after a microcode delay
500A09: DXR/PA parity check (bit 0 of LPACK) did not set by forcing method
500A0A: CSTAT1 register bit 0 (upper port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0B

Description

This test forces a DXR/PA overrun check (bit 2 of UPACK register) by setting the COMMADI register to X'12' and executing a store data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0B' Run only test 0B

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500B02: Reset value of UPACK register is not correct
500B03: CSPRDIC indicates an error
500B04: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500B09: DXR/PA overrun check (bit 2 of UPACK) did not set by forcing method
500B0A: CSTAT1 register bit 0 (upper port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0C

Description

This test forces a DXR/PA overrun check (bit 2 of LPACK register) by setting the COMMADI register to a X'12' and executing a store data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0C' Run only test 0C

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500C02: Reset value of LPACK register is not correct
500C03: CSPRDIC indicates an error
500C04: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
500C09: DXR/PA overrun check (bit 2 of LPACK) did not get set by forcing method
500C0A: CSTAT1 register bit 1 (lower port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0D

Description

This test forces a DXR/PA underrun check (bit 2 of UPACK) by setting the COMMADI register to X'13' and executing a fetch data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0D' Run only test 0D

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500D02: Reset value of UPACK register is not correct
500D03: CSPRDIC indicates an error
500D04: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500D06: Data transfer complete bit did not set after a microcode delay
500D09: DXR/PA underrun check (bit 2 OF UPACK register) did not set by forcing method
500D0A: CSTAT1 register bit 0 (upper port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0E

Description

This test forces a DXR/PA underrun check (bit 2 of LPACK register) by setting the COMMADI register to X'13' and executing a fetch data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0E' Run only test 0E

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500E02: Reset value of LPACK register is not correct
500E03: CSPRDIC indicates an error
500E04: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
500E06: Data transfer complete bit did not set after a microcode delay
500E09: DXR/PA underrun check (bit 2 of LPACK register) did not set by forcing method
500E0A: CSTAT1 register bit 1 (lower port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 0F

Description

This test forces a PA/PB overrun check (bit 5 of UPACK register) by setting the COMMADI register to X'1D' and executing a store data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0F' Run only test 0F

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

500F02: Reset value of UPACK register is not correct
500F03: CSPRDIC indicates an error
500F04: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
500F06: Data transfer complete bit did not set after a microcode delay
500F09: PA/PB overrun check (bit 5 of UPACK) register did not set by forcing method
500F0A: CSTAT1 register bit 0 (upper port check) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 10

Description

This test forces a PA/PB overrun check (bit 5 of LPACK register) by setting the COMMADI register to X'1D' and executing a store data operation with a byte count of 14.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'10' Run only test 10

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

501002: Reset value of UPACK register is not correct
501003: CSPRDIC indicates an error
501004: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
501006: Data transfer complete bit did not set after a microcode delay
501009: PA/PB overrun check (bit 5 of LPACK register) did not set by forcing method
50100A: Lower port check (bit 1 of CSTAT1 register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 11

Description

This test forces a PA/PB data in/out parity check (bit 6 of UPACK register) by setting the COMMADI register to X'11' and executing a store data operation with at least one byte having an odd number of active data bits. A byte count of 14 is used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'11' Run only test 11

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

501102: Reset value of UPACK register is not correct
501103: CSPRDIC indicates an error
501104: CSTAT1 register bit 0 (upper port ck) or bit 6 (upper port data transfer complete) did not reset
501106: Data transfer complete bit did not set after a microcode delay
501109: PA/PB data in/out parity check (bit 6 of UPACK register) did not set by forcing method
50110A: Upper port check (bit 0 of CSTAT1 register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test 12

Description

This test forces a PA/PB data in/out parity check (bit 6 of LPACK register) by setting the COMMADI register to X'11' and executing a store data operation with at least one byte having an odd number of active data bits. A byte count of 14 is used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'12' Run only test 12

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

501202: Reset value of LPACK register is not correct
501203: CSPRDIC indicates an error
501204: CSTAT1 register bit 1 (lower port ck) or bit 7 (lower port data transfer complete) did not reset
501206: Data transfer complete bit did not set after a microcode delay
501209: PA/PB data in/out parity check (bit 6 of LPACK register) did not set by forcing method
50120A: Lower port check (bit 1 of CSTAT1 register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 50 Test A5

Description

This test is called when unexpected errors occur in test 05. It checks the IR bus to provide better isolation than that in test 05. If this test finds no fault, the original error code for test 05 is used.

Parameters

None required

Isolation Codes

50A501: Bits 4 and 5 of the CMADEC register not on
50A502: Bit 3 of the CMADEC register not on
50A503: Bit 0 of the CMADEC register not on
50A504: Bit 1 of the CMADEC register not on
50A505: SSARs not as expected
50A506: Byte counter high not as expected
50A507: No bits in CSACK when bit 4 of the CSPRDIC register is on
50A508: CSACK register bit 1 is on but CMADEC is correct
50A5E1: CSPRDIC not reset, CCTL register is correct, CCTLS register error
50A5E2: CSPRDIC not reset, CCTL register error, CCTLS register error
50A5E3: CSPRDIC not reset, CCTL register error, CCTLS register is correct
50A5x0: Bit 0 of CSPRDIC is on
50A5x1: Bit 1 of CSPRDIC is on
50A5x2: Bit 2 of CSPRDIC is on
50A5x3: Bit 3 of CSPRDIC is on
50A5x4: Bit 4 of CSACK is on with bit 4 of CSPRDIC on
50A5x5: Bit 5 of CSACK is on with bit 4 of CSPRDIC on
50A5x6: Bit 6 of CSACK is on with bit 4 of CSPRDIC on
50A5x7: Bit 7 of CSACK is on with bit 4 of CSPRDIC on
50A5x8: Bit 2 of CSACK is on with bit 4 of CSPRDIC on
50A5x9: Bit 4 of CSPRDIC is on
50A5xA: Bit 0 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A5xB: Bit 1 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A5xC: Bit 2 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A5xD: Bit 3 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A5xE: Bit 4 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A5xF: Bit 5 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on

Where

if x = 1: CSPRDIC register did not reset

if x = 2: CSPRDIC register detected an error on a write to the SA card

if x = 3: CSPRDIC register detected an error on a read from the SA card

if x = 4: CSPRDIC register detected an error on a write to the PB card

if x = 5: CSPRDIC register detected an error on a read from the PB card

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Contents of the CSPRDIC register
- E4 = Contents of the CSACK register
- E5 = Contents of the CMADEC register

Routine 50 Test A6

Description

This test is called when unexpected errors occur in test 06. It checks the IR bus to provide better isolation than that in test 06. If this test finds no fault, the original error code for test 06 is used.

Parameters

None required

Isolation Codes

50A601: Bits 4 and 5 of the CMADEC register not on
50A602: Bit 3 of the CMADEC register not on
50A603: Bit 0 of the CMADEC register not on
50A604: Bit 1 of the CMADEC register not on
50A605: SSARs not as expected
50A606: Byte counter high not as expected
50A607: No bits in CSACK when bit 4 of the CSPRDIC register is on
50A608: CSACK register bit 1 is on but CMADEC is correct
50A6E1: CSPRDIC not reset, CCTL register is correct, CCTLS register error
50A6E2: CSPRDIC not reset, CCTL register error, CCTLS register error
50A6E3: CSPRDIC not reset, CCTL register error, CCTLS register is correct
50A6x0: Bit 0 of CSPRDIC is on
50A6x1: Bit 1 of CSPRDIC is on
50A6x2: Bit 2 of CSPRDIC is on
50A6x3: Bit 3 of CSPRDIC is on
50A6x4: Bit 4 of CSACK is on with bit 4 of CSPRDIC on
50A6x5: Bit 5 of CSACK is on with bit 4 of CSPRDIC on
50A6x6: Bit 6 of CSACK is on with bit 4 of CSPRDIC on
50A6x7: Bit 7 of CSACK is on with bit 4 of CSPRDIC on
50A6x8: Bit 2 of CSACK is on with bit 4 of CSPRDIC on
50A6x9: Bit 4 of CSPRDIC is on
50A6xA: Bit 0 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A6xB: Bit 1 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A6xC: Bit 2 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A6xD: Bit 3 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A6xE: Bit 4 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on
50A6xF: Bit 5 of CMADEC is on with CSPRDIC bit 4 and CSACK bit 1 on

Where

if x = 1: CSPRDIC register did not reset

if x = 2: CSPRDIC register detected an error on a write to the SA card

if x = 3: CSPRDIC register detected an error on a read from the SA card

if x = 4: CSPRDIC register detected an error on a write to the PB card

if x = 5: CSPRDIC register detected an error on a read from the PB card

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Contents of the CSPRDIC register
- E4 = Contents of the CSACK register
- E5 = Contents of the CMADEC register

Routine 51 Test 01

Description

This test forces a communication adapter IR check (CCOMACK register bit 0) in the following two ways:

- Set the CCOMADI register to X'19', then read another register on the CMCA card. This simulates both W/R gates active.
- Set the CCOMADI register to X'1C', then read another register on the CMCA card. This simulates no W/R gates active.

Parameters:

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

51010D: CCOMACK register indicates an error occurred
510110: Communication adapter IR check did not set (bit 0 of CCOMACK register)
510114: Common check (bit 3 of CSTAT1 register) did not set
510115: CSPRDIC register indicates an error occurred
510116: Communication adapter IR summary check did not set (bit 1 of CSPRDIC register)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 02

Description

This test forces a communication adapter IR check (bit 0 of register CCOMACK) in the following two ways:

- Set CCOMADI register to X'1A' and write to an addressable register on the CMCA card. This simulates a parity check on the IR address bus.
- Set CCOMADI register to X'1B' and write to an addressable register the CMCA card. This simulates a parity check on the IR data bus.

Parameters:

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

51020D: CCOMACK register indicates an error occurred
510210: Communication adapter IR check did not set (bit 0 of CCOMACK register)
510214: Common check (bit 3 of CSTAT1 register) did not set
510215: CSPRDIC register indicates an error occurred
510216: Communication adapter IR summary check did not set (bit 1 of CSPRDIC register)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 03

Description

This test forces a duplicate IR address decode check (bit 4 of CCOMACK register) by setting the CCOMADI register to X'03' and writing to a register on the CMCA card.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

51030D: CCOMACK register indicates an error occurred
510310: CA duplicate IR address decode check (bit 4 of CCOMACK register) did not set
510314: Common check (bit 3 of CSTAT1 register) did not set
510315: CSPRDIC register indicates an error occurred
510316: Communication adapter IR summary check did not set (bit 1 of CSPRDIC register)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 04

Description

This test forces an SD indicator check (bit 7 of CCOMACK register) by setting the CCOMADI register to X'0A'

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

51040D: CCOMACK register indicates an error occurred
510410: SD indicator check (bit 7 of CCOMACK register) did not set
510414: Common check (bit 3 of CSTAT1 register) did not set
510415: CSPRDIC register indicates an error occurred
510416: CSPRDIC register indicates an error occurred after forcing the check

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 05

Description

This test verifies that active inhibit SD reset (bit 3 of CSTAT3 register) is turned on by SP OP Set Inhibit SD Reset and is turned off by SP OP Reset Inhibit SD Reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

510501: Active inhibit SD reset (bit 3 of CSTAT3 register) is on
510509: Active inhibit SD reset (bit 3 of CSTAT3 register) is on and should be reset by SP OP Reset Inhibit SD Reset
51050C: Active inhibit SD reset (bit 3 of CSTAT3 register) is off and should be turned on by SP OP Set Inhibit SD Reset
51050D: CCOMACK register indicates an error occurred
510515: CSPRDIC register indicates an error occurred

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 06

Description

This test verifies that active inhibit SD reset (bit 3 of CSTAT3 register) is turned on by setting SP OP Set Inhibit SD Reset and is turned off when the 28-57 millisecond timer times out. The timer is started when the Special OP is set. It also checks that the timer overflow (bit 4 in CSTAT4 register) is turned on after the timer times out.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

510601: Active inhibit SD reset (bit 3 of CSTAT3 register) is on
510605: Timer overflow (bit 4 of CSTAT4) is on. It should be reset by SP OP Reset Timer Overflow.
510608: Active inhibit SD reset (bit 3 of CSTAT3) is on. It should have reset after 57 milliseconds.
51060A: Timer overflow (bit 4 of CSTAT4) is off
51060B: Active inhibit SD reset (bit 3 of CSTAT3) should still be on. It should stay on for 57 milliseconds.
51060C: Active inhibit SD reset (bit 3 of CSTAT3) did not get set by SP OP Set Inhibit SD Reset
51060D: CCOMACK register indicates an error occurred
51060E: Timer overflow (bit 4 of CSTAT4) is off. It should set after the 57 millisecond timer times out.
510615: CSPRDIC register indicates an error occurred

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 07

Description

This test verifies that a level 2 interrupt will not occur when the device byte count is 64 or greater and the 'cause device gap interrupt bit' (bit 5 of CCTL register) is on. It also verifies that a level 2 interrupt occurs when the device count is less than 64 and the 'cause device gap interrupt bit' (bit 5 of CCTL register) is on. The counter will decrement by one for each diagnostic sync-in issued.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

510701: New level 2 (bit 2 of ILR register) is on
510707: New level 2 (bit 2 of ILR register) should be set after the sync-in
51070D: CCOMACK register indicates an error occurred
510715: CSPRDIC register indicates an error occurred

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 51 Test 08

Description

This test verifies that a level 2 interrupt will not occur when the device byte count is less than 64 and 'cause device gap interrupt bit' (bit 5 of CCTL register) is not on. The count is set to 64 and is decremented once by each diagnostic sync-in.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

510801: New level 2 (bit 2 of ILR register) is on
510807: New level 2 (bit 2 of ILR register) should be set after diagnostic sync-in
51080D: CCOMACK register indicates an error occurred
510815: CSPRDIC register indicates an error occurred

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 5107

Routine 52 Test 01

Description

This test checks the port control IR parity check (bit 5 of CCOMACK register) by forcing a port control IR parity error. A check is also made to ensure that this bit will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

520101: Port control IR parity check (bit 5 of register CCOMACK) will not reset
520102: Port control IR parity check (bit 5 of register CCOMACK) will not set for a parity error on the data bus, while writing to a register
520103: Port control IR parity check (bit 5 of register CCOMACK) will not set for a parity error on the address bus, while writing to a register
520104: Port control IR parity check (bit 5 of register CCOMACK) will not set for a parity error on the address bus, while reading from a register
520106: Port control IR summary check (bit 3 of CSPRDIC register) will not reset
520107: Port control IR summary check (bit 3 of CSPRDIC register) will not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 52 Test 02

Description

This test checks the port control IR read parity check (bit 6 of CCOMACK register) by forcing a port control IR read parity error. A check is made to each leg (CI, SA, and PB) of the checker by writing and reading a register on each card. A check is also made to ensure that this bit will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

520201: Port control IR read parity check (bit 6 of CCOMACK register) will not reset
520206: Port control IR summary check (bit 3 of CSPRDIC register) will not reset
520207: Port control IR summary check (bit 3 of CSPRDIC register) will not set
520208: Port control IR read parity check (bit 6 of CCOMACK register) will not set for a parity error on the data bus

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 52 Test 03

Description

This test checks the port control IR read parity check (bit 5 of CCOMACK register). Data patterns of hex 80, 81, 82, 84, 88, 90, A0, C0, and 7F are written into register X'1B' (WRB) to check for port control IR summary checks (bit 3 of CSPRDIC register) on the address bus.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

520309: Data pattern on the address bus caused a port control IR summary check (bit 3 of CSPRDIC register)
52030A: Data pattern set a port control IR parity check (bit 5 of CCOMACK register)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Diagnostic Tests DC 5204

Routine 52 Test 04

Description

This test checks the port control IR parity check (bit 5 of CCOMACK register). A floating pattern (X'01' to X'80', X'FF') is written into UCTRH register to check for port control IR summary checks in the data bus (CSPRDIC bit 3).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

520409: Data pattern on the data bus caused a port control IR summary check (bit 3 of register CSPRDIC)
52040A: Data pattern caused a port control IR parity check (bit 5 of register CCOMACK)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Data pattern
- E4 = register setting

Note: All other errors are ignored.

Diagnostic Tests DC 5204

Routine 53 Test 01

Description

This test checks the addressability of the upper port byte counter high register (UCTRH). A floating data pattern of hex characters (01,...,80,FF,00) is first written then read and a compare is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530102: Data pattern caused a port control IR summary check (bit 3 of CSPRDIC register)
530103: Writing a data pattern to the UCTRH register caused a control board IR summary check (bit 4 of CSPRDIC)
530105: SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530106: Data pattern received does not equal data pattern expected for UCTRH register

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 02

Description

This test checks the addressability of the upper port byte counter low register (UCTRL). A floating pattern of hex characters (01,...,80,FF,00) is first written then read and a compare is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530202: Data pattern caused a port control IR summary check (bit 3 of register CSPRDIC)
530203: Writing a data pattern to the UCTRL register caused a control board IR summary check (bit 4 of register CSPRDIC)
530205: SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530206: Data pattern received does not equal data pattern expected for UCTRL register .

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 03

Description

This test checks the addressability of the lower port byte counter high register (LCTRH). A floating pattern of hex characters (01,...,80,FF,00) is first written then read and a compare is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530302: Data pattern caused a port control IR summary check (bit 3 of register CSPRDIC)
530303: Writing a data pattern to the LCTRH register caused a control board IR summary check (bit 4 of register CSPRDIC)
530305: SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530306: Data pattern received does not equal data pattern expected for the LCTRH register

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 04

Description

This test checks the addressability of the lower port byte counter low register (LCTRL). A floating data pattern of hex characters (01,...,80,FF,00) is first written then read and a comparison is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530402: Data pattern caused a port control IR summary check (bit 3 of register CSPRDIC)
530403: Writing a data pattern to the LCTRL register caused a control board IR summary check (bit 4 of register CSPRDIC) to set
530405: SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530406: Data pattern received does not equal data pattern expected for LCTRL register.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 05

Description

This test checks the addressability of the upper port buffer diagnostic register (UPBDI). A floating data pattern of hex characters (01,...,80,FF,00) is first written then read and a comparison is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530502: Data pattern caused a port control IR summary check (bit 3 of register CSPRDIC)
530503: Writing a data pattern to the UPBDI register caused a control board IR summary check (bit 4 of register CSPRDIC) to set
530505: SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530506: Data pattern received does not equal data pattern expected for UPBDI register

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 06

Description

This test checks the addressability of the lower port buffer diagnostic register (LPBDI). A floating data pattern of hex characters (01,...,80,FF,00) is first written then read and a comparison is made on each data pattern for any data errors.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern

Isolation Codes

530602: Data pattern caused a port control IR summary check (bit 3 of register CSPRDIC)
530603: Writing a data pattern to the LPBDI register caused a control board IR summary check (bit 4 of register CSPRDIC)
530605 SP OP read IR checks register (CSPRDIC) did not reset (bits 3 and 4)
530606: Data pattern received does not equal Data pattern expected for LPBDI register

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CCOMACK register
- E6 = CSACK register

Note: All other errors are ignored.

Routine 53 Test 07

Description

This test checks the upper port byte counter high and low shadow registers (UCTRHS UCTRLS) for addressability, and proper initialization to a multiple of sixteen. This test is executed twice with a floating data pattern; first with SRC off, second with SRC on.

Byte counter low shadow data pattern hex characters:

(0000, 0001, 0002, 0004, 0008, 0010, 0020, 0040, 0080, 00FF)

Byte counter high shadow data pattern hex characters:

(00FF, 01FF, 02FF, 04FF, 08FF, 10FF, 20FF, 40FF, 80FF, FFFF)

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

530708: UCTRHS and UCTRLS registers are not as expected with SRC OFF
530709: UCTRHS and UCTRLS registers are not as expected with SRC ON

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data - UCTRHS
- E4 = Expected data - UCTRLS
- E5 = Received data - UCTRHS
- E6 = Received data - UCTRLS

Routine 53 Test 08

Description

This test checks the lower port byte counter high and low shadow registers (LCTRHS/LCTRLS) for addressability, and proper initialization to a multiple of sixteen. This test is executed twice with a floating data pattern; first with SRC off, second with SRC on.

Byte counter low shadow data pattern hex characters:

(0000,0001,0002,0004,0008,0010,0020,0040,0080,00FF)

Byte counter high shadow data pattern hex characters:

(00FF,01FF,02FF,04FF,08FF,10FF,20FF,40FF,80FF,FFFF)

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

530808: LCTRHS and LCTRLS registers are not as expected with SRC OFF
530809: LCTRHS and LCTRLS registers are not as expected with SRC ON

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data - LCTRHS
- E4 = Expected data - LCTRLS
- E5 = Received data - LCTRHS
- E6 = Received data - LCTRLS

Routine 54 Test 01

Description

This test first checks that the SSAR registers can be loaded correctly. Then it sets the test loop write to read port buffer and uses a byte count of 127 on a store and fetch to check that the SRC bytes can be split across the two port buffer arrays with no errors (upper port).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540103: SSAR registers did not load correctly
540181: SRC check after a 127-byte fetch operation
5401E0: No data transfer complete after a microcode delay on a store operation
5401E1: No data transfer complete after a microcode delay on a fetch operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 02

Description

This test first checks that the SSAR registers can be loaded correctly. Then it sets the test loop write to read port buffer and uses a byte count of 127 on a store and fetch to check that the SRC bytes can be split across the two port buffer arrays with no errors (lower port).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540203: SSAR registers did not load correctly
540281: SRC check after a 127-byte fetch operation
5402E0: No data transfer complete after a microcode delay on a store operation
5402E1: No data transfer complete after a microcode delay on a fetch operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 03

Description

This test checks the setting and resetting of the upper port P/B overrun/underrun check (bit 0 of register UPBCK).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540303: Upper port overrun check (bit 0 of register UPBCK) is not on
540304: Upper port buffer check register will not reset
54031F: Overrun check (bit 0 of register UPBCK) sets with one byte less than it should
5403B0: Upper port check (bit 0 of register CSTAT1) will not set after setting the port buffer check register (UPBCK)
5403E0: Data transfer complete did not set after a microcode delay on a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Diagnostic Tests DC 5401

Routine 54 Test 04

Description

This test checks the setting and resetting of the lower port P/B overrun check (bit 0 of register LPBCK).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540403: Overrun check (bit 0 of register LPBCK) is off
540404: Lower port buffer check register (LPBCK) will not reset
54041F: Overrun check (bit 0 of register LPBCK) sets with one byte less than it should
5404B0: Lower port check (bit 1 of register CSTAT1) will not set after setting the port buffer check register (LPBCK)
5404E0: Data transfer complete (bit 7 of register CSTAT1) did not set after a microcode delay store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 05

Description

This test checks that the upper port byte counter zero check (bit 1 of register UPBCK) and the upper port byte counter parity check (bit 3 of register UPBCK) will set. A check is also made to ensure that these bits will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540504: Upper port buffer check register (UPBCK) will not reset
540508: Byte counter parity check (bit 3 of register UPBCK) did not set
54052D: Byte count zero check (bit 1 of register UPBCK) will not set
5405B0: Upper port check (bit 0 of register CSTAT1) will not set after setting the port buffer check register (UPBCK)
5405E0: Data transfer complete (bit 6 of register CSTAT1) did not set after a microcode delay

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 06

Description

This test checks that the lower port byte counter zero check (bit 1 of register LPBCK) and the lower port byte counter parity check (bit 3 of register LPBCK) will set. A check is also made to ensure that these bits will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540604: Lower port buffer check register (LPBCK) will not reset
540608: Byte counter parity check (bit 3 of register LPBCK) did not set
54062D: Byte count zero check (bit 1 of register LPBCK) will not set
5406B0: Lower port check (bit 1 of register CSTAT1) will not set after setting the port buffer check register (LPBCK)
5406E0: Data transfer complete (bit 7 of register CSTAT1) did not set after a microcode delay

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 07

Description

This test checks that the upper port PA/PB data in parity check (bit 5 of register UPBCK) will set. A check is also made to ensure that this bit will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540704: Upper port buffer check register (UPBCK) will not reset
54072C: PA/PB data in parity check (bit 5 of register UPBCK) did not set
5407B0: Upper port check (bit 0 of register CSTAT1) will not set after setting the port buffer check register (UPBCK)
5407E0: Data transfer complete (bit 6 of register CSTAT1) did not set after a microcode delay

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 08

Description

This test checks that the lower port PA/PB data in parity check (bit 5 of register LPBCK) will set. A check is also made to ensure that this bit will reset to zero.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540804: Lower port buffer check register (LPBCK) will not reset
54082C: PA/PB data in parity check (bit 5 of register LPBCK) did not reset
5408B0: Lower port check (bit 1 of register CSTAT1) will not set after setting the port buffer check register (LPBCK)
5408E0: Data transfer complete (bit 7 of register CSTAT1) did not set after a microcode delay

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 54 Test 09

Description

This test checks the upper port ECC/PB data in parity check 1 and ECC/PB data in parity check 2 (bits 6 and 7 of register UPBCK). These bits are checked to ensure that they can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'09' Run only test 09

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540904: Upper port buffer check register (UPBCK) will not reset
540905: ECC/PB data in parity check 1 (bit 6 of register UPBCK) did not set
540906: ECC/PB data in parity check 2 (bit 7 of register UPBCK) did not set
5409B0: Upper port check (bit 0 of register CSTAT1) will not set after setting the port buffer check register (UPBCK)
5409E0: Data transfer complete (bit 6 of register CSTAT1) did not set after a microcode delay on a store operation
5409E1: Data transfer complete (bit 6 of register CSTAT1) did not set after a microcode delay on a fetch operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Diagnostic Tests DC 540A

Routine 54 Test 0A

Description

This test checks the lower port ECC/PB data in parity check 1 and ECC/PB data in parity check 2 (bits 6 and 7 of register LPBCK). These bits are checked that they can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0A' Run only test 0A

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

540A04: Lower port buffer check register (LPBCK) will not reset
540A05: ECC/PB data in parity check 1 (bit 6 of register LPBCK) did not set
540A06: ECC/PB data in parity check 2 (bit 7 of register LPBCK) did not set
540AB0: Lower port check (bit 1 of register CSTAT1) will not set after setting the port buffer check register (LPBCK)
540AE0: Data transfer complete (bit 7 of register CSTAT1) did not set after a microcode delay on a store operation
540AE1: Data transfer complete (bit 7 of register CSTAT1) did not set after a microcode delay on a fetch operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Diagnostic Tests DC 540A

Routine 55 Test 01

Description

This test checks the upper port buffer addressability. Each byte location is loaded with a different incremented data pattern, then each byte location is loaded with a different decremented data pattern.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550101: Data received is not equal to the data expected
550103: CSTAT1 register will not reset (bits 2 and 3 not checked)
5501E0: No Data Transfer Complete on a store
5501E1: No Data Transfer Complete on a fetch
5501F0: Port Check on a store
5501F1: Port Check on a fetch

Error Display Bytes

Error Code: 550101

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Port Buffer Address

Error Codes: 550103 - 5501F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 02

Description

This test checks the lower port buffer addressability. Each byte location is loaded with a different incremented data pattern, then each byte location is loaded with a different decremented data pattern.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550201: Data received is not equal to the data expected
550203: CSTAT1 register will not reset (bits 2 and 3 not checked)
5502E0: No Data Transfer Complete on a store
5502E1: No Data Transfer Complete on a fetch
5502F0: Port Check on a store
5502F1: Port Check on a fetch

Error Display Bytes

Error Code: 550201

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Port Buffer Address

Error Codes: 550203 - 5502F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 03

Description

This test checks the data integrity of the upper port buffer. The following data patterns are used: X'00', X'FF', and X'34'.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550301: Data received is not equal to the data expected
550303: CSTAT1 register will not reset (bits 2 and 3 not checked)
5503E0: No Data Transfer Complete on a store
5503E1: No Data Transfer Complete on a fetch
5503F0: Port Check on a store
5503F1: Port Check on a fetch

Error Display Bytes

Error Code: 550301

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Port Buffer Address

Error Codes: 550303 - 5503F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 04

This test checks the data integrity of the lower port buffer. The following patterns are used: X'00', X'FF', and X'34'.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550401: Data received is not as expected
550403: CSTAT1 register will not reset (bits 2 and 3 not checked)
5504E0: No Data Transfer Complete on a store
5504E1: No Data Transfer Complete on a fetch
5504F0: Port check on a store
5504F1: Port check on a fetch

Error Display Bytes

Error Code: 550401

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Port Buffer Address

Error Codes: 550403 - 5504F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 05

Description

This test checks the upper port storage redundancy check (SRC) (bit 1 of register UPACK). The generation of the SRC bytes is done on the CMCD card.

- Variable data patterns are stored into the port buffer then fetched back. These patterns are selected so that each of the SRC bits are toggled on and off.
- The Inhibit SRC function is also checked.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550503: CSTAT1 register will not reset (bits 2 and 3 not checked)
550505: The received SRC does not equal the expected value
550507: SRC check bit set with no SRC error
550508: SRC bytes were generated with Inhibit SRC on
5505E0: No Data Transfer Complete on a store
5505E1: No Data Transfer Complete on a fetch
5505F0: Port check on a store
5505F1: Port check on a fetch

Error Display Bytes

Error Code: 550505

- E1 = Test ID
- E2 = Error Code
- E3 = Expected SRC Byte 0
- E4 = Expected SRC Byte 1
- E5 = Received SRC Byte 0
- E6 = Received SRC Byte 1

Error Codes: 550503, 550507 - 5505F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 06

Description

This test checks the lower port storage redundancy check (SRC) (bit 1 of register LPACK). The generation of the SRC bytes is done on the CMCD card.

- Variable data patterns are stored into the port buffer then fetched back. These patterns are selected so that each of the SRC bits are toggled on and off.
- The Inhibit SRC function is also checked.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550603: CSTAT1 register will not reset (bits 2 and 3 not checked)
550605: The received SRC does not equal the expected value
550607: SRC check bit set with no SRC error
550608: SRC bytes were generated with Inhibit SRC on
5506E0: No Data Transfer Complete on a store
5506E1: No Data Transfer Complete on a fetch
5506F0: Port check on a store
5506F1: Port check on a fetch

Error Display Bytes

Error Code: 550605

- E1 = Test ID
- E2 = Error Code
- E3 = Expected SRC byte 0
- E4 = Expected SRC byte 1
- E5 = Received SRC byte 0
- E6 = Received SRC byte 1

Error Codes: 550603, 550607 - 5506F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 07

Description

This test checks the upper port SRC Accumulate function on a store operation, two store operations, and one fetch operation. The SRC data values are then compared to the expected SRC data values.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550703: CSTAT1 register will not reset (bits 2 and 3 not checked)
550709: The received SRC is not equal to the expected value
5507E0: No Data Transfer Complete on a store operation
5507E1: No Data Transfer Complete on a fetch operation
5507F0: Upper Port Check on a store operation
5507F1: Upper Port Check on a fetch operation

Error Display Bytes

Error Code: 550709

- E1 = Test ID
- E2 = Error Code
- E3 = Expected SRC Byte 0
- E4 = Expected SRC Byte 1
- E5 = Received SRC Byte 0
- E6 = Received SRC Byte 1

Error Codes: 550703, 5507D0 - 5507F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 08

Description

This test checks the lower port SRC Accumulate function on a store operation, two store operations, and one fetch operation. The SRC data values are then compared to the expected SRC data values.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550803: CSTAT1 register will not reset (bits 2 and 3 not checked)
550809: The received SRC is not equal to the expected value
5508E0: No Data Transfer Complete on a store operation
5508E1: No Data Transfer Complete on a fetch operation
5508F0: Lower Port Check on a store operation
5508F1: Lower Port Check on a fetch operation

Error Display Bytes

Error Code: 550809

- E1 = Test ID
- E2 = Error Code
- E3 = Expected SRC Byte 0
- E4 = Expected SRC Byte 1
- E5 = Received SRC Byte 0
- E6 = Received SRC Byte 1

Error Codes: 550803, 5508D0 - 5508F1

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Note: All other errors are ignored.

Routine 55 Test 09

Description

This test checks that the read clock delayed bit (bit 5 of the CPACK1 register) will set and then reset. A check is first made to ensure that the bit is reset, then an invalid register address is written. The bit is checked for being set. A reset is performed to remove the check and the bit is checked for being off.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'09' Run only test 09

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

550902: Read clock delayed did not reset with a SD check reset
550903: Read clock delayed did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Expected data
- E4 = Received data

Note: All other errors are ignored.

Routine 56 Test 01

Description

This test checks that the upper port buffer can read a diagnostic word from the four words that have been reserved by the functional microcode in subsystem storage. Fourteen data bytes of X'DEAD' should be stored at a reserved cache location. This data was set by an IML.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

560101: CSPRDIC register is not zero when reading GSSCIN register
560102: Diagnostic word addresses not initialized
560103: Diagnostic word compare incorrect
560106: Diagnostic mode switches not set/correct
5601A0: IR check on a transfer
5601B0: Communication, common check, or unsupported check 2
5601D1: Port check with Op Complete on a fetch
5601E1: No check, no Op Complete on a fetch
5601F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Codes: 560101 - 560106

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error

Error Code: 5601A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR check (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common storage addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 5601B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cable out (GSSCIN)

Error Codes: 5601D1, 5601F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' check registers are upper port
  X'80' check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (UPACK)
- E6 = Port buffer ck (UPBCK)
- E7 = SSAR0 (USSAR0)
- E8 = SSAR1 (USSAR1)
- E9 = SSAR2 (USSAR2)
- EA = Storage adapt ck (USADPCK)
- EB = Storage card addr ck (USCACK)
- EC = ECC ck (UECCCK)
- ED = Storage control ck (USCCK)

Error Code: 5601E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Diagnostic Tests DC 5601

Routine 56 Test 02

Description

This test checks that the lower port buffer can read a diagnostic word from the four words in subsystem storage that have been reserved by the functional microcode. Fourteen data bytes of X'DEAD' should be stored at a reserved cache location. This data was set by an IML.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

560201: CSPRDIC register not zero when reading GSSCIN register
560202: Diagnostic word addresses not initialized
560203: Diagnostic word compare not correct
560206: Diagnostic mode switches not set/correct
5602A0: IR check on a transfer
5602B0: Communication, common check, or an unsupported check 2
5602D1: Port check with Op Complete on a fetch
5602E1: No check, no Op Complete on a fetch
5602F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Codes: 560201 - 560203

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error

Error Code: 5602A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR cks (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 5602B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cable out (GSSCIN)

Error Codes: 5602D1, 5602F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - Check registers are upper port
  X'80' - Check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Code: 5602E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Diagnostic Tests DC 5602

Routine 56 Test 03

Description

This test checks the upper port buffer data path to an error-free cache location on a storage board. Four data patterns are alternately written to the first good cache location. The cache location (16 data bytes) is read back and verified after each store operation. The data patterns used are:

First Pass	X'00'
Second Pass	X'55'
Third Pass	X'AA'
Last Pass	X'FF'

The data pattern may be selected by inserting a non-zero data pattern in parameter byte 3. The diagnostic word used is restored before exiting the test if looping was not selected.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test

Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected non-zero data pattern

Isolation Codes

560301: CSPRDIC register not zero when reading GSSCIN register
560302: Diagnostic word addresses not initialized
560303: Diagnostic word compare not correct
560305: Upper port data integrity error when writing a storage board diagnostic word
560306: Diagnostic mode switches not set/correct
5603A0: IR check on a transfer
5603B0: Communication, common check, or unsupported check 2
5603D0: Port check with Op Complete on a store
5603D1: Port check with Op Complete on a fetch
5603E0: No check, no Op Complete on a store
5603E1: No check, no Op Complete on a fetch
5603F0: Port check and no Op Complete on a store
5603F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Codes: 560301 - 560306

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error

Error Code: 5603A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common Port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 5603B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cable out (GSSCIN)

Error Codes: 5603D0, 5603D1, 5603F0, 5603F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (UPACK)
- E6 = Port buffer ck (UPBCK)
- E7 = SSAR0 (USSAR0)
- E8 = SSAR1 (USSAR1)
- E9 = SSAR2 (USSAR2)
- EA = Storage adapt ck (USADPCK)
- EB = Storage card addr ck (USCACK)
- EC = ECC ck (UECCCK)
- ED = Storage control ck (USCCK)

Error Codes: 5603E0, 5603E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 56 Test 04

Description

This test checks the lower port buffer data path to an error-free cache location on a storage board. Four data patterns are alternately written to the first good cache location. The cache location (16 data bytes) is read back and verified after each store operation. The data patterns used are:

First Pass X'00'
Second Pass X'55'
Third Pass X'AA'
Last Pass X'FF'

The data pattern may be selected by inserting a non-zero data pattern in parameter byte 3. The diagnostic word used is restored before exiting the test if looping was not selected.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected non-zero data pattern

Isolation Codes

560401: CSPRDIC register not zero when reading GSSCIN register
560402: Diagnostic word addresses not initialized
560403: Diagnostic word compare not correct
560405: Lower port data integrity error writing a storage board diagnostic word
560406: Diagnostic mode switches not set/correct
5604A0: IR check on a transfer
5604B0: Communication, common check, or unsupported check 2
5604D0: Port check with Op Complete on a store
5604D1: Port check with Op Complete on a fetch
5604E0: No check, no Op Complete on a store
5604E1: No check, no Op Complete on a fetch
5604F0: Port check and no Op Complete on a store
5604F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Codes: 560401 - 560406

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error

Error Code: 5604A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR cks (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 5604B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cable out (GSSCIN)

Error Codes: 5604D0, 5604D1, 5604F0, 5604F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Codes: 5604E0, 5604E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 56 Test 05

Description

This test checks that the check 2 circuitry is operating correctly. An upper port buffer check is set, then the upper port check and check2 are checked for being set. Run is dropped, then check2 is checked to ensure that it is off.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

560501: Upper port check bit did not reset
560502: Upper port buffer check register (UPBCK) did not reset
560503: Check2 (bit 0 of the XCS register) did not reset
560504: Data transfer complete bit did not get set
560505: Byte count equal zero (bit 1 of the UPBCK register) did not set
560506: Upper port check bit did not set
560507: Check2 bit did not set
560508: Check2 bit (bit 0 of the XCS register) is set with STG run off

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 56 Test 06

Description

This test checks that the check 2 circuitry is operating correctly. An upper port buffer check is set, then the lower port check and check2 are checked for being set. Run is dropped, then check2 is checked to ensure that it is off.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

560601: Lower port check bit did not reset
560602: Lower port buffer check register (LPBCK) did not reset
560603: Check2 (bit 0 of the XCS register) did not reset
560604: Data transfer complete bit did not get set
560605: Byte count equal zero (bit 1 of the LPBCK register) did not set
560606: Lower port check bit did not set
560607: Check2 bit did not set
560608: Check2 bit (bit 0 of the XCS register) is set with STG run off

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 56 Test 07

Description

This test checks that the check 2 circuitry is operating correctly. An error is forced on the storage address card. Common check and check2 are checked for being set. Run is dropped, then check2 is checked to ensure that it is off.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

560701: Common check bit did not reset
560702: Storage address common check register (CSACK) did not reset
560703: Check2 (bit 0 of the XCS register) did not reset
560705: Upper port buffer IR check (bit 2 of the CSACK register) did not set
560706: Common check bit did not set
560707: Check2 bit did not set
560708: Check2 bit (bit 0 of the XCS register) is set with STG run off

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 57 Test 01

Description

This test checks that byte zero of the upper port SSAR (USAR0) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal patterns
X'xx' Selected data pattern

Isolation Codes

570101: Read operation of upper port high order byte SSAR (USARO) did not compare with a write operation
570102: Controlled machine reset (bit 2 of register CCTL) did not reset register USARO
570103: CSPRDIC register indicates an error after a write operation
570104: CSPRDIC register indicates an error after a read operation
570115: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570101 - 570104

- E1 = Test ID
- E2 = Error code
- E3 = Expected USAR0 register
- E4 = Received USAR0 register
- E5 = CSPRDIC register

Error Code: 570115

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 02

Description

This test checks that byte one of the upper port SSAR (USAR1) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570201: Read operation of upper port SSAR1 register (USAR1) did not compare with write operation
570202: Controlled machine reset (bit 2 of register CCTL) did not reset register USAR1
570203: CSPRDIC register indicates an error after a write operation
570204: CSPRDIC register indicates an error after a read operation
570215: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570201 - 570204

- E1 = Test ID
- E2 = Error code
- E3 = Expected data USAR1 register
- E4 = Received data USAR1 register
- E5 = CSPRDIC register

Error Code: 570215

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 03

Description

This test checks that byte two of the upper port SSAR (USAR2) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570301: Read operation of upper port SSAR2 register (USAR2) did not compare with write operation
570302: Controlled machine reset (bit 2 of register CCTL) did not reset register USAR2
570303: CSPRDIC register indicates an error after a write operation
570304: CSPRDIC register indicates an error after a read operation
570315: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570301 - 570304

- E1 = Test ID
- E2 = Error code
- E3 = Expected data USAR2 register
- E4 = Received data USAR2 register
- E5 = CSPRDIC register

Error Code: 570315

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 04

Description

This test checks that byte zero of lower port SSAR (LSAR0) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570401: Read of lower port register (LSAR0) did not agree with write operation
570402: Controlled machine reset (bit 2 of register CCTL) did not reset register LSAR0
570403: CSPRDIC register indicates an error after a write operation
570404: CSPRDIC register indicates an error after a read operation
570415: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570401 - 570404

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LSAR0 register
- E4 = Received data LSAR0 register
- E5 = CSPRDIC register

Error Code: 570415

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 05

Description

This test checks that byte one of the lower port SSAR register (LSAR1) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570501: Read operation of lower port SSAR register (LSAR1) did not agree with write operation
570502: Controlled machine reset (bit 2 of register CCTL) did not reset register LSAR1
570503: CSPRDIC register indicates an error after a write operation
570504: CSPRDIC register indicates an error after a read operation
570515: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570501 - 570504

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LSAR1 register
- E4 = Received data LSAR1 register
- E5 = CSPRDIC register

Error Code: 570515

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 06

Description

This test checks that byte one of the lower port SSAR register (LSAR2) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570601: Read operation of lower port SSAR register (LSAR2) did not agree with write operation
570602: Controlled machine reset (bit 2 of register CCTL) did not reset register LSAR2
570603: CSPRDIC register indicates an error after a write operation
570604: CSPRDIC register indicates an error after a read operation
570615: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570601 - 570604

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LSAR2 register
- E4 = Received data LSAR2 register
- E5 = CSPRDIC register

Error Code: 570615

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 07

Description

This test checks that the upper port OP/CTL shadow register (UOPCTLS) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570701: Read operation of upper port OP/CTL shadow register (UOPCTLS) did not agree with the write operation
570702: Controlled machine reset (bit 2 of register CCTL) did not reset register UOPCTLS
570703: CSPRDIC register indicates an error after an write operation
570704: CSPRDIC register indicates an error after an read operation
570715: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570701 - 570704

- E1 = Test ID
- E2 = Error code
- E3 = Expected data UOPCTLS register
- E4 = Received data UOPCTLS register
- E5 = CSPRDIC register

Error Code: 570715

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 08

Description

This test checks that the lower port OP/CTL shadow register (LOPCTLS) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'08' Run only test 08

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570801: Read operation of lower port OP/CTL shadow register (LOPCTLS) did not agree with the write operation
570802: Controlled machine reset (bit 2 of register CCTL) did not reset register LOPCTLS
570803: CSPRDIC register indicates an error after an write operation
570804: CSPRDIC register indicates an error after an read operation
570815: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570801 - 570804

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LOPCTLS register
- E4 = Received data LOPCTLS register
- E5 = CSPRDIC register

Error Code: 570815

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 09

Description

This test checks that the upper port control shadow register (UCTLS) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'09' Run only test 09

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570901: Read operation of upper port shadow register (UCTLS) did not agree with the write operation
570902: Controlled machine reset (bit 2 of register CCTL) did not reset register UCTLS
570903: CSPRDIC register indicates an error after an write operation
570904: CSPRDIC register indicates an error after an read operation
570915: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570901 - 570904

- E1 = Test ID
- E2 = Error code
- E3 = Expected data UCTLS register
- E4 = Received data UCTLS register
- E5 = CSPRDIC register

Error Code: 570915

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 0A

Description

This test checks that the lower port control shadow register (LCTLS) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) Run all tests in this routine
X'0A' Run only test 0A

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570A01: Read operation of lower port control shadow register (LCTLS) did not agree with the write operation
570A02: Controlled machine reset (bit 2 of register (CCTL) did not reset register LCTLS
570A03: CSPRDIC register indicates an error after after a write operation
570A04: CSPRDIC register indicates an error after after a read operation
570A15: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570A01 - 570A04

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LCTLS register
- E4 = Received data LCTLS register
- E5 = CSPRDIC register

Error Code: 570A15

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 0B

Description

This test checks that the common storage address diagnostic register (CSADI) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0B' Run only test 0B

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

570B01: Read operation of storage address diagnostic register (CSADI) not agree with the write operation
570B02: Controlled machine reset (bit 2 of register (CCTL) did not reset register CSADI
570B03: CSPRDIC register indicates an error after after a write operation
570B04: CSPRDIC register indicates an error after after a read operation
570B15: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 570B01 - 570B04

- E1 = Test ID
- E2 = Error code
- E3 = Expected data CSADI register
- E4 = Received data CSADI register
- E5 = CSPRDIC register

Error Code: 570B15

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 0C

Description

This test checks that the read only registers located on the CMSA card can be read without causing an error and also no bits remain on following a reset. The registers involved are USADPCK, LSADPCK, CSTAT1, CMADEC, CSACK, CSARCK, CSCCK, CSRACK, USCCK, LSCCK, USCACK, LSCACK, USCCCK, AND LSCCCK.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0C' Run only test 0C

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

570C08: IR summary check on after reading the USCCK register
570C09: Upper storage control ck did not reset to 0
570C18: IR summary check on after reading the LSCCK register
570C19: Lower storage control ck did not reset to 0
570C28: IR summary check on after reading the USCACK register
570C29: Upper storage card addr ck did not reset to 0
570C38: IR summary check on after reading the LSCACK register
570C39: Lower storage card addr ck did not reset to 0
570C48: IR summary check on after reading the CSCCK register
570C49: Common storage control ck did not reset to 0
570C50: IR summary check on after reading the USADPCK register
570C51: Upper storage adapter ck did not reset to 0
570C58: IR summary check on after reading the CSCRACK register
570C59: Common stg card refresh addr ck did not reset to 0
570C60: IR summary check on after reading the LSADPCK register
570C61: Lower storage adapter ck did not reset to 0
570C70: IR summary check on after reading the CSTAT1 register
570C71: Common status 1 did not reset to 0
570C80: IR summary check on after reading the CMADEC register
570C81: Multiple address decode did not reset to 0
570C88: IR summary check on after reading the UECCCK register
570C89: Upper ECC ck did not reset to 0
570C90: IR summary check on after reading the CSACK register
570C91: Common storage address ck did not reset to 0
570C98: IR summary check on after reading the LECCCK register
570C99: Lower ECC ck did not reset to 0
570CA0: IR summary check on after reading the CSARCK register
570CA1: Common storage refresh ck did not reset to 0
570CA8: IR summary check on after reading the GECCCK1 register
570CA9: ECC check byte 1 did not reset to 0
570CB8: IR summary check on after reading the GECCCK2 register
570CB9: ECC check byte 2 did not reset to 0
570CC8: IR summary check on after reading the GSYN1 register
570CC9: ECC syndrome byte 1 did not reset to 0
570CD8: IR summary check on after reading the GSYN2 register
570CD9: ECC syndrome byte 2 did not reset to 0
570CE8: IR summary check on after reading the GIDSW or GSSCIN register
570CF8: IR summary check on after reading the CSTAT2 register
570CF9: Common status 2 did not reset

Error Display Bytes

Error Codes: 570C08 - 570CE9

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = CSPRDIC register

Routine 57 Test 0D

Description

This test verifies that the PB overrun/underrun check bit in the upper port buffer check register (UPBCK) can be set and reset. It sets up conditions that force the bit to go on and off and verifies that it does.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0D' Run only test 0D

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

570D01: Bit under test in the UPBCK register did not set
570D04: Upper ck reset did not reset the UPBCK register
570D09: Upper port check off

Error Display Bytes

Error Code: 570D01 - 570D05

- E1 = Test ID
- E2 = Error code
- E3 = Expected data in the UPBCK register
- E4 = Received data in the UPBCK register

Error Code: 570D09 - 570D0B

- E1 = Test ID
- E2 = Error code
- E3 Common status 1 (CSTAT1)
- E4 = Port adapt ck (UPACK)
- E5 = Port buffer ck (UPBCK)
- E6 = ECC ck (UECCCK)
- E7 = Storage control ck (USCCK)
- E8 = Storage card addr ck (USCACK)
- E9 = Storage adapt ck (USADPCK)

Routine 57 Test 0E

Description

This test verifies that the PB overrun/underrun check bit in the lower port buffer check register (LPBCK) can be set and reset. It sets up conditions that force the bit to go on and off and verifies that it does.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0E' Run only test 0E

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

570E01: Bit under test in the LPBCK register did not set
570E04: Lower ck reset did not reset the LPBCK register
570E09: Lower port check off

Error Display Bytes

Error Code: 570E01 - 570E05

- E1 = Test ID
- E2 = Error code
- E3 = Expected LPBCK
- E4 = Received LPBCK

Error Code: 570E057

- E1 = Test ID
- E2 = Error code
- E3 = Expected UPBCK
- E4 = Received UPBCK

Error Code: 570E09 - 570E0B

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Port adapt ck (LPACK)
- E5 = Port buffer ck (LPBCK)
- E6 = ECC ck (LECCCK)
- E7 = Storage control ck (LSCCK)
- E8 = Storage card addr ck (LSCACK)
- E9 = Storage adapt ck (LSADPCK)

Routine 57 Test 0F

Description

This test verifies that the test and set register on the CMC1 card can be set, and the same data can be obtained on a reread.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'0F' Run only test 0F

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

570F01: Read of test and set register did not agree with write
570F02: CMR did not reset the test and set register
570F03: IR summary check on after a write
570F04: IR summary check on after a read
570F05: Test and set bit (bit 2 of the CSTAT1 register) was off
570F06: Test and set bit (bit 2 of the CSTAT1 register) was on
570F15: Writeable register unexpectedly non-zero

Error Display Bytes

Error Code: 570F01 - 570F05

- E1 = Test ID
- E2 = Error code
- E3 = Expected Test and Set register
- E4 = Received Test and Set register
- E5 = CSPRDIC register

Error Code: 570F15

- E1 = Test ID
- E2 = Error code
- E3 = Unused
- E4 = Received non-zero register contents
- E4 = Address of unexpected non-zero register

Routine 57 Test 10

Description

This test checks that the general microcode (GMIC) register can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) Run all tests in this routine
X'10' Run only test 10

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571001: Read operation of general microcode register (GMIC) did not agree with the write operation
571002: Controlled machine reset (bit 2 of register (CCTL) did not reset register GMIC
571003: CSPRDIC register indicates an error after after a write operation
571004: CSPRDIC register indicates an error after after a read operation
571015: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571001 - 571004

- E1 = Test ID
- E2 = Error code
- E3 = Expected data GMIC register
- E4 = Received data GMIC register
- E5 = CSPRDIC register

Error Code: 571015

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 11

Description

This test checks that the general diagnostic register (GDI) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'11' Run only test 11

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571101: Read operation of general diagnostic register (GDI) did not agree with the write operation
571102: Controlled machine reset (bit 2 of register (CCTL) did not reset register GDI
571103: CSPRDIC register indicates an error after after a write operation
571104: CSPRDIC register indicates an error after after a read operation
571115: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571101 - 571104

- E1 = Test ID
- E2 = Error code
- E3 = Expected data GDI register
- E4 = Received data GDI register
- E5 = CSPRDIC register

Error Code: 571115

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 12

Description

This test checks that the ECC diagnostic register (GECCDI) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'12' Run only test 12

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571201: Read operation of the ECC diagnostic register (GDI) did not agree with the write operation
571202: Controlled machine reset (bit 2 of register (CCTL) did not reset register GECCDI
571203: CSPRDIC register indicates an error after after a write operation
571204: CSPRDIC register indicates an error after after a read operation
571215: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571201 - 571204

- E1 = Test ID
- E2 = Error code
- E3 = Expected data GECCDI register
- E4 = Received data GECCDI register
- E5 = CSPRDIC register

Error Code: 571215

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 13

Description

This test checks that the write check 1 register (GWRCK1) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'13' Run only test 13

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571301: Read operation of the write check 1 register (GWRCK1) did not agree with the write operation
571302: Controlled machine reset (bit 2 of register CCTL) did not reset register GWRCK1
571303: CSPRDIC register indicates an error after after a write operation
571304: CSPRDIC register indicates an error after after a read operation
571315: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571301 - 571304

- E1 = Test ID
- E2 = Error code
- E3 = Expected data GWRCK1 register
- E4 = Received data GWRCK1 register
- E5 = CSPRDIC register

Error Code: 571315

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 14

Description

This test checks that the write check 2 register (GWRCK2) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'14' Run only test 14

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571401: Read operation of the write check 2 register (GWRCK2) did not agree with the write operation
571402: Controlled machine reset (bit 2 of register (CCTL) did not reset register GWRCK2
571403: CSPRDIC register indicates an error after after a write operation
571404: CSPRDIC register indicates an error after after a read operation
571415: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571401 - 571404

- E1 = Test ID
- E2 = Error code
- E3 = Expected data GWRCK2 register
- E4 = Received data GWRCK2 register
- E5 = CSPRDIC register

Error Code: 571415

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 15

Description

This test checks that the common shadow control register (CCTLS) can be set and the same data obtained on the read operation.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'15' Run only test 15

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571501: Read operation of the common shadow control (CCTLS) did not agree with the write operation
571502: Controlled machine reset (bit 2 of register (CCTL) did not reset register CCTLS
571503: CSPRDIC register indicates an error after after a write operation
571504: CSPRDIC register indicates an error after after a read operation
571515: Writeable register on SA card is not zero

Error Display Bytes

Error Codes: 571501 - 571504

- E1 = Test ID
- E2 = Error code
- E3 = Expected data CCTLS register
- E4 = Received data CCTLS register
- E5 = CSPRDIC register

Error Code: 571515

- E1 = Test ID
- E2 = Error code
- E3 = Zero
- E4 = Received register
- E5 = Address of register

Routine 57 Test 16

Description

This test verifies that any bit on in the microcode register (GMIC) will cause bit 5 of CSTAT2 register to be on.

Parameters

Byte 1

X'00' (default) Run all tests in this routine
X'16' Run only test 16

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571601: Common status register bit 5 not on with nonzero GMIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = GMIC contents
- E4 = CSTAT2 contents

Routine 57 Test 17

Description

This test verifies that storage size/cables in register (GSSCIN) is set to a valid combination.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'17' Run only test 17

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Run normal data patterns
X'xx' Selected data pattern

Isolation Codes

571705: Storage board 1 cables out
571706: Diagnostic mode switch off
571707: Invalid storage size
571708: Storage board 2 cables out indicator and storage size do not agree
571709: Storage board 2 power is off

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = GSSCIN contents
- E4 = CSTAT5 contents

Routine 58 Test 01

Description

This test verifies that the error check bits in the upper storage adapter check register (USADPCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

580101: Bit under test in USADPCK register did not set
580103: Check 2 (bit 0 of the XCS register) is on
580104: Upper port check reset (bit 1 of register UCTL) did not reset register USADPCK
580105: Bit in USADPCK register should not be on
580107: LSADPCK is not as expected while testing upper port
580109: Upper port check (bit 0 of register CSTAT1) is off
58010B: Check 2 (bit 0 of register XCS) off

Error Display Bytes

Error Codes: 580101 - 580105

- E1 = Test ID
- E2 = Error code
- E3 = Expected data USADPCK register
- E4 = Received data USADPCK register

Error Code: 580107

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LSADPCK register
- E4 = Received data LSADPCK register

Error Codes: 580109 - 58010B

- E1 = Test ID
- E2 = Error code
- E3 = Common Status 1
- E4 = Upper Port Adapt Check
- E5 = Upper Port Buffer Check
- E6 = Upper ECC Check
- E7 = Upper Storage Control Check
- E8 = Upper Storage Card Address Check
- E9 = Upper Storage Adapter Check

Routine 58 Test 02

Description

This test verifies that the error check bits in the lower port storage adapter check register (LSADPCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

580201: Bit under test in LSADPCK register did not set
580203: Check 2 (bit 0 of the XCS register) is on
580204: Lower port check reset (bit 1 of register LCTL) did not reset register LSADPCK
580205: Bit in LSADPCK register should not be on
580207: USADPCK is not as expected while testing lower port
580209: Lower port check (bit 1 of register CSTAT1) is off
58020B: Check 2 (bit 0 of register XCS) off

Error Display Bytes

Error Codes: 580201 - 580205

- E1 = Test ID
- E2 = Error code
- E3 = Expected data LSADPCK register
- E4 = Received data LSADPCK register

Error Code: 580207

- E1 = Test ID
- E2 = Error code
- E3 = Expected data USADPCK register
- E4 = Received data USADPCK register

Error Codes: 580209 - 58020B

- E1 = Test ID
- E2 = Error code
- E3 = Common Status 1
- E4 = Lower Port Adapter Check
- E5 = Lower Port Buffer Check
- E6 = Lower ECC Check
- E7 = Lower Storage Control Check
- E8 = Lower Storage Card Address Check
- E9 = Lower Storage Adapter Check

Routine 58 Test 03

Description

This test verifies that the error check bits in the common storage address refresh check register (CSARCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

580301: Bit under test in CSARCK register did not set
580304: Common check reset (bit 4 of register CCTL) did not reset register CSARCK
580305: Bit 7 of CSARCK register is on
580309: Common check (bit 3 of CSTAT1) is off
58030B: Check 2 (bit 0 of register XCS) off

Error Display Bytes

Error Codes: 580301 - 580305

- E1 = Test ID
- E2 = Error code
- E3 = Expected data CSARCK register
- E4 = Received data CSARCK register

Error Codes: 580309 - 58030B

- E1 = Test ID
- E2 = Error code
- E3 = Common Status 1
- E4 = Common Storage Control Check
- E5 = Communication Adapter Check
- E6 = Common Storage Address Check
- E7 = Storage Card Refresh Address Check
- E8 = Storage Address Refresh Check

Routine 58 Test 04

Description

This test verifies that the error check bits in the common storage address check register (CSACK) can be set and reset.

Note: Bit 1 is not tested in this test. It is tested in test 5.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

580401: Bit under test in CSACK register did not set
580404: Common check reset (bit 4 of register CCTL) did not reset register CSACK
580406: Bit 4 of CSPRDIC register is not on
580407: Bit 4 of CSPRDIC register is on
580409: Common check (bit 3 of register CSTAT1) off

Error Display Bytes

Error Codes: 580401 - 580405

- E1 = Test ID
- E2 = Error code
- E3 = Expected data CSACK register
- E4 = Received data CSACK register

Error Codes: 580409 - 58040B

- E1 = Test ID
- E2 = Error code
- E3 = Common Status 1
- E4 = Common Storage Control Check
- E5 = Communication Adapter Check
- E6 = Storage Adapter Check
- E7 = Storage Card Refresh Address Check
- E8 = Storage Address Refresh Check

Routine 58 Test 05

Description

This test verifies that the error indications in the multiple IR address decode register (CMADEC) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

580501: Bit under test in CMADEC register did not set
580502: Unexpected bit on in the CMADEC register
580504: Common check reset (bit 4 of register CCTL) did not reset register CMADEC or bit 1 of the CSACK register
580505: Bit in CMADEC register should be off
580506: Bit 4 of CSPRDIC register is not on
580509: Common check (bit 3 of CSTAT1) is off

Error Display Bytes

Error Codes: 580501 - 580505

- E1 = Test ID
- E2 = Error code
- E3 = Expected data CMADEC register
- E4 = Received data CMADEC register

Error Codes: 580509 - 58050B

- E1 = Test ID
- E2 = Error code
- E3 = Common Status 1
- E4 = Common Storage Control Check
- E5 = Communication Adapter Check
- E6 = Storage Adapter Check
- E7 = Storage Card Refresh Address Check
- E8 = Storage Address Refresh Check

Routine 59 Test 01

Description

This test checks the data path from the upper port SSAR register (USAR2) through the incrementer and back to USAR2.

Parameters

Byte 1

X'00' (default) - Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590101: SSAR register is not correct with inhibit increment on
590102: SSAR register did not increment correctly
5901E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Upper Port SSAR2
- E4 = Expected Data Upper Port SSAR2
- E5 = Received Data Upper Port SSAR2
- E6 = Port Adapter Check (UPACK)
- E7 = Port Buffer Check (UPBCK)
- E8 = ECC Check (UECCCK)
- E9 = Storage Control Check (USCCK)
- EA = Storage Card Address Check (USCACK)
- EB = Storage Adapter Check (USADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 02

Description

This test checks the data path from the upper port SSAR register (USAR1) through the incrementer and back to USAR1.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590201: SSAR register is not correct with inhibit increment on
590202: SSAR register did not increment correctly
5902E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Upper SSAR1
- E4 = Expected Upper SSAR1
- E5 = Received Upper SSAR1
- E6 = Port Adapter Check (UPACK)
- E7 = Port Buffer Check (UPBCK)
- E8 = ECC Check (UECCCK)
- E9 = Storage Control Check (USCCK)
- EA = Storage Card Address Check (USCACK)
- EB = Storage Adapter Check (USADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 03

Description

This test checks the data path from the upper port SSAR register (USAR0) through the incrementer and back to USAR0.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590301: SSAR register is not correct with inhibit increment on
590302: SSAR register did not increment correctly
5903E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Upper SSAR0
- E4 = Expected Upper SSAR0
- E5 = Received Upper SSAR0
- E6 = Port Adapter Check (UPACK)
- E7 = Port Buffer Check (UPBCK)
- E8 = ECC Check (UECCCK)
- E9 = Storage Control Check (USCCK)
- EA = Storage Card Address Check (USCACK)
- EB = Storage Adapter Check (USADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 04

Description

This test checks the data path from the lower port SSAR register (LSAR2) through the incrementer and back to LSAR2.

Parameters

Byte 1

X'00' (default) - Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590401: SSAR register is not correct with inhibit increment on
590402: SSAR register did not increment correctly
5904E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Lower SSAR2
- E4 = Expected Lower SSAR2
- E5 = Received Lower SSAR2
- E6 = Port Adapter Check (LPACK)
- E7 = Port Buffer Check (LPBCK)
- E8 = ECC Check (LECCCK)
- E9 = Storage Control Check (LSCCK)
- EA = Storage Card Address Check (LSCACK)
- EB = Storage Adapter Check (LSADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 05

Description

This test checks the data path from the lower port SSAR register (LSAR1) through the incrementer and back to LSAR1.

Parameters

Byte 1

X'00' (default) - Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590501: SSAR register is not correct with inhibit increment on
590502: SSAR register did not increment correctly
5905E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Lower SSAR1
- E4 = Expected Lower SSAR1
- E5 = Received Lower SSAR1
- E6 = Port Adapter Check (LPACK)
- E7 = Port Buffer Check (LPBCK)
- E8 = ECC Check (LECCCK)
- E9 = Storage Control Check (LSCCK)
- EA = Storage Card Address Check (LSCACK)
- EB = Storage Adapter Check (LSADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 06

Description

This test checks the data path from the lower port SSAR register (LSAR0) through the incrementer and back to LSAR0.

Parameters

Byte 1

X'00' (default) - Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590601: SSAR register is not correct with inhibit increment on
590602: SSAR register did not increment correctly
5906E0: Data transfer complete is not on after a store operation

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Initial Lower SSAR0
- E4 = Expected Lower SSAR0
- E5 = Received Lower SSAR0
- E6 = Port Adapter Check (LPACK)
- E7 = Port Buffer Check (LPBCK)
- E8 = ECC Check (LECCCK)
- E9 = Storage Control Check (LSCCK)
- EA = Storage Card Address Check (LSCACK)
- EB = Storage Adapter Check (LSADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 59 Test 07

Description

This test checks the path from SSAR to storage. An incrementing pattern is used in all upper SSAR bytes.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run test 07 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

590701: Addressing error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 to E5 = SSAR value
- E6 = Port Adapter Check (UPACK)
- E7 = Port Buffer Check (UPBCK)
- E8 = ECC Check (UECCCK)
- E9 = Storage Control Check (USCCK)
- EA = Storage Card Address Check (USCACK)
- EB = Storage Adapter Check (USADPCK)
- EC = Common Storage Card Refresh Address Check

Routine 5A Test 01

Description

This test checks the upper test loop write to read ECC. A data pattern is stored using the upper port one word prior to the diagnostic area. A fetch is performed using the upper port and, if the upper test loop is not functioning, then a fetch of the diagnostic word X'DEAD DEAD DEAD DEAD' will occur; otherwise the original data pattern stored will be fetched. Eight data patterns are used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5A0110: The data pattern fetched is X'DEAD'. Test loop write to read ECC is not functioning correctly.
5A0111: Data is not as expected
5A01E0: Microcode timeout waiting for data transfer complete on a store operation
5A01E1: Microcode time-out waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Codes: 5A0111

- E1 = Test ID
- E2 = Error code
- E3 = Not used
- E4 = X'00' through X'0C' - Address of leftmost byte displayed in bytes E5 and E9
- E5 through E8 = Expected 4 bytes, generally starting with first byte to miscompare
- E9 through EC = Received 4 bytes, generally starting with first byte to miscompare

Error Codes: 5A0110, 5A01E0, and 5A01E1

- E1 = Test ID
- E2 = Error code

Diagnostic Tests DC 5A02

Routine 5A Test 02

Description

This test checks the lower test loop write to read ECC. A data pattern is stored using the lower port one word prior to the diagnostic area. A fetch is performed using the lower port and, if the lower test loop is not functioning, then a fetch of the diagnostic word X'DEAD DEAD DEAD DEAD' will occur; otherwise the original data pattern stored will be fetched. Eight data patterns are used.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5A0210: The data pattern fetched is X'DEAD'. Test loop write to read ECC is not functioning correctly.
5A0211: Data is not as expected
5A02E0: Microcode timeout waiting for data transfer complete on a store operation
5A02E1: Microcode time-out waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Codes: 5A0211

- E1 = Test ID
- E2 = Error code
- E3 = Not used
- E4 = X'00' through X'0C' - Address of leftmost byte displayed in bytes E5 and E9
- E5 through E8 = Expected 4 bytes, generally starting with first byte to miscompare
- E9 through EC = Received 4 bytes, generally starting with first byte to miscompare

Error Codes: 5A0210, 5A02E0, and 5A02E1

- E1 = Test ID
- E2 = Error code

Diagnostic Tests DC 5A02

Routine 5A Test 03

Description

This test checks the test loop write to read storage and the data path from the storage control board to the storage boards by exercising them in a storage loop from the upper port. Eight different test words are sent through the storage loop and checked. The data patterns ensure that each data bit is distinct and can be set and reset. The data patterns are not written into subsystem storage. If a fetch results in data of X'DEAD...DEAD' which is stored in the diagnostic word, test loop storage is not working.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Test both storage boards if installed
X'02' Test second storage board (A2) only
X'03' Test first storage board (B2) only

Isolation Codes

5A0310: The data pattern fetched is X'DEAD'. Test loop write to read storage is not functioning correctly.
5A0340: Data is not as expected
5A03E0: Microcode time-out waiting for data transfer complete on a store operation
5A03E1: Microcode time-out waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Codes: 5A0340

- E1 = Test ID
- E2 = Error code
- E3 =
  X'0x' - First storage board being tested
  X'1x' - Second storage board being tested
  X'x0' - One storage board installed
  X'x4' - Two storage boards installed
- E4 = X'00' through X'0C' - Storage bus byte displayed in bytes E5 and E9
- E5 through E8 = Expected 4 bytes
- E9 through EC = Received 4 bytes

Error Codes: 5A0310, 5A03E0, and 5A03E1

- E1 = Test ID
- E2 = Error code
- E3 =
  X'0x' - First storage board being tested
  X'1x' - Second storage board being tested
  X'x0' - One storage board installed
  X'x4' - Two storage boards installed

Routine 5A Test 04

Description

This test checks the check bit data paths from the storage control board to the storage boards by exercising them in storage loop from the upper port. Five different test check bit data patterns are put into the storage loop to check the ECC data path. Data bits are ignored and subsystem storage is not written.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Test both storage boards if installed
X'02' Test second storage board (A2) only
X'03' Test first storage board (B2) only

Isolation Codes

5A0450: Check bits do not compare
5A04E0: Microcode time-out waiting for data transfer complete on a store operation
5A04E1: Microcode time-out waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Code: 5A0450

- E1 = Test I.D.
- E2 = Error code
- E3 =
  X'0x' - First storage board being tested
  X'1x' - Second storage board being tested
  X'x0' - One storage board installed
  X'x4' - Two storage boards installed
- E4 = Unused
- E5 and E6 = Expected two bytes of check bits
- E7 and E8 = Received two bytes of check bits

Error Codes: 5A04E0 and 5A04E1

- E1 = Test ID
- E2 = Error code
- E3 =
  X'0x' - First storage board being tested
  X'1x' - Second storage board being tested
  X'x0' - One storage board installed
  X'x4' - Two storage boards installed

Diagnostic Tests DC 5A04

Routine 5A Test 05

Description

This test checks the upper port buffer padding function. With storage byte counts of 1 through 16 and SRC off, it should pad with 15 through 0 bytes of zeroes respectively. With byte counts of 1 through 14 and SRC on, the padding should be 13 through 0 bytes, with 2 bytes of SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5A0501: Upper port buffer did not get the data bytes right. SRC was inhibited.
5A0502: Upper port buffer did not pad zeroes correctly. SRC was inhibited.
5A0503: Upper port buffer did not get the data bytes right. SRC was enabled.
5A0504: Upper port buffer did not pad zeroes correctly. SRC was enabled.
5A05E0: Microcode timeout waiting for data transfer complete on a store operation
5A05E1: Microcode timeout waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Codes: 5A0501 through 5A0504

- E1 = Test I.D.
- E2 = Error code
- E3 = Expected data
- E4 = Received data
- E5 = Byte count (UCTRL)
- E6 = Byte number that miscompared

Error Codes: 5A05E0 and 5A05E1

- E1 = Test ID
- E2 = Error code

Routine 5A Test 06

Description

This test checks the lower port buffer padding function. With storage byte counts of 1 through 16 and SRC off, it should pad with 15 through 0 bytes of zeroes respectively. With byte counts of 1 through 14 and SRC on, the padding should be 13 through 0 bytes, with 2 bytes of SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5A0601: Lower port buffer did not get the data bytes right. SRC was inhibited.
5A0602: Lower port buffer did not pad zeroes correctly. SRC was inhibited.
5A0603: Lower port buffer did not get the data bytes right. SRC was enabled.
5A0604: Lower port buffer did not pad zeroes correctly. SRC was enabled.
5A06E0: Microcode timeout waiting for data transfer complete on a store operation
5A06E1: Microcode timeout waiting for data transfer complete on a fetch operation

Error Display Bytes

Error Codes: 5A0601 through 5A0604

- E1 = Test I.D.
- E2 = Error code
- E3 = Expected data
- E4 = Received data
- E5 = Byte count (LCTRL)
- E6 = Byte number that miscompared

Error Codes: 5A06E0 and 5A06E1

- E1 = Test ID
- E2 = Error code

Routine 5B Test 01

Description

This test checks that the error conditions of the upper port storage control check register (USCCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'x0' Selected data pattern (Bits 0-3 valid)

Isolation Codes

5B0101: Bit being tested did not set
5B0102: Upper port check (bit 0 of register CSTAT1) is off
5B0103: Bit being tested did not reset
5B0105: Controlled machine reset (bit 2 of register CCTL) did not reset register USCCK
5B0106: Upper ECC check bit 6 or 7 set
5B0108: Bit 0 not zero
5B0109: Bit 1 not zero
5B010A: Bit 2 not zero
5B010B: Bit 3 not zero
5B010C: Lower port bit set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5B Test 02

Description

This test checks that the error conditions of the lower port storage control check register (LSCCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'x0' Selected data pattern (Bits 0-3 only)

Isolation Codes

5B0201: Bit being tested did not set
5B0202: Lower port check (bit 1 of register CSTAT1) is off
5B0203: Bit under test did not reset
5B0205: Controlled machine reset (bit 2 of register CCTL) did not reset register LSCCK
5B0206: Lower ECC check bit 6 or 7 set
5B0207: Upper port (USCCK) bit on
5B0208: Bit 0 not zero
5B0209: Bit 1 not zero
5B020A: Bit 2 not zero
5B020B: Bit 3 not zero
5B020C: Upper port bit set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5B Test 03

Description

This test checks that the error conditions of the upper port storage control check register (USCACK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern (Bits 0-5 only)

Isolation Codes

5B0301: Bit being tested did not set
5B0302: Upper port check (bit 0 of register CSTAT1) is off
5B0303: Bit being tested did not reset
5B0305: Controlled machine reset (bit 2 of register CCTL) did not reset register USCACK
5B0306: Upper port DA data address 6-15 (bit 3 of register USADPCK) is on
5B030C: Lower port (LSCACK) bit is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5B Test 04

Description

This test checks that the error conditions of the lower port storage control check register (LSCACK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern (Bits 0-5 only)

Isolation Codes

5B0401: Bit being tested did not set
5B0402: Lower port check (bit 1 of register CSTAT1) is off
5B0403: Bit being tested did not reset
5B0405: Controlled machine reset (bit 2 of register CCTL) did not reset register LSCACK
5B0406: Lower port DA data address 6-15 (bit 3 of register LSADPCK) is on
5B040C: Upper port (USCACK) bit is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5B Test 05

Description

This test checks that the error conditions of the common storage control check register (CSCCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'x0' Selected data pattern (Bits 0-1 only)

Isolation Codes

5B0501: Bit being tested did not set
5B0502: Upper port check (bit 0 of register CSTAT1) is off
5B0503: Bit being tested did not reset
5B0505: Controlled machine reset (bit 2 of register CCTL) did not reset CSCCK register
5B0509: Bit 1 set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5B Test 07

Description

This test checks that the error conditions of the common storage card refresh address check (CSCRACK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'07' Run only test 07

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5B0701: Bits being tested did not set
5B0702: Common Check off
5B0703: Bits under test did not reset
5B0705: Controlled machine reset (bit 2 of register CCTL) did not reset register CSCRACK

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 5C Test 01

Description

This test checks the receivers and drivers between port buffers and ECC. A pattern is read from the port buffer to the storage data registers. A check is made for any bits on in the upper port ECC check register (UECCCK). The pattern is then fetched back to the port buffer and the UECCCK register is again checked for checks. Test loop write to read storage mode is used so no data is stored or fetched to the cache. The byte count is 256 to check both port buffers.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5C0101: Upper port ECC check bit 1 (bit 1 of UECCCK register) is on
5C0102: Upper port ECC check bit 2 (bit 2 of UECCCK register) is on
5C0103: Upper port ECC check bit 3 (bit 3 of UECCCK register) is on
5C0104: Upper port ECC check bit 4 (bit 4 of UECCCK register) is on
5C0105: Upper port ECC check bit 5 (bit 5 of UECCCK register) is on
5C0106: Upper port ECC check bit 6 (bit 6 of UECCCK register) is on
5C0107: Upper port ECC check bit 7 (bit 7 of UECCCK register) is on
5C0108: ECC/PB data-in parity check 1 (bit 6 of UPBCK register) is on
5C0109: Bit 7 of LPBCK register is on
5C010A: Data not as expected
5C01E0: Store operation did not end
5C01E1: Fetch operation did not end

Error Display Bytes

Error Codes: 5C0101 through 5C010A

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error pointer

Error Codes: 5C01E0 and 5C01E1

- E1 = Test ID
- E2 = Error Codes
- E3 = CSTAT1
- E4 = UPACK
- E5 = UPBCK
- E6 = UECCCK
- E7 = USCCK
- E8 = USCACK
- E9 = USADPCK

Routine 5C Test 02

Description

This test checks the receivers and drivers between port buffers and ECC. A pattern is read from the port buffer to the storage data registers. A check is made for any bits on in the lower port ECC check register (LECCCK). The pattern is then fetched back to the port buffer and the LECCCK register is again checked for checks. Test loop write to read storage mode is used so no data is stored or fetched to the cache. The byte count is 256 to check both port buffers.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5C0201: Lower port ECC check bit 1 (bit 1 of LECCCK register) is on
5C0202: Lower port ECC check bit 2 (bit 2 of LECCCK register) is on
5C0203: Lower port ECC check bit 3 (bit 3 of LECCCK register) is on
5C0204: Lower port ECC check bit 4 (bit 4 of LECCCK register) is on
5C0205: Lower port ECC check bit 5 (bit 5 of LECCCK register) is on
5C0206: Lower port ECC check bit 6 (bit 6 of LECCCK register) is on
5C0207: Lower port ECC check bit 7 (bit 7 of LECCCK register) is on
5C0208: ECC/PB data-in parity check 1 (bit 6 of LPBCK register) is on
5C0209: Bit 7 of LPBCK register is on
5C020A: Data not as expected
5C02E0: Store operation did not end
5C02E1: Fetch operation did not end

Error Display Bytes

Error Codes: 5C0201 through 5C020A

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error pointer

Error Codes: 5C02E0 and 5C02E1

- E1 = Test ID
- E2 = Error Codes
- E3 = CSTAT1
- E4 = UPACK
- E5 = UPBCK
- E6 = UECCCK
- E7 = USCCK
- E8 = USCACK
- E9 = USADPCK

Routine 5C Test 03

Description

This test checks that the error conditions of the upper port ECC check register (UECCCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern **(Bits 1-7 only)**

Isolation Codes

5C0301: Bit being tested did not set
5C0302: Upper port check (bit 0 of register CSTAT1) is off bit being tested
5C0304: Upper port check (bit 0 of register CSTAT1) is on
5C0305: Controlled machine reset (bit 2 of register CCTL) did not reset register UECCCK.
5C0309: Bit under test was not reset by upper check reset
5C030A: Lower port (LECCCK) bit set
5C03E0: Store operation did not end
5C03E1: Fetch operation did not end

Error Display Bytes

Error Codes: 5C0301 through 5C030A

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error pointer

Error Codes: 5C03E0 and 5C03E1

- E1 = Test ID
- E2 = Error Codes
- E3 = CSTAT1
- E4 = UPACK
- E5 = UPBCK
- E6 = UECCCK
- E7 = USCCK
- E8 = USCACK
- E9 = USADPCK

Routine 5C Test 04

Description

This test checks that the error conditions of the lower port ECC check register (LECCCK) can be set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' Selected data pattern **(Bits 1-7 only)**

Isolation Codes

5C0401: Bit being tested did not set
5C0402: Lower port check (bit 1 of register CSTAT1) is off
5C0404: Lower port check (bit 1 of register CSTAT1) is on
5C0405: Controlled machine reset (bit 2 of register CCTL) did not reset register LECCCK.
5C0409: Bit being tested not reset by lower check reset (bit 1 of register UCTL)
5C040A: Upper port (UECCCK) bit set
5C04E0: Store operation did not end
5C04E1: Fetch operation did not end

Error Display Bytes

Error Codes: 5C0401 through 5C040A

- E1 = Test ID
- E2 = Error Codes
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error pointer

Error Codes: 5C04E0 and 5C04E1

- E1 = Test ID
- E2 = Error Codes
- E3 = CSTAT1
- E4 = UPACK
- E5 = UPBCK
- E6 = UECCCK
- E7 = USCCK
- E8 = USCACK
- E9 = USADPCK

Routine 5D Test 01

Description

This test checks that all ECC single bit errors are detected and that the correction is done successfully. The ECC single bit error circuitry is tested by using only the bit under test. A check is made that no errors are generated.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' The number of the bit (0-127) to be tested in the 16-byte cache location, specified as follows:

Byte 3 Bit							
0	1	2	3	4	5	6	7
	Byte (0-15)				Bit (0-7)		

For example: X'00' will test bit 0 of byte 0
X'08' will test bit 0 of byte 1
X'7F' will test bit 7 of byte 15

Isolation Codes

5D0101: Lower port check bytes not as expected
5D0102: Lower port syndrome bytes not as expected
5D0103: Lower port fetched data not as expected
5D0105: Lower port CSTAT2 register incorrect
5D0106: Lower port store or ROS parity check 1 on
5D0107: Lower port store or ROS parity check 2 on
5D0108: Lower port ROS-M parity check on
5D0111: Upper port check bytes not as expected
5D0112: Upper port syndrome bytes not as expected
5D0113: Upper port fetched data not as expected
5D0115: Upper port CSTAT2 register incorrect
5D0116: Upper port store or ROS parity check 1 on
5D0117: Upper port store or ROS parity check 2 on
5D0118: Upper port ROS-M parity check on
5D01E0: Store operation did not end lower port
5D01E1: Fetch operation did not end lower port
5D01F0: Store operation did not end upper port
5D01F1: Fetch operation did not end upper port

Error Display Bytes

Error Codes: 5D0101 - 5D0115

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E5 = Byte in error pointer

Error Codes: 5D01E0, 5D01E1, 5D01F0, 5D01F1

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = LPACK
- E5 = LPBCK
- E6 = LECCCK
- E7 = LSCCK
- E8 = LSCACK
- E9 = LSADPCK

Diagnostic Tests DC 5D01

Routine 5E Test 01

Description

This test checks that selected ECC double bit errors are detected and that the corrections are done successfully. The ECC double bit error circuitry is tested by using bit C16 with every other bit. A check is made that no errors are generated.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'xx' The number of the bit (0-127) to be tested in the 16-byte cache location, specified as follows:

Byte 3 Bit							
0	1	2	3	4	5	6	7
	Byte (0-15)				Bit (0-7)		

For example: X'00' will test bit 0 of byte 0
X'08' will test bit 0 of byte 1
X'7F' will test bit 7 of byte 15

Isolation Codes

5E0101: Lower port check bytes not as expected
5E0102: Lower port syndrome bytes not as expected
5E0103: Lower port data bits not as expected
5E0105: Lower port CSTAT2 register incorrect
5E0106: Lower port store or ROS parity check 1 on
5E0107: Lower port store or ROS parity check 2 on
5E0108: Lower port ROS-M parity check on
5E0111: Upper port check bytes not as expected
5E0112: Upper port syndrome bytes not as expected
5E0113: Upper port fetched data not as expected
5E0115: Upper port CSTAT2 register incorrect
5E0116: Upper port store or ROS parity check 1 on
5E0117: Upper port store or ROS parity check 2 on
5E0118: Upper port ROS-M parity check on
5E01E0: Store operation did not end lower port
5E01E1: Fetch operation did not end lower port
5E01F0: Store operation did not end upper port
5E01F1: Fetch operation did not end upper port

Error Display Bytes

Error Codes: 5E0101 - 5E0115

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E6 = Byte in error pointer

Error Codes: 5E01E0, 5E01E1, 5E01F0, 5E01F1

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = LPACK
- E6 = LPBCK
- E7 = LECCCK
- E8 = LSCCK
- E9 = LSCACK
- E10= LSADPCK

Routine 5F Test 01

Description

This test checks that some of the ECC uncorrectable errors are detected. A check is made that all appropriate errors are set.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5F0101: Lower port check bytes not as expected
5F0102: Lower port syndrome bytes not as expected
5F0103: Lower port check (bit 1 of register CSTAT1) is off
5F0104: Lower port uncorrectable check (bit 0 of register LECCCK) is off
5F0105: Lower port CSTAT2 register incorrect
5F0106: Lower port data bits not as expected
5F0107: Lower port uncorrectable check (bit 0 of register LECCCK) is on
5F0108: Lower port uncorrectable check (bit 0 of register LECCCK) not reset
5F0109: Lower port ROS-M check (bit 5 of register LECCCK) not reset
5F0111: Upper port check bytes not as expected
5F0112: Upper port syndrome bytes not as expected
5F0113: Upper port check (bit 1 of register CSTAT1) is off
5F0114: Upper port uncorrectable check (bit 0 of register UECCCK) is off
5F0115: Upper port CSTAT2 register incorrect
5F0116: Upper port data bits not as expected
5F0117: Upper port uncorrectable check (bit 0 of register UECCCK) is on
5F0118: Upper port uncorrectable check (bit 0 of register UECCCK) not reset
5F0119: Upper port ROS-M check (bit 5 of register UECCCK) not reset
5F01E0: Store operation did not end lower port
5F01E1: Fetch operation did not end lower port
5F01F0: Store operation did not end upper port
5F01F1: Fetch operation did not end upper port

Error Display Bytes

Error Codes: 5F0101 - 5F0119

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)
- E6 = Byte in error pointer

Error Codes: 5F01E0, 5F01E1, 5F01F0, 5F01F1

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = LPACK
- E6 = LPBCK
- E7 = LECCCK
- E8 = LSCCCK
- E9 = LSCACK
- E10 = LSADPCK

Routine 5F Test 02

Description

This test checks that the Inhibit ECC function is controlled by the degate decodes.

Byte 1

X'00' (default) Run all tests in this routine
X'01' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

5F0201: Inhibit ECC per degate decodes inoperative

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected
- E4 = Received
- E5 = Byte-in-error pointer

Routine 60 Test 01

Description

This test verifies that the upper port can store and fetch data in subsystem storage. A 767 byte count is used and SRC is not inhibited. By using the byte count of 767, this test checks that the two SRC bytes can be split across two port buffer arrays with no errors. An incrementing data test pattern is written into the ADT buffer and transferred to storage. After the store operation, the ADT buffer is written with a X'FF' data pattern. The data is then fetched and compared against the expected data pattern. If a single- or double-bit error occurred, then 16 bytes of data are stored and fetched every 64K storage words, with ECC and SRC inhibited. If a similar error occurs in every location checked, an error is reported.

The area of subsystem storage used may be controlled with parameter byte 3. If the default parameter is used and a second storage board is installed, the test is repeated on the second board.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600101: Fetched data miscompared
600102: Common data error across board
600103: Op complete obtained but after microcode timeout
6001A0: IR check on a transfer
6001B0: Communication, common check, or a unsupported check 2
6001D0: Port check with op complete on a store
6001D1: Port check with op complete on a fetch
6001E0: No check, no op complete on a store
6001E1: No check, no op complete on a fetch
6001F0: Port check and no op complete on a store
6001F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600101

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare data (SSAR2)
- E4 = Byte position of miscompare data
- E5 = expected
- E6 = received

Error Code: 600102

- E1 = Test ID
- E2 = Error code
- E3 = SSAR0
- E4 = Bit position of error

Error Code: 600103

- E1 = Test ID
- E2 = Error code

Error Code: 6001A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6001B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6001D0, 6001D1, 6001F0, 6001F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
- E4 = CSTAT1
- E5 = Port adapt ck (UPACK)
- E6 = Port buffer ck (UPBCK)
- E7 = SSAR0 (USSAR0)
- E8 = SSAR1 (USSAR1)
- E9 = SSAR2 (USSAR2)
- EA = Storage adapt ck (USADPCK)
- EB = Storage card addr ck (USCACK)
- EC = ECC ck (UECCCK)
- ED = Storage control ck (USCCK)

Error Codes: 6001E0, 6001E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout

Routine 60 Test 02

Description

This test verifies that the lower port can store and fetch data in subsystem storage. A 767 byte count is used and SRC is not inhibited. By using the byte count of 767, this test checks that the two SRC bytes can be split across two port buffer arrays with no errors. A test pattern is written into the ADT buffer and transferred to storage. After the store operation, the ADT buffer is written with a X'FF' data pattern. The data is then fetched and compared against the expected data pattern. The area of subsystem storage used may be controlled with parameter byte 3. If the default parameter is used and a second storage board is installed, the test is repeated on the second board.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run test 02 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600201: Fetched data miscompared
600203: Op complete obtained but after microcode timeout
6002A0: IR Check on a transfer
6002B0: Communication, common check, or a unsupported check 2
6002D0: Port check with op complete on a store
6002D1: Port check with op complete on a fetch
6002E0: No check, no op complete on a store
6002E1: No check, no op complete on a fetch
6002F0: Port check and no op complete on a store
6002F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600201

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare word (SSAR2)
- E4 = Byte address of miscompare word
- E5 = Expected
- E6 = Received

Error Code: 600203

- E1 = Test ID
- E2 = Error code

Error Code: 6002A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6002B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6002D0, 6002D1, 6002F0, 6002F1

- E1 = Test ID
- E2 = Error code
- E3 = X'80' - check registers are lower port
- E4 = CSTAT1
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Codes: 6002E0, 6002E1

- E1 = Test ID
- E2 = Error code
- E3 = X'80' - lower port timeout

Routine 60 Test 03

Description

This test verifies that the upper and lower ports can store data in an interleaved fashion into the subsystem storage. Two 384 byte test patterns are written from the ADT buffer into two adjacent areas of the subsystem storage. The upper port is stored into first and the results are checked when the store operations are completed. The data is then fetched and compared. The area of subsystem storage used may be controlled with parameter byte 3.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run test 03 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600301: Fetched data miscompared
6003A0: IR check on a transfer
6003B0: Communication, common check, or a unsupported check 2
6003D0: Port check with op complete on a store
6003D1: Port check with op complete on a fetch
6003E0: No check, no op complete on a store
6003E1: No check, no op complete on a fetch
6003F0: Port check and no op complete on a store
6003F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600301

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare word (SSAR2)
- E4 = Byte address of miscompare word
- E5 = Expected
- E6 = Received

Error Code: 6003A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6003B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6003D0, 6003D1, 6003F0, 6003F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = CSTAT1
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6003E0, 6003E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 60 Test 04

Description

This test verifies that the upper port can store data into the subystems storage, interleaved with the lower port fetching the same data back from the subsystem storage. A 2K byte test pattern is written from the ADT buffer into the subsystem storage using the upper port. At the correct time during the store operation, the lower port starts fetching the first 384 bytes from the subsystem storage. When the operation is completed, the results are checked and the fetched data is verified. The area of subsystem storage used may be controlled with parameter byte 3.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run test 04 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600401: Fetched data miscompared
6004A0: IR check on a transfer
6004B0: Communication, common check, or an unsupported check 2
6004D0: Port check with op complete on a store
6004D1: Port check with op complete on a fetch
6004E0: No check, no op complete on a store
6004E1: No check, no op complete on a fetch
6004F0: Port check and no op complete on a store
6004F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600401

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare word (SSAR2)
- E4 = Byte address of miscompare word
- E5 = Expected
- E6 = Received

Error Code: 6004A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6004B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6004D0, 6004D1, 6004F0, 6004F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = CSTAT1
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6004E0, 6004E1

- E1: = Test ID
- E2: = Error code
- E3: = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 60 Test 05

Description

This test verifies that the lower port can store data into the subsystem storage, interleaved with the upper port and fetching the same data back from the subsystem storage. A 2K byte test pattern is written from the ADT buffer into the subsystem storage using the lower port. At the correct time during the store operation, the upper port starts fetching the first 384 bytes from the subsystem storage. When the operation is completed the results are checked and the fetched data is verified. The area of subsystem storage used may be controlled with parameter byte 3.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run test 05 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600501: Fetched data miscompared
6005A0: IR check on a transfer
6005B0: Communication, common check, or an unsupported check 2
6005D0: Port check with op complete on a store
6005D1: Port check with op complete on a fetch
6005E0: No check, no op complete on a store
6005E1: No check, no op complete on a fetch
6005F0: Port check and no op complete on a store
6005F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600501

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare word (SSAR2)
- E4 = Byte address of miscompare word
- E5 = Expected
- E6 = Received

Error Code: 6005A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM checK (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6005B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6005D0, 6005D1, 6005F0, 6005F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = CSTAT1
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6005E0, 6005E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 60 Test 06

Description

This test verifies that the upper and lower ports can both fetch data in an interleaved fashion from the subsystem storage. To get the test pattern into the subsystem storage, a 768 byte incrementing pattern is written from the ADT buffer into an area of the subsystem storage using the lower port. The test pattern is then read back from the subsystem storage. One half is read back by the upper port and the other half is read back by the lower port in an interleaved fashion. The upper port is started first. When the fetch operations are completed the results are checked and the fetched data is verified. The area of subsystem storage used may be controlled with parameter byte 3.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run test 06 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Default area of storage
X'XX' Use XX for SSAR0

Note: Byte 3 bits 0-5 must not attempt to address storage that is not installed on the machine.

Isolation Codes

600601: Fetched data miscompared
6006A0: IR check on a transfer
6006B0: Communication, common check, or an unsupported check 2
6006D0: Port check with op complete on a store
6006D1: Port check with op complete on a fetch
6006E0: No check, no op complete on a store
6006E1: No check, no op complete on a fetch
6006F0: Port check and no op complete on a store
6006F1: Port check and no op complete on a fetch

Error Display Bytes

Error Code: 600601

- E1 = Test ID
- E2 = Error code
- E3 = Address of miscompare word (SSAR2)
- E4 = Byte address of miscompare word
- E5 = Expected
- E6 = Received

Error Code: 6006A0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6006B0

- E1 = Test ID
- E2 = Error code
- E3 = CSTAT1
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Stor size, cables in check (GSSCIN)

Error Codes: 6006D0, 6006D1, 6006F0, 6006F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = CSTAT1
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6006E0, 6006E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 61 Test 01

Description

This test checks that the upper byte counter shadow parity check (bit 4 of register UPBCK) will set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

610101: Byte counter shadow bit set without forcing it
610102: Upper port buffer check register (UPBCK) will not reset
610103: Data transfer complete (bit 6 of register CSTAT1) did not set
610104: Byte counter shadow check (bit 4 of register UPBCK) did not set
610105: Upper port check (bit 0 of register CSTAT1) will not set after setting the port buffer check register (UPBCK)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 61 Test 02

Description

This test checks that the lower byte counter shadow parity check (bit 4 of register LPBCK) will set and reset.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

610201: Byte counter shadow bit set without forcing it
610202: Lower port buffer check register (LPBCK) did not reset
610203: Data transfer complete (bit 7 of register CSTAT1) did not set
610204: Byte counter shadow check (bit 4 of register LPBCK) did not set
610205: Lower port check (bit 1 of register CSTAT1) will not set after setting the port buffer check register (LPBCK)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

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Routine 62 Test 01

Description

This test verifies a direct data transfer between cache and channel. A one-byte data transfer is performed. Four data patterns of '00', 'FF', '55', and 'AA' are used. The data is checked at Channel Bus In.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run test 01 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

62010D: Data in ADT buffer is not correct
62010F: Data in CBI is not correct
6201A0: IR check on a data transfer
6201B0: Communications, common check, or an unsupported check 2
6201D0: Port check with Op Complete on a store
6201D1: Port check with Op Complete on a fetch
6201E0: No check and no Op Complete on a store
6201E1: No check and no Op Complete on a fetch
6201F0: Port check and no Op Complete on a store
6201F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Code: 62010D - 62010F

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Error Code: 6201A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR cks (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6201B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cables in (GSSCIN)

Error Codes: 6201D0, 6201D1, 6201F0, 6201F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers for upper port
  X'80' - check registers for lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (UPACK)
- E6 = Port buffer ck (UPBCK)
- E7 = SSAR0 (USSAR0)
- E8 = SSAR1 (USSAR1)
- E9 = SSAR2 (USSAR2)
- EA = Storage adapt ck (USADPCK)
- EB = Storage card addr ck (USCACK)
- EC = ECC ck (UECCCK)
- ED = Storage control ck (USCCK)

Error Codes: 6201E0, 6201E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - timeout in the upper port

Routine 62 Test 02

Description

This test verifies a direct data transfer between cache and device. A one-byte data transfer is performed. Four data patterns of '00', 'FF', '55', and 'AA' are used. The data is checked at Device Bus Out.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run test 02 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test

Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

62020D: Data in ADT buffer is not correct
6202A0: IR check on a data transfer
6202B0: Communications, common check, or an unsupported check 2
6202D0: Port check with Op Complete on a store
6202D1: Port check with Op Complete on a fetch
6202E0: No check and no Op Complete on a store
6202E1: No check and no Op Complete on a fetch
6202F0: Port check and no Op Complete on a store
6202F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Code: 62020D - 62020F

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Error Code: 6202A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6202B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cables in (GSSCIN)

Error Codes: 6202D0, 6202D1, 6202F0, 6202F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers for upper port
  X'80' - check registers for lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Codes: 6202E0, 6202E1

- E1 = Test ID
- E2 = Error code
- E3 = X'80' - timeout in the lower port

Routine 63 Test 01

Description

This test checks the upper byte counter equals zero function. The byte counter is set to zero, then a store operation is performed with a pattern of X'55's to the diagnostic area. The data is fetched, then checked to ensure that the data pattern was never stored.

Note: This test is first done with SRC then without SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

630107: Byte count equal zero function error
6301A0: IR check on a data transfer
6301B0: Communications, common check, or an unsupported check 2
6301D0: Port check with Op Complete on a store
6301D1: Port check with Op Complete on a fetch
6301E0: No check and no Op Complete on a store
6301E1: No check and no Op Complete on a fetch
6301F0: Port check and no Op Complete on a store
6301F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Code: 630107

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Error Code: 6301A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status1 (CSTAT1)
- E4 = SP OP read IR cks (CSPRDIC)
- E5 = Common port adpt ck1 (CPACK1)
- E6 = Common port Adpt ck2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adapter ck (CCOMACK)
- E9 = Common storage address ck (CSACK)
- EA = Multiple IR address decode (CMADEC)

Error Code: 6301B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cables in (GSSCIN)

Error Codes: 6301D0, 6301D1, 6301F0, 6301F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (UPACK)
- E6 = Port buffer ck (UPBCK)
- E7 = SSAR0 (USSAR0)
- E8 = SSAR1 (USSAR1)
- E9 = SSAR2 (USSAR2)
- EA = Storage adapt ck (USADPCK)
- EB = Storage card addr ck (USCACK)
- EC = ECC ck (UECCCK)
- ED = Storage control ck (USCCK)

Error Codes: 6301E0, 6301E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - timeout occurred in upper port

Routine 63 Test 02

Description

This test checks the lower byte counter equals zero function. The byte counter is set to zero, then a store operation is performed with a pattern of X'55's to the diagnostic area. The data is fetched, then checked to ensure that the data pattern was never stored.

Note: This test is first done with SRC then without SRC.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test

Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

630207: Byte count equal zero function error
6302A0: IR check on a data transfer
6302B0: Communications or common check on a data transfer
6302D0: Port check with Op Complete on a store
6302D1: Port check with Op Complete on a fetch
6302E0: No check and no Op Complete on a store
6302E1: No check and no Op Complete on a fetch
6302F0: Port check and no Op Complete on a store
6302F1: Port check and no Op Complete on a fetch

Error Display Bytes

Error Code: 630207

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Error Code: 6302A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR cks (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port Adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6302B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cables in (GSSCIN)

Error Codes: 6302D0, 6302D1, 6302F0, 6302F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers for upper port
  X'80' - check registers for lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Codes: 6302E0, 6302E1

- E1 = Test ID
- E2 = Error code
- E3 = X'80' - timeout occurred in lower port

Routine 64 Test 01

Description

This test verifies that the disable padding function on the channel is working correctly. A manual store is done with all byte counts equal to 15 and with SRC. An auto fetch is done with the same byte counts with SRC and with the SSARs equal to X'00000F'. If Op Complete is not set, the disable function is not working correctly.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run test 01 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

640101: No Op Complete, disable padding function on upper port not functioning
640102: Port check during a store operation
640103: No Op complete during a store operation

Error Display Bytes

Error Code: 640101

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Error Code: 6401A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6401B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Storage size/cables in (GSSCIN)

Error Codes: 6401D0, 6401F0

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers for upper port
  X'80' - check registers for lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (LPACK)
- E6 = Port buffer ck (LPBCK)
- E7 = SSAR0 (LSSAR0)
- E8 = SSAR1 (LSSAR1)
- E9 = SSAR2 (LSSAR2)
- EA = Storage adapt ck (LSADPCK)
- EB = Storage card addr ck (LSCACK)
- EC = ECC ck (LECCCK)
- ED = Storage control ck (LSCCK)

Error Codes: 6401E0

- E1 = Test ID
- E2 = Error code
- E3 = X'80' - timeout in the lower port

Routine 65 Test 01 (Model 21 Only)

Note: Routines 65, 66, and 67 check the communications between storage directors. They must be run in one of the following sequences:

- Run Routine 65 on SD1, then 66 on SD2, then 66 on SD1, then 67 on SD1, then run Routine 65 on SD2, then 67 on SD2
- Run Routine 65 on SD2, then 66 on SD1, then 66 on SD2, then 67 on SD2, then run Routine 65 on SD1, then 67 on SD1

Description

This test forces a communication check (bit 4 of register CSTAT3) by forcing a communication address register parity check when the CCOMADI register is set to X'1B' and written to register CCOMADR.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

650101: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650102: Communication check (bit 4 of register CSTAT3) is on
650103: CPACK1 register indicated an error
650104: CPACK2 register indicated an error
650105: CCOMACK register indicated an error
650106: CSPRDIC register indicated an IR summary check.
650107: Port connection ADT buffer check (bit 7 of register CHK) is on
650108: Check 2 (bit 0 of register XCS) is on
65010D: Communication request (bit 0 of register CCOMCTL) did not set
65010E: Request honored (bit 2 of register CSTAT3) did not set
650115: Communication request (bit 0 of register CCOMCTL) did not reset
650116: Request honored (bit 2 of register CSTAT3) did not reset
650126: Communication check (bit 5 of register CSTAT3) did not set
650130: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 65 Test 02 (Model 21 Only)

Description

This test forces a communication check (bit 4 of register CSTAT3) by forcing:

- A communication buffer write parity check when register CCOMADI is set to a X'1B' and written to the communication buffer
- A communication buffer read parity check by writing data parity errors into the communication buffer, resetting the errors and then reading the data from the buffer

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run only test 02

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

650201: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650202: Communication check (bit 4 of register CSTAT3) is on
650203: CPACK1 register indicated an error
650204: CPACK2 register indicated an error
650205: CCOMACK register indicated an error
650206: CSPRDIC register indicated an IR summary check.
650207: Port connection ADT buffer check (bit 7 of register CHK) is on
650208: Check 2 (bit 0 of register XCS) is on
65020D: Communication request (bit 0 of register CCOMCTL) did not set
65020E: Request honored (bit 2 of register CSTAT3) did not set
650215: Communication request (bit 0 of register CCOMCTL) did not reset
650216: Request honored (bit 2 of register CSTAT3) did not reset
650226: Communication check (bit 5 of register CSTAT3) did not set
650230: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 65 Test 03 (Model 21 Only)

Description

This test forces a communication check (bit 4 of register CSTAT3) by forcing:

- A communication sequence check when register CCOMADI is set to a X'19' and reading register CCOMADR
- A communication sequence check when register CCOMADI is set to a X'1C' and reading register CCOMADR
- A communication sequence check when register CCOMADI is set to a X'19' and reading the communication buffer

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'03' Run only test 03

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

650301: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650302: Communication check (bit 4 of register CSTAT3) is on
650303: CPACK1 register indicated an error
650304: CPACK2 register indicated an error
650305: CCOMACK register indicated an error
650306: CSPRDIC register indicated an IR summary check.
650307: Port connection ADT buffer check (bit 7 of register CHK) is on
650308: Check 2 (bit 0 of register XCS) is on
65030D: Communication request (bit 0 of register CCOMCTL) did not set
65030E: Request honored (bit 2 of register CSTAT3) did not set
650315: Communication request (bit 0 of register CCOMCTL) did not reset
650316: Request honored (bit 2 of register CSTAT3) did not reset
650326: Communication check (bit 5 of register CSTAT3) did not set
650330: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 65 Test 04 (Model 21 Only)

Description

This test forces a communication check (bit 4 of register CSTAT3) by setting register CCOMADI to a X'86' and then writing to the CCOMADR register.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'04' Run only test 04

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

650401: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650402: Communication check (bit 4 of register CSTAT3) is on
650403: CPACK1 register indicated an error
650404: CPACK2 register indicated an error
650405: CCOMACK register indicated an error
650406: CSPRDIC register indicated an IR summary check.
650407: Port connection ADT buffer check (bit 7 of register CHK) is on
650408: Check 2 (bit 0 of register XCS) is on
65040D: Communication request (bit 0 of register CCOMCTL) did not set
65040E: Request honored (bit 2 of register CSTAT3) did not set
650415: Communication request (bit 0 of register CCOMCTL) did not reset
650416: Request honored (bit 2 of register CSTAT3) did not reset
650426: Communication check (bit 5 of register CSTAT3) did not set
650430: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 65 Test 05 (Model 21 Only)

Description

This test checks that the communication buffer is not read if request honored (bit 2 of register CSTAT3) is not on. Data is written to the communication buffer in the normal manner. Communication request (bit 0 of register CCOMCTL) is then reset so that request honored (bit 2 of register CSTAT3) can be reset. The communication buffer is read and the read data is compared to the data that was written to the communication buffer. If the data is the same, an error exit will be taken.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'05' Run only test 05

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

650501: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650502: Communication check (bit 4 of register CSTAT3) is on
650503: CPACK1 register indicated an error
650504: CPACK2 register indicated an error
650505: CCOMACK register indicated an error
650506: CSPRDIC register indicated an IR summary check.
650507: Port connection ADT buffer check (bit 7 of register CHK) is on
650508: Check 2 (bit 0 of register XCS) is on
65050D: Communication request (bit 0 of register CCOMCTL) did not set
65050E: Request honored (bit 2 of register CSTAT3) did not set
650515: Communication request (bit 0 of register CCOMCTL) did not reset
650516: Request honored (bit 2 of register CSTAT3) did not reset
650527: Communication buffer is readable while request honored is not on
650530: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 65 Test 06 (Model 21 Only)

Description

The communication buffer is written with 256 bytes of incrementing data. The data is then read and compared to an expected value. The Test and Set function is then tested by writing to the test and set register (GTS). An incrementing data pattern is written to bits 3 through 7 and a check is made to ensure that the correct storage director responded after every write. If this is successful, message waiting (bit 0 of register CSTAT3) is set and the test and set register (GTS) is read before the routine is terminated.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'06' Run only test 06

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors
Bit 4 - 1 Loop test 6 while looping routine 66 test 1 on the other SD

Isolation Codes

650601: Port adapter control cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
650602: CSTAT3 register indicated a communication check
650603: CPACK1 register indicated an error
650604: CPACK2 register indicated an error
650605: CCOMACK register indicated an error
650606: CSPRDIC register indicated an IR summary check.
650607: CHK register indicated an error
650608: Check 2 (bit 0 of register XCS) is on
650609: Test and set check (bit 0 of register CSACK) is on
65060A: Test and set obtained (bit 2 of register CSTAT1) is on
65060B: GTS register contents are not X'00'
65060C: SD1 indicator or SD2 indicator (bits 1 and 2 of register CSTAT4) is off
65060D: Communication request (bit 0 of register CCOMCTL) did not set
65060E: Request honored (bit 2 of register CSTAT3) did not set
65060F: Communication address is not X'01'
650610: Communication address is not as expected after a write operation
650611: Data read from communication buffer not as expected
650612: Communication address is not as expected after a read operation
650613: Message waiting echo back to sender (bit 1 of register CSTAT3) did not set
650614: Message waiting echo back to sender (bit 1 of register CSTAT3) did not reset
650615: Communication request (bit 0 of register CCOMCTL) did not reset
650616: Request honored (bit 2 of register CSTAT3) did not reset
650617: GTS register data is not as expected
650618: Test and set obtained (bit 2 of register CSTAT1) is off
650619: GMIC register contents is not X'00'
65061A: Microcode bit active should not be on
65061B: Data in GMIC register is not as expected
65061C: Microcode register bit active (bit 5 of register CSTAT2) is off
65062A: SD1 indicator and SD2 indicator (bits 1 and 2 of register CSTAT4) is on
65062B: Msg Wait is on before the test starts
65062C: Other SD did not set Msg Wait for this SD during SD to SD Communication.
650630: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 66 Test 01 (Model 21 Only)

Note: Routines 65, 66, and 67 check the communications between storage directors. They must be run in one of the following sequences:

- Run Routine 65 on SD1, then 66 on SD2, then 66 on SD1, then 67 on SD1, then run Routine 65 on SD2, then 67 on SD2
- Run Routine 65 on SD2, then 66 on SD1, then 66 on SD2, then 67 on SD2, then run Routine 65 on SD1, then 67 on SD1

Description

Routine 65 must be run before this routine can be run.

This routine reads the message written by the other storage director. The read communication protocol is used to read the message. After successful reading of the message, this SD sets the message waiting bit, for the other SD to read. This routine also checks that the Test/Set cannot be obtained by this SD. The Test/Set should have been obtained by the other SD. Then this SD will reset the Test/Set and then obtain the Test/Set for this SD.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

Data Pattern (same as routine 65, non zero)

Isolation Codes

660101: Port adapter cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
660102: Communication check (bit 4 of register CSTAT3) is on
660103: CPACK1 register indicated an error
660104: CPACK2 register indicated an error
660105: CCOMACK register indicated an error
660106: CSPRDIC register indicated a port control IR summary check
660107: CHK register indicated an error
660108: Check 2 (bit 0 of register XCS) is on
660109: Test and set check (bit 0 of register CSACK) is on
66010A: Test and set obtained (bit 2 of register CSTAT1) did not reset
66010B: Test and set register (GTS) did not reset
66010C: SD indicator (bits 1 and 2 of register CSTAT4) is not on for either storage director
66010D: Communication request (bit 0 of register CCOMCTL) did not set
66010E: Request honored (bit 2 of register CSTAT3) did not set
66010F: Communication Buffer contents is not X'01'
660111: Communication buffer data is not as expected
660112: CCOMADR register address did not increment after a read operation
660113: Message waiting echo back to sender (bit 1 of register CSTAT3) did not set
660115: Communication request (bit 0 of register CCOMCTL) did not reset
660116: Request honored (bit 2 of register CSTAT3) did not reset
660117: GTS register data is not X'C5' and X'A5'
660118: Test and set obtained (bit 2 of register CSTAT1) did not set
66011E: Message waiting (bit 0 of register CSTAT3) was not set by the other storage director
66011F: Message waiting (bit 0 of register CSTAT3) was not set by this storage director
660122: GTS register data is not X'CA' and X'AA'
660123: GMIC register data is not X'55'
660124: Microcode register bit active (bit 5 of register CSTAT2) should have been set by writing X'55' to the GMIC register
66012A: SD indicator (bits 1 and 2 of register CSTAT4) is on for both storage directors
660130: Communication cable out (bit 6 of register CSTAT3) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 67 Test 01 (Model 21 Only)

Note: Routines 65, 66, and 67 check the communications between storage directors. They must be run in one of the following sequences:

- Run Routine 65 on SD1, then 66 on SD2, then 66 on SD1, then 67 on SD1, then run Routine 65 on SD2, then 67 on SD2
- Run Routine 65 on SD2, then 66 on SD1, then 66 on SD2, then 67 on SD2, then run Routine 65 on SD1, then 67 on SD1

Description

Routine 65 must be run before this routine can be run.

This test clears the message in the communications buffer and resets the test/set function.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

670101: Port adapter cable out (bit 5 of register CSTAT3) or other SD powered off (bit 7 of register CSTAT3) is on
670102: Communication check (bit 4 of register CSTAT3) is on
670103: CPACK1 register indicated a error
670104: CPACK2 register indicated a error
670105: CCOMACK register indicated a error
670106: CSPRDIC register indicated an port control IR summary check
670107: CHK register indicated a error
670108: Check 2 (bit 0 of register XCS) is on
670109: Test and set check (bit 0 of register CSACK) is on
67010B: Test and set register (GTS) did not reset
67010C: SD indicator (bits 6 and 7 of register CSTAT4) is not on for either storage director
67010D: Communication request (bit 0 of register CCOMCTL) did not set
67010E: Request honored (bit 2 of register CSTAT3) did not set
670112: Communication address register (CCOMADR) did not increment
670113: Msg Wait Echo did not set by this SD
670114: Msg Wait Echo did not reset by this SD
670115: Communication request (bit 0 of register CCOMCTL) did not reset
670116: Request honored (bit 2 of register CSTAT3) did not reset
670117: GTS register data is not as X'CA' and X'AA'
670125: GMIC register did not reset
67012A: SD indicator (bits 6 and 7 of register CSTAT4) is on for both storage directors

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 68 Test 01

Description

This test checks the ability of subsystem storage to store and fetch data in each location as defined by input parameters 3 and 4. A single partition or multiple partitions may be tested. The data patterns used are X'FFF...F' and X'000...0' so that all bits are set on and off. The upper and lower ports are interleaved for speed. The partitions are as follows:

Machines Without Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'03'	0-4MB	0	01B-B2	D2,G2,P2,S2
'04'-'07'	4-8MB	1	01B-B2	B2,J2,M2,U2
'08'-'0B'	8-12MB	2	01B-B2	E2,F2,Q2,R2
'0C'-'0F'	12-16MB	3	01B-B2	C2,H2,N2,T2
'10'-'13'	16-20MB	4	01B-A2	D2,G2,P2,S2
'14'-'17'	20-24MB	5	01B-A2	B2,J2,M2,U2
'18'-'1B'	24-28MB	6	01B-A2	E2,F2,Q2,R2
'1C'-'1F'	28-32MB	7	01B-A2	C2,H2,N2,T2

Machines With Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-16MB	0	01B-B2	D2,G2,P2,S2
'10'-'1F'	16-32MB	1	01B-B2	C2,H2,N2,T2
'20'-'2F'	32-48MB	2	01B-B2	E2,F2,Q2,R2
'30'-'3F'	48-64MB	3	01B-B2	B2,J2,M2,U2

Bits Per Card By Partition Are:

```
                                        Partition
With expanded storage -      Bd B2 - 0              1

Without expanded storage -   Bd B2 - 0    1    2    3
                             Bd A2 - 4    5    6    7
```

Bits			Cards			
0	-	15	D2	B2	E2	C2
16	-	31	S2	U2	R2	T2
32	-	47	D2	B2	E2	C2
48	-	63	S2	U2	R2	T2
64	-	67	D2	B2	E2	C2
68	-	79	G2	J2	F2	H2
80	-	83	S2	U2	R2	T2
84	-	95	P2	M2	Q2	N2
96	-	111	G2	J2	F2	H2
112	-	127	P2	M2	Q2	N2
C0	-	C7	P2	M2	Q2	N2
C8	-	C15	G2	J2	F2	H2

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run test 01 only

Byte 2

Bit 0 - Run selected test once
Bit 1 - Loop selected test

Byte 3

X'00' Start with partition 0 (default)
X'00'-X'07' Starting partition number

Byte 4

X'00'-X'07' Ending partition number
X'FF' End with last installed partition (default)

Note: Bytes 3 and 4 cannot be larger than the number of installed partitions. Byte 4 cannot be smaller than byte 3.

Isolation Codes

680101: Uncorrectable error indicated
6801A0: IR check on a transfer
6801B0: Communication, common check, or an unsupported check 2
6801D0: Port check with operation complete on a store operation
6801D1: Port check with operation complete on a fetch operation
6801E0: No port check or no operation complete on a store operation
6801E1: No port check or no operation complete on a fetch operation
6801F0: Port check and no operation complete on a store operation
6801F1: Port check and no operation complete on a fetch operation

Error Display Bytes

Error Code: 680101

- E1 = Test ID
- E2 = Error code
- E3-E5 = Address of uncorrectable error
- E6 = First error bit
- E7 = Second error bit
- E8 = Third error bit

Error Code: 6801A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6801B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common STG addr ck (CSACK)
- E7 = Common STG control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Multiple IR addr decode (CMADEC)

Error Codes: 6801D0, 6801D1, 6801F0, 6801F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6801E0, 6801E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 69 Test 01

Description

This test checks the addressing path from the SSAR registers to storage for errors. A data pattern of thirteen 16 byte words is set into the ADT buffer, then written throughout subsystem storage from the low addresses to the high addresses. It is read back a word at a time and checked for uncorrectable errors or data that has been changed. Both upper and lower ports are used alternately.

Machines Without Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'03'	0-4MB	0	01B-B2	D2,G2,P2,S2
'04'-'07'	4-8MB	1	01B-B2	B2,J2,M2,U2
'08'-'0B'	8-12MB	2	01B-B2	E2,F2,Q2,R2
'0C'-'0F'	12-16MB	3	01B-B2	C2,H2,N2,T2
'10'-'13'	16-20MB	4	01B-A2	D2,G2,P2,S2
'14'-'17'	20-24MB	5	01B-A2	B2,J2,M2,U2
'18'-'1B'	24-28MB	6	01B-A2	E2,F2,Q2,R2
'1C'-'1F'	28-32MB	7	01B-A2	C2,H2,N2,T2

Machines With Expanded Storage (8MB Only)

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-8MB	0	01B-B2	D2,G2,P2,S2

Machines With Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-16MB	0	01B-B2	D2,G2,P2,S2
'10'-'1F'	16-32MB	1	01B-B2	C2,H2,N2,T2
'20'-'2F'	32-48MB	2	01B-B2	E2,F2,Q2,R2
'30'-'3F'	48-64MB	3	01B-B2	B2,J2,M2,U2

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run test 01 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

690101: Addressing error
6901A0: IR check on a transfer
6901B0: Communication, common check, or an unsupported-check 2
6901D0: Port check with operation complete on a store operation
6901D1: Port check with operation complete on a fetch operation
6901E0: No operation complete or port check on a store operation
6901E1: No operation complete or port check on a fetch operation
6901F0: Port check and no operation complete on a store operation
6901F1 Port check and no operation complete on a fetch operation

Error Display Bytes

Error Code: 690101

- E1 = Test ID
- E2 = Error code
- E3-E5 = Address in error
- E6 = Number of bits in error - Card 1
- E7 = Number of bits in error - Card 2
- E8 = Number of bits in error - Card 3
- E9 = Number of bits in error - Card 4

Error code: 6901A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6901B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Multiple IR addr decode (CMADEC)

Error Codes: 6901D0, 6901D1, 6901F0, 6901F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check is for upper port
  X'80' - check is for lower port
- E4 = CSTAT1
- E5 = Port adapt ck (U/LPACK)
- E6 = Port Buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6901E0, 6901E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 69 Test 02

Description

This test checks the addressing path from the SSAR registers to storage for errors by setting a data pattern of thirteen 16 byte words into the ADT buffer and then repeating it throughout subsystem storage from the high addresses to the low addresses. It is read back a word at a time and checked for uncorrectable errors or data that has changed. Both upper and lower ports are used alternately.

Machines Without Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'03'	0-4MB	0	01B-B2	D2,G2,P2,S2
'04'-'07'	4-8MB	1	01B-B2	B2,J2,M2,U2
'08'-'0B'	8-12MB	2	01B-B2	E2,F2,Q2,R2
'0C'-'0F'	12-16MB	3	01B-B2	C2,H2,N2,T2
'10'-'13'	16-20MB	4	01B-A2	D2,G2,P2,S2
'14'-'17'	20-24MB	5	01B-A2	B2,J2,M2,U2
'18'-'1B'	24-28MB	6	01B-A2	E2,F2,Q2,R2
'1C'-'1F'	28-32MB	7	01B-A2	C2,H2,N2,T2

16MB Machines With Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-16MB	0	01B-B2	D2,G2,P2,S2

32MB Machines With Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-16MB	0	01B-B2	D2,G2,P2,S2
'10'-'1F'	16-32MB	1	01B-B2	C2,H2,N2,T2
'20'-'2F'	32-48MB	2	01B-B2	E2,F2,Q2,R2
'30'-'3F'	48-64MB	3	01B-B2	B2,J2,M2,U2

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'02' Run test 02 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

690201: Addressing error
6902A0: IR check on a transfer
6902B0: Communication, common check or an unsupported check 2
6902D0: Port check with operation complete on a store operation
6902D1: Port check with operation complete on a fetch operation
6902E0: No operation complete or port check on a store operation
6902E1: No operation complete or port check on a fetch operation
6902F0: Port check and no operation complete on a store operation
6902F1 Port check and no operation complete on a fetch operation

Error Display Bytes

Error Code: 690201

- E1 = Test ID
- E2 = Error code
- E3-E5 = Address in error
- E6 = Number of bits in error - Card 1
- E7 = Number of bits in error - Card 2
- E8 = Number of bits in error - Card 3
- E9 = Number of bits in error - Card 4

Error Code: 6902A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM ck (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6902B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Multiple IR addr decode (CMADEC)

Error Codes: 6902D0, 6902D1, 6902F0, 6902F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check is for upper port
  X'80' - check is for lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6902E0, 6902E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 6A Test 01

Description

This test counts the number of bits in error for a partition per each card. (A partition is four storage cards with the same high-order address byte, as indicated in the chart below.) Data patterns used are 'X'FFF...F' and X'000...0' so that all data and check bits are set off and on. The upper and lower ports are used alternately. The partitions are:

Machines Without Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'03'	0- 4MB	0	01B-B2	D2,G2,P2,S2
'04'-'07'	4- 8MB	1	01B-B2	B2,J2,M2,U2
'08'-'0B'	8-12MB	2	01B-B2	E2,F2,Q2,R2
'0C'-'0F'	12-16MB	3	01B-B2	C2,H2,N2,T2
'10'-'13'	16-20MB	4	01B-A2	D2,G2,P2,S2
'14'-'17'	20-24MB	5	01B-A2	B2,J2,M2,U2
'18'-'1B'	24-28MB	6	01B-A2	E2,F2,Q2,R2
'1C'-'1F'	28-32MB	7	01B-A2	C2,H2,N2,T2

Machines With Expanded Storage (8MB Only)

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-8MB	0	01B-B2	D2,G2,P2,S2

Machines With Expanded Storage

High Order Address Byte		Partition	Board	Cards 1 2 3 4
'00'-'0F'	0-16MB	0	01B-B2	D2,G2,P2,S2
'10'-'1F'	16-32MB	1	01B-B2	C2,H2,N2,T2
'20'-'2F'	32-48MB	2	01B-B2	E2,F2,Q2,R2
'30'-'3F'	48-64MB	3	01B-B2	B2,J2,M2,U2

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run test 01 only

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Byte 3

X'00' Test partition 0
X'00'- X'07' Partition to be tested

Note: Byte 3 must be the number of an installed partition.

Isolation Codes

6A0101: Bit error count per card presented
6A01A0: IR check on a transfer
6A01B0: Communication, common check, or an unsupported check 2
6A01D0: Port check with operation complete on a store operation
6A01D1: Port check with operation complete on a fetch operation
6A01E0: No port check and no operation complete on a store operation
6A01E1: No port check and no operation complete on a fetch operation
6A01F0: Port check and no operation complete on a store operation
6A01F1: Port check and no operation complete on a fetch operation

Error Display Bytes

Error Code: 6A0101

- E1 = Test ID
- E2 = Error code
- E3 = Partition number
- E4-E6 = Bit Error Count - Card 1
- E7-E9 = Bit Error Count - Card 2
- EA-EC = Bit Error Count - Card 3
- ED-EF = Bit Error Count - Card 4

Error Code: 6A01A0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = SP OP read IR ck (CSPRDIC)
- E5 = Common port adpt ck 1 (CPACK1)
- E6 = Common port adpt ck 2 (CPACK2)
- E7 = ADT/ASDM check (CAAJCK)
- E8 = Communication adpt ck (CCOMACK)
- E9 = Common stor addr ck (CSACK)
- EA = Multiple IR addr decode (CMADEC)

Error Code: 6A01B0

- E1 = Test ID
- E2 = Error code
- E3 = Common status 1 (CSTAT1)
- E4 = Common status 3 (CSTAT3)
- E5 = Communication adpt ck (CCOMACK)
- E6 = Common stg addr ck (CSACK)
- E7 = Common stg control ck (CSCCK)
- E8 = Common stg addr ref ck (CSARCK)
- E9 = Common stg card ref addr ck (CSCRACK)
- EA = Multiple IR addr decode (CMADEC)

Error Codes: 6A01D0, 6A01D1, 6A01F0, 6A01F1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - check registers are upper port
  X'80' - check registers are lower port
- E4 = Common status 1 (CSTAT1)
- E5 = Port adapt ck (U/LPACK)
- E6 = Port buffer ck (U/LPBCK)
- E7 = SSAR0 (U/LSSAR0)
- E8 = SSAR1 (U/LSSAR1)
- E9 = SSAR2 (U/LSSAR2)
- EA = Storage adapt ck (U/LSADPCK)
- EB = Storage card addr ck (U/LSCACK)
- EC = ECC ck (U/LECCCK)
- ED = Storage control ck (U/LSCCK)

Error Codes: 6A01E0, 6A01E1

- E1 = Test ID
- E2 = Error code
- E3 = X'00' - upper port timeout
  X'80' - lower port timeout

Routine 6B Test 01

Description

This test checks the integrity of the 1B register by writing a walking ones pattern and then doing a read.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0107: Address in 1B register not correct

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 02

Description

This test checks that the 1B register is incremented after a 'WRF' instruction. Addresses X'83, 86, A3, A6, and FF' are loaded in to the 1B register and a WRF instruction is executed. The 1B register is then read to check that it was incremented. The 1B shadow register is also read to check that it was incremented.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0207: Address in 1B register not correct
6B0208: Read of UOPCLT not as expected
6B020B: Address in the 1B shadow register did not increment after a WRF instruction
6B020E: Address in the 1B register did not increment after a WRF instruction

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 03

Description

This test will force a port adapter IR check (bit 0 of register CPACK1) in the following two ways.

1. Set CCOMADI = X'19' and then read a register within this card. This simulates both W/R gates active.
2. Set CCOMADI = X'1C' and then read a register within this card. This simulates no R/W gates active.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0302: CPACK2 register indicates an error
6B0303: CHK register indicates an error
6B0306: CPACK1 register indicates an error
6B0310: PA IR check did not get set in CPACK1
6B0311: PORT connection ADT check did not get set in CHK
6B0312: CHECK-2 register did not get set in XCS
6B0315: CSPRDIC register indicates an error
6B0316: PA IR SUM check did not get set in CSPRIDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 04

Description

This test will force a port adapter IR check (bit 0 of register CPACK1) in the following two ways.

1. Set CCOMADI = X'1A' and write to an addressable register on this card. This simulates a parity check on the IR address bus.
2. Set CCOMADI = X'1F' and write to an addressable register on this card. This simulates a decoder check on the IR address bus.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0402: CPACK2 register indicates an error
6B0403: CHK register indicates an error
6B0406: CPACK1 register indicates an error
6B0410: PA IR check did not get set in CPACK1
6B0411: Port connection ADT check did not get set in CHK
6B0412: CHECK-2 did not get set in XCS
6B0415: CSPRDIC register indicates an error
6B0416: PA IR SUM check did not get set in CSPRIDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 05

Description

This test will force a port adapter IR check (bit 0 of register CPACK1) in the following two ways.

1. Set CCOMADI = X'1E' and write to an addressable register on this card. This simulates an address decoder check.
2. Set CCOMADI = X'1B' and write to an addressable register on this card. This simulates a parity check. (X'1B' will also cause a IR data out parity check, bit 4 of register CPACK1)

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0502: CPACK2 register indicates an error
6B0503: CHK register indicates an error
6B0506: CPACK1 register indicates an error
6B0510: PA IR check did not get set in CPACK1
6B0511: Port connection ADT check did not get set in CHK
6B0512: CHECK-2 did not get set in XCS
6B0515: CSPRDIC register indicates an error
6B0516: PA IR SUM check did not get set in CSPRIDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 06

Description

This test forces an SMD ALU out parity check (bit 1 of register CPACK1) and a RDF register read parity check (bit 7 of register CPACK1). The SMD parity check is forced by setting CCOMADI = X'16' and writing to an addressable register on this card with an odd number of bits. The RDF parity check is forced by reading the register that was written in the first part of the test. (The SDM ALU out parity check will also cause a PA IR check and a IR data out parity check.)

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0602: CPACK2 register indicates an error
6B0603: CHK register indicates an error
6B0606: CPACK1 register indicates an error
6B0610: SDM ALU out/RDF register parity check did not get set in CPACK1
6B0611: Port connection ADT check did not get set in CHK
6B0612: CHECK-2 did not get set in XCS
6B0615: CSPRDIC register indicates an error
6B0616: PA IR SUM check did not get set in CSPRIDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Diagnostic Tests DC 6B04

Routine 6B Test 07

Description

This test forces an external register address or decoder check (bit 2 of register CPACK1) following two ways:

1. Set CCOMADI = X'17' and write to the 1B register.
2. Set CCOMADI = X'10' setting this will immediately force the error. This setting will also cause a ALU out control check (bit 6 of register CPACK1).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0702: CPACK2 register indicates an error
6B0703: CHK register indicates an error
6B0706: CPACK1 register indicates an error
6B0710: EXT register address/decoder check/ALU out control check did not get set in CPACK1
6B0711: Port connection ADT check did not get set in CHK
6B0712: CHECK-2 did not get set in XCS
6B0715: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 08

Description

This test forces an external register selection check (bit 3 or register CPACK1) by setting CCOMADI =X'0C' and then writing to an addressable register on a card other than the CMCD.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0802: CPACK2 register indicates an error
6B0803: CHK register indicates an error
6B0806: CPACK1 register indicates an error
6B0810: EXT register selection check did not get set in CPACK1
6B0811: Port connection ADT check did not get set in CHK
6B0812: CHECK-2 did not get set in XCS
6B0815: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 09

Description

This test forces an read clock delay check (bit 5 of register CPACK1) by setting CCOMADI =X'14', and reading any addressable register (UOPCTL).

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0902: CPACK2 register indicates an error
6B0903: CHK register indicates an error
6B0906: CPACK1 register indicates an error
6B0910: Read clock delay check did not get set in CPACK1
6B0911: Port connection ADT check did not get set in CHK
6B0912: CHECK-2 did not get set in XCS
6B0915: CSPRDIC register indicates an error
6B0916: PA IR Sum check did not set in CSPRDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 0A

Description

This test forces an ALU out control check (bit 6 of register CPACK1) by setting CCOMADI =X'15'.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0A02: CPACK2 register indicates an error
6B0A03: CHK register indicates an error
6B0A06: CPACK1 register indicates an error
6B0A10: ALU out control check did not get set in CPACK1
6B0A11: Port connection ADT check did not get set in CHK
6B0A12: CHECK-2 did not get set in XCS
6B0A15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 0B

Description

This test forces a clock check (bit 4 of register CPACK2) by setting CCOMADI =X'08'.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0B02: CPACK2 register indicates an error
6B0B03: CHK register indicates an error
6B0B06: CPACK1 register indicates an error
6B0B10: Clock check did not get set in set CPACK2
6B0B11: Port connection ADT check did not get set in CHK
6B0B12: CHECK-2 did not get set in XCS
6B0B15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Routine 6B Test 0C

Description

This test forces a CD duplicate IR address decode check (bit 5 of register CPACK2) by setting CCOMADI =X'18' and writing to a register on this card.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0C02: CPACK2 register indicates an error
6B0C03: CHK register indicates an error
6B0C06: CPACK1 register indicates an error
6B0C10: DC duplicate IR address decode check did not get set in set CPACK2
6B0C11: Port connection ADT check did not get set in CHK
6B0C12: CHECK-2 did not get set in XCS
6B0C15: CSPRDIC register indicates an error
6B0C16: PA IR summary check did not get set in CSPRDIC

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Diagnostic Tests DC 6B0D

Routine 6B Test 0D

Description

This test forces a range select check (bit 7 of register CPACK2) by setting CCOMADI =X'0D' and setting the ADT buffer address to X'4000'.

Parameters

Byte 1

X'00' (default) = Run all tests in this routine
X'01' Run only test 01

Byte 2

Bit 0 - 0 Run selected test once
- 1 Loop selected test
Bit 1 - 0 Display errors
- 1 Do not display errors

Isolation Codes

6B0D02: CPACK2 register indicates an error
6B0D03: CHK register indicates an error
6B0D06: CPACK1 register indicates an error
6B0D08: Range select check should not be on
6B0D10: Range select check did not get set in CPACK2
6B0D11: Port connection ADT check did not get set in CHK
6B0D12: CHECK-2 did not get set in XCS
6B0D15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = expected
- E4 = received

Diagnostic Tests DC 6B0D

Diagnostic Routine 70 Information and Execution Procedures

Descriptive Name

Function tests

Description

Routine 70 provides the same testing as IML hardcore tests 01 through 20. It also provides the ability to loop on specific tests and allows run options and parameters to be specified.

Routine 70 has some special control storage diagnostics tests 21 through 29.

Refer to DC HC00 for a cross-reference of error codes and test numbers between routine 70 and the IML hardcore tests.

Prerequisites For Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Remove any installed wrap cables.
4. Perform an IML operation.

Diagnostic Parameters

The following optional diagnostic parameters can be specified during the execution of this routine:

Note: If any parameters are specified, all parameter bytes must be specified.

Byte 1: Beginning test ID.
The default is X'01'.

Byte 2: Ending test ID.
The default is X'1F'.
The highest value is X'29'.

Execution Post Requisites

After executing routing 70

1. Perform a IML operation on the 3880

Diagnostic Error Displays

The display format on the MD when running diagnostics under support option 7 is:

```
DIAGNOSTIC DETECTED
AN ERROR. IC=rrttcc
BYTES=E1E2E3E4E5E6E7
E8E9EAEBECEDEEEF

Where: rr = routine ID
       tt = test ID
       cc = error code
```

Those six hex digits make up the isolation codes described under each routine on the following pages. The error display bytes (E1, E2, and so forth) are also described under each routine.

Hardcore to Routine 70 Test Cross Reference Listing

HARDCORE TEST NUMBER	ROUTINE 70 TEST NUMBER	TEST DESCRIPTION
01	01	Branch Direct
02	02	Branch and Link
03	03	Branch and Link Register
04	04	Branch on Condition
05	05	Jump on Internal Register Bit
06	06	Jump on External Register Bit
07	08	Internal to Internal Register
08	09	Internal Register Immediate
09	0A	External Register
0A	0B	Control Store Op 0
0B	0C	Control Store Op 1
0C	0D	Internal Register Array Fixed
0D	0E	Internal Register Array Variable
0E	--	External Register Reset
0F	0F	External Register Read/Write
10	10	Control Storage Fixed
11	11	Control Storage Variable
12	07	Interrupt Test
13	12	Automatic Data Transfer Buffer Test #1
14	13	Automatic Data Transfer Buffer Test #2
15	14	Automatic Data Transfer Buffer Test #3
16	15	Automatic Data Transfer Buffer to Device Bus Out
17	16	Device Bus In to Automatic Data Transfer
18	17	Automatic Data Transfer Pad/Drop Buffer
19	18	Automatic Data Transfer Padding Circuit
1A	19	Automatic Data Transfer Buffer Wrap
1B	1A	Automatic Data Transfer Buffer to Channel Bus In
1C	1B	Check 2 and Device Overrun
1D	1B	Search Compare Hardware
1E	1D	CSC Card Check
1F	1E	CDX Card Check
20	1F	Interval Timer

Routine 70 Test 01

Description

This test checks the operation of the microprocessor Branch Direct command. It tests that:

- A branch is taken
- A branch is taken to the correct address
- No registers are modified

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700101: Failed to branch
700102: Registers 0-15 not equal zero

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 TEST 02

Description

This test checks the operation of the microprocessor Branch and Link command. It tests that:

- A branch is taken
- IAR+1 is saved in register PR4
- No other registers are modified

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700201: Failed to branch
700202: Registers 0, 1, and 6-16 not zero
700203: Register 4 contents not as expected
700204: Register 5 contents not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 TEST 03

Description

This test checks the operation of the microprocessor Branch and Link Register command.

It tests that:

- A branch is taken to IR1
- IAR+1 is saved in IR2
- No other registers are modified

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700301: Failed to branch
700302: Registers 0-5 and 8-15 not zero

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Diagnostic Tests DC 7001

Routine 70 Test 04

Description

This test checks the operation of the microprocessor Branch on Condition command. It tests that a branch is taken only when appropriate.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700401: Erroneous conditional branch taken

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 Test 05

Description

This test checks the operation of the microprocessor Jump on Internal Register Bit command. It tests that a branch is taken only when appropriate.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700501: Branch on register R0 bit (or bits) not taken
700502: Branch on register R1 bit (or bits) not taken

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 Test 06

Description

This test checks the operation of the microprocessor Jump on External Register Bit command.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700602: Branch on DCL register bit not taken
700603: Erroneous branch on DCL Register bit taken

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 Test 07

Description

This test checks the operation of the microprocessor Interrupt Processing command. It tests:

- The ability to change interrupt levels from:
  - Level 3 to Level 2 to Level 1
  - Level 1 to Level 2, Level 2 to Level 3
  - Level 3 to Level 1
  - Level 1 to Level 3
- That PSWs contents are valid after an interrupt
- That IUR and IRG register contents are valid after an interrupt

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700701: Erroneous interrupt occurred
700702: Interrupt not taken or condition code not valid
700703: Contents of interrupt level register not valid
700704: PSW not valid

Error Display Bytes

- E1 = Test ID
- E2 = Error code

Routine 70 Test 08

Description

This test checks the operation of the microprocessor Internal Register to Internal Register instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700801: Register containing output from ALU has incorrect value
700802: The condition code set following instruction execution is incorrect

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 09

Description

This test checks the operation of the microprocessor Internal Register Immediate instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700901: Register containing output from ALU has incorrect value
700902: The condition code set following instruction execution is incorrect

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 0A

Description

This test checks the operation of the microprocessor External Register instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700A01: The register containing output from ALU has incorrect contents
700A02: The condition code set following instruction execution is incorrect

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 0B

Description

This test checks the operation of the microprocessor Control Store OP 0 instruction. The following are validated.

- Fetch from a known location (correct data loaded)
- Increments address only when it should
- Store does not take place during a fetch operation
- Registers not altered during operation

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700B01: Registers involved in fetch not valid (no increment)
700B02: Registers involved in fetch not valid (increment)
700B03: Registers involved in store not valid (no increment)
700B04: Registers involved in store not valid (increment)
700B05: Registers in group 2 and 3 not valid

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E3 = Received data

Routine 70 Test 0C

Description

This test checks the operation of the microprocessor Control Store OP 1 instruction. The following are validated.

- Fetch from a known location (correct data loaded)
- Increments address only when it should
- Store does not take place during a fetch operation
- Registers not altered during operation

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700C01: Registers involved in fetch not valid (no increment)
700C02: Registers involved in fetch not valid (increment)
700C03: Registers involved in store not valid (no increment)
700C04: Registers involved in store not valid (increment)
700C05: Registers in group 2 and 3 not valid

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 0D

Description

This test checks the microprocessor internal register array. It tests:

- The ability to store various data patterns in each register location
- The ability to fetch from the stored location
- The validity of register selection

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700D01: Data in one of the secondary registers is incorrect

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 0E

Description

This test checks the microprocessor internal register array. It stores a unique data pattern at each register location, then validates the store after every location has been stored into. It tests:

- The ability to store various data patterns in each register location
- The ability to fetch from the stored location
- The validity of register selection

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700E01: Registers involved in fetch not valid

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 0F

Description

This test checks the storage director external registers. It tests the ability to:

- Store and fetch all possible data patterns into the read/write registers
- Store all possible data patterns into the write only registers
- Read a read only register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

700F02: BAP toggle (bit 2 of the TFR register) did not set
700F04: DXA card check (bit 0 of the CHK register) did not set
700F06: BAP toggle (bit 2 of the TFR register) did not reset
700F08: DXA card check (bit 0 of the CHK register) did not reset
700F0A: DXA card check (bit 0 of the CHK register) did not reset
700F10: Data in DBO register not as expected
700F12: Data in DCH register not as expected
700F14: Data in DCL register not as expected
700F16: Data in MCS register not as expected
700F18: Data in RLL register not as expected
700F1A: Data in DTG register not as expected
700F1C: Data in CXC register not as expected
700F1E: Data in CC2 register not as expected
700F20: Data in CBI register not as expected
700F22: Data in CC1 register not as expected
700F24: Data in CS3 register not as expected
700F26: Data in CCH register not as expected
700F28: Data in CCL register not as expected
700F30: CDX card check (bit 2 of the CR0 register) is on
700F34: BAP toggle (bit 2 of the TFR register) is not in the correct state
700F36: DXA card check (bit 0 of the CHK register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Tests DC 700D

Routine 70 Test 10

Description

This test checks the ability to store and fetch various data patterns to and from static and dynamic control storage. Each block (address range) of control storage is stored into prior to fetching for verification.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

70101X: Data fetch from an address in the range X'1000' to X'1FFF' not as expected
70106X: Data fetch from an address in the range X'6000' to X'6FFF' not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 11

Description

This test checks the ability to store and fetch a unique data pattern into each static and dynamic control storage location. All addresses are stored into prior to fetch verification to test for any control storage access decode failures.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

70111X: Data fetch from an address in the range X'1000' to X'1FFF' not as expected
70116X: Data fetch from an address in the range X'6000' to X'6FFF' not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 12

Description

This test checks writing and reading of the ADT buffer using the BFR register. It also tests for pre-fetch failures and array out parity checks.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701202: Address in the BAL register not as expected
701204: Address in the BAH register not as expected
701206: DXA card check (bit 0 of the CHK register) is on
701208: DXD card check (bit 6 of the CHK register) is on
701212: Array out parity check (bit 4 of the CHK register) is on
701218: Array out parity check (bit 4 of the CHK register) did not set
701220: Address in the BAL register not as expected
701222: Address in the BAH register not as expected
701224: Data in the buffer is not as expected
70122A: Clock check (bit 3 of the XES register) or DXD card check (bit 6 of the CHK register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 13

Description

This test checks writing and reading of the ADT buffer using the BFI register. The BAP (buffer pointer) registers are validated as the data is written and read from the ADT buffer.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701302: Address in the BAH register not as expected
701304: Address in the BAL register not as expected
701306: BAP register did not wrap to the correct address of X'0200'
701308: DXA card check (bit 0 of the CHK register) is on
70130A: Array out parity check (bit 4 of the CHK register) is on
70130C: DXD card check (bit 6 of the CHK register) is on
70130E: Data loaded from CFI register not as expected
70132A: Clock check (bit 3 of the XES register) or DXD card check (bit 6 of the CHK register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 14

Description

This test checks writing and reading of the ADT buffer using the CFI register. The CPB (buffer pointer) registers are validated as the data is written and read from the ADT buffer.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701402: Address in the CBH register not as expected
701404: Address in the CBL register not as expected
701406: CBP register did not wrap to the correct address X'0200', or DXA card check (bit 0 of the CHK register) is on
701408: Array out parity check (bit 4 of the CHK register) is on
70140A: DXD card check (bit 6 of the CHK register) is on
70140C: Data loaded from the CFI register is not as expected
70142A: Clock check (bit 3 of the XES register) or DXD card check (bit 6 of the CHK register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 15

Description

This test transfers data from the ADT buffer to the device bus out (DBO) on the DCC card using a two-byte data transfer. It tests:

- The integrity of the data transferred
- The decrement of the device count registers
- The device end of transfer indication
- The presence of any error check indicators during or following the data transfer
- The proper increment of the buffer pointer register (DBP)
- The DRC register
- The suspend DRC operation

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701502: Device buffer check (bit 7 of the XES register) is on
701504: Data in DBO register not as expected
701506: Data in DCH/DCL registers not as expected
70150A: DDC card check (bit 4 of the XES register) is on
70150E: First sync in latch (bit 6 of the XCS register) did not set
701510: DDC end of transfer (bit 2 of the XCS register) did not set
701512: DDC end of transfer (bit 2 of the XCS register) did not set
701514: First sync in latch (bit 6 of the XCS register) did not set
701516: Value in DRC register not as expected
701518: DDC end of transfer (bit 2 of the XCS register) is on
70151A: First sync in latch (bit 6 of the XCS register) did not reset
70151C: Value in DBP register not as expected
701520: Value in DRC register not as expected (reset value)
701522: Device buffer check (bit 7 of the XES register) is on
701524: DXD card check (bit 6 of the CHK register) is on
701526: DXA card check (bit 0 of the CHK register) is on
701528: Value in DRC register not as expected (reset value)
7015B2: Value in DRC register not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 16

Description

This test transfers data from device bus in (DBI) to the ADT buffer using one- and two-byte data transfers. It tests:

- The integrity of the data transferred
- The decrement of the device count registers
- The device end-of-transfer indication
- The presence of any error check indicators during or following the data transfer
- The proper increment of the buffer pointer register (DBP)
- The DRC register
- The suspend DRC operation

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701602: First sync in latch (bit 6 of the XCS register) did not set
701604: Data in BFR register not as expected
701606: Data in DRC register not as expected
701608: Device buffer check (bit 7 of the XES register) is on
70160A: DXD card check (bit 6 of the CHK register) is on
70160C: DXA card check (bit 0 of the CHK register) is on
701636: DCC card check (bit 4 of the XES register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 17

Description

This test checks the ADT pad/drop hardware and validates the following:

- The data transmitted from/to the ADT buffer prior/at/following the pad/drop transition point
- Status and error indications at and following the pad/drop transition point
- Status and error indication following the completion of the data transfer operation

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701710: Device buffer check (bit 7 of the XES register) is on
701712: Data in DBO register not as expected
701714: Data in DBO register not as expected
701716: DDC end of transfer (bit 2 of the XCS register) is on
701718: First sync in latch (bit 6 of the XCS register) is on
701730: Device buffer check (bit 7 of the XES register) is on
701732: Data in DBO register not as expected
70171A: DDC end of transfer (bit 2 of the XCS register) is on
70171C: DDC end of transfer (bit 2 of the XCS register) did not set
70171E: Value in DRC register not as expected
70171F: Value in RLL register not as expected
701720: DDC end of transfer (bit 2 of the XCS register) is on
701722: First sync in latch (bit 6 of the XCS register) is on
701723: DXA card check (bit 0 of the CHK register) is on
701724: Value in DBP register not as expected
70172A: DCC card check (bit 4 of the XES register) or DDC end of transfer (bit 2 of the XES register) is on
70172C: DXD card check (bit 6 of the CHK register) is on, or the contents of the DBP register is not as expected
701728: Value in BFR register not as expected
70172B: Value in RLL register not as expected
70172E: DXA card check (bit 0 of the CHK register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 18 (USED ONLY FOR DCC)

Description

This test checks the device tag out (DTO) register during a transfer of data from the ADT buffer to the device bus out (DBO) register.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701802: Value in DTO register does not equal X'20'
701804: Value in DTO register does not equal X'E0'
701806: Value in DTO register does not equal X'60'

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 19

Description

This test checks:

- The successful increment of the DBH and DBL registers from X'0001' to X'03FF'
- The successful decrement of the DCH and DCL registers from X'0400' to X'0000'
- The wrap of the DBH and DBL registers from X'03FF' to X'0200'
- The device end-of-transfer when the DCH and DCL registers are decremented through X'0000'

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701902: Value in DBP register not as expected
701906: Value in the DCH and DCL registers not as expected
70190A: Value in DBP register does not equal X'020'
70190E: DXA card check (bit 0 of the CHK register) is on
701910: DCT card check (bit 1 of the CHK register) is on
701912: DDC card check (bit 4 of the XCS register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 1A

Description

This test checks transfers from the ADT Buffer to the channel bus in (CBI) register, and status and error indications during and following the transfer.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701A02: BC1 full and BC2 empty (bits 6 and 7 of the TFR register) should be binary '01'
701A04: CDX end-of-transfer (bit 4 of the XCS register) is on
701A06: Channel buffer check (bit 6 of the XES register) is on
701A08: Data in CBI register not as expected
701A0A: CSR Card Check (bit 3 of the CR0 register) is on
701A0C: CDX end-of-transfer (bit 4 of the XCS register) did not set
701A0E: CDX end-of-transfer (bit 4 of the XCS register) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 1B

Description

This test checks the level 2 interrupt hardware and the hardware error checks.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701B02: Level 2 interrupt (bit 2 of the ILR register) is on
701B04: Level 2 interrupt (bit 2 of the ILR register) did not set
701BC8: Level 2 interrupt (bit 2 of the ILR register) is on
701B06: Device overrun (bit 0 of the XES register) did not set
701B08: Device overrun (bit 0 of the XES register) did not reset
701B0A: Device overrun (bit 0 of the XES register) did not set
701B0C: Device overrun (bit 0 of the XES register) did not reset
701B0E: First sync in latch (bit 5 of the XES register) did not set
701B10: First sync in latch (bit 5 of the XES register) did not reset
701B12: Device buffer check (bit 7 of the XES register) did not set
701B14: Device buffer check (bit 7 of the XES register) did not reset
701B16: Channel buffer check (bit 6 of the XES register) did not set
701B18: Channel buffer check (bit 6 of the XES register) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Tests DC 7019

Routine 70 Test 1C

Description

This test checks the search compare hardware. It checks that a compare successful condition comes on during a one-byte data transfer to the CBI register and that the compare successful indicator can be reset.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701C02: Compare successful (bit 5 of the XCS register) did not set
701C04: Compare successful (bit 5 of the XCS register) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 1D

Description

This test checks the CSC card check hardware. It validates that channel check 1 (bit 7 of the CS2 register) causes a level 1 interrupt condition. The channel check is caused by turning on microprocessor service in (bit 0 of the CXC register) and status in (bit 2 of the CC1 register) simultaneously.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701D01: CSC card check and channel check 1 (bits 4 and 7 of the CS2 register) should be on
701D02: Level 1 interrupt (bit 1 of the ILR register) should be on

Error Display Bytes

Format of Error Display

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 1E

Description

This test checks the CDX card check hardware. It validates that channel check 1 (bit 7 of the CS2 register) causes a level 1 interrupt condition. The channel check is caused by turning on set speed control register and allow run channel (bits 4 and 5 of the CXC register) simultaneously.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701E01: CDX card check (bit 2 of the CRO register) did not set
701E02: Level 1 interrupt (bit 1 of the ILR register) did not set

Error Display Bytes

Format of Error Display

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 1F

Description

This test checks that a timer interrupt occurs within the specified tolerance, 650 milliseconds +30% -20%, and that the timer, once enabled, can be disabled.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

701F01: Level 1 interrupt (bit 1 of the ILR register) did not set
701F02: The time interval for the interrupt is too short
701F03: The time interval for the interrupt is too long
701F04: Level 1 interrupt (bit 1 of the ILR register) should not be on

Error Display Bytes

Format of Error Display

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 20

Description

This test is resident in static control storage and is used to test all dynamic control storage using selected data patterns.

Note: This test is not part of the normal routine 70 linked series and must be selected via parameter entry. Running of this test requires an IML to execute any subsequent routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702002: Data fetched does not equal the data stored

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 21

Description

This test is resident in static control storage and is used to test all dynamic control storage using unique data patterns at each storage location to check for decoder failures.

The data pattern stored at each location is the address of the location being stored into.

Note: This test is not part of the normal routine 70 linked series and must be selected via parameter entry. Running of this test requires an IML to execute any subsequent routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702102: Data fetched does not equal the data stored

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 22

Description

This test is resident in dynamic control storage and is used to validate all of static control storage using selected data patterns.

Note: This test is not part of the normal routine 70 linked series, and must be selected using parameter entry. Running of this test requires an IML to execute any routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702202: Data fetched does not equal the data stored

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Received data
- E4 = Expected data

Routine 70 Test 23

Description

This test is resident in dynamic control storage and is used to check for address decoder failures in static control storage. Each location is loaded with its own address then read back and verified.

Note: This test is not part of the normal routine 70 linked series, and must be selected using parameter entry. Running of this test requires an IML to execute any routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702302: Data fetched does not equal the data stored

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Received data
- E4 = Expected data

Routine 70 Test 24

Description

This test is resident in dynamic control storage and is used to validate all of static control storage using unique data patterns stored successively at each location. Following each store, the remainder of memory is validated to insure that it remained unaltered as a result of a store into the location currently under test.

Note: This test takes 60 seconds to execute. This test is not part of the routine 70 linked series and must be selected using parameter entry. Running of this test requires an IML to execute any routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702402: Data fetched does not equal the data stored
702404: Data in address block should equal X'5555'

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Received data
- E4 = Expected data

Diagnostic Tests DC 7022

Routine 70 Test 25

Description

This test is resident in static control storage and is used to test the dynamic control storage for an excessive number of ECC correctable storage checks.

Note: This test is not part of the normal routine 70 linked series and must be selected via parameter entry. Running of this test requires an IML to execute any subsequent routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702502: An excessive number of ECC correctable storage checks occurred

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 26

Description

This test is resident in static control storage and is used to test all dynamic control storage. Special data patterns are stored successively at each location, then all other locations are validated for no modification as a result of a store in the location under test.

Note: This test takes 150 seconds to execute. It is not part of the normal routine 70 linked series, and must be selected via parameter entry. Running of this test requires an IML to execute any subsequent routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702602: Data fetched does not equal the data stored
702604: Data in address block should be X'5555'.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 70 Test 28

Description

This test is resident in dynamic control storage and is used to validate all of static control storage using unique data patterns stored successively at each location. Following each store, the remainder of memory is validated to insure that it remained unaltered as a result of a store into the location currently under test.

Note: This test takes three minutes per card to execute. This test is not part of the routine 70 linked series and must be selected using parameter entry. Running of this test requires an IML to execute any routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702802: Data fetched does not equal the data stored
702804: Data in address block should equal X'5555'

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Received data
- E4 = Expected data

Routine 70 Test 29

Description

This test is resident in static control storage and is used to count the number of ECC correctable checks in dynamic control storage.

Note: This test is not part of the normal routine 70 linked series and must be selected via parameter entry. Running of this test requires an IML to execute any subsequent routine or test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

702901: Read data check not zero (bit 3 of register XCS)

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Error count high
- E4 = Error count low

Diagnostic Tests DC 7028

Diagnostic Routine 71 Information and Execution Procedures

Descriptive Name

Control Interface (CTL-I) Wrap Diagnostic

Description

The control interface wrap diagnostic provides extended testing of the 3880 CTL-I hardware by wrapping the outbound lines to the inbound lines using an external wrap cable. In addition, the wrap cable may be installed at the device controller for use in isolating cable and device interface failures.

Prerequisites for Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Install the control interface wrap cable.
4. Perform an IML operation.

Diagnostic Parameters

The following diagnostic parameters can be optionally specified during the execution of this routine.

Note: If any parameters are specified, all parameter bytes must be specified.

Byte 1: Beginning test number. The default is X'01' if not specified.

Byte 2: Ending test number. The default is X'06' if not specified. The highest value is X'07'.

Diagnostic Error Displays

Refer to pages DC 71xx for description of isolation codes.

Wrap Cable Installation

Refer to CTL-I section in the ECM manual for control interface wrap connection diagram.

Refer to the CARR section of the MIM manual for control interface wrap cable installation procedures.

Routine 71 Test 00

Description

This portion of routine 71 performs the following functions:

- Loads remaining overlays of the routine from the diskette into control storage
- Processes and verifies parameters entered
- Selects and executes each test in the routine sequentially
- Formats error displays and takes error exits to COLIC
- Tests for outstanding check 1 or check 2 errors following test execution
- Initializes registers prior to each test execution

Isolation Codes

710001: Invalid parameters were entered for this routine
710002: Error return code on return from overlay loader
71xxF8: Check 2 (bit 0 of register XCS) is on. This occurred in test xx.

Diagnostic Tests DC 7100

Routine 71 Test 01

Description

This test wraps the device bus out (DBO) to the device bus in (DBI) and checks for continuity, shorts and permanent errors.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710110: DBI data is not X'00'
710111: DBI data is not X'FF'
710112: DBI data is not X'01'
710113: DBI data is not X'02'
710114: DBI data is not X'04'
710115: DBI data is not X'08'
710116: DBI data is not X'10'
710117: DBI data is not X'20'
710118: DBI data is not X'80'
710119: DBI data is not X'00'
71011E: Check 2 (bit 0 of register XCS) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 71 Test 02

Description

This test checks the CTL-I cable for continuity, shorts and permanent errors.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710220: Device in tag register (DTI) is not X'00'
710221: Bit 0 of DTI register is not on (wrapped from bit 0 of device tag out register DTO)
710222: Bit 1 of DTI register is not on (wrapped from bit 4 of DTO register)
710223: Bit 4 of DTI register is not on (wrapped from bit 5 of DTO register)
710224: Bit 2 of DTI register is not on (wrapped from bit 6 of DTO register)
710225: Bit 6 of DTI register is not on (wrapped from bits 1,2 of DTO register)
710226: Bit 7 of DTI register is not on (wrapped from bit 6 of DTO register)
710227: Bit 6 of DTI register is not on (wrapped from bit 2 of DTO register)
710228: Bit 3 of DTI register is not on (wrapped from bit 0 of DTO register)
71022A: Check 2 (bit 0 of register XCS) is on
71022B: CTL-I sync in check (bit 5 of register XES) did not set
71022E: Check 2 (bit 0 of register XCS) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 71 Test 03

Description

This test checks the sync out function. A diagnostic sync in generates the sync out which is wrapped to the index latch.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710330: Device in tag register (DTI) is not X'00'
710332: Bit 1 of DTI register is not on (wrapped from bit 7 of DTG register)
710334: Bit 1 of DTI register is not on (wrapped from bit 7 of DXC register)
710336: Bits 1,6 of DTI register is not on (wrapped from bits 1,2,6 of DTG register)
710338: Device in tag register (DTI) is not X'00'
71033E: Check 2 (bit 0 of register XCS) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Tests DC 7101

Routine 71 Test 04

Description

This test checks that the recycle line is active when the DCL and DCH count is 8 or more. The recycle line is wrapped to tag valid. This test also checks the ability of the byte counter to decrement properly.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710441: DCH register is not X'FF'
710442: DCL register is not X'FF'
710443: DCH register is not X'FF'
710444: DCL register is not X'FF'
710445: DCH register contents is not equal to contents in R2
710446: DCL register contents is not equal to contents in R3
710447: Bit 1 of register DTI should be reset if PR2 not less than 7
710448: Bit 1 of register DTI should be set if PR2 not less than 7
71044A: CTL-I end of transfer (bit 2 of register XCS) is off
71044B: First sync in latch (bit 6 of register XCS) is off
71044E: Check 2 (bit 0 of register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 71 Test 05

Description

This test checks that the CTL-I hardware sets sync in check if any sync in is received after the DCH and DCL count reaches zero. This test will provide a sync in after the DCH and DCL count has reached zero to ensure that the sync in check circuitry works.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710550: XES register is not X'00'
710551: End of transfer and first sync in latch (bits 2 and 6 of register XCS) should both be on
710552: Sync in Check (bit 5 of register XES) did not set
710553: Check 2 (bit 0 of register XCS) did not set
71055E: Check 2 (bit 0 of register XCS) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 71 Test 06

Description

This test checks that the recycle line is active when the DCL and DCH count is 8 or more. The recycle line is wrapped to tag valid. This test also checks the ability of the byte counter to decrement properly.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710661: DCH register is not X'FF'
710662: DCL register is not X'FF'
710663: DCH register is not X'FF'
710664: DCL register is not X'FF'
710665: DCH register is not equal to value in R2
710666: DCL register is not equal to value in R3
710667: Bit 1 of register DTI should be reset if PR2 less than 7
710668: Bit 1 of register DTI should be set if PR2 greater than 7
710669: CTL-I end of transfer (bit 2 of register XCS) did not set
71066A: First sync in latch (bit 6 of register XCS) did not set
71066E: Check 2 (bit 0 of register XCS) is off

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Tests DC 7104

Routine 71 Test 07

Description

This test is used for scoping the CTL-I interface. The bits in the DTO and DBO registers are set and reset then wrapped back to the DBI and DTI registers.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

710710: DBI register is not X'00'
710711: DBI register is not X'FF'
710721: Bit 0 of register DTI is not on (wrapped from bit 0 of register DTO)
710722: Bit 1 of register DTI is not on (wrapped from bit 4 of register DTO)
710723: Bit 4 of register DTI is not on (wrapped from bit 5 of register DTO)
710724: Bit 2 of register DTI is not on (wrapped from bit 6 of register DTO)
710726: Bit 7 of register DTI is not on (wrapped from bit 7 of register MCR)
710727: Bit 6 of register DTI is not on (wrapped from bit 2 of register DTG)
71077E: CTL-I end of transfer (bit 2 of register XCS) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Routine 72 Information and Execution Procedures

Descriptive Name

Inline Display Utility

Description

The inline display utility is used by the MD to access data in control storage of a selected storage director concurrent with the customer operation. See Diagnostic Error Displays on DC 7000 for a description of data displayed by this routine.

Each test in this diagnostic will fail in order to display sense information. These error stops do not indicate actual errors and are not intended to be used to analyze symptoms.

Note: In support mode, diagnostic option "SS" (read stored SD sense data) can be selected to display useful sense data. See MD section in the MSM for more information.

Diagnostic Parameters

A single parameter byte is used when running this routine. Refer to the 'Parameter Entry' column in the following charts for the parameter byte used for each display. If the parameter byte is not specified, the default is 'A0'.

Prerequisites for Execution

This routine runs concurrently with customer operation on either storage director. There are no prerequisites for this routine.

Routine 72 Displays

- Only 16 bytes of information will be displayed by the MD when running Diagnostic 72 with the entry of A0 and B0. Use the "SS" (read stored SD sense data) command to get all 24 bytes of information, for parameters A0 and B0.
- Only those display bytes mentioned in the following table are of importance, all other bytes shown by the MD should be ignored. Notice that byte E2 is not used in this table.

PARAMETER ENTRY	DISPLAY BYTE												
	E1	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE
A0 1st Half	A0	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10	Byte 11
	ALTERNATE STORAGE DIRECTOR FORMAT 3 SENSE DATA												
A0 2nd Half	A0	Byte 12	Byte 13	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19	Byte 20	Byte 21	Byte 22	Byte 23
	ALTERNATE STORAGE DIRECTOR FORMAT 3 SENSE DATA												
B0 1st Half	B0	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10	Byte 11
	SELECTED STORAGE DIRECTOR SENSE DATA												
B0 2nd Half	B0	Byte 12	Byte 13	Byte 14	Byte 15	Byte 16	Byte 17	Byte 18	Byte 19	Byte 20	Byte 21	Byte 22	Byte 23
	SELECTED STORAGE DIRECTOR SENSE DATA												
C0	C0	xx	Byte E3 is the controller and device address used on the controller and device selection tags										
D0	D0	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6					
	FUNCTIONAL MICROCODE PART NUMBER												
E0	E0	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5						
	FUNCTIONAL MICROCODE EC NUMBER												
AF	xx	Byte E1 is the message format (byte 7) of the alternate storage director format 3 sense data.											
BF	xx	Byte E1 is the message format (byte 7) of the last sense data issued by the storage director.											

PARAMETER ENTRY	DISPLAY Byte												
	E1	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE
10	10	xx	xx	Byte E3: Alternate SD test pattern transmitted Byte E4: Alternate SD test pattern received									
20	20	xx	xx	Byte E3: Bit 0=1 Indicates error detected in IML SD-SD maintenance connection test Bits 2-4 = Diskette seek error count Bits 5-7 = Diskette read error count Byte E4: IML code from alternate SD IML									
01	01	xx	Byte E3 is the contents of the storage director identification register (complemented)										
02	02	xx	Byte E3 is the contents of the storage director IML external register										
03	03	yy	zz	yy	zz	yy	zz	yy	zz				
		Channel A		Channel B		Channel C		Channel D					
05	05	yy	zz	yy	zz	yy	zz	yy	zz				
		Channel E		Channel F		Channel G		Channel H					
04	04	0	1	2	3	Bytes E3 to E6 contain the contingent connection control block information							
40 to 7F	40 to 7F	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7				
		Maintenance connection trace table data where parameter byte '40' displays first 8 bytes, '41' the second 8 bytes and so on											

xx = Variable hexadecimal data
yy = SD address derived from CB0 regsiter during reset (delimiter bit not included)
zz = Highest valid service address for the channel derived from yy

Introduction

Diagnostic Routine 75 Information and Execution Procedures

Descriptive Name

T3880B OLT Microcode Support

Description

The T3880B OLT Microcode Support Routine provides the functional microcode to support the T3880B online test. This routine is used to test the following:

- Disconnect In processing
- Mark-In and control unit retry
- Channel unit control word (UCW) plugged shared or unshared

Prerequisites for Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Remove any installed wrap cables.
4. Perform an IML operation.
5. Enable the channel to be tested at the operator panel.
6. See the PROG section in the MIM for OLT selection and running instructions.

Diagnostic Parameters

Routine 75 uses no parameters.

Diagnostic Error Displays

This routine issues a single error display byte, E1.

Diagnostic Tests DC 7501

Routine 75 Test 01

Description

This routine is used with OLT T3880B and it processes the special CCW commands issued by the OLT used in the testing of:

- Mark In tag and CU retry
- UCW plug share and unshared testing
- Disconnect In selective reset

Isolation Codes

750100: Channel switch locked (bit 4 of register CC2) is on
750200: Address out and select out trapped (bits 1 and 4 of register CS1) should be on
750400: Halt I/O (bit 0 of register CS2) should not be on
750500: Selective reset (bit 1 of register CS2) did not occur after a channel Check 1 (bit 7 of register CS2)
750600: Halt I/O (bit 0 of register CS2) and command out (bit 2 of register CS1) should not be on
750800: Select out trapped (bit 4 of register CS1) did not set
750B00: Command chain aborted (bit 1 of register CS3) should not be on
750C00: Command out value is not X'C2'
750D00: Command chain aborted (bit 1 of register CS3) should not be on
750E00: Command out value is not X'D6'

Diagnostic Tests DC 7501

Diagnostic Routine 77 Information and Execution Procedures

Descriptive Name

Bidirectional Control Interface Wrap Diagnostic (Model 23)

Description

This routine provides extended testing of the Model 23 bidirectional control interface hardware. It connects the outbound lines to the inpbound lines using an external wrap cable. In addition, the wrap cable may be installed at the device controller for use in isolating cable and device interface failures.

Prerequisites for Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Install the control interface wrap cable.

   Note: Refer to Control Interface Wrap Cable Connection in the CARR section of the MIM for installation procedures. Refer to Control Interface Wrap Connection of the CTL-I section of this (ECM) manual for a connection diagram.

4. Perform an IML operation.

Diagnostic Error Displays

770001: Parameters entered are not valid
770002: Return code from microcode overlay loader was not zero

Routine 77 Test 01

Description

This test wraps data bus out to data bus in to test the tag-out drivers and tag-in connection check alert receivers. It also tests the tag-in decoding circuitry. The tag and bus lines are switched on and off for use in scoping.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

770101: DBI register not as expected
770102: Bit 4 of the DTI register (null disconnect state) not on
770103: DBI register not as expected
770104: Bit 5 of the DTI register (valid/sync in) not on
770106: Bit 6 of the DTI register (selected null) not on
770108: Bit 7 of the DTI register (end op) not on
77010A: Bit 4 of the DTI register (null disconnect state) not on
77010C: Bit 0 of the XCS register (check 2 errors) is on
77010E: DTI register does not contain X'61' (sequence check and end op)
770110: Bit 0 of the XCS register (check 2 errors) is not on
770112: DTI register does not contain X'A1' (connection check alert and end op)
770114: Bit 0 of the XCS register (check 2 errors) is not on
77011E: Bit 5 of the DTI register (valid/sync in) not on
77012E: Bit 2 or 4 of the XES register (interface checks) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 77 Test 02

Description

This test checks that a sync out can be generated with a diagnostic sync in. The stop (recycle) function is also checked.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

770202: DTI register does not contain X'C8' (connection check alert and null disconnect)
770204: DTI register does not contain X'C1' (connection check alert and end op)
770206: DTI register does not contain X'C2' (connection check alert and selected null), or bit 6 of the XES register (DXR bus in check) not on
770208: DTI register does not contain X'81' (connection check alert and end op)
77020A: DCL register does not contain X'08'
77020C: DCH register does not contain X'FF'
77020E: DCL register does not contain X'FF'
770210: DCH register not as expected
770212: DCL register not as expected
770214: XCS register does not contain X'22' (end of transfer and 1st sync in)
770216: XES register bit 2 or 5 (sync in check) not on
770218: DTI register does not contain X'81' (connection check alert and end op)
77021E: XES register bit 2 or 4 (interface check) on
77022E: XCS register bit 0 (check 2 error) on
77023E: DTI register bit 1 (tag sequence check) on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7800

Diagnostic Routine 78 information and Execution Procedures

Descriptive Name

Electronic Channel Wrap Diagnostic

Description

The electronic channel interface diagnostic provides extended testing of the channel and automatic data transfer hardware. This routine uses the electronic channel wrap hardware. Routine 78 does not require the connection of an external wrap cable.

Note: Diagnostic routine 78 does not have tests 1F or 20.

Prerequisites for Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Perform an IML operation.

Diagnostic Parameters

The following diagnostic parameters can be specified during the execution of this routine.

Note: If any parameters are specified, all parameter bytes must be specified.

Byte 1 - Beginning test ID (the default is X'01' if not specified)

Note: Test 00 does not test hardware logic

Byte 2 - Ending test ID (the default is X'21' if not specified)

Note: When running from the maintenance device under support option 7, parameters are entered under the control of MD prompting.

Diagnostic Error Displays

Refer to pages DC 78xx for a description of isolation codes.

Routine 78 Test 00

Description

This portion of routine 78 performs the following functions:

- Loads remaining overlays of the routine from the diskette into control storage
- Processes and verifies the parameters entered
- Establishes system reset trap for system/selective resets
- Reads the channel address switches by performing a system reset
- Selects and executes each test in the routine sequentially
- Formats error displays and takes error exits to COLIC
- Tests for outstanding check 1 or check 2 errors following the test execution
- Initializes registers prior to each test execution

Isolation Codes

780001: Invalid parameters were entered
780002: Unexpected error upon return from overlay loader
7800F0: No system reset occurred after dropping OP Out
7800F2: Level 1 interrupt (bit 1 of register ILR) was set because of check 1 condition
78XXF4: Level 1 interrupt (bit 1 of register ILR) was set because of check 1 condition
78XXF8: Check 2 (bit 0 of register XCS) is on

Routine 78 TEST 01

Description

This test checks the system reset function by forcing a system reset by dropping OP Out, then validates that:

- Active inhibit SD reset (bit 3 of register CSTAT3) will delay system reset by 57-114 milliseconds
- A system reset is performed (IAR set to X'0000').
- Channel switch locked is present and the address presented is valid
- The system reset indicator is present (CS2 register bit 2)

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780110: No system reset occurred after dropping OP Out
780111: System reset occurred before 57 milliseconds
780112: Channel switch locked (bit 4 of register CC2) did not set
780113: Active inhibit SD reset (bit 3 of register CSTAT3) did not set
780114: CC2 does not have a valid channel address
780115: System reset occurred after 114 milliseconds
780116: System Reset (bit 2 of register CS2) did not set
780117: Active inhibit SD reset (bit 3 of register CSTAT3) did not reset
780118: Timer overflow (bit 4 of register CSTAT4) did not reset
780119: Timer overflow (bit 4 of register CSTAT4) did not set
78011A: The microcode timer expired before the timer overflow set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7801Dx or 7801Ex, see page DC 78SL.

Routine 78 Test 02

Description

This channel wrap diagnostic test checks for active bus and tag in and out lines and also that the channel registers are not selected. This test checks that the following registers contain X'00':

- CC1, CC2, CR0, CR1
- CR2, CR3, CR6, CS1
- CS2, CXC, CBO, CBI

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780210: CC1 register reset value is not correct
780212: CC2 register reset value is not correct
780214: CR0 register reset value is not correct
780218: CR2 register reset value is not correct
78021A: CR3 register reset value is not correct
78021C: CR6 register reset value is not correct
78021E: CS1 register reset value is not correct
780220: CS2 register reset value is not correct
780224: CXC register reset value is not correct
780230: Wrap tag in control register should equal zero
780232: Wrap bus in control register should equal zero
780234: Data in CBO register does not equal the expected data
780236: Data in CBO register does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7802Dx or 7802Ex, see page DC 78SL.

Routine 78 Test 03

Description

This channel wrap diagnostic test checks the control unit initiated selection using unsuppressable request in. The test validates the following:

- Request in present following raising of unsuppressable request in
- Select out is propagated after raising select-out/hold-out.
- Channel switch locked is present
- Select out trapped is present
- Level 2 interrupt occurs (new level in ILR register)
- Select out trapped drops after propagating select out

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780310: Request in (bit 0 of register DTI) did not set
780312: Select out propagated (bit 6 of register) did not set
780314: Channel switch locked (bit 4 of register CC2) did not set
780316: Select out trapped and suppress out (bits 4 and 7 of register CS1) should be on
780318: New level 2 (bit 2 of register ILR) did not set
78031A: Select out propagated (bit 6 of register DTI) did not set
78031C: Select out trapped (bit 4 of register CS1) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7803Dx or 7803Ex, see page DC 78SL.

Routine 78 Test 04

Description

This channel wrap diagnostic test checks for active bus and tag in and out lines and also that the channel register states are selected. The test validates these registers after a CU initiated selection:

- CC1, CC2, CR0, CR1
- CR2, CR3, CR6, CS1
- CS2, CXC, CBO, CBI

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780410: Request in (bit 0 of register DTI) did not set
780412: Channel switch locked (bit 4 of register CC2) did not set
780414: OP in and Mark in (bits 3 and 6 of register DTI) should be on
780416: CR0 register bits 0 through 4 should be off
780418: CS2 register bits 3 through 7 should be off
78041A: CS2 register bits 0 through 2 should be off
78041E: Channel switch locked (bit 4 of register CS1) did not set
780420: CBO register should be zero
780422: CSR Card Check (bit 3 of register CR0) should not be on
780424: CR3 register should be zero

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7804Dx or 7804Ex, see page DC 78SL.

Routine 78 Test 05

Description

This channel wrap diagnostic test sets suppressible request in then validates that:

- Request in and channel switch locked were set
- A level 2 interrupt was set
- The interrupting channel address is valid

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780510: Channel check 1 (bit 7 of register CS2) is on
780512: Check 2 (bit 0 of register XCS) is on
780514: Request in (bit 0 of register DTI) did not set
780516: Request in (bit 0 of register DTI) did not reset
780518: Request in (bit 0 of register DTI) did not set
78051A: Channel switch locked (bit 4 of register CC2) did not set
78051C: New level 2 interrupt (bit 2 of register ILR) did not set
78051E: Interrupting channel in the CC2 register is the wrong channel
780520: OP in (bit 3 of register DTI) did not set
780522: Mark in (bit 6 of register DTI) did not set
780524: Address in (bit 5 of register DTI) did not set
780526: Command out (bit 2 of register CS1) did not set
780528: CBO register data did not wrap correctly from DBO register
78052A: Check 2 (bit 0 of register XCS) is on
78052C: CSR card check (bit 0 of register CR3) is on
78052E: Bus in parity check and CIF card check (bits 0 and 1 of register CR0) should not be on
780530: Status in (bit 7 of register DTI) did not set
780532: DBI register data did not wrap correctly from CBI register
780534: Check 2 (bit 0 of register XCS) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7805Dx or 7805Ex, see page DC 78SL.

Routine 78 Test 06

Description

This channel wrap diagnostic test checks initial selection and the Halt I/O command.

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780610: OP in (bit 3 of register DTI) did not set
780612: Halt I/O (bit 0 of register CS2) did not set
780614: OP in (bit 3 of register) did not reset
780616: Select out trapped (bit 4 of register CS1) did not reset
780618: Halt I/O (bit 0 of register CS2) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7806Dx or 7806Ex, see page DC 78SL.

Routine 78 Test 07

Description

This channel wrap diagnostic test checks the channel bus in and channel bus out parity check circuitry.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780713: Bus out parity check (bit 5 of register CS2) did not set
780710: Check 2 (bit 0 of register XCS) should not be on
780715: Check 2 (bit 0 of register XCS) should be on
780722: CSR card check (bit 3 of register CR0) did not set
780724: Channel check 1 (bit 7 of register CS2) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 780ADx or 780AEx, see page DC 78SL.

Routine 78 Test 08

Description

This channel wrap diagnostic test checks all possible addresses during selection to ensure that only valid addresses are selected and that invalid addresses are not selected.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780812: Select out trapped (bit 4 of register CS1) did not set
780814: Select out trapped (bit 4 of register CS1) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 780BDx or 780BEx, see page DC 78SL.

Routine 78 Test 09

Description

This channel wrap diagnostic test checks CU busy activation under the following conditions.

- Long select bit on
- CU busy bit on
- Halt I/O bit on

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

780910: Channel switch locked (bit 4 of register CC2) is on
780912: Status in (bit 7 of register DTI) did not set
780914: Status in DBI register is not correct
780916: Status in (bit 7 of register DTI) did not reset
780918: Status in DBI register is not correct
78091A: CS3 register does not contain a valid address for CU end
780920: Status in (bit 7 of register DTI) did not set
780930: Channel switch locked (bit 4 of register CC2) did not set
780932: Halt I/O (bit 0 of register CS2) did not set
780934: Status in (bit 7 of register DTI) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 780CDx or 780CEx, see page DC 78SL.

Routine 78 Test 0A

Description

The selective reset test forces a selective reset by raising suppress out and dropping OP out. This verifies that:

- Active inhibit SD reset will delay the selective reset by 57-114 milliseconds
- Selective reset does occur (IAR set to X'0000')
- Channel switch locked is present and the address presented is valid
- Selective reset indicator is active

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780A10: Selective reset did not occur after OP out was dropped
780A11: Selective reset occurred before 57 milliseconds
780A13: Active inhibit SD reset (bit 3 of register CSTAT3) did not set
780A15: Selective reset occurred after 114 milliseconds
780A17: Active inhibit SD reset (bit 3 of register CSTAT3) did not reset
780A18: Timer overflow (bit 4 of CSTAT4) did not reset
780A19: Timer overflow (bit 4 of CSTAT4) did not set
780A1A: Microcode timer timed out before timer overflow was set
780A1B: Timer overflow (bit 4 of CSTAT4) did not set
780A20: Selective reset (bit 1 of register CS2) did not set
780A22: OP in (bit 3 of register DTI) did not reset
780A24: Select out trapped (bit 4 of register CS1) did not reset
780A30: Status in (bit 7 of register DTI) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 0B

Description

The channel check 1 and disconnect in tests checks the channel check 1 circuits by raising microcode service in, raising address in, then dropping them. The following are verified:

- Check 1 conditions are valid
- That check 1 resets active inhibit SD reset
- That conditions are valid following the presentation of a disconnect in
- CU busy is presented
- Selective reset occurs

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780B10: CSC card check (bit 4 of register CS2) did not set
780B12: Channel check 1 (bit 7 of register CS2) did not set
780B14: Level 1 interrupt (bit 1 of register ILR) did not set
780B15: Active inhibit SD reset (bit 3 of register CSTAT3) did not reset
780B16: Request in (bit 0 of register DTI) did not set
780B18: Channel switch locked (bit 4 of register CC2) did not set
780B1A: Select out trapped (bit 4 of register CS1) did not set
780B1C: Level 2 interrupt (bit 2 of register ILR) did not set
780B1E: OP in (bit 3 of register DTI) did not set
780B20: Address in (bit 5 of register DTI) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 0C

Description

This tests checks channel tag check circuits.

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780C10: Data in (bit 2 of register DTI) did not set
780C12: CSC card check and channel check 1 (bits 4 and 7 of register CSC) should be on
780C14: CSC card check and channel check 1 (bits 4 and 7 of register CSC) should be off
780C20: Data in (bit 2 of register DTI) did not set
780C22: CSC card check and channel check 1 (bits 4 and 7 of register CSC) should be on
780C24: CSC card check and channel check 1 (bits 4 and 7 of register CSC) should be off
780C30: Channel overrun (bit 1 of register XES) did not set
780C32: Check 2 (bit 0 of register XCS) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 0D

Description

This test checks chain re-selection by forcing chain abort.

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

780D50: Status in (bit 7 of register DTI) did not set
780D51: Command out (bit 2 of register CS1) did not set
780D52: Command chain aborted (bit 1 of register CS3) did not set
780D53: Halt I/O (bit 0 of register CS2) did not set
780D54: Command chain aborted (bit 1 of register CS3) did not set
780D55: Status in (bit 7 of register DTI) did not set
780D56: Suppress out (bit 7 of register CS1) did not set
780D57: Select hold (bit 4 of register CS1) did not reset
780D58: Service out (bit 0 of register CS1) did not set
780D59: OP in and status in (bits 3 and 7 of register DTI) did not reset
780D5A: Service out (bit 0 of register CS1) did not set
780D5B: Address out (bit 1 of register CS1) did not set
780D5C: Select hold (bit 4 of register CS1) did not reset
780D5D: OP in (bit 3 of register DTI) did not set
780D5E: Suppress out (bit 7 of register CS1) did not reset
780D5F: Address out (bit 1 of register CS1) did not set
780D60: Address in (bit 5 of register DTI) did not set
780D61: Address in DBI register did not wrap correctly from CBI register
780D62: Command out (bit 2 of register CS1) did not set
780D63: Sequence complete (bit 0 of register CS3) did not set
780D64: Command chain aborted (bit 1 of register CS3) did not set
780D65: CS1 register status has changed since last test
780D66: OP in (bit 3 of register DTI) did not set
780D67: Command out (bit 2 of register CS1) did not reset
780D68: Status in (bit 7 of register DTI) did not set
780D69: Status in (bit 7 of register DTI) did not reset
780D6A: Command chain complete (bit 0 of register CS3) did not set
780D6B: Command chain aborted (bit 1 of register CS3) did not reset

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 780DDx or 780DEx, see page DC 78SL.

Routine 78 Test 10

Description

The read data transfer test transfers data patterns X'01', X'02', X'03', and so on, from subsystem storage locations 001,002,003,...,200 to the channel bus in register (CBI). Each byte is sent via a single byte transfer with microcode toggle of the data and service out lines. The channel transfer rate is 1.14M bytes per second.

Parameters

Byte 1 - Beginning test ID
Byte 2 - Ending test ID

Isolation Codes

781040: Channel check 1 (bit 7 of register CS2) should not be on
781042: CDX end of transfer (bit 4 of register XCS) did not set
781070: Data on CBI is not equal to the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7810Dx or 7810Ex, see page DC 78SL.

Routine 78 Test 11

Description

The electronic channel wrap tests the read data transfer circuitry. This test transfers data patterns X'01', X'02', X'03' and so on, from locations X'0300' to X'03FF', followed by a wrap location X'0200', to channel bus in (CBI). Each byte is sent via a single byte transfer with microcode toggle of the data and service out lines. The channel transfer rate is 1.14M bytes per second.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781140: Channel check 1 (bit 7 of register CS2) should not be on
781142: CDX end of transfer (bit 4 of register XCS) did not set
781170: Data on CBI is not equal to the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7811Dx or 7811Ex, see page DC 78SL.

Routine 78 Test 12

Description

The electronic channel wrap tests the read data transfer circuitry. This test transfers data from the CTL-I interface to the ADT buffer. Data is then transferred from the ADT Buffer to the channel. After the data transfer, the last data byte sent is verified at CBI. This test runs at a channel speed of .568M bytes per second. This test should terminate with no LRC check or check 2 error.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781202: Data on CBI is not equal to the expected data
78120A: Data on CRC/DRC is not equal to the expected data
781232: DCC end of transfer and first sync in latch (bits 2 and 6 of register XCS) should be on
781234: Channel check 1 (bit 7 of register CS2) should not be on
781240: Channel check 1 (bit 7 of register CS2) should not be on
781242: CDX end of transfer (bit 4 of register XCS) did not set
781250: CDX end of transfer (bit 4 of register XCS) did not set
781260: Data in BFR is not equal to the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7812Dx or 7812Ex, see page DC 78SL.

Routine 78 Test 13

Description

The electronic channel wrap tests the read data transfer circuitry. This test transfers data from the CTL-I interface to the ADT Buffer. The first byte is changed in the buffer to cause an LRC check. Data is then transferred from the ADT buffer to the channel. After the data transfer, the last data byte sent is verified at CBI. This test should terminate with an LRC check, and check 2 error.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781302: Data on CBI is not equal to the expected data
781308: Level 2 interrupt (bit 2 of register ILR) should not be on
78130A: Data in CRC and DRC registers are not equal to the expected data
781332: DCC end of transfer and first sync in latch (bits 2 and 6 of register XCS) should be on
781334: Channel check 1 (bit 7 of register CS2) should not be on
781340: Channel check 1 (bit 7 of register CS2) should not be on
781342: CDX end of transfer (bit 4 of register XCS) did not set
781350: CDX end of transfer (bit 4 of register XCS) did not set
781360: Data in BFR register is not equal to the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7813Dx or 7813Ex, see page DC 78SL.

Routine 78 Test 14

Description

The electronic channel wrap tests the write data transfer circuitry. This test transfers data patterns X'02', X'03', X'04', and so on, from the CBO to ADT buffer locations 001, 002....200. Each byte is sent via a single byte transfer with microcode toggle of the data and service out lines. The channel transfer rate is 1.14M bytes per second.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781440: Channel check 1 (bit 7 of register CS2) should not be on
781442: CDX end of transfer (bit 4 of register XCS) did not set
781460: Data in BFR register does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7814Dx or 7814Ex, see page DC 78SL.

Routine 78 Test 15

Description

The electronic channel wrap tests the write data transfer circuitry. This test transfers the data patterns X'02', X'03', X'04', and so on, from the CBO register to the ADT buffer locations X'0301', X'0302',....X'03FF.. Each byte is sent via a single byte transfer with microcode toggle of the data and service out lines. In addition, the ADT wrap from X'03FF' to X'0200' is also verified. The channel transfer rate is 1.14M bytes per second.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781540: Channel check 1 (bit 7 of register CS2) should not be on
781542: CDX end of transfer (bit 4 of register XCS) did not set
781560: Data in BFR register does not equal the expected data

Note: For isolation codes 7815Dx or 7815Ex, see page DC 78SL.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 16

Description

The electronic channel wrap tests the write data transfer circuitry. This test transfers data from the CBO wrap register to the ADT buffer. The ADT buffer data is then verified and transferred from the ADT to the device. Each byte sent is verified at the DBO register. This test runs at a channel speed of .568M bytes per second. This test should terminate with no LRC check, or check 2 error.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

78160A: Data in the CRC and DRC registers do not equal the expected data
781630: Data in the DBO register does not equal the expected data
781632: DCC end of transfer and first sync in latch (bits 2 and 6 of register XCS) should be on
781650: CDX end of transfer (bit 4 of register XCS) did not set
781660: Data in BFR register does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7816Dx or 7816Ex, see page DC 78SL.

Routine 78 Test 17

Description

This electronic channel wrap routine tests the write data transfer circuitry. The test transfers data from the channel to the ADT buffer. Data in the buffer is then changed in the buffer to cause an LRC check. Data is then transferred from the ADT buffer to the device. The test should terminate with an LRC check and a check 2 error.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781708: Level 2 interrupt (bit 2 of register ILR) should not be on
78170A: Data in the CRC and DRC registers do not equal the expected data
781730: Data in the DBO register does not equal the expected data
781732: DCC end of transfer and first sync in latch (bits 2 and 6 of register XCS) should be on
781750: CDX end of transfer (bit 4 of register XCS) did not set
781760: Data in the BFR register does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7817Dx or 7817Ex, see page DC 78SL.

Routine 78 Test 18

Description

This electronic channel wrap routine tests the channel truncation circuitry. The test truncates the first byte of data on a read operation by raising command out in response to the first data byte in.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781804: Pass count is too high
781808: Command out (bit 2 of register CS1) did not set
78180A: Channel truncation (bit 7 of register XCS) did not set
78180C: The number of bytes transferred (4) is not correct
78180E: CDX end of transfer (bit 4 of register XCS) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7818Dx or 7818Ex, see page DC 78SL.

Routine 78 Test 19

Description

This electronic channel wrap routine tests the channel truncation circuitry. The test truncates the second byte of data on a read operation by raising command out in response to the first service in.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781904: Pass count is too high
781908: Command out (bit 2 of register CS1) did not set
78190A: Channel truncation (bit 7 of register XCS) did not set
78190C: The number of bytes transferred (16) is not correct
78190E: CDX end of transfer (bit 4 of register XCS) did not set
781970: Data in the CBI register does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 7819Dx or 7819Ex, see page DC 78SL.

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Routine 78 Test 1A

Description

This electronic channel wrap routine tests the write data transfer circuitry. The test validates channel truncation during write operations. The test truncates the fourth byte during a write transfer by responding to service in with command out.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781A08: Command out (bit 2 of register CS1) did not set
781A0A: Channel truncation (bit 7 of register XCS) did not set
781A30: Data in the DBO register does not equal the expected data
781A40: Check 1 (bit 7 of register CS2) should not be on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 781ADx or 781AEx, see page DC 78SL.

Routine 78 Test 1B

Description

This electronic channel wrap routine tests the channel LRC check circuitry. The test transfers data from the CTL-I interface to the ADT buffer. Data is then transferred from the ADT buffer to the channel. After the third byte of a five byte data transfer, the CBI register contents are changed to force a channel LRC check.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 781BDx or 781BEx, see page DC 78SL.

Isolation Codes

781B02: CDX end of transfer and check 2 (bits 0 and 4 of register XCS) should be on
781B04: Channel data check (bit 3 of register CHK) should be on
781B70: Data in the CBI register does not equal the expected data

Routine 78 Test 1C

Description

This electronic channel wrap routine tests the enable limited buffer circuitry. The test transfers seven bytes of data from the channel to the buffer. The buffer is then validated to ensure that only six bytes of data are transferred. Two bytes of data are then sent from the ADT buffer to the device and the buffer is again validated to ensure that the additional data has been received from the channel.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781C02: Data in the ADT buffer was overlaid (seven bytes of data were transferred instead of six bytes of data)
781C30: Data in the DBO register does not equal the expected data
781C40: Check 1 (bit 7 of register CS2) should not be on
781C60: Data in the ADT buffer does not equal the expected data

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Note: For isolation codes 781CDx or 781CEx, see page DC 78SL.

Routine 78 Test 1D

Description

This is an electronic channel wrap test of a Halt I/O command during a data transfer. The test performs a Halt I/O during a write data transfer operation by dropping select out and hold out in response to data out.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781D02: Halt I/O (bit 0 of the CS2 register) did not set
781D04: Data in CBO register not as expected
781D06: CSC card check (bit 4 of the CS2 register) did not set

Note: For isolation codes 781DDx or 781DEx, see page DC 78SL.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 1E

Description

This is an electronic channel wrap test of search compare operations. The test performs searches with data from the channel (in write mode) compared with data from the ADT buffer. There are nine separate passes with the following conditions:

- Channel data = ADT data, with search mode high and not equal
- Channel data = ADT data, with search mode equal and not high
- Channel data = ADT data, with search mode high and equal
- Channel data greater than ADT data, with search mode high and not equal
- Channel data greater than ADT data, with search mode equal and not high
- Channel data greater than ADT data, with search mode high and equal
- Channel data less than ADT data, with search mode high and not equal
- Channel data less than ADT data, with search mode equal and not high
- Channel data less than ADT data, with search mode high and equal

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

781E04: Search compare status is not as expected
781E40: Check 1 (bit 7 of the CS2 register) is on

Note: For isolation codes 781EDx or 781EEx, see page DC 78SL.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test 21

Description

This is an electronic channel wrap pad count check test. This test forces a pad count check by causing data end of transfer before the pad count goes to zero during a write operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

782102: CDX end of transfer and check 2 (bit 0 and 4 of the XCS register) should be on
782104: Pad count check (bit 0 of the CHK register) is set
782106: Expected data in the XES register (X'00') is not correct
782130: Data in the CBO register does not equal the expected data
782150: CDX ent of transfer (bit 4 of the XCS register) did not set

Note: For isolation codes 7821Dx or 7821Ex, see page DC 78SL.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test SL

Description

This subroutine is used in various tests in routine 78 to perform initial selection.

Note: This test is a subroutine and will not run as a normal test under MD control.

Isolation Codes

78xxE1: Register CS1 reset value is not correct
78xxE2: Select in (bit 6 of the DTI register) did not set
78xxE3: Channel Switch locked (bit 4 of the CC2 register) did not set
78xxE4: Address out and select out trapped (bits 1 and 4 of register CS1) should both be on
78xxE5: New level 2 interrupt (bit 2 of the ILR register) did not set
78xxE6: Address in the CBO register is not correct
78xxE7: OP in and Mark in (bits 3 and 6 of the DTI register) did not set
78xxE8: Address out (bit 4 of the CS1 register) did not reset
78xxE9: Address in (bit 5 of the DTI register) did not set
78xxEA: Address in the DBI register is not correct
78xxEB: Command out and select out trapped (bits 2 and 4 of register CS1) should both be on
78xxEC: Address in the CBO register is not correct
78xxED: Address in (bit 5 of the DTI register) did not reset
78xxEE: Command out (bit 4 of the CS1 register) did not reset
78xxEF: Channel check 1 (bit 7 of the CS2 register) is on

Error Display Bytes

- E1 = Test no.
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 78 Test ST

Description

This subroutine is used in various tests in routine 78 to check initial status.

Note: This test is a subroutine and will not run as a normal test under MD control.

Isolation Codes

78xxD2: Select out (bit 4 of the CS1 register) did not set
78xxD3: OP in and mark in (bits 1 and 6 of the DTI register) should both be on
78xxD4: Status in (bit 7 of the DTI register) did not set
78xxD5: Address in the CBI register is not correct
78xxD7: Service out (bit 4 of the CS1 register) did not set
78xxD8: Status in (bit 7 of the DTI register) did not reset
78xxD9: Select out (bit 4 of the CS1 register) did not reset

Error Display Bytes

- E1 = Test no.
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Routine 79 Information and Execution Procedures

Descriptive Name

This is an external block wrap diagnostic.

Description

Routine 79 provides extended testing of the external channel interface hardware. Routine 79 tests the wrapping of inbound tag and bus lines to outbound tag and bus lines, via a set of external wrap blocks which can be installed at the channel tailgate connectors or at the end of the channel tag and bus cables.

In addition, routine 79 also tests the disconnect-in and selective reset function using the internal electronic channel wrap hardware. This test is not included in the execution of the electronic wrap diagnostics which execute during an IML.

Prerequisites for Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Install the external wrap blocks on the tag and bus connectors for the channel to be tested.
4. Perform an IML operation.

Diagnostic Parameters

The following diagnostic parameters can be specified during the execution of this routine.

Note: If any parameters are specified, all parameter bytes must be specified.

Byte 1: Beginning test ID. The default is '01' if not specified.

Note: Test 00 does not test hardware logic

Byte 2: Ending test ID. The default is '02' if not specified. The highest value is '02'.

Byte 3: Run options

X'01' bypass error halt
X'02' loop test(s) (the default is X'00' if not specified.)

Byte 4: Bit significant channel address is used to specify the channel to test. Channel A = X'80', channel B = X'40', and so on.

Note: When running from the maintenance device under support option 7, bytes 1 through 4 are entered under the control of MD prompting.

The Diagnostic Execution Procedures section shows the parameter and run option entry normally used to put a test into a scoping loop. These are not, however, the only valid parameter and run option specifications that can be used with these tests.

Diagnostic Error Displays

Refer to page 79xx for a description of isolation codes.

Routine 79 Test 00

Description

This portion of routine 79 performs the following functions:

- Loads remaining overlays of routine from diskette into control storage
- Processes and verifies parameters entered
- Establishes system reset trap for system and selective resets
- Reads channel address switches by performing a system reset
- Selects and executes each test in routine sequentially
- Formats error displays and takes error exits to COLIC
- Tests for outstanding check 1 or check 2 errors following execution of each test
- Initializes registers prior to executing each test.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

790001: Invalid parameter was entered when trying to run routine
790002: Error return code from overlay loader
7900F0: System reset failed to occur after dropping OP out
7900F2: Level 1 interrupt (bit 1 of the ILR register) is on
7900F4: Level 1 interrupt (bit 1 of the ILR register) got set during test XX
7900F8: Check 2 (bit 0 of the XCS register) got set during test XX.

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Routine 79 Test 01

Description

This is the channel-wrap/cable-wrap portion of the channel test. It uses wrap blocks to check the:

NPL drivers and receivers
cables and connectors between the channel tag and bus in interface
channel tag and bus out interface.

See the CARR section of the MIM for setup instructions.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7901F0: Channel switch locked (bit 4 of the CC2 register) did not set
790102: Data in the CBO register not as expected
790104: Data in the CBO register not as expected
79010A: Data in the CBO register not as expected
79010B: Data in the CBO register not as expected
79010C: Data in the CBO register not as expected
79010D: Data in the CBO register not as expected
79010E: Data in the CBO register not as expected
79010F: Data in the CBO register not as expected
79011C: Data in the CS2 register not as expected
79012C: Data in the CS2 register not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Expected data
- E4 = Received data

Diagnostic Routine 7E Information and Execution Procedures

Descriptive Name

Function tests

Description

Routine 7E provides the same testing as IML hardcore tests 21 through 50. It also provides the ability to loop on specific tests and allows run options and parameters to be specified.

Refer to DC HC00 for a cross-reference of error codes and test numbers between routine 7E and the IML hardcore tests.

Prerequisites For Execution

1. Vary the storage director and the devices offline from the attached system.
2. Disable all storage director channels at the operator panel.
3. Remove any installed wrap cables.
4. Perform an IML operation.

Diagnostic Parameters

The following diagnostic parameters can be specified during the execution of this routine:

Note: If any parameters are specified, all parameter bytes must be specified.

Byte 1: Beginning test ID.
The default is X'01'.

Byte 2: Ending test ID.
The default is X'1F'.
The highest value is X'30'.

Diagnostic Error Displays

The display format on the MD when running diagnostics under support option 7 is:

```
DIAGNOSTIC DETECTED
AN ERROR. IC=rrttcc
BYTES=E1E2E3E4E5E6E7
E8E9EAEBECEDEEEF

Where: rr = routine ID
       tt = test ID
       cc = error code
```

Those six hex digits make up the isolation codes described under each routine on the following pages. The error display bytes (E1, E2, and so forth) are also described under each routine.

Hardcore to Routine 7E Test Cross Reference Listing (Model 21 Only)

HARDCORE TEST NUMBER	ROUTINE 7E TEST NUMBER	TEST DESCRIPTION
21	01	CPACK1, CPACK2 Reset Value Test
22	02	1B, 1B Shadow, '08' Register Test
23	03	1B Register Increment
24	04	CCOMAD1 Write/Read
25	05	Force Port Adapter IR Check 1
26	06	Force Port Adapter IR Check 2
27	07	Force Port Adapter IR Check 3
28	08	Force SDM ALU Out Parity Check
29	09	Force External Register Address or Decode Check
2A	0A	Force External Register Selection Check
2B	0B	Force Read Clock Delay Check
2C	0C	Force ALU Out Control Check
2D	0D	Force Clock Check
2E	0E	Force CD Duplicate IR Address Decode Check
2F	0F	Force Range Select Check
30	10	Force ADT/ASDM IR Check 1
31	11	Force ADT/ASDM IR check 2
32	12	Force ADT Buffer/ASDM CS In Parity
33	13	Force Duplicate IR Address Check
34	14	Force Car Check
35	15	CACTL Write/Read
36	16	CARD1, CARD2 Write/Read
37	17	ASDM Control Store Write/Read
38	18	ADT Buffer Write/Read
39	19	ASDM Control Store/ADT buffer Write/Read
3A	1A	ASDM Control Store/ADT Buffer Write/Read
3B	1B	ADT Buffer Write/Read
3C	1C	ASDM Control Store Wrap 1
3D	1D	ASDM Control Store Wrap 2
3E	1E	ASDM Branch Direct Command
3F	1F	ASDM Branch and Link Command
40	20	ASDM Command Branch and Link Register
41	21	ASDM Command Branch on Condition
42	22	ASDM Command Jump on Internal Register
43	23	ASDM Command Jump on External Register
44	24	ASDM Internal Register to Int Register
45	25	ASDM Int Register to Immediate Inst
46	26	ASDM External Register Instruction
47	27	ASDM Control Store Op 0
48	28	ASDM Control Store Op 1
49	29	ASDM Internal Register Array
4A	2A	ASDM Internal Register Array
4B	2B	ASDM External Register Write/Read
4C	2C	Force ASDM LSR/External Register Address Parity 1
4D	2D	Force ASDM LSR/External Register Address Parity 2
4E	2E	Force ASDM Internal Check
4F	2F	Force ASDM SC Address Parity
50	30	ASDM Level 6/7 Interrupt

Routine: 7E Test 01

Description

This test checks the reset value of the CPACK1 and CPACK2 registers on the CMCD Card.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0101: Address for CPACK2 register not correct in register X'1B'
7E0102: Reset value of CPACK2 register not correct
7E0103: CHK register indicates an error
7E0104: Check 2 (bit 0 of the XCS register) is on
7E0105: Address for CPACK1 register not correct in register X'1B'
7E0106: Reset value of CPACK1 register not correct
7E0115: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 02

Description

This test checks the integrity of the X'0F', X'1B', and X'1B' shadow registers. It also checks special operations SP OP hold 1B shadow and SP OP restore 1B by testing for the reset value of ASDM indirect registers CAAJCK, CACTL, CARD1, and CARD2 on the CMAA Card.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0202: CPACK2 register indicates an error
7E0203: CHK register indicates an error
7E0204: Check 2 (bit 0 of the XCS register) is on
7E0206: CPACK1 register indicates an error
7E0207: Address in register X'1B' not correct
7E0208: Reset value of the register read is not correct
7E0209: SP OP Hold 1B Shadow address in register X'1B' not correct
7E020A: X'1B' shadow address in register X'1B' not correct
7E020B: Address in X'1B' shadow register not correct
7E020C: Restored address in X'1B' register not correct
7E0215: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 03

Description

This test checks that the X'1B' register address is incremented after a WRF instruction. Hex addresses 83, 86, A3, A6, and FF are loaded into the X'1B' register and a WRF instruction is then executed. The X'1B' register is then read to make sure it was incremented.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0307: Address in X'1B' register not correct
7E030B: Address in X'1B' shadow register did not increment after a WRF instruction
7E030E: Address in X'1B' register did not increment after a WRF instruction

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E01

Routine 7E Test 04

Description

This test will check the CCOMADI register by writing and reading hex data patterns 00, 05, 0B, and 10.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0402: CPACK2 register indicates an error
7E0403: CHK register indicates an error
7E0404: Check 2 (bit 0 of the XCS register) is on
7E0406: CPACK1 register indicates an error
7E040F: Value in CCOMADI register not correct
7E0415: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 05

Description

This test will force a port adapter IR check (CPACK1 register bit 0) in two ways:

- Set CCOMADI register to X'19', then read a register within this card. This simulates both W/R gates active.
- Set CCOMADI register to X'1C', then read a register within this card. This simulates no W/R gates active.

Note: The REF section of the MSM manual shows which card each external register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0502: CPACK2 register indicates an error
7E0503: CHK register indicates an error
7E0504: Check 2 (bit 0 of the XCS register) is on
7E0506: CPACK1 register indicates an error
7E0510: Port adapter IR summary check (bit 2 of the CPACK1 register) did not set
7E0511: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0512: Check 2 (bit 0 of the XCS register) did not set
7E0515: CSPRDIC register indicates an error
7E0516: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 06

Description

This test will force a port adapter IR check (CPACK1 register bit 0) in two ways:

- Set CCOMADI register to X'1A', then write to an addressable register on this card. This simulates a parity check on the IR address bus.
- Set CCOMADI register to X'1F', then write to an addressable register on this card. This simulates a decoder check on the IR address bus.

Note: The REF section of the MSM manual shows which card each external register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0602: CPACK2 register indicates an error
7E0603: CHK register indicates an error
7E0604: Check 2 (bit 0 of the XCS register) is on
7E0606: CPACK1 register indicates an error
7E0610: Port adapter IR summary check (bit 2 of the CPACK1 register) did not set
7E0611: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0612: Check 2 (bit 0 of the XCS register) did not set
7E0615: CSPRDIC register indicates an error
7E0616: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 07

Description

This test will force a port adapter IR check (CPACK1 register bit 0) in two ways:

- Set CCOMADI register to X'1E', then write to an addressable register on this card. This simulates an address decoder check.
- Set CCOMADI register to X'1B', then write to an addressable register on this card. This simulates a parity check. X'1B' will also cause an IR data out parity check (CPACK1 register bit 4).

Note: The REF section of the MSM manual shows which card each register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0702: CPACK2 register indicates an error
7E0703: CHK register indicates an error
7E0704: Check 2 (bit 2 of the XCS register) is on
7E0706: CPACK1 register indicates an error
7E0710: Port adapter IR check and IR data out parity check (bits 0 and 4 of the CPACK1 register) did not set
7E0711: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0712: Check 2 (bit 0 of the XCS register) did not set
7E0715: CSPRDIC register indicates an error
7E0716: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 08

Description

This test forces an SDM ALU out parity check and an external register read parity check (bits 1 and 7 of the CPACK1 register).

The SDM parity check is forced by setting CCOMADI register to X'16', then writing to an addressable register on this card with an odd number of bits.

The external register read parity check is forced by reading the register that was written in the first part of the test.

Note: The REF section of the MSM manual shows which card each register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0802: CPACK2 register indicates an error
7E0803: CHK register indicates an error
7E0804: Check 2 (bit 0 of the XCS register) is on
7E0806: CPACK1 register indicates an error
7E0810: SDM ALU out parity check and external register parity check (bits 1 and 7 of the CPACK1 register) did not set
7E0811: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0812: Check 2 (bit 0 of the XCS register) did not set
7E0815: CSPRDIC register indicates an error
7E0816: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 09

Description

This test forces an external register address or decoder check (CPACK1 register bit 2) in two ways:

1. Set CCOMADI register to X'17', then write to register X'1B'.
2. Set CCOMADI register to X'10'. This immediately forces the error above and an ALU out control check (CPACK1 register bit 6).

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0902: CPACK2 register indicates an error
7E0903: CHK register indicates an error
7E0904: Check 2 (bit 0 of the XCS register) is on
7E0906: CPACK1 register indicates an error
7E0910: External register address or decode check, and ALU out control check (bits 2 and 6 of the CPACK1 register) did not set
7E0911: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0912: Check 2 (bit 0 of the XCS register) did not set
7E0915: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E07

Routine 7E Test 0A

Description

This test forces an external register selection check (CPACK1 register bit 3) by setting the CCOMADI register to X'0C', then writing to an addressable register on a card other than the CMCD card.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0A02: CPACK2 register indicates an error
7E0A03: CHK register indicates an error
7E0A04: Check 2 (bit 0 of the XCS register) is on
7E0A06: CPACK1 indicates an error
7E0A10: External register selection check (bit 3 of the CPACK1 register) did not set
7E0A11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0A12: Check 2 (bit 0 of the XCS register) did not set
7E0A15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 0B

Description

This test forces a read clock delay check (CPACK1 register bit 5) by setting CCOMADI register to X'14', then reading any addressable register.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0B02: CPACK2 register indicates an error
7E0B03: CHK register indicates an error
7E0B04: Check 2 (bit 0 of the XCS register) is on
7E0B06: CPACK1 register indicates an error
7E0B10: Read clock delay check (bit 5 of the CPACK1 register) did not set
7E0B11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0B12: Check 2 (bit 0 of the XCS register) did not set
7E0B15: CSPRDIC register indicates an error
7E0B16: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 0C

Description

This test forces an ALU out control check (CPACK1 register bit 6) by setting the CCOMADI register to X'15'.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0C02: CPACK2 register indicates an error
7E0C03: CHK register indicates an error
7E0C04: Check 2 (bit 0 of the XCS register) is on
7E0C06: CPACK1 register indicates an error
7E0C10: ALU out control check (bit 6 of the CPACK1 register) did not set
7E0C11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0C12: Check 2 (bit 0 of the XCS register) did not set
7E0C15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 0D

Description

This test forces a clock check (CPACK2 register bit 4) by setting the CCOMADI register to X'08'.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0D02: CPACK2 register indicates an error
7E0D03: CHK register indicates an error
7E0D04: Check 2 (bit 0 of the XCS register) is on
7E0D06: CPACK1 register indicates an error
7E0D10: Clock check (bit 4 of the CPACK2 register) did not set
7E0D11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0D12: Check 2 (bit 0 of the XCS register) did not set
7E0D15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 0E

Description

This test forces a CD duplicate IR address decode check (CPACK2 register bit 5) by setting the CCOMADI register to X'18', then writing to a register on this card.

Note: The REF section of the MSM manual shows which card each register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0E02: CPACK2 register indicates an error
7E0E03: CHK register indicates an error
7E0E04: Check 2 (bit 0 of the XCS register) is on
7E0E06: CPACK1 register indicates an error
7E0E10: CD duplicate IR address decode check (bit 5 of the CPACK2 register) did not set
7E0E11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0E12: Check 2 (bit 0 of the XCS register) did not set
7E0E15: CSPRDIC register indicates an error
7E0E16: Port adapter IR summary check (bit 2 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 0F

Description

This test forces a range select check (CPACK2 register bit 7) in two ways:

- Set the CCOMADI register to X'0D', then set the ADT buffer address to X'4000'
- Set the CCOMADI register to X'0D', then set the ASDM control storage address to X'2000'

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E0F02: CPACK2 register indicates an error
7E0F03: CHK register indicates an error
7E0F04: Check 2 (bit 0 of the XCS register) is on
7E0F06: CPACK1 register indicates an error
7E0F10: Range select check (bit 7 of the CPACK2 register) did not set
7E0F11: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E0F12: Check 2 (bit 0 of the XCS register) did not set
7E0F15: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 10

Description

This test forces an ADT/ASDM IR check (CAAJCK register bit 0) in two ways:

- Set the CCOMADI register to X'19', then read a register within this card. This simulates both W/R Gates active.
- Set the CCOMADI register to X'1C', then read a register within this card. This simulates no W/R Gates active.

Note: The REF section of the MSM manual shows which card each register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1002: CPACK2 register indicates an error
7E1003: CHK register indicates an error
7E1004: Check 2 (bit 0 in the XCS register) is on
7E1006: CPACK1 register indicates an error
7E100D: CAAJCK register indicates an error
7E1010: ADT/ASDM IR check (bit 0 of the CAAJCK register) did not set
7E1011: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E1012: Check 2 (bit 0 in the XCS register) did not set
7E1015: CSPRDIC register indicates an error
7E1016: Aux adapter IR summary check (bit 0 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 11

Description

This test forces an ADT/ASDM IR check (CAAJCK register bit 0) in two ways:

- Set the CCOMADI register to X'1A', then write to an addressable register on this card. This simulates multiple decodes of the CD address bus.
- Set the CCOMADI register to X'1B', then write to an addressable register on this card. This simulates a parity check on the register data bus.

Note: The REF section of the MSM manual shows which card each register is located on.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1102: CPACK2 register indicates an error
7E1103: CHK register indicates an error
7E1104: Check 2 (bit 0 in the XCS register) is on
7E1106: CPACK1 register indicates an error
7E110D: CAAJCK register indicates an error
7E1110: ADT/ASDM IR check (bit 0 of the CAAJCK register) did not set
7E1111: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E1112: Check 2 (bit 0 in the XCS register) did not set
7E1115: CSPRDIC register indicates an error
7E1116: Aux adapter IR summary check (bit 0 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 12

Description

This test forces an ADT buffer/ASDM CS in parity check (CAAJCK register bit 3) by setting the CCOMADI register to X'05', then writing to the ADT buffer.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1202: CPACK2 register indicates an error
7E1203: CHK register indicates an error
7E1204: Check 2 (bit 0 in the XCS register) is on
7E1206: CPACK1 register indicates an error
7E120D: CAAJCK register indicates an error
7E1210: ADT buffer/ASDM CS in parity check (bit 3 of the CAAJCK register) did not set
7E1211: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E1212: Check 2 (bit 0 in the XCS register) did not set
7E1215: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 13

Description

This test forces an AA duplicate IR address decode check (CAAJCK register bit 4) by setting the CCOMADI register to X'03', then writing to a register on the CMAA Card.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1302 = CPACK2 register indicates an error
7E1303 = CHK register indicates an error
7E1304 = Check 2 (bit 0 of the XCS register) is on
7E1306 = CPACK1 register indicates an error
7E130D = CAAJCK register indicates an error
7E1310 = AA duplicate IR address decode check (bit 4 of the CAAJCK register) did not set
7E1311 = Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E1312 = Check 2 (bit 0 of the XCS register) did not set
7E1315 = CSPRDIC register indicates an error
7E1316 = Aux adapter IR summary check (bit 0 of the CSPRDIC register) did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 14

Description

This test forces CAR check (CAAJCK register bit 7) in two ways:

- Set the CCOMADI register to X'09', then write to ASDM control storage
- Set the CCOMADI register to X'07', then write to ASDM control storage

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1402 = CPACK2 register indicates an error
7E1403 = CHK register indicates an error
7E1404 = Check 2 (bit 0 of the XCS register) is on
7E1406 = CPACK1 register indicates an error
7E140D = CAAJCK register indicates an error
7E1410 = CAR check (bit 7 of the CAAJCK register) did not set
7E1411 = Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E1412 = Check 2 (bit 0 of the XCS register) did not set
7E1415 = CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 15

Description

This test checks ASDM write register CACTL. The register is written with a floating 1 data pattern, then read and the value compared to an expected value. Bit 0 is not checked in this test. Registers CAAJCK, CPACK1, CPACK2, CHK, and XCS are checked for errors after the write/read operations.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1502 = CPACK2 register indicates an error
7E1503 = CHK register indicates an error
7E1504 = Check 2 (bit 0 of the XCS register) is on
7E1506 = CPACK1 register indicates an error
7E150D = CAAJCK register indicates an error
7E1514 = CACTL register contents not as expected
7E1515 = CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E13

Routine 7E Test 16

Description

This test checks ASDM write registers CARD1/2. The registers are written with a floating 1 data pattern, then read and the value compared to an expected value. Registers CAAJCK, CPACK1, CPACK2, CHK, and XCS are checked for errors after the write/read operations.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1602: CPACK2 register indicates an error
7E1603: CHK register indicates an error
7E1604: Check 2 (bit 0 of the XCS register) is on
7E1606: CPACK1 register indicates an error
7E160D: CAAJCK register indicates an error
7E1614: CARD1/CARD2 register contents not as expected
7E1615: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 17

Description

This test checks the ASDM control storage. A data pattern is written to control storage, then is read and compared to an expected value. The ADT buffer is read to ensure that no data was written to the buffer when the buffer ALU pointer (BAP) register is set to 2XXX/3XXX. The read operation from control storage uses BAP = 2XXX/3XXX. The read operation from the buffer uses CBP = 0XXX. The CBP and BAP registers are checked for correct wrap addresses after the write/read operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1701: The address in the BAP register was not as expected after a write/read operation
7E1702: CAAJCK register indicates an error
7E1703: CPACK1 register indicates an error
7E1704: CPACK2 register indicates an error
7E1705: CHK register indicates an error
7E1706: Check 2 (bit 0 of the XCS register) is on
7E1707: Data read from ASDM control storage is not as expected
7E1708: Data read from the ADT buffer is not 00
7E1709: The address in the CBP register was not as expected after a write/read operation
7E170D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 18

Description

This test checks the ADT buffer. A data pattern is written to it, then is read and compared to an expected value. The ASDM control storage is read to ensure that no data was written to it when the buffer ALU pointer (BAP) register is set to 0XXX. The read operation from control storage uses CBP = 3XXX. The read operation from the buffer uses BAP = 4XXX. The CBP and BAP registers are checked for correct wrap addresses after the write/read operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1801: The address in the BAP register was not as expected after a write/read operation
7E1802: CAAJCK register indicates an error
7E1803: CPACK1 register indicates an error
7E1804: CPACK2 register indicates an error
7E1805: CHK register indicates an error
7E1806: Check 2 (bit 0 of the XCS register) is on
7E1809: The address in the CBP register was not as expected after a write/read operation
7E180B: Data read from the ADT buffer is not as expected
7E180C: Data read from ASDM control storage is not 00
7E180D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E16

Routine 7E Test 19

Description

This test checks that data is written to the ADT buffer and to ASDM control storage at the same time when the channel buffer pointer (CBP) register is set to 5XXX. The read operation from control storage uses BAP = 3XXX. The read operation from the ADT buffer uses CBP = 5XXX. The CBP and BAP registers are checked for correct wrap addresses after the write/read operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1901: The address in the BAP register was not as expected after a write/read operation
7E1902: CAAJCK register indicates an error
7E1903: CPACK1 register indicates an error
7E1904: CPACK2 register indicates an error
7E1905: CHK register indicates an error
7E1906: Check 2 (bit 0 of the XCS register) is on
7E1907: Data read from ASDM control storage is not as expected
7E1909: The address in the CBP register was not as expected after a write/read operation
7E190B: Data read from the ADT buffer was not as expected
7E190D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 1A

Description

This test checks that no data is written to the ADT buffer or to ASDM control storage when the BAP register is set to 4XXX. The read operation from control storage uses BAP = 3XXX. The read from the buffer uses CBP = 6XXX. The CBP and BAP registers are checked for correct wrap addresses after the write/read operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1A01: The address in the BAP register was not as expected after a write/read operation
7E1A02: CAAJCK register indicates an error
7E1A03: CPACK1 register indicates an error
7E1A04: CPACK2 register indicates an error
7E1A05: CHK register indicates an error
7E1A06: Check 2 (bit 0 of the XCS register) is on
7E1A09: The address in the CBP register was not as expected after a write/read operation
7E1A0B: Data read from the ADT buffer is not 00
7E1A0C: Data read from ASDM CS is not 00
7E1A0D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 1B

Description

This test writes data to the ADT buffer then reads it back and compares it to an expected value. The ASDM control storage is read to ensure that no data was written to it when BAP was set to 6XXX. The read operation from the ADT buffer uses BAP = 6XXX. The read operation from control storage uses CBP = 3XXX. The CBP and BAP registers are checked for correct wrap addresses after the write/read operation.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1B01: The address in the BAP register was not as expected after a write/read operation
7E1B02: CAAJCK register indicates an error
7E1B03: CPACK1 register indicates an error
7E1B04: CPACK2 register indicates an error
7E1B05: CHK register indicates an error
7E1B06: Check 2 (bit 0 of the XCS register) is on
7E1B09: The address in the CBP register was not as expected after a write/read operation
7E1B0B: Data read from the ADT buffer was not as expected
7E1B0C: Data read from ASDM control storage is not 00
7E1B0D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E19

Routine 7E Test 1C

Description

This test checks the ASDM control storage wrap addresses. Four bytes are written to each block starting at location X'2XFC'. The address should wrap after the fourth byte. The wrap addresses are:

- From X'23FF' to X'2200'
- From X'2BFF' to X'2A00'

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1C01: The address in the BAP register was not as expected
7E1C02: CAAJCK register indicates an error
7E1C03: CPACK1 register indicates an error
7E1C04: CPACK2 register indicates an error
7E1C05: CHK register indicates an error
7E1C06: Check 2 (bit 0 of the XCS register) is on
7E1C0D: CSPRDIC indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 1D

Description

This test checks the ASDM control storage wrap addresses. Four bytes are written to each block starting at location X'3XFC'. The address should wrap after the fourth byte. The wrap addresses are:

- From X'33FF' to X'3200'
- From X'3BFF' to X'3A00'

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1D02: CAAJCK register indicates an error
7E1D03: CPACK1 register indicates an error
7E1D04: CPACK2 register indicates an error
7E1D05: CHK register indicates an error
7E1D06: Check 2 (bit 0 of the XCS register) is on
7E1D09: The address in the CBP register was not as expected
7E1D0D: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 1E

Description

This test checks the operation of the ASDM Branch Direct command. It tests that a branch is taken and that all other registers remain unaltered.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1E01: CAAJCK register indicates an error
7E1E02: CPACK1 register indicates an error
7E1E03: CPACK2 register indicates an error
7E1E04: CHK register indicates an error
7E1E05: Check 2 (bit 0 of the XCS register) is on
7E1E06: Branch failed
7E1E07: Register contents not as expected
7E1E0E: ASDM did not respond, timeout occurred
7E1E0F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 1F

Description

This test checks the operation of the ASDM Branch and Link command. It tests that:

1. A branch is taken (next instruction not executed)
2. IAR-1 (return address) is saved in register PR4
3. All other registers except PR4 are unaltered

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E1F01: CAAJCK register indicates an error
7E1F02: CPACK1 register indicates an error
7E1F02: CPACK1 register indicates an error
7E1F03: CPACK2 register indicates an error
7E1F04: CHK register indicates an error
7E1F05: Check 2 (bit 0 of the XCS register) is on
7E1F06: Branch error
7E1F07: Register contents not correct
7E1F08: High return address in register R4 not as expected
7E1F09: Low return address in register R5 was not as expected
7E1F0E: ASDM did not respond, timeout occurred
7E1F0F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 20

Description

This test checks the operation of the ASDM Branch and Link command register. It tests that:

- A branch is taken to IR1 (PR6)
- IAR+1 is saved in IR2 (PR2)
- All other registers except PR6 and PR2 are unaltered

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2001: CAAJCK register indicates an error
7E2002: CPACK1 register indicates an error
7E2003: CPACK2 register indicates an error
7E2004: CHK register indicates an error
7E2005: Check 2 (bit 0 of the XCS register) is on
7E2006: Branch error
7E2006: Branch error
7E2007: Register contents not as expected
7E2008: High return address in register R2 not as expected
7E2009: Low return address in register R3 not as expected
7E200E: ASDM did not respond, timeout occurred
7E200F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 21

Description

This test checks the operation of the ASDM Branch on Condition command. It tests that a branch is taken only when appropriate.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2101: CAAJCK register indicates an error
7E2102: CPACK1 register indicates an error
7E2103: CPACK2 register indicates an error
7E2104: CHK register indicates an error
7E2105: Check 2 (bit 0 of the XCS register) is on
7E2106: Branch error
7E210A: Condition code did not set correctly
7E210E: ASDM did not respond, timeout occurred
7E210F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 22

Description

This test checks the operation of the ASDM Jump on Internal Register Bit command. It tests that a branch is taken only when appropriate.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2201: CAAJCK register indicates an error
7E2202: CPACK1 register indicates an error
7E2203: CPACK2 register indicates an error
7E2204: CHK register indicates an error
7E2205: Check 2 (bit 0 of the XCS register) is on
7E2206: Branch error
7E2207: Invalid branch
7E220E: ASDM did not respond, timeout occurred
7E220F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 23

Description

This test checks the operation of the ASDM Jump on External Register Bit command. It tests that a branch is taken only when appropriate.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2301: CAAJCK register indicates an error
7E2302: CPACK1 register indicates an error
7E2303: CPACK2 register indicates an error
7E2304: CHK register indicates an error
7E2305: Check 2 (bit 0 of the XCS register) is on
7E2306: Branch error
7E2307: Invalid branch
7E230E: ASDM did not respond, timeout occurred
7E230F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 24

Description

This test checks the operation of the ASDM Internal Register to Internal Register instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Register Utilization

Group 2:

R0 = Test accumulator
PR2 = Table pointer (on entry)
R4 = Accumulator test value from table fetch
R5 = Condition code test value from table fetch

Group 3:

R8 = Work register
R9 = Work register
R10 = Work register
R11 = Work register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2401: CAAJCK register indicates an error
7E2402: CPACK1 register indicates an error
7E2403: CPACK2 register indicates an error
7E2404: CHK register indicates an error
7E2405: Check 2 (bit 0 of the XCS register) is on
7E2406: Condition code did not set properly
7E2407: Accumulator contents not as expected
7E240E: ASDM did not respond, timeout occurred
7E240F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 25

Description

This test checks the operation of the ASDM Internal Register Immediate instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Register Utilization

Group 2:

R0 = Test accumulator
PR2 = Table pointer (on entry)
R4 = Accumulator test value from table fetch
R5 = Condition code test value from table fetch

Group 3:

R8 = Work register
R9 = Work register
R10 = Work register
PR12 = Work register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2501: CAAJCK register indicates an error
7E2502: CPACK1 register indicates an error
7E2503: CPACK2 register indicates an error
7E2504: CHK register indicates an error
7E2505: Check 2 (bit 0 of the XCS register) is on
7E2506: Condition code did not set properly
7E2507: Accumulator content is not as expected
7E250E: ASDM did not respond, timeout occurred
7E250F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 26

Description

This test checks the operation of the ASDM External Register instruction. It tests that condition codes are set properly following execution and that the accumulator (destination register) contains valid results.

Register Utilization

Group 2:

R0 = Test accumulator
PR2 = Table pointer (on entry)
R4 = Accumulator test value from table fetch
R5 = Condition code test value from table fetch

Group 3:

R8 = Work register
R9 = Work register
R10 = Work register
PR12 = Work register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2601: CAAJCK register indicated an error
7E2602: CPACK1 register indciated an error
7E2603: CPACK2 register indicated an error
7E2604: CHK register indicated an error
7E2605: Check 2 (bit 0 of the XCS register) is on
7E2608: Condition code did not set properly
7E2609: Accumulator content is not as expected
7E260E: ASDM did not respond, timeout occurred
7E260F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 27

Description

This test checks the operation of the ASDM Control Store OP 0 instruction. It tests:

- The ability to fetch data from a known location
- The ability to store data to a known location
- That addresses are incremented only when appropriate
- That uninvolved registers are not altered

Register Utilization

Group 2:

PR0 = Store and fetch data register
PR2 = Store and fetch address register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2701: CAAJCK register indicates an error
7E2702: CPACK1 register indicates an error
7E2703: CPACK2 register indicates an error
7E2704: CHK register indicates an error
7E2705: Check 2 (bit 0 of the XCS register) is on
7E2706: Error while fetching with no increment
7E2707: Error while fetching with increment
7E2708: Error while storing with no increment
7E2709: Error while storing with increment
7E270A: Incorrect register modified
7E270E: ASDM did not respond, timeout occurred
7E270F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 28

Description

This test checks the operation of the ASDM Control Store OP 1 instruction. It tests:

- The ability to fetch data from a known location
- The ability to store data to a known location
- That addresses are incremented only when appropriate
- That uninvolved registers are not altered

Register Utilization

Group 2:

PR0 = Store and fetch data register
PR2 = Store and fetch address register

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2801: CAAJCK register indicates an error
7E2802: CPACK1 register indicates an error
7E2803: CPACK2 register indicates an error
7E2804: CHK register indicates an error
7E2805: Check 2 (bit 0 of the XCS register) is on
7E2806: Error while fetching with no increment
7E2807: Error while fetching with increment
7E2808: Error while storing with no increment
7E2809: Error while storing with increment
7E280A: Incorrect register modified
7E280E: ASDM did not respond, timeout occurred
7E280F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 29

Description

This test checks the integrity of the ASDM internal register array. It tests:

- The ability to store various data patterns in each register location
- The ability to fetch from the stored location
- The validity of register selection

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2901: CAAJCK register indicates an error
7E2902: CPACK1 register indicates an error
7E2903: CPACK2 register indicates an error
7E2904: CHK register indicates an error
7E2905: Check 2 (bit 0 of the XCS register) is on
7E2906: Pattern received not as expected
7E290E: ASDM did not respond, timeout occurred
7E290F: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error Code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2A

Description

This test checks the ASDM internal register array. Each register is loaded with its register ID and group ID, then is read back to verify the information.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2A01: CAAJCK register indicates an error
7E2A02: CPACK1 register indicates an error
7E2A03: CPACK2 register indicates an error
7E2A04: CHK register indicates an error
7E2A05: Check 2 (bit 0 of the XCS register) is on
7E2A06: Pattern received not as expected
7E2A0E: ASDM did not respond, timeout occurred
7E2A15: Aux adapter IR summary check or port adapter IR summary check (bit 0 or 2 of the CSPRDIC register) is on

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2B

Description

This test checks the ASDM read/write registers in the following manner:

- The SDM writes a data pattern to the CARD1 and CARD2 registers, then passes control to the ASDM.
- The ASDM reads those registers (using the ARD1 and ARD2 register addresses) and compares the contents to an expected value.
- The ASDM then writes those contents to the AWR1 and AWR2 registers, then reads those registers back and compares the data to an expected value.
- The SDM then reads the AWR1 and AWR2 registers (using the CAWR1 and CAWR2 register addresses), then compares that data to an expected value.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2B01: Data in CAWR1 register not as expected
7E2B02: Data in CAWR2 register not as expected
7E2B07: CPACK1 register indicates an error
7E2B08: CPACK2 register indicates an error
7E2B0B: CAAJCK register indicates an error
7E2B0E: CHK register indicates an error
7E2B0F: XCS register indicates an error
7E2B10: CSPRDIC register indicates an error
7E2B11: Data in ARD1 register not as expected
7E2B12: Data in ARD2 register not as expected
7E2B13: Data in AWR1 register not as expected
7E2B14: Data in AWR2 register not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2C

Description

This test forces an ASDM LSR external register address parity check (CAAJCK register bit 1) by setting the CCOMADI register to X'0B', then having the ASDM read one of its external registers.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2C03: ASDM did not respond, timeout occurred
7E2C04: ASDM responded with an error condition code
7E2C06: ASDM LS external register address parity check (bit 1 of the CAAJCK register) did not set
7E2C07: CPACK1 register indicates an error
7E2C08: CPACK2 register indicates an error
7E2C09: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E2C0A: Check 2 (bit 0 of the XCS register) did not set
7E2C0B: CAAJCK register indicates an error
7E2C0E: CHK register indicates an error
7E2C0F: XCS register indicates an error
7E2C10: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2D

Description

This test forces an ASDM LS ext reg addr parity check (CAAJCK register bit 1) by setting the CCOMADI register to X'02', then having the ASDM access one of its internal registers.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2D03: ASDM did not respond, timeout occurred
7E2D04: ASDM responded with an error condition code
7E2D06: ASDM LS external register address parity check (bit 1 of the CAAJCK register) did not set
7E2D07: CPACK1 register indicates an error
7E2D08: CPACK2 register indicates an error
7E2D09: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E2D0A: Check 2 (bit 0 of the XCS register) did not set
7E2D0B: CAAJCK register indicates an error
7E2D0E: CHK register indicates an error
7E2D0F: XCS register indicates an error
7E2D10: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2E

Description

This test forces an ASDM internal check (CAAJCK register bit 2) by setting the CCOMADI register to X'1B', then having the ASDM read the ARD2 register (which should have bad parity).

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2E03: ASDM did not respond, timeout occurred
7E2E04: ASDM responded with an error condition code
7E2E06: ASDM internal check (bit 2 of the CAAJCK register) did not set
7E2E07: CPACK1 register indicates an error
7E2E08: CPACK2 register indicates an error
7E2E09: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E2E0A: Check 2 (bit 0 of the XCS register) did not set
7E2E0B: CAAJCK register indicates an error
7E2E0E: CHK register indicates an error
7E2E0F: XCS register indicates an error
7E2E10: CSPRDIC register indicates an error
7E2E17: Aux Adapter IR Sum Check did not set

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 2F

Description

This test forces an ASDM CS address parity check (CAAJCK register bit 6) by setting the CCOMADI register to X'01', then having ASDM read its control storage.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E2F03: ASDM did not respond, timeout occurred
7E2F04: ASDM responded with an error condition code
7E2F06: ASDM CS address parity check (bit 6 of the CAAJCK register) did not set
7E2F07: CPACK1 register indicates an error
7E2F08: CPACK2 register indicates an error
7E2F09: Port connection ADT buffer check (bit 7 of the CHK register) did not set
7E2F0A: Check 2 (bit 0 of the XCS register) did not set
7E2F0B: CAAJCK register indicates an error
7E2F0E: CHK register indicates an error
7E2F0F: XCS register indicates an error
7E2F10: CSPRDIC register indicates an error

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Routine 7E Test 30

Description

This test checks the ability of ASDM to change interrupt levels. The first part of the test changes from interrupt level 7. The second part of the test change from a interrupt level 7 to a interrupt level 6.

Parameters

Byte 1 - Beginning test ID

Byte 2 - Ending test ID

Isolation Codes

7E3003: ASDM did not respond, timeout occurred
7E3004: ASDM responded with an error condition code
7E3007: CPACK1 shows that an error has occurred
7E3008: CPACK2 shows that an error has occurred
7E300B: CAAJCK shows that an error has occurred
7E300E: CHK shows that an error has occurred
7E300F: XCS shows that an error has occurred
7E3010: CSPRDIC shows an IR Check has occurred
7E3014: Data in CACTL is not as expected
7E3016: Data in CAWR1/2 is not as expected

Error Display Bytes

- E1 = Test ID
- E2 = Error code
- E3 = Isolation code register contents (expected)
- E4 = Isolation code register contents (received)

Diagnostic Tests DC 7E2E

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