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IBM Systems Reference Library

IBM System/360 Model 40

Functional Characteristics

This manual presents the organization, characteristics, functions and features unique to the IBM System/360 Model 40. Major areas described are system structure, generalized information flow, standard and optional features, system control panel, instruction timings, and channel characteristics and functional evaluation.

Descriptions of specific input/output devices used with the IBM System/360 Model 40 appear in separate publications. Configurators for the IBM 2040 Processing Unit and I/O devices are available. See *IBM System/360 Bibliography,* Form A22-6822.

It is assumed that the reader has a knowledge of the System/360 as defined in the *IBM System/360 Principles of Operation,* Form A22-6821 and the *IBM System Summary,* Form A22-6810.

SECOND EDITION

This is a major revision of, and obsoletes, Forms A22-6881-0 and A22-6881-1, and Technical Newsletters N22-0228 and N22-0291. Additional material includes IBM 2400 tape data in channel evaluation factors, autopolling data for IBM 2702, revision of 2702 worksheet example; an additional load limits table on multpilexer in burst mode is included, as is channel-to-channel feature information. Address switching has been clarified, all instruction timings (including floating-point) have been revised. An index has been added. Changes to the text are indicated by a vertical line to the left of the change; revised illustrations are denoted by the symbol • to the left of the caption.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM branch office.

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This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B98, P.O. Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for readers' comments. If the form has been removed, comments may be sent to the above address.

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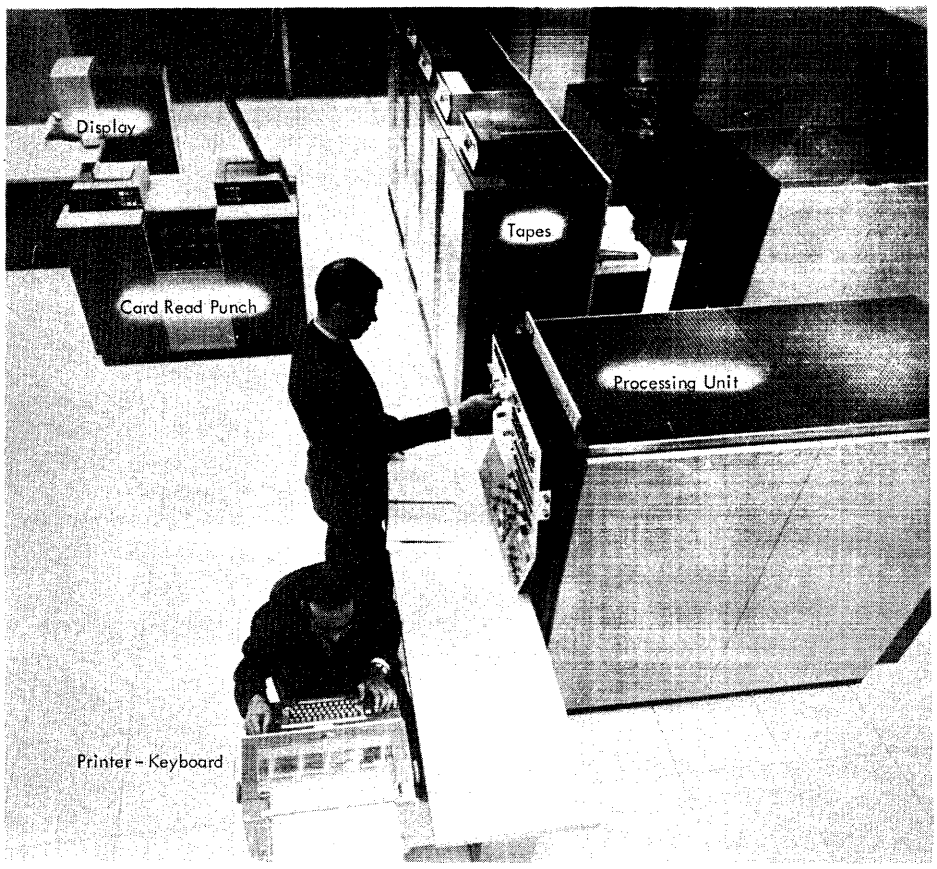


IBM System/360 Model 40

The IBM System/360 Model 40 is one of a series of models of compatible, general purpose, data processing systems designed for commercial, scientific, communications or control applications. The Model 40 includes the advantages, characteristics and functional logic established for the System/360, as defined in the *IBM System/360 Principles of Operation,* Form A22-6821.

The basic structure of a System/360 Model 40 consists of a 2040 Processing Unit, main storage, and multiplexer channel with input/output devices attached to the channel through control units (Figure 1). There are five models of the Model 40 termed D40, E40, F40, G40 and H40. These five models differ only in the amount of main storage required with a 2040 Processing Unit. The significant differences are:

IBM SYSTEM/360 MODEL	PROCESSING UNIT MODEL	DESCRIPTION
D40	2040D	16,384 bytes of main storage 16 multiplexer subchannels
E40	2040E	32,768 bytes of main storage 32 multiplexer subchannels
F40	2040F	65,536 bytes of main storage 64 multiplexer subchannels
G40	2040G	131,072 bytes of main storage 128 multiplexer subchannels
H40	2040H	262,144 bytes of main storage 128 multiplexer subchannels

The system control panel is located at one end of the 2040 Processing Unit. Standard features for any System/360 Model 40 include:

Multiplexer channel
Standard instruction set
Interval timer

Optional features for any Model 40 system include:

Decimal arithmetic instruction set
Floating-point arithmetic instruction set
Storage protection (store protection only)
Direct control
Selector channels (one or two)
Channel-to-channel adapter (one per 2040)
1401/1460 Compatibility feature
1410/7010 Compatibility feature
1052 Adapter, 1052 Printer-Keyboard (console typewriter)
Emergency power-off control (multisystem)

The 1401/1460 compatibility feature is optional for models E40, F40, G40, and H40. The 1311 compatibility feature is available with the 1401/1460 compatibility feature for models F40, G40, and H40.

The 1410/7010 compatibility feature is optional for models F40, G40, and H40. The 1311 compatibility feature is available with the 1410/7010 compatibility feature.

A variety of control units and input/output devices are available for use with the Model 40. Descriptions of specific input/output devices appear in separate publications. Configurators for the I/O devices and system components are also available. See *IBM System/360 Bibliography,* Form A22-6822.

2040 Processing Unit

The 2040 Processing Unit contains the facilities for addressing main storage, for fetching or storing information, for arithmetic and logical processing of data, for sequencing instructions in the desired order, and for initiating the communication between storage and external devices. The 2040H occupies more floor space than the other models; otherwise the five models of the 2040 Processor Unit vary only in the capacity of the main storage unit.

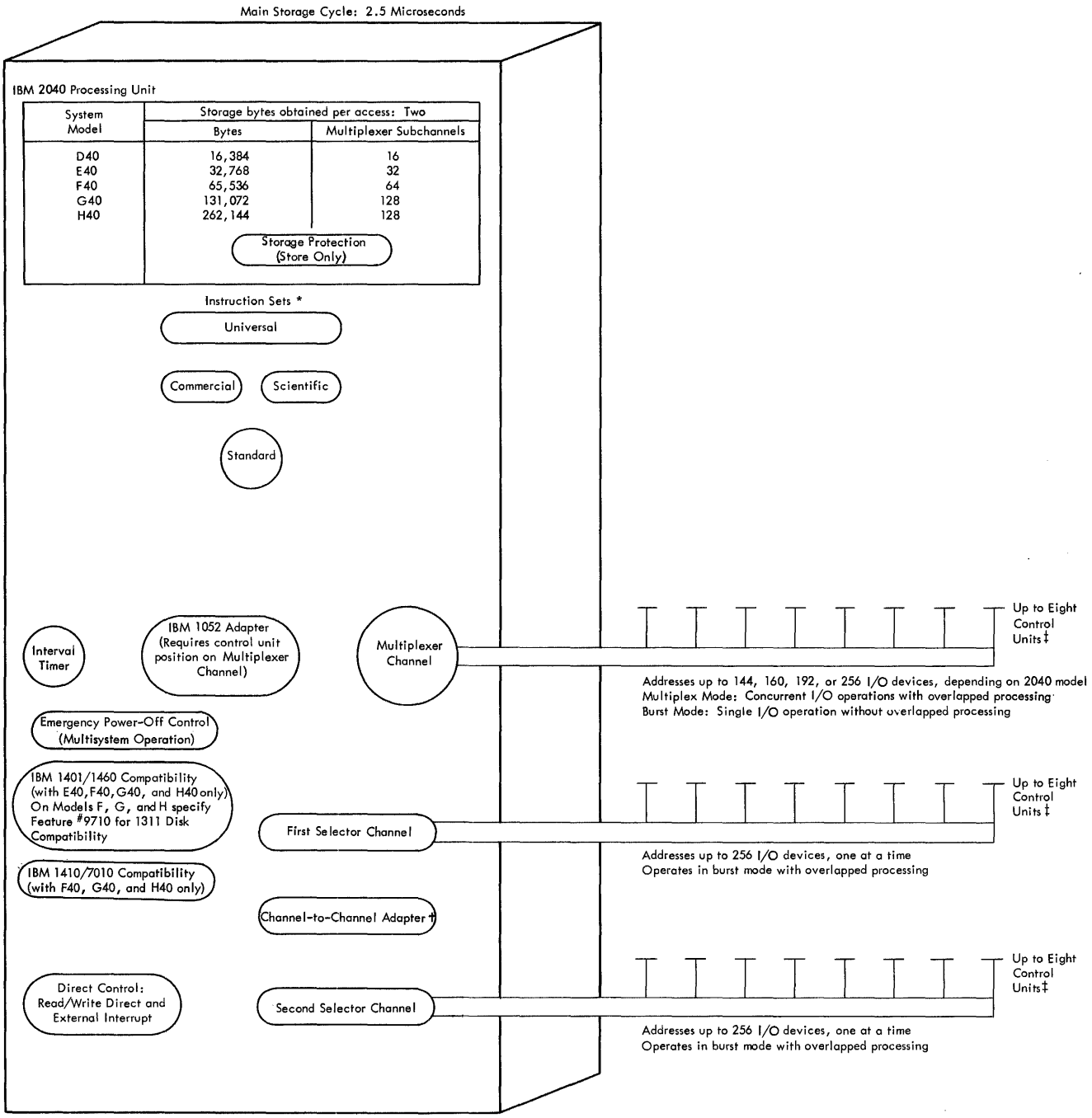
The 2040 Processing Unit contains the following major components:

Main storage
Arithmetic-logic unit
Local storage
General registers
Floating-point registers
Read only storage (ROS)
Mutiplexer channel
Selector channels
System control panel

Main Storage

Main storage is available in five storage capacities as previously listed. The main storage read/write cycle time is 2.5 microseconds with access to two bytes. Byte locations are consecutively numbered starting with zero. An addressing exception is recognized when any part of an operand is located beyond the maximum available installed main storage capacity.

The Model 40 transfers information between main storage and the processing unit in units of two bytes. The storage function in main storage is possible on a one byte or a two byte basis in one storage cycle. Main storage has a small extension of special channel storage. This special channel storage is not accessible by the problem programmer and is used to store the control and status information for each subchannel attached to the multiplexer channel. The number of these special channel storage locations determines the number of subchannels available to the multiplexer channel.



NOTES:

Indicates Standard Feature

Indicates Optional Feature

* The Universal Instruction Set includes the two storage protection instructions, plus the following subsets: Standard, Commercial, and Scientific

† A Channel-to-Channel Adapter option (one per 2040) permits interconnection of two channels. One channel position can connect to one channel position on any other IBM System/360 channel. Only one Channel-to-Channel Adapter needed per connection; it counts as a control unit on each channel.

‡ Input/Output Control Units and devices are shown on the IBM System/360 Input/Output Configurator, Form A22-6823.

● Figure 1. IBM System/360 Model 40 Configurator

Arithmetic-Logic Unit

The arithmetic-logic unit contains a one byte wide adder-subtractor which operates with either hexadecimal or decimal values. It is capable of producing both arithmetic and logical combinations of the input data streams. Cycle time is 0.625 microseconds.

Local Storage

Local storage consists of a small high-speed core storage unit providing registers for fixed-point and floating-point storage, for channel operations, for dumping of the 2040 Processing Unit working registers by error conditions and I/O interrupts, and for general working storage. Only the general registers and the floating-point registers are addressable by the main program. Local storage cycle time is 1.25 microseconds with access to two bytes. The storage cycle time can be split cycled on occasions giving an effective access of 0.625 microseconds.

General Registers

The 16 general registers are used in address arithmetic and indexing, and as accumulators in fixed-point arithmetic and logical operations. The general-purpose registers have a capacity of one word. For some operations, two adjacent registers can be coupled together, providing a double word capacity. The general registers are implemented in local storage and have a cycle time of 1.25 microseconds per two bytes.

Floating-Point Registers

Four floating-point registers are available for floating-point operations. These registers are two words in length and can contain either a short (one word) or a long (two word) floating-point operand. The floating point registers are implemented in local storage and have a cycle time of 1.25 microseconds per two bytes.

Read Only Storage

The control function of the Model 40 is achieved by the use of a read only storage (ROS). The ROS is self addressable and contains predetermined information of a nondestructive nature used to control the functions of data flow, and instruction execution. ROS is not directly addressable by the main program. Modification of the unit is made by physically changing the ROS unit.

Channels

The channel directs the flow of information between the I/O devices and main storage. It relieves the CPU of the task of communicating directly with the I/O devices and permits data processing to proceed concurrently with I/O operations. Data are transferred a byte at a time between the I/O device and the channel. Data transfers between the channel and storage are parallel by two bytes (half word) for selector channels, and serial by byte for the multiplexer channel. See Figure 2.

For efficiency, the channels are integrated with the processing unit and share many of its facilities. For example, the channels utilize the same read only storage for control, and use the CPU data paths for handling nearly all data and control information. A standard I/O interface provides a uniform method of attaching I/O control units to all channels, making the Model 40 adaptable to a broad spectrum of applications and devices.

Channel-to-Channel Feature

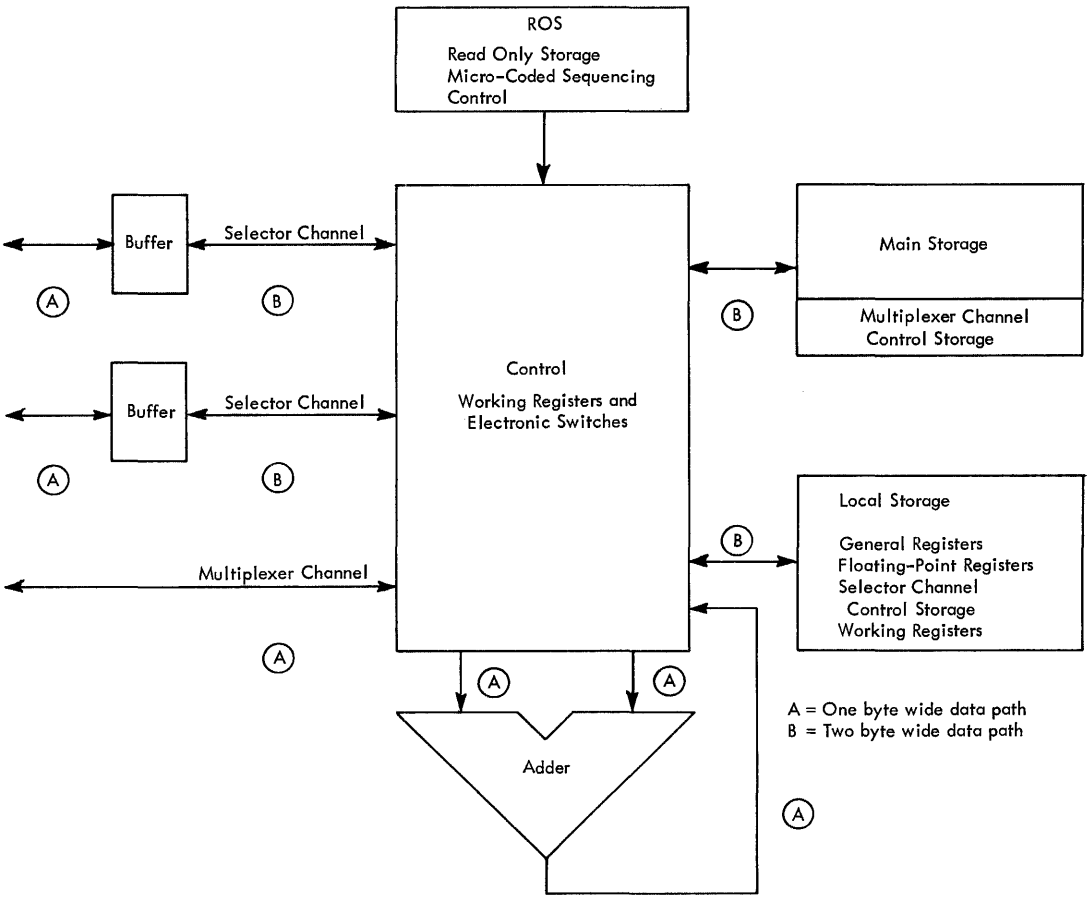
A channel-to-channel adapter is available as an optional feature. The adapter permits communication between two System/360 channels, thus providing the capability for interconnection of two processing units. The adapter uses one control unit position on each of the two channels. This feature is required on only one of the two connected channels. Only one channel-to-channel adapter can be installed on a Model 40.

If, at any time during a channel-to-channel adapter operation initiated by a Model 40 multiplexer channel, the other system fails to respond to the Model 40 within 32 seconds, the Model 40 channel disconnects and generates a machine-check interruption condition. The other system's failure to respond could be caused by its power being off, its operation in the stopped state, or by its channel being masked against an I/O interruption; i.e., a data transfer request or an attention condition initiated by the Model 40 is not recognized by the other system within 32 seconds.

Multiplexer Channel

The multiplexer channel is a standard feature of the Model 40. This channel is capable of controlling several low to medium speed I/O units concurrently in multiplex mode or a single high-speed unit in burst mode.

The channel facility necessary to sustain an I/O operation with an I/O device is called a subchannel. The number of multiplexer subchannels is determined by the size of the main storage unit. See Figure 2. In the multiplex mode, the multiplexer channel sustains concurrent I/O operations on several subchannels. Bytes of data are interleaved and transmitted to or from the selected I/O devices and to or from the desired locations in main storage. A maximum of eight control units may be attached to the multiplexer channel.



	Capacity/Number	Data Width	Access/Speed/Rate
General registers	16	1 word	1.25 R/W cycle/16 bits
Floating-point registers	4	2 words	1.25 R/W cycle/16 bits
Adder		1 byte	0.625 microsecond
Local storage			1.25 microsecond R/W cycle*
Read only storage			0.625 microsecond Rd cycle
Basic machine cycle			0.625 microsecond
Multiplexer channel			
Burst mode		1 byte	See section on channel loading
Multiplex mode		1 byte	
Selector channel		2 bytes	
Data transfers			
Processor to storage		2 bytes	
Storage to storage		2 bytes	
Selector channel to processor		2 bytes	
Multiplexer channel to processor		1 byte	
Control unit to channel		1 byte	

* Can be split cycled on occasions giving effective access of 0.625 microseconds.

● Figure 2. Model 40 Data Flow Diagram and System Statistics

In burst mode, the multiplexer channel sustains one I/O operation on one subchannel. Only one I/O device can be selected at a time and no other device on the multiplexer channel can transfer data until the selected I/O activity has been terminated.

Selector Channel

One or two selector channels are available, as optional features, for the Model 40. The selector channel operates in burst mode only, although up to eight control units can be attached and the channel has the facilities for addressing up to 256 devices. Only one I/O device may be selected at a time on a selector channel. No other I/O device on the selector channel can transfer data until the selected activity has been terminated.

System Control Panel

The system control panel located on one end of the 2040 Processing Unit provides the switches, the keys and the lights necessary to operate, monitor and control the Model 40. The need for operator manipulation of manual controls is held to a minimum by the system design and the governing supervisory program. A detailed description of operator functions provided by the switches, keys and lights of the control panel is located in the system control panel section of this manual.

Instruction Configurations

The Model 40 is available with many different instruction configurations. The minimum configuration is the standard instruction set. The standard instruction set, with the addition of the decimal feature, comprises the commercial instruction set. The standard instruction set, with the addition of the floating-point feature, comprises the scientific instruction set. The standard instruction set, with the decimal feature, floating-point feature and storage protection feature composes the universal instruction set.

The direct control feature adds 2 additional instructions.

Descriptions of all instructions are found in the *IBM System/360 Principles of Operation,* Form A22-6821. Timing information for each of the instructions is found in the instruction timing information section of this manual.

Interruption Times

Interruption times vary for the class of interruption and the type of instruction being executed at the time of the interruption. The following information gives the interruption times for the five classes of interruptions, with examples when applicable, to show how the interruption times can vary.

External Interruption

External interruption extends from the time the external interruption is discovered to the next instruction. The time is 25.63 microseconds.

Supervisor Call Interruption

Supervisor call interruption extends from the time the supervisor call interruption is discovered to the next instruction. The time is 23.75 microseconds.

Program Interruption

Program interruption extends from the time the program interruption is discovered to the next instruction. The program interruption time is equal to or less than the following time, plus the instruction time.

20.63 microseconds after an RR or RX instruction.
20.00 microseconds after an RS or SS instruction.

Examples: Time assumes base register not equal to 0. Add 1.25 microseconds to total time if an RX instruction is indexed.

1. Invalid Operations
   - 00 23.75 μs
   - 4D 29.38 μs
   - C0 23.13 μs
   - D8 31.25 μs
   - F0 32.50 μs
2. RX fixed-point full word
   28.23 μs
3. Odd or invalid instruction addresses
   24.38 μs

Machine Check Interruption

Machine check interruption time extends from the time the machine check interruption is discovered to the next instruction. The time is 572 microseconds and includes scan out and reset time.

I/O Interruption

I/O interruption time depends on the type of I/O interruption and the type of channel.

	MULTIPLEXER CHANNEL	SELECTOR CHANNEL
Device end	56.88+U_1 μs*	60.0+U_1 μs*
Channel end	60.63 μs	40.63 μs
Program Controlled Interruption (PCI)	61.88 μs	40.63 μs

*See timing chart legend U_1.

System Control Panel

The system control panel contains the switches and lights necessary to operate, display, and control the system. The system consists of the CPU, storage, channels, on-line control units, and I/O devices. Off-line control units and I/O devices, although a part of the system environment, are not considered part of the system proper.

System controls are logically divided into three classes: operator control, operator intervention, and customer engineer control. This section of the manual discusses the system control functions provided by the system control panel as well as the purpose and use of the switches and lights on the panel.

System Control Functions

Using the control panel, the operator can perform these system control functions:

1. Reset the system.
2. Store and display information in storage and registers.
3. Load initial program information.

System Reset

The system reset function resets the CPU, channels, and on-line, nonshared control units and I/O devices.

The CPU is placed in the stopped state and all pending interruptions are eliminated. The parity of the general and floating-point registers, as well as the parity of the PSW are corrected. All error-status indicators are reset to zero.

In general, the system is placed in such a state that processing can be initiated without the occurrence of machine checks, except those caused by subsequent machine malfunction.

The reset state for a control unit or device is described in the appropriate System Reference Library (SRL) publication. A system reset signal from a CPU resets only the functions in a shared control unit or device belonging to that CPU. Any function pertaining to another CPU remains undisturbed.

The system reset function is performed when the system reset key is pressed, when initial program loading is initiated, or when a power-on sequence is performed.

Programming Notes

If a system reset occurs in the middle of an operation, the contents of the PSW and of the result registers or storage locations are unpredictable. If the CPU is in the wait state when the system reset is performed, and I/O is not working, this uncertainty is eliminated.

A system reset does not correct parity in storage but does correct parity in the registers. Because a machine check occurs when information with incorrect parity is used, the incorrect information should be replaced by loading new information.

Store and Display

The store and display function permits manual intervention in the progress of a program. The storing and/or displaying data may be provided by a supervisor program in conjunction with proper I/O equipment and the interrupt key.

In the absence of an appropriate supervisor program, the controls on the operator intervention panel allow direct storage and display of data. This is done by placing the CPU in the stopped state, and subsequently storing and/or displaying information in main storage, in general and floating-point registers, and in the instruction-address part of the PSW. The stopped state is achieved at the end of the current instruction when the stop key is pressed, when single instruction execution is specified, or when a preset address is reached. The store and display function is then achieved through the store and display keys, the address switches, the data switches and the storage select switch. Once the desired intervention is completed, the CPU can be started again.

All basic store and display functions can be simulated by a supervisor program. The stopping and starting of the CPU in itself does not cause any alteration in program execution other than the time element involved in the transition from operating to stopped state.

Machine checks occurring during store and display functions do not log immediately, but create a pending log condition that can be removed by a system reset or check reset. The error condition, when not masked off, forces a log-out and a subsequent machine check interruption when the CPU is returned to the operating state.

Initial Program Loading

Initial program loading (IPL) is provided for the initiation of processing when the contents of storage or the PSW are not suitable for further processing.

Initial program loading is initiated manually by selecting an input device with the load-unit switches and subsequently pressing the load key.

Pressing the load key causes a system reset, turns on the load light, turns off the manual light, and subsequently initiates a read operation from the selected input device. When reading is completed satisfactorily, the IPL PSW is obtained, the CPU starts operating, and the load light is turned off.

System reset suspends all instruction processing, interruptions, and timer updating and also resets all channels, on-line nonshared control units, and I/O devices. The contents of general and floating-point registers remain unchanged.

When IPL is initiated, the selected input device starts reading. The first 24 bytes read are placed in storage locations 0-23. Storage protection, program controlled interruption, and a possible incorrect length indication are ignored. The double word read into location 8 is used as the channel command word (CCW) for a subsequent I/O operation. When chaining is specified in this CCW, the operation proceeds with the CCW in location 16. Either command chaining or data chaining may be specified.

After the input operation is performed, the I/O address is stored in bits 21-31 of the first word in storage. Bits 16-20 are made zero. Bits 0-15 remain unchanged.

The CPU subsequently fetches the double word in location 0 as a new PSW and proceeds under control of the new PSW. The load light is turned off. When the I/O operations and PSW loading are not completed satisfactorily, the CPU idles, and the load light remains on.

Programming Notes

Initial program loading resembles a start I/O that specifies the I/O device selected in the load-unit switches and a zero protection key. The CCW for this start I/O is simulated by CPU circuitry, and contains a read command, zero data address, a byte count of 24, chain command flag on, suppress-length-indication flag on, program-controlled-interruption flag off, chain-data flag off and skip flag off. The CCW has a virtual address of zero.

Initial program loading reads new information into the first six words of storage. Since the remainder of the IPL program may be placed in any desired section of storage, the areas of storage reserved for the timer and PSW's may be preserved.

If the selected input device is a disk, the IPL information is read from track 0.

The selected input device may be a channel-to-channel adapter connecting the channels of two CPU's. After a system reset is performed, and a read command is issued to the adapter by the requesting CPU, the adapter sends an attention signal to the addressed CPU. That CPU then should issue the write command necessary to load a program into main storage of the requesting CPU.

When the PSW placed in location 0 has bit 14 set to one, the CPU goes into the wait state after the IPL procedure (the manual, system, and load lights are off, and the wait light is on). Interruptions that become pending during IPL are taken before instruction execution.

System Control Panel Controls

System controls are divided into three logical groups identified as operator control, operator intervention and customer engineer control. Figure 3 shows the operator controls located in areas labeled B and H and operator intervention controls in areas F and G of the system control panel. The customer engineer will use all controls, but the controls in areas C and D are intended primarily for customer engineer use.

Operator Controls

Sections B and H of the system control panel contain the controls required by the operator when the CPU is operating under full supervisor control. Under supervisor control, a minimum of direct manual intervention is required because the supervisor performs operations such as store and display.

The main functions provided by the operator controls are the control and indication of power, the indication of system status, operator to machine communication and initial program loading. The controls in area H are identical in all models of the System/360.

The following table lists all operator controls and indicators by name and their implementation. All operator controls except the emergency pull switch are located in the area labeled H of the control panel shown in Figure 3. The emergency pull switch is located in area B.

NAME	IMPLEMENTATION
Emergency Pull	Pull switch
Power On	Key, backlighted
Power Off	Key
Interrupt	Key
Load Unit	Three rotary switches
Load	Key
Wait	Light
Manual	Light
System	Light
Test	Light
Load	Light

NOTE: All keys have momentary action.

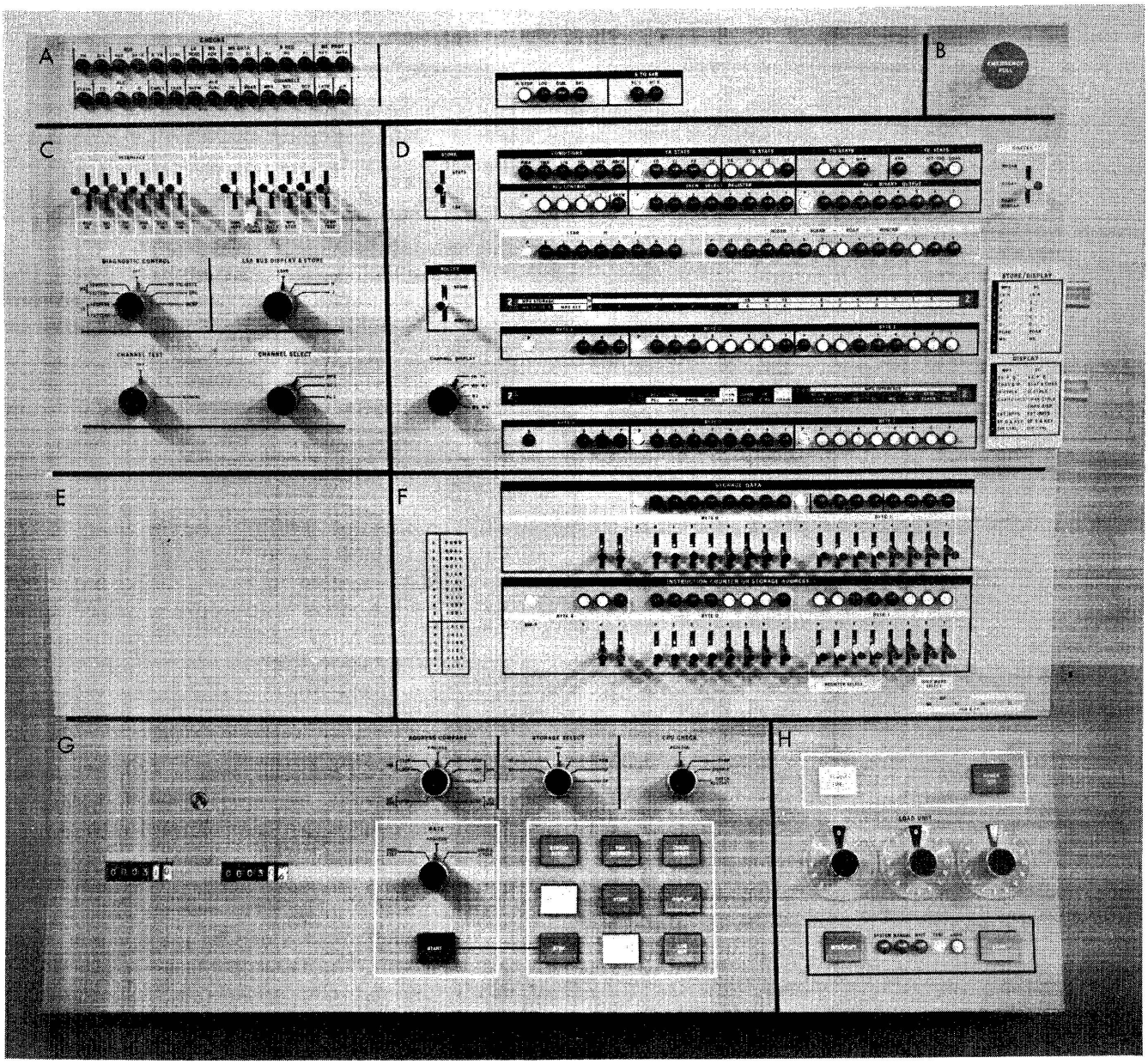


Figure 3. Model 40 System Control Panel

Emergency

Pulling this switch turns off all power beyond the power-entry terminal on every unit that is part of the system or that can be switched onto the system. (Exception: In the CPU, primary power is available within the unit at CB1.) Therefore, the switch controls the system proper and all off-line and shared control units and I/O devices.

The switch latches in the out position and can be restored to its in position by maintenance personnel only.

When the emergency pull switch is in the out position, the power-on key is ineffective.

Power On

This key is pressed to initiate the power-on sequence of the system.

As part of the power-on sequence, a system reset is performed in such a manner that the system performs no instructions or I/O operations until explicitly directed. The contents of main storage, including the protection keys, remain preserved.

The power-on key is backlighted to indicate when the power-on sequence is completed. The key is effective only when the emergency pull switch is in the in position.

Power Off

The power-off key is pressed to initiate the power-off sequence of the system.

The contents of main storage and its protection keys are preserved, provided that the CPU is in the stopped state. The key is effective while power is on the system.

Interrupt

The interrupt key is pressed to request an external interruption.

The interruption is taken when not masked off and when the CPU is not stopped. Otherwise, the interruption request remains pending. Bit 25 in the interruption-code portion of the current PSW is made 1 to indicate that the interrupt key is the source of the external interruption. The key is effective while power is on the system.

Load Unit

Three rotary switches provide the 11 rightmost bits of the I/O address to be used for initial program loading.

The leftmost rotary switch has eight positions labeled 0-7 used for the channel address. The other two 16-position rotary switches are labeled with the hexadecimal characters 0-9, A-F, and are used for the unit address.

Load

The load key is pressed to start initial program loading. The key is effective while power is on the system.

Wait

The wait light is on when the CPU is in the wait state.

Manual

The manual light is on when the CPU is in the stopped state. Several of the manual controls are effective only when the CPU is stopped (manual light on).

System

The system light is on when the CPU usage meter or customer engineer meter is running.

Programming Notes

The states indicated by the wait and manual lights are independent of each other; however, the state of the system light is not independent of the state of these two lights because of the definition of the running condition for the meters. The following table shows possible conditions when power is on:

SYSTEM LIGHT	MANUAL LIGHT	WAIT LIGHT	CPU STATE	I/O STATE
Off	Off	Off	*	*
Off	Off	On	Wait	Not working
Off	On	Off	Stopped	Not working
Off	On	On	Stopped, wait	Not working
On	Off	Off	Running	Undetermined
On	Off	On	Wait	Working
On	On	Off	Stopped	Working
On	On	On	Stopped, wait	Working

* Abnormal condition

Test

The test light is on when a manual control is not in its normal position or when a maintenance function is being performed for CPU, channels, or storage.

Any abnormal switch setting on the system control panel or on any separate maintenance panel for the CPU, storage, or channels that can affect the normal operation of a program causes the test light to be on.

The following switches cause the test light to be on if any are not in their normal position:

Rate switch not to process
Diagnostic control switch not to off
Address compare switch not to process
Channel test switch not to off
Reverse data parity switch on
Display lever switch not set to ROBAR
MPX store switch on
Disable interval timer switch on
CPU check switch not to process
Key-operated meter switch to CE
Any manual interface switch on
DSAB IRPT switch on

The test light may be on when one or more diagnostic function under control of DIAGNOSE is activated or when certain abnormal circuit breaker or thermal conditions occur.

The test light does not reflect the state of marginal voltage controls.

Load

The load light is on during initial program loading; it is turned on when the load key is pressed and is turned off after the loading of the new PSW is completed successfully.

Operator Intervention Controls

Sections G and F of the system control panel contain the controls required for the operator to intervene in

normal programmed operation. These controls are intermixed with the customer engineer controls. Only operator intervention controls are described in detail.

Operator intervention controls provide the system reset and the store and display functions.

The following table lists all intervention controls and indicators by name and their implementation.

NAME	IMPLEMENTATION
System Reset	Key
Check Reset	Key
Stop	Key
Rate	Rotary switch
Start	Key
Storage Select	Rotary switch
Address	Lever switches
Data	Lever switches
Store	Key
Display	Key
Log-Out	Key
PSW Restart	Key
Address Compare	Rotary switch
CPU Check	Rotary switch

NOTE: All keys have momentary action.

System Reset

The system reset key is pressed to cause a system reset; it is effective while power is on the system. A system reset resets CPU, channels, and control units to their initial state. All CPU and channel error indicators are reset to the no-error state. The CPU is placed in the stopped state, and all pending interruptions are eliminated.

Check Reset

The check reset key resets all CPU and channel error indicators to the no-error state. The check reset function can thus be considered a subset of the system reset function.

Check reset can be performed regardless of the setting of the rate switch. Error indicators remaining on after check reset must be cleared at the error source by use of appropriate manual controls.

Stop

The stop key causes the CPU to enter the stopped state and turns on the manual light. (The CPU first completes the instruction being executed at the time the stop signal is recognized, and processes all pending unmasked interruptions.) Any I/O operation in progress is completed, while the CPU is in the (manual) stop state. The key is effective while power is on the system.

Pressing the stop key has no effect when a continuous string of interruptions is performed or when the CPU is unable to complete an instruction because of machine malfunction.

Rate

This three-position rotary switch is used to indicate the manner in which instructions are to be performed. The position of the switch should be changed only while the CPU is in the stopped state. Otherwise, unpredictable results may occur. The rate switch positions and their effects are:

Process: The system starts operating at normal speed when the start key is pressed. The test light is on when the rate switch is not set to PROCESS.

Insn Step (Instruction Step): The system executes one instruction each time the start key is pressed. After each instruction is executed, all pending interruptions not masked off are taken. The CPU then returns to the stopped state. The timer is not updated when the switch is in this position.

Any instruction can be executed with the rate switch set to INSN STEP. Input/output operations are completed to the interruption point. When the CPU is in the wait state, no instruction is performed, but pending interruptions, if any, are taken before the CPU returns to the stopped state. Initial program loading is completed with the loading of the new PSW before any instruction is performed.

Single Cycle: The system executes one machine cycle each time the start key is pressed. Single cycle operates with I/O equipment to the point of initiation of the asynchronous operation. The asynchronous operation begins the next time the start key is pressed and runs to completion. The single cycle position is primarily for customer engineer use.

Start

The start key is pressed to start instruction execution as specified by the rate switch. The key is effective only while the CPU is in the stopped state.

Pressing the start key after a normal stop causes instruction processing to continue as if no stop had occurred, provided that the rate switch is in the PROCESS or INSN STEP position. Pressing the start key after system reset without first introducing a new instruction address may yield unpredictable results.

Storage Select

This six-position rotary switch indicates whether the contents of main storage or one of a variety of registers are to be displayed or replaced by new data. The actual main storage or register address is given by the address lever switches. The switch is active only in the stopped state (manual light on). The storage select switch has the following settings:

MS (Main Storage): Selects a main storage location specified by the address switches.

GP (General Register): Selects a general register specified by the register-select address switches.

FP (Floating Point): Selects a floating-point register specified by the register-select address switches.

IC (Instruction Counter): Automatically selects the instruction counter register (instruction address in the PSW).

PSW (Program Status Word): Selects the register containing the current program status word.

SP (Storage Protection): Selects the storage protection key register.

Address Switches

When used with the storage select switch, the 18 address lever switches provide a means of manually addressing a location in storage. Correct parity is automatically generated.

Addressing Main Storage: When the storage select switch is set to the MS position, the 18 address switches are used to manually address a main storage location.

When main storage is being addressed, the 18 switches represent the 18 low-order bits of a 24 bit binary address. Because the Model 40 has a maximum of 262,144 bytes of main storage, these 18 switches are sufficient for addressing all main storage locations.

The rightmost switch is the units position. Because data, in main storage, are stored or displayed a half word at a time, the units position address switch is not involved in determining the address.

When an address switch is in the down position it represents a 1 bit; when in the center or restored position it represents a 0 bit. The setting of the address switches in the correct order of 1 and 0 positions is used to represent the low-order positions of a 24 bit binary number to address main storage.

The address switches are color coded to help identify the hexadecimal digit groupings.

Selecting the General and Floating-Point Registers: Four lever switches, a subset of the address switches, are used to select one of 16 general registers (0-15) or one of four floating-point registers (0, 2, 4, 6) when used with the proper setting of the storage select switch.

With the storage select switch set to the GP position, a general (purpose) register is selected by setting its number (0-15) into the four register select switches located in positions 0, 1, 2, and 3 of byte 1. Information is displayed or stored a half word at a time for the general registers. Address switch 7, located in byte 1, is used to select the register half word. When the address switch is set in the 0 position (center), it selects the first half word; when set in the 1 position (down), it selects the second half word. Address switches 4, 5, and 6 of byte 1 are not used.

The address format is:

Address switches — byte 1

0	1	2	3	4	5	6	7	
0	1	1	1	x	x	x	0	1st half word general register 7
0	1	1	1	x	x	x	1	2nd half word general register 7
1	1	0	1	x	x	x	0	1st half word general register 13
1	1	0	1	x	x	x	1	2nd half word general register 13

x = no effect

When the storage select switch is set to FP (floating-point) position, a floating-point register is selected by setting its number (0, 2, 4, or 6) into the four register select switches located in positions 0, 1, 2, and 3 of byte 1.

Information is stored or displayed one half word at a time for the floating-point registers. Address switches 6 and 7 of byte 1 are used to select the required half word. Address switches 4 and 5 of byte 1 are not used.

The address format is:

Address switches — byte 1

0	1	2	3	4	5	6	7	
x	1	1	x	x	x	0	0	1st half word — FP register 6
x	1	1	x	x	x	0	1	2nd half word — FP register 6
x	1	1	x	x	x	1	0	3rd half word — FP register 6
x	1	1	x	x	x	1	1	4th half word — FP register 6

Selecting the Program Status Word (PSW): The PSW is contained in two words occupying four locations in local storage. PSW information is displayed or stored a half word at a time; thus, four operations are required to store or display the data of a PSW.

The PSW half word is selected by setting the storage select switch in the PSW position, and by setting the number 0, 1, 2, or 3 into address switches 6 and 7 located in byte 1 of the address switches. Address switches 0, 1, 2, 3, 4, and 5 of byte 1 are not used.

The address format is:

Address switches — byte 1

x	x	x	x	x	x	0	0	1st PSW half word
x	x	x	x	x	x	0	1	2nd PSW half word
x	x	x	x	x	x	1	0	3rd PSW half word
x	x	x	x	x	x	1	1	4th PSW half word

Selecting the Instruction Counter (IC): Setting the storage select switch to the IC position automatically selects the instruction counter. The register select switches are not required. See "Store" and "Display."

Selecting the Storage Protection Register: Setting the storage select switch to the SP position automatically selects the storage protection register (PSW protection key data). The register select switches are not required. See "Store" and "Display."

Data Switches

The storage data switches (upper group of 18 switches in panel F) are used to represent the data to be stored in the location indicated by the storage select switch and the address switches. Correct data parity is automatically generated.

The storage data switches can be used to represent a half word of information. The two leftmost switches are not used as part of the half word for customer store functions. A storage data switch in the down position represents a 1 bit and in the center position a 0 bit.

Store

The store key is pressed to store information in the location specified by the storage select switch and address switches. The key is effective only while the CPU is in the stopped state.

When the store key is pressed, the number indicated by the data switches is placed in the specified location in main or local storage or in a general or floating-point register. *Storage protection is ignored.* When the location designated by the address switches and storage select switch is not available, data is not stored.

When the storage select switch is set to MS, pressing the store key stores the data bytes represented by the data switches into the main storage location indicated by the address switches. The data bytes stored are displayed in the 18 (16 data plus two parity) storage data lights, and the address generated by the address switches is displayed in the storage address lights.

When the storage select switch is set to GP, pressing the store key stores the data bytes represented by the data switches into the general register half word addressed by the storage address switches. The data bytes stored are displayed in the storage data lights, and the address generated by the address switches is displayed in the storage address lights.

When the storage select switch is set to FP, pressing the store key stores the data bytes represented by the data switches into the floating-point register half word addressed by the storage address switches. The data bytes stored are displayed in the storage data lights, and the address generated by the address switches is displayed in the storage address lights.

When the storage select switch is set to IC, pressing the store key places the address indicated by the 18 storage address switches into the instruction address portion of the PSW. The instruction address stored is displayed in the storage address lights.

When the storage select key is set to PSW, pressing the store key places the data bytes represented by the data switches into the PSW half word addressed by the register select switches. The data bytes stored are displayed in the 16 storage data lights, and the address generated by the register select switches is displayed in the storage address lights.

When the storage select key is set to SP, pressing the store key stores the data bytes represented by the data switches into the storage protection register (PSW protection key area). The data stored is displayed in the storage data lights.

Display

The display key is pressed to display information in the location specified by the storage select switch and address switches.

The specified data in main or local storage or in a general or floating-point register is displayed in the storage data lights.

When the designated location is not available, the displayed information is unpredictable.

The key is effective only while the CPU is in the stopped state.

Log-Out

A ROS microprogram, log-out, is automatically executed on detection of any CPU or channel error or on depressing the log-out key. Log-out is the technique of recording in main storage, the status of the CPU and channels existing immediately prior to the initiation of the log-out. The log-out area of main storage is at locations 128-384.

On completion of the log-out microprogram, the CPU checkout microprogram is automatically executed. The checkout microprogram tests and diagnoses large sections of the CPU. Any error detected by the checkout microprogram or any machine error occurring during the execution of the checkout microprogram will result in an immediate stop.

Successful execution of the checkout microprogram is followed by a system reset and a machine interruption. The machine interruption stores the current PSW in the machine check old PSW location (48) of main storage and loads the PSW from the machine check new PSW location (112) of main storage. The system at this point is returned to an operating state.

The checkout microprogram, following a log-out operation, helps to guarantee the validity of the log-out information. If a log-out occurred, and the CPU is not returned to an operating state following the checkout microprogram, the validity of the log-out information could be in question.

The CPU checkout microprogram is executed under the following conditions:

After depression of system reset key
After depression of the load key
After depression of start key with diagnostic control set to CPU
Immediately after a log-out operation

PSW Restart

A PSW is loaded from storage location zero and the CPU is changed from stopped to operating state.

Address Compare

The address compare switch provides a means of stopping the CPU on a successful address comparison. The process position of the switch is the normal operating position. Only the stop on MS position concerns operator intervention. The remainder of the switch positions are for customer engineer use.

The address compare switch can be manipulated without disrupting CPU operation other than by causing the address-comparison stop. When the switch is set to any position except PROCESS, the test light is on.

Stop on MS (Main Storage): When the instruction or data fetching mechanism accesses a main storage location indicated by the address set in the address keys, the processor enters the stopped state at the completion of the current machine instruction.

Programming Note

When an address not used in the program is selected in the address switches, the CPU runs as if the address-compare switch was set to PROCESS.

CPU Check

The CPU check rotary switch provides selective control of the system upon error.

Process Position: In the normal processing mode, if the machine check mask bit in the PSW is on, the processor will pause on an error, a log-out will occur, followed by system reset with a CPU checkout and a machine-check interruption.

Stop Position: On error detection, the CPU stops. CPU is interruptible.

Disable Position: On error detection, the error checking indication is still active but machine operation continues without log-out.

Check Restart Position: On error detection, the checker is activated and error latch is set. System reset, CPU checkout, and machine-check interruption follow.

Key Switch and Meters

The customer usage (CPU) meter and the CE meter are on panel G of the system control panel. The CE *key* switch controls which of these meters is to be run while the system is in operation; i.e., initiating, executing, or completing instructions including I/O and assignable unit operations. The test light is turned on when the key (meter) switch is in the CE meter position. (For other conditions, see "Test.") The system light, located on panel H, indicates when the system is in operation.

Channel Characteristics and Functional Evaluation

This channel section has three purposes. It specifies:

1. Model 40 channel implementation.
2. How to determine whether the I/O devices required to run concurrently by a particular application will perform satisfactorily.
3. How to determine the available CPU time during I/O operations.

General Channel Information

IBM System/360 channels transfer data between core storage and I/O devices under control of a channel program executed independently of the CPU program. The Model 40 CPU is free to resume the CPU program after initiating an I/O operation, except for burst mode operation of the multiplexer channel.

Model 40 channels may run concurrently, within the data transfer rate and channel programming conventions specified in this manual.

A major feature of the channels is their common I/O interface connection to all System/360 input/output control units. The I/O interface provides for attachment of a variety of I/O devices to a channel.

At the end of an I/O operation, the channel signals an I/O interruption request to the CPU. If not masked off, an I/O interruption occurs that places the I/O new PSW in control of the CPU. When I/O interruptions are masked, interruption requests are queued. Until honored, an I/O interruption condition is called a pending I/O interruption.

At the end of an I/O operation, a channel has information concerning the success of the operation, or details about any lack of success. The information is available to the CPU program.

Each System/360 channel has facilities for performing the following functions:

Accepting an I/O instruction from the CPU
Addressing the device specified by an I/O instruction
Fetching the channel program from core storage
Decoding the channel command words that make up the channel program
Testing each channel command word (CCW) for validity
Executing CCW functions
Placing control signals on the I/O interface
Accepting control-response signals from the I/O interface
Transferring data between an I/O device and core storage
Checking parity of bytes transferred
Counting the number of bytes transferred
Accepting status information from I/O devices
Maintaining channel-status information
Signaling interruption requests to the CPU
Sequencing interruption requests from I/O devices
Sending status information to location 64 when an interruption occurs
Sending status information to location 64 upon CPU request

Channel Control

IBM System/360 channels provide a common input/output interface to all System/360 control units. All control units are governed with six basic channel commands and a common set of only four CPU instructions. The instructions are:

Start I/O
Test channel
Test I/O
Halt I/O

All I/O instructions set the PSW condition code, and, under certain conditions, all but test channel may cause a channel status word to be stored. A test channel instruction elicits information about the addressed channel; a test I/O instruction elicits information about a channel and a particular device. Halt I/O terminates any operation on the addressed channel, subchannel, or device. None of the three instructions makes use of channel command words (CCW's).

A start I/O instruction initiates execution of one or more I/O operations. It specifies a channel, subchannel, control unit, and I/O device. It causes the channel to fetch the channel address word (CAW) from location 72. The CAW contains the protection key and the address of the first channel command word (CCW) for the operation. The channel fetches and executes one or more CCW's, beginning with the first CCW specified by the CAW.

Six channel commands are used:

Read
Write
Read backward
Control
Sense
Transfer in channel

The first three are self-explanatory.

Control commands specify such operations as set tape density, rewind tape, advance paper in a printer, etc.

A sense command brings information from a control unit into main storage concerning unusual conditions detected during the last I/O operation, and detailed status about the device.

A transfer in channel (TIC) command specifies the location in main storage from which the next CCW in the channel program is to be fetched. A TIC may not specify another TIC. Also, the CAW may not address a TIC.

Each CCW specifies the channel operation to be performed and, for data transfer operations, specifies contiguous locations in main storage to be used. One or more CCW's make up a channel program that directs a channel operation.

Channel Registers

System/360 channels maintain the following channel control information for each I/O device selected for operation:

Protection key (when applicable)
Data address
Identity of operation specified by command code
CCW flags
Byte count
Channel status
Address of next CCW

A selector channel has only one set of registers for the above information because it operates with only one I/O device at a time.

On a multiplexer channel, the listed information must be maintained for each subchannel in operation. Storage for this information is provided by special channel storage that is not directly addressable. Each subchannel has provision in channel storage for channel register information. When a particular subchannel is selected by a start I/O instruction and a channel program initiated, the channel storage locations for the subchannel are loaded with the information necessary for operation of the subchannel.

The channel refers to channel storage in order to communicate with a device and with main storage. At each cessation of activity in a subchannel, its particular area in channel storage contains updated information, and the multiplexer channel is available for operation of another subchannel. The sharing of facilities by the multiplexer channel and the CPU is shown in Figure 4.

Chaining

A single CCW may specify contiguous locations in main storage for a data transfer operation, or successive CCW's may be chained together to specify a set of noncontiguous storage areas. Chaining to the next CCW is caused by the presence of a flag bit in a CCW.

In data chaining, the address and count information in a new CCW is used; the command code field is ignored.

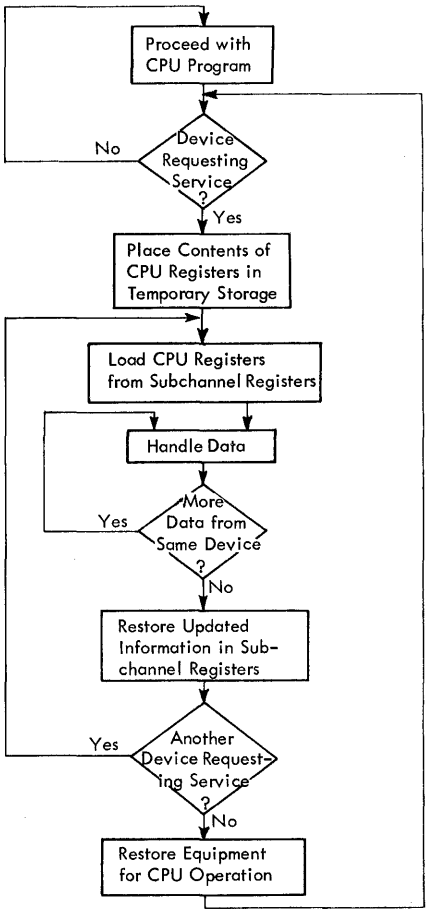


Figure 4. Equipment Sharing by Model 40 CPU and Multiplexer Channel

Entire CCW's, including the command code field, may also be chained together for use in a sequence of channel operations. Such coupling is called command chaining, and is specified by a different flag bit in a CCW. Command chaining provides additional control information for operation of a device.

Data chaining has no effect on a device, as long as the channel has sufficient time to perform both data chaining and data transfer for the device.

In this manual, when a device is said to data chain, it means that the channel program for the device specifies data chaining.

Fetching Channel Command Words

The channel must fetch a new CCW whenever a CCW specifies data chaining, command chaining, or transfer in channel (TIC). The extra control activity caused by these operations takes time and diminishes a channel's ability to do other work.

A data chaining fetch usually occurs while a channel also has a data transfer load from the same device.

The time required to fetch the new CCW necessarily limits the interval of time available for successive data transfers through the channel. An absence of data chaining ordinarily permits a channel to operate with a faster I/O device. Similarly, when a channel is not transferring data, a data chaining operation has a lesser impact on channel facilities.

Data Chaining in Gaps

For direct access storage devices, such as IBM 2311 Disk Storage or IBM 2303 Drum Storage, formatting write commands cause the control unit to create gaps between count, key, and data fields on the recording track. Read, write, and search commands that address more than one of the fields may specify data chaining to define separate areas in main storage for the fields.

The gaps on a track have significance to channel programming considerations for direct access storage devices. The channel does not transfer data during the time a gap is created or passes under the read-write head, and this time is sufficient for a Model 40 to perform a command chaining or data chaining operation.

Command chaining ordinarily occurs only during gap time, but data chaining may occur during gap time or while data is being transferred. A data chaining operation occurring during gap time has a lesser impact on channel facilities than when data transfers also occur. If a channel program for a direct access storage device calls for data chaining only during gap time, the device's overall load on channel facilities is significantly less.

When a direct access device is said to data chain in a gap, the reference is to a gap other than a gap following a data field. The latter gap causes a device end indication and command chaining is used in such a gap if the transfer of more information is desired. A device end occurring in the absence of a CCW specifying command chaining results in termination of the operation. When command chaining continues the operation, the status information available at the end of the operation relates to the last operation in the chain.

While reading, an attempt to data chain in a gap following a data field causes an incorrect length indication in the channel status byte.

Late Command Chaining

Operation of direct access devices, such as disk storage, requires the use of command chaining. Between certain operations, such as the search for a record identification key and the reading of a data field on a direct access storage device, the control unit has a fixed time interval during which it must receive and execute a new command. If activity on other channel(s) causes too much delay in initiation of the operation specified by the new command, the channel program is terminated and an I/O interruption condition occurs.

Storage Addressing

When data chaining, the beginning and ending byte addresses and the minimum number of bytes transferred are factors in the maximum data rates that different System/360 channels can sustain. If the storage width of larger models and the possibility of using faster I/O devices are kept in mind when writing channel programs for small models, better performance will be obtained when the programs run on larger models or with faster I/O devices.

For example, a tape operation at a 30 kb (kilobyte) data rate may data chain with a byte count of one on a Model 30 with one selector channel, but the same tape operation cannot be performed at 90 kb on a Model 40. In this instance, the use of a larger count for data chaining would permit the Model 40 to execute the channel program at 90 kb.

Data chaining and other aspects of channel programming compatibility for the various models of System/360 are discussed in "Conventions for Satisfactory Channel Programs."

The Model 40 has two types of channels. One or two selector channels are optional; the multiplexer channel is standard.

Each selector channel provides a path for moving data between storage and a selected I/O device. It has its own address register and data buffers. Provision is made for as many as 256 device addresses. A selector channel on the Model 40 has buffering to move data to or from storage one or two bytes at a time. Data goes to or from an I/O device one byte at a time.

All channels on the Model 40 are integrated with the 2040 Processor and share part of the CPU facilities. Channel operations are overlapped with CPU operations except for burst mode operations on the multiplexer channel. A multiplexer channel has a single data path that may be monopolized by one I/O device or shared concurrently by many selected I/O devices. Transfer of a byte on the multiplexer channel requires use of CPU facilities. When a single device pre-empts multiplexer channel facilities, the operation is in burst mode. During such operation, CPU facilities are used for data transfer; no instruction may be executed.

As many as eight control units may be attached to a channel. A control unit determines whether its operation on the multiplexer channel is in burst mode or in multiplex mode. All selector channel operations are in burst mode.

Channel Priority

Priority for allocation of Model 40 CPU facilities is in this order:

1. Machine check interruption handling
2. Selector channel data transfer
3. Selector channel data chaining
4. Selector channel command chaining
5. Multiplexer channel operation
6. CPU operation

Selector channels 1 and 2 alternate priority, except that selector channel 1 is favored when both request service during a CPU cycle.

Multiplexer Subchannels

When multiple I/O devices concurrently share multiplexer channel facilities, the operations are in multiplex mode. Each device in operation is selected, one at a time, for transfer of a byte or a few bytes to or from main storage. Bytes from multiple devices are interleaved together and routed to or from desired locations in main storage. Thus, the multiplexer channel data path is used by one device for transfer of one or a few bytes of data and then another device uses the same data path. The sharing of the data path makes each device to appear to the programmer as if it has a data path of its own. This leads to calling a device's share of the data path as a subchannel. Each data path available to a programmer is called a subchannel.

The numbering scheme for multiplexer subchannels relates to I/O device addresses; the device address assigned to each device determines the subchannel that controls its operation. For an unshared subchannel, one device address is used. A shared subchannel permits use of several device addresses. The devices share a single control unit, which connects them to the shared subchannel. The devices may be selected for use one at a time, but may not be selected concurrently.

Device addresses zero to less than 128 refer uniquely to the correspondingly numbered unshared subchannels. Devices addressed 128-255 are assigned to shared subchannels 0-7 in eight groups of 16. For example, subchannel zero may be used by device addresses 000 or 128-143, and subchannel 1 may be used by device addresses 001 or 144-159, etc. Thus, each shared subchannel 0-7 has 17 different device addresses. Unshared control units may use shared subchannel addresses in the lower range; shared control units use addresses in the higher range.

The maximum number of multiplexer channel device addresses is 128 in the shared range, plus the number of uniquely addressed subchannels provided by the system. In the listing below, the Model D40 has 16 multiplexer subchannels; eight are shared subchannels (addresses 0-7 and 128-255) and eight are unshared subchannels (addresses 8-15).

MODEL	SUB-CHANNELS	I/O DEVICE ADDRESSES	SHARED SUBCHANNEL I/O DEVICE ADDRESSES	UNSHARED SUBCHANNEL I/O DEVICE ADDRESSES
D40	16	0-15, 128-255	0-7, 128-255	8-15
E40	32	0-31, 128-255	0-7, 128-255	8-31
F40	64	0-63, 128-255	0-7, 128-255	8-63
G40	128	0-255	0-7, 128-255	8-127
H40	128	0-255	0-7, 128-255	8-127

Concurrent Input/Output Capabilities

Each I/O device in operation places a load on its channel facilities. The magnitude of a load depends on a device's channel programming and its data transfer rate. In this manual, numeric factors are used to relate the loads caused by operation of I/O devices to the channel's abilities to sustain concurrent operation of the devices.

One or more numeric factors are specified for each I/O device and channel available with a Model 40. The numeric factors are referenced from tables in this manual and used in arithmetic procedures that indicate satisfactory or less than optimum operation for specific Model 40 input/output configurations.

Several procedures are provided for evaluating a configuration of I/O devices for concurrent operation on Model 40 channels. Channel programming considerations are included. Use of the basic procedures will suffice to find an indication of satisfactory operation for most configurations; the more detailed procedures are used only for configurations that approach or temporarily exceed Model 40 input/output capabilities.

Worst Case Loads

The evaluation factors and procedures allow for a worst case situation when the most demanding devices in the configuration all make their heaviest demands on Model 40 I/O capabilities at the same time. Such a situation may not occur frequently, but it is the situation that the evaluation procedures place under test. If a particular configuration fails to pass testing, one or more devices may be expected to incur overrun or loss of performance during the worst case situation.

Overrun

Overrun occurs when a channel does not accept or transfer data within required time limits during a read, read backward, or write operation. This data loss may occur when the total channel activity initiated by the program exceeds channel capabilities. Depending on the device, it may halt operation, or it may continue transferring data until the end of the block is reached.

An overrun causes a unit-check indication in the channel status word. An I/O interruption condition is generated at the conclusion of the operation. The cause for the unit check is indicated by turning on bit 5 of sense byte zero, the overrun bit, for subsequent sense and interrogation.

Loss of Performance

Overrun occurs only on unbuffered I/O devices. Buffered devices are not subject to overrun. Instead, when buffer service is not provided within required time limits, the device merely waits for channel service. While it is waiting, the device is said to incur a loss of performance.

Conventions for Satisfactory Channel Programs

Execution of a channel program causes a load on channel and system I/O facilities. Some I/O devices require execution of a chain of commands, preparatory to transfer of a data block. However, the impact of the load caused by a channel program is not a simple function of the number of commands used: the sequence in which particular types of commands appear in a channel program is also a factor.

A type of command particularly significant to sequencing considerations are control commands that are executed at electronic speeds, and which do not cause any mechanical motion. Such commands are executed as immediate operations and provide device end in the initial status byte. When command chaining is specified in such an immediate operation, channel facilities are not disengaged from the channel program until such a chain ends or a command causing mechanical motion or data transfer is executed. Therefore, when immediate operations with device end in the initial status byte are chained together, fetching and execution of the CCW's may cause a heavy load on channel facilities. Such a load may cause excessive delay in channel service to one or more devices in the I/O configuration with resultant overrun or loss of performance. For example, a chain of no-op commands can contribute heavily to a channel overload situation that would not otherwise have occurred. Such a programming convenience may cause a severe overrun situation for concurrently operating devices.

Another aspect of the way in which CCW sequencing considerations affect channel capabilities is their effect on a channel's data transfer capabilities. For example, if a command causing data transfer does not specify data chaining, a channel is able to transfer data at a faster rate, without overrun, than if data chaining is specified.

Data Chaining Considerations

A System/360 user is free to specify data chaining in channel programs whenever he chooses to do so. The

channel evaluation procedures and tables in this manual provide guidance in considering data chaining operations.

The factors in Table 1 allow for data chaining on the 2702 and as specified for other devices, with exclusion of allowance for data chaining on telegraph controls on a 2702. The other 2702 factors in Table 1 assume a count of 32 for data chaining. (Tables 1-5 are part of the Appendix, which has been placed at the end of this manual so that it can be removed for easy reference.)

To obtain maximum compatibility for data chaining channel programs, addressing resolution on double word boundaries and byte counts of 16 or greater are necessary. These parameters are assumed by the channel evaluation procedures in this manual. The procedures allow for computing proper priority load values for data chaining counts other than those specified in Table 1.

Relationship of Conventions and Evaluation Procedures

The evaluation procedures are premised on channel programs having command sequences that provide efficient operation of I/O devices and avoid unnecessary loads on channel facilities. Channel programming conventions have been established to guide I/O programmers in avoiding overrun situations.

Observance of channel programming conventions is fundamental to the selection of an I/O configuration that will permit concurrent operation of I/O devices in a satisfactory manner. The channel programming conventions described below are integral to the channel evaluation procedures. An evaluation yielding an indication of satisfactory channel performance is not dependable when channel programs written in violation of the conventions are used.

Scope of Conventions

1. The conventions relate to the sequence in which certain types of commands may be executed, and not to their sequence in main storage.

2. The conventions define four classes of commands and the sequence in which they may be used.

3. The command sequences provided by the conventions are different for different types of devices. Sequences are provided for these devices:

Direct access storage devices — 2302, 2311, 2321, 7320
Tape units — series 2400
Card units — 1442, 2501, 2520, 2540
Printers — 1403, 1443
Console — 1052
Communication adapters — 2701, 2702

Sequences for other devices will appear in a subsequent publication.

4. The conventions relate to all the commands in a chain, including the CCW addressed by the CAW and the terminating CCW that does not specify any chaining.

5. The conventions do not relate to commands addressed by the CAW which do not specify any chaining.

6. The conventions relate only to the avoidance of overrun; they do not define invalid command sequences that are rejected by a channel, such as TIC to TIC, or that are rejected by a control unit. CCW sequences causing command reject are specified in the I/O device manuals.

Note that item 4 is of particular interest to I/O programmers working on segments of a single channel program: the rules are not susceptible to abrogation when one segment is chained to another segment.

The channel programming conventions in this manual are recommended to System/360 users, particularly in a multi-programming environment where a programmer is not aware of the overall load on channel facilities. Where a programmer controls or has knowledge of all I/O activity, he may establish somewhat less restrictive channel programming conventions of his own which may be particularly suited to his application and configuration.

Also, channel programs used infrequently, such as error routines, may have small probability of contributing to channel overload. For such routines, deviation from the conventions may be considered, and not found inappropriate.

Classes of Commands

The conventions establish four classes of commands. Commands that always cause mechanical motion are in one class. The other three classes encompass commands that are always executed at electronic speeds, plus commands that are sometimes executed at electronic speeds. An example of the latter is rewind, which is executed at electronic speed when tape is already at load point. The three classes of commands having electronic-speed properties differ in the length of time required for their execution.

The conventions for the different devices specify classifications for the specific commands pertinent to each device.

The conventions define the four classifications by the sequence in which they may precede or follow other commands:

Class A Commands: These commands may be chained in any order, without restriction. Class A commands cause mechanical motion.

Class B Commands: Only one Class B command may be chained between two Class A commands:

→ A → B → A = permissible command chaining sequence
→ A → B → B = command chaining sequence excluded by conventions

A Class B command may be substituted for a Class C or Class D command.

Class C Commands: A Class C command may appear only once in a channel program, and then only as the first command in a channel program; a Class C command may appear only in the location specified by the CAW:

CAW → C → A → B. = permissible program
CAW → A → C → A. = program excluded by conventions

A Class B command may be substituted for a Class C command:

CAW → B → A → B → A → B. = permissible program

Class D Commands: A Class D command may appear only as the last command in a channel program; it may not specify any chaining:

CAW → X → X → D. = permissible program
CAW → X → D → A. = program excluded by conventions

A Class B command may be substituted for a Class D command.

Some devices have conventions that exclude specific sequences of commands not excluded by the classifications above.

Some of the devices have conventions that allow a specific command sequence to be substituted for a single command of a specified class.

Command Classifications for I/O Devices

The rules below define classifications for specific commands used with a particular device. The bit pattern for each command code byte is specified to provide positive identification of commands.

Commands not classified may not specify any chaining and may be placed only in the location specified by the CAW. Each such command thus constitutes an entire channel program in which it is the only command. The sense command is used in this manner for all devices.

Direct Access Storage Devices: These command classifications are valid for all devices attached to a 2841 control unit.

Class A commands (any order):

Read	XXXX XX10	
Write, Search, Erase	XXXX XX01	
Space Record	0000 1111	
Recalibrate	0001 0011	(Class A on 2311 only)
NoOp	0000 0011	(NoOp may be used only when preceded by a formatting write 0001 XX01 or 0000 0001)

Class B commands (not more than one between Class A commands):

TIC	XXXX	1000
SEEK	0000	0111
	000X	1011

These command chains have the properties of a single Class B command:

TIC → SEEK XXXX 1000 → 0000 0111 / 000X 1011

SEEK → TIC 0000 0111 / 000X 1011 → XXXX 1000

Class C commands (first CCW in program). These command chains have the properties of a single Class C command:

Seek → Set File Mask → TIC 0000 0111 / 000X 1011 → 0001 1111 → XXXX 1000

Class D commands (last CCW in program):

NoOp	0000	0011	(except when preceded by a formatting write)
Restore	0001	0111	(NoOp on other than 2311)

Excluded chains:

SEARCH → TIC → WRITE X011 0001 / X010 1001 → XXXX 1000 → 0000 X101

Data chaining may propagate through a TIC command for gap-only data-chaining, as described in the "Data Chaining in Gaps" section of this manual.

Series 2400 Tape Units

Class A commands (any order):

Read	XXXX	XX10
Write	XXXX	XX01
Read backward	XXXX	1100
Forward space	0011	X111
Backspace	0010	X111
Write tape mark	0001	1111
Erase gap	0001	0111

Class B commands (not more than one between Class A commands):

TIC	XXXX	1000

Class C commands (first CCW in program):

Set Mode	XXXX	X011

This command chain has the properties of a single Class C command:

Set Mode → TIC XXXX X011 → XXXX 1000

Class D commands (last CCW in program):

Rewind	0000	0111
Rewind and Unload	0000	1111
NoOp	0000	0011

Mixed Mode Seven-Track Tape Operations: A routine may be used to select a tape unit, set its density mode, and then TIC to a desired channel program:

SIO → Set Mode / TIC → Class C sequence

The conventions require the CCW addressed by the TIC to be Class A.

If the tape applications involve mixed mode seven-track operations, the programmer may make provision for placing the proper set mode command in the location addressed by the CAW before SIO is issued, or the programmer may begin each channel program addressed by the TIC with an appropriate set mode com-

mand. Such an additional set mode command violates the convention for Class C commands, and causes an additional load on channel facilities. Provision for the extra load is made in the multiplex mode evaluation procedure in this manual by use of a set mode load factor.

Card Units (1442, 2501, 2520, 2540)

Class A commands (any order):

READ	XXXX	XX10
WRITE	XXXX	XX01

Class B commands (not more than one between Class A commands):

TIC	XXXX	1000

Class C commands (first ccw in program):

CONTROL	XXXX	XX11

Class D commands (last ccw in program):

CONTROL	XXXX	XX11

Printers (1403, 1443)

Class A commands (any order):

WRITE	XXXX	XX01

Class B command (not more than one between Class A commands):

TIC	XXXX	1000

Class C commands (first ccw in program):

CONTROL	XXXX	XX11

Class D commands (last ccw in program):

CONTROL	0000	0011

Console (1052)

Class A commands (any order):

Read inquiry	0000	1010
Write auto carriage return	0000	1001
Write inhibit carriage return	0000	0001

Class B commands (not more than one between Class A commands):

TIC	XXXX	1000

Class C commands:

Not applicable

Class D commands (last ccw in program):

Control	XXXX	XX11

Communication Adapters (2701, 2702): Data chaining with or without TIC may be used for these adapters.

Class A commands (any order):

Write Dial Break Diagnostic write	XXXX	XX01
Read Prepare Inhibit Search Diagnostic read	XXXX	XX10

Class B commands:

Not applicable

Class C commands (first ccw in program):

Control*	XXXX	XX11

Class D commands (last ccw in program):

Control*	XXXX	XX11

*For a communication network of switch-type terminals, these two control commands are Class A:

Disable	0010	1111
Enable	0010	0111

Evaluating Heavily Loaded Channels

In evaluating an I/O configuration for successful operation under worst case conditions, consideration may be given to toleration of occasional overloading. A need to restart an operation due to an occasional I/O interruption may not be unduly objectionable and/or reduction in performance of some I/O devices may be insignificant in many applications.

Concurrent operation of multiplex mode devices important to an application may be assured by giving them higher priority than devices having less importance, or, higher priority may reduce the frequency of overrun or loss of performance incurred by a device.

When evaluating the performance of a system susceptible to channel overload conditions, consideration should be given to the relative ease of restarting an interrupted I/O operation. For example, an overrun on a communication line coupling two CPU's is handled more readily than a read overrun on a card read punch. Preferential priority may be given to devices that require manual intervention in response to an overrun condition.

Some circumstances may make it desirable to place devices with heavy load factors on the same selector channel, rather than on separate selector channels, in order to preclude interference with each other.

Evaluations should not ignore the characteristics of IBM Programming Systems packages:

1. Operating System/360
2. Tape Operating System
3. Disk Operating System
4. Basic Operating System
5. Basic Programming Support

These programs will attempt to execute any start I/O instruction for which the channel and device are available. The programs that permit concurrent operation of more than one device on a multiplexer channel will not, however, initiate a burst mode operation on the multiplexer channel while any device subject to overrun is in operation on the multiplexer channel.

Selector Channel Loading

The impact on a selector channel of a load caused by operation of an unbuffered I/O device depends on the device's data transfer rate and on:

Whether the device data chains

Whether the device data chains and also uses TIC's

Whether the other selector channel data chains

The data chaining and TIC considerations give rise to several selector channel program relationships. Provision has been made for the various situations by specifying five different load factors for each unbuffered selector channel device. The first two load factors relate to channel capabilities and the other three load factors relate to the input/output capabilities of the system:

Data Load on Channel (data load factor).
Data Chaining Load on Channel (DC load factor).
System Load Case 1
Device under test data chains; the other device does not data chain (C-1 factor).
System Load Case 2
Device data chains; other device data chains with or without transfer in channel (TIC) operations (C-2 factor).
System Load Case 3
Device data chains and use TIC's; other device may be performing any type of channel operation (C-3 factor).

Each device's five factors appear in Table 1. They are arranged and identified in this left-to-right sequence of column headings:

CHANNEL LOAD		SYSTEM LOAD		
		C-1	C-2	C-3
Data Load	DC Load	DC NO DC	DC DC	DC & T ANY

The values in the table for the two channel load factors and the three system load factors assume a minimum byte count of seven, with no restriction on the byte addresses of the first and last bytes in a block.

One or more of the five load factors are used in test procedures that ascertain whether a particular selector channel configuration will run satisfactorily or not. The test procedures consider operation of one selector channel only, or concurrent operation of both selector channels.

When both channels are desired to run concurrently, each device is tested against overloading its channel. Maximum selector channel load handling capabilities are specified in Table 5 for use in the test procedures. For satisfactory operation, the applicable channel load limit factor from Table 5 must not be exceeded by the load computed for a device being considered in a test procedure. If exceeded, overrun is indicated.

In addition, if either or both of the pair of devices on selector channels desired to run concurrently use data chaining, the pair is tested against overloading the input/output facilities of the system. For the latter test, a system load sum is computed. If it is not greater than the system load limit factor of 100, satisfactory operation is indicated. Otherwise, overrun is indicated.

Note that a system load sum vs system load limit test is performed whenever data chaining is used on one or both channels; data chaining on one channel has an effect on the other channel.

An exception to the preceding paragraph exists: when the exception consideration described below is applicable to both of a pair of devices operating concurrently, their evaluation need not include the system load sum vs system load limit test.

Overrun Test Exception

Under certain circumstances, the load on channel facilities caused by data chaining may be ignored in testing for channel overload. It then is not a consideration in selecting a load factor or a selector channel load limit. The exception is valid only for direct access storage devices that are programmed in a certain way.

A channel program for direct access storage devices, such as IBM 2311 Disk Storage, must specify command chaining and it may, of course, specify data chaining operations. The time it takes a gap on a track to pass a read-write head on one of these devices is sufficient for the channel to perform a data chaining operation. Gap time occurs in such operations as "write count key and data": gap time occurs between writing the count and the key, and between writing the key and the data.

If the program causes data chaining to occur only during gap time, the data chaining load on channel facilities will not be additive to the device's data transfer load. Therefore, data chaining that occurs only during the gap time may be ignored in testing the channel against overrun. This gap-only data chaining cannot be ignored, however, in testing the other channel for overload, if the other channel is using data chaining other than in gaps.

When both devices are direct access storage devices, and data chaining occurs for each device only during gap time, no system load sum vs system load limit test need be made. It is necessary only to test each direct access storage device's data load against overloading its own channel, without regard to the effect on each other.

The overrun test exception for direct access storage devices has four rules which are:

1. That gap-only data chaining may be ignored in testing the channel against overload.
2. That gap-only data chaining on one channel may not be ignored when testing the other channel against overload, if the other channel is data chaining.
3. That if gap-only data chaining occurs on both channels, neither data chaining need be considered.
4. That whenever data chaining is ignored, only the device's data load and the selector channel no DC load limit is used in testing the channel receiving the benefit of the exception consideration.

Use of the overrun test exception is demonstrated in some of the test procedure examples given in this manual.

Overrun Test Procedures

Two selector channel test procedures for unbuffered devices are given: one for operation of one channel and one for operation of two channels. They are similar; for the sake of clarity, each is presented separately, with examples.

Each procedure has been broken into numbered steps that facilitate discussion and illustration of examples. Once understood, the procedures may be used rapidly, without specific attention to every numbered step.

One Channel Overrun Tests

The test procedure for operation of only one selector channel is performed for each device on the channel that can be overrun.

The test procedure considers three situations:

Situation 1 No data chaining: The device's data load factor value from Table 1 is compared with the channel load limit of 60 from Table 5.

Situation 2 Data chaining: The device's DC load factor value from Table 1 is compared with the channel load limit of 50 from Table 5.

Situation 3 Data chaining and TIC: The device's DC load factor value from Table 1 is compared with the channel load limit of 40 from Table 5.

For satisfactory operation of the device, the load value used in the comparison must not be greater than the selector channel load limit specified. A failure to pass the test indicates overrun for the device during worst case conditions.

In the following examples only one channel is in operation on a Model 40. Two types of devices are attached:

IBM 2401 Model 3 Tape Unit
IBM 2311 Disk Storage

Channel programming considerations are as specified in the examples.

Situation 1 Example

Model 40 – one selector channel only.
Device – IBM 2401 Model 3, 90 kb, no chaining.
Device load factor from Table 1 = 15.3.
Selector channel no DC load limit = 60.

The device load is not greater than the pertinent limit; satisfactory operation is indicated.

Situation 2 Example

Model 40 – one selector channel only.
Device – IBM 2401 Model 3, 62.5 kb, data chaining.
DC load factor from Table 1 = 11.5.
Selector channel DC load limit = 50.

The device load is not greater than the limit; satisfactory operation is indicated.

Situation 3 Example

Model 40 – one selector channel only.
Device – IBM 2311 Disk Storage, 156 kb, data chaining and TIC.
DC load factor from Table 1 = 30.4.
Selector channel DC and TIC load limit = 40.

The device load is not greater than the limit; satisfactory operation is indicated.

Exception Example

Model 40 – one selector channel only.
Device – IBM 2311 Disk Storage, 156 kb, data chaining and TIC.

Channel program data chains only during gap times.

This configuration is the same as used in the Situation 3 example, but, because the direct access 2311 data chains only during gaps, the data chaining is ignored:

Data load from Table 1 = 20.3.
Selector channel no DC load limit = 60.

These factors are the same type used in a Situation 1 test. The operation performed is the same as in the Situation 3 example, but, because data chaining is ignored, a smaller load value is compared with a larger load value.

Two Channel Overrun Tests

The test procedure for operation of two selector channels is presented here in six numbered steps that aid comment upon examples; in practice, attention need not be focused on every numbered step.

The overrun test exception for direct access devices, previously discussed, is valid.

The step 3 comparison of channel load to channel load limit is performed for each device in each pair of devices desired to run concurrently.

The step 6 comparison of system load sum to system load limit is performed for each pair of devices desired to run concurrently whenever either or both devices data chain (subject to overrun test exception).

Steps in Test Procedure

Step 1. Assign device identity to each channel for devices to be tested.

Step 2. Reference each device's data load factor from Table 1.

Step 3. For each device that data chains, reference its data chaining load factor (DC load) from Table 1.

Step 4. Reference each channel's channel load limit data chaining factor from Table 5. If a device does not data chain, compare its data load with its channel load limit. If a device data chains, compare its DC load with its channel load limit. For optimum operation, the factor selected may not exceed its channel load limit. Otherwise, overrun is indicated for one or more devices in the I/O configuration, multiplexor channel device(s) in operation not excepted.

If neither device data chains, the test has been completed. If either device data chains, the following steps are performed:

Step 5. Reference each data chaining device's system load Case 1, 2, or 3 (C1, C2, or C3), as applicable, from Table 1.

Step 6. To each factor found in step 5, add the data load factor from the other channel. The sum is the system load sum.

Step 7. Compare each system load sum found in step 7 with the system load limit of 100.

For optimum operation, no system load sum may exceed 100. Otherwise, overrun is indicated for one or more devices in the I/O configuration, multiplexor channel device(s) in operation not excepted.

Example Configuration

In the following examples, IBM 2401, Model 3 Tape Units and IBM 2311 Disk Storage units are attached to each selector channel.

All channel programs for the 2311 direct access storage device data chain only in gaps; the overrun test exception will apply in the 2311 examples. Data chaining and transfer in channel considerations for the 2401-3 tape unit are as specified in the examples (DC indicates data chaining; no DC indicates its absence).

Case 1 Example:

	CHANNEL 1	CHANNEL 2	
Device	2401-3, 90 kb, DC	2401-3, 90 kb, no DC	Step 1
Data load*	15.3	15.3	Step 2
DC load*	17.2	.....	Step 3
Channel load limit**	32.	40	Step 4 compare
System load case 1(C1)*	40.7	.....	Step 5
System load sum***	56.0 (15.3+40.7)	.....	Step 6
System load limit****	100.0	.....	Step 7 compare

* From Table 1
** From Table 5
*** Tested channel system load plus opposite channel data load
**** Fixed value = 100

The tests indicate satisfactory operation. In the absence of data chaining on channel 2, a system load sum is not computed for it.

If the devices exchange priority, their channel load limits are also exchanged but are still ample. The system load sum for the data chaining 2401-3 remains the same; brief study of the tests already performed shows satisfactory operation for either priority arrangement.

Case 2 Example:

	CHANNEL 1	CHANNEL 2	
Device	2401-3,90kb, DC	2401-3,90kb, DC	Step 1
Data load	15.3	15.3	Step 2
DC load	17.2	17.2	Step 3
Channel load limit	32.	32.	Step 4 compare
System load Case 2	62.2	62.2	Step 5
System load sum	77.5	77.5	Step 6
System load limit	100.	100.	Step 7 compare

Neither load sum exceeds the system load limit; satisfactory operation is indicated.

Case 3 Example:

	CHANNEL 1	CHANNEL 2	
Device	2401-3,90kb, DC & TIC	2401-3,90kb, DC & TIC	Step 1
Data load	15.3	15.3	Step 2
DC load	17.2	17.2	Step 3
Channel load limit	21.6	21.6	Step 4 compare
System load Case 3	79.3	79.3	Step 5
System load sum	94.6	94.6	Step 6 (Compare Steps 2&3)
System load limit	100	100	Step 7 compare

Neither load sum exceeds the system load limit; satisfactory operation is indicated.

Exception Example, Both Channels:

	CHANNEL 1	CHANNEL 2	
Device	2311, DC & TIC	2311, DC & TIC	Step 1
Data load	20.3	20.3	Step 2
Channel load limit	50	40	Step 4 compare

Data chaining occurs only during gap time (exception consideration). Therefore, the DC load and system load Case 3 factors are not used; no system load sum need be computed.

Exception Example, One Channel:

	CHANNEL 1	CHANNEL 2	
Device	2311, DC	2401-3, 90 kb DC	Step 1
Data load	20.3	15.3	Step 2
DC load	.....	17.2	Step 3
Channel load limit	50.	+ 32.	Step 4 compare
System load Case 2	.....	62.2	Step 5
System load sum	.....	82.5	Step 6
System load limit	.....	100.	Step 7 compare

Again, step 1 suffices for the direct access storage device; a system load sum is computed only for the tape unit.

If the 2311 and 2401-3 exchange channel priority, their channel load limits are also exchanged, but are still ample. The system load sum for the 2401-3 remains the same; brief study of the tests already performed shows satisfactory operation for either priority arrangement.

Multiplexer Channel Loading

The multiplexer channel on the Model 40 can handle a burst mode I/O device with a Table 1 data load factor not greater than 25. If multiplex mode devices are in operation when a burst mode operation is initiated on the multiplexer channel, they will overrun or lose performance when their ability to wait for channel service is exceeded. Selector channel devices in operation are not affected, but the CPU is unavailable for halt I/O, start I/O, or any instruction until burst mode operation of the multiplexer channel terminates. See Table 6 for limitations on simultaneous burst mode operations.

Multiplex Mode Considerations

Concurrent operation of I/O devices on a multiplexer channel involves many variables:

1. Devices vary in their data transfer rates.
2. Devices have buffers varying in capacity from 1 byte to 132 bytes.
3. Devices vary in the number and type of CCW's needed for their operation.
4. Combinations of devices on the selector channels vary in the interference they cause.
5. The large number of I/O devices available for use on a multiplexer channel may be combined in many different configurations.
6. Devices in a particular configuration may be physically connected in many different priority sequences.

The problem of determining whether a particular multiplexer channel configuration will run concurrently in a satisfactory manner has been reduced to arithmetic procedures using a worksheet form and factors provided in the tables in this manual. The evaluation procedures minimize the need for judgement on the part of the user by providing a clear-cut decision path specified in step-by-step procedures.

Device Load

A numeric factor has been computed for each multiplex mode device to specify its combined data transfer and channel program load on multiplexer channel facilities. It is called a device load. The factors are listed in Table 1 of this manual under the columns headed Device Load.

The term, device load, refers specifically to the Table 1 values mentioned. Each device in Table 1 has other types of load factors listed for use in considering the impact of higher priority devices on lower priority devices.

Device Waiting Time

After a multiplex mode device requests channel service, it has a fixed length of time that it can wait for service. If the channel provides service within this length of time, the device operates satisfactorily. If, however, the channel does not service the device within the device's waiting time, the device must continue waiting (device not susceptible to overrun) or lose data and subsequently cause an I/O interruption condition (device susceptible to overrun). For example, when an IBM 1403 Printer on an overloaded multiplexer channel fails to receive data within its particular waiting time, it merely waits until service is provided by the multiplexer channel. The delay does not cause an interruption condition; nor is a new start I/O instruction required to select the 1403. The only effect is a lessening of performance. If an IBM 1442 Card Read Punch read operation does not receive data service within its waiting time, however, overrun occurs.

Multiplex mode device wait time factors, expressed in milliseconds, are listed in Table 1.

Device Priority on Multiplexer Channel

Priority of devices on a multiplexer channel is determined at the time of installation by the sequence in which they are connected to the channel. The cabling facilities provide considerable flexibility in physical location and logical position of I/O devices.

Devices may have the priority sequence in which they are attached to the cable (select-out line priority) or the device most remote from the channel may be connected to have highest priority, and the device nearest the channel connected to have lowest priority (select-in line priority).

Each device on the multiplexer channel cable may be connected for selection either to the select-out line, or to the select-in line. Thus, one or the other of the lines is specified in establishing priority for a desired physical layout of devices.

Priority assignments and machine room layout should be established during the physical planning phase of an installation so that cables for the I/O devices may be properly specified.

A major consideration in assigning priority to multiplex mode devices is their susceptibility to overrun. Devices are identified in this manual as being in one of three categories:

1. Devices subject to overrun, such as magnetic tape units.

2. Devices that require channel service to be in synchronization with their mechanical operations. For example, the IBM 2540 Card Read Punch has a fixed mechanical cycle. Delay in channel service for such devices usually occasions additional delay due to synchronization lag.

3. Devices that do not require synchronized channel service. An IBM 2550 Display is such a device; it is entirely electronic in nature. An IBM 1443 Printer is another device that does not require synchronized channel service; it can begin printing as soon as its buffer is full and line spacing is completed. Any loss of performance by category 3 devices is limited to that caused by channel delay in providing service.

Devices in the first category have need for highest priority. The devices in the last two categories may incur lost performance on an overloaded channel, but are not subject to overrun; their control units have data buffers or an ability to wait for channel service. Devices in the second category, however, require higher priority than those in the third category.

Within each category, devices are assigned decreasing priority in the order of their increasing wait time factors; smaller wait time factors require higher priority. The factors are listed in Table 1.

When devices that operate only in burst mode, such as magnetic tape or disk storage devices, are attached to the multiplexer channel, they should have lower priority than multiplex mode devices. Low priority devices take longer to respond to selection than do higher priority devices; a burst mode device need be selected only once for an operation, but a multiplex mode device must be selected for transfer of each byte or few bytes of data.

The control unit determines whether a device operates on the multiplexer channel in burst mode or in multiplex mode.

Some devices, such as the IBM 2520 Card Punch, the IBM 2701 Data Adapter Unit, and the IBM 2821 Control Unit, may operate on a multiplexer channel in either burst mode or in multiplex mode, as determined by the setting of a manual switch on the control unit's customer engineer panel. Such devices are assigned priority on the multiplexer channel as specified above.

A multiplexer channel can transfer data most rapidly in burst mode. Where an application uses only category 2 or 3 devices that have the mode choice, improved multiplexer channel efficiency may be obtained by operating the devices in burst mode.

Table 1 specifies whether a device operates in burst mode, in multiplex mode, or in either mode.

Interference from Priority Devices

The multiplexer channel sustains concurrent operations in multiplex mode by servicing one device at a time. The operating devices compete for service, and the multiplexer channel services them in the order of their priority.

Devices on the selector channels or higher priority devices on the multiplexer channel may force a lower priority multiplex mode device to wait for channel service. The former is called a priority device and the latter is called a waiting device.

When a higher priority device forces a lower priority device to wait for channel service, the priority device is said to interfere with the lower priority device. The device generating interference may be on a selector channel or on the multiplexer channel.

When more than one priority device forces a multiplex mode device to wait, each of the priority devices generates interference. All such interference must be considered in determining whether the waiting device will receive channel service before its waiting time is exceeded.

The test precedures for concurrent operation of multiplex mode devices assume that a waiting device has made its request for channel service at the worst possible time: when the priority devices will cause maximum interference during the waiting device's waiting time.

The channel ordinarily works its way through the interference, and the waiting device is unaffected by the wait. If, however, heavy interference forces the waiting device to wait past its particular waiting time, it will be subject to overrun, or it will continue waiting for service.

Priority Loads

To evaluate the effect of priority device interference on a waiting device, a numerical priority load is computed. The significance of wait time as a factor in computing an accurate priority load is pointed up by these facts:

1. Each multiplex mode device has a particular wait time that is critical to its continuous operation.

2. A device's wait time is pertinent to its priority assignment.

3. A device's wait time is related to the degree to which it is impacted by interference from a priority device.

4. This impact, called a priority load, is expressed numerically as a function of a device's wait time.

Three factors are considered in determining a priority load:

1. The control load cause by execution of CCW's, including chaining and transfer in channel operations.

2. The priority device's data transfer load.
3. The waiting time of the device being evaluated.

Note that since a priority load is a function of waiting time, a fixed priority load cannot be established for a priority device; the priority load caused by a priority device must be computed as a function of a particular waiting device's waiting time.

Ranges of Wait Times

The relationship between a priority device's load on channel facilities and various waiting times is shown in Figure 5. The abscissa relates to device waiting times. The short waiting time shown results in a heavy priority load; the longer waiting time falls in a part of the curve showing much less priority load. The overall impact of a priority device on a waiting device is more intense for a waiting device with a short waiting time than it is to a device with a long waiting time. The latter device can wait for diminishment in the priority load on channel facilities and still obtain service within its waiting time.

Two factors, called A and B, are provided in this manual to relate each device's priority load curve to different wait times. The priority load curve was considered in segments related to different wait times and two factors were computed for each curve segment. These A and B factors are used to compute the device's priority load in relationship to any waiting device having a wait time falling within range of wait times established for the curve segment. They are used in a function which defines hyperbolic curves of average load vs time, based on device/channel time relationships and channel programming considerations.

Multiple A and B Factors: Table 1 lists A and B factors for each Model 40 input/output device. Where Table 1 shows a hyphen for an A or a B factor a zero value is indicated.

Some devices have only one set of A and B factors. Other devices have more than one set. Only one set is used in computing a priority load for the device. Each set has an associated priority time factor that is used to select the set of A and B factors appropriate to a particular waiting device.

Priority Time Factors: The priority time factors in Table 1 are used in the evaluation procedure only to identify A and B factors for subsequent use.

As each waiting device is evaluated on a multiplex mode worksheet, its wait time is used to select a set of A and B factors for each priority device.

Each set of A and B factors in Table 1 has a priority time factor next to it that specifies the beginning of a range of wait times significant to that set of A and B factors. The range extends from the priority time factor specified for the set to the device's next larger priority time factor.

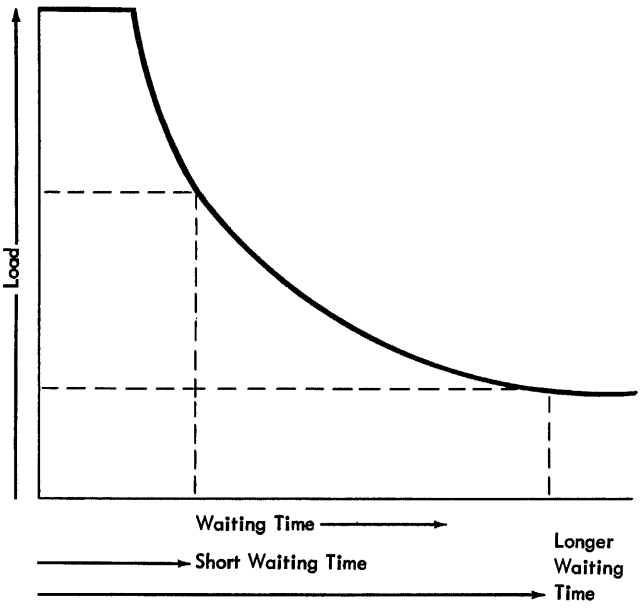


Figure 5. Priority Load Curve

These ranges of Wait Times . . . . . are defined by these priority time factors

	Priority Load		
	Time	A	B
.200 to 4.77	.200	-	100
4.77 to 100	4.77	477.	-
100 up	100	454.	4.77

A wait time factor of 6.5 falls in this range . . .

. . . and this set of A and B factors are significant to a waiting device with a wait time factor of 6.5

Rule: The largest priority time factor that is less than a waiting device's wait time factor identifies the priority device's set of A and B factors to be used in computing priority load.

Figure 6. Use of Priority Time Factors

For example, a device may have three sets of A and B values with three priority time factors specifying three ranges of wait times. Figure 6 shows priority factors and A and B factors for such a device, as they appear in Table 1 for a 1443 N1 Printer with 13-character set.

Priority Load Formula

The A and B and wait time factors in Table 1 have been computed for use in a formula that yields the priority load which occurs when a particular priority device interferes with a particular waiting device.

The sum of the B factor and the quotient obtained by dividing the A factor by the wait time factor is the priority load. The arithmetic looks like this:

A/wait time + B = priority load

The tables in this manual provide the A, B and wait time factors for use in the formula.

Table 1 provides priority load factors for data chaining byte counts of 20 and 100; the factors may be interpolated or extrapolated for other counts by using a linear function of 1/count.

The procedure for arbitrary counts is:

1. Use wait time to select A and B factors for a count of 20, compute the priority load, and call it L_{20}:

$$\frac{A_{20}}{\text{wait time}} + B_{20} = L_{20}$$

2. Repeat step 1 for a count of 100, and call the result L_{100}:

$$\frac{A_{100}}{\text{wait time}} + B_{100} = L_{100}$$

3. Compute the priority load for the desired count:

$$L_{100} + \left(\frac{25}{\text{count}} - .25\right)\left(L_{20} - L_{100}\right) = \text{Priority load for count}$$

Set Mode Load

As described in the section "Conventions for Satisfactory Channel Programs," additional priority load occurs when a set mode command is used in violation of the convention for Class C commands. Such use of a set mode command in a location other than that addressed by the CAW may be considered desirable in mixed mode seven-track tape operations. If so, the additional priority load is allowed for in the evaluation procedure by adding the set mode load factor of 2.5 to the A factor selected for the tape unit. This factor of 2.5 is an approximation that lends itself to convenient use.

Previous Load

A waiting multiplex mode device may be forced to wait for channel facilities, not only by devices with higher priority, but also by a device with lower priority that is in operation when the waiting device requests channel facilities. This is called a previous load and must be added to the priority load caused by priority devices. The device with lowest priority on the channel has no previous load; a zero value is used in the addition. Previous load factors are provided in Table 1.

Load Sum

Several load factors relating to multiplex mode operations have been described:

Priority load
Device load
Set mode load
Previous load

These loads are developed for each waiting device and are added together to form a load sum for each waiting device. The load sum for a waiting device represents the total load on system channel facilities under a worst case condition when:

1. All priority devices are causing maximum priority loads.
2. Any lower priority device, already in operation, is making maximum demands on channel facilities (previous load).
3. The waiting device places its maximum device load on channel facilities.

A step-by-step procedure for computing load sums is given in the section "Multiplex Mode Evaluation Procedure."

Multiplex Mode Channel Load Limit

A numeric factor of 100 has been established as the multiplex mode channel load limit. If a load sum exceeds 100, loss of performance or overrun is indicated during worst case situations. The amount of such loss of performance may be computed; it is usually small and infrequent.

Lost Performance Time

A loss of performance indicated by a load sum greater than 100 is caused by the waiting device having been forced to wait past its wait time. The total length of time the device waits for channel service during a worst case situation is computed as:

$$\frac{\text{load sum} \times \text{wait time}}{\text{multiplex mode channel load limit of 100}} = \text{total delay in channel service in ms}$$

Wait time is subtracted from the quotient to find the amount of time lost:

total delay in ms − wait time = lost performance time in ms

By relating the amount of time lost to the device's normal operating cycle time, the effect on performance may be seen:

$$\frac{\text{lost time}}{\text{cycle time}} \times 100 = \text{percentage loss of performance}$$

For a hypothetical device having:

Wait time = 20
Load sum = 120
Cycle time = 200 ms

The arithmetic is:

$$\frac{120 \text{ load sum} \times 20 \text{ wait time}}{100 \text{ (limit)}} = 24 \text{ ms total delay}$$

and,

24 ms total delay − 20 ms wait time = 4 ms lost performance time

and

$$\frac{4 \text{ lost time}}{200 \text{ cycle time}} \times 100 = 2 \text{ percent loss of performance (occurs only during worst case situations)}$$

Reduced I/O device performance during worst case situations may be inconsequential to many applications. Even where reduced I/O performance may cause some programs to have longer run times, the situation may be not only tolerable, but also practical and economical.

Multiplex Mode Evaluation Procedure

This section specifies the multiplex mode evaluation procedure. The next section provides examples of its use. The subsequent section provides additional information. An understanding of the three sections will suffice for evaluation of most Model 40 input/output configurations.

For evaluation of a configuration having 2702 equipment, only as much as necessary of the subsequent 2702 sections need be read. All of the sections relate to this section: it must be understood first.

The step-by-step procedure given below is used with a *System/360 Multiplexer Channel Worksheet*, Form X24-3407, shown in Figure 8. (Figures 8-11 are part of the Appendix, which has been placed at the end of this manual so that it can be removed for easy reference.)

Each step in the procedure is numbered. Most of the steps call for an entry to be made on a Multiplexer Channel Worksheet. Figure 9 shows where such steps cause entries to be made. Each number in the worksheet spaces in Figure 9 refers to the numbered step in the procedure below that causes an entry to be made in the space. For example, the top of Figure 9 has a 1 in each of the two spaces that receive the entries called for by step 1.

As an additional aid in seeing where entries are made on a worksheet, Figure 10 shows factor values referenced from Table 1 for evaluation of a configuration specified in the next section of the manual, which discusses the Figure 10 worksheet example.

The procedure below assumes prior definition and satisfactory evaluation of the selector channel configuration.

1. Enter system identification and date.

2. Enter identification of the device in each selector channel group of devices that has the heaviest Table 1 data load or DC load, as previously determined in the selector channel evaluation procedure. These are the selector channel priority devices that may impact waiting devices. (Where one or more devices in a selector channel group have similar loads, but different priority loads, it may be necessary to repeat the multiplexer channel evaluation procedure with these other devices entered as priority devices.)

3. Enter the time A B sets from Table 1 for the devices entered in step 2.

4. Arrange the multiplex mode devices proposed for simultaneous operation into the three priority categories, 1, 2, and 3 as specified for the devices in the column in Table 1 headed Key.

5. Assign decreasing priority to devices within each category in the order of their increasing wait time factors, which also appear in Table 1. The device with the smallest wait time receives highest priority.

6. Enter the devices in the priority sequence established in steps 4 and 5.

7. Enter the wait time, time, A, B, previous load, and device load factors from Table 1 for the first device entered in step 6.

8. Repeat step 7 for each remaining device entered in step 6, except that the lowest priority device has no previous load factor.

9. Compare the wait time factor of the waiting device being evaluated to the time factor(s) of the first selector channel priority device; the largest time factor that is less than the wait time factor identifies the priority device's A and B factors to be entered. (See Figure 6 for guidance.) Where a priority device has only one set of A and B factors, it is entered.

10. Repeat step 9 for the other selector channel priority device entered in step 2.

11. (This step is performed when evaluating devices with second or lower priority.) Repeat step 9 for multiplexer channel priority devices instead of selector channel priority devices.

12. If step 11 has been performed, repeat it for each remaining multiplex mode waiting device. (This step 12 is effective when evaluating waiting devices with third or lower priority.)

13. Add the selected A factors and enter the A sum. When a set mode load factor is necessary, increment the A sum by 2.5.

14. Divide the A sum by the wait time factor for the waiting device and enter the quotient.

15. Add the B values entered in step 9, the quotient entered in step 14, and the device load and previous load entered in step 7, and enter the load sum.

16. The load sum must be less than or equal to 100 for satisfactory operation of the waiting device. If a 2702 Transmission Control has a load sum greater than 100, further evaluation is required; consult the "Load Sums for 2702" section of this manual.

17. Evaluate the waiting device with second priority by performing for it steps 9-16 (step 12 is not performed).

18. Perform steps 9-16 for all remaining waiting devices.

Worksheet Example

The following I/O configuration is evaluated for use on a Model 40 (Figure 10):

Selector Channel 1	2311 Disk Storage, data chaining only in record gaps
Selector Channel 2	2400 Tape, 60 kb, no data chaining
Multiplexer Channel	1442-N1 Card Read Punch, card image
	1442-N2 Punch, card image
	1443 Printer, 39-character set
	1052 Keyboard-Printer

The section "Exception Example, One Channel" showed satisfactory operation for a similar selector channel configuration having a greater load (the selector channel 2 tape operation was at 90 kb and used data chaining). Therefore, satisfactory operation is indicated for the selector channel devices in this example.

Selection of the priority load factors for the selector channel devices in the multiplex mode evaluation assumes tape writing and gap-only data chaining on the 2311.

The 1442-N1 is evaluated for reading, which causes a greater channel load than punching. Card image operations are assumed for both 1442's.

The 1052 has been assigned lowest priority on an arbitrary basis.

The multiplexer channel configuration is evaluated for multiplex mode operations (Figure 10), as specified in the preceding section of this manual. The procedure has four parts:

1. Assign priority to devices
2. Reference factor values from Table 1
3. Enter the values found on the Multiplex Mode Worksheet
4. Compute load sums

The completed worksheet (Figure 10) shows satisfactory operation for all multiplex mode devices: no load sum exceeds 100.

Worksheet Entries for 2821

Each device attached to an IBM 2821 Control Unit is evaluated as if it were a separate control unit. Each device has its own channel service requirements and is evaluated in a separate column on the Multiplexer Channel Worksheet. This may cause the worksheet evaluation procedure for some configurations to spill over onto blank paper.

The priority sequence for 2821 devices is:

1. IBM 1402 Card Read
2. IBM 1402 Card Punch
3. Printer(s)
   Printer Control No. 1
   Printer Control No. 2
   Printer Control No. 3

IBM 2702 Considerations

The IBM 2702 Communication Control may connect a variety of communication terminals to a multiplexer channel; 1-15 or 1-31 terminal lines may be connected.

The 2702 uses delay lines for storage of data and control information. The information circulates in the delay lines and may be accessed for transfer to or from the multiplexer channel or to or from a terminal.

When priority devices force a 2702 to wait for channel service, additional delay may occur in the 2702 due to any time required for synchronization with the delay line. Such additional delay exists only for the 2702 and does not affect other devices on the multiplexer channel.

A bit of information takes a certain length of time to go once around a delay line. A 2702 with capacity for 15 terminal lines takes 0.480 milliseconds per revolution, and a 31-line 2702 has a delay line revolution time of 0.992 milliseconds. The longer delay line can hold more information. The number of communication lines attached to a 2702 has a direct bearing on how long they can wait for channel service. Maximum waiting time exists when only one communication line is used. Each additional line in operation reduces the length of time a 2702 can wait for channel service.

In addition, the data transfer speed of a terminal affects 2702 waiting time; a high speed line cannot wait as long for channel service as can a lower speed line. Therefore, different wait time factors are specified in Table 1 for the different types of terminal controls and numbers of lines available. Table 1 also provides different wait time and device load, previous load, CPU interference, and priority load factors for each type of terminal control. The values in Table 1 are for all lines operating at the same speed.

Worksheet Example With Two 2702's and a 2821

The following Model 40 I/O configuration is evaluated in this example:

Selector Channel 1:	2311 Disk Storage, all data chaining in gaps
Selector Channel 2:	90 kb Magnetic Tape, data chaining 100 bytes
Multiplexer Channel:	2702 – 15 1030's @ 600 bps
	2702 – 31 1050's @ 14.8 bps
	2821 – 2540 Reading EBCD
	2540 Punching EBCD
	1403-N1 Printing 1100 LPM
	1403-N1 Printing 1100 LPM
	1443-N1 – Printing 240 LPM – 52 character set
	1052 – Console Typewriter

The selector channel evaluation example already given in this manual indicated satisfactory operation of the selector channel configuration. The multiplexer channel configuration is evaluated for multiplex mode operations by:

1. Assigning priority to devices.
2. Referencing factor values from Table 1.
3. Entering the values found on the Multiplexer Channel Worksheet.
4. Computing load sums.

The completed worksheet is shown in Figure 10. The 1052 has been assigned lowest priority on an arbitrary basis.

The load sum for the IBM 1443 Printer is 116.3; loss of performance is indicated for the 1443 during worst case priority loads.

The maximum length of time that channel service to the 1443 Printer would be delayed may be computed:

$$\frac{\text{waiting device load sum} \times \text{waiting device wait time}}{100} = \text{maximum delay in ms}$$

Values for the 1443 are:

$$\frac{116.3 \times 18.5}{100} = 21.6 \text{ ms}$$

The 1443 can wait 18.5 ms for its buffer to be serviced; in this worst case situation, it must wait an additional 3.1 ms (21.6 − 18.5 = 3.1). The 1443 ordinarily prints a line in 250 ms. An increase to 253.1 ms during a period of maximum priority loads is little more than 1 percent.

When a 2702 has a load sum in excess of 100, the "Load Sums for 2702" section of this manual is pertinent.

When a 2702 contributes priority load to any device having a load sum in excess of 100, the "Priority Load Factors for 2702" section of this manual is pertinent.

Load Sums for 2702: Because of the variables involved, the wait time, device load, and previous load factor values specified in Table 1 have been computed with a conservative bias for use with a Multiplexer Channel Worksheet. In most instances, their use in computing 2702 load sums will give an indication of satisfactory operation. Whenever a 2702 load sum exceeds 100, additional examination of the situation is in order.

To this end, a special analysis procedure, unique to the 2702 is provided in the next section of this manual. The procedure uses a special 2702 worksheet for analysis of the situation, with resolution to a single delay line cycle.

When the special analysis indicates satisfactory operation of the 2702, attention may be returned to the Multiplexer Channel Worksheet for evaluation of the next waiting device. If, however, the special analysis load sum still indicates an overrun, some of the communication lines may have to be connected to another 2702 in order to eliminate overrun.

In a system with a large number of terminal lines, construction of a probabilistic model may lead to the conclusion that the frequency of overrun will not be great enough to be objectionable for a particular application.

Special Analysis of 2702 Performance

Whenever the Multiplexer Channel Evaluation Worksheet procedure finds a load sum greater than 100 for an IBM 2702 Communication Control, the more sophisticated performance analysis given here may indicate satisfactory operation. A special worksheet and special tables, unique to the 2702, are used.

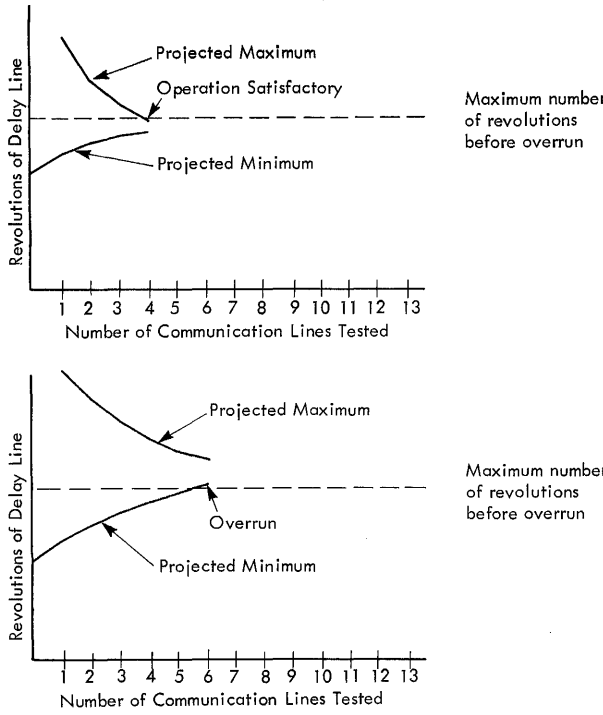
The special analysis assumes that all attached communication lines will request service during a single delay line revolution and that a scanning sequence will occur that gives service last of all to the highest speed communication line. The analysis reveals whether, considering priority loads, the number of delay line revolutions available is sufficient for the total delay line revolution requirements of all communication lines.

It is seldom necessary to test every communication line's requirements for delay line revolutions. After a communication line tests satisfactorily, a projection is made of both the minimum and the maximum number of revolutions needed to service the remaining communication lines. When a projected maximum is less than the maximum revolutions needed for the highest speed remaining line, satisfactory operation is indicated and no further analysis is required. Similarly, if a projected minimum is greater than the maximum revolutions needed for the highest speed remaining line, overrun is indicated, and the analysis is complete.

The projections are made on the 2702 Worksheet as the procedure progresses. Figure 7 illustrates the relationship of the two projections to the maximum number of revolutions needed for the highest speed line. Satisfactory operation is indicated in Figure 7 whenever an upper curve crosses the line indicating the maximum number of revolutions before overrun.

To determine the number of delay line cycles required by a particular communication line, tables of factor values are provided in this manual for use with the *2702 Worksheet*, Form X24-3406.

The factors are used to compute a load sum occurring during the servicing of each communication line. The load sum consists of priority load functions caused by selector channel priority devices and by multiplexor channel priority devices, plus a device load factor and a previous load factor for the terminal being tested. The various factors are entered on the 2702 Worksheet and used to compute a load sum which is compared to the load limit specified on the worksheet for that particular delay line revolution (first, second, etc.).



● Figure 7. Projection of Delay Line Revolution Requirements

If the load sum is greater than the specified load limit, the communication line under consideration requires an additional delay line revolution. The projected minimum time for service is increased one revolution and tested. If overrun is not indicated, the next column of the 2702 Worksheet is used to compute a new load sum which is compared, etc.

If, however, the first load sum mentioned in the previous paragraph was not greater than the specified load limit, adequate service is indicated for the communication line under consideration, and if it was serviced in one revolution, or if it is the last communicaton line to be considered, satisfactory operation of the 2702 is indicated. But if the communication line serviced was not the last one and was not serviced in a single revolution, it is necessary to see if the remaining communication lines can be serviced within the number of revolutions remaining to them. A new projecton of the maximum time for service is made.

In this analysis, no remaining communication line will take more revolutions than the communication line for which satisfactory service was just indicated, so if the number of revolutions it required is multiplied by the number of remaining lines, the results may be compared to the remaining number of revolutions available. A low or equal comparison indicates satisfactory operation and the analysis is complete. A high comparison indicates a need to test the next communication line. This is done by transferring some of the values on the worksheet in use to a fresh 2702 Worksheet and testing the next communication line for satisfactory operation. A load sum is computed and compared with the load limit. Comparison results have the significance already described.

Special Analysis Procedure

The procedure given below is used with the 2702 Worksheet, shown in Figure 12. Each step in the procedure is numbered. Most of the steps call for an entry to be made on the 2702 Worksheet. The numbers in the Figure 13 spaces refer to the step numbers that cause entries to be made in the spaces. (Figures 12-16 are part of the Appendix, which has been placed at the end of this manual so that it can be removed for easy reference.)

The procedure is shown in flow chart form in Figure 14. It also is keyed to the numbered steps in the procedure. Figure 15 shows the worksheet example discussed in the next section of this manual.

The procedure for using the 2702 Worksheet is:

1. Enter the number of communication lines proposed for attachment into the number of lines space and also into the first and second n spaces.
2. Enter 1 in the line number space.
3. Subtract the step 2 entry from the step 1 entry and enter the remainder in the K space.
4. Consult Table 2 and find the smallest Nmax value among the terminals proposed for attachment. Enter the value found in the Nmax space.
5. From Table 2, enter device load and previous load values shown for the terminal selected in step 4.
6. Enter identification of selector channel and multiplexer channel priority devices in the leftmost column in the order of their priority (copy from the Multiplexer Channel Worksheet).
7. Enter a t1 value of zero.
8. Enter zero values in the A 1 and B 1 spaces.
9. Enter a t2 value.
   When j = 1, the t2 value is:
   t1 + .464 for a 15-line 2702
   t1 + .976 for a 31-line 2702
   When j > 1, the t2 value is:
   for a 15-line 2702, previous t2 + .480
   for a 31-line 2702, previous t2 + .992
10. Use the t2 value just entered to select A2 and B2 factors from the left-hand column of the Multiplexer Channel Worksheet. The selected A's and B's are copied from the Multiplexer Channel Worksheet into the A 2 and B 2 spaces on the 2702 Worksheet.

The second set of time A B factors used for a pri-

ority 2702 with a mix of communication line speeds may be:

a. As specified in Table 1 for the highest speed line, or

b. As computed with the procedure given in the "Priority Load Factors for 2702" section of this manual.

11. This step is performed only once per worksheet: enter the A1 sum and B1 sum. (When line number = 1, A1 sum and B1 sum have zero values.)

12. This step is performed only once per worksheet: multiply the B1 sum by the t1 value and enter the product.

13. Enter the A2 sum and B2 sum.

14. Multiply the B2 sum by the t2 value and enter the product.

15. Subtract the A1 sum from the A2 sum and enter the A remainder.

16. Subtract the B1 product from the B2 product and enter the B remainder.

17. Add A remainder, B remainder, device load, previous load, and enter the load sum.

18. The load sum is compared to the appropriate load limit. If not greater, adequate communication line service is indicated; go to step 22. If greater, the communication line needs another delay line revolution; go to step 19.

19. Add 1 to the last entered n value, and enter the sum in the next n space.

20. If the new n value is greater than the Nmax value, no additional delay line revolution is available for the communication line. This indicates overrun.

21. If the new n is not greater than Nmax, go to step 9 and repeat the performance analysis for the fresh delay line revolution. When j is greater than 8, the analysis spills over to another worksheet, and each new load limit is computed by adding a load limit increment to the old load limit.

Load limit increment:

48.0 for 15-line 2702

99.2 for 31-line 2702

22. The step 18 load sum was not greater than the load limit, thereby indicating adequate channel service for the communication line under test. If this is the last communication line, or if it was serviced by the first delay line revolution (j = 1), satisfactory operation of the 2702 is indicated. But if the communication line serviced was not the last one and was not serviced by the first revolution (j greater than 1) add its n value to the product of its revolution number minus one (j − 1) times K, and enter the sum in the space at the bottom of the worksheet, where n + (j − 1) K is printed.

23. If the value just entered is not greater than the Nmax, satisfactory operation of the 2702 is indicated. If greater, get a fresh 2702 worksheet.

24. The number of lines entry for the fresh worksheet stays the same as it was on the old worksheet.

25. The new line number entered is 1 greater than the old line number. The subtraction specified on the worksheet gives a new K value entry 1 less than the old.

26. Enter a new t1 value by adding 0.048 to old t2.

27. The new t1 is used to select priority device A and B factors from the Multiplexer Channel Worksheet for entry into the A1 and B1 spaces.

28. The old n value is entered into the spaces under t1 and j = 1.

29. Go to step 9.

2702 Special Analysis Example

Figure 15 shows a Multiplex Mode Worksheet evaluation of a Model 40 configuration having these I/O devices:

Selector Channel 1:	2311 Disk Storage, chaining with record size = 20
Selector Channel 2:	2311 Disk Storage, data chaining only in record gaps
Multiplexer Channel:	2702 with 15 1030's* running at 600 bps 2702 with 15 1030's running at 600 bps 2702 with 10 1030's running at 600 bps 2702 with 1 1030 running at 600 bps and 10 telegraph lines (45 bps) 1443 Printer (Other devices in the multiplexer channel configuration are not operated concurrently.)

*Data Collection System

Figure 15 shows an excessive load sum of 119.7 for the 2702 having fourth priority; use of the 2702 special analysis procedure is indicated.

Figure 16 shows the completed 2702 Worksheet used in the special analysis. The 2702 special analysis procedure in the preceding section of this manual was used in making the entries.

Figure 16 (Sheet 1) shows service to be completed for the 1030 on the fifth cycle; the projected maximum number of cycles needed is 55, which is greater than the Nmax of 30; a fresh 2702 Worksheet is used.

Figure 16 (Sheet 2) continues the analysis. The Nmax factor of 30 does not change; the procedure assumes that if all terminals request service, the 1030 may be the last to be serviced. The Nmax factor for the highest speed line is always used.

Figure 16 (Sheet 2) shows that the projected maximum number of revolutions needed for the remaining telegraph lines is not greater than Nmax.

This indication of satisfactory operation for the 2702 completes the evaluation of the communication configuration for concurrent operation.

Priority Load Factors for 2702

An IBM 2702 Communication Control may have terminal lines attached that all operate at the same speed. Where this is the case, priority load A and B factors used for the Multiplexer Channel Worksheet evaluation are referenced from Table 1 for the type of terminal control and number of lines attached.

An IBM 2702 Communication Control may have a configuration of terminal lines that operate at different speeds. Where this is the case, the Table 1 priority load factors for the highest speed line may be used. The A and B factors are referenced for the number of lines attached and are entered on the Multiplexer Channel Worksheet. In so doing, the slower speed lines receive undue weight, but if their use does not cause any load sum to exceed 100, satisfactory operation is indicated. The disparity in line speeds may be ignored.

If their use indicates unsatisfactory multiplexer channel operation, however, a more accurate assessment of the situation may be made, as described below.

When A and B factors from Table 1 for a priority 2702 having more than one terminal speed are selected for the highest speed line, their use may contribute to an excessive load sum for a lower priority device and a false indication of unsatisfactory operation.

More accurate time, A, and B factors may be computed for consideration in computing priority loads for 2702's with terminal lines of different speeds attached. The computation has three basic steps:

1. Retain the first set of time A B factors already entered on the Multiplexer Channel Worksheet for the priority 2702.

2. Compute a new second set of time A B factors which replace the second set already entered.

3. Use the new wait time ranges established in steps 1 and 2 immediately above to select A and B factors for use in computing a new priority load for the 2702.

New load sums are then computed. Any new load sum that is less than or equal to 100 indicates satisfactory operation for the load sum device.

Each new second set of time A B factors is computed as specified in steps 1-7 below. An example computation is shown immediately following step 7.

1. Select from Table 3, Segment 1, a b factor for each type of terminal. Multiply each b factor by the number of terminal lines having that b factor, and add all of the products. The sum of the products is the new B factor.

2. Subtract the new B factor, from the B factor specified in Segment 2 of Table 3. The remainder is an intermediate value used in step 4.

Note that the set of time A B factors in Segment 2 are the same as the first (uppermost) set already entered for the priority 2702 on the Multiplexer Channel Worksheet. This first set does not change.

3. Find the time factor for the number of lines attached in Segment 3 of Table 3. This is the new time factor.

4. Multiply the new time factor by the remainder found in step 2. The product is an intermediate factor used in step 5.

5. Add the A factor in Segment 2 of Table 3, to the product found in step 4. The sum is the new A factor.

6. Substitute the time A B factors found in steps 3, 5, and 1 in place of the second set of time A B factors previously entered on the Multiplexer Channel Worksheet for the priority 2702.

7. Repeat steps 1-6 for any remaining 2702 priority devices and consider the new time A B factors in computing new load sums for the devices previously found to have excessive load sums.

For example, a new second set of time A B factors are computed for a 2702 with a mix of line speeds as shown below.

Consider a 15-line 2702 to which is attached:

One 1030 Line – IBM Terminal Control – Type 11 @ 60 bps
Ten 1050 Lines – IBM Terminal Control – Type 1 @ 135.5 bps

Step 1. From Table 3, Segment 1

1030:	1 x .166	= .166
1050:	10 x .035	= .350
	new B	= .516

Step 2. From Segment 2: B = 12.01
From step 1: new B = .516
11.494

Step 3. For 11 lines: Time = 5.182

Step 4: From step 2: Difference = 11.494
Time = 5.182
Product = 59.562

Step 5. From Segment 2: A = 5.411
From step 4 Product = 59.562
new A = 64.973

Step 6. Previous priority load factors (from Table 1):

TIME	A	B
.200	5.41	12.0
5.18	58.2	1.83

New priority load factors:

TIME	A	B
.200	5.41	12.0
5.18	65.0	.516

Synchronization Tendency of Buffer Servicing

When evaluation of a multiplex mode configuration shows loss of performance for several buffered devices, additional analysis may show that some of them can be expected to have infrequent, trifling reduction in performance, and that others will have loss in performance somewhat more often. This is because of

the tendency of multiple buffered devices to synchronize, to a greater or lesser extent, their use of channel facilities. The analysis enables an estimate to be made of how often a buffered device can be expected to have loss in performance.

By estimating the delays involved in servicing the device's buffers and relating the delays to the device's requests for channel service, it may be discovered that some of the buffered priority devices do not interfere with buffered waiting devices to the extent premised in the evaluation procedure. The procedure assumes a random relationship between the operations of the various I/O devices that may not apply to buffered devices.

For example, if both of two card readers in operation request channel service at the same time, the higher priority device will force the other device to wait; and having once waited, the second card reader will next request channel service after the first device has already made its next request for channel service. The two new requests will not coincide unless the first card reader has been similarly delayed by some other device. This synchronization effect tends to organize buffered device's requests for channel service into a sequence that enables the channel to service them on a rotating basis, and a loss of performance premised on random channel service requests may be significantly reduced.

The analysis of the synchronization effect is done by laying out the operating cycles of the buffered devices in their priority sequence, one below another, on a millisecond scale. The devices that operate satisfactorily are drawn with a zero starting point. A new starting point is established on the millisecond scale for each device found to incur delay. The resulting synchronization pattern may be studied to see which buffered device priority loads may be ignored in computing new load sums.

Operation cycle times are specified in Systems Reference Library manuals for the devices.

Multiplexer channel capabilities for maintaining performance of multiple buffered I/O devices may be calculated through simulation with greater accuracy when the number of characters in a line of print, forms layout, programming requirements, etc., are known for a particular application. On the other hand, an application known to be CPU-limited will cause reduced input/output performance, even though the channels are capable of operating the I/O devices concurrently at their rated speeds.

A channel operation on the Model 40 interferes with CPU use of main storage whenever the channel requests access to main storage. Additional CPU interference is generated because the channels use some CPU facilities. Burst mode operation of the multiplexer channel locks out the CPU.

Each device operating in multiplex mode causes CPU interference. The amount of CPU interference caused by an I/O device over a period of time depends on its data transfer rate and its channel programming. Table 4 lists the factors used to compute Model 40 channel interference with CPU.

When an application requires concurrent operation of I/O devices, it must first be determined that the devices will operate without overrun. This is done as described in the channel loading sections of this manual.

Channel Interference Procedure

After an indication of satisfactory operation has been found, channel interference with the CPU may be computed, after which available CPU time may be computed. The procedure has three steps:

1. Examine record lengths, data transfer rates, gap times, device operating cycle times, etc., and establish an I/O operation time span in milliseconds pertinent to the application.
2. Add the microseconds of CPU interference caused during the I/O time span by:
   a. Execution of start I/O's
   b. Execution of CCW's
   c. Data transfer
   d. I/O interruptions

   Interference for fetching the CAW and the specified CCW are not a factor; they are fetched during start I/O interference time.
3. Subtract the sum of total CPU interference time in milliseconds from the I/O time span. The difference is the milliseconds of time available for CPU operations during the time span.

Dividing the available CPU time by the time span and multiplying by 100 gives the percentage of available CPU time for the application considered:

$$\frac{\text{available CPU time}}{\text{time span}} \times 100 = \%\ \text{available CPU time}$$

The CPU time required by a program to identify interruptions, etc., is not considered in this manual.

An application that uses more CPU time to process input data for output than is computed to be available will have an actual I/O time span greater than that found in the computation of available CPU time. The increased I/O time span will result in an increase in job time for the application that may be computed as:

channel interference time + CPU time needed = increased time span

increased time span − original time span = time span increment

$$\frac{\text{time span increment}}{\text{original time span}} \times 100 = \%\ \text{increment in job time}$$

In the rare instance where available CPU time is computed to be zero, CPU operations are not necessarily precluded; the CPU may yet gain occasional access to storage. Thus, a finding of 100 percent CPU interference cannot be depended upon to prevent execution of a start I/O instruction that could overload the channels and cause overrun or loss of performance.

On the other hand, a computation of less than 100 percent CPU interference does not insure that the I/O devices will run concurrently. As stated previously, the configuration must be separately evaluated for concurrent operations.

Available CPU Time Example

Application

Tape-to-printer operation

Configuration

The Model 40 uses a data-chaining IBM 2403 Model 2 tape unit at 800 bytes per inch (bpi) on the first selector channel, and an IBM 1403-N1 Printer on the multiplexer channel.

Analysis

The tape read operation handles 1000-byte tape blocks data chained into ten scattered 100-byte blocks in main storage.

The printer may be programmed with a start I/O for each line of print, or it may be programmed with one start I/O and nine chained commands for each ten lines of print. The difference in CPU interference caused by the two approaches is examined in the example.

Evaluation for Concurrent Operation

Overrun or loss of performance appear unlikely. Briefly, however, these are the considerations:

The 2403-2, 800 bpi DC load of 11 is less than the single selector channel DC load limit of 50; it will run satisfactorily. Only one set of A B factors are listed for the priority 2403-2, 800 bpi, without byte conversion and they are A = 0.98 B = 8.10. The 1403 has a wait time of 15.7.

The A/wait time + B = priority load formula yields:

$$\frac{.98}{15.7} + 8.10 = 8.16 \text{ priority load}$$

The 1403 device load is 14.4 and its previous load is 0.64. A load sum is computed:

Priority load	=	8.16
Device load	=	14.4
Previous load	=	0.64
Load sum	=	23.20

The load sum is less than 100; satisfactory concurrent operation is indicated.

Arithmetic for Channel Interference Example

The computation of available CPU time demonstrated below uses the same four steps already described:

1. Establish I/O time span.
2. Compute channel interference with CPU.
3. Subtract sum of interference from the time span to find available CPU time.
4. Divide available CPU time by time span to obtain percentage of CPU time available.

The information necessary to execute step 2 is found in Tables 1 and 4, and operating cycle times for I/O devices are found in the IBM Systems Reference Library Principles of Operation manuals for the devices.

Table 1 provides data transfer rates, gap times, and multiplex mode CPU interference per byte in microseconds.

Table 4 provides selector channel microseconds CPU delay per byte transferred, plus microseconds CPU delay per CCW execution and end interruptions.

Step 1: Establish time span.

The time needed to read this 1000-byte tape record block (24.7 ms) may be referenced directly from the tape timing card, *IBM System/360 Magnetic Tape Record Characteristics for IBM 2400 Series Magnetic Tape Units,* Form X22-6837, or computed from the factor values for the formula on the same card:

Model 1 – ms per record block = 16.0 + 0.0333N
Model 2 – ms per record block = 8.0 + 0.0167N
Model 3 – ms per record block = 5.3 + 0.0111N
N = Number of bytes in record block

This formula, gap time plus byte time x number of bytes, allows for both tape start and stop time.

For our example:

0.0167 x 1000 = 16.7
8.0 + 16.7 = 24.7 milliseconds to read each 1000 byte block

The time to print ten lines is ten times 1403 N1 print cycle time:

10 x 54.5 = 545 milliseconds to print 10 lines

The tape and printer operations will be overlapped, and the longer printer time of 545 ms is the time span pertinent to the application configuration.

Step 2: Compute channel interference with CPU.

Tape transfer interference time is the product of the number of bytes in the tape block multiplied by the selector channel byte transfer CPU interference factor, 1.25 microseconds (from Table 4):

1000 x 1.25 = 1250 microseconds tape transfer interference

Tape data chaining interference time is the product of the number of data chaining operations per record block and the selector channel data chaining CPU interference factor, 10.625 microseconds (from Table 4):

9 x 10.625 = 95.625 microseconds tape data chaining interference

Printer transfer interference is found by referencing Table 1 and computing the product of the number of characters per print line times the multiplex channel byte transfer CPU interference factor, 16.5 microseconds (from Table 1) times the number of print lines handled during the time span:

100 x 16.5 x 10 = 16500 microseconds printer transfer interference

Printer command time is the product of the number of chained commands per time span times the multiplexer channel command chaining CPU interference factor, 68.1 microseconds (from Table 4):

9 x 68.1 = 612.9 microseconds printer command interference

Start I/O interference factors are referenced from the instruction timing section of this manual, end interruption factors are referenced from Table 4, and total interference time may be computed:

	MICROSECONDS
Tape	
Start I/O	45.0
Transfer interference (as previously computed)	1250.0
Data chaining interference (as previously computed)	95.6
Channel end with device end interruption	45.0
Printer	
Start I/O	65.0
Transfer interference	16,500.0
Command chaining interference	612.9
Channel end interruption	60.6
Device end interruption	56.9
Total interference time =	18,731.0

Step 3: Compute available CPU time in milliseconds.

Available CPU time is found by subtracting the interference time from the time span:

545. – 18.7 = 526.3 milliseconds available CPU time

Step 4: Compute available CPU time as a percentage.

The CPU interference may be expressed as a per-

centage by dividing the interference time by the time span and multiplying by 100:

18.7/545 x 100 = 3.4 percent CPU interference

Command Chaining Efficiency

By ignoring printer data transfer interference, attention may be focused on the CPU interference caused by channel control functions for the printer. In the example, command chaining may be eliminated if a start I/O is used for each print line. A comparison of the CPU interferences caused by the two methods reveals which is more efficient, as shown below.

Printer control interference using command chaining is:

	MICROSECONDS
Start I/O	65.0
Command chaining	612.9
Channel end	60.6
Device end	56.9
Printer control interference using command chaining =	795.4

If command chaining is not used for printer operation each print line occasions a start I/O and an end interruption, and the following arithmetic applies:

	MICROSECONDS
Start I/O – 65 x 10 =	650.
Device end – 56.88 x 10	568.8
Channel end – 60.63 x 10	606.3
Total	1825.1

Printer control interference using no command chaining is 1825.1 microseconds.

The use of a start I/O for each print-line occasions 1825.1 – 795.4 = 1029.7 microseconds additional CPU interference. Command chaining is clearly more efficient.

System/360 Model 40 Instruction Times

The instruction time tables presented in this bulletin are divided into two groups:

Group 1 — This group of instruction times provides the average time for all instructions used with the Model 40.

Group 2 — This group of instruction times contains the detailed timing formulas for all variable field length (VFL) instructions used with the Model 40.

All symbols used in the VFL formulas should be interpreted in accordance with the Legend for System/360 Timing.

Within each group, timings are provided for instruction execution when instructions and data are located in processor storage. All times are given in microseconds. Complete information for each instruction is included in the publication *IBM System/360 Principles of Operation,* Form A22-6821. Standard System/360 Timing Legends have been provided, therefore all legends listed may not apply to the Model 40.

Timing Considerations

The following conditions (unless otherwise noted) were used in the development of these instruction time tables (both groups).

1. The time required for indexing by a base register is included in the times given. For those instructions that may be double indexed (indicated by one or two asterisks in the instruction name column), an additional 1.25 microsecond (one asterisk) or 1.88 microsecond (two asterisks) must be added to the times given in the table.
2. In all arithmetic operations, positive and negative operands are equally probable.
3. Each bit location has equal probability of containing bit values 0 or 1, and each bit location is independent of other bit locations.

Decimal data may contain digit values 0-9 in each digit position with equal probability.

4. Instructions may start on even or odd halfwords with equal probability.
5. Interruptions are not reflected in these timings.
6. All timings provided include both decoding and execution of the instruction.

Timing Assumptions

The following assumptions (unless otherwise noted) were used in the development of the instruction time tables.

1. For decimal add (AP) and decimal subtract (SP) instructions, the first operand (i.e., the destination field) is assumed to be equal to or greater than the length of the second operand (i.e., the source field).
2. The instruction times for the floating-point instructions depend on the number of hexadecimal digits that are preshifted and postshifted, as well as the number of times recomplementation of the result occurs. Each of the floating-point instruction times listed is an *average* of actual execution times. Although each value is the most accurate that can be given, the actual time is data-dependent.
3. The supervisor call (SVC) instruction includes interruption time.

Average Times

INSTRUCTION	FORMAT	MNEMONIC	
Add	RR	AR	$7.5 + 1.25G_2$
Add*	RX	A	$11.88 + 1.25G_2$
Add Decimal	SS	AP	$28.75 + 1.25N_1 + 2.5M - 1.25T_{16}$
Add Halfword*	RX	AH	A_5: 10.63 A_6: $11.25+1.25G_2$
Add Logical	RR	ALR	7.5
Add Logical*	RX	AL	11.88
Add Normalized (Long)	RR	ADR	34.20

INSTRUCTION	FORMAT	MNEMONIC	
Add Normalized (Long)**	RX	AD	39.70
Add Normalized (Short)	RR	AER	14.50
Add Normalized (Short)**	RX	AE	18.85
Add Unnormalized (Long)	RR	AWR	31.75
Add Unnormalized (Long)**	RX	AW	37.20
Add Unnormalized (Short)	RR	AUR	13.85
Add Unnormalized (Short)*	RX	AU	18.20
AND	RR	NR	7.5
AND*	RX	N	11.88
AND	SI	NI	9.38
AND	SS	NC	$16.88 + 3.13N$
Branch and Link	RR	BALR	$6.88 + 1.88F_2$
Branch and Link*	RX	BAL	11.25
Branch on Condition	RR	BCR	$3.13 + F_2\ (1.26 + .63F_1)$
Branch on Condition*	RX	BC	9.38
Branch on Count	RR	BCTR	$7.50 + 1.25F_2 - .63F_1$
Branch on Count*	RX	BCT	$11.26 - .63F_1$
Branch on Index High	RS	BXH	16.25
Branch on Index Low or Equal	RS	BXLE	16.25
Compare	RR	CR	7.5
Compare*	RX	C	11.88
Compare Decimal	SS	CP	$22.19 + 1.25N_1 + 1.25M + 1.25T_{16}$
Compare Halfword*	RX	CH	(Inequality determined by:) Signs 9.38 Byte 0 or 1 10.00 Byte 2 10.63 Byte 3 or = 11.25
Compare Logical	RR	CLR	7.5
Compare Logical*	RX	CL	11.88
Compare Logical	SI	CLI	8.75
Compare Logical	SS	CLC	$12.04 + 2.81B + 3.73T_{15}$
Compare (Long)	RR	CDR	33.15

INSTRUCTION	FORMAT	MNEMONIC	
Compare (Long)**	RX	CD	28.80
Compare (Short)	RR	CER	11.90
Compare (Short)**	RX	CE	16.38
Convert To Binary*	RX	CVB	*Number of Significant Digits* / *Average Time*: 0 — 31.88; 1 — 31.88; 2 — 32.19; 3 — 36.25; 4 — 40.31; 5 — 46.88; 6 — 53.44; 7 — 60.63; 8 — 67.81; 9 — 77.50; 10 — 86.56
Convert To Decimal*	RX	CVD	(Subscript shows number of leading zero bytes:) CVD_4 28.13; CVD_3 40.00; CVD_2 53.75; CVD_1 72.50; CVD_0 95.63
Divide	RR	DR	*Significant Divisor Bytes* / *Time*: 4 — 188.0; 3 — 192.5; 2 — 143.8; 1 — 156.0
Divide*	RX	D	*Significant Divisor Bytes* / *Time*: 4 — 143.0; 3 — 146.9; 2 — 139.4; 1 — 141.0
Divide Decimal	SS	DP	$13.13 + 29.06N_1 - 22.81N_2 + 11.25N_2 (N_1 - N_2)$
Divide (Long)	RR	DDR	472.5
Divide (Long)**	RX	DD	480.65
Divide (Short)	RR	DER	136.30
Divide (Short)**	RX	DE	141.08
Edit	SS	ED	$21.25 + 3.12N + 3.44N_2 - .94N_4 + .63N_5 + 2.5SG$
Edit and Mark	SS	EDMK	$21.25 + 3.12N + 3.44N_2 - .94N_4 + .63N_5 + 2.5SG + 3.13MK$

INSTRUCTION	FORMAT	MNEMONIC	
Exclusive OR	RR	XR	7.5
Exclusive OR*	RX	X	11.88
Exclusive OR	SI	XI	9.38
Exclusive OR	SS	XC	$16.88 + 3.13N$
Execute*	RX	EX	$8.13 + .625T_{12} + E$
Halt I/O	SI	HIO	See I/O Tables
Halve (Long)	RR	HDR	$231.85 + 9.4X + 7.25H_2$
Halve (Short)	RR	HER	$101.16 + 3.84X + 3.75H_2$
Insert Character*	RX	IC	9.38
Insert Storage Key	RR	ISK	7.5
Load	RR	LR	7.5
Load*	RX	L	11.88
Load Address*	RX	LA	10.0
Load and Test	RR	LTR	7.5
Load and Test (Long)	RR	LTDR	12.5
Load and Test (Short)	RR	LTER	7.5
Load Complement	RR	LCR	$7.5 + 1.25G_2$
Load Complement (Long)	RR	LCDR	12.5
Load Complement (Short)	RR	LCER	7.5
Load Halfword*	RX	LH	10.63
Load (Long)	RR	LDR	12.5
Load (Long)**	RX	LD	16.88
Load Multiple	RS	LM	$6.25 + 5GR$
Load Negative	RR	LNR	7.5
Load Negative (Long)	RR	LNDR	12.5
Load Negative (Short)	RR	LNER	7.5
Load Positive	RR	LPR	$7.5 + 1.25G_2$
Load Positive (Long)	RR	LPDR	12.5
Load Positive (Short)	RR	LPER	7.5
Load PSW	SI	LPSW	16.25

INSTRUCTION	FORMAT	MNEMONIC	
Load (Short)	RR	LER	7.5
Load (Short)**	RX	LE	11.88
Move	SI	MVI	9.38
Move	SS	MVC	$16.57 + 2.5N$
Move Numerics	SS	MVN	$16.88 + 3.75N$
Move With Offset	SS	MVO	$13.75 + 5.63N_1 + T_{13}\,[2.50 - 2.50N_1 + 2.50N_2]$
Move Zones	SS	MVZ	$16.88 + 3.75N$
Multiply	RR	MR	60.0
Multiply*	RX	M	49.4
Multiply Decimal	SS	MP	$22.92 + 21.81N_1 - 17.84N_2 + 3.75N_2\,(N_1 - N_2) + 3.75T_7$
Multiply Halfword*	RX	MH	45.0
Multiply (Long)	RR	MDR	255.0
Multiply (Long)**	RX	MD	259.4
Multiply (Short)	RR	MER	76.3
Multiply (Short)**	RX	ME	80.6
OR	RR	OR	7.5
OR*	RX	O	11.88
OR	SI	OI	9.38
OR	SS	OC	$16.88 + 3.13N$
Pack	SS	PACK	$11.88 + 5.63N_1 + 1.25N_2 + T_{17}\,(2.17 - 2.50N_1 + .63N_2)$
Read Direct	SI	RDD	$12.5 + ED$
Set Program Mask	RR	SPM	5.0
Set Storage Key	RR	SSK	8.75
Set System Mask	SI	SSM	10.0
Shift Left Double	RS	SLDA	See Shift Table – SLDA
Shift Left Double-Logical	RS	SLDL	See Shift Table – SLDL
Shift Left Single	RS	SLA	See Shift Table – SLA
Shift Left Single-Logical	RS	SLL	See Shift Table – SLL

INSTRUCTION	FORMAT	MNEMONIC	
Shift Right Double	RS	SRDA	See Shift Table – SRDA
Shift Right Double-Logical	RS	SRDL	See Shift Table – SRDL
Shift Right Single	RS	SRA	See Shift Table – SRA
Shift Right Single-Logical	RS	SRL	See Shift Table – SRL
Start I/O	SI	SIO	See I/O Tables
Store*	RX	ST	12.5
Store Character*	RX	STC	10.0
Store Halfword*	RX	STH	10.0
Store (Long)**	RX	STD	17.5
Store Multiple	RS	STM	$6.87 + 5GR$
Store (Short)**	RX	STE	12.5
Subtract	RR	SR	$7.5 + 1.25G_2$
Subtract*	RX	S	$11.88 + 1.25G_2$
Subtract Decimal	SS	SP	$28.75 + 1.25N_1 + 2.5M - 1.25T_{16}$
Subtract Halfword*	RX	SH	A_5: 10.63 A_6: $11.25 + 1.25G_2$
Subtract Logical	RR	SLR	7.5
Subtract Logical*	RX	SL	11.88
Subtract Normalized (Long)	RR	SDR	35.70
Subtract Normalized (Long)**	RX	SD	41.30
Subtract Normalized (Short)	RR	SER	16.25
Subtract Normalized (Short)**	RX	SE	20.62
Subtract Unnormalized (Long)	RR	SWR	33.15
Subtract Unnormalized (Long)**	RX	SW	38.80
Subtract Unnormalized (Short)	RR	SUR	15.0
Subtract Unnormalized (Short)**	RX	SU	19.4
Supervisor Call	RR	SVC	23.75
Test and Set	SI	TS	10.00
Test Channel	SI	TCH	B_1: 11.88 B_3: 13.75
Test I/O	SI	TIO	See I/O Tables
Test Under Mask	SI	TM	8.75

INSTRUCTION	FORMAT	MNEMONIC	
Translate	SS	TR	$16.88 + 6.25N$
Translate and Test	SS	TRT	Case 1: *Condition Code 0* $18.13 + 3.75N - 2.50T_{18}$ Case 2: *Condition Code 1* $21.88 + 3.75B$ Case 3: *Condition Code 2* $21.88 + 3.75N$
Unpack	SS	UNPK	$16.32 + 3.12N_1 - T_{19}$ $(2.03 + .78N_1 - 2.5H_2)$
Write Direct	SI	WRD	9.37
Zero and Add	SS	ZAP	$25.32 + 2.5M$

I/O Tables

START I/O

CONDITION CODE		MULTIPLEXER CHANNEL	SELECTOR CHANNEL
0	I/O operation initiated and channel proceeding with its execution	$65.00 + U_1$	$45.00 + U_1$
1	CSW stored; immediate operation initiated or command rejected	$60.00 + U_1$	$48.75 + U_1$
2	Channel or subchannel busy	14.38	13.13
3	Device not operational	$41.25 + U_1$	$43.75 + U_1$
3	Channel or subchannel not operational	15.00	10.00

TEST I/O

CONDITION CODE		MULTIPLEXER CHANNEL	SELECTOR CHANNEL
0	Subchannel and device available	$31.25 + U_1$	$31.88 + U_1$
1	CSW stored, device status only	$48.13 + U_1$	$48.75 + U_1$
1	CSW stored: end interruption in subchannel	50.63	28.13
1	CSW stored: end interruption in device	$63.13 + U_1$	Not applicable
2	Channel or subchannel busy	15.00	15.00
3	Device not operational	$26.88 + U_1$	$27.5 + U_1$
3	Channel or subchannel not operational	15.00	10.00

HALT I/O

CONDITION CODE		MULTIPLEXER CHANNEL	SELECTOR CHANNEL
0	Interrupt pending in subchannel	15.0	13.75
1	CSW stored	$31.88 + U_1$	$32.5 + U_1$
2	Burst operation terminated	Not applicable	$19.38 + U_2$
3	Device not operational	$23.75 + U_1$	$27.5 + U_1$
3	Channel not operational	15.00	10.00

Shift Tables

NO OF PLACES SHIFTED	SRL	SLL	SRA*	SLA*	SRDL	SLDL	SRDA*	SLDA†
0	11.25	10.62	14.37	16.25	11.87	11.87	18.12	20.00
1	15.00	15.00	18.13	20.63	20.63	18.75	26.88	26.88
2	20.00	19.38	23.13	25.00	27.50	27.50	33.75	35.63
3	15.00	18.13	18.13	23.75	18.13	24.38	24.38	32.50
4	15.00	15.00	18.13	20.63	18.13	18.75	24.38	26.88
5	18.13	15.00	21.25	20.63	26.25	18.75	32.50	26.88
6	20.00	19.38	23.13	25.00	27.50	27.50	33.75	35.63
7	15.00	18.13	18.13	23.75	18.13	24.38	24.38	32.50
8	15.00	14.37	18.13	20.00	18.13	18.12	24.38	26.26
9	18.13	14.37	21.25	20.00	26.25	18.12	32.50	26.26
10	19.38	19.38	22.50	25.00	26.25	27.50	32.50	35.63
11	15.00	18.13	18.13	23.75	19.38	24.38	25.63	32.50
12	15.00	14.37	18.13	20.00	19.38	18.12	25.63	26.26
13	18.75	14.37	21.88	20.00	28.13	18.12	24.38	26.26
14	19.38	19.38	22.50	25.00	26.25	27.50	32.50	35.63
15	15.00	16.25	18.13	21.88	19.38	25.00	25.63	33.13
Additional Times for shifts to be added to shifts of less than 16 places								
16	3.75	3.13	3.75	3.75	7.50	5.63	7.50	6.25
32	6.88	5.63	6.88	6.88	14.38	10.63	14.38	11.88
48	10.00	8.13	10.00	10.00	21.25	15.63	21.25	17.50

Notes: Add .625 μs to total if base addressing is used.
*Subtract 1.88 μs if number shifted is negative.
†Subtract 4.38 μs if number shifted is negative.

Variable Field Length Instructions

In the following timing formulas, the times for the variable field length instructions (i.e., those instructions that contain an "L" field) are given in terms of word boundary crossovers and the operand addresses. The term "word boundary" is used to specify the boundary between two physical words. A physical word is the amount of information fetched in a single storage cycle (for Model 40 this is 16 bits). Thus, the number of word boundary crossovers is one less than the number of half words spanned by the field.

All symbols used in the following VFL detailed timing formulas should be interpreted in accordance with the Legend for System/360 Timing (Detail VFL Times).

ADD Decimal—AP

$$26.88 + 1.25N_1 + 2.5M + .625 \\ [3HB_1 - LB_1 + (1 - T_{16}) + 2(1 - T_{16})\,HB_2]$$

AND—NC

$$14.38 + 3.13N + 3.13\,HB_1 + 3.75\,HB_2 \\ - 3.13\,(HB_1)\,(HB_2) - .63\,(LB_1)\,(LB_2)$$

Compare Decimal—CP

$$22.5 + 1.25N_1 + 1.25M + .625 \\ [(1 - T_{16}) + 2(1 - T_{16})\,HB_2 - LB_1]$$

Compare Logical—CLC

Case 1: If number of bytes compared before inequality is found to be less than or equal to N

$$16.26 + 5.63\,NWBB_1 + .63\,HB_2 \\ + 4.38\,HB_1\,(1 - HB_2)$$

Case 2: If operands are equal

$$14.06 + 2.81\,N + .31 \\ [3HB_1 + 6HB_2 + 4LB_1 + 3LB_2 \\ -10\,(LB_1)\,(LB_2)]$$

Divide Decimal—DP

$$13.13 + 29.06\,N_1 - 22.81\,N_2 + 11.25\,N_2\,(N_1 - N_2)$$

EDIT—ED

$$28.13 + 3.12N + 1.25HB_1 - .63LB_1 + .63N_5 \\ - .94N_4 + 6.88\,NWBL_2 - .63HB_2 + 2.5\,SG$$

EDIT and MARK—EDMK

$$28.13 + 3.12N + 1.25HB_1 - .63LB_1 + .63N_5 - .94N_4 \\ + 6.88NWBL_2 - .63HB_2 + 2.5SG + 3.13MK$$

Exclusive OR—XC

$$14.38 + 3.13\,N + 3.13HB_1 + 3.75HB_2 \\ - 3.13\,(HB_1)\,(HB_2) - .63\,(LB_1)\,(LB_2)$$

Move Characters—MVC

$$14.38 + 2.5N + 2.5HB_1 + 3.13HB_2 \\ - 1.88\,(HB_1)\,(HB_2) + .63LB_2 \\ - 1.88\,(LB_1)\,(LB_2)$$

Move Numerics—MVN

$$14.38 + 3.75N + 3.13\,HB_1 + 3.75\,HB_2 \\ - 3.13\,(HB_1)\,(HB_2) - .63\,(LB_1)\,(LB_2)$$

Move with Offset—MVO

$$13.75 + 5.63N_1 + T_{13}\,(2.50 - 2.5N_1 + 2.5N_2)$$

Move Zones—MVZ

$$14.38 + 3.75N + 3.13HB_1 + 3.75HB_2 \\ - 3.13\,(HB_1)\,(HB_2) - .63\,(LB_1)\,(LB_2)$$

Multiply Decimal—MP

$$22.92 + 21.81N_1 - 17.84N_2 + 3.75N_2\,(N_1 - N_2) \\ + 3.75T_7$$

OR—OC

$$14.38 + 3.13N + 3.13\,HB_1 + 3.75\,HB_2 \\ - 3.13\,(HB_1)\,(HB_2) - .63\,(LB_1)\,(LB_2)$$

Pack—PACK

Case 1:

If $N_1 > \frac{N_2}{2}$

$$13.13 + 3.13N_1 + 1.25N_2 \\ + 1.25N_2\,(LB_2) + 1.25\,(1 - LB_2)\,(HB_2 + 1)$$

Case 2:

If $N_1 \leq \frac{N_2}{2}$

$$13.13 + 5.63N_1 + 2.5\,(LB_2)\,(N_2 - 1)$$

Subtract Decimal—SP

$$26.88 + 1.25N_1 + 2.5M + .625 \\ [3HB_1 - LB_1 + (1 - T_{16}) + 2(1 - T_{16})\,HB_2]$$

Translate—TR

$$15.63 + 6.25N + 1.88HB_1 + .63LB_1$$

Translate and Test—TRT

Case 1:

Condition Code 0

$$15.63 + 3.75N + (4.38HB_1 + .63LB_1)\,(1 - T_{18})$$

Case 2:

Condition Code 1

$$20.63 + 3.75B + 4.38HB_1 - 1.88LB_1$$

Case 3:

Condition Code 2

$$20.0 + 5.63N + (4.38HB_1 - .63LB_1 \\ - 1.88N)\,(1 - T_{18})$$

Unpack—UNPK

Case 1:

If $N_1 > 2N_2$

$$13.13 + 1.56N_1 + 2.5N_2 + 1.56(LB_1)\,N_1 \\ + .94\,(1 - LB_1)\,(HB_1 + 2)$$

Case 2:

If $N_1 \leq 2N_2$

$$15.94 + 2.34N_1 + 1.56\,(LB_1)\,N_1 + 3.44HB_1 \\ - 4.69\,(LB_1)\,(HB_1) - .31LB_1$$

Zero and Add—ZAP

$$24.38 + 2.5M + 1.88HB_1$$

Legend for System/360 Timing

This section contains legends for the timing formulas for the cases where multiple timing formulas for instructions are listed. In some cases more than one timing formula for an instruction may be given.

Legends A_1 to A_4 are timing formulas for Store Multiple or Load Multiple instructions depending on quantity of general registers and position with respect to doubleword boundaries.

A_1: Use if the number of registers is 2, and if the operand lies on doubleword boundaries

A_2: Use if the number of registers is $>$ 2 and even, and if the operand lies on doubleword boundaries

A_3: Use if the number of registers is even, and if the operand does *not* lie on doubleword boundaries

A_4: Use if the number of registers is odd

Legends A_5 and A_6 are timing formulas for the Subtract Halfword instruction.

A_5: Use if leading 16 bits are *not* changed by Subtract Halfword instruction

A_6: Use if leading 16 bits are changed by Subtract Halfword instruction

Legends B_1 to B_4 are timing formulas to be used when addressing a channel.

B_1: Use when addressing the multiplexer channel in the multiplex mode

B_2: Use when addressing the multiplexer channel in the burst mode — first execution

B_3: (Same as B_2) — executions subsequent to the first, during the same burst mode operation

B_4: Use when addressing the selector channel

Legends CH_1 to CH_4 are timing formulas to use for Compare Halfword instruction, depending on the nature of the numbers being handled.

CH_1: Use if signs differ

CH_2: Use if signs are alike, and the high-order 16 bits of the first operand are significant

CH_3: Use if inequality is found in byte 2

CH_4: Use if inequality is found in byte 3, or if comparison is equal

Legends C_1 to C_3 are timing formulas to use for radix (number base) conversion instructions, depending on the size of the number converted.

C_1: Use when the number converted contains eight or less decimal digits

C_2: Use when the number converted contains more than eight decimal digits, but seven or less hexadecimal digits

C_3: Use when the number converted contains more than seven hexadecimal digits

Legends CVD_0 to CVD_4 are timing formulas to use for the Convert to Decimal instruction, depending on the number of leading zero bytes.

CVD_0: Use if there are no leading zero bytes

CVD_1: Use if there is one leading zero byte

CVD_2: Use if there are two leading zero bytes

CVD_3: Use if there are three leading zero bytes

CVD_4: Use if there are four leading zero bytes

Legends D_1 to D_8 are timing formulas to be used depending on the state of the addressed channel.

D_1: Use if the multiplexer channel is busy and in the multiplex mode

D_2: Use if the multiplexer channel is busy and in the burst mode — first execution

D_3: (Same as D_2) — executions subsequent to the first, during the same burst mode operation

D_4: Use if the multiplexer channel is idle

D_5: Use if the multiplexer channel has an interruption pending

D_6: Use if the selector channel is busy

D_7: Use if the selector channel is idle

D_8: Use if the selector channel has an interruption pending

Legends E_1 to E_4 are timing formulas to use for the Execute instruction, depending on the instruction length code and varying conditions.

E_1: Use when subject instruction is one halfword long

E_2: Use when subject instruction is two halfwords long

E_3: Use when subject instruction is a three-halfword character instruction

E_4: Use when subject instruction is a three-halfword decimal instruction

Legends V_1 to V_4 are timing formulas to use for the Move instruction, depending on the location of operand fields.

V_1: Use if first and second operand fields start and end on doubleword boundaries

V_2: Use if first and second operand fields start at corresponding byte addresses within doublewords but do not lie on doubleword boundaries

V_3: Use if first and second operand fields do not start at corresponding byte addresses within doublewords or if $N < 8$.

V_4: Use if first and second operand fields start on doubleword boundaries but do not end on doubleword boundaries. N must be greater than seven to use this case.

NOTE: A byte address of a doubleword can have the value 0, 1, 2, 3, 4, 5, 6, or 7.

This section contains the legends for terms to be used in the timing formulas for System/360.

ABV = Absolute value (i.e., unsigned value) of $NWBL_1 - NWBL_2$

B = Total number of bytes of the first operand which are processed (applies to instructions with a single-length field)

E = Time for the subject instruction which is executed by the Execute instruction

ED = External delay

F = Input/output field length specified in Transfer I/O instruction

F_1 = 1 if the branch operation is successful
= 0 otherwise

F_2 = 0 if the R_2 field (specified in the RR formatted branch instruction) is zero (i.e., branch is suppresssed)
= 1 otherwise

G_1 = 1 if an overflow interruption occurs (PSW bit 36 = 1 or fixed-point divide interruption occurs
= 0 otherwise

G_2 = 1 if overflow occurs and fixed-point interruption is masked (PSW bit 36 = 0)
= 0 otherwise

G_3 = 0 if operand to be converted is positive
= 1 otherwise

G_4 = 1 if condition code is zero; i.e., all of the selected bits are zero or mask is all zero
= 0 otherwise

G_5 = 0 if first operand is positive
= 1 otherwise

GR = Number of general registers loaded or stored

HB_1 = 1 if the address of the high-order (leftmost) byte of the first operand is odd
= 0 otherwise

HB_2 = 1 if the address of the high-order (leftmost) byte of the second operand is odd
= 0 otherwise

H = number of significant (i.e., other than high-order zeros) hexadecimal digits in the binary operand

H_2 = Number of high-order hexadecimal zeros in the second operand

H_3 = $H_2/2$ if H_2 is even
= $H_2/2 + 1$ if H_2 is odd

H_4 = $4 - H/2$ if H is even
= $4 - \frac{H-1}{2}$ if H is odd

(H_4 has a minimum value of 1)

K_1 = Number of zero-hexadecimal digits (both leading and imbedded) in the absolute value (recomplemented if negative) of the factor with a smaller absolute value. In Multiply Halfword K_1 applies only to the 16 low-order bits of that factor

L_1 = 1 if a guard digit is involved
= 0 otherwise

LB_1 = 1 if the address of the low-order (rightmost) byte of the first operand is odd
= 0 otherwise

LB_2 = 1 if the address of the low-order (rightmost) byte of the second operand is odd
= 0 otherwise

M = greater of N_1 or N_2

MK = number of times the mark address is stored in the Edit and Mark instruction

MQ_1 = 0 if multiplier or quotient lies on a word boundary
= 1 otherwise

N = total number of bytes in the first operand for those instructions with a single length field

N_1 = total number of bytes in the first operand (destination)

N_2 = total number of bytes in the second operand (source)

N_3 = total number of bytes which overlap between the first and second operands
= 0 for nonoverlapping fields, and for overlapping fields where the address of the second operand is greater than or equal to ($\geq$) the first operand address

N_4 = total number of field separator characters in the edit pattern

N_5 = total number of control characters in the edit pattern

N_6 = number of bytes of the field which lie outside of that part of the field bounded by double words

$NWBB_1$ = number of word boundary crossovers for that part of the first operand processed

$NWBB_2$ = number of word boundary crossovers for that part of the second operand processed

$NWBL_1$ = number of word boundary crossovers for the first operand (destination)

$NWBL_1L_2$ = number of word boundary crossovers for that part of the first operand which consists of N_2 bytes of high-order zeros

$NWBL_2$ = number of word boundary crossovers for the second operand (source)

$NWBQ_1$ = number of word boundary crossovers for the quotient field

$NWBR_1$ = number of word boundary crossovers for the remainder field

q_4 = quotient found by dividing the number of positions to be shifted by 4

q_8 = quotient found by dividing the number of positions to be shifted by 8

Q_4 = 1 of $q_4 = 0$
= 0 otherwise

QS = smaller of $N_1 - 8$ or $N_1 - N_2$

r_4 = remainder found after dividing the number of positions to be shifted by 4

R_3 = remainder when N is divided by 8

R_4 = 1 if $r_4 = 0$
= 0 otherwise

SG = number of signs in the field to be edited

S_1 = 1 if $r_4 = 3$, or if $q_4 = 0$
= 2 if $r_4 = 3$ and $q_4 = 0$
= 0 otherwise

S_2 = -1 if $r_4 = 0$
= 1 if $r_4 = 1$, and $q_4 = 0$
= 0 otherwise

S_3 = 0 if $r_4 = 0$, and $q_4 \neq 0$
= 1 if $r_4 = 0$, and $q_4 = 0$
= 3 if $r_4 = 1$
= 5 if $r_4 = 2$ or 3

S_4 = 0 if $r_4 = 0$
= 4 if $q_4 = 0$ and $r_4 = 1$, or if $q_4 \neq 0$ and $r_4 = 2$
= 3 if $q_4 = 0$ and $r_4 = 2$, or if $q_4 \neq 0$ and $r_4 = 3$
= 2 if $q_4 = 0$ and $r_4 = 3$
= 5 if $q_4 \neq 0$ and $r_4 = 1$

S_5 = 1 if the even-numbered register is zero
= 0 otherwise

S_6 = 1 if operand is negative
= 0 otherwise

S_7 = 1 if $r_4 \neq 0$ and operand is negative
= 0 otherwise

T_1 = 1 if the result field is recomplemented (i.e., changes sign)
= 0 otherwise

T_2 = 1 if the result field is zero
= 0 otherwise

T_3 = 1 if $N_2 < \frac{1}{2}(N_1 + 1)$
= 0 otherwise

T_4 = 1 if the second operand has leading hexadecimal zeros
= 0 otherwise

T_6 = 0 if $N_2 \leq 4$
= 1 otherwise

T_7 = 0 if $N_1 \leq 8$
= 1 otherwise

T_8 = 0 if fields do not overlap
= 1 otherwise

T_9 = 0 if any nonzero function byte is found
= 1 otherwise

T_{11} = 1 if $N_1 > \frac{1}{2}(N_2 + 1)$
= 0 otherwise

T_{12} = 1 if R_1 field of the Execute instruction is not zero
= 0 otherwise

T_{13} = 0 if $N_2 \geq N_1$
= 1 otherwise

T_{14} = 1 if $NWBL_2 = 0$
= 0 otherwise

T_{15} = 1 if B = N and operands are equal
= 0 otherwise

T_{16} = 0 if $N_1 \geq N_2$
= 1 otherwise

T_{17} = 1 if $N_1 > \frac{N_2}{2}$
= 0 otherwise

T_{18} = 1 if N = 1
= 0 otherwise

T_{19} = 1 if $N_1 > 2N_2$
= 0 otherwise

T_{20} = 1 if signs are unlike for Add Decimal or if signs are alike for Subtract Decimal, when second operand > first operand
= 0 otherwise

U_1 = select out delay plus device delay

U_2 = device delay for halt I/O sequence

V = absolute value (i.e., unsigned value) of $N_1 - N_2$

X = number of binary 1's in the fraction of the number to be halved

W = total number of doublewords in the first operand for those instructions with a single length field

INPUT/ OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			SELECTOR CHANNEL			MULTIPLEXER CHANNEL						
						1	2	3	PRIORITY LOAD			WAIT-ING	DEVICE	PREV-IOUS	CPU	PRIORITY LOAD		
				DATA LOAD	DC LOAD	DC NODC	DC DC	DC&T ANY	TIME	A	B	TIME	LOAD	LOAD	INTF	TIME	A	B
Consoles																		
1052 Ptrkbd	2M	14.8cs	Var	....	....	....	....	....	.....	.....	.....	70.0	.034	.143	28.0	.200	5.63	.....
																70.0	3.06	.037
Punched Card I/O and Printers																		
1442-N1 Reading EBCD	1M	.53kb	150 ms	0.3	0.4	1.0	1.5	1.9	.200	.....	0.31	.800	4.20	12.5	39.0	.200	7.05	7.55
									2.80	0.48	0.14					2.80	17.3	3.90
Card Image	1M	1.07kb	150 ms						.200	.....	0.62	.800	5.90	12.5	26.5	.200	7.05	7.55
									2.80	0.95	0.28					2.80	13.4	5.30
Punching EBCD	2M	.12kb	656 ms	0.1	0.0	0.0	0.0	0.0	.200	0.75	0.01	11.0	0.30	0.90	39.0	.200	8.56	.....
																12.5	.....	0.65
Card Image	2M	.24kb	656 ms	0.1	0.0	0.0	0.0	0.0	.200	0.75	0.02	11.0	0.43	0.90	26.5	.200	8.56	.....
																12.5	.....	0.98
1442-N2 Punching		Same as 1442-N1 Punching																
1443-N1 Printer																		
13 Char Set	3M	1.44kc	100 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	10.6	18.5	25.8	0.54	29.6	.200	.....	100.
									1.70	18.0	.....					4.77	477.	.....
									100.	.....	0.19					100.	454.	4.77
39 Char Set	3M	.72kc	200 ms	0.0	0.0	0.0	0.0	0.0	.200	....	10.6	18.5	25.8	0.54	29.6	.200	.....	100.
									1.70	18.0	.....					4.77	477.	.....
									200.	.....	.095					200.	466.	2.38
52 Char Set	3M	.58kc	250 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	10.6	18.5	25.8	0.54	29.6	.200	.....	100.
									1.70	18.0	.....					4.77	477.	.....
									250.	.....	.076					250.	468.	1.90
63 Char Set	3M	.48kc	300 ms	0.0	0.0	0.0	0.0	0.0	.200	....	10.6	18.5	25.8	0.54	29.6	.200	.....	100.
									1.70	18.0	.....					4.77	477.	.....
									300.	.....	.063					300.	469.	1.59

Key:
1– May be overrun
2– Will not overrun – Synchronous mechanical operation
3– Will not overrun – Asynchronous operation
–B Burst mode operation on multiplexer channel
–M Multiplex mode operation on multiplexer channel

Table 1. IBM System/360 Model 40 Channel Evaluation Factors

INPUT/ OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			SELECTOR CHANNEL			MULTIPLEXER CHANNEL						
						1	2	3	PRIORITY LOAD			WAIT-ING		PREV-IOUS		PRIORITY LOAD		
				DATA	DC	DC	DC	DC&T					DEVICE		CPU			
				LOAD	LOAD	NODC	DC	ANY	TIME	A	B	TIME	LOAD	LOAD	INTF	TIME	A	B
2821 Ctrl Unit																		
2540 Card Read Punch																		
51 Col Rd EBCD	2M	1.07kb	75 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	8.00	21.8	1.22	21.0	.200	.....	100.
									.480	10.0	.....					1.75	175.	.....
									75.0	9.95	0.13					75.0	171.	2.34
Column Binary	2M	2.13kb	75 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	8.00	42.8	1.22	21.0	.200	.....	100.
									.960	20.0	.....					3.42	342.	.....
									75.0	19.8	0.27					75.0	326.	4.56
Std Read EBCD	2M	1.33kb	60 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	6.50	26.9	1.50	21.0	.200	.....	100.
									.480	10.0	.....					1.75	175.	.....
									60.0	9.94	0.16					60.0	170.	2.90
Column Binary	2M	2.67kb	60 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	6.50	52.6	1.50	21.0	.200	.....	100.
									.960	20.0	.....					3.42	342.	.....
									60.0	19.7	0.33					60.0	324.	5.70
Punch EBCD	2M	.33kb	200 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	14.0	14.1	0.70	23.7	.200	.....	100.
									.480	10.0	.....					1.98	198.	.....
									200.	9.98	0.05					200.	196.	0.90
Column Binary	2M	.67kb	200 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	21.0	14.0	27.7	0.70	23.7	.200	.....	100.
									.960	20.0	.....					3.88	388.	.....
									200.	19.9	0.10					200.	381.	1.94
1403 Ptr Model 2 Std 600 LPM	3M	1.32kc	100 ms	0.0	0.0	0.0	0.0	0.0	.200	....	25.0	15.7	14.4	0.64	16.5	.200	.....	100.
									.660	16.5	.....					2.26	226.	.....
									100.	16.4	0.16					100.	221.	2.26
UCS 750 LPM	3M	1.65kc	80 ms	0.0	0.0	0.0	0.0	0.0	.200	....	25.0	15.7	14.4	0.64	16.5	.200	.....	100.
									.660	16.5	.....					2.26	226.	.....
									80.0	16.4	0.21					80.0	219	2.83
Mdl 3&N1 Std 1100 LPM	3M	2.42kc	54.5 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	25.0	15.7	14.4	0.64	16.5	.200	.....	100.
									.660	16.5	.....					2.26	226.	.....
									54.5	16.3	0.30					54.5	216	4.10
UCS 1400 LPM	3M	3.08kc	42.8 ms	0.0	0.0	0.0	0.0	0.0	.200	.....	25.0	15.7	14.4	0.64	16.5	.200	.....	100.
									.660	16.5	.....					2.26	226.	.....
									42.8	16.3	0.38					42.8	214.	5.30

Key:
1— May be overrun
2— Will not overrun — Synchronous mechanical operation
3— Will not overrun — Asynchronous operation
—B Burst mode operation on multiplexer channel
—M Multiplex mode operation on multiplexer channel

Table 1. (continued)

INPUT/OUTPUT DEVICE			KEY	NOMINAL DATA RATE	GAP OR CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			PRIORITY LOAD								
											NO DATA CHAINING			DATA CHAINING					
														COUNT = 20			COUNT = 100		
						DATA LOAD	DC LOAD	1 DC NODC	2 DC DC	3 DC&T ANY	TIME	A	B	TIME	A	B	TIME	A	B
2400 SERIES MAGNETIC TAPE READING																			
MDL	DEN-SITY	BYTE CONV			GAP TIME														
1	200	No	1B	7.5kc	20.0ms	1.3	1.3	3.1	4.7	6.0	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											2.56	.....	0.94	1.03	1.05	1.31	1.34	1.05	1.01
		Yes	1B	5.6kb	20.0ms	1.3	1.3	3.1	4.7	6.0	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											3.43	.....	0.70	1.77	1.05	0.98	.355	1.05	0.76
	556	No	1B	20.8kc	20.0ms	3.5	3.6	8.6	13.2	16.8	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											.923	.....	2.60	.355	1.02	3.64	.449	1.03	2.81
		Yes	1B	15.6kb	20.0ms	3.5	3.6	8.6	13.2	16.8	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											1.28	.....	1.95	.502	1.03	2.73	.645	1.04	2.11
	800	No*	1B	30.0kb	16.0ms	5.1	5.3	12.7	19.4	24.7	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											.640	.....	3.75	.267	1.00	5.25	.341	1.02	4.05
		Yes	1B	22.5kb	20.0ms	5.1	5.3	12.7	19.4	24.7	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											.854	.....	2.81	.352	1.02	3.93	.452	1.03	3.03
2	200	No	1B	15.0kc	10.0ms	2.6	2.7	6.3	9.6	12.3	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											1.28	.....	1.88	.523	1.03	2.62	.674	1.04	2.02
		Yes	1B	11.3kb	10.0ms	2.6	2.7	6.3	9.6	12.3	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											1.70	.....	1.41	.690	1.04	1.97	.895	1.04	1.52
	556	No	1B	41.7kc	10.0ms	7.1	7.5	17.8	27.2	34.6	.200	2.40	.....	.200	0.98	7.29	.200	2.40	.....
											.461	.....	5.21				.248	1.00	5.65
		Yes	1B	31.3kb	10.0ms	7.1	7.5	17.8	27.2	34.6	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											.614	.....	3.91	.256	1.00	5.47	.327	1.02	4.22
	800	No*	1B	60.0kb	8.0ms	10.2	11.0	26.1	39.9	50.9	.200	2.40	.....	.200	0.95	10.5	.200	0.98	8.10
											.320	.....	7.50						
		Yes	1B	45.0kb	10.0ms	10.2	11.0	26.1	39.9	50.9	.200	2.40	.....	.200	0.98	7.88	.200	2.40	.....
											.426	.....	5.63				.230	1.00	6.08
3	200	No	1B	22.5kc	6.7ms	3.8	4.0	9.4	14.3	18.3	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											.854	.....	2.81	.352	1.02	3.93	.450	1.03	3.04
		Yes	1B	16.9kb	6.7ms	3.8	4.0	9.4	14.3	18.3	.200	2.40	.....	.200	2.40	.....	.200	2.40	.....
											1.14	.....	2.11	.464	1.03	2.95	.597	1.04	2.28
	556	No	1B	62.5kc	6.7ms	10.6	11.5	27.3	41.7	53.2	.200	2.40	.....	.200	0.95	10.9	.200	0.97	8.44
											.307	.....	7.81						
		Yes	1B	46.9kb	6.7ms	10.6	11.5	27.3	41.7	53.2	.200	2.40	.....	.200	0.98	8.2	.200	2.40	.....
											.410	.....	5.86				.221	1.00	6.33
	800	No*	1B	90.0kb	5.3ms	15.3	17.2	40.7	62.2	79.3	.200	2.40	.....	.200	0.90	15.8	.200	0.94	12.2
											.213	.....	11.3						
		Yes	1B	67.5kb	6.7ms	15.3	17.2	40.7	62.2	79.3	.200	2.40	.....	.200	0.94	11.8	.200	0.97	9.13
											.284	.....	8.44						

*Gap time nine track only
Loads for seven or nine track

Key:
1– May be overrun
–B Burst mode operation on multiplexer channel

Table 1. (continued)

INPUT/OUTPUT DEVICE			KEY	NOMINAL DATA RATE	GAP OR CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			PRIORITY LOAD								
											NO DATA CHAINING			DATA CHAINING					
														COUNT = 20			COUNT = 100		
						DATA LOAD	DC LOAD	1 DC NODC	2 DC DC	3 DC&T ANY	TIME	A	B	TIME	A	B	TIME	A	B
WRITING																			
MDL	DEN-SITY	BYTE CONV																	
1	200	No	1B	7.5kc	20.0ms	1.3	1.3	3.1	4.7	6.0	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											3.36	.....	0.94	1.60	1.05	1.31	2.08	1.05	1.02
		Yes	1B	5.6kb	20.0ms	1.3	1.3	3.1	4.7	6.0	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											4.50	.....	0.70	2.14	1.05	0.98	2.75	1.05	0.76
	556	No	1B	20.8kc	20.0ms	3.5	3.6	8.6	13.2	16.8	.200	3.15	....	.200	3.15	....	.200	3.15	.....
											1.21	.....	2.60	.548	1.42	3.89	.695	1.03	3.05
		Yes	1B	15.6kb	20.0ms	3.5	3.6	8.6	13.2	16.8	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											1.62	.....	1.95	.777	1.03	2.73	1.00	1.04	2.11
	800	No*	1B	30.0kb	16.0ms	5.1	5.3	12.7	19.4	24.7	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.840	.....	3.75	.410	1.00	5.25	.527	1.02	4.04
		Yes	1B	22.5kb	20.0ms	5.1	5.3	12.7	19.4	24.7	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											1.12	.....	2.81	.541	1.02	3.93	.700	1.03	3.43
2	200	No	1B	15.0kc	10.0ms	2.6	2.7	6.3	9.6	12.3	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											1.68	.....	1.88	.810	1.03	2.62	1.04	1.04	2.02
		Yes	1B	11.3kb	10.0ms	2.6	2.7	6.3	9.6	12.3	.200	3.15	....	.200	3.15	.....	.200	3.15	.....
											2.23	.....	1.41	1.06	1.04	1.97	1.37	1.04	1.52
	556	No	1B	41.7kc	10.0ms	7.1	7.5	17.8	27.2	34.6	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.605	.....	5.21	.298	0.98	7.29	.382	1.00	5.63
		Yes	1B	31.3kb	10.0ms	7.1	7.5	17.8	27.2	34.6	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.806	....	3.91	.393	1.00	5.47	.505	1.02	4.22
	800	No*	1B	60.0kb	8.0ms	10.2	11.0	26.1	39.9	50.9	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.420	.....	7.50	.210	0.95	10.5	.268	0.98	8.10
		Yes	1B	45.0kb	10.0ms	10.2	11.0	26.1	39.9	50.9	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.560	.....	5.63	.275	0.98	7.88	.354	1.00	6.08
3	200	No	1B	22.5kc	6.7ms	3.8	4.0	9.4	14.3	18.3	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											1.12	.....	2.81	.542	1.02	3.93	.697	1.03	3.04
		Yes	1B	16.9kb	6.7ms	3.8	4.0	9.4	14.3	18.3	.204	3.15	....	.200	3.15	.....	.200	3.15	.....
											1.49	.....	2.11	.719	1.03	2.95	.925	1.04	2.28
	556	No	1B	62.5kc	6.7ms	10.6	11.5	27.3	41.7	53.2	.200	3.15	.....	.202	0.95	10.9	.200	3.15	.....
											.403	.....	7.81				.258	0.97	8.44
		Yes	1B	46.9kb	6.7ms	10.6	11.5	27.3	41.7	53.2	.200	3.15	.....	.200	3.15	.....	.200	3.15	.....
											.538	.....	5.86	.255	0.98	8.24	.340	1.00	6.33
	800	No*	1B	90.0kb	5.3ms	15.3	17.2	40.7	62.2	79.3	.200	3.15	.....	.200	0.95	15.8	.200	0.94	12.2
											.280	.....	11.3						
		Yes	1B	67.5kb	6.7ms	15.3	17.2	40.7	62.2	79.3	.200	3.15	....	.200	0.94	11.8	.200	3.15	.....
											.373	.....	8.45				.243	0.93	9.13

*Gap time nine track only
Loads for seven or nine track

Key:
1– May be overrun
–B Burst mode operation on multiplexer channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	GAP OR CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			PRIORITY LOAD								
									NO DATA CHAINING			DATA CHAINING					
												COUNT = 20			COUNT =100		
				DATA LOAD	DC LOAD	1 DC NODC	2 DC DC	3 DC&T ANY	TIME	A	B	TIME	A	B	TIME	A	B
2400 SERIES MAGNETIC TAPE																	
MDL DEN- SITY READING	BYTE CONV					GAP TIME											
4 800	#	1B	30kb	5.1	5.3	12.7	19.4	24.7	.200	2.40	0	.200	2.4	0	.200	2.4	0
									.640	0	3.75	.267	1.0	5.25	.346	1.0	4.1
1600	#	1B	60kb	10.2	11.0	26.1	39.9	50.9	.200	2.40	0	.200	1.0	10.5	.200	1.0	8.1
									.320	0	7.5	0	0	0	0	0	0
5 800	#	1B	60kb	8.0ms	10.2	11.0	26.1	39.9	50.9	.200	2.40	0	.200	1.0	10.5	.200	1.0	8.1
									.320	0	7.5	0	0	0	0	0	0
1600	#	1B	120kb	8.0ms	20.4	23.9	56.8	86.6	**	.200	0	15.0	.200	1.0	21.0	.200	1.0	16.2
6 800	#	1B	90kb	5.3ms	15.3	17.2	40.7	62.2	79.3	.200	0	11.3	.200	1.0	15.8	.200	1.0	12.2
1600	#	1B	180kb	5.3ms	30.6	39.1	**	**	**	.200	0	22.5	.200	1.0	31.5	.200	1.0	24.3
WRITING																	
4 800									.200	3.15	0	.200	3.15	0	.200	3.15	0
									.840	0	3.75	.410	1.0	5.25	.530	1.0	4.1
1600									.200	3.15	0	.210	1.0	10.5	.200	3.15	0
									.420	0	7.5	0	0	0	.265	1.0	8.1
5 800		(All data same as for reading)							.200	3.15	0	.200	1.0	10.5	.200	3.15	0
									.420	0	7.5	0	0	0	.265	1.0	8.1
1600									.200	0	15.0	2.00	1.0	21.0	.200	1.0	16.2
6 800									.200	3.15	0	.200	1.0	15.8	.200	1.0	12.2
									.280	0	11.3	0	0	0	0	0	0
1600									.200	0	22.5	.200	1.0	31.5	.200	1.0	24.3

Data conversion not used on this model
** Exceeds system load limit

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	GAP OR CYCLE TIME	CHANNEL LOAD		SYSTEM LOAD			PRIORITY LOAD								
						1	2	3	NO DATA CHAINING			DATA CHAINING					
												COUNT =20			COUNT = 100		
				DATA LOAD	DC LOAD	DC NODC	DC DC	DC&T ANY	TIME	A	B	TIME	A	B	TIME	A	B
Direct Access Storage			*Rotatn Time*														
2302 Disk Storage Models 3 and 4	1B	156kb	34.0ms	20.1	30.1	71.3	**	**									
2303 Drum	1C	303.8kb	17.5ms	39.1	**	**	**	**									
2311 Disk Storage Drive Model 1	1B	156kb	25.0ms	20.3	30.4	72.1	**	**	.200	3.40	21.3	.200	1.60	28.9	.200	3.40	21.3
									.8	2.80	20.3				.8	1.06	22.0
2314 Direct Access Storage Facility	1C	312kb	25.0ms	40.9	**	**	**	**	.200	2.05	41.5						
									.8	1.17	40.9						
2321 Data Cell Drive	1B	54.7kb	50.0ms	7.3	10.2	24.2	36.9	47.0									

**Exceeds system load limit

Key:
1– May be overrun
–B Burst mode operation on multiplexer channel
–C Selector channel only

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl IBM Term Ctl-I 75 bps	1M	8.3cps	29.6	116.	.016	.086	.200	6.15	.020	1	116.	0.16	.086	.200	6.15	.020
				58.1	.033	.172	.200	5.41	12.0	2	57.5	.033	.174	.200	5.78	6.01
							.573	12.3	.040					1.09	12.3	.040
				38.4	.049	.261	.200	5.41	12.0	3	38.7	.049	.259	.200	5.78	6.01
							1.09	18.4	.060					2.11	18.3	.060
				28.8	.066	.347	.200	5.41	12.0	4	28.8	.066	.348	.200	5.78	6.01
							1.60	24.5	.080					3.13	24.3	.080
				23.0	.083	.434	.200	5.41	12.0	5	22.8	.083	.439	.200	5.78	6.01
							2.11	30.5	.100					4.16	30.3	.100
				19.2	.099	.521	.200	5.41	12.0	6	18.8	.101	.531	.200	5.78	6.01
							2.62	36.6	.120					5.18	36.3	.120
				16.3	.117	.613	.200	5.41	12.0	7	15.9	.120	.631	.200	5.78	6.01
							3.13	42.6	.140					6.21	42.2	.140
				14.4	.132	.695	.200	5.41	12.0	8	13.9	.137	.721	.200	5.78	6.01
							3.65	48.6	.160					7.23	48.0	.160
				12.5	.152	.802	.200	5.41	12.0	9	12.9	.148	.776	.200	5.78	6.01
							4.16	54.6	0.18					8.25	53.9	.180
				11.5	.165	.869	.200	5.41	12.0	10	10.9	.174	.918	.200	5.78	6.01
							4.67	60.6	.200					9.28	59.6	.200
				10.5	.180	.948	.200	5.41	12.0	11	9.90	.192	1.01	.200	5.78	6.01
							5.18	66.5	.220					10.3	65.4	.220
				9.58	.198	1.04	.200	5.41	12.0	12	8.91	.213	1.12	.200	5.78	6.01
							5.69	72.4	.240					11.3	71.1	.240
				8.62	.220	1.16	.200	5.41	12.0	13	8.91	.213	1.12	.200	5.78	6.01
							6.21	78.3	.260					12.3	76.7	.260
				8.14	.233	1.23	.200	5.41	12.0	14	7.92	.240	1.26	.200	5.78	6.01
							6.72	84.2	.280					13.4	82.4	.280
				7.66	.248	1.31	.200	5.41	12.0	15	6.93	.274	1.44	.200	5.78	6.01
							7.23	90.1	.300					14.4	87.9	.300
										16	6.93	.274	1.44	.200	5.78	6.01
														15.4	93.5	.320
										17	5.94	.320	1.69	.200	5.78	6.01
														16.4	99.0	.340
										18	5.94	.320	1.69	.200	5.78	6.01
														17.5	104.	.360
										19	5.94	.320	1.69	.200	5.78	6.01
														18.5	110.	.380
										20	4.94	.384	2.02	.200	5.78	6.01
														19.5	115.	.400
										21	4.94	.384	2.02	.200	5.78	6.01
														20.5	121.	.420
										22	4.94	.384	2.02	.200	5.78	6.01
														21.6	126.	.440
										23	4.94	.384	2.02	.200	5.78	6.01
														22.6	131.	.460
										24	3.95	.481	2.53	.200	5.78	6.01
														23.6	136.	.480
										25	3.95	.481	2.53	.200	5.78	6.01
														24.6	141.	.500
										26	3.95	.481	2.53	.200	5.78	6.01
														25.7	147.	.520
										27	3.95	.481	2.53	.200	5.78	6.01
														26.7	152.	.540
										28	3.95	.481	2.53	.200	5.78	6.01
														27.7	157.	.560
										29	3.95	.481	2.53	.200	5.78	6.01
														28.7	162.	.580
										30	2.96	.642	3.38	.200	5.78	6.01
														29.8	167.	.600
										31	2.96	.642	3.38	.200	5.78	6.01
														30.8	172.	.620

Key: 1– May be overrun –M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORTY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl IBM Term Ctl-I 75 bps (with autopolling)	IM	8.3cps	29.6	116.	.053	.086	.200	6.12	.452	1	116.	.053	.086	.200	6.14	.204
							.482	6.33	.020					.994	6.32	.020
				58.1	.106	.172	.200	5.41	12.0	2	57.5	.107	.174	.200	5.78	6.01
							.577	12.1	.371					1.09	12.1	.186
							1.47	12.6	.040					3.01	12.6	.040
				38.4	.160	.261	.200	5.41	12.0	3	38.7	.159	.259	.200	5.78	6.01
							1.09	18.1	.371					2.11	18.1	.186
							2.47	18.9	.060					5.03	18.7	.060
				28.8	.214	.347	.200	5.41	12.0	4	28.8	.214	.348	.200	5.78	6.01
							1.60	24.1	.371					3.14	24.1	.186
							3.46	25.1	.080					7.04	24.8	.080
				23.0	.267	.434	.200	5.41	12.0	5	22.8	.270	.439	.200	5.78	6.01
							2.12	30.0	.371					4.16	30.0	.186
							4.45	31.3	.100					9.06	30.8	.100
				19.2	.321	.521	.200	5.41	12.0	6	18.8	.327	.531	.200	5.78	6.01
							2.63	36.0	.371					5.19	36.0	.186
							5.44	37.4	.120					11.1	36.7	.120
				16.3	.377	.613	.200	5.41	12.0	7	15.9	.388	.631	.200	5.78	6.01
							3.14	42.0	.371					6.21	42.0	.186
							6.43	43.5	.140					13.1	42.5	.140
				14.4	.428	.695	.200	5.41	12.0	8	13.9	.443	.721	.200	5.78	6.01
							3.66	48.0	.371					7.24	47.9	.186
							7.43	49.5	.160					15.1	48.3	.160
				12.5	.493	.802	.200	5.41	12.0	9	12.9	.477	.776	.200	5.78	6.01
							4.17	53.9	.371					8.26	53.9	.186
							8.42	55.5	.180					17.1	54.0	.180
				11.5	.535	.869	.200	5.41	12.0	10	10.9	.564	.918	.200	5.78	6.01
							4.68	59.9	.371					9.29	59.8	.186
							9.41	61.5	.200					19.1	59.6	.200
				10.5	.583	.948	.200	5.41	12.0	11	9.90	.621	1.01	.200	5.78	6.01
							5.19	65.9	.371					10.3	65.8	.186
							10.4	67.5	.220					21.2	65.1	.220
				9.58	.642	1.04	.200	5.41	12.0	12	8.91	.690	1.12	.200	5.78	6.01
							5.71	71.9	.371					11.3	71.8	.186
							11.4	73.3	.240					23.2	70.5	.240
				8.62	.713	1.16	.200	5.41	12.0	13	8.91	.690	1.12	.200	5.78	6.01
							6.22	77.8	.371					12.4	77.7	.186
							12.4	79.2	.260					25.2	75.9	.260
				8.14	.755	1.23	.200	5.41	12.0	14	7.92	.777	1.26	.200	5.78	6.01
							6.73	83.8	.371					13.4	83.7	.186
							13.4	85.0	.280					27.2	81.1	.280
				7.66	.802	1.31	.200	5.41	12.0	15	6.93	.888	1.44	.200	5.78	6.01
							7.25	89.8	.371					14.4	89.7	.186
							14.4	90.8	.300					29.2	86.3	.300
										16	6.93	.888	1.44	.200	5.78	6.01
														15.4	95.6	.186
														31.2	91.4	.320
										17	5.94	1.04	1.68	.200	5.78	6.01
														16.5	102.	.186
														33.3	96.5	.340
										18	5.94	1.04	1.68	.200	5.78	6.01
														17.5	108.	.186
														35.3	101.	.360
										19	5.94	1.04	1.68	.200	5.78	6.01
														18.5	114.	.186
														37.3	106.	.380
										20	4.94	1.24	2.02	.200	5.78	6.01
														19.5	120.	.186
														39.3	111.	.400

Key: 1– May be overrun —M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl IBM Term Ctl-I 75 bps (with autopolling)	IM	8.3cps	29.6							21	4.94	1.24	2.02	.200	5.78	6.01
														40.6	125.	.186
														41.3	116.	.420
										22	4.94	1.24	2.02	.200	5.78	6.01
														21.6	131.	.186
														43.3	120.	.440
										23	4.94	1.24	2.02	.200	5.78	6.01
														22.6	137.	.186
														45.3	125.	.460
										24	3.95	1.56	2.53	.200	5.78	6.01
														23.6	143.	.186
														47.4	129.	.480
										25	3.95	1.56	2.53	.200	5.78	6.01
														24.7	149.	.186
														49.4	134.	.500
										26	3.95	1.56	2.53	.200	5.78	6.01
														25.7	155.	.186
														51.4	138.	.520
										27	3.95	1.56	2.53	.200	5.78	6.01
														26.7	161.	.186
														53.4	142.	.540
										28	3.95	1.56	2.53	.200	5.78	6.01
														27.7	167.	.186
														55.4	146.	.560
										29	3.95	1.56	2.53	.200	5.78	6.01
														28.8	173.	.186
														57.4	151.	.580
										30	2.96	2.08	3.38	.200	5.78	6.01
														29.8	179.	.186
														59.5	155.	.600
										31	2.96	2.08	3.38	.200	5.78	6.01
														30.8	185.	.186
														61.5	158.	.620

Key: 1– May be overrun –M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
Communication Equipment																
2702 Transmission Ctl IBM Term Ctl-I 135.5 bps	1M	14.8cps	29.6	66.7	0.28	.150	.200	6.15	.035	1	66.4	.029	.150	.200	6.15	.035
				33.1	.057	.302	.200	5.41	12.0	2	32.7	.058	.306	.200	5.78	6.01
							.573	12.3	.070					1.09	12.2	.070
				22.1	.086	.453	.200	5.41	12.0	3	21.8	.087	.459	.200	5.78	6.01
							1.09	18.3	.105					2.11	18.2	.105
				16.3	.117	.613	.200	5.41	12.0	4	15.9	.120	.631	.200	5.78	6.01
							1.60	24.4	.140					3.13	24.2	.140
				12.9	.147	.773	.200	5.41	12.0	5	12.9	.148	.776	.200	5.78	6.01
							2.11	30.4	.175					4.16	30.0	.175
				11.0	.172	.907	.200	5.41	12.0	6	10.9	.174	.918	.200	5.78	6.01
							2.62	36.3	.210					5.18	35.8	.210
				9.10	.209	1.10	.200	5.41	12.0	7	8.91	.213	1.12	.200	5.78	6.01
							3.13	42.3	.245					6.21	41.5	.245
				8.14	.233	1.23	.200	5.41	12.0	8	7.92	.240	1.26	.200	5.78	6.01
							3.65	48.2	.280					7.23	47.2	.280
				7.18	.264	1.39	.200	5.41	12.0	9	6.93	.274	1.44	.200	5.78	6.01
							4.16	54.0	.315					8.25	52.8	.315
				6.22	.305	1.61	.200	5.41	12.0	10	5.9	.320	1.69	.200	5.78	6.01
							4.67	59.9	.350					9.28	58.3	.350
				5.74	.331	1.74	.200	5.41	12.0	11	5.94	.320	1.69	.200	5.78	6.01
							5.18	65.7	.385					10.3	63.7	.385
				5.26	.361	1.90	.200	5.41	12.0	12	4.94	.384	2.02	.200	5.78	6.01
							5.69	71.4	.420					11.3	69.0	.420
				4.78	.397	2.09	.200	5.41	12.0	13	4.94	.384	2.02	.200	5.78	6.01
							6.21	77.1	.455					12.3	74.3	.455
				4.30	.441	2.32	.200	5.41	12.0	14	3.95	.481	2.53	.200	5.78	6.01
							6.72	82.8	.490					13.4	79.5	.490
				4.30	.441	2.32	.200	5.41	12.0	15	3.95	.481	2.53	.200	5.78	6.01
							7.23	88.5	.525					14.4	84.7	.525
										16	3.95	.481	2.53	.200	5.78	6.01
														15.4	89.8	.560
										17	2.96	.642	3.38	.200	5.78	6.01
														16.4	94.8	.595
										18	2.96	.642	3.38	.200	5.78	6.01
														17.5	99.7	.630
										19	2.96	.642	3.38	.200	5.78	6.01
														18.5	105.	.665
										20	2.96	.642	3.38	.200	5.78	6.01
														19.5	109.	.700
										21	2.96	.642	3.38	.200	5.78	6.01
														20.5	114.	.735
										22	2.96	.642	3.38	.200	5.78	6.01
														21.6	119.	.770
										23	1.97	.965	5.08	.200	5.78	6.01
														22.6	123.	.805
										24	1.97	.965	5.08	.200	5.78	6.01
														23.6	128.	.840
										25	1.97	.965	5.08	.200	5.78	6.01
														24.6	132.	.875
										26	1.97	.965	5.08	.200	5.78	6.01
														25.7	137.	.910
										27	1.97	.965	5.08	.200	5.78	6.01
														26.7	141.	.945
										28	1.97	.965	5.08	.200	5.78	6.01
														27.7	145.	.980
										29	1.97	.965	5.08	.200	5.78	6.01
														28.7	149.	1.02
										30	1.97	.965	5.08	.200	5.78	6.01
														29.8	153.	1.05
										31	1.97	.965	5.08	.200	5.78	6.01
														30.8	157.	1.09

Key: 1– May be overrun –M Multiplex mode operation on Mutltiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl IBM Term Ctl-I 135.5 bps (with autopolling)	IM	14.8cps	29.6	66.7	.092	.150	.200	6.12	.452	1	66.4	.093	.150	.200	6.14	.204
							.482	6.32	.035					.994	6.31	.035
				33.1	.186	.302	.200	5.41	12.0	2	32.7	.188	.306	.200	5.78	6.01
							.577	12.1	.371					1.09	12.1	.186
							1.47	12.6	.070					3.01	12.5	.070
				22.1	.279	.453	.200	5.41	12.0	3	21.8	.282	.459	.200	5.78	6.01
							1.09	18.1	.371					2.11	18.1	.186
							2.47	18.8	.105					5.03	18.5	.105
				16.3	.377	.613	.200	5.41	12.0	4	19.9	.388	.631	.200	5.78	6.01
							1.60	24.1	.371					3.14	24.1	.186
							3.46	24.9	.140					7.04	24.4	.140
				12.9	.475	.773	.200	5.41	12.0	5	12.9	.477	.776	.200	5.78	6.01
							2.12	30.0	.371					4.16	30.0	.186
							4.45	30.9	.175					9.06	30.1	.175
				11.0	.558	.907	.200	5.41	12.0	6	10.9	.564	.918	.200	5.78	6.01
							2.63	36.0	.371					5.19	36.0	.186
							5.44	36.9	.210					11.1	35.7	.210
				9.10	.676	1.10	.200	5.41	12.0	7	8.91	.690	1.12	.200	5.78	6.01
							3.14	42.0	.371					6.21	42.0	.186
							6.43	42.8	.245					13.1	41.2	.245
				8.14	.755	1.23	.200	5.41	12.0	8	7.92	.777	1.26	.200	5.78	6.01
							3.66	48.0	.371					7.24	47.9	.186
							7.43	48.6	.280					15.1	46.5	.280
				7.18	.856	1.39	.200	5.41	12.0	9	6.93	.888	1.44	.200	5.78	6.01
							4.17	53.9	.371					8.26	53.9	.186
							8.42	54.4	.315					17.1	51.7	.315
				6.22	.988	1.61	.200	5.41	12.0	10	5.94	1.04	1.68	.200	5.78	6.01
							4.68	59.9	.371					9.29	59.8	.186
							9.41	60.1	.350					19.1	56.7	.350
				5.74	1.07	1.74	.200	5.41	12.0	11	5.94	1.04	1.68	.200	5.78	6.01
							5.19	65.9	.371					10.3	65.8	.186
							10.4	65.7	.385					21.2	61.6	.385
				5.26	1.17	1.90	.200	5.41	12.0	12	4.94	1.24	2.02	.200	5.78	6.01
							5.71	71.9	.371					11.3	71.8	.186
							11.4	71.3	.420					23.2	66.3	.420
				4.78	1.29	2.09	.200	5.41	12.0	13	4.94	1.24	2.02	.200	5.78	6.01
							6.22	77.8	.371					12.4	77.7	.186
							12.4	76.8	.455					25.2	71.0	.455
				4.30	1.43	2.32	.200	5.41	12.0	14	3.95	1.56	2.53	.200	5.78	6.01
							6.73	83.8	.371					13.4	83.7	.186
							13.4	82.2	.490					27.2	75.4	.490
				4.30	1.43	2.32	.200	5.41	12.0	15	3.95	1.56	2.53	.200	5.78	6.01
							7.25	89.8	.371					14.4	89.7	.186
							14.4	87.6	.525					29.2	79.8	.525
										16	3.95	1.56	2.53	.200	5.78	6.01
														15.4	95.6	.186
														31.2	83.9	.560
										17	2.96	2.08	3.38	.200	5.78	6.01
														16.5	102.	.186
														33.3	88.0	.595
										18	2.96	2.08	3.38	.200	5.78	6.01
														17.5	108.	.186
														35.3	91.9	.630
										19	2.96	2.08	3.38	.200	5.78	6.01
														18.5	114.	.186
														37.3	95.7	.665
										20	2.96	2.08	3.38	.200	5.78	6.01
														19.5	120.	.186
														39.3	99.3	.700

Key: 1– May be overrun —M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl																
IBM Term Ctl-I																
135.5 bps										21	2.96	2.08	3.38	.200	5.78	6.01
(with autopolling)														20.6	125.	.186
														41.3	103.	.735
										22	2.96	2.08	3.38	.200	5.78	6.01
														21.6	131.	.186
														43.3	106.	.770
										23	1.97	3.13	5.08	.200	5.78	6.01
														22.6	137.	.186
														45.3	109.	.805
										24	1.97	3.13	5.08	.200	5.78	6.01
														23.6	143.	.186
														47.4	112.	.840
										25	1.97	3.13	5.08	.200	5.78	6.01
														24.7	149.	.186
														49.4	115.	.875
										26	1.97	3.13	5.08	.200	5.78	6.01
														25.7	155.	.186
														51.4	118.	.910
										27	1.97	3.13	5.08	.200	5.78	6.01
														26.7	161.	.186
														53.4	121.	.945
										28	1.97	3.13	5.08	.200	5.78	6.01
														27.7	167.	.186
														55.4	123.	.980
										29	1.97	3.13	5.08	.200	5.78	6.01
														28.8	173.	.186
														57.4	126.	1.02
										30	1.97	3.13	5.08	.200	5.78	6.01
														29.8	179.	.186
														59.5	128.	1.05
										31	1.97	3.13	5.08	.200	5.78	6.01
														30.8	185.	.186
														61.5	130.	1.09

Key: 1– May be overrun –M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl														(with autopolling)		
IBM Term Ctl-I																
600 bps	1M	66.6cps	29.6	14.4	.132	.695	.200	6.14	.174	1	14.4	.428	.695	.200	6.12	.452
														.482	6.26	.174
				7.18	.264	1.39	.200	5.41	12.0	2	7.18	.856	1.39	.200	5.41	12.0
							.573	12.1	.348					.577	12.1	.371
														1.47	12.2	.348
				4.78	.397	2.09	.200	5.41	12.0	3	4.78	1.29	2.09	.200	5.41	12.0
							1.09	17.9	.522					1.09	18.1	.371
														2.47	17.7	.522
				3.34	.568	2.99	.200	5.41	12.0	4	3.34	1.84	2.99	.200	5.41	12.0
							1.60	23.5	.696					1.60	24.1	.371
														3.46	23.0	.696
				2.86	.663	3.49	.200	5.41	12.0	5	2.86	2.15	3.49	.200	5.41	12.0
							2.11	28.9	.870					2.12	30.0	.371
														4.45	27.8	.870
				2.38	.797	4.20	.200	5.41	12.0	6	2.38	2.58	4.19	.200	5.41	12.0
							2.62	34.2	1.04					2.63	36.0	.371
														5.44	32.4	1.04
				1.90	.998	5.25	.200	5.41	12.0	7	1.90	3.23	5.25	.200	5.41	12.0
							3.13	39.2	1.22					3.14	42.0	.371
														6.43	36.5	1.22
				1.42	1.33	7.02	.200	5.41	12.0	8	1.42	4.32	7.02	.200	5.41	12.0
							3.65	44.1	1.39					3.66	48.0	.371
														7.43	40.4	1.39
				1.42	1.33	7.02	.200	5.41	12.0	9	1.42	4.32	7.02	.200	5.41	12.0
							4.16	48.8	1.57					4.17	53.9	.371
														8.42	43.9	1.57
				1.42	1.33	7.02	.200	5.41	12.0	10	1.42	4.32	7.02	.200	5.41	12.0
							4.67	53.4	1.74					4.68	59.9	.371
														9.41	47.0	1.74
				.944	2.01	10.6	.200	5.41	12.0	11	.944	6.51	10.6	.200	5.41	12.0
							5.18	57.7	1.91					5.19	65.9	.371
														10.4	49.8	1.91
				.944	3.01	10.6	.200	5.41	12.0	12	.944	6.51	10.6	.200	5.41	12.0
							5.69	61.9	2.09					5.71	71.9	.371
														11.4	52.3	2.09
				.944	2.01	10.6	.200	5.41	12.0	13	.944	6.51	10.6	.200	5.41	12.0
							6.21	65.9	2.26					6.22	77.8	.371
														12.4	54.4	2.26
				.944	2.01	10.6	.200	5.41	12.0	14	.944	6.51	10.6	.200	5.41	12.0
							6.72	69.7	2.44					6.73	83.8	.371
														13.4	56.2	2.44
				.944	2.01	10.6	.200	5.41	12.0	15	.944	6.51	10.6	.200	5.41	12.0
							7.23	73.4	2.61					7.25	89.8	.371
														14.4	57.6	2.61
IBM Term Ctl-II	1M	60.0cps	29.6	14.4	.132	.695	.200	6.14	.166	1	14.4	.428	.695	.200	6.12	.452
600 bps														.482	6.26	.166
				7.18	.264	1.39	.200	5.41	12.0	2	7.18	.856	1.39	.200	5.41	12.0
							.573	12.1	.332					.577	12.1	.371
														1.47	12.2	.332
				4.78	.397	2.09	.200	5.41	12.0	3	4.78	1.29	2.09	.200	5.41	12.0
							1.09	17.9	.498					1.09	18.1	.371
														2.47	17.8	.498
				3.34	.568	2.99	.200	5.41	12.0	4	3.34	1.84	2.99	.200	5.41	12.0
							1.60	23.5	.664					1.60	24.1	.371
														3.46	23.1	.664

Key:
1– May be overrun
–M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B	NR OF LA	31 LINE MAXIMUM WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD TIME	A	B
Communication Equipment																
2702 Transmission Ctl														(with autopolling)		
IBM Term Ctl-II																
600 bps				2.86	.663	3.49	.200	5.41	12.0	5	2.86	2.15	3.49	.200	5.41	12.0
							2.11	290.	.830					2.12	30.0	.371
														4.45	28.0	.830
				2.38	.797	4.20	.200	5.41	12.0	6	2.38	2.58	4.19	.200	5.41	12.0
							2.62	34.3	.996					2.63	36.0	.371
														5.44	32.6	.996
				1.90	.998	5.25	.200	5.41	12.0	7	1.90	3.23	5.25	.200	5.41	12.0
							3.13	39.4	1.16					3.14	42.0	.371
														6.43	36.9	1.16
				1.42	1.33	7.02	.200	5.41	12.0	8	1.42	4.32	7.02	.200	5.41	12.0
							3.65	44.4	1.33					3.66	48.0	.371
														7.43	40.9	1.33
				1.42	1.33	7.02	.200	5.41	12.0	9	1.42	4.32	7.02	.200	5.41	12.0
							4.16	49.1	1.49					4.17	53.9	.371
														8.42	44.5	1.49
				1.42	1.33	7.02	.200	5.41	12.0	10	1.42	4.32	7.02	.200	5.41	12.0
							4.67	53.7	1.66					4.68	59.9	.371
														9.41	47.8	1.66
				.944	2.01	10.6	.200	5.41	12.0	11	.944	6.51	10.6	.200	5.41	12.0
							5.18	58.2	1.83					5.19	65.9	.371
														10.4	50.7	1.83
				.944	2.01	10.6	.200	5.41	12.0	12	.944	6.51	10.6	.200	5.41	12.0
							5.69	62.5	1.99					5.71	71.9	.371
														11.4	53.4	1.99
				.944	2.01	10.6	.200	5.41	12.0	13	.944	6.51	10.6	.200	5.41	12.0
							6.21	66.6	2.16					6.22	77.8	.371
														12.4	55.7	2.16
				.944	2.01	10.6	.200	5.41	12.0	14	.944	6.51	10.6	.200	5.41	12.0
							6.72	70.5	2.32					6.73	83.8	.371
														13.4	57.7	2.32
				.944	2.01	10.6	.200	5.41	12.0	15	.944	6.51	10.6	.200	5.41	12.0
							7.23	74.2	2.49					7.25	89.8	.371
														14.4	59.3	2.49

Key:
1– May be overrun
–M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
Communication Equipment																
2702 Transmission Ctl Telegraph Ctl-I 45 bps	1M	6.0cps	29.6	159.	.012	.063	.200	6.15	.013	1	159.	.012	.063	.200	6.15	.013
				79.7	.024	.126	.200	5.41	12.0	2	79.3	.024	.126	.200	5.78	6.01
							.573	12.3	.026					1.09	12.3	.026
				52.8	.036	.189	.200	5.41	12.0	3	52.6	.036	.190	.200	5.78	6.01
							1.09	18.4	.039					2.11	18.4	.039
				39.8	.048	.251	.200	5.41	12.0	4	39.7	.048	.252	.200	5.78	6.01
							1.60	24.5	.052					3.13	24.4	.052
				31.7	.060	.316	.200	5.41	12.0	5	31.7	.060	.315	.200	5.78	6.01
							2.11	30.6	.065					4.16	30.5	.065
				26.4	.072	.379	.200	5.41	12.0	6	25.8	.074	.388	.200	5.78	6.01
							2.62	36.7	.078					5.18	36.5	.078
				22.5	.084	.444	.200	5.41	12.0	7	21.8	.087	.459	.200	5.78	6.01
							3.13	42.8	.091					6.21	42.5	.091
				19.7	.097	.509	.200	5.41	12.0	8	19.8	.096	.504	.200	5.78	6.01
							3.65	48.8	.104					7.23	48.4	.104
				17.3	.110	.579	.200	5.41	12.0	9	16.8	.113	.594	.200	5.78	6.01
							4.16	54.9	.117					8.25	54.4	.117
				15.8	.120	.632	.200	5.41	12.0	10	15.9	.120	.631	.200	5.78	6.01
							4.67	60.9	.130					9.28	60.3	.130
				14.4	.132	.695	.200	5.41	12.0	11	13.9	.137	.721	.200	5.78	6.01
							5.18	66.9	.143					10.3	66.2	.143
				12.9	.147	.773	.200	5.41	12.0	12	12.9	.148	.776	.200	5.78	6.01
							5.69	72.9	.156					11.3	72.0	.156
				12.0	.159	.834	.200	5.41	12.0	13	11.9	.160	.841	.200	5.78	6.01
							6.21	78.9	.169					12.3	77.9	.169
				11.2	.172	.907	.200	5.41	12.0	14	10.9	.174	.918	.200	5.78	6.01
							6.72	84.9	.182					13.4	83.7	.182
				10.5	.180	.948	.200	5.41	12.0	15	9.90	.192	1.01	.200	5.78	6.01
							7.23	90.8	.195					14.4	89.4	.195
										16	8.90	.192	1.01	.200	5.78	6.01
														15.4	95.2	.208
										17	8.91	.213	1.12	.200	5.78	6.01
														16.4	101.	.221
										18	7.92	.240	1.26	.200	5.78	6.01
														17.5	107.	.234
										19	7.92	.240	1.26	.200	5.78	6.01
														18.5	112.	.247
										20	7.92	.240	1.26	.200	5.78	6.01
														19.5	118.	.260
										21	6.93	.274	1.44	.200	5.78	6.01
														20.5	124.	.273
										22	6.93	.274	1.44	.200	5.78	6.01
														21.6	129.	.286
										23	5.94	.320	1.69	.200	5.78	6.01
														22.6	135.	.299
										24	5.94	.320	1.69	.200	5.78	6.01
														23.6	140.	.312
										25	5.94	.320	1.69	.200	5.78	6.01
														24.6	146.	.325
										26	5.94	.320	1.69	.200	5.78	6.01
														25.7	151.	.338
										27	4.94	.384	2.02	.200	5.78	6.01
														26.7	157.	.351
										28	4.94	.384	2.02	.200	5.78	6.01
														27.7	162.	.364
										29	4.94	.384	2.02	.200	5.78	6.01
														28.7	168.	.377
										30	4.94	.384	2.02	.200	5.78	6.01
														29.8	173.	.390
										31	4.94	.384	2.02	.200	5.78	6.01
														30.8	178.	.403

Key: 1– May be overrun –M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
Communication Equipment																
2702 Transmission Ctl																
Telegraph Ctl-I																
57 bps	1M	7.5cps	29.6	125.	.015	.080	.200	6.15	.016	1	125.	.015	.080	.200	6.15	.016
				62.4	.030	.160	.200	5.41	12.0	2	62.5	0.03	0.16	0.20	5.78	6.01
							.573	12.3	.032					1.09	12.3	.032
				41.3	.046	.242	.200	5.41	12.0	3	41.6	.046	.240	.200	5.78	6.01
							1.09	18.4	.048					2.11	18.3	.048
				31.2	.061	.321	.200	5.41	12.0	4	30.7	.062	.325	.200	5.78	6.01
							1.60	24.5	.064					3.13	24.4	.064
				24.9	.076	.401	.200	5.41	12.0	5	24.8	.077	.403	.200	5.78	6.01
							2.11	30.6	.080					4.16	30.4	.080
				20.6	.092	.485	.200	5.41	12.0	6	20.8	.091	.480	.200	5.78	6.01
							2.62	36.6	.096					5.18	36.4	.096
				17.7	.107	.564	.200	5.41	12.0	7	17.8	.107	.561	.200	5.78	6.01
							3.13	42.7	.112					6.21	42.4	.112
				15.3	.124	.652	.200	5.41	12.0	8	14.9	.128	.673	.200	5.78	6.01
							3.65	48.7	.128					7.23	48.3	.128
				13.4	.142	.745	.200	5.41	12.0	9	13.9	.137	.721	.200	5.78	6.01
							4.16	54.8	.144					8.25	54.2	.144
				12.5	.152	.802	.200	5.41	12.0	10	11.9	.160	.841	.200	5.78	6.01
							4.67	60.8	.160					9.28	60.0	.160
				11.0	.172	.907	.200	5.41	12.0	11	10.9	.174	.918	.200	5.78	6.01
							5.18	66.7	.176					10.3	65.8	.176
				10.1	.189	.994	.200	5.41	12.0	12	9.90	.192	1.01	.200	5.78	6.01
							5.69	72.7	.192					11.3	71.6	.192
				9.58	.198	1.04	.200	5.41	12.0	13	8.91	.213	1.12	.200	5.78	6.01
							6.21	78.7	.208					12.3	77.4	.208
				8.62	.220	1.16	.200	5.41	12.0	14	8.91	.213	1.12	.200	5.78	6.01
							6.72	84.6	.224					13.4	83.1	.224
				8.14	.233	1.23	.200	5.41	12.0	15	7.92	.240	1.26	.200	5.78	6.01
							7.23	90.5	.240					14.4	88.8	.240
										16	6.93	.274	1.44	.200	5.78	6.01
														15.4	94.5	.256
										17	6.93	.274	1.44	.200	5.78	6.01
														16.4	100.	.272
										18	6.93	.274	1.44	.200	5.78	6.01
														17.5	106.	.288
										19	5.94	.320	1.69	.200	5.78	6.01
														18.5	111.	.304
										20	5.94	.320	1.69	.200	5.78	6.01
														19.5	117.	.320
										21	5.94	.320	1.69	.200	5.78	6.01
														20.5	122.	.336
										22	4.94	.384	2.02	.200	5.78	6.01
														21.6	128.	.352
										23	4.94	.384	2.02	.200	5.78	6.01
														22.6	133.	.368
										24	4.94	.384	2.02	.200	5.78	6.01
														23.6	139.	.384
										25	4.94	.384	2.02	.200	5.78	6.01
														24.6	144.	.400
										26	3.95	.481	2.53	.200	5.78	6.01
														25.7	149.	.416
										27	3.95	.481	2.53	.200	5.78	6.01
														26.7	155.	.432
										28	3.95	.481	2.53	.200	5.78	6.01
														27.7	160.	.448
										29	3.95	.481	2.53	.200	5.78	6.01
														28.7	165.	.464
										30	3.95	.481	2.53	.200	5.78	6.01
														29.8	170.	.480
										31	3.95	.481	2.53	.200	5.78	6.01
														30.8	175.	.496

Key: 1— May be overrun —M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
Communication Equipment																
2702 Transmission Ctl																
Telegraph Ctl-I																
75 bps	1M	10.0cps	29.6	96.0	.020	.104	.200	6.15	.021	1	95.2	.020	.105	.200	6.15	.021
				48.0	.040	.208	.200	5.41	12.0	2	47.6	.040	.210	.200	5.78	6.01
							.573	12.3	.042					1.09	12.3	.042
				31.7	.060	.316	.200	5.41	12.0	3	31.7	.060	.315	.200	5.78	6.01
							1.09	18.4	.063					2.11	18.3	.063
				24.0	.079	.417	.200	5.41	12.0	4	23.8	.080	.420	.200	5.78	6.01
							1.60	24.5	.084					3.13	24.3	.084
				19.2	.099	.521	.200	5.41	12.0	5	18.8	.101	.531	.200	5.78	6.01
							2.11	30.5	.105					4.16	30.3	.105
				15.8	.120	.632	.200	5.41	12.0	6	15.9	.120	.631	.200	5.78	6.01
							2.62	36.6	.126					5.18	36.2	.126
				13.4	.142	.745	.200	5.41	12.0	7	12.9	.148	.776	.200	5.78	6.01
							3.13	42.6	.147					6.21	42.1	.147
				12.0	.159	.834	.200	5.41	12.0	8	11.9	.160	.841	.200	5.78	6.01
							3.65	48.6	.168					7.23	48.0	.168
				10.5	.180	.948	.200	5.41	12.0	9	9.90	.192	1.01	.200	5.78	6.01
							4.16	54.6	.189					8.25	53.8	.189
				9.58	.198	1.04	.200	5.41	12.0	10	8.91	.213	1.12	.200	5.78	6.01
							4.67	60.5	.210					9.28	59.6	.210
				8.62	.220	1.16	.200	5.41	12.0	11	7.92	.240	1.26	.200	5.78	6.01
							5.18	66.5	.231					10.3	65.3	.231
				7.66	.248	1.31	.200	5.41	12.0	12	7.92	.240	1.26	.200	5.78	6.01
							5.69	72.4	.252					11.3	70.9	.252
				7.13	.264	1.39	.200	5.41	12.0	13	6.93	.274	1.44	.200	5.78	6.01
							6.21	78.3	.273					12.3	76.6	.273
				6.70	.283	1.49	.200	5.41	12.0	14	5.94	.320	1.69	.200	5.78	6.01
							6.72	84.1	.294					13.4	82.2	.294
				6.22	.305	1.61	.200	5.41	12.0	15	5.94	.320	1.69	.200	5.78	6.01
							7.23	90.0	.315					14.4	87.8	.315
										16	5.94	.320	1.69	.200	5.78	6.01
														15.4	93.2	.336
										17	4.94	.384	2.02	.200	5.78	6.01
														16.4	98.7	.357
										18	4.94	.384	2.02	.200	5.78	6.01
														17.5	104.	.378
										19	4.94	.384	2.02	.200	5.78	6.01
														18.5	109.	.399
										20	3.95	.481	2.53	.200	5.78	6.01
														19.5	115.	.420
										21	3.95	.481	2.53	.200	5.78	6.01
														20.5	120.	.441
										22	3.95	.481	2.53	.200	5.78	6.01
														21.6	125.	.462
										23	3.95	.481	2.53	.200	5.78	6.01
														22.6	131.	.483
										24	3.95	.481	2.53	.200	5.78	6.01
														23.6	136.	.504
										25	2.96	.642	3.38	.200	5.78	6.01
														24.6	141.	.525
										26	2.96	.642	3.38	.200	5.78	6.01
														25.7	146.	.546
										27	2.96	.642	3.38	.200	5.78	6.01
														26.7	151.	.567
										28	2.96	.642	3.38	.200	5.78	6.01
														27.7	156.	.588
										29	2.96	.642	3.38	.200	5.78	6.01
														28.7	161.	.609
										30	2.96	.642	3.38	.200	5.78	6.01
														29.8	166.	.630
										31	2.96	.642	3.38	.200	5.78	6.01
														30.8	171.	.651

Key: 1— May be overrun —M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
Communication Equipment																
2702 Transmission Ctl Telegraph Ctl-II 110 bps	1M	10.0cps	29.6	96.9	.020	.103	.200	6.15	.021	1	97.2	.020	.103	.200	6.15	.021
				48.5	.039	.206	.200	5.41	12.0	2	48.6	.039	.206	.200	5.78	6.01
							.573	12.3	.042					1.09	12.3	.042
				32.1	.059	.311	.200	5.41	12.0	3	31.7	.060	.315	.200	5.78	6.01
							1.09	18.4	.063					2.11	18.3	.063
				24.0	.079	.417	.200	5.41	12.0	4	23.8	.080	.420	.200	5.78	6.01
							1.60	24.5	.084					3.13	24.3	.084
				19.2	.099	.521	.200	5.41	12.0	5	18.8	.101	.531	.200	5.78	6.01
							2.11	30.5	.105					4.16	30.3	.105
				15.8	.120	.632	.200	5.41	12.0	6	15.9	.120	.631	.200	5.78	6.01
							2.62	36.6	.126					5.18	36.2	.126
				13.4	.142	.745	.200	5.41	12.0	7	13.9	.137	.721	.200	5.78	6.01
							3.13	42.6	.147					6.21	42.1	.147
				12.0	.159	.834	.200	5.41	12.0	8	11.9	.160	.841	.200	5.78	6.01
							3.65	48.6	.168					7.23	48.0	.168
				10.5	.180	.948	.200	5.41	12.0	9	9.90	.192	1.01	.200	5.78	6.01
							4.16	54.6	.189					8.25	53.8	.189
				9.58	.198	1.04	.200	5.41	12.0	10	8.91	.213	1.12	.200	5.78	6.01
							4.67	60.5	.210					9.28	59.6	.210
				8.62	.220	1.16	.200	5.41	12.0	11	7.92	.240	1.26	.200	5.78	6.01
							5.18	66.5	.231					10.3	65.3	.231
				7.66	.248	1.31	.200	5.41	12.0	12	7.92	.240	1.26	.200	5.78	6.01
							5.69	72.4	.252					11.3	70.9	.252
				7.18	.264	1.39	.200	5.41	12.0	13	6.93	.274	1.44	.200	5.78	6.01
							6.21	78.3	.273					12.3	76.6	.273
				6.70	.283	1.49	.200	5.41	12.0	14	6.93	.274	1.44	.200	5.78	6.01
							6.72	84.1	.294					13.4	82.2	.294
				6.22	.305	1.61	.200	5.41	12.0	15	5.94	.320	1.69	.200	5.78	6.01
							7.23	90.0	.315					14.4	87.7	.315
										16	5.94	.320	1.69	.200	5.78	6.01
														15.4	93.2	.336
										17	4.94	.384	2.02	.200	5.78	6.01
														16.4	98.7	.357
										18	4.94	.384	2.02	.200	5.78	6.01
														17.5	104.	.378
										19	4.94	.384	2.02	.200	5.78	6.01
														18.5	109.	.399
										20	3.95	.481	2.53	.200	5.78	6.01
														19.5	115.	.420
										21	3.95	.481	2.53	.200	5.78	6.01
														20.5	120.	.441
										22	3.95	.481	2.53	.200	5.78	6.01
														21.6	125.	.462
										23	3.95	.481	2.53	.200	5.78	6.01
														22.6	131.	.483
										24	3.95	.481	2.53	.200	5.78	6.01
														23.6	136.	.504
										25	2.96	.642	3.38	.200	5.78	6.01
														24.6	141.	.525
										26	2.96	.642	3.38	.200	5.78	6.01
														25.7	146.	.546
										27	2.96	.642	3.38	.200	5.78	6.01
														26.7	151.	.567
										28	2.96	.642	3.38	.200	5.78	6.01
														27.7	156.	.588
										29	2.96	.642	3.38	.200	5.78	6.01
														28.7	161.	.609
										30	2.96	.642	3.38	.200	5.78	6.01
														29.8	166.	.630
										31	2.96	.642	3.38	.200	5.78	6.01
														30.8	171.	.651

Key: 1— May be overrun —M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

INPUT/OUTPUT DEVICE	KEY	NOMINAL DATA RATE	CPU INTF	15 LINE MAXIMUM						NR OF LA	31 LINE MAXIMUM					
				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD				WAIT TIME	DEV LOAD	PREV LOAD	PRIORITY LOAD		
							TIME	A	B					TIME	A	B
World Trade TTY 50 bps	1M	6.6cps	29.6	144.	.013	.069	.200	6.15	.014	1	144.	.013	.070	.200	6.15	.014
				72.0	.026	.139	.200	5.41	12.0	2	71.4	.027	.140	.200	5.78	6.01
							.573	12.3	.028					1.09	12.3	.028
				48.0	.040	.208	.200	5.41	12.0	3	47.6	.040	.210	.200	5.78	6.01
							1.09	18.4	.042					2.11	18.4	.042
				36.0	.053	.278	.200	5.41	12.0	4	35.7	.053	.280	.200	5.78	6.01
							1.60	24.5	.056					3.13	24.4	.056
				28.8	.066	.347	.200	5.41	12.0	5	28.8	.066	.348	.200	5.78	6.01
							2.11	30.6	.070					4.16	30.5	.070
				24.0	.079	.417	.200	5.41	12.0	6	23.8	.080	.420	.200	5.78	6.01
							2.62	36.7	.084					5.18	36.5	.084
				20.1	.094	.496	.200	5.41	12.0	7	19.8	.096	.504	.200	5.78	6.01
							3.13	42.7	.098					6.20	42.4	.098
				17.7	.107	.564	.200	5.41	12.0	8	17.8	.107	.561	.200	5.78	6.01
							3.65	48.8	.112					7.23	48.4	.112
				15.8	.120	.632	.200	5.41	12.0	9	15.9	.120	.631	.200	5.78	6.01
							4.16	54.8	.126					8.25	54.3	.126
				14.4	.132	.695	.200	5.41	12.0	10	13.9	.137	.721	.200	5.78	6.01
							4.67	60.8	.140					9.28	60.2	.140
				12.9	.147	.773	.200	5.41	12.0	11	12.9	.148	.776	.200	5.78	6.01
							5.18	66.9	.154					10.3	66.1	.154
				12.0	.159	.834	.200	5.41	12.0	12	11.9	.160	.841	.200	5.78	6.01
							5.69	72.8	.168					11.3	71.9	.168
				11.0	.172	.907	.200	5.41	12.0	13	10.9	.174	.918	.200	5.78	6.01
							6.21	78.8	.182					12.3	77.7	.182
				10.1	.189	.994	.200	5.41	12.0	14	9.90	.192	1.01	.200	5.78	6.01
							6.72	84.8	.196					13.4	83.5	.196
				9.58	.198	1.04	.200	5.41	12.0	15	8.91	.213	1.12	.200	5.78	6.01
							7.23	90.7	.210					14.4	89.2	.210
										16	8.91	.213	1.12	.200	5.78	6.01
														15.4	94.9	.224
										17	7.92	.240	1.26	.200	5.78	6.01
														16.4	101.	.238
										18	7.92	.240	1.26	.200	5.78	6.01
														17.5	106.	.252
										19	6.93	.274	1.44	.200	5.78	6.01
														18.5	112.	.266
										20	6.93	.274	1.44	.200	5.78	6.01
														19.5	118.	.280
										21	5.94	.320	1.69	.200	5.78	6.01
														20.5	123.	.294
										22	5.94	.320	1.69	.200	5.78	6.01
														21.6	129.	.308
										23	5.94	.320	1.69	.200	5.78	6.01
														22.6	134.	.322
										24	5.94	.320	1.69	.200	5.78	6.01
														23.6	140.	.336
										25	4.94	.384	2.02	.200	5.78	6.01
														24.6	145.	.350
										26	4.94	.384	2.02	.200	5.78	6.01
														25.7	151.	.364
										27	4.94	.384	2.02	.200	5.78	6.01
														26.7	156.	.378
										28	4.94	.384	2.02	.200	5.78	6.01
														27.7	161.	.392
										29	4.94	.384	2.02	.200	5.78	6.01
														28.7	167.	.406
										30	3.95	.481	2.53	.200	5.78	6.01
														29.8	172.	.420
										31	3.95	.481	2.53	.200	5.78	6.01
														30.8	177.	.434

Key:
1– May be overrun
–M Multiplex mode operation on Multiplexer Channel

Table 1. (continued)

TERMINAL CONTROL	NMax 15 LINE	31 LINE
IBM Type I		
75 bps	242	117
135.5 bps	139	67
600 bps	30	.....
IBM Type II		
600 bps	30	.....
Telegraph I		
45 bps	332	160
57 bps	260	126
75 bps	200	96
Telegraph Type II		
110 bps	202	98
WTC Telegraph		
50 bps	300	145
75 bps	200	96
	15 LINE MAX	31 LINE MAX
Device Load	1.9	1.9
Previous Load	10.0	10.0

Table 2. IBM System/360 Model 40 Evaluation Factors for 2702 Special Analysis

Segment 1 — One Line Priority Load Function

TERMINAL CONTROL	b	15 LINE MAX TIME	15 LINE MAX A	15 LINE MAX B	31 LINE MAX TIME	31 LINE MAX A	31 LINE MAX B
IBM Type I							
75 bps	0.02	.200	6.149	0.02	.200	6.149	0.02
135.5 bps	0.035	.200	6.148	0.035	.200	6.149	0.035
600 bps	0.174	.200	6.139	0.174	.200	6.139	0.174
IBM Type II							
600 bps	0.166	.200	6.140	0.166	.200	6.140	0.166
Telegraph Type I							
45 bps	0.013	.200	6.149	0.013	.200	6.149	0.013
57 bps	0.016	.200	6.149	0.016	.200	6.149	0.016
75 bps	0.021	.200	6.149	0.021	.200	6.149	0.021
Telegraph Type II							
110 bps	0.021	.200	6.149	0.021	.200	6.149	0.021
World Trade Telegraph							
50 bps	0.014	.200	6.149	0.014	.200	6.149	0.014
75 bps	0.021	.200	6.149	0.021	.200	6.149	0.021

Segment 2 — Multiple Line Priority Load Function

15 LINE MAX TIME	15 LINE MAX A	15 LINE MAX B	31 LINE MAX TIME	31 LINE MAX A	31 LINE MAX B
.200	5.411	12.01	.200	5.781	6.005

Segment 3

15 LINE MAX NUMBER OF LINES	15 LINE MAX TIME	31 LINE MAX NUMBER OF LINES	31 LINE MAX TIME	31 LINE MAX NUMBER OF LINES	31 LINE MAX TIME
2	0.574	2	1.086	17	16.446
3	1.086	3	2.110	18	17.470
4	1.598	4	3.134	19	18.494
5	2.110	5	4.158	20	19.518
6	2.622	6	5.182	21	20.542
7	3.134	7	6.206	22	21.560
8	3.646	8	7.230	23	22.590
9	4.158	9	8.254	24	23.614
10	4.670	10	9.278	25	24.638
11	5.182	11	10.302	26	25.662
12	5.694	12	11.326	27	26.686
13	6.206	13	12.350	28	27.710
14	6.718	14	13.374	29	28.734
15	7.230	15	14.398	30	29.758
		16	15.422	31	30.782

Table 3. IBM System/360 Model 40 Priority Load Factors for 2702

	SELECTOR CHANNEL	MULTIPLEXER CHANNEL
Data Service	1.25 μs/Byte	see Table 1**
Command Chaining	17.5 μs/CCW	68.1+U_1 μs/CCW*
if status modifier, add add'l	.625 μs/CCW	1.25 μs/CCW
if status modifier plus carry, add add'l	1.25 μs/CCW	1.25 μs/CCW
if TIC add	5.625 μs/TIC	7.5 μs/TIC
Data Chaining	10.625 μs/CCW	20.0 μs/CCW
if TIC	5.0 μs/TIC	12.5 μs/TIC
Program Controlled Interruption	40.63 μs/PCI	61.88 μs/PCI
Channel End Interruption	40.63 μs/each	60.63 μs/each
Device End or Control Unit End Interruption	45.0+U_1 μs/each*	56.88+U_1 μs/each*

*U_1 = Select out delay + device delay

**The CPU Intf column in Table 1 lists interference caused by multiplex mode devices in microseconds per byte of data transferred. Burst mode operation of the multiplexer channel causes 100 percent CPU interference.

Table 4. IBM System/360 Model 40 CPU Interference Factors

	SELECTOR CHANNEL LOAD LIMITS		
	CHAINING SPECIFICATIONS		
	No DC	DC	DC & TIC
One channel in operation	60	50	40
Two channels in operation			
Selector Channel 1	50	32	21.6
Selector Channel 2	41	32	21.6

Table 5. IBM System/360 Model 40 Selector Channel Load Limits — with Multiplexer Channel Operating in Byte-Multiplex Mode

	COMBINED SELECTOR CHANNEL LOAD LIMITS (SEL 1 & SEL 2) NO DC	MULTIPLEXER LOAD LIMITS
Selector Channels Not Operating	0	25
Selector Channels Operating	41	16

Table 6. IBM System/360 Model 40 Channel Load Limits with Multiplexer Channel Operating in Burst Mode

MULTIPLEXER CHANNEL WORKSHEET

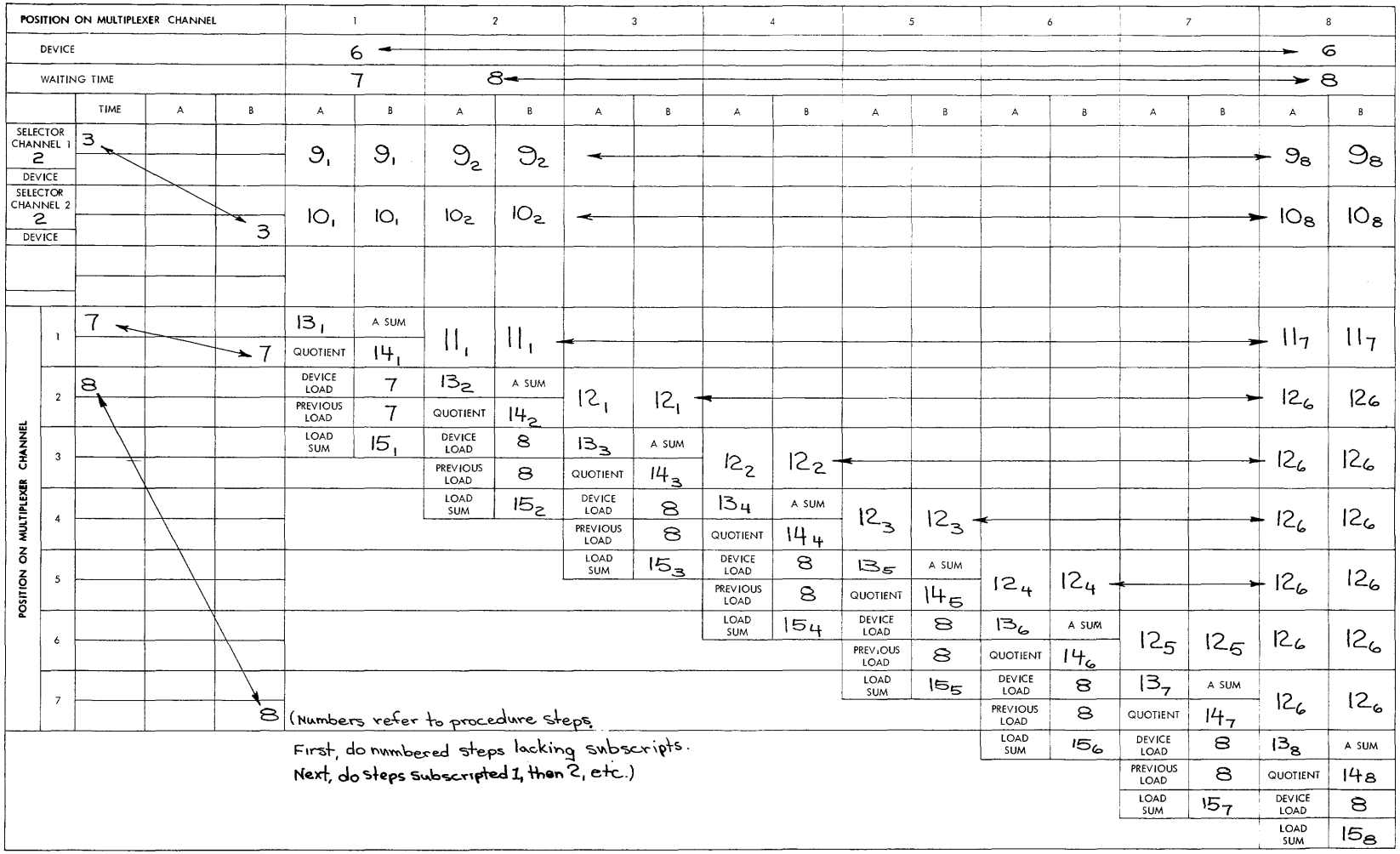
SYSTEM IDENTIFICATION _____ DATE _____

POSITION ON MULTIPLEXER CHANNEL				1		2		3		4		5		6		7		8	
DEVICE																			
WAITING TIME																			
	TIME	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
SELECTOR CHANNEL 1																			
DEVICE																			
SELECTOR CHANNEL 2																			
DEVICE																			
POSITION ON MULTIPLEXER CHANNEL 1					A SUM														
				QUOTIENT															
2				DEVICE LOAD			A SUM												
				PREVIOUS LOAD		QUOTIENT													
3				LOAD SUM		DEVICE LOAD			A SUM										
						PREVIOUS LOAD		QUOTIENT											
4						LOAD SUM		DEVICE LOAD			A SUM								
								PREVIOUS LOAD		QUOTIENT									
5								LOAD SUM		DEVICE LOAD			A SUM						
										PREVIOUS LOAD		QUOTIENT							
6										LOAD SUM		DEVICE LOAD			A SUM				
												PREVIOUS LOAD		QUOTIENT					
7												LOAD SUM		DEVICE LOAD			A SUM		
														PREVIOUS LOAD		QUOTIENT			
														LOAD SUM		DEVICE LOAD			A SUM
																PREVIOUS LOAD		QUOTIENT	
																LOAD SUM		DEVICE LOAD	
																		LOAD SUM	

● Figure 8. Example of Blank Worksheet

MULTIPLEXER CHANNEL WORKSHEET

SYSTEM IDENTIFICATION 1 DATE 1



● Figure 9. Sequence for Worksheet Entries

MULTIPLEXER CHANNEL WORKSHEET

SYSTEM IDENTIFICATION Model 40 DATE

POSITION ON MULTIPLEXER CHANNEL					1		2		3		4		5		6		7		8	
DEVICE					1442-N1		1442-N2		1443		1052									
WAITING TIME					.800		11.0		18.5		70.0									
		TIME	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
SELECTOR CHANNEL 1 2311 DEVICE		.200	3.40	21.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3								
		.800	2.80	20.3																
SELECTOR CHANNEL 2 2400 60KB DEVICE		.200	3.15	—	—	7.50	—	7.50	—	7.50	—	7.50								
		.420	—	7.50																
POSITION ON MULTIPLEXER CHANNEL	1	.200	7.05	7.55	2.80	A SUM	13.4	5.30	13.4	5.30	13.4	5.30								
		2.80	13.4	5.30	QUOTIENT	3.50														
	2	.200	8.56	—	DEVICE LOAD	5.90	16.2	A SUM	—	0.98	—	0.98								
		12.5	—	0.98	PREVIOUS LOAD	12.50	QUOTIENT	1.48												
	3	.200	—	100	LOAD SUM	49.70	DEVICE LOAD	0.43	16.2	A SUM	417	—								
		4.77 200	417 466	— 2.38			PREVIOUS LOAD	0.90	QUOTIENT	0.88										
	4						LOAD SUM	35.91	DEVICE LOAD	25.8	433.2	A SUM								
									PREVIOUS LOAD	0.64	QUOTIENT	6.19								
	5								LOAD SUM	61.3	DEVICE LOAD	.034		A SUM						
											PREVIOUS LOAD	—	QUOTIENT								
	6										LOAD SUM	40.30	DEVICE LOAD			A SUM				
													PREVIOUS LOAD		QUOTIENT					
	7												LOAD SUM		DEVICE LOAD			A SUM		
															PREVIOUS LOAD		QUOTIENT			
															LOAD SUM		DEVICE LOAD			A SUM
																	PREVIOUS LOAD		QUOTIENT	
																	LOAD SUM		DEVICE LOAD	
																			LOAD SUM	

● Figure 10. Worksheet Example

MULTIPLEXER CHANNEL WORKSHEET

SYSTEM IDENTIFICATION Model 40 DATE

POSITION ON MULTIPLEXER CHANNEL					1		2		3		4		5		6		7		8	
DEVICE					2702-15-1030's		2702 31-1050's		2540R		2540P		1403-N1		1403-N1		1443		1052	
WAITING TIME					.944		1.97		6.5		14.0		15.7		15.7		18.5		70.0	
		TIME	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
SELECTOR CHANNEL 1 2311 DEVICE		.200	3.40	21.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3
		.800	2.80	20.3																
SELECTOR CHANNEL 2 2400-3 DEVICE		.200	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2	0.94	12.2
POSITION ON MULTIPLEXER CHANNEL	1	.200	5.41	12.0	3.74	A SUM	5.41	12.0	5.41	12.0	74.2	2.49	74.2	2.49	74.2	2.49	74.2	2.49	74.2	2.49
		7.23	74.2	2.49	QUOTIENT	4.0														
	2	.200	5.78	6.01	DEVICE LOAD	2.01	9.15	A SUM	5.78	6.01	5.78	6.01	5.78	6.01	5.78	6.01	5.78	6.01	157.	1.09
		30.8	157.	1.09	PREVIOUS LOAD	10.6	QUOTIENT	4.64												
	3	1.75	175.	—	LOAD SUM	49.1	DEVICE LOAD	.965	14.93	A SUM	175	—	175	—	175	—	175	—	170	2.90
		60.0	170.	2.90			PREVIOUS LOAD	5.08	QUOTIENT	2.3										
	4	1.98	198	—			LOAD SUM	55.19	DEVICE LOAD	26.9	258.72	A SUM	198	—	198	—	198	—	198	—
		200	196	0.99					PREVIOUS LOAD	1.50	QUOTIENT	18.5								
	5	2.26	226	—					LOAD SUM	81.2	DEVICE LOAD	14.1	456.72	A SUM	226	—	226	—	216	4.10
		54.5	216	4.10							PREVIOUS LOAD	0.70	QUOTIENT	29.1						
	6	2.26	226	—							LOAD SUM	74.3	DEVICE LOAD	14.4	682.72	A SUM	226		216	4.10
		54.5	216	4.10									PREVIOUS LOAD	0.64	QUOTIENT	43.4				
	7	4.77	477	—									LOAD SUM	85.1	DEVICE LOAD	14.4	968.72	A SUM	477	—
		2.50	468	1.90											PREVIOUS LOAD	0.64	QUOTIENT	49.1		
															LOAD SUM	99.4	DEVICE LOAD	25.8	1511.94	A SUM
																	PREVIOUS LOAD	0.54	QUOTIENT	21.6
																	LOAD SUM	116.3	DEVICE LOAD	.034
																			LOAD SUM	68.8

● Figure 11. Worksheet Example with Two 2702's and a 2821

IBM 2702 WORKSHEET

SYSTEM IDENTIFICATION _____ DATE _____

NUMBER OF LINES= _____	REVOLUTION		i = 1		i = 2		i = 3		i = 4		i = 5		i = 6		i = 7		i = 8	
LINE NUMBER= _____	t_1 =		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =	
SUBTRACT: K= _____	n =		n =		n =		n =		n =		n =		n =		n =		n =	
n_{max} = _____	A_1	B_1	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2
SELECTOR CHANNEL 1																		
SELECTOR CHANNEL 2																		
DEVICE 1																		
DEVICE 2																		
DEVICE 3																		
DEVICE 4																		
DEVICE 5																		
DEVICE 6																		
DEVICE 7																		
DEVICE 8																		
DEVICE 9																		
DEVICE 10																		
SUM A's AND B's																		
MULTIPLY: t_i X SUM B_i	X		X		X		X		X		X		X		X		X	
A REMAINDER																		
B REMAINDER																		
DEVICE LOAD																		
PREVIOUS LOAD																		
LOAD SUM																		
LOAD LIMIT	15 Line 2702		46.4		94.4		142.4		190.4		238.4		286.4		334.4		382.4	
	31 Line 2702		97.6		196.8		296.0		395.2		494.4		593.6		692.8		792.0	

MAXIMUM NUMBER OF REVOLUTIONS TO COMPLETE SERVICE: $n + (i - 1)k$

Figure 12. Example of Blank 2702 Worksheet

IBM 2702 WORKSHEET

SYSTEM IDENTIFICATION _____ DATE _____

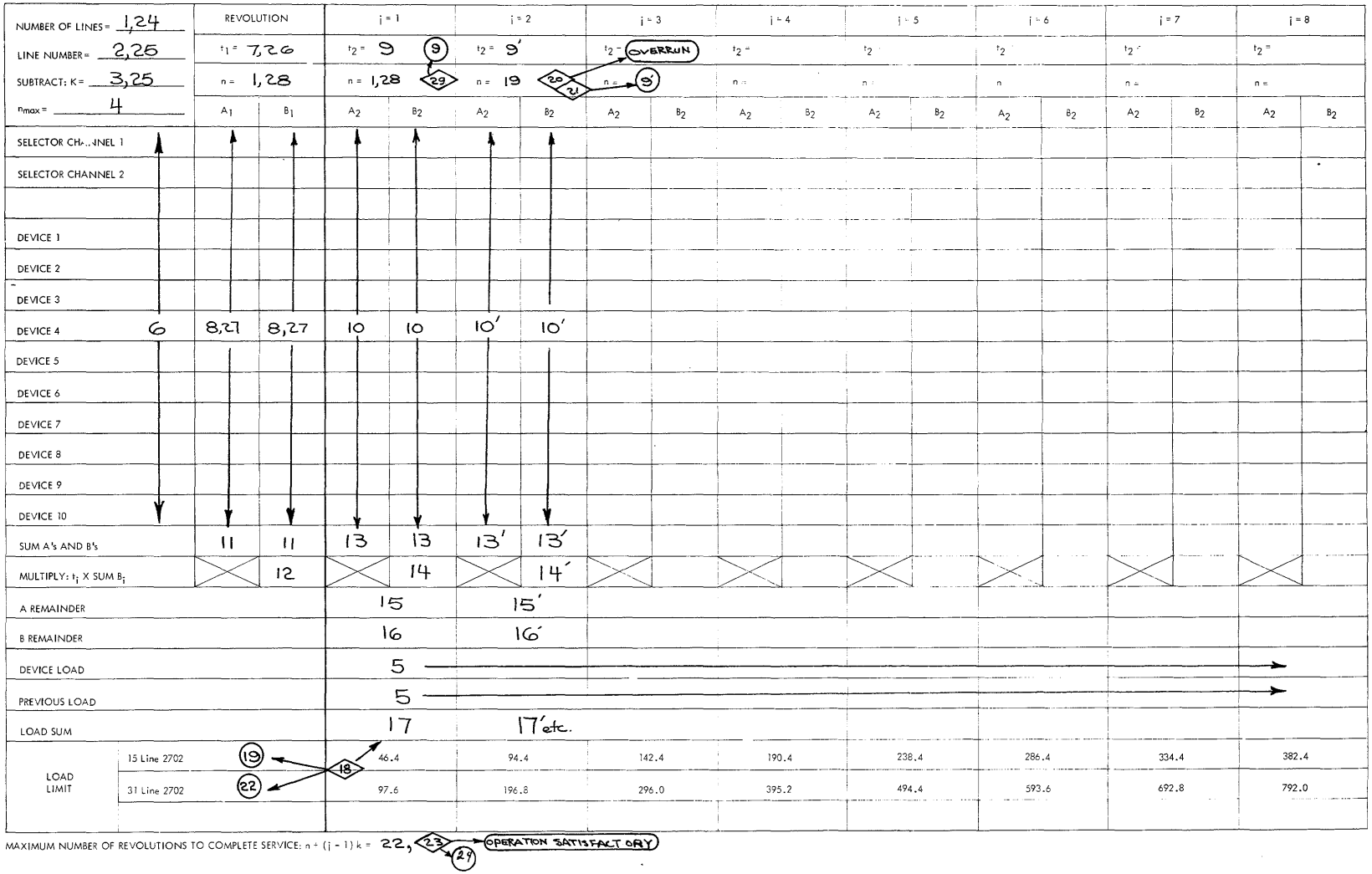
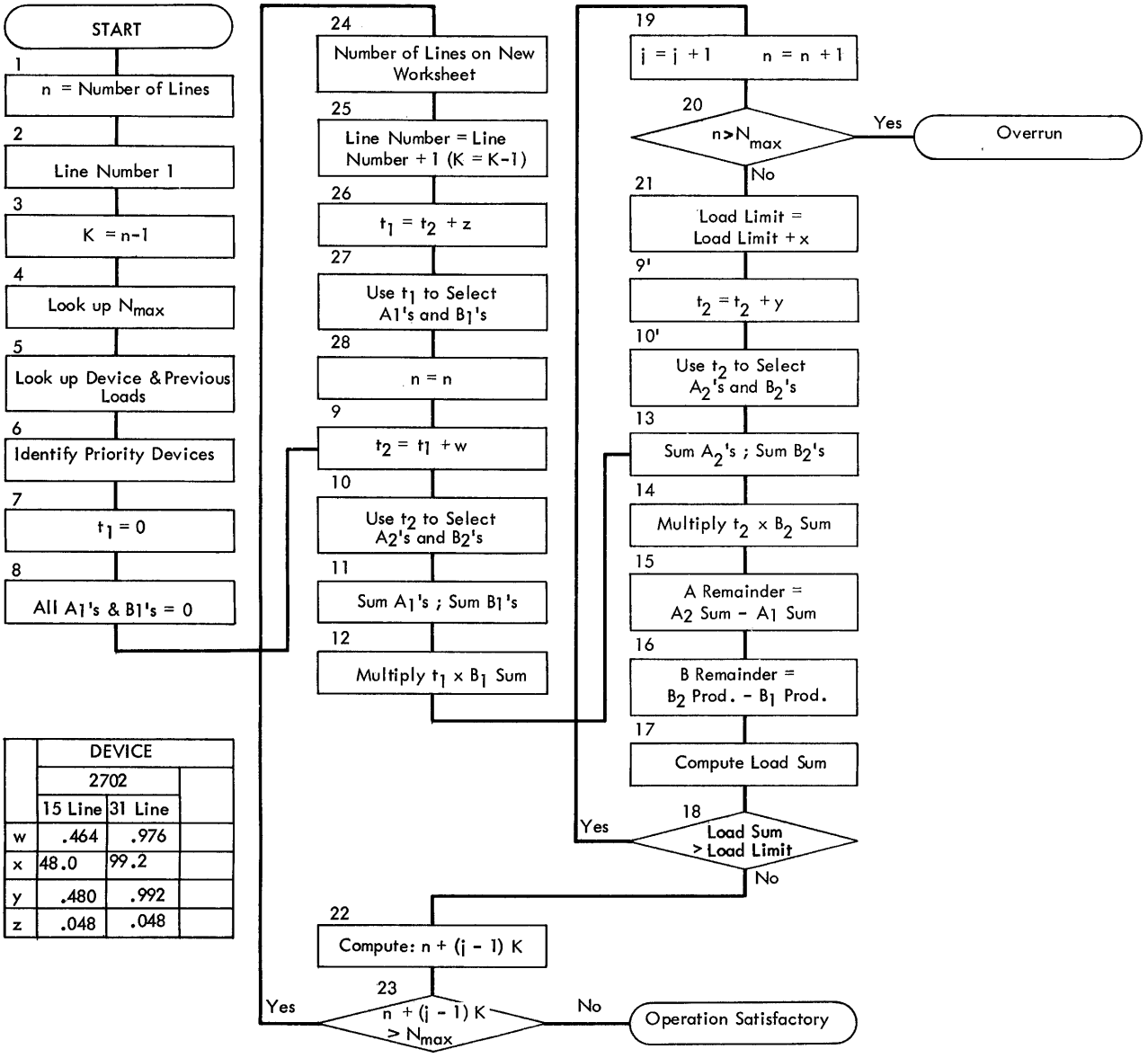


Figure 13. Sequence for 2702 Worksheet Entries



	DEVICE		
	2702		
	15 Line	31 Line	
w	.464	.976	
x	48.0	99.2	
y	.480	.992	
z	.048	.048	

Figure 14. Flowchart for 2702 Special Analysis Worksheet Procedure

MULTIPLEXER CHANNEL WORKSHEET

SYSTEM IDENTIFICATION Model 40 DATE

POSITION ON MULTIPLEXER CHANNEL			1		2		3		4		5		6		7		8	
DEVICE			2702/15-1030		2702/15-1030		2702/10-1030		2702/1-1030 / 10-83B2		1443							
WAITING TIME			.944		.944		1.42		.944		18.5							
	TIME	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
SELECTOR CHANNEL 1 2311 DC DEVICE	.200	1.60	28.9	1.60	28.9	1.60	28.9	1.60	28.9	1.60	28.9	1.60	28.9						
SELECTOR CHANNEL 2 2311 DEVICE	.200	3.40	21.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3						
	.8	2.80	20.3																
POSITION ON MULTIPLEXER CHANNEL 1	.200	5.41	12.0	4.40	A SUM	5.41	12.0	5.41	12.0	5.41	12.0	74.2	2.5						
	7.23	74.2	2.49	QUOTIENT	4.7														
2	.200	5.41	12.0	DEVICE LOAD	2.0	9.81	A SUM	5.41	12.0	5.41	12.0	74.2	2.5						
	7.23	74.2	2.49	PREVIOUS LOAD	10.6	QUOTIENT	10.4												
3	.200	5.41	12.0	LOAD SUM	66.5	DEVICE LOAD	2.0	15.22	A SUM	5.41	12.0	53.7	1.7						
	4.67	53.7	1.66			PREVIOUS LOAD	10.6	QUOTIENT	10.7										
4	.200	5.41	12.0			LOAD SUM	84.2	DEVICE LOAD	1.3	20.63	A SUM	74.2	2.5						
	7.23	74.2	2.49					PREVIOUS LOAD	7.0	QUOTIENT	21.9								
5								LOAD SUM	92.2	DEVICE LOAD	2.0	280.7	A SUM						
										PREVIOUS LOAD	10.6	QUOTIENT	15.2						
6										LOAD SUM	119.7	DEVICE LOAD	25.8		A SUM				
												PREVIOUS LOAD	—	QUOTIENT					
7												LOAD SUM	99.4	DEVICE LOAD			A SUM		
														PREVIOUS LOAD		QUOTIENT			
														LOAD SUM		DEVICE LOAD			A SUM
																PREVIOUS LOAD		QUOTIENT	
																LOAD SUM		DEVICE LOAD	
																		LOAD SUM	

● Figure 15. Excessive 2702 Load Sum Worksheet Example

IBM 2702 WORKSHEET

SYSTEM IDENTIFICATION Model 40-2702 DATE

NUMBER OF LINES = 11	REVOLUTION		i = 1		i = 2		i = 3		i = 4		i = 5		i = 6		i = 7		i = 8	
LINE NUMBER = 1	t_1 = 0		t_2 = .464		t_2 = .944		t_2 = 1.424		t_2 = 1.904		t_2 = 2.384		t_2 =		t_2 =		t_2 =	
SUBTRACT: K = 10	n = 11		n = 11		n = 12		n = 13		n = 14		n = 15		n =		n =		n =	
n_{max} = 30	A_1	B_1	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2
SELECTOR CHANNEL 1 2311	0	0	1.60	28.9	1.60	28.9	1.60	28.9	1.60	28.9	1.60	28.9						
SELECTOR CHANNEL 2 2311	0	0	3.40	21.3	2.80	20.3	2.80	20.3	2.80	20.3	2.80	20.3						
DEVICE 1 2702	0	0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0						
DEVICE 2 2702	0	0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0						
DEVICE 3 2702	0	0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0	5.41	12.0						
DEVICE 4																		
DEVICE 5																		
DEVICE 6																		
DEVICE 7																		
DEVICE 8																		
DEVICE 9																		
DEVICE 10																		
SUM A's AND B's	0	0	21.23	86.2	20.63	85.2	20.63	85.2	20.63	85.2	20.63	85.2						
MULTIPLY: t_i X SUM B_i	X	0	X	40.0	X	80.3	X	121.3	X	162.2	X	203	X		X		X	
A REMAINDER				21.23		20.63		20.6		20.6		20.6						
B REMAINDER				40.00		80.3		121.3		162.2		203						
DEVICE LOAD				1.9		1.9		1.9		1.9		1.9						
PREVIOUS LOAD				10.0		10.0		10.1		10.1		10.0						
LOAD SUM				73.13		112.83		153.8		194.7		235.5						
LOAD LIMIT — 15 Line 2702			46.4		94.4		142.4		190.4		238.4		286.4		334.4		382.4	
LOAD LIMIT — 31 Line 2702			97.6		196.8		296.0		395.2		494.4		593.6		692.8		792.0	

MAXIMUM NUMBER OF REVOLUTIONS TO COMPLETE SERVICE: $n + (i - 1)k$ = 15 + (5-1)10 = 55

● Figure 16. IBM 2702 Special Analysis Worksheet Example (Sheet 1 of 2)

IBM 2702 WORKSHEET

SYSTEM IDENTIFICATION Model 40-2702 DATE

NUMBER OF LINES = 11	REVOLUTION		j = 1		j = 2		j = 3		j = 4		j = 5		j = 6		j = 7		j = 8	
LINE NUMBER = 2	t_1 = 2432		t_2 = 2.896		t_2 = 3.376		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =		t_2 =	
SUBTRACT: K = 9	n = 15		n = 15		n = 16		n =		n =		n =		n =		n =		n =	
n_{max} = 30	A_1	B_1	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2	A_2	B_2
SELECTOR CHANNEL 1 2311	1.6	28.9	1.6	28.9	1.6	28.9												
SELECTOR CHANNEL 2 2311	2.8	20.3	2.8	20.3	2.8	20.3												
DEVICE 1 2702	5.4	12.0	5.4	12.0	5.4	12.0												
DEVICE 2 2702	5.4	12.0	5.4	12.0	5.4	12.0												
DEVICE 3 2702	5.4	12.0	5.4	12.0	5.4	12.0												
DEVICE 4																		
DEVICE 5																		
DEVICE 6																		
DEVICE 7																		
DEVICE 8																		
DEVICE 9																		
DEVICE 10																		
SUM A's AND B's	20.6	85.2	20.6	85.2	20.6	85.2												
MULTIPLY: t_i X SUM B_i		207		247		288												
A REMAINDER				0.0		0.0												
B REMAINDER				40.0		81.0												
DEVICE LOAD				1.9		1.9												
PREVIOUS LOAD				10.0		10.0												
LOAD SUM				51.9		92.9												
LOAD LIMIT — 15 Line 2702			46.4		94.4		142.4		190.4		238.4		286.4		334.4		382.4	
LOAD LIMIT — 31 Line 2702			97.6		196.8		296.0		395.2		494.4		593.6		692.8		792.0	

MAXIMUM NUMBER OF REVOLUTIONS TO COMPLETE SERVICE: $n + (j - 1)k$ = 16 + (2-1)9 = 24

● Figure 16. IBM 2702 Special Analysis Worksheet Example (Sheet 2 of 2)

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