IBM

Field Engineering Education

Supplementary Course Material

SYSTEM/360

Model 40 CPU and Channels

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SYSTEM/360

Model 40 CPU and Channels

PREFACE

This Instructional Diagram package is for use by the student on the System/360 Model 40 Course on CAL.

The content figures and charts do not constitute a complete maintenance package, and their use is restricted to instruction only.

(September 1970)

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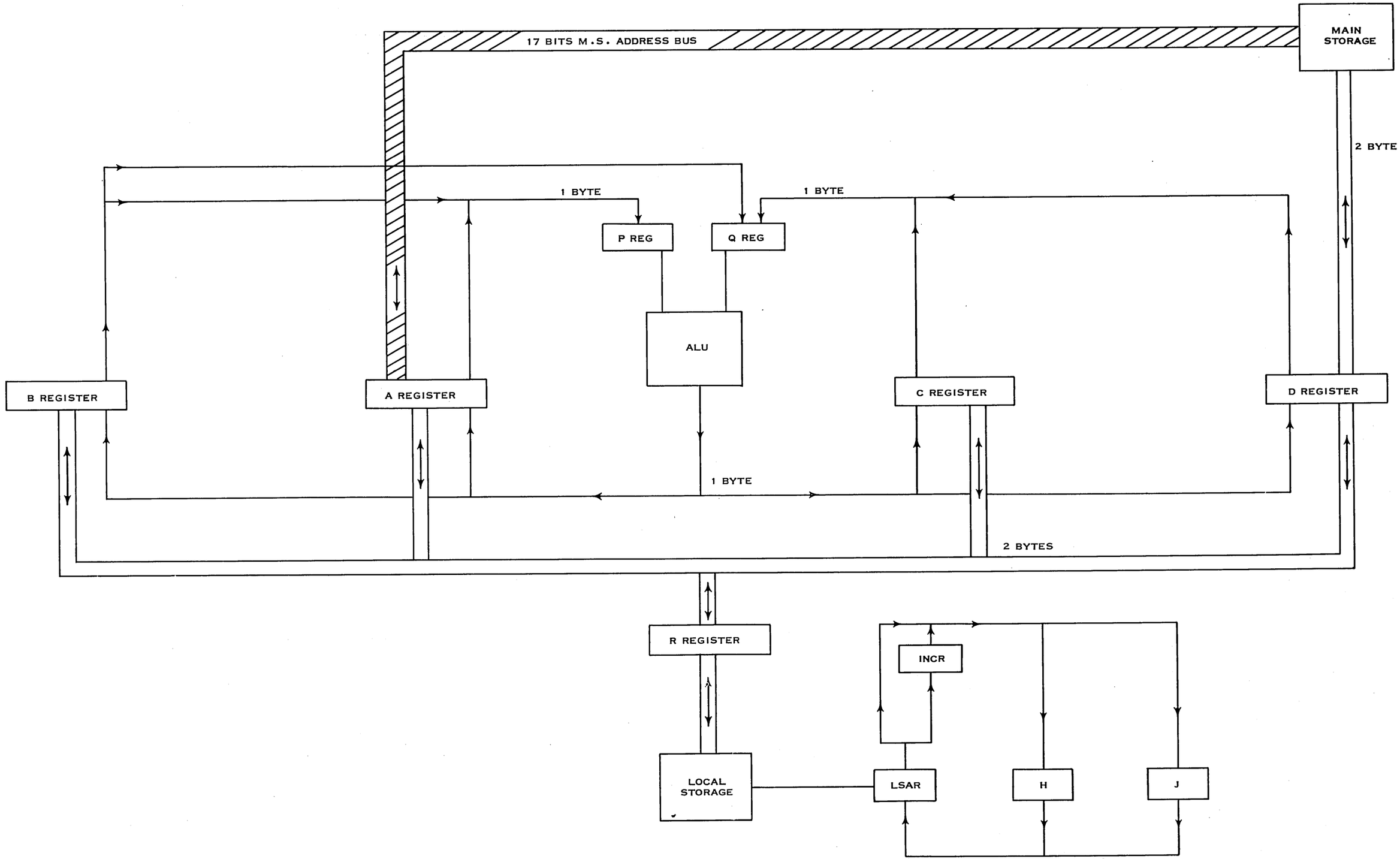
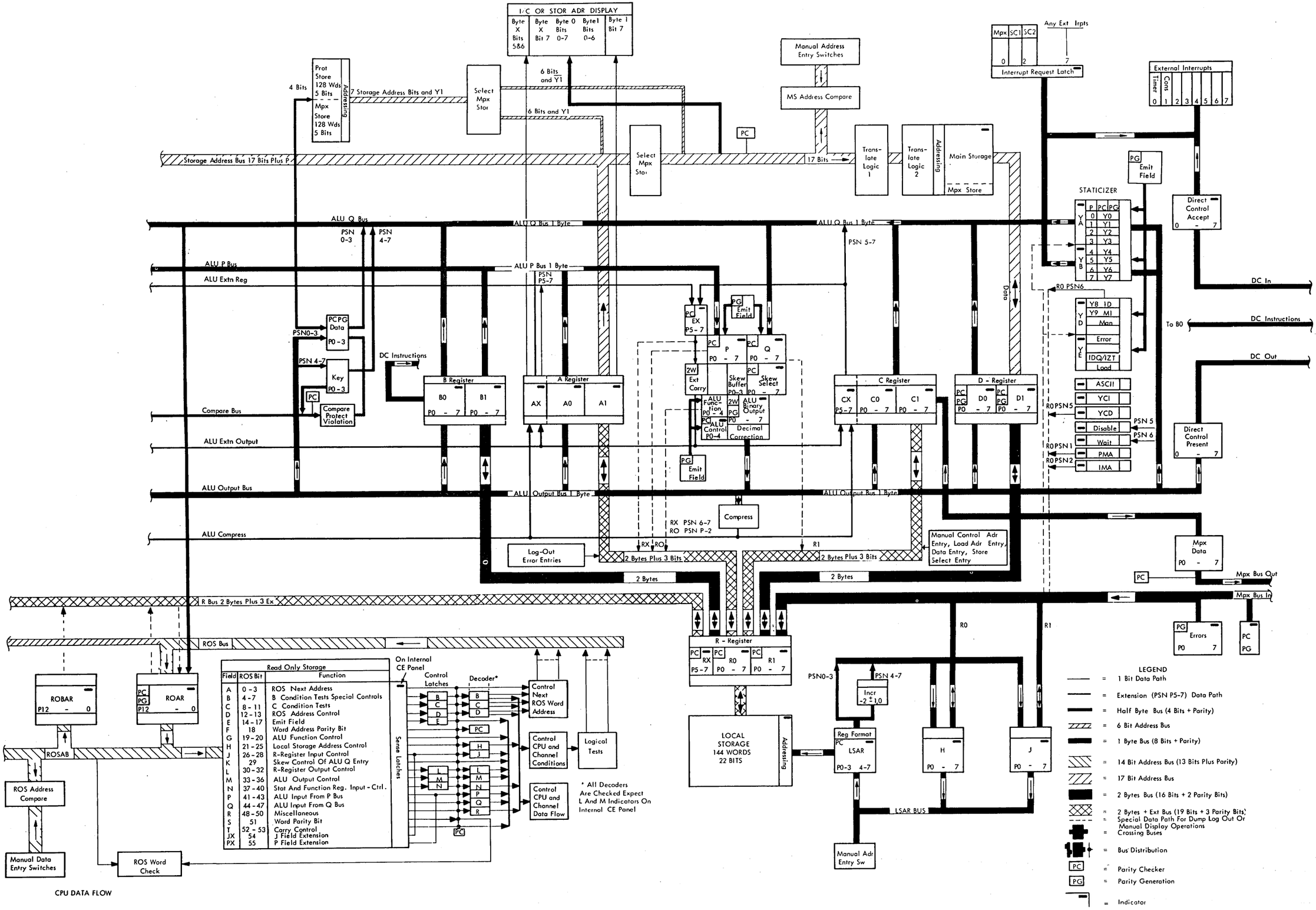

17 BITS M.S. ADDRESS BUS
MAIN STORAGE
2 BYTE
1 BYTE
1 BYTE
P REG
Q REG
ALU
B REGISTER
A REGISTER
C REGISTER
D REGISTER
1 BYTE
2 BYTES
R REGISTER
INCR
LOCAL STORAGE
LSAR
H
J

FIGURE 1



Field	ROS Bit	Function
A	0 - 3	ROS Next Address
B	4 - 7	B Condition Tests Special Controls
C	8 - 11	C Condition Tests
D	12 - 13	ROS Address Control
E	14 - 17	Emit Field
F	18	Word Address Parity Bit
G	19 - 20	ALU Function Control
H	21 - 25	Local Storage Address Control
J	26 - 28	R-Register Input Control
K	29	Skew Control Of ALU Q Entry
L	30 - 32	R-Register Output Control
M	33 - 36	ALU Output Control
N	37 - 40	Stat And Function Reg. Input - Ctrl.
P	41 - 43	ALU Input From P Bus
Q	44 - 47	ALU Input From Q Bus
R	48 - 50	Miscellaneous
S	51	Word Parity Bit
T	52 - 53	Carry Control
JX	54	J Field Extension
PX	55	P Field Extension

FIGURE 2

CPU DATA FLOW

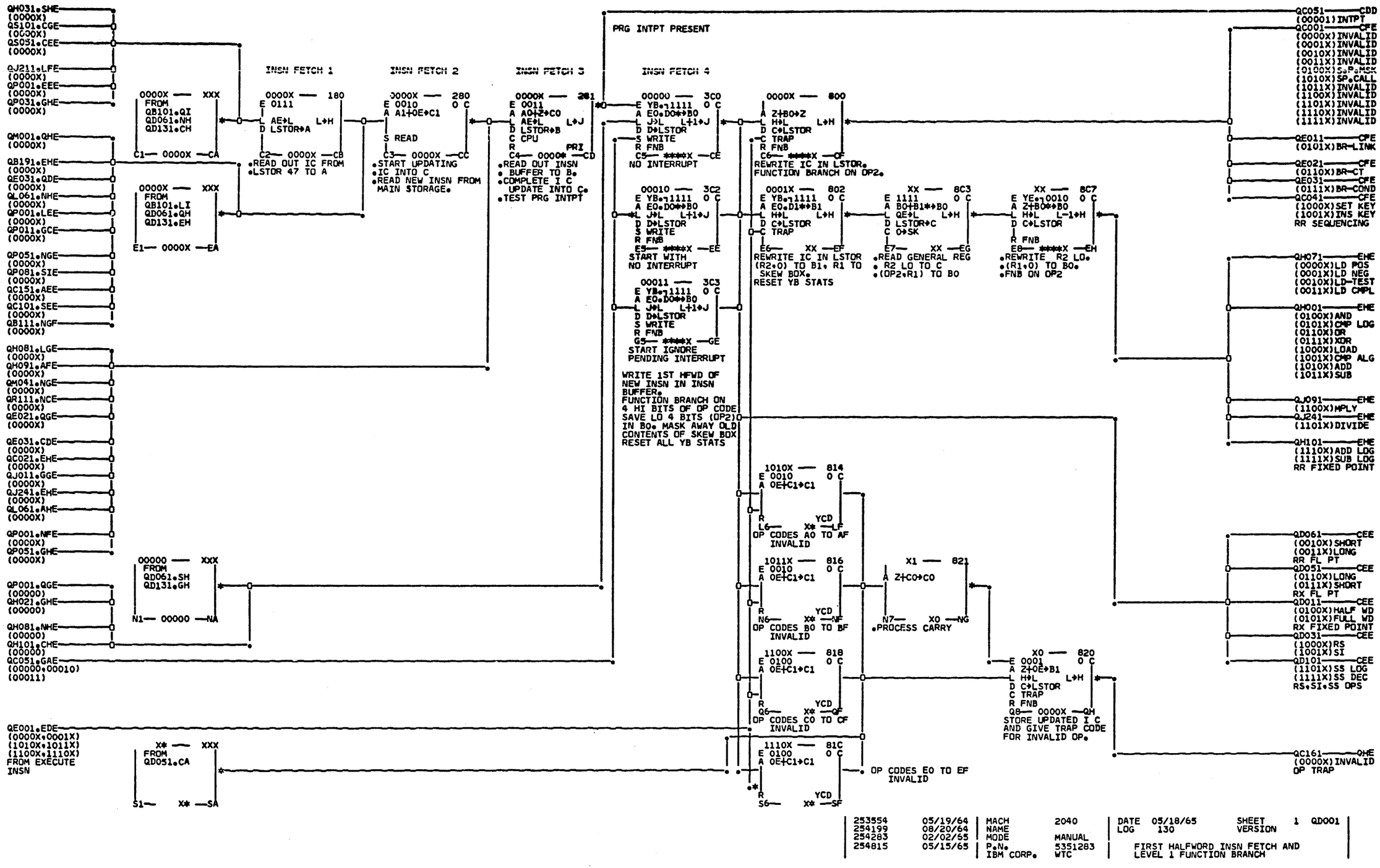
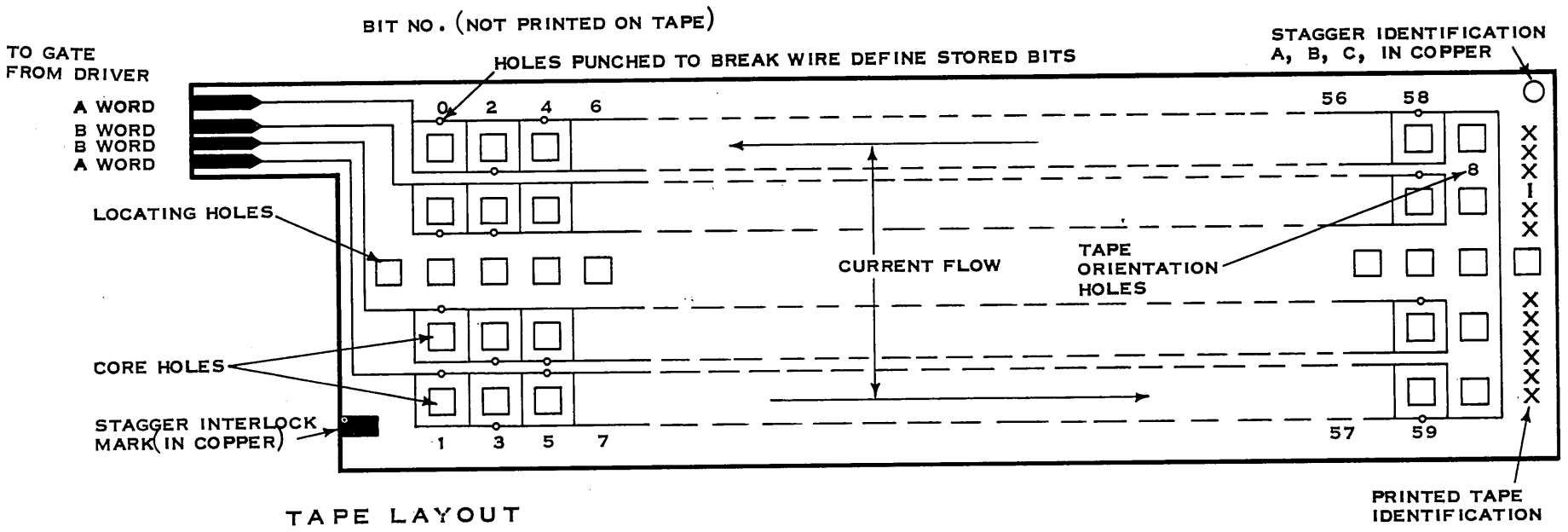


FIGURE 3

CLD Sample



TAPE LAYOUT

FIGURE 4

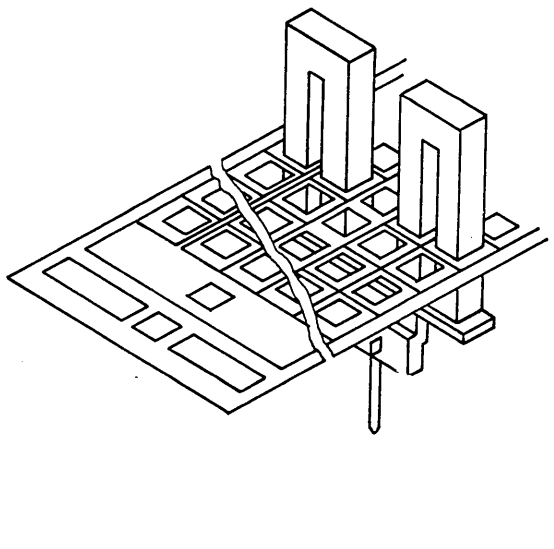
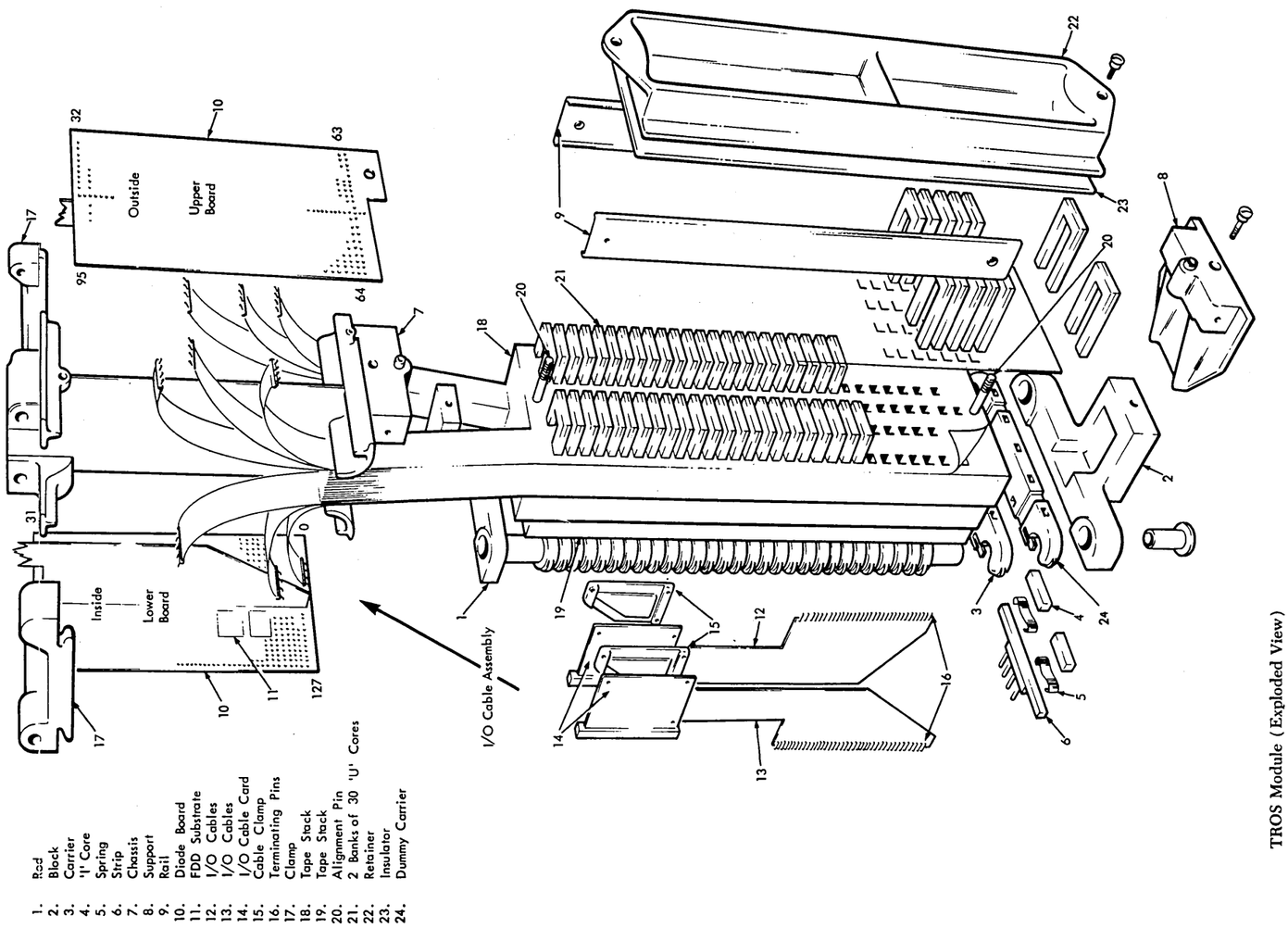


FIGURE 5



TROS Module (Exploded View)

FIGURE 6

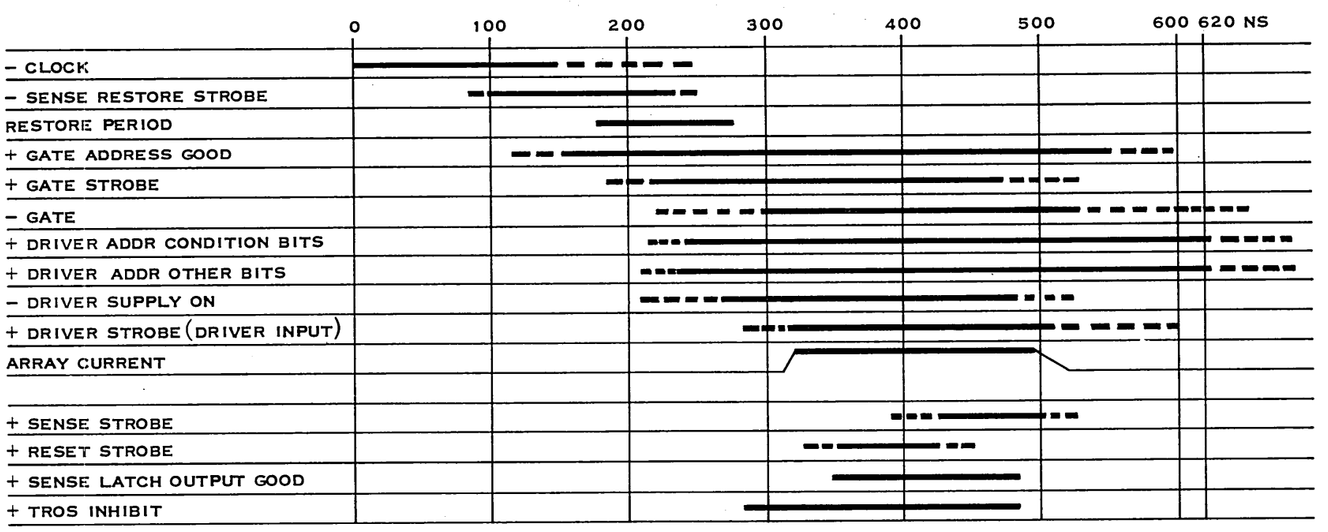


FIGURE 7

PRINT POSITIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1		X	X	X	X	X									3C0
2	E	EMIT STATEMENT													
3	A	ARITHMETIC													
4	L	LOCAL STORAGE ADDRESS													
5	D	DATA TRANSFER													
6	S/C	MAIN STORAGE OR SPECIAL CONTROL													
7	R	TROS ADDRESS CONTROL													
8															

PRINT LINES

	X	X		X	X	X	X	X					X	X	

FIGURE 8

?	INDIRECT ALU FUNCTION
⎍	DIRECT OR FUNCTION
•	DIRECT AND FUNCTION
—	DIRECT SUBTRACT FUNCTION (P-Q)
+	DIRECT ADD FUNCTION (BINARY)

FIGURE 9

DATA CONTENTS PRIOR TO OPERATIONS

B05FF
A0102
C0000
D1111
YA 1001
YB 1100
YCD OFF
J 41
H 00
LSTOR LOC 41 0A01
MS LOC 0A01 0A0A

FIGURE 10

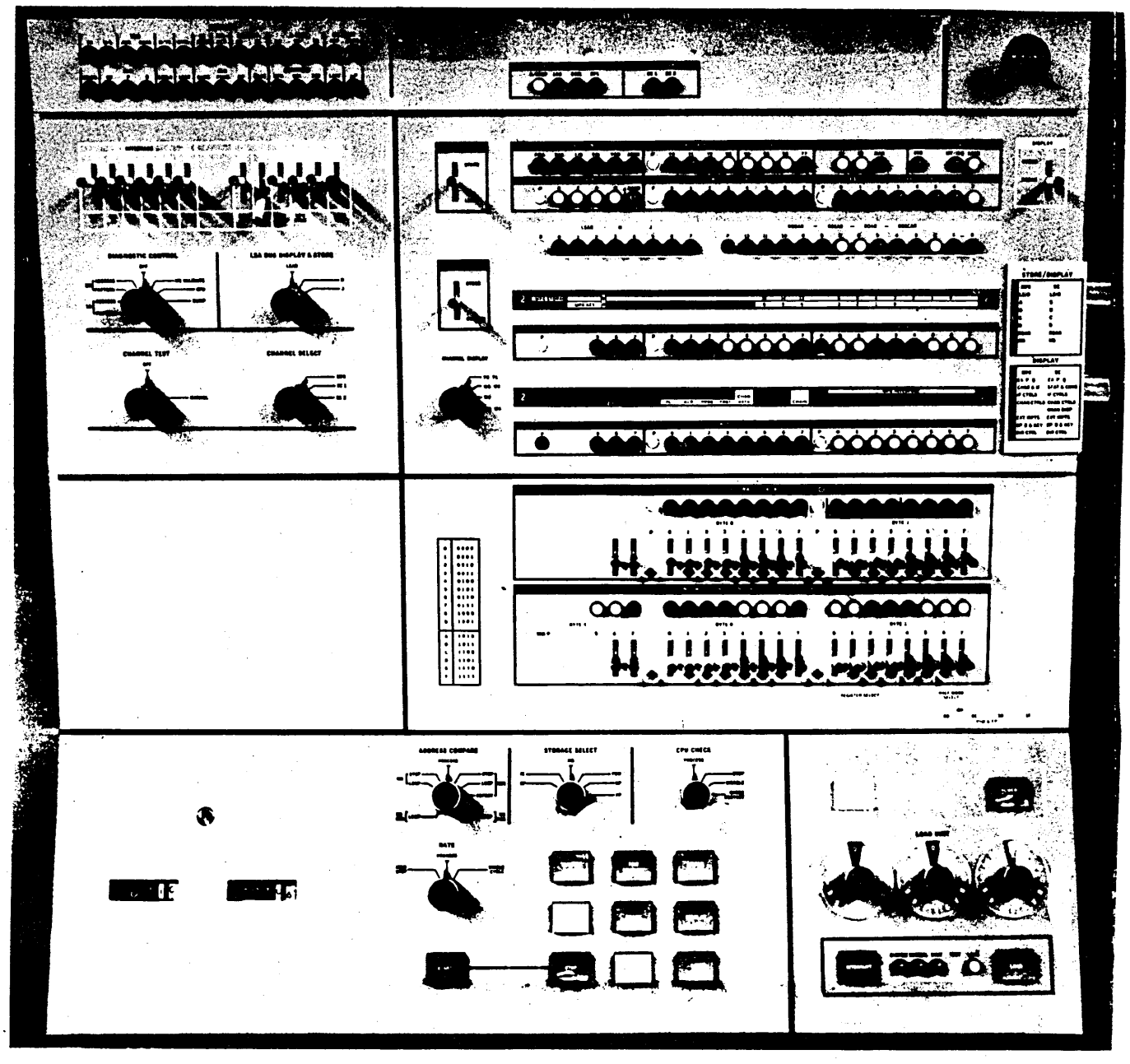
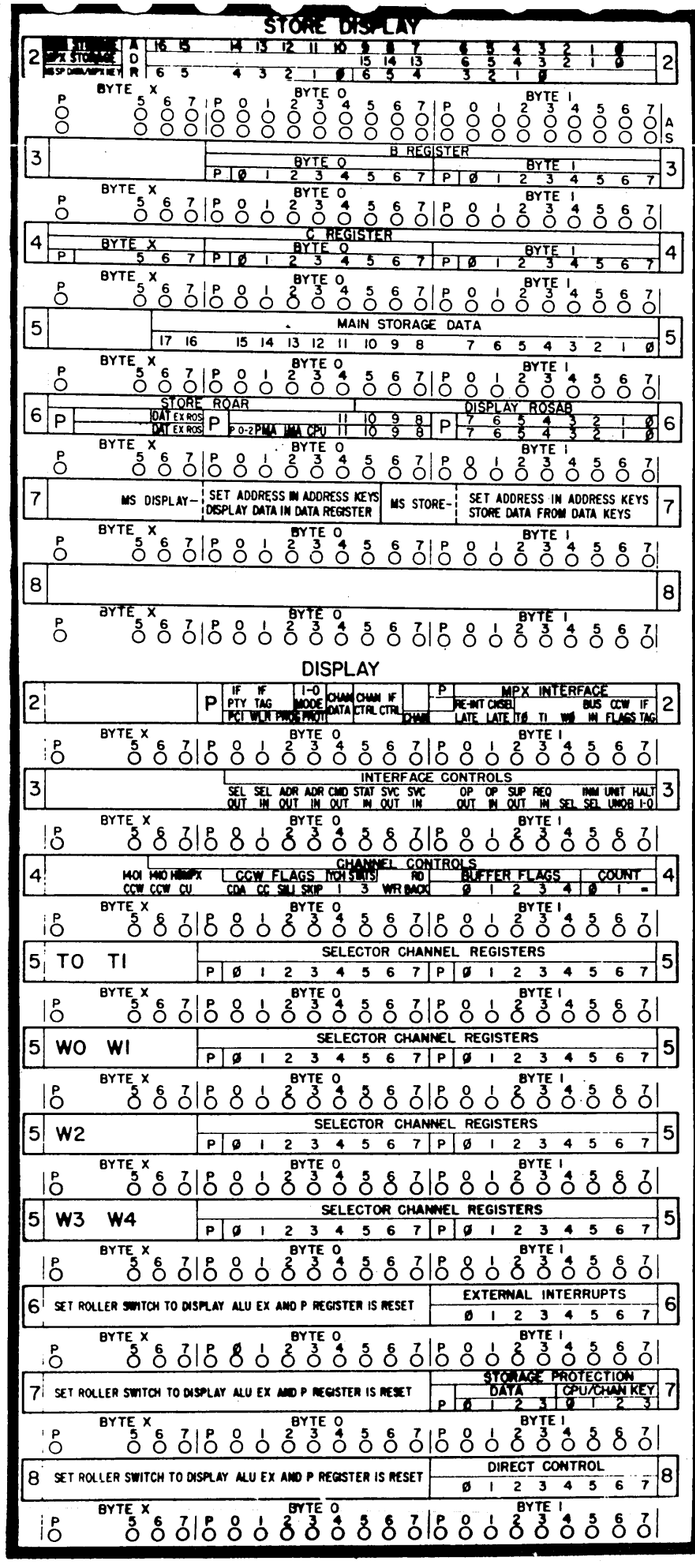
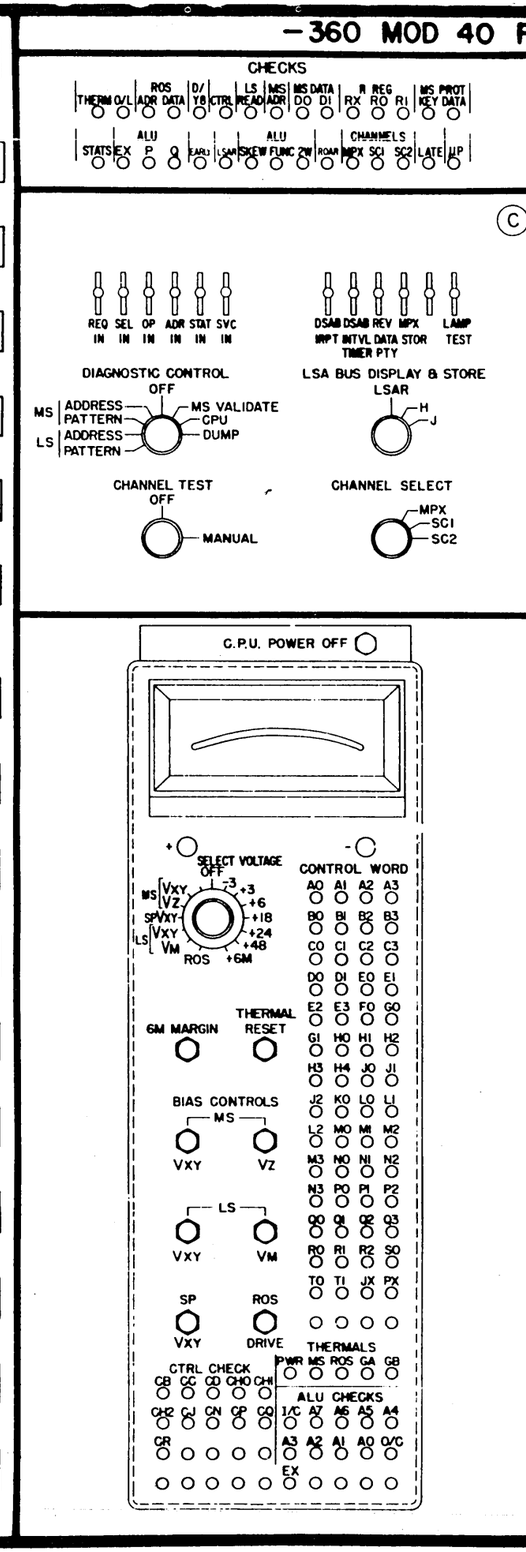


FIGURE 11





—360 MOD 40 FAILURE SYMPTOMS DISPLAY—

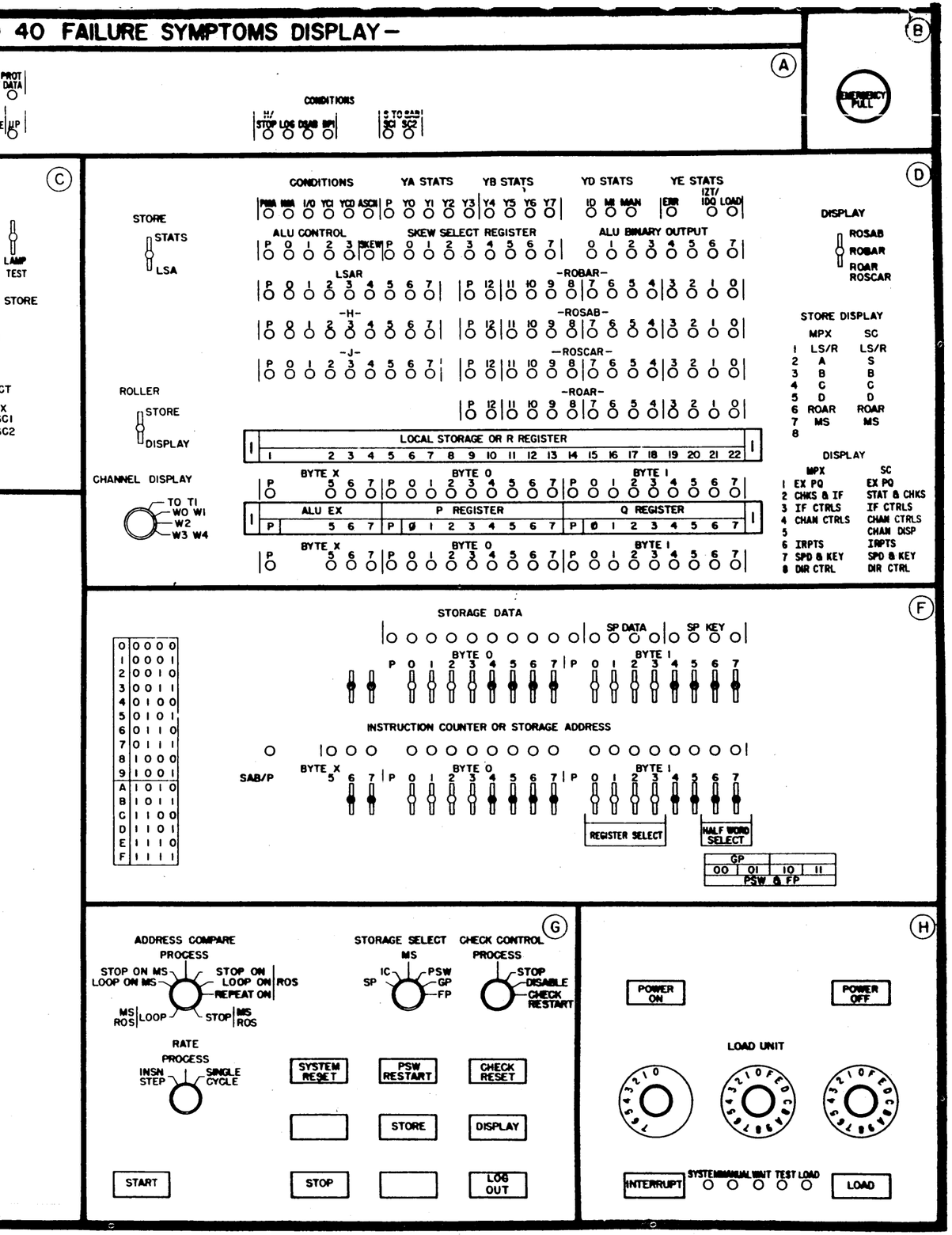


FIGURE 12

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

STORE DISPLAY

2 — MPX STORAGE / SEL STORAGE / MS SP DATA/KEY/MPX — A D R — 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — 15 14 13 6 5 4 3 2 1 0 — 6 5 4 3 2 1 0 — 2

BYTE X | BYTE 0 | BYTE 1 — P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7 — A S

3 — B REGISTER — 3

4 — C REGISTER — 4

5 — MAIN STORAGE DATA — 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — 5

6 — STORE ROAR — DAT EX ROS / DAT EX ROS — P 0-2 PMA MRA I/O YCU — DISPLAY ROSAB — 6

7 — MS DISPLAY- — SET ADDRESS IN ADDRESS KEYS / DISPLAY DATA IN DATA REGISTER — MS STORE- — SET ADDRESS IN ADDRESS KEYS / STORE DATA FROM DATA KEYS — 7

8

DISPLAY

2 — IF PTY TAG PCI WLR — IF PROG PROT — I-O MODE — CHAN DATA — CHAN CTRL — IF CHAN — MPX INTERFACE: PRE-INT LATE — CHSEL LATE — BUS TO — CCW TI — IF WD — IF IN — FLAGS TAG — 2

3 — INTERFACE CONTROLS: SEL OUT — SEL IN — ADR OUT — ADR IN — CMD OUT — STAT IN — SVC OUT — SVC IN — OP OUT — OP IN — SUP OUT — REQ IN — INH SEL — UNIT SEL — HALT I-O — 3

4 — CHANNEL CONTROLS: M40 CCW — M40 CCW — MPX CU — CCW FLAGS: CDA — CC — SLI — SKIP — TCH 1 — STATS 3 — WR — RD BACK — BUFFER FLAGS: Ø 1 2 3 4 — COUNT: Ø 1 = — 4

5 TO TI — SELECTOR CHANNEL REGISTERS — 5

5 W0 W1 — SELECTOR CHANNEL REGISTERS — 5

5 W2 — SELECTOR CHANNEL REGISTERS — 5

5 W3 W4 — SELECTOR CHANNEL REGISTERS — 5

6 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — EXTERNAL INTERRUPTS: Ø 1 2 3 4 5 6 7 — 6

7 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — STORAGE PROTECTION: DATA P Ø 1 2 3 — CPU/CHAN KEY Ø 1 2 3 — 7

8 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — DIRECT CONTROL: Ø 1 2 3 4 5 6 7 — 8

BYTE X | BYTE 0 | BYTE 1 — P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

CHECKS

THERM | O/L | ROS ADR | ROS DATA | D/ Y8 | CTRL | LS READ | MS ADR | MS DATA DO | MS DATA DI | R REG RX | R REG RO | R REG RI | MS PROT KEY | MS PROT DATA

ALU STATS | ALU EX | ALU P | ALU Q | ALU EARL | ALU LSAR | ALU SKEW | ALU FUNC | ALU 2W | ALU ROAR | CHANNELS MPX | CHANNELS SCI | CHANNELS SC2 | CHANNELS LATE | CHANNELS UP

CONDITIONS

H/ STOP | LOG | DSAB | BPT | S TO SAB SCI | S TO SAB SC2

(A) (B)

EMERGENCY PULL

(C)

REQ IN | SEL IN | OP IN | ADR IN | STAT IN | SVC IN

DSAB MPT | DSAB INTVL TIMER | REV DATA | MPX STOR PTY | LAMP TEST

DIAGNOSTIC CONTROL — OFF — MS: ADDRESS PATTERN — LS: ADDRESS PATTERN — MS VALIDATE — CPU — DUMP

LSA BUS DISPLAY & STORE — LSAR — H — J

CHANNEL TEST — OFF — MANUAL

CHANNEL SELECT — MPX — SCI — SC2

G.P.U. POWER OFF

SELECT VOLTAGE — OFF — -3 — +3 — +6 — +18 — +24 — +48 — +6M — MS: VXY VZ — SP VXY — LS: VXY VM — ROS

6M MARGIN — THERMAL RESET

BIAS CONTROLS — MS: VXY VZ — LS: VXY VM — SP VXY — ROS DRIVE

CONTROL WORD

A0	A1	A2	A3
B0	B1	B2	B3
C0	C1	C2	C3
D0	D1	E0	E1
E2	E3	F0	G0
G1	H0	H1	H2
H3	H4	J0	J1
J2	K0	L0	L1
L2	M0	M1	M2
M3	N0	N1	N2
N3	P0	P1	P2
Q0	Q1	Q2	Q3
R0	R1	R2	S0
T0	T1	JX	PX

THERMALS: PWR | MS | ROS | GA | GB

CTRL CHECK: CB | CC | CD | CHO | CHI | CH2 | CJ | CN | CP | CQ | CR

ALU CHECKS: 1/C | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | O/C | EX

(D)

CONDITIONS: PMA | MRA | I/O | YCU | YCD | ASCH

YA STATS: P | Y0 | Y1 | Y2 | Y3

YB STATS: Y4 | Y5 | Y6 | Y7

YD STATS: ID | MI | MAN

YE STATS: ERR | IZT/IDQ | LOAD

ALU CONTROL: P | 0 | 1 | 2 | 3 | SKEW

SKEW SELECT REGISTER: P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

ALU BINARY OUTPUT: 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

LSAR: P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

-ROBAR-: P | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0

-H-: P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

-ROSAB-: P | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0

-J-: P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7

-ROSCAR-: P | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0

-ROAR-: P | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0

STORE — STATS — LSA

ROLLER — STORE — DISPLAY

CHANNEL DISPLAY — TO TI — WO WI — W2 — W3 W4

LOCAL STORAGE OR R REGISTER: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

BYTE X | BYTE 0 | BYTE 1 — P | 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

ALU EX | P REGISTER | Q REGISTER — P | 5 6 7 | P Ø 1 2 3 4 5 6 7 | P Ø 1 2 3 4 5 6 7

BYTE X | BYTE 0 | BYTE 1 — P | 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

DISPLAY — ROSAB — ROBAR — ROAR ROSCAR

STORE DISPLAY

	MPX	SC
1	LS/R	LS/R
2	A	S
3	B	B
4	C	C
5	D	D
6	ROAR	ROAR
7	MS	MS
8		

DISPLAY

	MPX	SC
1	EX PQ	EX PQ
2	CHKS & IF	STAT & CHKS
3	IF CTRLS	IF CTRLS
4	CHAN CTRLS	CHAN CTRLS
5		CHAN DISP
6	IRPTS	IRPTS
7	SPD & KEY	SPD & KEY
8	DIR CTRL	DIR CTRL

(F)

STORAGE DATA — SP DATA — SP KEY — BYTE 0 | BYTE 1 — P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

INSTRUCTION COUNTER OR STORAGE ADDRESS

SAB/P — BYTE X | BYTE 0 | BYTE 1 — 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

REGISTER SELECT — HALF WORD SELECT

GP			
00	01	10	11
PSW & FP			

(G)

ADDRESS COMPARE — PROCESS — STOP ON MS LOOP ON MS — STOP ON LOOP ON REPEAT ON ROS — MS ROS LOOP — STOP MS ROS

STORAGE SELECT — MS — IC — PSW — SP — GP — FP

CHECK CONTROL — PROCESS — STOP — DISABLE — CHECK RESTART

RATE — PROCESS — INSN STEP — SINGLE CYCLE

SYSTEM RESET | PSW RESTART | CHECK RESET

STORE | DISPLAY

START | STOP | LOG OUT

(H)

POWER ON | POWER OFF

LOAD UNIT — 7 6 5 4 3 2 1 0 — F E D C B A 9 8

INTERRUPT | SYSTEM MANUAL WAIT TEST LOAD | LOAD

FIGURE 13

	ENTER ADDRESS INTO ADDRESS KEYS	ENTER ADDRESS INTO DATA KEYS	STORE/DISPLAY SWITCH POSITION	DISPLAY ROLLER SWITCH POSITION	CHANNEL DISPLAY SWITCH POSITION	CHANNEL SELECT SWITCH POSITION	SETTING OF LSA BUS DISPLAY & STORE	MPX STOR TOGGLE SWITCH DOWN	ROLLER TOGGLE SWITCH ON DISPLAY	DISPLAY TOGGLE SWITCH SETTING	MUST BE DISPLAYED FIRST OR IS WIPED OUT	ROLLER TOGGLE SWITCH ON DISPLAY WILL WIPE OUT THIS READING
R REGISTER *			1						X		X	X
LOCAL STORAGE **	X		1						X			
A REGISTER			2									
B REGISTER			3									
C REGISTER			4									
D REGISTER			5									
ROAR			6						X			
MAIN STOR DATA	X		7									X
ALU EX, P, Q			NOT 1	1								
MPX CHECKS & IF			NOT 1	2		MPX						
IF CONTROLS			NOT 1	3		ROTATE						
CHANNEL CONTROLS			NOT 1	4		SC1 / SC2						
EXT INTERRUPTS			NOT 1	6					X			
SP DATA & REG			NOT 1	7					X			
DIRECT CONTROL			NOT 1	8					X			
ROSAB										ROSAB		
ROBAR ***										ROBAR	X	
LSAR							LSAR				X	
H REGISTER							H					
J REGISTER							J					
MPX STORAGE	X		7					X	X			
TO – T1			NOT 1	5	TO / T1	SC1 / SC2						
W0 – W1			NOT 1	5	W0 / W1	SC1 / SC2						
W2			NOT 1	5	W2	SC1 / SC2						
W3 – W4			NOT 1	5	W3 / W4	SC1 / SC2						
S REGISTER			2			SC1 / SC2						
ROSCAR						SC1 / SC2				ROAR / ROSCAR		
SP KEY ****			NOT 1	5	W2	SC1 / SC2						
ROAR						MPX				ROAR / ROSCAR		
SC CHECKS & IF			NOT 1	4		SC1 / SC2						
W BUFFER FLAGS												

* IF THE STORE DISPLAY ROLLER SWITCH WAS ON POSITION 1 BEFORE STOPPING, THE ACTUAL CONTENT OF R REGISTER WILL BE DISPLAYED. IN EVERY OTHER POSITION, THE CONTENT OF THE R REGISTER WILL BE DESTROYED.

** (THE CONTENT OF LSAR WILL BE CHANGED).

*** THE CONTENT OF ROBAR WILL BE DESTROYED IF ROBAR DISPLAY TOGGLE SWITCH IS SET OUT OF POSITION ROBAR.

**** TO DISPLAY THE STORAGE PROTECT KEY CORRESPONDING TO A PARTICULAR AREA OF MAIN STORAGE OR TO A PARTICULAR UCW, DISPLAY ONE POSITION OF THIS AREA FIRST. (REFER TO "MAIN STORAGE DATA" OR "MULTIPLEX STORAGE" ABOVE.) AFTER SETTING THE ABOVE CONDITIONS, THIS KEY WILL APPEAR IN THE SP DATA REGISTER POSITIONS.

NOTE: THE P BIT APPEARING ON THIS POSITION OF THE LOWER ROLL CHART IS THE RESULT OF EXCLUSIVE ORING (NOT SPLS DATA PARITY, AND SP KEY PARITY.)

DISPLAYING PROCEDURE WHEN IN HARDSTOP CONDITION

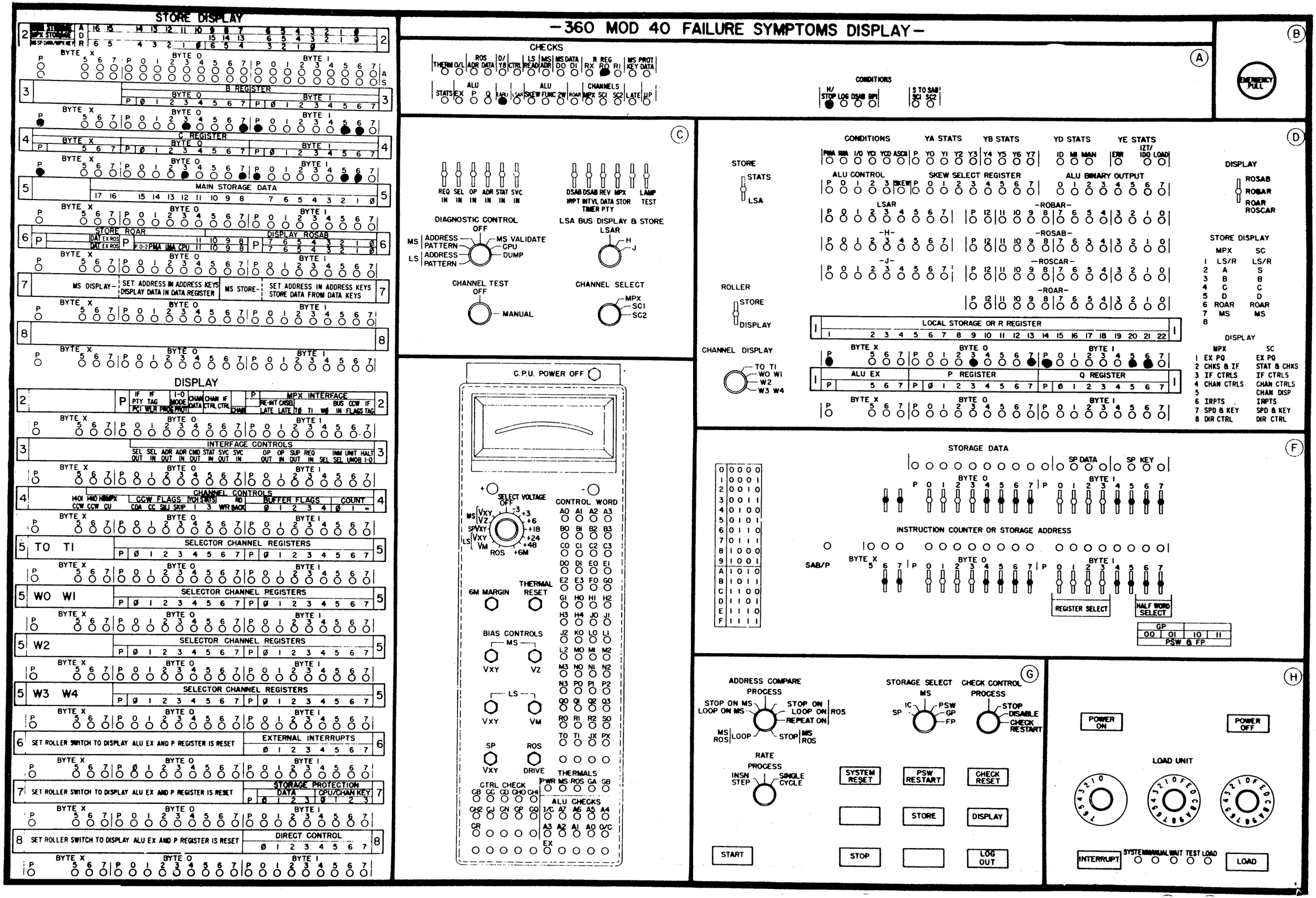
FIGURE 15

	ENTER DATA INTO DATA KEYS	ENTER DATA INTO ADDRESS KEYS	ENTER ADDRESS INTO DATA KEYS	ENTER ADDRESS INTO ADDRESS KEYS		SETTING OF LSA BUS DISPLAY AND STORE SWITCH	STORE TOGGLE SWITCH SETTING	MPX STOR KEY	STORE / DISPLAY ROLLER SWITCH POSITION	ROLLER TOGGLE SWITCH TO STORE
A REGISTER	X								2	X
B REGISTER	X								3	X
C REGISTER	X								4	X
D REGISTER	X								5	X
R REGISTER	X								1	X
LOCAL STORAGE	X			X					1	X
LSAR		X				LSAR	LSA			
H REGISTER		X				H	LSA			
J REGISTER		X				J	LSA			
Y STATS *	X						STATS			
MAIN STORAGE DATA	X			X					7	X
MPX STORAGE	X			X				X	7	X
ROAR			X						6	X

* Y 14 (IZT/IDQ) CANNOT BE STORED MANUALLY

STORING PROCEDURE WHEN IN HARDSTOP CONDITION

FIGURE 14


STORE DISPLAY
DISPLAY
INTERFACE CONTROLS
CHANNEL CONTROLS
SELECTOR CHANNEL REGISTERS
EXTERNAL INTERRUPTS
STORAGE PROTECTION
DIRECT CONTROL
SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET
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DIAGNOSTIC CONTROL
LSA BUS DISPLAY & STORE
CHANNEL TEST
CHANNEL SELECT
C.P.U. POWER OFF
SELECT VOLTAGE
CONTROL WORD
THERMALS
ALU CHECKS
BIAS CONTROLS
6M MARGIN
THERMAL RESET
STORE
ROLLER
CHANNEL DISPLAY
LOCAL STORAGE OR R REGISTER
STORAGE DATA
SP DATA
SP KEY
INSTRUCTION COUNTER OR STORAGE ADDRESS
REGISTER SELECT
HALF WORD SELECT
ADDRESS COMPARE
STORAGE SELECT
CHECK CONTROL
RATE
SYSTEM RESET
PSW RESTART
CHECK RESET
STORE
DISPLAY
LOG OUT
START
STOP
POWER ON
POWER OFF
LOAD UNIT
INTERRUPT
LOAD

FIGURE 16

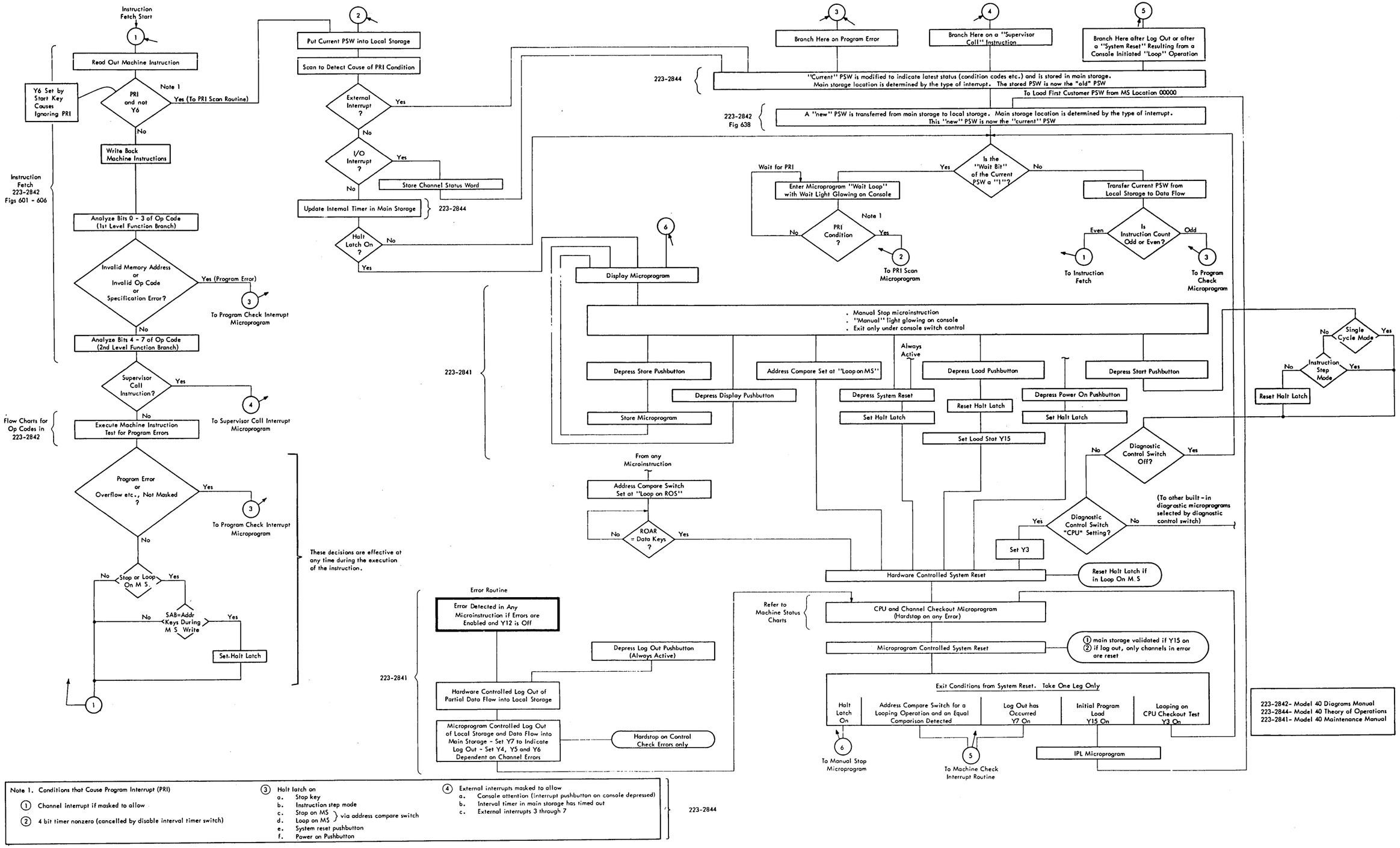
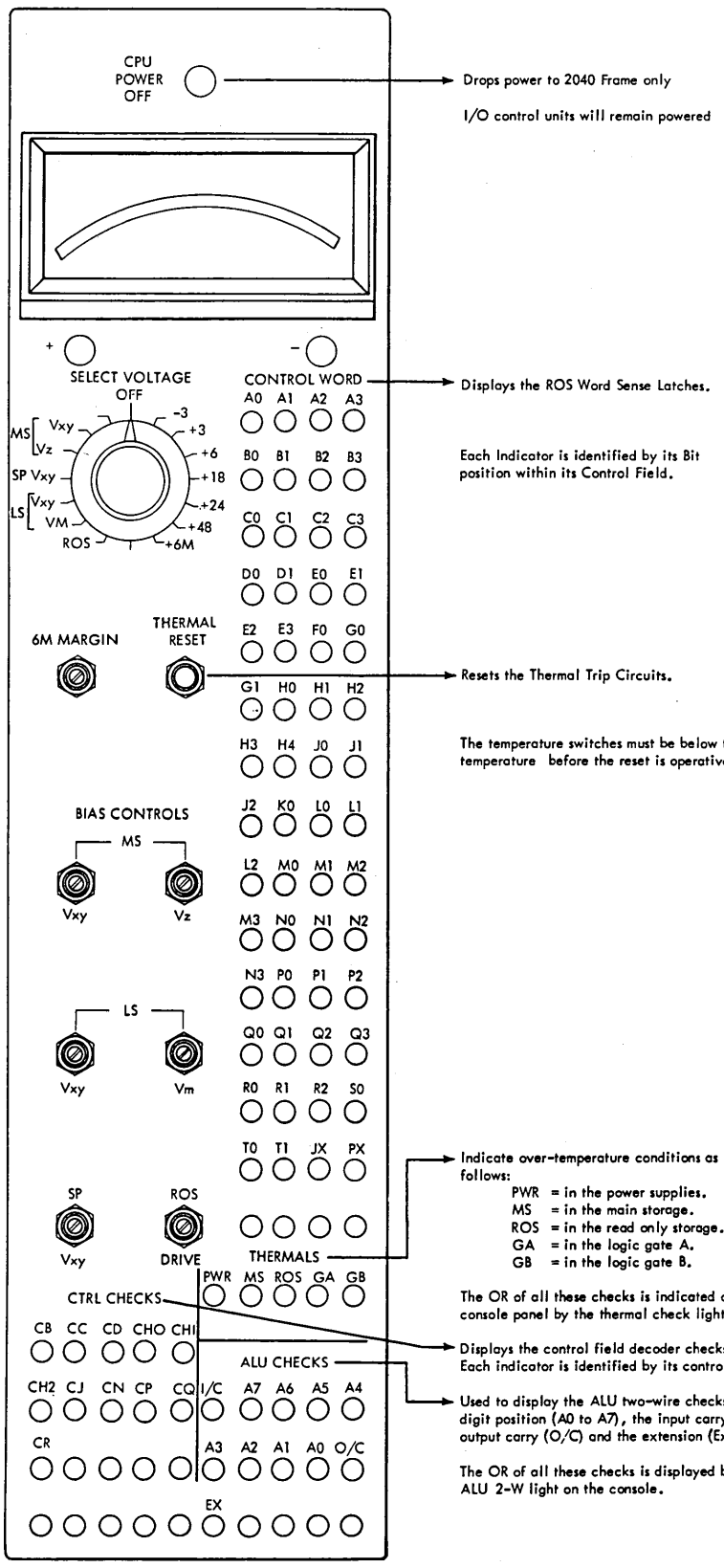


FIGURE 17

CPU MICROPROGRAM FLOW CHART (CHANNEL DATA SERVICE NOT SHOWN)



Model 40 Internal Console Panel (HF)

FIGURE 18

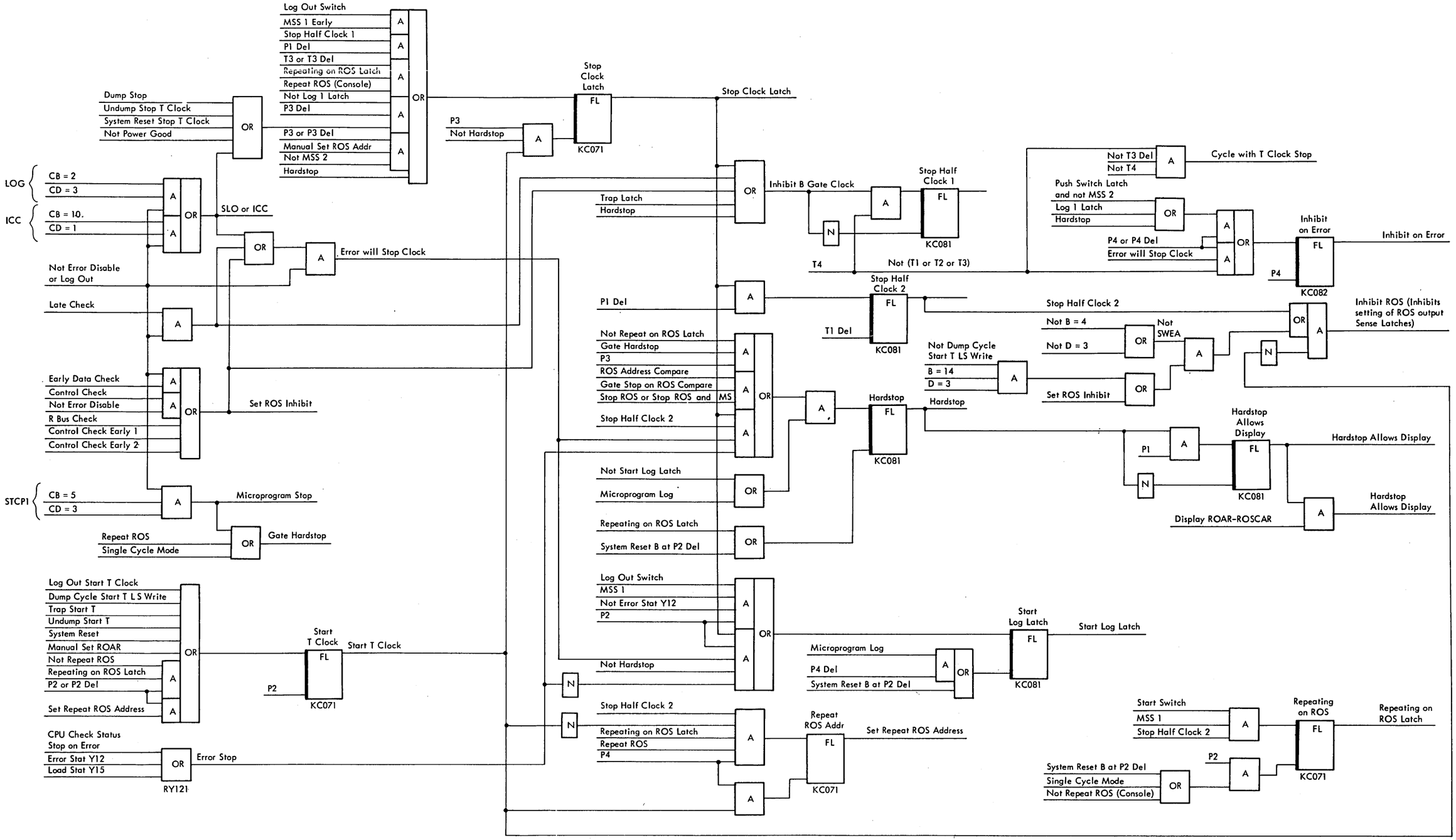
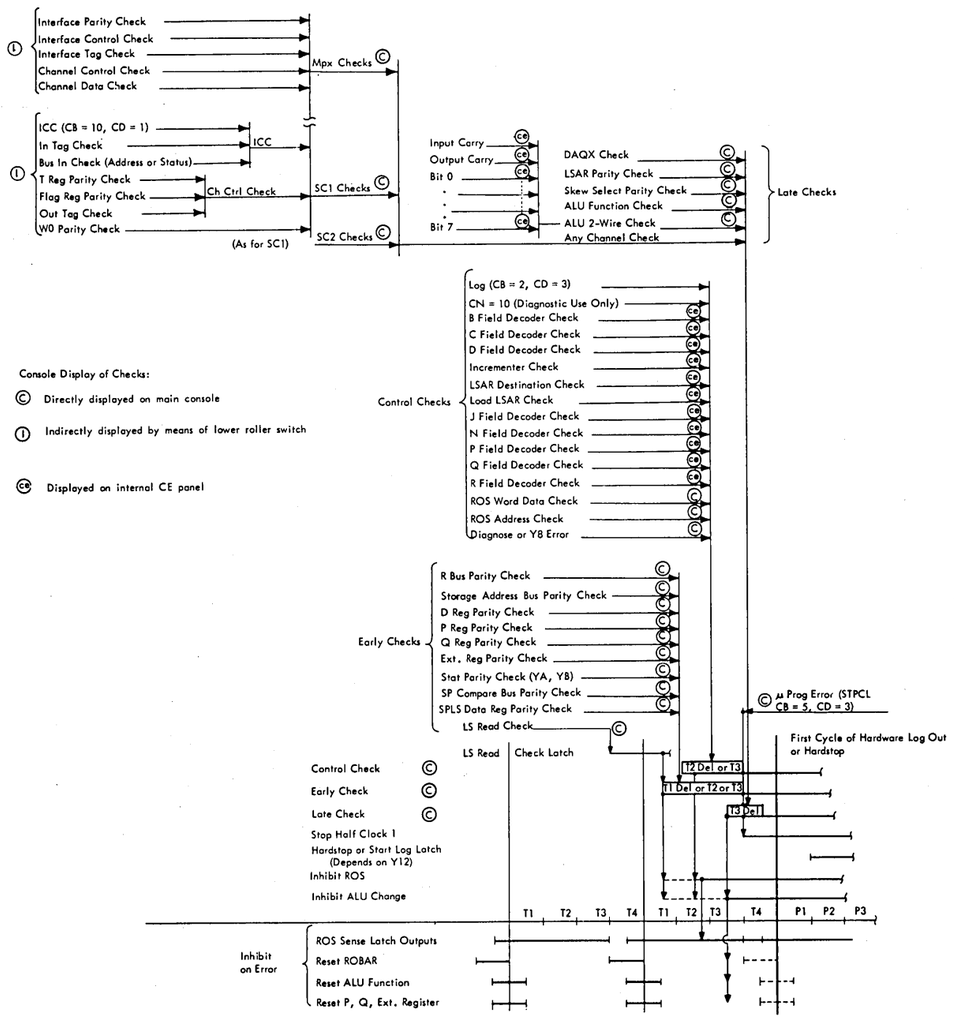


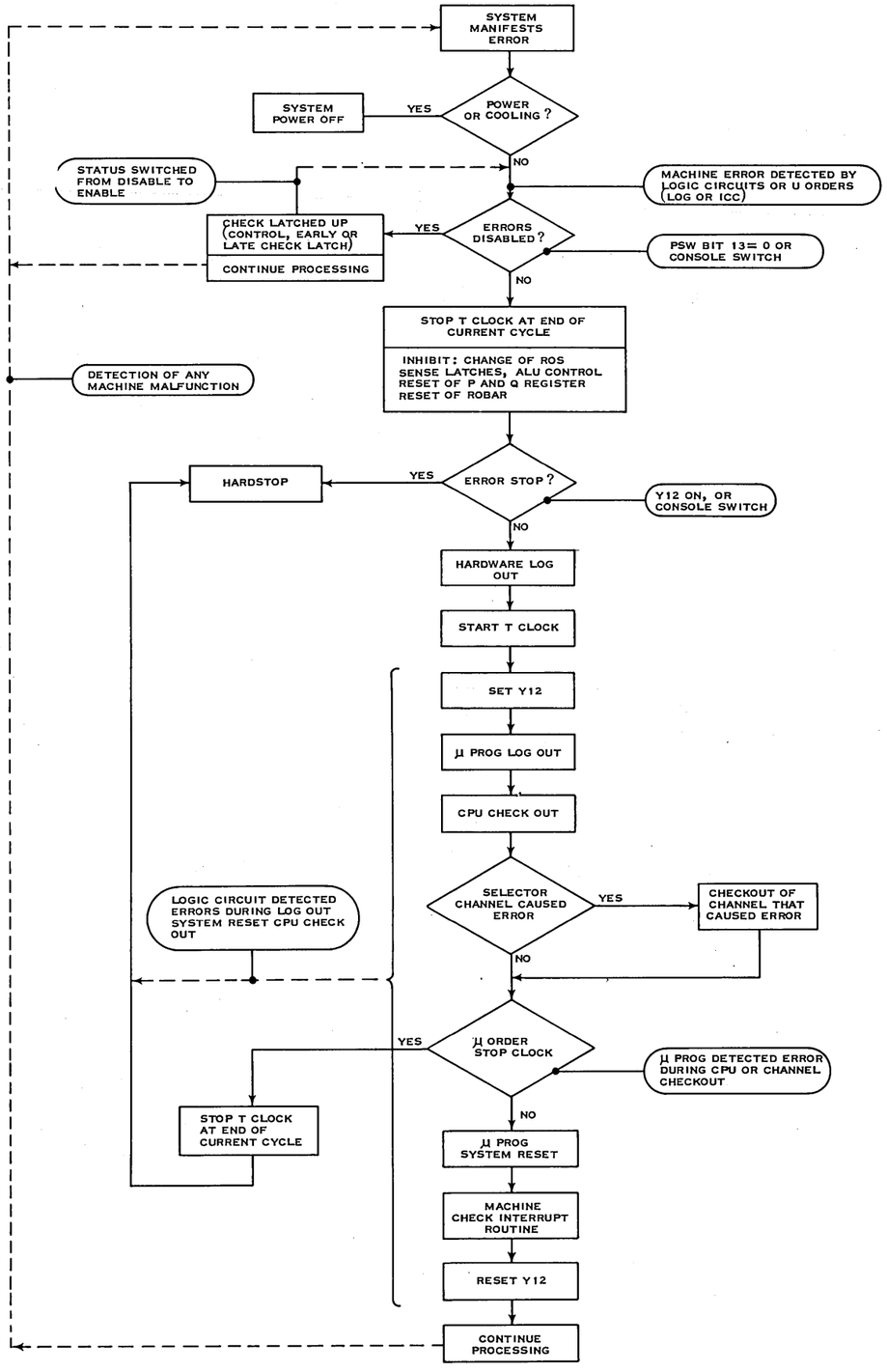
FIGURE 19

CLOCK CONTROL (KC071-KC081)



Checks in Relation to Timing

FIGURE 21



SYSTEM OPERATION AFTER ERROR DETECTION

FIGURE 20

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

STORE DISPLAY

2 — MAIN STORAGE / MPX STORAGE / MS SP DATA/MPX KEY — A D R — BYTE X / BYTE O / BYTE I — P — A S

3 — B REGISTER — BYTE O / BYTE I

4 — C REGISTER — BYTE X / BYTE O / BYTE I

5 — MAIN STORAGE DATA — 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 Ø

6 — STORE ROAR — DAT EX ROS / DAT EX ROS — P 0-2 PMA MMA CPU — DISPLAY ROSAB

7 — MS DISPLAY- SET ADDRESS IN ADDRESS KEYS, DISPLAY DATA IN DATA REGISTER — MS STORE- SET ADDRESS IN ADDRESS KEYS, STORE DATA FROM DATA KEYS

8 —

DISPLAY

2 — P — IF PTY TAG PCI — IF WLR PMCK — I-O MODE PROT — CHAN DATA — CHAN CTRL — CHAN IF CTRL — CHAN — P — MPX INTERFACE — RE-INT CHSEL LATE — ADR LATE — ITG — TI — WG — BUS IN — CCW FLAGS — IF TAG

3 — INTERFACE CONTROLS — SEL OUT — SEL IN — ADR OUT — ADR IN — CMD OUT — STAT IN — SVC OUT — SVC IN — OP OUT — OP IN — SUP OUT — REQ IN — SEL — IMM SEL — UNIT UNQS — HALT I-O

4 — CHANNEL CONTROLS — HIO CCW — HIO CU — MPX — CCW FLAGS CDA CC SILI SKIP — ITCH STATS 1 3 — WRT BACK — RD BACK — BUFFER FLAGS Ø 1 2 3 4 — COUNT Ø 1 =

5 — SELECTOR CHANNEL REGISTERS — TO TI

5 — SELECTOR CHANNEL REGISTERS — WO WI

5 — SELECTOR CHANNEL REGISTERS — W2

5 — SELECTOR CHANNEL REGISTERS — W3 W4

6 — EXTERNAL INTERRUPTS — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET

7 — STORAGE PROTECTION — DATA — CPU/CHAN KEY — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET

8 — DIRECT CONTROL — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET

CHECKS

THERM O/L | ROS ADR DATA | D/Y8 CTRL | LS READ | MS ADR | MS DATA DO DI | R REG RX RO RI | MS PROT KEY DATA

STATS | EX P Q | ALU EARL SAR SKEW FUNC 2W | ROAR | CHANNELS MPX SCI SC2 | LATE | U/P

CONDITIONS

U/C STOP LOG DSAB DPI | S TO SAB SCI SC2

EMERGENCY PULL

C

REQ IN | SEL IN | OP IN | ADR IN | STAT IN | SVC IN

DSAB MPT | DSAB INTVL | REV DATA TIMER | MPX STOR PTY | LALGP TEST

DIAGNOSTIC CONTROL — OFF — MS ADDRESS / MS PATTERN — LS ADDRESS / LS PATTERN — MS VALIDATE — CPU — DUMP

LSA BUS DISPLAY & STORE — LSAR — H — J

CHANNEL TEST — OFF — MANUAL

CHANNEL SELECT — MPX — SCI — SC2

C.P.U. POWER OFF

SELECT VOLTAGE — OFF — -3 — +3 — +6 — +18 — +24 — +48 — +6M — MS VXY VZ — SP VXY VXY VM — LS — ROS

CONTROL WORD

A0	A1	A2	A3	
B0	B1	B2	B3	
C0	C1	C2	C3	
D0	D1	E0	E1	
E2	E3	F0	G0	
G1	H0	H1	H2	
H3	H4	J0	J1	
J2	K0	L0	L1	
L2	M0	M1	M2	
M3	N0	N1	N2	
N3	P0	P1	P2	
Q0	Q1	Q2	Q3	
R0	R1	R2	S0	
T0	T1	J X	P X	

6M MARGIN — THERMAL RESET

BIAS CONTROLS — MS — VXY — VZ — LS — VXY — VM — SP — VXY — ROS — DRIVE

THERMALS — PWR MS ROS GA GB

CTRL CHECK — CB CC CD CHO CHI — CH2 CJ CN CP CQ — CR

ALU CHECKS — I/C A7 A6 A5 A4 — A3 A2 A1 A0 O/C — EX

D

CONDITIONS — PMA MMA I/O YCI YCO ASCH — YA STATS P Y0 Y1 Y2 Y3 — YB STATS Y4 Y5 Y6 Y7 — YD STATS ID MI MAN — YE STATS ERR — IZT/IDQ LOAD

STORE — STATS — LSA

ALU CONTROL — P 0 1 2 3 SKEW

SKEW SELECT REGISTER — P 0 1 2 3 4 5 6 7

ALU BINARY OUTPUT — 0 1 2 3 4 5 6 7

LSAR — P 0 1 2 3 4 5 6 7 — P 12 11 10 9 8 7 6 5 4 3 2 1 0

-H- — P 0 1 2 3 4 5 6 7 — P 12 11 10 9 8 7 6 5 4 3 2 1 0

-J- — P 0 1 2 3 4 5 6 7 — P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROAR- — P 12 11 10 9 8 7 6 5 4 3 2 1 0

ROLLER — STORE — DISPLAY

CHANNEL DISPLAY — TO TI — WO WI — W2 — W3 W4

1 — LOCAL STORAGE OR R REGISTER — 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

BYTE X / BYTE O / BYTE I — P — 5 6 7 — P 0 1 2 3 4 5 6 7 — P 0 1 2 3 4 5 6 7

1 — ALU EX — P REGISTER — Q REGISTER — P — 5 6 7 — P Ø 1 2 3 4 5 6 7 — P Ø 1 2 3 4 5 6 7

BYTE X / BYTE O / BYTE I — P Ø — 5 6 7 — P 0 1 2 3 4 5 6 7 — P 0 1 2 3 4 5 6 7

DISPLAY — ROSAB — ROBAR — ROAR — ROSCAR

STORE DISPLAY

	MPX	SC
1	LS/R	LS/R
2	A	S
3	B	B
4	C	C
5	D	D
6	ROAR	ROAR
7	MS	MS
8		

DISPLAY

	MPX	SC
1	EX PQ	EX PQ
2	CHKS & IF	STAT & CHKS
3	IF CTRLS	IF CTRLS
4	CHAN CTRLS	CHAN CTRLS
5		CHAN DISP
6	IRPTS	IRPTS
7	SPD & KEY	SPD & KEY
8	DIR CTRL	DIR CTRL

F

STORAGE DATA — SP DATA — SP KEY — BYTE O — P 0 1 2 3 4 5 6 7 — P — BYTE I — 0 1 2 3 4 5 6 7

INSTRUCTION COUNTER OR STORAGE ADDRESS

SAB/P — BYTE X — 5 6 7 — BYTE O — P 0 1 2 3 4 5 6 7 — P — BYTE I — 0 1 2 3 4 5 6 7

REGISTER SELECT — HALF WORD SELECT

GP			
00	01	10	11
PSW & FP			

G

ADDRESS COMPARE PROCESS — STOP ON MS LOOP ON MS — STOP ON LOOP ON ROS REPEAT ON — MS ROS LOOP — STOP MS ROS

STORAGE SELECT — MS — IC — PSW — SP — GP — FP

CHECK CONTROL PROCESS — STOP DISABLE CHECK RESTART

RATE PROCESS — INSN STEP — SINGLE CYCLE

SYSTEM RESET | PSW RESTART | CHECK RESET

STORE | DISPLAY

START | STOP | LOG OUT

H

POWER ON | POWER OFF

LOAD UNIT — 7 6 5 4 3 2 1 0 — F E D C B A 9 8 — F E D C B A 9 8 7 6 5 4 3 2 1 0

INTERRUPT | SYSTEM/MANUAL UNIT TEST LOAD | LOAD

FIGURE 22

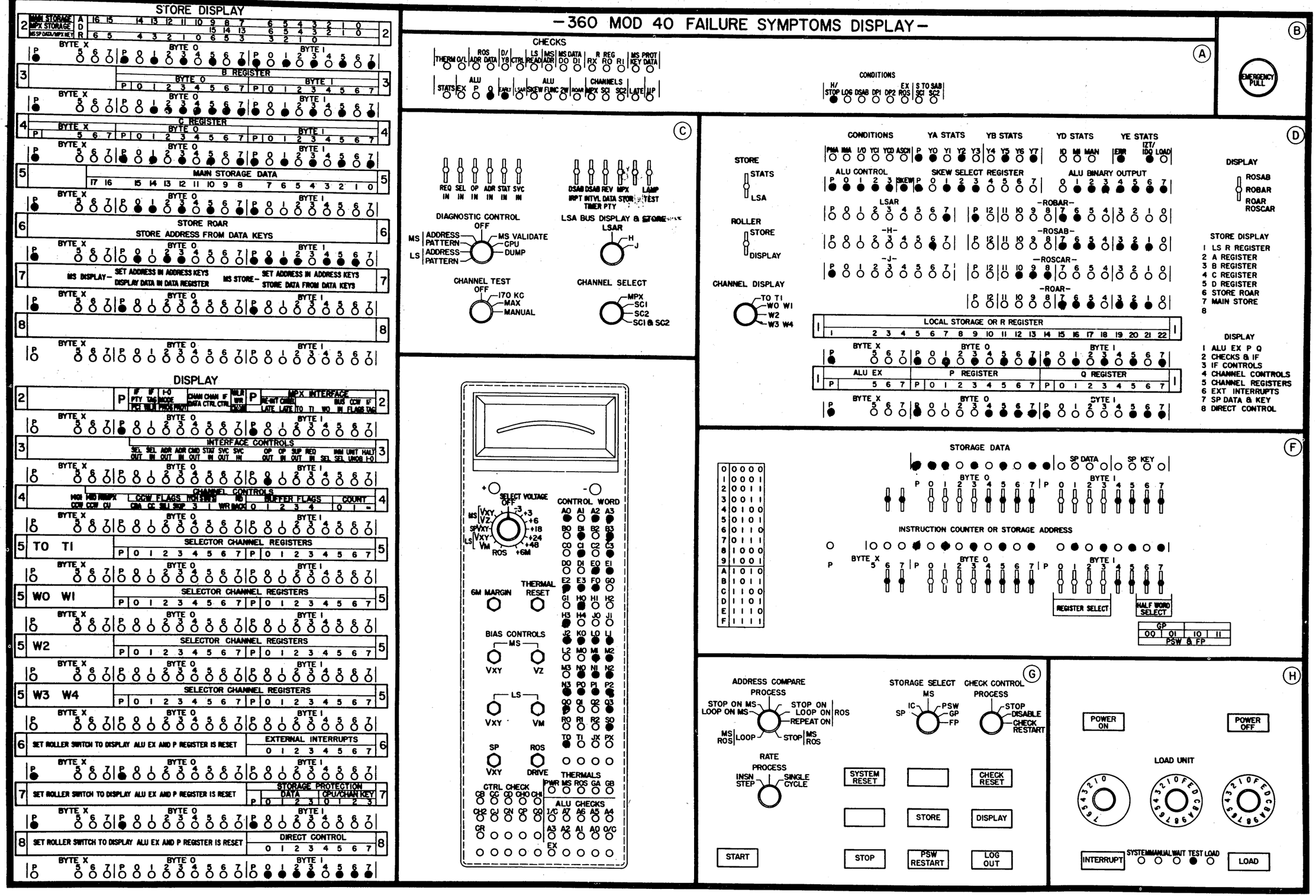

STORE DISPLAY
MAIN STORAGE
MPX STORAGE
MS SP DATA/MPX KEY
A
D
R
BYTE X
BYTE O
BYTE I
B REGISTER
C REGISTER
MAIN STORAGE DATA
STORE ROAR
STORE ADDRESS FROM DATA KEYS
MS DISPLAY– SET ADDRESS IN ADDRESS KEYS DISPLAY DATA IN DATA REGISTER
MS STORE– SET ADDRESS IN ADDRESS KEYS STORE DATA FROM DATA KEYS
DISPLAY
MPX INTERFACE
INTERFACE CONTROLS
CHANNEL CONTROLS
SELECTOR CHANNEL REGISTERS
TO TI
WO WI
W2
W3 W4
SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET
EXTERNAL INTERRUPTS
STORAGE PROTECTION
DIRECT CONTROL
–360 MOD 40 FAILURE SYMPTOMS DISPLAY–
CHECKS
CONDITIONS
A
B
EMERGENCY PULL
C
REQ SEL OP ADR STAT SVC IN
DSAB DSAB REV MPX LAMP IRPT INTVL DATA STOR TEST TIMER PTY
DIAGNOSTIC CONTROL
MS ADDRESS PATTERN
LS ADDRESS PATTERN
OFF
MS VALIDATE
CPU
DUMP
LSA BUS DISPLAY & STORE
LSAR
CHANNEL TEST
I70 KC
MAX
MANUAL
CHANNEL SELECT
MPX
SCI
SC2
SCI & SC2
SELECT VOLTAGE
+3
+6
+18
+24
+48
ROS +6M
CONTROL WORD
6M MARGIN
THERMAL RESET
BIAS CONTROLS
VXY
VZ
SP
ROS
DRIVE
CTRL CHECK
ALU CHECKS
THERMALS
D
STORE
STATS
LSA
ROLLER
STORE
DISPLAY
CHANNEL DISPLAY
TO TI
WO WI
W2
W3 W4
CONDITIONS
YA STATS
YB STATS
YD STATS
YE STATS
ALU CONTROL
SKEW SELECT REGISTER
ALU BINARY OUTPUT
LSAR
–ROBAR–
–H–
–ROSAB–
–J–
–ROSCAR–
–ROAR–
LOCAL STORAGE OR R REGISTER
ALU EX
P REGISTER
Q REGISTER
DISPLAY
ROSAB
ROBAR
ROAR
ROSCAR
STORE DISPLAY
1 LS R REGISTER
2 A REGISTER
3 B REGISTER
4 C REGISTER
5 D REGISTER
6 STORE ROAR
7 MAIN STORE
8
DISPLAY
1 ALU EX P Q
2 CHECKS & IF
3 IF CONTROLS
4 CHANNEL CONTROLS
5 CHANNEL REGISTERS
6 EXT INTERRUPTS
7 SP DATA & KEY
8 DIRECT CONTROL
F
STORAGE DATA
SP DATA
SP KEY
INSTRUCTION COUNTER OR STORAGE ADDRESS
REGISTER SELECT
HALF WORD SELECT
GP
PSW & FP
G
ADDRESS COMPARE PROCESS
STOP ON MS
LOOP ON MS
STOP ON LOOP ON
REPEAT ON
ROS
LOOP
STOP
RATE PROCESS
INSN STEP
SINGLE CYCLE
STORAGE SELECT
MS
IC
SP
PSW
GP
FP
CHECK CONTROL PROCESS
STOP
DISABLE
CHECK RESTART
SYSTEM RESET
CHECK RESET
STORE
DISPLAY
START
STOP
PSW RESTART
LOG OUT
H
POWER ON
POWER OFF
LOAD UNIT
INTERRUPT
SYSTEM
MANUAL
WAIT
TEST
LOAD

FIGURE 23

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

STORE DISPLAY

2 MAIN STORAGE / MPX STORAGE / MS SP DATA/MPX KEY — A / D / R — BYTE X, BYTE 0, BYTE 1 — 2

3 B REGISTER — 3

4 C REGISTER — 4

5 MAIN STORAGE DATA — 5

6 STORE ROAR — STORE ADDRESS FROM DATA KEYS — 6

7 MS DISPLAY — SET ADDRESS IN ADDRESS KEYS, DISPLAY DATA IN DATA REGISTER — MS STORE — SET ADDRESS IN ADDRESS KEYS, STORE DATA FROM DATA KEYS — 7

8

DISPLAY

2 P | IF PCI | IF WAIT | I-O PROG OUT | MODE | CHAN DATA | CHAN CTRL | IF CTRL | WAIT | P | MPX INTERFACE: RE-ENT CHANGE, LATE, LATE, ITO, TI, WO, WI, BUS IN, CCW IN, IF FLAGS, TAG — 2

3 INTERFACE CONTROLS: SEL OUT, SEL IN, ADR OUT, ADR IN, CMD OUT, STAT IN, SVC OUT, SVC IN, OP OUT, OP IN, SUP OUT, RED IN, SEL, INH SEL, UNIT UNBUS, HALT I-O — 3

4 CHANNEL CONTROLS: MASK CCW, MIS RUNPX CCW, CU; CCW FLAGS: CMA, CC, SILI, SKIP, 3, I; WAIT BACK; RD: 0; BUFFER FLAGS: 1, 2, 3, 4; COUNT: 0, 1, = — 4

5 TO TI — SELECTOR CHANNEL REGISTERS — 5

5 WO WI — SELECTOR CHANNEL REGISTERS — 5

5 W2 — SELECTOR CHANNEL REGISTERS — 5

5 W3 W4 — SELECTOR CHANNEL REGISTERS — 5

6 SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — EXTERNAL INTERRUPTS: 0 1 2 3 4 5 6 7 — 6

7 SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — STORAGE PROTECTION DATA: P 0 1 2 3; CPU/CHAN KEY: 0 1 2 3 — 7

8 SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — DIRECT CONTROL: 0 1 2 3 4 5 6 7 — 8

BYTE X, BYTE 0, BYTE 1

A

CHECKS

THERM O/L | ROS ADR | ROS DATA | D/Y8 | CTRL | LS READ | MS ADR | MS DATA DO | MS DATA DI | R REG RX | R REG RO | R REG RI | MS PROT KEY | MS PROT DATA

STATS | EX | ALU P | ALU Q | EARLY | LSAR | SKEW | ALU FUNC | ZW | ROAR | CHANNELS MPX | CHANNELS SCI | CHANNELS SC2 | LATE | UP

CONDITIONS

H/STOP | LOG | DSAB | DPI | DP2 | EX ROS | S TO SAB SCI | S TO SAB SC2

B

EMERGENCY PULL

C

REQ IN | SEL IN | OP IN | ADR IN | STAT IN | SVC IN

DSAB IRPT | DSAB INTVL TIMER | REV DATA | MPX STOR PTY | LAMP TEST

DIAGNOSTIC CONTROL

MS: ADDRESS, PATTERN — LS: ADDRESS, PATTERN — OFF — MS VALIDATE — CPU — DUMP

LSA BUS DISPLAY & STORE

LSAR — H — J

CHANNEL TEST

OFF — 170 KC — MAX — MANUAL

CHANNEL SELECT

MPX — SCI — SC2 — SCI & SC2

D

CONDITIONS

PMA | MA | I/O | YCI | YCD | ASCH | P | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | ID | MI | MAIN | ERR | IZT/IDQ | LOAD

YA STATS | YB STATS | YD STATS | YE STATS

ALU CONTROL: P 0 1 2 3 SKEW

SKEW SELECT REGISTER: P 0 1 2 3 4 5 6 7

ALU BINARY OUTPUT: 0 1 2 3 4 5 6 7

LSAR: P 0 1 2 3 4 5 6 7

-ROBAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-H-: P 0 1 2 3 4 5 6 7

-ROSAB-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-J-: P 0 1 2 3 4 5 6 7

-ROSCAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

STORE: STATS / LSA

ROLLER: STORE / DISPLAY

CHANNEL DISPLAY: TO TI — WO WI — W2 — W3 W4

1 LOCAL STORAGE OR R REGISTER: I 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 I

BYTE X, BYTE 0, BYTE 1

1 ALU EX | P REGISTER | Q REGISTER 1: P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

BYTE X, BYTE 0, BYTE 1

DISPLAY: ROSAB / ROBAR / ROAR / ROSCAR

STORE DISPLAY
1 LS R REGISTER
2 A REGISTER
3 B REGISTER
4 C REGISTER
5 D REGISTER
6 STORE ROAR
7 MAIN STORE
8

DISPLAY
1 ALU EX P Q
2 CHECKS & IF
3 IF CONTROLS
4 CHANNEL CONTROLS
5 CHANNEL REGISTERS
6 EXT INTERRUPTS
7 SP DATA & KEY
8 DIRECT CONTROL

E

SELECT VOLTAGE

OFF — MS: VXY, VZ — SP: VXY, VM — LS: VXY, VM — ROS — +3 — +6 — +18 — +24 — +48 — +6M

CONTROL WORD

A0 A1 A2 A3 | B0 B1 B2 B3 | C0 C1 C2 C3 | D0 D1 E0 E1 | E2 E3 F0 G0 | G1 H0 H1 H2 | H3 H4 J0 J1 | K2 K0 L0 L1 | L2 M0 M1 M2 | M3 N0 N1 N2 | N3 P0 P1 P2 | Q0 Q1 Q2 Q3 | R0 R1 R2 S0 | T0 T1 JX PX

6M MARGIN — THERMAL RESET

BIAS CONTROLS

MS: VXY — VZ

LS: VXY — VM

SP: VXY — ROS: DRIVE

THERMALS

PWR | MS ROS | GA | GB

CTRL CHECK

CB | CC | CD | CH0 | CH1 | CH2 | CJ | CN | CP | CQ | CR

ALU CHECKS

I/C | A7 | A6 | A5 | A4 | A3 | A2 | AI | A0 | O/C | EX

F

STORAGE DATA — SP DATA — SP KEY

BYTE X, BYTE 0, BYTE 1

0	0000
1	0001
2	0011
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

INSTRUCTION COUNTER OR STORAGE ADDRESS

BYTE X, BYTE 0, BYTE 1

REGISTER SELECT — HALF WORD SELECT

GP: 00 | 01 | 10 | 11

PSW & FP

G

ADDRESS COMPARE PROCESS

STOP ON MS LOOP ON MS — STOP ON LOOP ON ROS REPEAT ON — MS ROS LOOP — STOP MS ROS

STORAGE SELECT

MS — IC — PSW — GP — FP — SP

CHECK CONTROL PROCESS

STOP — DISABLE CHECK RESTART

RATE PROCESS

INSN STEP — SINGLE CYCLE

SYSTEM RESET | CHECK RESET | STORE | DISPLAY | START | STOP | PSW RESTART | LOG OUT

H

POWER ON — POWER OFF

LOAD UNIT

INTERRUPT — SYSTEM/MANUAL/WAIT TEST LOAD — LOAD

FIGURE 24

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

STORE DISPLAY

2 — MAIN STORAGE / MPX STORAGE / MS SP DATA/MPX KEY — A / D / R — BYTE X, BYTE 0, BYTE 1 — 2

3 — B REGISTER — BYTE X, BYTE 0, BYTE 1 — 3

4 — C REGISTER — BYTE X, BYTE 0, BYTE 1 — 4

5 — MAIN STORAGE DATA — BYTE X, BYTE 0, BYTE 1 — 5

6 — STORE ROAR — STORE ADDRESS FROM DATA KEYS — BYTE X, BYTE 0, BYTE 1 — 6

7 — MS DISPLAY- SET ADDRESS IN ADDRESS KEYS, DISPLAY DATA IN DATA REGISTER — MS STORE- SET ADDRESS IN ADDRESS KEYS, STORE DATA FROM DATA KEYS — BYTE X, BYTE 0, BYTE 1 — 7

8 — BYTE X, BYTE 0, BYTE 1 — 8

DISPLAY

2 — P — IF PTY PCI — IF TAG WLR — I-O MODE PROCEDURE — CHAN DATA — CHAN CTRL — IF CTRL — WLR SVR CHAIN — P — MPX INTERFACE: RE-ENT LATE — CHNEL LATE — TO — TI — WO — IN — BMR FLAGS — OCW — IF TAG — BYTE X, BYTE 0, BYTE 1 — 2

3 — INTERFACE CONTROLS: SEL OUT — SEL IN — ADR OUT — ADR IN — CMD OUT — STAT IN — SVC OUT — SVC IN — OP OUT — OP IN — SUP OUT — SUP IN — REQ IN — SEL — IMM UNIT — HALT I-O — BYTE X, BYTE 0, BYTE 1 — 3

4 — CHANNEL CONTROLS: HIGH CCW — HIGH CCW — MPX CCW — CCW FLAGS: CMD — CC — SILI — SKIP — 3 — 1 — WITH BACK — NO BUFFER FLAGS: 0 — 1 — 2 — 3 — 4 — COUNT: 0 — 1 — = — BYTE X, BYTE 0, BYTE 1 — 4

5 — TO TI — SELECTOR CHANNEL REGISTERS — BYTE X, BYTE 0, BYTE 1 — 5

5 — WO WI — SELECTOR CHANNEL REGISTERS — BYTE X, BYTE 0, BYTE 1 — 5

5 — W2 — SELECTOR CHANNEL REGISTERS — BYTE X, BYTE 0, BYTE 1 — 5

5 — W3 W4 — SELECTOR CHANNEL REGISTERS — BYTE X, BYTE 0, BYTE 1 — 5

6 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — EXTERNAL INTERRUPTS — BYTE X, BYTE 0, BYTE 1 — 6

7 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — STORAGE PROTECTION: DATA — CPU/CHAN KEY — BYTE X, BYTE 0, BYTE 1 — 7

8 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — DIRECT CONTROL — BYTE X, BYTE 0, BYTE 1 — 8

A

CHECKS: THERM O/L — ROS ADR — ROS DATA — D/Y8 CTRL — LS READ — MS ADR — MS DATA DO — MS DATA DI — R REG RX — R REG RO — R REG RI — MS PROT INT — MS PROT DATA

CHECKS: STATS — ALU EX — ALU P — ALU Q — ALU EARLY — ALU LSAR — ALU SKEW — ALU FUNC — ALU 2W — CHANNELS ROAR — CHANNELS MPX — CHANNELS SCI — CHANNELS SC2 — LATCHES

CONDITIONS: H/STOP — LOG — DSAB — DPI — DP2 — EX ROS — S TO SAB SCI — SC2

B

EMERGENCY PULL

C

REQ IN — SEL IN — OP IN — ADR IN — STAT IN — SVC IN

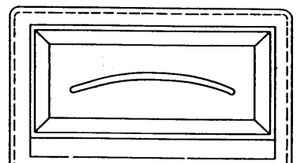
DSAB IRPT — DSAB INTVL TIMER — REV DATA — MPX STOR PTY — LAMP TEST

DIAGNOSTIC CONTROL: OFF — MS: ADDRESS PATTERN — LS: ADDRESS PATTERN — MS VALIDATE — CPU — DUMP

LSA BUS DISPLAY & STORE: LSAR — H — J

CHANNEL TEST: OFF — 170 KC — MAX — MANUAL

CHANNEL SELECT: MPX — SCI — SC2 — SCI & SC2



SELECT VOLTAGE: OFF — MS VXY VZ — SP VXY — LS VXY VM — ROS — −3 — +3 — +6 — +18 — +24 — +48 — +6M

6M MARGIN — THERMAL RESET

BIAS CONTROLS: MS VXY VZ — LS VXY VM — SP VXY — ROS DRIVE

CONTROL WORD: A0 AI A2 A3 — B0 BI B2 B3 — C0 CI C2 C3 — D0 DI E0 EI — E2 E3 F0 G0 — GI HO HI H2 — H3 H4 JO JI — J2 KO LO LI — LC MO MI M2 — M3 NO NI N2 — N3 PO P1 P2 — Q0 QI Q2 Q3 — R0 RI R2 S0 — T0 TI JX PX

THERMALS: PWR — MS — ROS — GA — GB

CTRL CHECK: CB CC CD CHO CHI — CH2 CJ CN GP CQ — CR

ALU CHECKS: I/C A7 A6 A5 A4 — A3 A2 AI A0 O/C — EX

D

CONDITIONS: PMA — MA — I/O — YCI — YCD — ASCH — P — YO — Y1 — Y2 — Y3 — YA STATS — Y4 — Y5 — Y6 — Y7 — YB STATS — ID — MI — MAN — YD STATS — ERR — IZT/IDO — LOAD — YE STATS

STORE: STATS — LSA

ROLLER: STORE — DISPLAY

CHANNEL DISPLAY: TO TI — WO WI — W2 — W3 W4

ALU CONTROL — SKEW SELECT REGISTER — ALU BINARY OUTPUT

LSAR — -H- — -J- — -ROBAR- — -ROSAB- — -ROSCAR- — -ROAR-

LOCAL STORAGE OR R REGISTER — BYTE X, BYTE 0, BYTE 1

ALU EX — P REGISTER — Q REGISTER — BYTE X, BYTE 0, BYTE 1

DISPLAY: ROSAB — ROBAR — ROAR — ROSCAR

STORE DISPLAY
1 LS R REGISTER
2 A REGISTER
3 B REGISTER
4 C REGISTER
5 D REGISTER
6 STORE ROAR
7 MAIN STORE
8

DISPLAY
1 ALU EX P Q
2 CHECKS & IF
3 IF CONTROLS
4 CHANNEL CONTROLS
5 CHANNEL REGISTERS
6 EXT INTERRUPTS
7 SP DATA & KEY
8 DIRECT CONTROL

F

0	0000
1	0001
2	0011
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

STORAGE DATA — SP DATA — SP KEY — BYTE 0 — BYTE 1

INSTRUCTION COUNTER OR STORAGE ADDRESS — BYTE X, BYTE 0, BYTE 1

REGISTER SELECT — HALF WORD SELECT

GP			
00	01	10	11
PSW & FP			

G

ADDRESS COMPARE PROCESS: STOP ON MS LOOP ON MS — STOP ON LOOP ON ROS REPEAT ON — MS ROS LOOP — STOP MS ROS

STORAGE SELECT: MS — IC — SP — PSW — GP — FP

CHECK CONTROL PROCESS: STOP DISABLE CHECK RESTART

RATE PROCESS: INSN STEP — SINGLE CYCLE

SYSTEM RESET — CHECK RESET — STORE — DISPLAY — START — STOP — PSW RESTART — LOG OUT

H

POWER ON — POWER OFF

LOAD UNIT

INTERRUPT — SYSTEM/MANUAL/WAIT/TEST/LOAD — LOAD

FIGURE 25

STORE DISPLAY

2 — MAIN STORAGE / MPX STORAGE / MS SP DATA/MPX KEY — ADR 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — DATA 15 14 13 6 5 4 3 2 1 0 — PARITY 6 5 4 3 2 1 0 — 2

BYTE X / BYTE O / BYTE I — P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7 — A S

3 — B REGISTER — BYTE O: P Ø 1 2 3 4 5 6 7 — BYTE I: P Ø 1 2 3 4 5 6 7 — 3

4 — C REGISTER — BYTE X: P 5 6 7 — BYTE O: P Ø 1 2 3 4 5 6 7 — BYTE I: P Ø 1 2 3 4 5 6 7 — 4

5 — MAIN STORAGE DATA — 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 Ø — 5

6 — STORE ROAR: DAT EX ROS, DAT EX ROS, P 0-2 PMA MA CPU, 11 10 9 8 — DISPLAY ROSAB: P 7 6 5 4 3 2 1 Ø — 6

7 — MS DISPLAY— SET ADDRESS IN ADDRESS KEYS / DISPLAY DATA IN DATA REGISTER — MS STORE— SET ADDRESS IN ADDRESS KEYS / STORE DATA FROM DATA KEYS — 7

8 — 8

DISPLAY

2 — P — IF PTY TAG PCI, IF WLR, I-O MODE PROG PROT, CHAN DATA, CHAN IF CTRL, CTRL, P, MPX INTERFACE: RE-INT CHSEL LATE, LATE IT0, TI, WB0, BUS CCW IF IN, FLAGS TAG — 2

3 — INTERFACE CONTROLS: SEL OUT, SEL IN, ADR OUT, ADR IN, CMD OUT, STAT IN, SVC OUT, SVC IN, OP OUT, OP IN, SUP OUT, REQ IN, SEL, INH SEL, UNIT UNOB, HALT I-O — 3

4 — CHANNEL CONTROLS: 1401, 1440 CCW, 1460 CCW, MPX CU, CCW FLAGS: CDA, CC, SILI, SKIP, MCH STATS: 1, 3, RD WR, BACK, BUFFER FLAGS: Ø 1 2 3 4, COUNT: Ø 1 — 4

5 — TO TI — SELECTOR CHANNEL REGISTERS: P Ø 1 2 3 4 5 6 7 P Ø 1 2 3 4 5 6 7 — 5

5 — WO WI — SELECTOR CHANNEL REGISTERS — 5

5 — W2 — SELECTOR CHANNEL REGISTERS — 5

5 — W3 W4 — SELECTOR CHANNEL REGISTERS — 5

6 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — EXTERNAL INTERRUPTS: Ø 1 2 3 4 5 6 7 — 6

7 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — STORAGE PROTECTION: DATA P Ø 1 2 3, GPU/CHAN KEY Ø 1 2 3 — 7

8 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — DIRECT CONTROL: Ø 1 2 3 4 5 6 7 — 8

BYTE X / BYTE O / BYTE I — P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

(A)

CHECKS: THERM, O/L, ROS ADR, ROS DATA, D/Y8, CTRL, LS READ, MS ADR, MS DATA DO, DI, R REG RX, RO, RI, MS PROT KEY, DATA

ALU: STATS, EX, P, Q, SKEW, FUNC, CH, ROAR, MPX, SCI, SC2, LATE, IMP

CONDITIONS: H/ STOP, LOG, DSAB, DPI

S TO SAB: SCI, SC2

EMERGENCY PULL

(C)

REQ IN, SEL IN, OP IN, ADR IN, STAT IN, SVC IN

DSAB IRPT, DSAB INTVL TIMER, REV DATA, MPX STOR PTY, LAMP TEST

DIAGNOSTIC CONTROL: OFF; MS: ADDRESS, PATTERN; LS: ADDRESS, PATTERN; MS VALIDATE, CPU, DUMP

LSA BUS DISPLAY & STORE: LSAR; H, J

CHANNEL TEST: OFF, MANUAL

CHANNEL SELECT: MPX, SCI, SC2

C.P.U. POWER OFF

SELECT VOLTAGE: OFF, MS VXY, VZ, SP VXY, LS VXY, VM, ROS +6M, +3, +6, +18, +24, +48

CONTROL WORD: A0 A1 A2 A3 … N3 P0 P1 P2 … EX

6M MARGIN

THERMAL RESET

BIAS CONTROLS: MS VXY VZ; LS VXY VM; SP VXY; ROS DRIVE

THERMALS: PWR, MS, ROS, GA, GB

CTRL CHECK: CB, CC, CD, CHO, CHI, CH2, CJ, CN, CP, CQ, CR

ALU CHECKS: I/C, A7, A6, A5, A4, A3, A2, A1, A0, O/C

(D)

CONDITIONS: PMA, MA, I/O, YCI, YCD, ASCII, P, YA STATS Y0 Y1 Y2 Y3, YB STATS Y4 Y5 Y6 Y7, YD STATS ID, MI, MAIN, YE STATS ERR, IZT/IDO, LOAD

STORE: STATS, LSA

ROLLER: STORE, DISPLAY

CHANNEL DISPLAY: TO TI, WO WI, W2, W3 W4

ALU CONTROL: P 0 1 2 3 SKEW

SKEW SELECT REGISTER: P 0 1 2 3 4 5 6 7

ALU BINARY OUTPUT: 0 1 2 3 4 5 6 7

LSAR: P 0 1 2 3 4 5 6 7 | P 12 11 10 9 8 7 6 5 4 3 2 1 0

-H-: P 0 1 2 3 4 5 6 7 | P 12 11 10 9 8 7 6 5 4 3 2 1 0

-J-: P 0 1 2 3 4 5 6 7 | P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROBAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROSAB-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROSCAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

1 — LOCAL STORAGE OR R REGISTER: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 — 1

BYTE X / BYTE O / BYTE I — P 5 6 7 | P 0 1 2 3 4 5 6 7 | P 0 1 2 3 4 5 6 7

1 — ALU EX: P 5 6 7 — P REGISTER: P Ø 1 2 3 4 5 6 7 — Q REGISTER: P Ø 1 2 3 4 5 6 7 — 1

DISPLAY: ROSAB, ROBAR, ROAR, ROSCAR

STORE DISPLAY

	MPX	SC
1	LS/R	LS/R
2	A	S
3	B	B
4	C	C
5	D	D
6	ROAR	ROAR
7	MS	MS
8		

DISPLAY

	MPX	SC
1	EX PQ	EX PQ
2	CHKS & IF	STAT & CHKS
3	IF CTRLS	IF CTRLS
4	CHAN CTRLS	CHAN CTRLS
5		CHAN DISP
6	IRPTS	IRPTS
7	SPD & KEY	SPD & KEY
8	DIR CTRL	DIR CTRL

(F)

STORAGE DATA: SP DATA, SP KEY

BYTE O: P 0 1 2 3 4 5 6 7 — BYTE I: P 0 1 2 3 4 5 6 7

INSTRUCTION COUNTER OR STORAGE ADDRESS

SAB/P

BYTE X: 5 6 7 — BYTE O: P 0 1 2 3 4 5 6 7 — BYTE I: P 0 1 2 3 4 5 6 7

REGISTER SELECT

HALF WORD SELECT

GP: 00, 01, 10, 11

PSW & FP

0	0	0	0	0				
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
A	1	0	1	0				
B	1	0	1	1				
C	1	1	0	0				
D	1	1	0	1				
E	1	1	1	0				
F	1	1	1	1				

(G)

ADDRESS COMPARE PROCESS: STOP ON MS LOOP ON MS, STOP ON LOOP ON ROS, REPEAT ON, STOP MS ROS, MS ROS LOOP

STORAGE SELECT: MS, IC, PSW, GP, FP, SP

CHECK CONTROL PROCESS: STOP, DISABLE, CHECK RESTART

RATE PROCESS: INSN STEP, SINGLE CYCLE

SYSTEM RESET

PSW RESTART

CHECK RESET

STORE

DISPLAY

START

STOP

LOG OUT

(H)

POWER ON

POWER OFF

LOAD UNIT: 7 6 5 4 3 2 1 0 — F E D C B A 9 8 — 7 6 5 4 3 2 1 0

INTERRUPT

SYSTEM MANUAL WAIT TEST LOAD

LOAD

FIGURE 26

-360 MOD 40 FAILURE SYMPTOMS DISPLAY-

STORE DISPLAY

2 — MS STORAGE / MPX STORAGE / MS SP DISPLAY/MPX KEY — A D R — BYTE X / BYTE 0 / BYTE 1 — A S

3 — B REGISTER

4 — C REGISTER

5 — MAIN STORAGE DATA

6 — STORE ROAR — DISPLAY ROSAB

7 — MS DISPLAY- SET ADDRESS IN ADDRESS KEYS, DISPLAY DATA IN DATA REGISTER — MS STORE- SET ADDRESS IN ADDRESS KEYS, STORE DATA FROM DATA KEYS

8

DISPLAY

2 — IF PTY TAG PCI WLR — IF PROG PROT — I-O MODE PROT — CHAN DATA — CHAN IF CTRL CTRL — CHAR — MPX INTERFACE: RE-INT CHSEL LATE LATE — BUS OUT TO TI WO — CCW IF IN FLAGS — IF TAG

3 — INTERFACE CONTROLS: SEL OUT, SEL IN, ADR OUT, ADR IN, CMD OUT, STAT IN, SVC OUT, SVC IN, OP OUT, OP IN, SUP OUT, REQ IN, SEL, INH SEL, UNIT UNOB, HALT I-O

4 — CHANNEL CONTROLS — CCW FLAGS: 1401 CCW, 1440 CCW, HSMPX CU, CDA, CC, SILI SKIP, TCH CHNS 1, STATUS 3, RD WR, BACK — BUFFER FLAGS: Ø 1 2 3 4 — COUNT: Ø 1 =

5 — TO TI — SELECTOR CHANNEL REGISTERS

5 — WO W1 — SELECTOR CHANNEL REGISTERS

5 — W2 — SELECTOR CHANNEL REGISTERS

5 — W3 W4 — SELECTOR CHANNEL REGISTERS

6 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — EXTERNAL INTERRUPTS Ø 1 2 3 4 5 6 7

7 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — STORAGE PROTECTION: DATA P Ø 1 2 3 — CPU/CHAN KEY Ø 1 2 3

8 — SET ROLLER SWITCH TO DISPLAY ALU EX AND P REGISTER IS RESET — DIRECT CONTROL Ø 1 2 3 4 5 6 7

BYTE X / BYTE 0 / BYTE 1 throughout

CHECKS

THERM O/L | ROS ADR DATA | D/ Y8 | CTRL | LS READ | MS ADR | MS DATA DO DI | R REG RX RO RI | MS PROT KEY DATA

STATS | EX | ALU P Q | BARU | LSAR | SKEW | ALU FUNC | ZW | ROAR | CHANNELS MPX SCI SC2 | LATE | UP

CONDITIONS

H/STOP | LOG | DSAB | DPI | S TO SAB SCI SC2

EMERGENCY PULL

REQ IN | SEL IN | OP IN | ADR IN | STAT IN | SVC IN

DSAB IRPT | DSAB INTVL | REV DATA | MPX STOR | LAMP TEST

DIAGNOSTIC CONTROL: OFF; MS: ADDRESS PATTERN; LS: ADDRESS PATTERN; MS VALIDATE; CPU; DUMP

LSA BUS DISPLAY & STORE LSAR: H J

CHANNEL TEST: OFF; MANUAL

CHANNEL SELECT: MPX SCI SC2

C.P.U. POWER OFF

SELECT VOLTAGE: OFF +3 +3 +6 +18 +24 +48 +6M; MS VXY VZ; SP VXY VM; LS

CONTROL WORD A0 A1 A2 A3 / B0 B1 B2 B3 / C0 C1 C2 C3 / D0 D1 E0 E1 / E2 E3 F0 G0 / G1 H0 H1 H2 / H3 H4 J0 J1 / J2 K0 L0 L1 / L2 M0 M1 M2 / M3 N0 N1 N2 / N3 P0 P1 P2 / Q0 Q1 Q2 Q3 / R0 R1 R2 S0 / T0 T1 J2 P2

6M MARGIN | THERMAL RESET

BIAS CONTROLS: MS VXY VZ; LS VXY VM; SP VXY; ROS DRIVE

CTRL CHECK: CB CC CD CH0 CH1 / CH2 CJ CN CP CQ / CR

THERMALS: PWR MS ROS GA GB

ALU CHECKS: I/C A7 A6 A5 A4 / A3 A2 A1 A0 O/C / EX

STORE

STATS | LSA

ROLLER

STORE | DISPLAY

CHANNEL DISPLAY

TO TI, WO W1, W2, W3 W4

CONDITIONS: PMA MMA I/O YCI YCD ASCH

YA STATS: P Y0 Y1 Y2 Y3

YB STATS: P Y4 Y5 Y6 Y7

YD STATS: ID MI MAN

YE STATS: ERR | IZT/IDQ LOAD

ALU CONTROL: P 0 1 2 3 SKEW

SKEW SELECT REGISTER: P 0 1 2 3 4 5 6 7

ALU BINARY OUTPUT: 0 1 2 3 4 5 6 7

LSAR: P 0 1 2 3 4 5 6 7

-ROBAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-H-: P 0 1 2 3 4 5 6 7

-ROSAB-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-J-: P 0 1 2 3 4 5 6 7

-ROSCAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

-ROAR-: P 12 11 10 9 8 7 6 5 4 3 2 1 0

LOCAL STORAGE OR R REGISTER: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

ALU EX | P REGISTER | Q REGISTER

BYTE X / BYTE 0 / BYTE 1

DISPLAY

ROSAB | ROBAR | ROAR ROSCAR

STORE DISPLAY

	MPX	SC
1	LS/R	LS/R
2	A	S
3	B	B
4	C	C
5	D	D
6	ROAR	ROAR
7	MS	MS
8		

DISPLAY

	MPX	SC
1	EX PQ	EX PQ
2	CHKS & IF	STAT & CHKS
3	IF CTRLS	IF CTRLS
4	CHAN CTRLS	CHAN CTRLS
5		CHAN DISP
6	IRPTS	IRPTS
7	SPD & KEY	SPD & KEY
8	DIR CTRL	DIR CTRL

STORAGE DATA

SP DATA | SP KEY

BYTE 0 / BYTE 1

INSTRUCTION COUNTER OR STORAGE ADDRESS

SAB/P

REGISTER SELECT | HALF WORD SELECT

GP			
00	01	10	11
PSW & FP			

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

ADDRESS COMPARE PROCESS

STOP ON MS LOOP ON MS | STOP ON LOOP ON REPEAT ON ROS | MS ROS LOOP | STOP MS ROS

STORAGE SELECT

MS: IC SP | PSW GP FP

CHECK CONTROL PROCESS

STOP | DISABLE | CHECK RESTART

RATE PROCESS

INSN STEP | SINGLE CYCLE

SYSTEM RESET | PSW RESTART | CHECK RESET

STORE | DISPLAY

START | STOP | LOG OUT

POWER ON | POWER OFF

LOAD UNIT

INTERRUPT | SYSTEM MANUAL WAIT TEST LOAD | LOAD

FIGURE 27

HEX PHYSICAL ADDRESS	ABSOLUTE ADDRESS	SHEET NUMBER	CLD BOX	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	JX	PX	E.C. NUMBER	VERSION	TAPE POSITION NUMBER	WORD NUMBER	STAGGER CLASS	GATE NUMBER	DRIVER NUMBER
0200	0001000000000	QL041	AA –	1001	1000	0111	10	1010	0	11	01111	100	0	001	0111	1111	000	0001	000	0	00	0	0	254283		000	A	A	00	00
0201	0001000000001		–	0000	0010	0000	11	0000	1	01	00000	000	0	000	0000	0000	000	0000	000	0	00	0	0	254283		001	A	B	08	01
0202	0001000000010	QL011	CA –	1001	0111	0001	00	1101	1	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		002	A	C	08	02
0203	0001000000011	QL021	GE –	0100	0111	0001	00	1000	0	00	00111	100	0	001	1111	0101	000	0101	000	0	00	0	0	254283		003	A	A	08	03
0204	0001000000100	QL011	EA –	1001	0111	0001	00	1101	1	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		004	A	B	08	04
0205	0001000000101	QL021	LC –	1110	0000	0111	00	0000	0	00	01010	000	0	000	1111	0000	000	0101	000	1	00	0	0	254283		005	A	C	08	05
0206	0001000000110	QL011	GA –	1001	0111	0001	00	1001	0	11	00000	000	1	000	0111	1111	100	0000	110	1	10	0	0	254283		006	A	A	08	06
0207	0001000000111	QL031	CG –	1011	0001	0000	00	0001	1	00	11000	001	0	001	0011	0000	000	0110	000	1	00	0	0	254283		007	A	B	08	07
0208	0001000001000	QL011	JA –	1001	0111	0001	00	1001	1	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		008	A	C	08	08
0209	0001000001001	QL031	EB –	1111	0000	0000	00	0000	0	00	00000	000	0	000	0111	0000	000	0111	000	0	10	0	0	254283		009	A	A	08	09
020A	0001000001010	QL011	LA –	1001	0111	0001	00	1101	0	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		010	A	B	08	10
020B	0001000001011	QL031	CB –	1111	0000	0000	00	0000	1	00	00000	000	0	100	0010	0000	000	0111	000	0	10	0	0	254283		011	A	C	08	11
020C	0001000001100	QL011	NA –	1001	0111	0001	00	1101	0	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		012	A	A	08	12
020D	0001000001101	QL011	NG –	1001	0001	1000	00	0011	1	00	11000	110	0	111	0000	0000	000	0010	000	0	00	0	0	254283		013	A	B	08	13
020E	0001000001110	QL031	AA –	0010	0111	0001	00	1001	1	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		014	A	C	08	14
020F	0001000001111	QL011	LF –	1000	0000	0001	00	0000	0	11	11111	110	0	110	1110	0000	000	0100	000	0	00	0	0	254283		015	A	A	08	15
0210	0001000010000	QL031	CA –	0010	0111	0001	00	1001	1	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		016	A	B	08	16
0211	0001000010001	QL021	EC –	0000	0001	0001	00	1000	0	00	11000	110	0	110	1110	0110	000	0100	000	0	00	0	0	254283		017	A	C	08	17
0212	0001000010010	QL031	EA –	0010	0111	0001	00	1101	0	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		018	A	A	08	18
0213	0001000010011	QL021	CC –	1101	0001	0000	00	0000	1	00	00111	110	0	110	1110	0000	000	0100	000	1	00	0	0	254283		019	A	B	08	19
0214	0001000010100	QL031	GA –	0010	0111	0001	00	1101	0	11	00000	000	0	000	0111	1111	100	0000	000	0	10	0	0	254283		020	A	C	08	20
0215	0001000010101	QL031	AE –	1110	0001	0000	00	0000	1	00	00111	110	0	000	1011	0000	000	0100	000	1	00	0	0	254283		021	A	A	08	21
0216	0001000010110	QL031	JA –	0010	0111	0001	00	1001	1	11	00000	000	1	000	0111	1111	100	0000	110	1	10	0	0	254283		022	A	B	08	22
0217	0001000010111	QL031	CE –	1111	0000	0001	00	0010	0	00	11001	001	0	001	0011	0000	000	0100	000	1	00	0	0	254283		023	A	C	08	23
0218	0001000011000	QL031	LA –	0010	0111	0001	00	1001	0	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		024	A	A	08	24
0219	0001000011001	QL031	JE –	1001	0001	0101	10	0000	1	00	00000	001	0	111	1011	0000	000	0100	000	0	00	0	0	254283		025	A	B	08	25
021A	0001000011010	QL031	NA –	0010	0111	0001	00	1101	1	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		026	A	C	08	26
021B	0001000011011	QL031	GE –	1001	0000	0101	10	0001	0	00	00000	001	0	110	0111	0110	000	0100	000	0	00	0	0	254283		027	A	A	08	27
021C	0001000011100	QL031	QA –	0010	0111	0001	00	1101	1	11	00000	000	1	000	0111	1111	100	0000	110	0	10	0	0	254283		028	A	B	08	28
021D	0001000011101	QL041	CC –	1101	0000	0001	00	0001	0	01	11001	011	0	001	0000	0000	000	0000	000	1	00	0	0	254283		029	A	C	08	29
021E	0001000011110	QL041	EA –	1001	0111	0111	10	0001	0	01	00000	000	0	000	0000	0110	000	0000	000	0	00	0	0	254283		030	A	A	08	30
021F	0001000011111	QL041	CE –	1001	0001	0000	10	0000	1	01	11001	010	0	001	0000	0000	000	0000	000	0	00	0	0	254283		031	A	B	08	31

FIGURE 28

25 FEB 65 254283
15 MAY 65 254815

ADDRESS LIST UNIT. 0002
DATE 15 MAY 65 MACH. 2040
LOG 044 UNIT P.N. 5348480
FRAME FF PAGE P.N. 5408454
IBM CORP. WTC PAGE 01

QN0020260

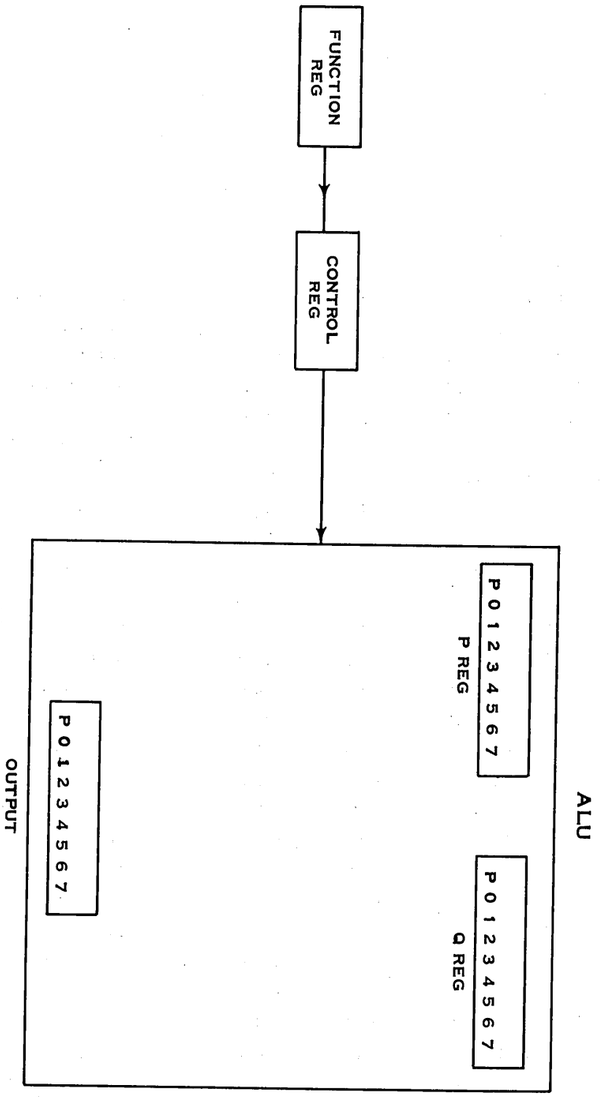


FIGURE 31

MODEL 40 SYSTEMS ENVIRONMENT RECORDING EDIT AND PRINT PROGRAM %SEREP¤

--- CPU ---

RDBAR	0 05FB	EARLY CK	0	CTRL CK	0	YA STATS	0000
A REG	0 00 08	LATE CK	1	ROS ADDR CK	0	YB STATS	1000
H REG	00 05	RX PTY CK	0	ROS DATA CK	0	FUNCT REG	0 01110
C REG	J 64 02	RO PTY CK	0	B DEC CK	0	INH DUMP YB	0
D REG	(00) 02	R1 PTY CK	0	C DEC CK	0	SKEW REG	0000
J REG	07	MSAD PTY CK	0	D DEC CK	0		
H REG	48	RDAR CK	0	H LOAD DEC CK	0		
P REG	00	LS RD PTY CK	0	H DES DEC CK	0		
Q REG	02	DO PTY CK	0	H INC DEC CK	0		
LS 43-INST BUF	9D	D1 PTY CK	0	J DEC CK	0	PMA	0
SPLS KEY	0000	SPLS KEY CK	0	N DEC CK	0	IMA	0
SPLS DATA	0000	SPLS DATA CK	0	P DEC CK	0	I/O	1
ALU EXT	000	STAT PTY CK	0	Q DEC CK	0	YCD	0
		P PTY CK	0	R DEC CK	0	YC1	0
MPX INTRPT	1	Q PTY CK	0	D/Y8 CK	0	DP1	0
SC1 INTRPT	0	2-WIRE I-P CAR	0				
SC2 INTRPT	0	2-WIRE O-P CAR	0				
EXT INTRPT	0	ALU 2-W CKS	00				
		EX PTY CK	0				
		SQ SEL CK	0				
		ALU FUN CK	0				
		LSAR PTY CK	0				

GP REGS 0-3	00 00 00 01	00 00 09 C1	00 00 08 E2	00 00 08 1F
GP REGS 4-7	00 00 00 00	00 00 09 EA	00 00 0F F0	00 07 00 00
GP REGS 8-B	00 00 08 24	A0 00 15 68	00 00 00 00	00 00 20 00
GP REGS C-F	00 00 00 0E	80 00 09 10	00 00 20 00	00 00 10 00
FP REGS 0-2	80 04 81 04	82 04 83 04	84 04 85 04	86 04 87 04
FP REGS 4-6	88 04 89 04	8A 04 8B 04	8C 04 8D 04	8E 04 8F 04

OLD MC PSW 00000000 40000E30

STORAGE KEYS - 32 STORAGE BLOCK KEYS PER LINE %64K¤

0 0 0 0 0 0 3 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

--- MULTIPLEXOR CHANNEL ---

CCW ADDR	00 00 00	CCK LOG INT	0	CDA	0	SEL OUT	0	I/F PTY	1
DATA ADDR	00 00 00	UE INT	0	CCW	0	SEL IN	0	I/F TAG	0
UNIT NO	*00	END INT	0	SILI	0	ADDR OUT	0	I/O MODE	0
COUNT	00 00	PCI INT	0	SKIP	0	ADDR IN	1	CHAN DATA	0
		WLR	0	PCI	0	COM OUT	0	CHAN CTRL	0
MPX-ROAR	*0*0*00	PGM CK	0	OP CODE	000	STAT IN	0	I/F CTRL	1
		PROT CK	0	CT ZERO	0	SER OUT	0	WLR WR	0
YMA	*0	CDK	0	END	0	SER IN	0	I/F REG	*05*
IMA	*0	CCK	0			OP OUT	1		
CPU STATE	*0	IFCC	0			OP IN	1		
DAT	*0					SUP OUT	0		
						REQ IN	0		
						SELECT	0		
						INH SEL	1		
						UNIT UNOB	0		
						HLT I/O	0		

--- HIGH SPEED B SELECTOR CHANNEL 1 ---

S REG	0 00 00	CDA	0	PCI	0	SEL OUT	0	REIN LATE	0
T REG	00 00	CC	0	WLR	0	SEL IN	0	CH SEL LATE	0
REF CCW AD	0 00 00	SILI	0	PGM CK	0	ADDR OUT	0	TO PTY CK	0
REF ADR WR	0 00 00	SKIP	0	PROT CK	0	ADDR IN	0	T1 PTY CK	0
LS 25 WORK	*0*00*00	CH Y3	0	CDK	0	COM OUT	0	WO PTY CK	0
LS 21 DREG	*0*00*00	CH Y1	0	CCK	0	STAT IN	0	BUS IN CK	0
LS 20 AREG	*0*00*00	RD/WR	0	ICC	0	SER OUT	0	CCW FLGS CK	0
UNIT NO	00	RD BACK	0	CHAIN	0	SER IN	0	I/F TAG CK	0
		LS 24 CH FLGS	00			OP OUT	1		
WO	*00	CHAIN FLAGS	00000			OP IN	0		
W1	*00	BUF CT 0	1			SUP OUT	1		
W2	*00	BUF CT 1	0			REQ IN	0		
W3	*00	BUF CT EQ	1			SELECT	0		
W4	*00	CHAN SP KEY	0000			INH SEL	0		
						UNIT UNOB	0		
						HLT I/O	0		

--- HIGH SPEED B SELECTOR CHANNEL 2 ---

S REG	*0*00*00	CDA	0	PCI	0	SEL OUT	0	REIN LATE	0
T REG	*00*00	CC	0	WLR	0	SEL IN	0	CH SEL LATE	0
REF CCW AD	0 00 00	SILI	0	PGM CK	0	ADDR OUT	0	TO PTY CK	0
REF ADR WR	0 00 00	SKIP	0	PROT CK	0	ADDR IN	0	T1 PTY CK	0
LS 35 WORK	*0*00*00	CH Y3	0	CDK	0	COM OUT	0	WO PTY CK	0
LS 31 DREG	*0*00*00	CH Y1	0	CCK	0	STAT IN	0	BUS IN CK	0
LS 30 AREG	*0*00*00	RD/WR	0	ICC	0	SER OUT	0	CCW FLGS CK	0
UNIT NO	00	RD BACK	0	CHAIN	0	SER IN	0	I/F TAG CK	0
		LS 34 CH FLGS	00			OP OUT	0		
WO	*00	CHAIN FLAGS	00000			OP IN	0		
W1	*00	BUF CT 0	0			SUP OUT	0		
W2	*00	BUF CT 1	0			REQ IN	0		
W3	*00	BUF CT EQ	0			SELECT	0		
W4	*00	CHAN SP KEY	*0000			INH SEL	0		
						UNIT UNOB	0		
						HLT I/O	0		

*** THE MACHINE LOG EDIT IS COMPLETE - PROGRAM FINISHED

FIGURE 29

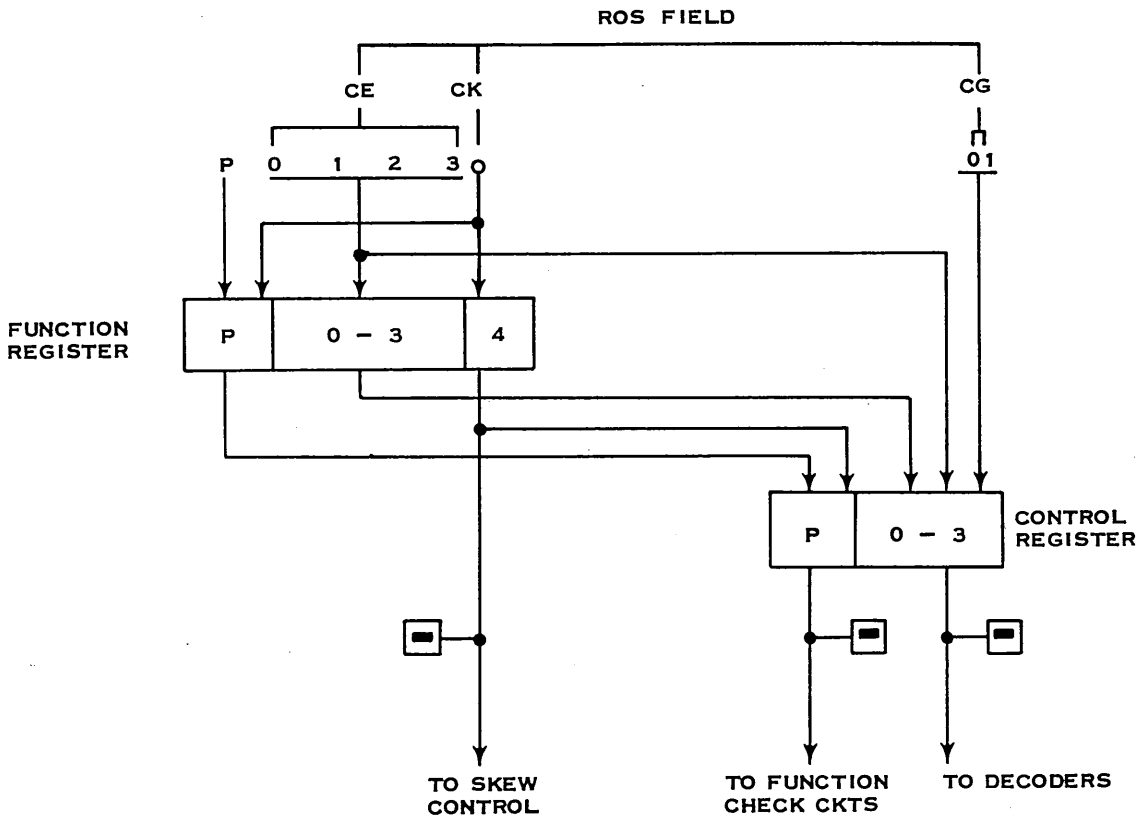


FIGURE 32

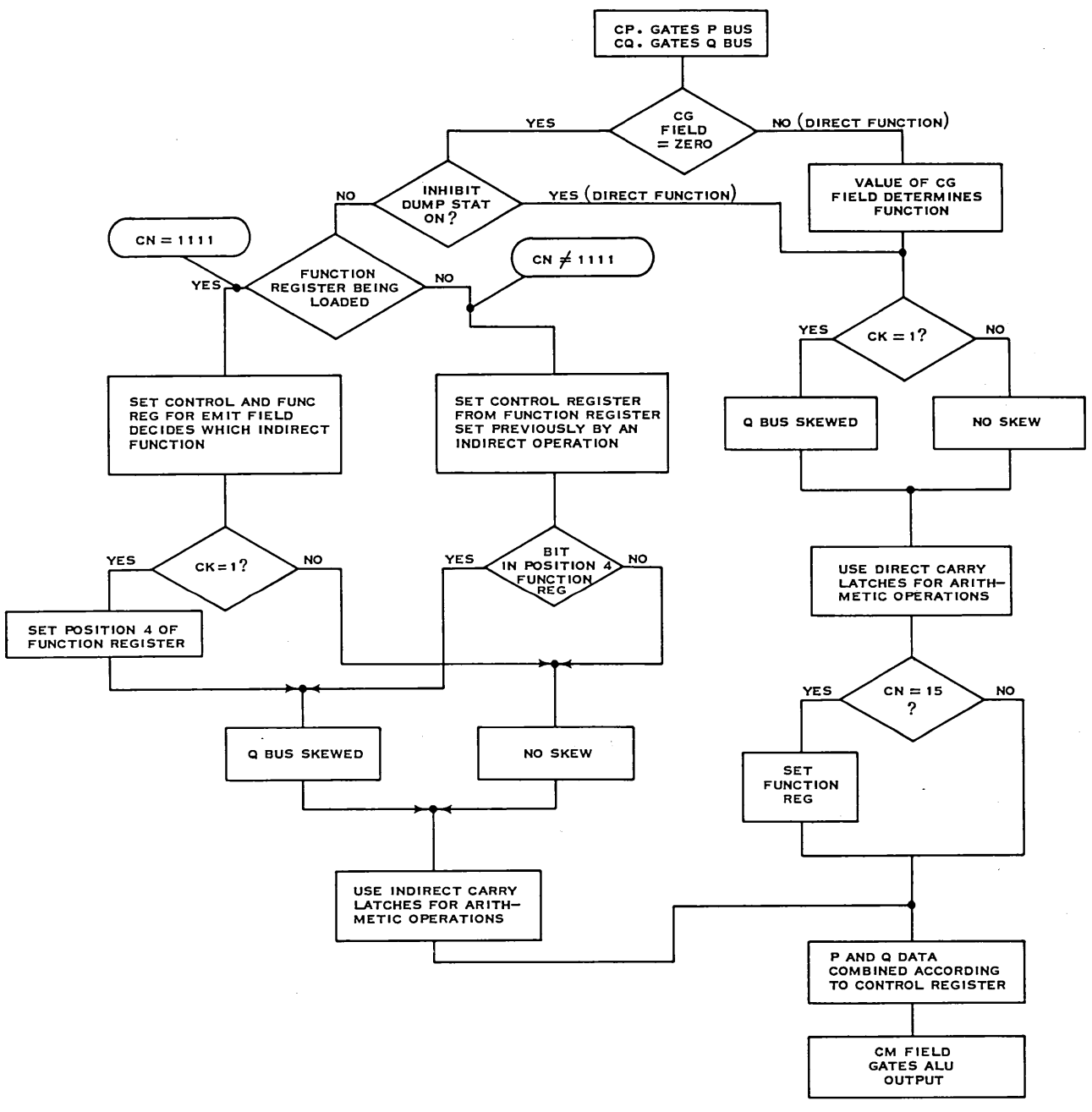


FIGURE 33

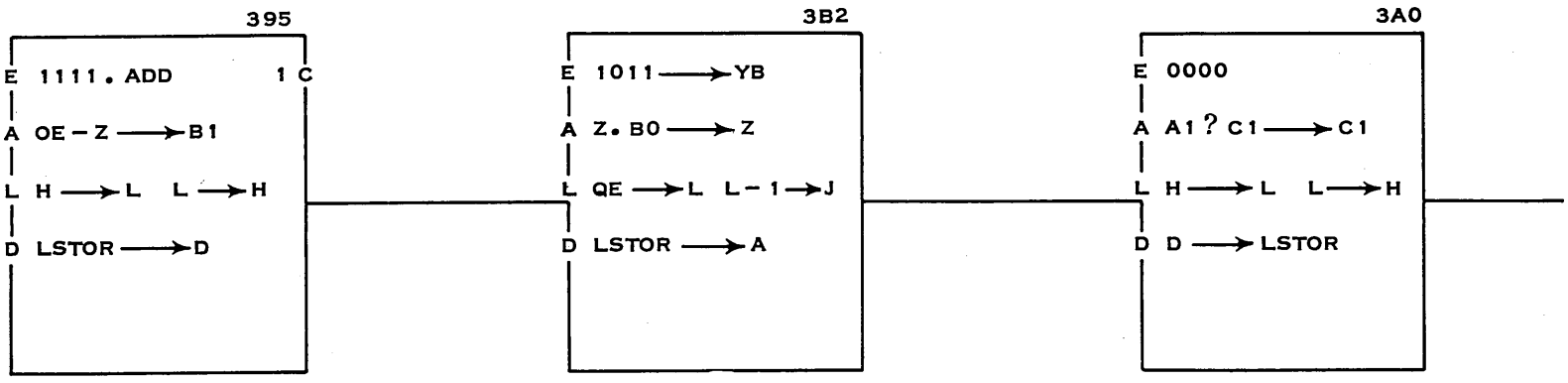


FIGURE 34

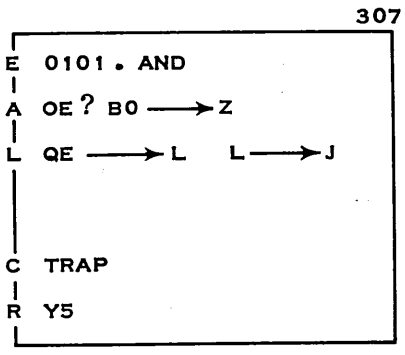


FIGURE 35

	ALU Control Bits	Logical Operation		Active Control Signals												Connect Box Function (F)	Right Shift Function (G)	YC Stat Conditions	YCI or YCD Stat Conditions
		Abb	Meaning	K	L	M	N	H	J	S	W	X	Y	V	U				
*P	0 0000	OR	P + Q	K	L	M									U	P or Q	Zero Output	No Effect on Bit 7	Not Affected
/	1 0001	AND	P . Q	K											U	P and Q	Zero Output	No Effect on Bit 7	Not Affected
	2 0010	DSQ	P - Q (Decimal)	K			N	H		S			Y	V	U	Equivalent P Q	Inverse of Q	YC Off Gives Carry to Bit 7	Set if No Carry Bit 0
*P	3 0011	SUQ	P - Q (Binary)	K			N			S			Y	V	U	Equivalent P Q	Inverse of Q	YC Off Gives Carry to Bit 7	Set if No Carry Bit 0
	4 0100	P	Pass P	K	L										U	Pass P	Zero Output	No Effect on Bit 7	Not Affected
*P	5 0101	AND	P . Q	K											U	P and Q	Zero Output	No Effect on Bit 7	Not Affected
P	6 0110	DSP	Q - P (Decimal)	K			N	H		S		X		V		Equivalent P Q	Q	YC Off Gives Carry to Bit 7	Set if No Carry Bit 0
	7 0111	SUP	Q - P (Binary)	K			N			S		X		V		Equivalent P Q	Q	YC Off Gives Carry to Bit 7	Set if No Carry Bit 0
	8 1000	PNQ	P . $\bar{Q}$		L											P . $\bar{Q}$	Zero Output	No Effect on Bit 7	Not Affected
P	9 1001	Q	Pass P	K		M										Pass Q	Zero Output	No Effect on Bit 7	Not Affected
P	10 1010	XOR	Exclusive OR (P Q)		L	M										P Q Exclusive OR	Zero Output	No Effect on Bit 7	Not Affected
	11 1011	QNP	$\bar{P}$. Q			M										$\bar{P}$. Q	Zero Output	No Effect on Bit 7	Not Affected
P	12 1100	RSH*	1 Bit Rt Shift of Q								W	X		V	U	Zero Output	Q Shifted Two Positions Rt	YC On Gives Rt Shift Output Bit 1	Set if There is Carry Bit 0
	13 1101	LSH	1 Bit Left Shift of Q									X		V	U	Zero Output	Q	YC On Gives Carry to Bit 7	Set if There is Carry Bit 0
	14 1110	DAD	P + Q (Decimal)		L	M		H	J			X		V	U	P Q Exclusive OR	Q	YC On Gives Carry to Bit 7	Set if There is Carry Bit 0
*P	15 1111	ADD	P + Q (Binary)		L	M						X		V		P Q Exclusive OR	Q	YC On Gives Carry to Bit 7	Set if There is Carry Bit 0

* Direct Function
/ Gives Function Check

FIGURE 36

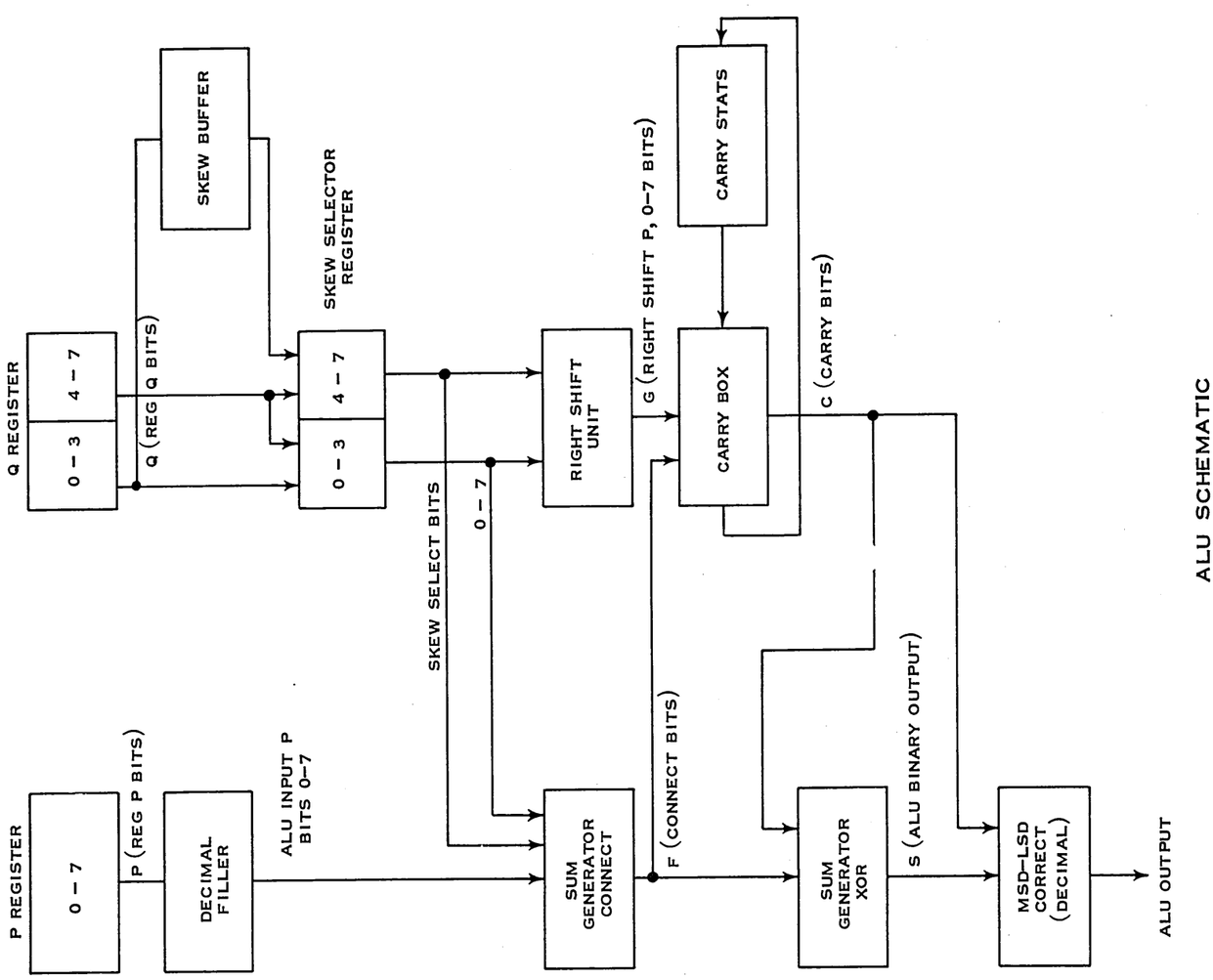


FIGURE 37

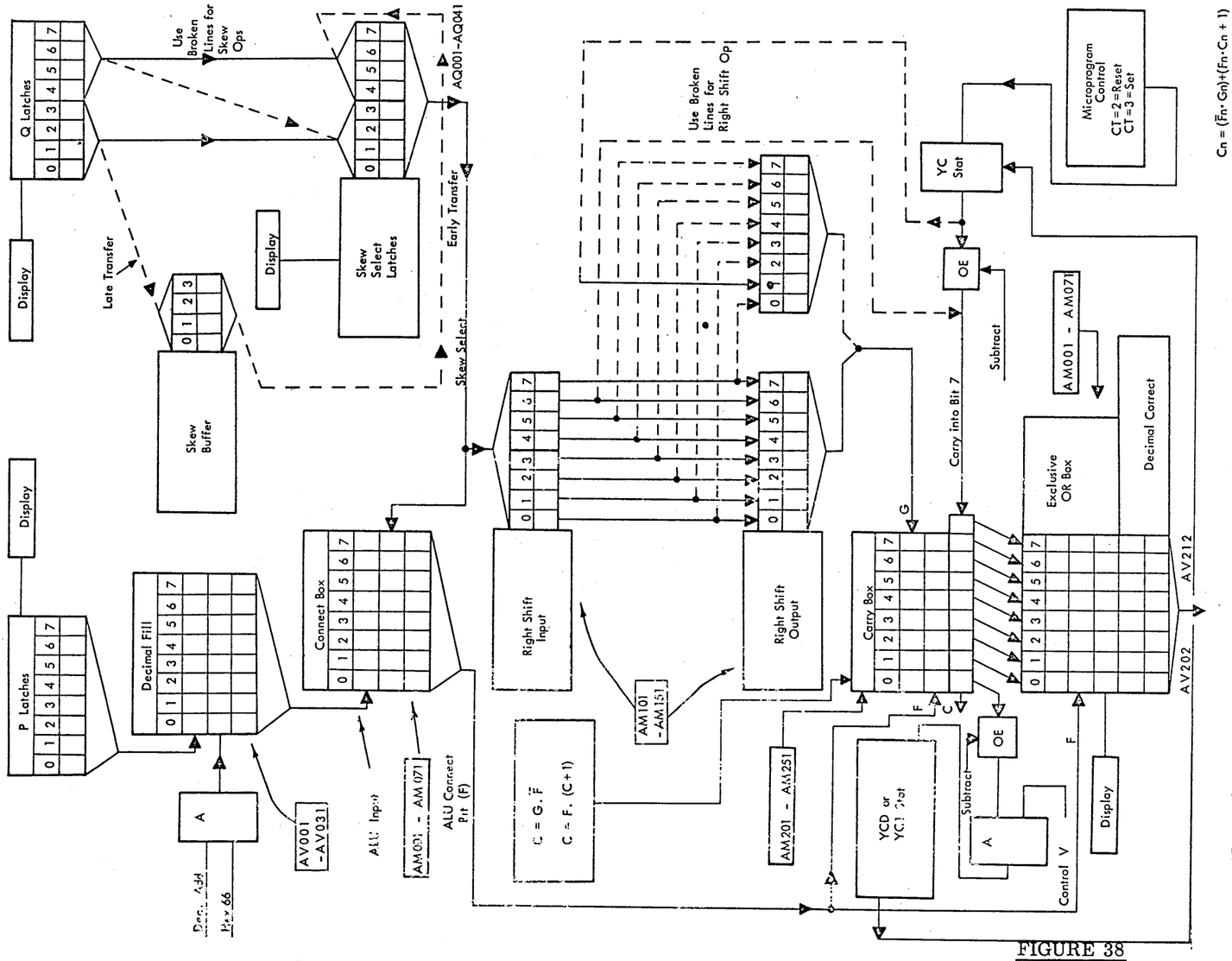


FIGURE 38

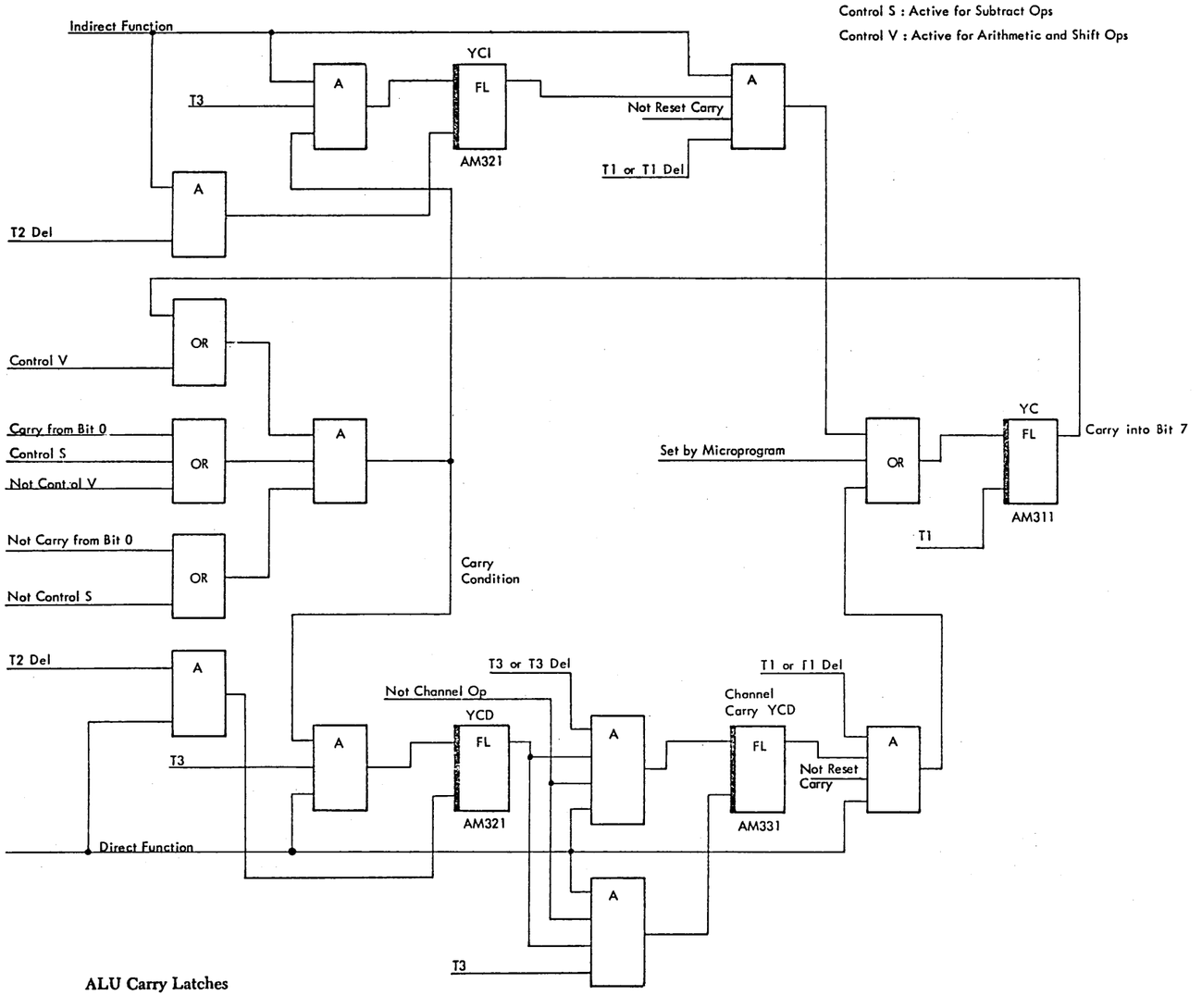


FIGURE 39

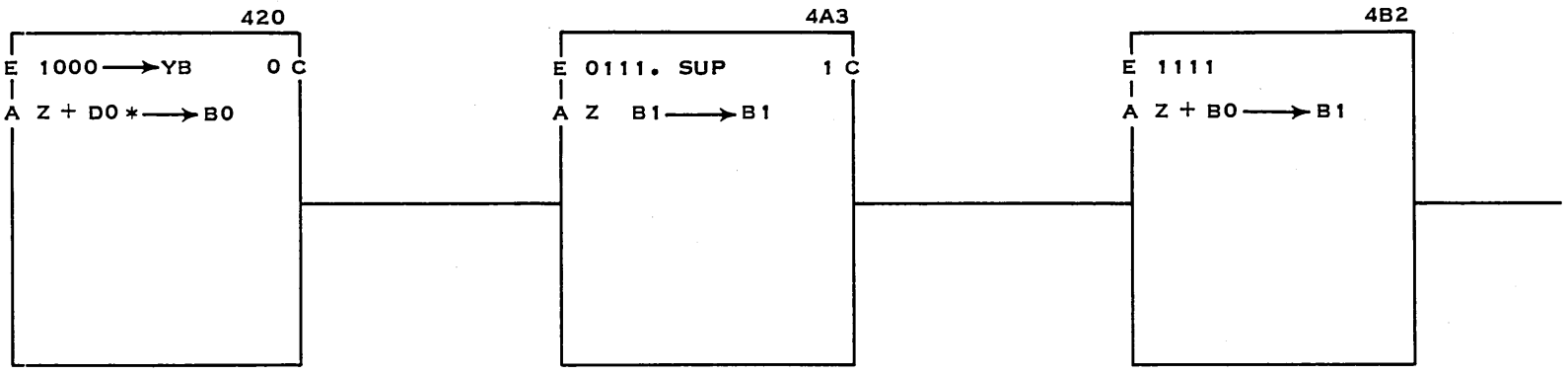


FIGURE 40

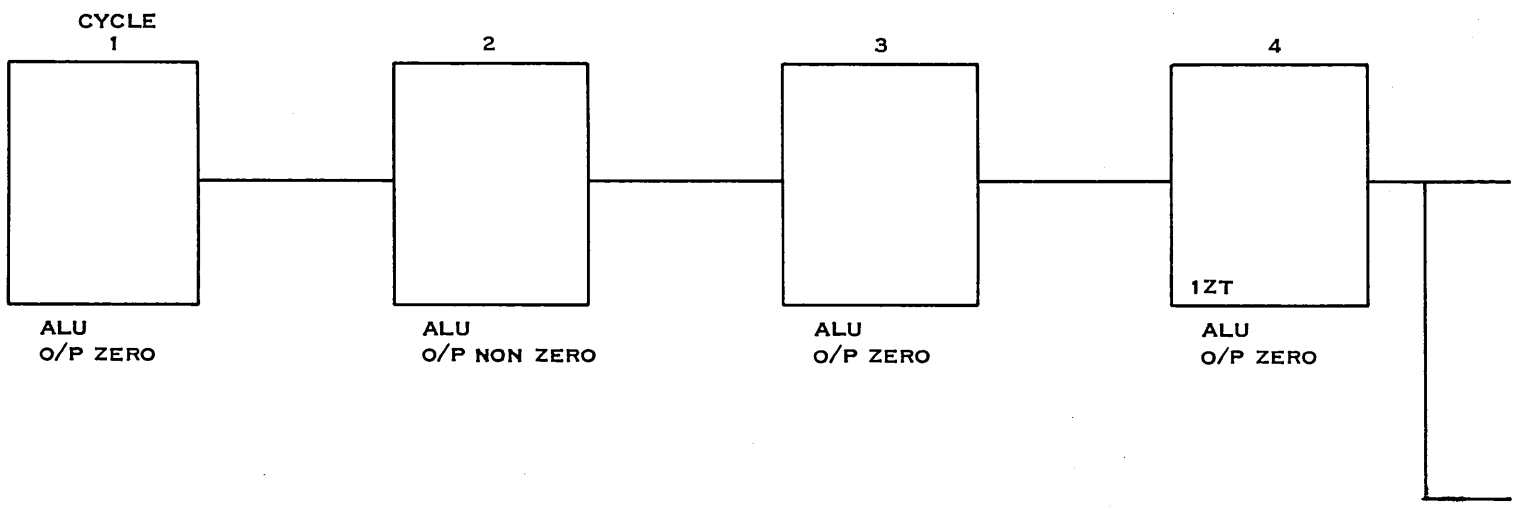


FIGURE 41

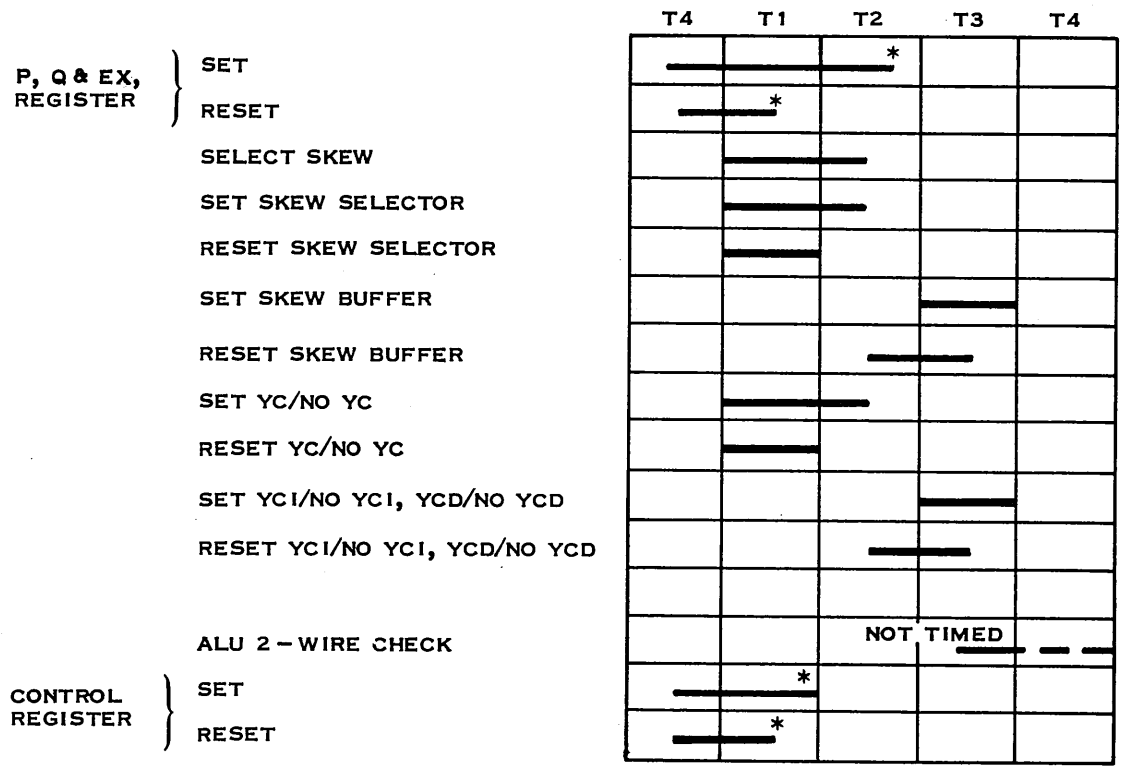
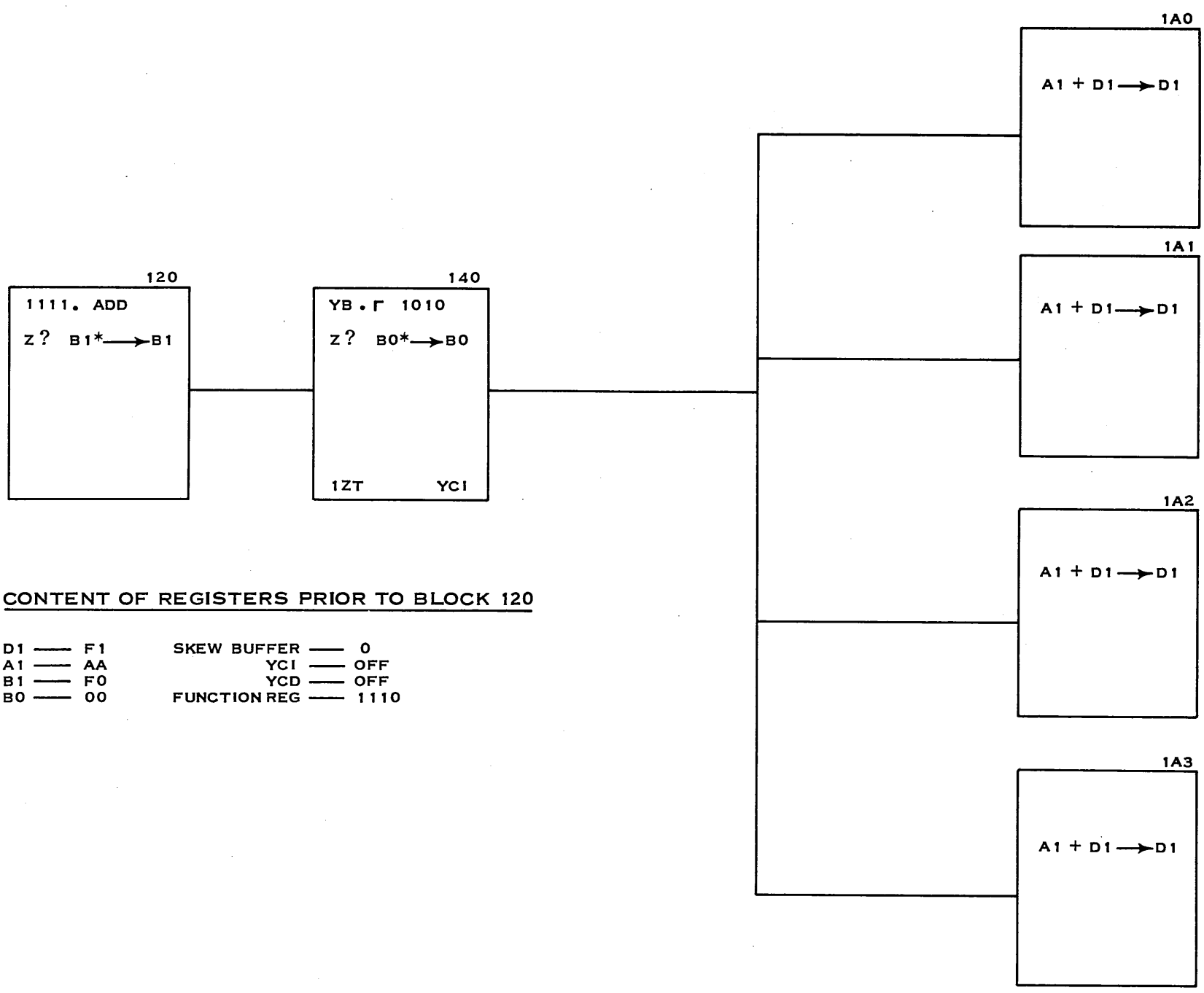


FIGURE 42



CONTENT OF REGISTERS PRIOR TO BLOCK 120

D1 —— F1
A1 —— AA
B1 —— F0
B0 —— 00

SKEW BUFFER —— 0
YCI —— OFF
YCD —— OFF
FUNCTION REG —— 1110

FIGURE 43

NORMAL ADDRESSING DECODING - BUMP LATCH OFF

	Z/S	Z/S									Z/S								
	Byte X		Byte 0								Byte 1								Bump Latch
ADDRESS REGISTER	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
STORAGE ADDRESS BUS BIT NUMBERING	1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	CPU Byte Designator	B
BINARY VALUE	1	8	4	4	2	1	8	4	2	1	1	2	1	8	4	2	1		
ASSIGNMENT	Model H 256K bytes	X, Y, Z, array Modifier	X DVR	Y Driver			Y Gate Decode				P/R	X Driver		X Gate Decode					OFF

Selects 1 of 2 128K byte units

Selects array 2 in 128K byte unit

Selects 1 of 8 Y array drivers 00-07

Array Modifier Selects Drivers 08-15

Selects 1 of 16 Y gate decode lines 00-15

Selects 1 of 8 X array drivers 00-07

Array Modifier Selects Drivers 08-15

Selects 1 of 16 X gate decode lines 00-15

Matrix combination of gate decode lines and drivers allow selection of 1 of 128 X and Y drive lines.

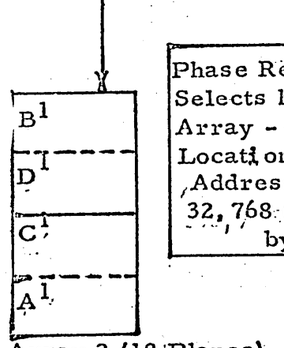
Normal coincident current addressing allows selection of 16,384 locations (128X, 128Y)
*Location = 2 bytes

Phase Reversal Bit Selects half of Array - Doubles Locations Addressable to 32,768 (65,536 bytes)

Phase Reversal Jumpering

	S	A	B
	15	14	6
A	0	0	0
B	0	0	1
C	0	1	0
D	0	1	1
A^1	1	0	0
B^1	1	0	1
C^1	1	1	0
D^1	1	1	1

Inhibit - Sense Segment Selection

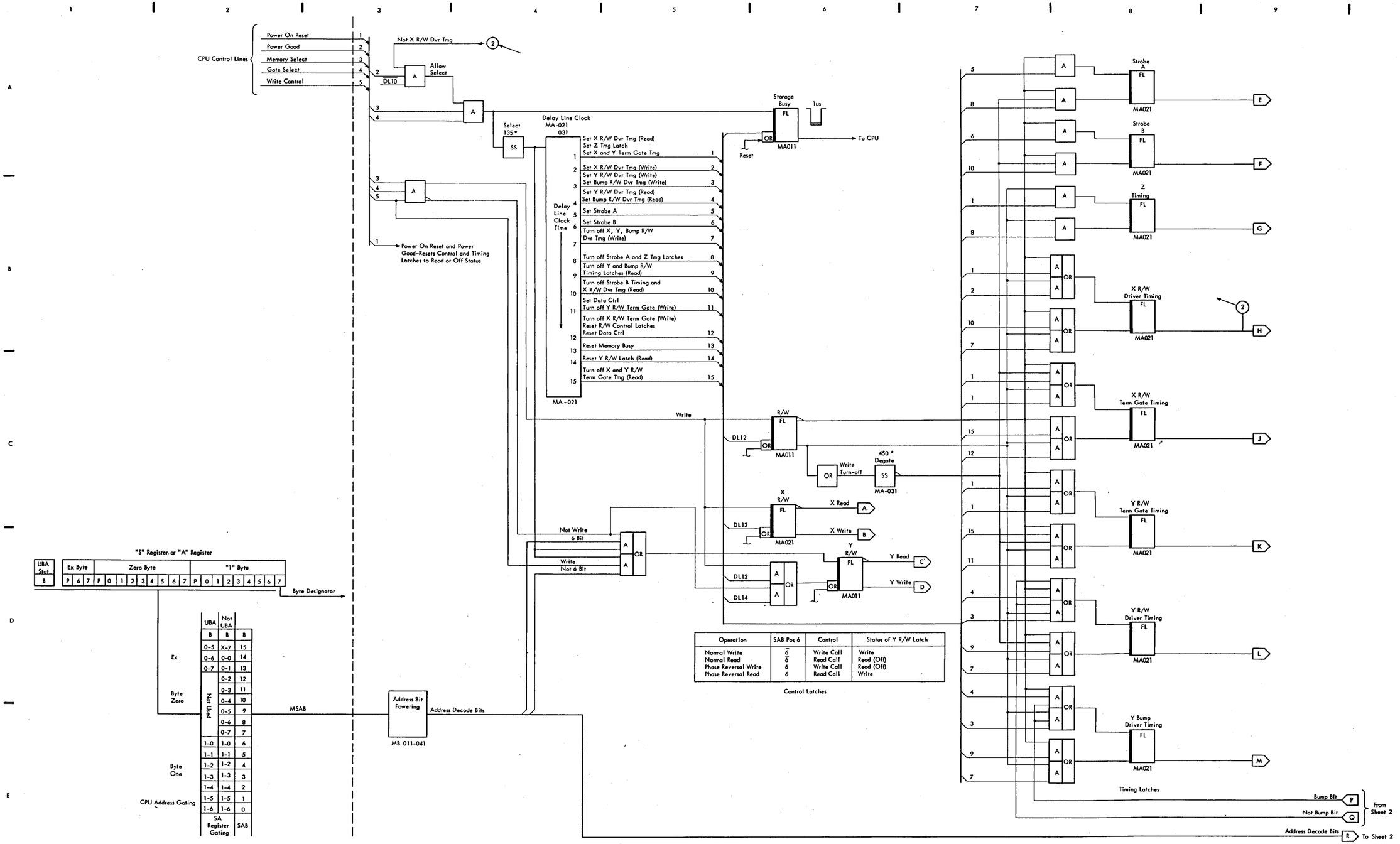


Array 2 (18 Planes)

Array 1 (18 Planes)

Figure 44

Figure 45



MAIN STORAGE CONTROL AND TIMING CIRCUITS

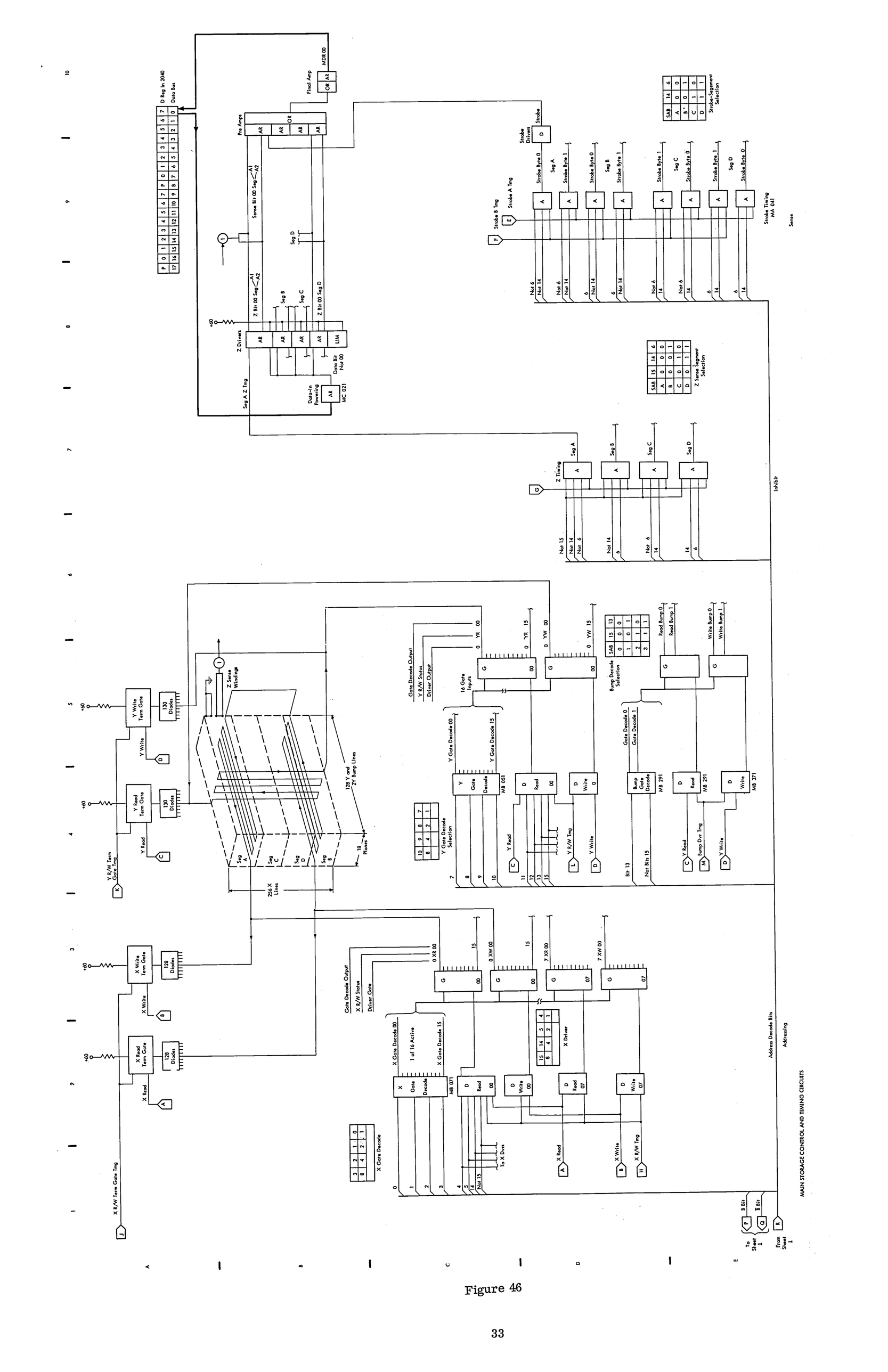

D Reg in 2040 Data Bus
Final Amp
MDR 00
Pre Amps
Sense Bit 00 Seg A1 A2
Seg D
Z Bit 00 Seg A1 A2
Seg B
Seg C
Z Bit 00 Seg D
Z Drivers
Data Bit Not 00
Data-in Powering
MC 021
Seg A Z Tmg
Strobe Driven
Strobe A Tmg
Strobe B Tmg
Strobe Byte 0
Strobe Byte 1
Seg A
Seg B
Seg C
Seg D
Strobe Timing MA 041
Stroke-Segment Selection
Z Sense Segment Selection
Z Timing
Inhibit
Sense
Z Sense Windings
Y Write Term Gate
Y Read Term Gate
130 Diodes
Y Write
Y Read
Y R/W Term Gate Tmg
128 Y and 2Y Bump Lines
18 Planes
Seg A
Seg C
Seg D
Seg B
256 X Lines
X Write Term Gate
X Read Term Gate
128 Diodes
X Write
X Read
X R/W Term Gate Tmg
Gate Decode Output
Y R/W Status
Driver Output
16 Gate Inputs
Y Gate Decode 00
Y Gate Decode 15
Y Gate Decode Selection
Y Gate Decode
MB 051
Read
Write
Bump Decode Selection
Read Bump 0
Read Bump 1
Write Bump 0
Write Bump 1
Gate Decode 0
Gate Decode 1
Bump Gate Decode
MB 291
MB 371
Bump Drv Tmg
Not Bits 15
Bit 13
X Gate Decode Output
X R/W Status
Driver Gate
X Gate Decode 00
X Gate Decode 15
1 of 16 Active
X Gate Decode
MB 071
X Driver
to X Drvs
X Write
X R/W Tmg
Address Decode Bits
Addressing
8 Bit
To Sheet 1
From Sheet 1
MAIN STORAGE CONTROL AND TIMING CIRCUITS

Figure 46

STORAGE PROJECT TIMING DIAGRAM

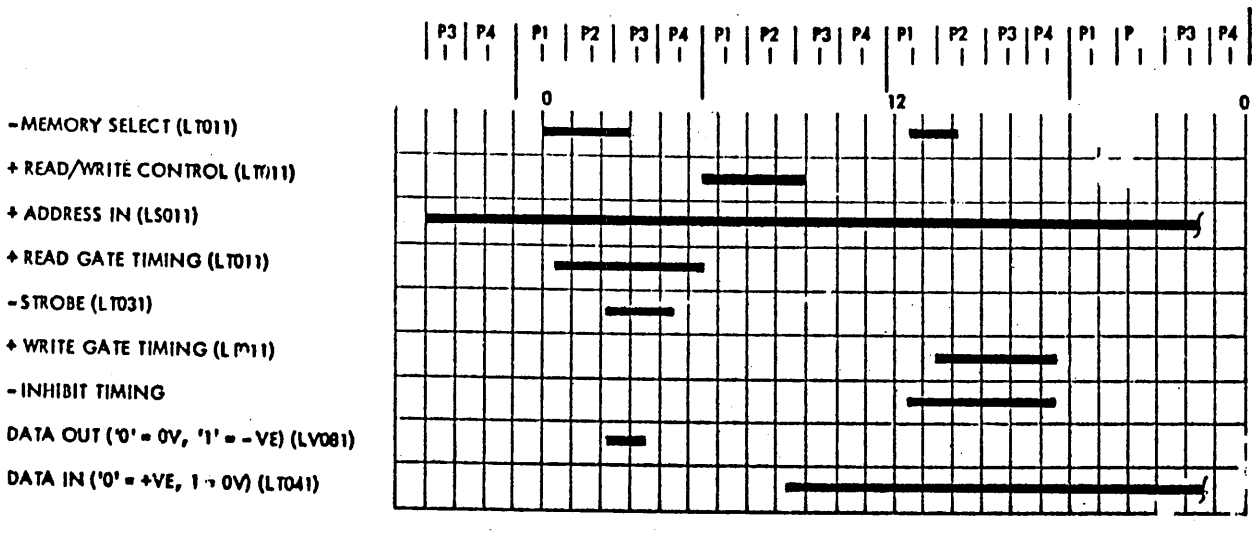
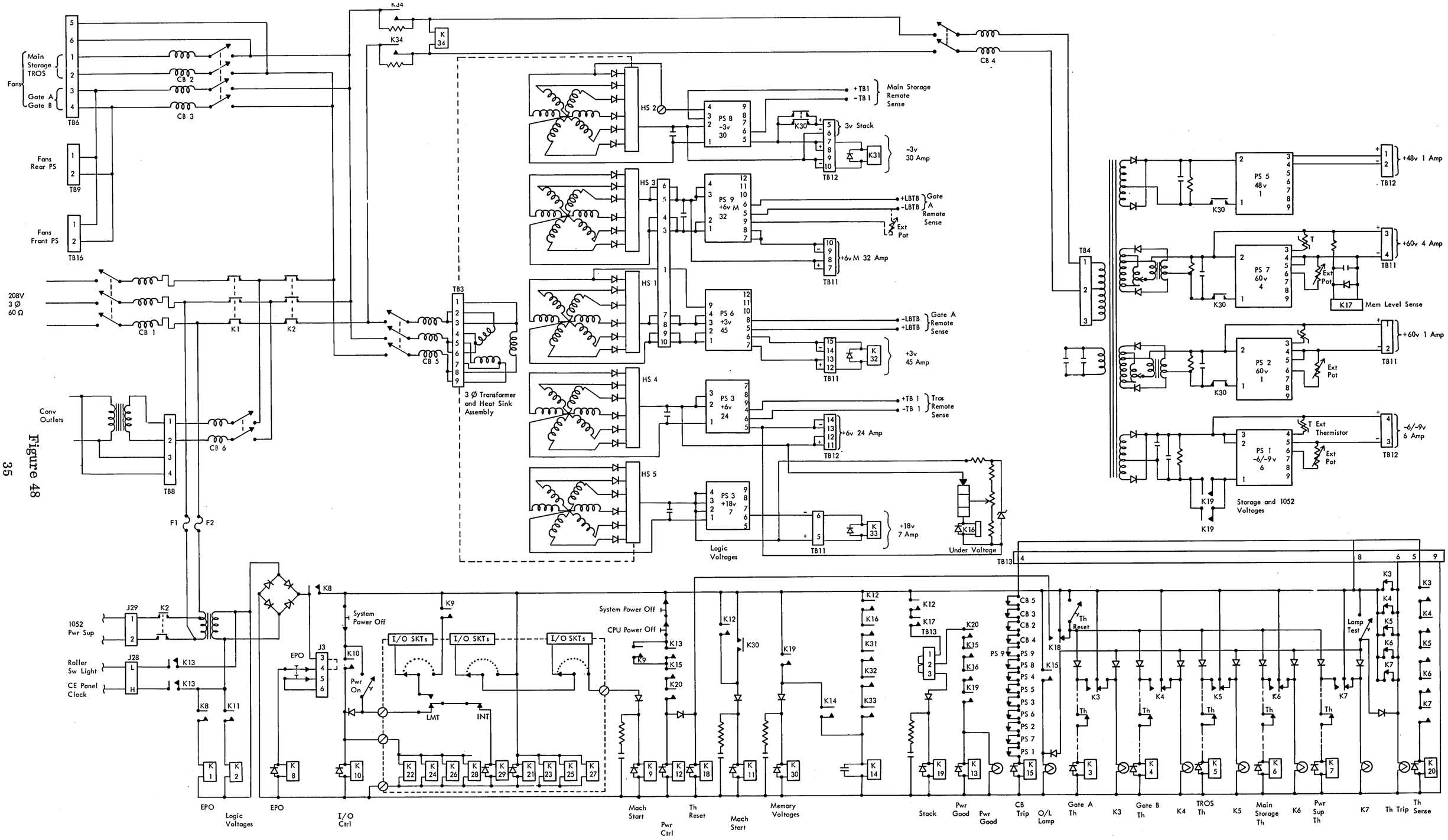


Figure 47

Figure 48



MID-PAC POWER SUPPLY WIRING DIAGRAM

```
MODEL 40 SYSTEMS ENVIRONMENT RECORDING EDIT AND PRINT PROGRAM (SEREP)

--- CPU ---

ROBAR          1 08C7    EARLY CK        1    CTRL CK         0    YA STATS       0000
A REG        0 36 A8     LATE CK         0    ROS ADDR CK     0    YB STATS       0000
B REG          10 60     RX PTY CK       0    ROS DATA CK     0    FUNCT REG  1 10010
C REG        0 00 19     RO PTY CK       0    B DEC CK        0    INH DUMP Y8        0
D REG          1A 16     R1 PTY CK       0    C DEC CK        0    SKEW REG        0010
J REG             44     MSAD PTY CK     0    D DEC CK        0
H REG             EC     ROAR CK         0    H LOAD DEC CK   0
P REG             00     LS RD PTY CK    0    H DES DEC CK    0
Q REG            *21     DO PTY CK       0    H INC DEC CK    0
LS 43-INST BUF    1A     D1 PTY CK       0    J DEC CK        0    PMA               0
SPLS KEY        0000     SPLS KEY CK     0    N DEC CK        0    IMA               0
SPLS DATA       0011     SPLS DATA CK    0    P DEC CK        0    I/O               0
ALU EXT          000     STAT PTY CK     0    Q DEC CK        0    YCD               0
                         P PTY CK        0    R DEC CK        0    YCI               0
                         Q PTY CK        1    D/Y8 CK         0    DP1               0
MPX INTRPT         0     2-WIRE I-P CAR  0
SC1 INTRPT         0     2-WIRE O-P CAR  0
SC2 INTRPT         0     ALU 2-W CKS    00
EXT INTRPT         0     EX PTY CK       0
                         SQ SEL CK       0
                         ALU FUN CK      0
                         LSAR PTY CK     0

 GP REGS 0-3     00 00 00 00     00 00 05 0A     00 00 20 00     00 00 30 00
 GP REGS 4-7     00 00 40 00     40 00 24 4C     00 00 00 19     00 00 04 F0
 GP REGS 8-B     00 00 00 80     00 00 79 B0     02 C5 D5 C4     00 00 00 02
 GP REGS C-F     45 30 00 00     04 00 00 00     00 00 48 A6     00 00 1F 00

 FP REGS 0-2     41 81 81 81     81 81 81 81     4E 10 10 10     10 0F DF DE
 FP REGS 4-6     41 11 22 22     33 33 11 11     AC 0F FF FF     FF FF FF FF

                 OLD MC PSW    00040000  400036AA
```

Figure 49

```
//EREP  JOB  NAME,NUMBER,MSGLEVEL=1
//ONLYSTEP  EXEC  PGM=IFCEREPO,PARM='
//SERLOG  DD  DSNAME=SYS1.LOGREC,DISP=
//EREPPT  DD  SYSOUT=A
// START RDR,00C
IEF236I ALLOC. FOR EREP      ONLYSTEP
IEF237I SERLOG   ON 190

OUTBOARD DATA EDITING AND PRINTING SEC

MODEL-UNIVERSAL

--- RECORD ENTRY SOURCE - OBR  ---

CHANNEL/UNIT ADDRESS  0182

PROGRAM IDENTITY  IEBGENER
                  C9C5C2C7 C5D5C5D9

      DAY  YEAR
DATE - 040  67

                CC   DA     FL     CT
FIRST CCW       02 02CDF0  00 00 0050
FAILING CCW     27 000000  60 00 0006

                K    CA     US CS  CT
CSW             00 001280  26 00 0006

 UNIT STATUS
  ATTENTION          0
  STATUS MODIFIER    0
  CONTROL UNIT END   1
  BUSY               0
  CHANNEL END        0
  DEVICE END         1
  UNIT CHECK         1
  UNIT EXCEPTION     0

SENSE BYTE DATA
  BYTE 0   BYTE 1   BYTE 2   BYTE 3
00000000 01001000 00000011 00000010

 CHANNEL STATUS
  PRGM-CTLD IRPT     0
  INCORRECT LENGTH   0
  PROGRAM CHECK      0
  PROTECTION CHECK   0
  CHAN DATA CHECK    0
  CHAN CTL CHECK     0
  I/F CTL CHECK      0
  CHAINING CHECK     0

  BYTE 4   BYTE 5
00000000 00000000
```

Figure 50

```
-- ENVIRONMENT RECORD EDITING AND PRINTING PROGRAM --

STATISTICAL DATA EDITING AND PRINTING SECTION

**********************************************************************

MODEL-UNIVERSAL
--- RECORD ENTRY SOURCE - SDR ---      TYPE - STATISTICAL DATA
CHANNEL/UNIT ADDRESS  000C             DEVICE TYPE  2540
TEMPY RDS          00001               TEMPY WRT          00000
INTRVN REQD        00030               BUS OUT CHK        00000
EQUIP CHK          00000

**********************************************************************

MODEL-UNIVERSAL
--- RECORD ENTRY SOURCE - SDR ---      TYPE - STATISTICAL DATA
CHANNEL/UNIT ADDRESS  000E             DEVICE TYPE  1403
TEMPY RDS          00000               TEMPY WRT          00000
INTRVN REQD        00030               BUS OUT CHK        00000
EQUIP CHK          00000               UNUSL CMND         00000

**********************************************************************

MODEL-UNIVERSAL
--- RECORD ENTRY SOURCE - SDR ---      TYPE - STATISTICAL DATA
CHANNEL/UNIT ADDRESS  0182             DEVICE TYPE  2400
TEMPY RDS          00003               TEMPY WRT          00001
INTRVN REQD        00011               BUS OUT CHK        00000
EQUIP CHK          00001               OVERRUN            00000
WD CT 0            00000               DATA CONV CHK      00000
R/W VRC            00002               LRCR               00002
SKEW               00000               CRC                00003
SKEW REG VRC       00001               NOISE              00001
```

Figure 51

MALFUNCTION ANALYSIS PROCEDURE - MAPS

BASIC HINTS FOR THE CE

1. The philosophy behind MAPS is basically to guide the CE and to minimize wrong conclusions
2. Analyse the console display carefully. Do not start logic page analysis until you are satisfied that the information provided by the indicators has been fully utilized
3. Locate the source check. This is particularly important in the case of channel checks
4. Some checks are more explicit than others. Always establish the amount of hardware funneled into a check by means of the appropriate ECAD. The amount of hardware involved will influence the procedure adopted to pinpoint the fault, i. e. in certain cases you can go straight to the card (s) involved
5. Switch on your scope at the beginning of the card-changing activity
6. Where possible change cards in preference to scoping since this process of elimation is far less susceptible to misleading conclusions
7. Always look for some common relationship between fault symptoms

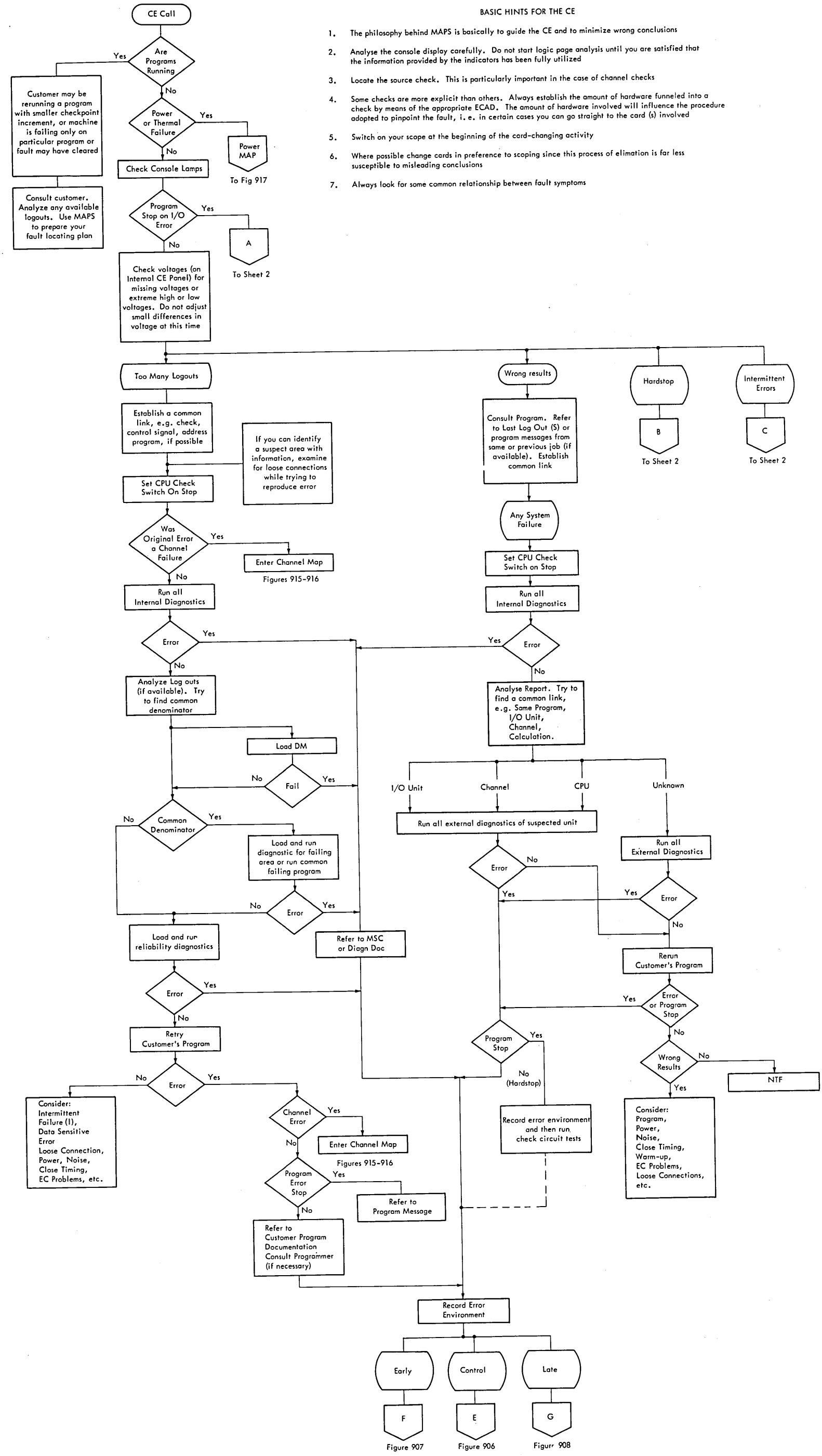


FIGURE 901. INTERPRET ERRORS (SHEET 1 OF 2)

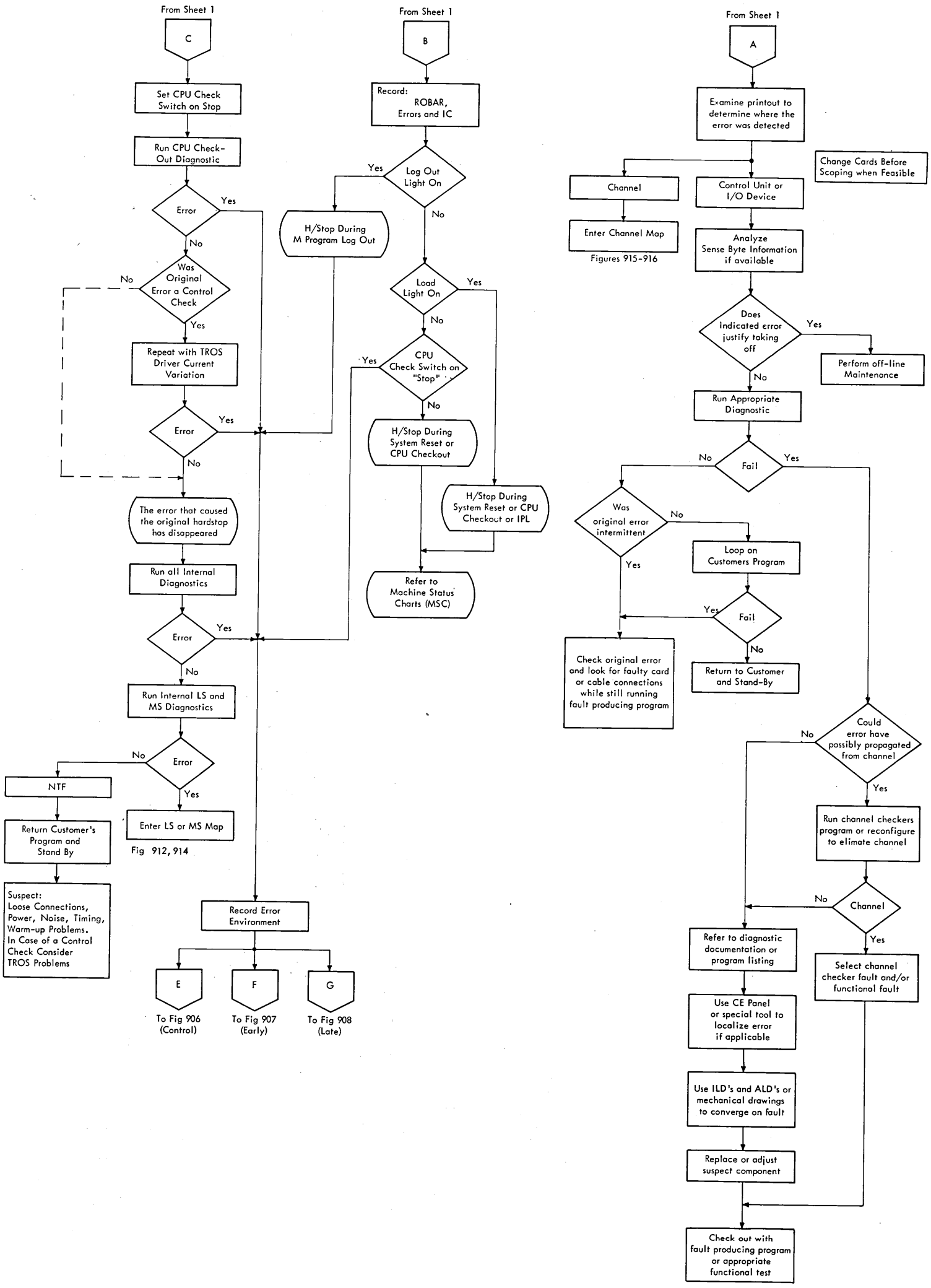


FIGURE 901. INTERPRET ERRORS (SHEET 2 OF 2)

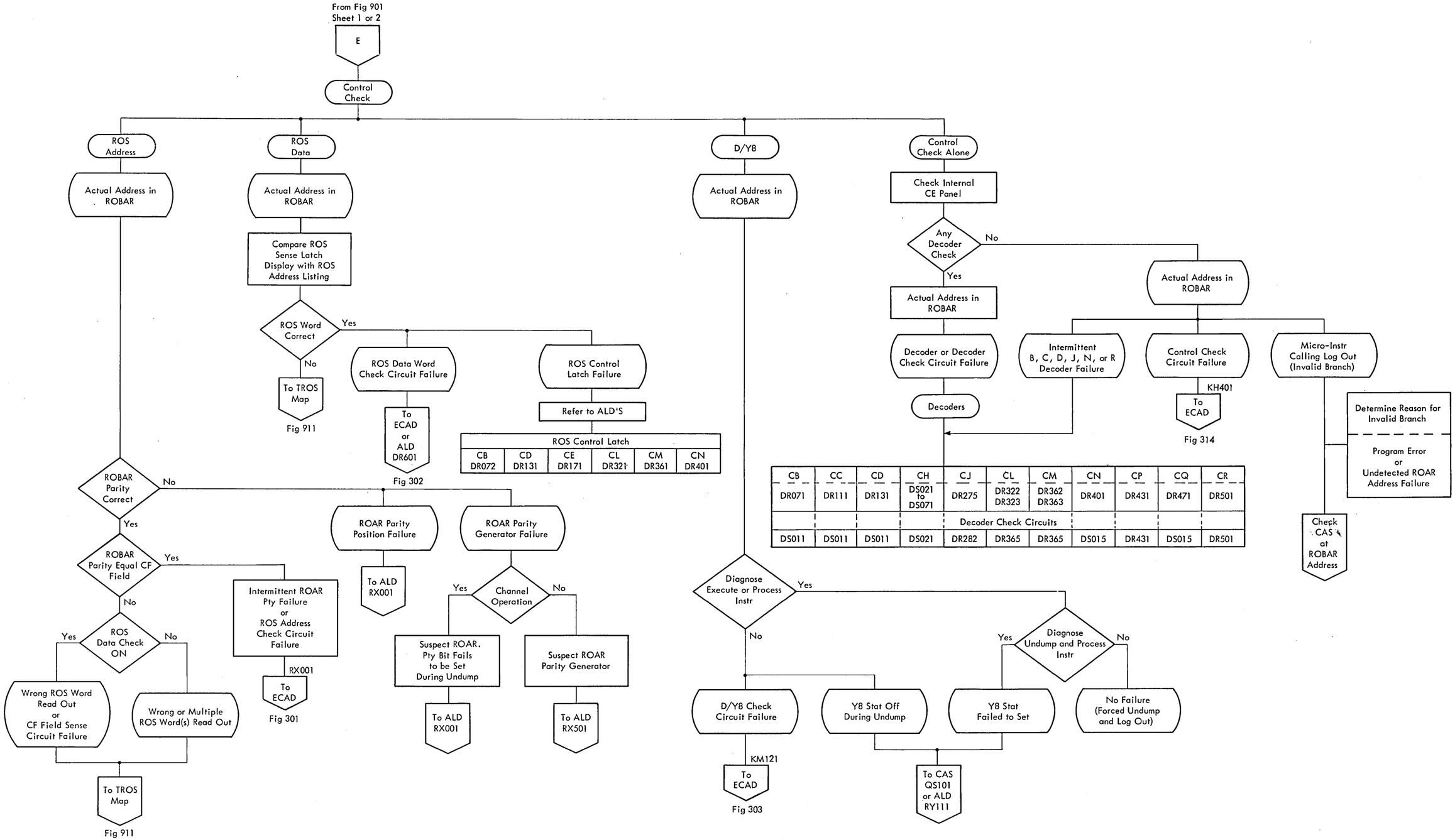


FIGURE 906. CONTROL CHECK

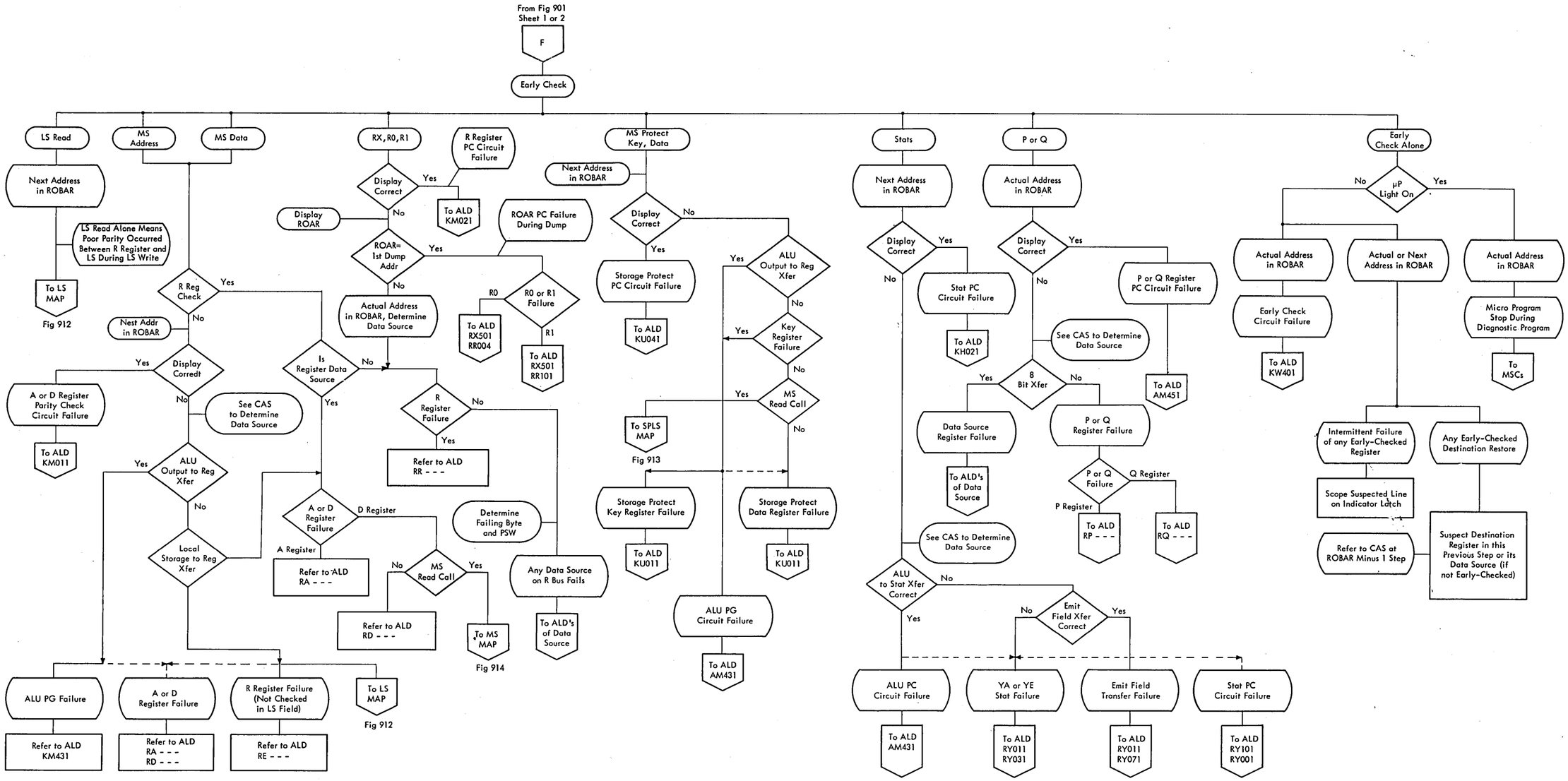


FIGURE 907. EARLY CHECK

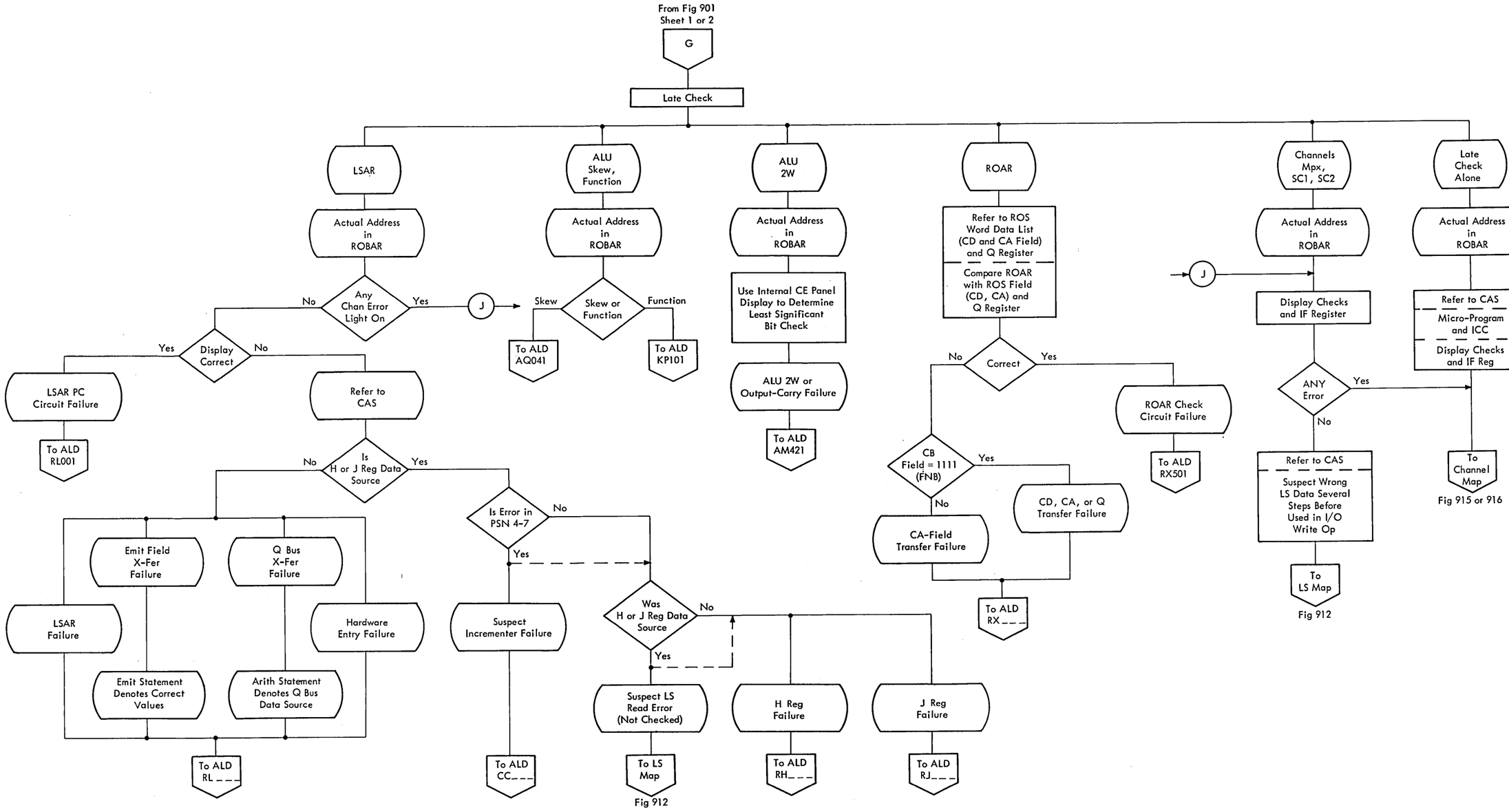


FIGURE 908. LATE CHECK

All 1's Test Word Address= 020
All 0's Test Work Address= 010

(a) ROS Error Suspected or Machine Stop with some ROS Check Lights On

(b) Note Check Lights, Note ROBAR Address and Control Word Contents

(c) Test all Check Lights to Prevent false deductions

(d) Check System Power Supplies -3, -3 +6, volts + 4% Check drive current — Do Not Adjust at this Point

(1)

Complete Word No '1's out

(1a) Manually Select All '1's Test Word (00800)

(2) See Note 1

(2a) Some or all '1's out

Revert to Error Word adr

Invert adr bits 0, 1, 2, 3, 4, 5

(3)

(3a) Some '1's out

Invert adr bits 3, 4, 5

(4)

(4a) Some '1's out

Invert adr bits 0, 2, 3, 4, 5

(5)

(5a) Some '1's out

Revert to Error Word Add

Invert Adr Bit 7

(6)

(6a) Some '1's out

Invert adr bit 7

Short Error Word Diode on Diode Card

(7)

(7a) Some '1's out

Change Diode

No '1's out (7b)

Check Word Tape for Continuity on Diode Card Pins

No '1's out (6b)

Change Driver Card

No '1's out (5b)

Change Driver Decoder Card

No '1's out (4b)

Change Driver Decoder

Change Driver Supplies Card

No '1's out (3b)

Revert to Error Word Add

Invert Adr Bit 6

(5)

(8a) Some '1's out

Invert Adr Bits 6, 7

(9)

(9a) Some '1's out

Change Gate Card

No '1's out (9b)

Change Gate Decoder Card

No '1's out (8b)

Invert Adr Bit 7

(10)

(10a) Some '1's out

Change Gate Decoder Card

No '1's out (10b)

Change Gate Strobe Card

No '1's out

Change Gate Strobe Select Card H3

No '1's out

No '1's out (2b)

Invert Adr Bits 0, 1, 2

(11)

(11a) Some '1's out

Invert Adr Bits 0, 1, 2, 3, 4, 5

(12)

(12a) Some '1's out

Change Driver Card

No '1's out (12b)

Change Driver Decoder Card

(13)

(13a) Some '1's out

Change Driver Decoder Card

Driver Supplies Card

No '1's out (13b)

Revert to all '1' Test Word

Invert Adr Bit 6

(14)

(14a) Some '1's out

Invert Adr Bits 6, 7

(15)

(15a) Some '1's out

Change Gate Card

No '1's out (15b)

Change Gate Decoder Card

No '1's out (14b)

Invert Adr Bit 7

(16a) Some '1's out

Change Gate Decoder Card

No '1's out (16b)

Interchange Gate Strobe Cards

(17a) If available

18

(18a) Some '1's out

Change Gate Strobe Card

No '1's out (18b)

If not available (17b)

Change Gate Strobe Card

(2)

Check Level of +PWR Good

02A1 - G6D12

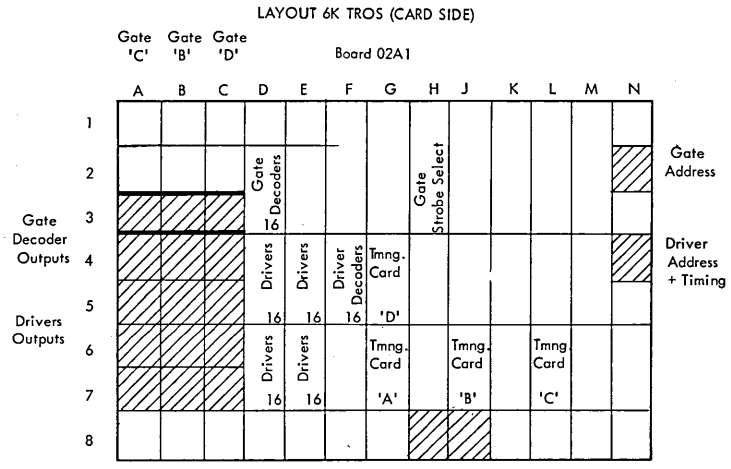
Change Timing Card A

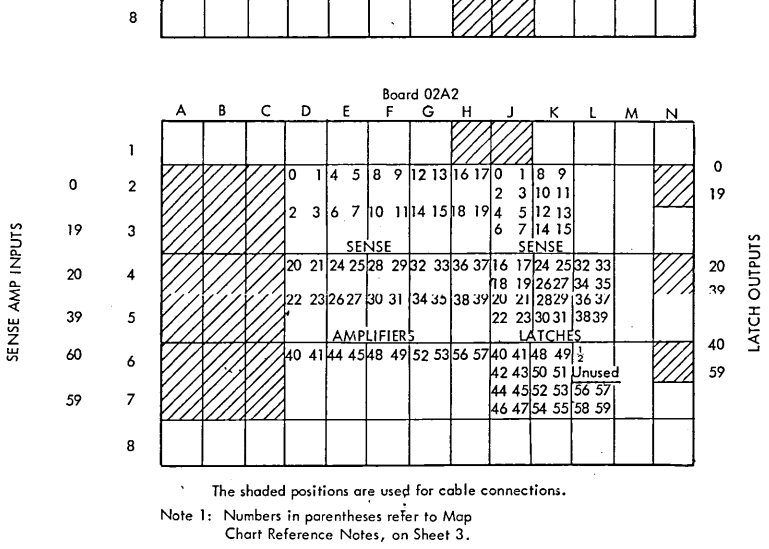
Change Timing Card B

Change Timing Card C

Change Timing Card D

LAYOUT 6K TROS (CARD SIDE)





The shaded positions are used for cable connections.

Note 1: Numbers in parentheses refer to Map Chart Reference Notes, on Sheet 3.

FIGURE 911. READ ONLY STORAGE (SHEET 1 OF 3)

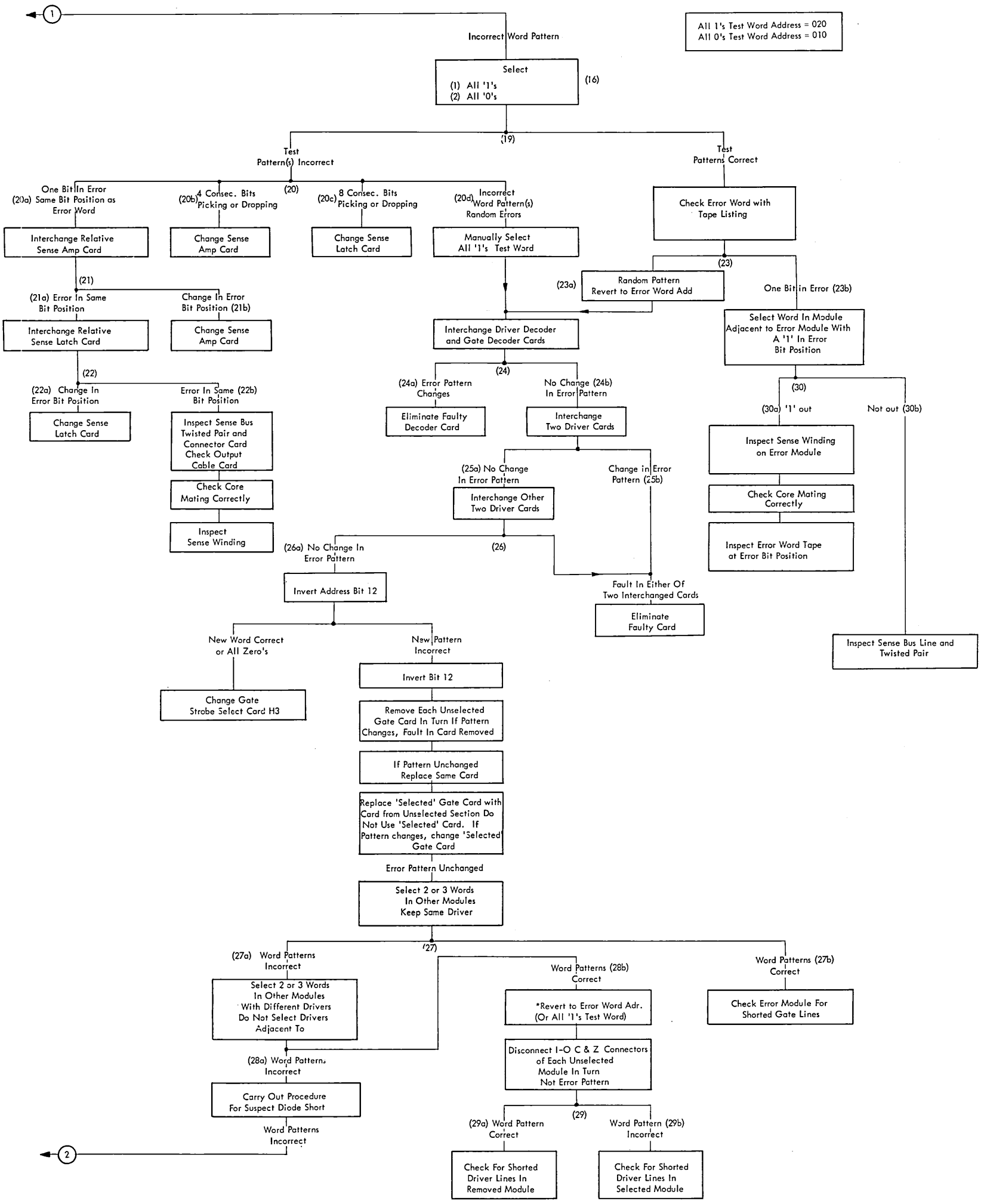
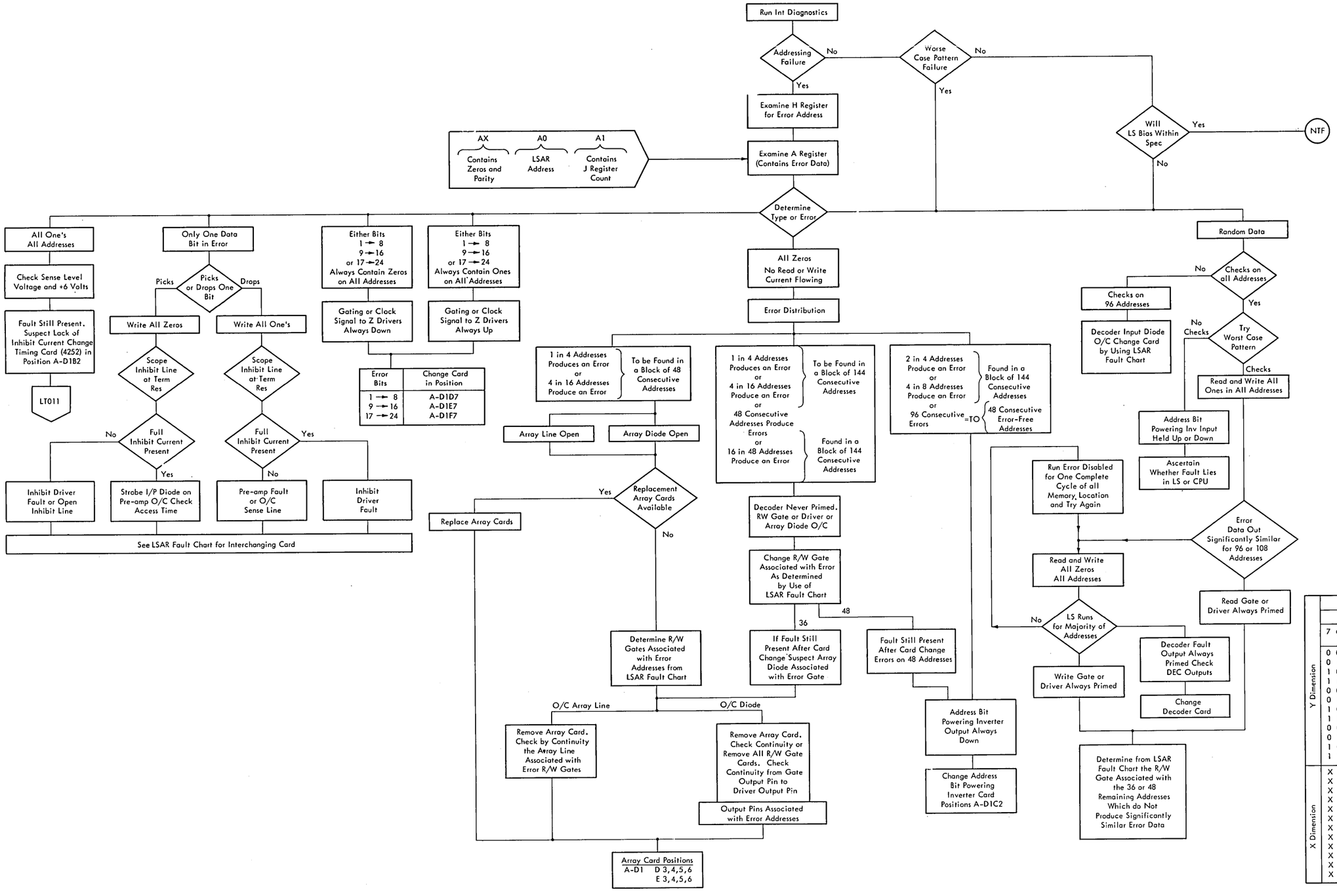


FIGURE 911. READ ONLY STORAGE (SHEET 2 OF 3)

MAP Chart Reference	Notes
a) b) c)	On entering the ROS MAP, the machine status, checks and supplies are noted before branching at 1. The presence of ROS drive current indicated by the CPU meter shows that drive current is available but does not necessarily mean that drive current is passing through the drive lines.
1 a)	The first branch is taken on the test for no 1's or incorrect word pattern. If no 1's, an attempt is made in the following tests to obtain some output, using the test word for all 1's if necessary, to prove the supplies, timing and sense circuits etc.
2	If some or all 1's out are obtained at branch 2 test, selecting the error address and inverting bits 0 through 5 will retain the gate of the error word but will select a different driver and driver decoder bits.
3 a) 4 5 5 7	Some 1's out at test 3 indicates a probable driver or driver decoder fault and tests 4, 5, and 6 are concerned with isolating such failures. Another possibility is an open circuit diode which is isolated by tests 6 and 7. Inverting bit 7 of the error address will retain the error word driver but will select a different gate in the same module.
4 b)	No 1's out at test 4 could indicate a fault in the tens driver decoder (address bits 6, 7, and 8). As the driver supply runs parallel to the decoded tens lines, it could also be a supply failure. The possible decoder error should be eliminated first.
3 b)	No 1's out at test 3 suggests a gate, a gate decoder, or a gate strobe failure. The various possibilities are isolated by tests 8, 9, and 10. Changing address bits 6 and 7 retains the original driver but changes the gates within the same module.
2 b) 11 through 18	If no 1's out are obtained at test 2, a similar series of tests to those listed above are conducted in tests 11 through 18, using the all 1's test word as the error word.
16 b) 17 b)	The interchange of gate strobe cards at 16 b) is only possible if both frames of ROS are used. If only one frame is used, a card change is made at 17 b).
1 b)	If incorrect word patters are obtained at test 1, the two diagnostic test words should be selected and the resulting outputs observed for a repeatable error pattern. Due to the packaging of the logic circuitry, this may give a clue to the faulty area as at branches 20 a), b), and c).
21 22	One particular bit in error is isolated by the interchange of cards and tests 21 and 22.
24 25 26	Random error patterns from the error word or all 1's test word are, as far as possible, isolated by the removal or interchange of card at tests 24, 25, and 26.
27 28	If the above tests do not affect the random error pattern, further tests are made to isolate the failing module. Drivers adjacent to the error drive should not be used in test 28, as a drive short would most likely be to an adjacent line.
28 b) 29	The error module is isolated by removal of the I/O connectors in branch 28 b) and the module checked for shorts at test 29.
28 a)	If throughout the tests branch 28 a) is reached without a correct pattern being obtained, a short-circuit diode should be suspected.
23 b) 30	Correct word patterns from the test words but one bit in error from the error word as in branch 23 suggest a sense circuit failure. The failing area can be isolated by test 30 and branches 30 a) and 30 b). Selecting a word in an adjacent module (i.e., on the same frame) with a 1 in the error position indicates a common fault (e.g., bus line) if there is no 1 out.

FIGURE 911. READ ONLY STORAGE (SHEET 3 OF 3)

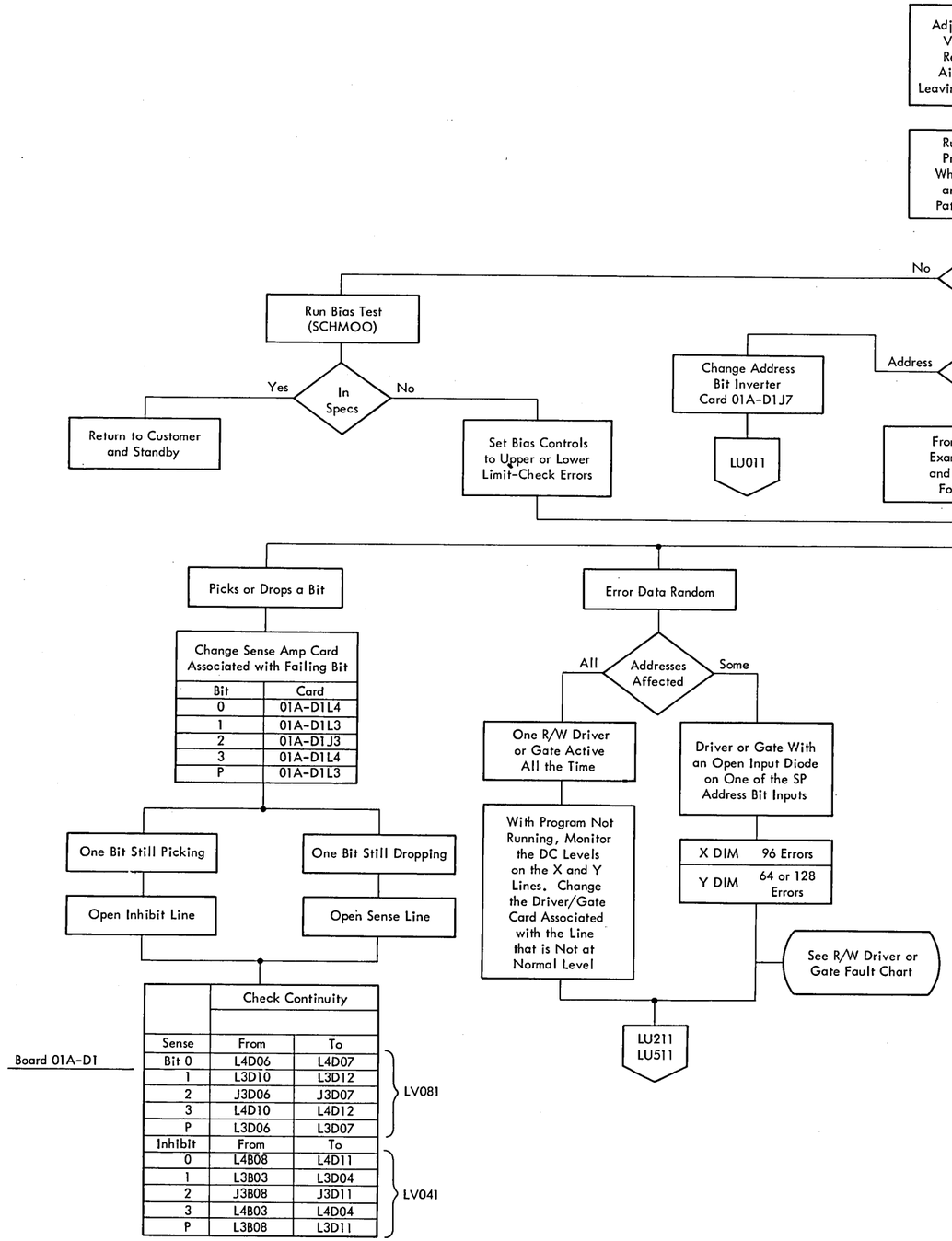


Bit Fails	Pre-amp Z Driver		Term Res or Output Pin
1	A-D1	B6	B03
2		C7	B08
3		B5	B08
4		C4	B08
5		C7	B03
6		C6	B08
7		C5	B08
8		C4	B03
9		B6	B08
10		C6	B03
11		B5	B03
12		C5	B03
13		F6	B03
14		G6	B08
15		F5	B03
16		F4	B08
17		G6	B03
18		F5	B08
19		G5	B03
20		F4	B03
21		F6	B08
22		G5	B08

LSAR Fault Chart

	LSAR Error Addresses								DEC and R/W Gate Faults	
									36 Error Addr	48 Error Addr
	7	6	5	4	3	2	1	0	Replace Card in Position	Replace Card in Position
Y Dimension	0	0	X	X	0	0	X	X	A-D1C3	A-D1E3
	0	1	X	X	0	0	X	X		
	1	0	X	X	0	0	X	X		
	1	1	X	X	0	0	X	X		
	0	0	X	X	1	0	X	X		
	0	1	X	X	1	0	X	X		
	1	0	X	X	1	0	X	X		
	1	1	X	X	1	0	X	X		
	0	0	X	X	1	1	X	X		
	0	1	X	X	1	1	X	X		
	1	0	X	X	1	1	X	X		
	1	1	X	X	1	1	X	X		
X Dimension	X	X	0	0	X	X	0	0	A-D1D2	A-D1E2
	X	X	0	1	X	X	0	0		
	X	X	1	0	X	X	0	0		
	X	X	1	1	X	X	0	0		
	X	X	0	0	X	X	0	1		
	X	X	0	1	X	X	0	1		
	X	X	1	0	X	X	0	1		
	X	X	1	1	X	X	0	1		
	X	X	0	0	X	X	1	1		
	X	X	0	1	X	X	1	1		
	X	X	1	0	X	X	1	1		
	X	X	1	1	X	X	1	1		

FIGURE 912. LOCAL STORAGE



Read/Write Driver or Gate Fault Chart

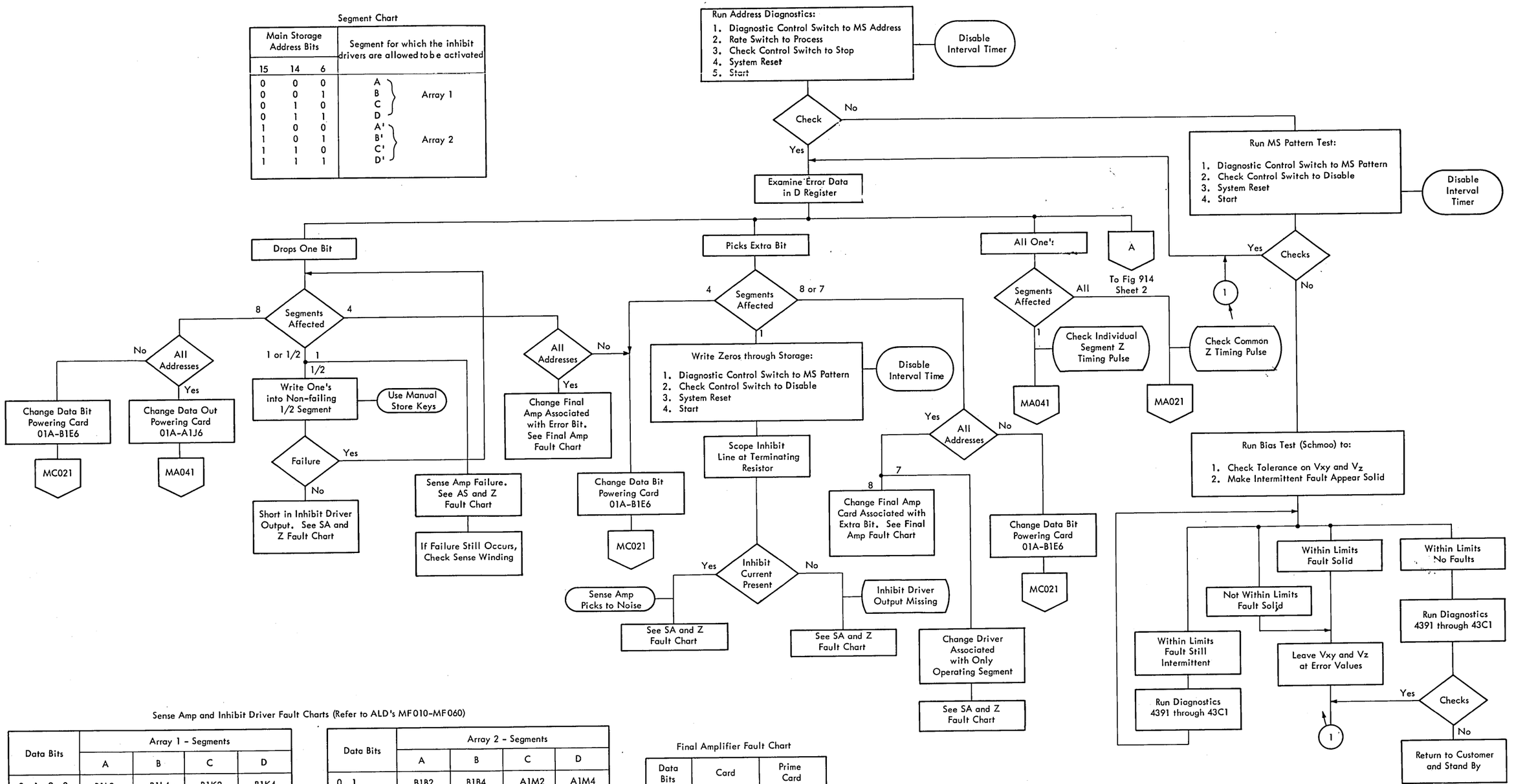
KEY	DIM	Main Storage Address Bits Common to All Error Addresses																Card Location
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
CPU	X					X	X											01A-D1L5
				X	X													D1J5
	Y	X	X															D1L2
		X	X															D1L2
MPX	X												X	X				D1L5
											X	X						D1J5
	Y		X	X														D1L2
								X										D1J2

LU211 to LU511

FIGURE 913. STORAGE PROTECT MAP

Segment Chart

Main Storage Address Bits			Segment for which the inhibit drivers are allowed to be activated	
15	14	6		
0	0	0	A	Array 1
0	0	1	B	
0	1	0	C	
0	1	1	D	
1	0	0	A'	Array 2
1	0	1	B'	
1	1	0	C'	
1	1	1	D'	



Sense Amp and Inhibit Driver Fault Charts (Refer to ALD's MF010-MF060)

Data Bits	Array 1 - Segments			
	A	B	C	D
0, 1, 2, 3	B1L2	B1L4	B1K2	B1K4
4, 5, 6, 7	B1J2	B1H4	B1H2	B1G4
8, 9, 10, 11	B1G2	B1F4	B1F2	B1E4
12, 13, 14, 15	B1E2	B1D4	B1D2	B1C4
16, 17	B1B2	B1B4	A1M2	A1M4

Data Bits	Array 2 - Segments			
	A	B	C	D
0, 1	B1B2	B1B4	A1M2	A1M4
2, 3, 4, 5	A1L2	A1L4	A1K2	A1K4
6, 7, 8, 9	A1H2	A1J4	A1G2	A1H4
10, 11, 12, 13	A1F2	A1G4	A1E2	A1F4
14, 15, 16, 17	A1D2	A1D4	A1C2	A1C4

Final Amplifier Fault Chart

Data Bits	Card	Prime Card	
0-8	01A-B1J4	01A-A1J2	ALD's MC031 through MC084
9-17	01A-B1C2	01A-A1E4	

FIGURE 914. 64K MAIN STORAGE MAP (SHEET 1 OF 2)

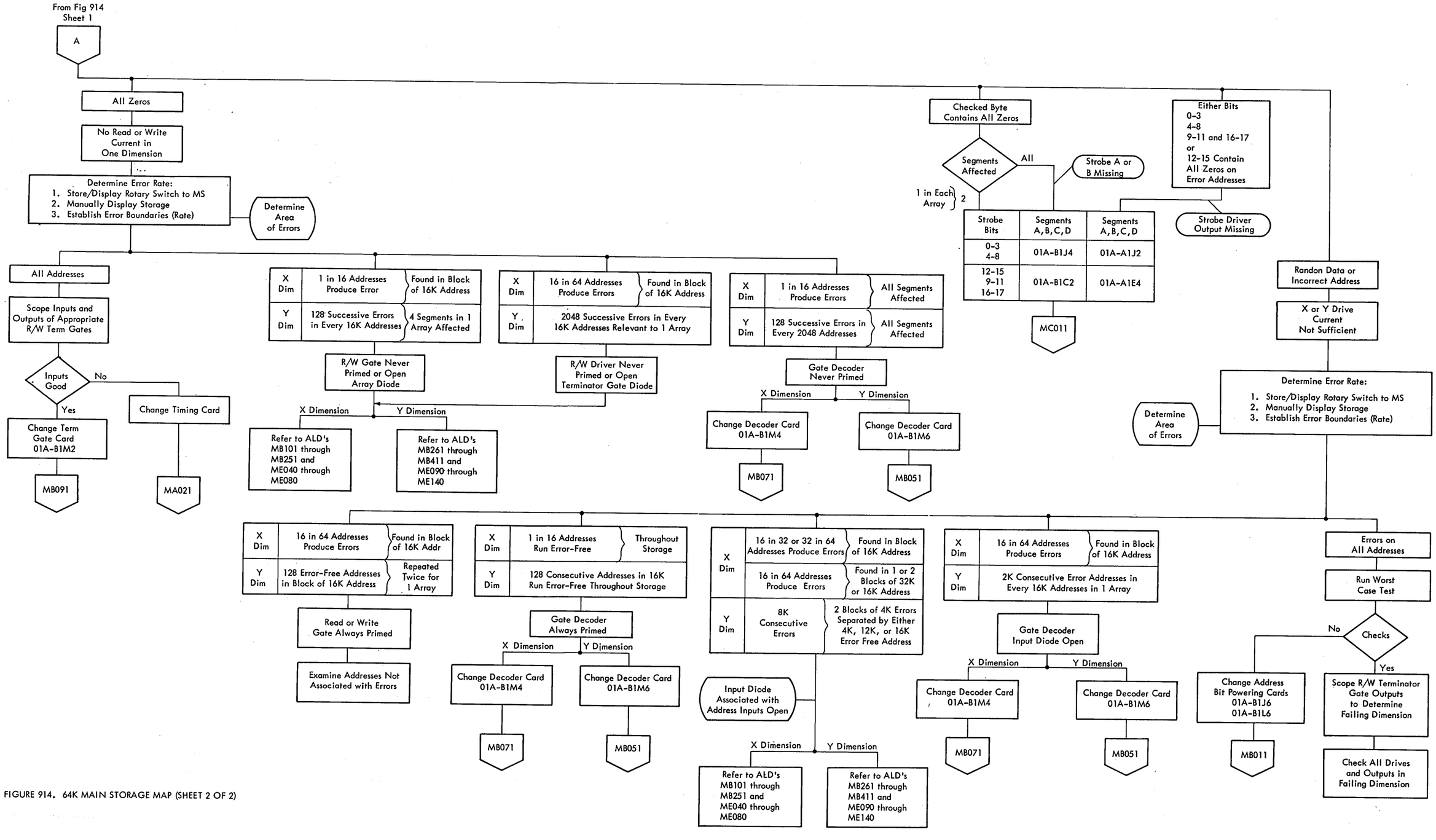
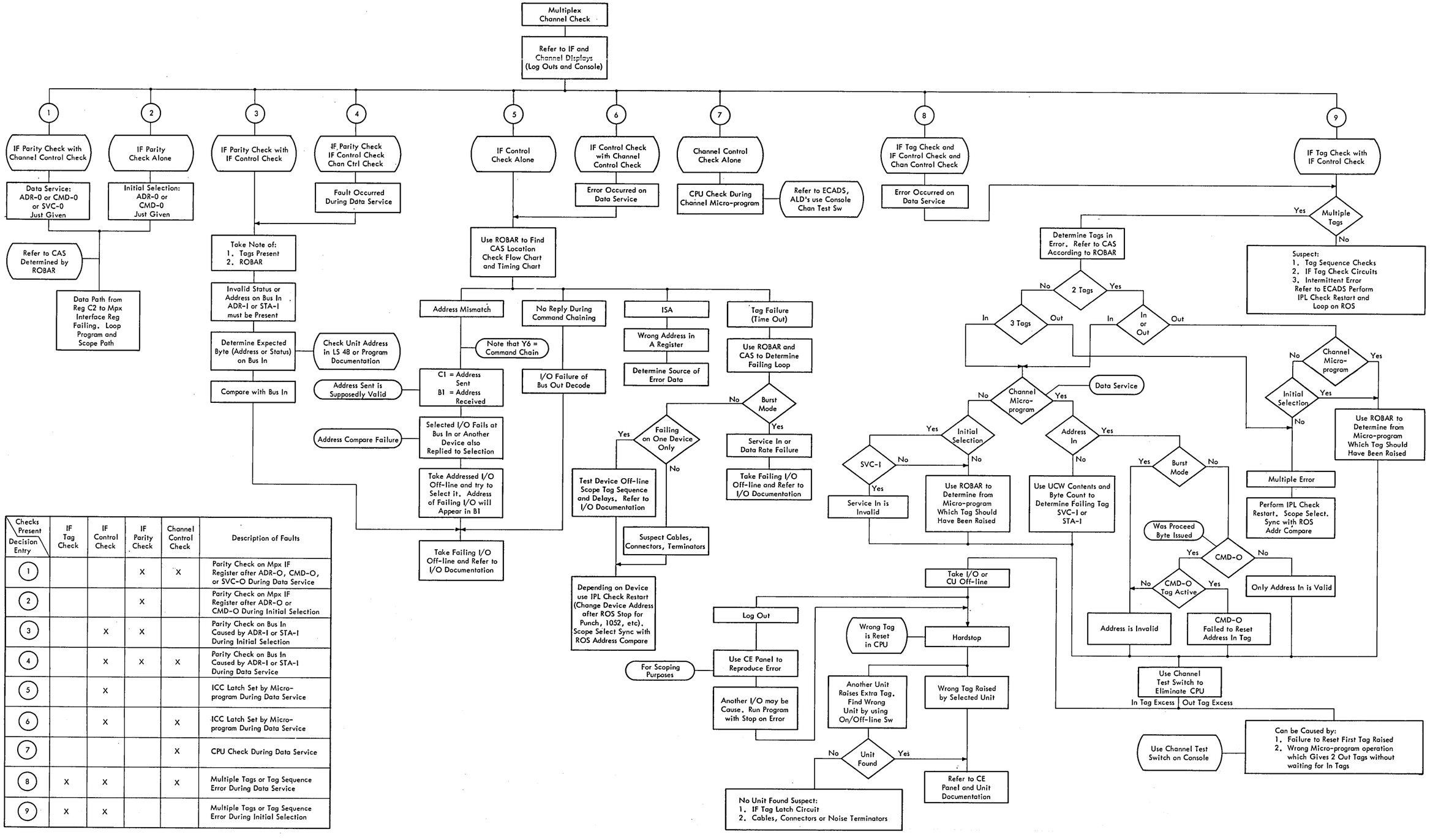
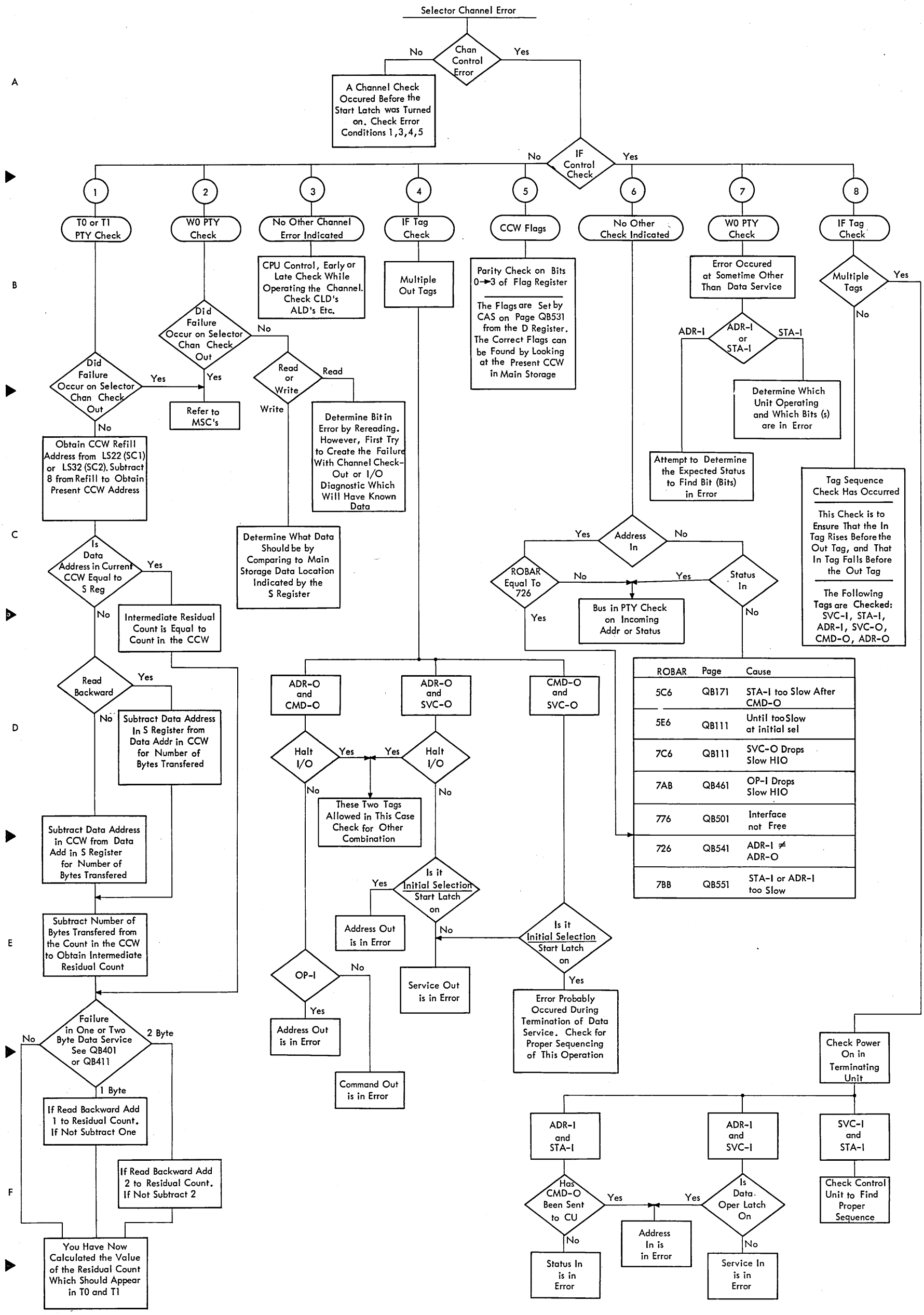


FIGURE 914. 64K MAIN STORAGE MAP (SHEET 2 OF 2)



Checks Present / Decision Entry	IF Tag Check	IF Control Check	IF Parity Check	Channel Control Check	Description of Faults
1			X	X	Parity Check on Mpx IF Register after ADR-O, CMD-O, or SVC-O During Data Service
2			X		Parity Check on Mpx IF Register after ADR-O or CMD-O During Initial Selection
3		X	X		Parity Check on Bus In Caused by ADR-I or STA-I During Initial Selection
4		X	X	X	Parity Check on Bus In Caused by ADR-I or STA-I During Data Service
5		X			ICC Latch Set by Micro-program During Data Service
6		X		X	ICC Latch Set by Micro-program During Data Service
7				X	CPU Check During Data Service
8	X	X		X	Multiple Tags or Tag Sequence Error During Data Service
9	X	X			Multiple Tags or Tag Sequence Error During Initial Selection

FIGURE 915. MULTIPLEX CHANNEL MAP



ROBAR	Page	Cause
5C6	QB171	STA-I too Slow After CMD-O
5E6	QB111	Until too Slow at initial sel
7C6	QB111	SVC-O Drops Slow HIO
7AB	QB461	OP-I Drops Slow HIO
776	QB501	Interface not Free
726	QB541	ADR-I ≠ ADR-O
7BB	QB551	STA-I or ADR-I too Slow

FIGURE 916. SELECTOR CHANNEL

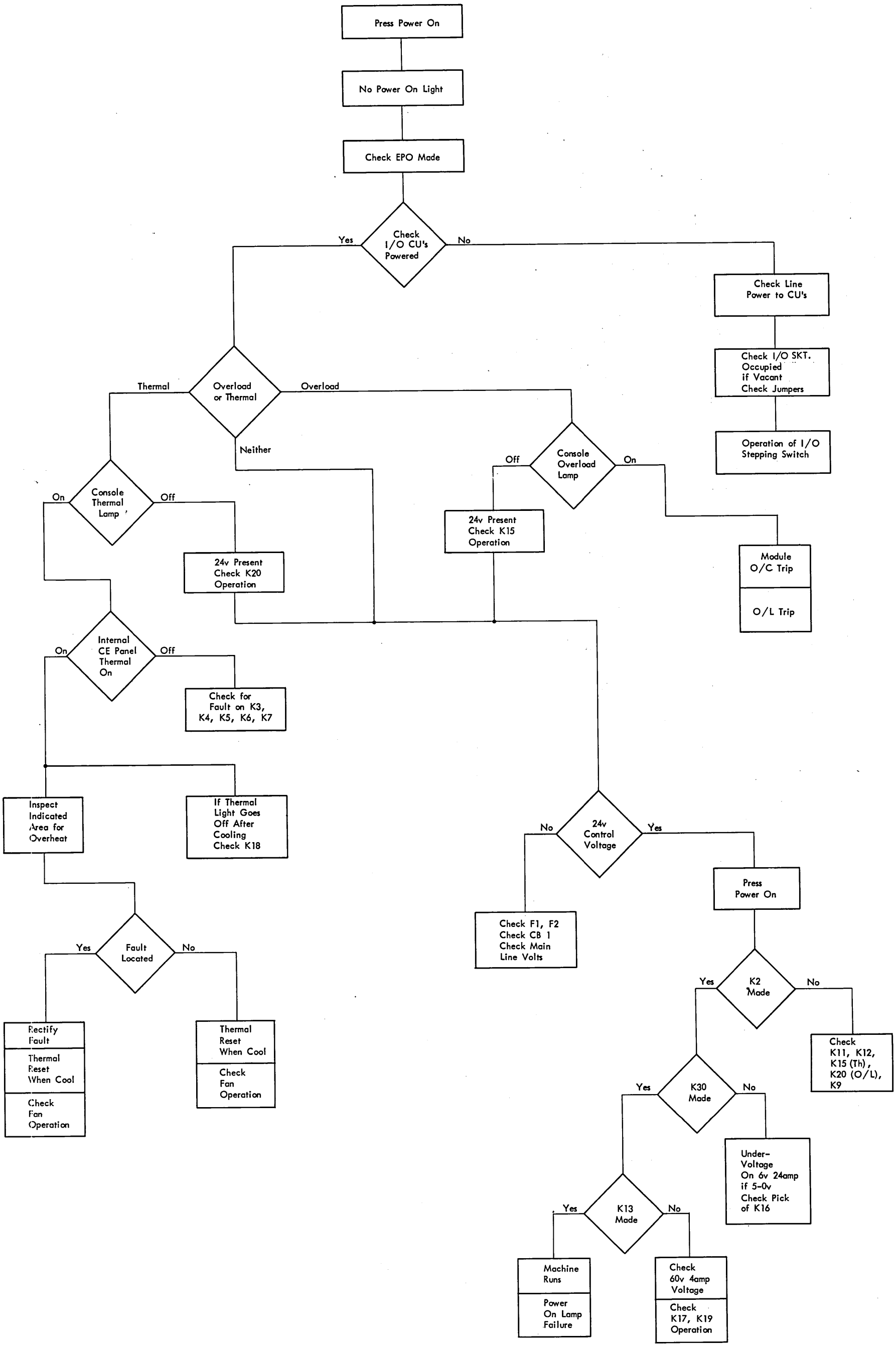
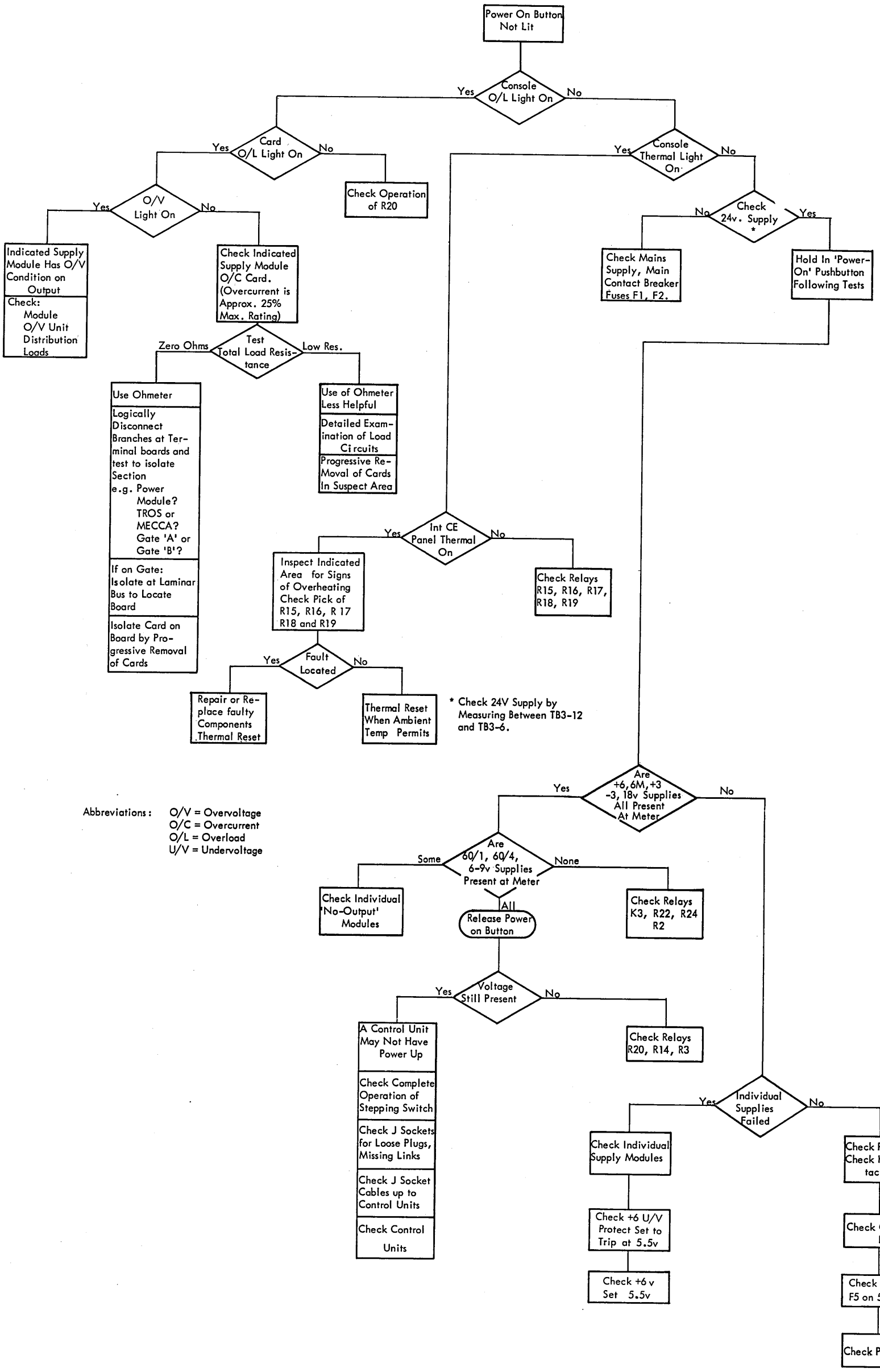


FIGURE 917. MID-PAC POWER SUPPLY



Abbreviations: O/V = Overvoltage
O/C = Overcurrent
O/L = Overload
U/V = Undervoltage

FIGURE 918. 2.5 KC HF POWER SUPPLY

CONTROL FIELD CHARTS

5420053

FIG 964

ROS CONTROL FIELD CHARTS

(FOR USE WITH THE FORTY STANDARD SYMBOLIC LANGUAGE: FOSSL)

MASTER

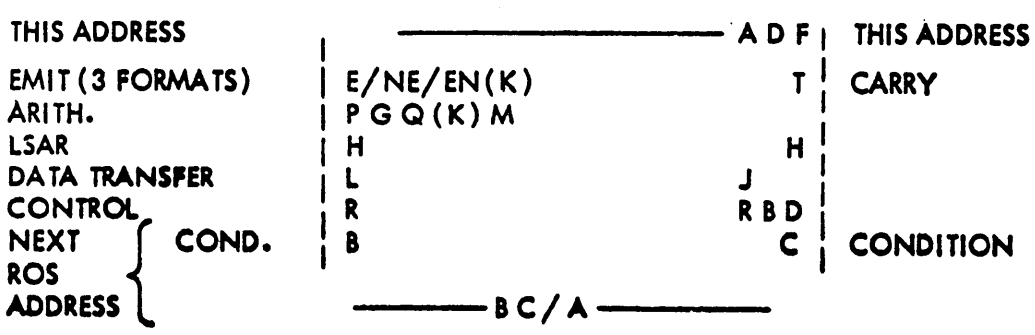
CAS TO ALD LINK

ALL FOSSL MICRO-ORDERS ARE LISTED WITH SIGNAL NAME AND ALD SHEET NUMBER IN THE CE ROS FIELD CHARTS, CLASSIFIED BY FIELD. TO AVOID SEARCHING THROUGH THE COMPLETE LIST FOR AN UNFAMILIAR MICRO-ORDER AND HARDWARE REFERENCE A LINKING DIAGRAM IS GIVEN BELOW.

THE LINK BOX CORRESPONDS LINE FOR LINE WITH CAS BOXES BUT INDICATES THE ROS FIELD PRODUCING EACH CAS STATEMENT AND IN MOST CASES THE ORDER IN WHICH THEY APPEAR.

THUS IF AN ARITHMETIC FUNCTION IS SUSPECTED, THE LINK BOX IN THE CORRESPONDING LINE SHOWS G IN THE ARITHMETIC FUNCTION POSITION PERMITTING IMMEDIATE REFERENCE TO CG FIELD IN THE ROS CONTROL FIELD CHART WHICH GIVES AN ALD SHEET, SIGNAL NAME, CONDITIONS AND OTHER HARDWARE REFERENCES.

LOCATION OF ROS FIELDS CAUSING CAS STATEMENTS



LETTERS IN THE BOX ARE ROS FIELDS

EDGE CHARACTERS ARE OMITTED FOR CLARITY

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420053
NAME	FIGURE 964					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291		
CAS TO ALD LINK (FOSSL)												
DESIGN	GDL	7OCT65	MODEL									
DETAIL												
CHECK	NCD	11OCT65	DRAW	GT	21SEP65						FIG 964	
APPRO	WRR	11OCT65	CHECK									

MASTER

CA FIELD — ROS BITS 0 - 3

PART OF NEXT ROS WORD ADDRESS UNDER CB AND CD FIELD CONTROL
(ROS ADDRESS IS SHOWN UNDER CD FIELD)

SENSE LATCHES EB181
A - FIELD ENTRY RX051

EDGE CHAR.	MICRO - ORDER	BITS	DEC. ORDER	FUNCTION	ALD
NOT APPLICABLE		XXXX		CA ROAR PSN 5 - 2 WHEN CB = 0 - 13 AND CD = NOT 2	RX091
				CA ROAR PSN 9 - 6 WHEN CB = 0 - 13 AND CD = 2, OR CB = 15	RX011
				CA NOT USED WHEN CB = 14	-

CB FIELD — ROS BITS 4 - 7

FORMS PSN1 OF NEXT ROS ADDRESS BY TESTING SPECIFIED CONDITIONS WITH CD = 0 OR 2 IN CPU OR I-O STATE. (ROS ADDRESS IS SHOWN UNDER CD FIELD). ISSUE SPECIAL CONTROLS WHEN CD = 1 OR 3

CPU STATE, CD FIELD = 0 OR 2

EDGE CHAR.	MICRO - ORDER	BITS	DEC. ORDER	FUNCTION - BRANCH CONDITION	ALD	
R	0	0000	CB0	NO OUTPUT (ROAR PSN 1 IS RESET TO 0)	DR751	
R	1	0001	CB1	SET PSN1 OF ROAR TO 1	DR751	
R	YCD	0010	CB2	DIRECT CARRY	RX111	
R	L2≠0	0011	CB3	LSAR PSN6 OR 7 NON ZERO (TEST AT T2 DEL. SAME CYCLE)	DR751	
R	ALU≠0	0100	CB4	ALU OUTPUT NON ZERO (TEST AT T2 DEL. SAME CYCLE)	RX111	
R	Y0	0101	CB5	STORAGE PROTECT PRIMER STAT = 1	DR751	
R	Y2	0110	CB6	CONDITION REGISTER PSN0 = 1	DR751	
R	Y4	0111	CB7	GENERAL - PURPOSE STAT Y4 = 1 (NOT REINT OR ROSCAR IN CONTROL)	DR751	
R	YCH3			(REINT OR ROSCAR IN CONTROL) CHANNEL GENERAL STAT YCH3	GE571	HE571
R	Y6	1000	CB8	GENERAL - PURPOSE STAT Y6 = 1 (NOT REINT OR ROSCAR IN CONTROL)	DR751	
R	S1 (7)			(REINT OR ROSCAR IN CONTROL) BIT 7 OF S - REGISTER	GE571	HE571
R	FXPTO	1001	CB9	FIXED POINT OVERFLOW (TEST AT T2 DEL. SAME CYCLE)	RX111	
R	ALU7	1010	CB10	ALU OUTPUT PSN7 = 1 (TEST AT T2 DEL. SAME CYCLE)	DR751	
R	IZT	1011	CB11	INTEGRATING ZERO TEST	DR751	
R	CBY			(REINT OR ROSCAR IN CONTROL) CHAINING BOUNDARY IN BUFFER (OUTPUT OPS)	GE571	HE571
R	IDQ	1100	CB12	INVALID DECIMAL DIGIT ON ALU ENTRY Q	DR751	
R	ASCII	1101	CB13	ASCII STAT	DR751	
R	MINUS	1110	CB14	Q BUS PSN4 - 7 = 11 OR 13	DR751	
R	PNB	1111	CB15	SPECIAL CONTROL FOR FUNCTION BRANCH (SEE CD FIELD)	RX011	

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 965					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CA, CB (FOSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	QT	21SEP65						FIG 965
APPRO	WRR	11OCT65	CHECK								

542005+

CB FIELD — 1-0 STATE, CD FIELD = 0 OR 2

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-BRANCH CONDITION	ALD	
R	0	0000	CB0	NO OUTPUT (ROAR PSN 1 IS RESET TO 0)	DR571	
R	1	0001	CB1	SET PSN 1 OF ROAR TO 1	DR571	
R	YCD	0010	CB2	DIRECT CARRY	RX111	
R	ADR-1	0011	CB3	ADDRESS IN LATCH GATED BY Y2, Y3	FL001	
R	ALU ≠ 0	0100	CB4	ALU OUTPUT NON ZERO (TEST AT T2 DEL. SAME CYCLE)	RX111	
R	BU < 2	0101	CB5	SEL, CHAN-LESS THAN 2 BYTES		
R	HALT	0110	CB6	MANUAL STOP LATCH	FL001	
R	Y4	0111	CB7	(NOT REINT OR ROSCAR IN CONTROL) GEN. STAT Y4 = 1	DR571	
R	YCH3			(REINT OR ROSCAR IN CONTROL) CHANNEL GEN. STAT Y3 = 1	GE571	HE571
R	Y6	1000	CB8	(NOT REINT OR ROSCAR IN CONTROL) GEN. STAT Y6 = 1	DR751	
R	S1 (7)			(REINT OR ROSCAR IN CONTROL) LS BIT OF S REGISTER	GE571	HE571
R	LOAD	1001	CB9	LOAD BUTTON (CONSOLE)	FL001	
R	ALU7	1010	CB10	ALU OUTPUT BIT 7 (TEST AT T2 DEL. SAME CYCLE)	DR751	
R	SVC-1	1011	CB11	(NOT REINT OR ROSCAR IN CONTROL) SERVICE IN AND NOT COMMAND OUT OR SERVICE OUT)	FL001	
R	CBY			(REINT OR ROSCAR IN CONTROL) CHAINING BOUNDARY IN BUFFER (OUTPUT OPS)	GE571	HE571
R	SOOCO	1100	CB12	SERVICE OUT OR COMMAND OUT	FL001	
		1101	CB13	NOT USED (CPU ONLY)		
		1110	CB14	NOT USED (CPU ONLY)		
R	FNB	1111	CB15	SPECIAL CONTROL FOR FUNCTION BRANCH	RX011	

CB FIELD — CD = 1

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-BRANCH CONDITION	ALD		
					MPX	SC1	SC2
R	ADR-O	0000	CB0	SET ADDRESS OUT	FB001	GG511	HG511
R	CMD-O	0001	CB1	SET COMMAND OUT	FB001	GG523	HG523
R	SVC-O	0010	CB2	SET SERVICE OUT	FB011	GG524	HG524
R	SEL	0011	CB3	SET SELECT LOGIC TO STOP INTERFACE SEQUENCE	FB031	GG511	
R	ISO	0100	CB4	INHIBIT SELECT OUT	FB031	GG512	HG512
R	1 → IR	0101	CB5	SET INTERRUPT REQUEST	FB021	GF503	HF503
R	0 → IR	0110	CB6	RESET INTERRUPT REQUEST	FB021	GF503	HF503
R	CL - CH	0111	CB7	CLEAR CHANNEL	FK051	GE571	HE571
R	⌐ OP - O	1000	CB8	RESET OPERATIONAL OUT	FB021	GG513	HG513
R		1001	CB9	UNUSED	-	-	-
R	ICC	1010	CB10	SET INTERFACE CONTROL CHECK; FORCE ERROR STAT Y12 AND FORCE LOG-OUT	KC081	GG543	HG543
R	REINT	1011	CB11	REINTERPRET CONDITIONS AS SHOWN IN CB, CC, CL AND CM FIELDS. REMAINS EFFECTIVE UNTIL RESTORE (REST)IS CALLED		GE571	HE571
R	DUMP	1100	CB12	TURN ON DUMP CONTROL WHEN STAT Y10 = 1	FJ021	-	-
R	HIO	1101	CB13	HALT DEVICE ON INTERFACE	FB021	GG531	HG531
		1110	CB14	UNUSED	-	-	-
R	FNB	1111	CB15	SPECIAL CONTROL FOR FUNCTION BRANCH	RX011	RX011	RX011

THE B CONDITION IS SET TO ZERO WHENEVER CB = 0-14 AND CD = 1 OR 3 (EXCEPT UNDUMP)

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 966					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CB (FOSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	GT	20SEP65						
APPRO	WRR	11OCT65	CHECK								FIG 966

5420055

CB FIELD:

CD = 3, CPU AND MPX AND SC

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-SPECIAL CONTROLS	ALD CPU/MPX	ALD SC1	ALD SC2
R	STAN	0000	CB0	SC CHANNEL ANALYSE STATUS, FORCE 4-WAY BRANCH ON RESULT		GE591	HE59
R	DC-IN	0001	CB1	TIMING LINE IN FOR DIRECT DATA ACCEPT	JA114		
R	LOG	0010	CB2	START LOG-OUT	KC081		
R	SSM	0011	CB3	SET EXTERNAL MASK WITH ALU BIT 7 WITH BIT 1 FOR CHANNEL 1 AND BIT 2 FOR CHANNEL 2	KM131	GE591	HE591
R	SWEA	0100	CB4	SET ASCII, WAIT AND ENABLE WITH ALU BITS 4, 5 AND 6	KH171		
R	STPC1	0101	CB5	STOP T CLOCK	KC081		
R	MANUAL	0110	CB6	DEFINE NORMAL STOP LOOP	KH161		
R	0→SL0	0111	CB7	RESET SELECT OUT GATED BY Y2, Y3		GG511	HG511
R	EDIT	1000	CB8	IF Q BUS = 001000XY SET NEXT ROS ADDRESS BIT 1 AND 0 TO XY	RX112		
				IF Q BUS ≠ 001000XY SET NEXT ROS ADDRESS BIT 1 AND 0 TO 11	RX112		
R	SMSC	1001	CB9	SET 1401 EMULATOR SELECTOR CHANNEL LATCH (Y2, Y3 GATED)	RX003		
R	DAT	1010	CB10	ENABLE/DISABLE DEC. ADDRESS TRANSLATOR (1401 EMULATOR)	RX003		
R		1011	CB11	UNUSED	-		
R		1100	CB12	UNUSED	-		
R	SUP-O	1101	CB13	SET SUPPRESS OUT GATED BY Y2, Y3		GG512	HG512
R	UNDUMP	1110	CB14	RESTORE ROAR FOR NEXT CYCLE	RX011		
R	FNB	1111	CB15	FUNCTION BRANCH	RX011		

THE B CONDITION IS SET TO ZERO WHENEVER CB = 0-14 AND CD = 1 OR 3 (EXCEPT UNDUMP)

CC FIELD

ROS BITS 0-11

CPU STATE

SENSE LATCHES EB201
DECODER DR111
DECODER CHECK DS011

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-CONDITION ANDED WITH CPU/I-O STATES TO FORM ROS NEXT ADDRESS BIT 0	ALD	
R	0	0000	CC0	NO OUTPUT (ROAR PSN0 IS RESET TO ZERO		
R	1	0001	CC1	SET PSN0 OF ROAR TO 1	DR752	
R	YCD	0010	CC2	DIRECT CARRY	DR752	
R	L4≠	0011	CC3	LSAR PSN4, 5, 6 OR 7 NON-ZERO (TEST AT T2 DEL. SAME CYCLE)	DR752	
R	ALU≠0	0100	CC4	ALU OUTPUT NON ZERO (TEST AT T2 DEL. SAME CYCLE)	RX113	
R	Y1	0101	CC5	MPX STORE ADDRESS STAT Y1 =1	DR752	
R	Y3	0110	CC6	CONDITION REGISTER PSN 1 =1	DR752	
R	Y5	0111	CC7	GENERAL - PURPOSE STAT Y5 = 1	DR752	
R	YCH1			(REINTERPRET OR ROSCAR IN CONTROL) GENERAL - PURPOSE CHANNEL STAT YCH1	GE571	HE571
R	Y7	1000	CC8	GENERAL - PURPOSE STAT Y7 = 1	DR752	
R	CH = WR			(REINTERPRET OR ROSCAR IN CONTROL) CHANNEL COMMAND WRITE CHANNEL READ/WRITE STAT = 1	GE571	HE571
R	ALU6	1001	CC9	ALU OUTPUT PSN6 = 1 (TEST AT T2 DEL. SAME CYCLE)	RX111	
R	ALU0	1010	CC10	ALU OUTPUT PSN0 = 1 (TEST AT T2 DEL. SAME CYCLE)	RX111	
R	CDA			(REINTERPRET OR ROSCAR IN CONTROL) DATA CHAINING INDICATOR	GE571	HE571
R	Q0≠0	1011	CC11	Q BUS PSN0-3 NON ZERO (TEST AT T2 DEL. SAME CYCLE)	DR752	
R	PRI	1100	CC12	PROGRAM INTERRUPT	DR752	
R	YCI	1101	CC13	INDIRECT CARRY	RX111	
R	SAT	1110	CC14	INVALID STORAGE (MEMORY) ADDRESS (IMA) OR PROTECTED STORAGE (MEMORY) VIOLATION (PMA, YM)	DR752	
R	QPTY	1111	CC15	TEST Q BUS FOR BAD PARITY (TEST AT T2 DEL. SAME CYCLE)	DR752	

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 967					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CB, CC (FOSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	GT	20SEP65						FIG 967
APPRO	WRR	11OCT65	CHECK								

5420056

5420057

FIG 968

MASTER

CC FIELD — I-O STATE

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-CONDITION ANDED WITH CPU/I-O STATES TO FORM ROS NEXT ADDRESS BIT 0	ALD MPX	ALD SC1	ALD SC2
R	0	0000	CC0	NO OUTPUT (ROAR PSN0 IS RESET TO ZERO	-	-	-
R	1	0001	CC1	SET PSN0 OF ROAR TO 1	DR752	DR752	DR752
R	YCD	0010	CC2	DIRECT CARRY	DR752	DR752	DR752
R	IR	0011	CC3	TEST INTERRUPT REQUEST LATCH (GATED BY Y2, Y3)	FL011	GE571	GE571
R	ALU ≠ 0	0100	CC4	ALU OUTPUT NON ZERO (TEST AT T2 DEL. SAME CYCLE)	RX113	RX113	RX113
R	DU/IF	0101	CC5	UNIT UNOBTAINABLE OR I - F FREE (GATED BY Y2, Y3)	FL011	GE571	HE571
R	MSC	0110	CC6	IS 1401 EMULATOR LATCH = 1			
R	Y5	0111	CC7	GENERAL - PURPOSE STAT Y5 = 1 (NOT REINT OR ROSCAR IN CONTROL)	DR572		
R	YCH1			SELECTOR CHANNEL GENERAL - PURPOSE STAT Y1 (REINT CALLED OR ROSCAR IN CONTROL)		GE571	HE571
R	Y7	1000	CC8	GENERAL - PURPOSE STAT Y7 = 1 (NOT REINT OR ROSCAR IN CONTROL)	DR752		
R	CH = WR			SELECTOR CHANNEL READ-WRITE STAT; WRITE = 1 (REINT CALLED OR ROSCAR IN CONTROL)		GE571	HE571
R	HLD ≠ 1	1001	CC9	SET DIRECT CONTROL ACCEPT REGISTER ON ABSENCE OF HOLD LINE	FL011		
R	CDA	1010	CC10	SELECTOR CHANNEL DATA CHAINING INDICATOR (CDA FLAG AND CNT. = 0 AND NOT CHAINING BOUNDARY)		GE571	HE571
R	STA-I	1011	CC11	STATUS IN GATED BY Y2, Y3	FL011		
		1100	CC12	NOT USED (CPU STATE ONLY)			
R	BU < I	1101	CC13	SELECTOR CHANNEL BUFFER EMPTY (GATED BY Y2, Y3)		GE531	HG531
R	SAT	1110	CC14	INVALID STORAGE ADDRESS (IMA) OR PROTECTED STORAGE VIOLATION (PMA, YM)	DR752		
R	OP - I	1111	CC15	(MX) OPERATIONAL IN AND NO (STATUS IN OR ADDRESS IN) GATED BY Y2, Y3	FL011		

CD FIELD — ROS BITS 12,13

ROS ADDRESS CONTROL, CB FIELD INTERPRETATION

SENSE LATCHES EB211
CTRL LATCH & DEC DR131
DECODER CHECK DS011

CONDITIONS	SOURCE OF ROS ADDRESS BITS 11	10	9	8	7	6	5	4	3	2	1	0
CD = XX CB = 15	D0	D1	A0	A1	A2	A3	0	Q0	Q1	Q2	Q3	
CD = 0 AND CB = 0-14	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	B COND	C COND
CD = 2 AND CB = 0-14	X0	X1	A0	A1	A2	A3	X6	X7	X8	X9	B COND	C COND
CD = 1 AND CB = 0-14	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	0	C COND
CD = 3 AND CB = 0-13	X0	X1	X2	X3	X4	X5	A0	A1	A2	A3	0	C COND
CD = 3 AND CB = 14	UNDUMP (RESTORE INTERRUPTED CPU ROS ADDRESS INTO ROAR)											

X BITS ARE UNCHANGED FROM LAST ROS ADDRESS
D BITS ARE FROM ROS CD FIELD
A BITS ARE FROM ROS CA FIELD
Q BITS ARE FROM Q BUS

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 968				20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CC, CD (FOSSL)									
DESIGN	GDL	7OCT65	MODEL							
DETAIL										
CHECK	NCD	11OCT65	DRAW	GT	20SEP65					
APPRO	WRR	11OCT65	CHECK							FIG 968

5420057

5420058

FIG969

MASTER

CE FIELD ROS BITS 14-17 EMIT FIELD

SENSE LATCHES EB211
CONTROL LATCH DR171

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-PROVIDE 4 BIT BINARY PATTERNS FOR CONTROL	ALD
E	0000	0000	CE0		
E	0001	0001	CE1	1. DATA SOURCE FOR LOCAL STORAGE ADDRESS FORMATION CONTROLLED BY CH FIELD	RLXXX
E	0010	0010	CE2		
E	0011	0011	CE3		
E	0100	0100	CE4	2. DATA SOURCE FOR SET OR RESET OF STATS CONTROLLED BY CN FIELD, SC ONLY:-BIT 2 SETS BUT CANNOT RESET PROGRAM CHECK	RYXXX
E	0101	0101	CE5		
E	0110	0110	CE6		
E	0111	0111	CE7		
E	1000	1000	CE8	3. DATA SOURCE FOR SETTING THE ALU FUNCTION REGISTER CONTROLLED BY CN = 15	RPXXX
E	1001	1001	CE9		
E	1010	1010	CE10		
E	1011	1011	CE11	4. DATA SOURCE FOR ALU P OR Q INPUTS CONTROLLED BY CP OR CQ FIELD	RPXXX RQXXX
E	1100	1100	CE12		
E	1101	1101	CE13		
E	1110	1110	CE14		
E	1111	1111	CE15		

CF FIELD ROS BIT 18

SENSE LATCH EB221
F FIELD ENTRY RX001

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-ROS WORD ADDRESS PARITY BIT (CURRENT)	ALD
		0	-	ODD PARITY COMPARED WITH ROAR PARITY (ROS ADDRESS CK) ≠	RX001
		1	-	EVEN PARITY COMPARED WITH ROAR PARITY (ROS ADDRESS CK) ≠	RX001

≠ CHECKS IF CORRECT WORD HAS BEEN READ OUT

CG FIELD ROS BITS 19-20

SENSE LATCHES EB221
G-FIELD ENTRY KP021

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-ALU FUNCTION CONTROL	ALD
A	?	00	CG0	INDIRECT FUNCTION IF Y8 = 0 AND NOT REINT OR ROSCAR IN CONTROL FUNCTION REGISTER F SET TO EMIT VALUE SEE FIELDS CN,CE	KP021 KP023
A	Q			DIRECT 'OR' FUNCTION IF Y8 = 1 OR REINT CALLED OR ROSCAR IN CONTROL. F REGISTER = 0000	
A	•	01	CG1	DIRECT LOGIC FUNCTION 'AND' P AND Q F REGISTER = 0101	KP023/32
A	-	10	CG2	DIRECT ARITHMETIC FUNCTION 'MINS', P-Q F REGISTER = 0011	KP023/32
A	+	11	CG3	DIRECT ARITHMETIC FUNCTION 'PLUS', P+Q F REGISTER = 1111	KP023/32

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 969					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CE, CF, CG (FOSSL)										
DESIGN	GDL	70CT65	MODEL								
DETAIL											
CHECK	NCO	110CT65	DRAW	GT	20SEP65						FIG969
APPRO	WRR	110CT65	CHECK								

5420058

5420059

FIG 970

MASTER

CH FIELD ROS BITS 21-25 CPU,MX,SC

SENSE LATCHES EC031
DECODER DS021
DECODER CHECK DS081

LEFT EDGE CHAR	MICRO-ORDER LEFT	MICRO-ORDER RIGHT	RIGHT EDGE CHAR	BITS	DEC ORDER	FUNCTION-LOCAL STORAGE ADDRESS CONTROL	ALD
L	BE→L			00000	CH0	LOAD LSAR FROM SOURCE BE AND USE	DS0XX
L				00001	CH1	NOT USED	-
L	H→L	L→H		00010	CH2	USE H-REGISTER	DS0XX
L				00011	CH3	NOT USED	-
L	AE→L	L→J		00100	CH4	LOAD LSAR FROM SOURCE AE,USE,LOAD J-REGISTER	DS0XX
L	BE→L	L→J		00101	CH5	LOAD LSAR FROM SOURCE BE,USE,LOAD J-REGISTER	DS0XX
L	QE→L	L→J		00110	CH6	LOAD LSAR FROM SOURCE QE,USE,LOAD J-REGISTER	DS0XX
L	J→L	L→J		00111	CH7	USE J-REGISTER	DS0XX
						DECREMENT=1	
L	BE→L	INT	C	01000	CH8	SELECTOR CHANNEL ONLY. ALLOW OTHER CHANNEL TO BREAK IN	HB506
L				01001	CH9	NOT USED	-
L	H→L	L-1→H		01010	CH10	USE H-REGISTER AND DECREMENT BY 1	DS0XX, CC001
L				01011	CH11	NOT USED	-
L	AE→L	L-1→J		01100	CH12	LOAD LSAR AS FOR AE,USE,DECREMENT BY 1, LOAD J	DS0XX, CC001
L	BE→L	L-1→J		01101	CH13	LOAD LSAR AS FOR BE,USE,DECREMENT BY 1, LOAD J	DS0XX, CC001
L	QE→L	L-1→J		01110	CH14	LOAD LSAR AS FOR QE,USE,DECREMENT BY 1, LOAD J	DS0XX, CC001
L	J→L	L-1→J		01111	CH15	USE J-REGISTER AND DECREMENT BY 1	DS0XX,CC001
						INCREMENT=1	
L	BE→L	REST	C	10000	CH16	SELECTOR CHANNEL ONLY. IF ROSCAR IN CONTROL,RESTORE CONTROL TO ROAR. IF ROAR IN CONTROL RESET THE REINTERPRET CONTROL.	GG512
L				10001	CH17	NOT USED	-
L	H→L	L+1→H		10010	CH18	USE H-REGISTER AND INCREMENT BY 1	DS0XX, CC001
L				10011	CH19	NOT USED	-
L	AE→L	L+1→J		10100	CH20	LOAD LSAR AS FOR AE,USE, INCREMENT BY 1,LOAD J	DS0XX, CC001
L	BE→L	L+1→J		10101	CH21	LOAD LSAR AS FOR BE,USE, INCREMENT BY 1,LOAD J	DS0XX, CC001
L	QE→L	L+1→J		10110	CH22	LOAD LSAR AS FOR QE,USE, INCREMENT BY 1,LOAD J	DS0XX, CC001
L	J→L	L+1→J		10111	CH23	USE J-REGISTER,AND INCREMENT BY 1	DS0XX, CC001
						INCREMENT=0	
L	JE→L	L→J		11000	CH24	LOAD LSAR FROM SOURCE JE,USE,LOAD J-REGISTER	DS0XX
L	JE→L			11001	CH25	LOAD LSAR FROM SOURCE JE, AND USE	DS0XX
L	AE→L			11010	CH26	LOAD LSAR FROM SOURCE AE,AND USE	DS0XX
L				11011	CH27	NOT USED	-
L	AE→L	L→H		11100	CH28	LOAD LSAR FROM SOURCE AE,USE,LOAD H-REGISTER	DS0XX
L	BE→L	L→H		11101	CH29	LOAD LSAR FROM SOURCE BE,USE,LOAD H-REGISTER	DS0XX
L	QE→L	L→H		11110	CH30	LOAD LSAR FROM SOURCE QE,USE,LOAD H-REGISTER	DS0XX
						INCREMENT=2	
L	J→L	L-2→J		11111	CH31	USE J-REGISTER,AND DECREMENT BY 2	CC001, DS071

LSAR LOAD DEFINITIONS E = EMIT FIELD, J = J-REGISTER, Q = Q BUS

LSAR PSN SOURCE	0	1	2	3	4	5	6	7	COMMENT
QE	E0	E1	E2	Q0	Q1	Q2	Q3	E3	Q BUS LOAD FOR FNB
AE	0	1	0	0	E0	E1	E2	E3	
BE	0	0	0	0	E0	E1	E2	E3	CPU STATE
BE	0	0	1	0	E0	E1	E2	E3	I-O STATE MPX OR SC1
BE	0	0	1	1	E0	E1	E2	E3	I-O STATE SC2
JE	J0	J1	J2	J3	J4	J5	E2	E3	J-REGISTER MODIFICATION

NOTES
ADDRESS XX01XXXX IS INVALID
10XXXXXX AND 11XXXXXX ARE EQUIVALENT
ON 'INCREMENT' A CARRY IS NOT PROPAGATED FROM BIT POSITION 4 TO BIT POSITION 2

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 970 FIELD CH (FOSSL)			20OCT65	253356			X PRINT TO ENG. SPEC. NO. 893291	
DESIGN	GDL	7OCT65	MODEL						
DETAIL									
CHECK	NCD	11OCT65	DRAW	GT 20SEP65					FIG 970
APPRO	WRR	11OCT65	CHECK						5420059

CJ FIELD — ROS BITS 26-28 — Y10 = 0 — JX = 0 (ROS BIT 54)

SENSE LATCHES E8241
DECODER DR275
DECODER CHECK DR282

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-R BUS INPUT CONTROL	ALD	
D	Z	000	CJ0	ZEROS WITH GOOD PARITY	-	
D	A	001	CJ1	A REGISTER. STORAGE ADDRESS	DR281	
D	B	010	CJ2	R REGISTER. BYTES B0, B1 WITH GOOD PARITY TO RX	DR281	
D	C	011	CJ3	C REGISTER. BYTES CX, C0, C1	DR281	
D	D	100	CJ4	STORAGE DATA REGISTER D, BYTES D0, D1 WITH GOOD PARITY TO RX	DR281	
D	HJ	101	CJ5	LOCAL STORE ADDRESS REGISTERS, H TO R0, J TO R1 GOOD PARITY TO RX	DR281	
D	LSTOR	110	CJ6	LOCAL STORE OUTPUT (SEE CL FIELD)	KM001	
D	CIB	111	CJ7	(MPX) CHANNEL INPUT BUS Y2, Y3 =00	DR275	DR278
				(SC1) STATUS TO R0 AND CHECKS TO R1, Y2, Y3 = 01	GE512	
				(SC2) STATUS TO R0 AND CHECKS TO R1, Y2, Y3 = 10	HE512	
				TIMER VALUE TO R0, R1 (CLOCK RESET TO ZERO WHEN SAMPLED)		

CJ FIELD — Y10 = 0 — JX = 1 (ROS BIT 54) — REINTERPRET

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-R BUS INPUT CONTROL	ALD
D	CST	000	CJ0	CHANNEL FLAG REGISTER TO R0. CHAINING BOUNDARY FLAGS TO R1 (0, 4). COUNT CONTROL TO R1 (5, 7)	GE511
D	S	001	CJ1	CHANNEL S REGISTER (BYTE ADDRESS)	GE511
D	T	010	CJ2	CHANNEL T REGISTER (BYTE COUNT)	GE511
D	W01	011	CJ3	BUFFER BYTES 0, 1 TO R0, R1 (RD/BK LATCH = 0) BUFFER BYTES 0, 1 TO R1, R0 (RD/BK LATCH = 1)	GE511
D	W2	100	CJ4	BUFFER BYTE W2 TO R0. CHANNEL STORE PROTECT KEY R1 (4, 7) BITS 0 TO 3 MUST = 0	GE511
D	W34	101	CJ5	BUFFER BYTES 3,4 TO R0, R1	GE511
D		110	CJ6	NOT USED	-
D		111	CJ7	NOT USED	-

CJ FIELD — Y10 = 1 JX = 0 (MANUAL STATE)

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-R BUS INPUT CONTROL	ALD
D		000	CJ0	NO OPERATION	
D	BAS	001	CJ1	MANUAL BINARY ADDRESS SWITCHES	DR282
D	LAS	010	CJ2	A. LOAD UNIT ADDRESS SWITCHES 1. UNIT ADDRESS 8 BITS-R1 2. CHANNEL SELECT BITS R0 POSITIONS 5, 6, 7	DR282
				B. STORAGE SELECT ROTARY SWITCH THIS SWITCH ENCODED TO GIVE A THREE-BIT FIELD INSERTED INTO R0 POSITIONS 1, 2, 3 DEFINED AS FOLLOWS: 000 = STOR PROTECT 0 001 = IC-INSTRUCTION COUNTER 100 = MS-MAIN STORAGE 011 = FP-FLOATING POINT REGISTERS 010 = GP-GENERAL PURPOSE REGISTERS 101 = PSW-PROGRAM STATUS WORD	
D	BDS	011	CJ3	MANUAL BINARY DATA SWITCHES	DR281
D	CIT	100	CJ4	CHANNEL INPUT INTERFACE TAGS SELECTED BY Y2, Y3	GE512
		101	CJ5	NOT USED	
D	LSTOR	110	CJ6	LOCAL STORE OUTPUT (SEE CL FIELD)	KM001
		111	CJ7	NOT USED	-

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 971					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CJ (FOSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	GT	20SEP65						FIG 971
APPRO	WRR	11OCT65	CHECK								

5420060

5420061

FIG972

MASTER

CK FIELD ROS BIT 29

SENSE LATCH EB251
F-REGISTER KP001

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-SKEW CONTROL	ALD
A		0	CK0	NO SKEW	AQ001
A	*	1	CK1	SKEW (SEE NOTE)	AQ001
				NOTE. CAUSES THE ALU OPERATION TO INCORPORATE A 4 BIT SHIFT ON THE Q BUS Q BUS POSITIONS 0-3 ARE SHIFTED INTO SKEW BUFFER Q BUS POSITIONS 4-7 ARE SHIFTED INTO ALU INPUT POSITIONS 0-3 OLD CONTENTS OF SKEW BUFFER ARE USED FOR ALU INPUT POSITIONS 4-7 WHEN 'LOAD F' OCCURS, CK IS LOADED INTO F4.	KP001

NOTE: THE ASTERISK CALLING FOR A SKEW OPERATION CAN APPEAR EITHER IN AN ARITHMETIC STATEMENT (EDGE CHAR. A) OR IN AN EMIT STATEMENT (EDGE CHAR. E) FOR A LOAD F MICRO-ORDER (SEE CN FIELD)

CL FIELD ROS BITS 30-32

CONTROL LATCH AND DEC. DR32X

EDGE CHAR	MICRO-ORDER	BITS	DEC. ORDER	FUNCTION-R BUS OUTPUT CONTROL	ALD
D	Z	000	CL0	NO DESTINATION, PARITY IGNORED	(KH025)
D	LSTOR	001	CL1	LOCAL STORE INPUT (CALL WRITE LIMITED TO 100 MICROSECONDS CONTINUOUS)	(KM001)
D	S	010	CL2	SELECTOR CHANNEL S REGISTER	(HE521)
D	HJ	011	CL3	R0 TO H, R1 TO J (NOT REINT CALLED OR ROSCAR IN CONTROL)	(RJ0XX)
D	W34			SELECTOR CHANNEL BUFFERS 3 AND 4 (IF REINT CALLED OR ROSCAR IN CONTROL)	(HE521)
D					
D	A	100	CL4	TO REGISTER A	(RAXXX)
D	B	101	CL5	TO REGISTER B	(RBXXX)
D	C	110	CL6	TO REGISTER C	(RCXXX)
D	D	111	CL7	TO REGISTER D	(RDXXX)
				IF CM AND CL BOTH CALL FOR A TRANSFER, THE ALU BIT TRANSFER OVER-RIDES THE BYTE THAT IT CONCERNS IN THE A, B, C & D REGISTERS ONLY, BUT THE OTHER BYTE OR BYTES OF THE R BUS TRANSFER TAKE PLACE NORMALLY. THE CL TRANSFER TO D OVER-RIDES THE MAIN STORAGE INPUT TO D IF BOTH OCCUR IN 'READ' CYCLE 2. IF MA OR PMA AND YM OCCURS M-D TAKES PRIORITY.	

THE CASES ARE:

ALU → D R → D M → D	ALU → D R → D (ONE BYTE OVER-WRITTEN BY ALU) M LOST	R → D M → D	VALID WITH R → D M LOST	ALU → D M → D NOT PERMITTED

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420061
NAME	FIGURE 972					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291		
	FIELD CK, CL (FOSSIL)											
DESIGN	GDL	7OCT65	MODEL									
DETAIL												
CHECK	NCD	11OCT65	DRAW	QT	20SEP65						FIG972	
APPRO	WRR	11OCT65	CHECK									

5420062

MASTER

FIG 973

CM FIELD ROS BITS 33-36 CPU, MX AND SC

SENSE LATCH EB261, EB271
CONTROL LATCH DR36X, KU081
AND DECODER

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-ALU OUTPUT CONTROL	ALD	
A	Z	0000	CM0	RESULT HAS NO DESTINATION	..	
A	AX	0001	CM1	OR OF ALU0-ALU6 TO AX6; ALU7 TO AX7; EX IS LOST	RA302	
A	A0	0010	CM2	ALU OUTPUT TO A0; EX TO AX	RA071	
A	A1	0011	CM3	ALU TO A1; EX IS LOST	RA171	
A	DATA	0100	CM4	ALU TO DIRECT DATA OUT; EX IS LOST	JA005	
A	CFL	0100	CM5	(REINT OR ROSCAR IN CONTROL) ALU TO CHANNEL FLAGS; EX IS LOST NOT USED (UNLESS REINT CALLED OR ROSCAR IN CONTROL)	GE541 -	HE541
A	W4			(REINT OR ROSCAR IN CONTROL) ALU TO BUFFER W4; EX IS LOST	GE541	HE541
A	B0	0110	CM6	ALU TO B0; EX IS LOST (REINT OR ROSCAR IN CONTROL) ALU TO T0; EX IS LOST	RB071 GE541	HE541
A	B1	0111	CM7	ALU TO B1; EX IS LOST	RB171	
A	T1			(REINT OR ROSCAR IN CONTROL) ALU TO T1; EX IS LOST	GE541	HE541
A	SP	1000	CM8	ALU TO STORAGE PROTECT KEYS EX IS LOST	KU041	
A	CSP			(REINT OR ROSCAR IN CONTROL) ALU TO STORAGE PROTECT KEYS; EX IS LOST	GE541	HE541
A	CX	1001	CM9	OR OF ALU0-ALU6 TO CX6; ALU7 TO CX7; EX IS LOST	RC001	
A	S1			(REINT OR ROSCAR IN CONTROL) ALU TO S1; EX IS LOST	GE541	HE541
A	C0	1010	CM10	ALU TO C0; EX TO CX	RC001	
A	S0			(REINT OR ROSCAR IN CONTROL) ALU TO S0; EX TO SX	GE541	HE541
A	C1	1011	CM11	ALU TO C1; EX IS LOST	RC171	
A	SX			(REINT OR ROSCAR IN CONTROL) OR OF ALU0-ALU6, TO SX6, ALU7 TO SX7, EX IS LOST	GE541	HE541
A	Y	1100	CM12	ALU TO YA AND YB STATS; EX IS LOST	RY001	
A	D0	1101	CM13	NOT USED	-	
A	D1	1110	CM14	ALU TO D0; EX IS LOST	RD051	
A		1111	CM15	ALU TO D1; EX IS LOST	RD151	

CN FIELD ROS BITS 37-40 CPU, MX AND SC

LATCHES AND DECODER DR401
ALU FUNCTION DEC KP0X1
ALU CONTROL REGISTER KP02X

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-CONTROL SET/RESET STATS AND ALU FREE FROM CE FIELD VALUES	ALD
E		0000	CN0	NO OPERATION	RY001
E	→YA	0001	CN1	SET STATS Y0-3 WITH EMIT FIELD	DR401
E	YA.¬	0010	CN2	STATS Y0-3 ANDED WITH 'NOT' EMIT (RESET STATS WITH EMIT ONES)	DR401
E	YAΩ	0011	CN3	STATS Y0-3 ORED WITH EMIT FIELD (SET STATS WITH EMIT ONES)	DR401
E	→YB	0100	CN4	SET STATS Y4-7 WITH EMIT FIELD	DR401
E	YB¬	0101	CN5	STATS Y4-7 ANDED WITH NOT EMIT (RESET STATS WITH EMIT ONES)	DR401
E	YBΩ	0110	CN6	STATS Y4-7 ORED WITH EMIT FIELD (SET STATS WITH EMIT ONES)	DR401
E	YD.¬	0111	CN7	STATS Y8-11 ANDED WITH NOT EMIT (RESET STATS WITH EMIT ONES)	DR401
E	YDΩ	1000	CN8	STATS Y8-11 ORED WITH EMIT FIELD (SET STATS WITH EMIT ONES)	DR402
E	YE.¬	1001	CN9	STATS Y12-15 ANDED WITH NOT EMIT (RESET STATS WITH EMIT ONES)	DR402
E		1010	CN10	FORCES ROS DECODER CHECK FOR DIAGNOSTIC USE (NO FOSSL STATEMENT)	DR363
E	YCHΩ	1011	CN11	(SC ONLY) YCH1, YCH3 ORED WITH EMIT (SET STATS WITH EMIT ONES) CE2, PROG. CHECK, CE4 UNUSED	DR402
E	YCH¬	1100	CN12	(SC ONLY) YCH1, YCH3 ANDED WITH NOT EMIT (RESET STATS WITH EMIT ONES) CE2, 4 UNUSED	DR402
E		1101	CN13	NOT USED	-
E		1110	CN14	NOT USED	-
E	0000, OR	1111	CN15	ALU INDIRECT FUNCTION P OR Q ≠ F REGISTER = 0000	DR402 KP01X
		1111	CN15	ALU INDIRECT FUNCTION ALU DECODER CHECK ≠ F REGISTER = 0001	KP001
E	0010, DSQ	1111	CN15	ALU INDIRECT FUNCTION P MINUS Q (DEC) F REGISTER = 0010	KP001
E	0011, SUQ	1111	CN15	ALU INDIRECT FUNCTION P MINUS Q (BIN) F REGISTER = 0011	KP001
E	0100, P	1111	CN15	ALU INDIRECT FUNCTION PASS P ONLY ≠ F REGISTER = 0100	KP001
E	0101, AND	1111	CN15	ALU INDIRECT FUNCTION P AND Q ≠ F REGISTER = 0101	KP001
E	0110, DSP	1111	CN15	ALU INDIRECT FUNCTION Q MINUS P (DEC) F REGISTER = 0110	KP001
E	0111, SUP	1111	CN15	ALU INDIRECT FUNCTION Q MINUS P (BIN) F REGISTER = 0111	KP001
E	1000, PNQ	1111	CN15	ALU INDIRECT FUNCTION P AND (NOT Q) ≠ F REGISTER = 1000	KP001
E	1001, Q	1111	CN15	ALU INDIRECT FUNCTION PASS Q ONLY ≠ F REGISTER = 1001	KP001
E	1010, XOR	1111	CN15	ALU INDIRECT FUNCTION EXCLUSIVE OR OF PQ ≠ F REGISTER = 1010	KP001

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 973 FIELD CM, CN (FOSSL)			20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
DESIGN	GDL 7OCT65	MODEL							
DETAIL									
CHECK	NCD 11OCT65	DRAW	GT 20SEP65						FIG 973
APPRO	WRR 11OCT65	CHECK							5420062

CN FIELD (CONTINUED)

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-CONTROL SET/RESET STATS AND ALU FREE FROM CE FIELD VALUES	ALD
E	1011,QNP	1111	CN15	ALU INDIRECT FUNCTION PASS (NOT P) AND Q = F REGISTER = 1011	KP001
E	1100,RSH	1111	CN15	ALU INDIRECT FUNCTION RIGHT SHIFT Q (HALF Q) F REGISTER = 1100	KP001
E	1101,LSH	1111	CN15	ALU INDIRECT FUNCTION LEFT SHIFT Q (2 Q) F REGISTER = 1101	KP001
E	1110,DAD	1111	CN15	ALU INDIRECT FUNCTION P PLUS Q (DEC) F REGISTER = 1110	KP001
E	1111,ADD	1111	CN15	ALU INDIRECT FUNCTION P PLUS Q (BIN) F REGISTER = 1111	KP001
E		1111	CN15	ALU INDIRECT FUNCTION SKEW IS APPLIED TO THAT FUNCTION WHICH HAS AN ASTERISK TO THE RIGHT OF IT	AQ001

THESE FUNCTIONS ARE LOGIC FUNCTIONS AND DO NOT ALTER THE YC1 OR YCD CARRY LATCHES
DIRECT ALU FUNCTIONS AFFECT THE DIRECT YCD CARRY LATCH
INDIRECT ALU FUNCTIONS AFFECT THE INDIRECT YC1 CARRY LATCH
'LOAD F' AND 'USE INDIRECT' MAY BE GIVEN IN THE SAME CYCLE IN WHICH CASE THE NEW FUNCTION CAN BE EXECUTED

CP FIELD ROS BITS 41-43 PX = 0 (ROS BIT 55) CPU AND MX SENSE LATCH EB281 DECODER DR431

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-ALU INPUT TO P BUS	ALD
A	Z	000	CP0	ZEROS, GOOD PARITY TO P AND EX #	RP001
A	AX	001	CP1	AX TO P, ZEROS TO EX	RP001
A	A0	010	CP2	A0 TO P, AX TO EX	RP001
A	A1	011	CP3	A1 TO P, ZEROS TO EX UNLESS CQ = 4 #	RP001
A	B0	100	CP4	B0 TO P, ZEROS TO EX UNLESS CQ = 4 #	RP001
A	B1	101	CP5	B1 TO P, ZEROS TO EX UNLESS CQ = 4 #	RP001
A	B0	110	CP6	EMIT FIELD AND 4 ZEROS (EMIT 0000) TO P, ZEROS TO EX UNLESS CQ = 4 #	RP001
A	0E	111	CP7	4 ZEROS AND EMIT FIELD (EMIT 0000) TO P, ZEROS TO EX UNLESS CQ = 4 #	RP001

ALU EXTENSION IS RESET TO ZERO UNLESS CQ = 0100 (C0)

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 974 FIELD CN, CP (FOSSL)					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	GT	20SEP65						FIG 974
APPRO	WRR	11OCT65	CHECK								

5420063

5420064

FIG975

CP FIELD PX = 1 (ROS BIT 55) SC ONLY

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION - ALU INPUT TO P BUS	ALD SC1	ALD SC2
A		000	CP0	NOT USED	-	-
A		001	CP1	NOT USED	-	-
A	S0	010	CP2	S0 TO P, SX TO EX	GE561	HE561
A	S1	011	CP3	S1 TO P, ZEROS TO EX	GE561	HE561
A	T0	100	CP4	T0 TO P, ZEROS TO EX	GE561	HE561
A	T1	101	CP5	T1 TO P, ZEROS TO EX	GE561	HE561
A	CSB	110	CP6	CHANNEL STATUS BYTE TO P, ZEROS TO EX	GE561	HE561
A	W0	111	CP7	CHANNEL BUFFER W0 BYTE TO P, ZEROS TO EX	GE561	HE561

CQ FIELD ROS BITS 44-47

SENSE LATCHES EB291
DECODER DR471
DECODER CHECK DS015

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION - ALU INPUT CONTROL TO Q BUS	ALD
A	Z	0000	CQ0	ZEROS, GOOD PARITY TO Q AND EX UNLESS CP=2	RQ0XX
A	B0	0001	CQ1	B0 TO Q, ZEROS TO EX, UNLESS CP = 2	RQ0XX
A	B1	0010	CQ2	B1 TO Q, ZEROS TO EX, UNLESS CP = 2	RQ0XX
A	CX	0011	CQ3	CX TO Q, ZEROS IN Q0, 5, CX6, 7 ORED TO Q6; ZEROS TO EX	RQ0XX
A	C0	0100	CQ4	C0 TO Q, CX TO EX	RQ0XX
A	C1	0101	CQ5	C1 TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	D0	0100	CQ6	D0 TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	D1	0111	CQ7	D1 TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	E0	1000	CQ8	EMIT FIELD AND 4 ZEROS (EMIT 0000) TO Q ZEROS TO EX UNLESS CP = 2	RQ0XX
A	0E	1001	CQ9	4 ZEROS AND EMIT FIELD (EMIT 0000) TO Q ZEROS TO EX UNLESS CP = 2	RQ0XX
A	Y	1010	CQ10	YA AND YB STATS TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	DATA	1011	CQ11	DIRECT DATA TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	CHI	1100	CQ12	CHANNEL INTERRUPTS TO Q, ZEROS TO EX UNLESS CP = 2	RQ0XX
A	EXI	1101	CQ13	EXTERNAL INTERRUPTS TO Q, ZEROS TO EX	RQ0XX
A	SP	1110	CQ14	CPU STORAGE PROTECT KEY TO Q0, 3 MX CHANNEL KEY TO Q4, 7, ZEROS TO EX UNLESS CP = 2 (REINT OR ROSCAR IN CONTROL) STORAGE PROTECT BUS TO Q4, 7 AND CHANNEL KEY UNLESS CP = 2 TO STORAGE PROTECT BUS UNLESS CP = 2	RQ0XX
A		1111	CQ15	NOT USED	

CR FIELD ROS BITS 48-50

SENSE LATCHES EB301
DECODER DR501
DECODER CHECK DR501

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION - ALU MISCELLANEOUS CONTROLS	ALD
S		000	CR0	NO OPERATION	DR501
S	READ	001	CR1	CALL MAIN STORAGE READ	KM101
S	WRITE	010	CR2	CALL MAIN STORAGE WRITE	KM101
C	TRAP	011	CR3	TRAP ON IMA OR (PMA, YM) ≠	KM001
C	IOS	100	CR4	SET I-O STATE (EFFECTIVE IN CYCLE DEFINED)	DR501
C	CPU	101	CR5	RESET I-O STATE	DR501
C	0→SK	110	CR6	RESET SKEW BUFFER (EFFECTIVE AFTER CURRENT USE OF SKEW) Y10=0	AQ001
C	0→ERR			MODIFY BY Y10 = 1 TO GIVE RESET ERRORS	KH141
C	ADCMP	111	CR7	SET ADDRESS COMPARE	KH142

≠ TRAP DURING READ PHASE : ROS ADDRESS 10100
TRAP DURING WRITE PHASE : ROS ADDRESS 10101

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 975					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CP,CQ,CR (FOSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW.	GT	20SEP65						FIG975
APPRO	WRR	11OCT65	CHECK								5420064

5420065

FIG976

MASTER

CS FIELD ROS BIT 51 — PARITY BIT OF CURRENT ROS WORD TO GIVE AN ODD NUMBER OF BITS FOR ROS WORD

SENSE LATCH EB301
S-FIELD ENTRY DR601

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-ROS WORD PARITY BIT	ALD
NOT APPLICABLE		0	-	ODD PARITY	DR601
NOT APPLICABLE		1	-	EVEN PARITY	DR601

CT FIELD ROS BITS 52,53

SENSE LATCHES EB311
T-FIELD ENTRY AM311

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-CARRY CONTROL	ALD
		00	CT0	NO OPERATION	-
C	M	01	CT1	(1401 EMULATOR ONLY) EXTEND ROS ADDRESS	RX003
C	0	10	CT2	RESET CARRY (DIRECT OR INDIRECT ACCORDING TO ALU FUNCTION SPECIFIED)	AM311
C	1	11	CT3	SET CARRY (DIRECT OR INDIRECT ACCORDING TO ALU FUNCTION SPECIFIED)	AM311

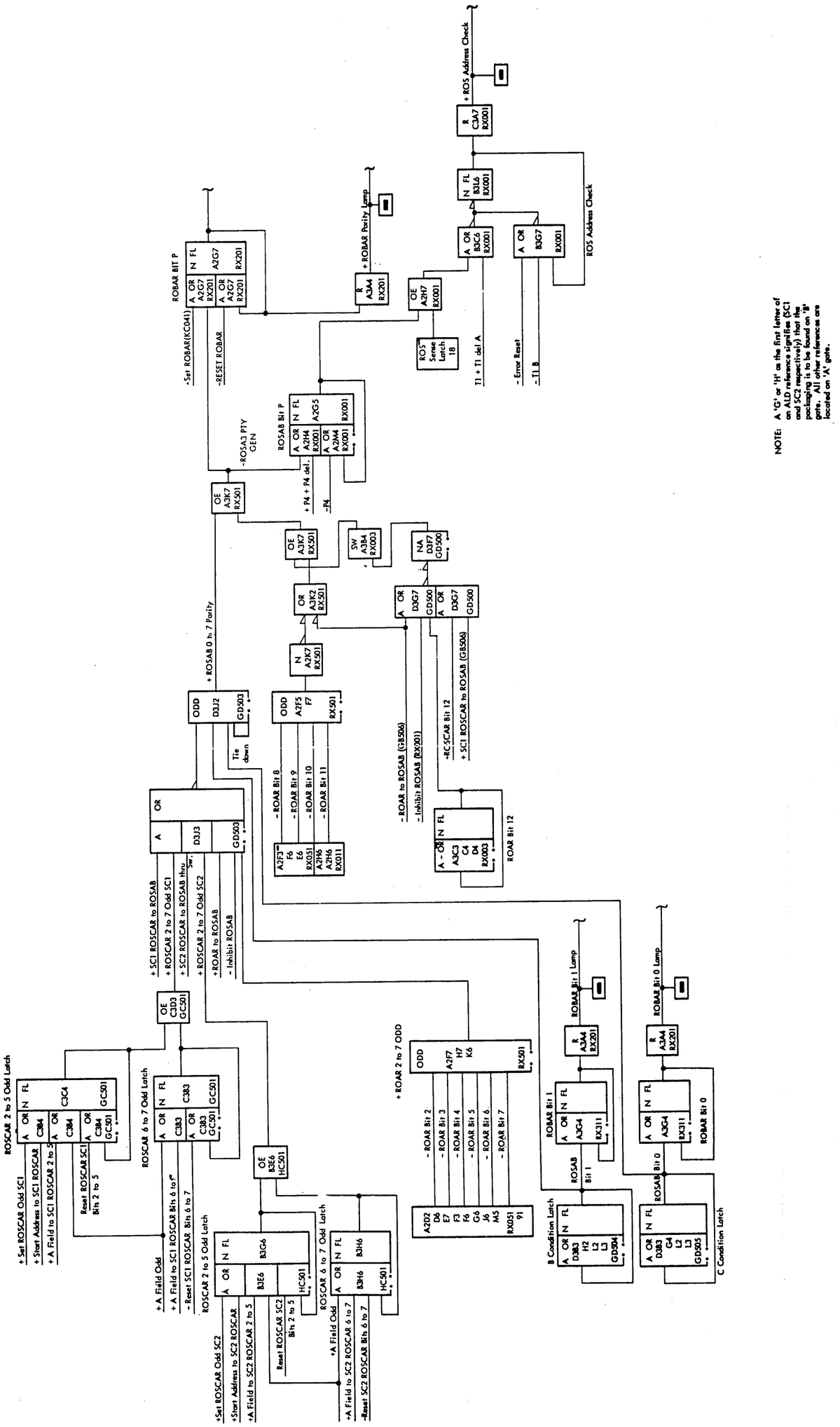
EXTENSION FIELD ROS BITS 54, 55

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION-EXTEND FIELDS J AND P	ALD	
					SENSE LATCH	DECODER
D		54	-	JX BIT EXTEND J FIELD (REF. J FIELD)	EB311	DR275
A		55	-	PX BIT EXTEND P FIELD (REF. P FIELD)	EB311	DR431

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	FIGURE 976					20OCT65	255356			X PRINT TO ENG. SPEC. NO. 895291	
	FIELD CS, CT, EXTENSION(POSSL)										
DESIGN	GDL	7OCT65	MODEL								
DETAIL											
CHECK	NCD	11OCT65	DRAW	QT	20SEP65						
APPRO	WRR	11OCT65	CHECK								FIG 976

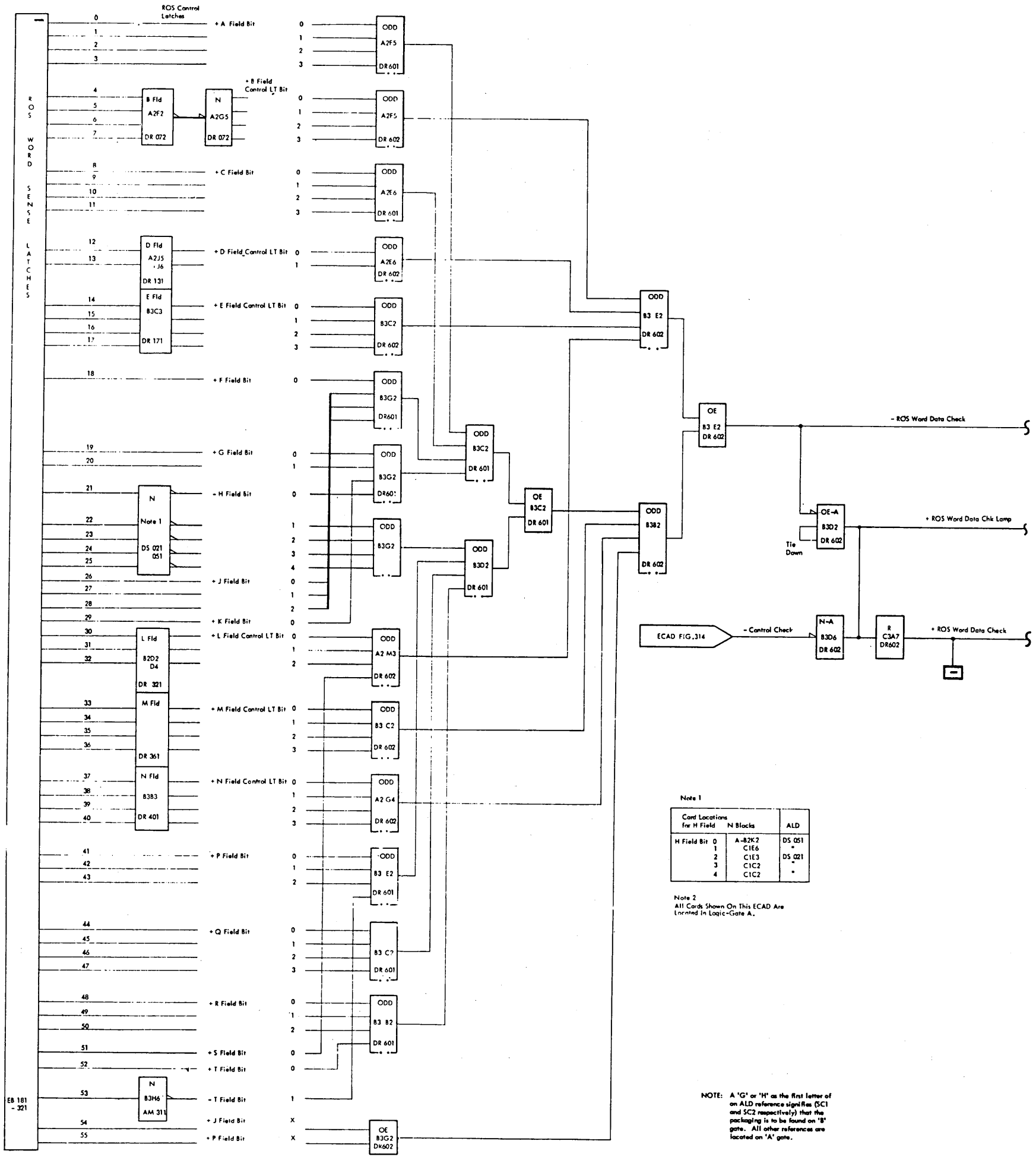
5420065

FIGURE 301 ROS ADDRESS CHECK



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420007
NAME	ROS ADDRESS CHECK ECAD					1 OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL	10CT65	MODEL	2040								
DETAIL												
CHECK			DRAW	GT	10CT 65						FIG 301	
PROG	WRR	10CT 65	CHECK									

FIGURE 302 ROS WORD DATA CHECK



Note 1

Card Locations for H Field	N Blocks	ALD
H Field Bit 0	A-B2K2	DS 051
1	C1E6	"
2	C1E3	DS 021
3	C1C2	"
4	C1C2	"

Note 2
All Cards Shown On This ECAD Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	ROS WORD DATA CHECK ECAD				
DESIGN	GDL	10CT65	MODEL	2040	
DETAIL					
CHECK			DRAW	GT	10CT65
APPRO	WRR	10CT65	CHECK		

DATE	CHANGE NO.	DATE	CHANGE NO.
1 OCT 65	255356		

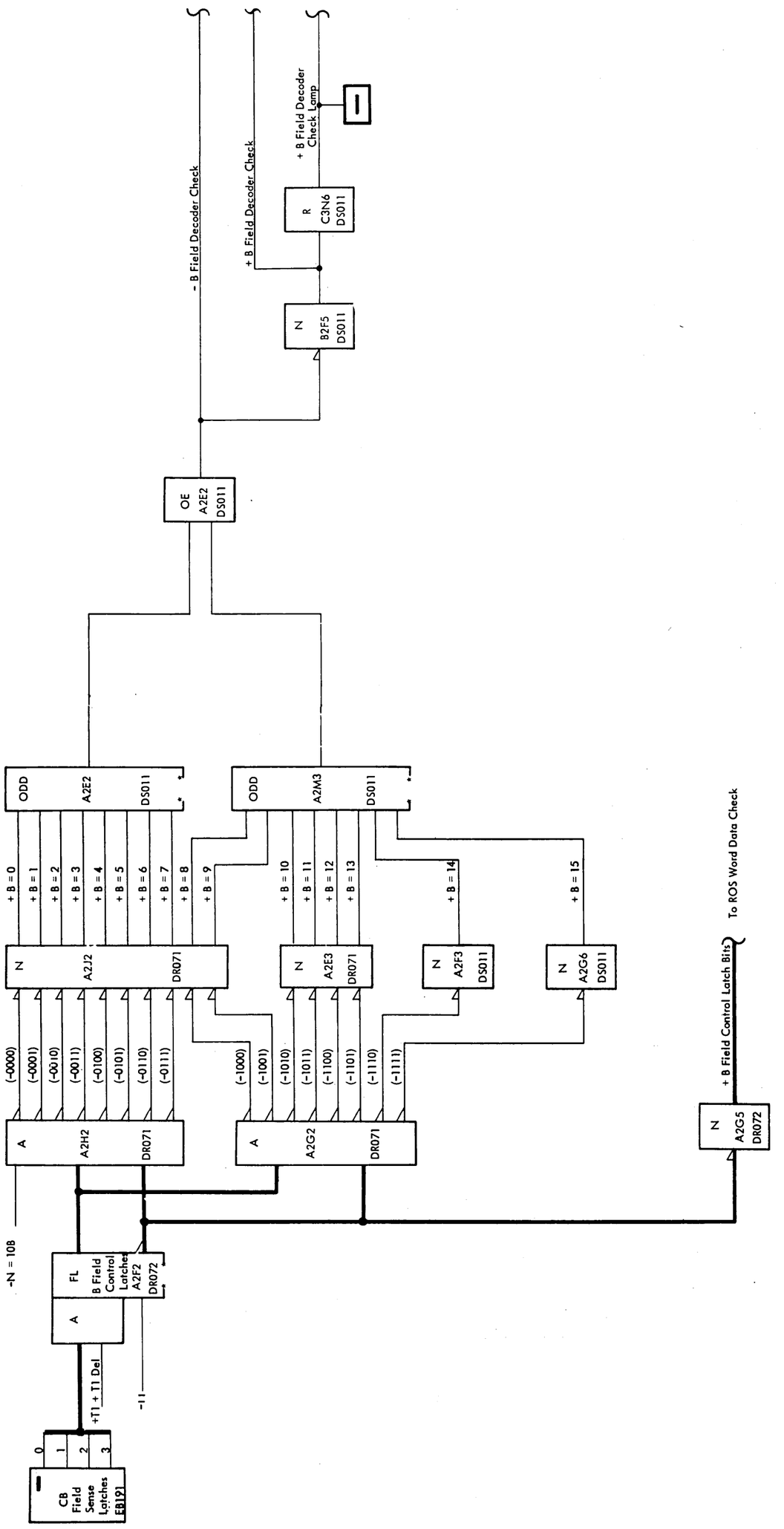
NOTE
X PRINT TO ENG. SPEC. NO.
895291

DEVELOPMENT NO.

FIG 302

5420008

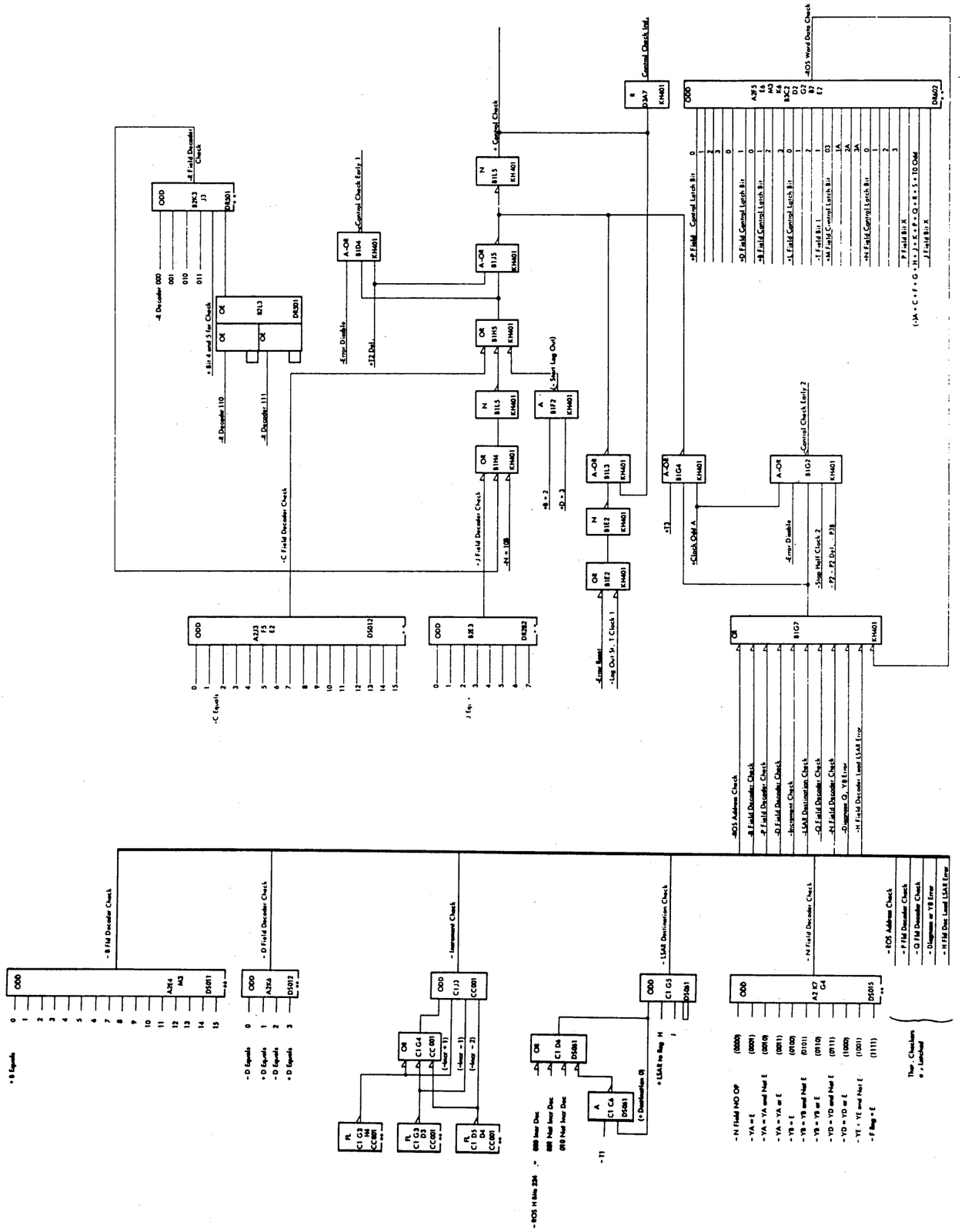
FIGURE 304 B FIELD DECODER CHECK



NOTE: A 'G' or 'H' as the first letter on an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420010
NAME	B FIELD DECODER CHECK ECAD					1 OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL	1OCT65	MODEL	2040								
DETAIL												
CHECK			DRAW	GT	1 OCT 65						FIG 304	

FIGURE 314 CONTROL CHECK



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	CONTROL CHECK ECAD					1 OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291	
ESIGN	GDL	10CT65	MODEL	2040							
DETAIL											FIG 314
CHECK			DRAW	GT	10CT65						
PPRO	WRR	10CT65	CHECK								

5420020

INTERNATIONAL BUSINESS MACHINES CORP.
NAME
DESIGN GDL 1OCT65
DETAIL
CHECK
PPRO WRR 1OCT65
CHECK
DRAW GT 1OCT65
DATE 1OCT65
CHANGE NO. 255356
DATE
CHANGE NO.
NOTE
X PRINT TO ENG. SPEC. NO. 895291
DEVELOPMENT NO.
FIG 318
5420024

RX REGISTER ECAD

(SHEET 1 OF 3)

MODEL 2040

Console Switches PA001 PA011
+ Address Switch RX Bits 6,7,P
+ Data Switch RX Bits 6,7,P
- Force RX Parity on transfer to R
A D2J3 GR521
OR D2K2 GR521
N - OR D2K5 GR521
P
SX Reg SC1 GS501
+SX Reg SC1 Bits
A - OR D2J3 GR521
+Enter S Reg to R Bus SC1
+ Enter S Reg to R Bus SC2
SX Reg SC2 HS501
+SX Reg SC2 Bits
A - OR B2B2 HRJ21
A B2B2
OR
N - OR B2C4 HR522
AX Reg RA001 RA002
- Force RX Parity on transfer to R
Register AX Bits
CX Reg RC001
Register CX Bits
From Local Storage
- Data Out Bits

+ Man Addr. Sw to R Reg.
+ Man Data Sw to R Reg.
+ Set RX Parity Bit
A A A OR-OR A3H6 RR001 RR002
P, 5, 6, 7
+ ROAR to R Man or Dump
+ DAT Ext ROS Parity
+ 2 Wire Check Ex.
+ Enter Error Group 3
A - OR A3J3 RR001
A - OR A3H2 RR001
P
- SC1 RX Entry Bus Bits RX
- SC2 RX Entry Bus Bits
+ DAT to RX Bit 6 on Dump Display
+ Ext ROS to RX Bit 7 Dump Display
+ A Register to R Register
+ C Register to R Register
- Reset R Register
A - FL A - FL A - FL OR - FL C2K5 RR001 RR002
OR - FL C2K4 RR001
N C3F3 RR001 002
ODD Note 2 C2J3 KH024
- Enter Error Group 2 (P, 6 only)
(+ MAB Parity Check) (7 only) (P, 6, 7 only)
+ Enter Data-Checks to Channel Bus MX
- Dump (P only) + Dump (6 only)
+ Enter Error Group 4 (P, 6, 7 only)
+ Register F Bit P (6 only) + Reg F Bit 0 (7only)
+ LSAR Parity Check (P only)
+ Enter Error Group 5 (All)
+ Register Ex Bits (All)
A - FL A - FL A - FL A - FL OR-OR Note 1 RR001 RR002

R Note 3 RR001 002
+ RX Bits Lamps 1
To Console Subpanel F
R Note 3 RR001 002
+ RX Bits Lamps 2
To Console Subpanel D
+ Reg RX Bits
To Registers AX and CX
- Data In Bits 5,6,7,P
To Local Storage

Note 1:

RX Reg. Bit	Card Location
P	A - C2G4
5	C2E5
6,7	C2H4

Note 2: The "ODD" Logic consists of And/Or block

Note 3:

Bit	Resistor-Cards Location Lamp 1	Lamp 2
P	A-C2B6	A-C2A4
5	C3A6	C3A6
6	C2B6	C2B6
7	C2B6	C2B6

RX Check Latch
- R Register RX Parity Check
OR A OR A3K4 KH411
R D3A7 KH411
+ RX Parity Check Lamp
A A3L5 KH411
-Error reset or Log out Start T clock
+ RX Check Latch

Figure 318-2
- R Register R0 Parity Check
R0 Check Latch
OR A OR A3K4 KH411
R D3A7 KH411
+ R0 Parity Check Lamp
A A3L5 KH411
+ R0 Check Latch

Figure 318-3
- R Register R1 Parity Check
R1 Check Latch
OR A OR A3K4 KH411
R D3A7 KH411
- R1 Parity Check Lamp
A A3L5 KH411
+ R1 Check Latch
- R Check to Early Check Latch - 0
to LS Read Check Latch

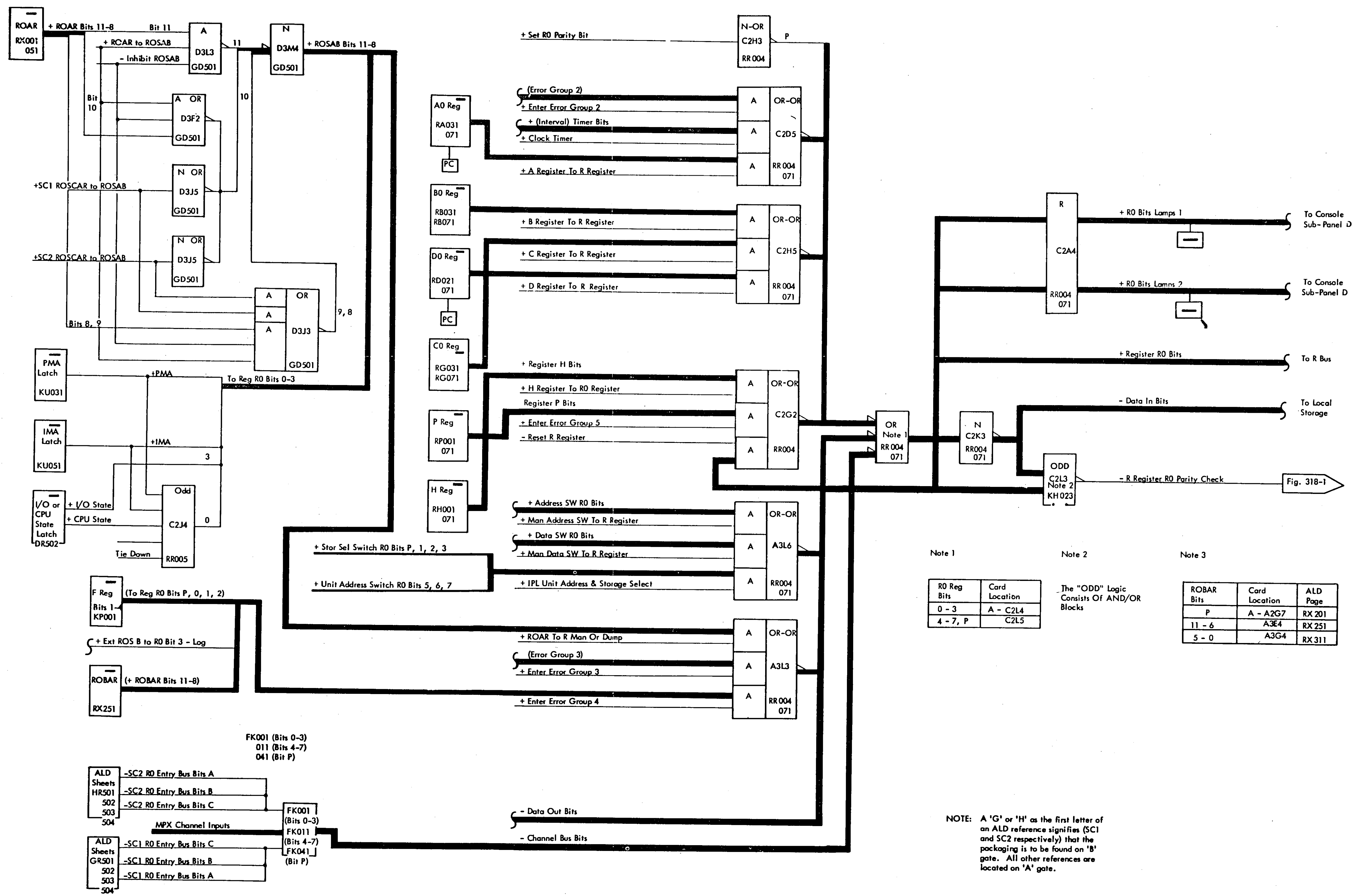
OR B1D2 KH025
A B1J2 KH411
+P3A
- Start Log-out

+ J = 6
+ T1 + T1 Del
A B1C4 KM001
RD Control Latch
OR - A A FL B1H4 B1E5
+ Power Good
- Undump Start T
- Manual Read Loc Store
- Log-out Stack Read
OR - A B1H3 KM001
-P1
-P1 Del
A B1E5 KM001
+ Allow R Bus Chk
+ P2
-P3
A A OR B1F4 KM001
- R Bus to be checked
N - A B1F5 KM001
+ LS Read Latches
OR B1J4 KH411
+Undump Cycle Inhibit (KM121)
N B1F5 KH411
A Dot KH411
-P1 Del
A B1G4 KH411
- Call Local Storage Write
- Log 2 Latch for Stack Write
- Dump Cycle Start T LS Write
- Manual Call Local Storage
OR - A B1H3 KM001

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 318 RX REGISTER
SHEET 1 OF 3
FIG 318

FIGURE 318 RO REGISTER



Note 1

R0 Reg Bits	Card Location
0 - 3	A - C2L4
4 - 7, P	C2L5

Note 2

The "ODD" Logic Consists Of AND/OR Blocks

Note 3

ROBAR Bits	Card Location	ALD Page
P	A - A2G7	RX 201
11 - 6	A3E4	RX 251
5 - 0	A3G4	RX 311

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 318

SHEET 2 OF 3

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	RO REGISTER ECAD (SHEET 2 OF 3)	DATE	CHANGE NO.	DATE	CHANGE NO.
DESIGN GDL 1 OCT 65	MODEL 2040	1 OCT 65	255356		
DETAIL / CHECK	DRAW GT 1 OCT 65				
RO WRR 1 OCT 65	CHECK				

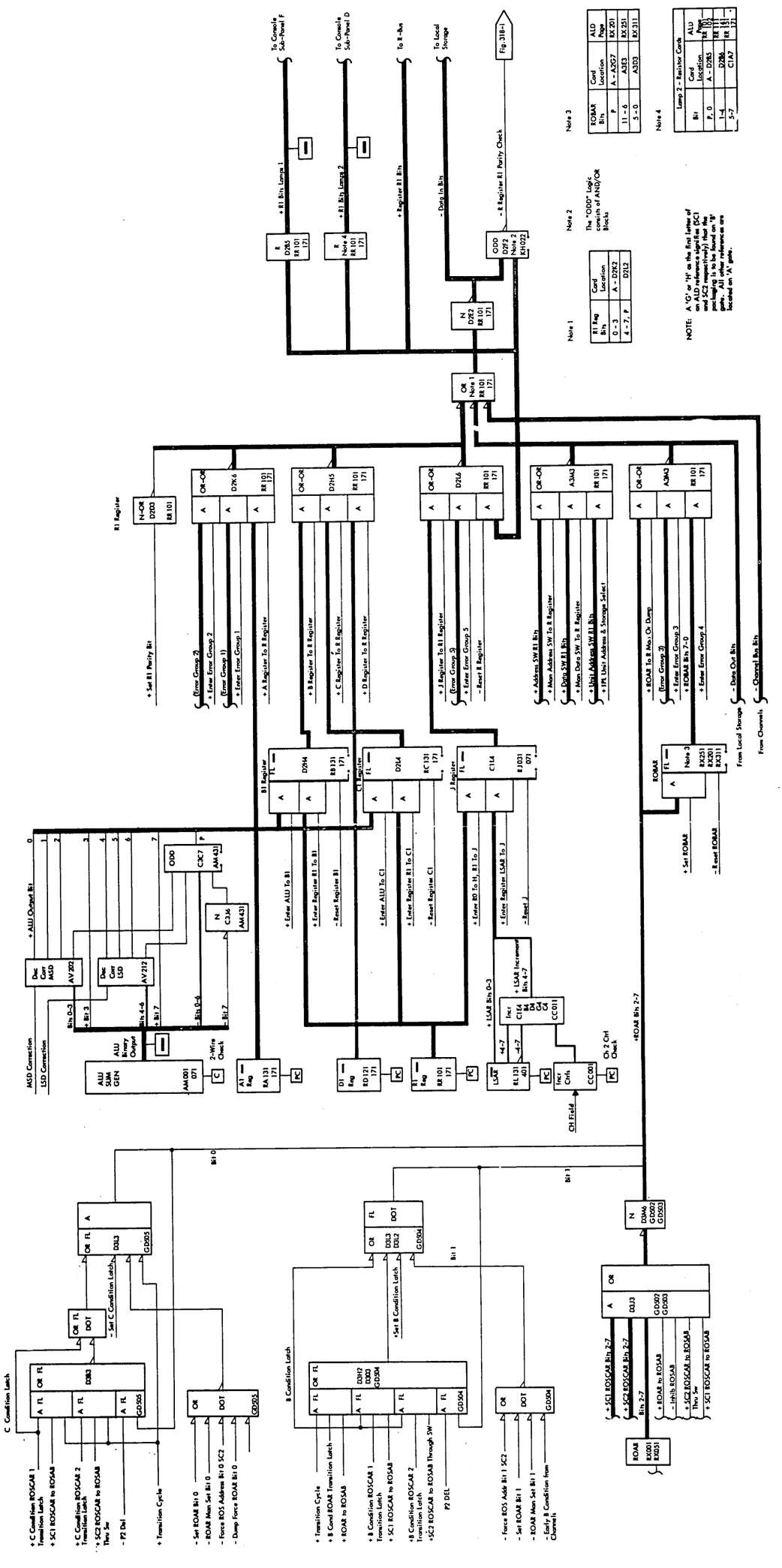
NOTE X PRINT TO ENG. SPEC. NO. 895291

DEVELOPMENT NO.

FIG 318

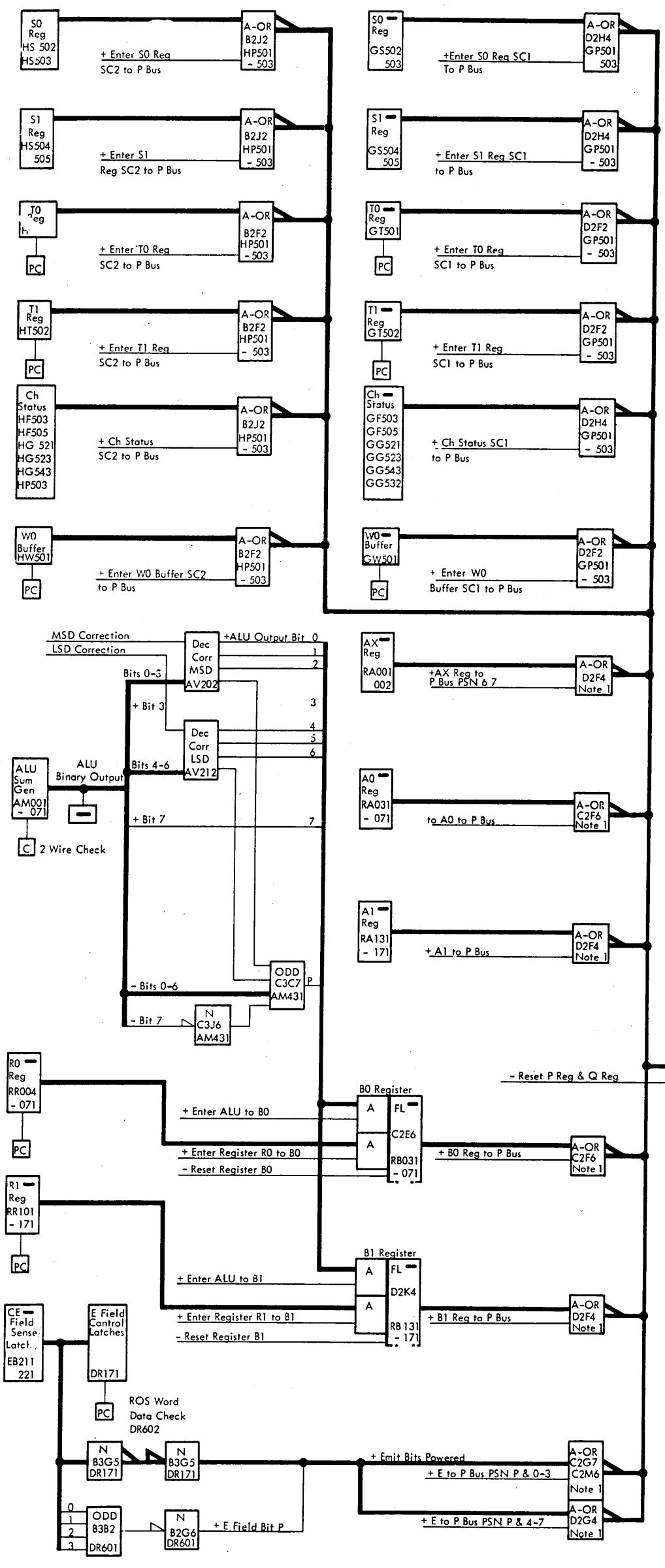
5420024

FIGURE 318 R1 REGISTER



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420024
AE	R1 REGISTER ECAD (SHEET 3 OF 3)					1 OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291		
SIGN	GDL	1OCT65	MODEL	2040								
AIL												
CHECK			DRAW	GT	1OCT 65						FIG 318	
RO	WRR	1OCT65	CHECK									

FIGURE 322 ALU P REGISTER



Note 1

P Register	
Bit	ALD Page
P	RP001
0	RP011
1	RP011
2	RP031
3	
4	RP051
5	
6	RP071
7	

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	ALU P REGISTER ECAD				
DESIGN	GDL	10CT 65	MODEL	2040	
DETAIL					
CHECK			DRAW	GT	10CT65
PRO	WRR	10CT 65	CHECK		

DATE	CHANGE NO.	DATE	CHANGE NO.
1 OCT 65	255356		

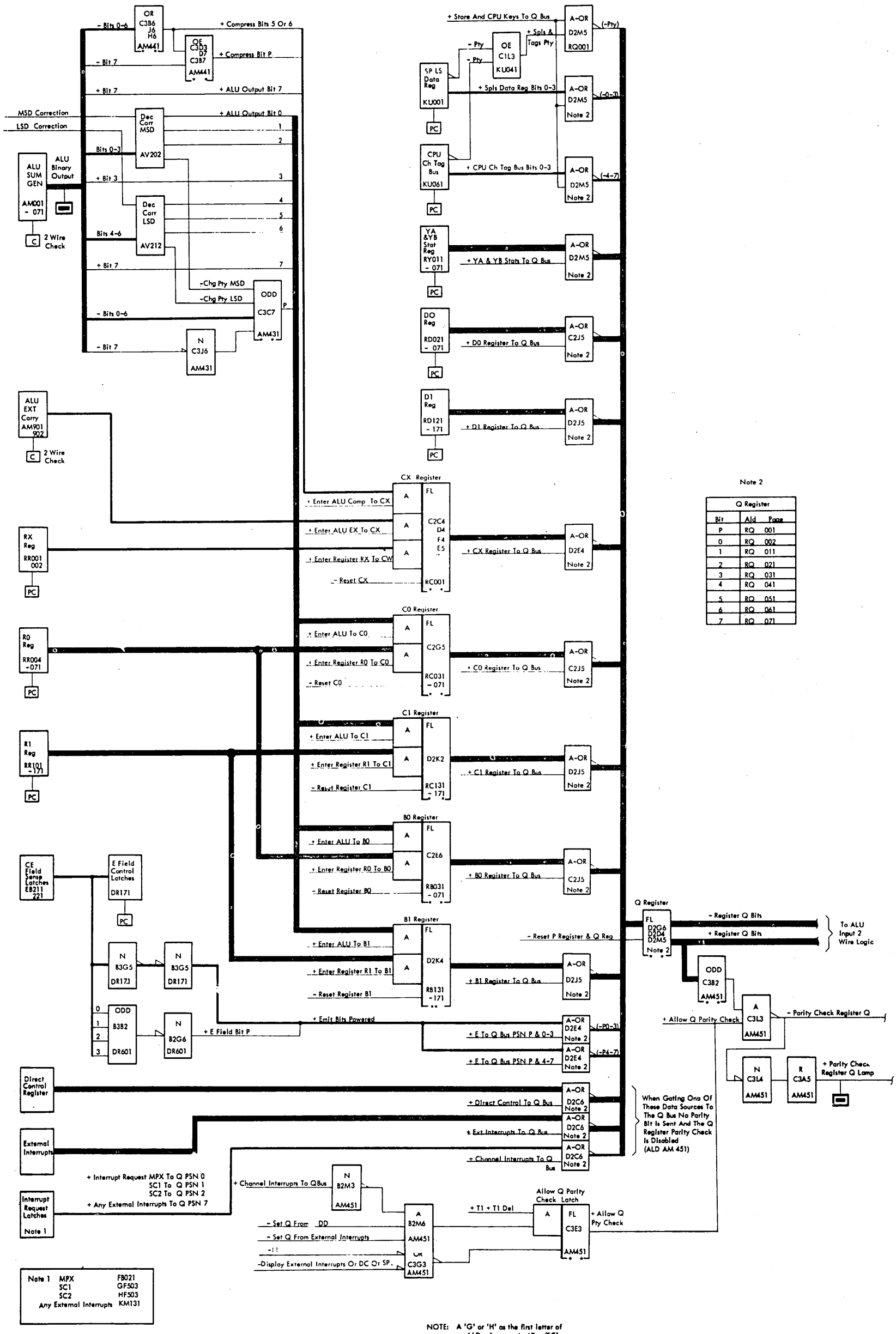
NOTE
X PRINT TO ENG. SPEC. NO.
895291

DEVELOPMENT NO.

FIG 322

5420028

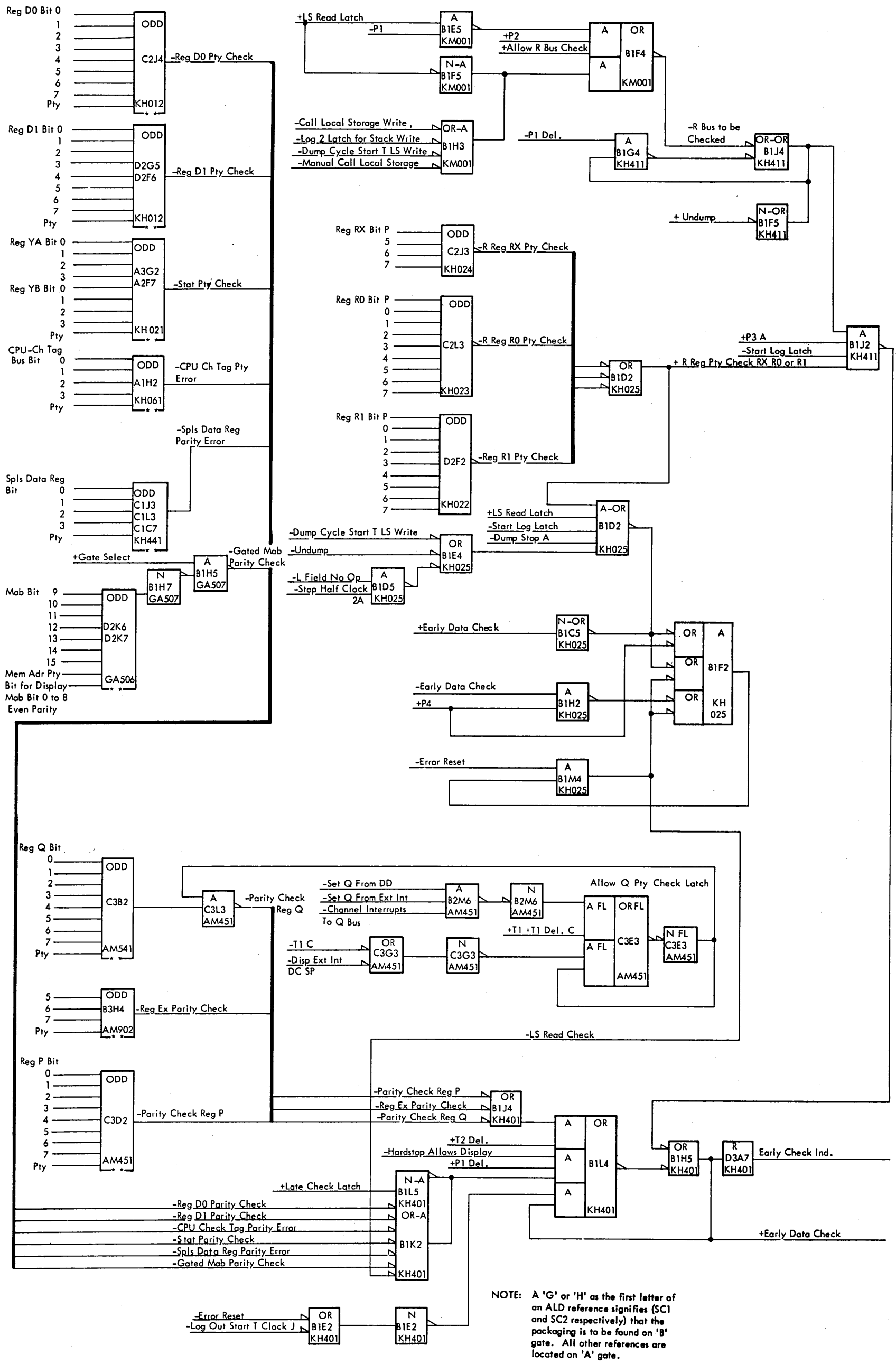
FIGURE 323 ALU Q REGISTER



NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420029
NAME	ALU Q REGISTER ECAD					1OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL	1OCT65	MODEL	2040								
DETAIL												
CHECK			DRAW	GT	1OCT 65						FIG 323	
APPRO	WRR	1OCT65	CHECK									

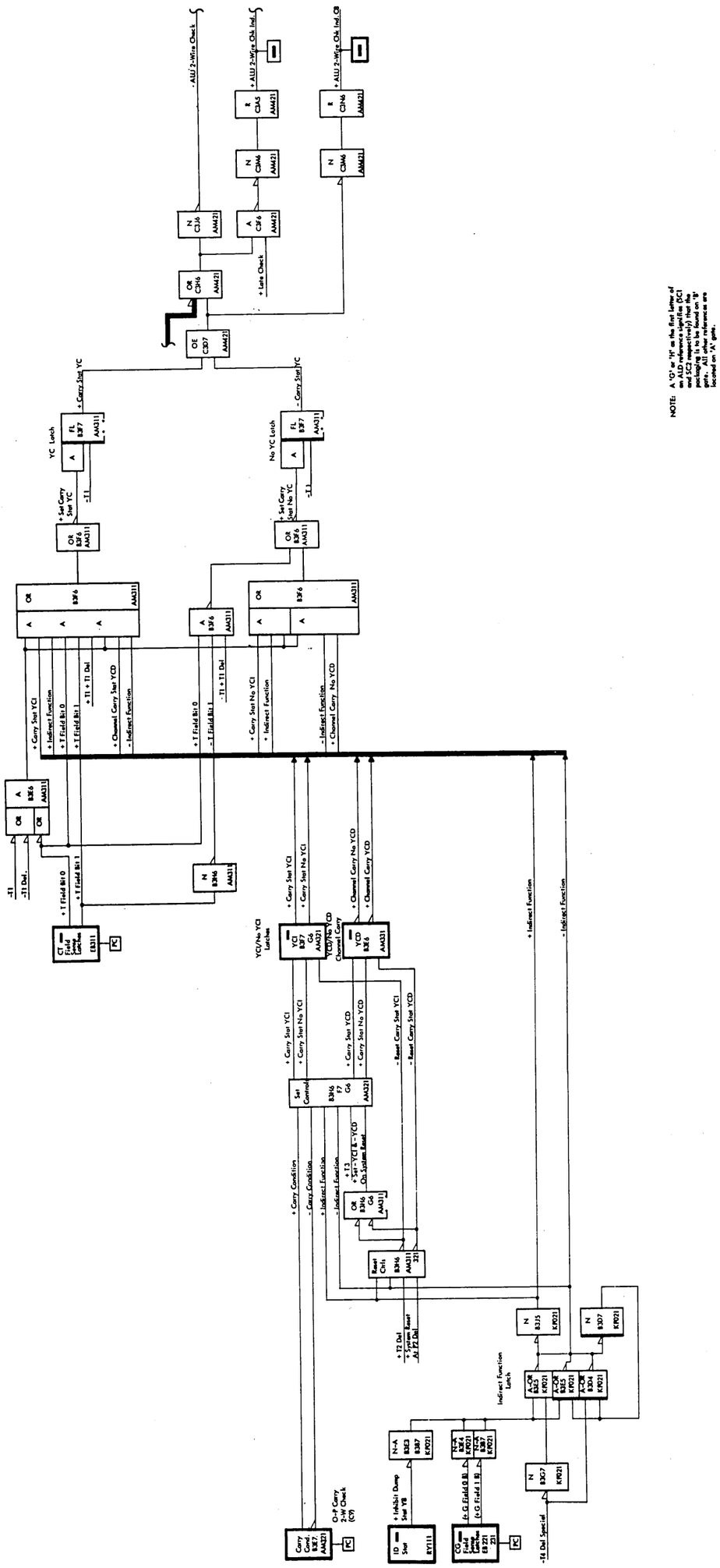
FIGURE 324 EARLY CHECK



NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420030
ME	EARLY CHECK ECAD					10CT65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL	10CT65	MODEL	2040								
DETAIL												
CHECK			DRAW	GT	10CT65						FIG 324	
PRO	WRR	10CT65	CHECK									

FIGURE 328 ALU 2-WIRE CHECK INPUT (CB)



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	5420034
NAME	ALU 2-WIRE CHECK INPUT (CB) ECAD					10CT65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL.	10CT65	MODEL		2040							
DETAIL											FIG 328	
CHECK			DRAW	GT	10CT65							
APPRO	WRF	10CT65	CHECK									

5420035

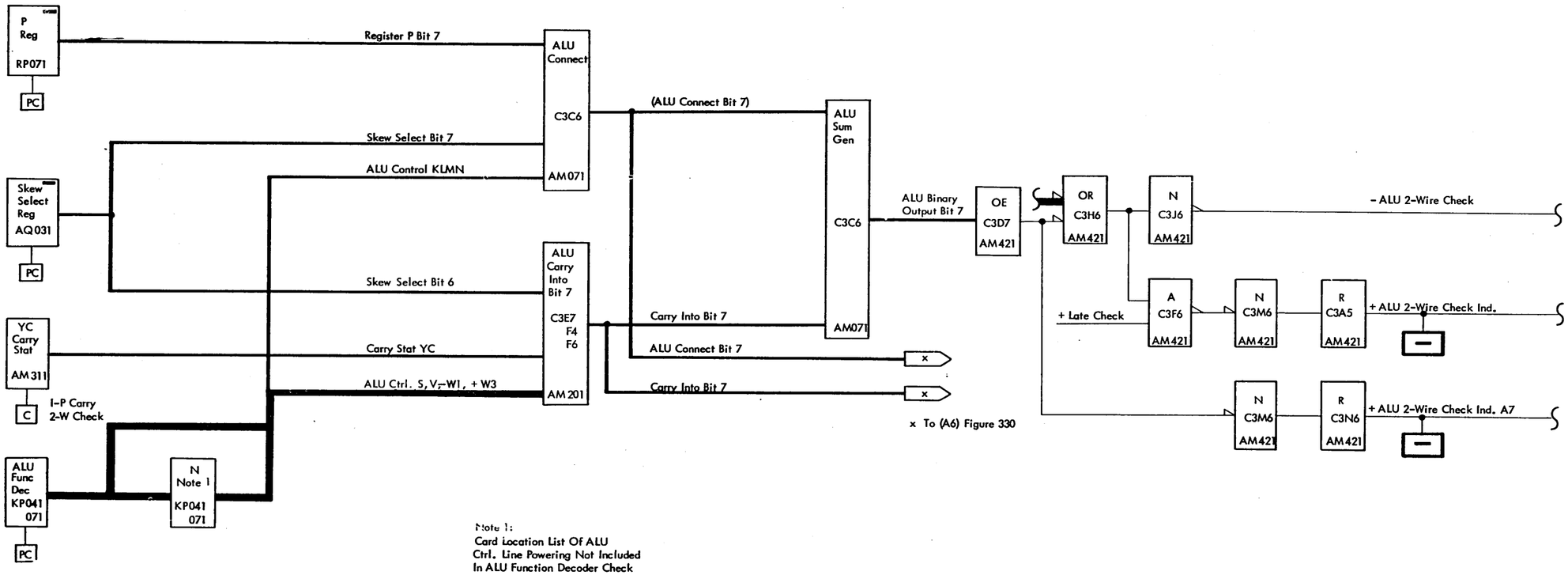


FIGURE 329 ALU 2-WIRE CHECK A7

Note 1:
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
B3E2	-S	KP051
B3M5	-W1	KP051
B3M6	+W3	KP051

Note 2:
All Cards Shown On This Ecad Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 329

APPRO	WRR	1OCT65			
CHECK					
DETAIL					
DESIGN	GDL	1OCT65	MODEL	2040	
CHECK			DRAW	GT	1OCT65

INTERNATIONAL BUSINESS MACHINES CORP.

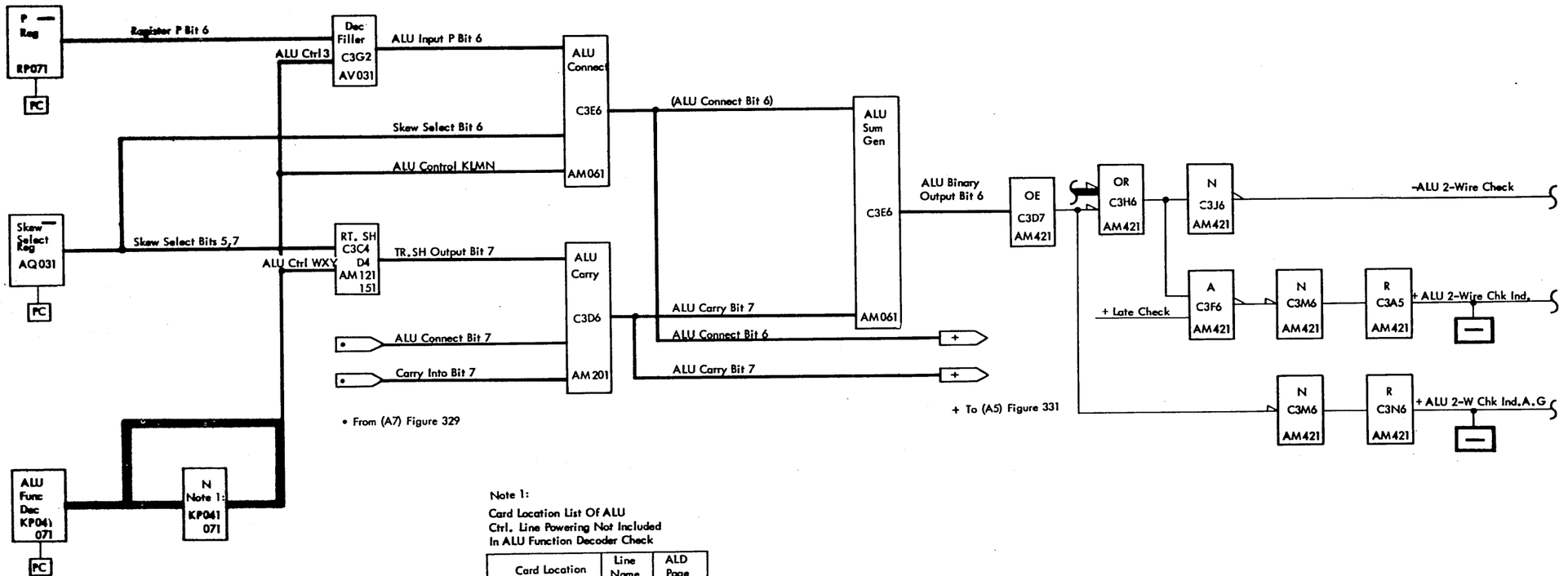
NAME ALU 2-WIRE CHECK A7 CHECK

DATE	CHANGE NO.
1OCT65	255356

NOTE
X PRINT TO ENG. SPEC. NO. 895291

DEVELOPMENT NO. 5420035

80



• From (A7) Figure 329

+ To (A5) Figure 331

Note 1:
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2:
All Cards Shown On This Ecad Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIGURE 330 ALU 2-WIRE CHECK A-6

FIG 330

	NAME	DATE
DESIGN	GDL	10CT65
DETAIL		
CHECK		
PRO	WRR	10CT65
DRAW	GT	10CT65
CHECK		

INTERNATIONAL BUSINESS MACHINES CORP.
ALU 2-WIRE CHECK A-6 ECAD
MODEL 2040

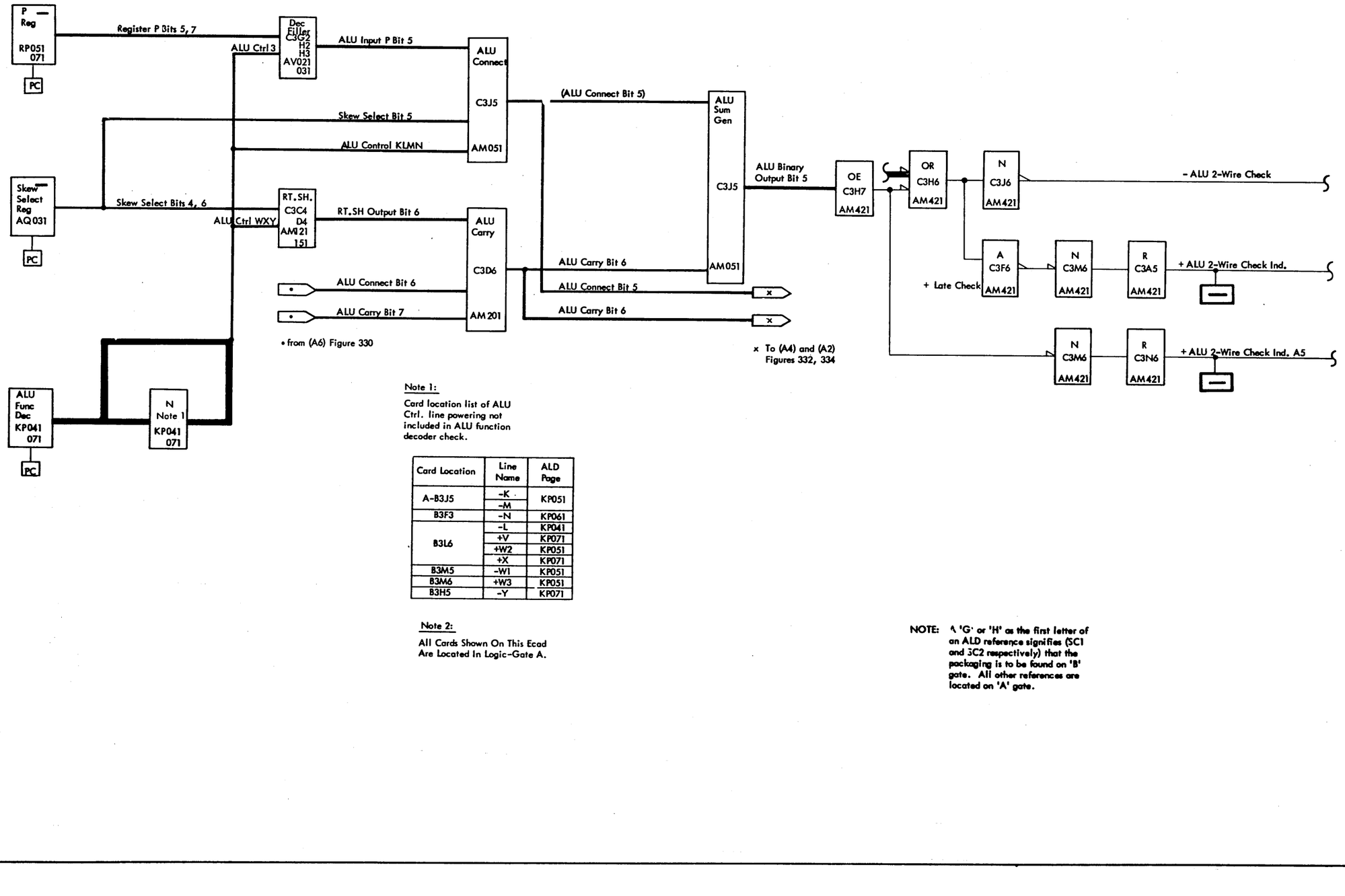
CHANGE NO.	DATE
255356	10CT65

NOTE
X PRINT TO ENG. SPEC. NO. 895291

DEVELOPMENT NO.

5420036

5420037



• from (A6) Figure 330

x To (A4) and (A2) Figures 332, 334

Note 1:

Card location list of ALU Ctrl. line powering not included in ALU function decoder check.

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2:

All Cards Shown On This Ecad Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and 3C2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIGURE 331 ALU 2-WIRE CHECK A5

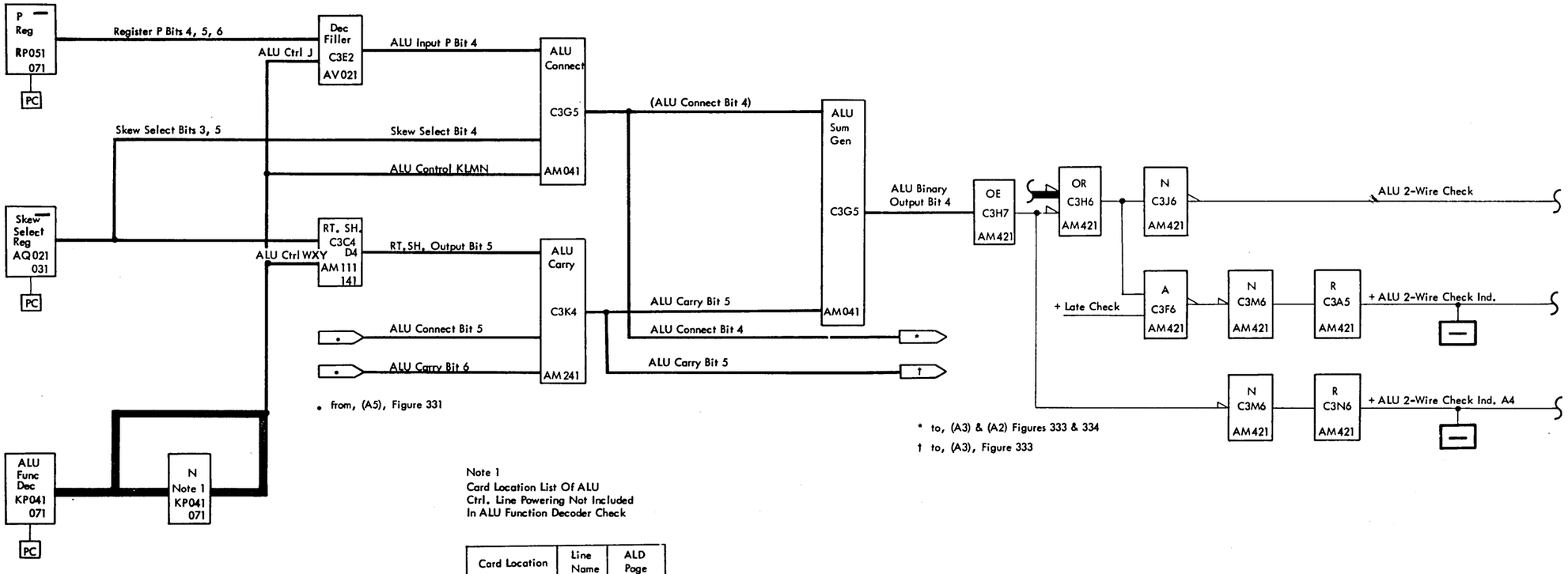
FIG 331

INTERNATIONAL BUSINESS MACHINES CORP.									
ALE	ALU 2-WIRE CHECK A5.ECAD								
DRAWN	GDL	10CT65	MODEL	2040					
CHECK									
DRAW	GT	10CT65							
CHECK	WRR	10CT65							
DATE									10CT65
CHANGE NO.									255356
DATE									
CHANGE NO.									
NOTE X PRINT TO ENG. SPEC. NO. 895291									
DEVELOPMENT NO.									

5420037

5420038

FIGURE 332 ALU 2-WIRE CHECK A4



• from, (A5), Figure 331

* to, (A3) & (A2) Figures 333 & 334

† to, (A3), Figure 333

Note 1
Card Location List Of ALU
Ctrl. Line Powering Not Included
In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2
All Cards Shown On This Ecac
Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 332

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	ALU 2-WIRE CHECK A4 ECAD				
SIGN	GDL	10CT65	MODEL	2040	
DETAIL					
CHECK					
DRAW	GT	10CT65			
CHECK					
PRO	WRR	10CT65			

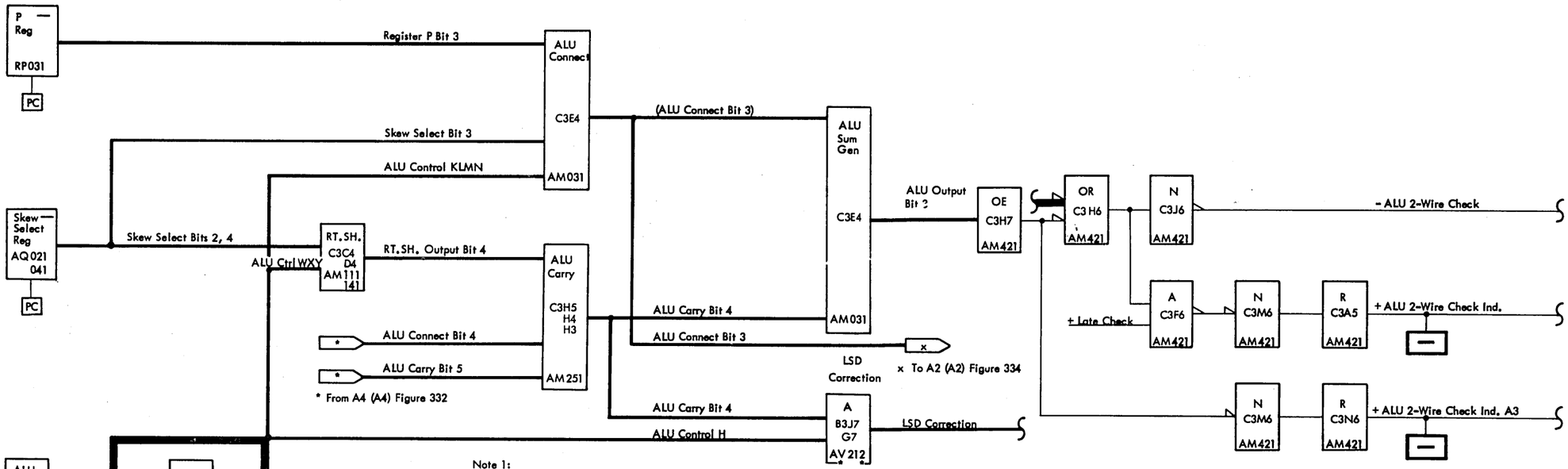
DATE	CHANGE NO.
10CT65	255356

NOTE
X PRINT TO ENG. SPEC. NO.
895291

DEVELOPMENT NO.
FIG 332

5420038

FIGURE 333 ALU 2-WIRE CHECK A3



Note 1:
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-C3J6	+H	KP101
B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP041
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2:
All Cards Shown On This Ecad Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 333

	NAME	DATE
DESIGN	GDL	10CT65
DETAIL		
CHECK		
APPRO	WRR	10CT65
CHECK		
DRAW	GT	10CT65

INTERNATIONAL BUSINESS MACHINES CORP.

ALU 2-WIRE CHECK A3 ECAD

MODEL 2040

CHANGE NO.	DATE
255356	10CT65

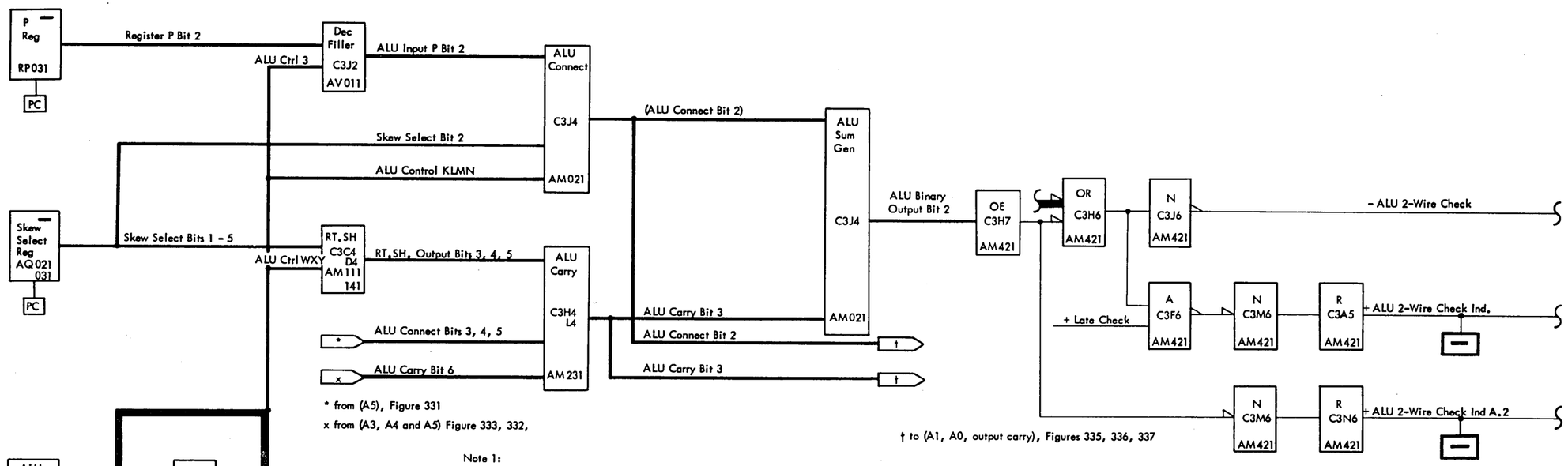
NOTE
X PRINT TO ENG. SPEC. NO. 895291

DEVELOPMENT NO. FIG 333

5420039

5420040

FIGURE 334 ALU 2-WIRE CHECK A2



* from (A5), Figure 331

x from (A3, A4 and A5) Figure 333, 332,

† to (A1, A0, output carry), Figures 335, 336, 337

Note 1:
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check.

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2:
All cards shown on this ECAD are located in logic-gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

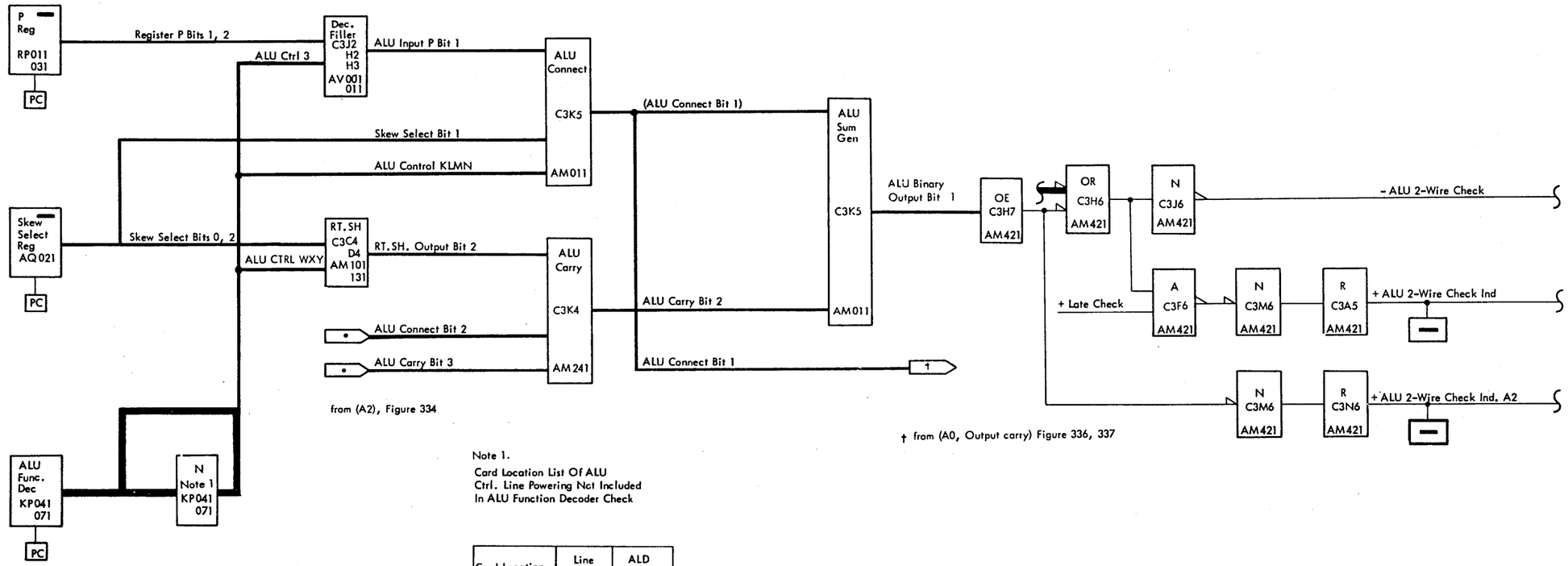
FIG 334

	NAME	DATE	CHANGE NO.
	INTERNATIONAL BUSINESS MACHINES CORP.		
	ALU 2-WIRE CHECK A2 ECAD	10CT65	255356
DETAIL			
CHECK			
DESIGN	GDL	10CT65	MODEL 2040
PPRO	WRR	10CT65	DRAW GT 10CT65
CHECK			

NOTE
X PRINT TO ENG. SPEC. NO. 895291

DEVELOPMENT NO. FIG 334

5420040



Note 1.
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	
B3F3	-N	KP061
B3L6	-L	KP041
	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

Note 2.
All Cards Shown On This Ecad Are Located In Logic-Gate A.

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIGURE 335 ALU 2-WIRE CHECK A1

FIG 335

	NAME	DATE	CHANGE NO.
DESIGN	GDL	10CT65	255356
DETAIL			
CHECK			
PRO	WRR	10CT65	

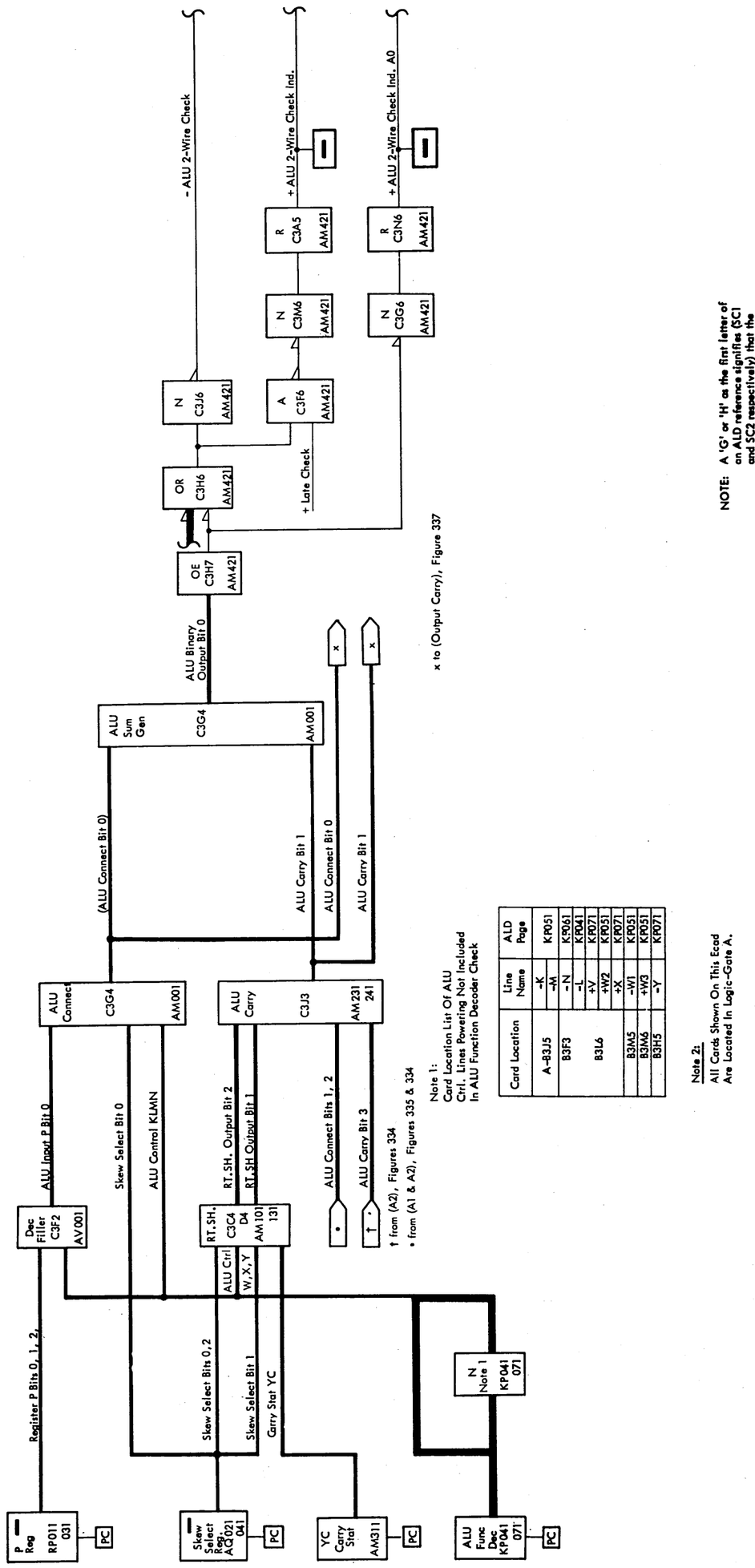
INTERNATIONAL BUSINESS MACHINES CORP.
ALU 2-WIRE CHECK A1 ECAD
MODEL 2040
DRAW GT 10CT65
CHECK

NOTE
X PRINT TO ENG. SPEC. NO. 89529!

DEVELOPMENT NO.
FIG 335

5420041

FIGURE 336 ALU 2-WIRE CHECK AO



NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

Note 1:
Card Location List Of ALU Ctrl. Lines Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A-B3J5	-K	KP051
	-M	KP051
B3F3	-N	KP061
	-L	KP041
B3L6	+V	KP071
	+W2	KP051
	+X	KP071
B3M5	-W1	KP051
B3M6	+W3	KP051
B3H5	-Y	KP071

† from (A2), Figures 334
• from (A1 & A2), Figures 335 & 334

Note 2:
All Cards Shown On This Ecad Are Located In Logic-Gate A.

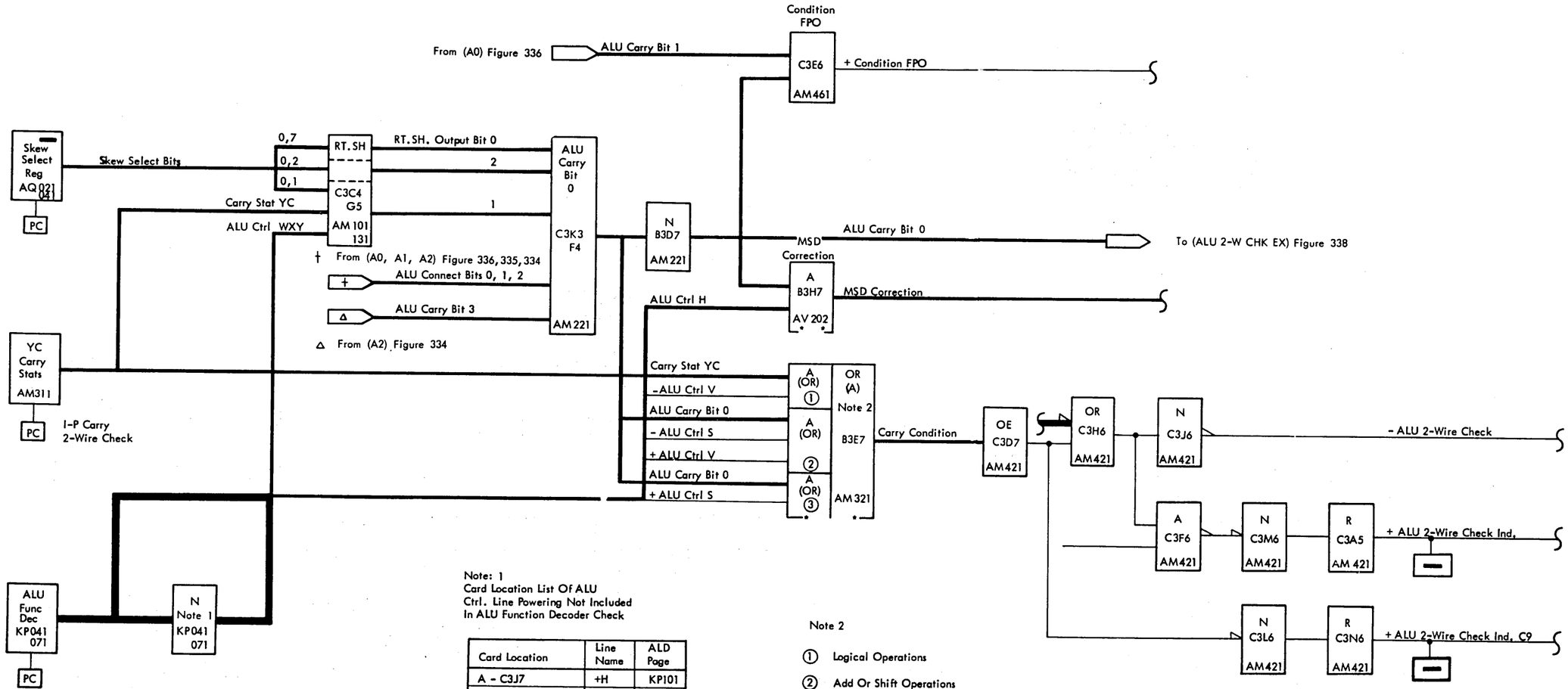
INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	ALU 2-WIRE CHECK AO ECAD					10CT65	255356			X PRINT TO ENG. SPEC. NO. 895291	5420042
DESIGN	GDL	10CT65	MODEL	2040							
DETAIL											FIG 336
CHECK			DRAW	GT	10CT65						
PPRO	WRR	10CT65	CHECK								

INTERNATIONAL BUSINESS MACHINES CORP.
NAME ALU 2-WIRE CHECK OUTPUT
CARRY (C9) ECAD
DESIGN GDL 10CT65 MODEL 2040
DETAIL
CHECK
APPRO WRR 10CT65 CHECK
DRAW GT 10CT65

DATE	CHANGE NO.
1 OCT 65	255356

NOTE
X PRINT TO ENG. SPEC. NO.
895291

DEVELOPMENT NO.
FIG 337
5420043



Note: 1
Card Location List Of ALU Ctrl. Line Powering Not Included In ALU Function Decoder Check

Card Location	Line Name	ALD Page
A - C3J7	+H	KP101
B3K7	-S	KP051
B3G7	+V	KP071
	+W1	KP051
	+W2	
	+Y	KP071
B3L7	-W1	KP051
	+X	KP071

Note 2

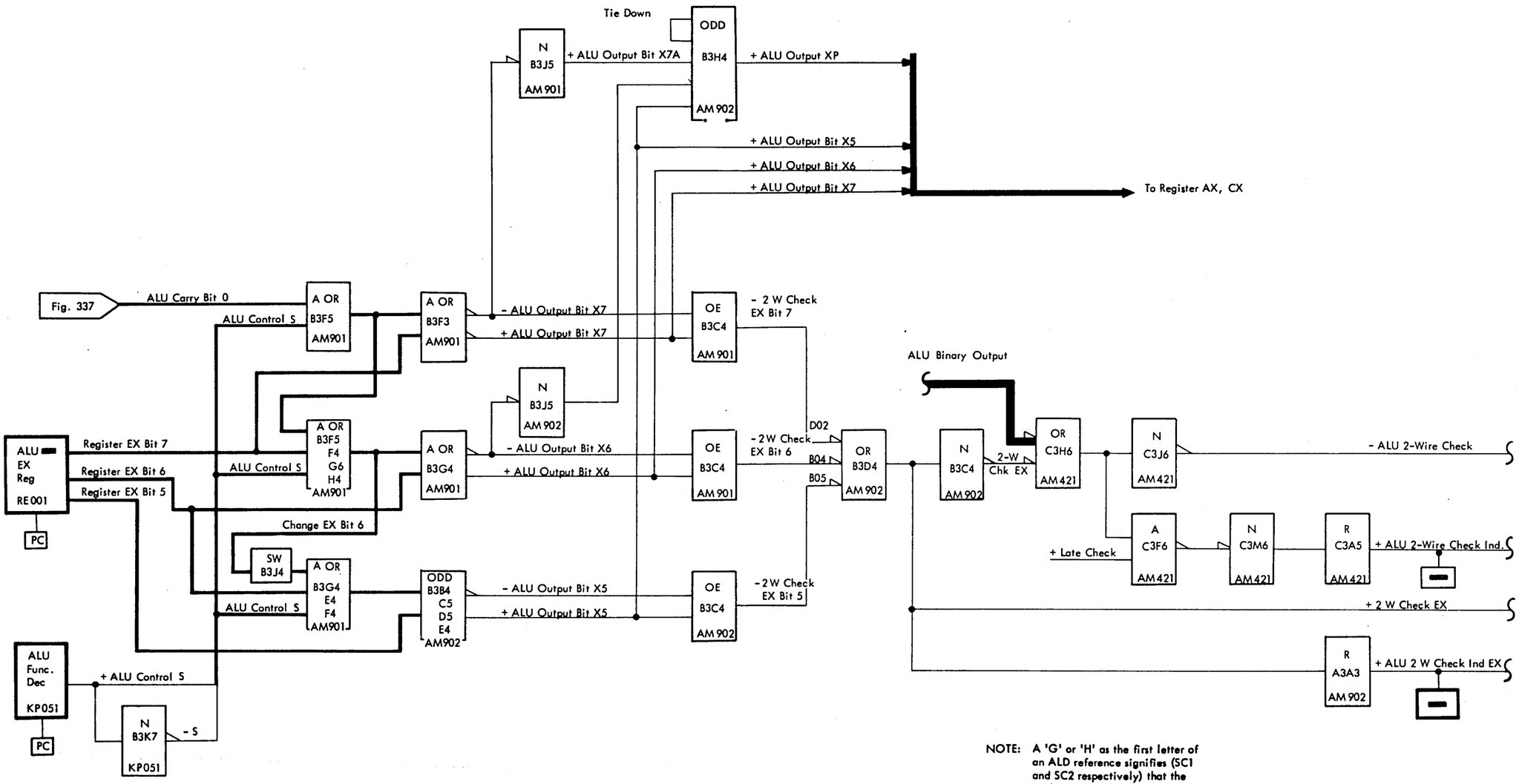
① Logical Operations
② Add Or Shift Operations
③ Subtract Operations

NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIGURE 337 ALU 2-WIRE CHECK OUTPUT CARRY (C9)

FIG 337

FIGURE 338 ALU 2-WIRE CHECK EX



NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

FIG 338

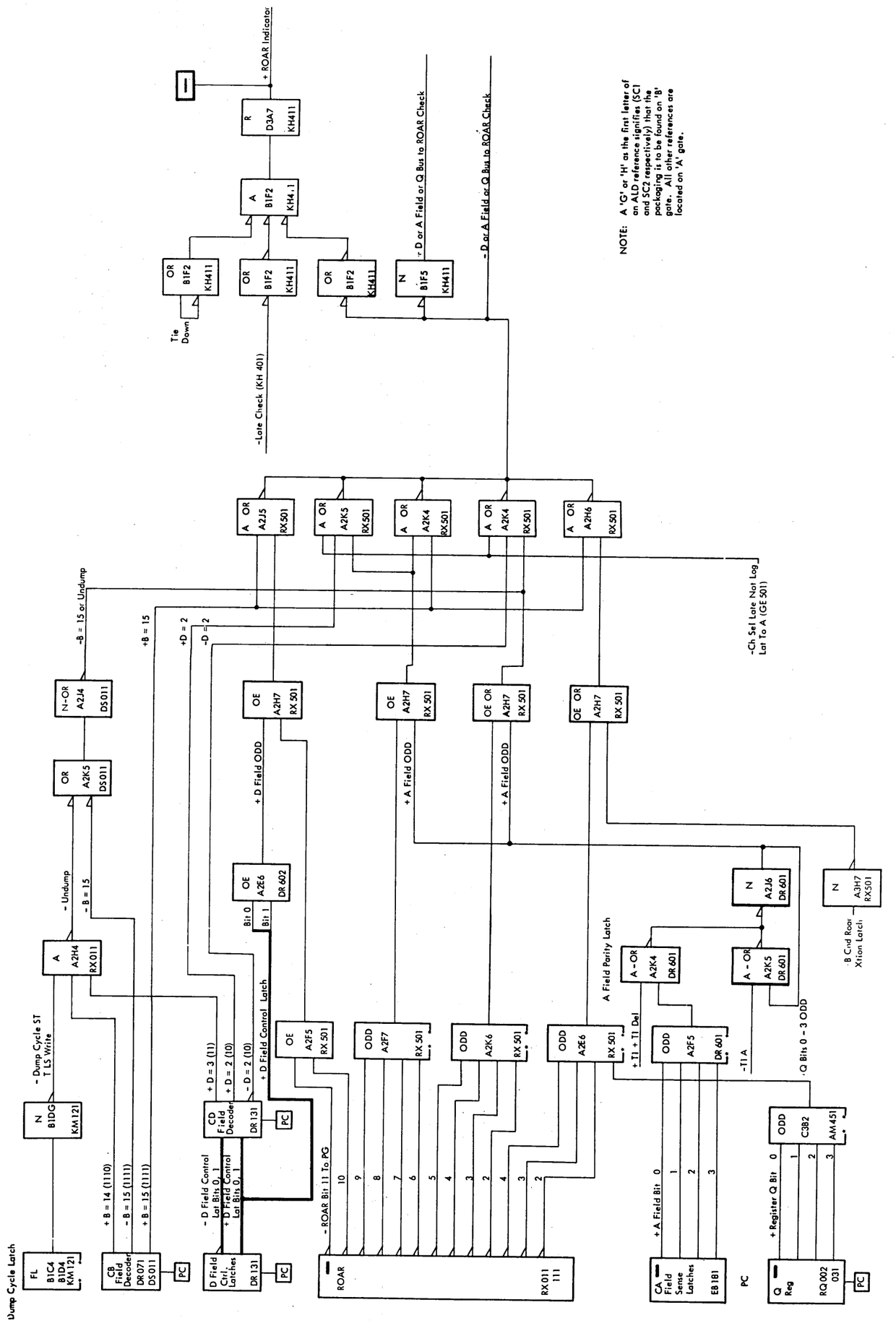
INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	ALU 2-WIRE CHECK EX ECAD				
DESIGN	GDL	10CT65	MODEL	2040	
DETAIL					
CHECK			DRAW	GT	1 OCT 65
APPRO	WRR	10CT65	CHECK		

CHANGE NO.	DATE
255356	1 OCT 65

NOTE
X PRINT TO ENG. SPEC. NO.
895291

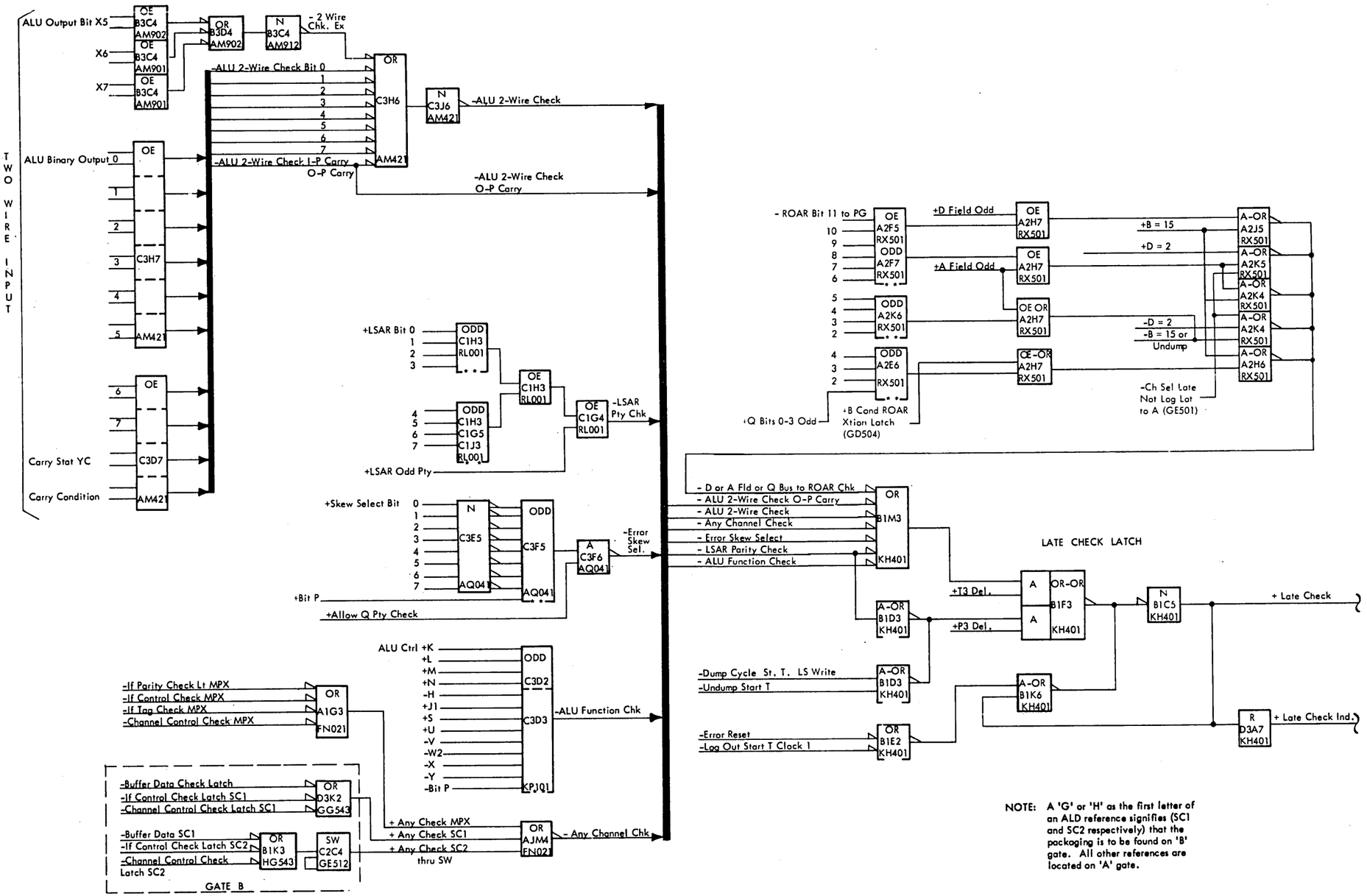
DEVELOPMENT NO.
5420044

FIGURE 339 ROAR LOAD CHECK



INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	542U045
NAME	ROAR LOAD CHECK ECAD					1 OCT 65	255356			X PRINT TO ENG. SPEC. NO. 895291		
DESIGN	GDL	10CT65	MODEL	2040								
DETAIL												
CHECK			DRAW	GT	1OCT 65						FIG 339	
APPRO	WRR	10CT65	CHECK									

FIGURE 343 LATE CHECK



NOTE: A 'G' or 'H' as the first letter of an ALD reference signifies (SC1 and SC2 respectively) that the packaging is to be found on 'B' gate. All other references are located on 'A' gate.

NAME	LATE CHECK ECAD				INTERNATIONAL BUSINESS MACHINES CORP.
DESIGN	GDL	10CT65	MODEL	2040	
DETAIL					
CHECK		DRAW	GT	10CT65	
PRO	WRR	10CT65			

DATE	CHANGE NO.	DATE
1 OCT 65	255356	

NOTE
X PRINT TO ENG. SPEC. NO.
895291

DEVELOPMENT NO.

FIG 343

5420046

System/360 Model 40

Machine Status Charts

PREFACE

Machine status charts record the valid machine status of various latches and registers at the end of each specified microinstruction in single cycle mode. Machine status charts are provided for:

1. Hardware System Reset
2. CPU Check-Out Microprogram
3. System Reset Microprogram
4. Initial Program Load Microprogram
5. Dump-Undump Microprogram
6. Selector Channel Microprogram

In order that the CPU check out will produce valid results, the hardware system reset must be successfully executed before entering the program. Thus, hardware system reset status provides a basic checking point in machine operation. This status can be displayed on the console panel by depressing the system reset pushbutton in single cycle mode, and the operation can be checked with the hardware system reset machine status chart. This operation is immediately followed by the CPU check-out microprogram. In the case of a solid failure in the CPU check-out section of system reset, the machine stops. If it is desired to loop on the error, use check restart because the normal CPU check-out loop is selected by the diagnostic control switch which is active only in the manual stop state. A failure during system reset will prevent the machine from reaching the manual stop state, thus the use of check restart. Machine status charts will also contain, where applicable, diagnostic hints in the form of descriptive notes. In addition the CAS statement is included on all status charts.

The two types of checks which will be detected by the CPU check-out microprogram are:

1. Hardware checks: Hard stop being forced with one of the check lights on panel A of the console.

2. Program checks: The program taking a wrong branch and ending at one of the microinstructions containing stop, i.e., EC200, EC211, ECW01, and ECW10.

The hardware checks are shown on the failure analysis diagrams. These notes are concerned with a failure which leads to a microprogram stop at one of the four preceding addresses.

In general, during the CPU check-out microprogram, the checks on the machine conditions are made two at a time and the pair is selected to be independent, so that a single failure will lead to just one of them failing. The program operates correctly and continues in the correct sequence if the branch is to EC201, EC210, ECW00 or ECW11; but a failure in either one of the machine conditions being tested will result in a stop. If the successful branch depends on the CB condition being off and the CC condition being on, it is unlikely that one single machine failure will result in the CB condition being on at the same time as the CC condition is off.

When the microprogram stop is encountered, the first requirement is to determine the last program instruction being executed. At the time of stopping, ROAR and ROBAR will give no information to help determine this address.

One way of determining the address is to observe the register states and compare these with the list of expected register states given on pages ECZ0001 and ECW0001.

During execution of the program, the expected status occurs when any EC201 or EC210 is known. These instructions are each executed many times, and if a stop occurs at EC200 or EC211, it is assumed that one EC201 or EC210 should have been selected. The lists previously referenced show all the expected register states when EC201 and EC210 are being executed and corresponding with each state is the last microinstruction address (the one that should have been executed last in the correct program sequence). An identical list is generated for ECW0001 as for EC20001. Having determined the microinstruction executed, a full description of expected register and latch status CAS statement and descriptive notes are given on the appropriate charts.

The descriptive notes detail the checks that are taking place, and what circuitry should be suspected if wrong branches are taken. These notes should prove sufficient to isolate to a small section of circuitry, using the notes on one chart only, together with fault analysis diagrams which are sometimes added.

If it is not possible to determine the microinstruction being executed when the data error first occurred, resulting in a later deviation from the correct sequence, it may be necessary to single cycle particular numbers of steps through the program performing spot checks on the address to determine where the first deviation from the correct sequence occurs.

Pointers on page address: The page address can be found as follows:

example (in upper right-hand corner)

Page MIC.P0.024
Date 12 Jul 65
Chart ----- 24

The page address is MIC P024. This is derived from the "MIC P0" on the first line and "24" on the third line. Note that the date in the upper right-hand corner of the page shows when the chart was first issued. The date at the lower left-hand corner of the page shows when the page was revised.

MAJOR REVISION (April 1966)
This edition, Form 223-2858-0, obsoletes Forms Z22-2858-0 and Z22-2892-0. Minor changes are indicated by an asterisk (*) to the left of the subject headings on the Contents page. A section on the selector channel microprogram has been added.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.
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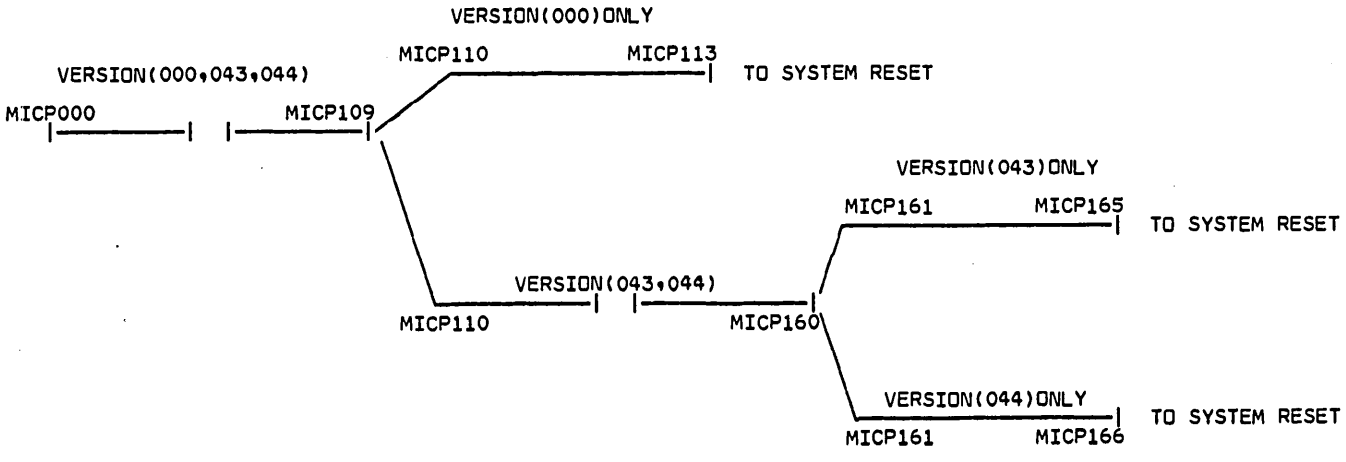
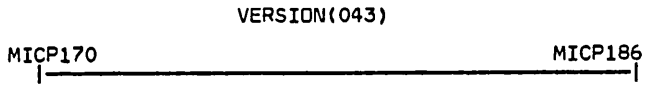
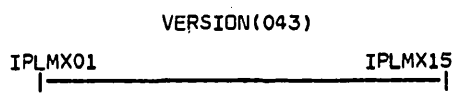
Table of Contents



- DUMP UNDUMP -

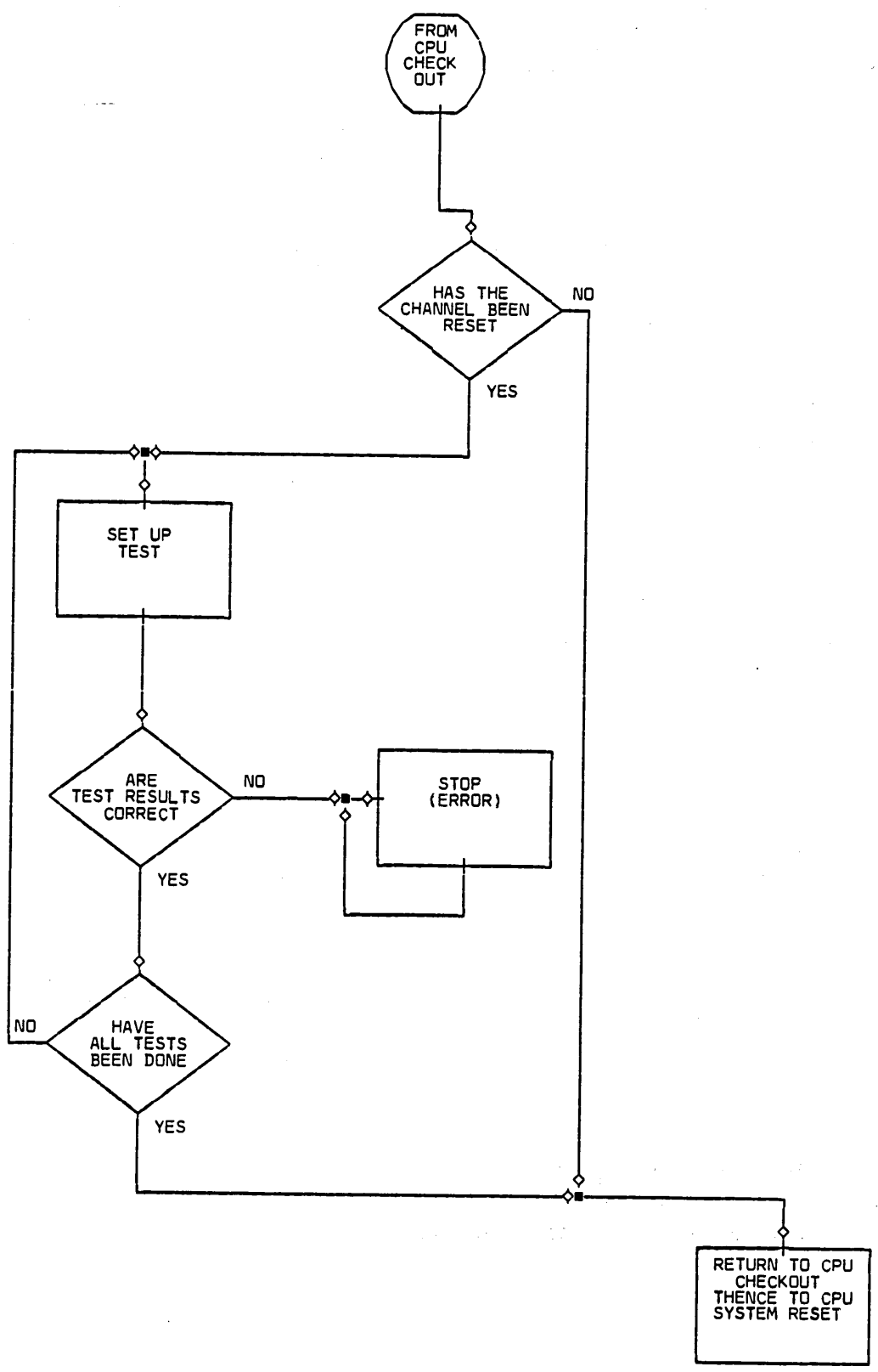


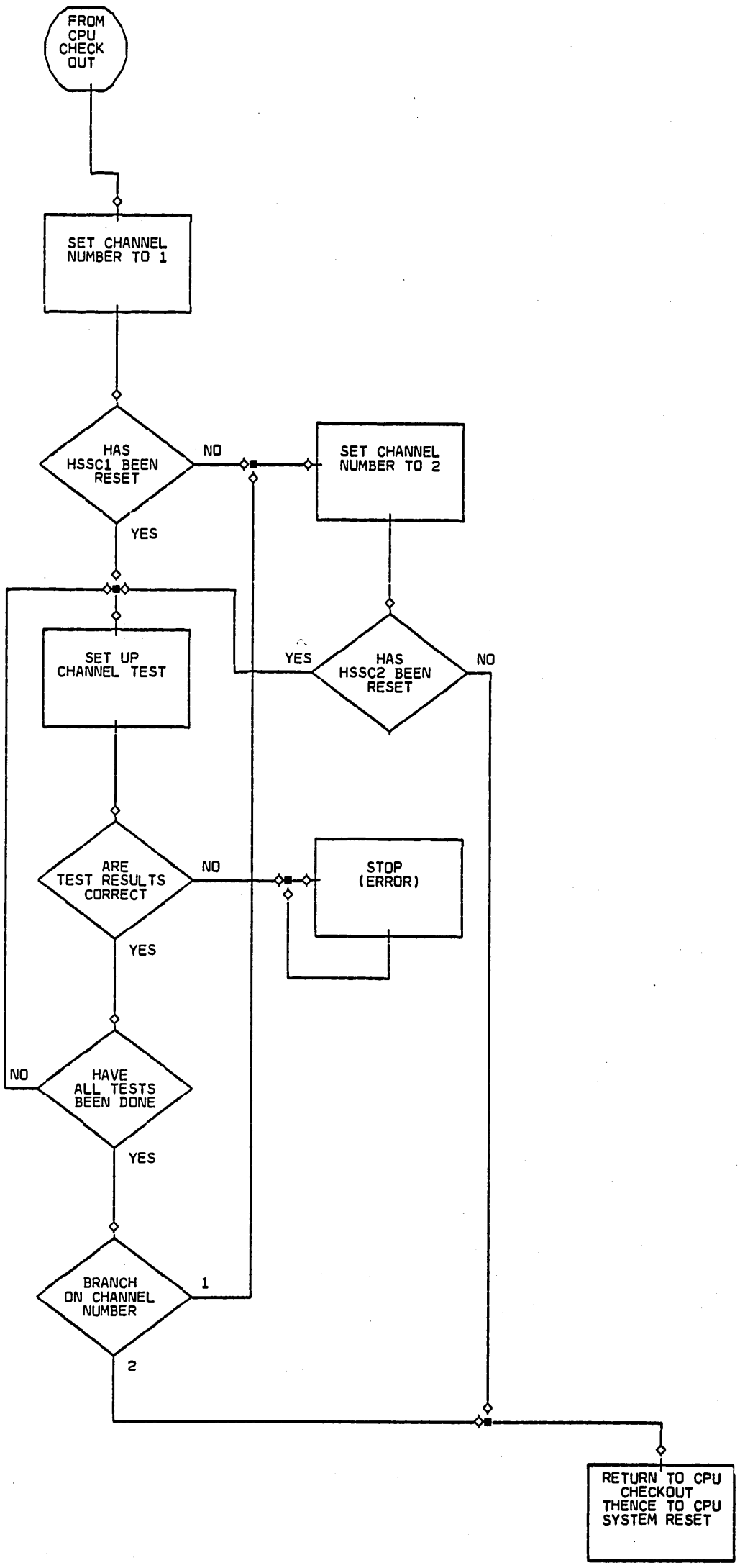
- LOAD - IPL CHECKPOINTS FOR MPX CHANNEL

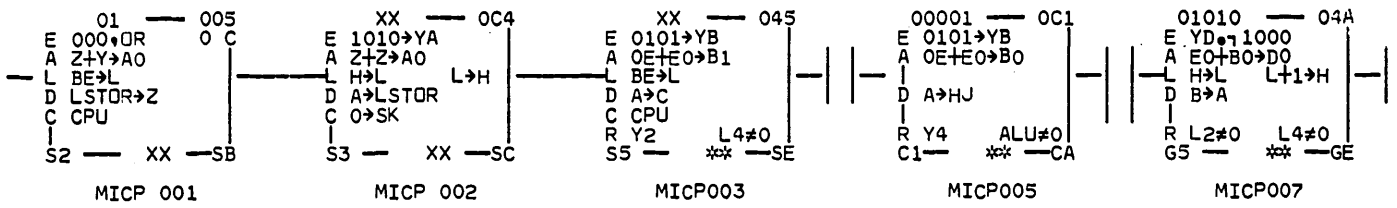


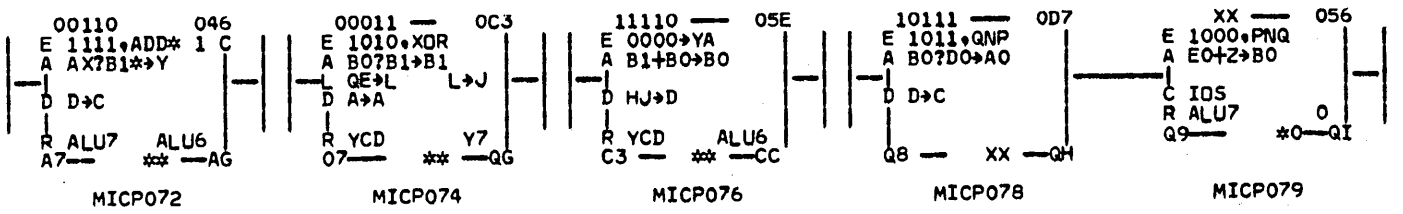
- NOTES -

VERSION(000) - BASIC SYSTEM - MPX ONLY
VERSION(043) - FIRST SELECTOR CHANNEL
VERSION(044) - FIRST AND SECOND SELECTOR CHANNELS

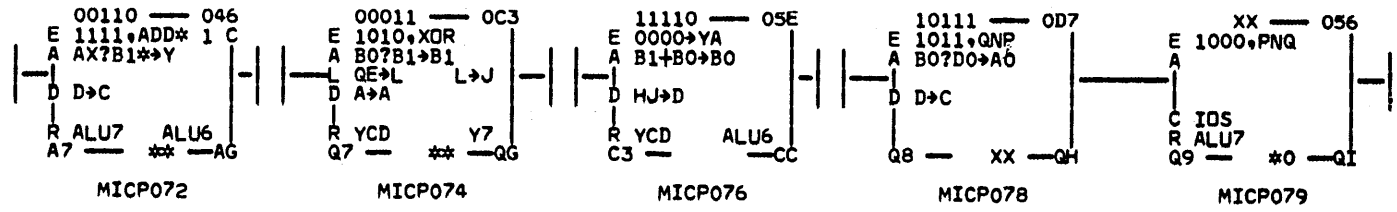

FROM CPU CHECK OUT
HAS THE CHANNEL BEEN RESET
NO
YES
SET UP TEST
ARE TEST RESULTS CORRECT
NO
STOP (ERROR)
YES
NO
HAVE ALL TESTS BEEN DONE
YES
RETURN TO CPU CHECKOUT THENCE TO CPU SYSTEM RESET

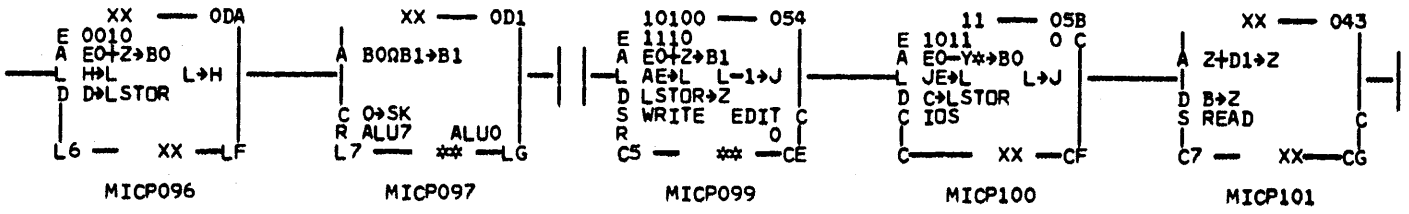

FROM CPU CHECK OUT
SET CHANNEL NUMBER TO 1
HAS HSSC1 BEEN RESET
NO
SET CHANNEL NUMBER TO 2
YES
SET UP CHANNEL TEST
YES
HAS HSSC2 BEEN RESET
NO
ARE TEST RESULTS CORRECT
NO
STOP (ERROR)
YES
NO
HAVE ALL TESTS BEEN DONE
YES
BRANCH ON CHANNEL NUMBER
1
2
RETURN TO CPU CHECKOUT THENCE TO CPU SYSTEM RESET

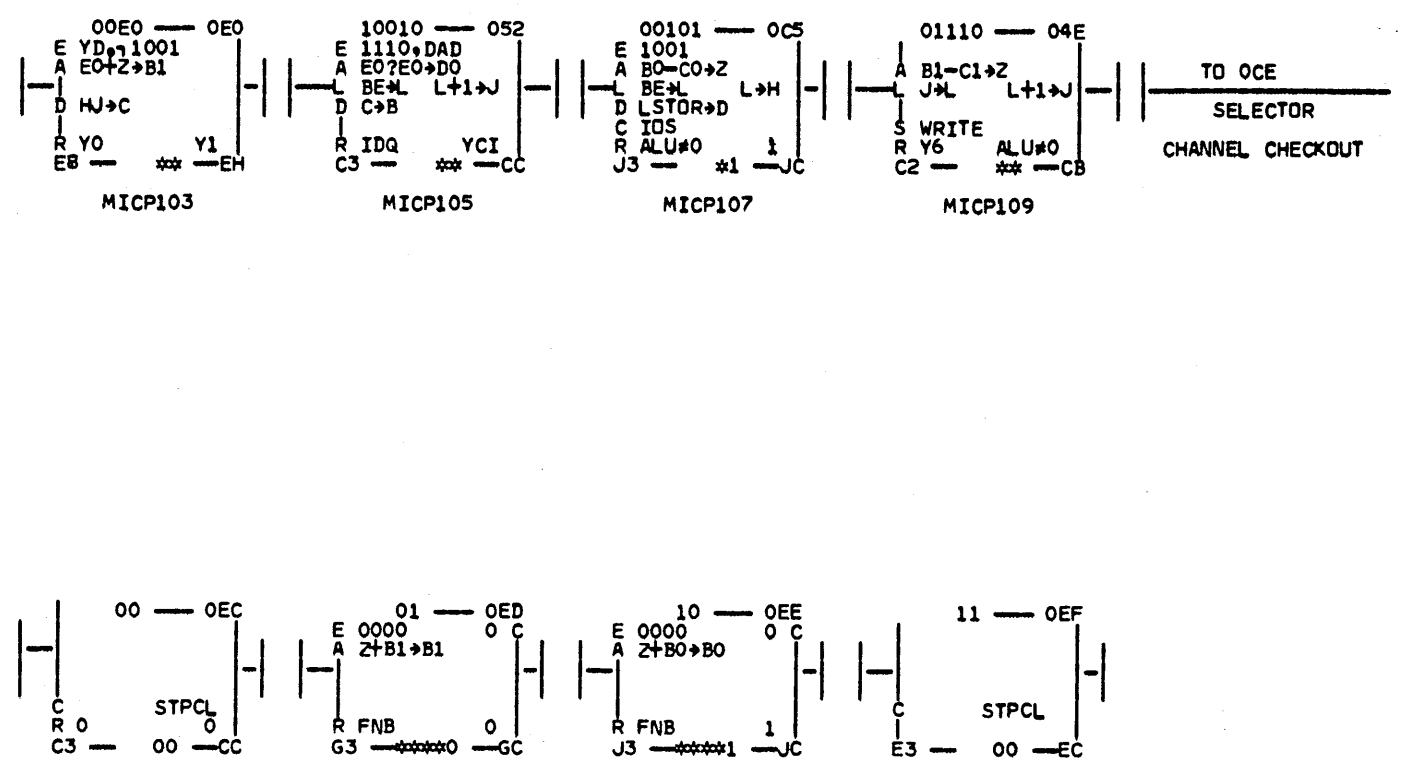

01 005
E 000,OR 0 C
A Z+Y→AO
L BE→L
D LSTOR→Z
C CPU
S2 XX SB
MICP 001
XX 0C4
E 1010→YA
A Z+Z→AO
L H→L L→H
D A→LSTOR
C 0→SK
S3 XX SC
MICP 002
XX 045
E 0101→YB
A 0E+E0→B1
L BE→L
D A→C
C CPU
R Y2 L4≠0
S5 ** SE
MICP003
00001 0C1
E 0101→YB
A 0E+E0→B0
D A→HJ
R Y4 ALU≠0
C1 ** CA
MICP005
01010 04A
E YD,¬1000
A E0+B0→D0
L H→L L+1→H
D B→A
R L2≠0 L4≠0
G5 ** GE
MICP007
00000 0C0
E 1111,ADD* 0 C
A 0E?0E*→B0
L H→L L+1→H
D
I
R Y0 Y1
G1 ** GA
MIP009
11111 05F
E 1111
A 0E?0E→C0
L H→L L-1→H
D A→B
C SWEA
R 0 Y3
L5 0* LE
MICP011
11110 0DE
E 1111 0 C
A 0E?C0→C1
D HJ→A
C IOS
R ALU7 YCD
J1 ** JA
MICP013
01011 04B
E 1001→YD
A E0+D0→A1
L BE→L L→H
D B→B
R ALU≠0 Y7
J5 ** JE
MICP015
11011 0DB
E 1111,ADD* 1 C
A Z+C0*→C0
L J→L L+1→J
D B→B
S READ
E8 XX EH
MICP017
XX 0E1
E YA0000
A Z?C1→C1
L J→L L+1→J
D B→B
C CPU EDIT
R 1
E9 ** EI
MICP018
11 0FF
E 0000,OR
A Z?C0→B0
D A→B
S WRITE
R IDQ YCD
J2 ** JB
MICP019
01100 04C
E YE,¬0000
A A0+C1→Y
D HJ→D
C
YCD Y3
A2 ** AB
MICP021
00111 0C7
E 1001→YB
A E0?Z→B0
L H→L L→H
D LSTOR→Z
R ALU≠0 YCI
Q2 ** QB
MICP023
10011 053
E 1001→YA
A E0+0E→D0
L H→L L→H
D A→LSTOR
R Y4 Y7
E5 ** EE
MICP025
10011 0D3
E 1010
A E0+D0→D0
L J→L L-2→J
D Z→B
R L2≠0 Y5
Q3 ** QC
MICP027
00001 041
E 1110,DAD
A Z?D0→B0
D HJ→C
R Y2 YCD
E2 ** EB
MICP029
00110 0C6
A A0?C0→Z
D D→HJ
R ASCII ALU6
N3 ** NC
MICP031
00111 047
E 1001,Q
A B0?E0→C0
L H→L L→H
D LSTOR→A
R YCD Y5
E3 ** EC
MICP033
10010 0D2
E 0101→YB 0 C
A 0E+E0→C1
D B→HJ
C SWEA
N4 0X ND
MICP035
0X 0D5
F 0101→YB
A 0E+E0→C0
L H→L L+1→A
D B→B
C CPU
R ASCII 1
N5 *1 NE
MICP036
01 055
E 1111,ADD
A E0+C0→Z
L QE→L L→J
D C→D
R ALU7 YCD
N6 ** NF
MICP037
01011 0CB
E 0010
A Z+E0→Z
D D→B
C EDIT
R 0
Q6 ** QF
MICP039
00 0FC
E 0110
A B0-C1→B0
L AE→L L→H
D B→A
R Y6 ALU≠0
Q7 ** QG
MICP040
01010 0CA
E 1111→YB
A B1-C0→C1
D HJ→B
R ALU≠0 Y5
N2 ** NB
MICP042
11100 05C
E 1111→YA
A E0?Z*→A0
D HJ→D
C CPU
R Y6 ALU≠0
C2 ** CB
MICP044
01001 0C9
E 1000,PNQ
A A0?C1→D0
L J→L L-1→J
D C→C
C SWEA
Q4 0X QD
MICP046
0X 0E9
E YB,¬1001
A Z+B0*→C0
D D→HJ
R IZT ALU0
Q5 ** QE
MICP047
01001 049
E YA,¬1001
A Z+C0*→A0
L H→L L+1→H
D D→B
C 0→SK
R IZT Y7
E4 ** ED
MICP049
01100 0CC
E 1000→YB
A A0?Z→B0
L BE→L L→J
D HJ→D
C IOS
N5 XX NE
MICP051
XX 04D
A Z+B1→Z
D B→C
C CPU
R MINUS ALU≠0
N6 ** NF
MICP052
11111 0DF
E 1100,RSH* 1
A Z?0E*→B0
L QE→L L→H
D A→A
R Y4 Y7
Q2 ** QB
MICP054
11101 05D
A Z+B0→D0
D HJ→C
C CPU
R 1 Y1
J3 1* JC
MICP056
11101 0DD
E 1101,LSH
A Z?B0→B1
L JE→L L→J
D C→A
C
R ALU7 Q0≠0
Q3 ** QC
MICP058
11000 058
E 0111,SUP 0 C
A B1?C0→D1
L J→L L-1→J
D Z→Z
R MINUS ALU≠0
C2 ** CB
MICP060
11000 0D8
E 1101,LSH 0 C
A Z?C1→B0
L QE→L L→H
D B→C
R Y4 QPTY
N2 ** NB
MICP062
01111 04F
E 0000→YB
A B0+B0→B1
D B→D
R OXPTO ALU0
E5 ** EE
MICP064
01111 0CF
E 1001,Q 1 C
A B0?CX→AX
D HJ→B
R Y2 Q0≠0
Q4 ** QD
MICP066
11001 059
E 1010,XOR
A B1?B0→CX
L QE→L L→H
D B→D
R 1 L4≠0
J2 1* JB
MICP068
11001 0D9
E 1110,DAD* 1 C
A A1?B1*→D0
D C→A
R Y0 Q0≠0
Q5 ** QE
MICP070


00110 046
E 1111.ADD* 1 C
A AX7B1*→Y
D D→C
R ALU7 ALU6
A7 ** AG
MICP072
00011 0C3
E 1010.XOR
A B0?B1→B1
L QE→L L→J
D A→A
R YCD Y7
07 ** QG
MICP074
11110 05E
E 0000→YA
A B1+B0→B0
D HJ→D
R YCD ALU6
C3 ** CC
MICP076
10111 0D7
E 1011.QNP
A B0?D0→A0
D D→C
Q8 XX QH
MICP078
XX 056
E 1000.PNQ
A E0+Z→B0
C IOS
R ALU7 0
Q9 *0 QI
MICP079
10110 0D6
E 0110.DSP 0 C
A A0?B0→B1
N3 XX NC
MICP081
XX 0D4
E 0101.AND
A B0?Y→D0
C CPU
R ALU≠0 Y7
N4 ** ND
MICP082
01000 048
E 0010.DSQ
A B0?B1→C0
C IOS
C4 XX CD
MICP084
XX 0C8
E 0011.SUQ
A A0?C0→D1
D HJ→A
R 1 ALU≠0
C5 1* CE
MICP085
10001 051
E 0100.P 0 C
A B0?Y→C0
D B→D
C CPU
R FXPTO YCD
E4 ** ED
MICP087
10000 0D0
E 1110.DAD
A B0?C0→C0
L BE→L
D A→B
R L2≠0 0
N7 *0 NG
MICP089
10111 057
E 0110→YA
A E0+C0→C1
D C+D
R FXPTO YCI
E6 ** EF
MICP091
01101 0CD
E 0111
A E0+0E→C1
D Z→A
C IOS
L3 XX LC
MICP093
XX 0E2
E 1001→YB
A Z+C1→C0
L BE→L L→H
D C→C
S READ
L4 XX LD
MICP094
XX 0E3
E YDQ1000
A E0+Z→B1
L H→L L→H
D LSTOR→Z
C CPU
L5 XX LE
MICP095
XX 0DA
E 0010
A E0+Z→B0
L H→L
D D→LSTOR
L6 XX LF
MICP096
XX 0D1
A B0ΩB1→B1
C 0→SK
R ALU7 ALU0
L7 ** LG
MICP097
10100 054
E 11100
A E0+Z→B1
L AE→L L-1→J
D LSTOR→Z
S WRITE EDIT
R 0
C5 ** CE
MICP099
11 05B
E 1010 0 C
A E0-Y*→B0
L JE→L L→J
D C→LSTOR
C IOS
C6 XX CF
MICP100
XX 043
A Z+D1→Z
D B→Z
S READ UNDUMP C
C7 XX CG
MICP101
.00E0 0E0
E YD.1001
A E0+Z→B1
D HJ→C
R YD Y1
E8 ** EH
MICP103
10010 052
E 1110.DAD
A E0?E0→D0
L BE→L L+1→J
D C→B
R IDQ YCI
C3 ** CC
MICP105
00101 0C5
E 1001
A B0-C0→Z
L BE→L L→H
D LSTOR→D
C IOS
R ALU≠0 1
J3 *1 JC
MICP107
01110 04E
A B1-C1→Z
L J→L L+1→J
S WRITE
R Y6 ALU≠0
C2 ** CB
MICP109
01110 0CE
E 0001→YA
A E0+Z→B1
L J→L L→J
D LSTOR→A
C CPU SWEA
R 0
Q1 0X QA
MICP111
0X 0FD
E 0000→YD
A A0+Z→B0
L H→L L→H
D LSTOR→D
Q6 XX QF
MICP112
XX 0FE
E 001.ACK
A A0?D0→Z
C CPU
R 0 QPTY
Q7 0* QG
MICP113
EXIT TO SYSTEM RESET
VIA 0ED
00 0EC
C
R 0 STPCL
C3 00 CC
01 0ED
E 0000 0 C
A Z+B1→B1
R FNB 0
G3 **** 0 GC
10 0EE
E 0000 0 C
A Z+B0→B0
R FNB 1
J3 ****1 JC
11 0EF
C STPCL
E3 00 EC
00 07C
E 0000 0 C
A Z+C0→C0
R FNB 0
L7 ****0 LG
01 07D
C STPCL
J7 01 JG
10 07E
C STPCL
R 0 1
G7 01 GG
11 07F
E 0000 0 C
A Z+D0→D0
R FNB 1
E7 ****1 EG

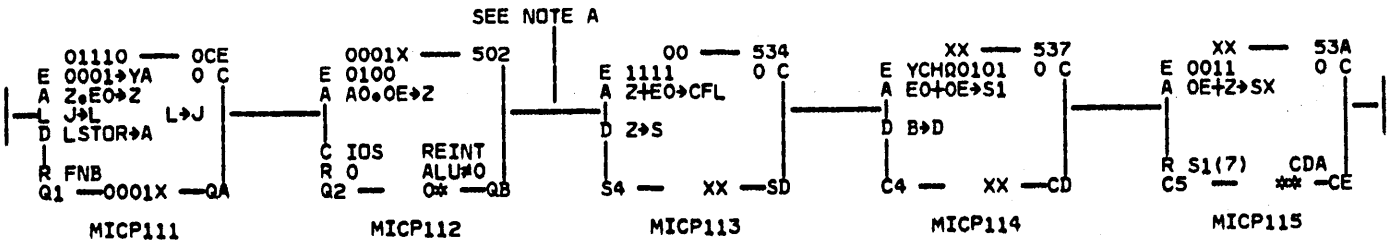
RUN 17 JAN 66


00110 046
E 1111.ADD* 1 C
A AX?B1*→Y
D D→C
R ALU7 ALU6
A7 ** AG
MICP072
00011 0C3
E 1010.XOR
A B0?B1→B1
L QE→L L→J
D A→A
R YCD Y7
Q7 ** QG
MICP074
11110 05E
E 0000→YA
A B1+B0→B0
D HJ→D
R YCD ALU6
C3 CC
MICP076
10111 0D7
E 1011.QNP
A B0?D0→A0
D D→C
Q8 XX QH
MICP078
XX 056
E 1000.PNQ
A
C IOS
R ALU7
Q9 *0 QI
MICP079
10110 0D6
E 0110.DSP 0 C
A A0?B0→B1
N3 XX NC
MICP081
XX 0D4
E 0101.AND
A B0?Y→D0
C CPU
R ALU≠0 Y7
N4 ** ND
MICP082
01000 048
E 0010.DSQ
A B0?B1→C0
C IOS
C4 XX CD
MICP084
XX 0C8
E 0011.SUQ
A A0?C0→D1
D HJ→A
R 1 ALU≠0
C5 1* CE
MICP085
10001 051
E 0100.P 0 C
A B0?Y→C0
D B→D
C CPU
R FXPTO YCD
E4 ** ED
MICP087
10000 0D0
E 1110.DAD
A B0?C0→C0
L BE→L
D A→B
R 0
N7 *0 NG
MICP089
10111 057
E 0110→YA
A E0+C0→C1
D C→D
R FXPTO YCI
E6 ** EF
MICP091
01101 0CD
E 0111
A E0+0E→C1
D Z→A
IOS
L3 XX LC
MICP093
XX 0E2
E 1001→YD
A Z+C1→C0
L BE→L L→H
D C→C
S READ
L4 XX LD
MICP094
XX 0E3
E YDQ1000
A E0+Z→B1
L H→L L→H
D LSTOR→Z
C CPU
L5 XX LE
MICP095

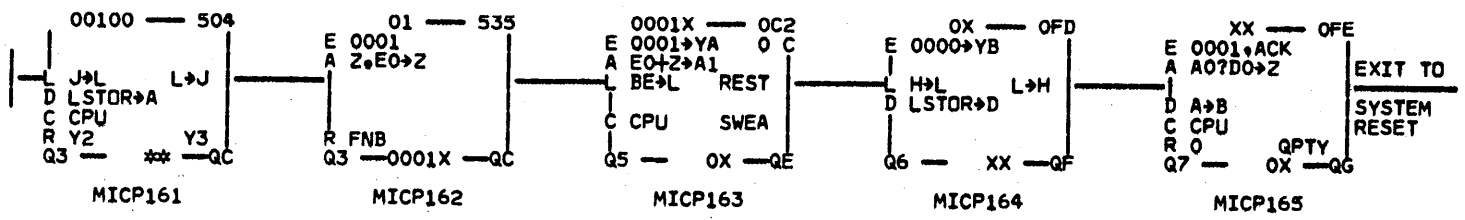

XX 0DA
E 0010
A E0+Z→B0
L H→L L→H
D D→LSTOR
L6 XX LF
MICP096
XX 0D1
A B0ΩB1→B1
C 0→SK
R ALU7 ALU0
L7 ** LG
MICP097
10100 054
E 1110
A E0+Z→B1
L AE→L L-1→J
D LSTOR→Z
S WRITE EDIT C
R 0
C5 ** CE
MICP099
11 05B
E 1011 0 C
A E0-Y*→B0
L JE→L L→J
D C→LSTOR
C IOS
C XX CF
MICP100
XX 043
A Z+D1→Z
D B→Z
S READ C
C7 XX CG
MICP101
00E0 0E0
E YDQ1001
A E0+Z→B1
D HJ→C
R Y0 Y1
E8 ** EH
MICP103
10010 052
E 1110.DAD
A E0?E0→D0
L BE→L L+1→J
D C→B
R IDQ YCI
C3 ** CC
MICP105
00101 0C5
E 1001
A B0-C0→Z
L BE→L L→H
D LSTOR→D
C IOS
R ALU≠0 1
J3 *1 JC
MICP107
01110 04E
A B1-C1→Z
L J→L L+1→J
S WRITE
R Y6 ALU≠0
C2 ** CB
MICP109
TO 0CE
SELECTOR
CHANNEL CHECKOUT


00 0EC
C
R 0 STPCL 0
C3 00 CC
01 0ED
E 0000 0 C
A Z+B1→B1
R FNB 0
G3 ****0 GC
10 0EE
E 0000 0 C
A Z+B0→B0
R FNB 1
J3 ****1 JC
11 0EF
C
STPCL
E3 00 EC
00 07C
E 0000 0 C
A Z+C0→C0
R FNB 0
L7 ****0 LG
01 07D
C
STPCL
J7 01 JG
10 07E
C
R0 STPCL 1
G7 01 GG
11 07F
E 0000 0 C
A Z+D0→D0
R FNB 1
E7 ****1 EG

RUN 17 JAN 66

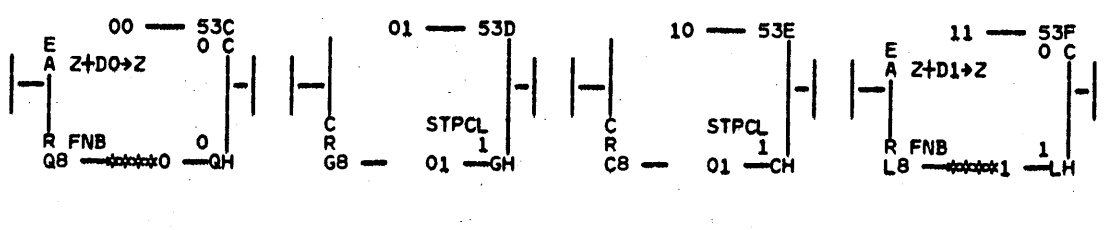

SEE NOTE A
01110 OCE
E 0001→YA 0 C
A Z.E0→Z
L J→L L→J
D LSTOR→A
R FNB
Q1 0001X QA
MICP111
0001X 502
E 0100
A A0.0E→Z
C IOS REINT
R 0 ALU≠0
Q2 0* QB
MICP112
00 534
E 1111 0 C
A Z+E0→CFL
D Z→S
S4 XX SD
MICP113
XX 537
E YCH.Q0101 0 C
A E0+0E→S1
D B→D
C4 XX CD
MICP114
XX 53A
E 0011 0 C
A 0E+Z→SX
R S1(7) CDA
C5 ** CE
MICP115
01111 50F
E 1010 0 C
A E0+0E→S0
D S→C
E3 XX EC
MICP117
XX 521
E YCH.¬0100 1 C
A 0E-CX.D0
D S→C
E4 XX ED
MMICP118
XX 516
E 0000 0 C
A S0-C0→S0
L J→L L→J
D A→LSTOR
E5 XX EE
MICP119
XX 513
A A0.D0→CFL
D S→D
R ALU≠0 YCH1
E6 ** EF
MICP120
10100 514
E YCH.¬1111 0 C
A Z+D0→W4
D D→C
G3 XX GC
MICP122
XX 510
E 0 C
A S1-C1→A1
D B→S
G4 XX GD
MICP123
XX 508
E 0 C
A W0-C0→D0
D D→W34
R ALU≠0 CDA
G5 ** GE
MICP124
00000 500
E 0 C
A B0+Z→T0
D HJ→D
J3 XX JC
MICP126
XX 539
E YCH.Q0001 0 C
A A1+Z→CFL
D W01→B
R YCH3 ALU≠0
J4 ** JD
MICP127
00110 506
E 1 C
A B0+B1→D1
D S→C
R YCH3 YCD
L3 ** LC
MICP129
00001 501
E 1001 0 C
A E0+0E→T1
N3 XX NC
MICP131
XX 51B
E YCH.Q0100 0 C
A T0+Z→D0
D HJ→W34
N4 XX ND
MICP132
XX 51A
E 0 C
A T1+D0→D1
D HJ→S
R YCD YCH1
N5 ** NE
MICP133
00011 503
E 1 C
A Z+Z→S0
D B→W34
Q3 XX QC
MICP135
XX 519
E 0001 0 C
A B1+E0→S1
D C→D
C 0→SK
R S1(7) CDA
Q4 ** QD
MICP136
01110 50E
E YCH.¬11110 C
A T1+Z→W4
D B→A
S READ
A3 XX AC
MICP138
XX 533
E 0101 0 C
A E0+Z→A0
D W34→B
A4 XX AD
MICP139
XX 532
E 0000 0 C
A B0+B1→T1
D B→W34
S WRITE
A5 XX AE
MICP140
XX 538
E 0011 0 C
A CSB+E0*→Z
D A→D
R YCH3 ALU≠0
A6 ** AF
MICP141
01010 50A
E 0011 0 C
A T1+0E*→S1
D W01→B
RALU7 YCD
C3 ** CC
MICP143
01011 50B
E 1000 0 C
A E0+0E→CFL
D HJ→L
E3 XX EC
MICP145
XX 549
E YCH.Q0010 0 C
A A0-B0→A1
D S→D
E4 XX ED
MICP146
XX 509
E 1100 0 C
A E0+0E→S1
D W2→C
R S1(7) ALU≠0
E5 ** EE
MICP147
00101 505
A A1.B1→Z
D C→D
C 0→SK
R ALU≠0 YCH1
G3 ** GC
MICP149
10010 512
E 1111 0 C
A S1+E0*→D0
D W01→B
J3 XX JC
MICP151
XX 507
E 1010 0 C
A CSB-E0→CFL
R S1(7) ALU≠0
J4 ** JD
MICP152
11000 518
E 0000 0 C
A B0+B1→A0
D T→B
L3 XX LC
MICP154
XX 52F
E 1111 0 C
A A0-0E*→Z
D A→D
R ALU≠0 CDA
L4 ** LD
MICP155
11110 51E
E 0010 0 C
A E0+0E→D0
D Z→S
N3 XX NC
MICP157
XX 52E
E 0000 0 C
A B1-B0→A1
D B→A
N4 XX ND
MICP158
XX 51F
E 0000 0 C
A A1-B0→Z
D A→B
C CL-CH
R ALU≠0
N5 0* NE
MICP159

RUN 17 JAN 66



THESE THREE MICROINSTRUCTIONS ARE THE THREE FINAL CYCLES OF CPU CHECKOUT

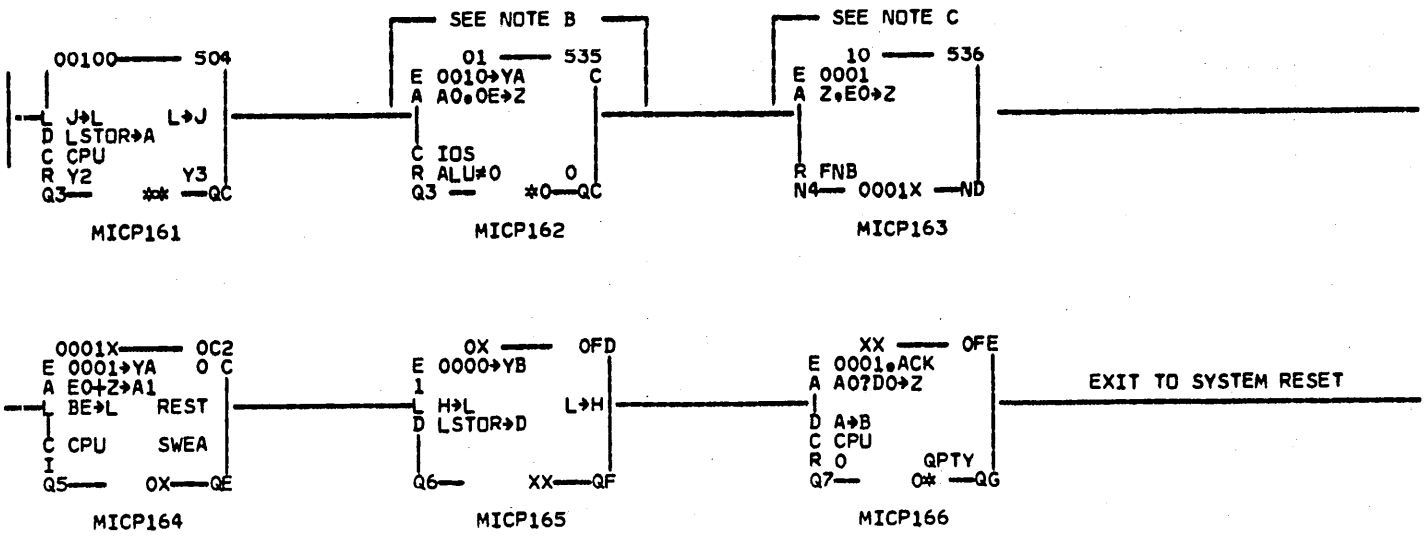
TEST MICROINSTRUCTIONS



NOTE A

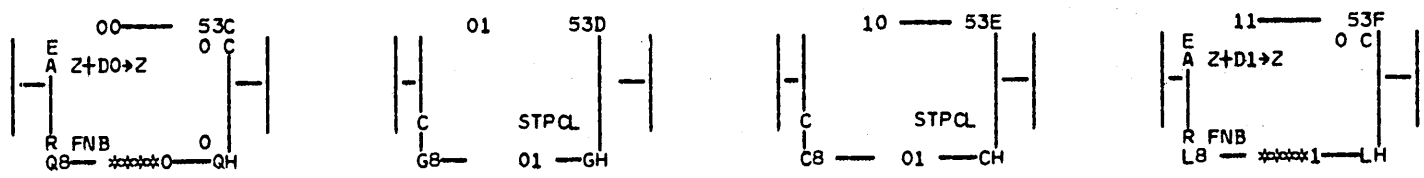
IF THE CHANNEL HAS NOT BEEN RESET, 502 BRANCHES TO 535 (MICP162) INSTEAD OF 534 AND THE CHANNEL CHECKOUT IS NOT EXECUTED.

RUN 17 JAN 66



THESE THREE MICROINSTRUCTIONS ARE THE THREE FINAL CYCLES OF CPU CHECKOUT

TEST MICROINSTRUCTIONS



NOTE A

IF HSSC1 HAS NOT BEEN RESET, 502 BRANCHES TO 535 INSTEAD OF 534 AND HSSC1 WILL NOT BE CHECKED OUT. FURTHER, IF HSSC2 HAS NOT BEEN RESET EITHER, BRANCHING WILL OCCUR FROM 535 TO 536 , THENCE TO EXIT SO THAT HSSC2 WILL NOT BE CHECKED OUT. IF HSSC2 HAS BEEN RESET, 535 WILL BRANCH TO 534 AND HSSC2 WILL BE CHECKED OUT.

NOTE B

IF HSSC2 HAS JUST BEEN CHECKED OUT, 504 WILL BRANCH DIRECTLY TO 536 AND THENCE TO EXIT.

NOTE C

IF HSSC2 HAS BEEN RESET, BRANCHING FROM 535 BACK TO 534 WILL OCCUR AND HSSC2 WILL BE CHECKED OUT (SEE NOTE A). OTHERWISE, SEQUENCING WILL LEAD TO 536 AND EXIT.

RUN 17 JAN 66

STOP AT 0EC OR 0EF

C REG.	D REG.	A REG.	B REG.	LAST ROS ADDRESS IN HEX.	SIMULATION PAGE NUMBER
00000	0000	00000	5555	0C1	5.
004EB	F0EB	00455	E0EB	0DF	54.
01938	1938	3E0C0	C7FF	0C3	74.
03900	3902	00165	3900	0C6	31.
05500	5555	05555	46EB	0CA	42.
05555	D500	05555	FF55	0C0	9.
06000	FFEB	0FF55	46EB	0E9	47.
07777	XXXX	00000	1090	0E0	103
07777	XXXX	00000	20A0	0D1	97.
07777	XXXX	00000	7777	0C5	107.
099E0	0000	00000	0000	0FE	165.
0B8A6	00A6	038C0	8042	0D4	82.
0C038	E0EB	0C038	E0C0	0DD	58.
0E0C0	70C0	0C038	C738	0CF	66.
0E0C0	E000	0C038	70C0	0D8	62.
0FFFF	D500	00100	5555	0DE	13.
100FF	3902	00165	0000	0D3	27.
100FF	3902	00165	9065	0C7	23.
100FF	5555	00165	0065	0FD	19.
160A6	8042	0B8A6	B8A6	0D0	89.
338A6	0000	0B8A6	8042	0C8	85.
3E0C0	1938	3E0C0	C738	0D9	70.

STOP AT 07D OR 07E

C REG.	D REG.	A REG.	B REG.	LAST ROS ADDRESS IN HEX.	SIMULATION PAGE NUMBER
00000	0000	00000	XX55	045	3.
00000	D500	05555	5555	04A	7.
004EB	F0EB	00455	04EB	04D	52.
01938	1938	3E0C0	C738	046	72.
01938	B8A6	3E0C0	C6FF	05E	76.
03900	3902	00165	3900	041	29.
05500	46EB	0FF55	46EB	05C	44.
05555	5555	00165	5555	055	37.
05555	5555	05555	0055	0FC	40.
06000	FFEB	00455	FFEB	049	49.
07777	XXXX	00000	7777	052	105.
07777	XXXX	00000	7777	04E	109.
080A6	8042	0B8A6	8042	051	87.
09000	3902	00165	3900	047	33.
0B8A6	B8A6	038C0	80FF	056	79.
0C038	E000	0C038	E0C0	058	60.
0C038	E0EB	00455	E0EB	05D	56.
0E0C0	70C0	0C038	70E0	04F	64.
0FFD5	D500	05555	5555	05F	11.
0FFFF	D500	00165	5555	04B	15.
100FF	3902	00165	0065	04C	21.
100FF	9902	00165	9065	053	25.
160C0	60A6	0B8A6	B8A6	057	91.
3E0C0	C738	0C038	C738	059	68.

STOP AT 53D OR 53E

A REGISTER	B REGISTER	C REGISTER	D REGISTER	S REGISTER	T REGISTER	LAST ROS ADDR (HEX)	MSC PAGE NUMBER
0.XX.XX	77.77	0.77.10	77.77	3.00.55	00.00	53A	115
0.00.00	77.77	0.AA.55	AA.55	0.AA.55	00.00	513	120
0.00.00	77.77	0.AA.55	00.55	0.77.77	00.00	508	124
0.00.00	AA.55	0.AA.55	39.00	0.77.77	77.00	539	127
0.00.00	AA.55	0.77.77	39.00	0.77.77	77.00	506	129
0.00.00	AA.55	0.77.77	77.10	0.39.00	77.99	51A	133
0.00.00	AA.55	0.77.77	77.77	0.01.65	77.99	519	136
0.50.55	55.99	0.77.77	50.55	0.01.65	77.EE	538	141
0.50.55	39.00	0.77.77	50.55	0.01.21	77.EE	50A	143
0.39.00	39.00	0.99.E0	01.21	0.01.CC	77.EE	509	147
0.39.00	39.00	0.99.E0	99.E0	0.01.CC	77.EE	505	149
0.39.00	AA.55	0.99.E0	CC.E0	0.01.CC	77.EE	507	152
0.FF.00	77.EE	0.99.E0	FF.00	0.01.CC	77.EE	52F	155
0.77.77	77.77	0.99.E0	22.00	0.00.00	77.EE	51F	159

WHEN TWO CHANNELS ARE INSTALLED. THE CHANNEL WHICH IS BEING CHECKED OUT CAN BE IDENTIFIED AS FOLLOWS

CHANNEL 1 BEING CHECKED OUT GENERAL PURPOSE STAT Y3 = 1. Y2 = 0

CHANNEL 2 BEING CHECKED OUT GENERAL PURPOSE STAT Y3 = 0. Y2 = 1

A CHANNEL WHICH HAS BEEN RESET. AND WHICH IS THEREFORE TO BE CHECKED OUT BY THE MICROPROGRAM. MAY BE IDENTIFIED FROM THE CONTENTS OF LOCAL STORAGE LOCATION 0 BYTE 0 AS FOLLOWS

CHANNEL 1 RESET. BIT 5 = 0 (1 IF NOT RESET).

CHANNEL 2 RESET. BIT 6 = 0 (1 IF NOT RESET).

THIS STATE IS NOT DISTURBED BY THE CHECKOUT MICROPROGRAM.

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SENSE LATCHES			
A0	A1	A2	A3
0	0	1	1
B0	B1	B2	B3
0	0	0	0
C0	C1	C2	C3
0	0	0	0
D0	D1	E0	E1
1	0	0	0
E2	E3	F0	G0
0	0	1	1
G1	H0	H1	H2
1	1	1	1
H3	H4	J0	J1
0	1	1	1
J2	K0	L0	L1
0	0	0	0
L2	M0	M1	M2
0	0	0	1
M3	N0	N1	N2
0	1	1	1
N3	P0	P1	P2
1	0	0	0
Q0	Q1	Q2	Q3
1	0	1	0
R0	R1	R2	S0
1	0	1	1
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
X	X	X	X
D0	D1	E0	E1
X	X	X	X
E2	E3		
X	X		
		L0	L1
		X	X
L2	M0	M1	M2
X	X	X	X
M3	N0	N1	N2
X	X	X	X
N3			
X			

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	X	X	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
P XXXXX	X	P XXX	P XXXX

EARLY B COND	INCREMENT CONTROL	-1	-2	+1	EARLY C COND
X		X	X	X	X
	DESTINATION	H	J	O	
		X	X	X	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
X	X	X	X

READ	SECOND MS CYCLE	WRITE
X	X	X

EXT MASK	HALT
X	X

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	X	X	X	X

STATS-		YA	YB	YD	YE
	P	X00X	XXXX	XXX	1 XX

ALU CONT.		SKEW SELECT		ALU BIN OUT
P XXXX	X	P XXXX	XXXX	XXXX XXXX

LSAR REGISTER		ROBAR	
P XXXX	XXXX	P X XXXX	XXXX XXXX
H REGISTER		ROAR	
P XXXX	XXXX	1 0 0000	0000 0101
J REGISTER		ROSCAR	
P XXXX	XXXX	X X XXXX	XXXX XXXX

R REGISTER		
P XXX	P XXXX XXXX	P XXXX XXXX

A REGISTER

1 000 1 0000 0000 1 0000 0000

S REGISTER		
P XXX	P XXXX XXXX	P XXXX XXXX

B REGISTER		
	P XXXX XXXX	P XXXX XXXX

C REGISTER		
P XXX	P XXXX XXXX	P XXXX XXXX

D REGISTER		
	1 0000 0000	1 0000 0000

EX REG	P REGISTER	Q REGISTER
P XXX	P XXXX XXXX	P XXXX XXXX

	CHECKS	IF REGISTER
	P XXXX XXXX	P XXXX XXXX

	INTERFACE CONTROLS	
	XXXX XXXX	XXXX XXXX

	CHANNEL CONTROLS	
XXX	XXXX XXXX	XXXX XXXX

CHANNEL DISPLAY

	T0	T1
P	XXXX XXXX	P XXXX XXXX
	W0	W1
X	XXXX XXXX	X XXXX XXXX
	W2	
X	XXXX XXXX	P XXXX XXXX
	W3	W4
X	XXXX XXXX	X XXXX XXXX

SP	-DATA	-KEY
	1 0000	0000

SYSTEM RESET HARDWARE CYCLE

DESCRIPTIVE NOTES

THE INITIAL MACHINE STATUS IS SHOWN ABOVE.
IT RESULTS FROM EITHER PERFORMING HARDWARE SYSTEM RESET, OR FROM EXECUTING THE LOG-OUT MICROPROGRAM.
THE Y STATS WILL BE SET AS FOLLOWS TO INDICATE THE METHOD OF ENTRY.

1. HARDWARE SYSTEM RESET CAUSED BY

   A. DEPRESSION OF SYSTEM RESET BUTTON
      YA =0000, YB =0000, HALT LATCH =1

   B. DEPRESSION OF LOAD BUTTON
      YA =0000, YB =0000, LOAD STAT (Y15) =1

   C. DEPRESSION OF START BUTTON WITH DIAGNOSTIC SELECT SWITCH SET TO CPU POSITION
      YA =1001, YB =0000

2. FOLLOWING A LOG-OUT
      YA =0000, YB =XXX1
      Y4, Y5, Y6 ARE SET TO INDICATE WHICH CHANNELS HAVE BEEN RESET.

NOTE

IF AN INVALID INITIAL STATUS RESULTS FROM THE MEMORY BUSY LATCH FAILING TO RESET, THEN IT MAY BE NECESSARY TO REMOVE POWER TO RESET THIS LATCH.

NOTE 2

ALL FOLLOWING CHARTS ASSUME ENTRY TO THE CHECKOUT PROGRAM BY DEPRESSION OF THE SYSTEM RESET BUTTON.

SENSE LATCHES	CONTROL LATCHES
A0 A1 A2 A3 0 0 0 1	
B0 B1 B2 B3 0 0 0 0	B0 B1 B2 B3 0 0 0 0
C0 C1 C2 C3 0 0 0 1	
D0 D1 E0 E1 1 0 1 0	D0 D1 E0 E1 1 0 0 0
E2 E3 F0 G0 1 0 0 1	E2 E3 0 0
G1 H0 H1 H2 1 0 0 0	
H3 H4 J0 J1 1 0 0 0	
J2 K0 L0 L1 1 0 0 0	L0 L1 0 0
L2 M0 M1 M2 1 0 0 1	L2 M0 M1 M2 0 0 0 1
M3 N0 N1 N2 0 0 0 0	M3 N0 N1 N2 0 1 1 1
N3 P0 P1 P2 1 0 0 0	N3 1
Q0 Q1 Q2 Q3 0 0 0 0	
R0 R1 R2 S0 1 1 0 1	
T0 T1 JX PX 0 0 0 0	

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1 -2 +1	EARLY C COND
0	1 0 0	0
	DESTINATION H-J-D: 1 0 0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS-	YA	YB	YD	YE
1	0000	0000	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0000 0000	0001 0000

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 0000 0101
H REGISTER	ROAR
1 0000 0000	0 0 0000 1100 0100
J REGISTER	ROSCAR
P XXXX XXXX	X X XXXX XXXX XXXX

R REGISTER

1 000 1 1111 1111 1 1111 1111

A REGISTER

1 000 1 0000 0000 1 0000 0000

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

P XXXX XXXX P XXXX XXXX

C REGISTER

P XXX P XXXX XXXX P XXXX XXXX

D REGISTER

1 0000 0000 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0000 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX
8

THE Y STATS HAVE BEEN SET UP TO INDICATE WHICH ENTRY WAS MADE INTO THE PROGRAM.
IF THE ENTRY HAS BEEN FROM PUSHING THE LOAD BUTTON, NONE OF Y0-Y7 WILL BE ON, BUT THE LOAD STAT WILL BE ON. THIS STAT WILL SERVE TO DIFFERENTIATE BETWEEN SYSTEM RESET KEY BEING DEPRESSED AND THE LOAD BUTTON BEING DEPRESSED.
THE OTHER ENTRIES, FROM LOGOUT, AND SETTING THE DIAGNOSTIC CONTROL SWITCH TO CPU AND PUSHING THE START KEY, WILL FORCE CERTAIN OF THE Y0-Y7 STATS ON.

THE STATS ARE SAVED IN THE NEXT MICROINSTRUCTION 002 IN LOCAL STORAGE LOCATION 0.
IN THE PRESENT MICROINSTRUCTION THEY ARE MOVED TEMPORARILY INTO THE A0 REGISTER.
THE H REGISTER IS SET TO 00(HEX) AS THE LOCAL STORAGE ADDRESS.
AT THE SAME TIME THE F (ALU FUNCTION) REGISTER, AND THE DIRECT CARRY STAT ARE RESET.
CPU MODE IS ALSO SET ON.

01 — 005
E 0000,OR 0 C
A Z+Y→A0
L BE→L L→H
D LSTOR→Z
C CPU
S2— XX —SB

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
1	1	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
0	1	1	0	0	0	0	0
C0	C1	C2	C3				
0	0	1	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	1	1	0	1	0
E2	E3	F0	G0	E2	E3		
0	1	0	1	1	0		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
1	0	1	1			0	0
L2	M0	M1	M2	L2	M0	M1	M2
0	0	1	1	1	0	0	1
M3	N0	N1	N2	M3	N0	N1	N2
1	0	1	0	0	0	0	0
N3	P0	P1	P2	N3			
0	1	1	1	1			
Q0	Q1	Q2	Q3				
1	0	0	0				
R0	R1	R2	S0				
1	0	1	0				
T0	T1	JX	PX				
0	0	0	0				

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1 -2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-O 1 0 0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS-	YA	YB	YD	YE
1	1010	0000	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0000	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 1100 0100
H REGISTER	ROAR
1 0000 0000	0 0 0000 0100 0101
J REGISTER	ROSCAR
P XXXX XXXX	X X XXXX XXXX XXXX

R REGISTER
1 000 1 0000 0000 1 0000 0000

A REGISTER
1 000 1 0000 0000 1 0000 0000

S REGISTER
P XXX P XXXX XXXX P XXXX XXXX

B REGISTER
P XXXX XXXX P XXXX XXXX

C REGISTER
P XXX P XXXX XXXX P XXXX XXXX

D REGISTER
1 0000 0000 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0000 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

THE A REGISTER CONTENTS ARE TRANSFERRED TO LOCAL STORAGE LOCATION (0).

A0 CONTAINED THE ENTRY STATUS OF THE YA AND YB STATS. AND THESE ARE USED AFTER THIS MICROPROGRAM AND THE SYSTEM RESET MICROPROGRAM ARE COMPLETED TO DETERMINE WHICH ENTRY CONDITION INITIATED THE CPU CHECK OUT MICROPROGRAM.
A0 IS RESET BY THE ALU OPERATION.
THE YA STATS ARE SET WITH Y0 AND Y2 ON FOR FUTURE CHECKS.

XX —— 004
E 1010→YA
A 2+Z→A0
L H→L L→H
D A→LSTOR
C 0→SK
S3— XX —SC

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SENSE LATCHES			
A0	A1	A2	A3
0	0	1	1
B0	B1	B2	B3
1	1	1	1
C0	C1	C2	C3
0	0	0	1
D0	D1	E0	E1
0	0	0	0
E2	E3	F0	G0
0	0	0	1
G1	H0	H1	H2
1	0	0	0
H3	H4	J0	J1
0	0	0	0
J2	K0	L0	L1
0	0	0	0
L2	M0	M1	M2
0	1	1	1
M3	N0	N1	N2
0	0	0	0
N3	P0	P1	P2
0	0	0	0
Q0	Q1	Q2	Q3
0	1	1	0
R0	R1	R2	S0
0	0	0	0
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
0	1	1	0
D0	D1	E0	E1
0	0	0	1
E2	E3		
0	1		
		L0	L1
		1	1
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
1	0	1	0
N3			
0			

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
0	0	0	0	0
	DESTINATION H-J-O			
	0	0	1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0101 0000	0101 0101

LSAR REGISTER	ROBAR
1 0000 0101	0 0 0000 0100 0101
H REGISTER	ROAR
1 0000 0000	0 0 0000 0111 1111
J REGISTER	ROSCAR
P XXXX XXXX	X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 1 0000 0000 1 0000 0000

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

P XXXX XXXX 1 0101 0101

C REGISTER

1 000 1 0000 0000 1 0000 0000

D REGISTER

1 0000 0000 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0101	1 0101 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 A CHECK IS MADE THAT THE Y2 STAT IS ON.
IF A BRANCH TO A STOP IN 07D OCCURS, CHECK THE Y2 SETTING.
IF IT IS CORRECT, SUSPECT THE CB FIELD DECODING IN THIS MICROINSTRUCTION.
IF IT IS WRONG, SUSPECT THE OPERATION IN THE PREVIOUS MICROINSTRUCTION 002.

2 L4≠0 IS CHECKED ON.
IF A BRANCH TO A STOP IN 07E OCCURS, CHECK THE SETTING OF THE LSAR REGISTER.
IF THIS IS CORRECT, SUSPECT THE L4≠0 CIRCUITRY OR THE CC FIELD DECODING.
IF IT IS WRONG, SUSPECT THE SETTING OF LSAR FROM THE (EB) OPERATION IN THIS CYCLE.

3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 0C1. MICROINSTRUCTION 005. CHECK THE SETTING OF THE D0 REGISTER. THIS SHOULD BE ZERO AND IF IT IS NOT, THEN THE DIAGNOSIS WILL DEPEND ON WHICH ENTRY WAS MADE TO THE MICROPROGRAM.
SYSTEM RESET AND LOAD ENTRIES SHOULD FORCE A HARDWARE RESET OF THE D REGISTER, THE OTHER ENTRIES FROM LOG-OUT AND ON CYCLING THE CPU CHECK OUT SHOULD RESET THE D REGISTER PRIOR TO ENTERING THIS MICROPROGRAM. THUS IF THE D0 REGISTER IS NOT ZERO, IT WILL BE NECESSARY TO CHECK THE MECHANISM OF THE ENTRIES WHICH SHOULD FORCE THE ZERO STATE.

FUNCTIONS OF BOX

THE B1 REGISTER IS FILLED WITH A PATTERN 55(HEX) WHICH IS USED LATER IN THE MAIN STORAGE READ AND WRITE TEST.
THE C REGISTER IS FILLED WITH ZEROES, RATHER THAN THE INDETERMINATE VALUE IT HELD BEFORE. IT IS NOT RESET DURING THE HARDWARE SYSTEM RESET CYCLES.

THE YB STATS ARE SET WITH Y5 AND Y7 ON AND THE Y4 AND Y6 OFF FOR LATER CHECKS.

XX — 045
E 0101→YB
A 0E+E0→B1
L BE→L
D A→C
C CPU
R Y2 L4≠0
S5 — ** —SE

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SENSE LATCHES			
A0	A1	A2	A3
1	0	1	1
B0	B1	B2	B3
0	1	1	1
C0	C1	C2	C3
0	1	0	0
D0	D1	E0	E1
0	0	0	1
E2	E3	F0	G0
0	1	0	1
G1	H0	H1	H2
1	0	0	0
H3	H4	J0	J1
0	0	0	0
J2	K0	L0	L1
1	0	0	1
L2	M0	M1	M2
1	0	1	1
M3	N0	N1	N2
0	0	1	0
N3	P0	P1	P2
0	1	1	1
Q0	Q1	Q2	Q3
1	0	0	0
R0	R1	R2	S0
0	0	0	0
T0	T1	JX	PX
0	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
		L0	L1
		0	0
L2	M0	M1	M2
0	1	1	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL	-1	-2	+1	EARLY C COND
0		0	0	0	0
	DESTINATION H-J-O	0	0	1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK		HALT
0		0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0000 0000	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0111 1111
H REGISTER	ROAR
1 0000 0000	0 0 0000 1100 0001
J REGISTER	ROSCAR
P XXXX XXXX	X X XXXX XXXX XXXX

	R REGISTER	
1 000 1	0000 0000	1 0000 0000
	A REGISTER	
1 000 1	0000 0000	1 0000 0000
	S REGISTER	
P XXX P	XXXX XXXX	P XXXX XXXX
	B REGISTER	
P	XXXX XXXX	1 0101 0101
	C REGISTER	
1 000 1	0000 0000	1 0000 0000
	D REGISTER	
1	0000 0000	1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0000 0000

	CHECKS	IF REGISTER
1	0000 0000	1 0000 0000

	INTERFACE CONTROLS	
	XXXX XXXX	XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

	T0		T1
P	XXXX XXXX	P	XXXX XXXX
	W0		W1
X	XXXX XXXX	X	XXXX XXXX
	W2		
X	XXXX XXXX	P	XXXX XXXX
	W3		W4
X	XXXX XXXX	X	XXXX XXXX

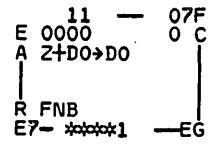
SP	-DATA	-KEY
1	0000	0000

Q

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE DO REGISTER BITS 0-3. DO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. DO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	0	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	0	1	1	1
C0	C1	C2	C3				
0	0	0	0				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	0	1
E2	E3	F0	G0	E2	E3		
0	0	1	1	0	1		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			0	1
L2	M0	M1	M2	L2	M0	M1	M2
0	0	1	1	1	0	1	1
M3	N0	N1	N2	M3	N0	N1	N2
1	0	0	0	0	0	1	0
N3	P0	P1	P2	N3			
0	0	0	0	0			
Q0	Q1	Q2	Q3				
0	0	1	0				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H=STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL	−1	−2	+1	EARLY C COND
0		0	0	0	0
	DESTINATION	H=J=0			
		0	0	1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I=O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS=	YA	YB	YD	YE
1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0101 0000	0101 0101

LSAR REGISTER	ROBAR
1 0000 0101	0 0 0000 1100 0001
H REGISTER	ROAR
1 0000 0000	1 0 0000 1110 1101
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 1 0000 0000 1 0000 0000

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

1 0101 0101 1 0101 0101

C REGISTER

1 000 1 0000 0000 1 0000 0000

D REGISTER

1 0000 0000 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0101	1 0101 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP =DATA =KEY

1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

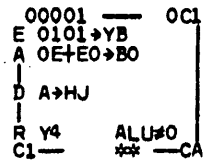
1 Y4 IS CHECKED OFF.
IF A BRANCH TO A STOP IN OEF OCCURS AFTER THIS MICROINSTRUCTION. CHECK THE SETTING OF THE Y4 STAT AFTER EXECUTING MICROINSTRUCTION 003.
ALTHOUGH THE YB=5 OPERATION ALSO EXISTS IN THE PRESENT MICROINSTRUCTION 005, THIS CURRENT ONE WOULD BE TOO LATE TO AFFECT THE SETTING OF Y4 BEING TESTED AS THE TEST IS PERFORMED ON THE PREVIOUS VALUE.
IF Y4 WAS CORRECT, SUSPECT THE CB FIELD DECODING.
IF INCORRECT, SUSPECT THE SETTING IN THE PREVIOUS MICROINSTRUCTION.

2 ALU≠0 IS CHECKED ON.
IF A BRANCH TO A STOP IN OEC OCCURS, CHECK THE SETTING OF THE BO REGISTER.
IF THIS IS CORRECT, SUSPECT THE ALU≠0 CIRCUITRY OR THE CC FIELD DECODING.
IF IT IS INCORRECT, SUSPECT THE CURRENT ALU OPERATION.

3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 04A MICROINSTRUCTION 007, CHECK THE SETTING OF B1 REGISTER BITS (0-3).
IF THEY ARE WRONG, SUSPECT THE ALU OPERATION IN MICROINSTRUCTION 003.

FUNCTIONS OF BOX

THE BO REGISTER IS FILLED WITH 55(HEX) TO COMPLETE THE MEMORY CHECK PATTERN 5555(HEX) IN THE B REGISTER.
THE H AND J REGISTERS ARE SET TO ZERO.



RUN 17 JAN 66

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
1	1	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
0	0	1	1	1	1	1	1
C0	C1	C2	C3				
0	0	1	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	1	0	0	0	0	0
E2	E3	F0	G0	E2	E3		
0	0	0	1	0	0		
G1	H0	H1	H2				
1	1	0	0				
H3	H4	J0	J1				
1	0	0	1				
J2	K0	L0	L1			L0	L1
0	0	1	0			0	0
L2	M0	M1	M2	L2	M0	M1	M2
0	1	1	1	0	0	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	1	1	1	0	0	0
N3	P0	P1	P2	N3			
1	1	1	0	0			
Q0	Q1	Q2	Q3				
0	0	0	1				
R0	R1	R2	S0				
0	0	0	1				
T0	T1	JX	PX				
0	0	0	0				

CONDITIONS

H—STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL −1	−2	+1	EARLY C COND
0	0	0	0	0

DESTINATION H—J—O: 0 0 1

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I—O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS—		YA	YB	YD	YE
	1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0101 0101	0101 0101

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 1110 1101
H REGISTER	ROAR
1 0000 0000	0 0 0000 0100 1010
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER			
1 000	1	0000 0000	1 0000 0000
A REGISTER			
1 000	1	0000 0000	1 0000 0000
S REGISTER			
P XXX	P	XXXX XXXX	P XXXX XXXX
B REGISTER			
	1	0101 0101	1 0101 0101
C REGISTER			
1 000	1	0000 0000	1 0000 0000
D REGISTER			
	1	0000 0000	1 0000 0000

EX REG	P REGISTER		Q REGISTER	
1 000	1	0000 0000	1	0101 0101

CHECKS		IF REGISTER	
	1	0000 0000	1 0000 0000

INTERFACE CONTROLS: XXXX XXXX XXXX XXXX

CHANNEL CONTROLS	
XXX	0000 0000 0000 0000

CHANNEL DISPLAY

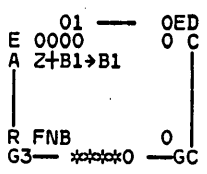
	T0		T1
P	XXXX XXXX	P	XXXX XXXX
	W0		W1
X	XXXX XXXX	X	XXXX XXXX
	W2		
X	XXXX XXXX	P	XXXX XXXX
	W3		W4
X	XXXX XXXX	X	XXXX XXXX

SP −DATA −KEY: 1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE B1 REGISTER BITS 0—3. B1 IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. B1 IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	0	0	1	1
C0	C1	C2	C3				
0	0	0	0				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	1	0
E2	E3	F0	G0	E2	E3		
0	0	0	1	0	0		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			1	0
L2	M0	M1	M2	L2	M0	M1	M2
0	1	0	1	0	1	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	0	0	0	0	1	1
N3	P0	P1	P2	N3			
0	0	0	0	1			
Q0	Q1	Q2	Q3				
0	1	0	0				
R0	R1	R2	S0				
0	0	0	1				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
0	0	0	1	0

DESTINATION H-J-O: 1 0 0

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0101 0101	1101 0101

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0100 1010
H REGISTER	ROAR
0 0000 0001	0 0 0000 0111 1100
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER: 1 000 1 0101 0101 1 0101 0101

A REGISTER: 1 000 1 0101 0101 1 0101 0101

S REGISTER: P XXX P XXXX XXXX P XXXX XXXX

B REGISTER: 1 0101 0101 1 0101 0101

C REGISTER: 1 000 1 0000 0000 1 0000 0000

D REGISTER: 0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	0 1000 0000	1 0101 0101

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS: XXXX XXXX XXXX XXXX

CHANNEL CONTROLS: XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY: 1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 L2≠0 AND L4≠0 ARE BOTH CHECKED OFF.
IF A BRANCH OCCURS TO ANY ADDRESS OTHER THAN 07C EITHER ONE OR BOTH OF THESE MAY BE AT FAULT.

A. BRANCH TO 07E. CHECK LSAR REGISTER AT THE END OF THE MICROINSTRUCTION 007 CYCLE.
IF THIS IS CORRECT. SUSPECT THE CB FIELD DECODING AND THE L2≠0 CIRCUITRY.

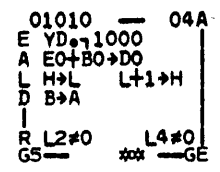
B. BRANCH TO 07D. AS A. EXCEPT THAT IF THE LSAR REGISTER IS CORRECT. SUSPECT THE CC FIELD DECODING AND THE L4≠0 CIRCUITRY.

C. BRANCH TO 07F. AS A. EXCEPT THAT IF THE LSAR REGISTER IS CORRECT. SUSPECT THE L2≠0 AND L4≠0 CIRCUITRY.
IF LSAR IS WRONG. CHECK THE H REGISTER.
IF THIS IS WRONG. SUSPECT THE SETTING OF H AND J REGISTERS IN MICROINSTRUCTION 005. AND THE FORMING OF A0 REGISTER IN MICROINSTRUCTION 002.
IF IT IS CORRECT. SUSPECT THE LSAR REGISTER.

2 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 0C0. MICROINSTRUCTION 009. SUSPECT THE 18 BIT DATA TRANSFER IN MICROINSTRUCTION 003 OR THE ALU OPERATION IN MICROINSTRUCTION 002.

FUNCTION OF BOX

THE D0 REGISTER IS FILLED WITH A PATTERN WHICH IS USED LATER TO GENERATE THE MAIN STORAGE ADDRESS. MICROINSTRUCTION 15. THE FIRST 4 BITS ARE ALSO USED AS A FUNCTION BRANCH ADDRESS. MICROINSTRUCTION 17. THE A REGISTER IS USED AS A TEMPORARY STORAGE FOR THE B REGISTER PATTERN WHICH IS USED LATER IN THE MAIN STORAGE READ AND WRITE TEST.



RUN 17 JAN 66

SENSE LATCHES			
A0	A1	A2	A3
1	0	1	1
B0	B1	B2	B3
0	1	0	1
C0	C1	C2	C3
0	1	0	1
D0	D1	E0	E1
0	0	1	1
E2	E3	F0	G0
1	1	1	0
G1	H0	H1	H2
0	1	0	0
H3	H4	J0	J1
1	0	0	0
J2	K0	L0	L1
1	1	1	1
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	1	1	1
N3	P0	P1	P2
1	1	1	1
Q0	Q1	Q2	Q3
1	0	0	1
R0	R1	R2	S0
0	0	0	1
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
		L0	L1
		0	0
L2	M0	M1	M2
0	1	0	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H—STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H—J—0	
	0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK		HALT
0		0

CONDITIONS

PMA	IMA	I—O	YCI	YCD	ASCII
X	X	0	X	0	X

STATS—		YA	YB	YD	YE
	1	1010	0101	000	1 00

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 1	1 0000 0000	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0111 1100
H REGISTER	ROAR
0 0000 0001	1 0 0000 1100 0000
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 1 0101 0101 1 0101 0101

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

1 0101 0101 1 0101 0101

C REGISTER

1 000 1 0000 0000 1 0000 0000

D REGISTER

0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0000 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

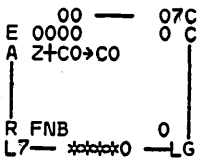
T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP —DATA —KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE CO REGISTER BITS 0—3. CO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. CO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	0	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	0	1	0	1
C0	C1	C2	C3				
0	0	0	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	1	1
E2	E3	F0	G0	E2	E3		
0	0	1	1	1	1		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			1	1
L2	M0	M1	M2	L2	M0	M1	M2
0	0	1	1	0	0	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	0	0	0	1	1	1
N3	P0	P1	P2	N3			
0	0	0	0	1			
Q0	Q1	Q2	Q3				
0	0	0	1				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
0	0	0	1	0
	DESTINATION H-J-O: 1 0 0			

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	0	0	X

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 1	1 11110000	1111 1111

LSAR REGISTER	ROBAR
0 0000 0001	1 0 0000 1100 0000
H REGISTER	ROAR
0 0000 0010	1 0 0000 1110 1110
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER			
1 000	1	0101 0101	1 0101 0101
A REGISTER			
1 000	1	0101 0101	1 0101 0101
S REGISTER			
P XXX	P	XXXX XXXX	P XXXX XXXX
B REGISTER			
	1	1111 1111	1 0101 0101
C REGISTER			
1 000	1	0101 0101	1 0101 0101
D REGISTER			
	0	1101 0101	1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 1111	1 0000 1111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

TO	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 THE YO AND Y1 STATS ARE CHECKED ON AND OFF RESPECTIVELY.
IF A BRANCH OCCURS TO SOME ADDRESS OTHER THAN OEE. CHECK THE YA STAT SETTINGS.
IF THESE ARE CORRECT, SUSPECT THE CB OR CC FIELD DECODING.
IF THEY ARE WRONG, SUSPECT THE SETTING OF THE YA STATS IN MICROINSTRUCTION 002.

2 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 05F. SUSPECT THE SETTING OF THE BO REGISTER IN THE CURRENT MICROINSTRUCTION.
THE EMIT FIELD SETTING FOR ADD IS 15 OR F(HEX) AND AS THE Q BUS IS SKEWED THIS SHOULD PRODUCE AN OUTPUT TO THE BO REGISTER OF FF(HEX).
INVESTIGATE P AND Q REGISTERS, AND SUSPECT ALSO THE SKEW OPERATION, AND POSSIBLY THE RESET OF THE SKEW REGISTER BEFORE 005. MICROINSTRUCTION 001. COMMENCES.

FUNCTION OF BOX

THE ALU OPERATION IS USED TO GENERATE THE NEXT FUNCTION BRANCH ADDRESS IN BO REGISTER BITS (0-3).
THE 18 BIT DATA TRANSFER DOES NOT AFFECT THE OPERATION. OF THE MICROPROGRAM AND IS USED MERELY TO EXERCISE THE DATA FLOW AND CONTROLS. RESET INDIRECT CARRY IS INCLUDED BECAUSE THIS IS THE FIRST INDIRECT FUNCTION BEING PERFORMED IN THE ROUTINE, AND THE STATUS OF THIS IS NOT NECESSARILY KNOWN.

```
  00000 ——  0C0
E 1111,ADD* 0 C
A 0E?0E*→B0   |
L H→L   L+1→H |
D A→C         |
|             |
R Y0      Y1  |
G1——    ** ——GA
```

SENSE LATCHES			
A0	A1	A2	A3
1	1	1	1
B0	B1	B2	B3
0	1	0	0
C0	C1	C2	C3
0	1	1	0
D0	D1	E0	E1
1	1	1	1
E2	E3	F0	G0
1	1	1	0
G1	H0	H1	H2
0	0	1	0
H3	H4	J0	J1
1	0	0	0
J2	K0	L0	L1
1	0	1	0
L2	M0	M1	M2
1	1	0	1
M3	N0	N1	N2
0	0	0	0
N3	P0	P1	P2
0	1	1	1
Q0	Q1	Q2	Q3
1	0	0	1
R0	R1	R2	S0
0	0	0	1
T0	T1	JX	PX
0	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
L0	L1		
0	0		
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-D 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	0 IMA	I-O	YCI	YCD	ASCII
X	X	0	0	0	X

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 1111 1111	1111 1111

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 1110 1110
H REGISTER	ROAR
0 0000 0010	1 0 0000 0101 1111
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 1 0101 0101 1 0101 0101

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

1 1111 1111 1 0101 0101

C REGISTER

1 000 1 0101 0101 1 0101 0101

D REGISTER

0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 1111 1111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

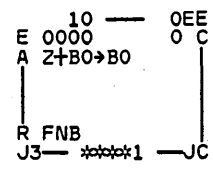
T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE BO REGISTER BITS 0-3. BO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. BO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES

A0	A1	A2	A3
0	0	1	1
B0	B1	B2	B3
1	1	1	1
C0	C1	C2	C3
0	0	0	0
D0	D1	E0	E1
0	0	0	0
E2	E3	F0	G0
0	0	0	1
G1	H0	H1	H2
1	0	0	0
H3	H4	J0	J1
0	0	0	0
J2	K0	L0	L1
0	0	0	0
L2	M0	M1	M2
0	1	0	1
M3	N0	N1	N2
0	0	0	0
N3	P0	P1	P2
0	0	0	0
Q0	Q1	Q2	Q3
0	1	0	0
R0	R1	R2	S0
0	0	0	1
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES

B0	B1	B2	B3
0	1	0	0
D0	D1	E0	E1
1	1	1	1
E2	E3		
1	1		
		L0	L1
		1	0
L2	M0	M1	M2
1	1	0	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H=STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
0	1	0	0	0

DESTINATION H=J=O: 1 0 0

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I=O	YCI	YCD	ASCII
X	X	0	0	0	1

STATS=		YA	YB	YD	YE
	1	1010	0101	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 1	1 11110000	1111 1111

LSAR REGISTER	ROBAR
0 0000 0010	1 0 0000 0101 1111
H REGISTER	ROAR
0 0000 0001	0 0 0000 0111 1100
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER
1 000 1 0101 0101 1 0101 0101

A REGISTER
1 000 1 0101 0101 1 0101 0101

S REGISTER QQ
P XXX P XXXX XXXX P XXXX XXXX

B REGISTER
1 0101 0101 1 0101 0101

C REGISTER
1 000 1 1111 1111 1 0101 0101

D REGISTER
0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 1111	1 00001111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP =DATA =KEY
1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 THE Y3 STAT IS CHECKED OFF.
IF A BRANCH TO A STOP AT 07D OCCURS. CHECK THE SETTING OF THE Y3 STAT. AND. IF IT IS CORRECT SUSPECT THE CC FIELD DECODING.
IF IT IS WRONG. SUSPECT THE SETTING OF THE YA STATS IN MICROINSTRUCTION 002.

2 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN ODE AT MICROINSTRUCTION 013. SUSPECT THE SETTING OF THE CO REGISTER IN THE CURRENT MICROINSTRUCTION. THE P AND Q REGISTERS SHOULD BE CHECKED AND THE SKEW AND ALU FUNCTION REGISTERS SHOULD BE SUSPECTED IF CO IS WRONG WHILE P AND Q ARE CORRECT.

FUNCTION OF BOX

THE MAIN STORAGE TEST PATTERN IS TRANSFERRED BACK TO THE B REGISTER.
THE H REGISTER IS DECREMENTED TO BE USED IN MICROINSTRUCTION 013 TO FORM PART OF THE MAIN STORAGE TEST ADDRESS.
THE CO REGISTER IS FORMED FOR THE NEXT FUNCTION BRANCH (MICROINSTRUCTION 013) AND THIS PATTERN IS ALSO USED LATER TO CHECK DIRECT CARRY. MICROINSTRUCTION 017 AND 019.

SWEA SETS ASCII. ENABLE AND WAIT ON.
ASCII IS CHECKED LATER IN MICROINSTRUCTION 031.
ENABLE IS ALREADY ON. BUT THIS OPERATION HAS A USE IN THE CHECKING THE CHECKERS ROUTINES. BY A SERIES OF DIAGNOSE INSTRUCTIONS IT IS POSSIBLE TO PRODUCE BAD PARITY IN THE REGISTERS. THESE DIAGNOSE INSTRUCTIONS WOULD BE PERFORMED WHILE THE CPU IS DISABLED. IF A FURTHER DIAGNOSE WITH UNDUMP TO THIS MICROINSTRUCTION IS PERFORMED. THE CPU WILL BE ENABLED. AND THE D0. D1. RX. R0. R1. LSAR. SKEW SELECT AND EX REG CHECKERS CAN BE FORCED ON. IF SUITABLE BAD PARITY DATA IS HELD IN THE APPROPRIATE REGISTERS.

```
 11111  —  05F
E 1111
A 0E?0E→CO
L H→L   L-1→H
D A→B
C          SWEA
R 0         Y3
LS—    0✲  —LE
```

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SENSE LATCHES

A0	A1	A2	A3
1	0	1	1
B0	B1	B2	B3
1	0	1	0
C0	C1	C2	C3
0	0	1	0
D0	D1	E0	E1
0	0	1	1
E2	E3	F0	G0
1	1	1	0
G1	H0	H1	H2
0	0	0	0
H3	H4	J0	J1
0	0	1	0
J2	K0	L0	L1
1	0	1	0
L2	M0	M1	M2
0	1	0	1
M3	N0	N1	N2
1	0	0	0
N3	P0	P1	P2
0	1	1	1
Q0	Q1	Q2	Q3
0	1	0	0
R0	R1	R2	S0
1	0	0	0
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES

B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
		L0	L1
		0	0
L2	M0	M1	M2
0	1	0	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 0000

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-O 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	0	0	0	1

STATS-	YA	YB	YD	YE
1	1010	0101	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 1111 1111	1111 1111

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0111 1100
H REGISTER	ROAR
0 0000 0001	1 0 0000 1101 1110
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER
1 000 1 0000 0000 1 0000 0000

A REGISTER
1 000 1 0101 0101 1 0101 0101

S REGISTER
P XXX P XXXX XXXX P XXXX XXXX

B REGISTER
1 0101 0101 1 0101 0101

C REGISTER
1 000 1 1111 1111 1 0101 0101

D REGISTER
0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 1111 1111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

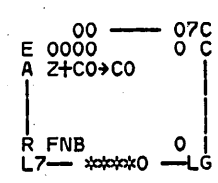
T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE CO REGISTER BITS 0-3. CO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. CO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	0	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	1	0	1	0
C0	C1	C2	C3				
0	0	0	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	1	1
E2	E3	F0	G0	E2	E3		
0	0	1	1	1	1		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			1	0
L2	M0	M1	M2	L2	M0	M1	M2
0	0	1	1	0	1	0	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	0	0	1	0	0	0
N3	P0	P1	P2	N3			
0	0	0	0	0			
Q0	Q1	Q2	Q3				
0	0	0	1				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H=STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H−J−O: 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I−O	YCI	YCD	ASCII
X	X	1	0	0	1

STATS−		YA	YB	YD	YE
	1	1010	0101	000	1 10

ALU CONT•	SKEW SELECT	ALU BIN OUT
1 1111 1	1 1111 0000	1111 1111

LSAR REGISTER	ROBAR
1 0011 1111	1 0 0000 1101 1110
H REGISTER	ROAR
0 0000 0001	1 0 0000 1110 1110
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER
1 000 0 0000 0001 1 0000 0000

A REGISTER
1 000 0 0000 0001 1 0000 0000

S REGISTER
P XXX P XXXX XXXX P XXXX XXXX

B REGISTER
1 0101 0101 1 0101 0101

C REGISTER
1 000 1 1111 1111 1 1111 1111

D REGISTER
0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 1111	1 1111 1111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP −DATA −KEY
1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 ALU OUTPUT BIT 7 ALU7 IS CHECKED ON•
IF A BRANCH OCCURS TO A STOP AT 0EC• CHECK THE SETTING OF THE C1 REGISTER•
IF THIS IS CORRECT• SUSPECT THE ALU7 CIRCUITRY OR THE CB FIELD DECODING•
IF IT IS WRONG• SUSPECT THE CURRENT ALU OPERATION AND INVESTIGATE THE P AND Q REGISTERS•

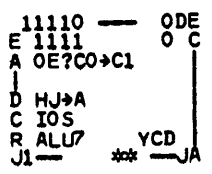
2 DIRECT CARRY (YCD) IS CHECKED OFF•
IF A BRANCH OCCURS TO A STOP AT 0EF• CHECK THE YCD STATUS•
IF CORRECT• SUSPECT THE CC FIELD DECODING•
IF WRONG• SUSPECT THE RESET OF CARRY IN PREVIOUS MICROINSTRUCTIONS WHICH HAVE HAD DIRECT ALU FUNCTIONS•

3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 04B• MICROINSTRUCTION 015• IT WILL BE NECESSARY TO INVESTIGATE JUST WHEN THE B REGISTER CHANGED OR HAS NOT SET CORRECTLY IN THE PREVIOUS MICROINSTRUCTION•

FUNCTION OF BOX

THE C1 REGISTER IS FILLED WITH FF(HEX) AND THIS PATTERN IS USED LATER WHEN SETTING THE YA AND YB STATS• MICROINSTRUCTION 021•

THE A REGISTER IS SET UP WITH PART OF THE MAIN STORAGE TEST ADDRESS•



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SENSE LATCHES			
A0	A1	A2	A3
1	1	1	1
B0	B1	B2	B3
0	1	0	0
C0	C1	C2	C3
1	0	0	0
D0	D1	E0	E1
0	0	1	0
E2	E3	F0	G0
0	1	1	1
G1	H0	H1	H2
1	1	1	1
H3	H4	J0	J1
0	1	0	1
J2	K0	L0	L1
0	0	1	0
L2	M0	M1	M2
1	0	0	1
M3	N0	N1	N2
1	0	1	0
N3	P0	P1	P2
0	1	1	0
Q0	Q1	Q2	Q3
0	1	1	0
R0	R1	R2	S0
0	0	0	0
T0	T1	JX	PX
0	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
		L0	L1
		0	0
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-Q: 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK		HALT
0		0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	1	0	0	1

STATS-		YA	YB	YD	YE
	1	1010	0101	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0101 0101	0101 0101

LSAR REGISTER	ROBAR
1 0011 0000	1 0 0000 1110 1110
H REGISTER	ROAR
0 0000 0001	1 0 0000 0100 1011
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 0 0000 0001 1 0000 0000

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

1 0101 0101 1 0101 0101

C REGISTER

1 000 1 1111 1111 1 1111 1111

D REGISTER

0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0101 0101

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

TO	T1
P XXXX XXXX	P XXXX XXXX
WO	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

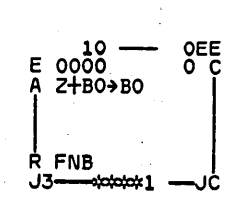
SP -DATA -KEY

1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE BO REGISTER BITS 0-3. BO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. BO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	0	1	0	0
C0	C1	C2	C3				
0	0	0	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	1	0
E2	E3	F0	G0	E2	E3		
0	0	0	1	0	1		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			1	0
L2	M0	M1	M2	L2	M0	M1	M2
0	1	1	1	1	0	0	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	0	0	1	0	1	0
N3	P0	P1	P2	N3			
0	0	0	0	0			
Q0	Q1	Q2	Q3				
0	1	1	0				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H=STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	0 001	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	1 0 0	0
	DESTINATION H=J=0 1 0 0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I=O	YCI	YCD	ASCII
X	X	1	0	1	1

STATS=		YA	YB	YD	YE
	1	1010	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	0 1101 0101	0110 0101

LSAR REGISTER	ROBAR
1 0011 1001	1 0 0000 0100 1011
H REGISTER	ROAR
1 0011 1001	0 0 0000 0111 1111
J REGISTER	ROSCAR
1 0000 0000	X X XXXX XXXX XXXX

R REGISTER

1	000	1	0101	0101	1	0101	0101

A REGISTER

1	000	0	0000	0001	1	0110	0101

S REGISTER

P	XXX	P	XXXX	XXXX	P	XXXX	XXXX

B REGISTER

		1	0101	0101	1	0101	0101

C REGISTER

1	000	1	1111	1111	1	1111	1111

D REGISTER

		0	1101	0101	1	0000	0000

EX REG	P REGISTER	Q REGISTER
1 000	1 1001 0000	0 1101 0101

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX	0000	0000	0000	0000

CHANNEL DISPLAY

T0		T1	
P	XXXX XXXX	P	XXXX XXXX
W0		W1	
X	XXXX XXXX	X	XXXX XXXX
W2			
X	XXXX XXXX	P	XXXX XXXX
W3		W4	
X	XXXX XXXX	X	XXXX XXXX

SP	=DATA	=KEY
1	0000	0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 ALU≠0 IS CHECKED ON (ALU OUTPUT NON-ZERO).
IF A BRANCH TO A STOP OCCURS IN 07D CHECK THE A1 REGISTER.
IF THIS IS CORRECT. SUSPECT THE ALU≠0 CIRCUITRY OR CB FIELD DECODING.

2 Y7 IS CHECKED ON.
IT WILL BE NECESSARY. IF A BRANCH OCCURS TO A STOP IN 07E TO INVESTIGATE THE SETTING OF Y7 IN MICROINSTRUCTION 005. AND IF Y7 IS CORRECT UNTIL MICROINSTRUCTION 015. SUSPECT THE CC FIELD DECODING.

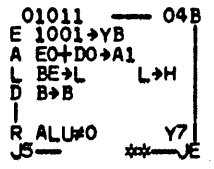
3. IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 0DB. MICROINSTRUCTION 017. SUSPECT THE SETTING OF THE DO REGISTER IN MICROINSTRUCTION 007.

FUNCTION OF BOX

THE A1 REGISTER IS SET WITH THE REST OF THE MAIN STORAGE TEST ADDRESS FOR THE MAIN STORAGE READ IN MICROINSTRUCTION 017.

THE H REGISTER IS SET TO 39(HEX) AND THIS LOCATION IS USED LATER TO HOLD THE MAIN STORAGE ADDRESS IN LOCAL STORAGE. MICROINSTRUCTION 025.

THE PATTERN IS ALSO USED IN FUNCTION BRANCHES. THE FIRST BEING TO 0C7 MICROINSTRUCTION 023.



RUN 17 JAN 66

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
1	0	0	0				
B0	B1	B2	B3	B0	B1	B2	B3
0	0	0	0	1	1	1	1
C0	C1	C2	C3				
0	0	0	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	1	1	0	0	0	0
E2	E3	F0	G0	E2	E3		
1	1	1	1	0	0		
G1	H0	H1	H2				
1	1	0	1				
H3	H4	J0	J1				
1	1	0	1				
J2	K0	L0	L1			L0	L1
0	1	1	0			0	0
L2	M0	M1	M2	L2	M0	M1	M2
1	1	0	1	0	1	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	1	1	1	0	0	0	0
N3	P0	P1	P2	N3			
1	0	0	0	0			
Q0	Q1	Q2	Q3				
0	1	0	0				
R0	R1	R2	S0				
0	0	1	0				
T0	T1	JX	PX				
1	1	0	0				

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-D 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
X	X	1	0	0	1

STATS-		YA	YB	YD	YE
	1	1010	1001	000	1 10

ALU CONT.		SKEW SELECT		ALU BIN OUT
1 1111	1	0 1101	0101	1101 0101

LSAR REGISTER		ROBAR
1 0011 0000		0 0 0000 0111 1111
H REGISTER		ROAR
1 0011 1001		1 0 0000 1101 1011
J REGISTER		ROSCAR
1 0000 0000		X X XXXX XXXX XXXX

R REGISTER

1 000 1 0000 0000 1 0000 0000

A REGISTER

1 000 0 0000 0001 1 0110 0101

S REGISTER

P XXX P XXXX XXXX P XXXX XXXX

B REGISTER

1 0101 0101 1 0101 0101

C REGISTER

1 000 1 1111 1111 1 1111 1111

D REGISTER

0 1101 0101 1 0000 0000

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	0 1101 0101

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY

1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE DO REGISTER BITS 0-3. DO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. DO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.

```
    11  —  07F
E 0000     0 C
A Z+DO→DO    |
|            |
|            |
R FNB      1 |
E7— ****1 —EG
```

SENSE LATCHES			
A0	A1	A2	A3
1	1	1	1
B0	B1	B2	B3
1	0	0	0
C0	C1	C2	C3
0	0	0	1
D0	D1	E0	E1
1	1	0	0
E2	E3	F0	G0
0	1	1	0
G1	H0	H1	H2
0	1	0	1
H3	H4	J0	J1
1	1	0	1
J2	K0	L0	L1
0	0	1	0
L2	M0	M1	M2
1	1	0	1
M3	N0	N1	N2
1	0	0	1
N3	P0	P1	P2
1	0	0	0
Q0	Q1	Q2	Q3
0	1	0	1
R0	R1	R2	S0
1	0	1	1
T0	T1	JX	PX
0	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
0	0	0	0
D0	D1	E0	E1
0	0	1	1
E2	E3		
1	1		
		L0	L1
		1	0
L2	M0	M1	M2
1	1	0	1
M3	N0	N1	N2
0	1	1	1
N3			
1			

CONDITIONS

H—STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	1	0 001	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
0	0 0 1	0
	DESTINATION H—J—O: 0 1 0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
1	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I—O	YCI	YCD	ASCII
0	0	1	0	1	1

STATS—		YA	YB	YD	YE
	1	1010	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 1111 1111	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 1101 1011
H REGISTER	ROAR
1 0011 1001	1 0 0000 1110 0001
J REGISTER	ROSCAR
0 0000 0001	X X XXXX XXXX XXXX

			R REGISTER		
1	000	1	0101 0101	1	0101 0101
			A REGISTER		
1	000	0	0000 0001	1	0110 0101
			S REGISTER		
P	XXX	P	XXXX XXXX	P	XXXX XXXX
			B REGISTER		
		1	0101 0101	1	0101 0101
			C REGISTER		
0	001	1	0000 0000	1	1111 1111
			D REGISTER		
		P	XXXX XXXX	P	XXXX XXXX

EX REG		P REGISTER		Q REGISTER	
1	000	1	0000 0000	1	1111 1111

	CHECKS		IF REGISTER
	1 0000 0000	1	0000 0000

	INTERFACE CONTROLS	
	XXXX XXXX	XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

	T0		T1
P	XXXX XXXX	P	XXXX XXXX
	W0		W1
X	XXXX XXXX	X	XXXX XXXX
	W2		
X	XXXX XXXX	P	XXXX XXXX
	W3		W4
X	XXXX XXXX	X	XXXX XXXX

SP	−DATA	−KEY
1	0000	0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

THE C0 REGISTER SHOULD BE SET TO ZERO AS FF(HEX)
IS ADDED TO 00(HEX) WITH DIRECT CARRY SET.
THIS ADDITION PRODUCES A DIRECT CARRY WHICH IS
CHECKED LATER IN MICROINSTRUCTION 019

MAIN STORAGE LOCATION 165(HEX) IS READ OUT TO EXERCISE
THE MEMORY CONTROLS.
THE SIMULATION GIVEN ABOVE IS CORRECT FOR SINGLE
CYCLE — IE THE D REGISTER SETTING IS UNKNOWN.
IF THE PROGRAM WERE DYNAMICALLY RUN HOWEVER, THIS
PATTERN WOULD NOT BE AVAILABLE UNTIL THE NEXT CYCLE.

11011 — ODB

```
E 1111,ADD* 1 C
A Z+C0*→C0
L J→L    L+1→J
D B→B
S READ
E8 —    XX —EH
```

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
1	0	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	0	0	1	0	0	0
C0	C1	C2	C3				
0	0	1	0				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	1	1	0	0
E2	E3	F0	G0	E2	E3		
0	0	0	0	0	1		
G1	H0	H1	H2				
0	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
1	0	1	0			1	0
L2	M0	M1	M2	L2	M0	M1	M2
1	0	1	1	1	1	0	1
M3	N0	N1	N2	M3	N0	N1	N2
0	1	1	1	1	0	0	1
N3	P0	P1	P2	N3			
1	0	0	0	1			
Q0	Q1	Q2	Q3				
0	1	0	0				
R0	R1	R2	S0				
0	1	0	0				
T0	T1	JX	PX				
0	0	0	0				

CONDITIONS

H=STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
0 11111	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1	−2	+1	EARLY C COND
0		0	0	1	0
	DESTINATION H=J=0			
		0	1	0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
1	1	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I=O	YCI	YCD	ASCII
0	0	0	0	1	1

STATS=		YA	YB	YD	YE
	0	1011	1001	000	1 10

ALU CONT.		SKEW SELECT		ALU BIN OUT
1 1111	1	1 1111	1111	1111 1111

LSAR REGISTER		ROBAR
0 0000 0001	1	0 0000 1110 0001
H REGISTER		ROAR
1 0011 1001	0	0 0000 1111 1111
J REGISTER		ROSCAR
0 0000 0010	X	X XXXX XXXX XXXX

R REGISTER

1	000	1	0101 0101	1	0101 0101

A REGISTER

1	000	0	0000 0001	1	0110 0101

S REGISTER

P	XXX	P	XXXX XXXX	P	XXXX XXXX

B REGISTER

		1	0101 0101	1	0101 0101

C REGISTER

0	001	1	0000 0000	1	1111 1111

D REGISTER

		P	XXXX XXXX	P	XXXX XXXX

EX REG		P REGISTER		Q REGISTER	
1	000	1	0000 0000	1	1111 1111

CHECKS		IF REGISTER	
	1	0000 0000	1	0000 0000

INTERFACE CONTROLS

				XXXX XXXX			

CHANNEL CONTROLS

XXX				0000 0000			

CHANNEL DISPLAY

T0				T1			
		P	XXXX XXXX	P	XXXX XXXX

W0				W1			
		X	XXXX XXXX	X	XXXX XXXX

W2							
		X	XXXX XXXX	P	XXXX XXXX

W3				W4			
		X	XXXX XXXX	X	XXXX XXXX

SP	DATA	KEY
1	0000	0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

THE EDIT FUNCTION IS CHECKED TO SEE THAT OFF IS SELECTED WHEN AN INVALID PATTERN IS TESTED ON THE Q BUS.
VALID PATTERNS ARE 0010. 00XY AND XY ARE USED AS THE BITS 11 AND 12 OF THE NEXT MICROINSTRUCTION ADDRESS. IF THE PATTERN IS NOT VALID. BITS 11 AND 12 SHOULD BE FORCED TO ZERO FOR THE NEXT MICROINSTRUCTION ADDRESS.
IF ANY ADDRESS OTHER THAN OFF. MICROINSTRUCTION 019. IS SELECTED. SUSPECT THE *EDIT CIRCUITRY AND THE CB FIELD DECODING.

FUNCTION OF BOX

THE SETTING OF Y3 BY THE OR FUNCTION IS CHECKED LATER IN MICROINSTRUCTION 021.

```
    XX ——  0E1
E YAQ0001
A Z?C1→C1
L J→L   L+1→J
D B→B
C CPU    EDIT
R          1
E9—    ** —E1
```

RUN 17 JAN 66

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	0	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	1	1	0	0
C0	C1	C2	C3				
0	0	0	0				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	0	0
E2	E3	F0	G0	E2	E3		
0	0	1	1	0	0		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			1	0
L2	M0	M1	M2	L2	M0	M1	M2
0	0	1	1	1	0	1	1
M3	N0	N1	N2	M3	N0	N1	N2
1	0	0	0	0	1	1	1
N3	P0	P1	P2	N3			
0	0	0	0	1			
Q0	Q1	Q2	Q3				
0	0	1	0				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
1	0	0	0	1
	DESTINATION H-J-D			
	0	0	1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
1	0	1

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	1	1

STATS-		YA	YB	YD	YE
	0	1011	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 0000 0	1 0000 0000	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 1111 1111
H REGISTER	ROAR
1 0011 1001	1 0 0000 1110 1101
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

	R REGISTER			
1	000	0	0000 0001	1 0110 0101

	A REGISTER			
1	000	0	0000 0001	1 0110 0101

	S REGISTER			
P	XXX	P	XXXX XXXX	P XXXX XXXX

	B REGISTER			
		1	0000 0000	1 0110 0101

	C REGISTER			
0	001	1	0000 0000	1 1111 1111

	D REGISTER		
	P	XXXX XXXX	P XXXX XXXX

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0000 0000

	CHECKS	IF REGISTER
	1 0000 0000	1 0000 0000

	INTERFACE CONTROLS	
	XXXX XXXX	XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

	T0		T1
P	XXXX XXXX	P	XXXX XXXX
	W0		W1
X	XXXX XXXX	X	XXXX XXXX
	W2		
X	XXXX XXXX	P	XXXX XXXX
	W3		W4
X	XXXX XXXX	X	XXXX XXXX

SP	-DATA	-KEY
1	0000	0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 INVALID DECIMAL IN Q REGISTER (IDQ) IS CHECKED OFF.
IF A BRANCH TO A STOP IN 0EF OCCURS. CHECK THE Q REGISTER VALUE DURING THIS CYCLE.
IF THIS IS CORRECT, SUSPECT THE IDQ CIRCUITRY OR THE CB FIELD DECODING.
IF IT IS WRONG, SUSPECT THE C0 REGISTER OR THE Q REGISTER.
THE RELEVANT C0 REGISTER SETTINGS OCCURRED IN MICROINSTRUCTION 011 AND 017.

2 DIRECT CARRY IS CHECKED ON.
IF A BRANCH TO A STOP IN 0EC OCCURS. CHECK THE YCD STATUS. IF THIS IS CORRECT, SUSPECT THE CC FIELD DECODING. IF WRONG INVESTIGATE THE ALU OPERATION IN MICROINSTRUCTION 017.

3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 04C, MICROINSTRUCTION 021, INVESTIGATE THE VALUE OF THE A1 REGISTER.
IF THIS IS CORRECT SUSPECT THE CURRENT 18 BIT DATA TRANSFER.
IF IT IS WRONG SUSPECT THE ALU OPERATION IN MICROINSTRUCTION 015.
DO SHOULD BE CORRECT. THE VALUE OF THE TOP FOUR BITS WAS USED TO GENERATE 0DB, MICROINSTRUCTION 017.

```
    11 ---- OFF
E 0000,OR       |
A Z?C0->B0      |
|               |
D A->B          |
S  WRITE        |
R  IDQ      YCD |
J2 --   **----JB
```

FUNCTION OF BOX

THE B0 REGISTER IS SET UP FOR THE NEXT FUNCTION BRANCH ADDRESS.
MAIN STORAGE LOCATION 165(HEX) IS REWRITTEN.

SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
1	1	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
0	0	1	0	1	1	1	1
C0	C1	C2	C3				
0	1	1	0				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	0	0
E2	E3	F0	G0	E2	E3		
0	0	0	1	0	0		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	1	0				
J2	K0	L0	L1			L0	L1
1	0	1	1			0	0
L2	M0	M1	M2	L2	M0	M1	M2
1	1	1	0	0	0	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	1	0	0	1	0	0	0
N3	P0	P1	P2	N3			
1	0	1	0	0			
Q0	Q1	Q2	Q3				
0	1	0	1				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
0	0	0	0				

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
1	0	0	0	1
	DESTINATION H-J-Q			
	0	0	1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	0	1

STATS-		YA	YB	YD	YE
	0	1011	1001	000	1 10

ALU CONT.		SKEW SELECT		ALU BIN OUT	
1	1111 0	1	0110	0101	

LSAR REGISTER		ROBAR	
1	0000 0000	1	0 0000 1110 1101
H REGISTER		ROAR	
1	0011 1001	0	0 0000 0100 1100
J REGISTER		ROSCAR	
0	0000 0010	X	X XXXX XXXX XXXX

		R REGISTER			
1	000	1	0000 0000	1	0000 0000
		A REGISTER			
1	000	0	0000 0001	1	0110 0101
		S REGISTER			
P	XXX	P	XXXX XXXX	P	XXXX XXXX
		B REGISTER			
		1	0000 0000	1	0110 0101
		C REGISTER			
0	001	1	0000 0000	1	1111 1111
		D REGISTER			
		P	XXXX XXXX	P	XXXX XXXX

EX REG		P REGISTER		Q REGISTER	
1	000	1	0000 0000	1	0110 0101

	CHECKS	IF REGISTER
1	0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

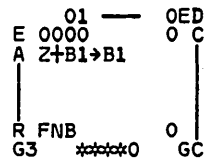
	T0		T1
P	XXXX XXXX	P	XXXX XXXX
	W0		W1
X	XXXX XXXX	X	XXXX XXXX
	W2		
X	XXXX XXXX	P	XXXX XXXX
	W3		W4
X	XXXX XXXX	X	XXXX XXXX

SP	-DATA	-KEY
1	0000	0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE B1 REGISTER BITS 0-3. B1 IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. B1 IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES	CONTROL LATCHES
A0 A1 A2 A3 0 0 1 1	
B0 B1 B2 B3 1 1 1 1	B0 B1 B2 B3 0 0 1 0
C0 C1 C2 C3 0 0 0 1	
D0 D1 E0 E1 0 0 0 0	D0 D1 E0 E1 0 0 0 0
E2 E3 F0 G0 0 0 0 1	E2 E3 0 0
G1 H0 H1 H2 1 0 0 0	
H3 H4 J0 J1 0 0 0 0	
J2 K0 L0 L1 0 0 0 0	L0 L1 1 1
L2 M0 M1 M2 0 1 1 1	L2 M0 M1 M2 1 1 1 0
M3 N0 N1 N2 0 0 0 0	M3 N0 N1 N2 0 1 0 0
N3 P0 P1 P2 0 0 0 0	N3 1
Q0 Q1 Q2 Q3 0 1 1 0	
R0 R1 R2 S0 0 0 0 0	
T0 T1 JX PX 1 0 0 0	

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	0 001	1 1111

EARLY B COND	INCREMENT CONTROL -1	-2	+1	EARLY C COND
1	0	0	0	1

DESTINATION H-J-O: 0 0 1

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	1	1

STATS-		YA	YB		YD	YE
	1	0000	0000		000	1 10

ALU CONT•	SKEW SELECT	ALU BIN OUT
1 1111 0	1 1111 1111	0000 0000

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0100 1100
H REGISTER	ROAR
1 0011 1001	0 0 0000 0111 1111
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

R REGISTER: 1 000 1 0011 1001 0 0000 0010

A REGISTER: 1 000 0 0000 0001 1 0110 0101

S REGISTER: P XXX P XXXX XXXX P XXXX XXXX

B REGISTER: 1 0000 0000 1 0110 0101

C REGISTER: 0 001 1 0000 0000 1 1111 1111

D REGISTER: 1 0011 1001 0 0000 0010

EX REG	P REGISTER	Q REGISTER
1 000	0 0000 0001	1 1111 1111

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS: XXXX XXXX XXXX XXXX

CHANNEL CONTROLS: XXX 0000 0000 0000 0000

CHANNEL DISPLAY

T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY: 1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

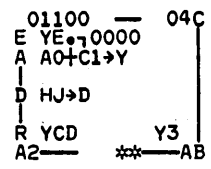
1 THE DIRECT CARRY (YCD) CONDITION IS CHECKED ON•
IF A BRANCH TO A STOP OCCURS AT 07D• CHECK THE
YCD SETTING•
IF THIS IS CORRECT• SUSPECT THE CB FIELD DECODING•
IF IT IS WRONG CHECK THE P AND Q REGISTER INPUT
VALUES TO THE ALU IN THIS CYCLE•
IF THESE ARE CORRECT• SUSPECT THE CURRENT ALU OPERATION•
IF P REGISTER IS WRONG• USE THE FAULT ANALYSIS
DIAGRAM A ON THE NEXT PAGE•
IF Q REGISTER IS WRONG• USE THE FAULT ANALYSIS
DIAGRAM B ON THE FOLLOWING PAGE•

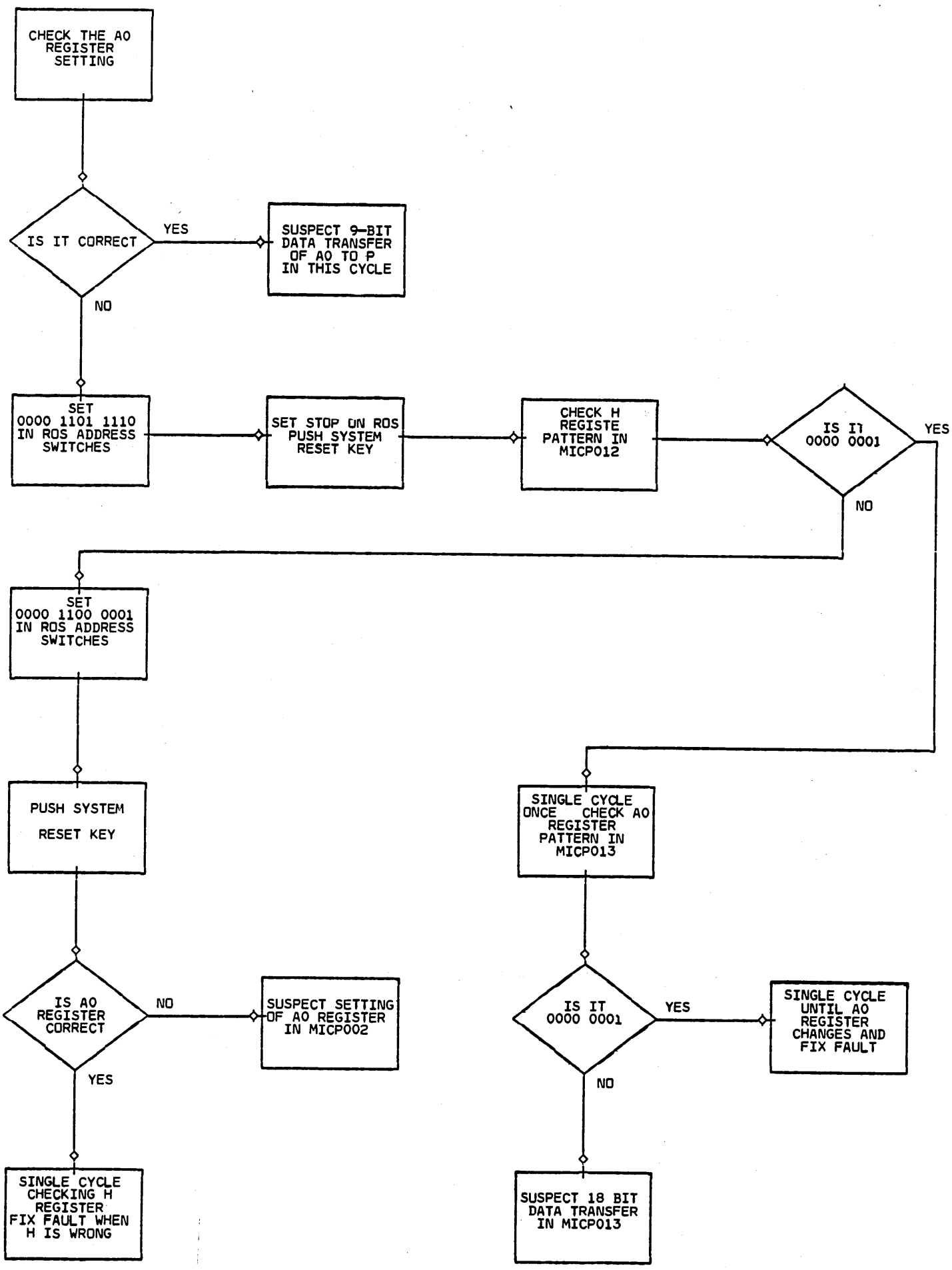
2 THE Y3 STAT IS CHECKED ON•
IF A BRANCH TO A STOP OCCURS AT 07E• SET
(0000 0100 1100) IN ROS ADDRESS SWITCHES• SET
STOP ON ROS• PUSH SYSTEM RESET AND CHECK THE Y3
STAT SETTING•
IF THIS IS CORRECT• SUSPECT THE CC FIELD DECODING
OR THE NEW Y3 SETTING PRODUCED IN MICROINSTRUCTION 021
OVERRIDING THE OLD VALUE•
IF IT IS WRONG• SUSPECT THE SETTING OF Y3 IN
MICROINSTRUCTION 018•

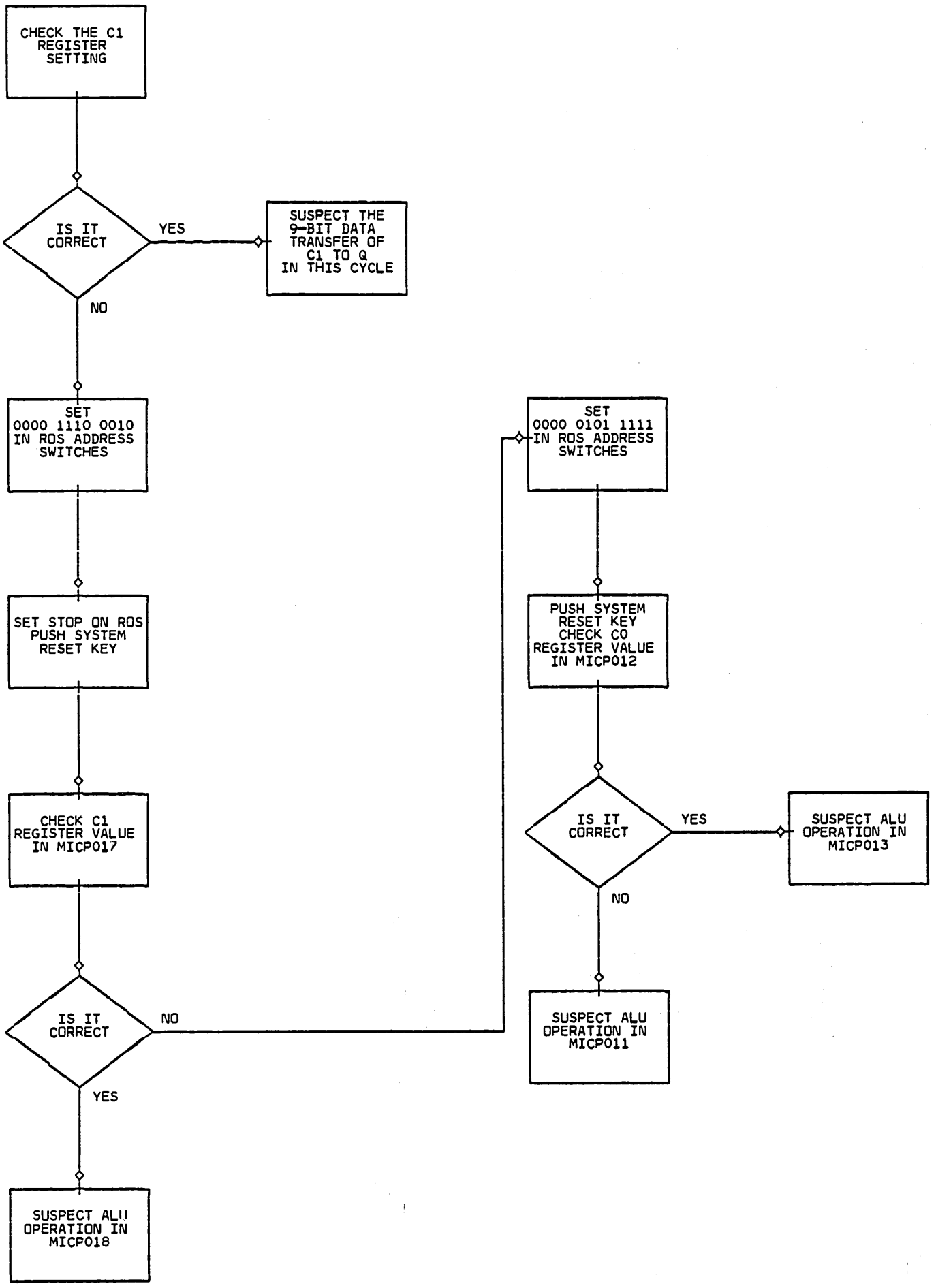
3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER
THAN 0C7 (MICROINSTRUCTION 023) CHECK THE H REGISTER
VALUE•
IF THIS IS CORRECT• SUSPECT THE 18 BIT DATA TRANSFER
IN MICROINSTRUCTION 021•
IF IT IS WRONG• SUSPECT THE GENERATION OF THE
H REGISTER BY (HB) IN MICROINSTRUCTION 015•

FUNCTION OF BOX

THE Y STATS ARE ALL RESET• AND SEVERAL OF THESE ARE
CHECKED LATER IN THE OFE STATE TO VERIFY THAT THE
ALU OUTPUT DOES MODIFY THE STATS•
DO REGISTER IS CHANGED FOR THE NEXT FUNCTION
BRANCH ADDRESS•




CHECK THE AO REGISTER SETTING
IS IT CORRECT
YES
SUSPECT 9-BIT DATA TRANSFER OF AO TO P IN THIS CYCLE
NO
SET 0000 1101 1110 IN ROS ADDRESS SWITCHES
SET STOP ON ROS PUSH SYSTEM RESET KEY
CHECK H REGISTE PATTERN IN MICP012
IS IT 0000 0001
YES
NO
SET 0000 1100 0001 IN ROS ADDRESS SWITCHES
PUSH SYSTEM RESET KEY
SINGLE CYCLE ONCE CHECK AO REGISTER PATTERN IN MICP013
IS AO REGISTER CORRECT
NO
SUSPECT SETTING OF AO REGISTER IN MICP002
YES
IS IT 0000 0001
YES
SINGLE CYCLE UNTIL AO REGISTER CHANGES AND FIX FAULT
NO
SINGLE CYCLE CHECKING H REGISTER FIX FAULT WHEN H IS WRONG
SUSPECT 18 BIT DATA TRANSFER IN MICP013


CHECK THE C1 REGISTER SETTING
IS IT CORRECT
YES
SUSPECT THE 9-BIT DATA TRANSFER OF C1 TO Q IN THIS CYCLE
NO
SET 0000 1110 0010 IN ROS ADDRESS SWITCHES
SET STOP ON ROS PUSH SYSTEM RESET KEY
CHECK C1 REGISTER VALUE IN MICP017
IS IT CORRECT
NO
YES
SUSPECT ALU OPERATION IN MICP018
SET 0000 0101 1111 IN ROS ADDRESS SWITCHES
PUSH SYSTEM RESET KEY CHECK CO REGISTER VALUE IN MICP012
IS IT CORRECT
YES
SUSPECT ALU OPERATION IN MICP013
NO
SUSPECT ALU OPERATION IN MICP011

SENSE LATCHES

A0	A1	A2	A3
1	0	1	1
B0	B1	B2	B3
0	1	0	0
C0	C1	C2	C3
1	1	0	1
D0	D1	E0	E1
0	0	1	0
E2	E3	F0	G0
0	1	0	0
G1	H0	H1	H2
0	0	0	0
H3	H4	J0	J1
1	0	1	1
J2	K0	L0	L1
0	0	0	0
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	0	1	0
N3	P0	P1	P2
0	1	1	0
Q0	Q1	Q2	Q3
0	0	0	0
R0	R1	R2	S0
0	0	0	0
T0	T1	JX	PX
0	0	0	0

CONTROL LATCHES

B0	B1	B2	B3
1	1	1	1
D0	D1	E0	E1
0	0	0	0
E2	E3		
0	0		
		L0	L1
		0	0
L2	M0	M1	M2
0	1	1	1
M3	N0	N1	N2
0	0	0	0
N3			
0			

CONDITIONS

H-STOP	LOG DSAB	DP1	S TO SAB SC1	SC2
1	0 0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL -1 -2 +1	EARLY C COND
0	0 0 0	0
	DESTINATION H-J-D 0 0 1	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	0	1

STATS-		YA	YB	YD	YE
	1	0000	0000	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0011 1001	0011 1001

LSAR REGISTER	ROBAR
1 0000 0000	0 0 0000 0111 1111
H REGISTER	ROAR
1 0011 1001	0 0 0000 1100 0111
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

	R REGISTER	
1 000 1	0000 0000	1 0000 0000
	A REGISTER	
1 000 0	0000 0001	1 0110 0101
	S REGISTER	
P XXX P	XXXX XXXX	P XXXX XXXX
	B REGISTER	
1	0000 0000	1 0110 0101
	C REGISTER	
0 001 1	0000 0000	1 1111 1111
	D REGISTER	
1	0011 1001	0 0000 0010

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 0011 1001

	CHECKS	IF REGISTER
1	0000 0000	1 0000 0000

	INTERFACE CONTROLS	
	XXXX XXXX	XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

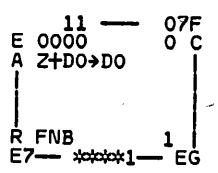
	T0	T1
P	XXXX XXXX	P XXXX XXXX
	W0	W1
X	XXXX XXXX	X XXXX XXXX
	W2	
X	XXXX XXXX	P XXXX XXXX
	W3	W4
X	XXXX XXXX	X XXXX XXXX

SP	-DATA	-KEY
1	0000	0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE D0 REGISTER BITS 0-3. D0 IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. D0 IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES			
A0	A1	A2	A3
0	0	0	1
B0	B1	B2	B3
1	1	1	1
C0	C1	C2	C3
0	0	0	1
D0	D1	E0	E1
0	0	0	0
E2	E3	F0	G0
0	0	1	1
G1	H0	H1	H2
1	0	0	0
H3	H4	J0	J1
0	0	0	0
J2	K0	L0	L1
0	0	0	0
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	0	0	0
N3	P0	P1	P2
0	0	0	0
Q0	Q1	Q2	Q3
0	0	0	1
R0	R1	R2	S0
0	0	0	0
T0	T1	JX	PX
1	0	0	0

CONTROL LATCHES			
B0	B1	B2	B3
0	1	0	0
D0	D1	E0	E1
0	0	1	0
E2	E3		
0	1		
		L0	L1
		0	0
L2	M0	M1	M2
0	0	1	1
M3	N0	N1	N2
0	0	1	0
N3			
0			

CONDITIONS

H-STOP	LOG	DSAB	DP1
1	0	0	0

S TO SAB

SC1	SC2
X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL	-1	-2	+1	EARLY C COND
0		0	0	0	0
	DESTINATION H-J-O	1	0	0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	0	1

STATS-		YA	YB	YD	YE
	1	0000	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 0000 0	1 0000 0000	1001 0000

LSAR REGISTER	ROBAR
1 0011 1001	0 0 0000 1100 0111
H REGISTER	ROAR
1 0011 1001	1 0 0000 1110 1110
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

R REGISTER					
1	000	1	0000 0000	1	0000 0000

A REGISTER					
1	000	0	0000 0001	1	0110 0101

S REGISTER					
P	XXX	P	XXXX XXXX	P	XXXX XXXX

B REGISTER					
		1	1001 0000	1	0110 0101

C REGISTER					
0	001	1	0000 0000	1	1111 1111

D REGISTER			
	1	0011 1001	0 0000 0010

EX REG	P REGISTER	Q REGISTER
1 000	1 1001 0000	1 0000 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

	CHANNEL CONTROLS	
XXX	0000 0000	0000 0000

CHANNEL DISPLAY

T0		T1	
P	XXXX XXXX	P	XXXX XXXX
W0		W1	
X	XXXX XXXX	X	XXXX XXXX
W2			
X	XXXX XXXX	P	XXXX XXXX
W3		W4	
X	XXXX XXXX	X	XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 ALU≠0 IS CHECKED ON.
IF A BRANCH TO A STOP AT 0EC OCCURS. CHECK THE B0 REGISTER SETTING.
IF THIS IS CORRECT. SUSPECT THE ALU≠0 CIRCUITRY AND THE CB FIELD DECODING.
IF IT IS WRONG. SUSPECT THE CURRENT ALU OPERATION.

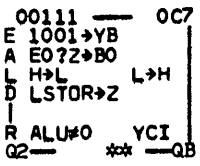
2 YCI IS CHECKED OFF.
IF A BRANCH TO A STOP AT 0EF OCCURS. CHECK THE YCI SETTING.
IF THIS IS CORRECT. SUSPECT THE CC FIELD DECODING.
IF IT IS WRONG. SET(0000 1101 1110) IN ROS ADDRESS SWITCHES. SET STOP ON ROS AND PUSH SYSTEM RESET KEY.
SINGLE CYCLE CHECKING YCI UNTIL AN ERROR OCCURS AND FIX FAULT.

3 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 053. MICROINSTRUCTION 025. SUSPECT THE CURRENT ALU OPERATION. CHECKING ESPECIALLY THAT THE CORRECT INDIRECT FUNCTION IS BEING PERFORMED.

FUNCTION OF BOX

LOCAL STORAGE LOCATION 39(HEX) IS READ OUT IN PREPARATION FOR STORING THE MAIN STORAGE ADDRESS REGISTER (A) CONTENTS.

THE B0 REGISTER IS SET FOR THE NEXT FUNCTION BRANCH ADDRESS.



SENSE LATCHES	CONTROL LATCHES
A0 A1 A2 A3 1 1 1 1	
B0 B1 B2 B3 0 1 1 1	B0 B1 B2 B3 1 1 1 1
C0 C1 C2 C3 1 0 0 0	
D0 D1 E0 E1 0 0 1 0	D0 D1 E0 E1 0 0 0 0
E2 E3 F0 G0 0 1 1 1	E2 E3 0 0
G1 H0 H1 H2 1 0 0 0	
H3 H4 J0 J1 1 0 0 0	
J2 K0 L0 L1 1 0 0 0	L0 L1 0 0
L2 M0 M1 M2 1 1 1 1	L2 M0 M1 M2 0 0 1 1
M3 N0 N1 N2 0 0 0 0	M3 N0 N1 N2 0 0 0 0
N3 P0 P1 P2 1 1 1 0	N3 0
Q0 Q1 Q2 Q3 1 0 0 1	
R0 R1 R2 S0 0 0 0 1	
T0 T1 JX PX 0 0 0 0	

CONDITIONS

H-STOP	LOG	DSAB	DP1	S TO SAB SC1	S TO SAB SC2
1	0	0	0	X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1	−2	+1	EARLY C COND
1	0	0	0	0

DESTINATION H-J-O: 0 0 1

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I-O	YCI	YCD	ASCII
0	0	0	0	0	1

STATS-		YA	YB	YD	YE
	1	0000	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 1001 0000	1001 0000

LSAR REGISTER	ROBAR
1 0000 0000	1 0 0000 1110 1110
H REGISTER	ROAR
1 0011 1001	1 0 0000 0101 0011
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

R REGISTER
1 000 1 0000 0000 1 0000 0000

A REGISTER
1 000 0 0000 0001 1 0110 0101

S REGISTER
P XXX P XXXX XXXX P XXXX XXXX

B REGISTER
1 1001 0000 1 0110 0101

C REGISTER
0 001 1 0000 0000 1 1111 1111

D REGISTER
1 0011 1001 0 0000 0010

EX REG	P REGISTER	Q REGISTER
1 000	1 0000 0000	1 1001 0000

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS
XXXX XXXX XXXX XXXX

CHANNEL CONTROLS
XXX 0000 0000 0000 0000

CHANNEL DISPLAY

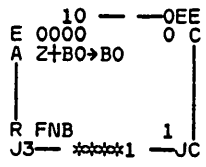
T0	T1
P XXXX XXXX	P XXXX XXXX
W0	W1
X XXXX XXXX	X XXXX XXXX
W2	
X XXXX XXXX	P XXXX XXXX
W3	W4
X XXXX XXXX	X XXXX XXXX

SP -DATA -KEY
1 0000 0000

DESCRIPTIVE NOTES

FUNCTION OF BOX

DIRECT CARRY IS RESET, AND A FUNCTION BRANCH IS EXECUTED BASED ON THE CURRENT STATUS OF THE BO REGISTER BITS 0-3. BO IS USED AS THE Q REGISTER INPUT, AND THE TOP FOUR BITS ARE USED TO COMPLETE THE FUNCTION BRANCH ADDRESS. NOTE THAT APART FROM THE RESET CARRY, ALL THE DATA FLOW IS PRESERVED IN THIS INSTRUCTION. BO IS CHANGED DURING THE MICROPROGRAM TO DEFINE THE DIFFERENT FUNCTION BRANCHES. IF THE WRONG FUNCTION BRANCH IS TAKEN, THE NOTES ON THE PREVIOUS MICROINSTRUCTION DEFINE THE DIAGNOSTIC PROCEDURE.



SENSE LATCHES				CONTROL LATCHES			
A0	A1	A2	A3				
0	0	1	1				
B0	B1	B2	B3	B0	B1	B2	B3
1	1	1	1	0	1	1	1
C0	C1	C2	C3				
0	0	0	1				
D0	D1	E0	E1	D0	D1	E0	E1
0	0	0	0	0	0	1	0
E2	E3	F0	G0	E2	E3		
0	0	0	1	0	1		
G1	H0	H1	H2				
1	0	0	0				
H3	H4	J0	J1				
0	0	0	0				
J2	K0	L0	L1			L0	L1
0	0	0	0			0	0
L2	M0	M1	M2	L2	M0	M1	M2
0	1	1	1	1	1	1	1
M3	N0	N1	N2	M3	N0	N1	N2
0	0	0	0	0	0	0	0
N3	P0	P1	P2	N3			
0	0	0	0	1			
Q0	Q1	Q2	Q3				
0	1	1	0				
R0	R1	R2	S0				
0	0	0	0				
T0	T1	JX	PX				
1	0	0	0				

CONDITIONS

H=STOP	LOG	DSAB	DP1
1	0	0	0

S TO SAB

SC1	SC2
X	X

MISCELLANEOUS

THESE LATCHES ARE NOT DISPLAYED

REG F	YC	ALU EX OP	SKEW
1 00000	0	1 000	1 1111

EARLY B COND	INCREMENT CONTROL −1 −2 +1	EARLY C COND
1	0 0 0	0
	DESTINATION H=J=0	
	1 0 0	

DUMP	UNDUMP	UNDUMP INH	CHAN MP IRPT
0	0	0	0

READ	SECOND MS CYCLE	WRITE
0	0	0

EXT MASK	HALT
0	0

CONDITIONS

PMA	IMA	I=O	YCI	YCD	ASCII
0	0	0	0	0	1

STATS=		YA	YB	YD	YE
	1	1001	1001	000	1 10

ALU CONT.	SKEW SELECT	ALU BIN OUT
1 1111 0	1 0000 1001	1001 1001

LSAR REGISTER	ROBAR
1 0011 1001	1 0 0000 0101 0011
H REGISTER	ROAR
1 0011 1001	0 0 0000 0111 1111
J REGISTER	ROSCAR
0 0000 0010	X X XXXX XXXX XXXX

R REGISTER

1	000	0	0000 0001	1	0110 0101

A REGISTER

1	000	0	0000 0001	1	0110 0101

S REGISTER

P	XXX	P	XXXX XXXX	P	XXXX XXXX

B REGISTER

	1	1001 0000	1	0110 0101

C REGISTER

0	001	1	0000 0000	1	1111 1111

D REGISTER

	1	1001 1001	0	0000 0010

EX REG	P REGISTER	Q REGISTER
1 000	1 1001 0000	1 0000 1001

CHECKS	IF REGISTER
1 0000 0000	1 0000 0000

INTERFACE CONTROLS

XXXX XXXX XXXX XXXX

CHANNEL CONTROLS

XXX 0000 0000 0000 0100

CHANNEL DISPLAY

TO		T1
P	XXXX XXXX	P XXXX XXXX
W0		W1
X	XXXX XXXX	1 0101 0101
W2		
1	0101 0101	P XXXX XXXX
W3		W4
1	0101 0101	X XXXX XXXX

SP	−DATA	−KEY
1	0000 0000	

DESCRIPTIVE NOTES

CHECKS TAKING PLACE

1 Y4 AND Y7 ARE CHECKED ON.
IF AN ADDRESS OTHER THAN 07F IS SELECTED AT MICROINSTRUCTION 026, CHECK THE YB STAT SETTINGS.
IF THESE ARE CORRECT, SUSPECT THE CB OR CC FIELD DECODING.
IF THEY ARE WRONG, SUSPECT THE YB=9 OPERATION IN MICROINSTRUCTION 023, AND THE Y4 AND Y7 CIRCUITRY.

2 IF A FUNCTION BRANCH OCCURS TO SOME ADDRESS OTHER THAN 0D3, MICROINSTRUCTION 027, SUSPECT THE ALU OPERATION IN THE CURRENT CYCLE.

FUNCTION OF BOX

THE D0 REGISTER IS SET FOR THE FUNCTION BRANCH AND THE PATTERN IS ALSO USED LATER TO SET UP THE H REGISTER FOR ADDRESSING LOCAL STORE.
THE MAIN STORAGE ADDRESS REGISTER (A) CONTENTS ARE SAVED IN LOCAL STORAGE ADDRESS 39(HEX).

THE YA STATS ARE SET UP FOR LATER OPERATIONS.

```
 10011 ——— 053
E 1001→YA      |
A E0+0E→D0     |
L H→L     L→H  |
D A→LSTOR      |
|              |
R Y4       Y7  |
E5—    ** —EE
```

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International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601